

CONFIDENTIAL

Mosaic Schematics Document

uFCBGA/uFCPGA Northwood

2001-09-19

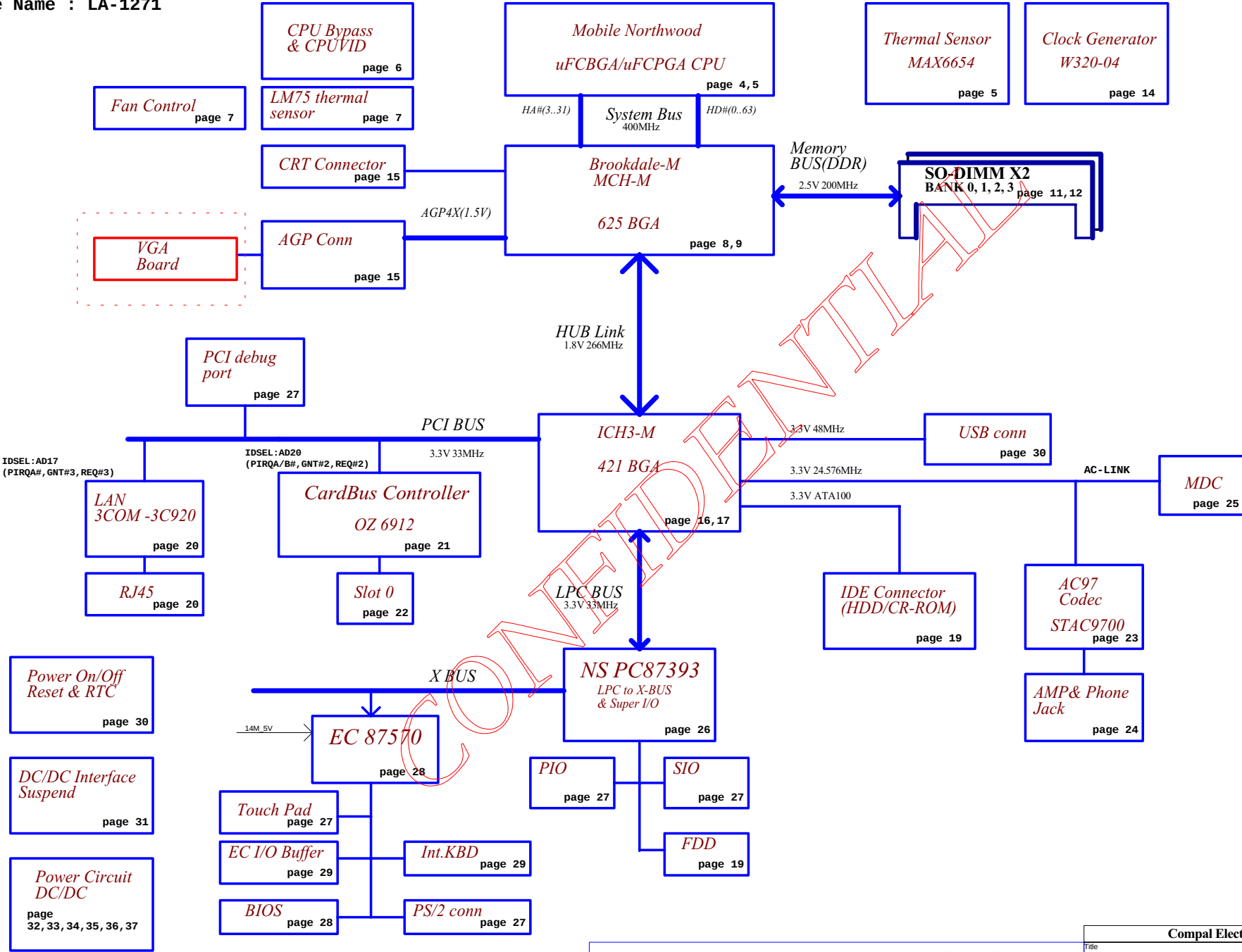
REV: 0.1

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Compal Electronics, Inc.		
Title		
Cover Sheet		
Size	Document Number	Rev
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Model Name :ADY13(Mosaic)

File Name : LA-1271



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Title		Block Diagram	
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Function	Model	Mosaic	Midas
FDD		YES	YES
PS/2		YES	YES
Serial port		NO	NO
Parallel port		YES	YES
RJ45		YES	YES
OZ6912/TPS2211		YES	YES
3Com Lan chipset(3C920)		YES S/W disable	YES

Note1: "@ " means all model depop

Note2: Removed serial port,because add 2nd Fan

Power Managment table

Signal			
State	+3VALW +5VALW +1.8VALW +12VALW	+3V +5V +2.5V	+3VS +5VS +1.8VS +1.5VS +1.2VP +CPU_CORE +1.25V
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

	CHIPS Rev R682845	CHIPS Rev FW82801CAM
SST-Build	A3(QC45)	B1(QC42)

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Title

Note & Revision

Size

Document Number

Rev

ADY13 LA-1271

0.1

Date:

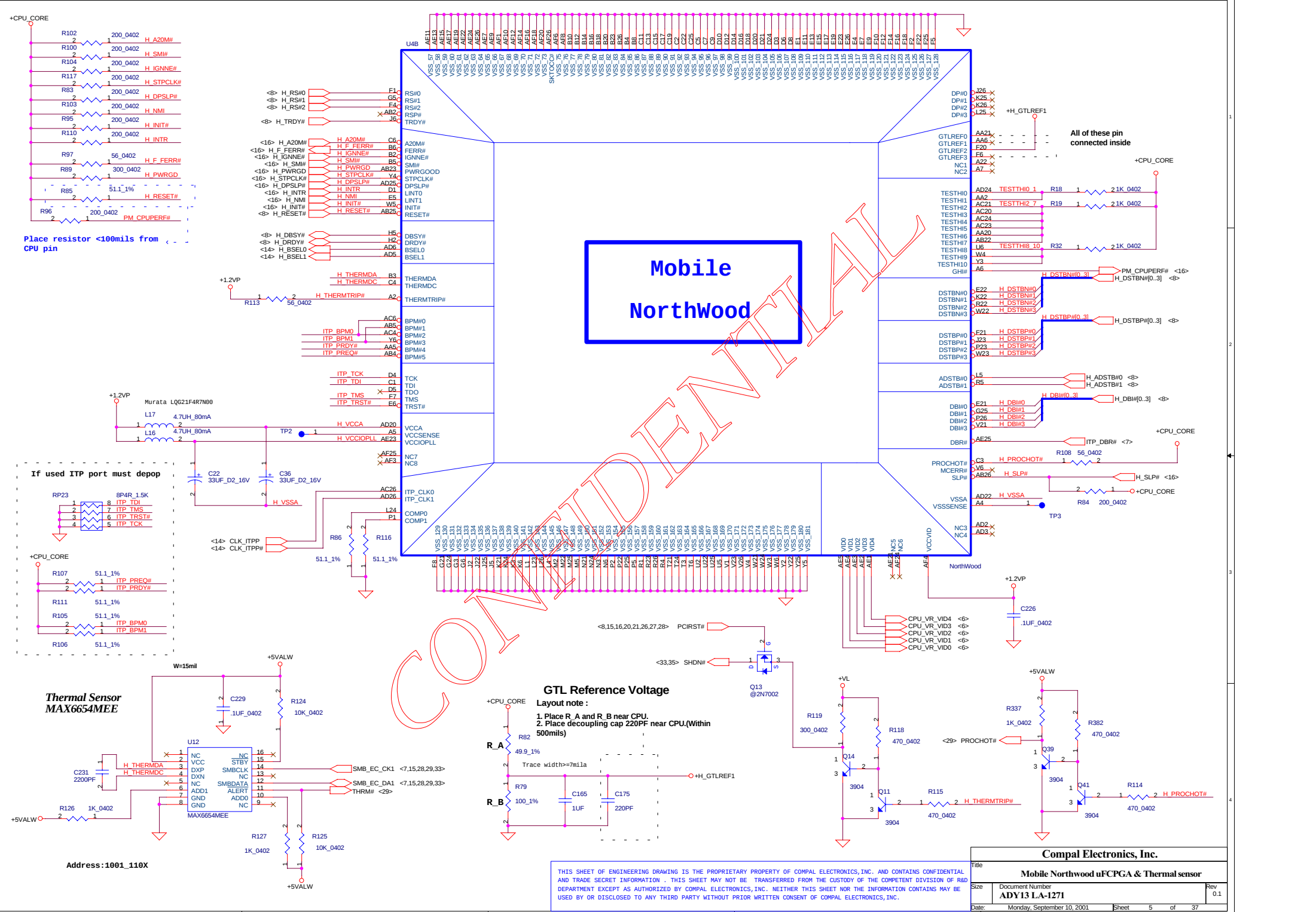
Wednesday, September 19, 2001

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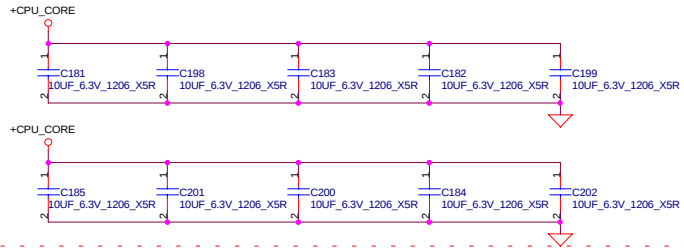
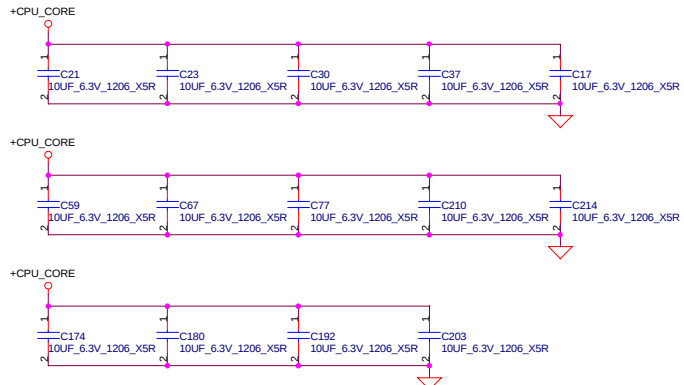
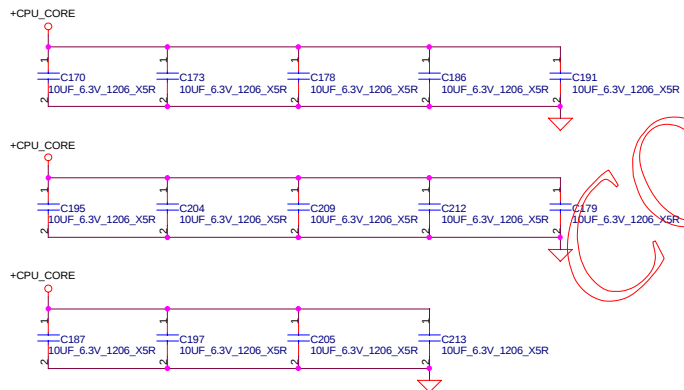
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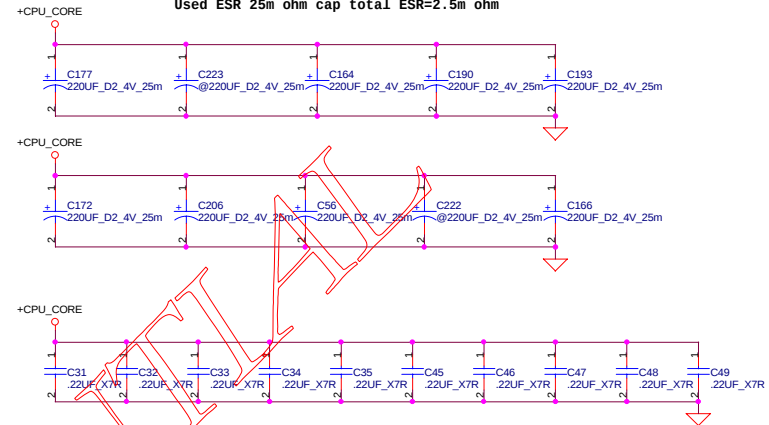
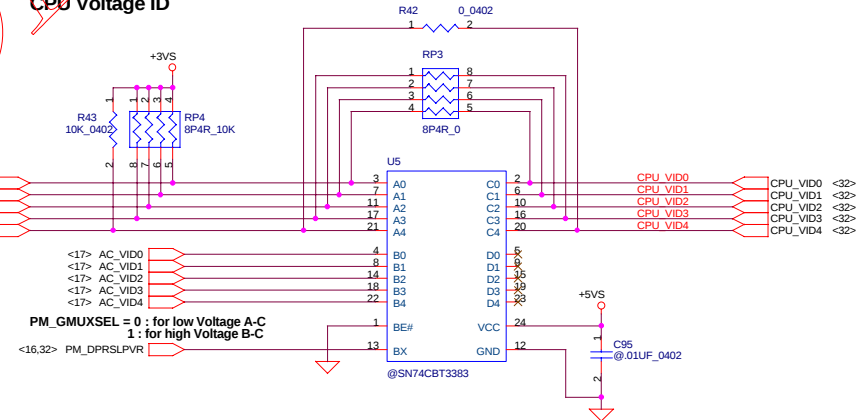
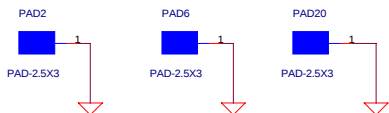


Layout note :

Place close to CPU. Use 2-3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2-3 vias per PAD.

Please place these cap in the socket cavity area**Please place these cap on the socket north side****Please place these cap on the socket south side****Layout note :**

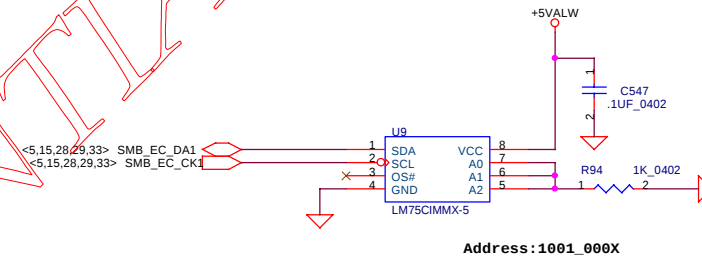
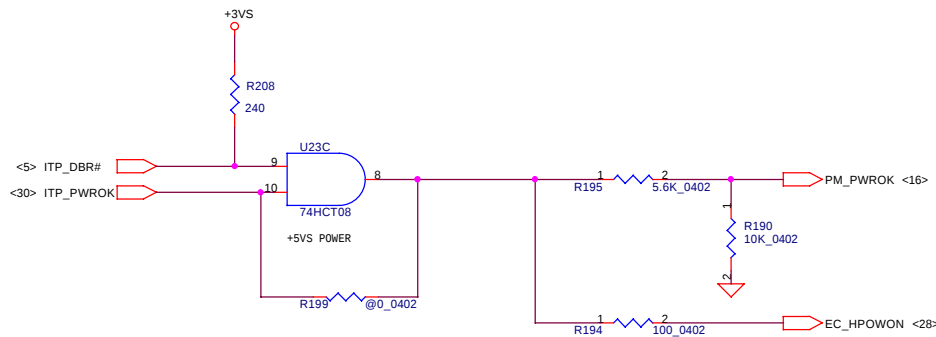
Place close to CPU power and
ground pin as possible
(<1inch)

Used ESR 25m ohm cap total ESR=2.5m ohm**CPU Voltage ID****EMI Clip PAD for CPU**

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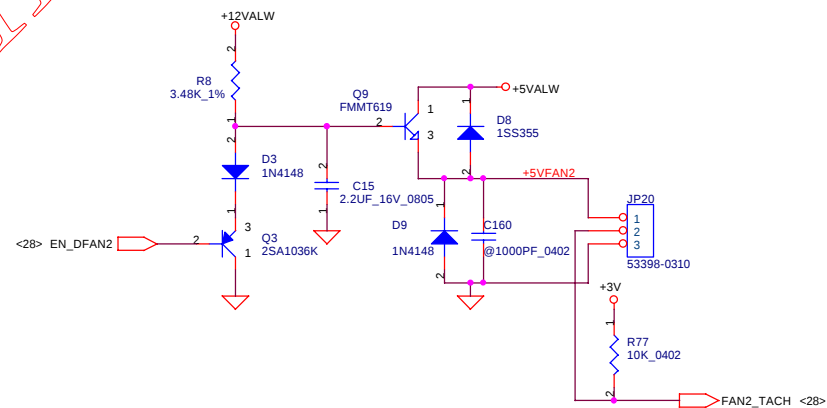
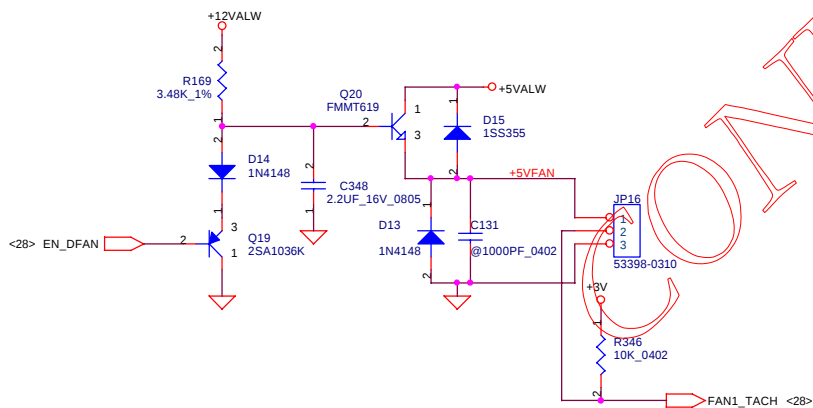
Compal Electronics, Inc.**CPU Bypass & CPU VID**

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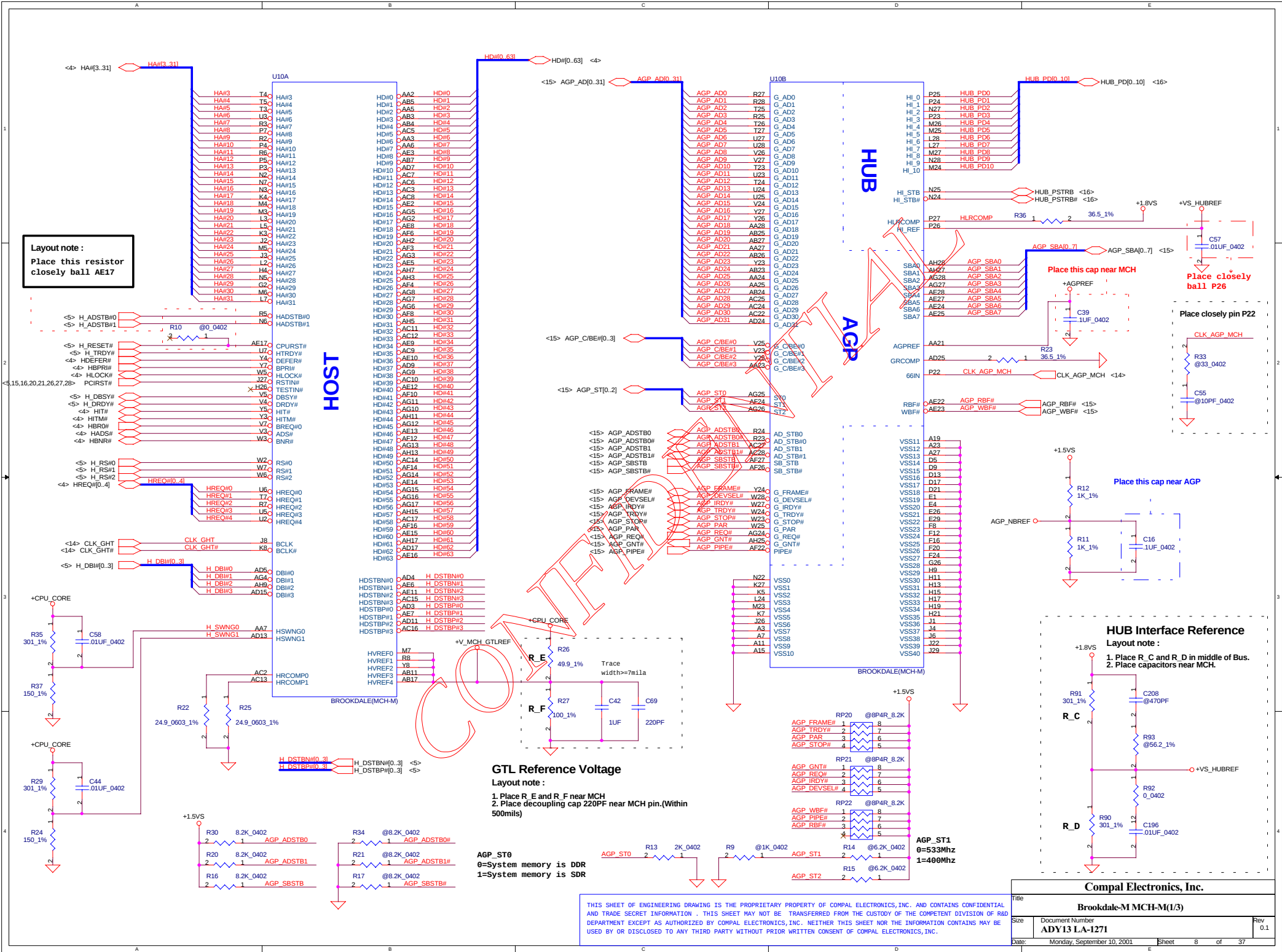
Fan1 Control circuit

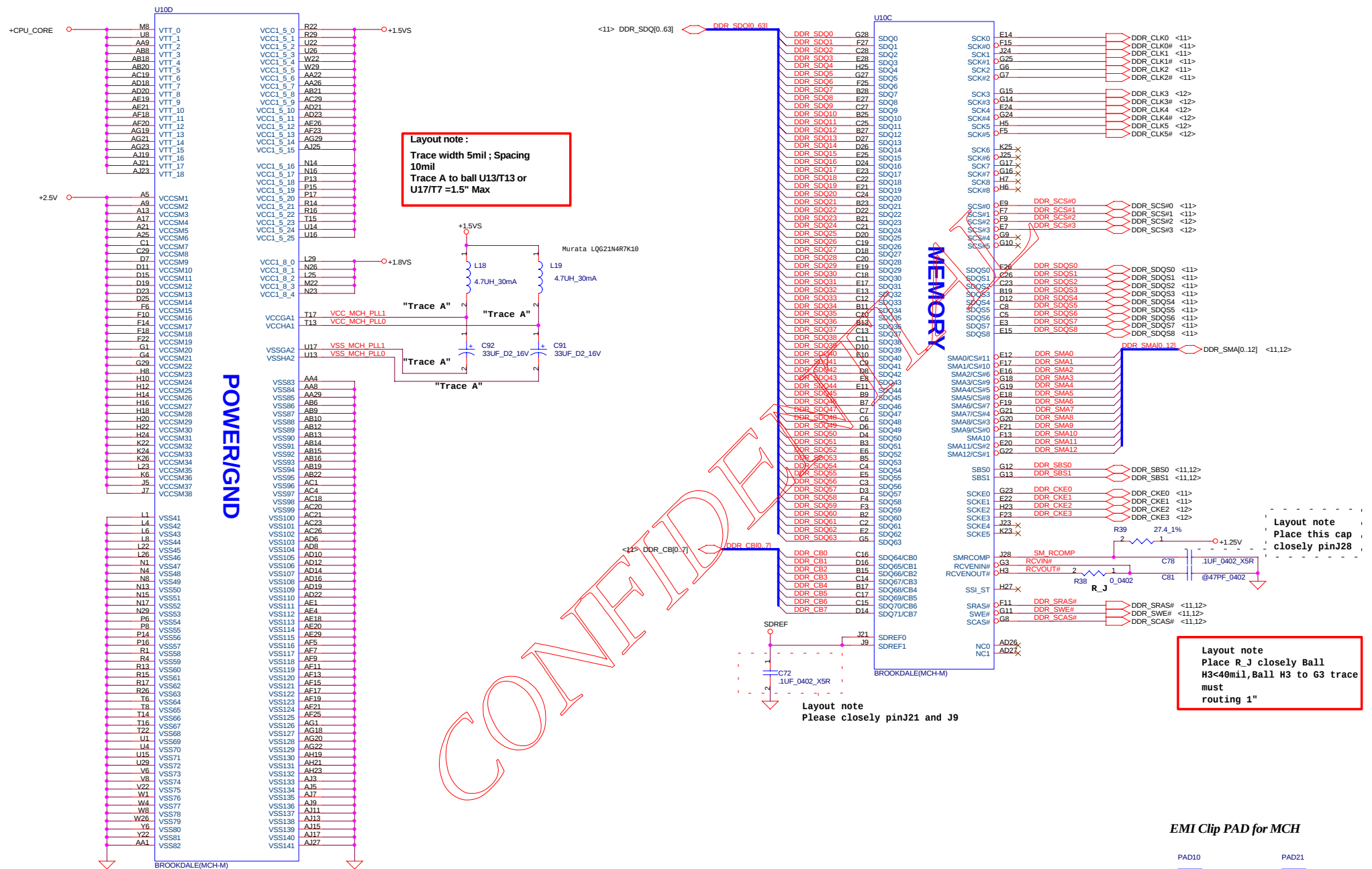
Fan2 Control circuit



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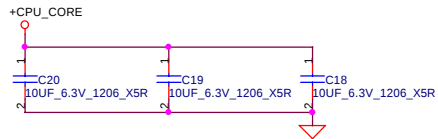
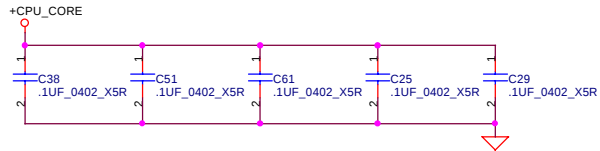
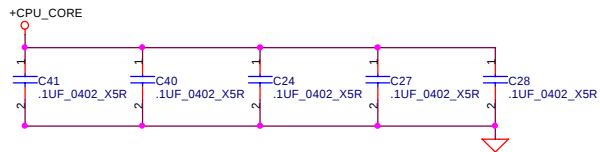
COMPAL Electronics, Inc			
Title	LM75 Thermal sensor & Fan control		
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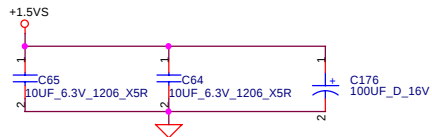
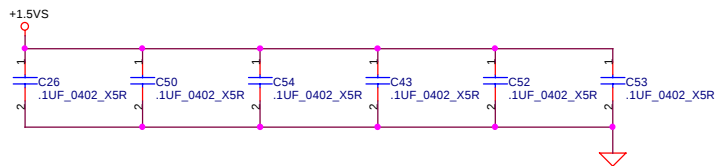


Layout note: Processor system bus

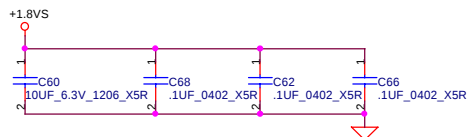
Distribute as close as possible
to MCH Processor Quadrant.(between VTTFB and VSS pin)

**Layout note: AGP/CORE**

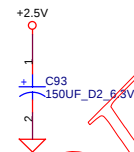
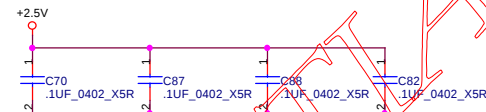
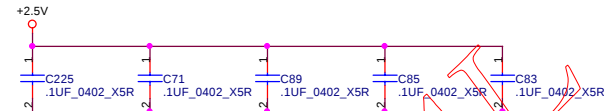
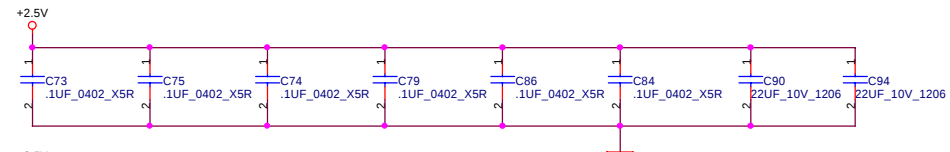
Distribute as close as possible
to MCH Processor Quadrant.(between VCCAGP/VCCCORE
and VSS pin)

**Layout note: Hub-Link**

Distribute as close as possible
to MCH Processor Quadrant.(between VCCHL and VSS pin)

**Layout note: DDR Memory interface**

Distribute as close as possible
to MCH Processor Quadrant.(between VCCSM and VSS pin)

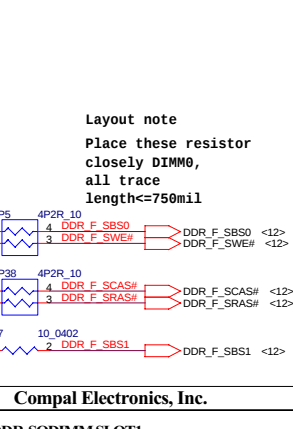
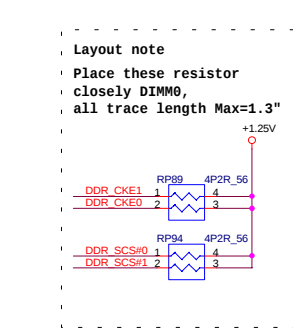
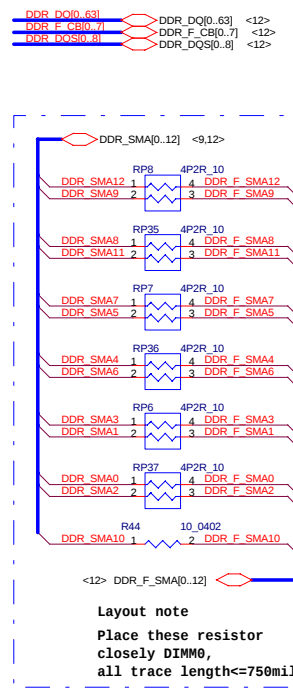
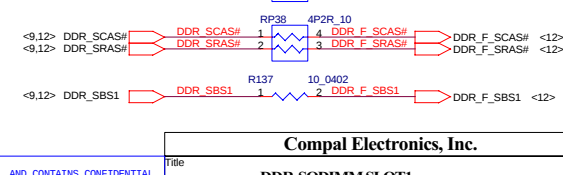
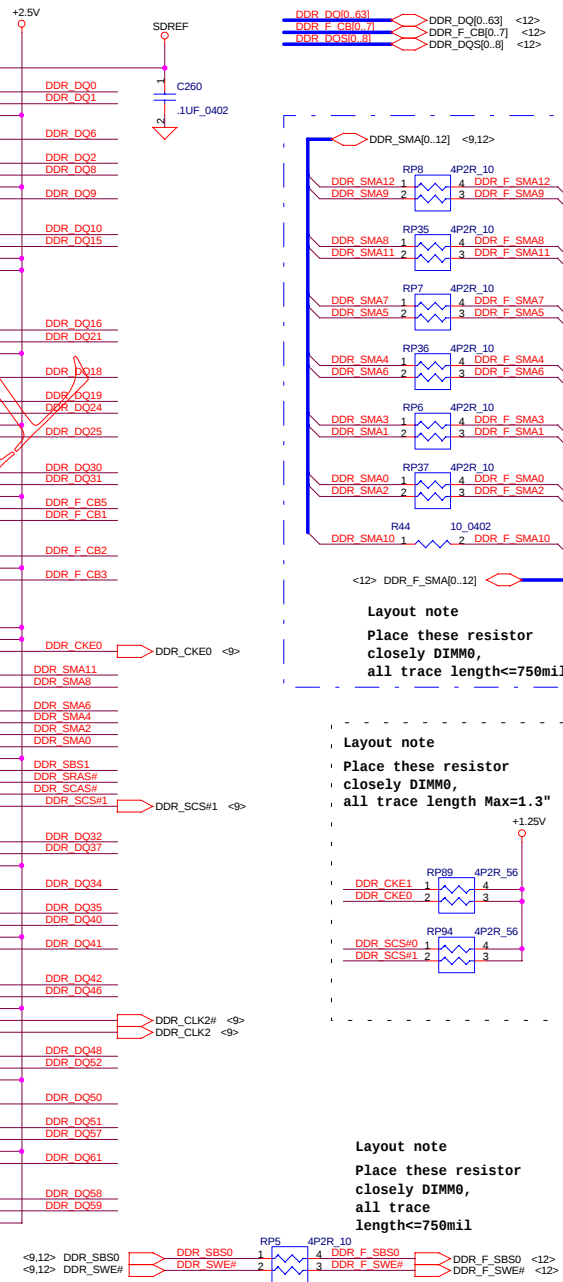
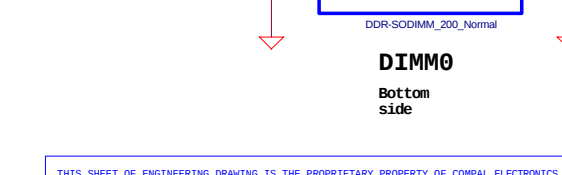
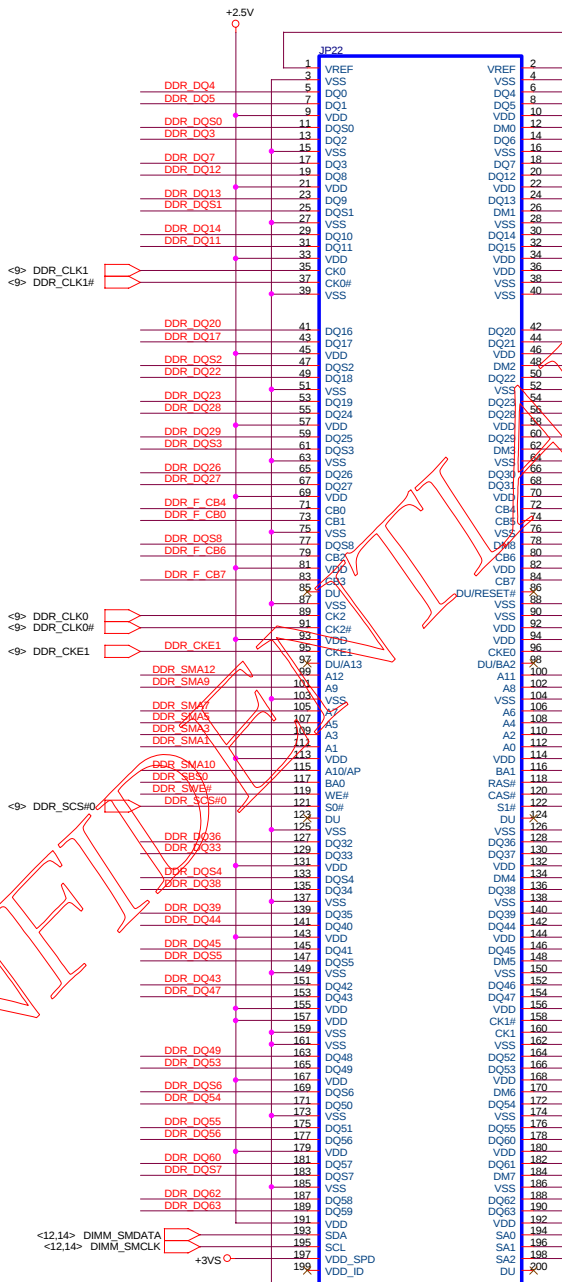
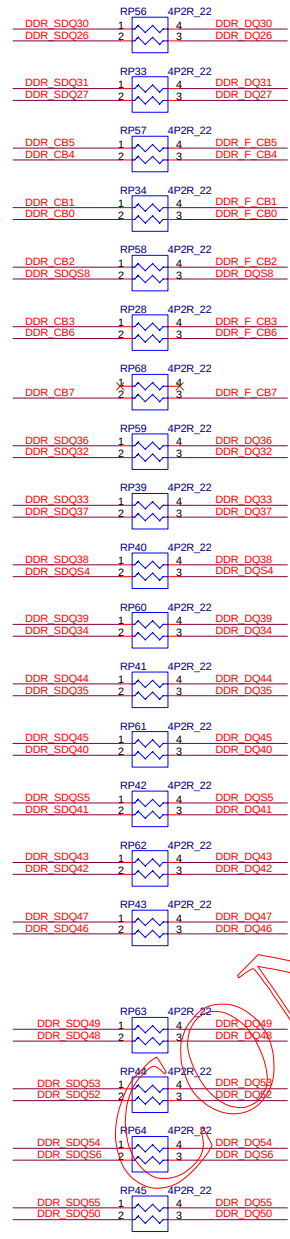
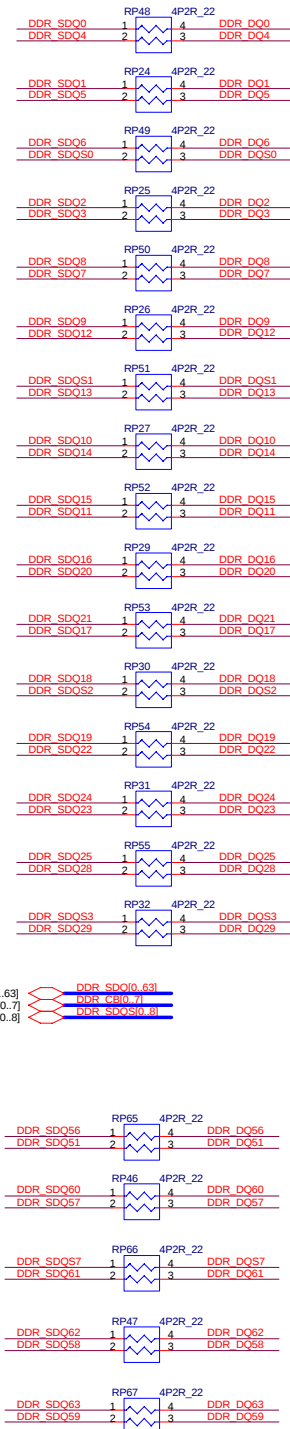


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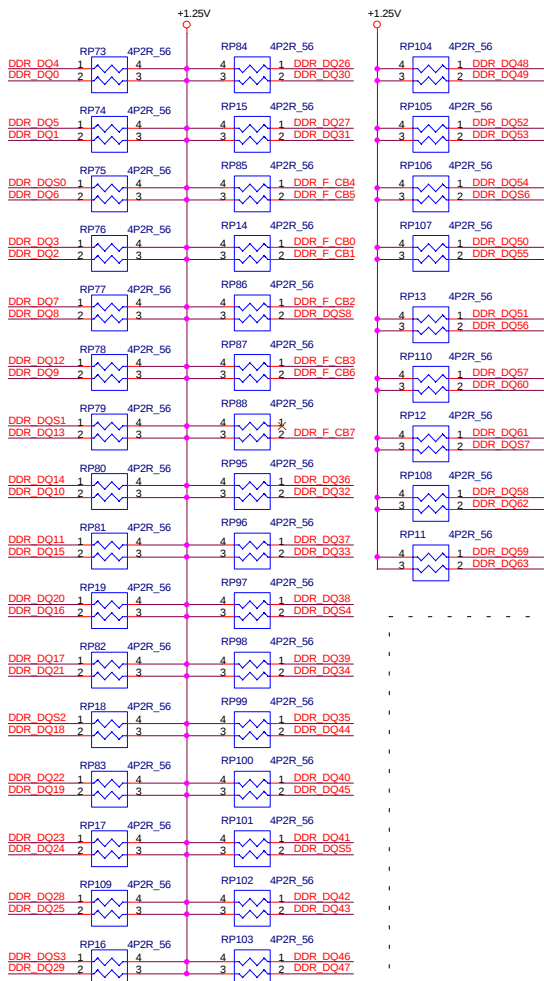
Title		MCH-M Decoupling	
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Layout note
Place these resistor
closely DIMM0,
all trace length<750mil



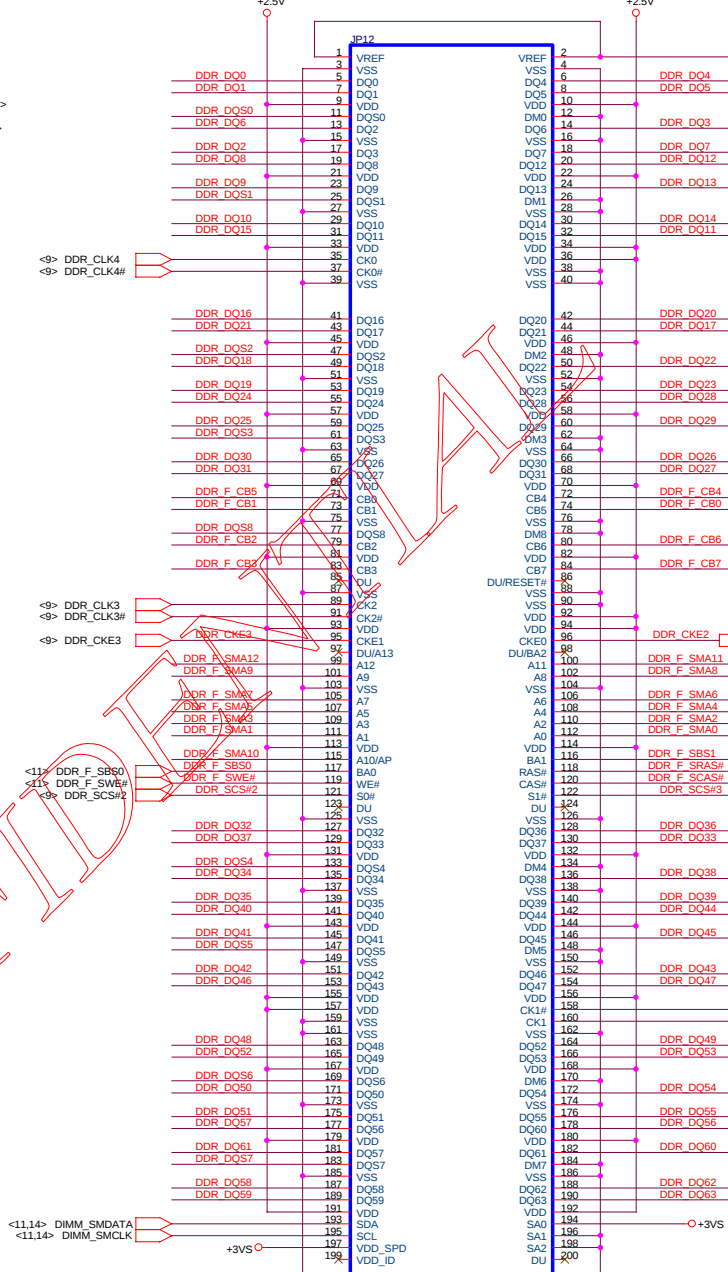
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DDR-SODIMM_SLOT1			
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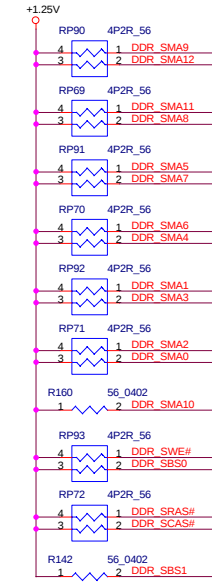
Layout note
Place these resistor
closely DIMM1,
all trace
length<=800mil

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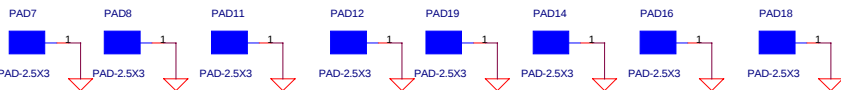
<114> DIMM_SMDATA
<114> DIMM_SMCLK

DIMM1
Top side



Layout note
Place these resistor
closely DIMM0,
all trace length
Max=1.3"

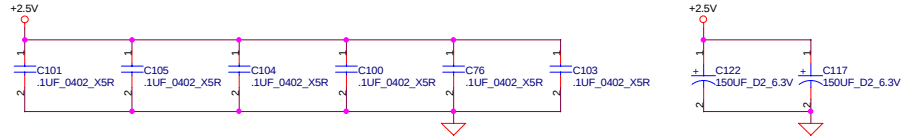
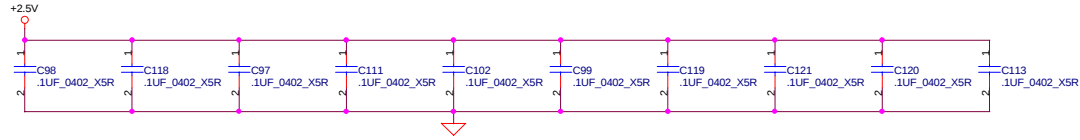
EMI Clip PAD for Memory Door



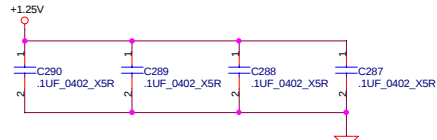
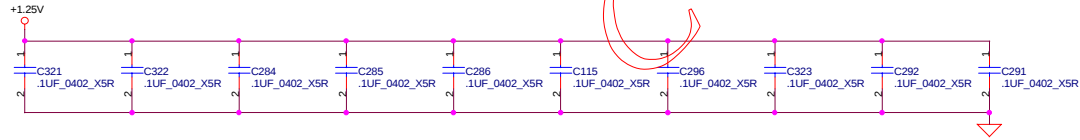
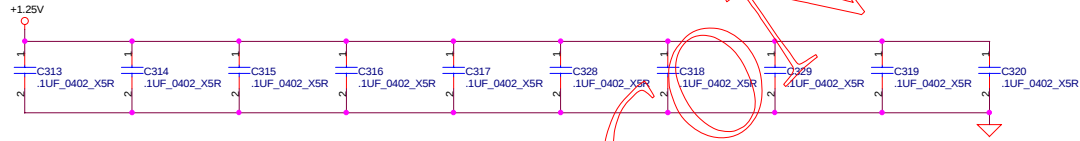
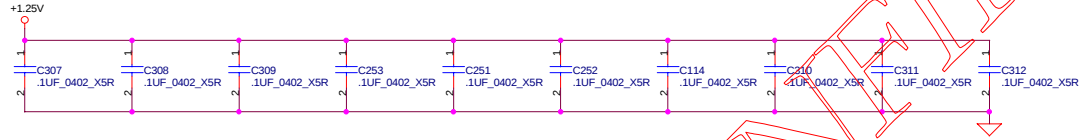
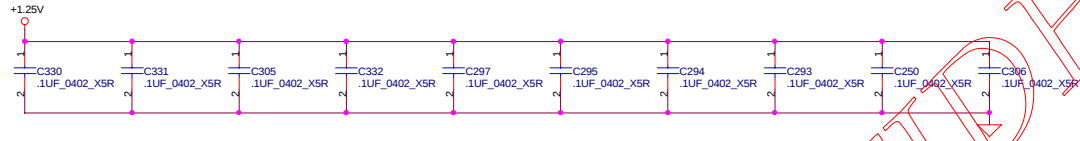
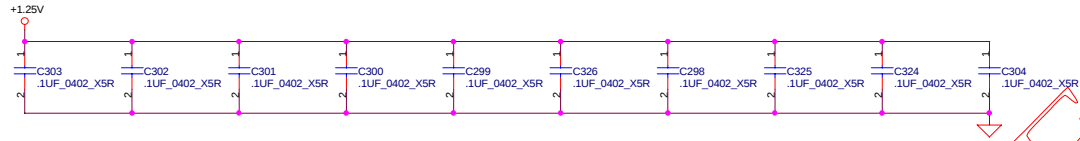
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Compal Electronics, Inc.			
Title DDR-SODIMM SLOT1			
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Layout note :
Distribute as close as possible
to DDR-SODIMM.



Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V

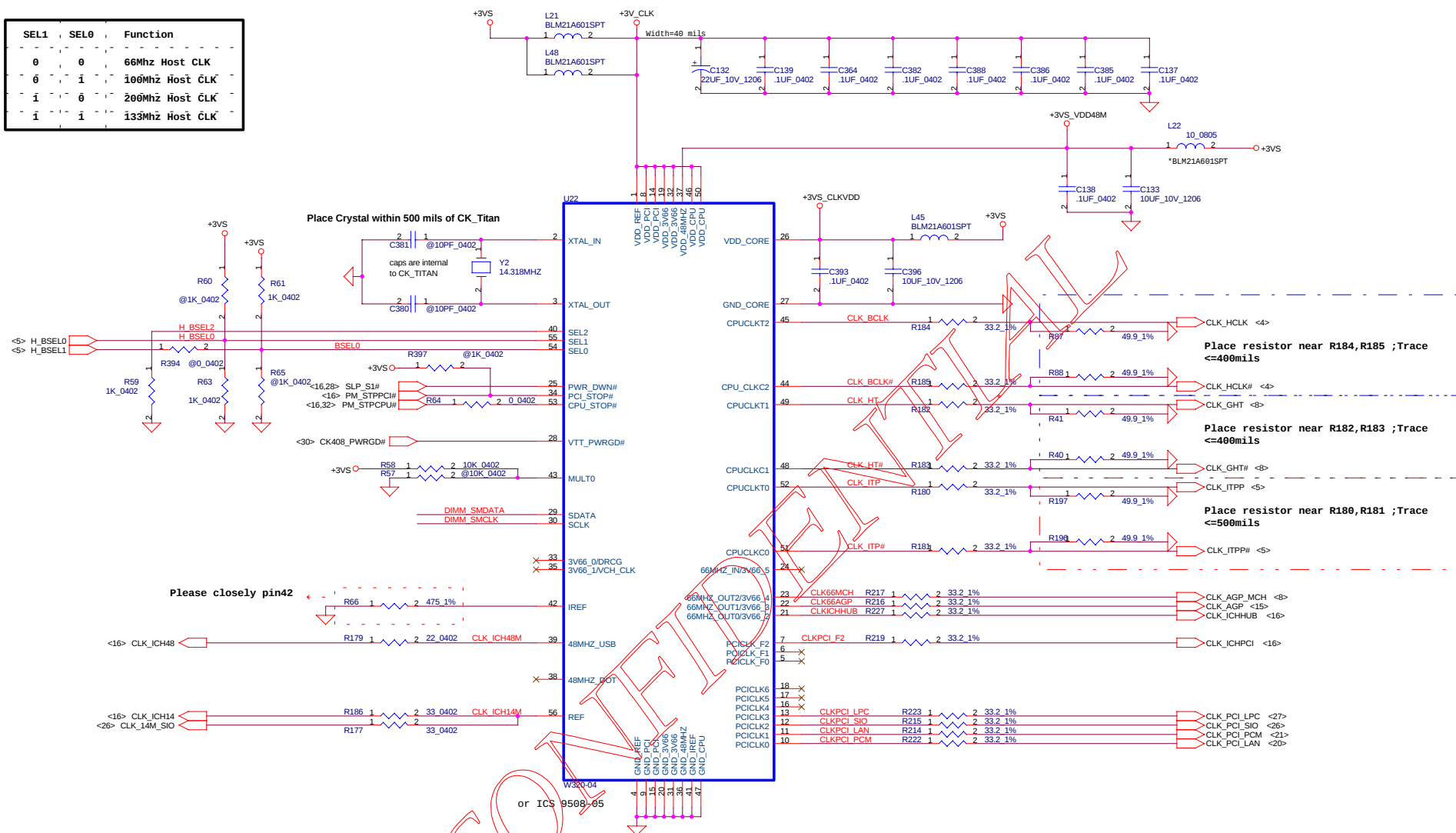


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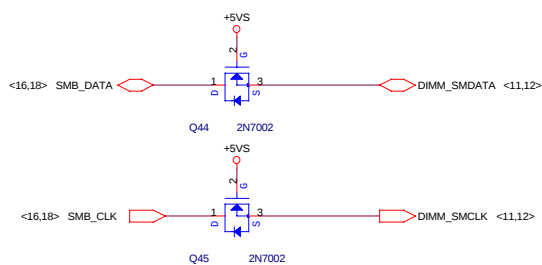
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Title			DDR SODIMM Decoupling	
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SEL1	SEL0	Function
0	0	66MHz Host CLK
0	1	100MHz Host CLK
1	0	200MHz Host CLK
1	1	133MHz Host CLK



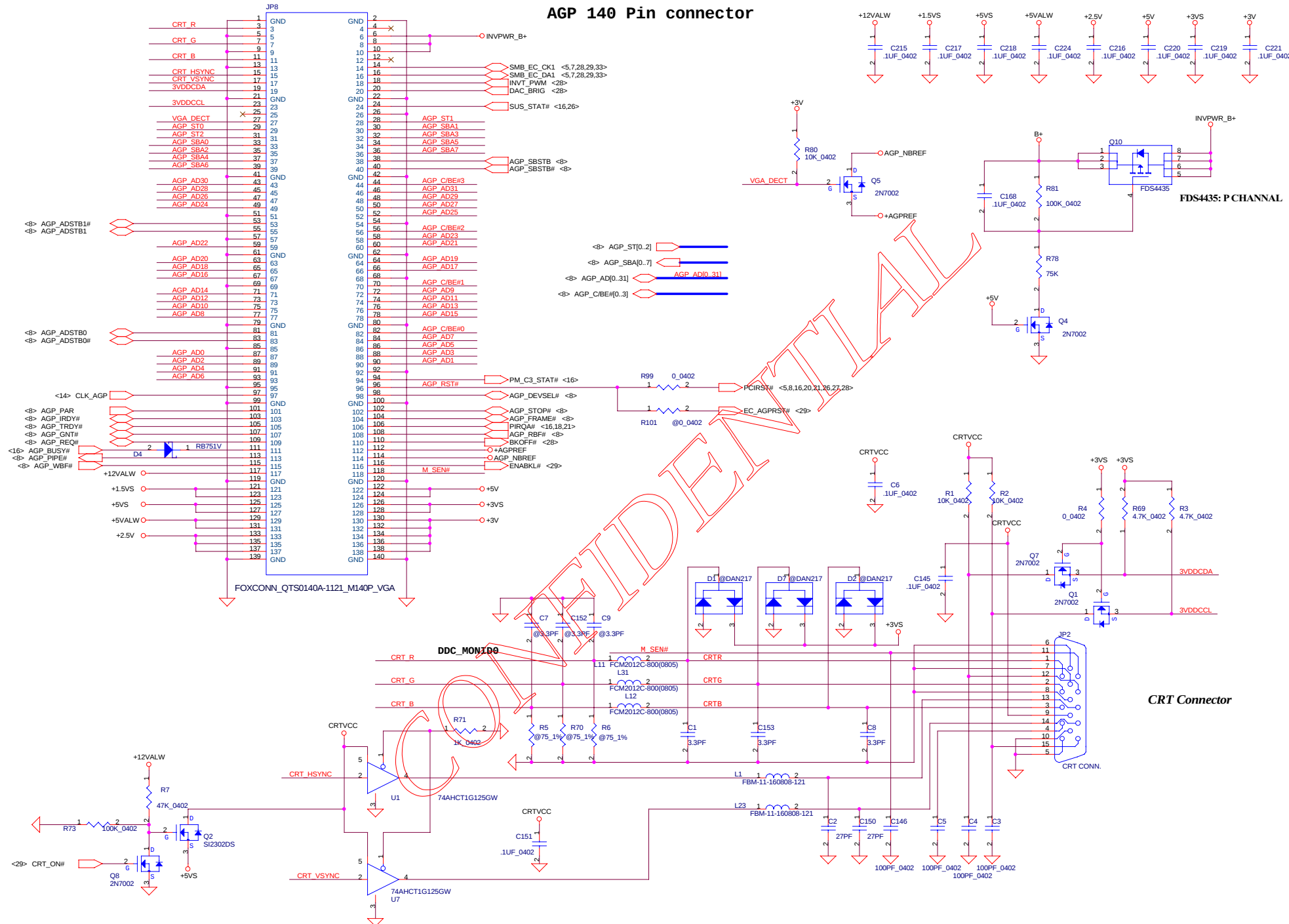
Note:
CPU_CLK[2:0] needs to be running in C3, C4.

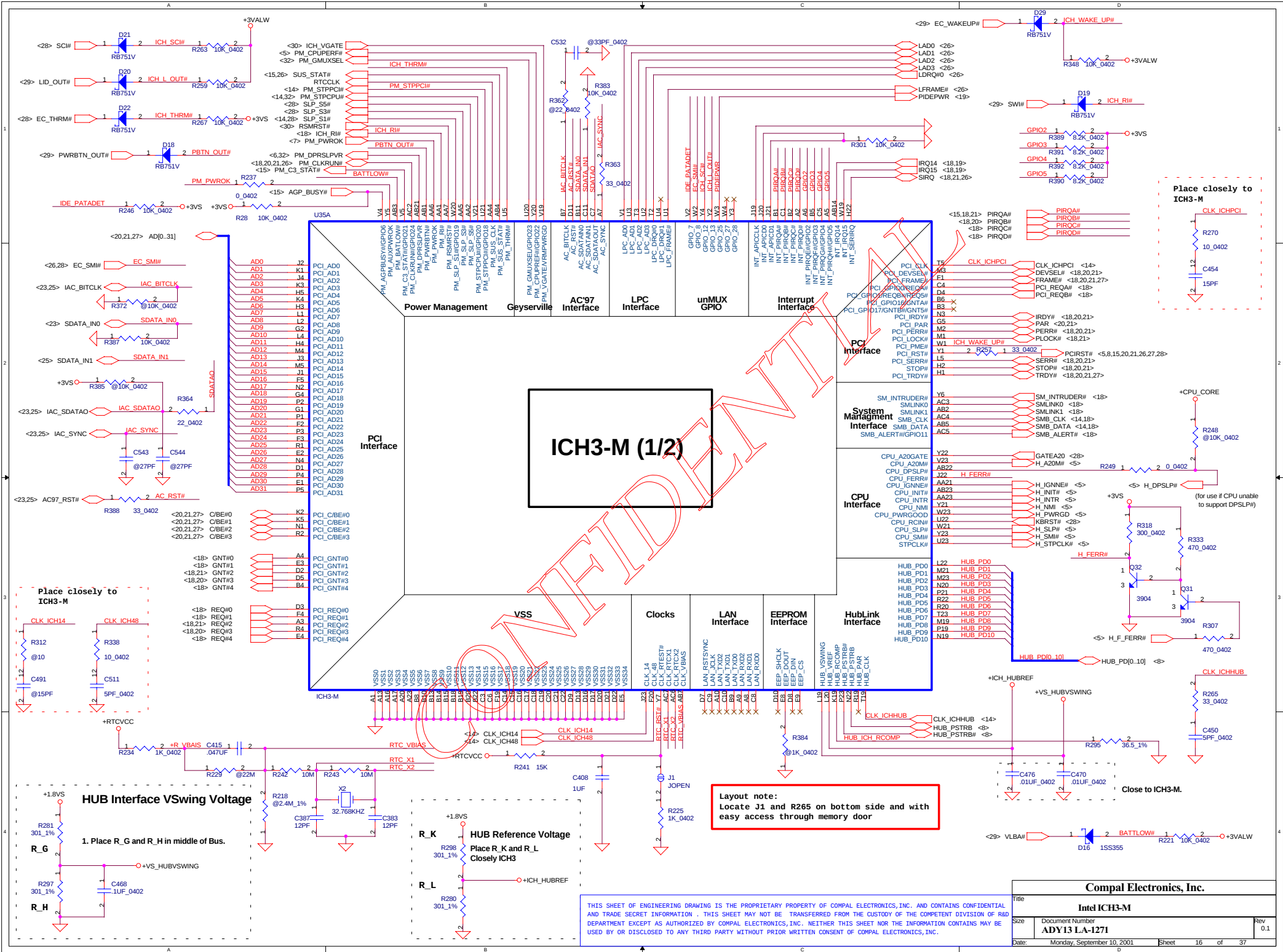


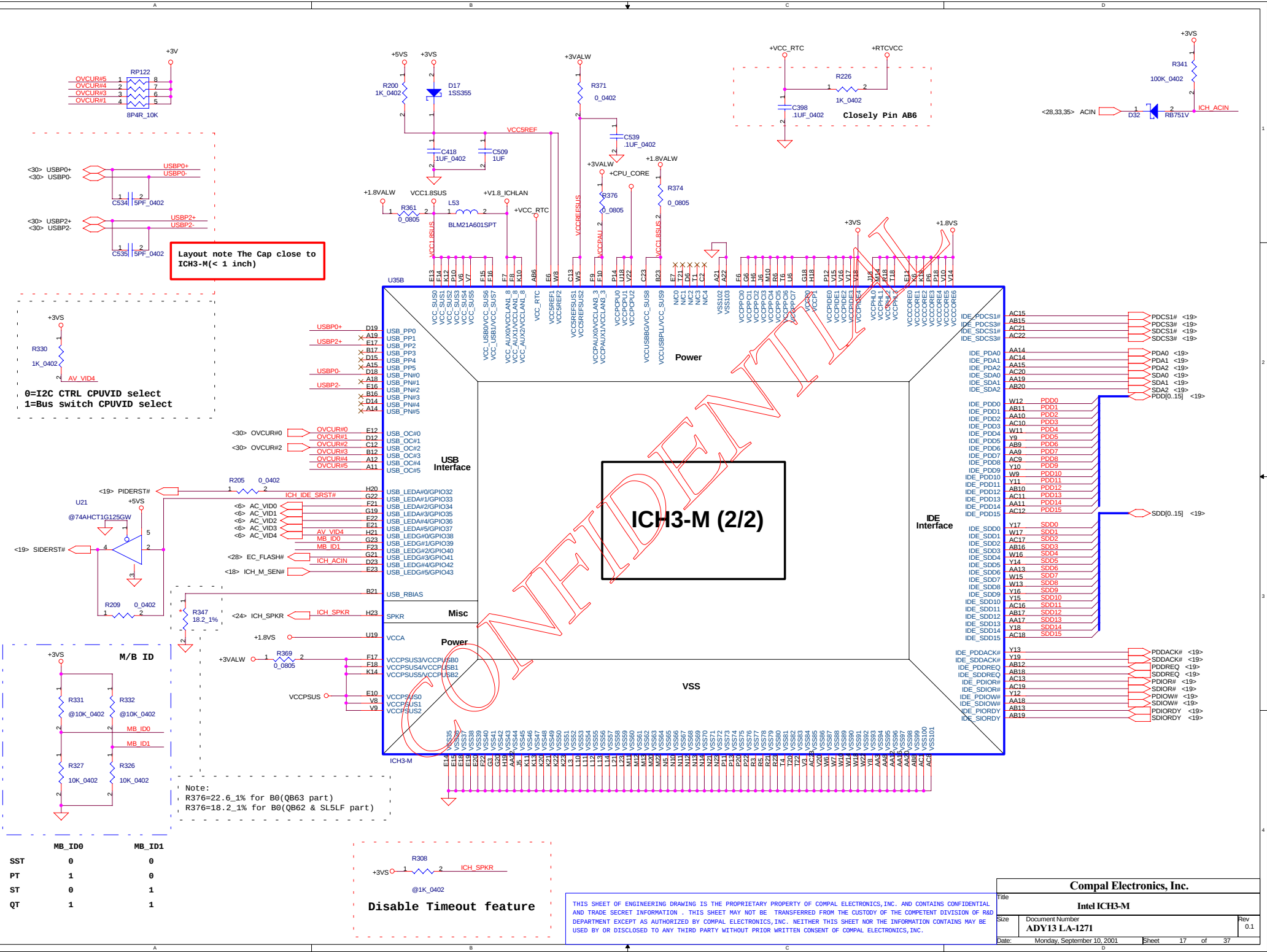
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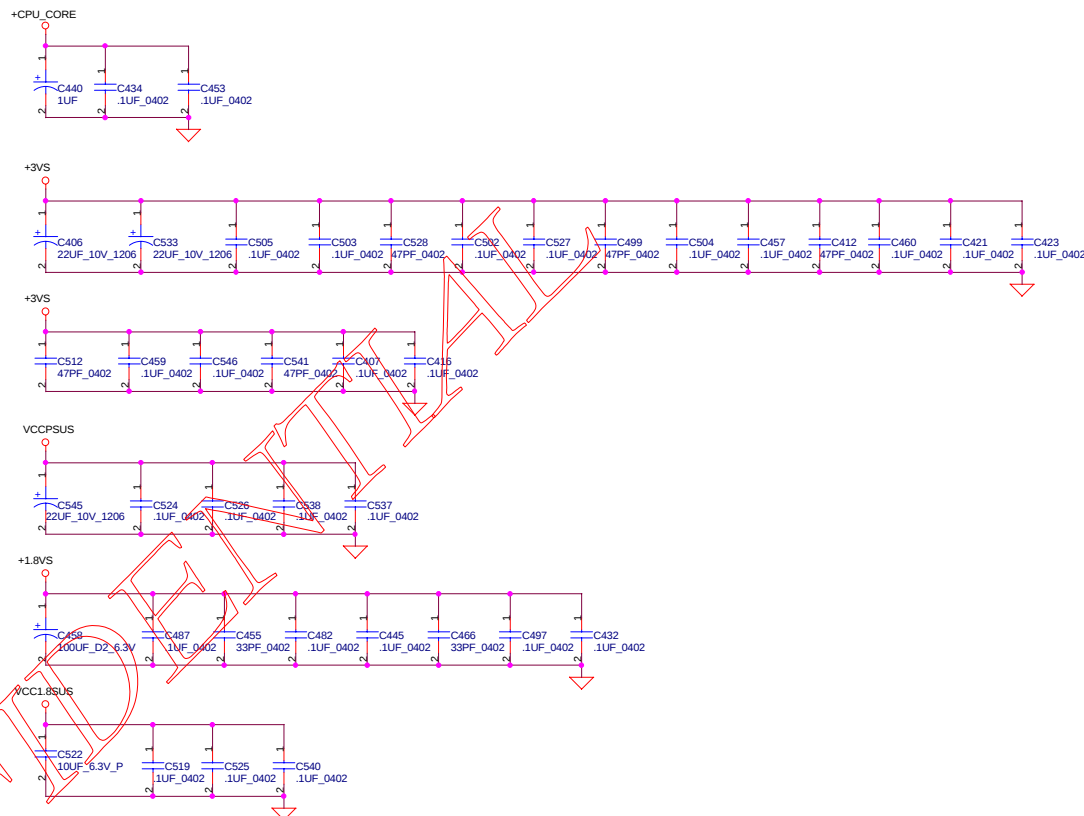
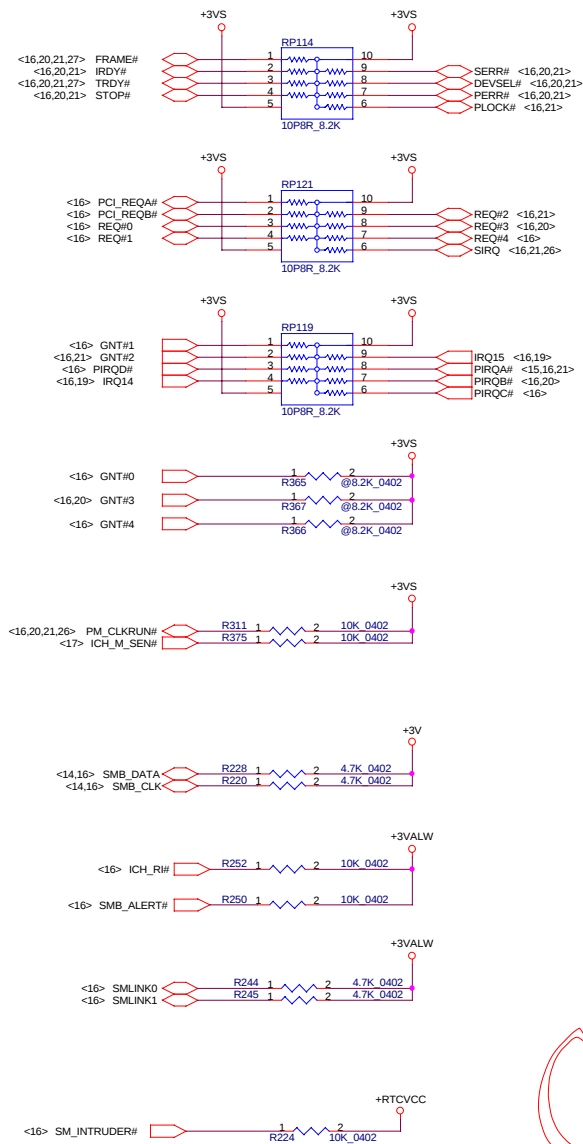
Compal Electronics, Inc.			
Title			
Clock Generator			
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AGP 140 Pin connector



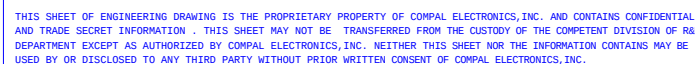


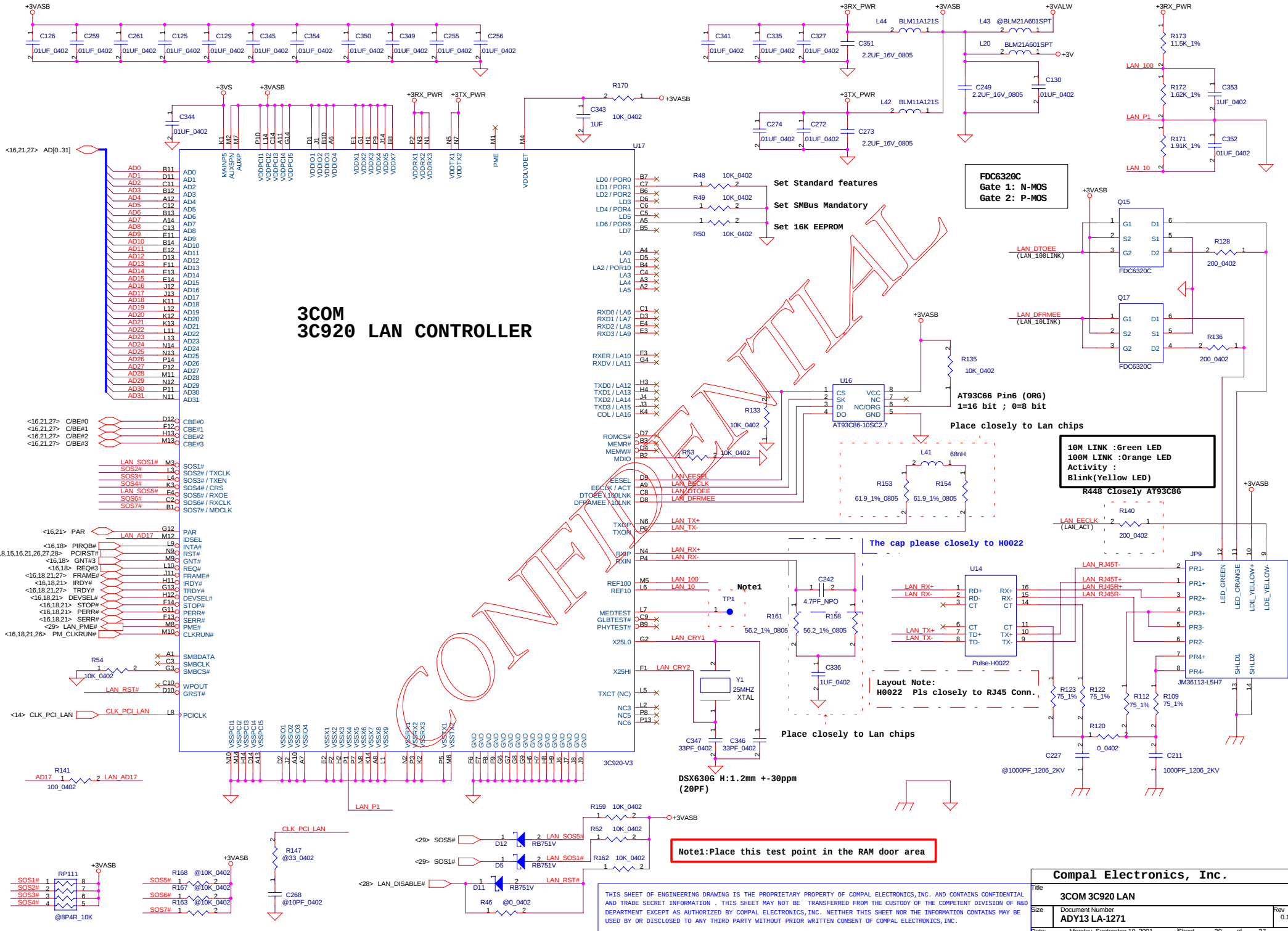


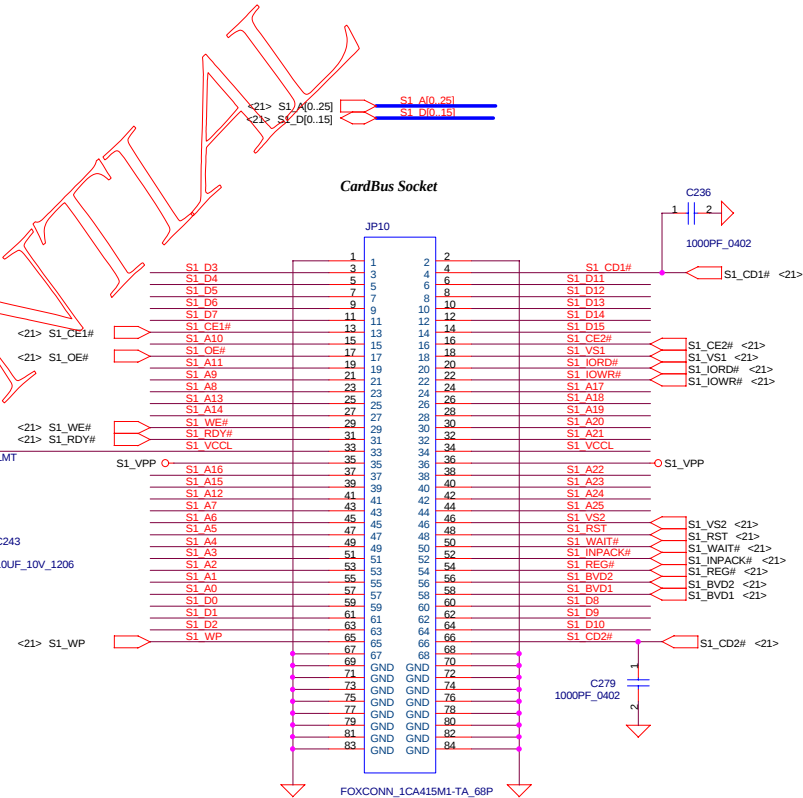
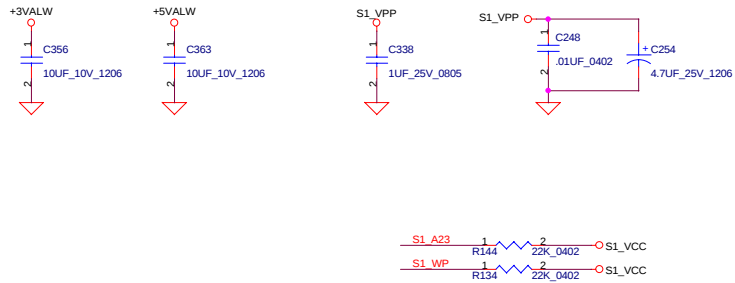


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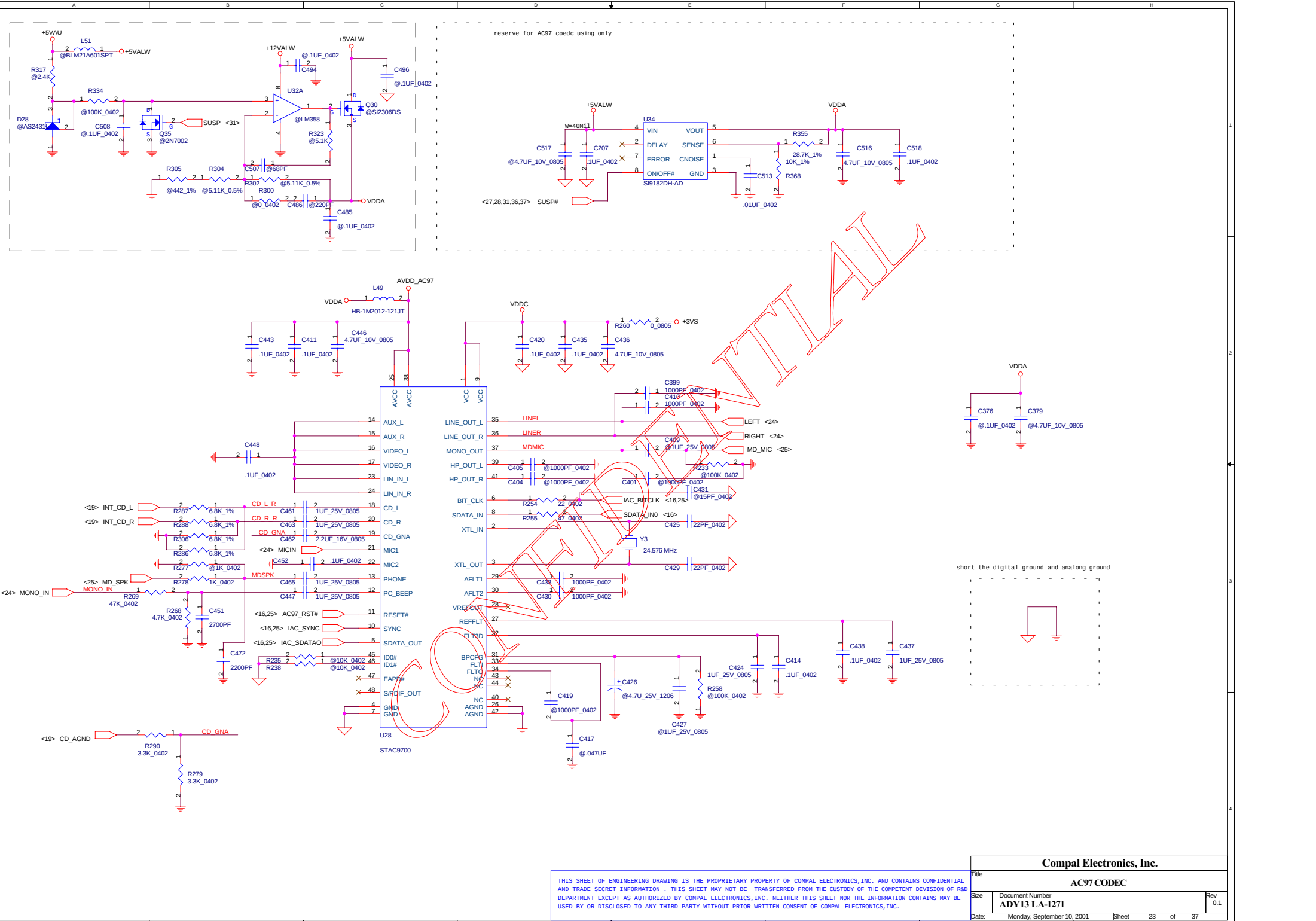
Compal Electronics, Inc.			
Title	ICH3-M Decoupling & Pull-Up		
Size	Document Number	Rev	
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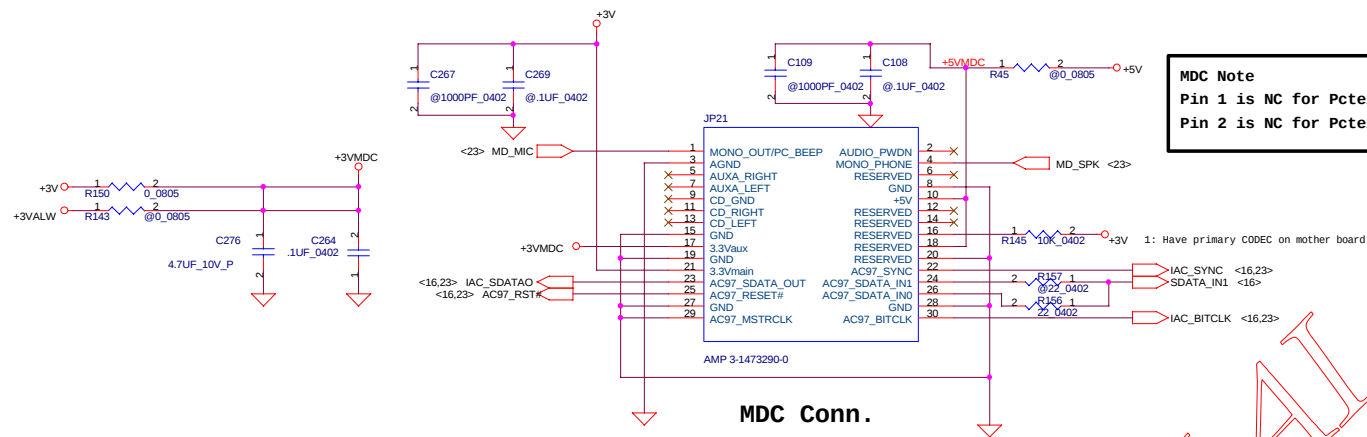
[illegible]

Compal Electronics, Inc.			
Title			
CardBus Socket			
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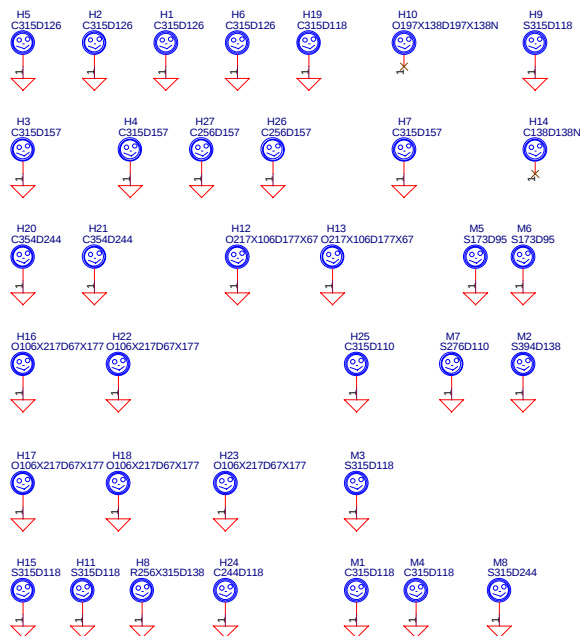
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Compal Electronics, Inc.			
Title			
AC97 CODEC			
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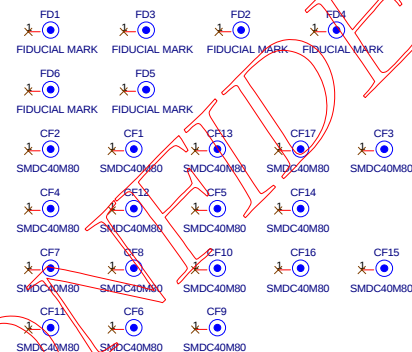


MDC Conn.

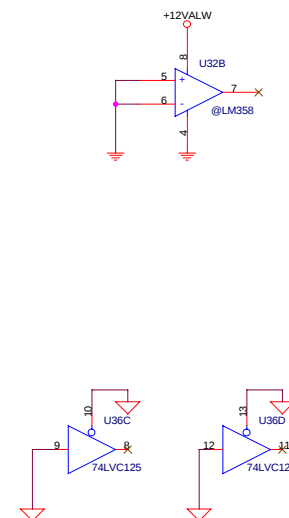
Screw Hole



Fiducial Mark



Spare Logic Gate



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Compal Electronics, Inc.			
Title		MDC connector / Skew Hole	
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The diagram illustrates the electrical connections for the JST BM20B-SRDS-G module, which includes a touch pad and status LEDs. The module is represented by a 20-pin connector (JP13) with pins numbered 1 through 20.

Pin Connections:

- Pin 1:** TP_CLK (Touch Pad Clock)
- Pin 2:** TP_DATA (Touch Pad Data)
- Pin 3:** +5VS (5V Supply)
- Pin 4:** +5VS (5V Supply)
- Pin 5:** +5VS (5V Supply)
- Pin 6:** +5VS (5V Supply)
- Pin 7:** +5VS (5V Supply)
- Pin 8:** +5VS (5V Supply)
- Pin 9:** ACT_LED# (Active Low LED)
- Pin 10:** BATT_LED# (Battery LED)
- Pin 11:** CHARGE_LED# (Charge LED)
- Pin 12:** CHARGE_LED# (Charge LED)
- Pin 13:** CHARGE_LED# (Charge LED)
- Pin 14:** CHARGE_LED# (Charge LED)
- Pin 15:** CHARGE_LED# (Charge LED)
- Pin 16:** CHARGE_LED# (Charge LED)
- Pin 17:** +3VS (3V Supply)
- Pin 18:** +3VS (3V Supply)
- Pin 19:** LID_SW# (Lid Switch)
- Pin 20:** LID_SW# (Lid Switch)

LED Connections:

- ACT_LED#:** Connected to Pin 9. The LED is labeled ACT_LED# <29>.
- BATT_LED#:** Connected to Pin 10. The LED is labeled BATT_LED# <29>.
- CHARGE_LED#:** Connected to Pins 11, 12, 13, 14, 15, and 16. The LED is labeled CHARGE_LED# <29>.
- LID_SW#:** Connected to Pins 19 and 20. The LED is labeled LID_SW# <29,30>.

Power Connections:

- +5VS:** Connected to Pins 3, 4, 5, 6, 7, 8, and 9.
- +3VS:** Connected to Pins 17 and 18.

Ground Connections:

- Ground is connected to Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20.

Component Values:

- TP_CLK: 220PF
- TP_DATA: 220PF
- ACT_LED#: 220PF
- BATT_LED#: 220PF
- CHARGE_LED#: 220PF
- LID_SW#: 220PF

PS2 CONN.

The schematic shows the PS2 keyboard and mouse connector circuit. It includes two 28-pin ICs, U3 (KBMF01SC6) and U2 (KBMF01SC6), which are PS/2 interface chips. U3 is connected to the PS2_DATA and PS2_CLK signals. U2 is connected to the KBD_DATA and KBD_CLK signals. The circuit also includes a 5V supply, a 1.1A polyswitch (F1), a 4516 capacitor, a 40mils trace, a 4516-1600T capacitor, a 25V 0805 capacitor (C14), and a 33005A-06T1-C1-PS2 connector (JPS5).

PS2 CONN.

PS2_DATA

PS2_CLK

U3

DATA IN

DATA OUT

GND

VCC

CLK IN

CLK OUT

KBMF01SC6

+5V_S

F1

W=40mils

PS2KB_VCC

KB_AS

W=40mils

C14

1UF_25V_0805

JPS5

4

6

2

3

1

5

KBDFPS2_6

33005A-06T1-C1-PS2

116795326

U2

DATA IN

DATA OUT

GND

VCC

CLK IN

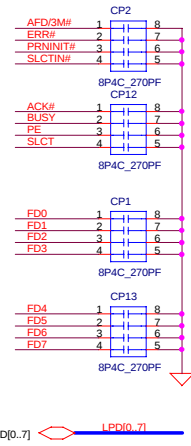
CLK OUT

KBMF01SC6

KBD_DATA

KBD_CLK

Debug PORT

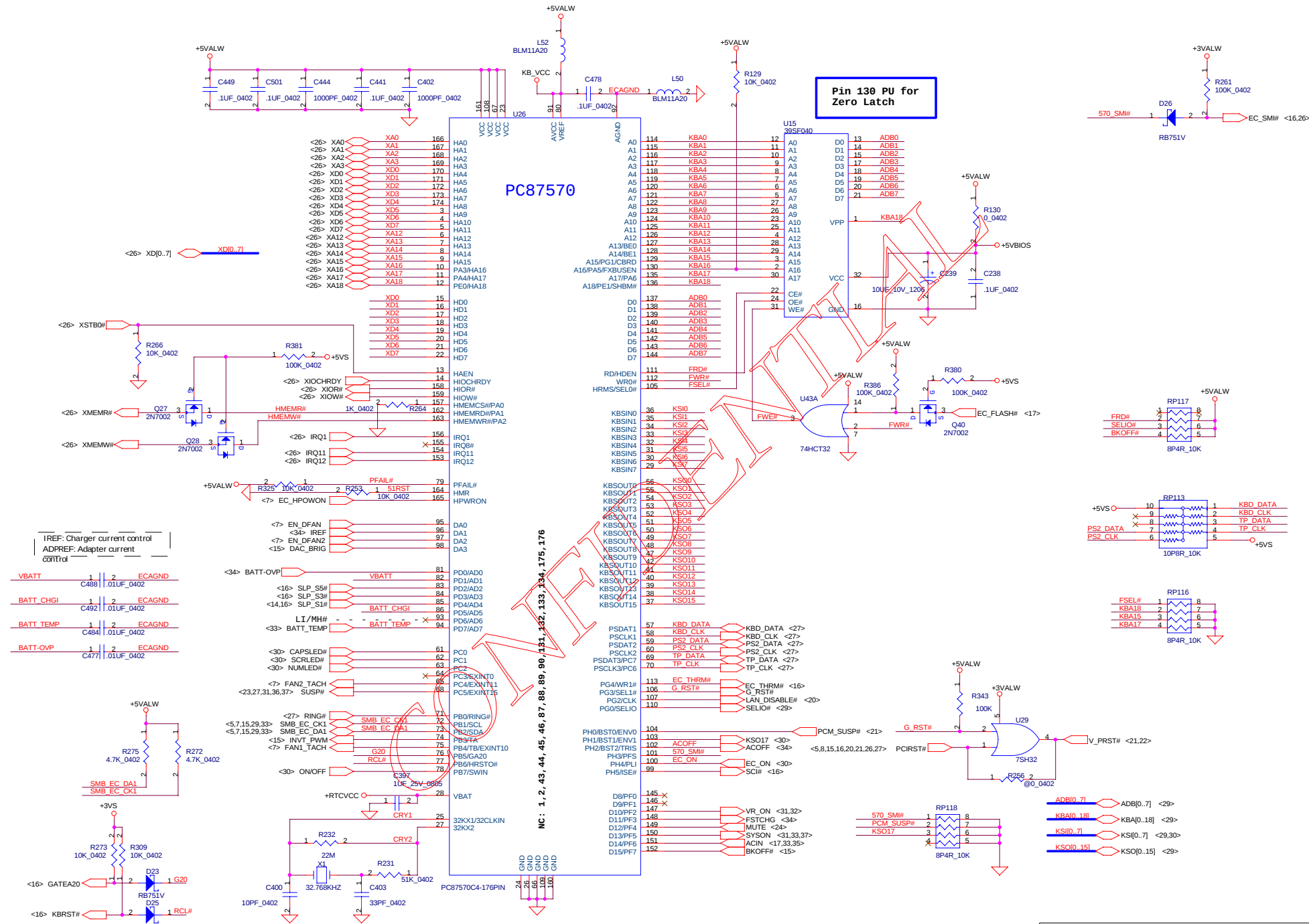
[illegible]

Reserved serial port for software ACPI debug

ACPI Debug port

Place close to COM1 connector.

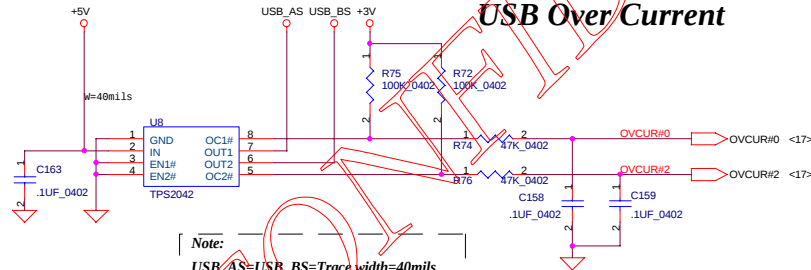
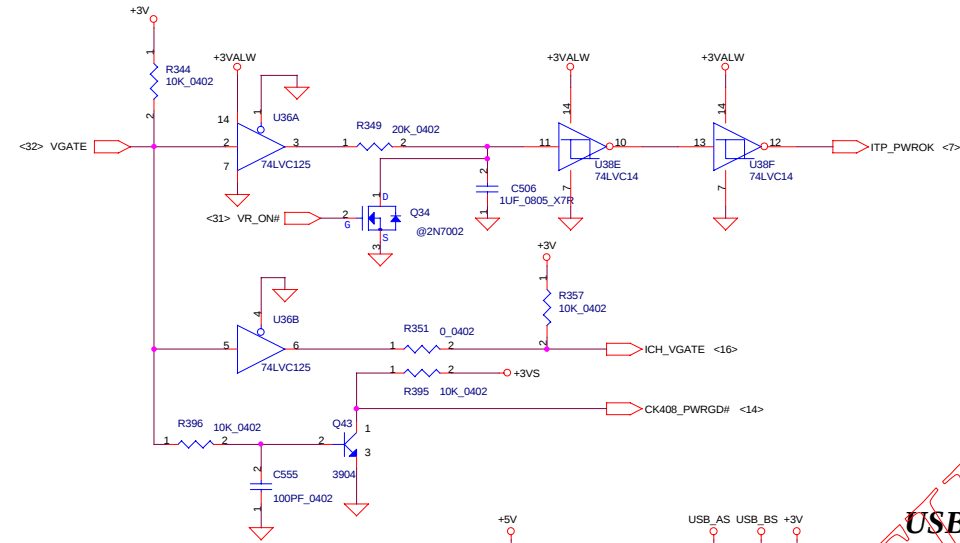
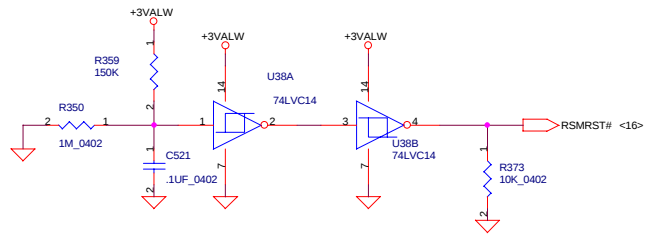
Compal Electronics, Inc.			
Title PIO/PS2 Port/T_P Conn. & PCI Debug Conn.			
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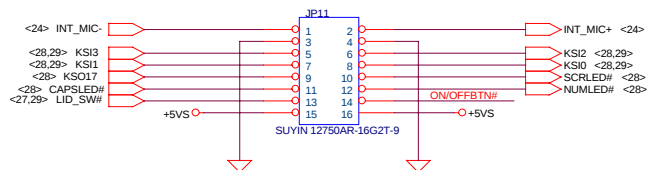
Compal Electronics, Inc.			
Title			
PC87570			
Size			
Document Number			
ADY13 LA-1271			
Date			
Monday, September 10, 2001			
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Rev			
0.1			

Power ON Circuit

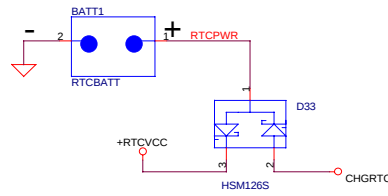


Note:
USB_AS=USB_BS=Trace width=40mils

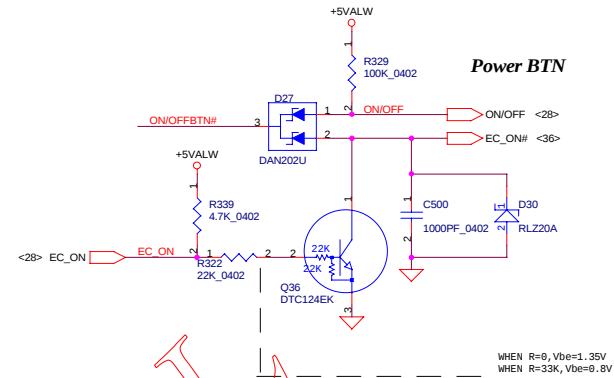
LID Switch & Function Button



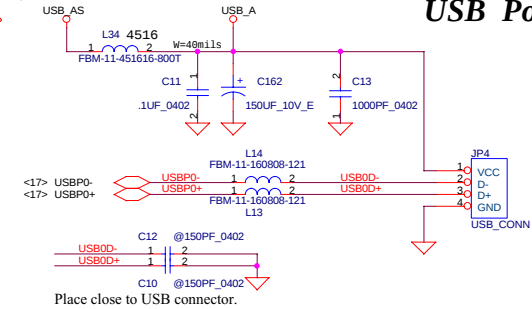
RTC Battery



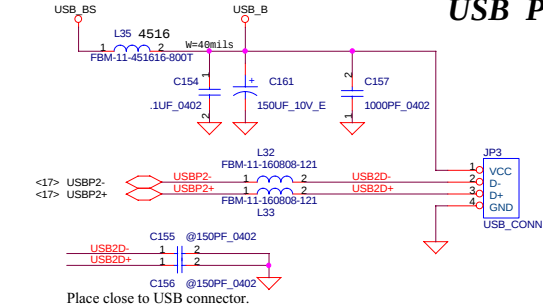
Power BTN



USB Port 0



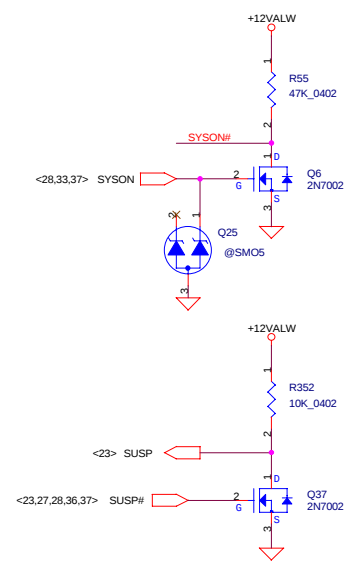
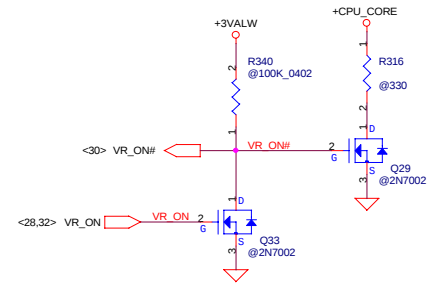
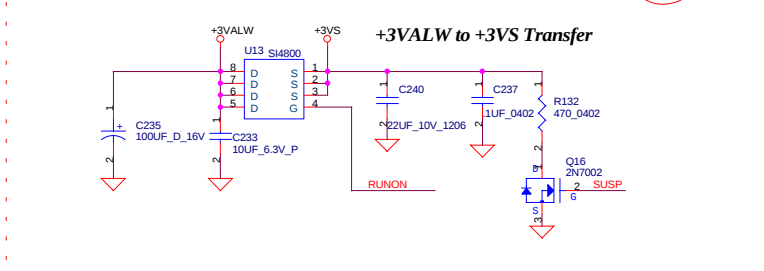
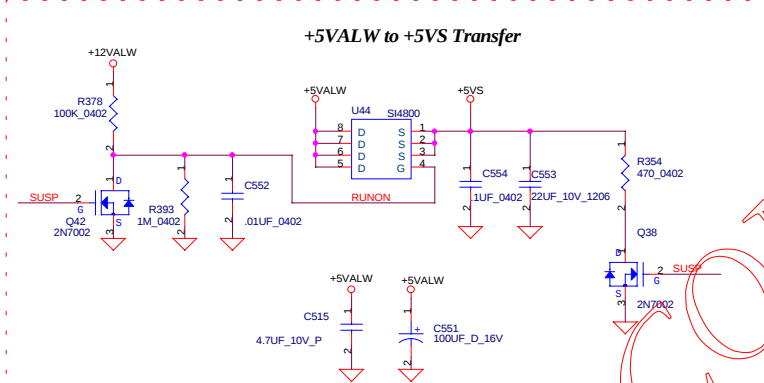
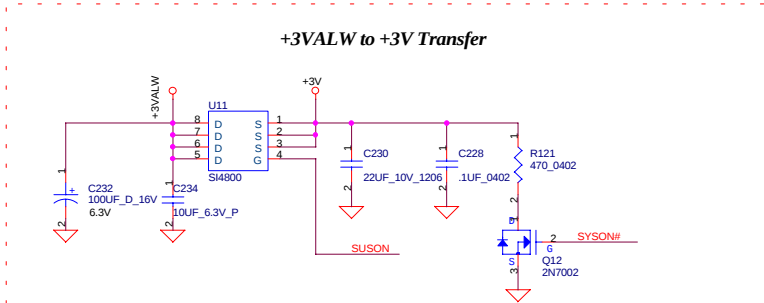
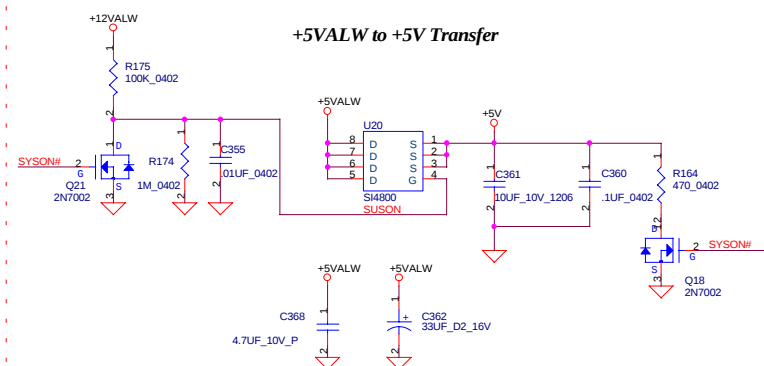
USB Port 1



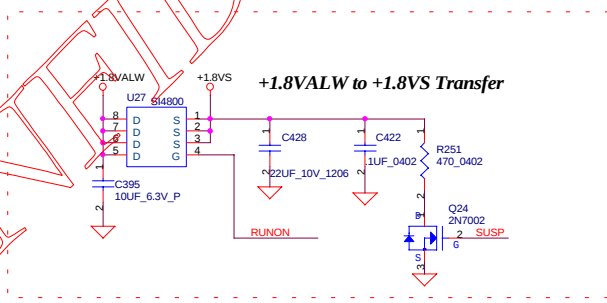
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Title	Power OK/Reset/RTC battery/USB Conn.& Lid Switch		
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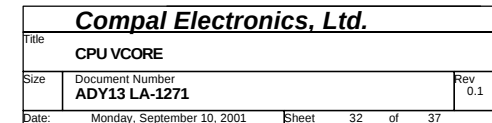


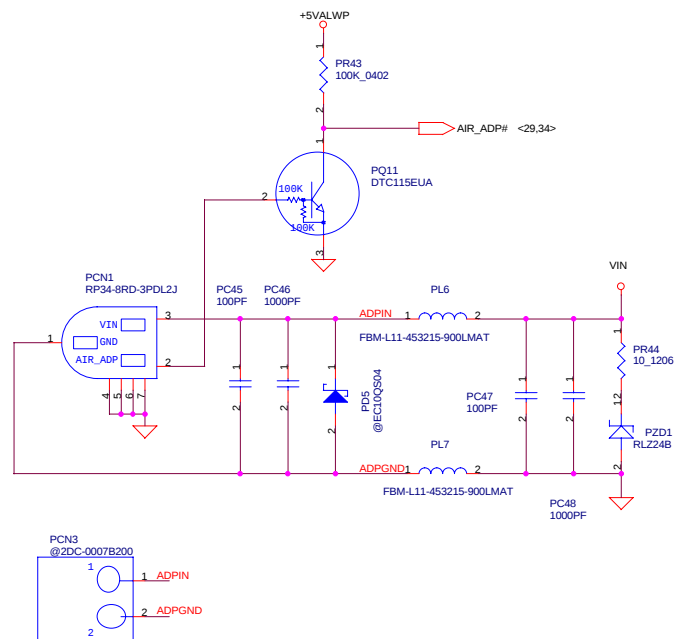
1.8VALW/+1.5VS Power direct provide



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Compal Electronics, Inc.			
Title	DC/DC Circuit		
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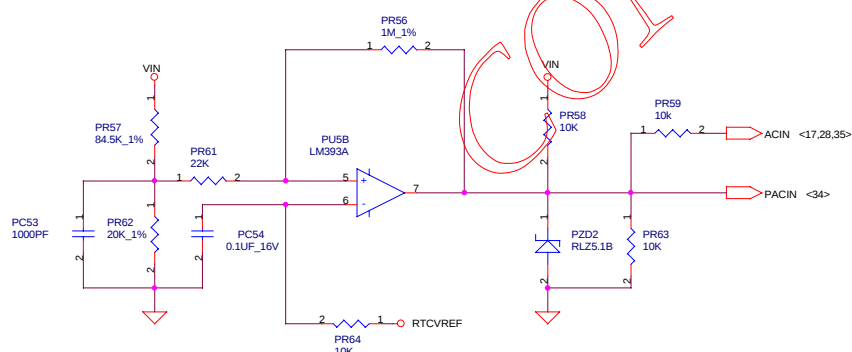




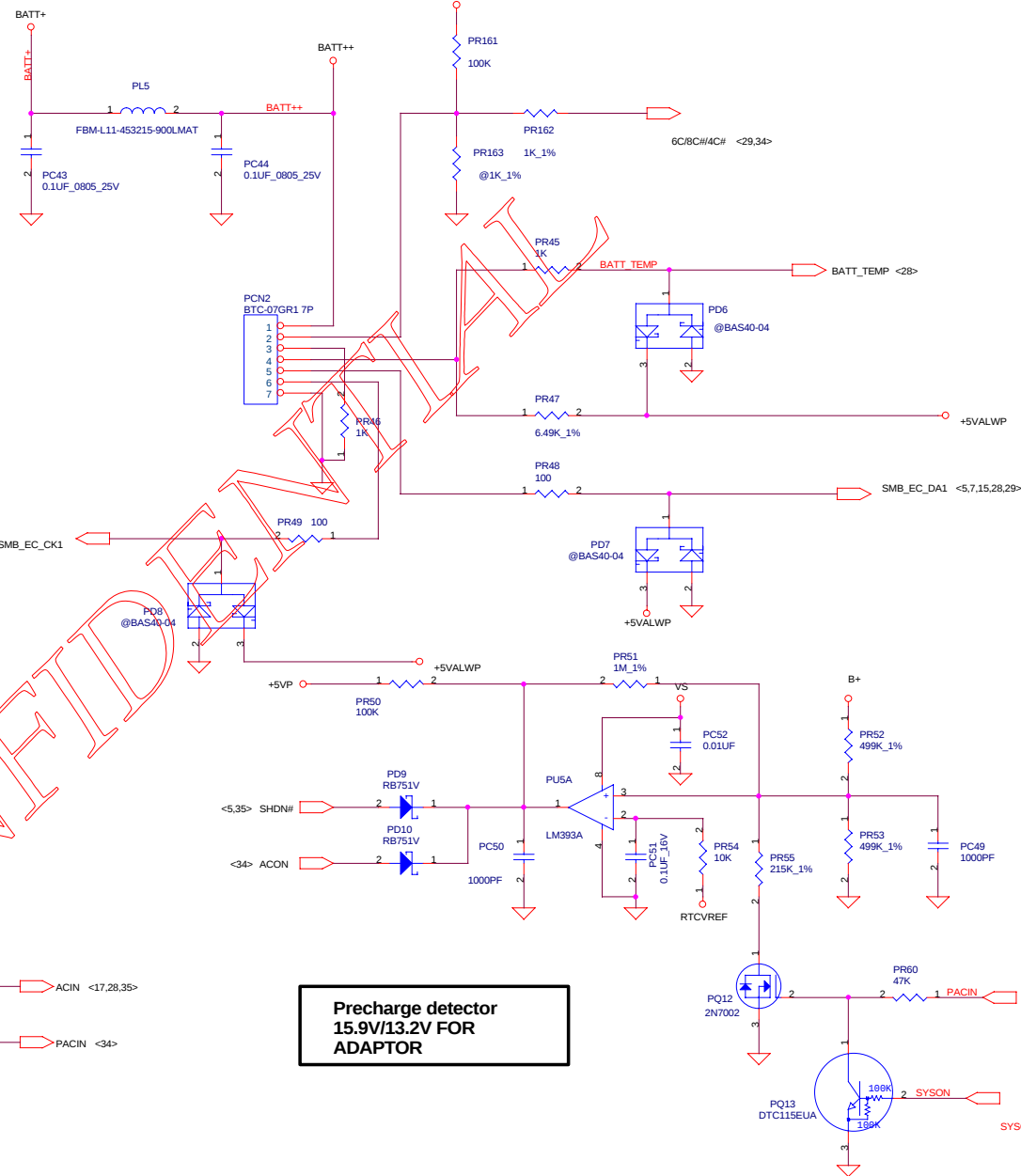
PCN2 battery connector pin assignment

SMART Battery:

1. BAT+
2. LI/MH#
3. B/I
4. TS
5. SMB_EC_DA1
6. SMB_EC_CK1
7. GND

Vin Detector
17.93V/17.2V

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Precharge detector
15.9V/13.2V FOR
ADAPTOR

Compal Electronics, Inc.

Title		
Detector		
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$I_{adp}=0\sim 3.22A$ <-----Actually about 3A
 $I_{air}=0\sim 2.26A$

$I_{REF}=1.746 \cdot I_{charge}$
 $I_{REF}=0\sim 5V$

Charge voltage
 4S LI-ION
 NI-MH : 17.00V
 3S LI-ION : 12.75V

OVP voltage :

LI-4S : 18.3V----BATT-OVP=4.04V

LI-3S : 13.5V----BATT-OVP=3.82V

BATT-OVP=0.2206*BATT++

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Charger

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+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

CPU thermal protection at 85 degree C
Recovery at 45 degree C

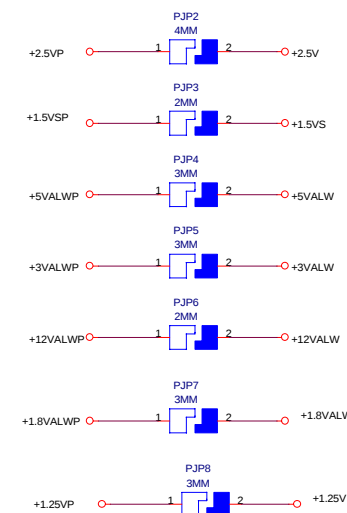
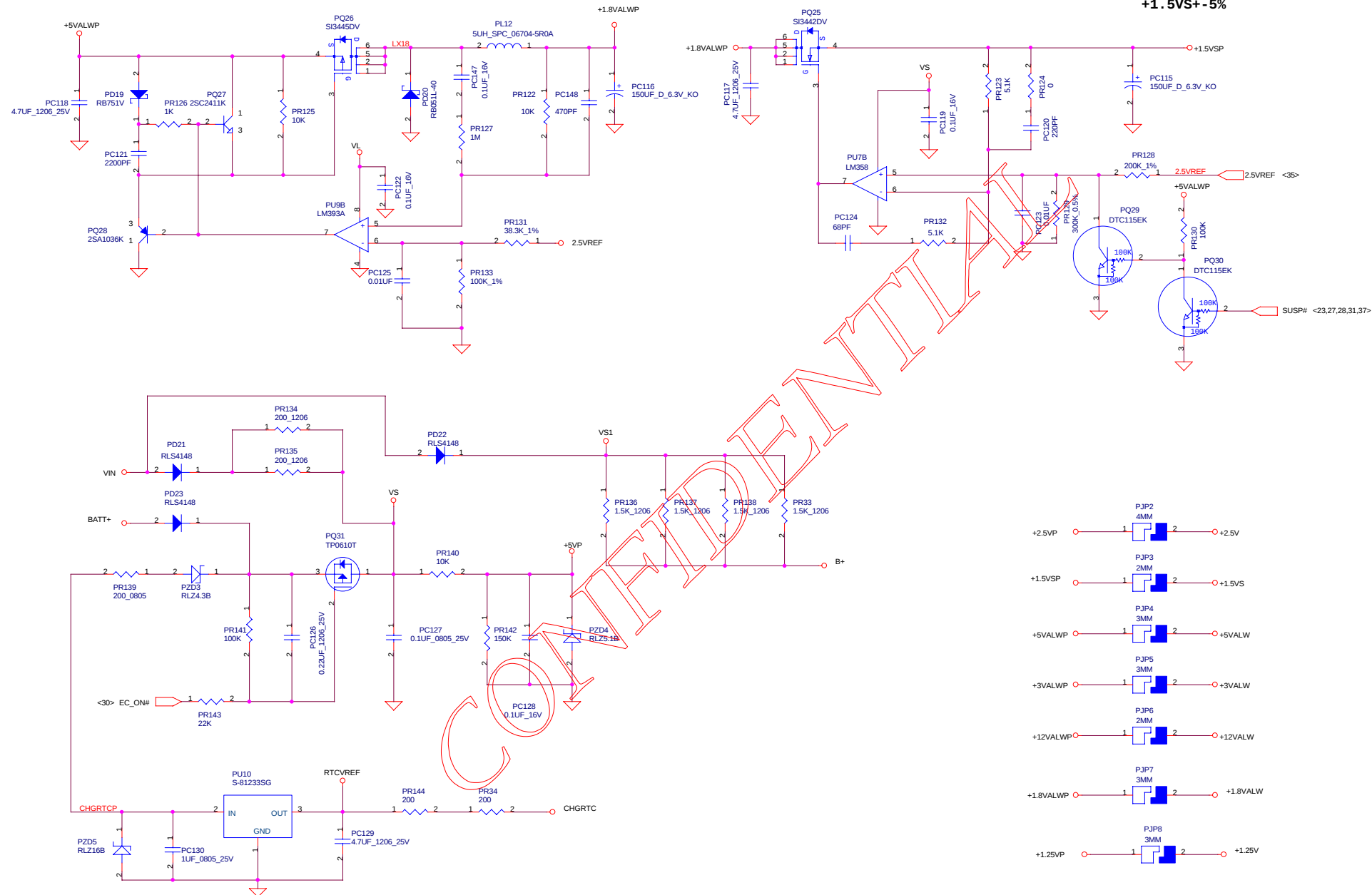
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Title			+3.3V/+5V/+12V	
Size	Document Number		Rev	
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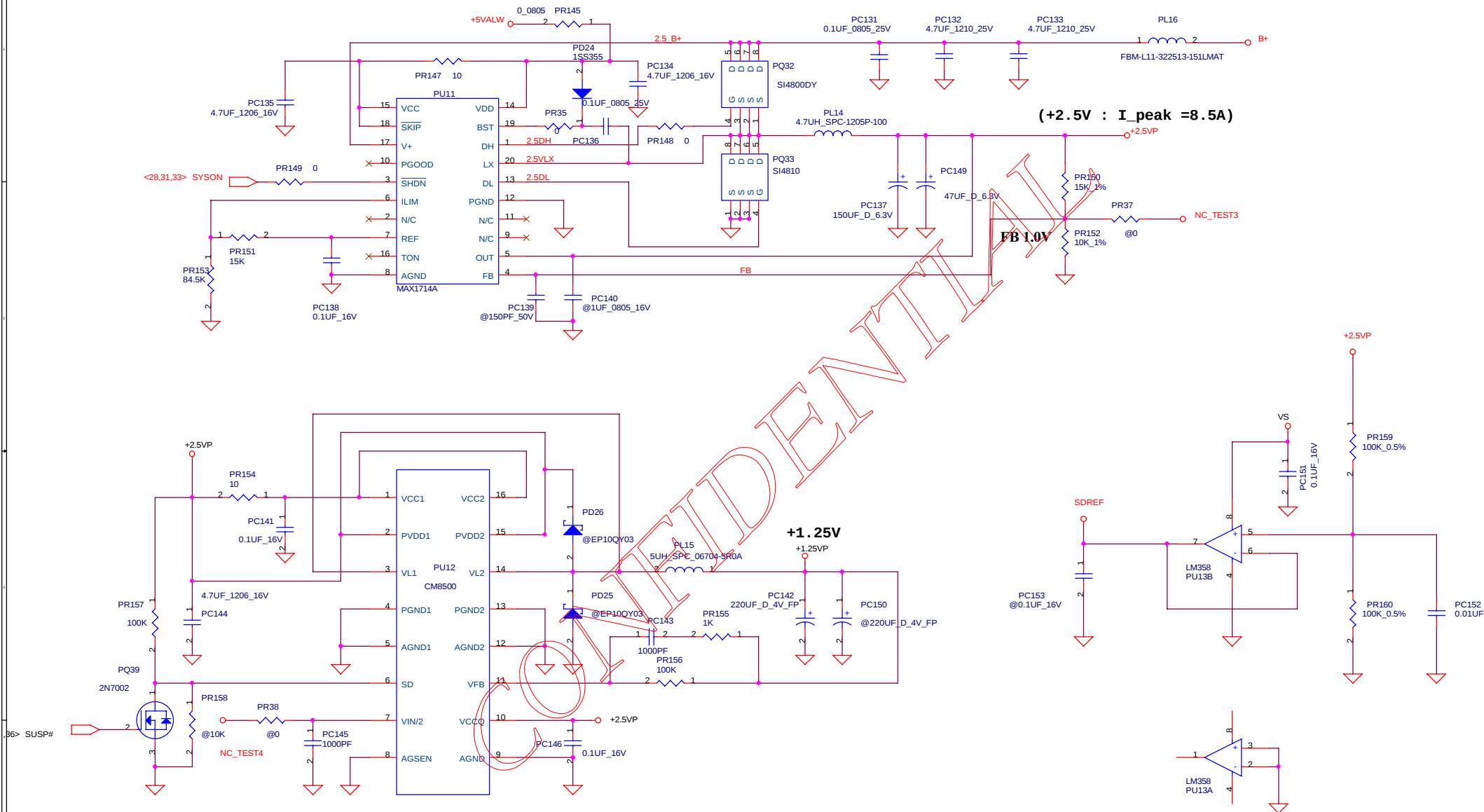
+1.8V+-5%

+1.5VS+-5%



Compal Electronics, Inc.

Title		+1.8VALW	
Size	Document Number	Rev	
	ADY13 LA-1271	0.1	
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COMPAL ELECTRONICS, INC			
Title			
DDR POWER 2.5V & 1.25V			
Size	Document Number		Rev
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