Enrico/Caruso 15" UMA Schematics Document
Sandy Bridge
Intel PCH
2011-06-02
REV : A00

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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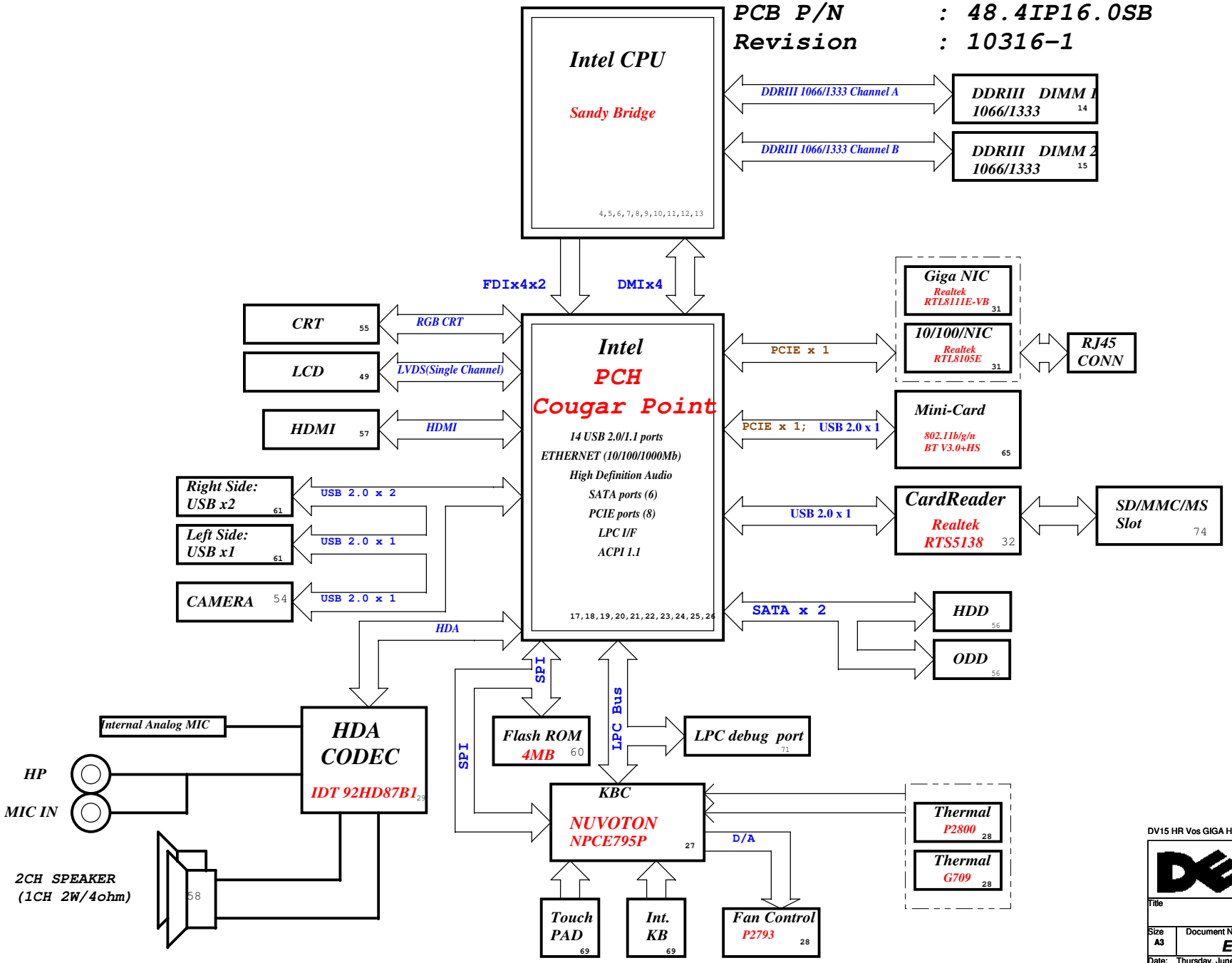
DV15 Huron River UMA Block Diagram

Project code : 91.4IP01.001
PCB P/N : 48.4IP16.0SB
Revision : 10316-1



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC ISL95831HRTZ 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

GFX DC/DC ISL95831HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC TPS51218 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51123RGER 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5

SYSTEM DC/DC TPS51216RUKR 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

MAXIM CHARGER BQ24707 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC TPS51311RGTR 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER	
L1:Top	L4:Signal
L2:GND	L5:VCC
L3:Signal	L6:Bottom

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Title: Block Diagram

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Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** **No Reboot Mode with TCO Disabled:**
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	9V-12.6V 9V-19V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	X
LANE2	Onboard LAN
LANE3	x
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	X
2	X
3	X
4	ODD1
5	X

USB Table

Pair	Device
0	X
1	USB Ext. port 1
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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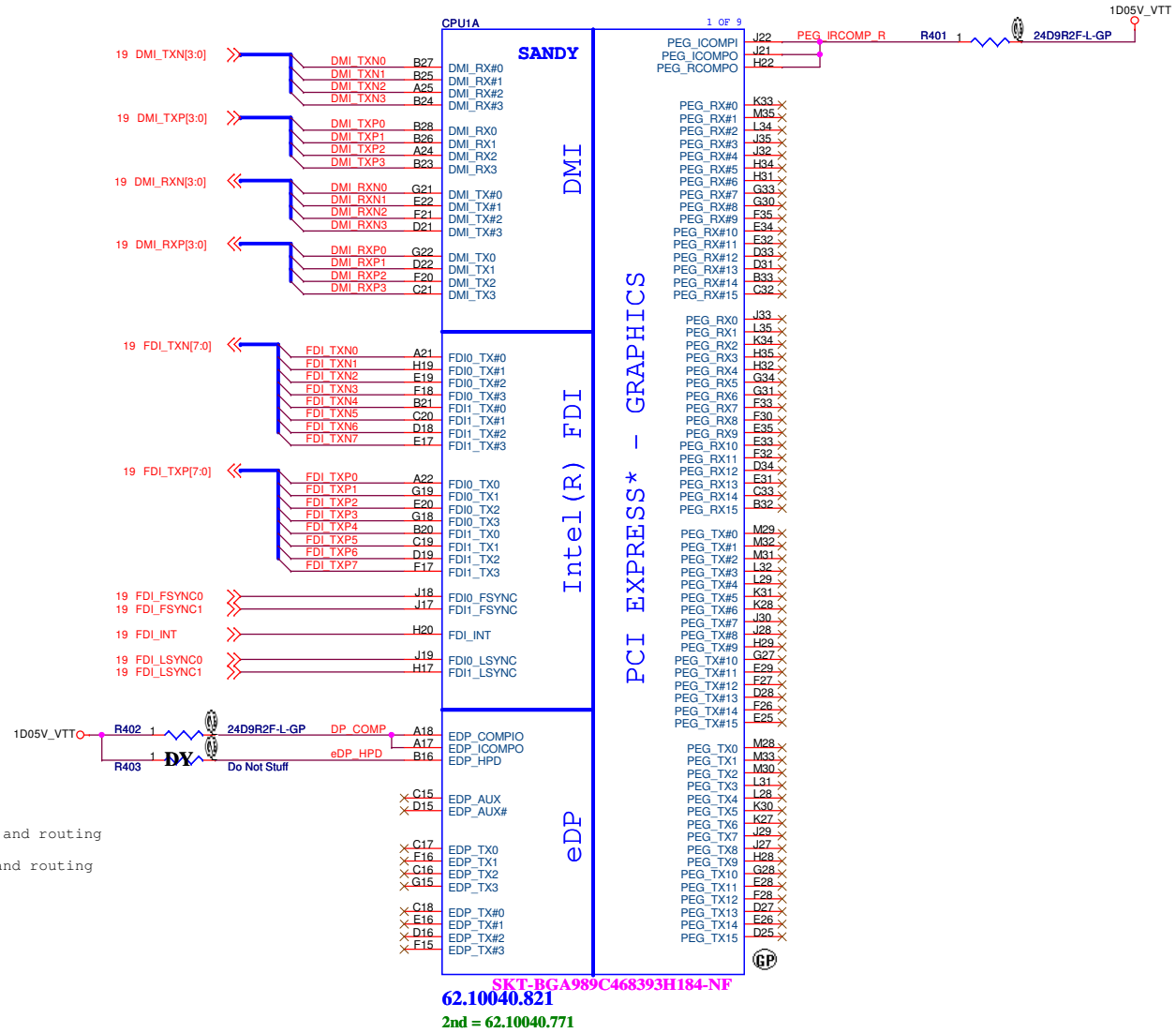
SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

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Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
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SSID = CPU

CPU1B

2 OF 9

SANDY

MISC

CLOCKS

THERMAL

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

SKT-BGA989C468393H184-NF

62.10040.821

2nd = 62.10040.771

CRB : 47pf
CEKLT:43pf

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

Buffered reset to CPU

Do Not Stuff

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Title: CPU (THERMAL/CLOCK/PM)

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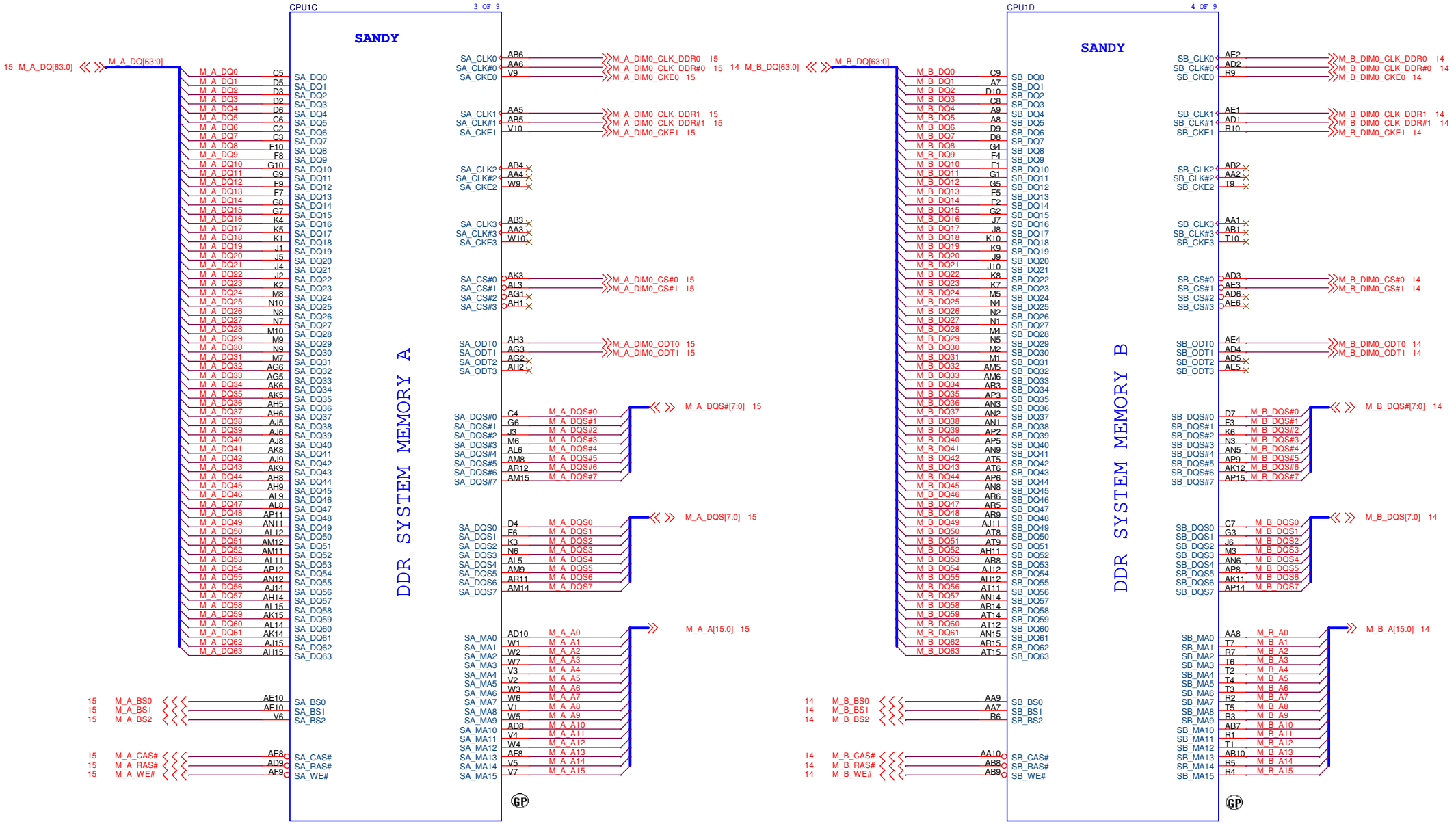
SSID = CPU



62.10040.821
2nd = 62.10040.771

62.10040.821
2nd = 62.10040.771

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Title: CPU (DDR)

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

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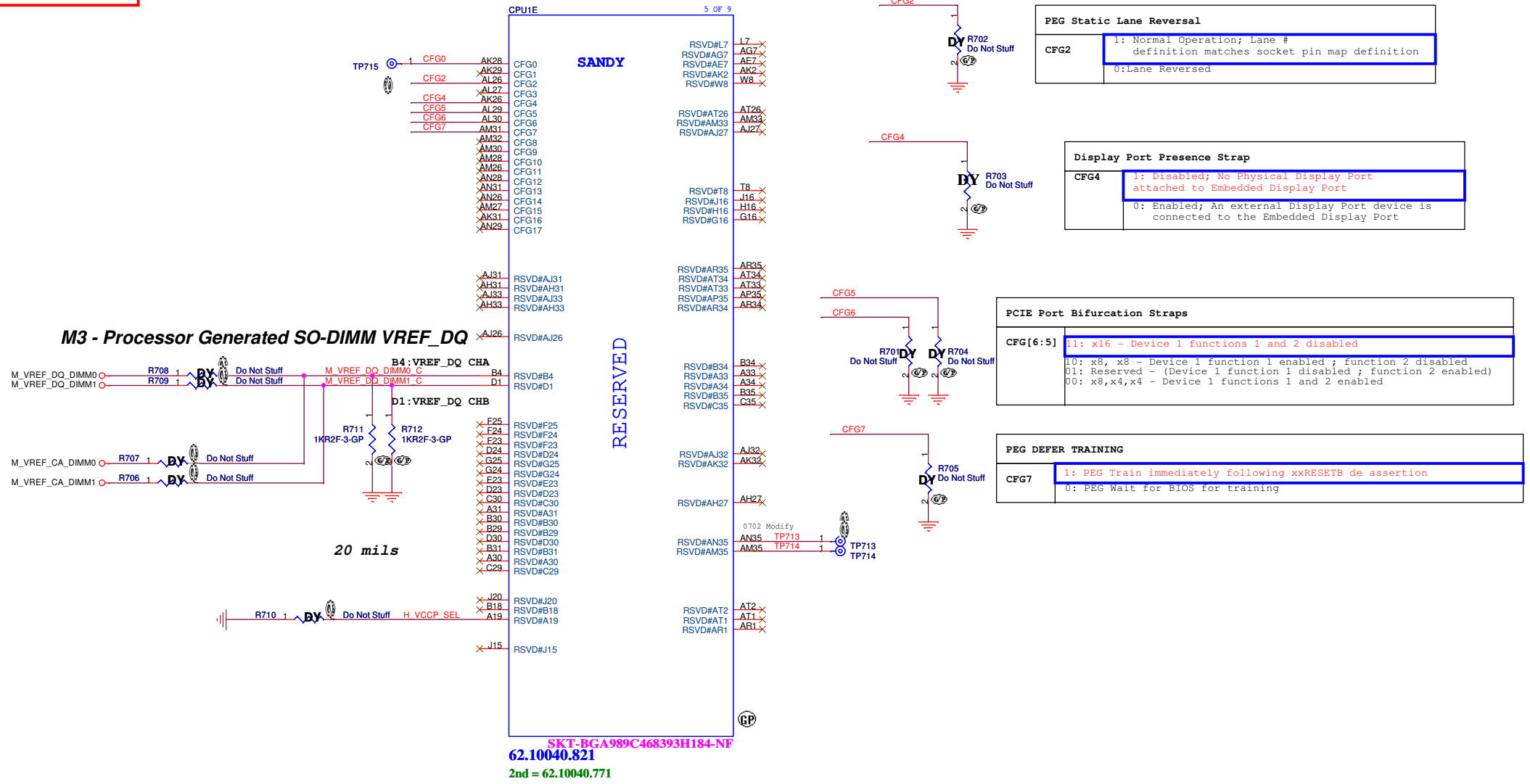
SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

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Title: *CPU (RESERVED)*

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SSID = CPU

POWER

CPU1F

SANDY

6 OF 9

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

VCC_CORE

PROCESSOR CORE POWER

53A

PROCESSOR VCCIO: 8.5A

1D05V_VTT

H_CPU_SVIDDAT R804 130R2F-1-GP

VIDALERT# AJ29 H_CPU_SVIDALRT# R806 43R2J-GP VR_SVID_ALERT# 42

VIDSCLK AJ30 H_CPU_SVIDCLK H_CPU_SVIDCLK 42

VIDSOUT AJ28 H_CPU_SVIDDAT H_CPU_SVIDDAT 42

VCC_SENSE AJ35 VCCSENSE 42

VSS_SENSE AJ34 VSSSENSE 42

VCCIO_SENSE B10 VCCIO_SENSE 45

VSSIO_SENSE A10 VSSIO_SENSE 45

R801 100R2F-L1-GP-U

R802 100R2F-L1-GP-U

DY R803 Do Not Stuff

DY R805 Do Not Stuff

VCCIO_SENSE

VSSIO_SENSE

62.10040.821

2nd = 62.10040.771

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Title: CPU (VCC_CORE)

Size: Custom | Document Number: Enrico/Caruso 15 HR | Rev: X01

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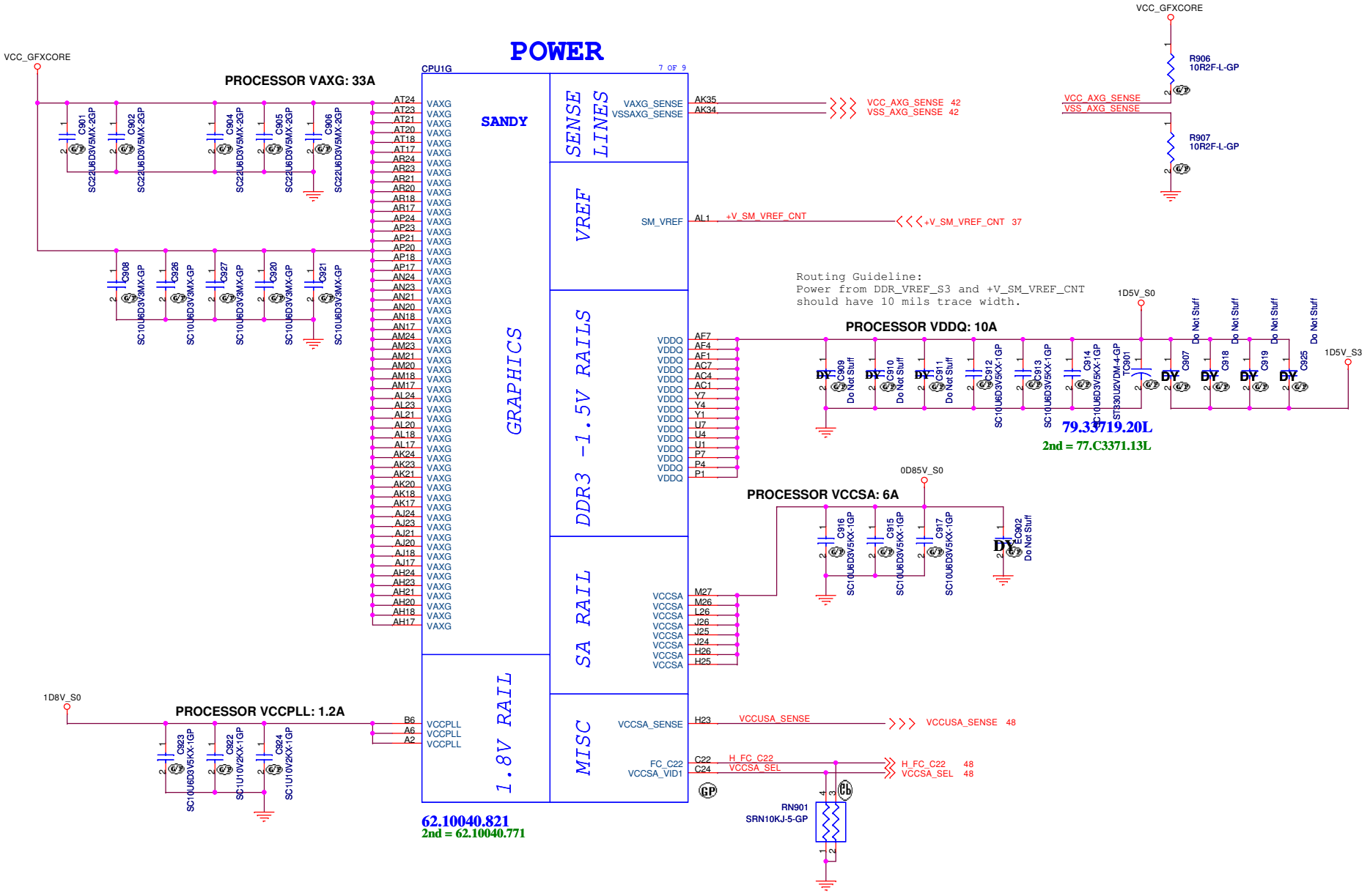
SSID = CPU

POWER



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Title: CPU (VCC_GFXCORE)

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

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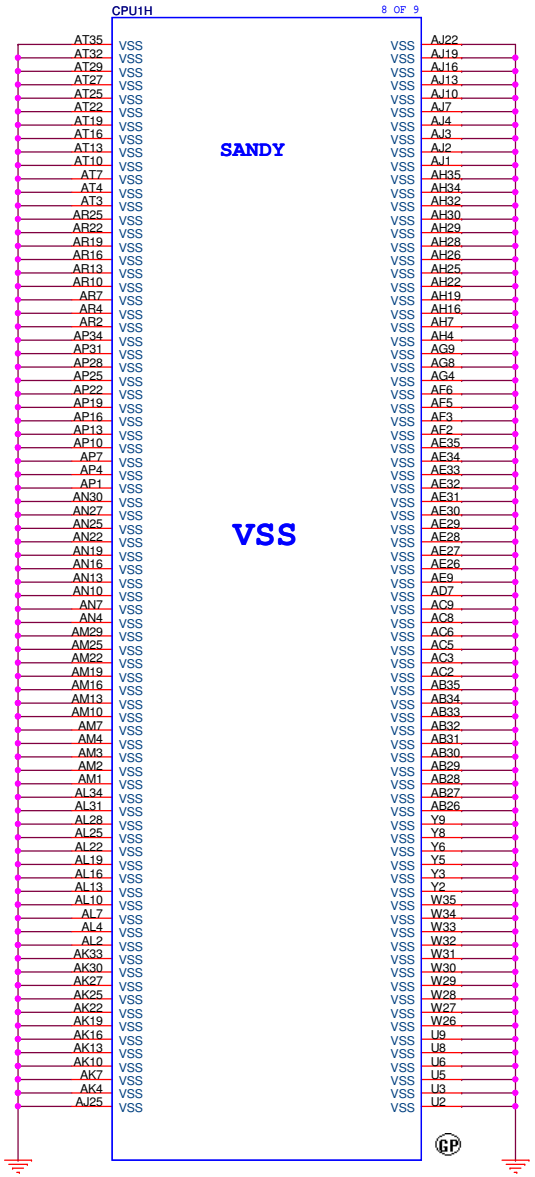
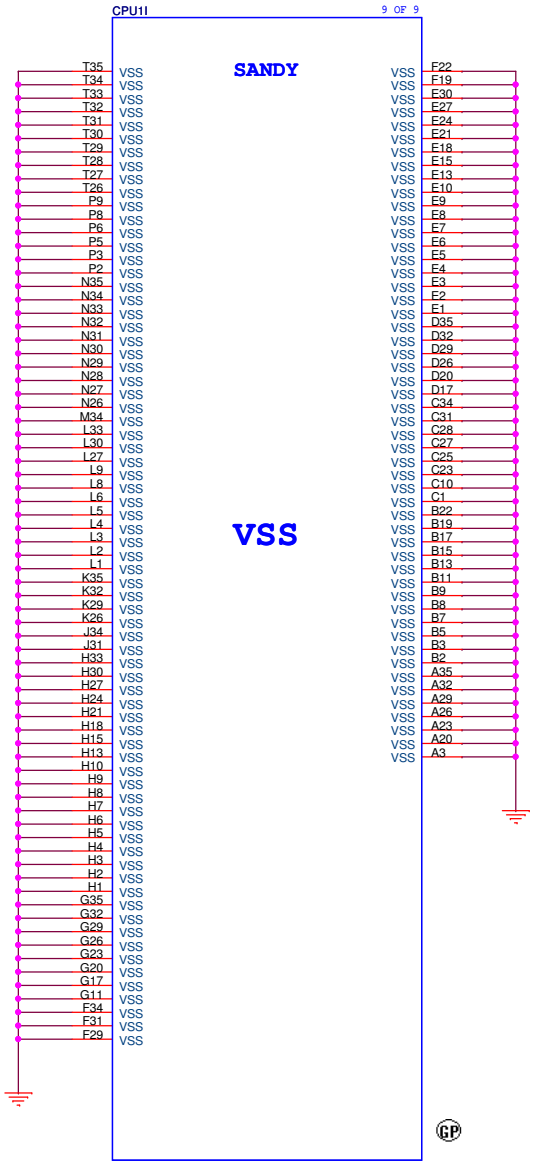
SSID = CPU



62.10040.821

2nd = 62.10040.771



62.10040.821

2nd = 62.10040.771

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Title: CPU (VSS)

Size	Document Number	Rev
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SSID = MEMORY

DM2

DDR_VREF_S3
X02-20110414
R1405
Do Not Stuff
M_VREF_CA_DIMM1
C1423 SCD1U10V2KX-5GP
C1425 DY Do Not Stuff
C1424 SCD1U10V2KX-5GP

DDR_VREF_S3
X02-20110414
R1404
Do Not Stuff
M_VREF_DQ_DIMM1
C1411 SCD1U10V2KX-5GP
C1412 DY Do Not Stuff
C1413 SCD1U10V2KX-5GP

0D75V_S0
Place these caps close to VTT1 and VTT2.
C1419 SC1U6D3V2KX-GP
C1420 DY Do Not Stuff
C1421 SC1U6D3V2KX-GP
C1422 DY Do Not Stuff
C1418 DY Do Not Stuff

M_B_A[15:0] 6
6 M_B_BS2
6 M_B_BS0
6 M_B_BS1
6 M_B_DQ[63:0]
M_B_DQS#[7:0] 6
M_B_DQS[7:0] 6
6 M_B_DIM0_ODT0
6 M_B_DIM0_ODT1
M_VREF_CA_DIMM1
M_VREF_DQ_DIMM1
15,37 DDR3_DRAMRST#
0D75V_S0

M_B_A0	98	A0
M_B_A1	97	A1
M_B_A2	96	A2
M_B_A3	95	A3
M_B_A4	92	A4
M_B_A5	91	A5
M_B_A6	90	A6
M_B_A7	86	A7
M_B_A8	89	A8
M_B_A9	85	A9
M_B_A10	107	A10/AP
M_B_A11	84	A11
M_B_A12	83	A12
M_B_A13	119	A13
M_B_A14	80	A14
M_B_A15	78	A15
	79	A16/BA2
	109	BA0
	108	BA1
M_B_DQ0	5	DQ0
M_B_DQ1	7	DQ1
M_B_DQ2	15	DQ2
M_B_DQ3	17	DQ3
M_B_DQ4	4	DQ4
M_B_DQ5	6	DQ5
M_B_DQ6	16	DQ6
M_B_DQ7	18	DQ7
M_B_DQ8	21	DQ8
M_B_DQ9	23	DQ9
M_B_DQ10	33	DQ10
M_B_DQ11	35	DQ11
M_B_DQ12	22	DQ12
M_B_DQ13	24	DQ13
M_B_DQ14	34	DQ14
M_B_DQ15	36	DQ15
M_B_DQ16	39	DQ16
M_B_DQ17	41	DQ17
M_B_DQ18	51	DQ18
M_B_DQ19	53	DQ19
M_B_DQ20	40	DQ20
M_B_DQ21	42	DQ21
M_B_DQ22	50	DQ22
M_B_DQ23	52	DQ23
M_B_DQ24	57	DQ24
M_B_DQ25	59	DQ25
M_B_DQ26	67	DQ26
M_B_DQ27	69	DQ27
M_B_DQ28	56	DQ28
M_B_DQ29	58	DQ29
M_B_DQ30	68	DQ30
M_B_DQ31	70	DQ31
M_B_DQ32	129	DQ32
M_B_DQ33	131	DQ33
M_B_DQ34	141	DQ34
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M_B_DQ37	132	DQ37
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M_B_DQ39	142	DQ39
M_B_DQ40	147	DQ40
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M_B_DQ42	157	DQ42
M_B_DQ43	159	DQ43
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M_B_DQ54	174	DQ54
M_B_DQ55	176	DQ55
M_B_DQ56	181	DQ56
M_B_DQ57	183	DQ57
M_B_DQ58	191	DQ58
M_B_DQ59	193	DQ59
M_B_DQ60	180	DQ60
M_B_DQ61	182	DQ61
M_B_DQ62	192	DQ62
M_B_DQ63	194	DQ63
M_B_DQS#0	10	DQS0#
M_B_DQS#1	27	DQS1#
M_B_DQS#2	45	DQS2#
M_B_DQS#3	62	DQS3#
M_B_DQS#4	135	DQS4#
M_B_DQS#5	152	DQS5#
M_B_DQS#6	169	DQS6#
M_B_DQS#7	186	DQS7#
M_B_DQS0	12	DQS0
M_B_DQS1	29	DQS1
M_B_DQS2	47	DQS2
M_B_DQS3	64	DQS3
M_B_DQS4	137	DQS4
M_B_DQS5	154	DQS5
M_B_DQS6	171	DQS6
M_B_DQS7	188	DQS7
	116	ODT0
	120	ODT1
	126	VREF_CA
	1	VREF_DQ
	30	RESET#
	203	VTT1
	204	VTT2

NP1	NP1	
NP2	NP2	
RAS#	110	M_B_RAS# 6
WE#	113	M_B_WE# 6
CAS#	115	M_B_CAS# 6
CS0#	114	M_B_DIM0_CS#0 6
CS1#	121	M_B_DIM0_CS#1 6
CKE0	73	M_B_DIM0_CKE0 6
CKE1	74	M_B_DIM0_CKE1 6
CK0	101	M_B_DIM0_CLK_DDR0 6
CK0#	103	M_B_DIM0_CLK_DDR#0 6
CK1	102	M_B_DIM0_CLK_DDR1 6
CK1#	104	M_B_DIM0_CLK_DDR#1 6
DM0	11	
DM1	28	
DM2	46	
DM3	63	
DM4	136	
DM5	153	
DM6	170	
DM7	187	
SDA	200	PCH_SMBDATA 15,20,65
SCL	202	PCH_SMBCLK 15,20,65
EVENT#	198	TS#_DIMM0_1 15
VDDSPD	199	
SA0	197	SA0_DIM1
SA1	201	SA1_DIM1
NC#1	77	
NC#2	122	
NC#/TEST	125	
VDD1	75	
VDD2	76	
VDD3	81	
VDD4	82	
VDD5	87	
VDD6	88	
VDD7	93	
VDD8	94	
VDD9	99	
VDD10	100	
VDD11	105	
VDD12	106	
VDD13	111	
VDD14	112	
VDD15	117	
VDD16	118	
VDD17	123	
VDD18	124	
VSS	2	
VSS	3	
VSS	8	
VSS	9	
VSS	13	
VSS	14	
VSS	19	
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VSS	25	
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VSS	161	
VSS	162	
VSS	167	
VSS	168	
VSS	172	
VSS	173	
VSS	178	
VSS	179	
VSS	184	
VSS	185	
VSS	189	
VSS	190	
VSS	195	
VSS	196	
VSS	205	
VSS	206	

DDR3-204P-43-GP
62.10017.N71

3D3V_S0
R1402 10KR2J-3-GP
SA1_DIM1
SA0_DIM1
R1401 10KR2J-3-GP

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT
3D3V_S0
TS#_DIMM0_1
R1403 10KR2J-3-GP

3D3V_S0
C1401 SCD1U10V2KX-5GP
C1402 DY Do Not Stuff

1D5V_S3

SODIMM A DECOUPLING
1D5V_S3
TC1401 Do Not Stuff
C1403 SC10U6D3V5KX-1GP
C1404 SC10U6D3V5KX-1GP
C1405 DY Do Not Stuff
C1406 SC10U6D3V5KX-1GP
C1407 DY Do Not Stuff
C1408 DY Do Not Stuff
C1409 SC10U6D3V5KX-1GP
C1410 DY Do Not Stuff

Layout Note:
Place these Caps near SO-DIMMA.
C1414 SCD1U10V2KX-5GP
C1415 SCD1U10V2KX-5GP
C1416 SC1U6D3V2KX-GP
C1417 SC1U6D3V2KX-GP

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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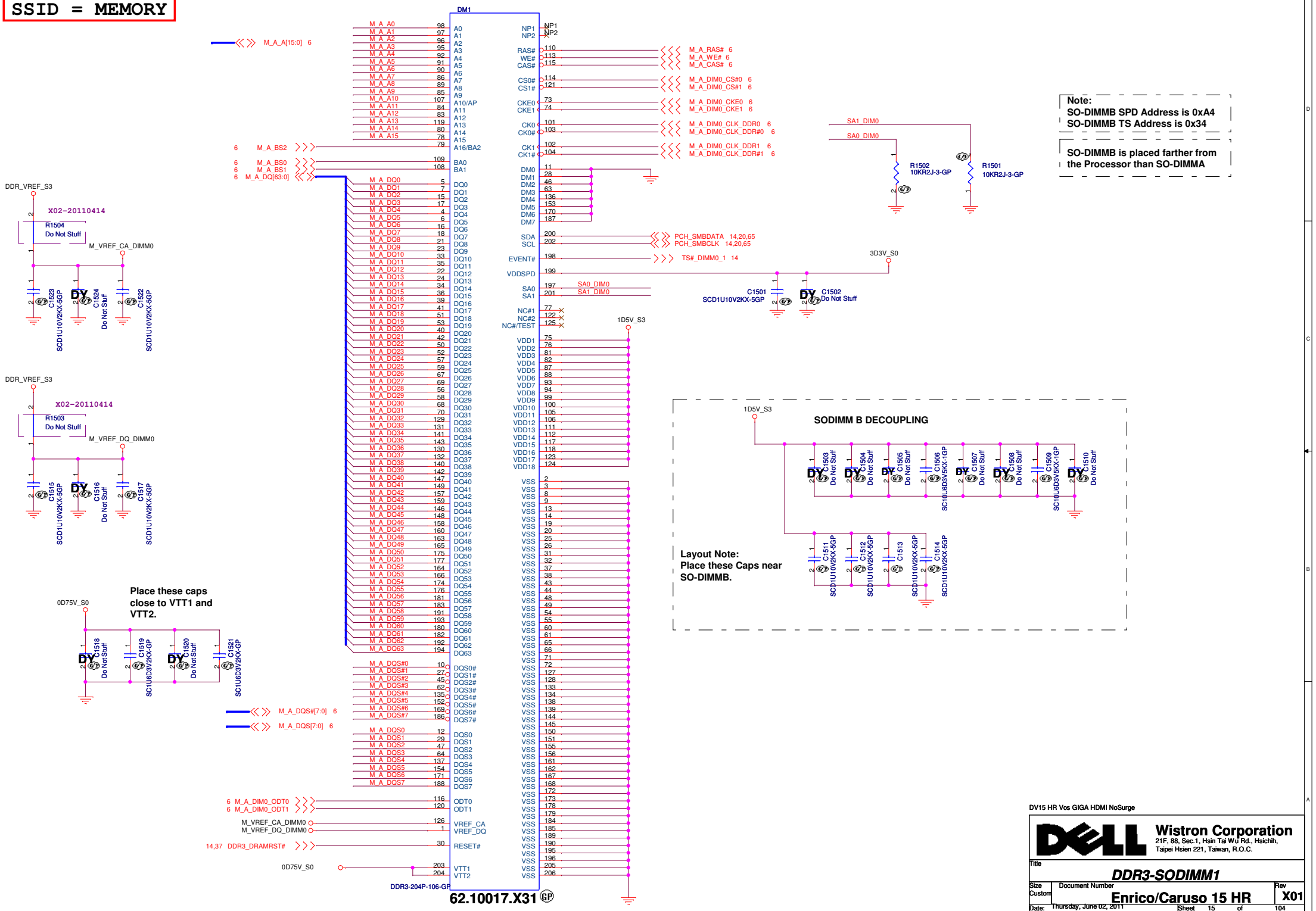
Title: DDR3-SODIMM2
Size: Custom
Document Number: Enrico/Caruso 15 HR
Rev: X01
Date: Thursday, June 02, 2011
Sheet 14 of 104

SSID = MEMORY



DV15 HR Vos GIGA HDMI NoSurge

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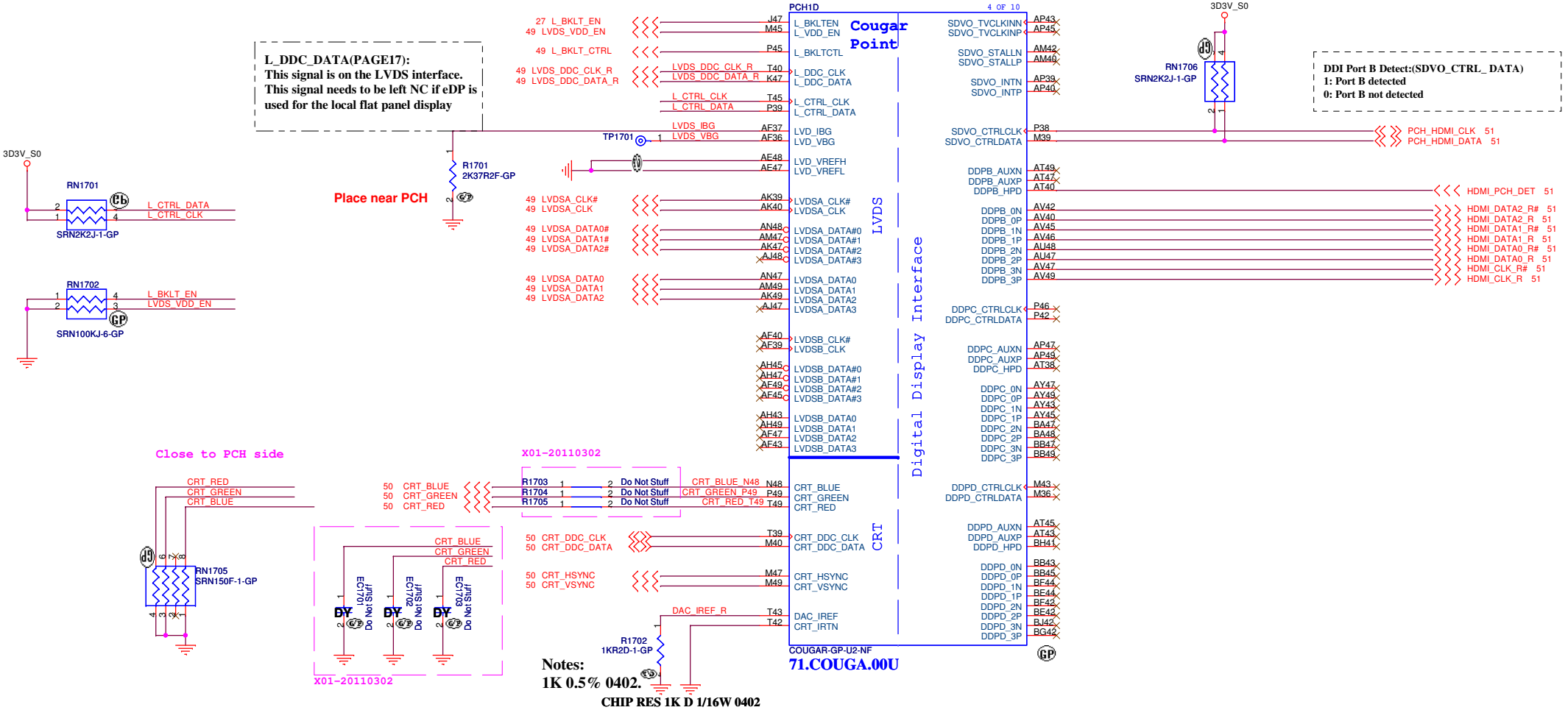
Title: DDR3-SODIMM1

Size	Document Number	Rev
Custom	Enrico/Caruso 15 HR	X01

Date: Thursday, June 02, 2011 Sheet 15 of 104



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
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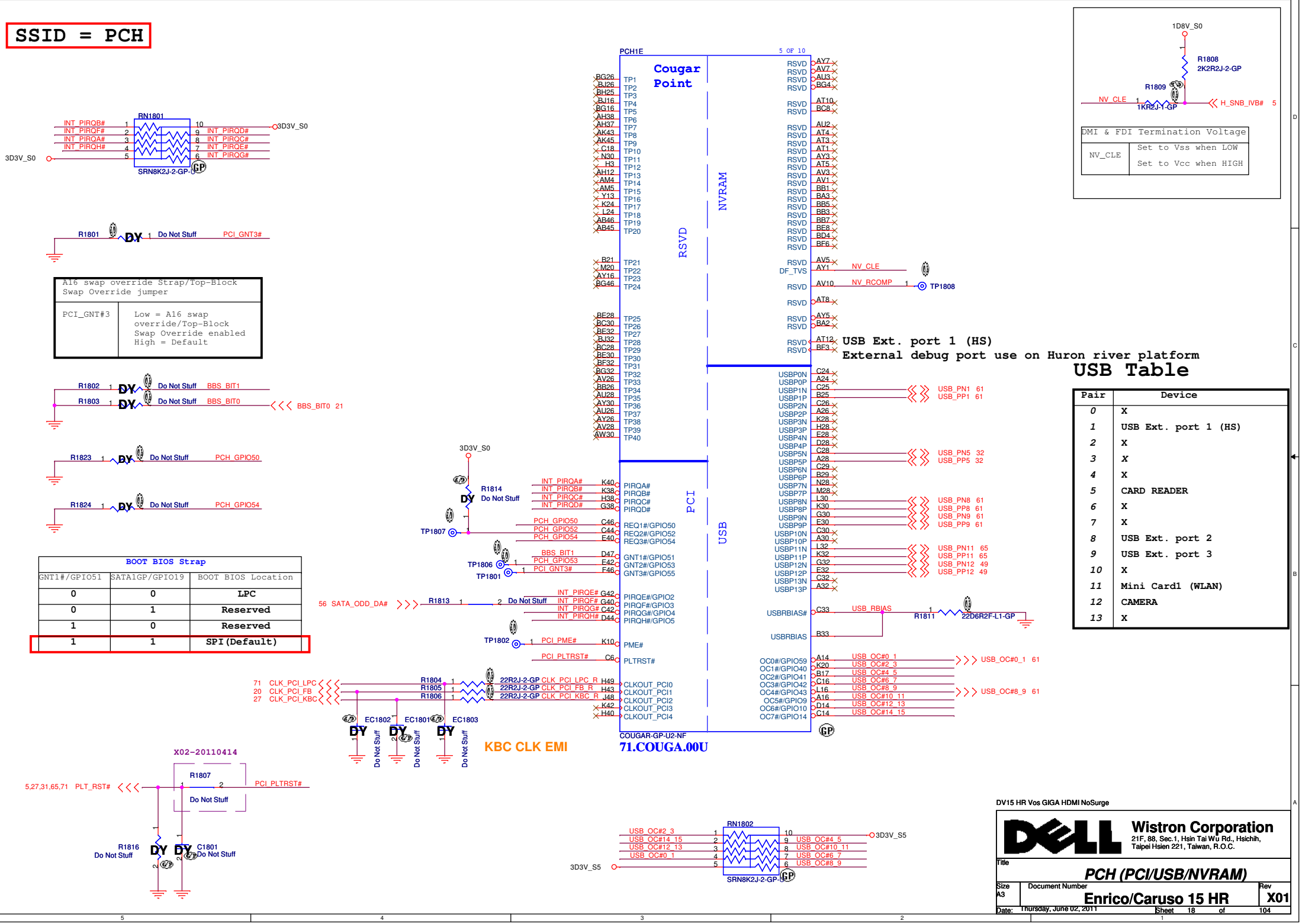
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

Date: Thursday, June 02, 2011 Sheet 17 of 104

SSID = PCH



USB Table

Pair	Device
0	X
1	USB Ext. port 1 (HS)
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
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Title: PCH (PCI/USB/NVRAM)

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

Date: Thursday, June 02, 2011 Sheet 18 of 104

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

PCH1C — 3 OF 10 — Cougar Point

DMI: DMI0RXN, DMI1RXN, DMI2RXN, DMI3RXN, DMI0RXP, DMI1RXP, DMI2RXP, DMI3RXP, DMI0TXN, DMI1TXN, DMI2TXN, DMI3TXN, DMI0TXP, DMI1TXP, DMI2TXP, DMI3TXP

FDI: FDI_RXN0–7, FDI_RXP0–7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

System Power Management: DSWVRMEN, DPWROK, WAKE#, CLKRUN#/GPIO32, SUS_STAT#/GPIO61, SUSCLK/GPIO62, SLP_S5#/GPIO63, SLP_S4#, SLP_S3#, SLP_A#, SLP_SUS#, PMSYNCH, SLP_LAN#/GPIO29, SUSACK#, SYS_RESET#, SYS_PWROK, PWROK, APWROK, DRAMPWROK, RSMRST#, SUSWARN#/SUSPWRDNACK/GPIO30, PWRBTN#, ACPRESENT/GPIO31, BATLOW#/GPIO72, RI#

COUGAR-GP-U2-NF

71.COUGA.00U

S0_PWR_GOOD after PM_SLP_S3# delay 150 ms

DSWODVREN – On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

DV15 HR Vos GIGA HDMI NoSurge

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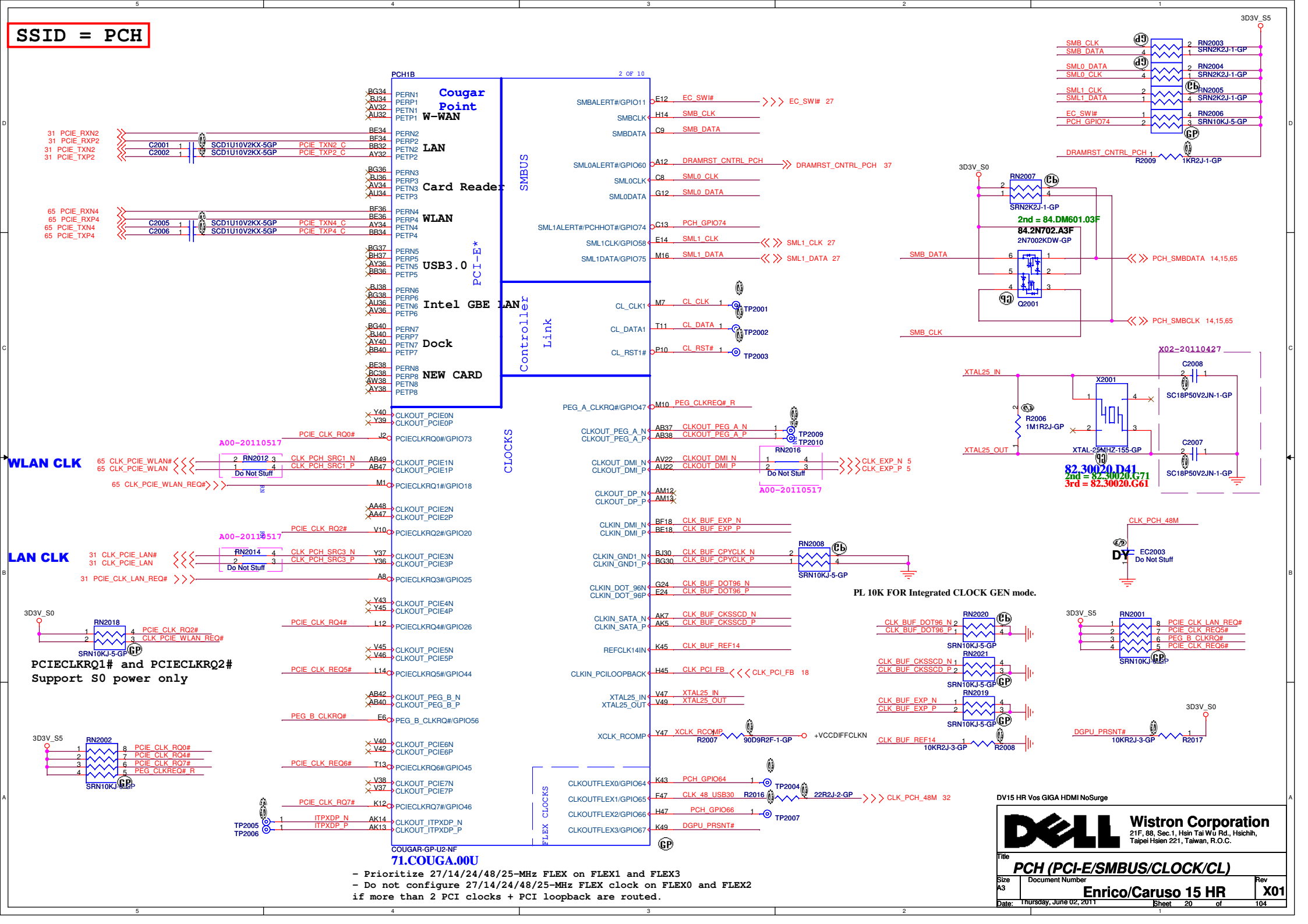
Title: **PCH (DM I/FDI/PM)**

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

Date: Thursday, June 02, 2011 Sheet 19 of 104

SSID = PCH


PCH1B
2 OF 10
Cougar Point
W-WAN
LAN
Card Reader
WLAN
USB3.0
Intel GBE LAN
Dock
NEW CARD
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGAR-GP-U2-NF
71.COUGA.00U
WLAN CLK
LAN CLK
PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only
PL 10K FOR Integrated CLOCK GEN mode.
- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2
if more than 2 PCI clocks + PCI loopback are routed.
DV15 HR Vos GIGA HDMI NoSurge
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (PCI-E/SMBUS/CLOCK/CL)
Enrico/Caruso 15 HR
X01
Thursday, June 02, 2011
Sheet 20 of 104

SSID = PCH

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V High = 1.5V (Default)

COUGAR-GP-U2-NF
71.COUGA.00U

DV15 HR Vos GIGA HDMI NoSurge

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Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

Date: Thursday, June 02, 2011 Sheet 21 of 104

SSID = PCH

3D3V_S0 — R2202 1 — DY — Do Not Stuff — SATA_ODD_PRSNT#

3D3V_S0 — RN2203 SRN10KJ-5-GP — H_A20GATE, H_RCIN#

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

3D3V_S0 — R2220 — DY — Do Not Stuff — PCH_GPIO48

3D3V_S5 — R2224 — 10KR2J-3-GP — PCH_GPIO12

3D3V_S0 — R2221 — DY — Do Not Stuff — PCH_GPIO6

3D3V_S0 — R2222 — DY — Do Not Stuff — PCH_GPIO17

3D3V_S0 — RN2204 — PSW_CLR#, PCH_GPIO0 — SRN10KJ-5-GP

3D3V_S0 — RN2201 — EC_SMI#, EC_SCI#, MFG_MODE, PCH_TEMP_ALERT# — SRN10KJ-6-GP

3D3V_S5 — R2201 — 1KR2J-1-GP — PCH_GPIO15

3D3V_S0 — R2207 — DY — Do Not Stuff — FDI_OVRVLTG — R2208 10KR2J-3-GP

3D3V_S0 — R2209 — DY — Do Not Stuff — DMI_OVRVLTG — R2210 10KR2J-3-GP

ICC_EN# — R2211 — 1KR2J-1-GP

PLL ON DIE VR ENABLE

NOTE:This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN — DY — R2212 — Do Not Stuff

PCH1F — Cougar Point — 6 OF 10

GPIO:
- PCH_GPIO0 T7 BMBUSY#/GPIO0
- 27 EC_SMI# A42 TACH1/GPIO1
- PCH_GPIO6 H36 TACH2/GPIO6
- 27 EC_SCI# E38 TACH3/GPIO7
- ICC_EN# C10 GPIO8
- 60 PCH_GPIO12 C4 LAN_PHY_PWR_CTRL/GPIO12
- PCH_GPIO15 G2 GPIO15
- 56 SATA_ODD_PRSNT# — R2213 — Do Not Stuff — PCH_GPIO16 U2 SATA4GP/GPIO16
- PCH_GPIO17 D40 TACH0/GPIO17
- TP2210 PCH_GPIO22 T5 SCLOCK/GPIO22
- TP2216 PCH_GPIO24 E8 GPIO24/MEM_LED
- TP2203 PCH_GPIO27 E16 GPIO27
- PLL_ODVR_EN P8 GPIO28
- PSW_CLR# K1 STP_PCI#/GPIO34
- TP2212 PCH_GPIO35 K4 GPIO35
- DMI_OVRVLTG V8 SATA2GP/GPIO36
- FDI_OVRVLTG M5 SATA3GP/GPIO37
- MFG_MODE N2 SLOAD/GPIO38
- TP2215 PCH_GPIO39 M3 SDATAOUT0/GPIO39
- TP2214 PCH_GPIO48 V13 SDATAOUT1/GPIO48
- PCH_TEMP_ALERT# V3 SATA5GP/GPIO49
- D6 GPIO57

G2201 — Do Not Stuff

CPU/MISC:
- C40 TACH4/GPIO68 — SATA_ODD_PWRGT 56
- B41 TACH5/GPIO69 — UMA_DIS#
- C41 TACH6/GPIO70 — PCH_GPIO70 — TP2204
- A40 TACH7/GPIO71 — PCH_GPIO71 — TP2205
- P4 A20GATE — H_A20GATE 27
- AU16 PECI — H_PECI_R — R2203 — DY — Do Not Stuff — H_PECI 5,27
- P5 RCIN# — H_RCIN# 27
- AY11 PROCPWRGD — H_CPUPWRGD 5,36
- AY10 THRMTRIP# — PCH_THERMTRIP_R — R2204 — 390R2J-1-GP — H_THERMTRIP# 5,36
- T14 INIT3_3V# — INIT3_3V# — TP2201
- AH8 TS_VSS1
- AK11 TS_VSS2
- AH10 TS_VSS3
- AK10 TS_VSS4 — TS_VSS — R2219 — Do Not Stuff
- P37 NC_1

NCTF:
- TP2206 PCH_NCTF_1 A4 NCTF_VSS#A4
- A44 NCTF_VSS#A44
- A45 NCTF_VSS#A45
- A46 NCTF_VSS#A46
- A5 NCTF_VSS#A5
- A6 NCTF_VSS#A6
- B3 NCTF_VSS#B3
- B47 NCTF_VSS#B47
- BD1 NCTF_VSS#BD1
- BD49 NCTF_VSS#BD49
- TP2207 PCH_NCTF_2 BE1 NCTF_VSS#BE1
- TP2208 PCH_NCTF_3 BF49 NCTF_VSS#BE49
- BF1 NCTF_VSS#BF1
- TP2209 PCH_NCTF_4 BF49 NCTF_VSS#BF49

NCTF TEST PIN: A4,A44,A45,A46,A5,A6,B3,B47,BD1,BD49,BE1,BE49,BF1,BF49

- NCTF_VSS#BG2 BG2
- NCTF_VSS#BG48 BG48
- NCTF_VSS#BH3 BH3
- NCTF_VSS#BH47 BH47
- NCTF_VSS#BJ4 BJ4
- NCTF_VSS#BJ44 BJ44
- NCTF_VSS#BJ45 BJ45
- NCTF_VSS#BJ46 BJ46
- NCTF_VSS#BJ5 BJ5
- NCTF_VSS#BJ6 BJ6
- NCTF_VSS#C2 C2
- NCTF_VSS#C48 C48
- NCTF_VSS#D1 D1
- NCTF_VSS#D49 D49
- NCTF_VSS#E1 E1
- NCTF_VSS#E49 E49
- NCTF_VSS#F1 F1
- NCTF_VSS#F49 F49

NCTF TEST PIN: BG2,BG48,BH3,BH47,BJ4,BJ44,BJ45,BJ46,BJ5,BJ6,C2,C48 D1,D49,E1,E49,F1,F49

COUGAR-GP-U2-NF

71.COUGA.00U

3D3V_S0 — R2223 — 10KR2J-3-GP — UMA_DIS#

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

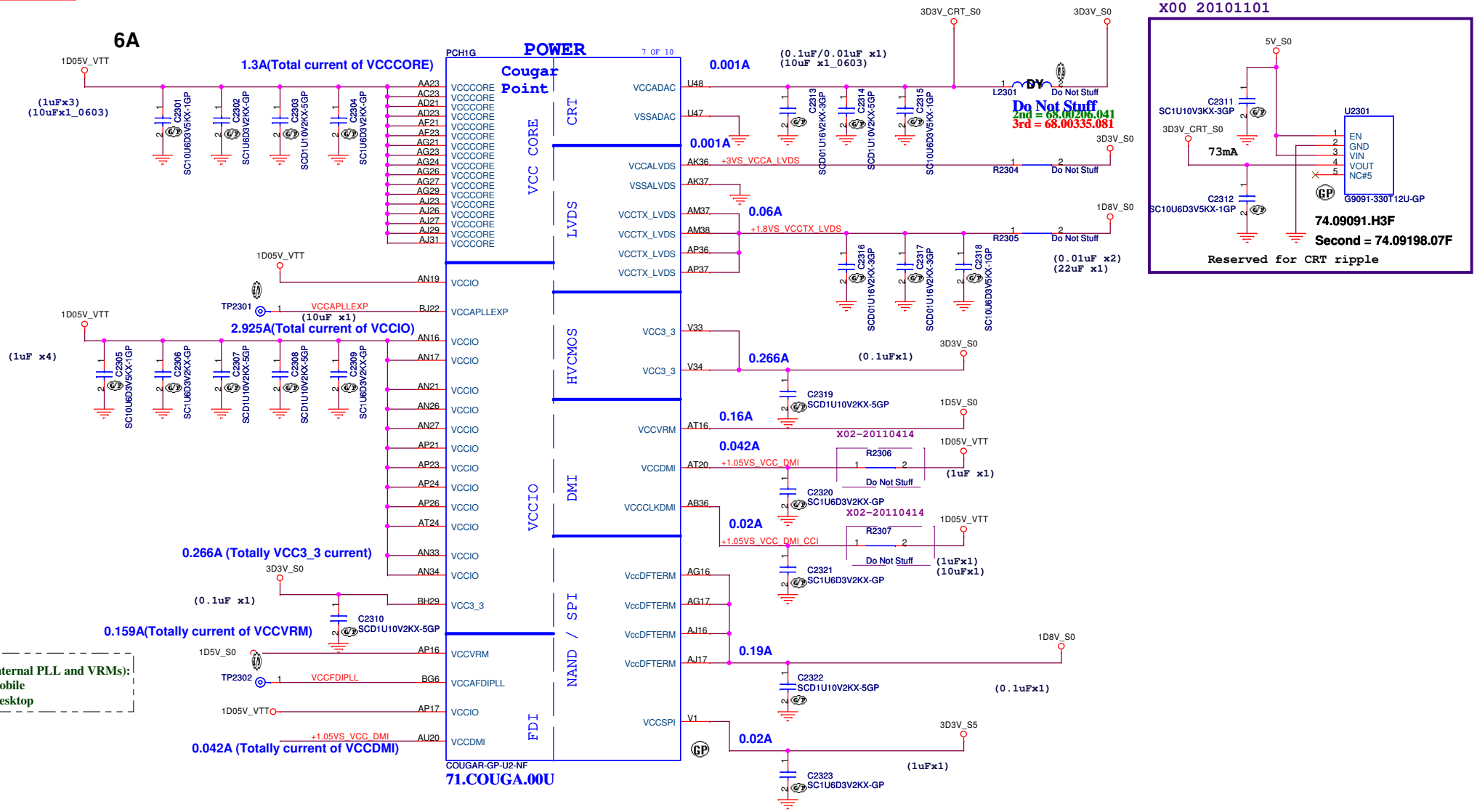
Title: **PCH (GPIO/CPU)**

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

Date: Thursday, June 02, 2011 Sheet 22 of 104

SSID = PCH

6A



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (POWER1)**

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

Date: Thursday, June 02, 2011 Sheet 23 of 104

SSID = PCH

POWER

PCH1J — 10 OF 10 — Cougar Point

Clock and Miscellaneous

TP2401	VCCACLK	AD49
0.002A		
3D3V_S5 (0.1uFx1)	VCCDSW3_3	T16
Do Not Stuff TP2405	DCPSUSBYP	V12
+V3.3S_VCC_CLKF33	VCC3_3	T38
TP2404 +VCCAPLL_CPY_PCH	VCCAPLLDMI2	BH23
1D05V_VTT (10uFx1)	VCCIO	AL29
TP2402 +VCCSUS1	DCPSUS	AL24

USB

VCCIO	N26	1D05V_VTT (1uFx1) C2423 SCD1U10V2KX-5GP
VCCIO	P26	
VCCIO	P28	
VCCIO	T27	
VCCIO	T29	
VCCSUS3_3	T23	0.097A (Totally current of VCCSUS3_3) 3D3V_S5 (0.1uFx1) C2424 SCD1U10V2KX-5GP
VCCSUS3_3	T24	
VCCSUS3_3	V23	
VCCSUS3_3	V24	3D3V_S5 (0.1uFx1) C2425 SCD1U10V2KX-5GP
VCCSUS3_3	P24	
VCCIO	T26	1D05V_VTT
V5REF_SUS	M26	+5VA_PCH_VCC5REFSUS 0.001A
DCPSUS	AN23	+VCCA_USBSUS TP2403
VCCSUS3_3	AN24	3D3V_S5 DY C2437 Do Not Stuff

3D3V_S5 — D2401 CH751H-40PT-GP 83.R0304.A8F 2nd = 83.R2004.B8F — 5V_S5
R2408 10R2J-2-GP (0.1uFx1) C2426 SCD1U10V2KX-5GP

3D3V_S0 — D2402 CH751H-40PT-GP 83.R0304.A8F 2nd = 83.R2004.B8F — 5V_S0
R2407 10R2J-2-GP (1uFx1) C2427 SC1U10V2KX-1GP

1D05V_VTT — 1.01A (Total current of VCCASW) (22uFx2_0603) (1uFx3)
C2403 SC10U6D3V5KX-1GP, C2404 SC10U6D3V5KX-1GP, C2406 SCD1U10V2KX-5GP, C2407 SC1U6D3V2KX-GP, C2408 SCD1U10V2KX-5GP

PCI/GPIO/LPC

VCCASW	AA19	
VCCASW	AA21	
VCCASW	AA24	
VCCASW	AA26	
VCCASW	AA27	
VCCASW	AA29	
VCCASW	AA31	
VCCASW	AC26	
VCCASW	AC27	
VCCASW	AC29	
VCCASW	AC31	
VCCASW	AD29	
VCCASW	AD31	
VCCASW	W21	
VCCASW	W23	
VCCASW	W24	
VCCASW	W26	
VCCASW	W29	
VCCASW	W31	
VCCASW	W33	
V5REF	P34	+5VS_PCH_VCC5REF 0.001A
VCCSUS3_3	N20	3D3V_S5 (1uFx1) C2428 SC1U6D3V2KX-GP
VCCSUS3_3	N22	
VCCSUS3_3	P20	
VCCSUS3_3	P22	
VCC3_3	AA16	3D3V_S0 (0.1uFx2) C2430 SCD1U10V2KX-5GP, C2431 SCD1U10V2KX-5GP
VCC3_3	W16	
VCC3_3	T34	

1D05V_VTT — 0.08A (1uFx1) (220uFx1)
L2402 IND-10UH-218-GP 68.10050.10Y 2nd = 68.1001E.10N — +1.05VS_VCCA_A_DPL — DY C2443 Do Not Stuff, C2409 SC1U6D3V2KX-GP

1D05V_VTT — 0.08A (1uFx1) (220uFx1)
L2403 IND-10UH-218-GP 68.10050.10Y 2nd = 68.1001E.10N — +1.05VS_VCCA_B_DPL — DY C2444 Do Not Stuff, C2410 SC1U6D3V2KX-GP

SATA

VCC3_3	AJ2	3D3V_S0 (0.1uFx1) C2429 SCD1U10V2KX-5GP
VCCIO	AF13	
VCCIO	AH13	1D05V_VTT (1uFx1)
VCCIO	AH14	
VCCIO	AF14	C2432 SC1U6D3V2KX-GP
VCCAPLLSATA	AK1	1D05V_VTT +V1.05S_VCCAPLL_SATA3 R2411 DY Do Not Stuff (10uFx1)
VCCVRM	AF11	1D05V_VTT DY C2434 Do Not Stuff
VCCIO	AC16	
VCCIO	AC17	1D05V_VTT (1uFx1) C2435 SCD1U10V2KX-5GP
VCCIO	AD17	

+VCCRTCEXT — 0.16A (Totally current of VCCVRM) — C2411 SCD1U10V2KX-5GP (0.1uFx1)
1D5V_S0 — DCPRTC N16, VCCVRM Y49

+1.05VS_VCCA_A_DPL — VCCADPLLA BD47
+1.05VS_VCCA_B_DPL — VCCADPLLB BF47

1D05V_VTT — X02-20110414 — Do Not Stuff R2404 — +VCCDIFFCLK — C2412 SC1U6D3V2KX-GP
1D05V_VTT — X02-20110414 — Do Not Stuff R2405 — +V1.05S_SSCVCC — C2413 SC1U6D3V2KX-GP

1D05V_VTT (1uFx1) R2406 Do Not Stuff — +VCCDIFFCLKN — +VCCDIFFCLK (1uFx1) — 0.055A
VCCIO, VCCDIFFCLKN AF17, VCCDIFFCLKN AF33, VCCDIFFCLKN AF34, VCCDIFFCLKN AG34
0.095A — C2414 SC1U6D3V2KX-GP — +V1.05S_SSCVCC (1uFx1) — VCCSSC AG33

(0.1uFx1) — C2415 SCD1U10V2KX-5GP — +VCCSST — DCPSST V16

(1uFx1) — TP2406 — DCPSUS — DCPSUS T17, DCPSUS V19

CPU

1D05V_VTT — 0.001A — (0.1uFx2) (4.7uFx1_0603) — C2417 SC4D7U6D3V3KX-GP, C2418 SCD1U10V2KX-5GP — V_PROC_IO BJ8

RTC

RTC_AUX_S5 — 6uA — (0.1uFx2) (1uFx1) — C2421 SCD1U10V2KX-5GP, C2422 SCD1U10V2KX-5GP — VCCRTC A22

COUGAR-GP-U2-NF
71.COUGA.00U

MISC

VCCASW	T21	1D05V_VTT
VCCASW	V21	
VCCASW	T19	

HDA

VCCSUSHDA P32 — 0.01A — +3VA_+1.5VA_HDA_IO (0.1uFx1) — C2433 SCD1U10V2KX-5GP

+3VA_+1.5VA_HDA_IO — R2409 Do Not Stuff — 3D3V_S5

DV15 HR Vos GIGA HDMI NoSurge

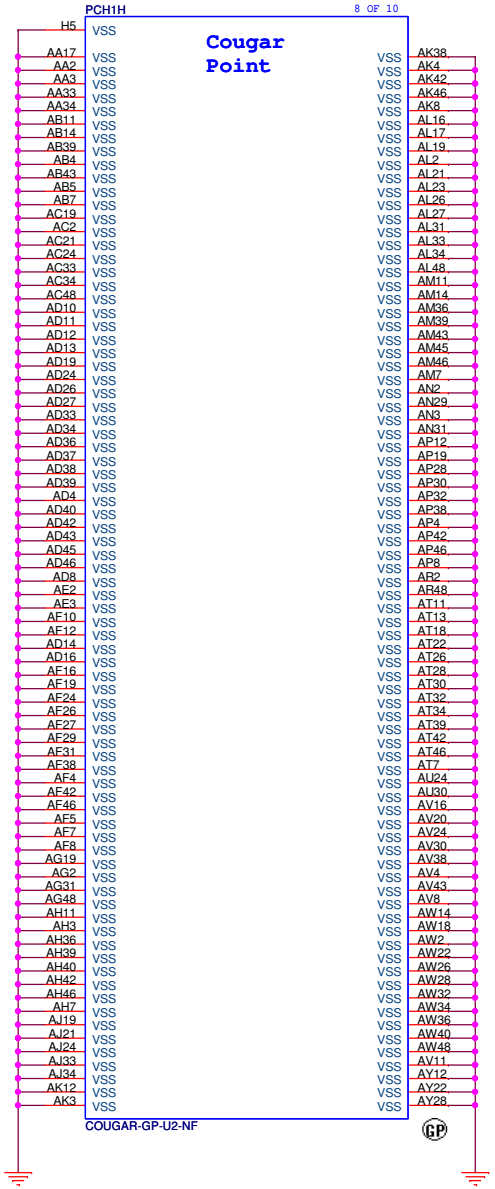
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

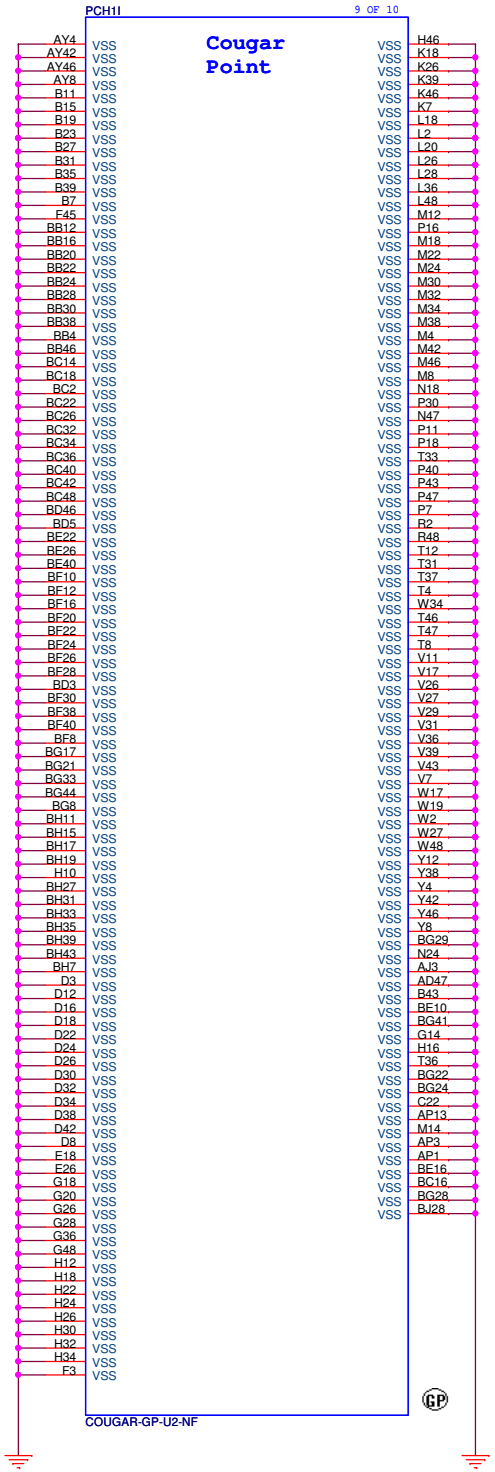
Title: PCH (POWER2)

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

Date: Thursday, June 02, 2011 Sheet 24 of 104

SSID = PCH





DV15 HR Vos GIGA HDMI NoSurge

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *PCH (VSS)*

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

Date: Thursday, June 02, 2011 Sheet 25 of 104

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DV14_UMA	100.0K	10.0K(64.10025.6DL)	3.0V
DV14_DIS_PX	100.0K	20.0K(64.20025.6DL)	2.75V
DV15_UMA with HDMI	100.0K	33.0K	2.48V
DV15_UMA without HDMI	100.0K	47.0K(64.47025.6DL)	2.24V
Reserved	100.0K	64.9K(64.64925.6DL)	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

C2712 Need very close to EC

NOTE:
Locate resistors R2736,R2719 and R2722 close to the NPCE795P.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

Need very close to EC

EC_GPIO47 High Active

PSL SOLUTION

10mW SOLUTION

VBACKUP

PSL_IN1

PSL_OUT

EC GPIO standard PH/PL

NOTES:
Please make sure there's no pull-down resistor on USB_PWR_EN#,AC_PRESENT,E51_TXD.

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE795

Size: A2 | Document Number: Enrico/Caruso 15 HR | Rev: X01

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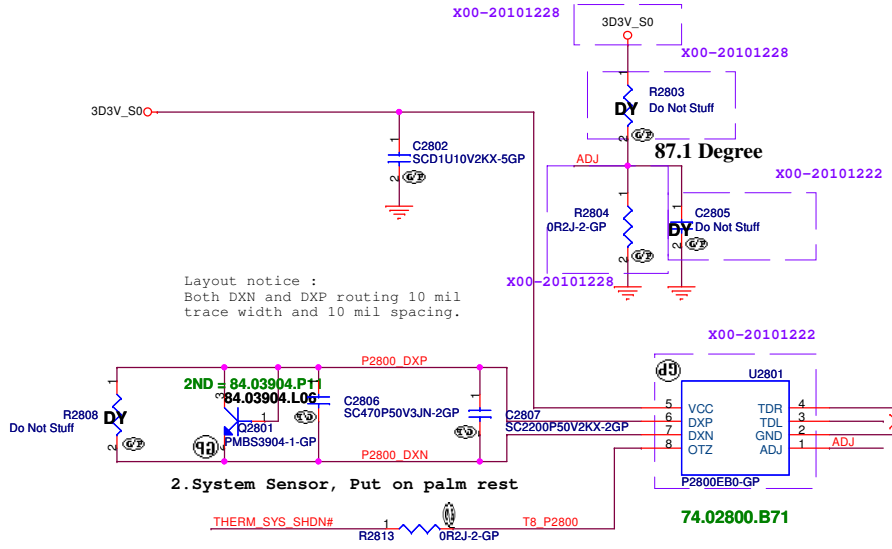
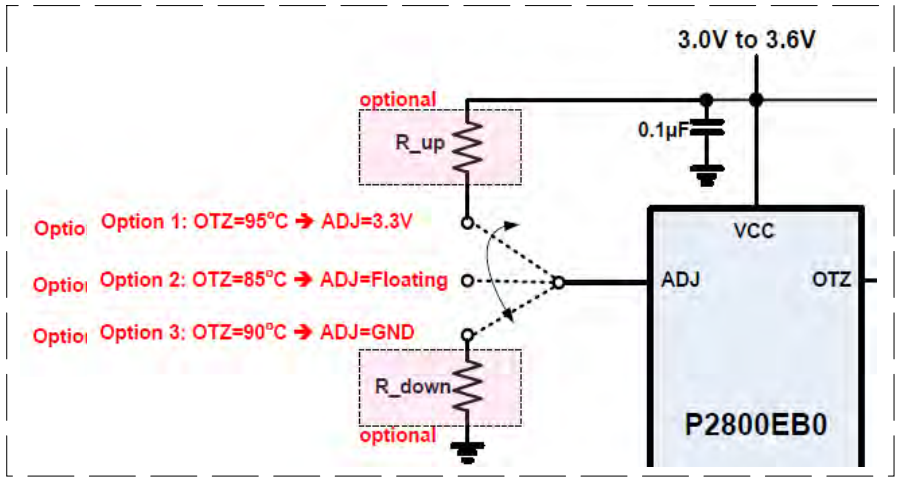
SSID = Thermal

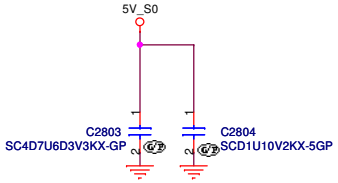
Thermal sensor P2800

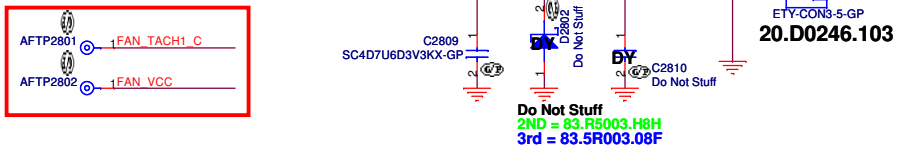


1.H/W T8 Shutdown

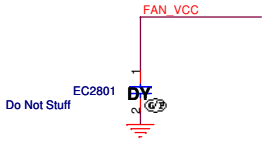


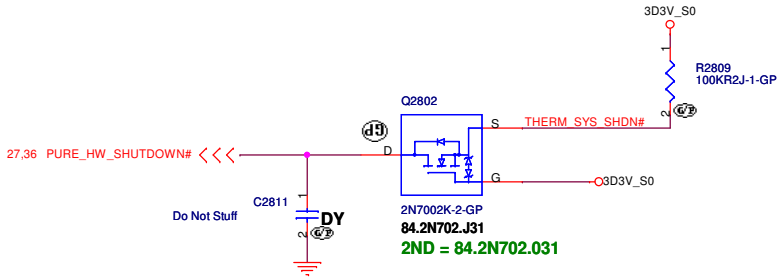
Fan controller G991

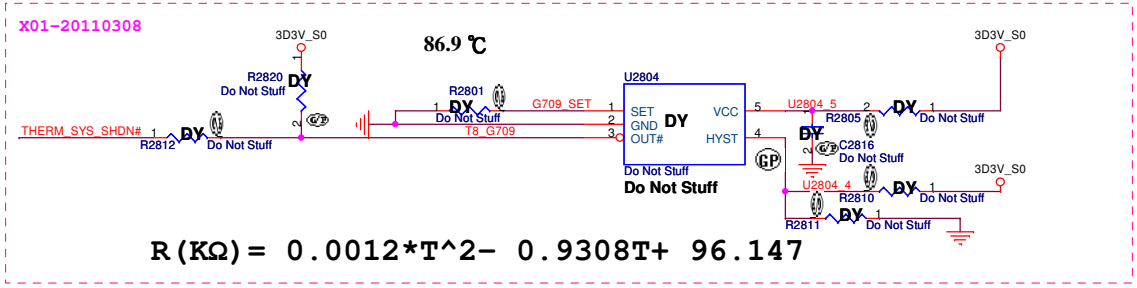




EMI/ESD







DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

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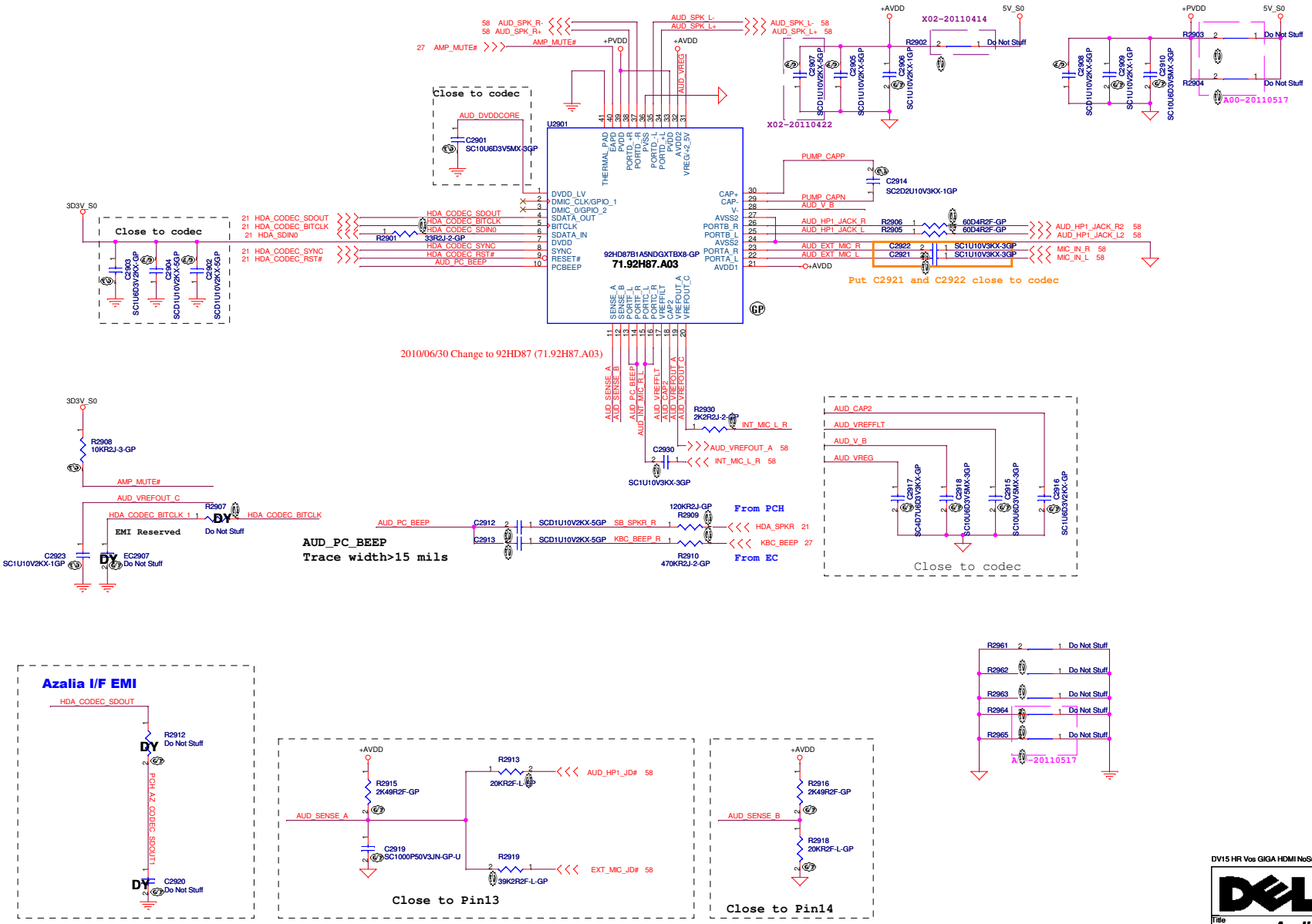
SSID = AUDIO



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD87B1

Size: Custom | Document Number: Enrico/Caruso 15 HR | Rev: X01

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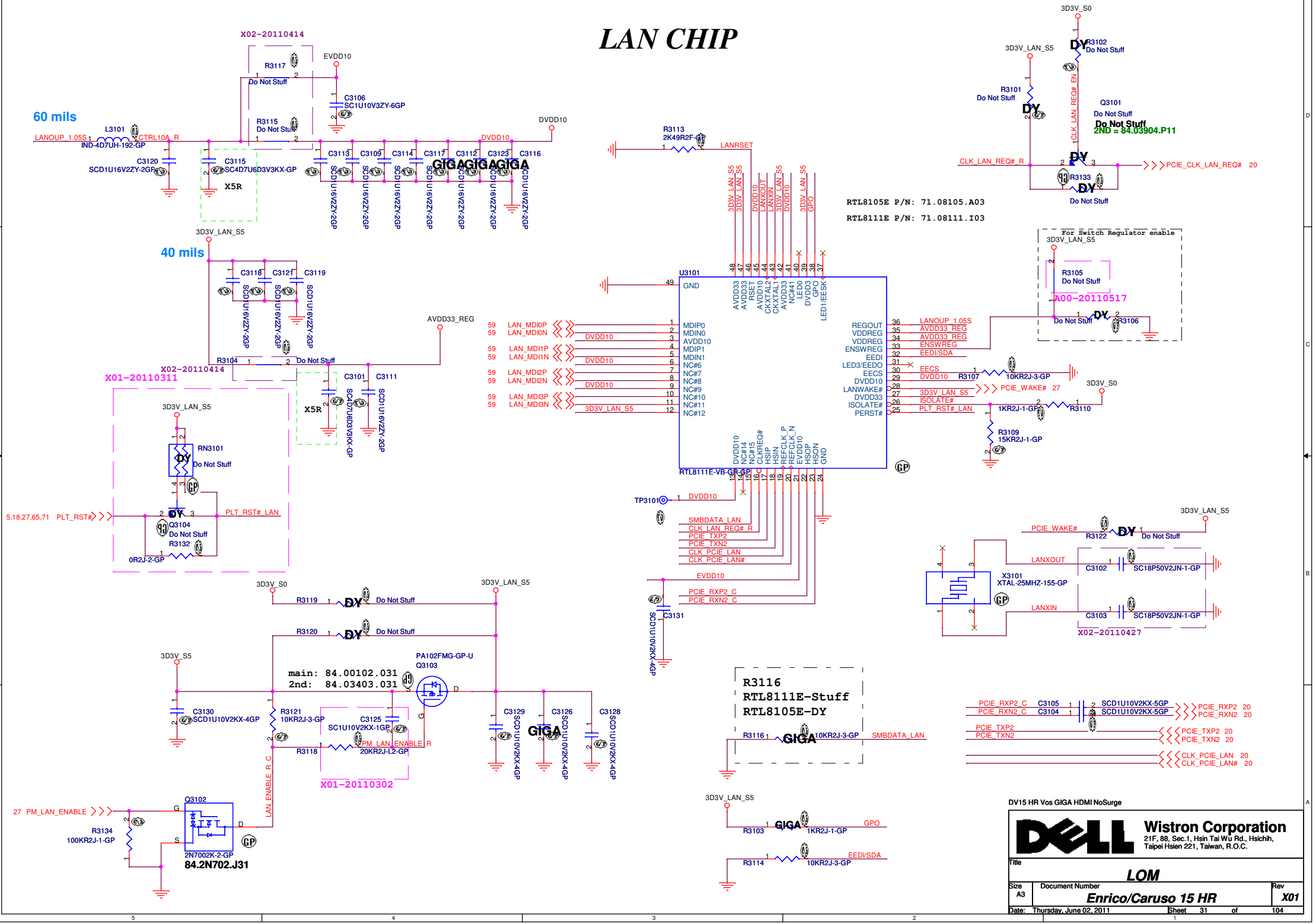
LAN CHIP

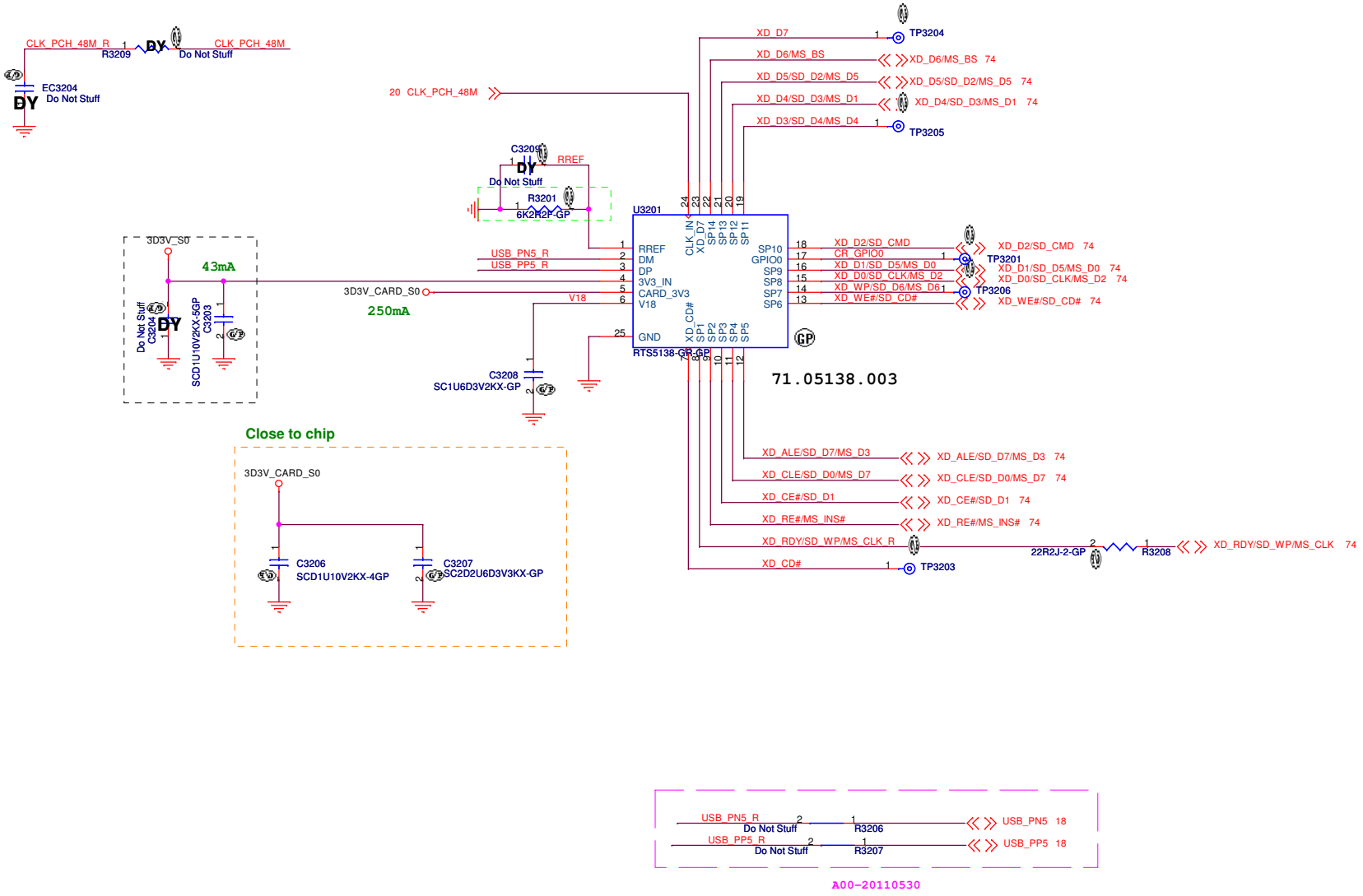


DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LOM**		
Size: A3	Document Number: **Enrico/Caruso 15 HR**	Rev: **X01**
Date: Thursday, June 02, 2011	Sheet 31 of 104	

SSID = SDIO



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138

Size	Document Number	Rev
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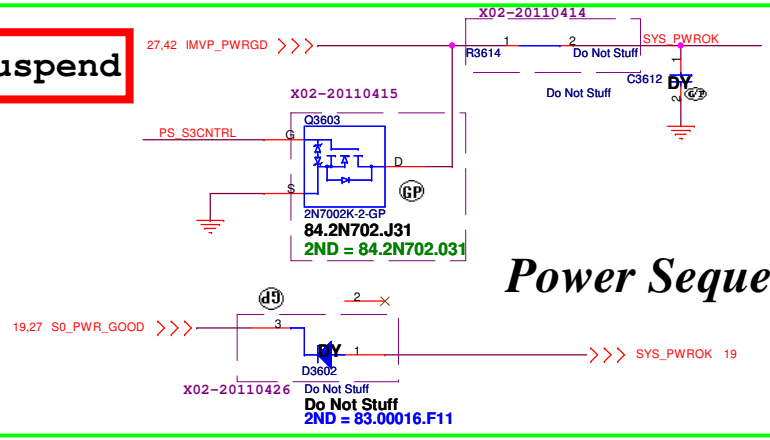
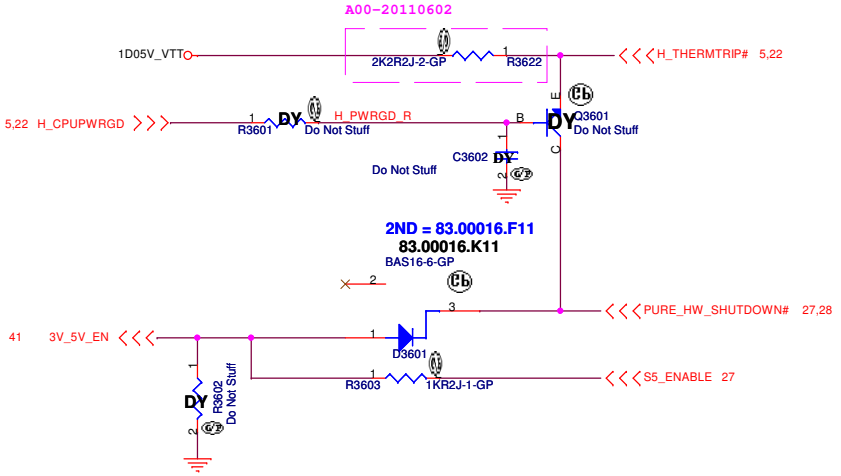
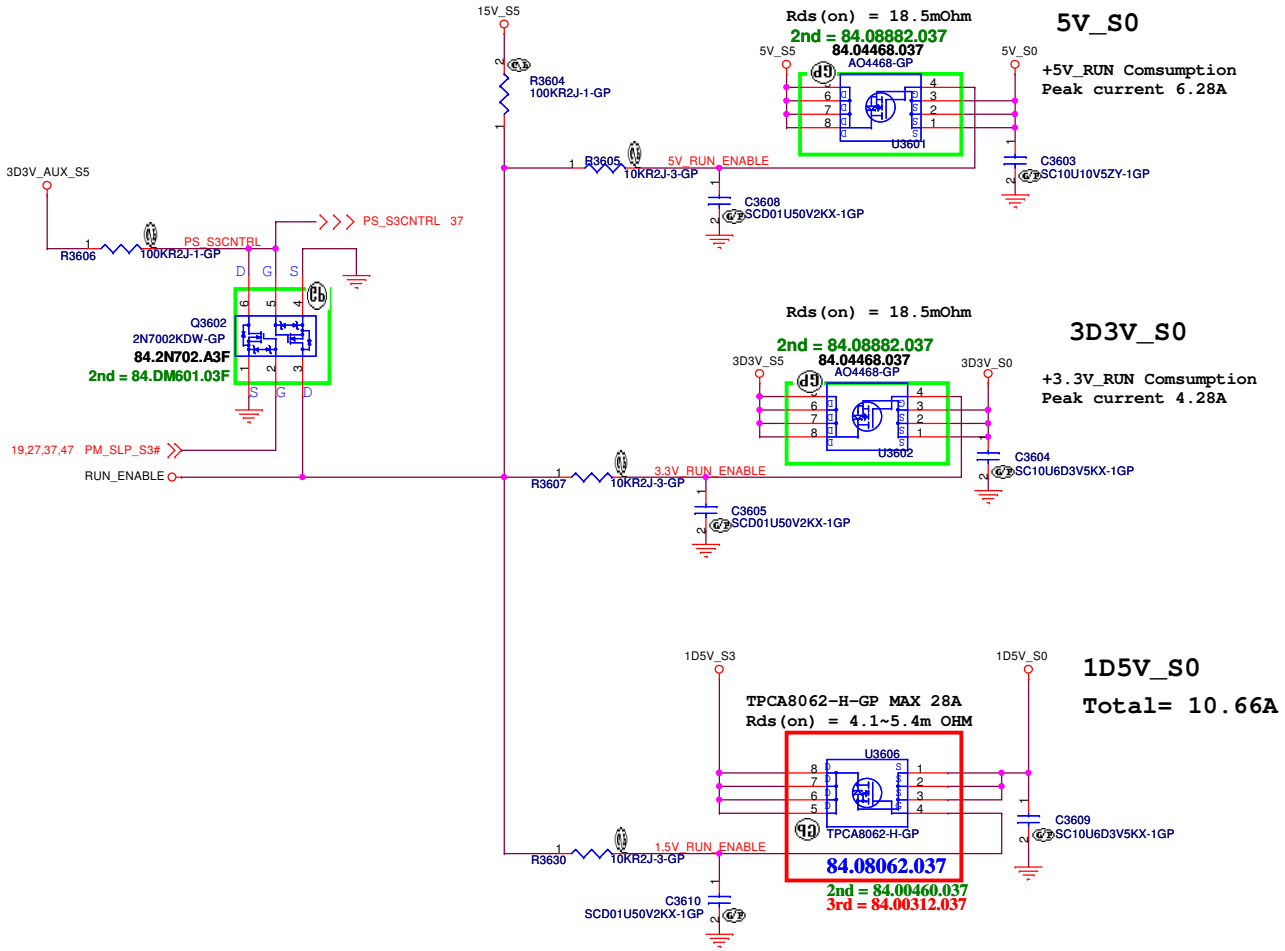
SSID = Reset.Suspend

Power Sequence





ROSA Run Power



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

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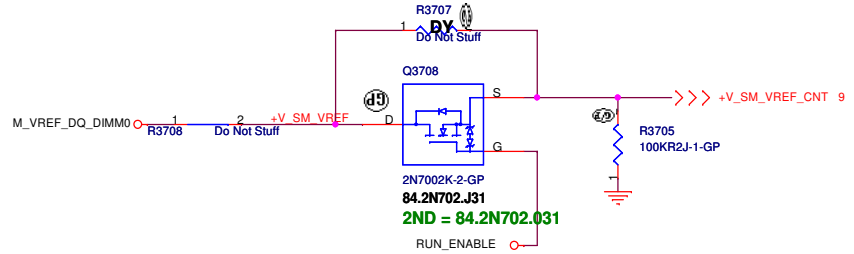
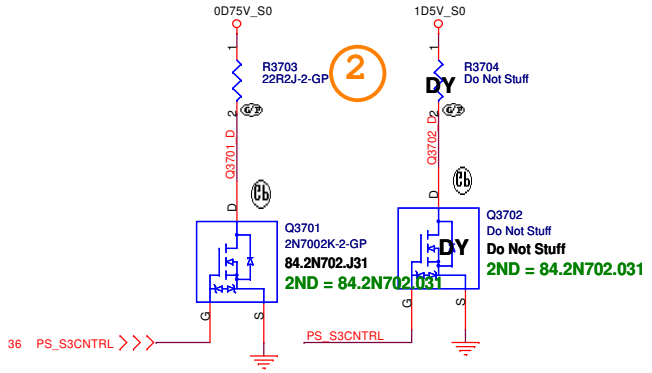
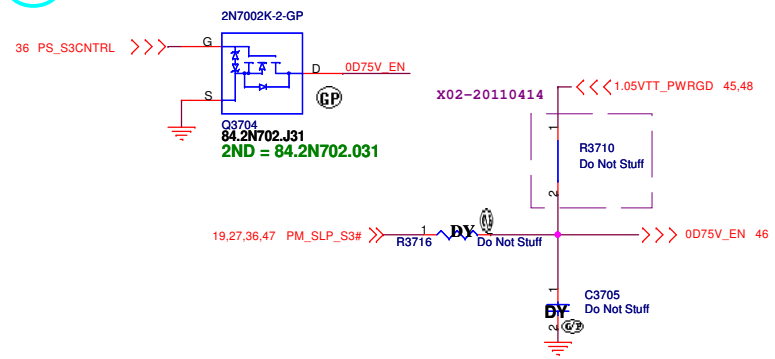
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



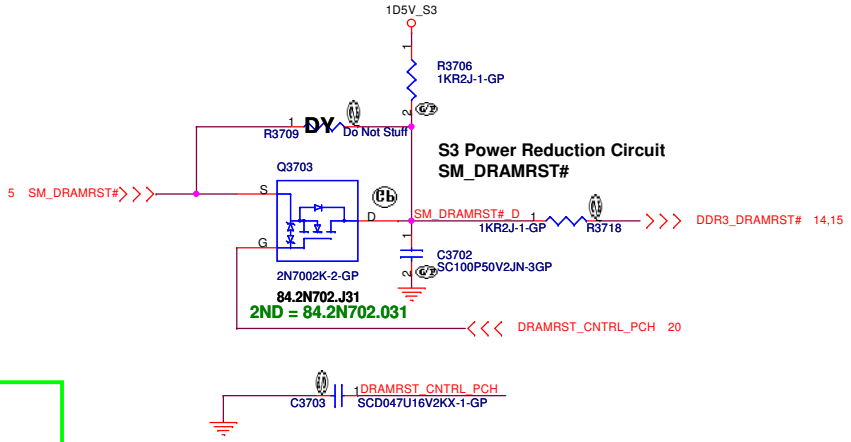
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



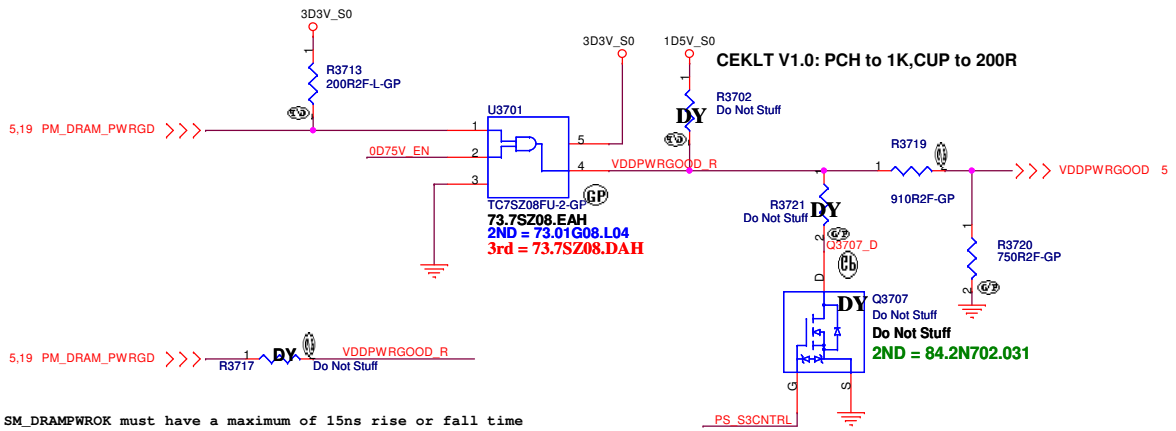
5 S3 Power Reduction



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

Size	Document Number	Rev
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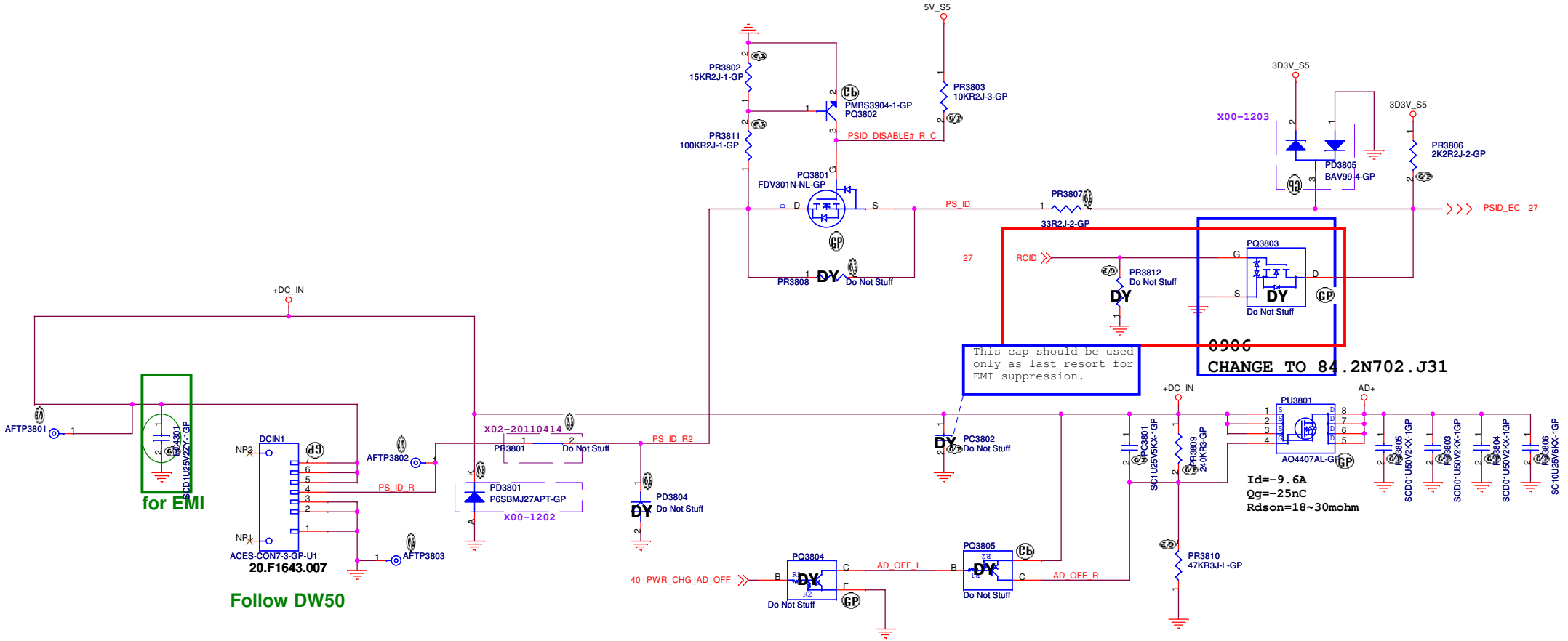
SSID = PWR.Support

DCin CONN



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
DCIN		
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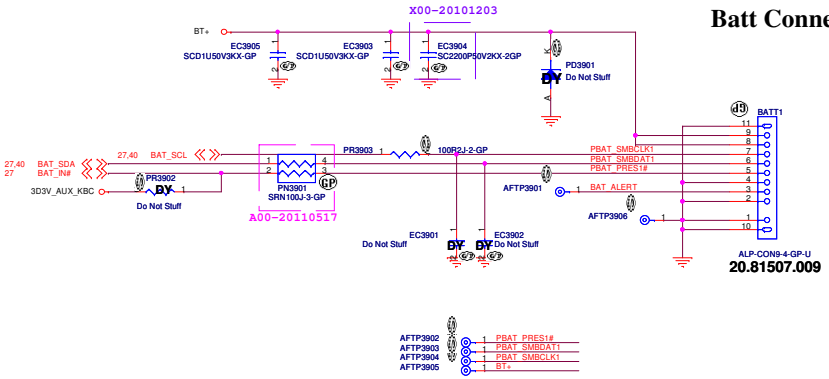
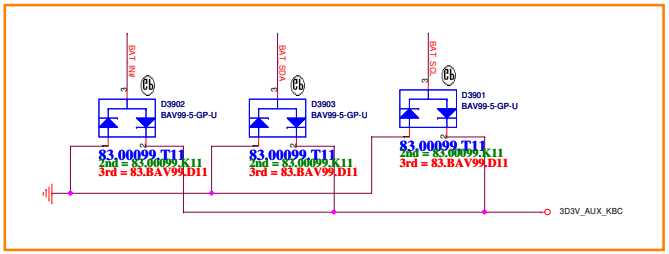
Batt Connecter



For actual location, need to be swap all pin

Close to Batt Connector



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

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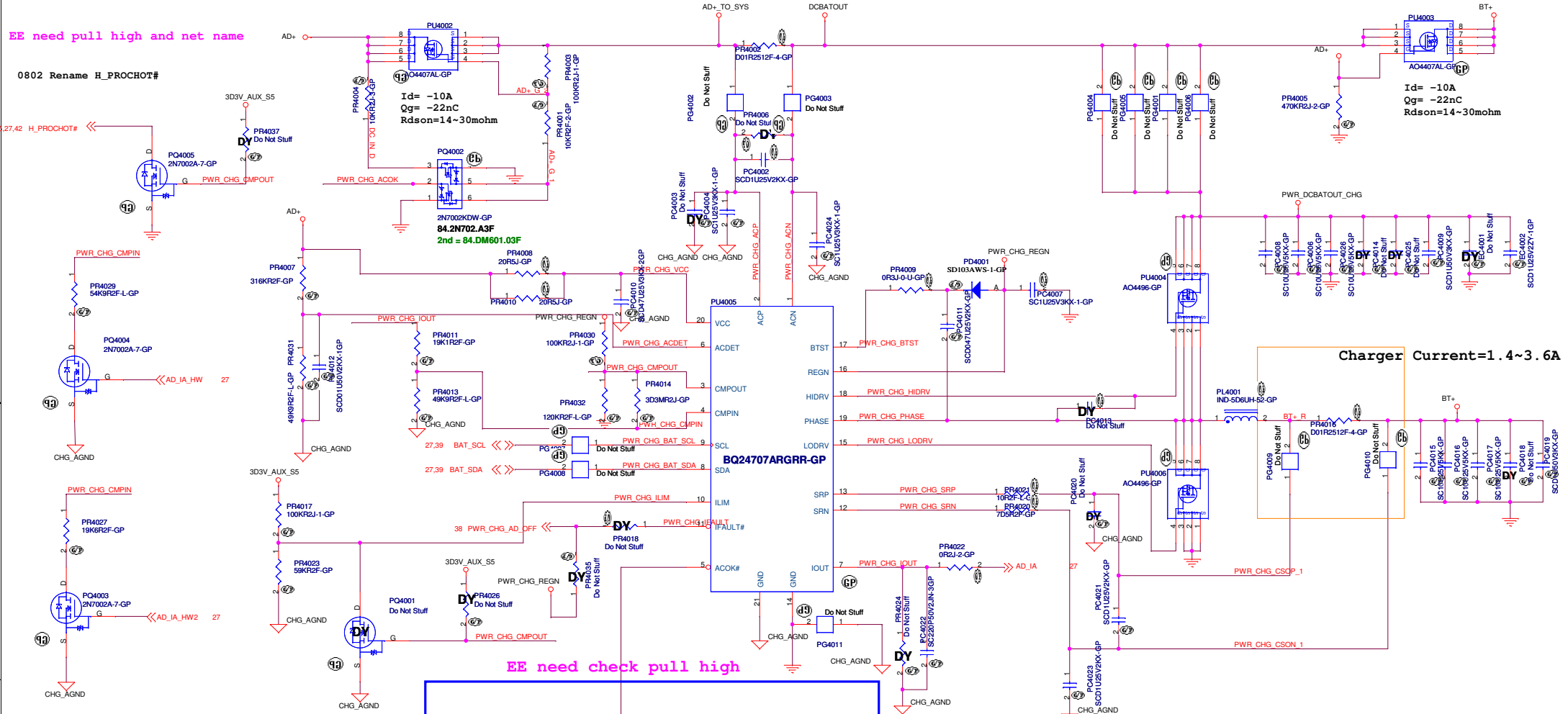
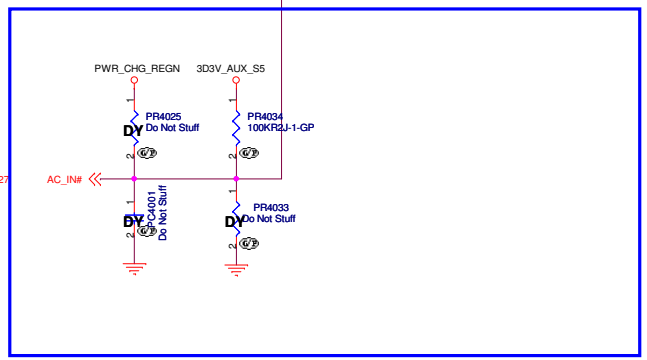
SSID = Charger

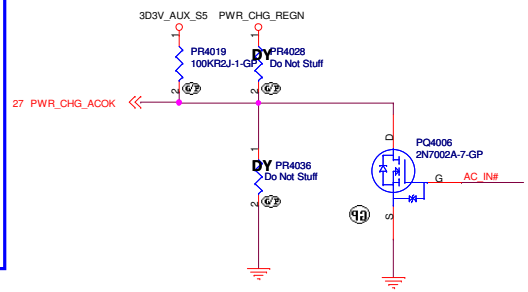
EE need pull high and net name

0802 Rename H_PROCHOT#



EE need check pull high





ROSA

Adapter type	PR4023
65W	24K
90W	33.2K
130W	59K

EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24707

Size	Document Number	Rev
Custom	Enrico/Caruso 15 HR	X01

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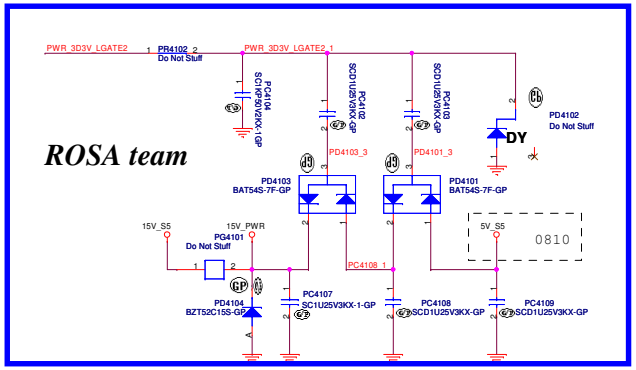
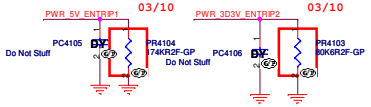
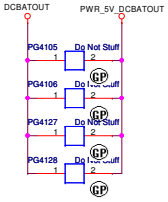
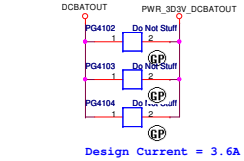
SSID = PWR.Plane.Regulator_5v3p3v









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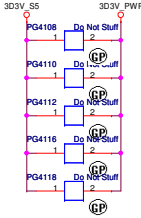
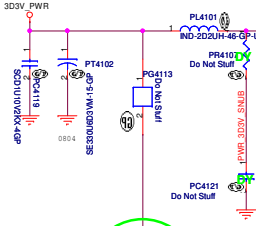
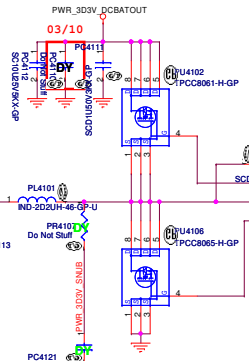
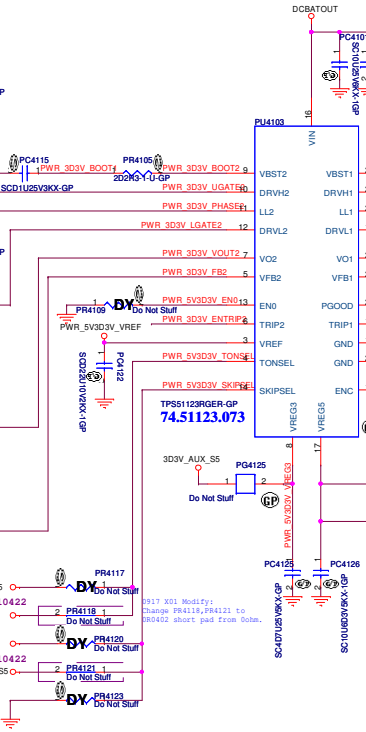
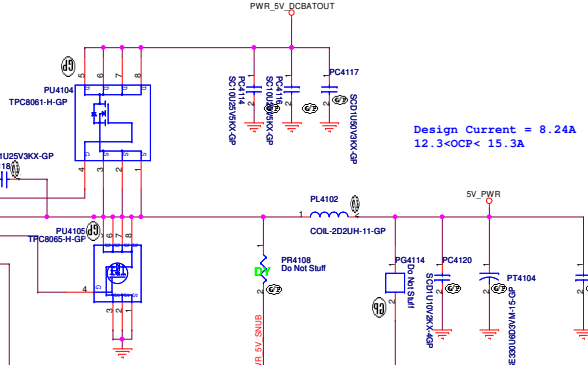
5.7A<OCP< 6.7A



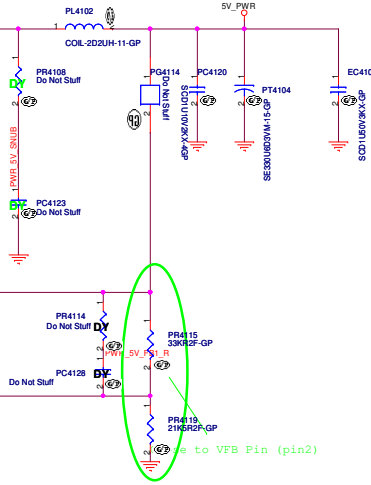


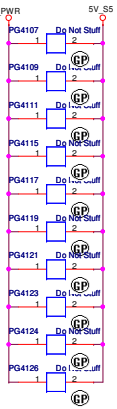


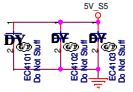


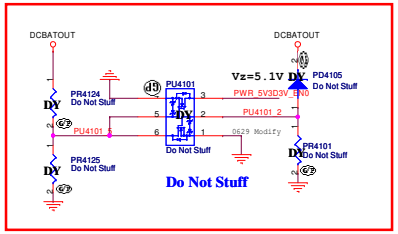


Design Current = 8.24A
12.3<OCP< 15.3A









TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.20UH PCMC104T-2R2 Cyntec 7mohm Isat =27Arms 68.2R210.20C
O/P cap: 330U6.3V M6.3*5.7 15mOhm 3.16Arms Matsuki/77.53371.04L
H/S: TPC8061-H / 21mohm/30mOhm@4.5Vgs/ 84.08061.037
L/S: TPC8065-H / 12mohm/15mOhm@4.5Vgs/ 84.08065.037

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2U PCMC063T-2R2MN Cyntec 20mohm Isat =14Arms 68.2R210.20B
O/P cap: 330U6.3V M6.3*5.7 15mOhm 3.16Arms Matsuki/77.53371.04L
H/S: TPCC8061-H NC 8P / 21mohm/29mOhm@4.5Vgs/ 84.08061.A37
L/S: TPCC8065-H NC 8P / 12.1mohm/17.4mOhm@4.5Vgs/ 84.08065.A37

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V/3D3V(TPS51123RGER)

Size	Document Number	Rev
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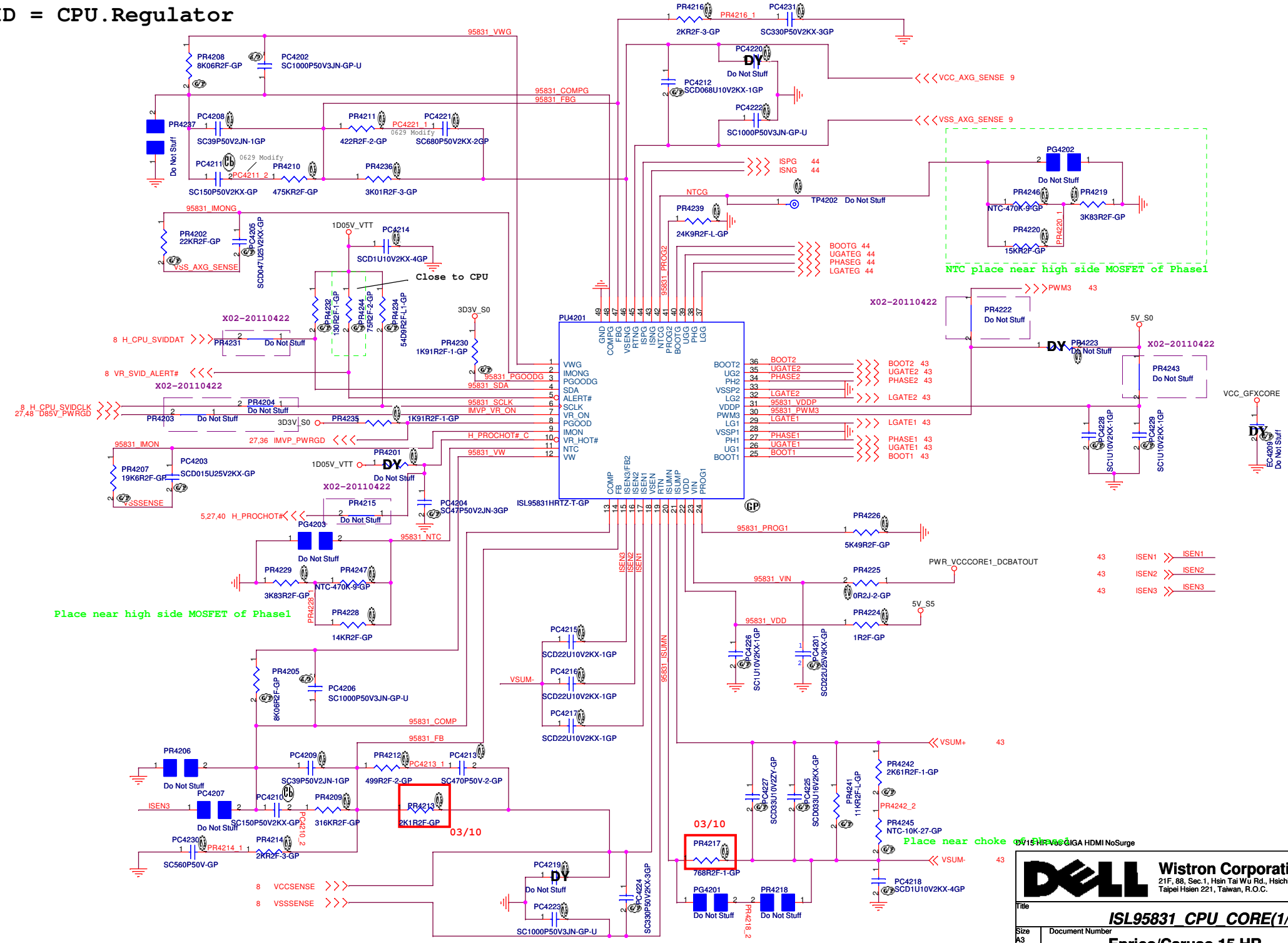
SSID = CPU.Regulator



Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ISL95831_CPU_CORE(1/3)		
Size: A3	Document Number: Enrico/Caruso 15 HR	Rev: X01
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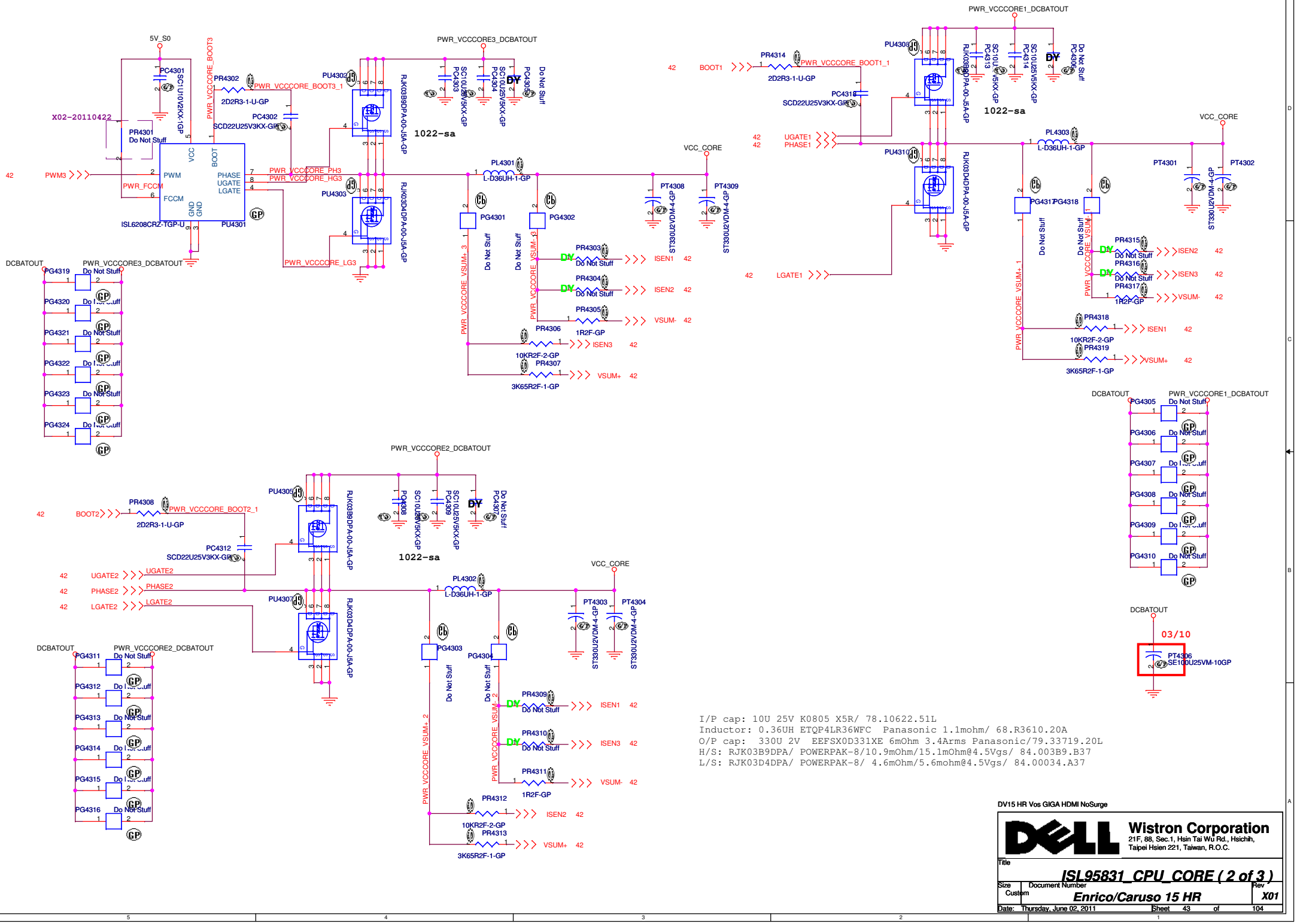

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 0.36UH ETQP4LR36WFC Panasonic 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95831_CPU_CORE (2 of 3)

Size	Document Number	Rev
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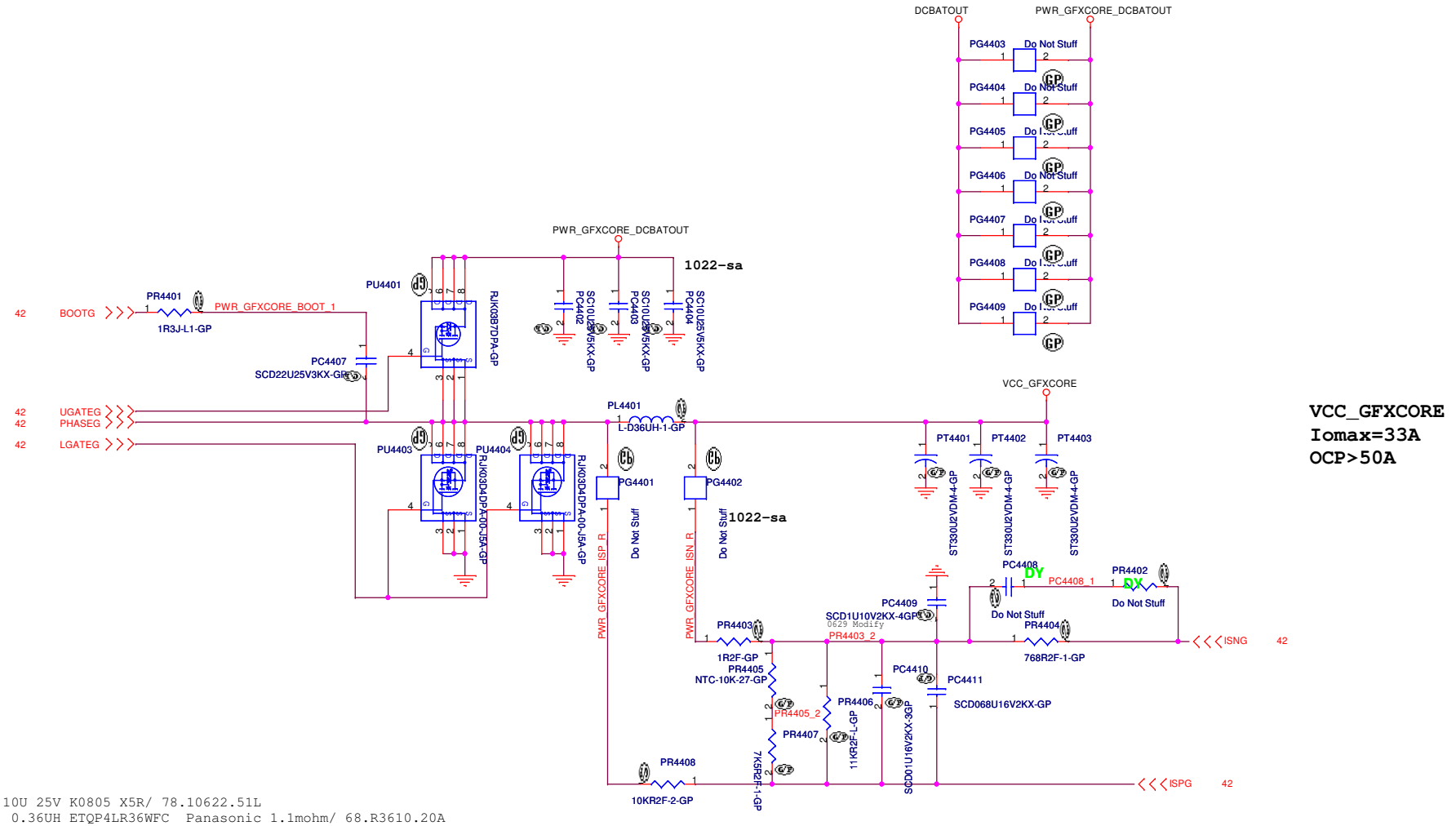
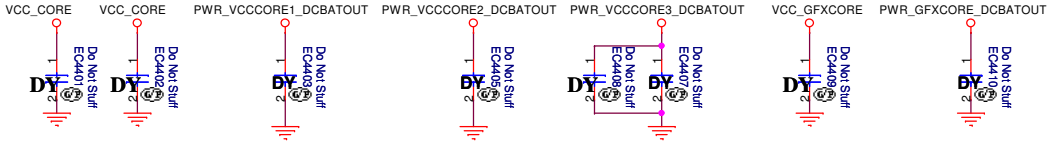


VCC_GFXCORE
Iomax=33A
OCP>50A

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 0.36UH ETQP4LR36WFC Panasonic 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
H/S: RJK03B7DPA NC WPAK 8P/7.7mOhm/10.7mOhm@4.5Vgs/84.003B7.037
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

EMI/ESD



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95831_CPU_CORE(3/3)

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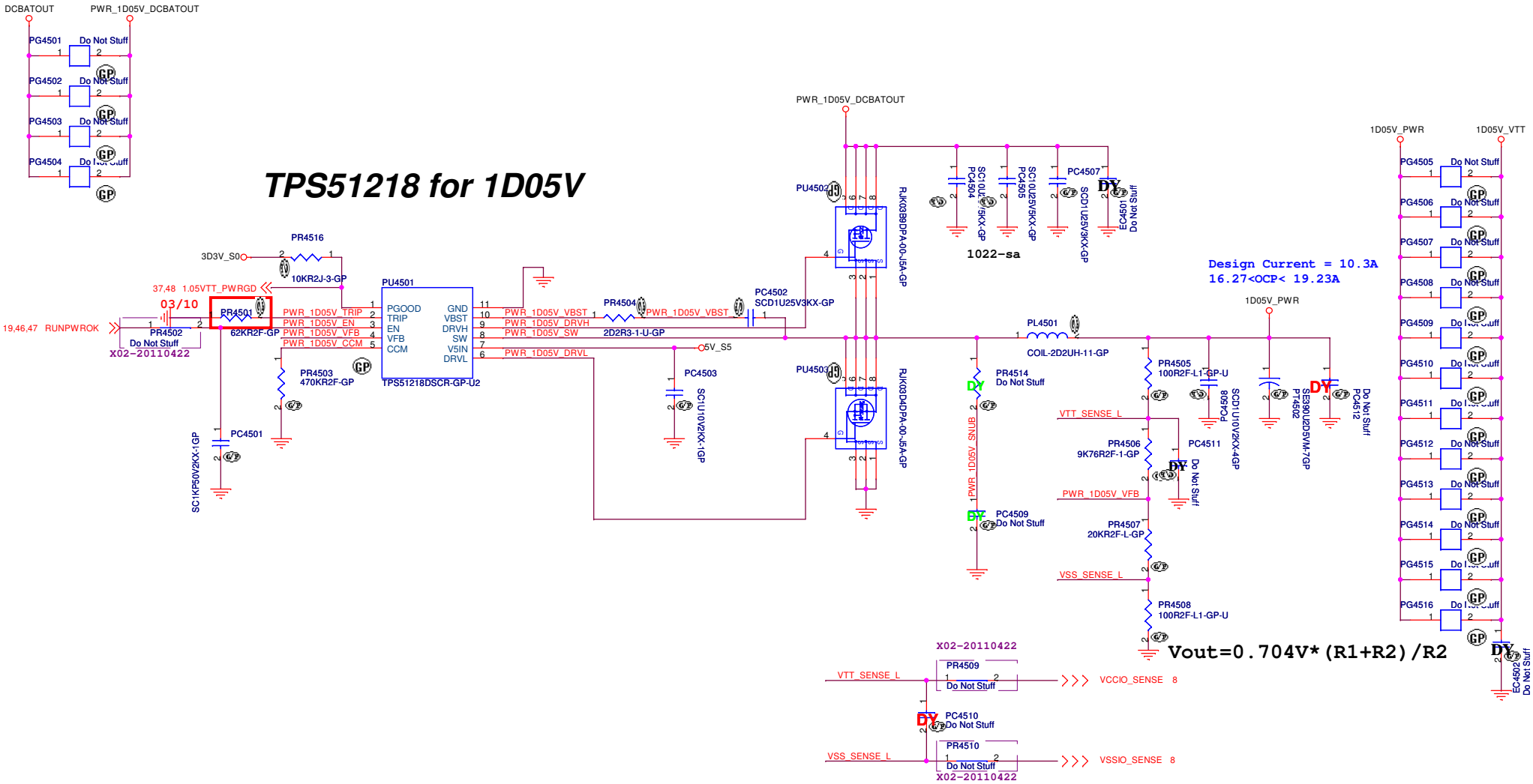

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.20UH PCMC104T-2R2 Cyntec 7mohm Isat =27Arms 68.2R210.20C
O/P cap: 390U 2.5V M 6.3*5.7/ 10mOhm 3.87Arms Matsuki/79.3971V.30L
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218_+1.05V_VTT

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

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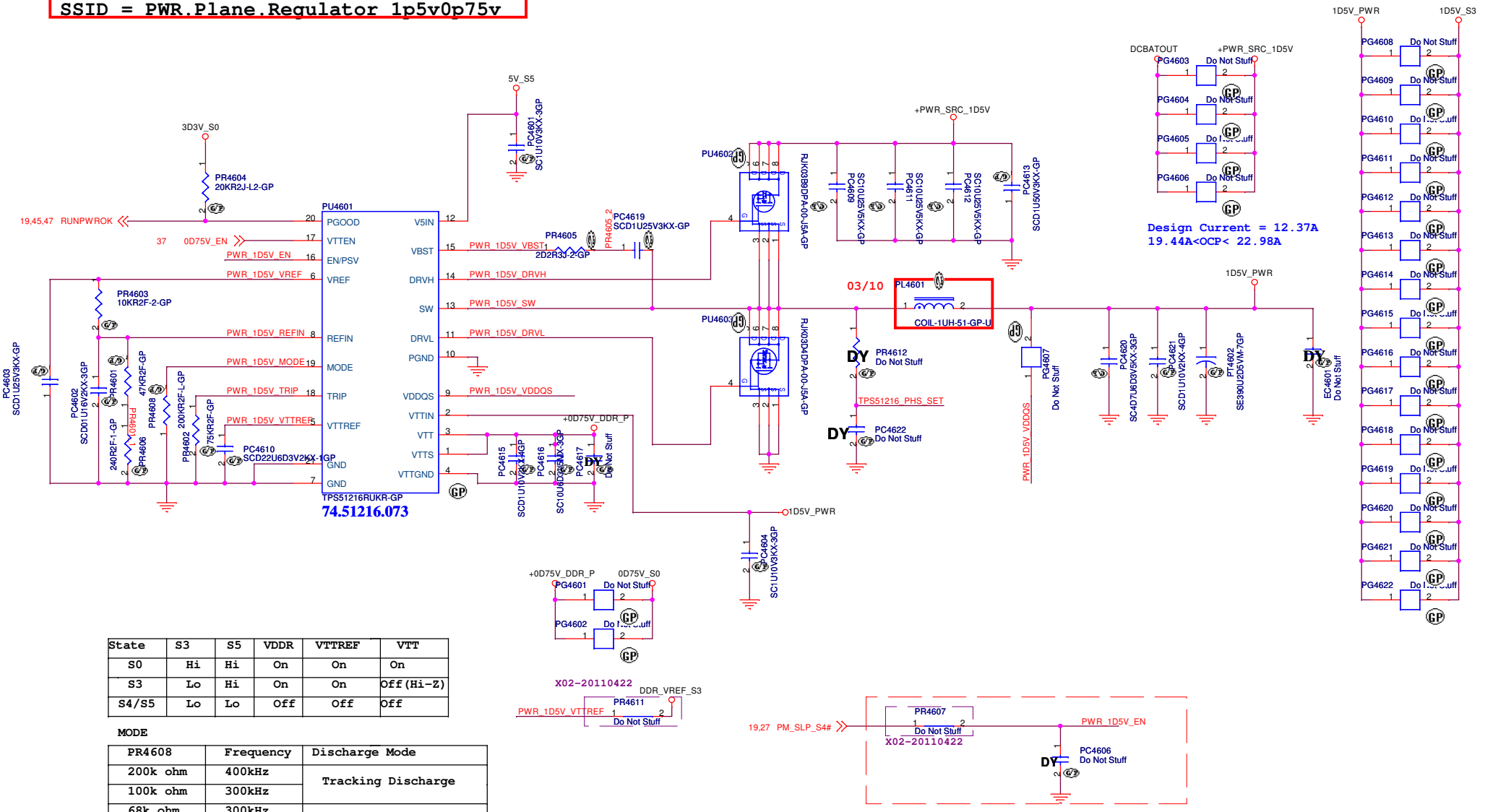
SSID = PWR.Plane.Regulator 1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.0UH PCMB104T-1R0M Cyntec 3mohm Isat =28Arms 68.1R01C.10Q
O/P cap: 390U 2.5V M 6.3*5.7/ 10mOhm 3.87Arms Matsuki/79.3971V.30L
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116_+1.5V_SUS

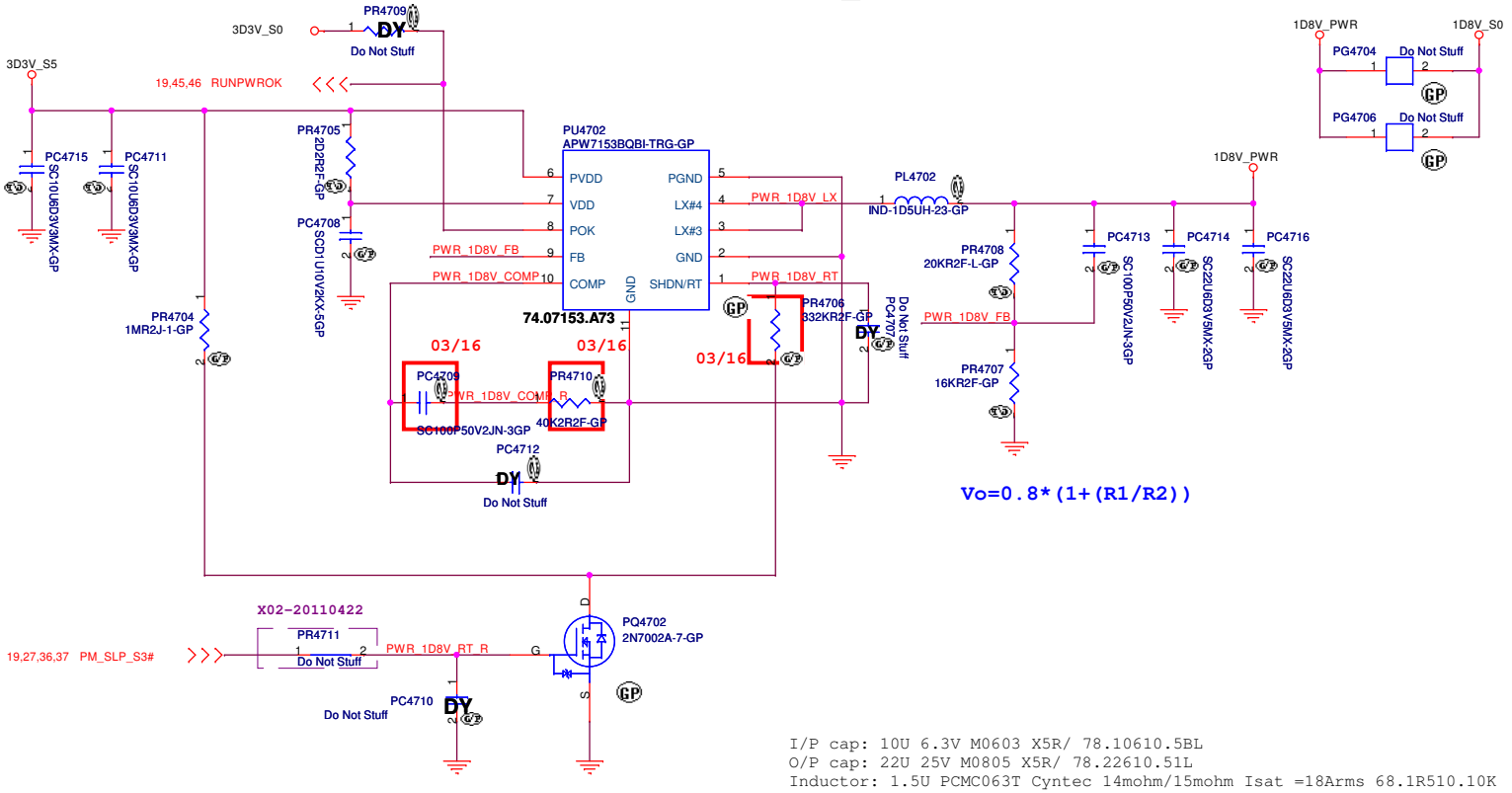
Size: A3 | Document Number: Enrico/Caruso 15 HR | Rev: X01

Date: Thursday, June 02, 2011 | Sheet 46 of 104

SSID = PWR.Plane.Regulator_1D8V_S0

+1.8V_RUN
Design current = 0.87A

APW7153B for 1D8V_S0



I/P cap: 10U 6.3V M0603 X5R/ 78.10610.5BL
O/P cap: 22U 25V M0805 X5R/ 78.22610.51L
Inductor: 1.5U PCMC063T Cyntec 14mohm/15mohm Isat =18Arms 68.1R510.10K

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51311 for 1D8V_S0

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A3	Enrico/Caruso 15 HR	X01

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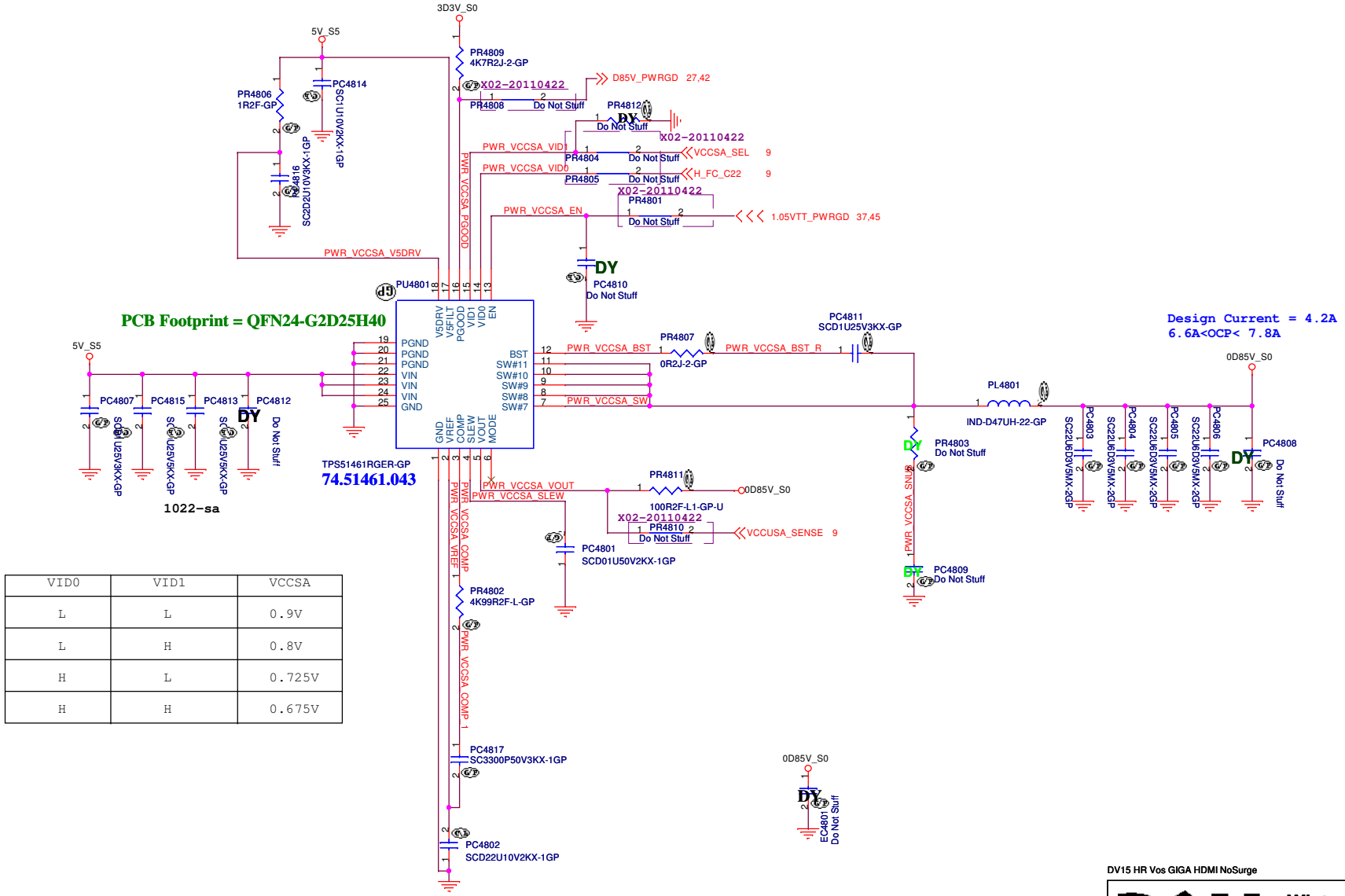
TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51461_VCCSA

Size	Document Number	Rev
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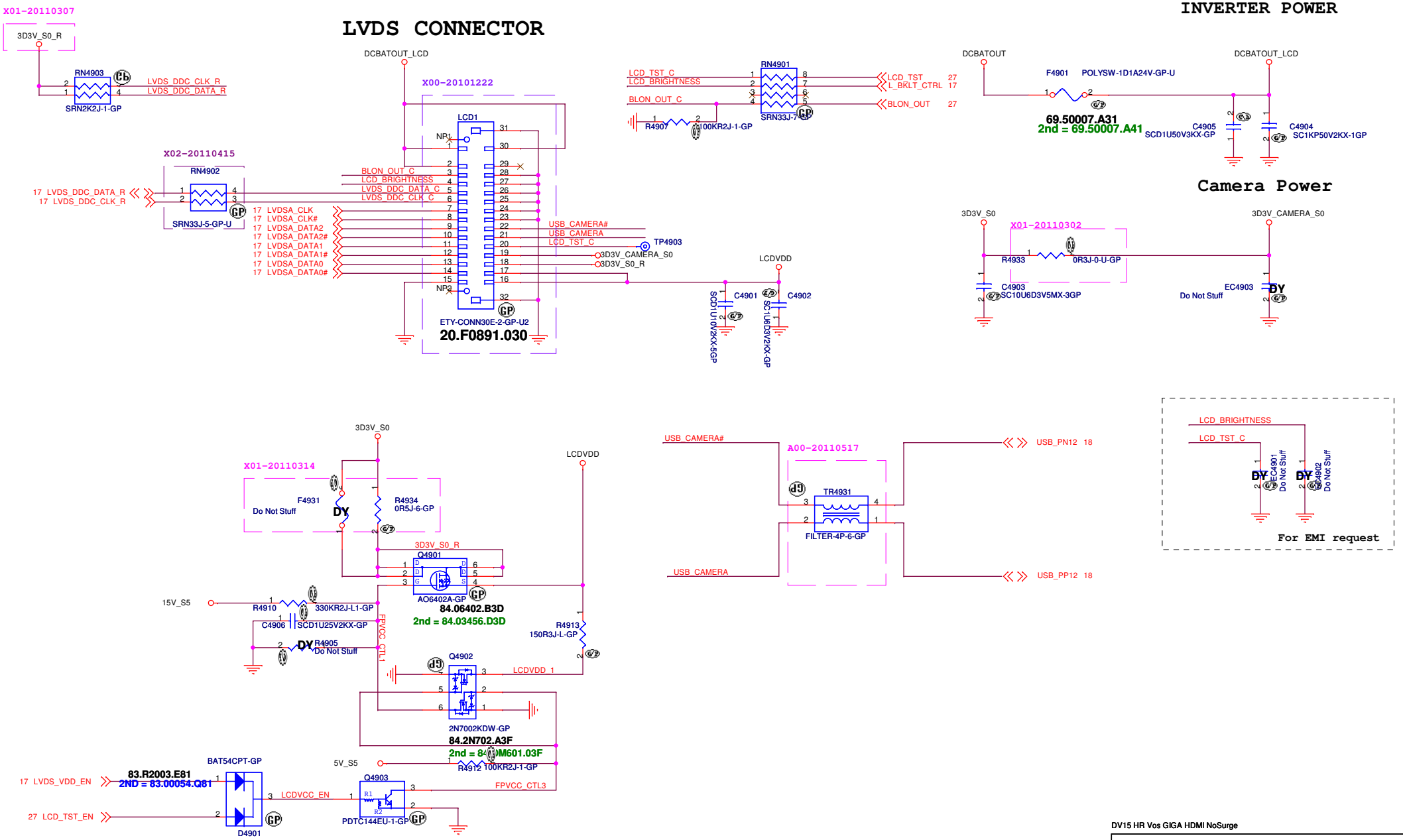

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LCD Connector*

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

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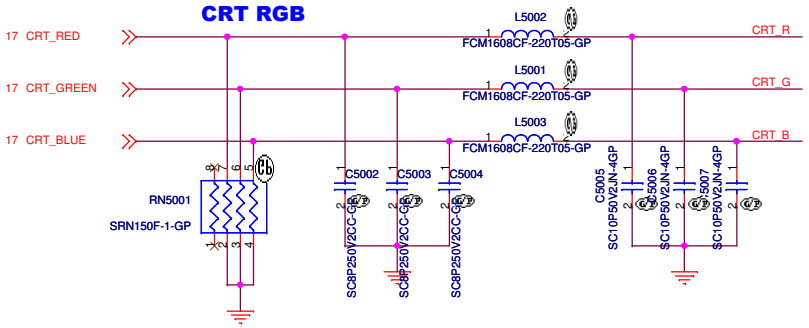
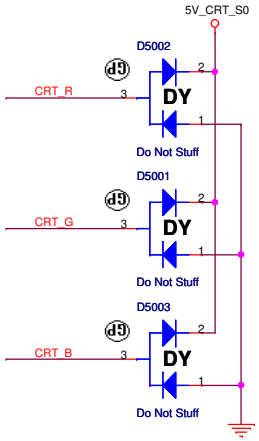
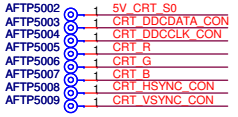
SSID = VIDEO

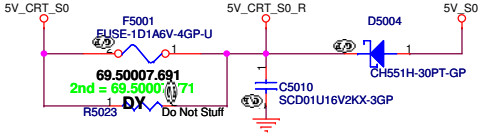
Layout Note:

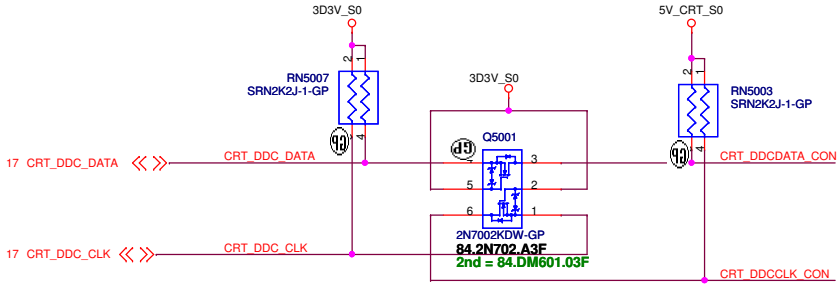
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

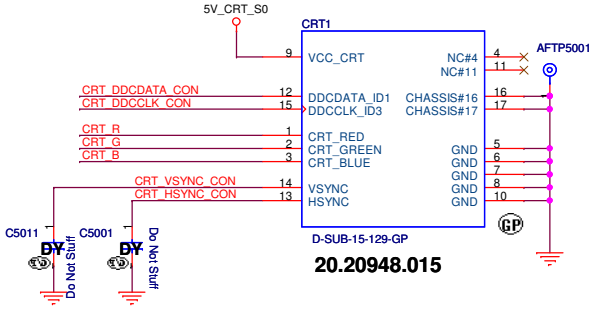




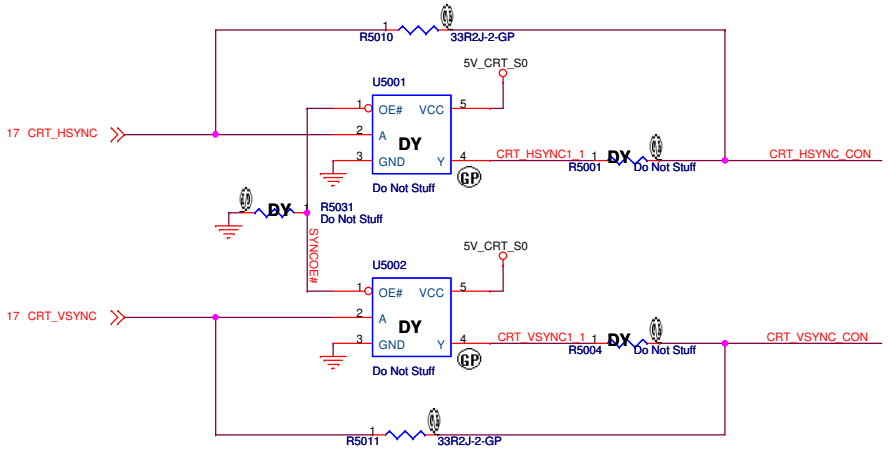


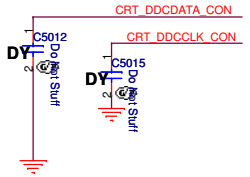






Hsync & Vsync





DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CRT Connector*

Size	Document Number	Rev
Custom	Enrico/Caruso 15 HR	X01

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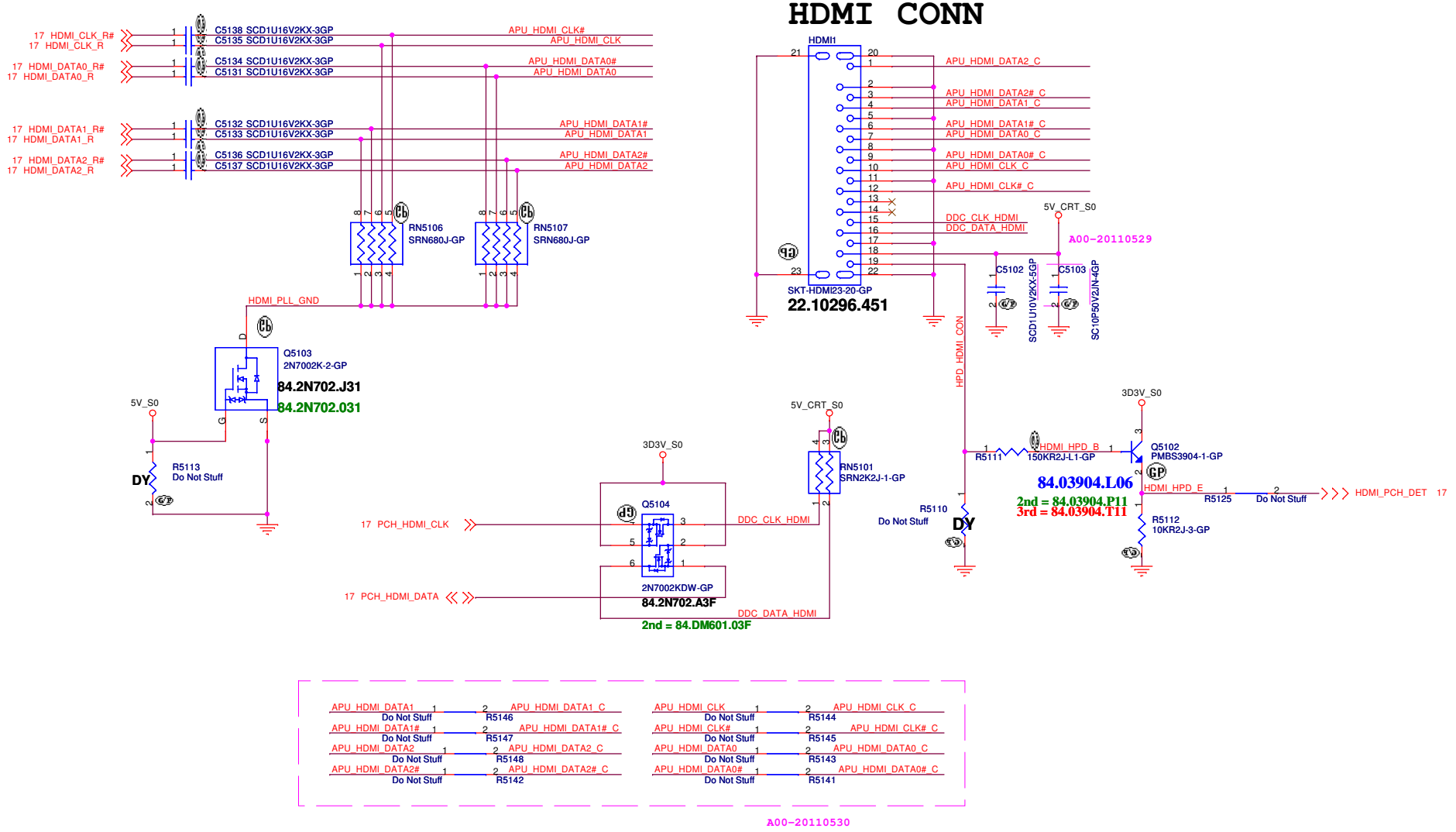
SSID = VIDEO

HDMI CONN



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

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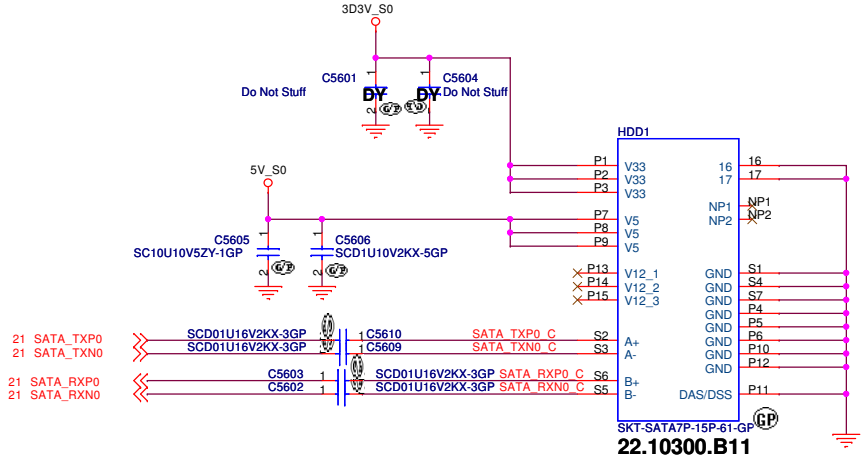
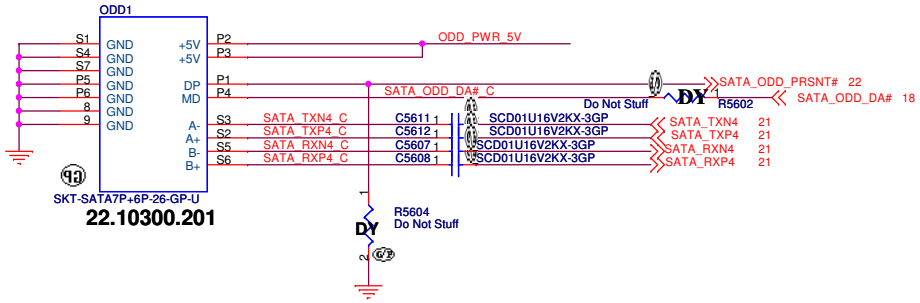
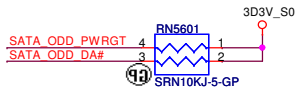
SSID = SATA

SATA HDD Connector

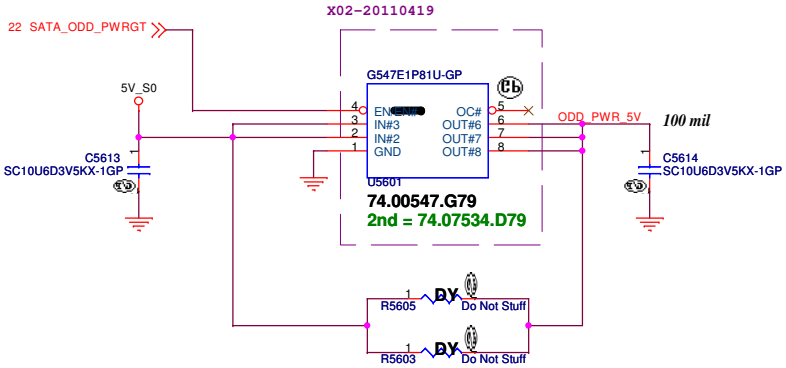


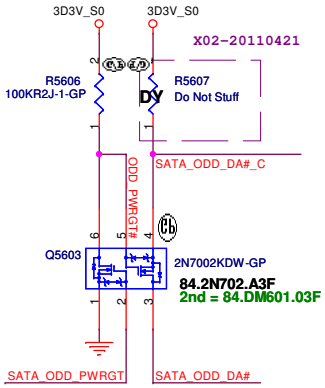
ODD Connector

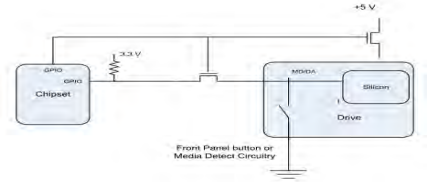




SUPPORT ZERO SATA ODD







When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
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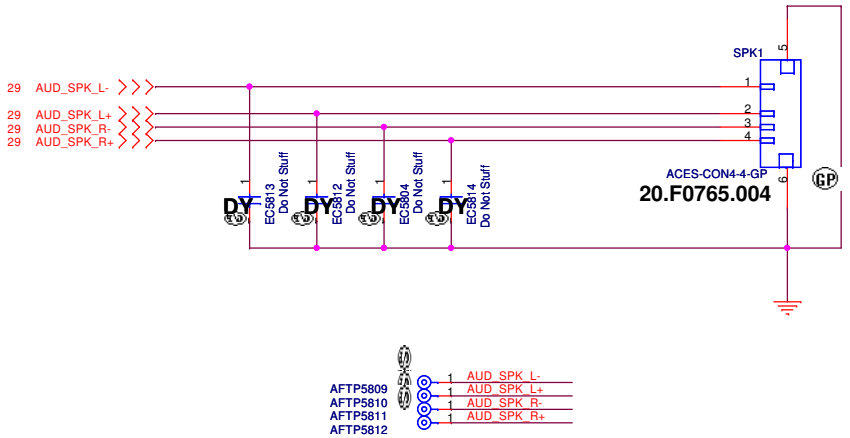
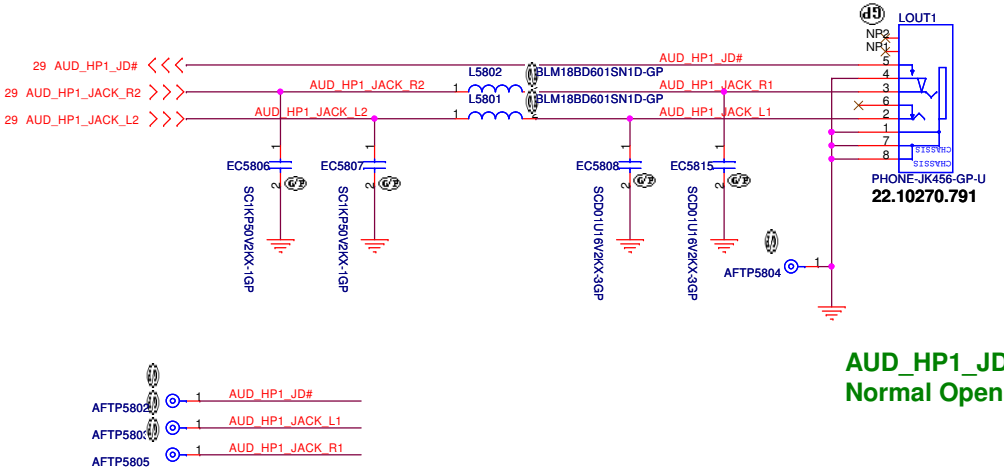
SSID = AUDIO

Speaker Connector

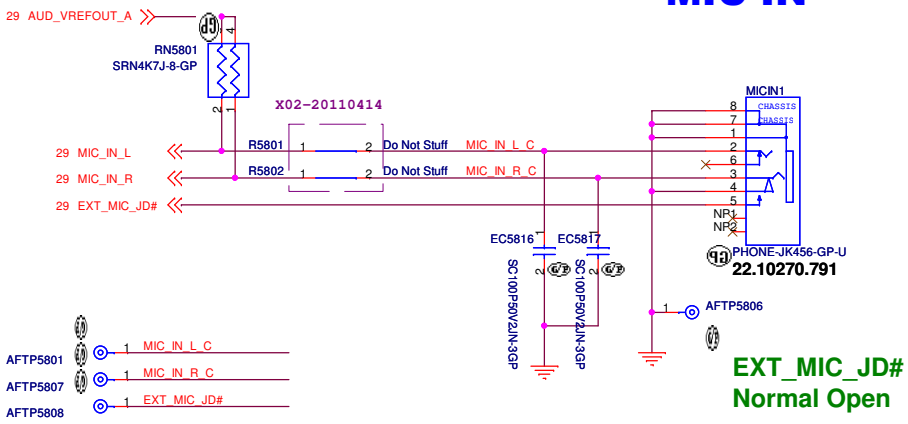


LINE1 OUT



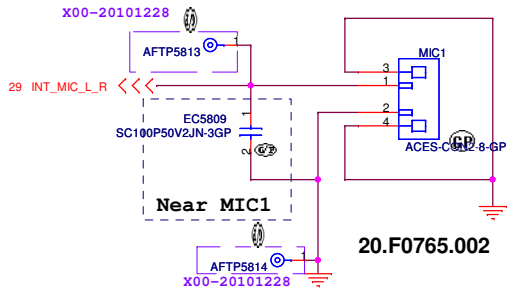
AUD_HP1_JD#
Normal Open

MIC IN



EXT_MIC_JD#
Normal Open

Internal Microphone



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SPEAKER CONN		
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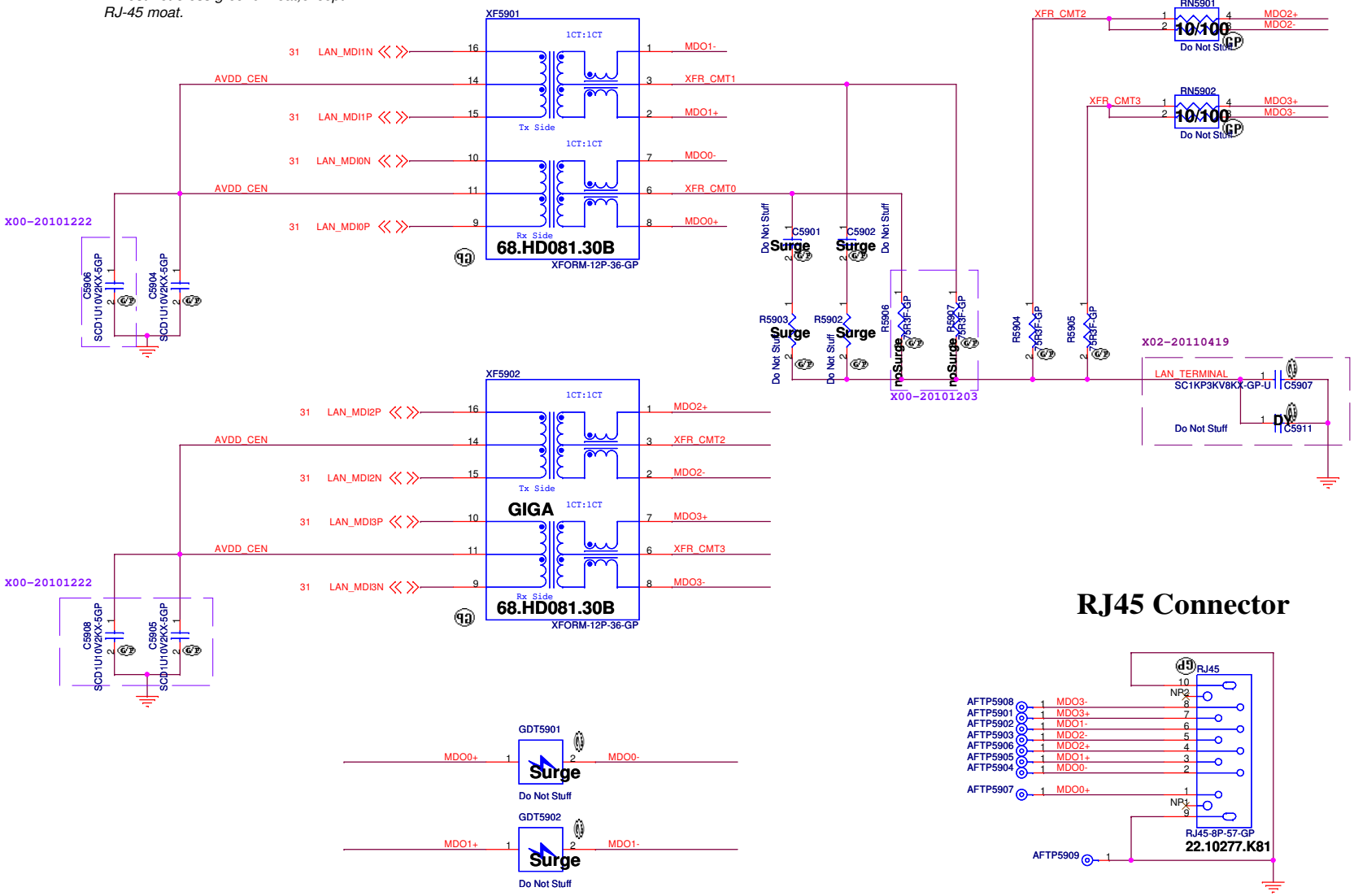
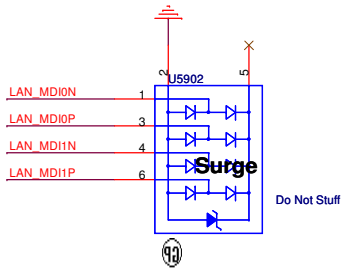
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

10/100M Lan Transformer





RJ45 Connector

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**

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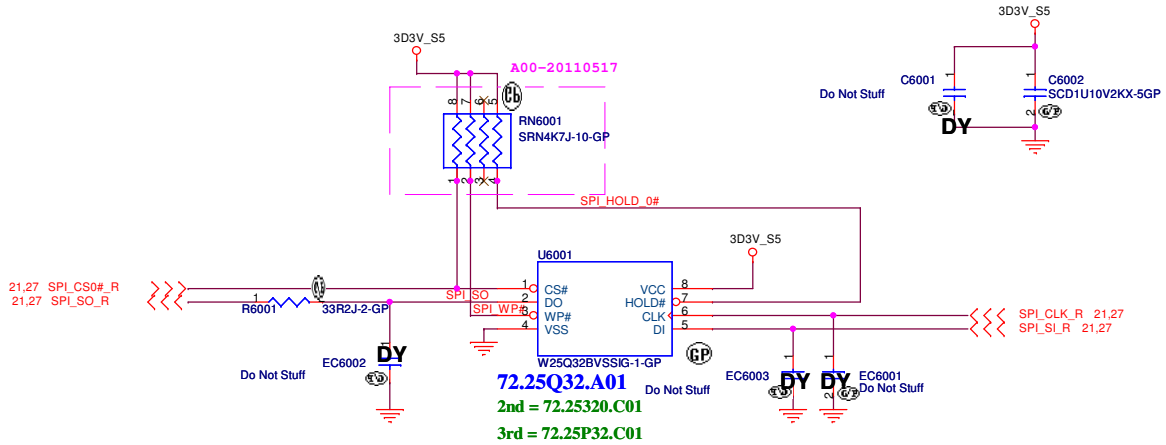
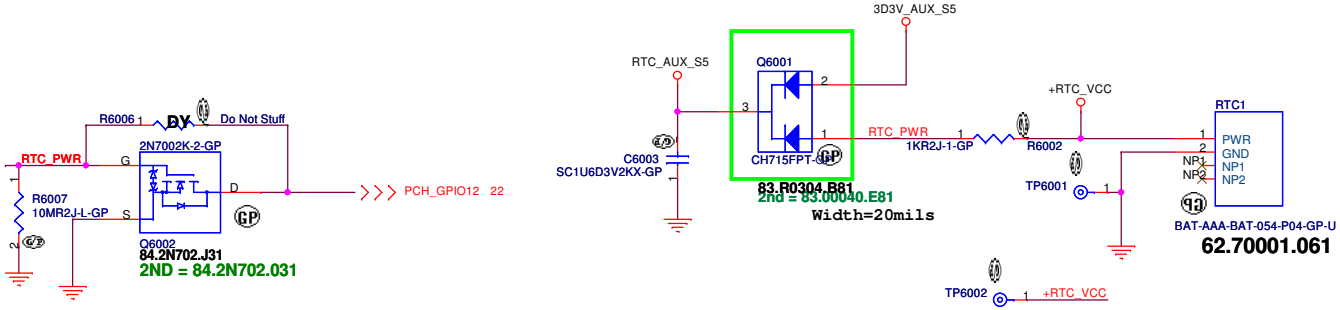
SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Flash/RTC		
Size: A3	Document Number: Enrico/Caruso 15 HR	Rev: X01
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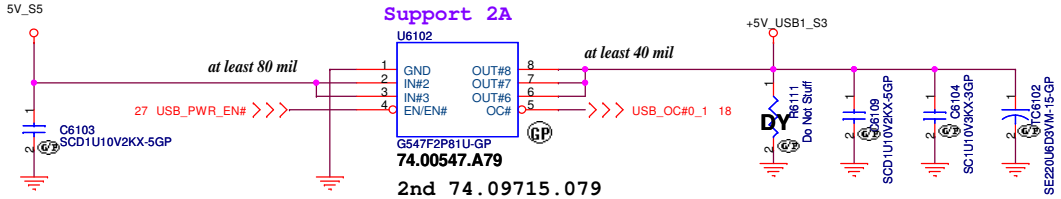
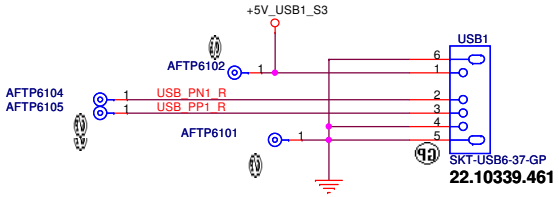
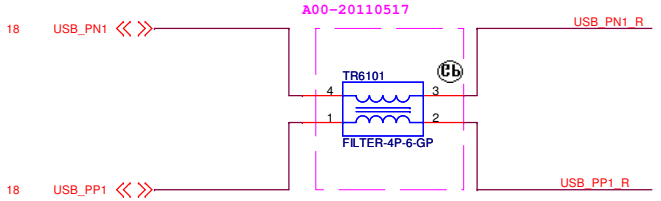
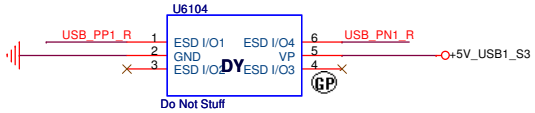
SSID = USB

Left USB Power x1

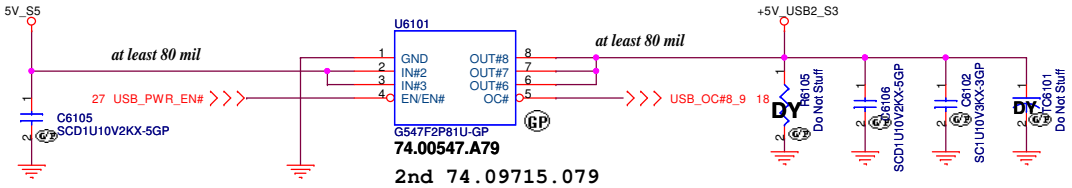


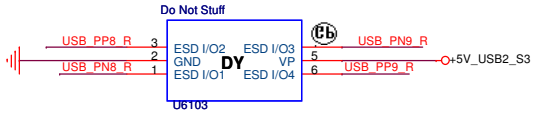


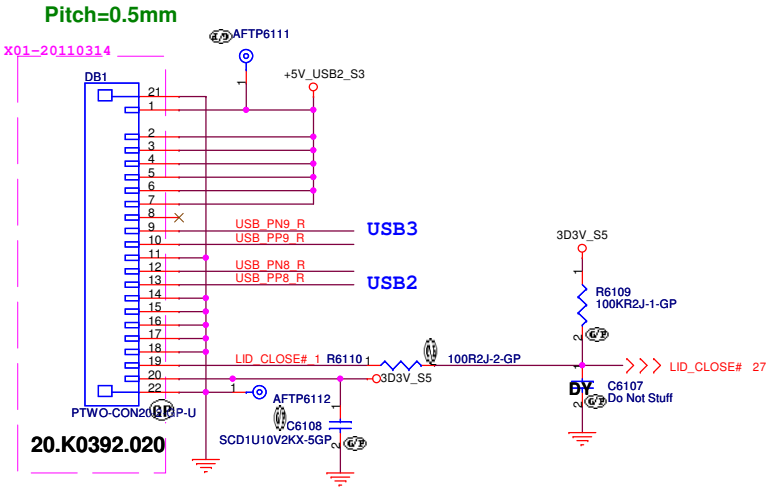


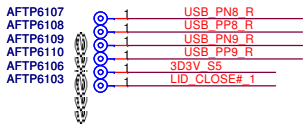


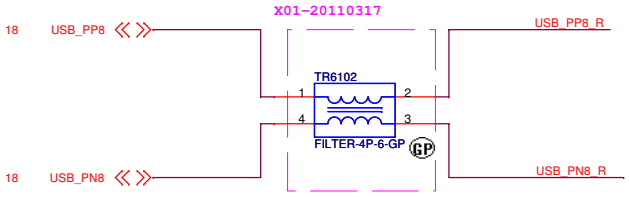
Right USB Power x2

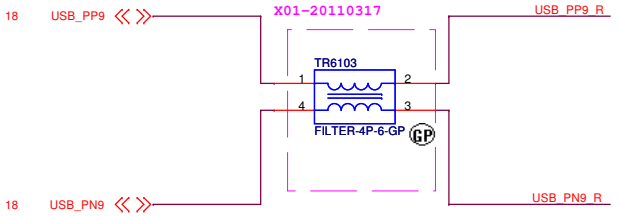












DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Power SW

Size | Document Number: Enrico/Caruso 15 HR | Rev: X01

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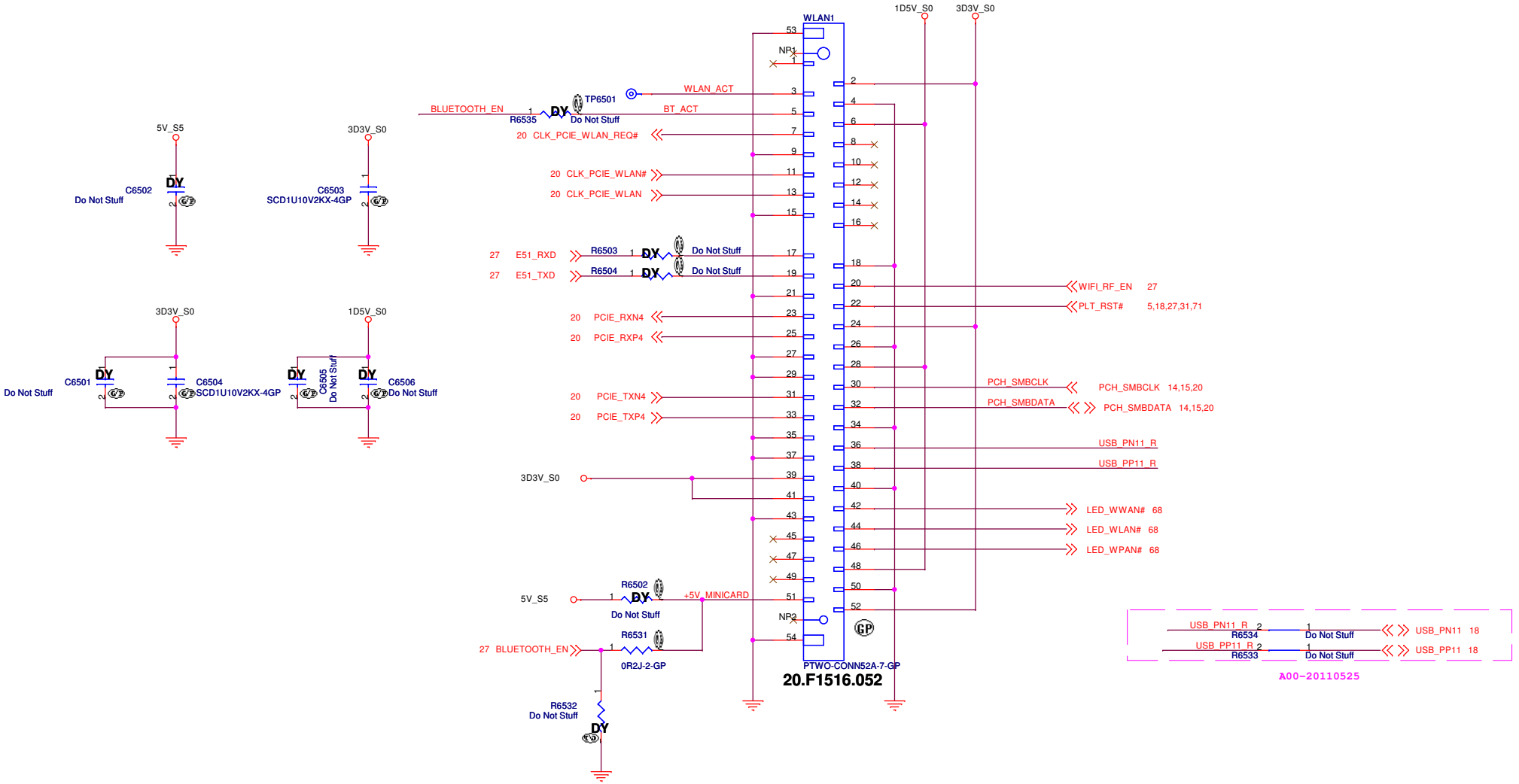
SSID = Wireless

Mini Card Connector(802.11b/g/n)



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

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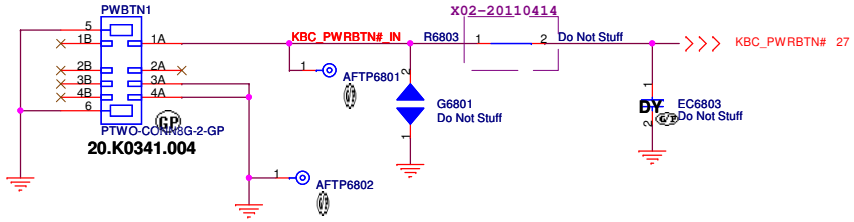
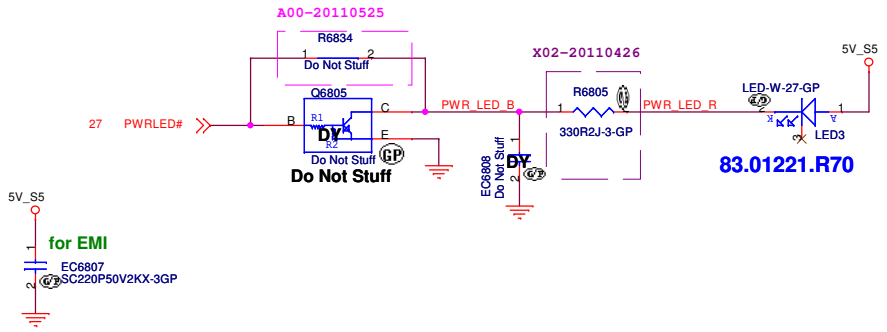
SSID = User.Interface

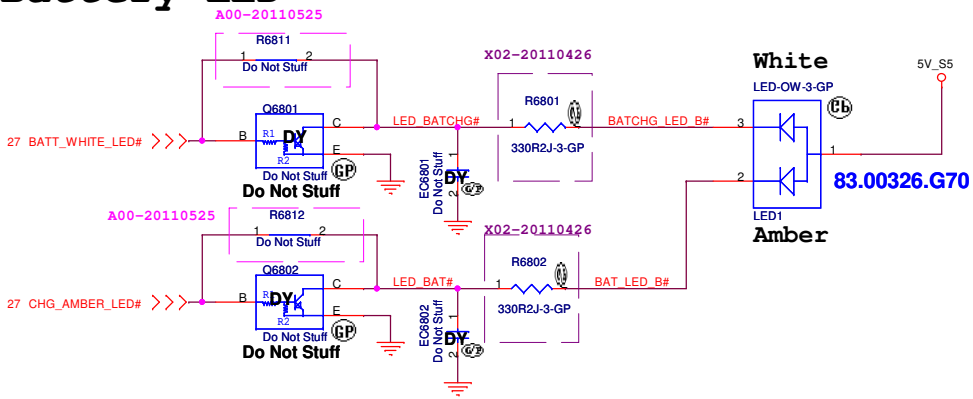
Power BTN Connector



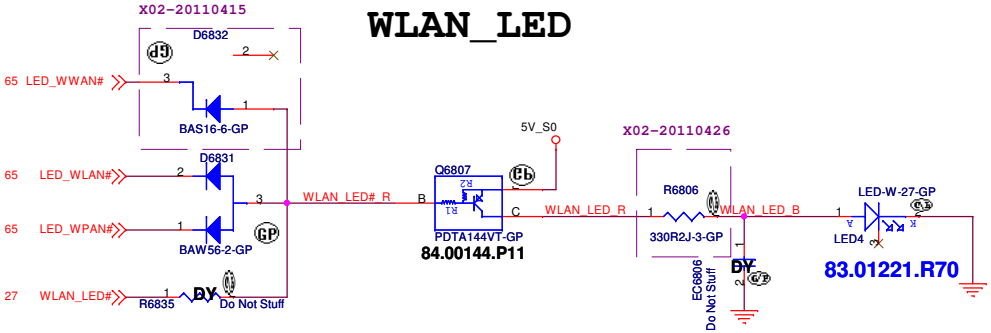
Power LED



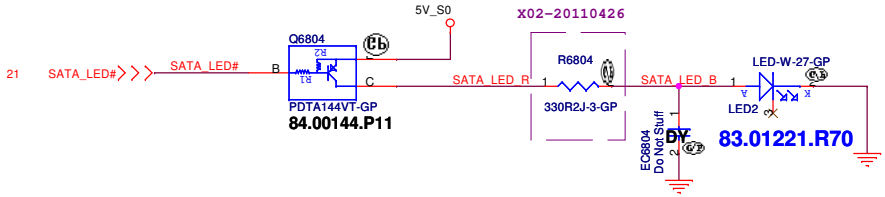
Battery LED



WLAN_LED



HDD LED



LED Location from left to right
(MB, Top View)

LED3	LED2	LED1	LED4
PWR	HDD	Battery	WiFi

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Title: LED Bard/Power Button

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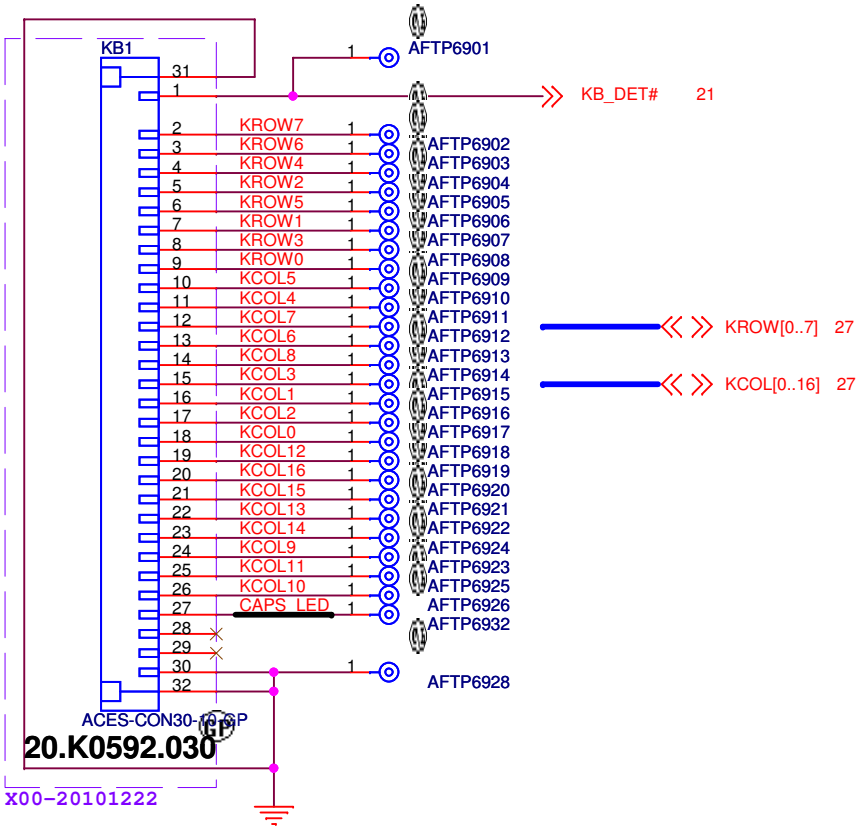
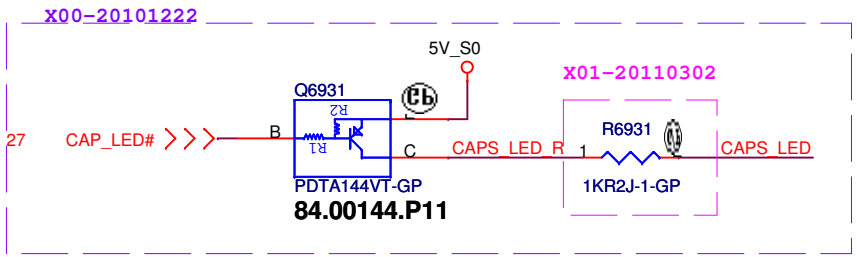
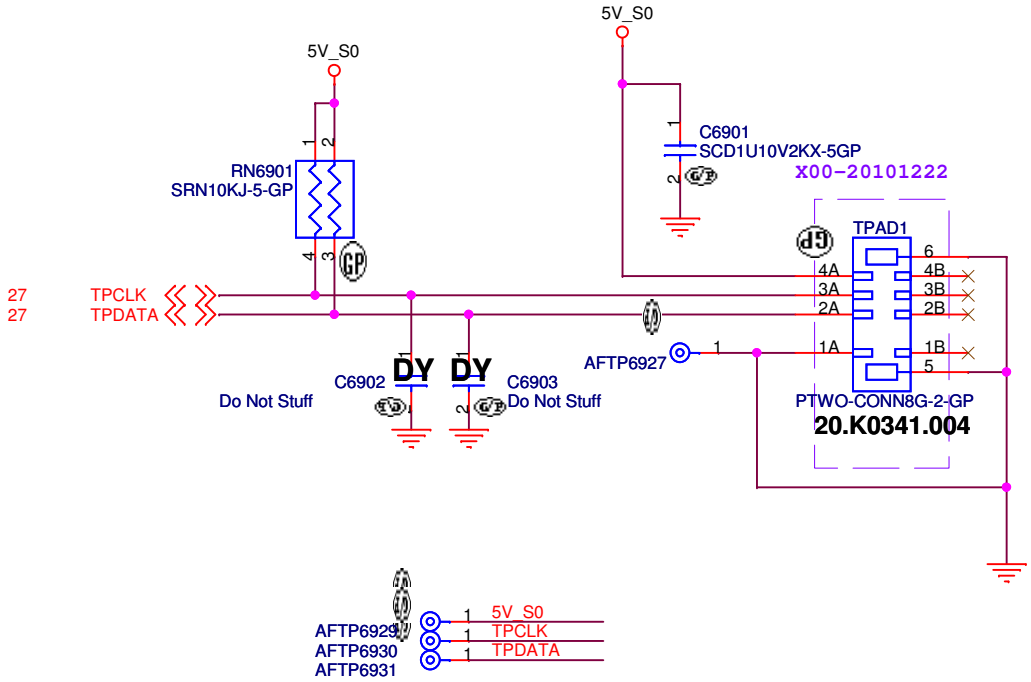
Internal KeyBoard Connector





TouchPad Connector



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Title: ***Key Board/Touch Pad***

Size	Document Number	Rev
A4	Enrico/Caruso 15 HR	X01

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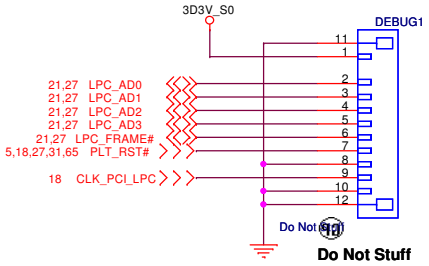

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Title: *Dubug connector*		
Size: A3	Document Number: *Enrico/Caruso 15 HR*	Rev: *X01*
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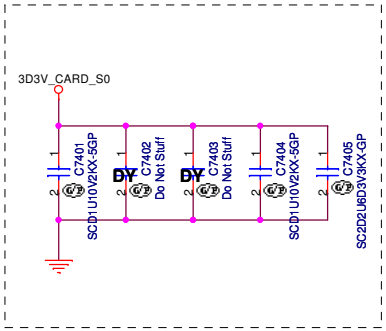
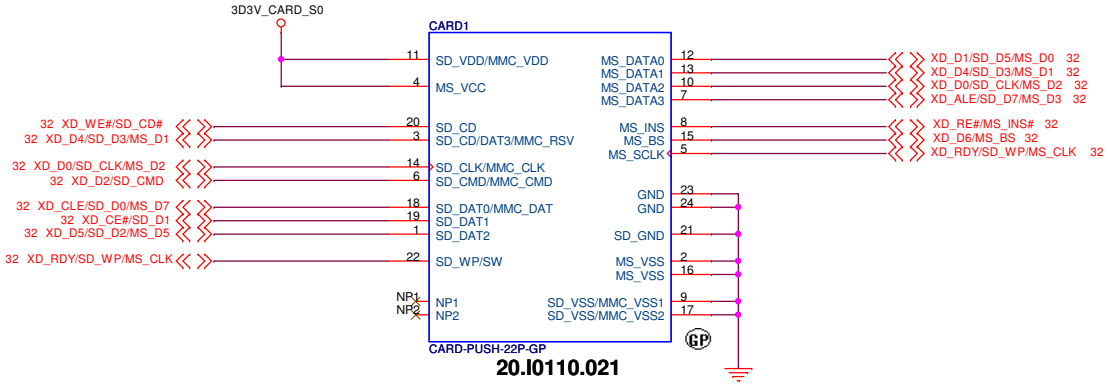
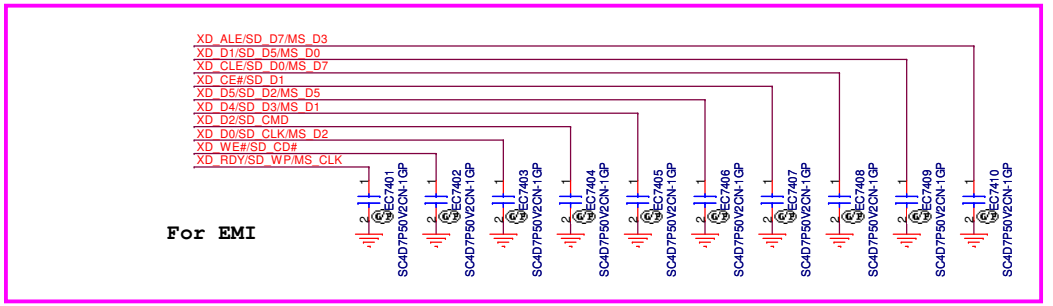
SSID = SDIO

SD/MMC/MS Card Reader





X01-20110315



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Title: SD/MS/MMC Card CONN

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SSID = Mechanical

H10 Do Not Stuff DY Do Not Stuff
H11 Do Not Stuff DY
H12 Do Not Stuff DY
H6 Do Not Stuff Do Not Stuff
H7 Do Not Stuff Do Not Stuff
H8 Do Not Stuff
H9 Do Not Stuff DY

H1 Do Not Stuff Do Not Stuff
H2 Do Not Stuff Do Not Stuff
H4 Do Not Stuff Do Not Stuff
H5 Do Not Stuff Do Not Stuff
H3 Do Not Stuff Do Not Stuff
H15 Do Not Stuff

Top Side

34.4B502.001 HMI1 STF256R117H119-GP

34.4CK01.001 HTH1 STF237R117H83-1-GP

34.4F822.002 SPR1 SPRING-51-GP

34.4F822.002 SPR2 SPRING-51-GP

34.4F822.002 SPR3 SPRING-51-GP

DCBATOUT EC9701 SCD1U25V2ZY-1GP
DCBATOUT EC9702 SCD1U25V2ZY-1GP
DCBATOUT EC9703 SCD1U25V2ZY-1GP
DCBATOUT EC9704 SCD1U25V2ZY-1GP
DCBATOUT EC9705 SCD1U25V2ZY-1GP
DCBATOUT EC9706 SCD1U25V2ZY-1GP
DCBATOUT EC9707 SCD1U25V2ZY-1GP
DCBATOUT C9711 SC1KP25V2JX-GP

DCBATOUT EC9709 SCD1U25V2ZY-1GP
DCBATOUT EC9711 SCD1U25V2ZY-1GP
DCBATOUT EC9712 SCD1U25V2ZY-1GP
DCBATOUT EC9713 SCD1U25V2ZY-1GP
DCBATOUT EC9714 SCD1U25V2ZY-1GP
DCBATOUT EC9708 SCD1U25V2ZY-1GP
DCBATOUT EC9710 SCD1U25V2ZY-1GP

1D5V_S3 EC9734 SCD1U10V2KX-5GP
1D5V_S3 EC9735 SCD1U10V2KX-5GP
1D5V_S0 EC9736 SCD1U10V2KX-5GP
1D05V_VTT EC9745 SCD1U10V2KX-5GP
VCC_CORE EC9748 SCD1U10V2KX-5GP
VCC_CORE EC9749 SCD1U10V2KX-5GP
VCC_GFXCORE EC9750 SCD1U10V2KX-5GP
0D85V_S0 EC9729 SCD1U10V2KX-5GP
5V_S0 EC9717 SCD1U10V2KX-5GP

3D3V_S0 EC9720 SCD1U10V2KX-5GP
3D3V_S0 EC9721 SCD1U10V2KX-5GP
3D3V_S0 EC9722 SCD1U10V2KX-5GP
3D3V_S5 EC9723 SCD1U10V2KX-5GP
3D3V_S5 EC9724 SCD1U10V2KX-5GP
3D3V_S5 EC9725 SCD1U10V2KX-5GP
3D3V_S5 EC9726 SCD1U10V2KX-5GP
5V_S0 EC9715 SCD1U10V2KX-5GP
5V_S0 EC9716 SCD1U10V2KX-5GP

FOR EMI REQUEST

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Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: Enrico/Caruso 15 HR
Rev: X01
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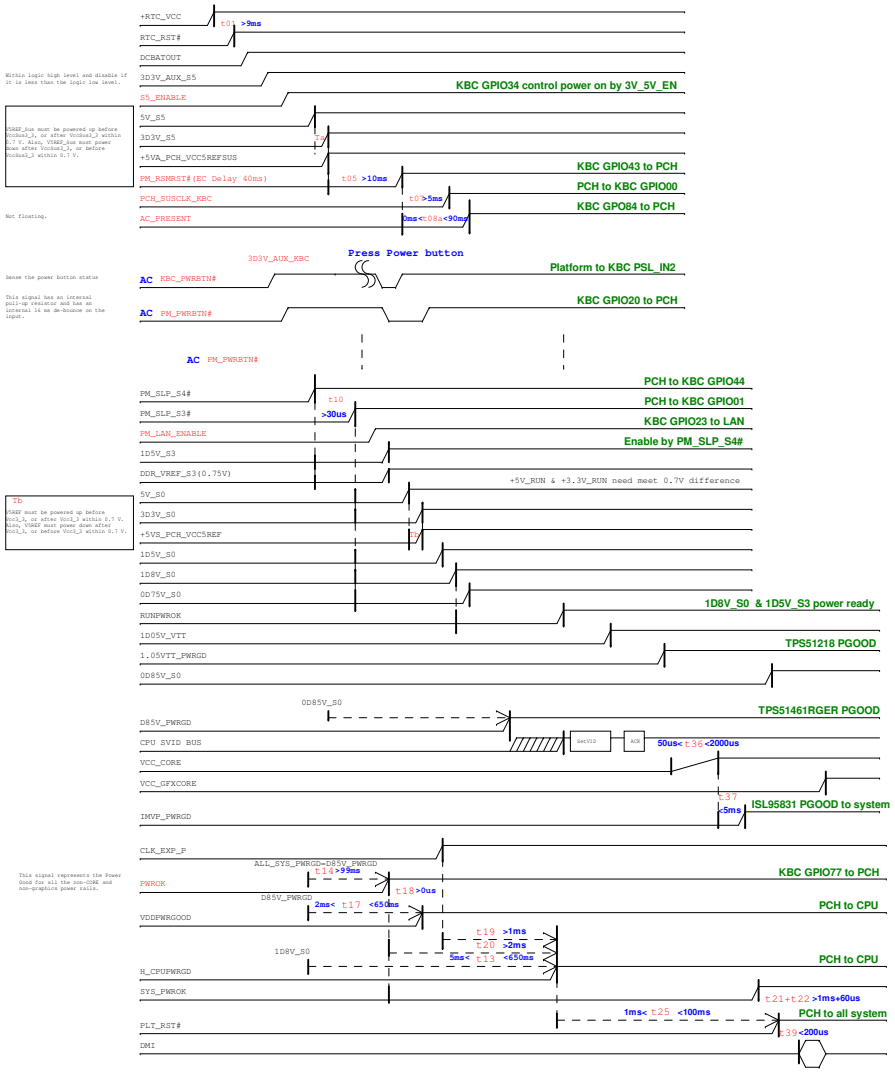
Huron River Platform Power Sequence

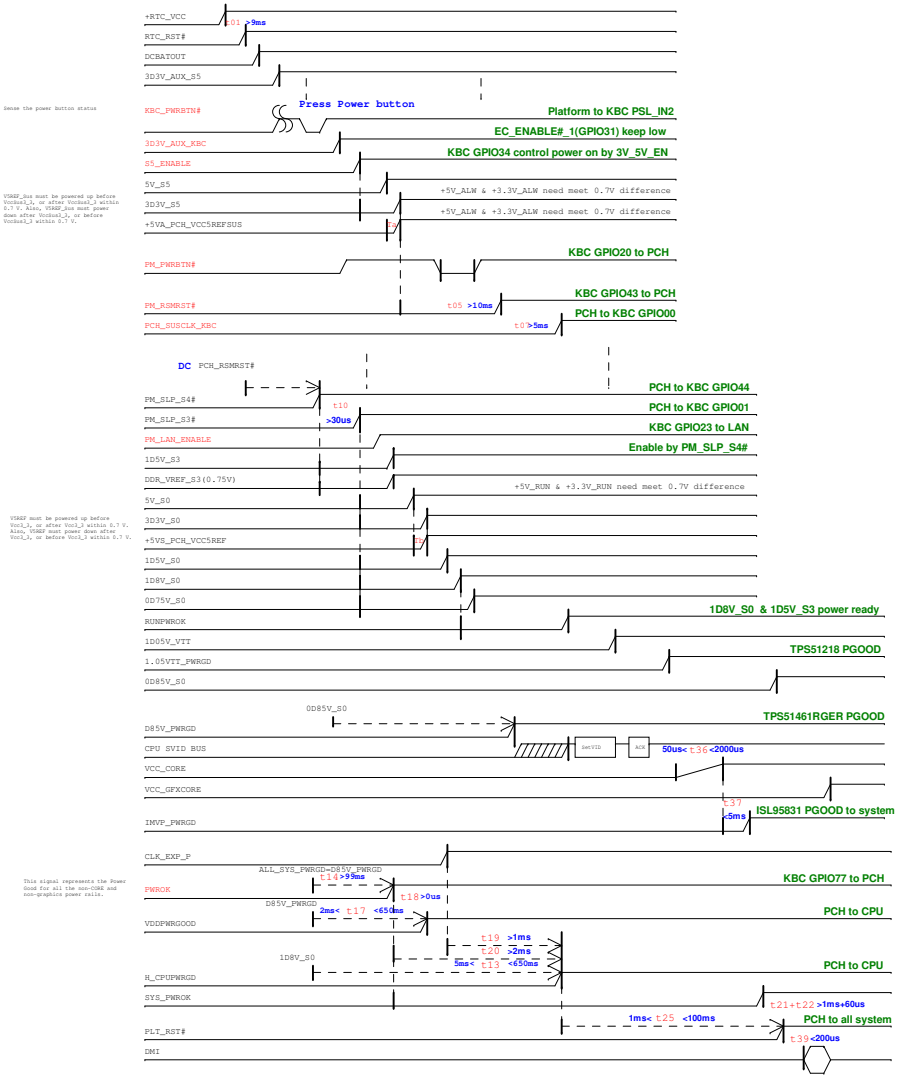
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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Title: Power Sequence

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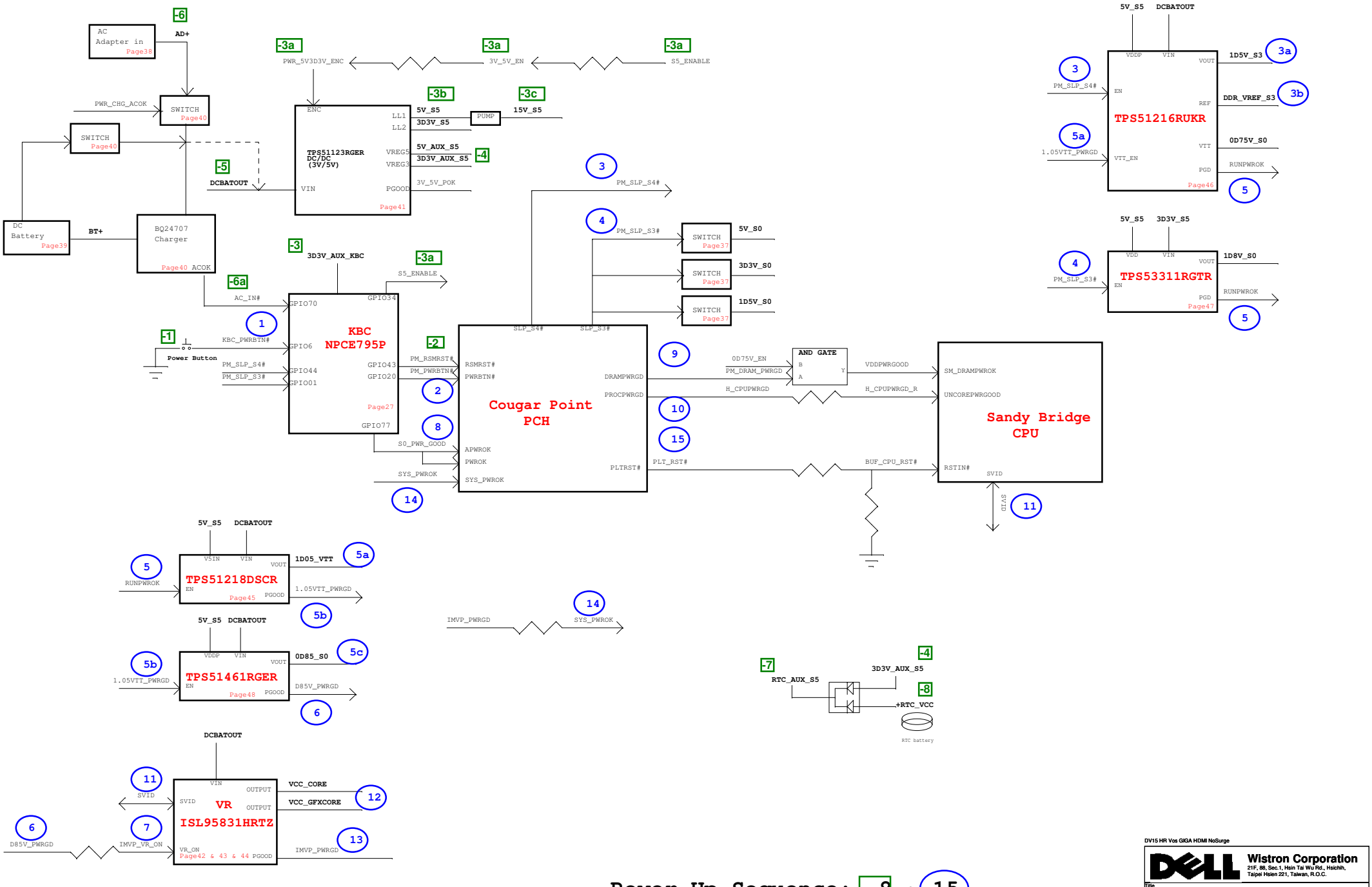
Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 15

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Title: Power Sequence Diagram

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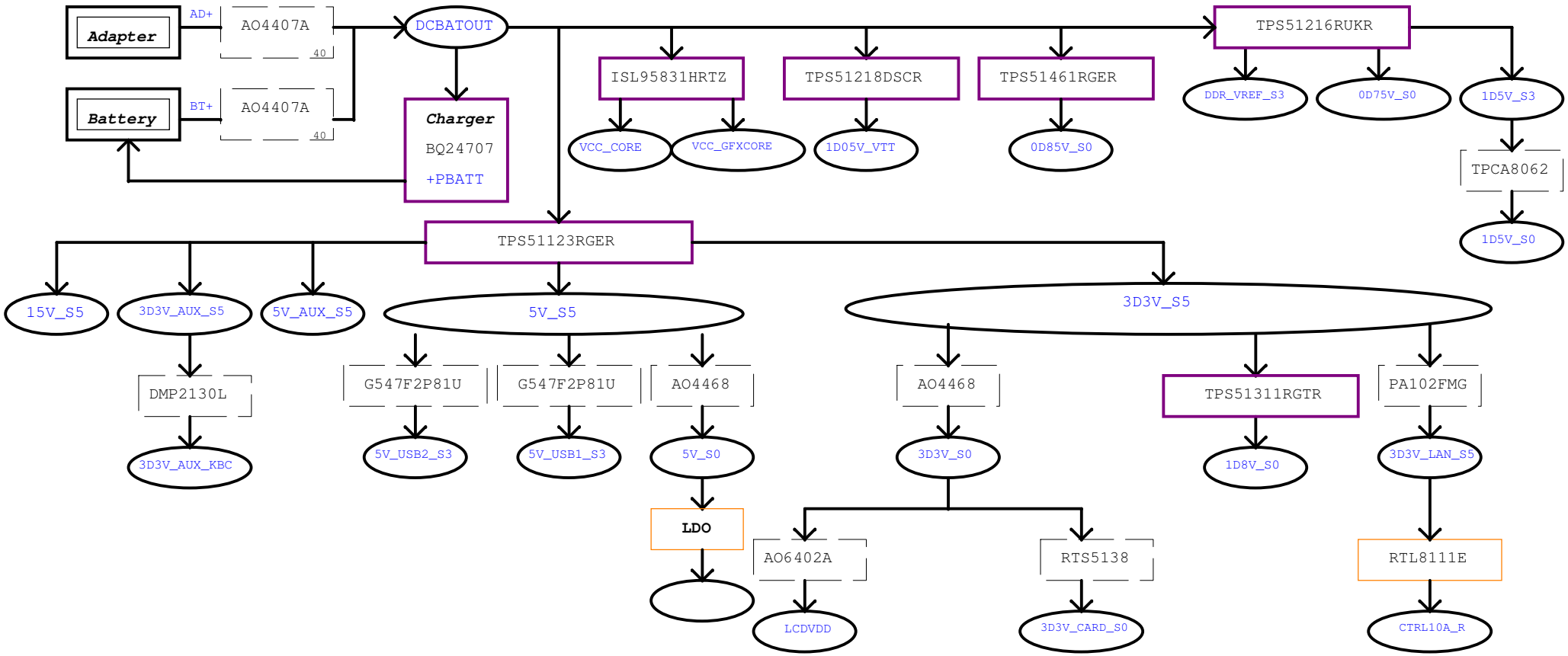

Power Shape

Regulator | **LDO** | **Switch**

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Title: ***Power Block Diagram***

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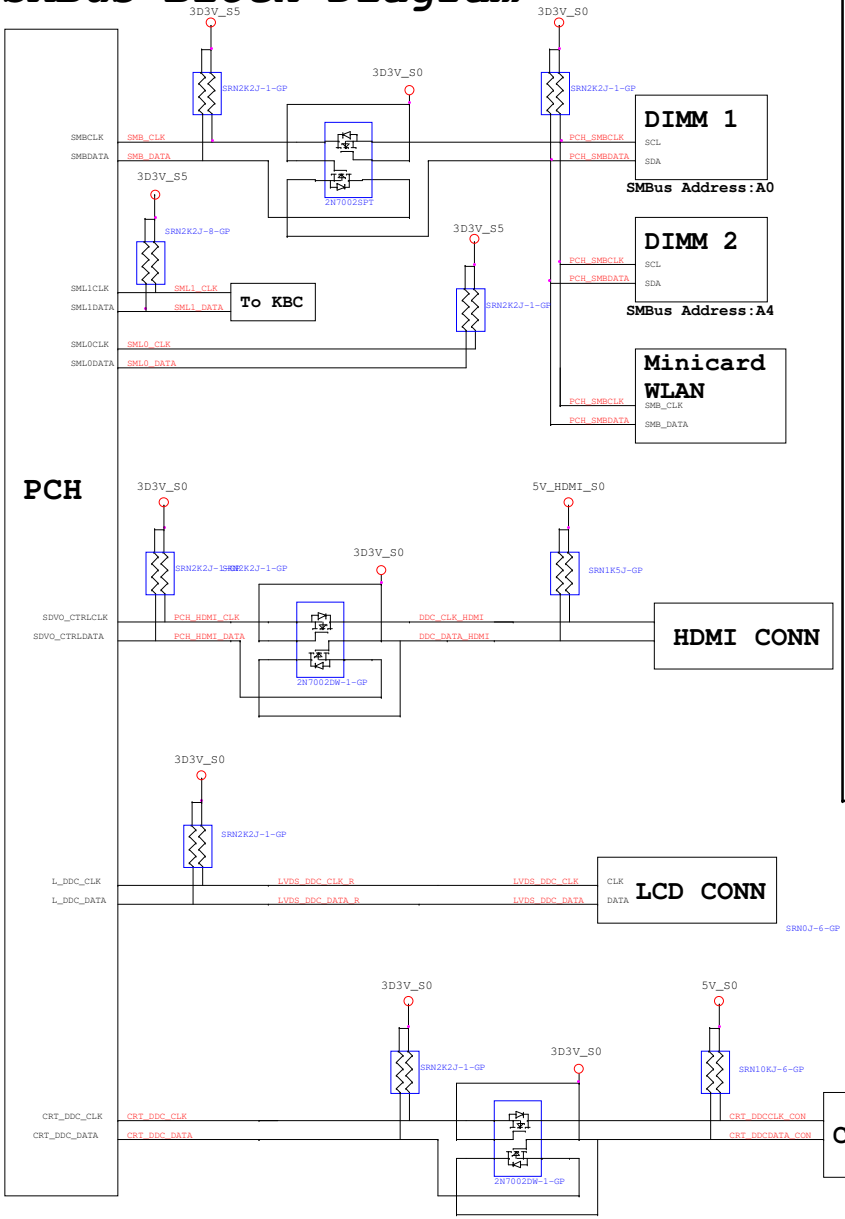
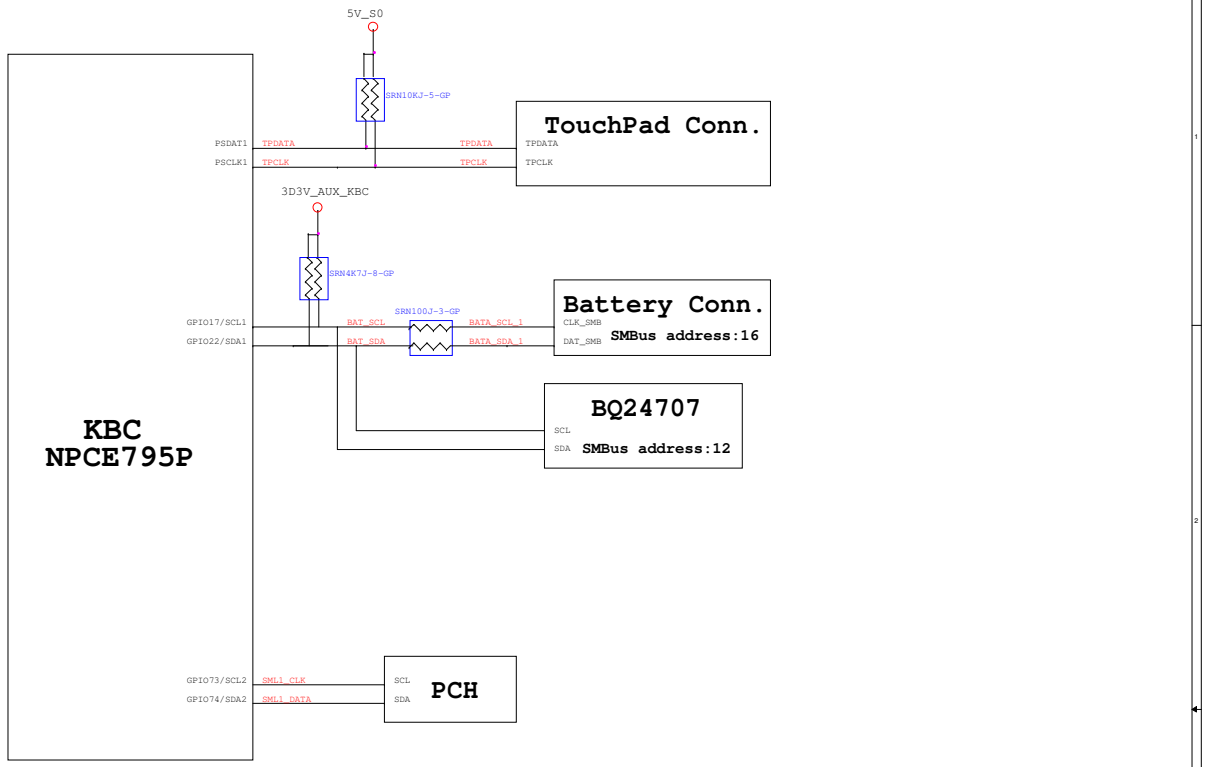
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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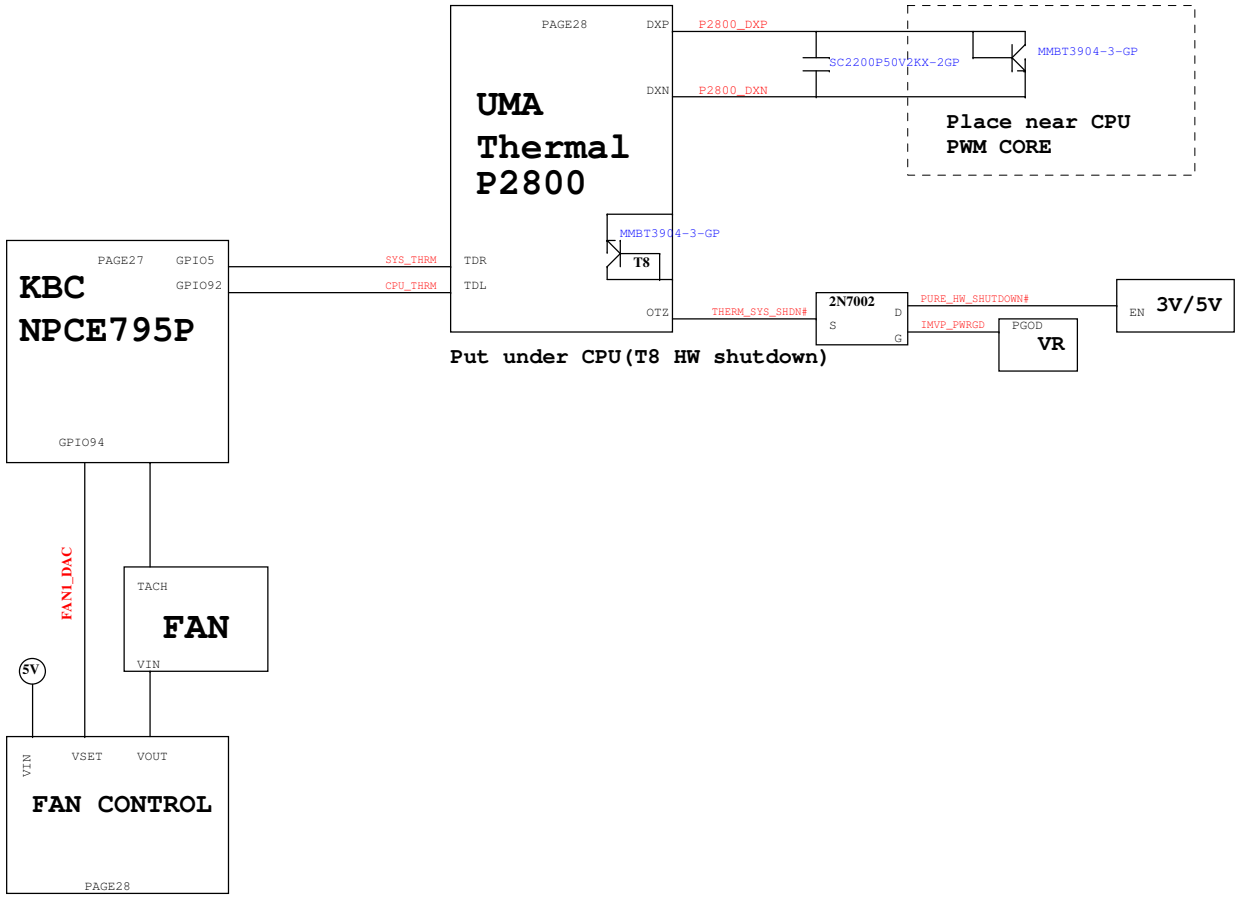
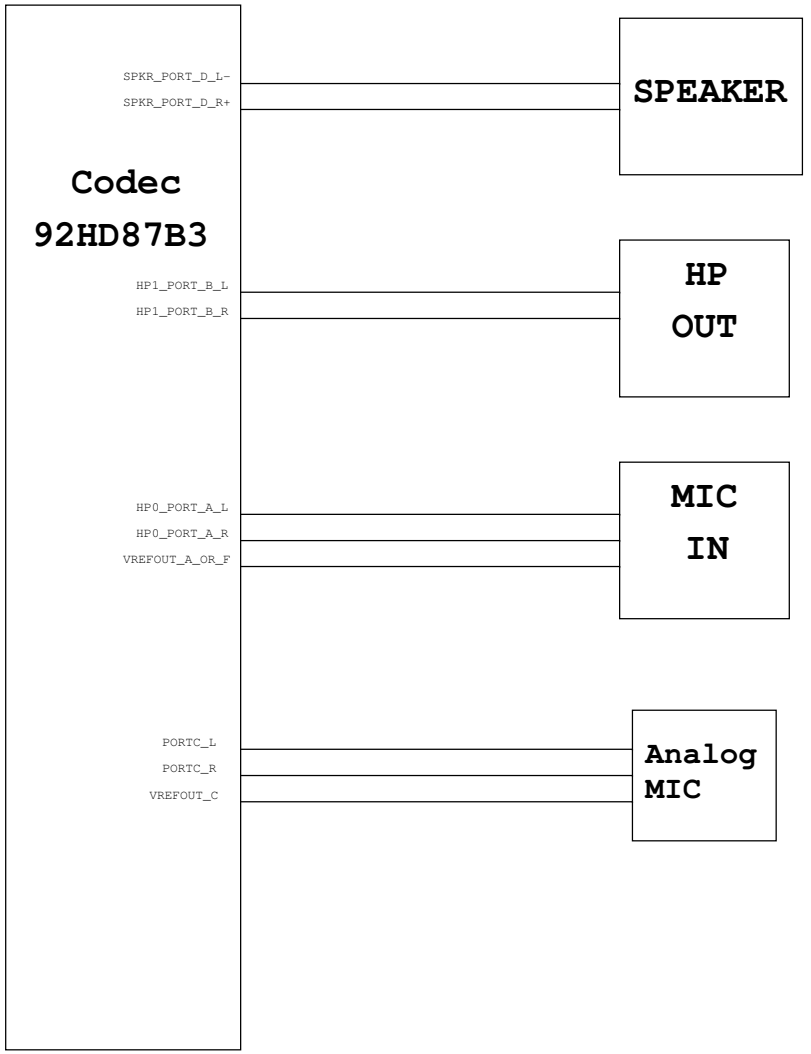
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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11/01	23		

DATA	PAGE	Change Item	Version
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Title: *Change History*

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DATA	PAGE	Change Item	Version

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Title
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