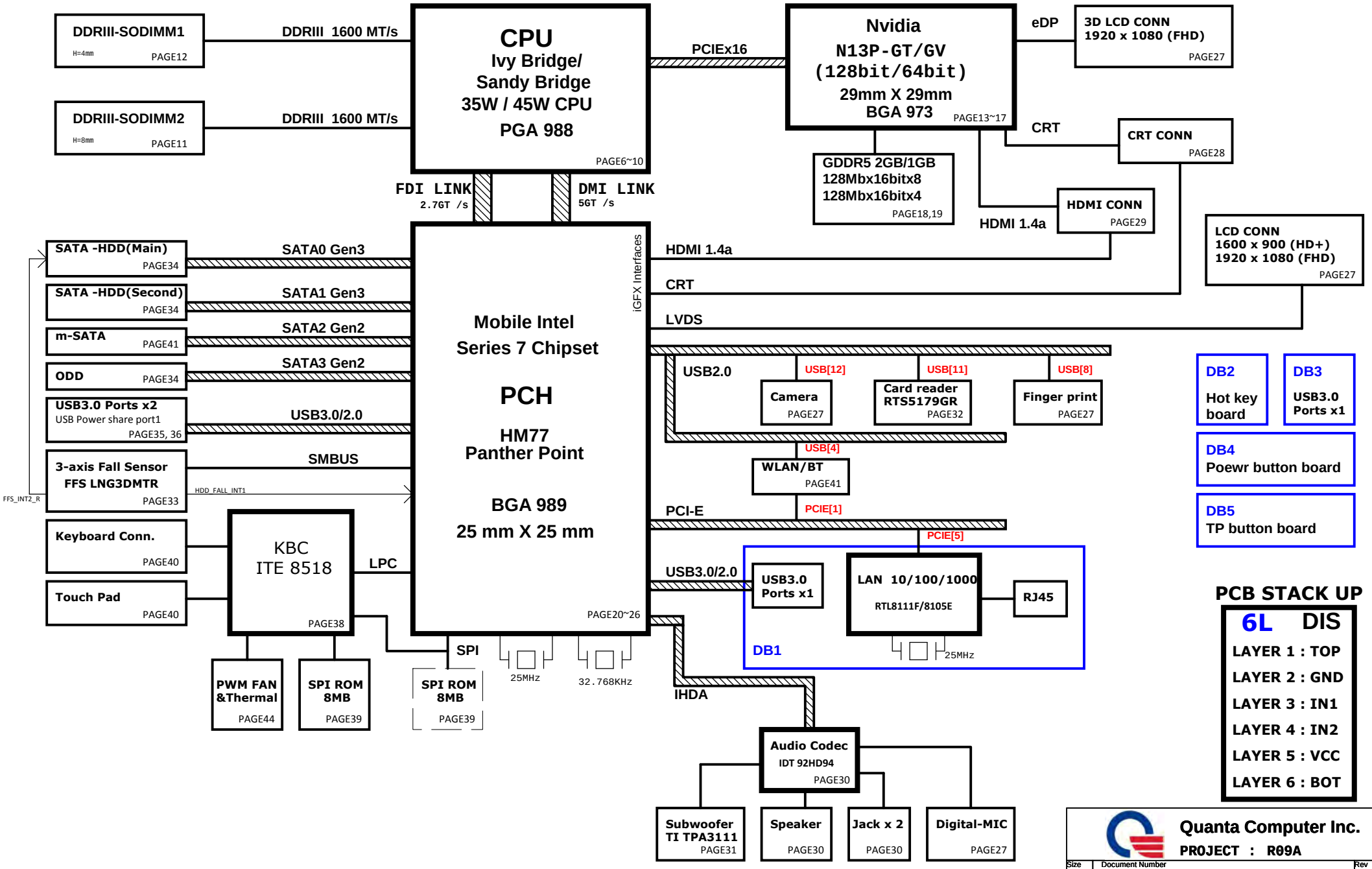
R09/A 17" OPT BLOCK DIAGRAM

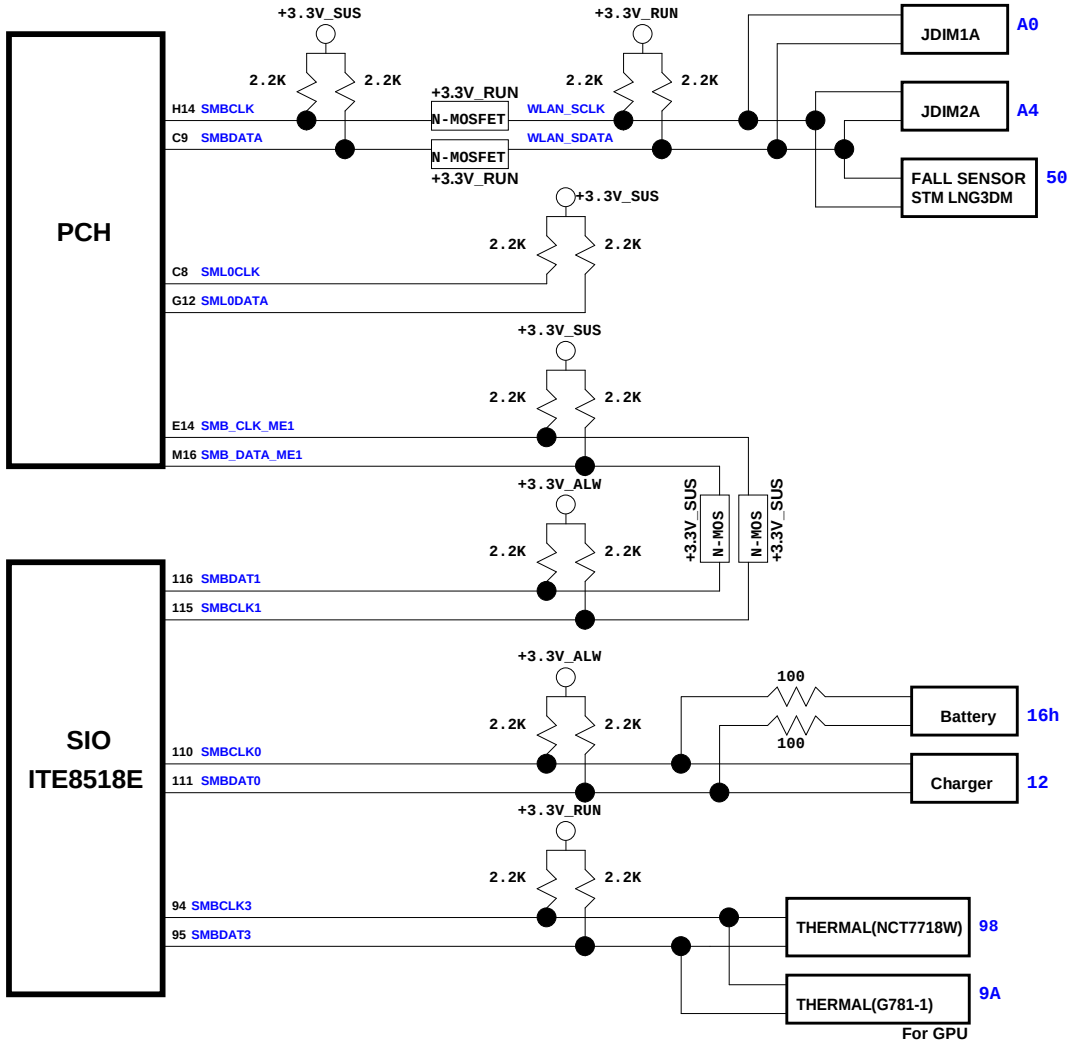


Quanta Computer Inc.

PROJECT : R09A

Size	Document Number	Rev
	BLOCK DIAGRAM	3A

Date: Monday, February 20, 2012 Sheet 1 of 58



Function	IC	SMBus Address
DDR3	JDIM1A JDIM2A	A0 A4
Thermal IC	G781-1P8	1001101xb (9Ah)
	EMC1422	1001100xb (98h)
Charge IC	BQ24707ARGRR	0b00010010 (0x12)
Battery	Battery	16h
Fall Sensor	LNG3DM	01010000 (50h)

Quanta Computer Inc.
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Size | Document Number: SMB/SCREW PAD | Rev 3A
Date: Wednesday, February 08, 2012 | Sheet 2 of 58

USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0 / Power share)
USB2	External port#3 (USB3.0)
USB3	External port#4 (USB3.0)
USB4	MiniCard 1 (WLAN/BT/WiMAX)
USB5	NC
USB6	X(FOR HM77)
USB7	X(FOR HM77)
USB8	Fingerprint
USB9	NC
USB10	Card Reader
USB11	Express Card
USB12	Camera
USB13	NC

SATA Master	Port Assignment
SATA0	HDD Main
SATA1	HDD Second
SATA2	mSATA
SATA3	ODD
SATA4	NC
SATA5	NC

PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	NC
PCIE 3	NC
PCIE 4	NC
PCIE 5	LAN
PCIE 6	NC
PCIE 7	NC
PCIE 8	NC

VER : 1A

Adapter 90W

Charger BQ24707RGRR

Battery 3S2P

PWR_SRC
Shapes: 280mil
Via: 10

+3.3V_EN2

ALW_ON

TI (PU1)
TPS51125ARGER

+3.3V_ALW
TDC: 6.2A
Shapes: 155mil
Via: ?

+5V_ALW
TDC: 10.8A
Shapes: 720mil
Via: ?

+15V_ALW

SIO_SLP_S3#

SIO_SLP_S4#

1.5V_SUS_PWRGD

TI(PU2)
TPS51216RUKR

LDO

+1.5V_SUS

+1.5V_SUS
TDC: 16A
Shapes: 326mil
Via: ?

+0.75V_DDR_VTT
TDC: 1A
Shapes: 40mil
Via: ?

VCCSA_EN

RichTek(PU4)
RT8241DGQW

+VCCSA_CORE
TDC: 4.2A
Shapes: 168mil
Via: ?

+3.3V_RUN

RichTek(PU3)
RT8240BGQW

+1.05V_PCH
TDC: 13.4A
Shapes: 415.6mil
Via: ?

IMVP_VR_ON

ON(PU7)
NCP6132A

PQ34

PQ35

PQ36

+VCC_CORE
TDC: 52A
Shapes: 1696mil
Via: ?

+VCC_iGFX_CORE
TDC: 38A
Shapes: 920mil
Via: ?

SUS_ON

Load Switch(PQ18)
FDC655BN

+3.3V_SUS
TDC: 0.226A
Shapes: 8mil
Via: ?

SUS_ON

Load Switch(PQ24)
FDC655BN

+5V_SUS
TDC: 0.1A
Shapes: 56.4mil
Via: ?

RUN_ON

Load Switch(PQ17)
MDV1522URH

+5V_RUN
TDC: 4.13A
Shapes: 140mil
Via: ?

RUN_ON

Load Switch(PQ25)
FDC655BN

+1.5V_RUN
TDC: 0.922A
Shapes: 40mil
Via: ?

DGPU_PWR_ON#

Load Switch(PQ26)
MDV1522URH

For dGPU only

+1.5V_GFX
TDC: 7.9A
Shapes: 40mil
Via: ?
For dGPU

SIO_SLP_S3#

Load Switch(Q4)
AON7410

+1.5V_CPU
TDC: 5A
Shapes: 200mil
Via: ?

DGFX_VR_PWRGD

Load Switch(PQ28)
MDV1522URH

For dGPU only

+1.05V_GFX
TDC: 2.7A
Shapes: 40mil
Via: ?

RUN_ON

Load Switch(PQ23)
MDV1522URH

+3.3V_RUN
TDC: 2.6A
Shapes: 140.8mil
Via: ?

DGPU_PWR_EN

Load Switch(PQ20)
FDC655BN

For dGPU only

+3.3V_GFX
TDC: 0.966A
Shapes: 8mil
Via: ?

1.05V_PCH_PWRGD

RichTek(PU5)
RT8068AZQW

+1.8V_RUN
TDC: 0.869A
Shapes: 40.8mil
Via: ?

+3V_GFX

ON(PU10)
NCP3218MNR2G

For dGPU only

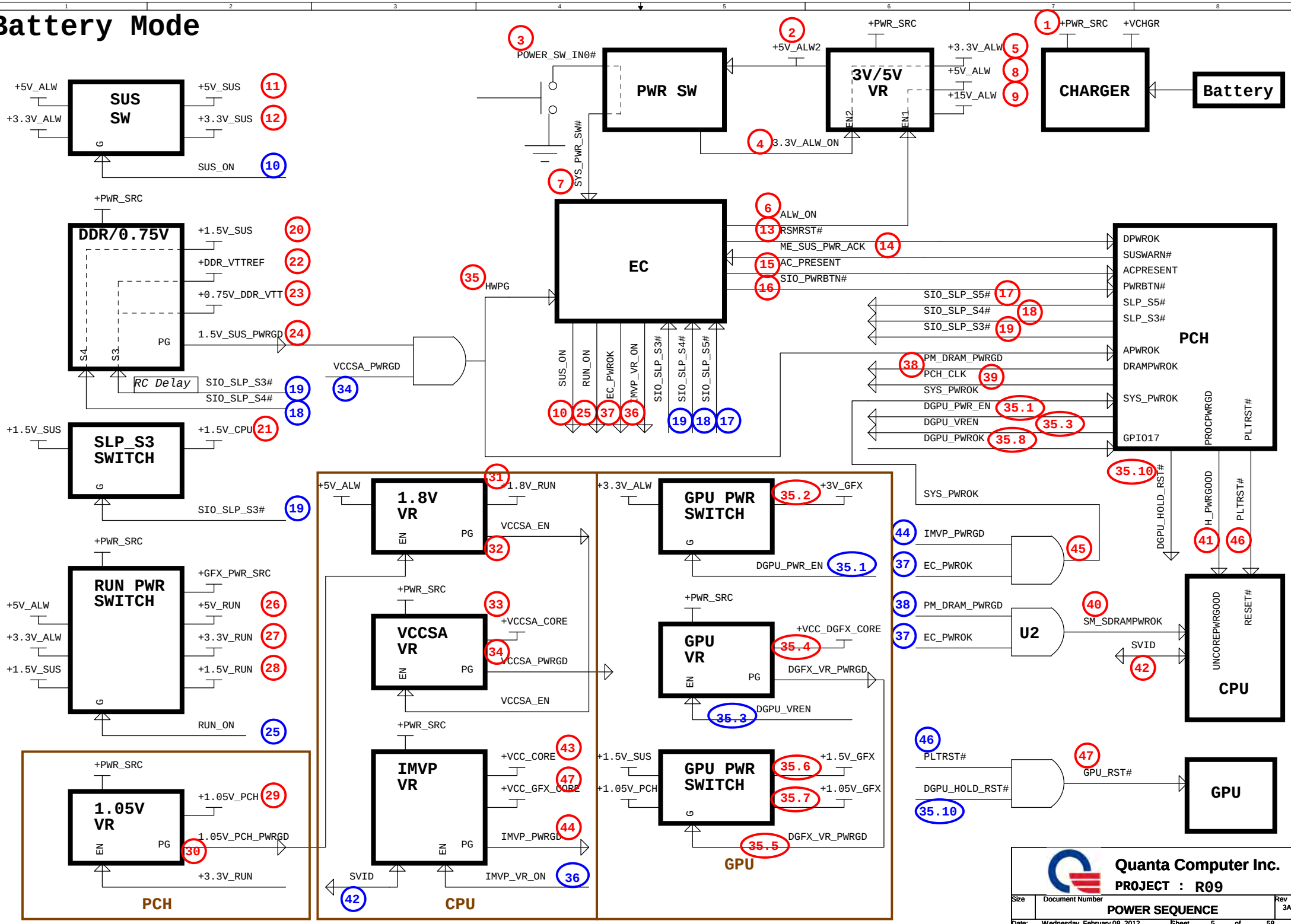
+VCC_DGFX_CORE
TDC: 60A
Shapes: 1600mil
Via: ?

Quanta Computer Inc.
PROJECT : R09A

Size	Document Number	Rev
	Power Block Diagram	3A

Date: Wednesday, February 08, 2012 Sheet 4 of 58

Battery Mode



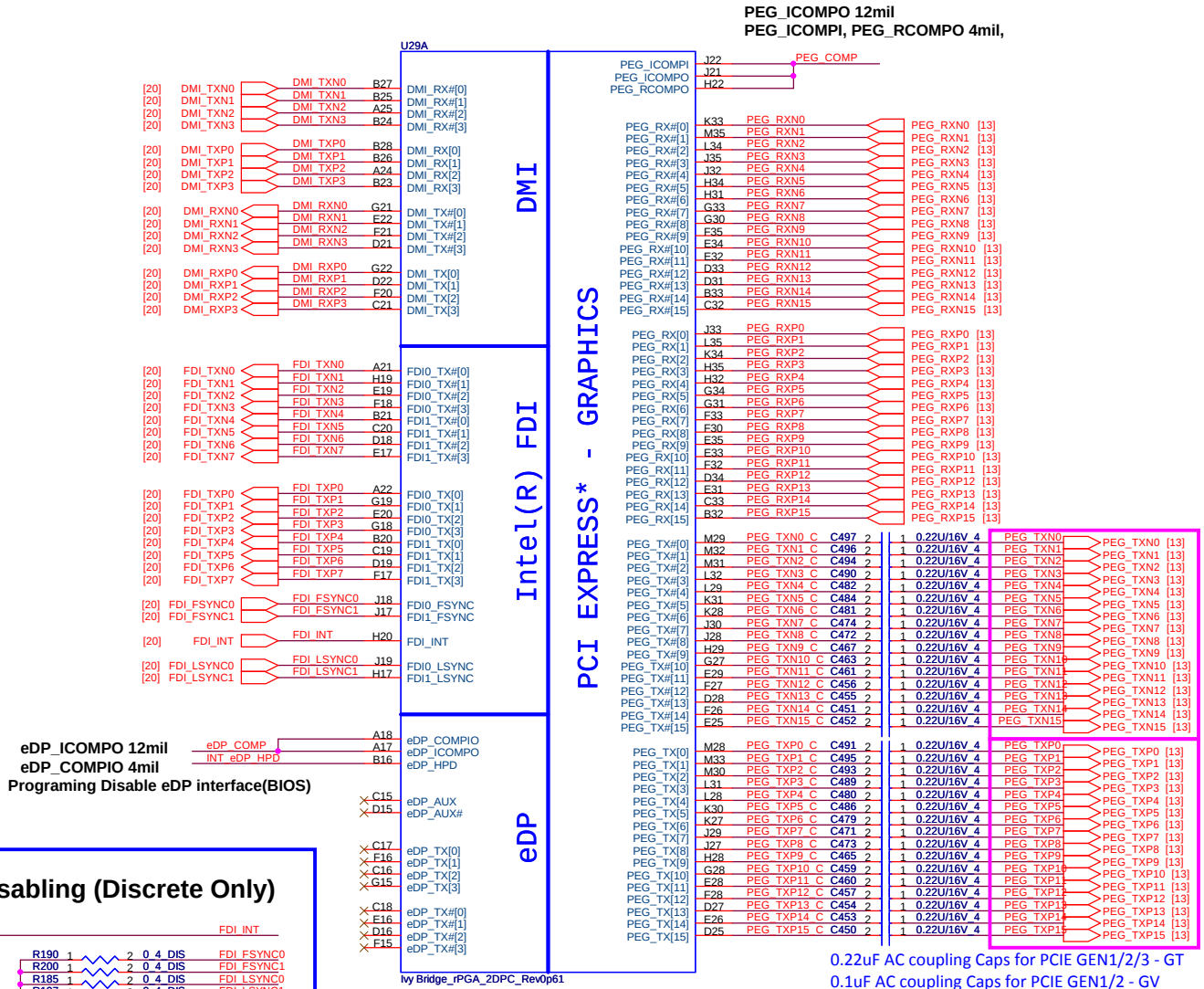
Quanta Computer Inc.

PROJECT : R09

Size	Document Number	Rev
	POWER SEQUENCE	3A

Date: Wednesday, February 08, 2012 Sheet 5 of 58

Ivy Bridge Processor (RESERVED, CFG)

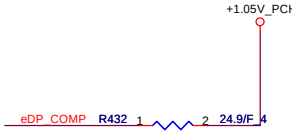


PEG_ICOMPO 12mil
PEG_ICOMPI, PEG_RCOMPO 4mil,

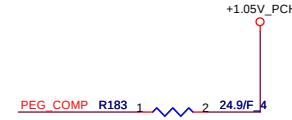
eDP_ICOMPO 12mil
eDP_COMPIO 4mil
Programing Disable eDP interface(BIOS)

0.22uF AC coupling Caps for PCIE GEN1/2/3 - GT
0.1uF AC coupling Caps for PCIE GEN1/2 - GV

DP & PEG Compensation



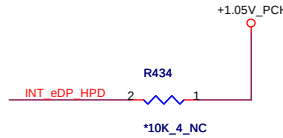
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed within 500 mils



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils

PEG_ICOMPO signals should be routed within 500 mils

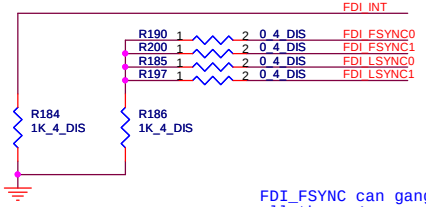
eDP Hot-plug (Disable)



CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

FDI Disabling (Discrete Only)



DIS: POP
UMA/ OTP: NC

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

VGA(U3)	AC coupling Cap	PN	TX location	RX location(page13)
N13P-GV	0.1uF CAP CHIP 0.1U 16V(10%,X7R,0402)	CH4103K1B08	C452,C451,C455, C456,C461,C463, C467,C472,C450, C453,C454,C457, C460,C459,C465, C473	C125,C126,C147 C145,C123,C124 C152,C153,C121 C122,C151,C150 C119,C120,C149 C148
N13P-GT	0.22uF CAP CHIP 0.22U 16V(10%,X7R,0402)	CH4223K1B00	ALL	ALL

Quanta Computer Inc.
PROJECT : R09A

Size	Document Number	Rev
	Ivy Bridge 1/5	3A
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Ivy Bridge Processor (CLK,MISC,JTAG)

U29B

SNB_IVB# N.A at SNB EDS #27637 0.7v1

[23] H_SNB_IVB# — H_SNB_IVB# — C26 PROC_SELECT#

[38] H_CPUDET# — H_CPUDET# — AN34 SKTOCC#

MISC

TP1 — CATERR# — AL33 CATERR#

[38] PECI_EC — PECI_EC — R150 43_4 — PECI_EC_R — AN33 PECI

[38,53,55] IMVP7_PROCHOT# — IMVP7_PROCHOT# — R151 56_4 — H_PROCHOT# — AL32 PROCHOT#

THERMAL

Over 130 degree C will drive low

[25] PM_THRMTRIP# — PM_THRMTRIP# — AN32 THERMTRIP#

[20] H_PM_SYNC — H_PM_SYNC — AM34 PM_SYNC

[25] H_PWRGOOD — H_PWRGOOD — AP33 UNCOREPWRGOOD

10K_4 — R136

SM_DRAMPWROK — V8 SM_DRAMPWROK

PWR MANAGEMENT

[13,23,38,41,57] PLTRST# — PLTRST# — R146 1.5K/F_4 — CPU_PLTRST#_R — AR33 RESET#

R147 750/F_4

Ivy Bridge_rPGA_2DPC_Rev0p61

Intel spec VinH min =VCCIO X 0.7

CLOCKS

BCLK A28 — CLK_CPU_BCLKP — CLK_CPU_BCLKP [24]

BCLK# A27 — CLK_CPU_BCLKN — CLK_CPU_BCLKN [24]

DPLL_REF_CLK A16 — CLK_DP_P_R — R439 1K_4

DPLL_REF_CLK# A15 — CLK_DP_N_R — R438 1K_4 — +1.05V_PCH

For internal eDP (Disable)

DDR3 MISC

SM_DRAMRST# — R8 — CPU_DRAMRST#

SM_RCOMP[0] AK1 — SM_RCOMP_0 — R236 140/F_4

SM_RCOMP[1] A5 — SM_RCOMP_1 — R231 25.5/F_4

SM_RCOMP[2] A4 — SM_RCOMP_2 — R230 200/F_4

SM_RCOMP_0, SM_RCOMP_1 20mil / SM_RCOMP_2 15mil.

JTAG & BPM

PRDY# AP29

PREQ# AP27

TCK AR26 — XDP_TCLK — P3

TMS AR27 — XDP_TMS — P5

TRST# AP30 — XDP_TRST# — P7

TDI AR28 — XDP_TDI — P6

TDO AP26 — XDP_TDO — P4

DBR# AL35 — XDP_DBRST# — R152 1K_4 — +3.3V_RUN

BPM#[0] AT28

BPM#[1] AR29

BPM#[2] AR30

BPM#[3] AT30

BPM#[4] AP32

BPM#[5] AR31

BPM#[6] AT31

BPM#[7] AR32

+1.05V_PCH

XDP_TMS — R142 *51_4_NC

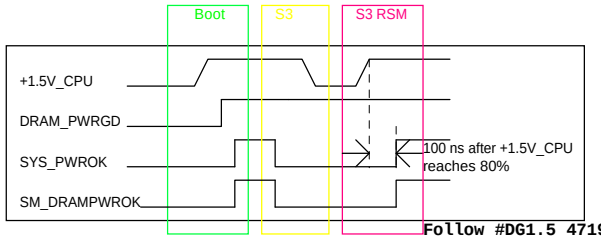
XDP_TDI — R143 *51_4_NC

XDP_TDO — R141 *51_4_NC

IMVP7_PROCHOT# — R139 62_4

XDP_TCLK — R129 *51_4_NC

XDP_TRST# — R144 *51_4_NC



Follow #DG1.5 471984 P119

Follow #DG1.5 471984 P130
DRAMRST# Routing Illustration

+1.5V_SUS

R463 1K_4

Q45 2N7002W

[11,12] DDR3_DRAMRST# — DDR3_DRAMRST# — R464 1K_4 — DDR3_DRAMRST#_R — CPU_DRAMRST#

[9,24] DDR_HVREF_RST_PCH — DDR_HVREF_RST_PCH

+3.3V_SUS — R462 1K_4

C586 0.047U/10V_4

R461 4.99K/F_4

Follow #DG1.5 471984 P128
DDR Power Gating Topology

+3.3V_SUS

R460 200_4

C585 0.1U/16V_4

U30

[20] PM_DRAM_PWRGD — PM_DRAM_PWRGD

[20,38] EC_PWROK

SM_DRAMPWROK_R

74AHC1G09GW

+1.5V_CPU

R229 200_4

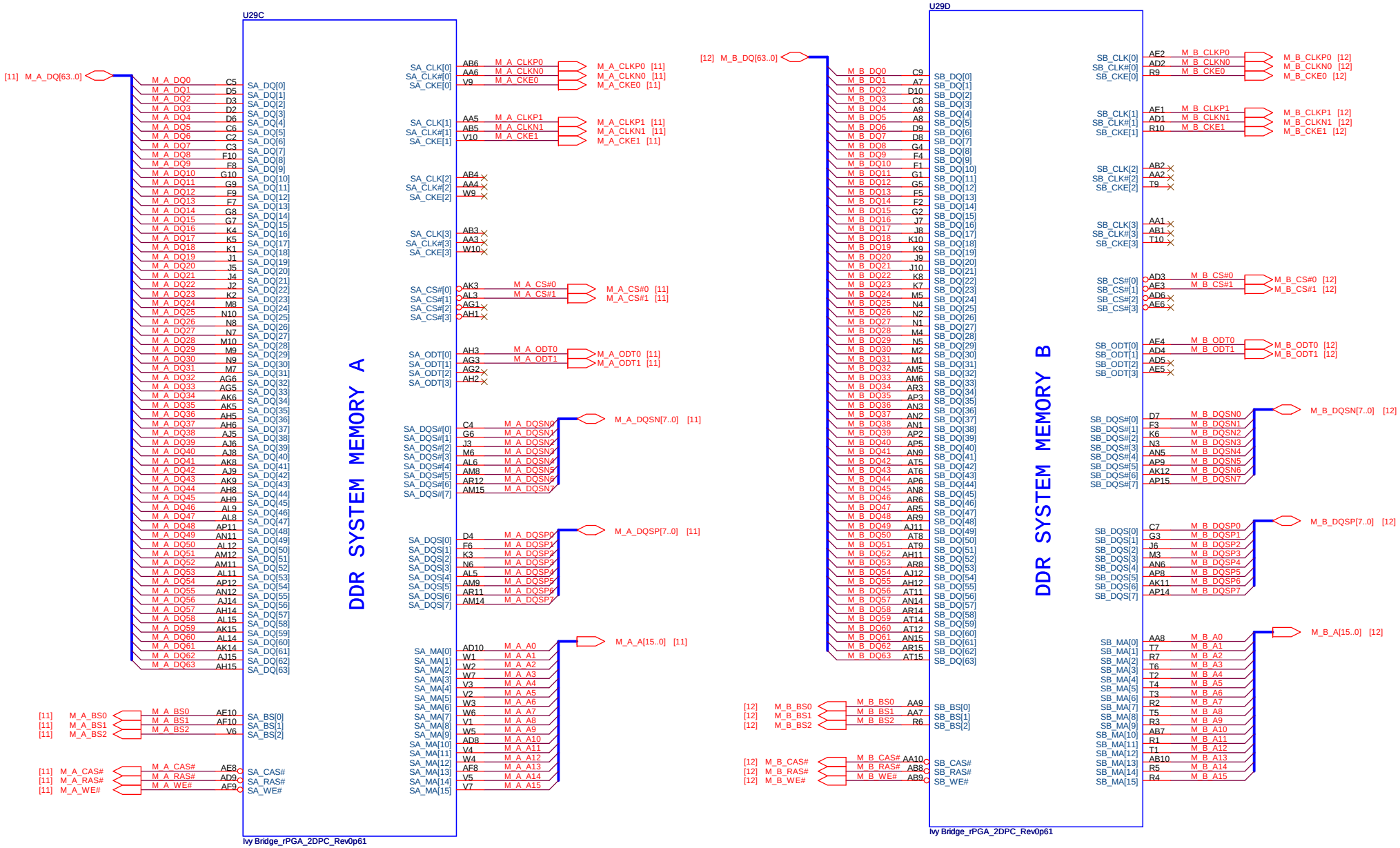
R225 130_4 — SM_DRAMPWROK

when 1,2 is high, 4 is high-impedance OFF-state

Quanta Computer Inc.
PROJECT : R09A

Size	Document Number	Rev
	Ivy Bridge 2/5	3A
Date: Friday, March 02, 2012	Sheet 7 of 58	

Ivy Bridge Processor (DDR3)



Quanta Computer Inc.

PROJECT : R09A

Size	Document Number	Rev
	Ivy Bridge 3/5	3A

Date: Wednesday, February 08, 2012 Sheet 8 of 58

Ivy Bridge Processor (GRAPHIC POWER)

35W	16pcs
45W	24pcs

CPU Core Power
IVY, SNB: 35W ~ 53A
IVY, SNB: 45W ~ 94A
10F x24

1.05V_PCH
SNB: 8.5A
IVY: 8.5A
10F x12

CPU VGT
SNB: 33A
IVY: 33A
10uF x 12

CPU VCCPL
SNB: 1.2A
IVY: 1.2A
10uF x 1
1uF x 2

CPU MCH
SNB: 5A
IVY: 5A
10uF x 6

CPU SA
SNB: 6A
IVY: 6A
10uF x 3

OTP/UMA : POP
DIS : NC

For internal GFX

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

DIS	0 ohm	C221,C223,C215
	CS00003J951	
	RESISTOR CHIP 0 1/10W+-5%(0603)	

UMA/OPT	C548,C202,C539,C530,C221, C536,C554,C219,C223,C217, C213,C215
10uF	
	CH6101M9905
	CAP CHIP 10U 6.3V(+-20%,X5R,0603)

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
VCC_SENSE / VSS_SENSE	100Ω	27-33Ω	<25 mils
VCCAXG_SENSE / VSSAXG_SENSE	100Ω		
VCCIO_SENSE / VSS_SENSE_VCCIO	10Ω	55Ω	
VCCSA	100Ω		

M3 VREF
Vgs=2.5V Rds=115m

S3 Power reduce
5A

Take care Q20 Vgs(MAX)=2.5

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

Place PU resistor close to CPU
SVID DATA
R148 130_4

Place PU resistor close to CPU
SVID ALERT
R138 75/F
R149 43_4

R34 and R36 pull-down 1K
Spec:This will ensure the VID is 00 prior to VCCIO stability.

Ivy Bridge_rPGA_2DPC_Rev0p61

Quanta Computer Inc.
PROJECT : R09A

Size	Document Number	Rev
	Ivy Bridge 4/5	3A
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Ivy Bridge Processor (GND)

U29H

VSS

Ivy Bridge_rPGA_2DPC_Rev0p61

U29I

VSS

Ivy Bridge_rPGA_2DPC_Rev0p61

Ivy Bridge Processor (RESERVED, CFG)

U29E

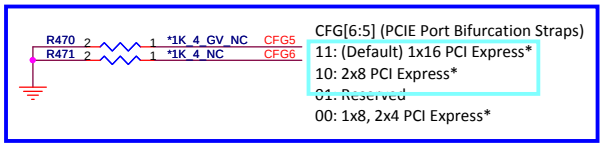
CFG

RESERVED

Ivy Bridge_rPGA_2DPC_Rev0p61

#27636 SNB EDS0.7v1 no function.

GV - R470 POP
GT, UMA - ALL NC



Processor Strapping

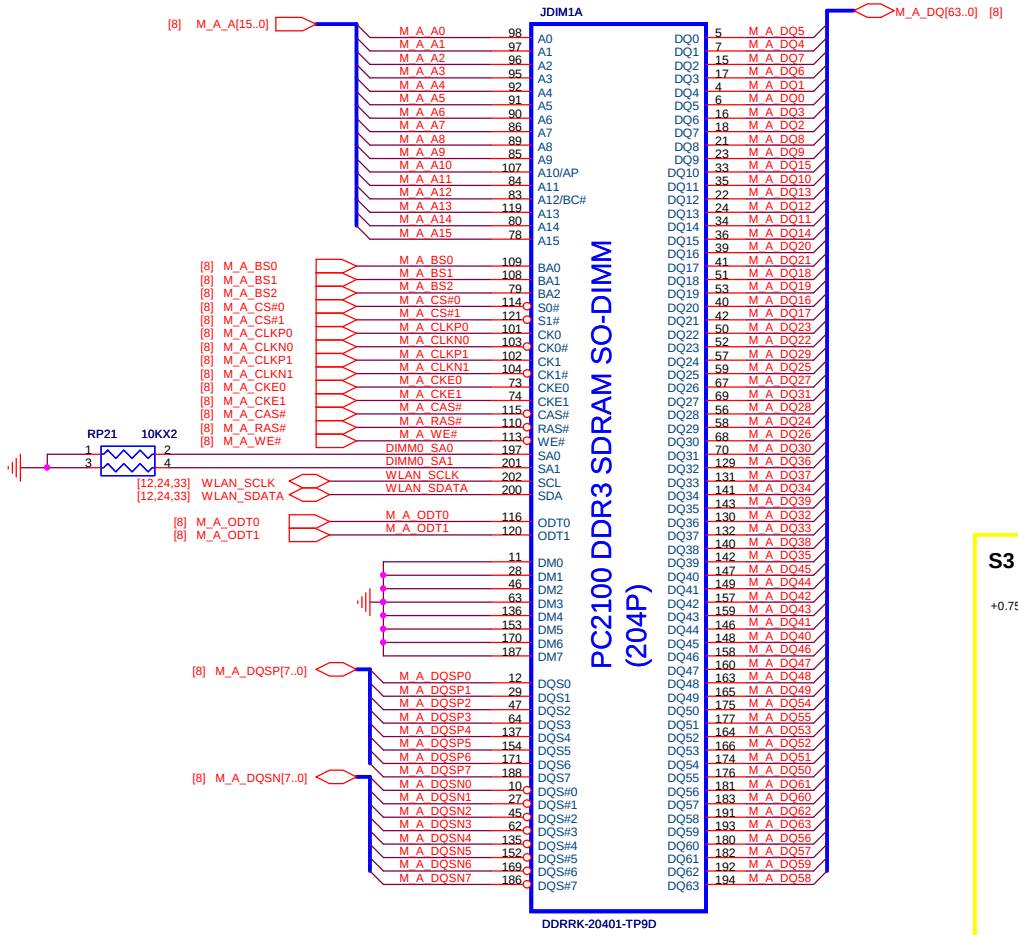
The CFG signals have a default value of '1' if not terminated on the board.

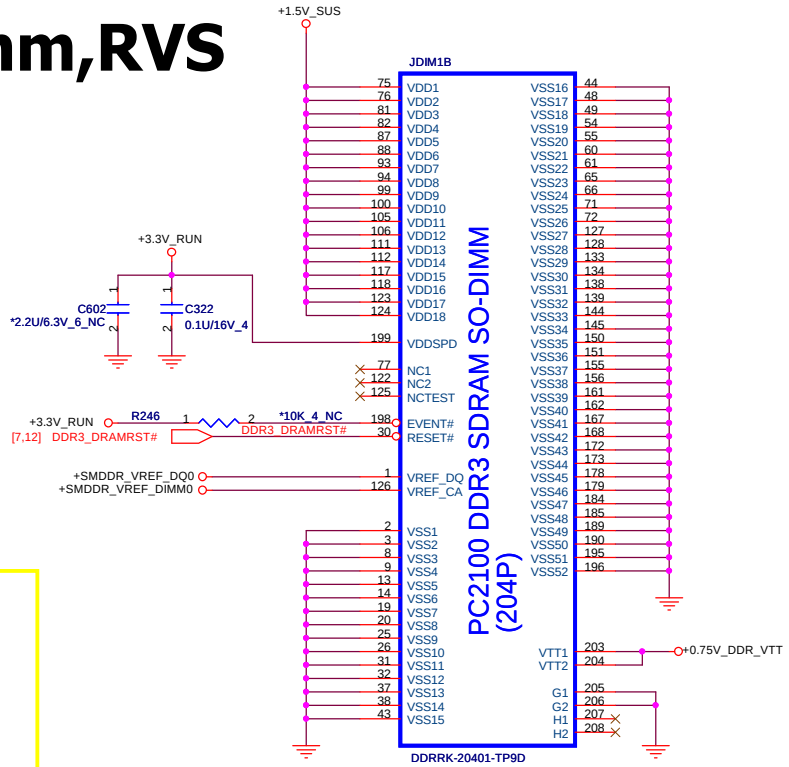
	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed CFG2 — R145 1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

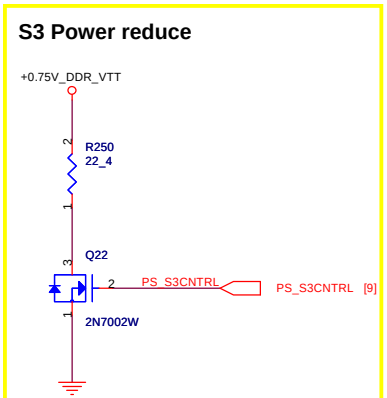
Quanta Computer Inc.
PROJECT : R09A

Size	Document Number	Rev
	Ivy Bridge 5/5	3A
Date: Saturday, March 03, 2012	Sheet 10 of 58	

H=9.2mm,RVS

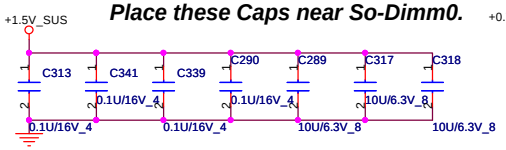


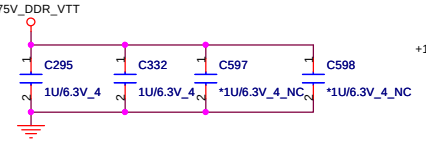




M1 VREF

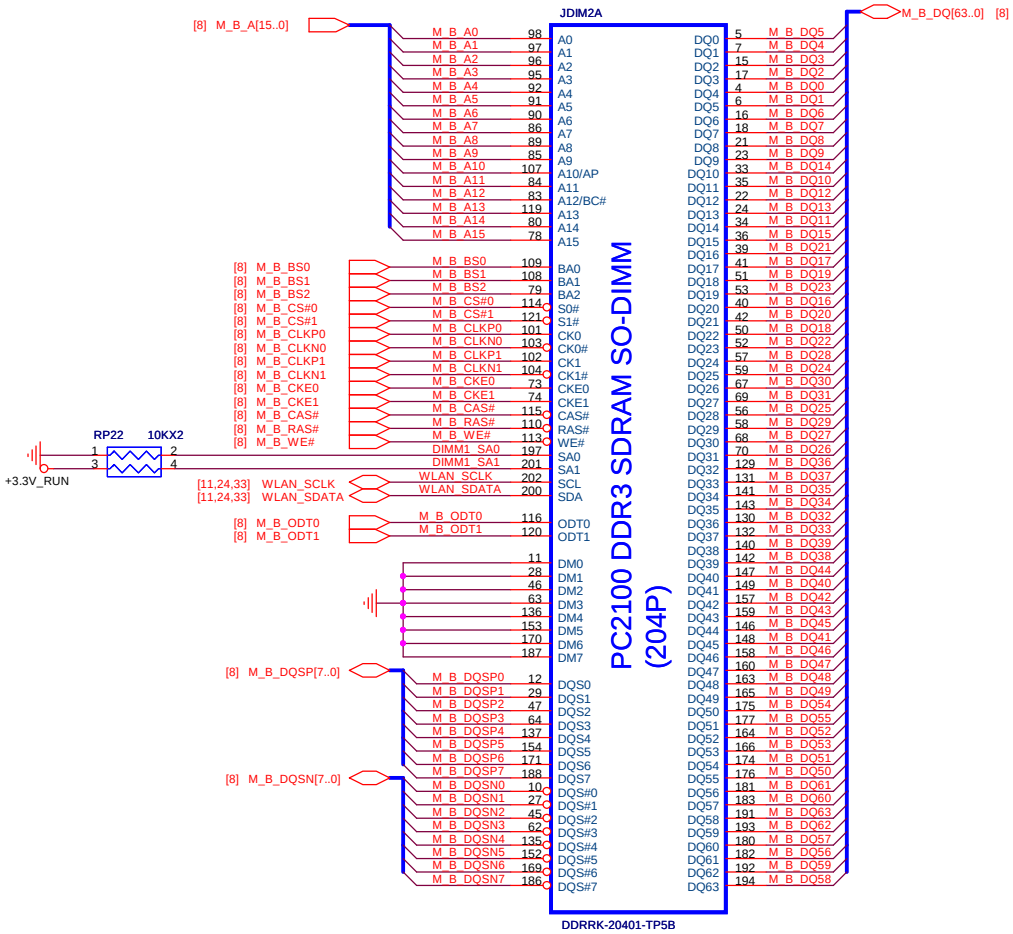
Place these Caps near So-Dimm0.



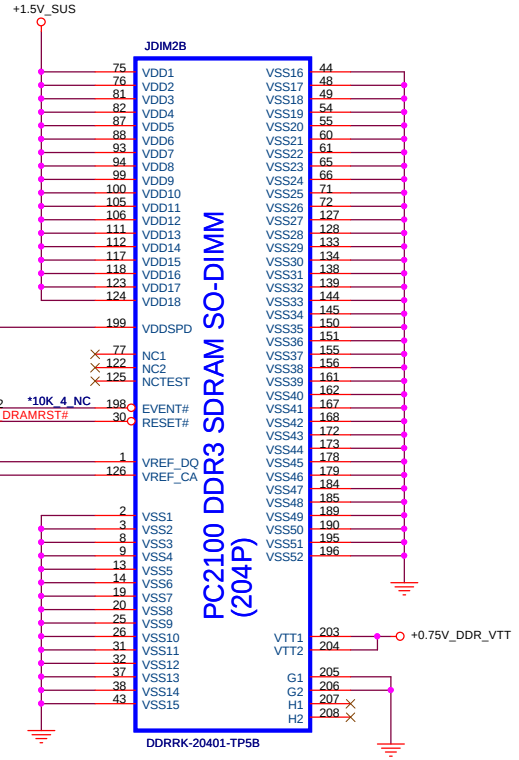


M3 VREF

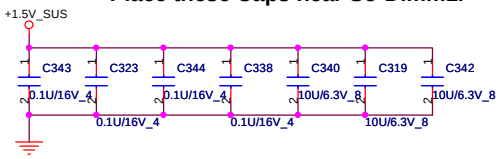
Quanta Computer Inc.
PROJECT : R09A
Size | Document Number: DDR3 DIMM-0 | Rev: 3A
Date: Wednesday, February 08, 2012 | Sheet 11 of 58

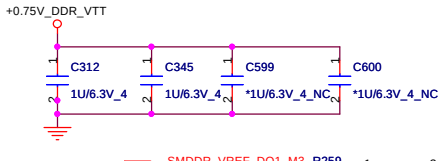


H=5.2mm,RVS

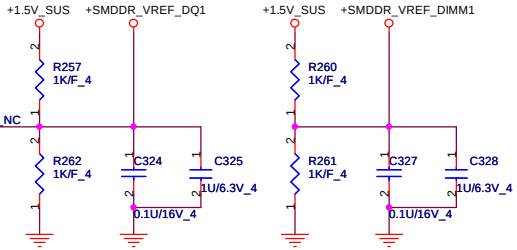


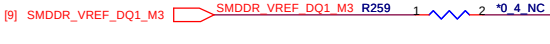
Place these Caps near So-Dimm1.





M1 VREF





M3 REF

Quanta Computer Inc.			
PROJECT : R09A			
Size	Document Number		Rev
	DDR3 DIMM-1		3A
Date:	Wednesday, February 08, 2012	Sheet 12 of 58	

PEX_IOVDD/Q <3.3A

U24A
N13P-GT-A2

+1.05V_GFX
C89 0.1U/16V_4
C45 1U/6.3V_4
C70 10U/6.3V_6
C104 10U/6.3V_6
AG19 AG21 AG22 AG24 AH21 AH25
PEX_IOVDD_1 PEX_IOVDD_2 PEX_IOVDD_3 PEX_IOVDD_4 PEX_IOVDD_5 PEX_IOVDD_6

+1.05V_GFX
C46 0.047U/10V_4
C61 0.1U/16V_4
C53 1U/6.3V_4
C75 1U/6.3V_4
C77 10U/6.3V_6
C65 10U/6.3V_6
C476 0.1U/16V_4
AG13 AG15 AG16 AG18 AG25 AH15 AH18 AH26 AH27 AJ27 AK27 AL27 AM28 AN28
PEX_IOVDDQ_1 PEX_IOVDDQ_2 PEX_IOVDDQ_3 PEX_IOVDDQ_4 PEX_IOVDDQ_5 PEX_IOVDDQ_6 PEX_IOVDDQ_7 PEX_IOVDDQ_8 PEX_IOVDDQ_9 PEX_IOVDDQ_10 PEX_IOVDDQ_11 PEX_IOVDDQ_12 PEX_IOVDDQ_13 PEX_IOVDDQ_14

GB4-128

PCI EXPRESS

C35 1U/25V_6
C19 1U/6.3V_4
+3.3V_GFX
J8 K8 L8 M8
VDD33_1 VDD33_2 VDD33_3 VDD33_4

C5 0.1U/16V_4
C28 0.1U/16V_4
+VCC_DGFX_CORE
R41 100_4
[56] VDD_SENSE
[56] GND_SENSE
R40 100_4
L4 L5
VDD_SENSE GND_SENSE

12~16 mils width
+1.05V_GFX
L8 BLM18AG121SN1D
150mA
C85 0.1U/16V_4
C98 1U/6.3V_4
C102 1U/25V_6
+PEX_PLLVDD AG26
PEX_PLLVDD

+3.3V_GFX
C36 0.1U/16V_4
C6 1U/25V_6
P8 AG12
3V3AUX_NC
PEX_SVDD_3V3
210mA 12~16 mils width
AH12
PEX_PLL_HVDD
AJ11
PEX_WAKE#

PEX_RX0 PEX_RX0* PEX_RX1 PEX_RX1* PEX_RX2 PEX_RX2* PEX_RX3 PEX_RX3* PEX_RX4 PEX_RX4* PEX_RX5 PEX_RX5* PEX_RX6 PEX_RX6* PEX_RX7 PEX_RX7* PEX_RX8 PEX_RX8* PEX_RX9 PEX_RX9* PEX_RX10 PEX_RX10* PEX_RX11 PEX_RX11* PEX_RX12 PEX_RX12* PEX_RX13 PEX_RX13* PEX_RX14 PEX_RX14* PEX_RX15 PEX_RX15*
AN12 AM12 AN14 AM14 AP14 AP15 AN15 AM15 AN17 AM17 AP17 AP18 AN18 AM18 AN20 AM20 AP20 AP21 AN21 AM21 AN23 AM23 AP23 AP24 AN24 AM24 AN26 AM26 AP26 AP27 AN27 AM27
PEG_TXP15 PEG_TXN15 PEG_TXP14 PEG_TXN14 PEG_TXP13 PEG_TXN13 PEG_TXP12 PEG_TXN12 PEG_TXP11 PEG_TXN11 PEG_TXP10 PEG_TXN10 PEG_TXP9 PEG_TXN9 PEG_TXP8 PEG_TXN8 PEG_TXP7 PEG_TXN7 PEG_TXP6 PEG_TXN6 PEG_TXP5 PEG_TXN5 PEG_TXP4 PEG_TXN4 PEG_TXP3 PEG_TXN3 PEG_TXP2 PEG_TXN2 PEG_TXP1 PEG_TXN1 PEG_TXP0 PEG_TXN0
PEG_TXP15 [6] PEG_TXN15 [6] PEG_TXP14 [6] PEG_TXN14 [6] PEG_TXP13 [6] PEG_TXN13 [6] PEG_TXP12 [6] PEG_TXN12 [6] PEG_TXP11 [6] PEG_TXN11 [6] PEG_TXP10 [6] PEG_TXN10 [6] PEG_TXP9 [6] PEG_TXN9 [6] PEG_TXP8 [6] PEG_TXN8 [6] PEG_TXP7 [6] PEG_TXN7 [6] PEG_TXP6 [6] PEG_TXN6 [6] PEG_TXP5 [6] PEG_TXN5 [6] PEG_TXP4 [6] PEG_TXN4 [6] PEG_TXP3 [6] PEG_TXN3 [6] PEG_TXP2 [6] PEG_TXN2 [6] PEG_TXP1 [6] PEG_TXN1 [6] PEG_TXP0 [6] PEG_TXN0 [6]

PEX_TX0 PEX_TX0* PEX_TX1 PEX_TX1* PEX_TX2 PEX_TX2* PEX_TX3 PEX_TX3* PEX_TX4 PEX_TX4* PEX_TX5 PEX_TX5* PEX_TX6 PEX_TX6* PEX_TX7 PEX_TX7* PEX_TX8 PEX_TX8* PEX_TX9 PEX_TX9* PEX_TX10 PEX_TX10* PEX_TX11 PEX_TX11* PEX_TX12 PEX_TX12* PEX_TX13 PEX_TX13* PEX_TX14 PEX_TX14* PEX_TX15 PEX_TX15*
AK14 AJ14 AH14 AG14 AK15 AJ15 AL16 AK16 AK17 AJ17 AH17 AG17 AK18 AJ18 AL19 AK19 AK20 AJ20 AH20 AG20 AK21 AJ21 AL22 AK22 AK23 AJ23 AH23 AG23 AK24 AJ24 AL25 AK25
PEG_RXP15_C PEG_RXN15_C PEG_RXP14_C PEG_RXN14_C PEG_RXP13_C PEG_RXN13_C PEG_RXP12_C PEG_RXN12_C PEG_RXP11_C PEG_RXN11_C PEG_RXP10_C PEG_RXN10_C PEG_RXP9_C PEG_RXN9_C PEG_RXP8_C PEG_RXN8_C PEG_RXP7_C PEG_RXN7_C PEG_RXP6_C PEG_RXN6_C PEG_RXP5_C PEG_RXN5_C PEG_RXP4_C PEG_RXN4_C PEG_RXP3_C PEG_RXN3_C PEG_RXP2_C PEG_RXN2_C PEG_RXP1_C PEG_RXN1_C PEG_RXP0_C PEG_RXN0_C
C125 C126 C147 C145 C123 C124 C152 C153 C121 C122 C151 C150 C119 C120 C149 C148 C128 C127 C161 C160 C129 C130 C158 C159 C157 C156 C134 C133 C155 C154 C131 C132
0.22U/16V
PEG_RXP15 PEG_RXN15 PEG_RXP14 PEG_RXN14 PEG_RXP13 PEG_RXN13 PEG_RXP12 PEG_RXN12 PEG_RXP11 PEG_RXN11 PEG_RXP10 PEG_RXN10 PEG_RXP9 PEG_RXN9 PEG_RXP8 PEG_RXN8 PEG_RXP7 PEG_RXN7 PEG_RXP6 PEG_RXN6 PEG_RXP5 PEG_RXN5 PEG_RXP4 PEG_RXN4 PEG_RXP3 PEG_RXN3 PEG_RXP2 PEG_RXN2 PEG_RXP1 PEG_RXN1 PEG_RXP0 PEG_RXN0
PEG_RXP15 [6] PEG_RXN15 [6] PEG_RXP14 [6] PEG_RXN14 [6] PEG_RXP13 [6] PEG_RXN13 [6] PEG_RXP12 [6] PEG_RXN12 [6] PEG_RXP11 [6] PEG_RXN11 [6] PEG_RXP10 [6] PEG_RXN10 [6] PEG_RXP9 [6] PEG_RXN9 [6] PEG_RXP8 [6] PEG_RXN8 [6] PEG_RXP7 [6] PEG_RXN7 [6] PEG_RXP6 [6] PEG_RXN6 [6] PEG_RXP5 [6] PEG_RXN5 [6] PEG_RXP4 [6] PEG_RXN4 [6] PEG_RXP3 [6] PEG_RXN3 [6] PEG_RXP2 [6] PEG_RXN2 [6] PEG_RXP1 [6] PEG_RXN1 [6] PEG_RXP0 [6] PEG_RXN0 [6]

0.22uF AC coupling Caps for PCIE GEN1/2/3
0.1uF AC coupling Caps for PCIE GEN1/2

PEX_REFCLK PEX_REFCLK*
AL13 AK13
CLK_PCIE_VGAP CLK_PCIE_VGAN
CLK_PCIE_VGAP [24] CLK_PCIE_VGAN [24]

PEX_TSTCLK_OUT PEX_TSTCLK_OUT*
AJ26 PEX_TSTCLK R64 *200_4_NC
AK26 PEX_TSTCLK#

PEX_RST*
AJ12 GPU_RST#

PEX_CLKREQ*
AK12 PEX_CLKREQ# R63 *10K_4_NC +3.3V_GFX

PEX_TERMP
AP29 PEX_TERMP R80 2.49K/F_4

TESTMODE
AK11 TESTMODE R46 10K_4

+3.3V_GFX
C413 *0.1U/16V_4_NC
GPU_RST#
U21 *TC7SH08FU_NC
PLTRST# [7,23,38,41,57]
DGPU_HOLD_RST# [23]
R351 0_4_DIS
DIS
R395 *0_4_OPT_NC
OPT

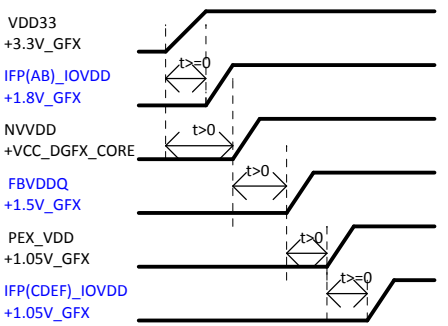
+3.3V_GFX
PEX_CLKREQ#
Q3 *2N7002W_NC
PEG_A_CLKRQ# [24]
R61 0_4

GPU all PWROK

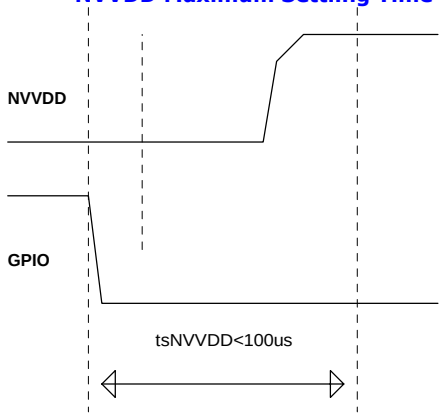
+3.3V_GFX
+3.3V_RUN
R25 *10K_4_NC
DGPU_PWROK [25]
R13 *330_4_NC
Q1 *2N7002W_NC
+1.05V_GFX
C2 *4700P/25V_4_NC
Q2 *PDTC143TT_NC

PDTC143TT
Hfe=200, Vce(sat)=0.1V, Vbe(sat)=0.7V, Rb=4.7K
Ib=(1.05-0.7)/4.7K=74.46uA,
Ic=(3.3-0.1)/220=9.69mA
Hfe*Ib > Ic, Saturation

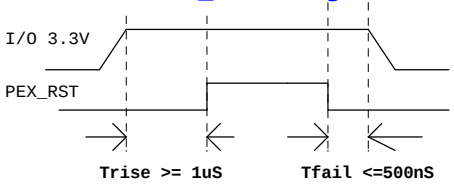
Power up sequence



NVVDD Maximum Settling Time



PEX_RST timing



Quanta Computer Inc.
PROJECT : R09A

Size	Document Number	Rev
	N13P-GS (PCIE I/F) 1/5	3A
Date: Monday, March 05, 2012	Sheet 13 of 58	

U24B
N13P-GT-A2

GB4-128

DBI

EDC

GDDR5 NO USE

MEMORY I/F A

U24C
N13P-GT-A2

GB4-128

DBI

EDC

GDDR5 NO USE

MEMORY I/F C

GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

For Debug only

15mils width

100mA

100mA

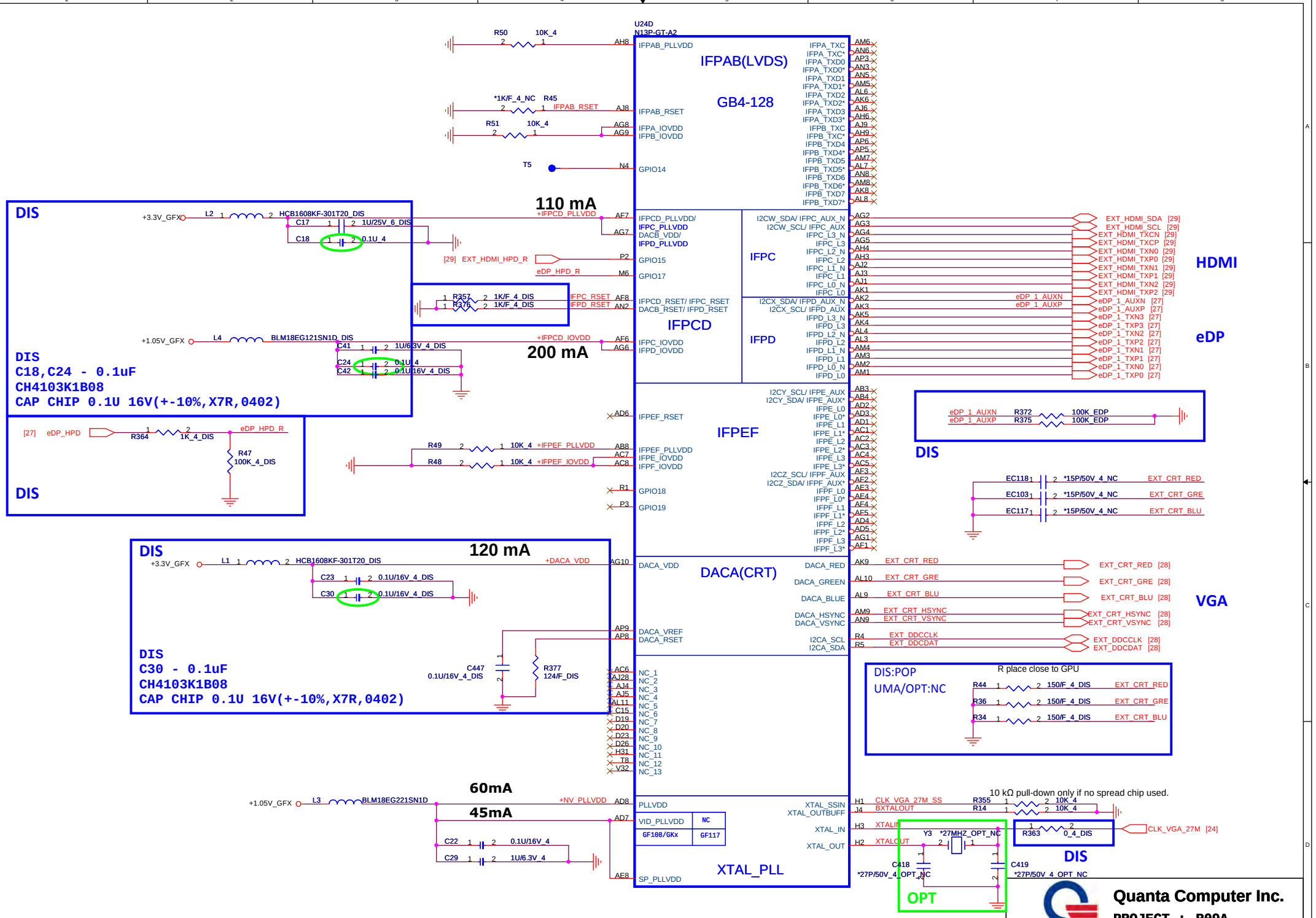
15mils width

GT	all POP
GV	NC C20,C33,C138

Quanta Computer Inc.
PROJECT : R09A

Size	Document Number	Rev
	N13P-GS (MEMORY I/F) 2/5	3A

Date: Saturday, March 03, 2012 Sheet 14 of 58


U24D
N13P-GT-A2
IFPAB(LVDS)
GB4-128
IFPCD
IFPEF
DACA(CRT)
XTAL_PLL
HDMI
eDP
VGA
110 mA
200 mA
120 mA
60mA
45mA
DIS
OPT
C18,C24 - 0.1uF
CH4103K1B08
CAP CHIP 0.1U 16V(+-10%,X7R,0402)
C30 - 0.1uF
DIS:POP
UMA/OPT:NC
R place close to GPU
10 kΩ pull-down only if no spread chip used.
Quanta Computer Inc.
PROJECT : R09A
N13P-GS (DISPLAY) 3/5
Monday, March 05, 2012
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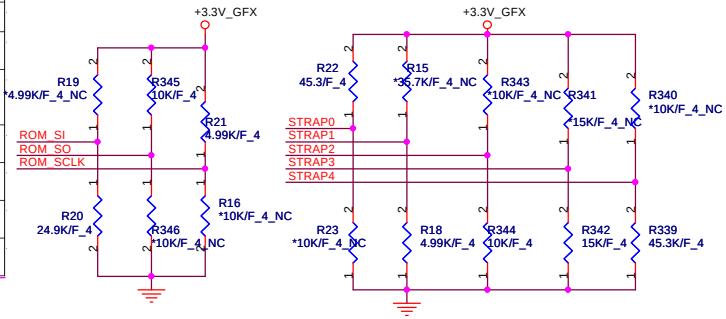
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)

24.9K/F_4: CS32492FB16 [RES CHIP 24.9K 1/16W +-1%(0402)]
30K/F_4: CS33002FB13 [RES CHIP 30K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

N13P-GT

	N13P-GT-OPT	N13P-GT-DIS
ROM_SCLK	5K-PU	5K-PU
ROM_SO	10K-PU	10K-PU
ROM_SI	GDDR5 Hynix-128MX16-25K-PD Samsung-128Mx16-30K-PD	GDDR5 Hynix-128MX16-25K-PD Samsung-128Mx16-30K-PD
STRAP-1	5K-PD	5K-PD
STRAP-2	10K-PD	10K-PD
STRAP-3	5K-PD	15K-PD
STRAP-4	45K-PD	45K-PD



N13P-GV

For N13P-GV-B-A2, the h/w strap setting must be modified as below
ROM_SO PD 10K
ROM_SI PD 10K
ROM_SCLK PD 10K
Strap 4 PD10K

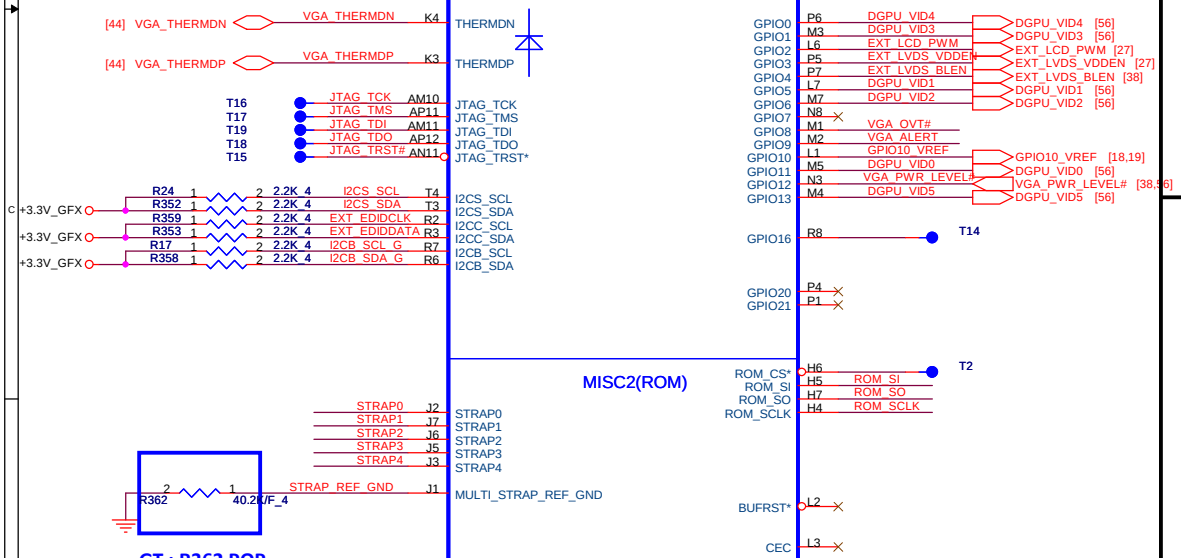
For Hynix 128MX16 GDDR5	For Samsung 128MX16 GDDR5
Strap 3 PD 10K	Strap 3 PD 10K
Strap 2 PU 10K	Strap 2 PU 10K
Strap 1 PD 10K	Strap 1 PD 10K
Strap 0 PD 10K	Strap 0 PU 10K

Default: Hynix VRAM (0100) VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Quanta P/N	Vendor P/N	ROM_SI
0100	GDDR5 128Mx16, 2500MHz	Hynix	AKG5MWUTW14	H5GQ2H24MFR-T2C	PD 25K
0101	GDDR5 128Mx16, 2500MHz	Samsung	AKG5MWDT509	K4G20325FD-F	PD 30K

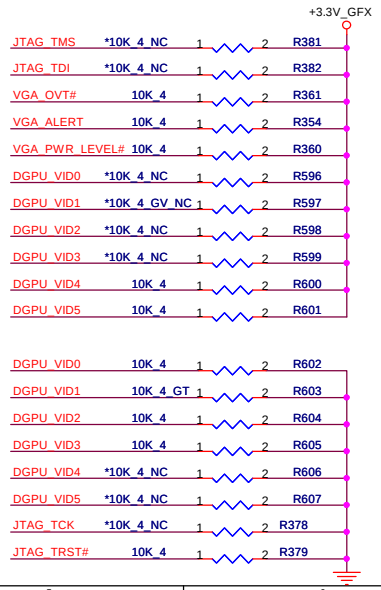
SOR_EXPOSED[3:0]		STRAP3
0000	Optimus	PD 5K
0010	Discret only	PD 15K

Display confiauration table



GT : R362 POP
GV : R362 NC

	Output	VID0	VID1	VID2	VID3	VID4	VID5
N13P-GV(QS)	0.875V	0	1	0	0	1	1
N13P-GT(QS)	0.9V	0	0	0	0	1	1



GPIO	I/O	ACTIVE	USAGE
0	OUT	N/A	NVVDD VID4
1	OUT	N/A	NVVDD VID3
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID1
6	OUT	N/A	NVVDD VID2
7	OUT	N/A	3D VERSION LEFT/RIGHT SIGNAL
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	MEMORY VREF CONTROL
11	OUT	N/A	NVVDD VID0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	NVVDD VID5

Quanta Computer Inc.
PROJECT : R09T

Size	Document Number	Rev
	N13P-GT (GPIO&STRAPS) 4/5	2B

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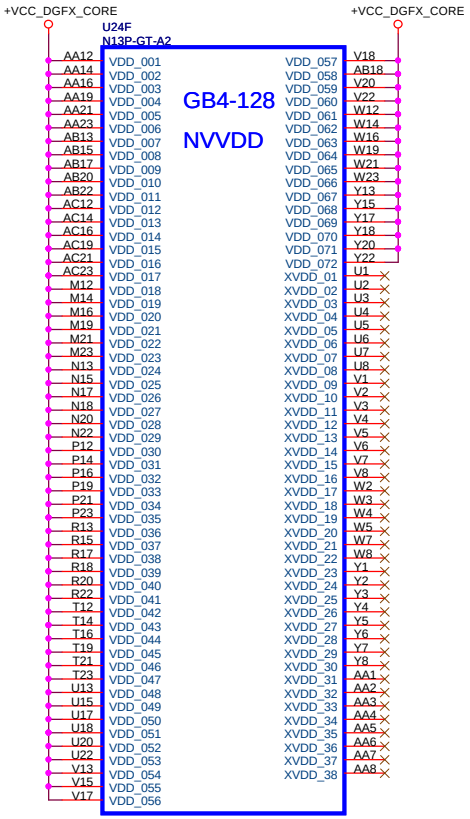
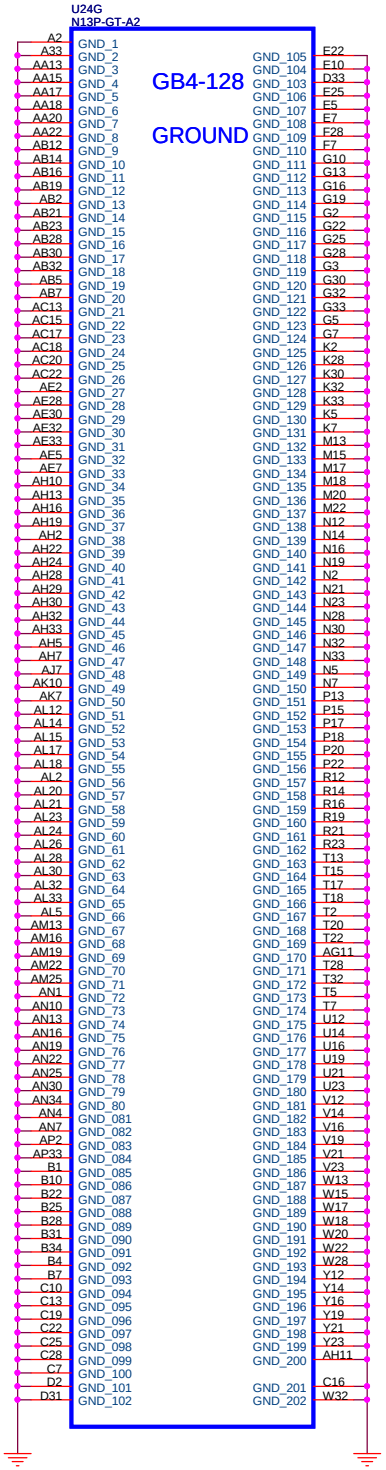
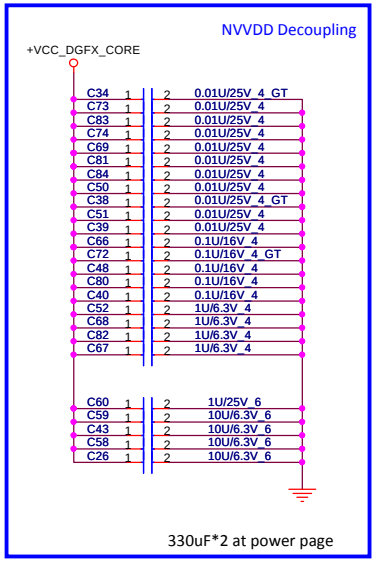




GT: 60A	all POP
GV: 42A	NC C34,C38,C72

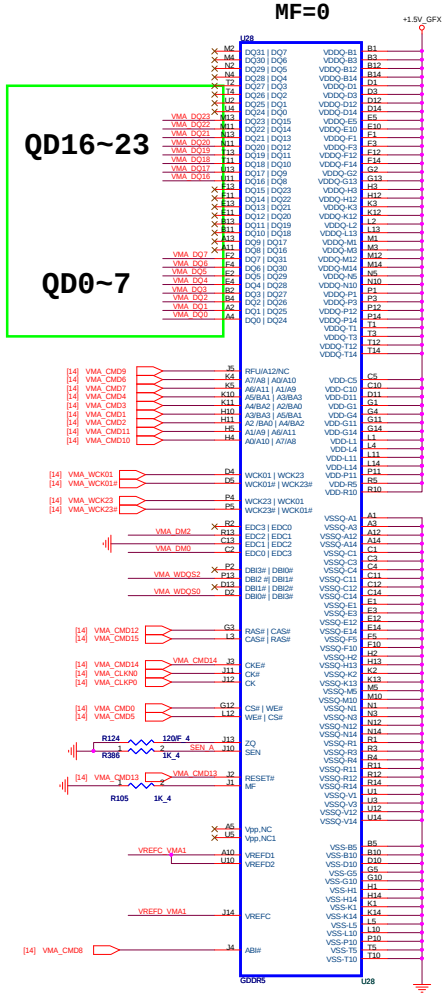


Quanta Computer Inc.			
PROJECT : R09A			
Size	Document Number		Rev
	N13P-GS (POWER & GND) 5/5		3A
Date:	Saturday, March 03, 2012	Sheet 17 of 58	

CHANNEL A: 1024MB GDDR5

LOWER HALF

MF=0



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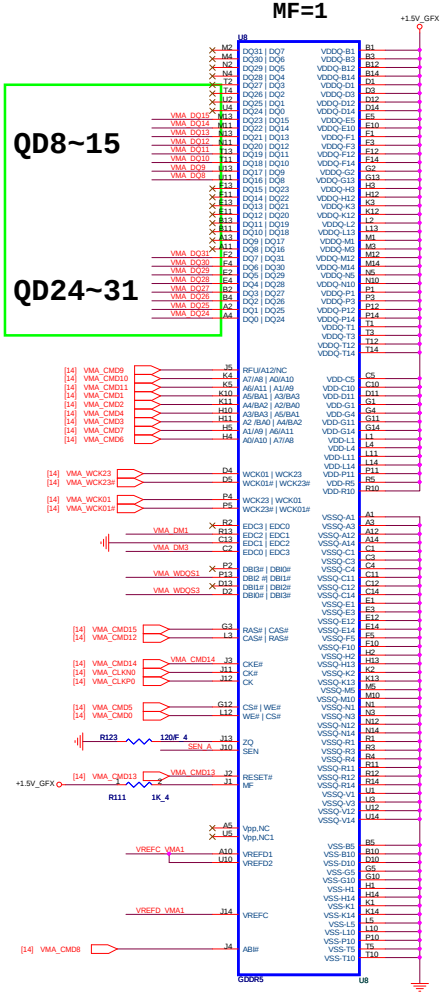

UPPER HALF

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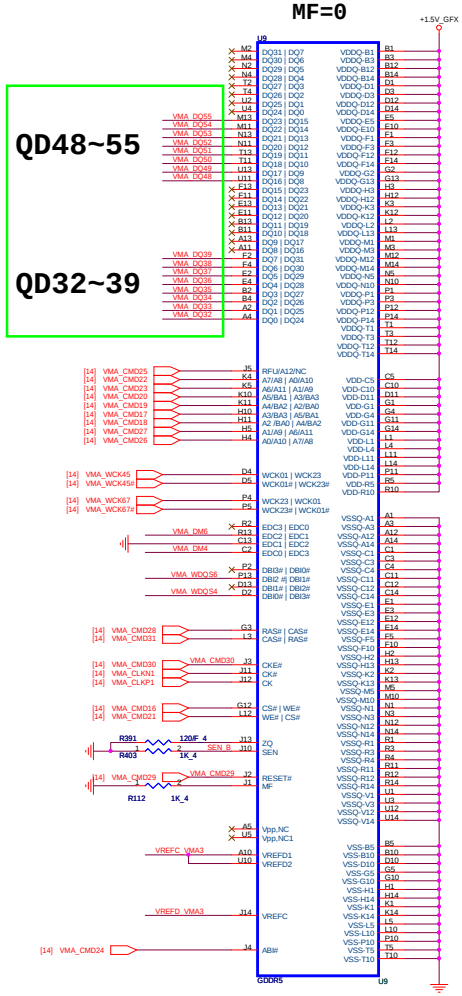

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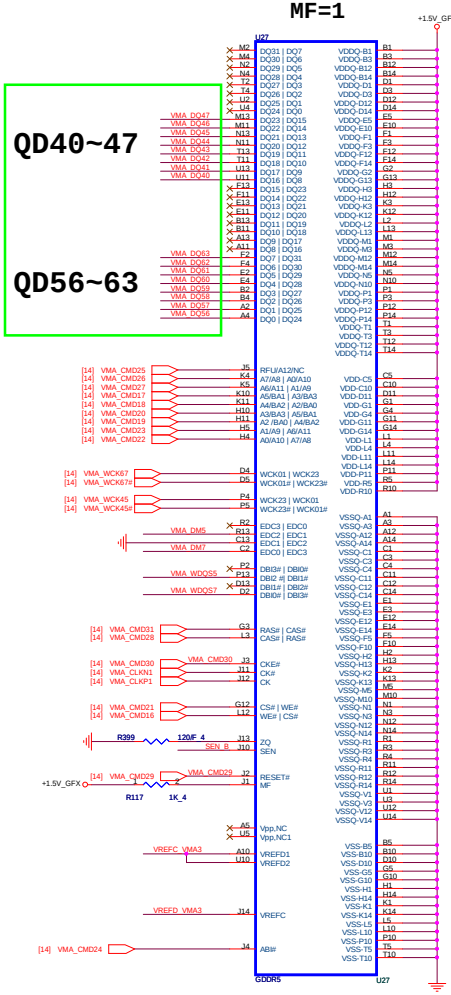
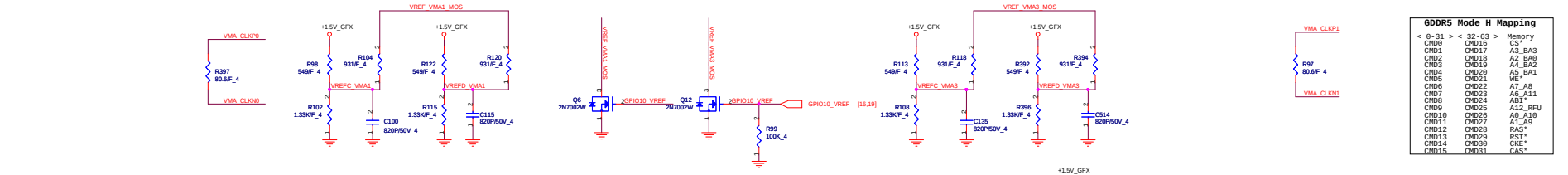
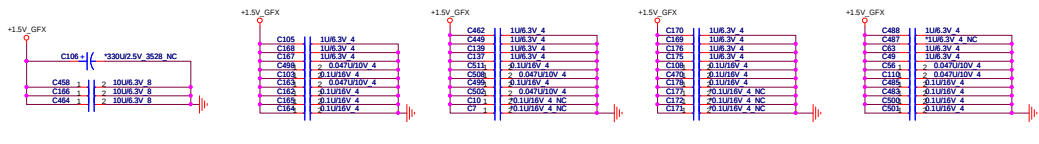




GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*



Quanta Computer Inc.			
PROJECT : R09A			
Size	Document Number		Rev
	N13P-GS VRAM-1(GDDR5 BGA170)		3A
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CHANNEL B: 1024MB GDDR5

LOWER HALF

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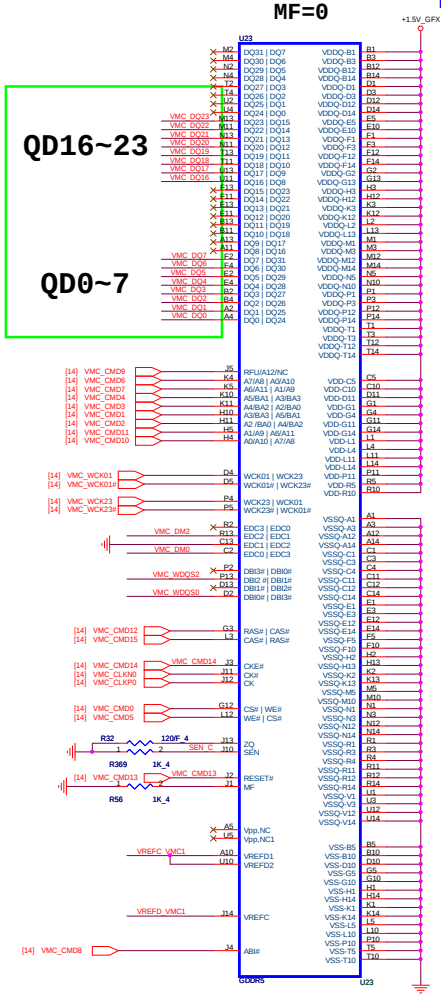

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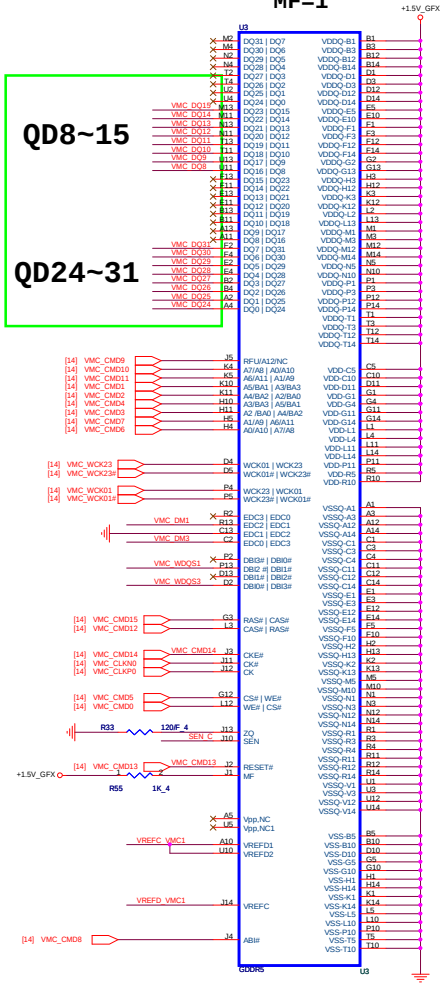

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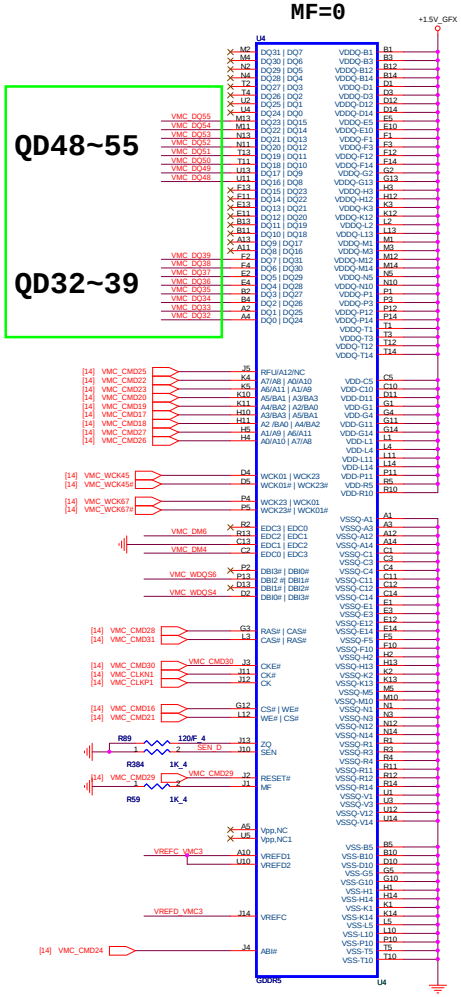

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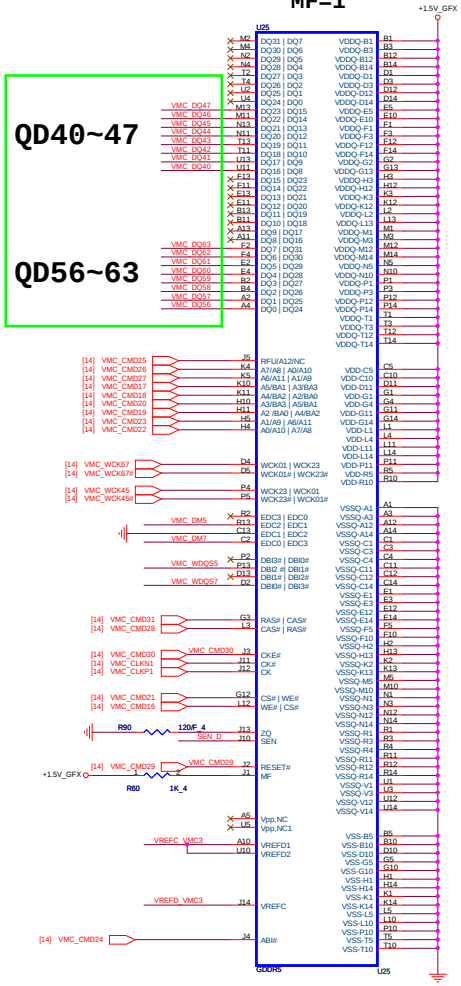
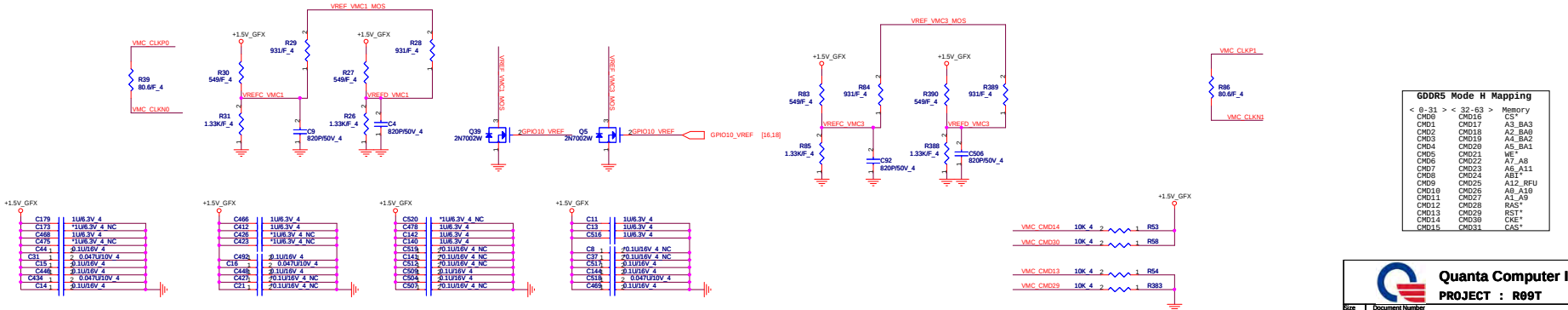
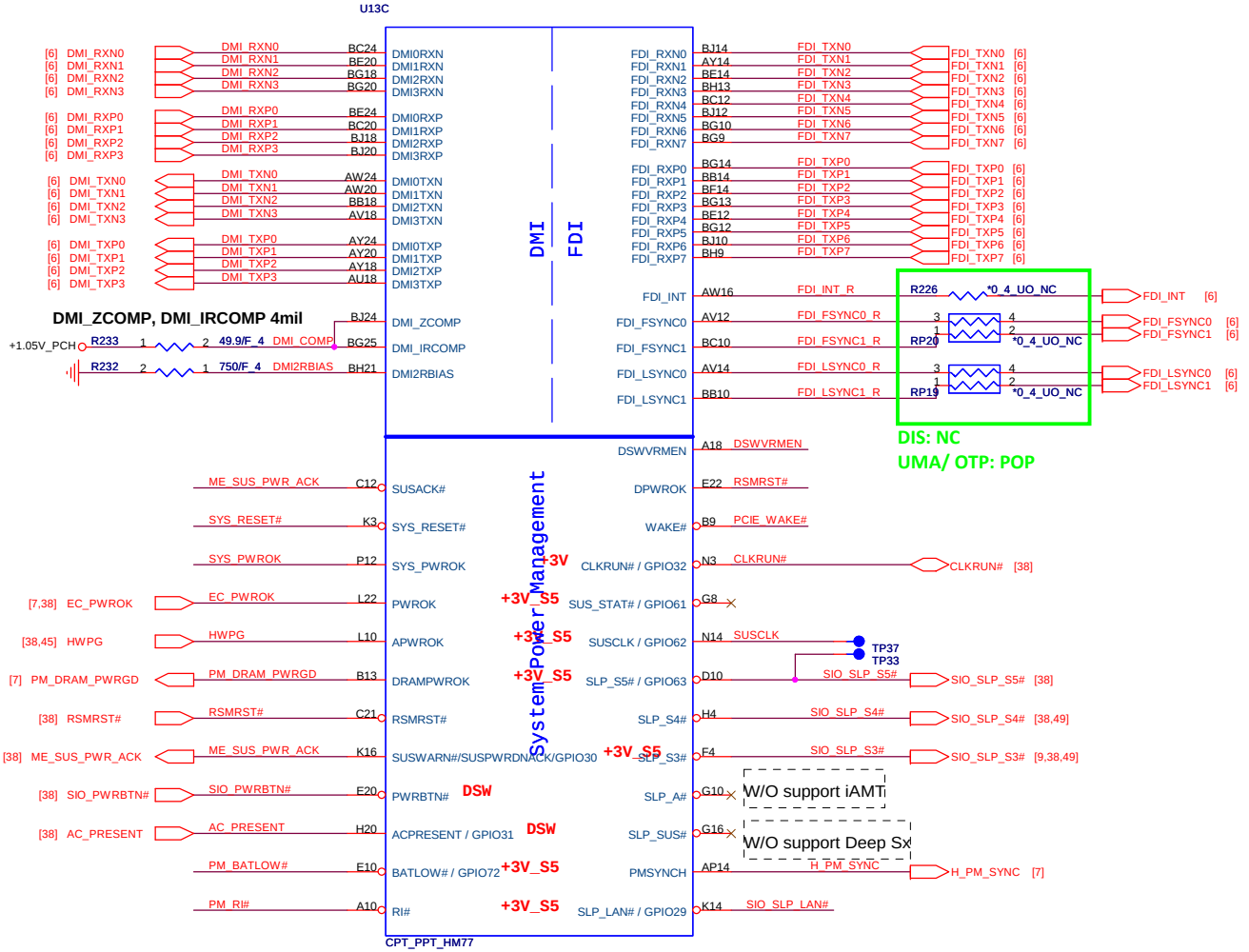
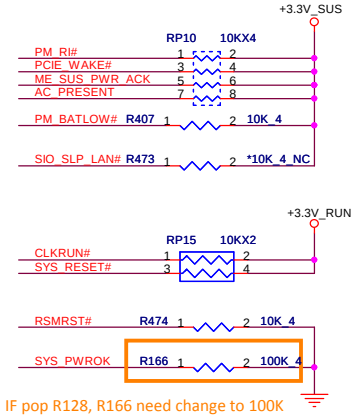


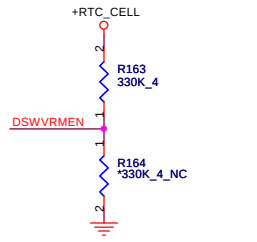


Cougar Point/Panther Point (DMI,FDI,PM)

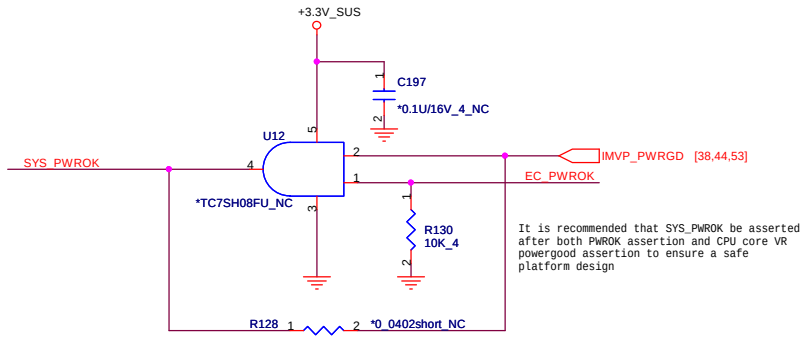


PCH Pull-high/low(CLG)





On Die DSW VR Enable
High = Enable (Default)
Low = Disable



Quanta Computer Inc.

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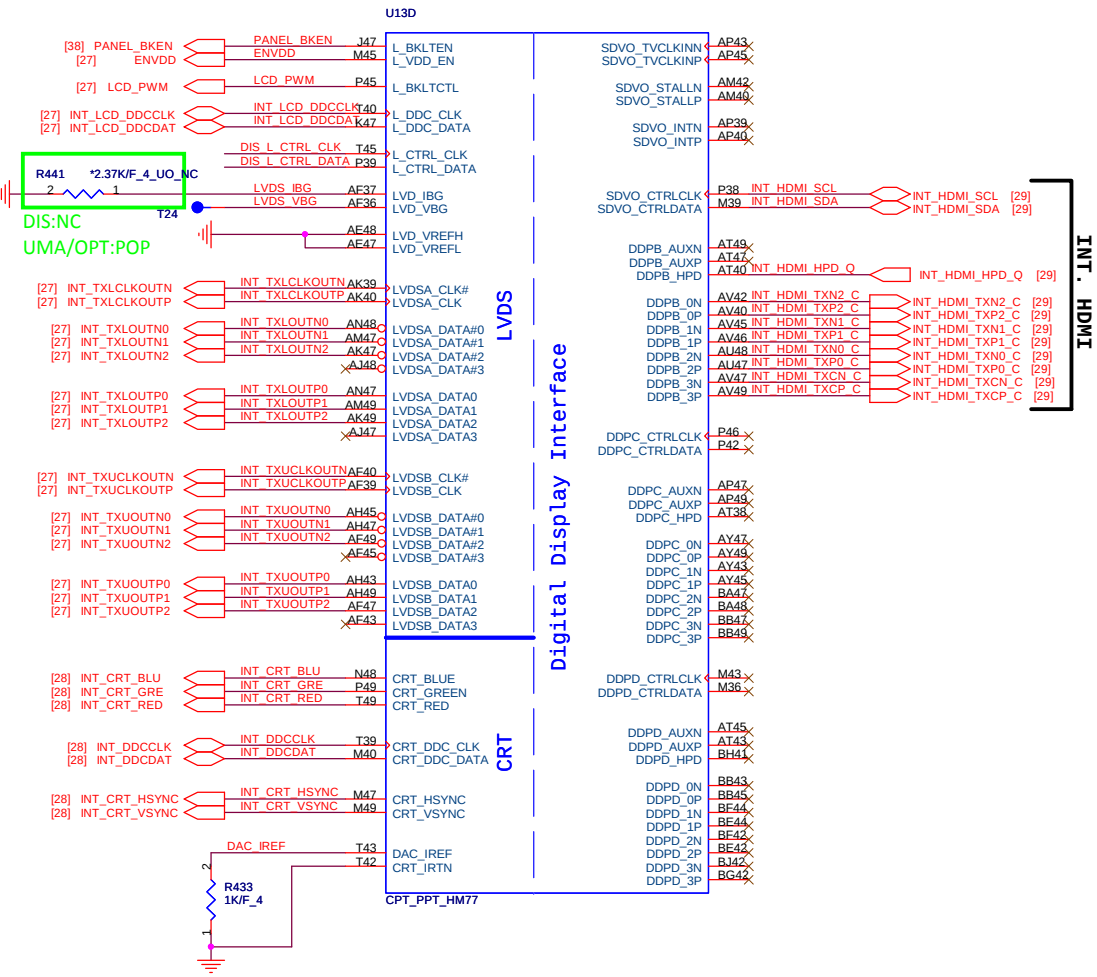
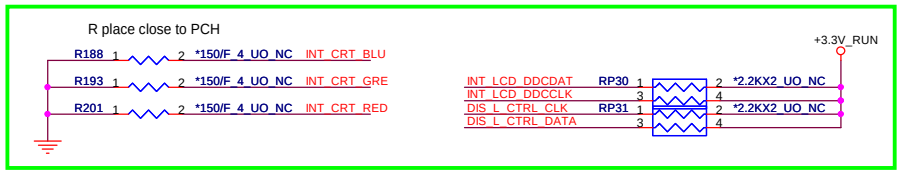
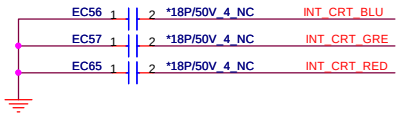
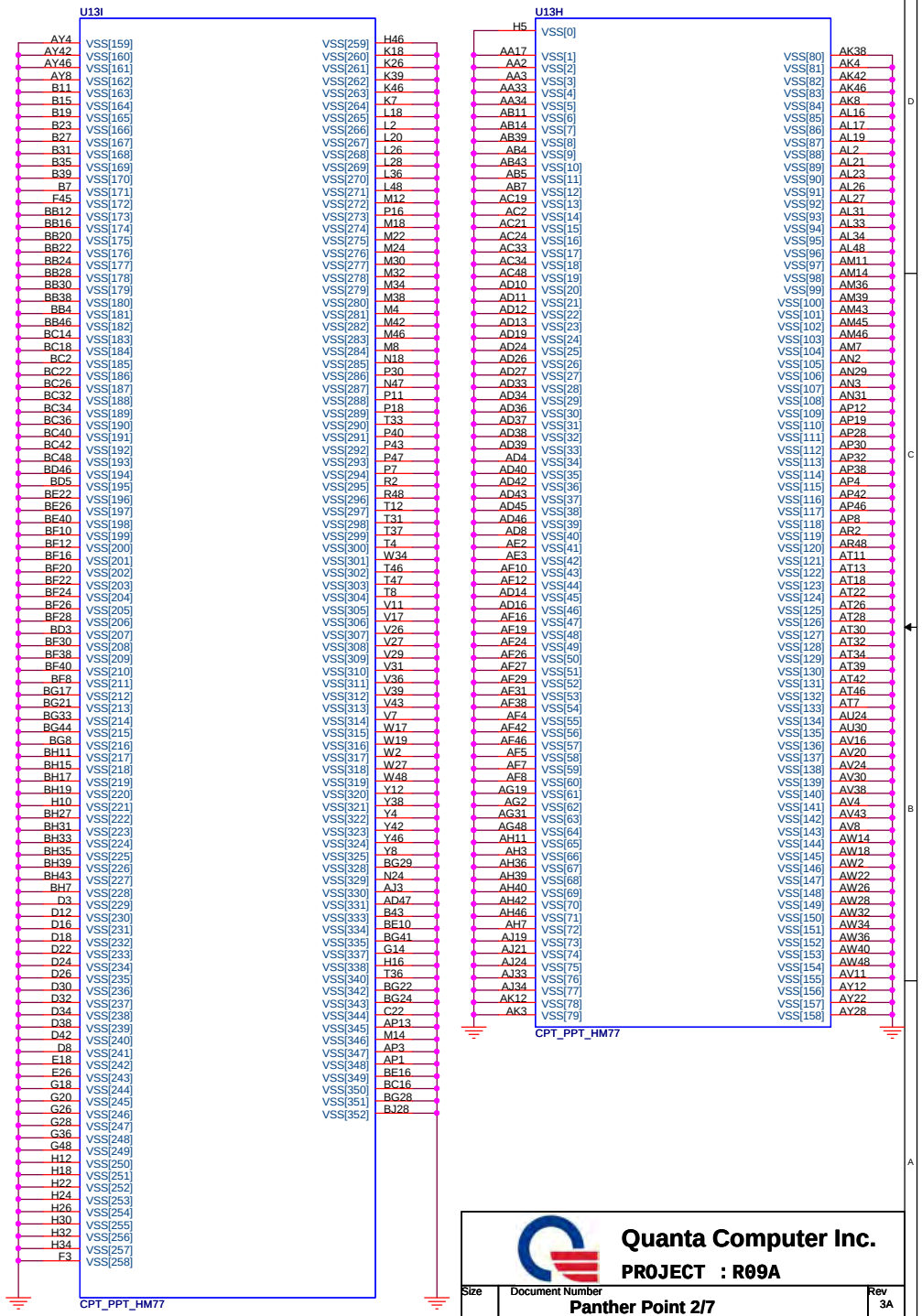
Cougar Point/Panther Point (LVDS,DDI)







Cougar Point/Panther Point (GND)



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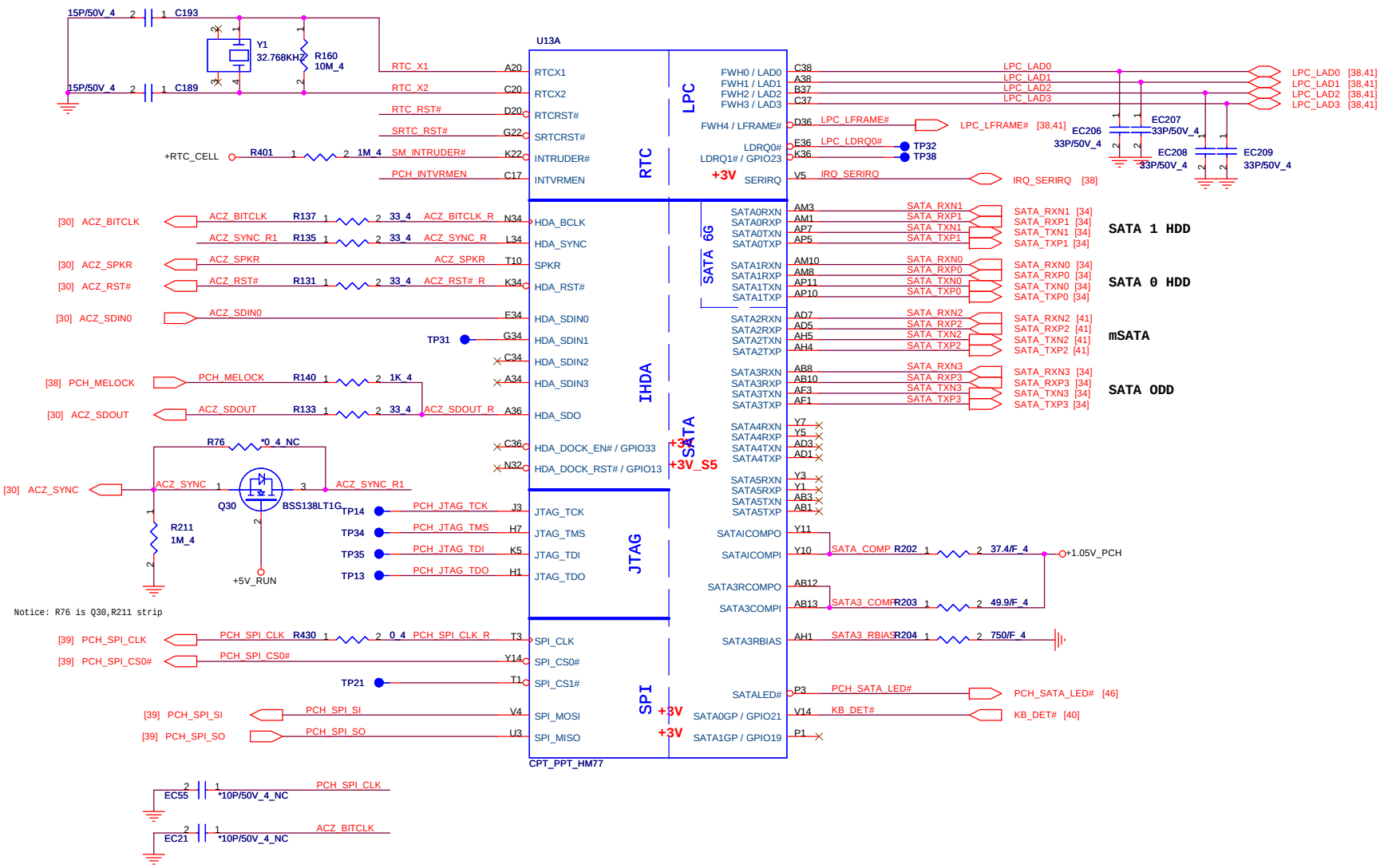
Cougar Point/Panther Point (HDA,JTAG,SATA)



Notice: R76 is Q30,R211 strip

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	**NC**
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	**NC**
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R162 330K_4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R134 1K_4 ACZ_SYNC_R

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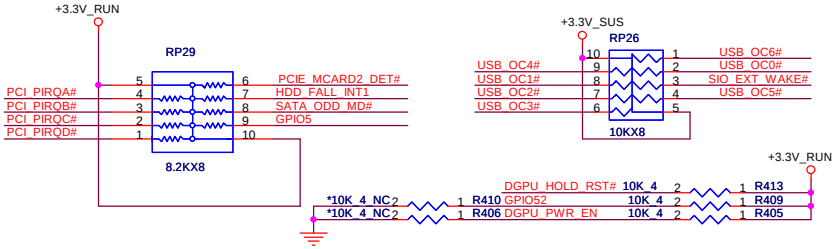
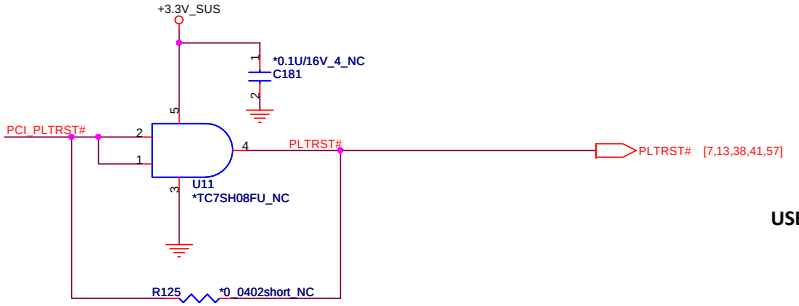
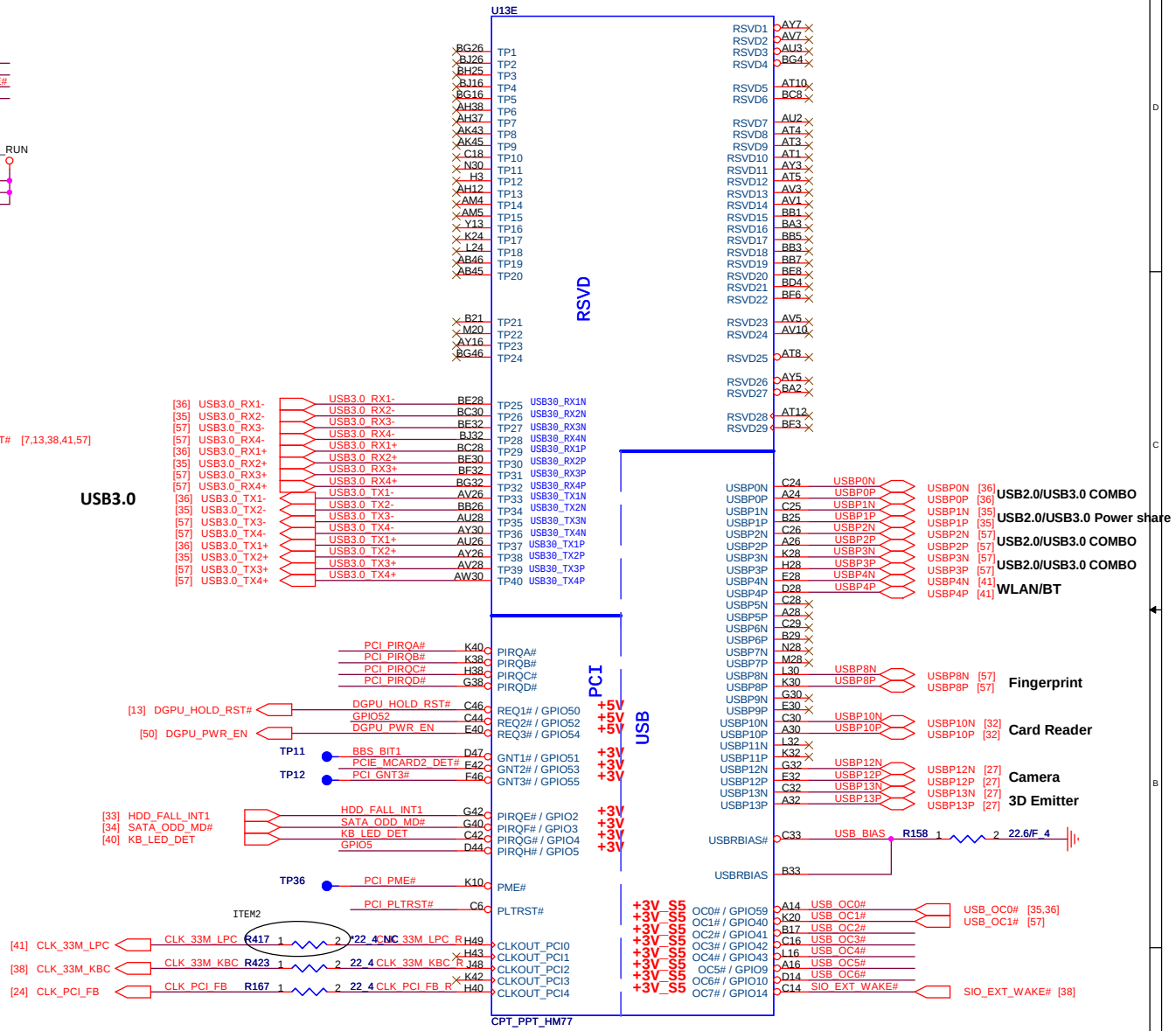
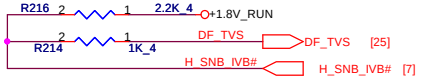
Cougar Point-M/Panther Point (PCI,USB,NVRAM)

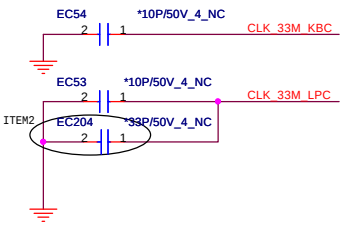






Pin Name	Strap description	Sampled	Configuration
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Bit 0 / Bit 1 / Boot Location 1 / 1 / SPI *
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	0 / 0 / LPC
			Default weak pull-up on GNT0/1# **[Need external pull-down for LPC BIOS]**
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm





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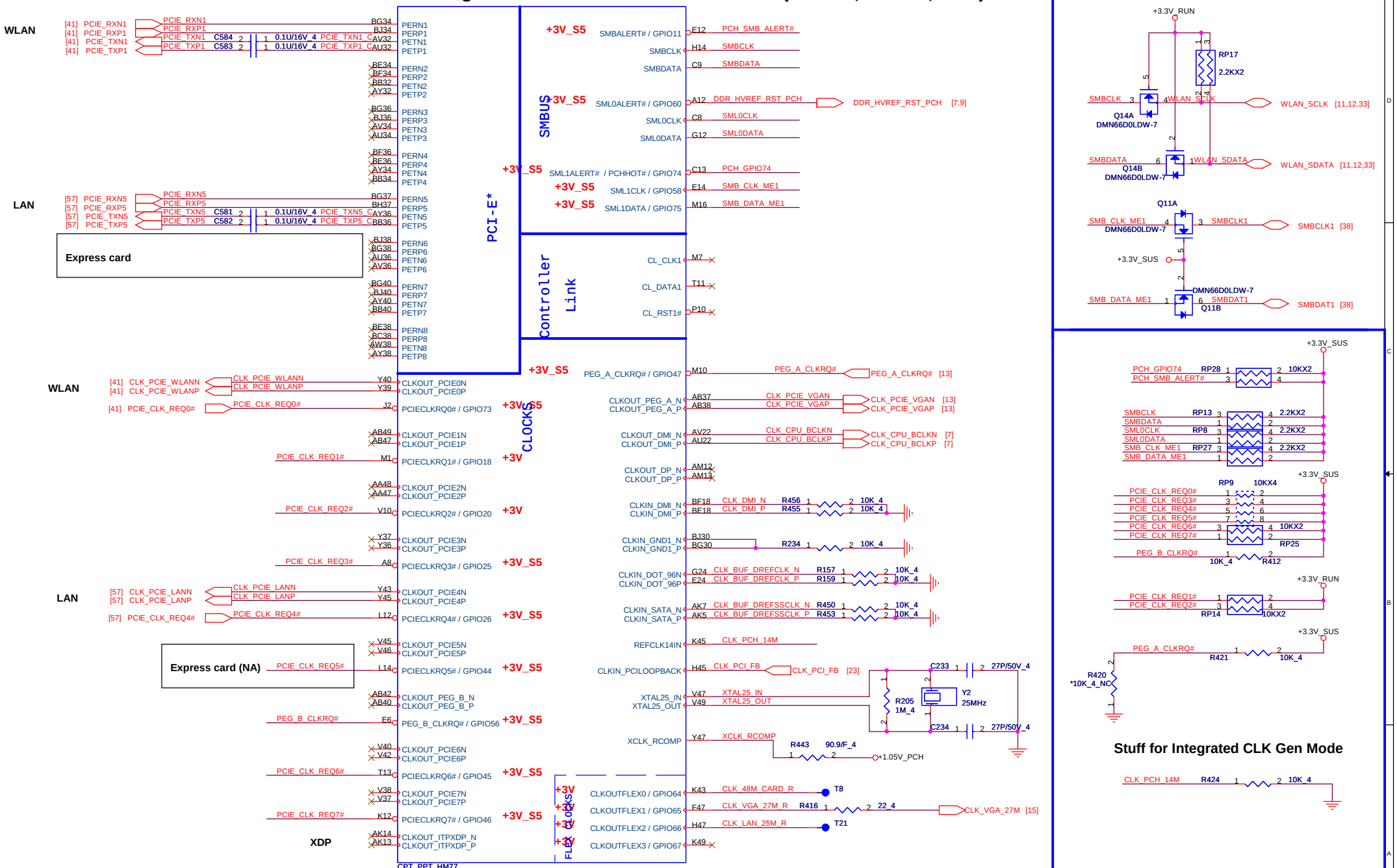
U13B Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 /GPIO64	• 33 /27 /48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 /GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC /48/24 MHz
CLKOUTFLEX2 /GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 /GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

SMBus/Pull-up(CLG)

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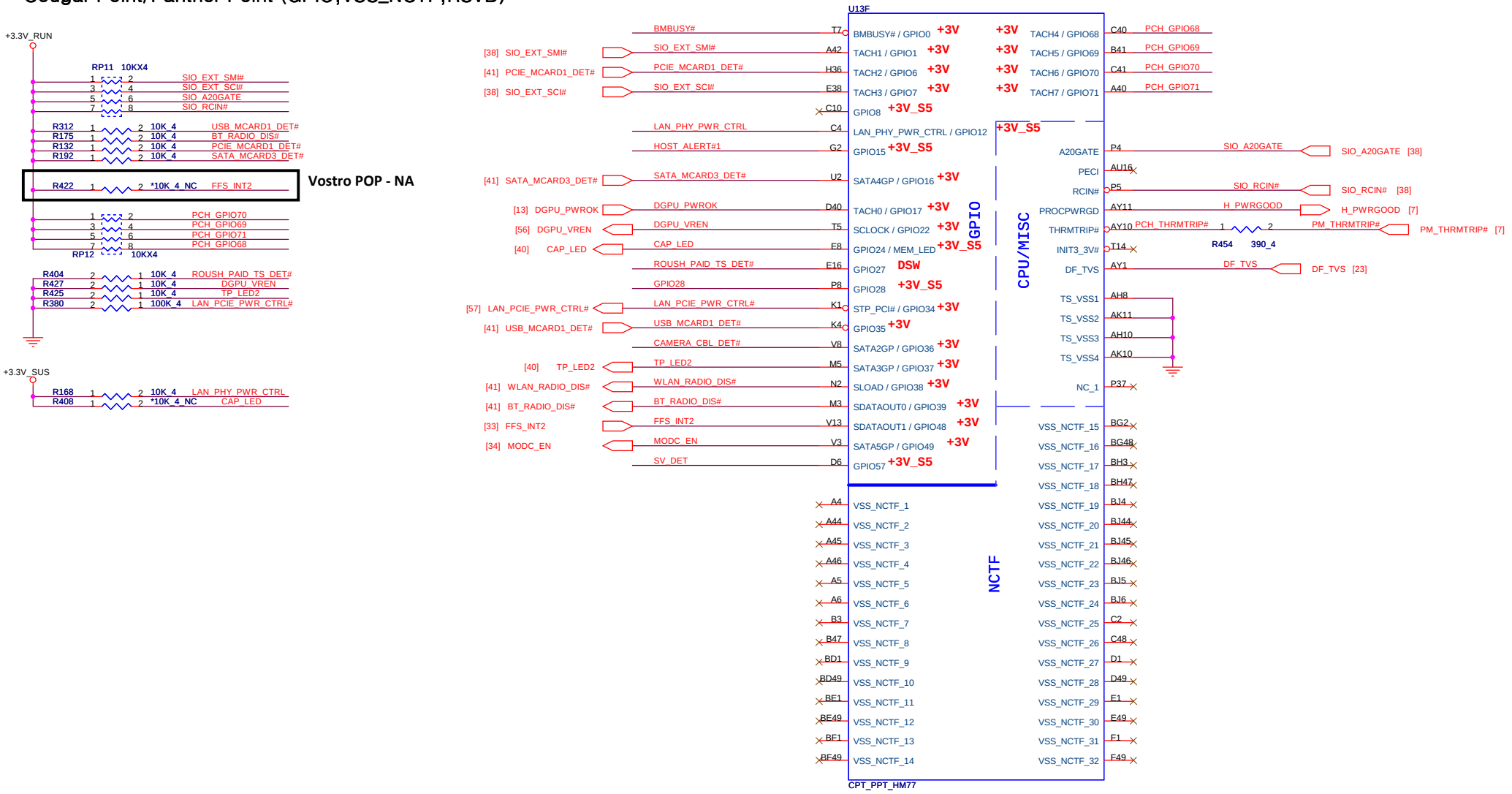
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

R426 1 2 *1K_4_NC GPIO28

CHECK LIST:
When Unused as GPIO or SATA*GP - Use 8.2K-10K pull-down to ground.

CAMERA_CBL_DET# R439 1 2 10K_4

+3.3V_RUN

BMBUSY# R435 1 2 10K_4

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

+3.3V_SUS

HOST_ALERT#1 R170 1 2 1K_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

+3.3V_SUS

R411 1 2 10K_4 SV_DET

MFG - TEST

+3.3V_RUN

WLAN_RADIO_DIS# R182 1 2 10K_4
R181 1 2 *0_4_NC

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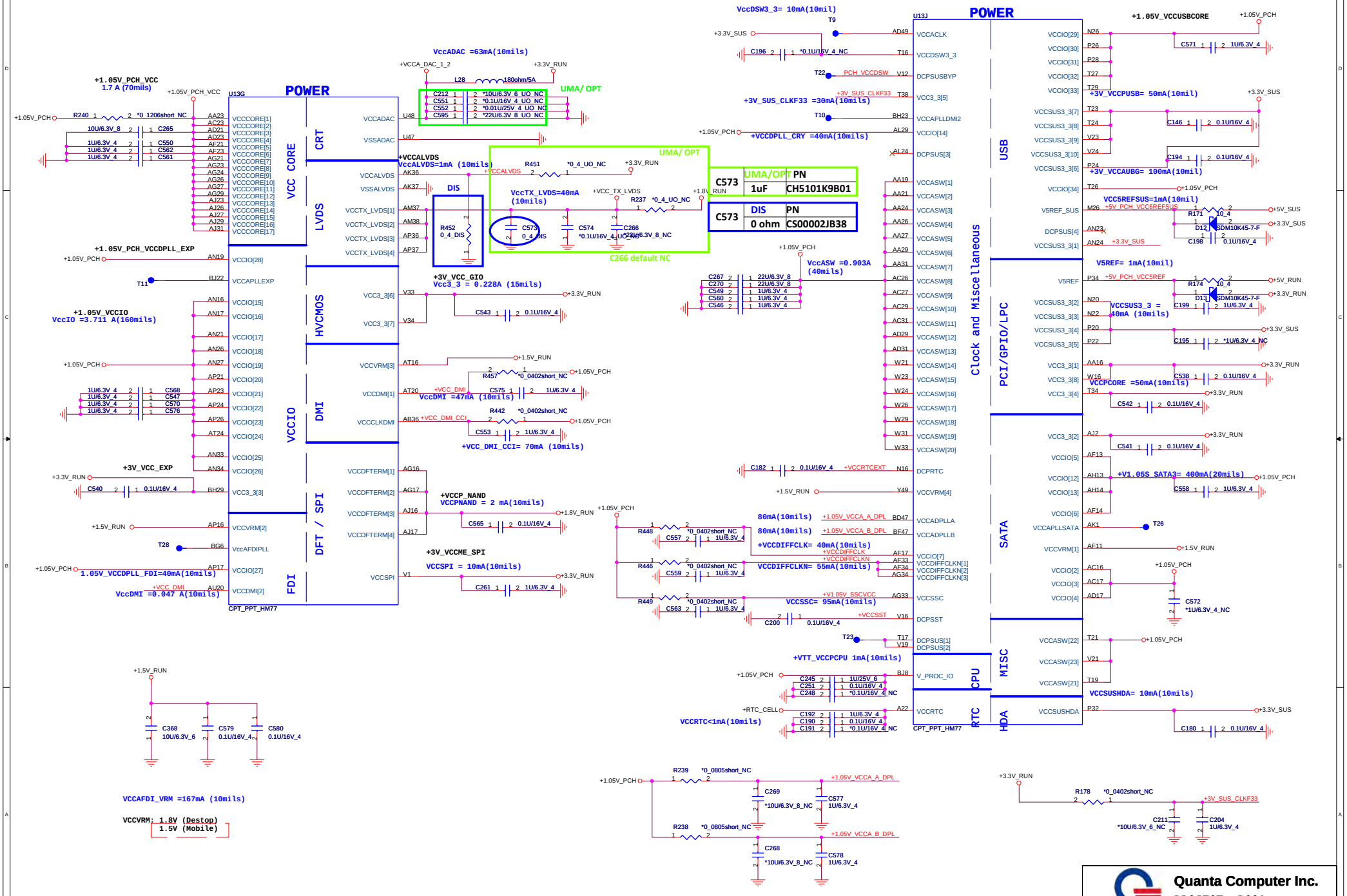
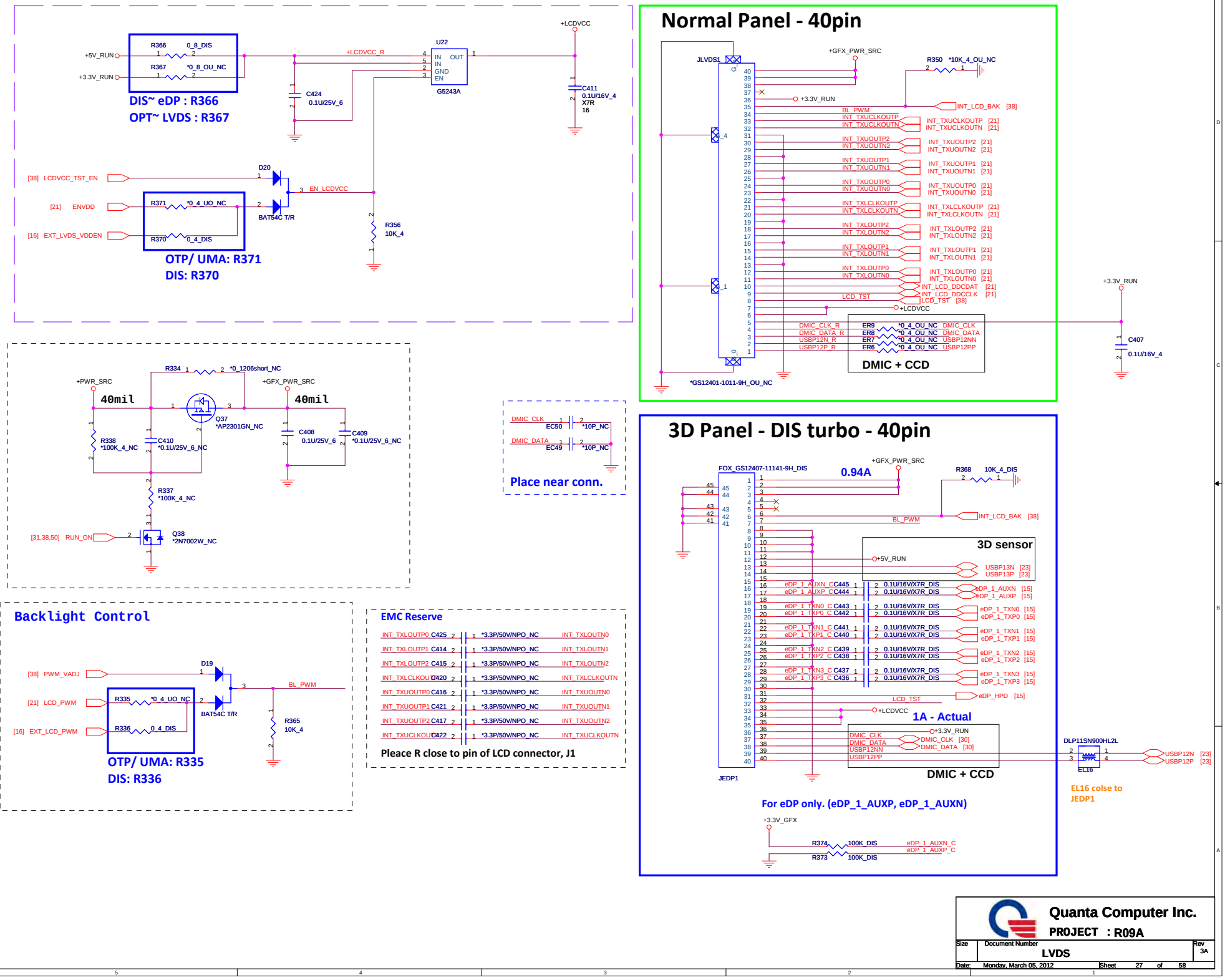
Cougar Point/Panther Point (POWER)

Cougar Point/Panther Point (POWER)




+5V_RUN
+3.3V_RUN
R366 0_8_DIS
R367 *0_8_OU_NC
DIS~ eDP : R366
OPT~ LVDS : R367
+LCDVCC_R
U22
IN OUT
IN
GND
EN
G5243A
C424 0.1U/25V_6
+LCDVCC
C411 0.1U/16V_4 X7R 16
[38] LCDVCC_TST_EN
[21] ENVDD
[16] EXT_LVDS_VDDEN
D20
BAT54C T/R
EN_LCDVCC
R371 *0_4_UO_NC
R370 0_4_DIS
OTP/ UMA: R371
DIS: R370
R356 10K_4
Normal Panel - 40pin
JLVDS1
+GFX_PWR_SRC
R350 *10K_4_OU_NC
+3.3V_RUN
BL_PWM
INT_LCD_BAK [38]
INT_TXUCLKOUTP [21]
INT_TXUCLKOUTN [21]
INT_TXUOUTP2 [21]
INT_TXUOUTN2 [21]
INT_TXUOUTP1 [21]
INT_TXUOUTN1 [21]
INT_TXUOUTP0 [21]
INT_TXUOUTN0 [21]
INT_TXLCLKOUTP [21]
INT_TXLCLKOUTN [21]
INT_TXLOUTP2 [21]
INT_TXLOUTN2 [21]
INT_TXLOUTP1 [21]
INT_TXLOUTN1 [21]
INT_TXLOUTP0 [21]
INT_TXLOUTN0 [21]
INT_LCD_DDCDAT [21]
INT_LCD_DDCCLK [21]
LCD_TST [38]
+LCDVCC
DMIC_CLK_R
DMIC_DATA_R
USBP12N_R
USBP12P_R
ER9 *0_4_OU_NC DMIC_CLK
ER8 *0_4_OU_NC DMIC_DATA
ER7 *0_4_OU_NC USBP12NN
ER6 *0_4_OU_NC USBP12PP
DMIC + CCD
*GS12401-1011-9H_OU_NC
C407 0.1U/16V_4
R334 *0_1206short_NC
+PWR_SRC
+GFX_PWR_SRC
40mil
40mil
Q37 *AP2301GN_NC
R338 *100K_4_NC
C410 *0.1U/25V_6_NC
C408 0.1U/25V_6
C409 *0.1U/25V_6_NC
R337 *100K_4_NC
[31,38,50] RUN_ON
Q38 *2N7002W_NC
DMIC_CLK
DMIC_DATA
EC50 *10P_NC
EC49 *10P_NC
Place near conn.
3D Panel - DIS turbo - 40pin
FOX_GS12407-11141-9H_DIS
0.94A
R368 10K_4_DIS
3D sensor
USBP13N [23]
USBP13P [23]
eDP_1_AUXN_C C445 0.1U/16V/X7R_DIS
eDP_1_AUXP_C C444 0.1U/16V/X7R_DIS
eDP_1_AUXN [15]
eDP_1_AUXP [15]
eDP_1_TXN0_C C443
eDP_1_TXP0_C C442
eDP_1_TXN1_C C441
eDP_1_TXP1_C C440
eDP_1_TXN2_C C439
eDP_1_TXP2_C C438
eDP_1_TXN3_C C437
eDP_1_TXP3_C C436
eDP_1_TXN0 [15]
eDP_1_TXP0 [15]
eDP_1_TXN1 [15]
eDP_1_TXP1 [15]
eDP_1_TXN2 [15]
eDP_1_TXP2 [15]
eDP_1_TXN3 [15]
eDP_1_TXP3 [15]
eDP_HPD [15]
LCD_TST
1A - Actual
DMIC_CLK [30]
DMIC_DATA [30]
DMIC + CCD
JEDP1
DLP11SN900HL2L
EL16
USBP12N [23]
USBP12P [23]
EL16 colse to JEDP1
For eDP only. (eDP_1_AUXP, eDP_1_AUXN)
+3.3V_GFX
R374 100K_DIS
R373 100K_DIS
eDP_1_AUXN_C
eDP_1_AUXP_C
Backlight Control
[38] PWM_VADJ
[21] LCD_PWM
[16] EXT_LCD_PWM
D19
BAT54C T/R
BL_PWM
R335 *0_4_UO_NC
R336 0_4_DIS
R365 10K_4
OTP/ UMA: R335
DIS: R336
EMC Reserve
INT_TXLOUTP0 C425 *3.3P/50V/NPO_NC INT_TXLOUTN0
INT_TXLOUTP1 C414 *3.3P/50V/NPO_NC INT_TXLOUTN1
INT_TXLOUTP2 C415 *3.3P/50V/NPO_NC INT_TXLOUTN2
INT_TXLCLKOUTP C420 *3.3P/50V/NPO_NC INT_TXLCLKOUTN
INT_TXUOUTP0 C416 *3.3P/50V/NPO_NC INT_TXUOUTN0
INT_TXUOUTP1 C421 *3.3P/50V/NPO_NC INT_TXUOUTN1
INT_TXUOUTP2 C417 *3.3P/50V/NPO_NC INT_TXUOUTN2
INT_TXUCLKOUTP C422 *3.3P/50V/NPO_NC INT_TXUCLKOUTN
Pleace R close to pin of LCD connector, J1
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VGA

[21] INT_CRT_RED
[15] EXT_CRT_RED
R2 *0_4_UO_NC
R327 0_4_DIS
CRT_RED

[21] INT_CRT_GRE
[15] EXT_CRT_GRE
R5 *0_4_UO_NC
R329 0_4_DIS
CRT_GRE

[21] INT_CRT_BLU
[15] EXT_CRT_BLU
R6 *0_4_UO_NC
R330 0_4_DIS
CRT_BLU

DIS: EXT POP
UMA/OPT: INT POP

[21] INT_DDCDAT
[15] EXT_DDCDAT
R9 *0_4_UO_NC
R332 0_4_DIS
DDCDAT

[21] INT_DDCCLK
[15] EXT_DDCCLK
R10 *0_4_UO_NC
R333 0_4_DIS
DDCCLK

[21] INT_CRT_HSYNC
[15] EXT_CRT_HSYNC
R3 *0_4_UO_NC
R328 0_4_DIS
CRT_HSYNC

[21] INT_CRT_VSYNC
[15] EXT_CRT_VSYNC
R7 *0_4_UO_NC
R331 0_4_DIS
CRT_VSYNC

DIS: EXT POP
UMA/OPT: INT POP

+3.3V_GFX
RP33 *2.2KX2_GT_OPT_NC
EXT_DDCDAT
EXT_DDCCLK

N13P-GT I2C must PH even VGA is disable
It is for Nvidia MODS test.

N13P-GT - OPT(POP)

+5V_RUN
D1 SDM10K45-7-F
CRTF1 KMC3S110RY
+5V CRT REF

Layout Note:
Setting R,G,B treac impedance to 50 ohm.

CRT_RED
CRT_GRE
CRT_BLU

EL1 BLM18BB750SN1D
EL2 BLM18BB750SN1D
EL3 BLM18BB750SN1D

RED
GREEN
BLUE

R8 150/F_4
R4 150/F_4
R1 150/F_4

EC6 18P/50V_4
EC4 18P/50V_4
EC2 18P/50V_4
EC5 10P/50V_4
EC3 10P/50V_4
EC1 10P/50V_4

0.1U/16V_4 EC119

JVGA1
YMI_10256-00001

R12 *0_4_UO_NC +3.3V_RUN
R11 0_4_DIS +3.3V_GFX
UMA/OPT:R12
DIS:R11

0.1U/16V_4 EC120
+3.3V_VGA
RP24 2.2KX2
RP23 2.2KX2
+5V_CRT_REF

Q36A DMN66D0LDW-7
DDCDAT
G_DAT_DDC_C
DDCCLK
G_CLK_DDC_C
Q36B DMN66D0LDW-7

+5V_RUN
U1 74AHCT1G125GW
U2 74AHCT1G125GW
C1 0.1U/16V_4

CRT_HSYNC
HSYNC_R
ER4 33_4
HSYNC

CRT_VSYNC
VSYNC_R
ER5 33_4
VSYNC

Place near
74AHCT125 <
200 mil

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HDMI W/O Re-driver

DIS HDMI

[15] EXT_HDMI_TXP2	EXT_HDMI_TXP2	C239	0.1U/16V_4_DIS	HDMI_TX2+_R
[15] EXT_HDMI_TXN2	EXT_HDMI_TXN2	C237	0.1U/16V_4_DIS	HDMI_TX2-_R
[15] EXT_HDMI_TXP1	EXT_HDMI_TXP1	C236	0.1U/16V_4_DIS	HDMI_TX1+_R
[15] EXT_HDMI_TXN1	EXT_HDMI_TXN1	C235	0.1U/16V_4_DIS	HDMI_TX1-_R
[15] EXT_HDMI_TXP0	EXT_HDMI_TXP0	C241	0.1U/16V_4_DIS	HDMI_TX0+_R
[15] EXT_HDMI_TXN0	EXT_HDMI_TXN0	C244	0.1U/16V_4_DIS	HDMI_TX0-_R
[15] EXT_HDMI_TXCP	EXT_HDMI_TXCP	C250	0.1U/16V_4_DIS	HDMI_CLK+_R
[15] EXT_HDMI_TXCN	EXT_HDMI_TXCN	C247	0.1U/16V_4_DIS	HDMI_CLK-_R

OTP/UMA HDMI

[21] INT_HDMI_TXP2_C	INT_HDMI_TXP2_C	C240	*0.1U/16V_4_UO_NC	HDMI_TX2+_R
[21] INT_HDMI_TXN2_C	INT_HDMI_TXN2_C	C238	*0.1U/16V_4_UO_NC	HDMI_TX2-_R
[21] INT_HDMI_TXP1_C	INT_HDMI_TXP1_C	C232	*0.1U/16V_4_UO_NC	HDMI_TX1+_R
[21] INT_HDMI_TXN1_C	INT_HDMI_TXN1_C	C226	*0.1U/16V_4_UO_NC	HDMI_TX1-_R
[21] INT_HDMI_TXP0_C	INT_HDMI_TXP0_C	C242	*0.1U/16V_4_UO_NC	HDMI_TX0+_R
[21] INT_HDMI_TXN0_C	INT_HDMI_TXN0_C	C246	*0.1U/16V_4_UO_NC	HDMI_TX0-_R
[21] INT_HDMI_TXCP_C	INT_HDMI_TXCP_C	C252	*0.1U/16V_4_UO_NC	HDMI_CLK+_R
[21] INT_HDMI_TXCN_C	INT_HDMI_TXCN_C	C249	*0.1U/16V_4_UO_NC	HDMI_CLK-_R

EL7: HDMI_TX2+_R / HDMI_TX2-_R → HDMI_TX2+_C / HDMI_TX2-_C, EXC24CG900U

EL8: HDMI_TX0+_R / HDMI_TX0-_R → HDMI_TX0+_C / HDMI_TX0-_C, EXC24CG900U

EL6: HDMI_TX1+_R / HDMI_TX1-_R → HDMI_TX1+_C / HDMI_TX1-_C, EXC24CG900U

EL9: HDMI_CLK+_R / HDMI_CLK-_R → HDMI_CLK+_C / HDMI_CLK-_C, EXC24CG900U

[15] EXT_HDMI_SCL	EXT_HDMI_SCL	R191	0_4_DIS	HDMI_SCL
[21] INT_HDMI_SCL	INT_HDMI_SCL	R187	*0_4_UO_NC	
[15] EXT_HDMI_SDA	EXT_HDMI_SDA	R195	0_4_DIS	HDMI_SDA
[21] INT_HDMI_SDA	INT_HDMI_SDA	R199	*0_4_UO_NC	
[15] EXT_HDMI_HPD_R	EXT_HDMI_HPD_R	R198	0_4_DIS	HDMI_HPD_Q
[21] INT_HDMI_HPD_Q	INT_HDMI_HPD_Q	R189	*0_4_UO_NC	

DIS - R191,R195,R198
UMA/OPT - R187,R199,R189

R213	499_4	HDMI_TX2+_R
R210	499_4	HDMI_TX2-_R
R209	499_4	HDMI_TX1+_R
R206	499_4	HDMI_TX1-_R
R215	499_4	HDMI_TX0+_R
R220	499_4	HDMI_TX0-_R
R224	499_4	HDMI_CLK+_R
R221	499_4	HDMI_CLK-_R

+3.3V_RUN — Q18 2N7002W

R691~702
UMA/OPT -- 680 ohm PN: CS16802JB27
DIS ----- 499 ohm PN: CS14992FB24

HDMI HPD

HDMI_HPD spec
VinH_min=2.0V

+3.3V_RUN — Q16 MMST3904-7-F — 150K — R196 — HDMI_HPD
HDMI_HPD_Q — R194 5.11K/F_4

IB=(5V-0.7V)/(150K+(70+1)5.1K)=8.4uA
IE=(1+70)X8.4uA=596.4uA
VE=596.4uA X 5.1K=3.04V
B=70

+3.3V_RUN / +3.3V_GFX — R37 *0_4_UO_NC / R42 0_4_DIS
UMA/OPT:R37
DIS:R42

+3.3V_HDMI — RP16 4.7KX2

HDMI_SCL — Q15 FDV301N
HDMI_SDA — Q17 FDV301N

+5V_HDMI — D14 SDM10K45-7-F / D21 SDM10K45-7-F
+5V_HDMIF1_D / +5V_HDMIF2_D — RP18 2.2KX2

HDMIF1 — KMC3S110RY — +5V_RUN

HDMI Conn.

CN5 DFHD19MR203, TYPE A

HDMI_TX2+_C	1
HDMI_TX2-_C	3
HDMI_TX1+_C	4
HDMI_TX1-_C	6
HDMI_TX0+_C	7
HDMI_TX0-_C	9
HDMI_CLK+_C	10
HDMI_CLK-_C	12
HDMI_CLK	15
HDMI_DAT	16
+5V_HDMI	18
HDMI_HPD	19
GND	22, 23

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CODEC

[22] ACZ_BITCLK — R274 *0_0402short_NC — ACZ_BITCLK_CODEC

EC41 *22P_NC

For EMI solution, can be reserved, place close to pin6

+5V_RUN — R302 *0_0805short_NC — +5V_AVDD

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

+3.3V_SUS, +3.3V_RUN

C360 0.1U/16V_4
C359 1U/6.3V_4
C358 0.1U/16V_4
C361 10U/6.3V_6

DVDD_IO should match with HDA Bus level

+5V_AVDD

C384 10U/6.3V_6
C393 1U/6.3V_4
C394 0.1U/16V_4

1A max current

+5V_RUN

C374 10U/6.3V_6
C380 0.1U/16V_4
C370 *10U/6.3V_6_NC
C371 *0.1U/16V_4_NC

U20

1	DVDD_CORE	AVDD1	27
3	DVDD_IO	AVDD2	38
9	DVDD	PVDD1	45
6	HDA_BITCLK	PVDD2	39
5	HDA_SDO	SENSE_A	13
10	HDA_SYNC	SENSE_B	14
8	HDA_SDI	HP0_PORTA_L	28
11	HDA_RST#	HP0_PORTA_R	29
47	EAPD	VREFOUT_A	23
2	DMIC_CLK/GPIO1	HP1_PORTB_L	31
4	DMIC0/GPIO2	HP1_PORTB_R	32
48	SPDIFOUT0/GPIO3	PORTC_L	19
46	DMIC1/GPIO0/SPDIFOUT1	PORTC_R	20
36	CAP+	VREFOUT_C/GPIO4	24
35	CAP-	PORTE_L	15
7	DVSS	PORTE_R	16
42	PVSS	PORTF_L	17
49	PAD	PORTF_R	18
		SPK_PORTD_+L	40
		SPK_PORTD_-L	41
		SPK_PORTD_+R	44
		SPK_PORTD_-R	43
		MONO_OUT	25
		PCBEEP	12
		VREFFILT	21
		CAP2	22
		V-	34
		VREG(+2.5V)	37
		AVSS1	26
		AVSS2	30
		AVSS3	33

92HD94B2X5NLGXYAX

[22] ACZ_SDOUT — ACZ_SDOUT
[22] ACZ_SYNC — ACZ_SYNC
[22] ACZ_SDIN0 — ACZ_SDIN0 — R277 33_4 — ACZ_SDIN0_CODEC
[22] ACZ_RST# — ACZ_RST#

+3.3V_RUN — R286 10K_4 — [31,38] NB_MUTE#

[27] DMIC_CLK — ER1 *0_0402short_NC — DMIC_CLK_ER
[27] DMIC_DATA — ER2 *0_0402short_NC — DMIC_DATA_ER

EC39 *10P_NC
EC38 *10P_NC

C396 4.7U/6.3V_6

SENSE_A — R282 20K/F_4 — HP_JD#
SENSE_B — R278 39.2K/F_4 — MIC_JD#

MIC1_L
MIC1_R
MIC1_VREFOUT

HP_OUT_L
HP_OUT_R

AUD_SPK_L+ [31]
AUD_SPK_L- [31]
AUD_SPK_R+ [31]
AUD_SPK_R- [31]
SUB_OUT [31]

AUD_PCBEEP — C364 0.1U/16V_4 — C375 0.1U/16V_4

R273 100K/F_4 — ACZ_SPKR — ACZ_SPKR [22]
R290 100K/F_4 — BEEP — BEEP [38]

C387 4.7U/6.3V_6
C395 4.7U/6.3V_6
C383 1U/6.3V_4
C379 10U/6.3V_6

PLACE CLOSE TO U1 PIN 13

+5V_AVDD — R280 2.49K/F_4 1% — SENSE_A — C369 1000P/50V_4 — AGND

PLACE CLOSE TO U1 PIN 14

+5V_AVDD — R291 10K_4 — SENSE_B

If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

R303 *0_0603short_NC
R271 *0_0603short_NC
R270 *0_0603short_NC
R269 *0_0603short_NC

AGND

Tied at one point only under the 92HD94 or near it.
QT change to short pad

Place C14~C17 close to Codec

R295 10K_4
R276 10K_4

Recommend to divide the amplitude of BEEP signal before input to PCBEEP pin.
R20,R21 are optional.

HP Jack

CON6

HP_OUT_L — R298 30/F_4 — HP_OUT_L_R — L12 HCB1608KF-601T10 — HP_OUT_L_RL
HP_OUT_R — R305 30/F_4 — HP_OUT_R_R — L14 HCB1608KF-601T10 — HP_OUT_R_RL

HP_JD#

C399 0.01U/25V_4
C377 0.01U/25V_4

AUDIO JACK 5P FR(H3.9)
Normal Open

AGND

C352 1U/6.3V_4

MIC1_VREFOUT — R272 4.7K_4 — R275 4.7K_4 — AGND

L24.L25,L30,L31,
FB_600ohm+-25%_100MHz
_200mA_0.6ohm DC

MIC Jack

CON5

MIC1_L — C349 2.2U/6.3V_6 — MIC1_L_C — L9 HCB1608KF-601T10 — MIC1_L_CL
MIC1_R — C357 2.2U/6.3V_6 — MIC1_R_C — L10 HCB1608KF-601T10 — MIC1_R_CL

MIC_JD#

C362 220P/50V_4
C347 220P/50V_4

AUDIO JACK 5P FR(H3.9)
Normal Open

AGND

Quanta Computer Inc.
PROJECT : R09A

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	CODEC	3A

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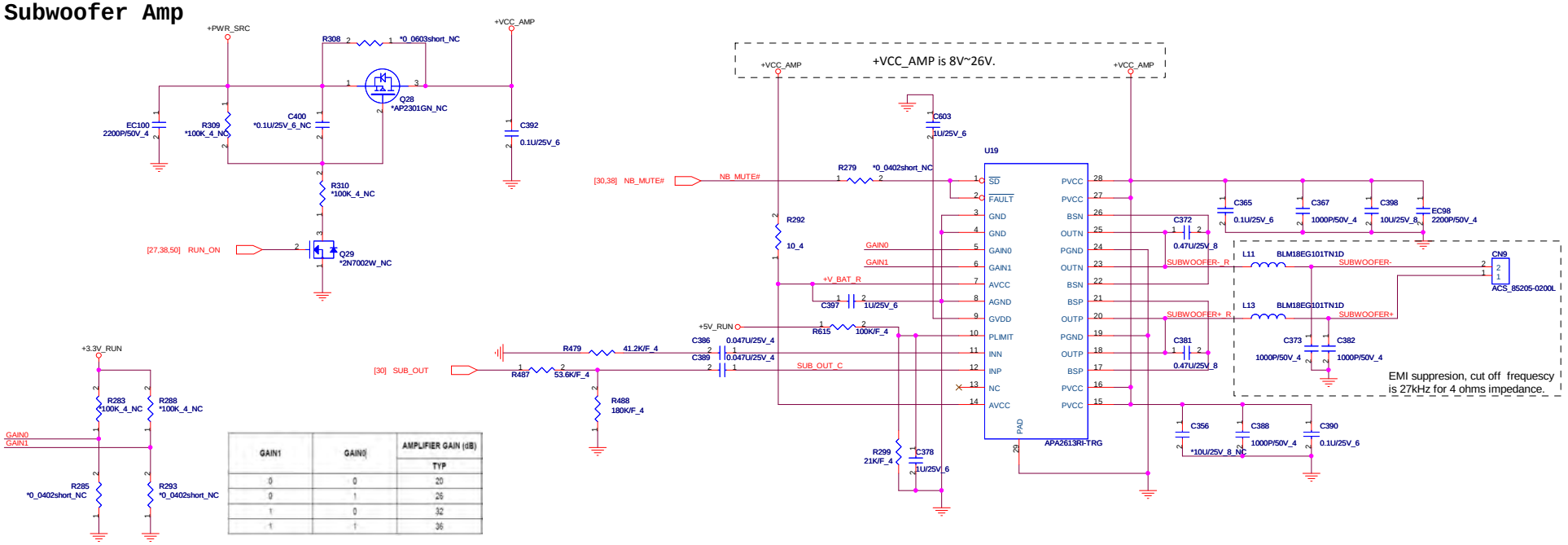
Subwoofer Amp

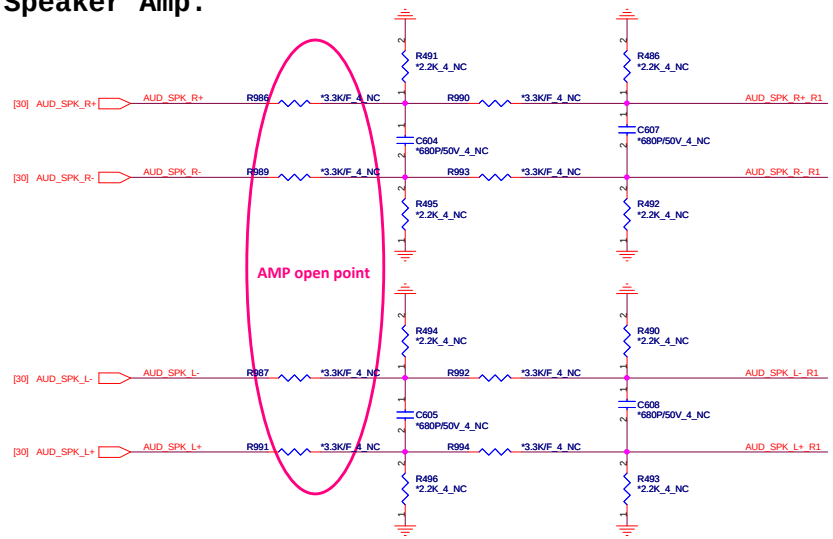


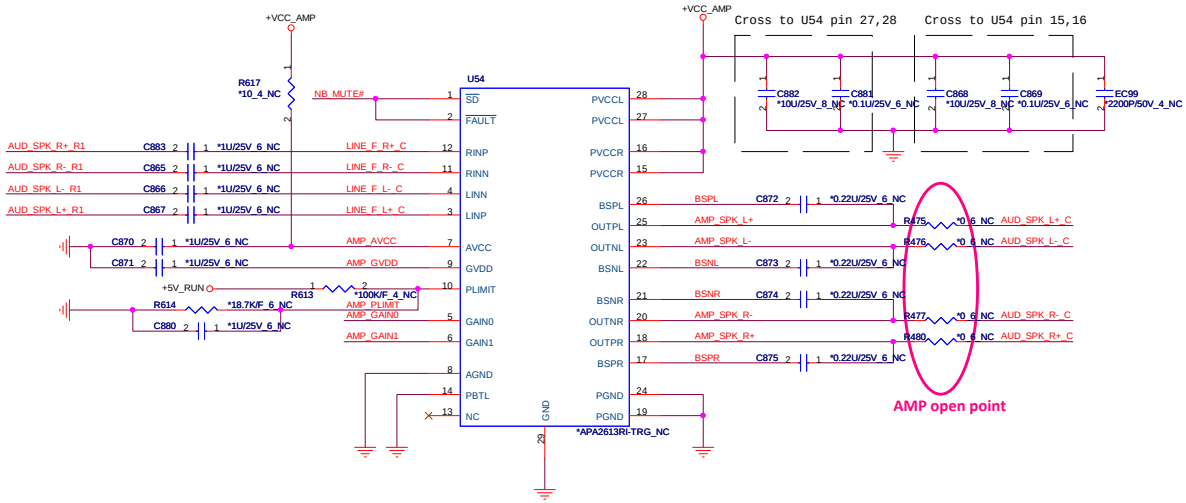
GAIN1	GAIN0	AMPLIFIER GAIN (dB)
		TYP
0	0	20
0	1	26
1	0	32
1	1	36

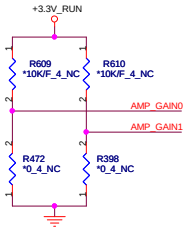
Speaker Amp.

R491,R495,R494,R496 default NC

APA2613 is P2P to TI TPA3113

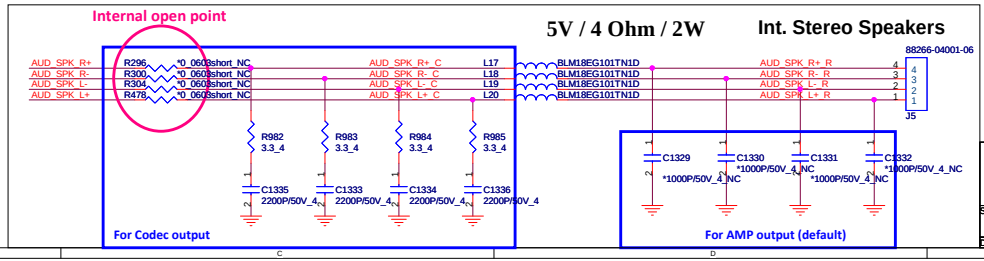






IDT default GAIN is 7dB

GAIN1	GAIN0	AMPLIFIER GAIN (dB)
		TYP
0	0	20
0	1	26
1	0	32
1	1	36



Quanta Computer Inc.

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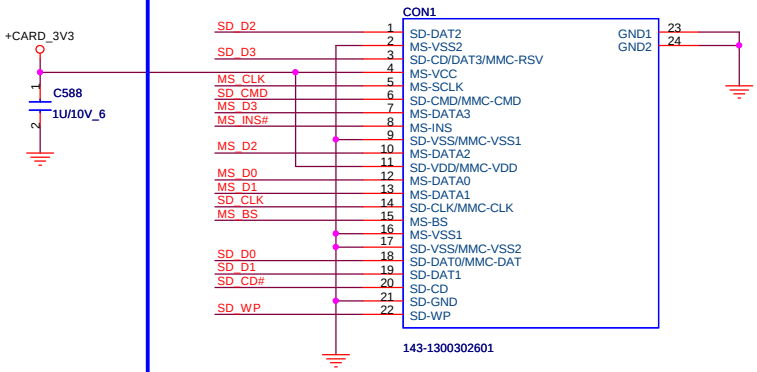
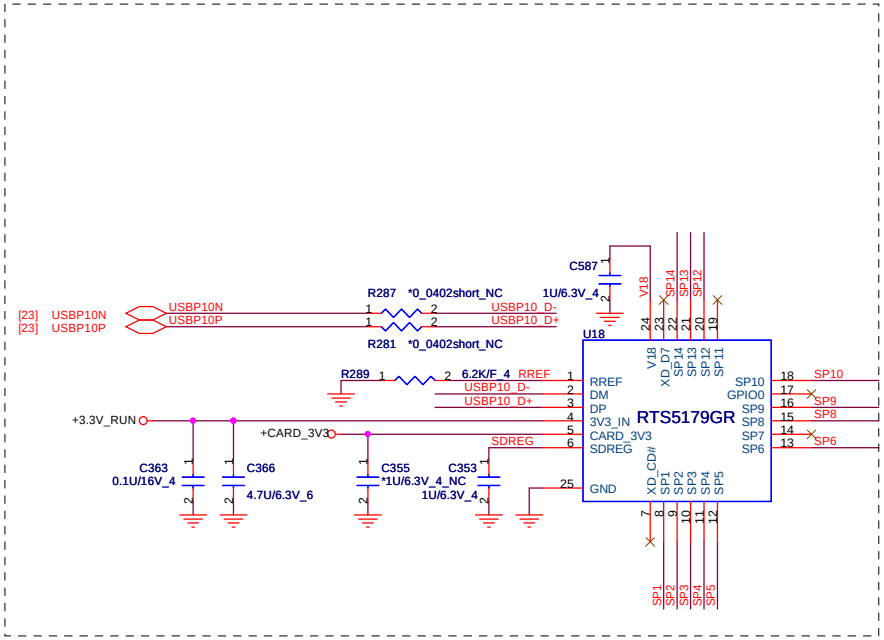
Size	Document Number	Rev
	WOOFER	3A
Date: Friday, March 02, 2012	Sheet 31 of 58	

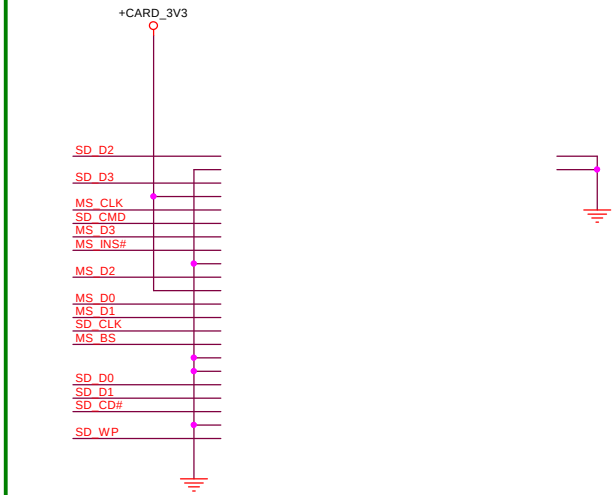
Cardreader (RTS5179GR) Support SD3.0 USH50

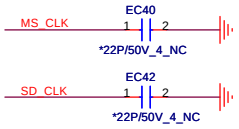
For INSPIRON Placement (R09,R09A,R09T)

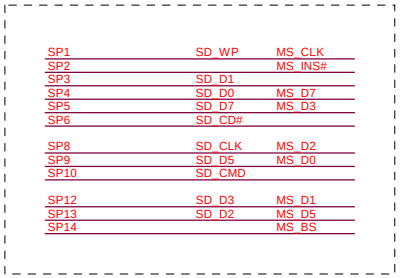




NA







Share Pin

Quanta Computer Inc.

PROJECT : R09A

Size	Document Number	Rev
	Cardreader (RTS5179GR)	3A

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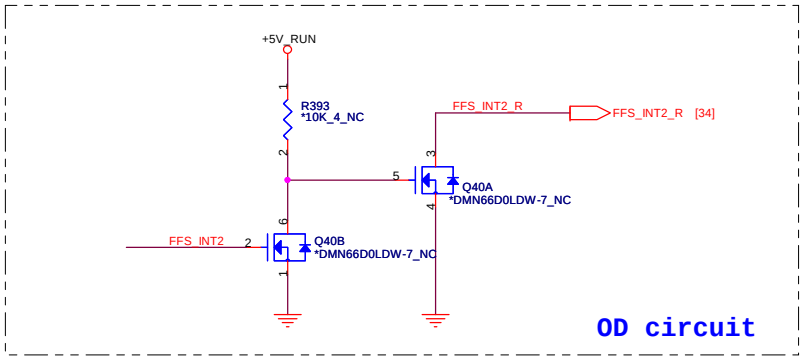
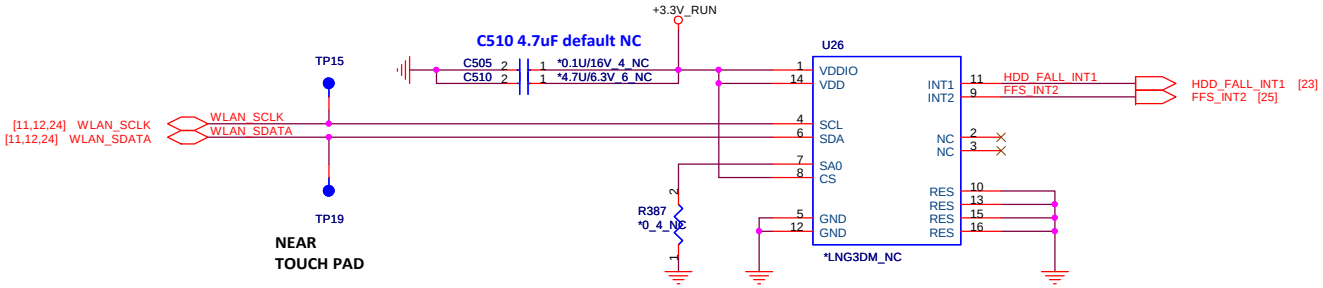
3-axis Fall Sensor - NC





SA0 is low: I2C device address is 00110000 (30h)

SA0 is high: I2C device address is 00110010 (32h)

Quanta Computer Inc.

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	3-axis Fall Sensor	3A
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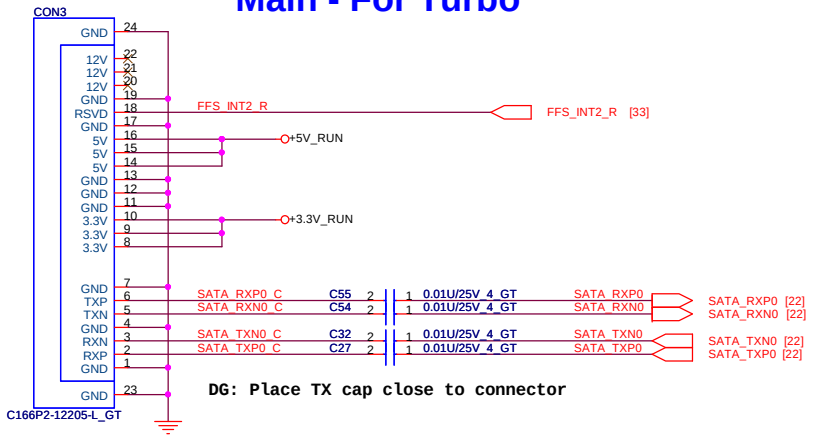
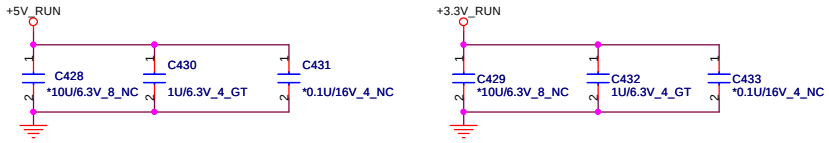
HDDX2

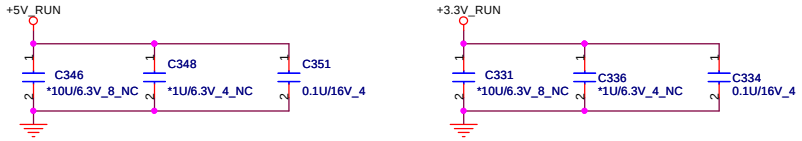
Main - For Turbo



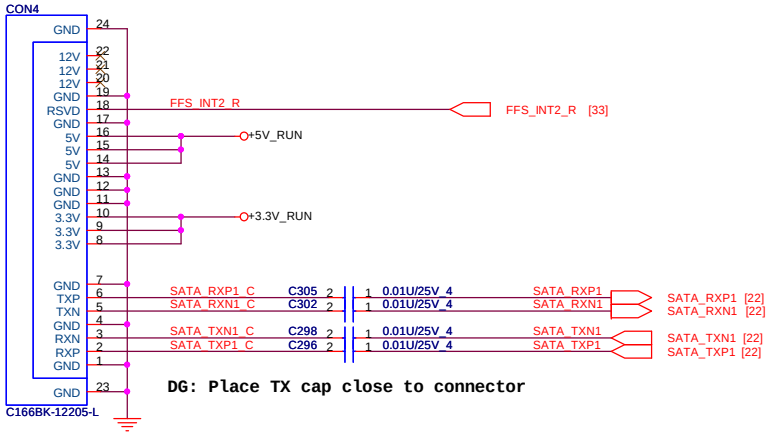


Default C351, C430 POP

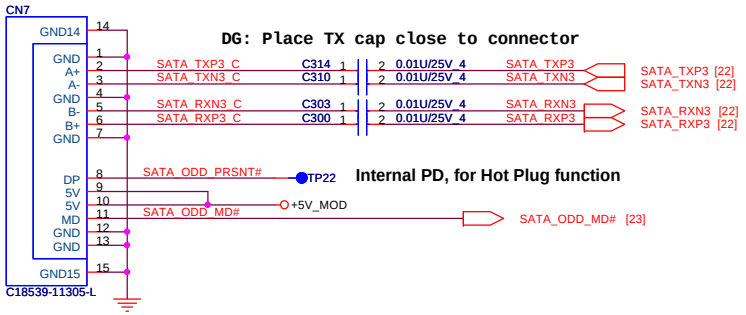
Default C334, C432 POP

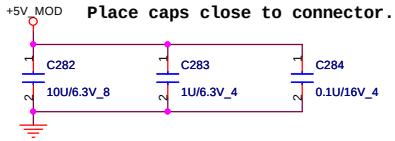


Second - For Inspiron

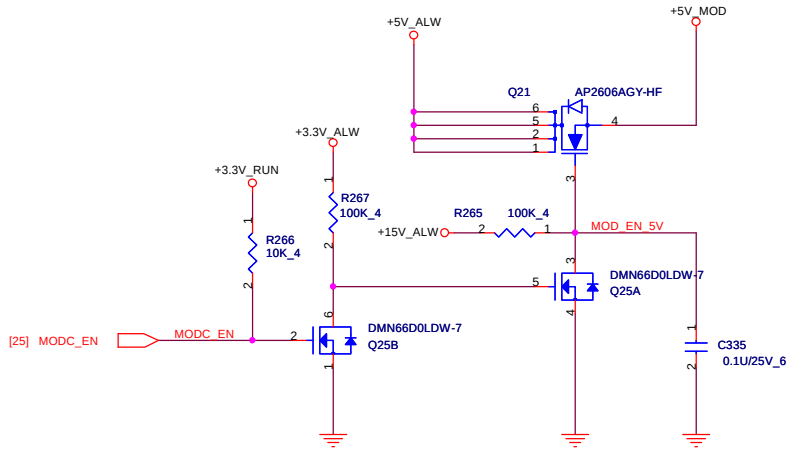


ODD





Support Zero power ODD



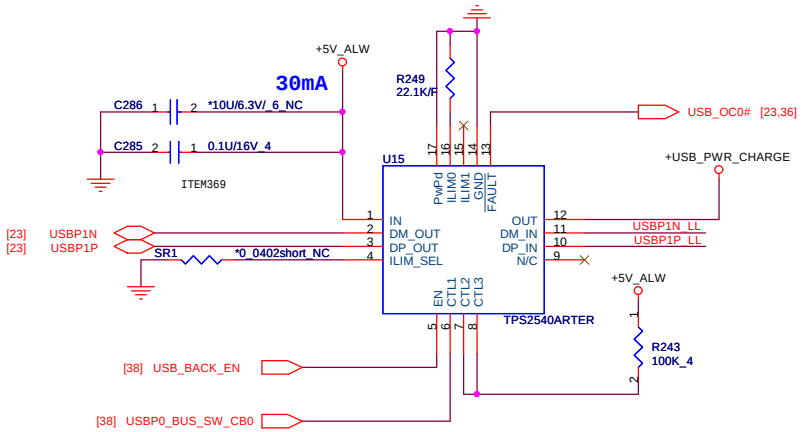
Quanta Computer Inc.

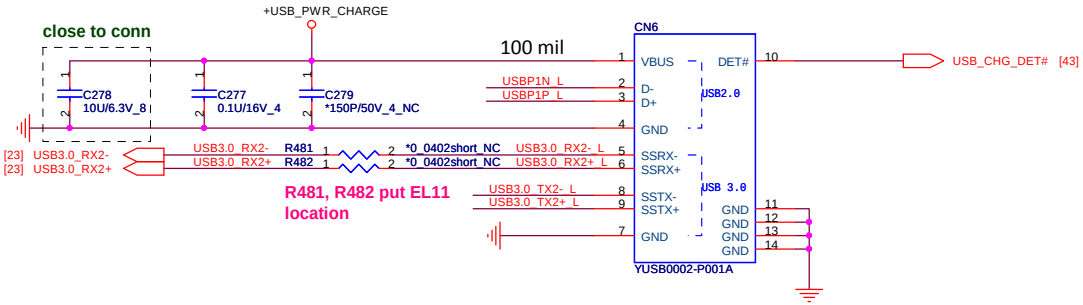
PROJECT : R09A

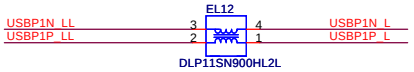
Size	Document Number	Rev
	SATA HDD/ODD	3A

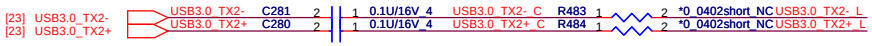
Date: Saturday, March 03, 2012 Sheet 34 of 58

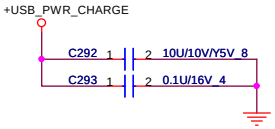
USB3.0x1 with Power share







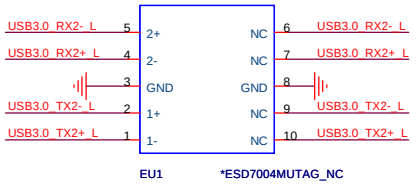




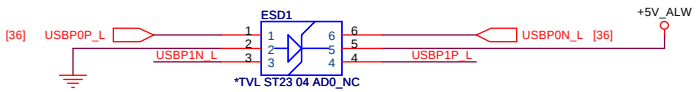
	R249	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

USBP0_BUS_SW_CB0	Mode	Operating at
Low	DCP, Auto-detect	S3/S4/S5, 1.5 A
High	CDP, BC Spec 1.1	S0, 1.5 A

USB 3.0 ESD



USB 2.0 ESD



Quanta Computer Inc.

PROJECT : R09A

Size	Document Number	Rev
	USB3.0 POWER SHARE	3A

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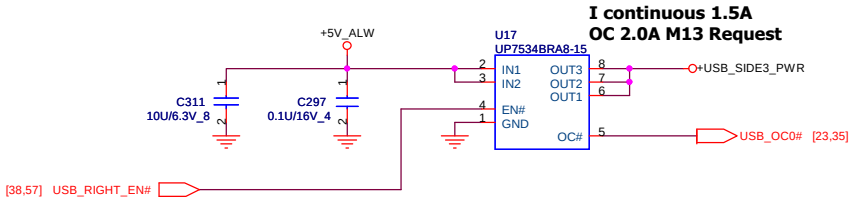
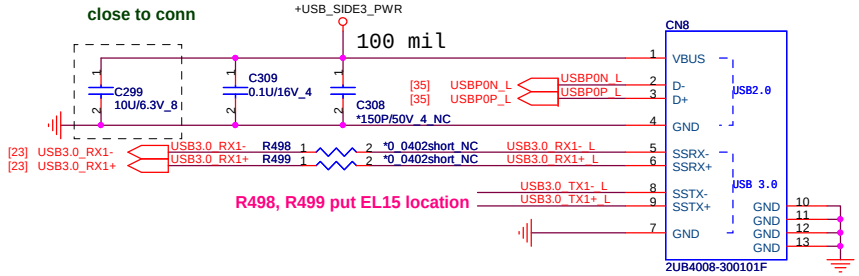
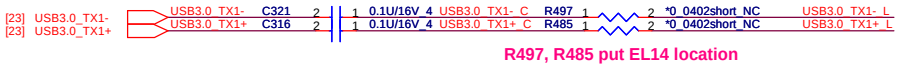
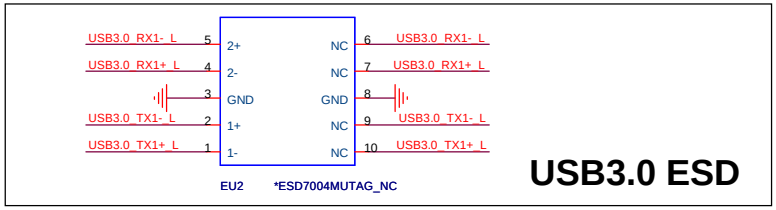
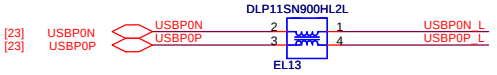
USB3.0x1











Quanta Computer Inc.		
PROJECT : R09A		
Size	Document Number: USB 3.0 port	Rev: 3A
Date: Friday, March 02, 2012	Sheet 36 of 58	

H19 *h-tc315bc236d118p2 h-tc315bc236d118p2
H24 *h-tc315bc236d118p2 H-TC315BC256D118P2
H23 *h-tc315bc236d118p2 h-tc315bc236d118p2
H20 *h-tc315bc236d118p2 h-tc315bc236d118p2
H25 *h-tc315bc354d118p2 h-tc315bc354d118p2
H18 *H-C433D433N H-C433D433N
H21 *o-r09-2 H-TC315BC236D118P2
H3 *o-r09-2 H-C118D118N
H2 *h-o189x228d189x228n h-o189x228d189x228n
H17 *H-O181X104D181X104N H-O181X104D181X104N
H6 *h-tc335bc315D118p2 h-tc335bc315D118p2
H12 *H-TC354BC315D118P2 H-TC354BC315D118P2
H22 *H-TC315BC354D118P2 H-TC315BC354D118P2
H5 *H-TC354BC315D118P2 H-TC354BC315D118P2
H10 *H-TC472BC315D118P2 H-TC472BC315D118P2
H13 *o-r09-1 o-r09-1
H7 *H-C154D154N H-C154D154N
H1 *H-C102D102N H-C102D102N
H4 *H-tc243bc154d154pt H-tc243bc154d154pt
H9 *H-C189D189N H-C189D189N
H16 *h-o165x106d165x106n h-o165x106d165x106n
H26 *O-R09-3 O-R09-3
H11 INTEL-CPU-BKT2 *INTEL-CPU-BKT2
CPU BLEKET
H8 H-TC217BC102D102PT H-TC217BC102D102PT
CPU NUT
MBIM3001010
H14 H-TC217BC102D102PT H-TC217BC102D102PT
mSATA NUT
MBIM3001010
H15 H-TC217BC65D61PT H-TC217BC65D61PT
WLAN NUT
FBFM8001010
+3.3V_SUS
Near H14
EC62 2200P/50V_4
EC63 1000P/50V_4
H27 *PAD-C197 PAD-C197
H28 *PAD-C177 PAD-C177
+3.3V_RUN
Near H22
EC64 2200P/50V_4
H29 *PAD-C189 PAD-C189
H30 *PAD-C189 PAD-C189
Near
C423/ESD2/H8/PR204/PR235/pq20/PL5/PC121/H10/R334/PL7/EC45
+PWR_SRC
EC66 1000P/50V_4
EC67 0.1U/25V_6
+PWR_SRC
EC77 2200P/50V_4
EC78 1000P/50V_4
EC79 0.1U/25V_6
+PWR_SRC
EC95 2200P/50V_4
EC97 0.1U/25V_6
+5V_ALW
EC96 2200P/50V_4
Near H26
+5V_ALW
EC102 0.1U/25V_6
Near EC96
+PWR_SRC
EC68 2200P/50V_4
EC69 1000P/50V_4
EC70 0.1U/25V_6
+PWR_SRC
EC80 2200P/50V_4
EC81 1000P/50V_4
EC82 0.1U/25V_6
+PWR_SRC
EC71 2200P/50V_4
EC72 1000P/50V_4
EC73 0.1U/25V_6
+PWR_SRC
EC83 2200P/50V_4
EC84 1000P/50V_4
EC85 0.1U/25V_6
+PWR_SRC
EC90 2200P/50V_4
EC89 1000P/50V_4
EC91 0.1U/25V_6
+VCC_DGFX_CORE
EC121 100P/50V_4
EC122 100P/50V_4
EC123 100P/50V_4
+PWR_SRC
EC74 2200P/50V_4
EC75 1000P/50V_4
+PWR_SRC
EC86 2200P/50V_4
EC87 1000P/50V_4
EC88 0.1U/25V_6
+PWR_SRC
EC93 2200P/50V_4
EC92 1000P/50V_4
EC94 0.1U/25V_6
Spring
S1 RHC-CP-55B01 SPAD-RE167X98
L5.6*W2.5*H5.5
S2 RHC-CP-25L03 SPAD-RE110X79
L3.5*W2.0*H2.5
AOI label
AOI LABEL on 31 header
PPID label
PPID LABEL on 31 header
AOI label
AOI LABEL on 31 header
Quanta Computer Inc.
PROJECT : R09A
Size
Document Number
SCREW HOLE
Rev 3A
Date: Wednesday, February 08, 2012
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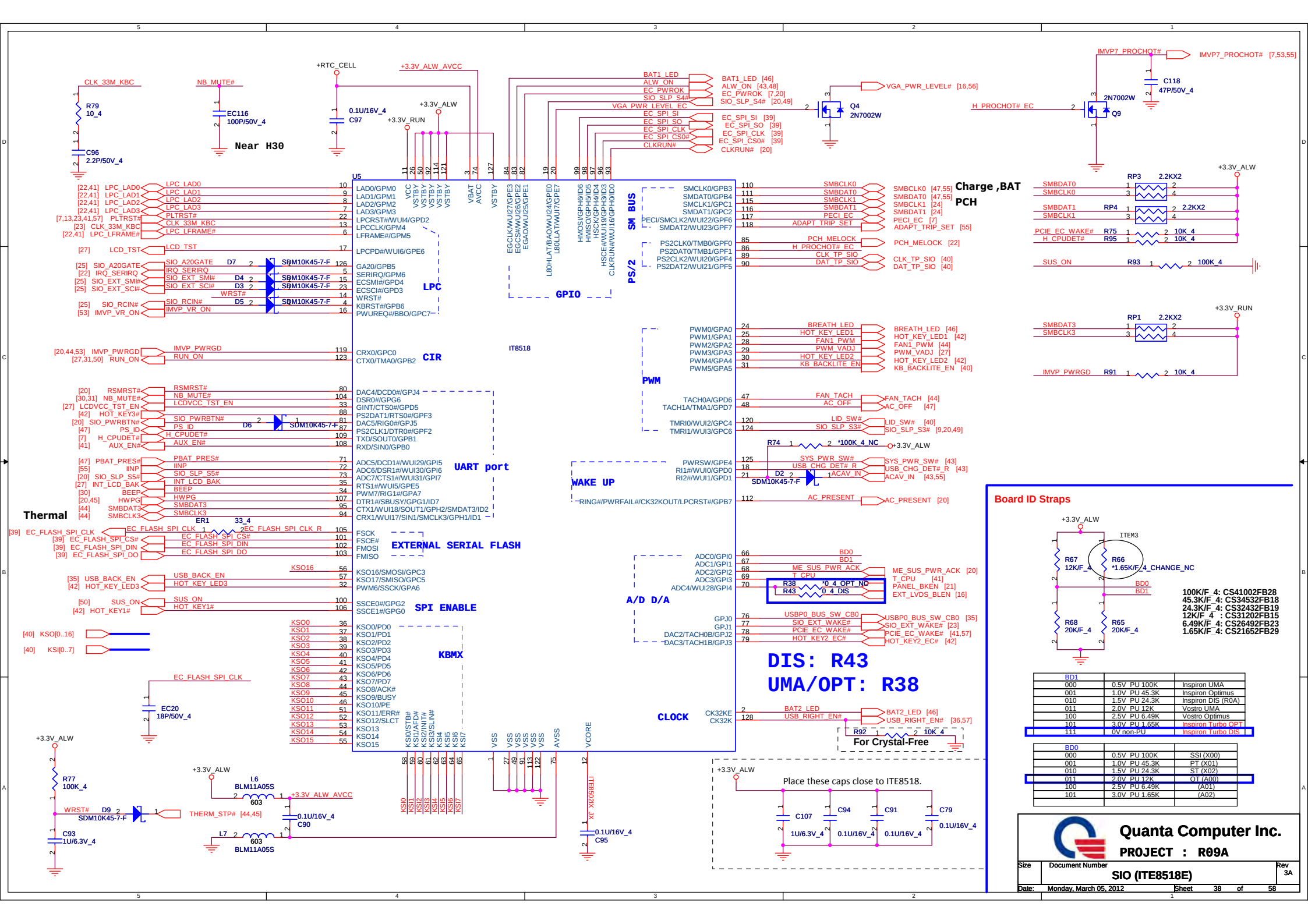
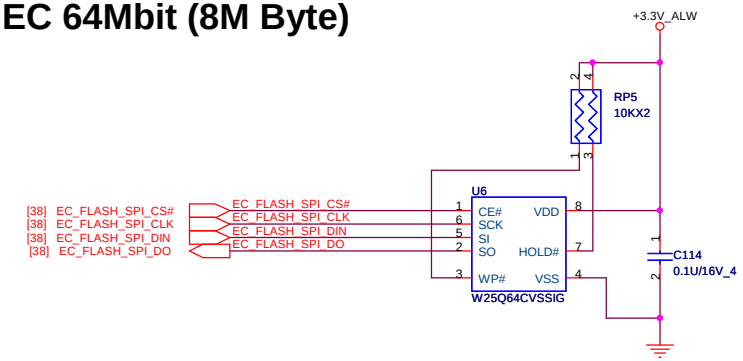
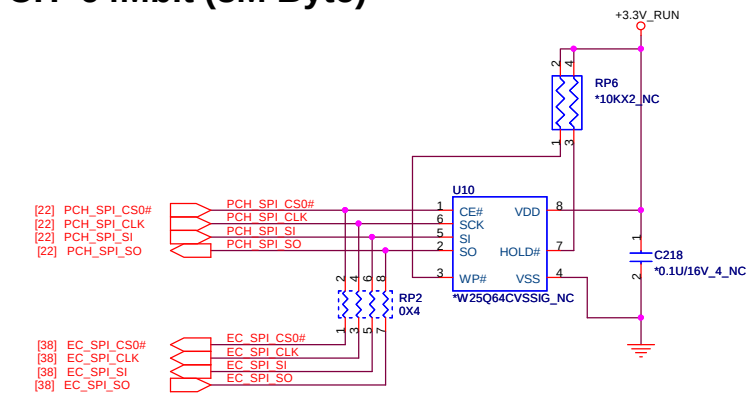

U5
IT8518
LPC
SM BUS
PS/2
GPIO
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Charge ,BAT
PCH
Thermal
Near H30
Board ID Straps
DIS: R43
UMA/OPT: R38
For Crystal-Free
Place these caps close to ITE8518.
Quanta Computer Inc.
PROJECT : R09A
SIO (ITE8518E)
Monday, March 05, 2012

FLASH / RTC

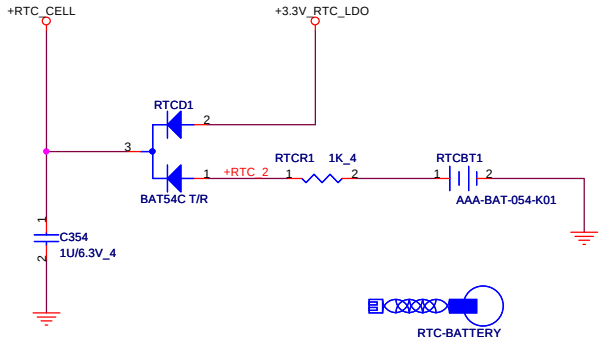
For EC 64Mbit (8M Byte)



For PCH 64Mbit (8M Byte)



RTC

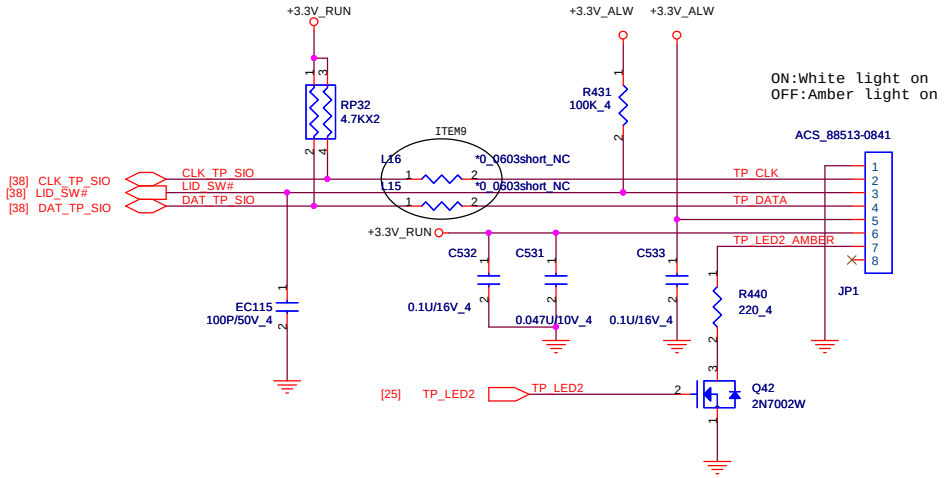


Double, 25'C, Vf=0.4V, If=25mA
one, 25'C, Vf=0.35V, If=15.8mA

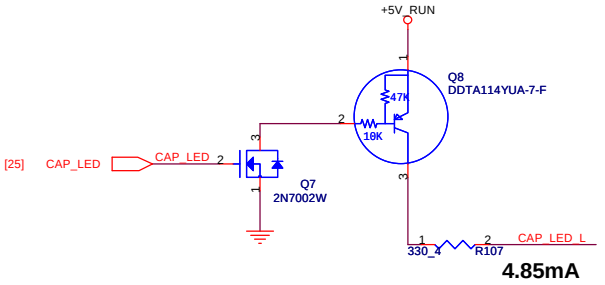
Quanta Computer Inc.
PROJECT : R09A

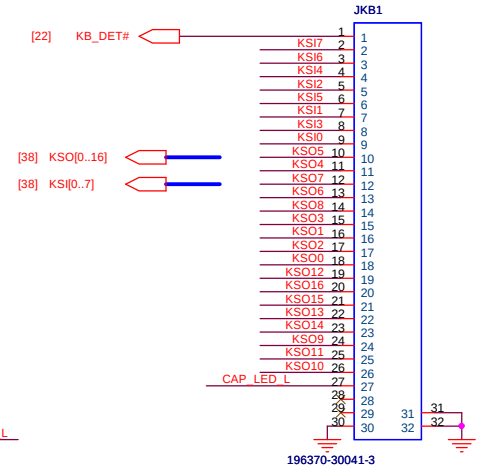
Size	Document Number	Rev
	FLASH / RTC	3A
Date: Wednesday, February 08, 2012	Sheet 39 of 58	

Touch Pad CONNECTOR



KEYBOARD CONNECTOR

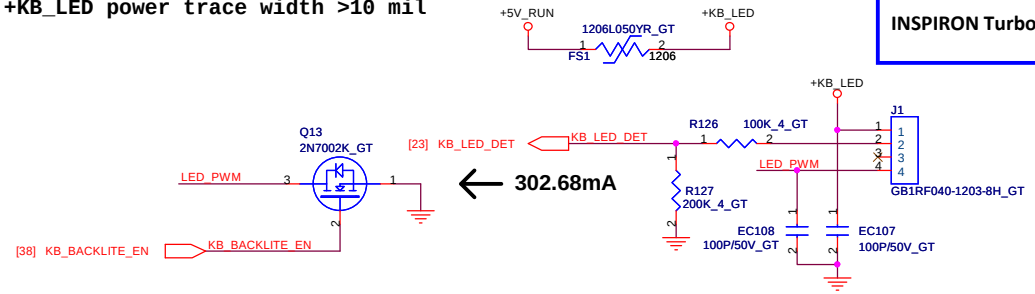


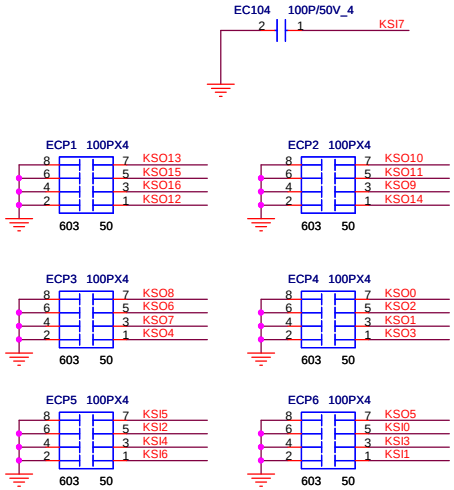


Key board illumination

+KB_LED power trace width >10 mil

INSPIRON	NC
INSPIRON Turbo	POP





Layout Note: 100P CAPS CLOSE TO JKB1

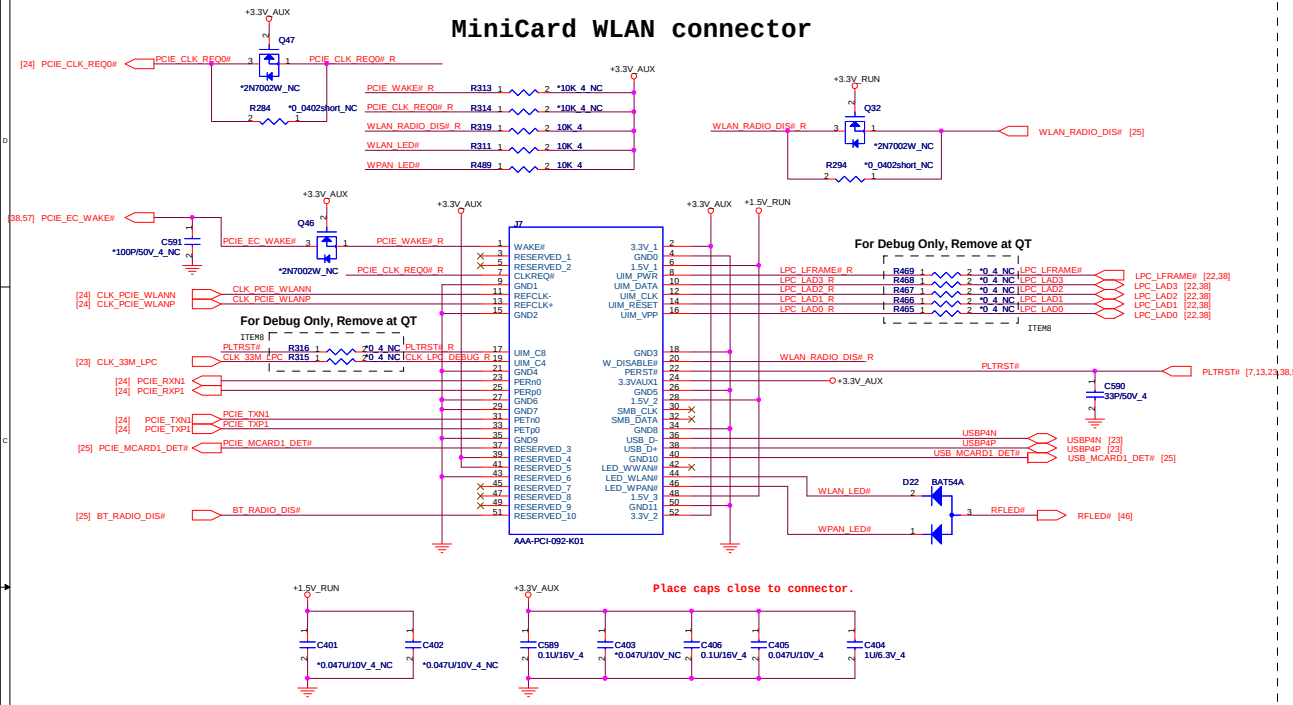
Quanta Computer Inc.

PROJECT : R09A

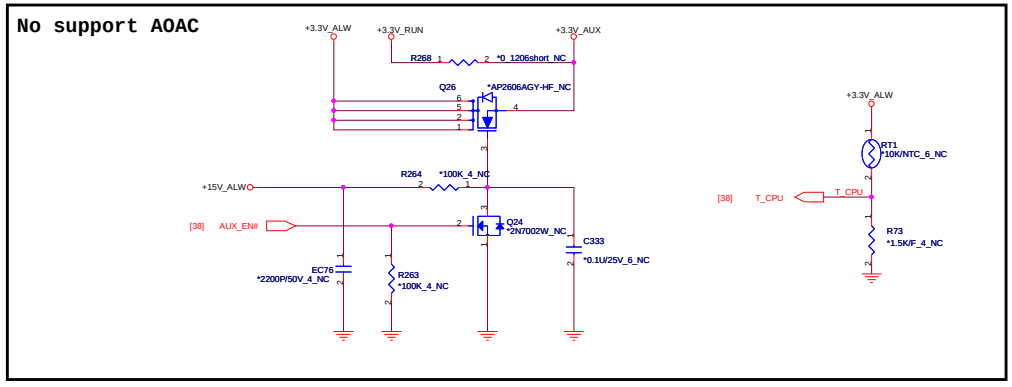
Size	Document Number	Rev
	TP / KB	3A

Date: Saturday, March 03, 2012 Sheet 40 of 58

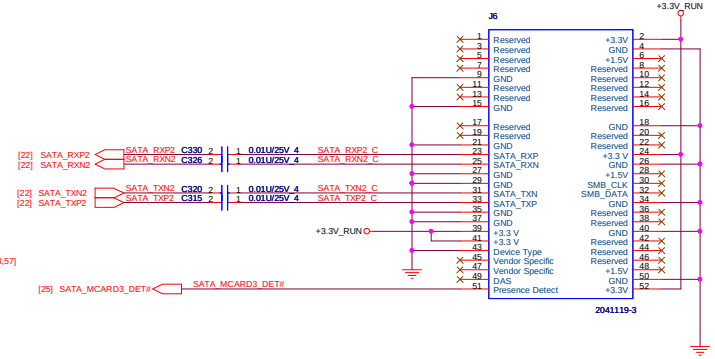
MiniCard WLAN connector

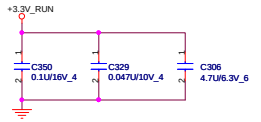


No support AOAC



MiniCard mSATA connector





Place caps close to connector.

Quanta Computer Inc.

PROJECT : R09A

Size	Document Number	Rev
	WLAN/mSATA	3A

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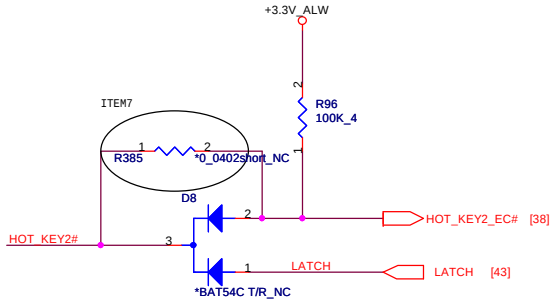
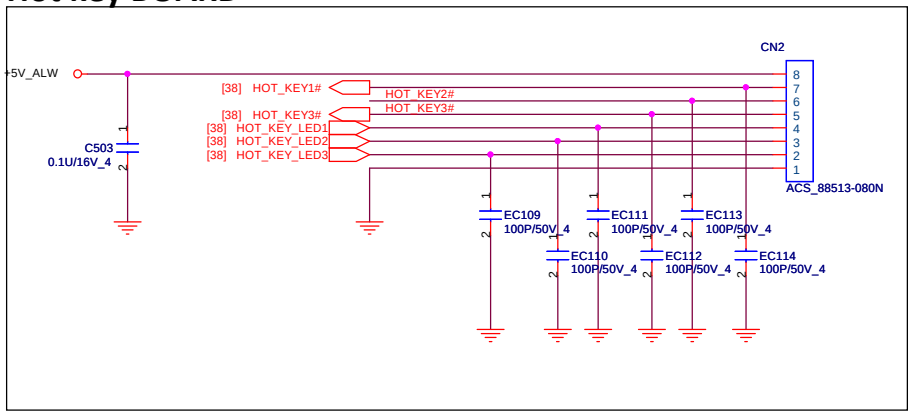
HOT_KEY2 support Pre-Boot Recovery



INSPIRON: R385 pop, D8 NC

Hot key BOARD



Quanta Computer Inc.

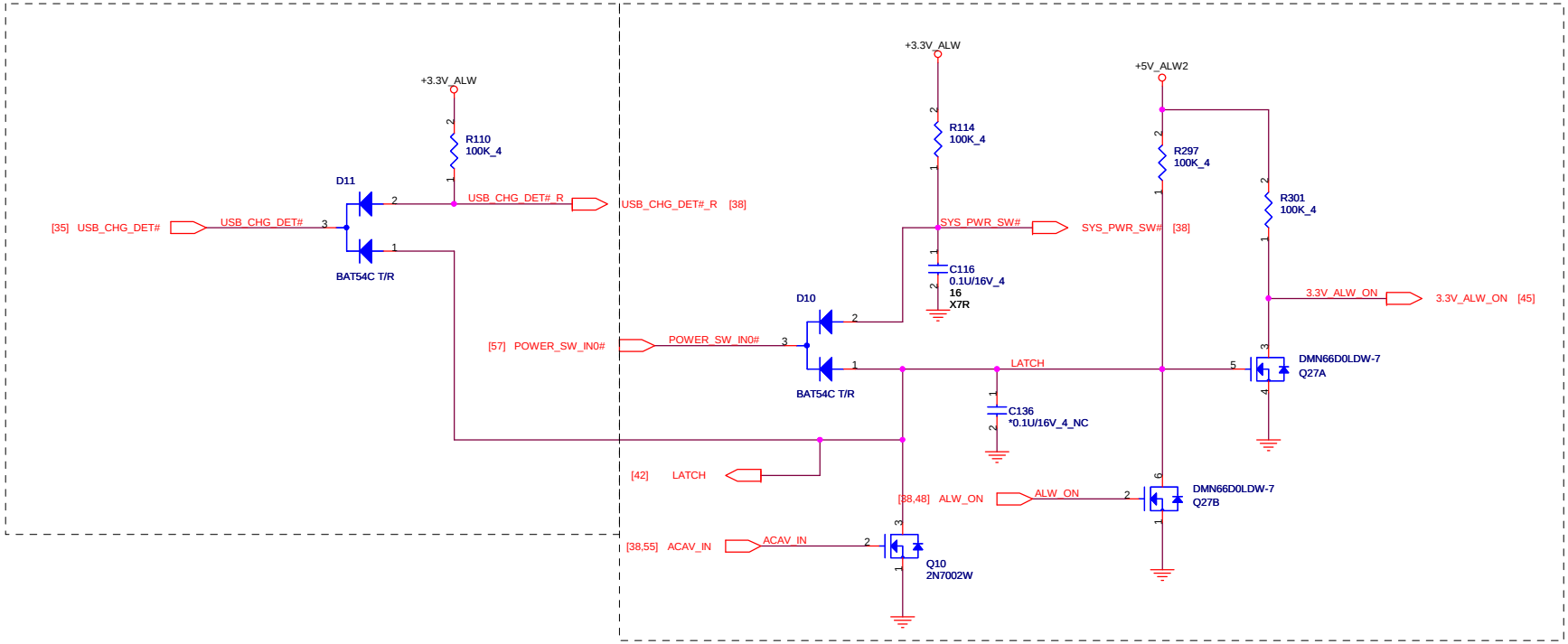
PROJECT : R09A

Size	Document Number	Rev
	HOT KEY	3A

Date: Wednesday, February 08, 2012 Sheet 42 of 58

For USB charger usage

3V ALW ON POWER LOGIC



Quanta Computer Inc.

PROJECT : R09A

Size	Document Number	Rev
	POWER SWITCH	3A

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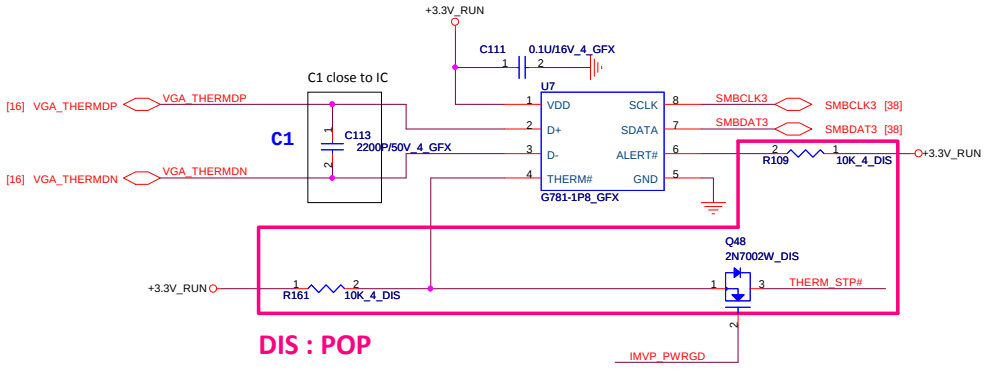
THERMAL IC

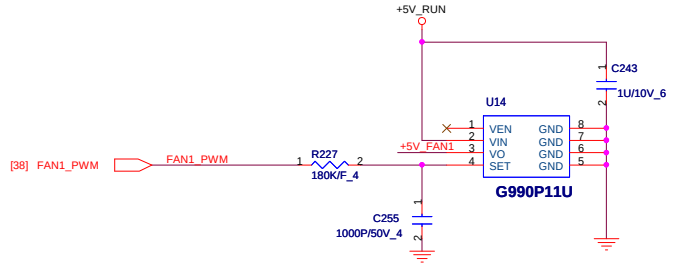
For GPU use

DIS/OPT:POP
UMA:NC

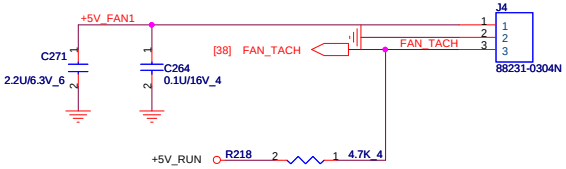
G781-1P8
SMBus address is 1001101xb (9Ah) (x is R/W bit).



DIS : POP
OPT: NC

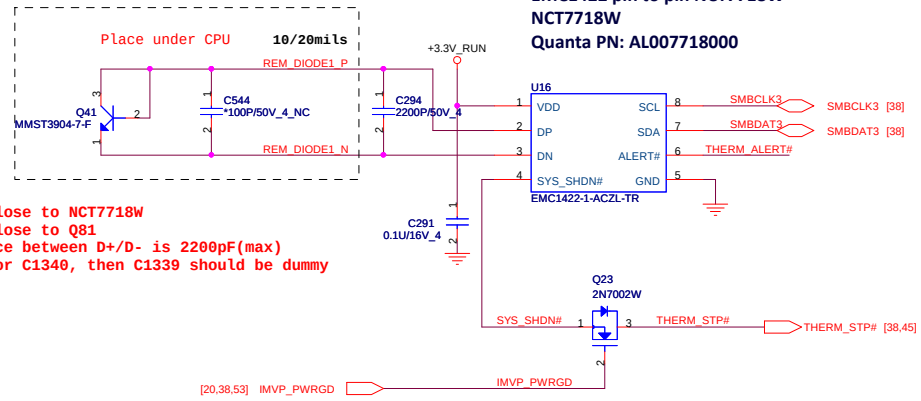


FAN CONN



For CPU use

Closed to CPU



Low cost
EMC1422 pin to pin NCT7718W
NCT7718W
Quanta PN: AL007718000

1.Place C1340 close to NCT7718W
2.Place C1339 close to Q81
Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C1340, then C1339 should be dummy

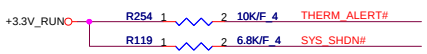
NCT7718W SMBus address is 1001100xb (98h) (x is R/W bit).

SYS_SHD# / ALERT#	2K	7.5K	10.5K	14K	18.7K
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C

EMC1422 SMBus address is 1001_100xb (98h) (x is R/W bit).

SYS_SHD# / ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C

OTP 85 degree C



EMC1422
OTP 85 degree : R996 = 10K, R997 = 6.8K
OTP 90 degree : R996 = 6.8K, R997 = 10K

Quanta Computer Inc.
PROJECT : R09A

Size	Document Number	Rev
	FAN & THERMAL	3A
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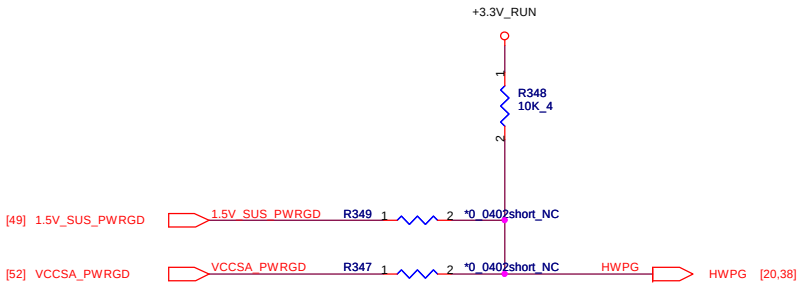
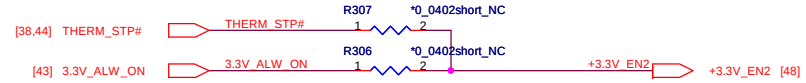
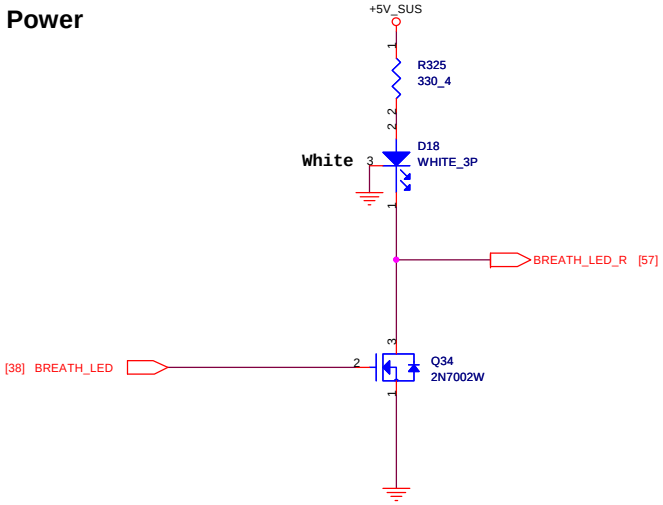


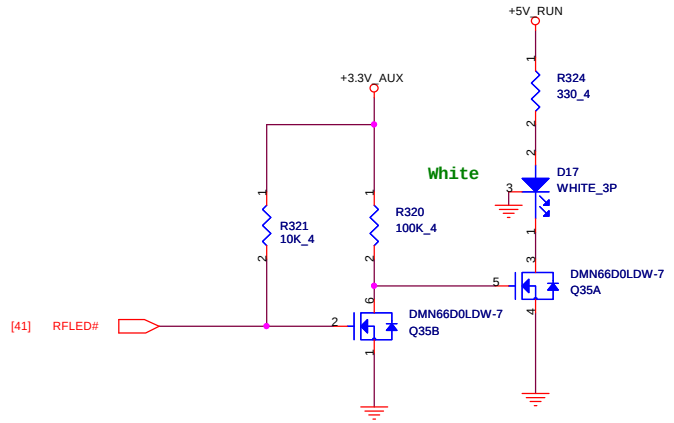


Quanta Computer Inc.		
PROJECT : R09A		
Size	Document Number: System Reset Circuit	Rev 3A
Date: Friday, March 02, 2012	Sheet 45 of 58	

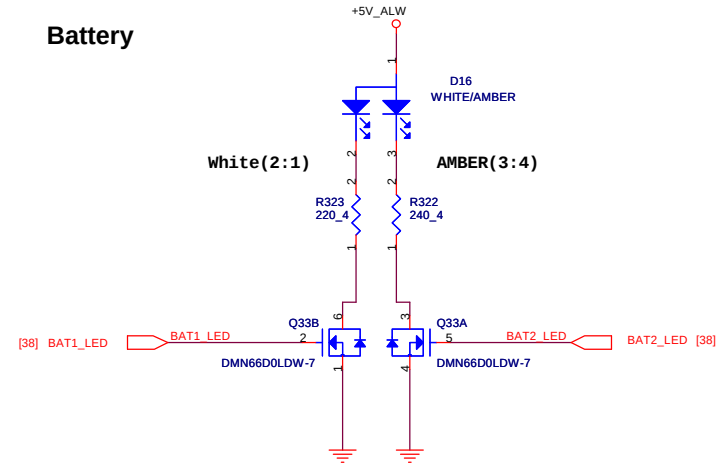
Power



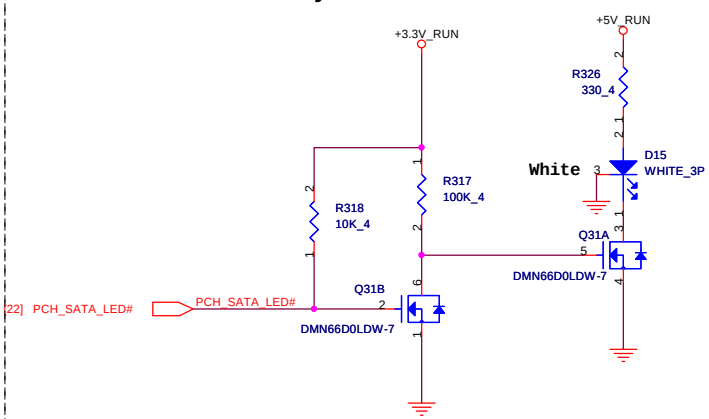
Bluetooth / WLAN on/off LED



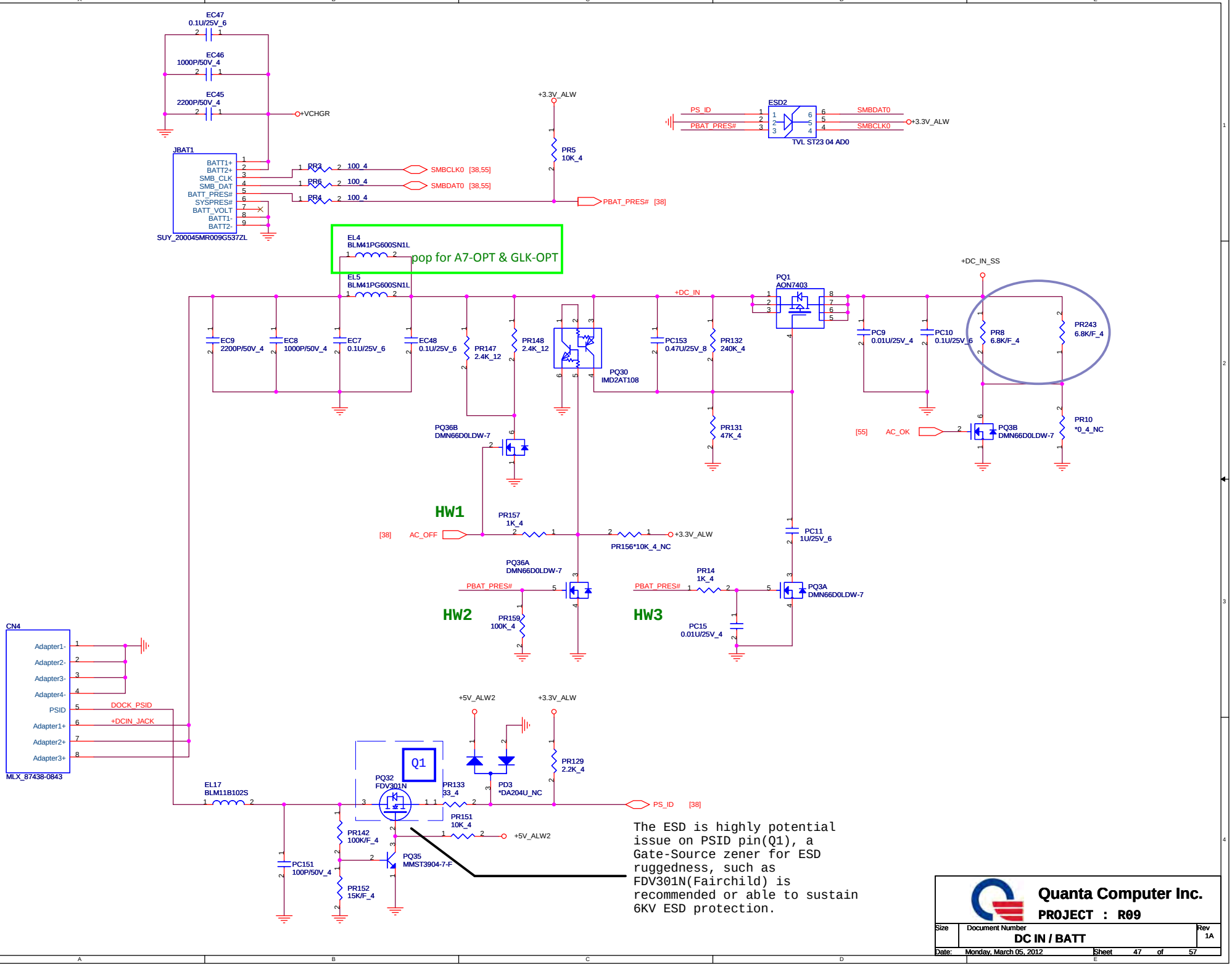
Battery



HDD activity LED.



Quanta Computer Inc.		
PROJECT : R09A		
Size	Document Number: LED	Rev: 3A
Date: Wednesday, February 08, 2012	Sheet 46 of 58	


EC47
0.1U/25V_6
EC46
1000P/50V_4
EC45
2200P/50V_4
+VCHGR
JBAT1
BATT1+
BATT2+
SMB_CLK
SMB_DAT
BATT_PRES#
SYSPRES#
BATT_VOLT
BATT1-
BATT2-
SUY_200045MR009G537ZL
PR3 100_4
PR6 100_4
PR4 100_4
SMBCLK0 [38,55]
SMBDAT0 [38,55]
+3.3V_ALW
PR5
10K_4
PBAT_PRES# [38]
ESD2
PS_ID
PBAT_PRES#
SMBDAT0
SMBCLK0
+3.3V_ALW
TVL ST23 04 AD0
EL4
BLM41PG600SN1L
pop for A7-OPT & GLK-OPT
EL5
BLM41PG600SN1L
+DC_IN
PQ1
AON7403
+DC_IN_SS
EC9
2200P/50V_4
EC8
1000P/50V_4
EC7
0.1U/25V_6
EC48
0.1U/25V_6
PR147
2.4K_12
PR148
2.4K_12
PQ30
IMD2AT108
PC153
0.47U/25V_8
PR132
240K_4
PC9
0.01U/25V_4
PC10
0.1U/25V_6
PR8
6.8K/F_4
PR243
6.8K/F_4
PQ36B
DMN66D0LDW-7
PR131
47K_4
[55] AC_OK
PQ3B
DMN66D0LDW-7
PR10
*0_4_NC
HW1
[38] AC_OFF
PR157
1K_4
PR156*10K_4_NC
+3.3V_ALW
PC11
1U/25V_6
PQ36A
DMN66D0LDW-7
PBAT_PRES#
HW2
PR159
100K_4
PBAT_PRES#
PR14
1K_4
PQ3A
DMN66D0LDW-7
HW3
PC15
0.01U/25V_4
CN4
Adapter1-
Adapter2-
Adapter3-
Adapter4-
PSID
Adapter1+
Adapter2+
Adapter3+
MLX_87438-0843
DOCK_PSID
+DCIN_JACK
+5V_ALW2
+3.3V_ALW
Q1
PQ32
FDV301N
PR129
2.2K_4
PD3
*DA204U_NC
EL17
BLM11B102S
PR133
33_4
PS_ID [38]
PR151
10K_4
+5V_ALW2
PR142
100K/F_4
PQ35
MMST3904-7-F
PC151
100P/50V_4
PR152
15K/F_4
The ESD is highly potential issue on PSID pin(Q1), a Gate-Source zener for ESD ruggedness, such as FDV301N(Fairchild) is recommended or able to sustain 6KV ESD protection.
Quanta Computer Inc.
PROJECT : R09
Size
Document Number
DC IN / BATT
Rev
1A
Date: Monday, March 05, 2012
Sheet 47 of 57

TPS51125A TONSEL Connection and Switching Frequency				
Ton	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz

+5V_ALW
Fsw : 300K
TDC : 10.8A
OCP : 15A

+3.3V_ALW
Fsw : 375K
TDC : 6.2A
OCP : 8.7A

PU4 TPS51125ARGER

PL1 2.2UH20%18A(TMPB1004M-2R2MN-Z01)

PL4 2.2UH20%12A(TMPB0603M-2R2MN-Z01)

PQ19 MDV1525URH

PQ18 MDV1522URH

PQ22 NTTFS4930N

PQ23 NTTFS4930N

AGND_DC/DC

close to output Cap

close to output Cap

Enable

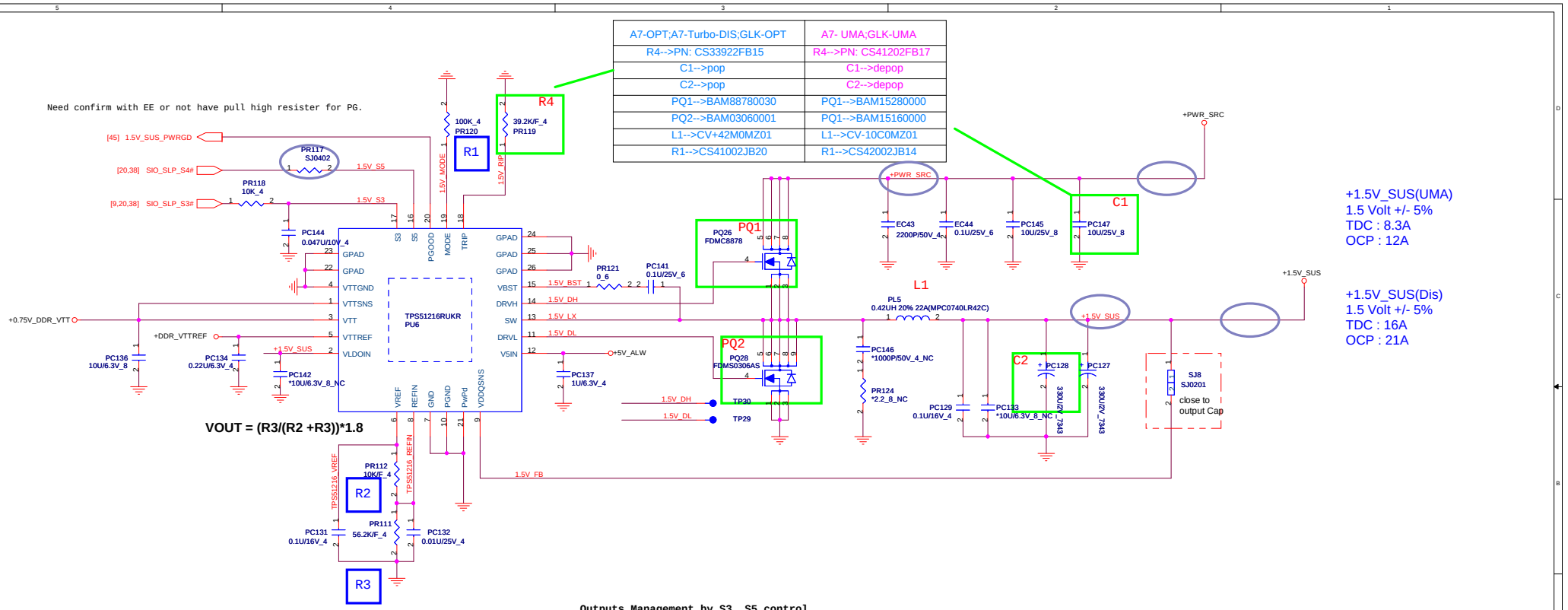
PQ20A DMN66D0LDW-7

PQ20B DMN66D0LDW-7

PQ16A DMN66D0LDW-7

PQ16B DMN66D0LDW-7

Quanta Computer Inc. PROJECT : R09			
Size	Document Number: 3.3V_ALW / 5V_ALW (TPS51125ARGER)		Rev 1A
Date: Monday, March 05, 2012	Sheet 48 of 57		



A7-OPT;A7-Turbo-DIS;GLK-OPT	A7- UMA;GLK-UMA
R4-->PN: CS33922FB15	R4-->PN: CS41202FB17
C1-->pop	C1-->depop
C2-->pop	C2-->depop
PQ1-->BAM88780030	PQ1-->BAM15280000
PQ2-->BAM03060001	PQ1-->BAM15160000
L1-->CV+42M0MZ01	L1-->CV-10C0MZ01
R1-->CS41002JB20	R1-->CS42002JB14

+1.5V_SUS(UMA)
1.5 Volt +/- 5%
TDC : 8.3A
OCP : 12A

+1.5V_SUS(Dis)
1.5 Volt +/- 5%
TDC : 16A
OCP : 21A

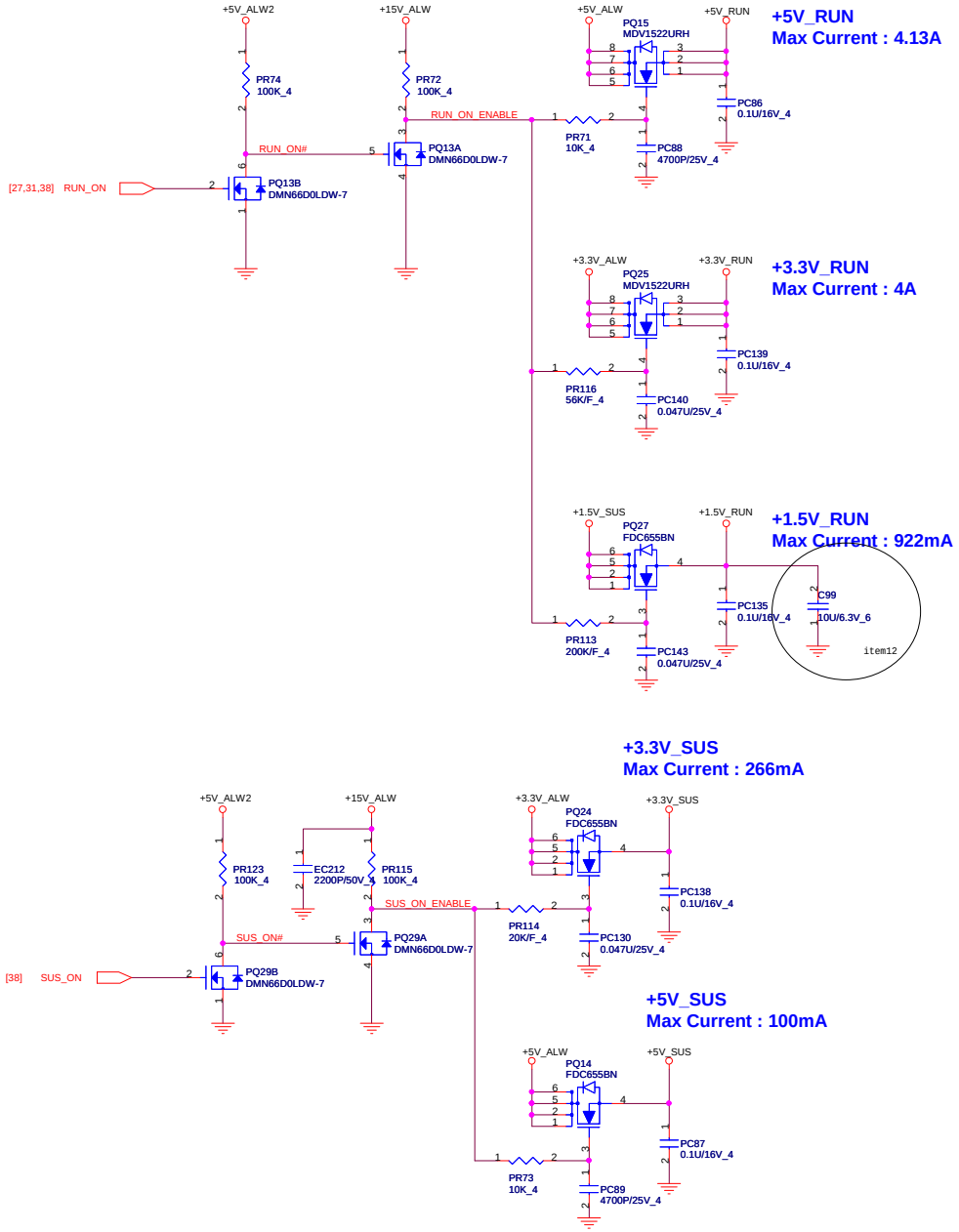
MODE Selection				
	Resistance between MODE and GND		Frequency	Discharge Mode
R1	200K_4	CS42002JB14	400k Hz	Tracking Discharge
R1	100K_4	CS41002JB20	300k Hz	
R1	68K_4	CS36802JB12	300k Hz	Non-tracking
R1	47K_4	CS34702JB21	400k Hz	Discharge

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

Quanta Computer Inc.
PROJECT : R09

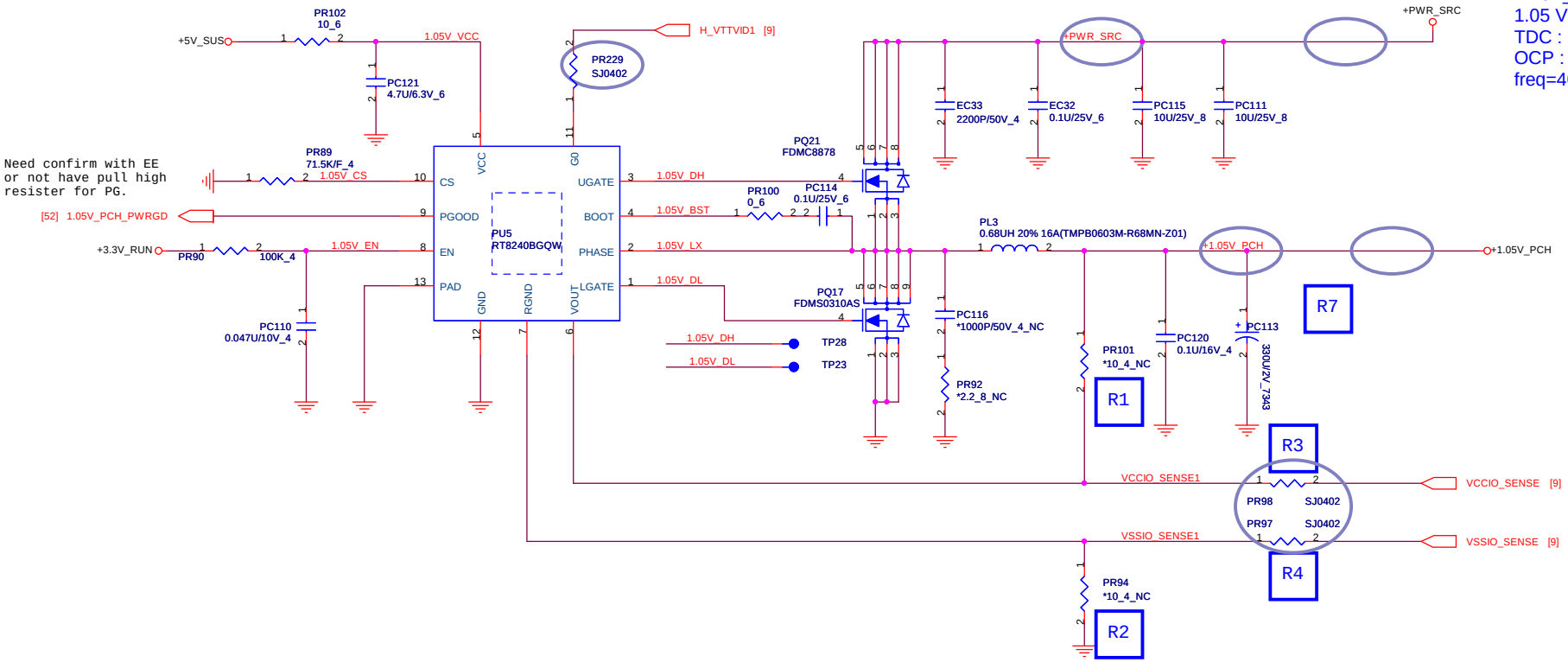
Size	Document Number	Rev
	1.5_SUS/0.75_DDR_VTT (TPS51216RUKR)	1A
Date: Monday, March 05, 2012	Sheet 49 of 57	



Quanta Computer Inc.

PROJECT : R09

Size	Document Number	Rev
	Load Switch	1A
Date: Monday, March 05, 2012	Sheet 50 of 57	



For EA test	
R1	10_4
R2	10_4
R3	NC
R4	NC
R5	NC
R6	NC
R7	NC

Quanta Computer Inc.
PROJECT : R09

Size	Document Number	Rev
	+1.05V_PCH / VTT (RT8240BGQW)	1A

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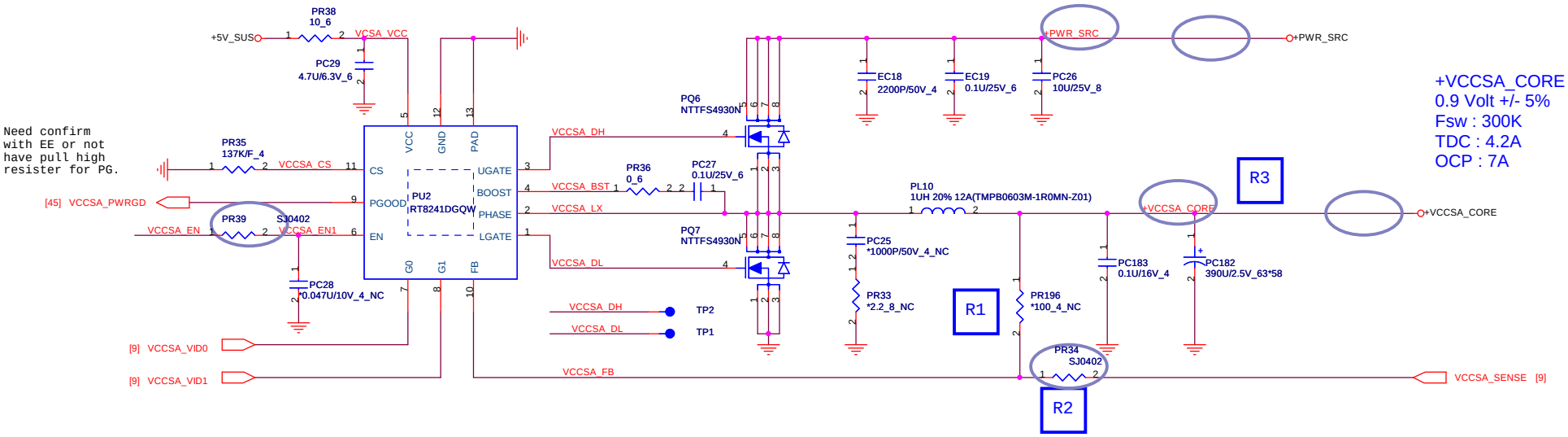
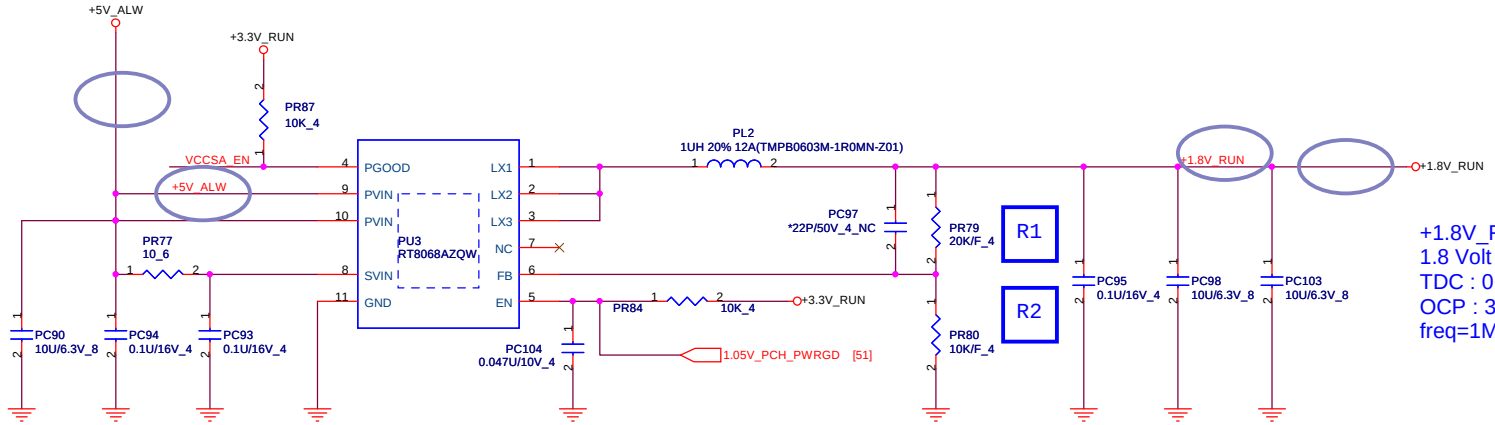


+VCCSA_CORE
0.9 Volt +/- 5%
Fsw : 300K
TDC : 4.2A
OCP : 7A

VCCSA_VID1	VCCSA_VID0	VCCSA_CORE
Low	Low	0.9V
High	Low	0.8V
Low	High	0.725V
High	High	0.675V

For EA test	
R1	100_4
R2	NC
R3	NC
R4	NC



+1.8V_RUN
1.8 Volt +/- 5%
TDC : 0.869A
OCP : 3.5A
freq=1M

VOUT = 0.6(1+R1/R2)

Quanta Computer Inc.
PROJECT : R09

Size	Document Number	Rev
	VCCSA (RT8241DGQW)	1A

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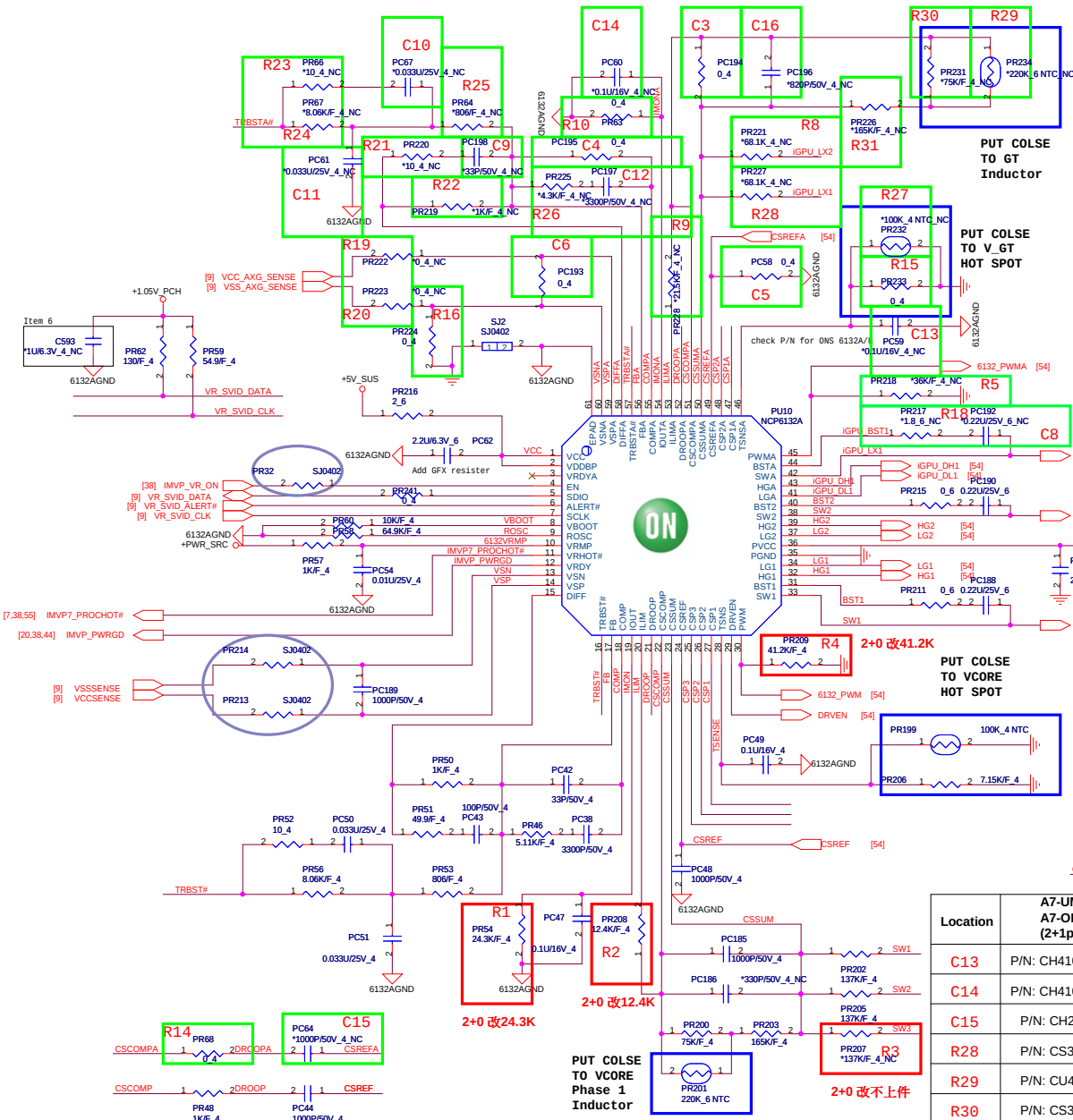

Location	A7-UMA A7-OPT (2+1phase)	A7 Turbo-DIS (3phase)	GLK-UMA GLK-OPT (3+2phase)
R1	P/N: CS32432FB01	P/N: CS32372FB05	P/N: CS32372FB05
R2	P/N: CS31242FB05	P/N: CS32102FB14	P/N: CS32102FB14
R3	depop	P/N: CS41302FB01	P/N: CS41302FB01
R4	P/N: CS34122FB19	P/N: CS37322FB14	P/N: CS37322FB14
R5	P/N: CS32552FB03	depop	P/N: CS33602FB07
R6	depop	P/N: CS25112FB15	P/N: CS25112FB15
C1	depop	P/N: CH34702KB10	P/N: CH34702KB10
R7	depop	depop	P/N: CS25112FB15
C2	depop	depop	P/N: CH34702KB10
R8	depop	depop	P/N: CS35762FB11
R9	P/N: CS31582FB12	depop	P/N: CS32152BB00
R10	P/N: CS32432FB01	P/N: CS00002JB38	P/N: CS32402FB15
R11	depop	P/N: CS00002JB38	depop
R12	P/N: CS00002JB38	P/N: CS00002JB38	depop
R13	P/N: CS00002JB38	depop	depop
C3	P/N: CH21006JB10	P/N: CS00002JB38	P/N: CH21006JB10
C4	P/N: CH01006JB08	P/N: CS00002JB38	P/N: CH01006JB08
C5	P/N: CH21006JB10	P/N: CS00002JB38	P/N: CH21006JB10
R14	P/N: CS15102FB19	P/N: CS00002JB38	P/N: CS15102FB19
C6	P/N: CH21006JB10	P/N: CS00002JB38	P/N: CH21006JB10
R15	P/N: CS28252FB15	P/N: CS00002JB38	P/N: CS28252FB15
R16	depop	P/N: CS00002JB38	depop
R17	P/N: CS25112FB15	depop	P/N: CS25112FB15
C7	P/N: CH34702KB10	depop	P/N: CH34702KB10
R18	P/N: CS00003J951	depop	P/N: CS00003J951
C8	P/N: CH4224K9904	depop	P/N: CH4224K9904
R19	P/N: CS00002JB38	depop	P/N: CS00002JB38
R20	P/N: CS00002JB38	depop	P/N: CS00002JB38
R21	P/N: CS01002JB22	depop	P/N: CS01002JB22
R22	P/N: CS21002FB24	depop	P/N: CS21002FB24
C9	P/N: CH03306JB04	depop	P/N: CH03306JB04
R23	P/N: CS01002JB22	depop	P/N: CS01002JB22
R24	P/N: CS22002FB19	depop	P/N: CS22002FB19
C10	P/N: CH16806KB17	depop	P/N: CH16806KB17
C11	P/N: CH24704KB19	depop	P/N: CH24704KB19
R25	P/N: CS31072FB10	depop	P/N: CS31072FB10
R26	P/N: CS24302FB07	depop	P/N: CS24302FB07
R28	P/N: CS35762FB11	depop	P/N: CS35762FB11
R29	P/N: CU422090000	depop	P/N: CU422090000
R30	P/N: CS37502FB12	depop	P/N: CS37502FB12
R31	P/N: CS41652FB14	depop	P/N: CS41652FB14
C12	P/N: CH23306JB16	depop	P/N: CH23306JB16
R27	P/N: CU4100B0000	depop	P/N: CU4100B0000

Location	A7-UMA A7-OPT (2+1phase)	A7 Turbo-DIS (3phase)	GLK-UMA GLK-OPT (3+2phase)
C13	P/N: CH4103K1B08	depop	P/N: CH4103K1B08
C14	P/N: CH4103K1B08	depop	P/N: CH4103K1B08
C15	P/N: CH21006JB10	depop	P/N: CH21006JB10
R28	P/N: CS35762FB11	depop	P/N: CS35762FB11
R29	P/N: CU422090000	depop	P/N: CU422090000
R30	P/N: CS37502FB12	depop	P/N: CS37502FB12
R31	P/N: CS41652FB14	depop	P/N: CS41652FB14
C16	P/N: CH18206KB11	depop	P/N: CH18206KB11

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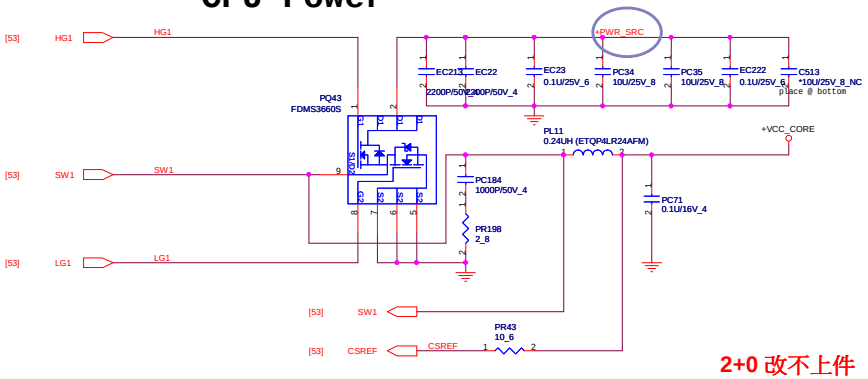
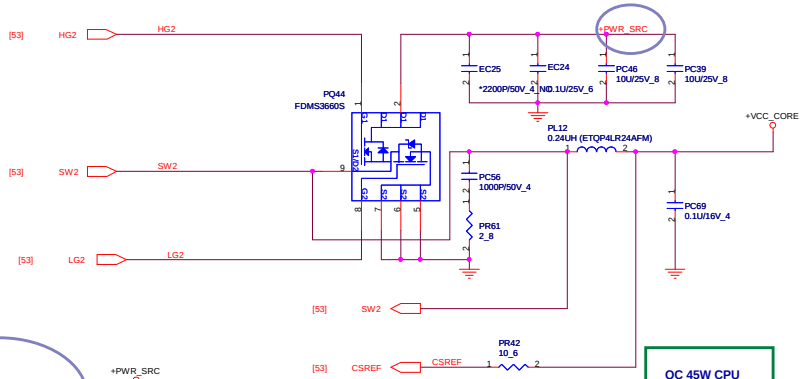
CPU Power

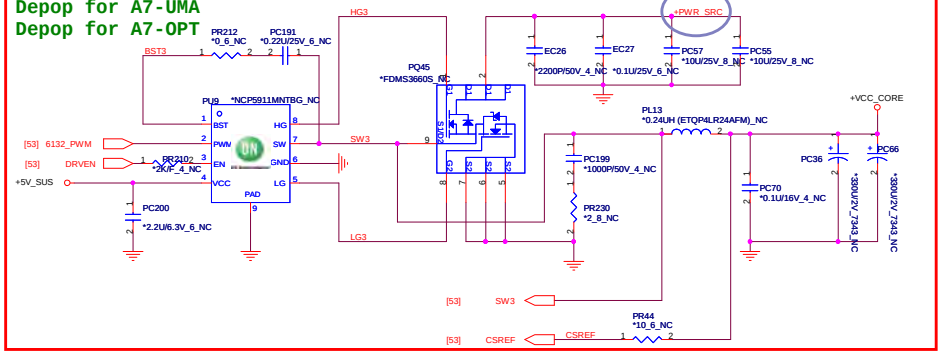


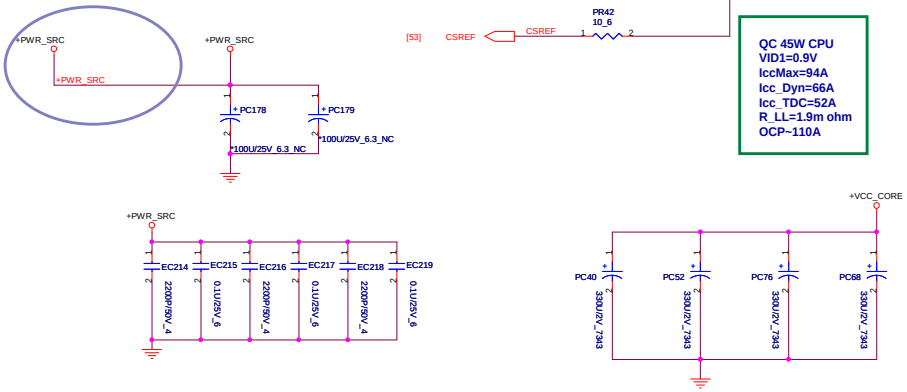


2+0 改不上件

QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

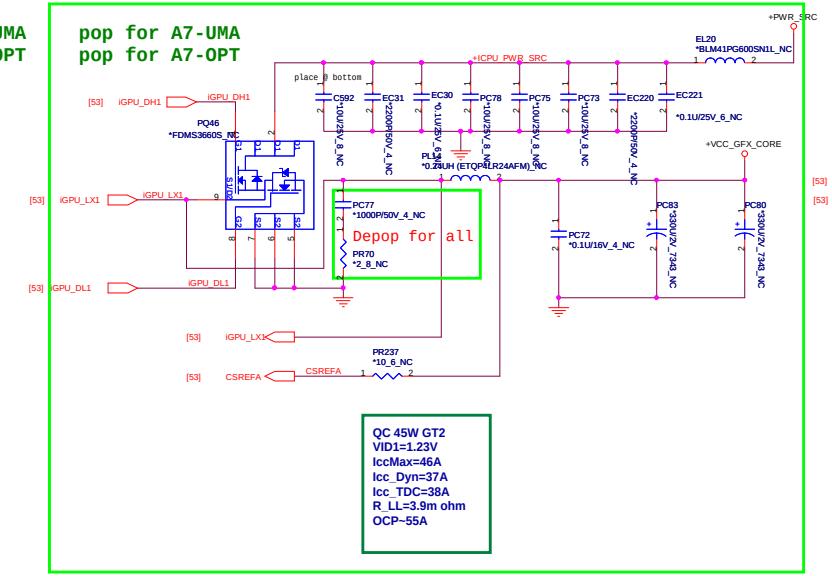
Depop for A7-UMA
Depop for A7-OPT

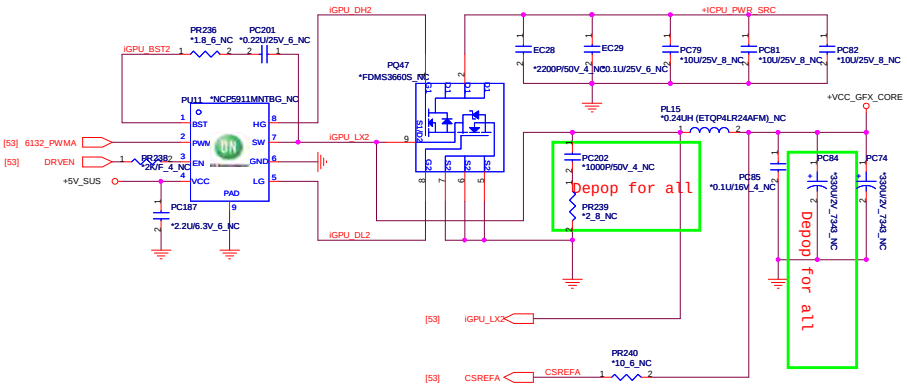




pop for GLK UMA
pop for GLK OPT

pop for A7-UMA
pop for A7-OPT





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	CPU_CORE (NCP6132)	1A
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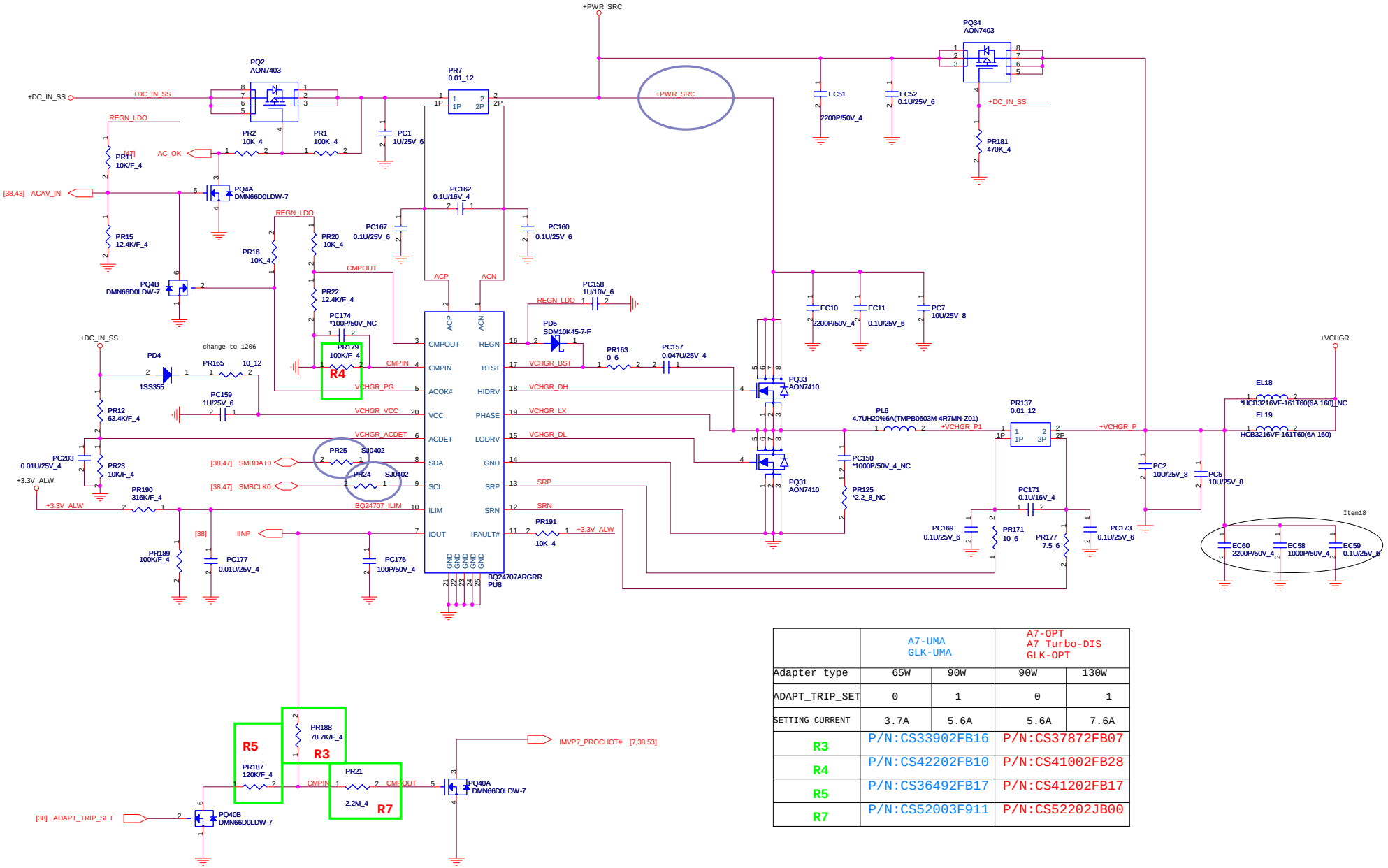

	A7-UMA GLK-UMA		A7-OPT A7 Turbo-DIS GLK-OPT	
Adapter type	65W	90W	90W	130W
ADAPT_TRIP_SET	0	1	0	1
SETTING CURRENT	3.7A	5.6A	5.6A	7.6A
R3	P/N:CS33902FB16		P/N:CS37872FB07	
R4	P/N:CS42202FB10		P/N:CS41002FB28	
R5	P/N:CS36492FB17		P/N:CS41202FB17	
R7	P/N:CS52003F911		P/N:CS52202JB00	

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	Charger (BQ24765RUVR)	1A

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Depop for A7-UMA
Depop for GLK-UMA

N13XXX2

	DGPU_VID3	DGPU_VID2	DGPU_VID1
0.85V	1	0	1
0.95V	0	1	1
1.0V	0	1	0

N13XXX1

	DGPU_VID3	DGPU_VID2	DGPU_VID1
0.825V	1	0	1
0.975V	0	1	0
1.0V	0	0	1

+VCC_GFX_CORE
Fs=400K
Dis =30A
Turbo =42A
Dis OC=42A
Turbo OC=60A

PR130 pop; PR135,PR242 depop
for Nvidia OS sample

Need confirm with EE
or not have pull high
resister for PG.

PU7
NCP3218MNR2G

PUT COLSE TO
+VCC_GFX_CORE
Phase 1 Inductor

For EA test	
R1	100_4
R2	100_4
R3	NC
R4	NC

Location	A7-OPT GLK-OPT (2phase)	A7 Turbo-DIS (3phase)
R5	P/N: CS41202FB17	P/N: CS37872FB15
R6	P/N: CS46492FB00	P/N: CS45622FB11
R7	P/N: CS21402FB02	P/N: CS22152FB07
R8	Depop	P/N: CS42742FB00
R9	P/N: CS00002JB38	Depop
R10	Depop	P/N: CS00002JB38

Depop for A7-OPT
Depop for GLK-OPT

PU1
ADP3611_DIS

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	VGA_N11P-dGFX (NCP3218MNR2G)	1A

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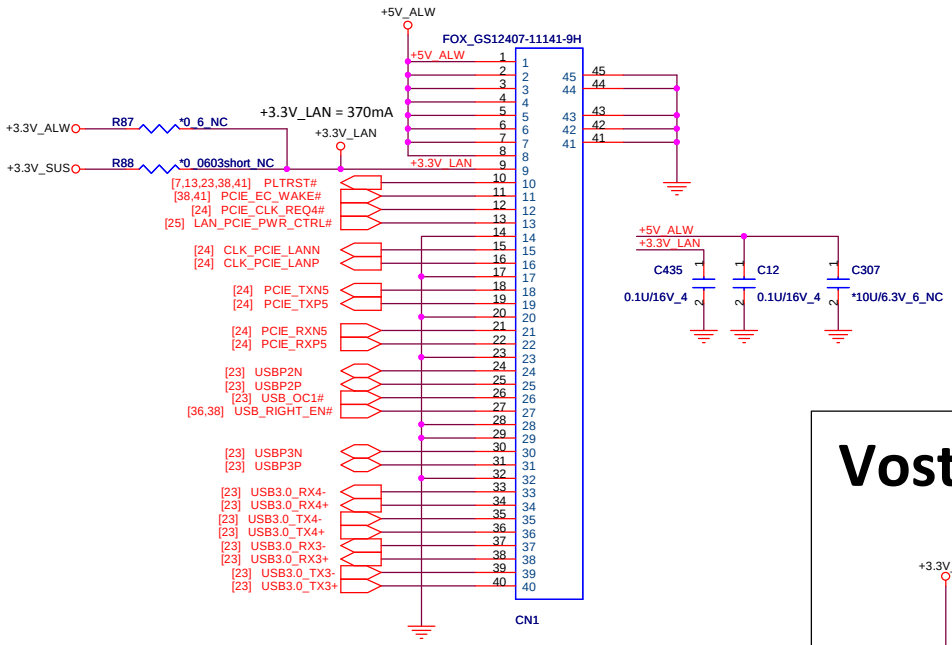
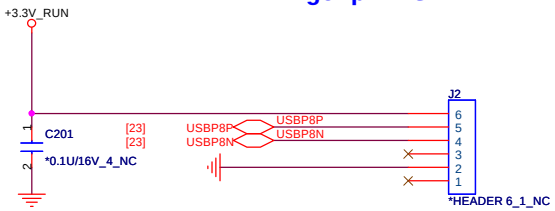
DB CONNECTOR

RJ45 + USB 3.0* 2

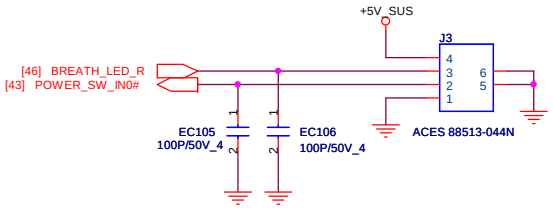


Vostro - NA

Fingerprint



Power button board



Quanta Computer Inc.		
PROJECT : R09A		
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