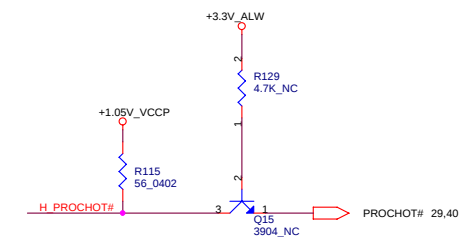
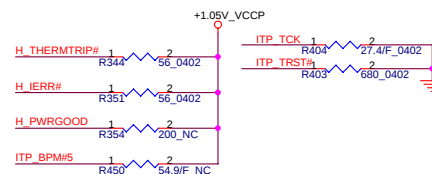
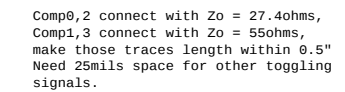
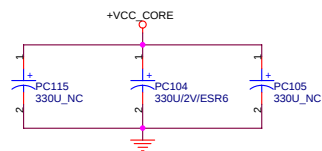
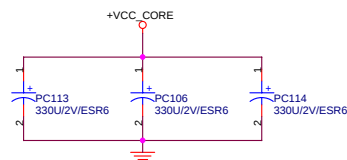
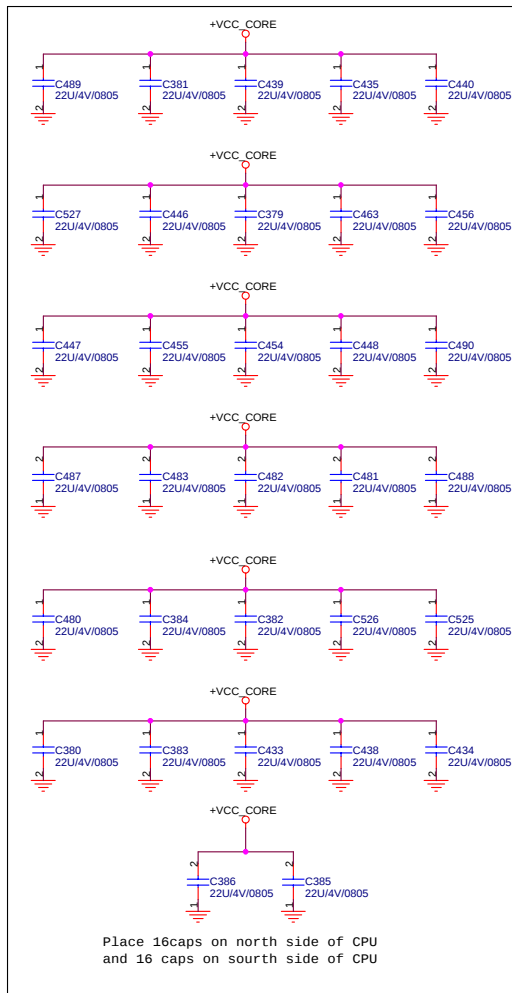


INDEX		
Pg#	Description	DNI LIST
1	Schematic Block Diagram 1	
2	Blank Page	
3	Front Page	
4-5	Dothan	
6-10	Alviso	
11-13	ICH6	
14-15	DDRII SO-DIMM(200P)	
16	Clock Generator	
17	CH7306/7	
18-19	Blank Pages	
20	LCD Conn. & SSP	
21	CRT & TV Conn.	
22	SATA & IDE Conn.	
23	Screw Hole	
24	TI PIC6515	
25	Mini PCI Conn.	
26	MDC Conn.	
27-28	SIO (LPC47N354)	
29	SERIAL PORT & USB	
30	PARALLEL CONN.	
31	Flash ROM	
32	TOUCH PAD & BLUE TOOTH	
33	Switch Board Conn. & LED	
34	FAN & Thermal	
35-36	Audio CODEC (STAC9751) & Phone Jack	
37-38	LOM (BCM5751), Switch	
39	FIR	
40-41	Docking Conn. & Q-Switch	
42	Power Good	
43-44	Battery Selector & Charger	
45	CPU Power	
46	1.8V,0.9V,1.5V,1.05V	
47	3VALW/5V/3V/Power ON	
48	RUN Power Switch	
49	VGA DC/DC	
50	DCIN/Batt Conn.	

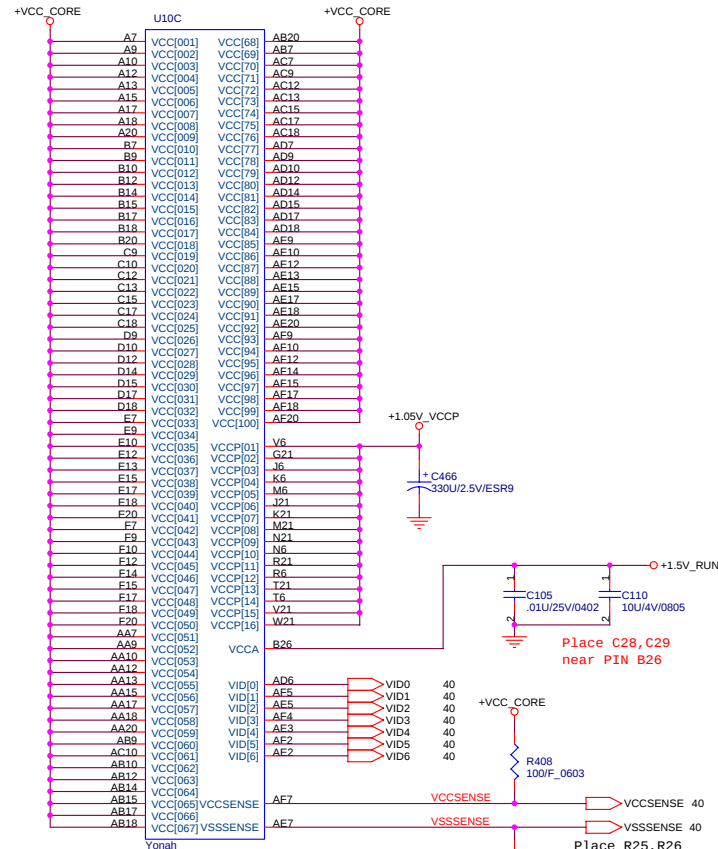
Power & Ground			
Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (20V)	
PBATT+		MAIN BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~20V)	
RTC_PWR3_3V		RTC & PCL POWER (3_3V)	
+12V		+12V	DRUNPWROK
VHCORE		CPU CORE POWER (1.25/1.15V)	RUNPWROK
V1_2RUN		AGTL+ POWER (1.2V)	RUNPWROK
+3VRUN		SLP_S3# CTRLD POWER	RUN_ON
+3VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VALW		8051 POWER (5V)	
+5VRUN		SLP_S3# CTRLD POWER	RUN_ON
+5VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VHDD		HDD POWER (5V)	HDDC_EN#
+5VMOD		MODULE POWER (5V)	MODC_EN#
STRB#/5V		EXTERNAL FDD POWER (5V)	FDD/LPT#
+5VFAN1, +5VFAN2		FAN POWER (5V)	FAN_OFF/ON#
VDDA		AUDIO ANALOG POWER (5V)	RUN_ON
1_8VSUS		RESUME WELL IN ICH	
1_8VRUN		SLP_S3# CTRLD POWER	
+3VALW		8051 POWER (3V)	
V1_5RUN		AGP I/O POWER	
 GND	ALL PAGES	DIGITAL GROUND	
 GNDP		CPU POWER GND	
 CGNDP		CHARGER GND	
 DGNDP		DC/DC POWER GND	
 LANGND		COMBO CONN GND	

02

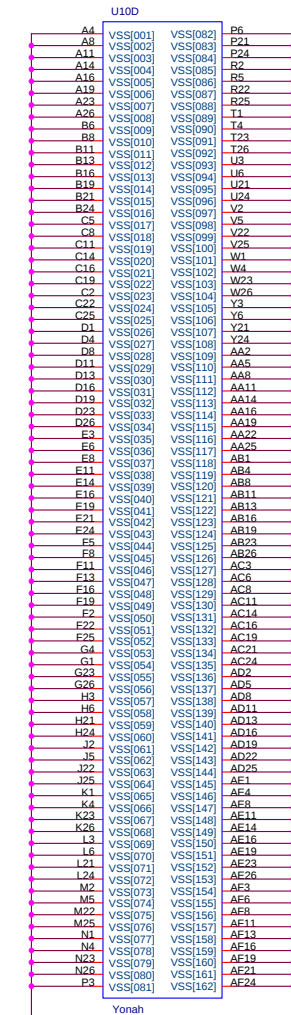
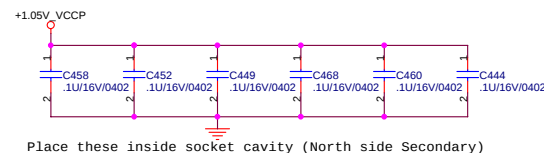




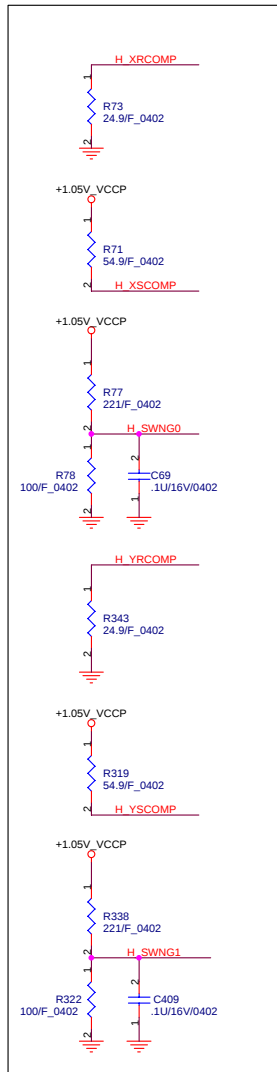
Total caps = 2684 uF
ESR = 6m ohm/4 // 3m ohm/32



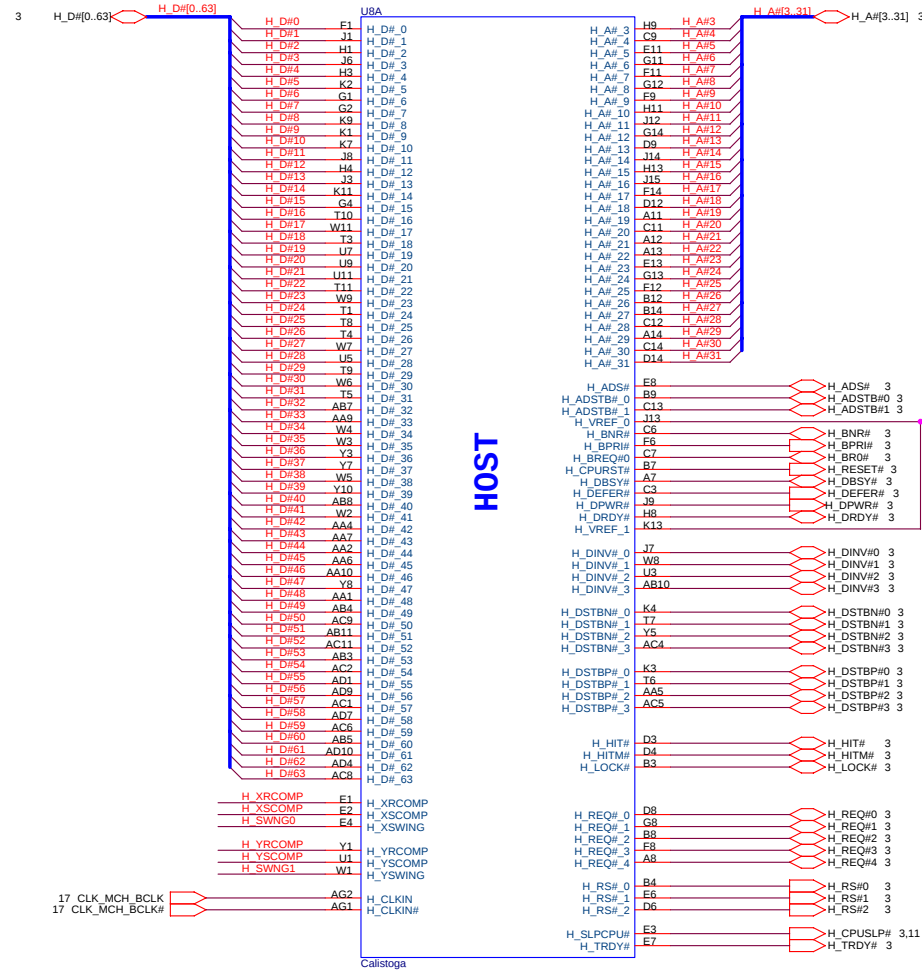
Route VCCSENSE and VSSSENSE
traces at 27.4ohms with 10mil
spacing and for other signals
keep out spacing 25mil.
length match within 25mil.
Place PU and PD within 2 inch
of CPU.

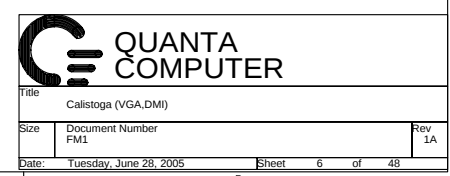


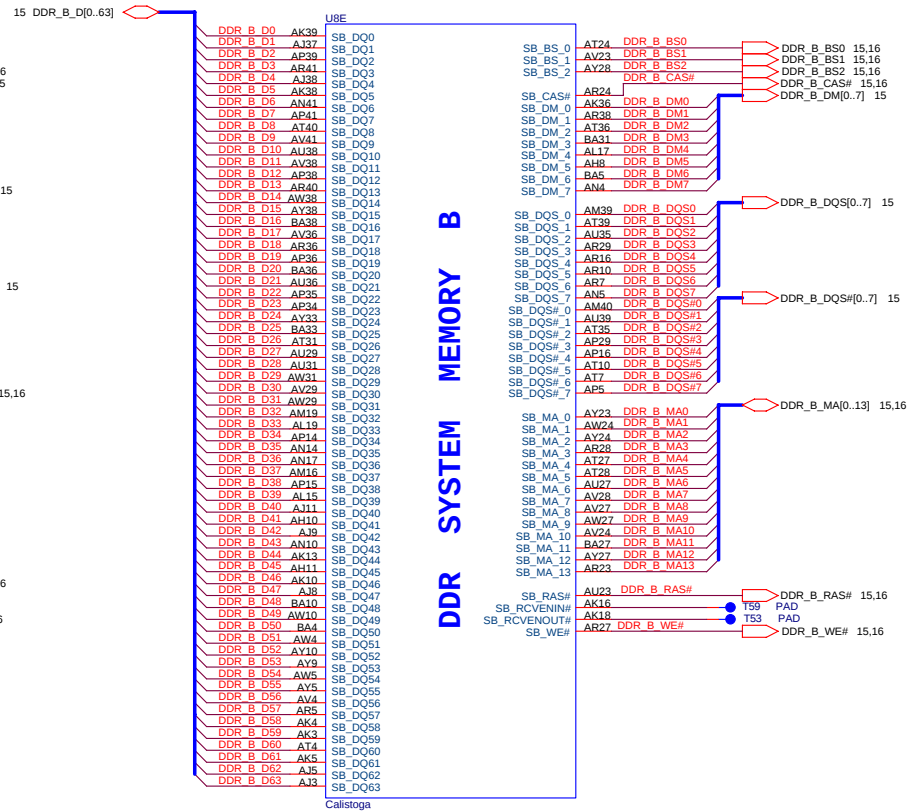
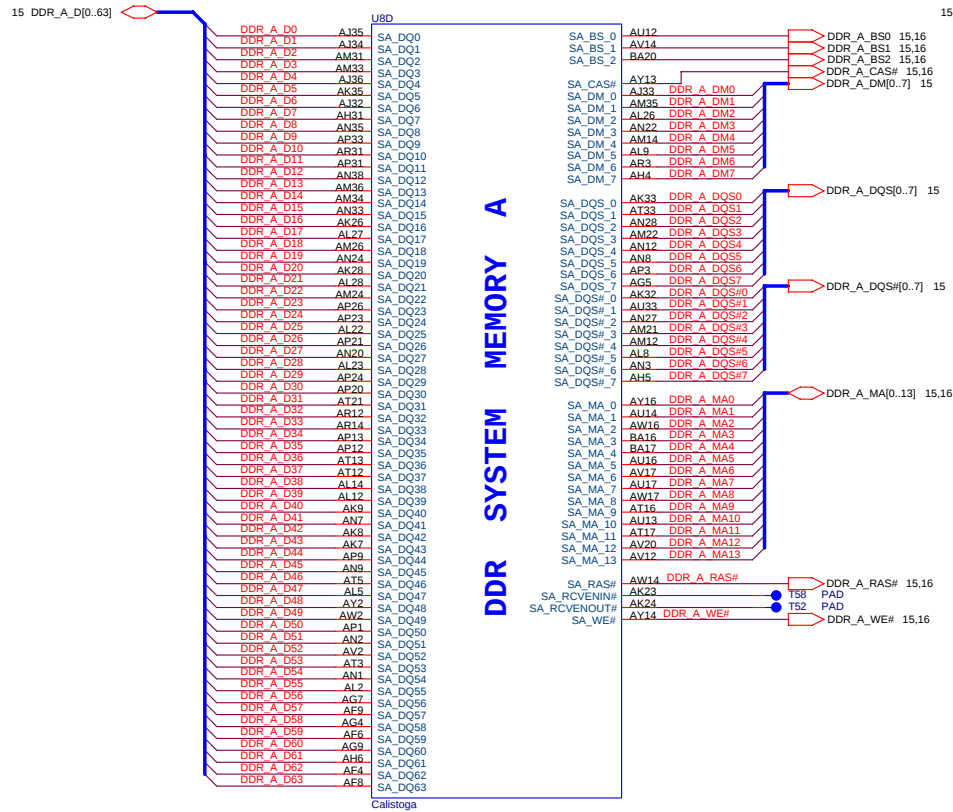
Title			Yonah Processor (POWER)	
Size	Document Number	Rev		1A
	FM1			
Date:	Tuesday, June 28, 2005	Sheet	4	of 48

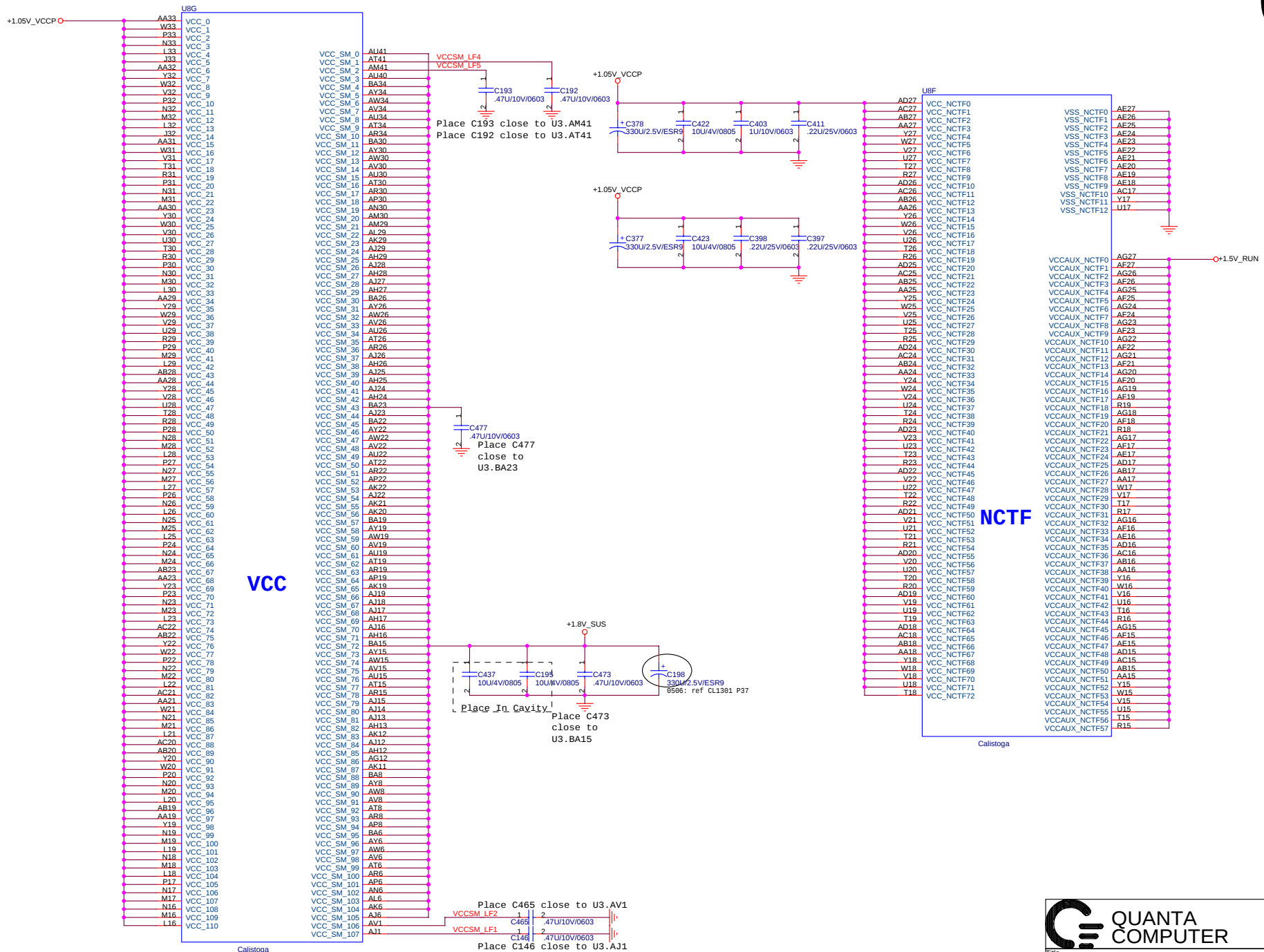


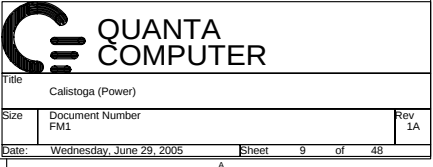
H_XRCOMP, H_XSCOMP, H_YRCOMP, H_YSCOMP,
H_SWNG0, H_SWNG1 used W:10/S:20 mil.
R & C of HXRCOMP, HXSCOMP, HYRCOMP, HYSCOMP,
H_SWNG0, H_SWNG1 trace length less 0.5" from U3

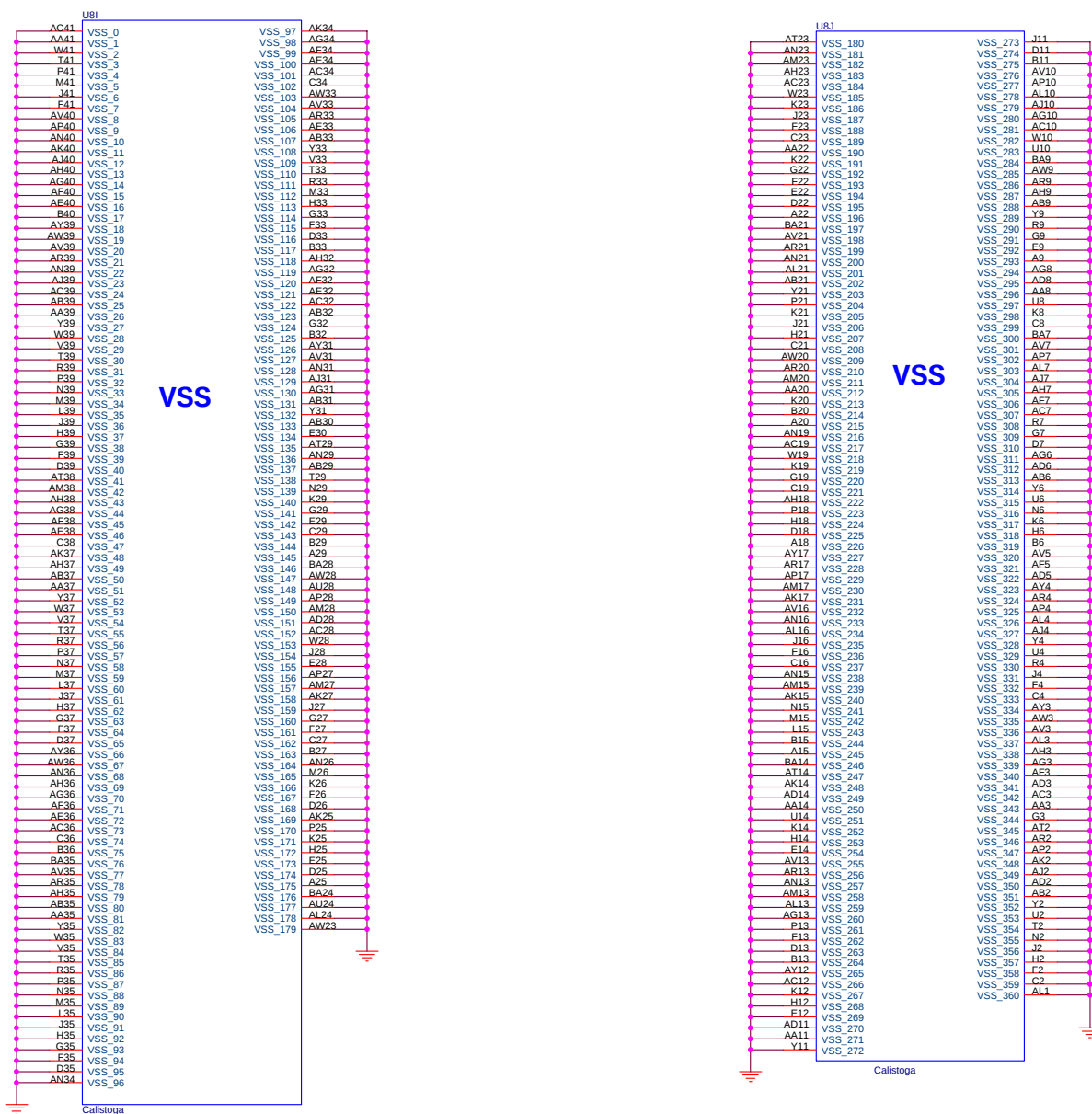




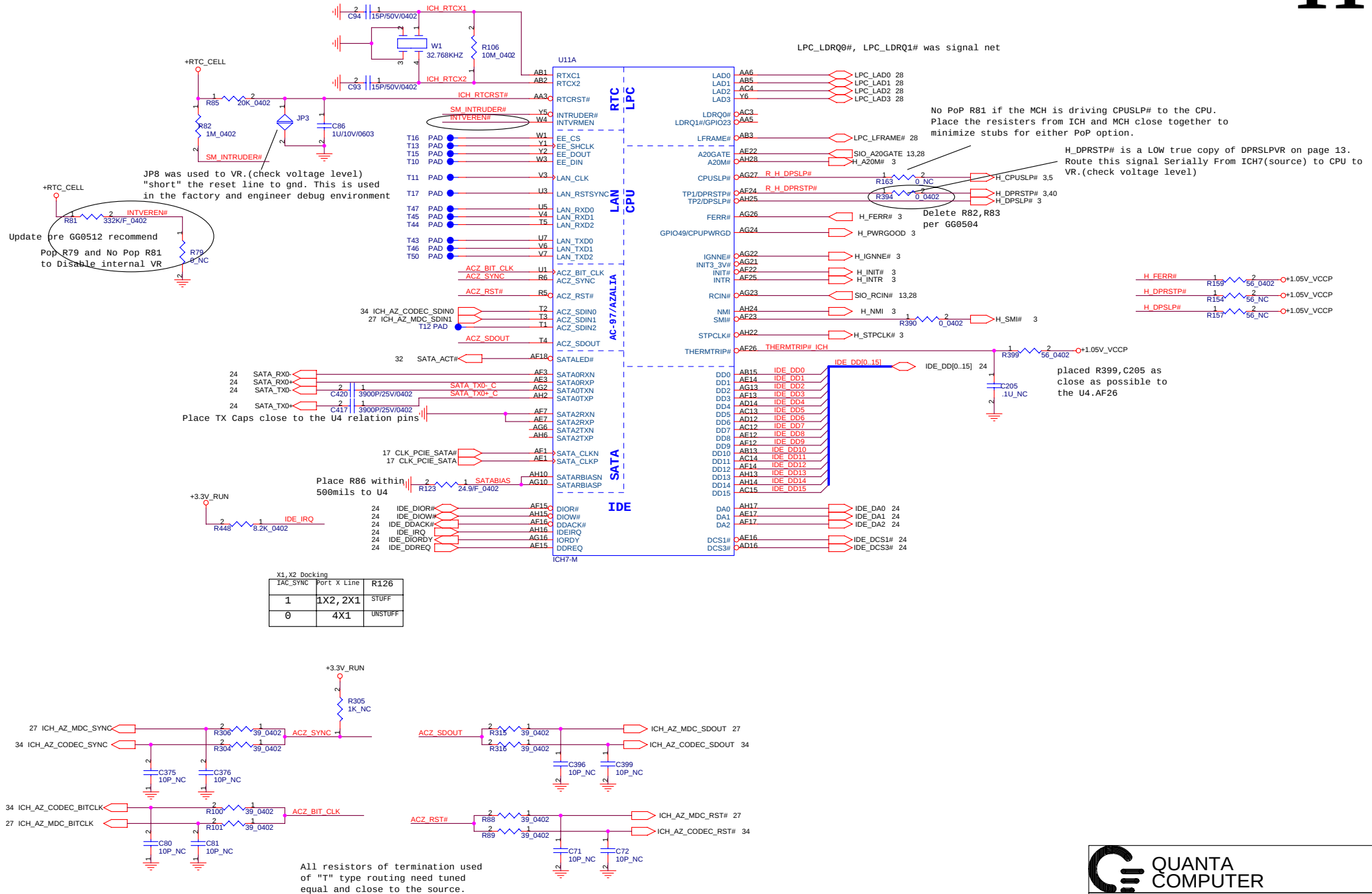


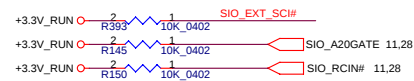
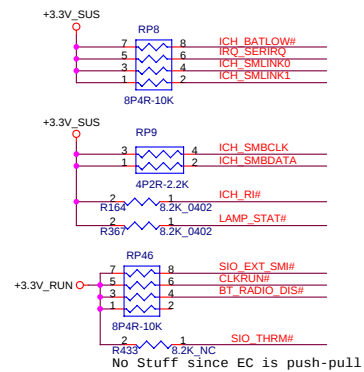
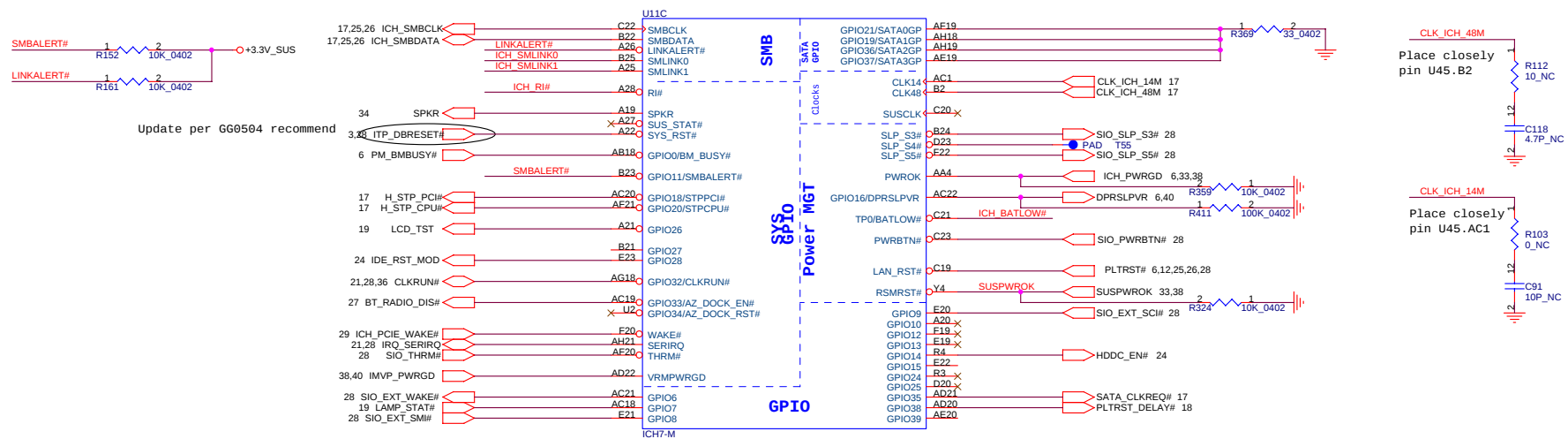


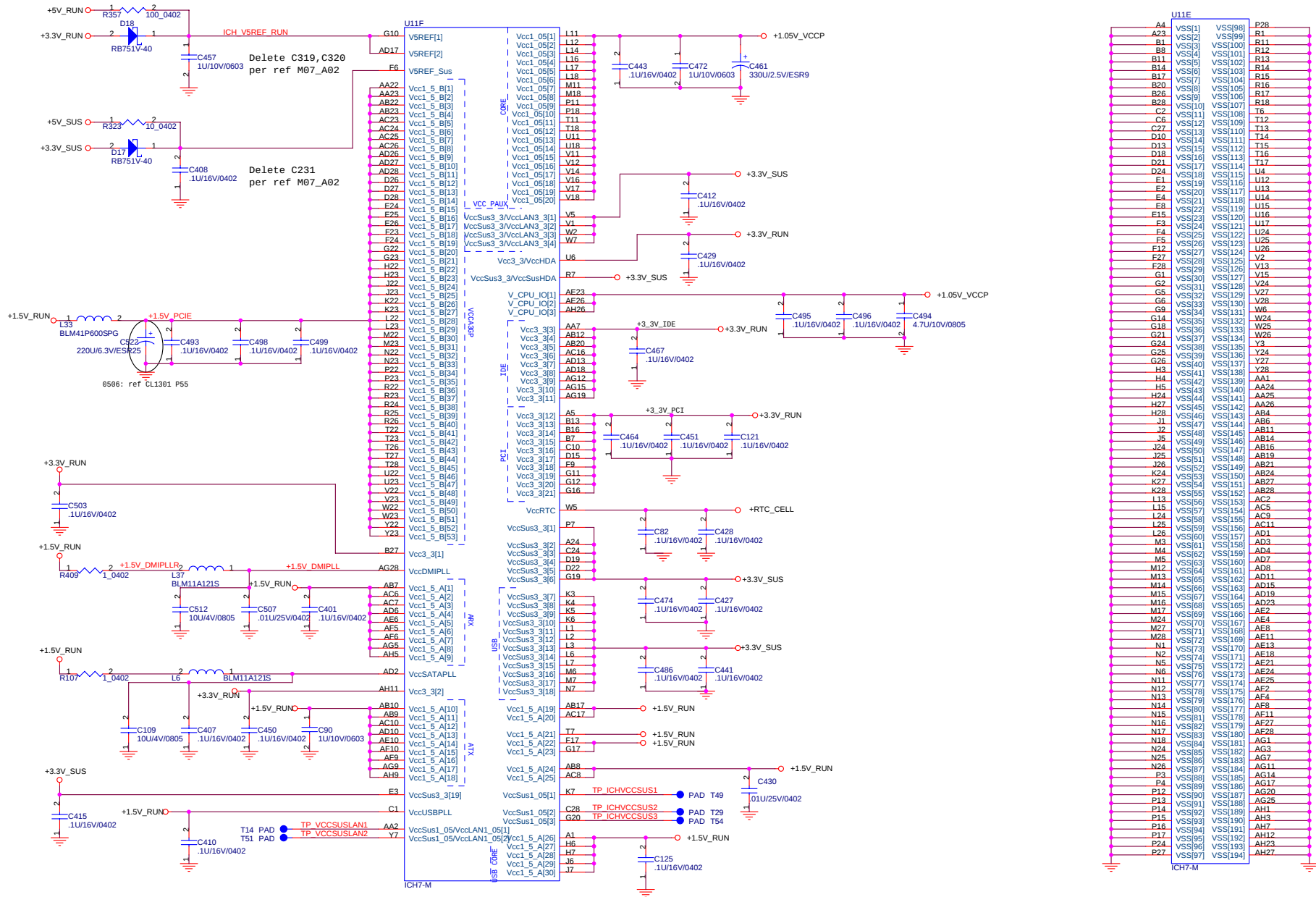


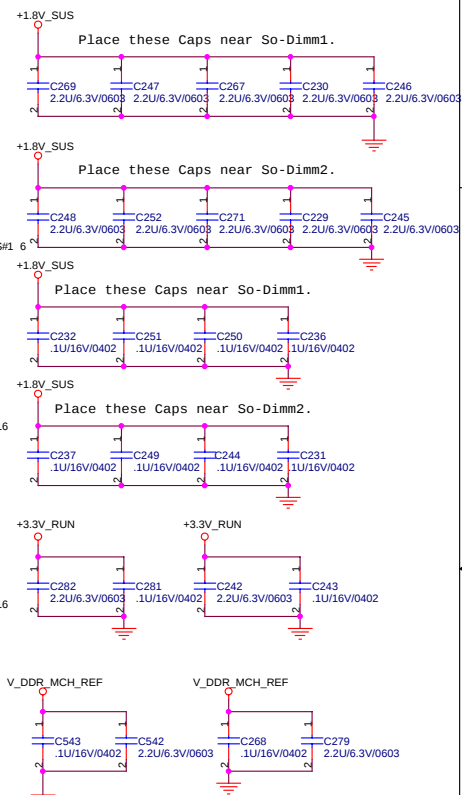
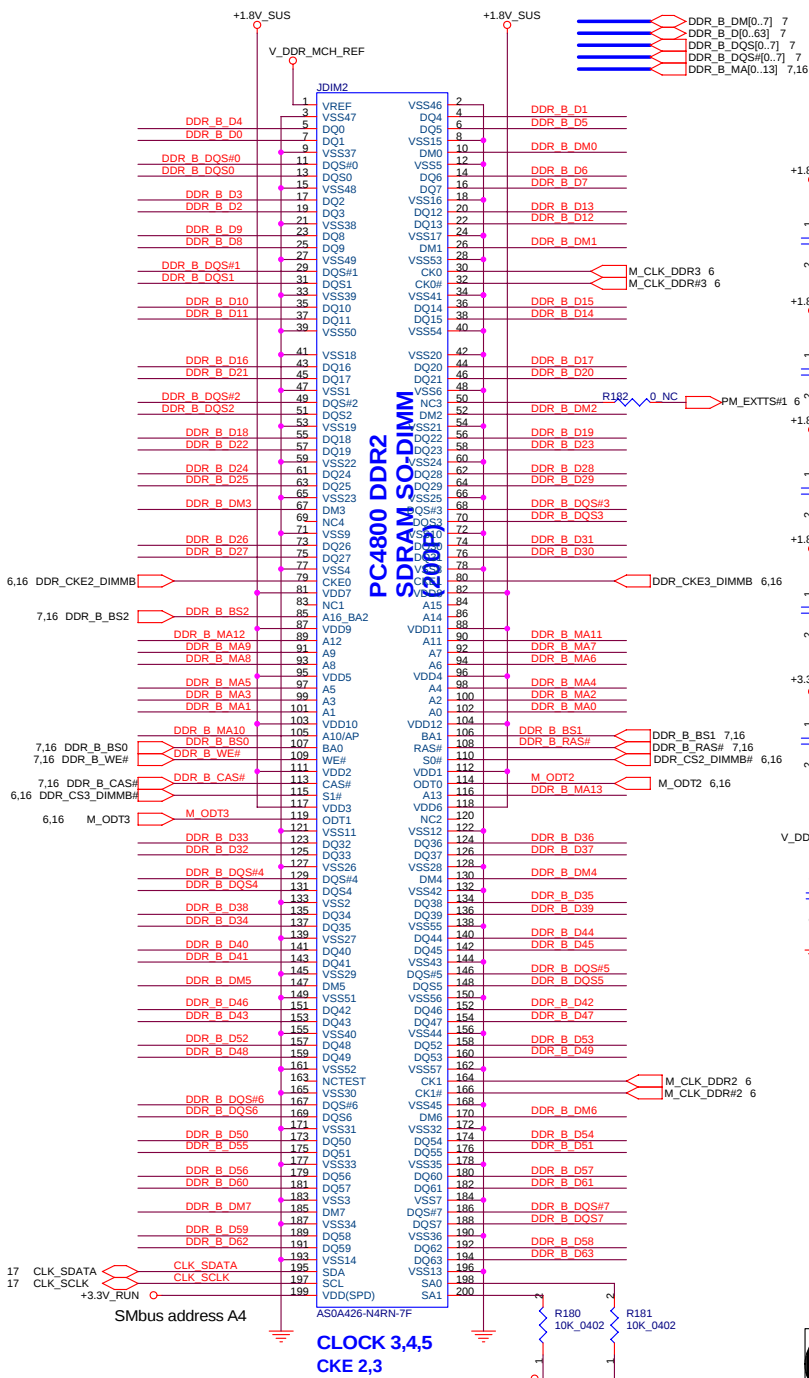
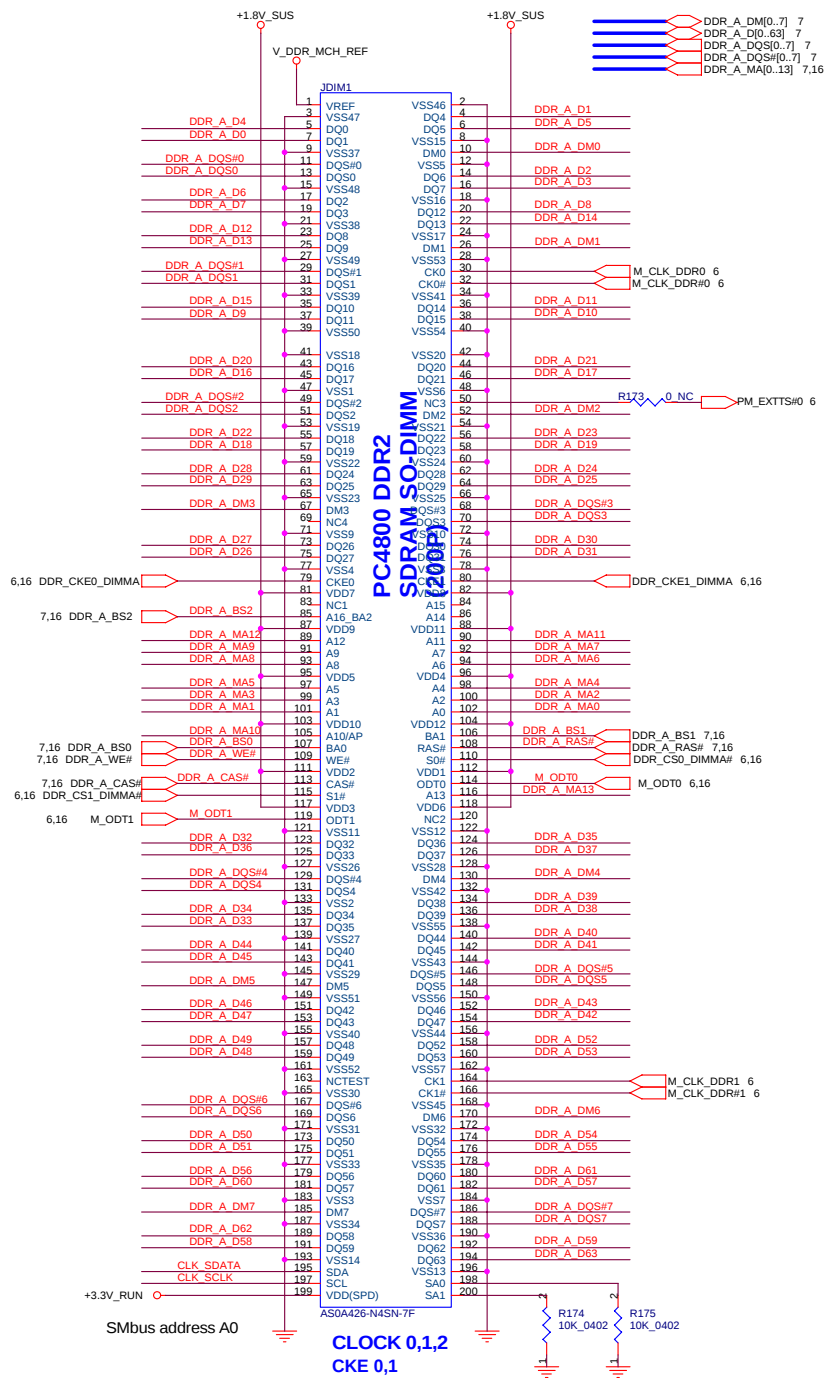


Title			
Calistoga (VSS,NCTF)			
Size	Document Number FM1		Rev 1A
Date:	Tuesday, June 28, 2005	Sheet 10 of 48	





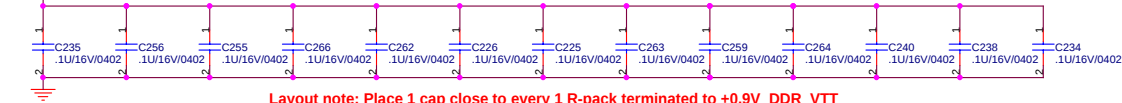




DDR_A_MA[0..13] 7,15

DDR_B_MA[0..13] 7,15

+0.9V_DDR_VTT



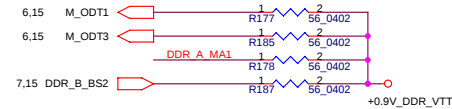
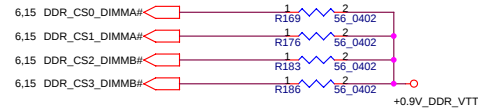
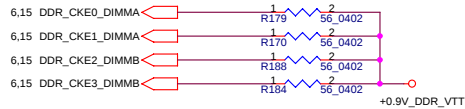
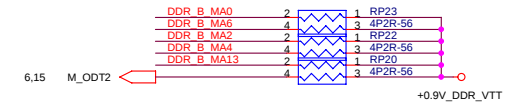
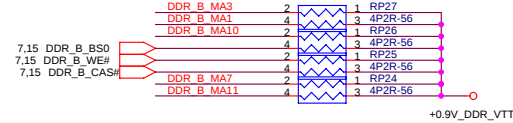
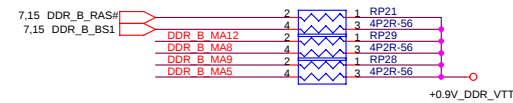
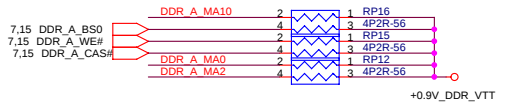
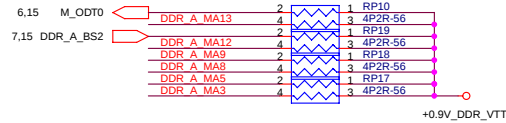
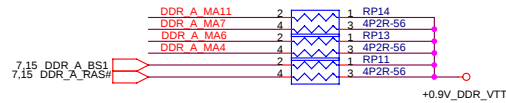
Layout note: Place 1 cap close to every 1 R-pack terminated to +0.9V_DDR_VTT

+0.9V_DDR_VTT



Layout note: Place 1 cap close to every 1 R-pack terminated to +0.9V_DDR_VTT

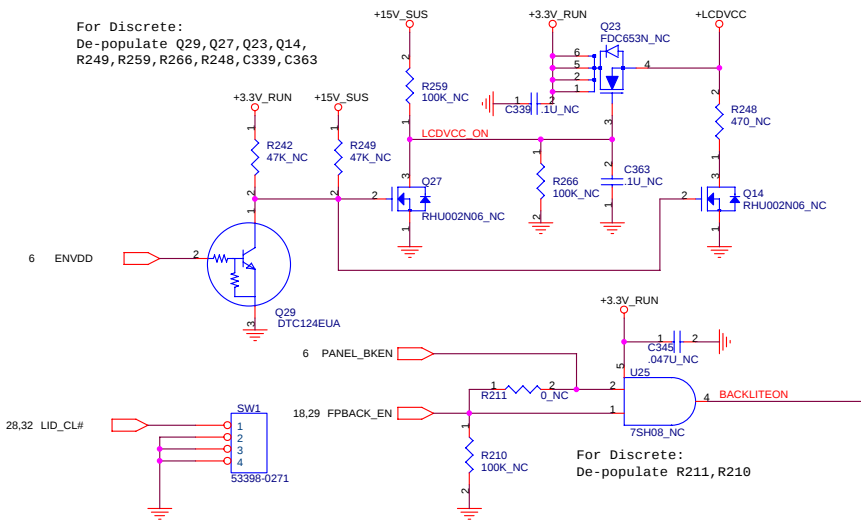
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT



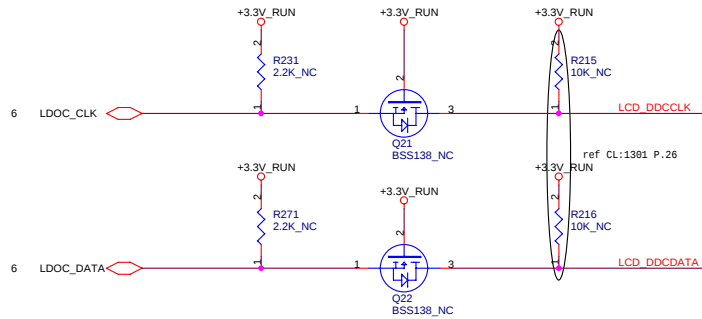
Title	DDR RES.ARRAY		
Size	Document Number	Rev	
	FM1	1A	
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For Discrete:
De-populate Q29, Q27, Q23, Q14,
R249, R259, R266, R248, C339, C363

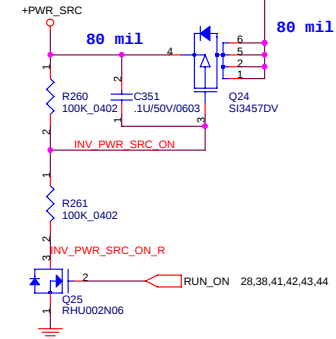
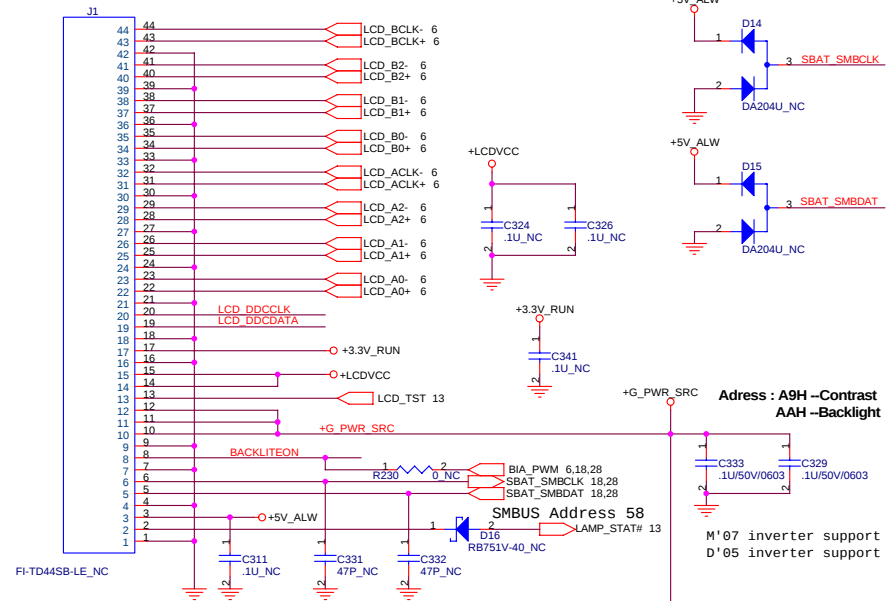


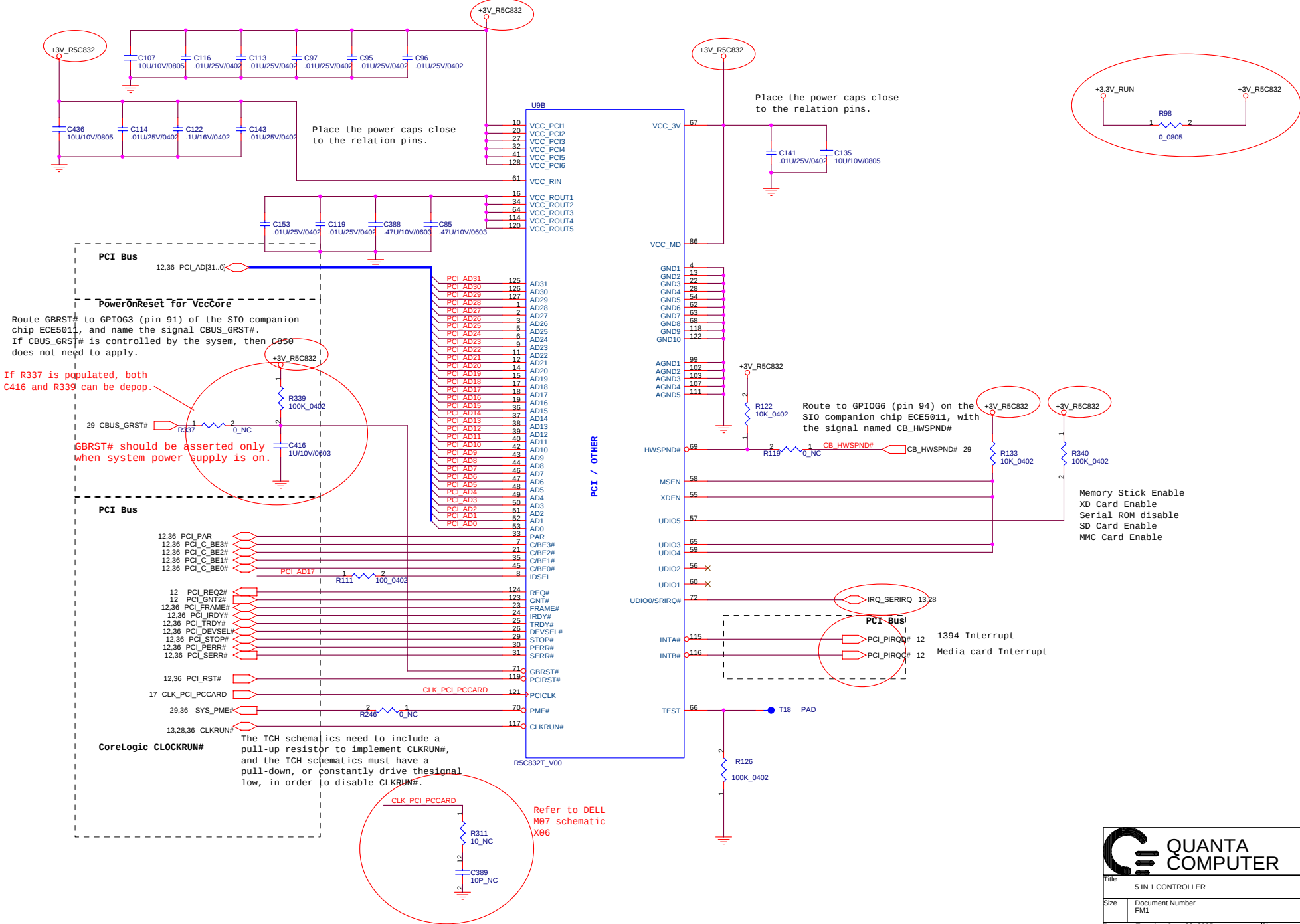
Support M07-Inverter: Populate R230, R211 and Depopulate U8, C345.
Support D05-Inverter: Depopulate R230, R211 and Populate U8, C345.

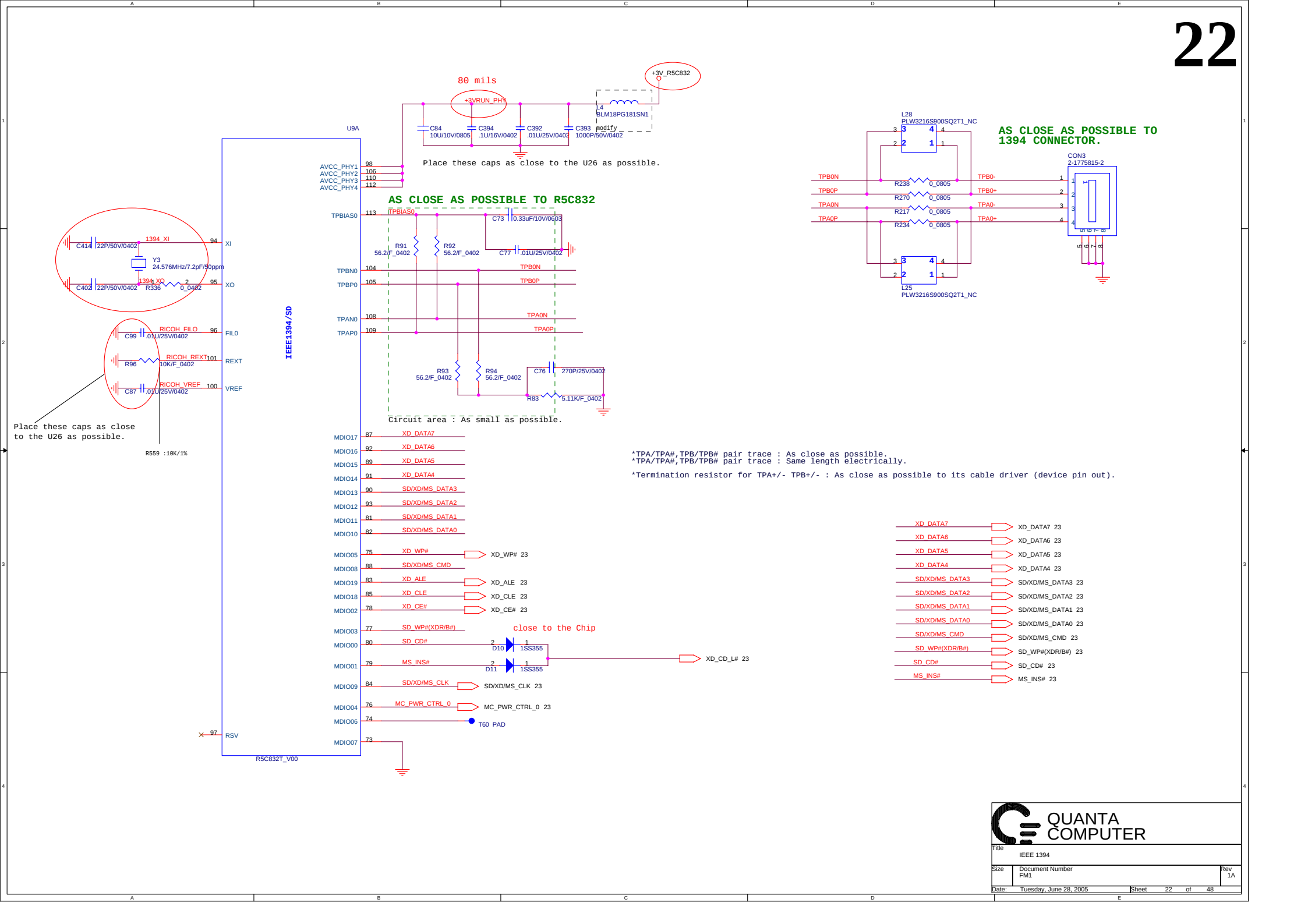


For Discrete:
Depopulate
R231, R271, R215, R216, Q21, Q22

For Discrete:
De-populate J1, R230, C311, C331, C332,
D16, C341, C324, C326

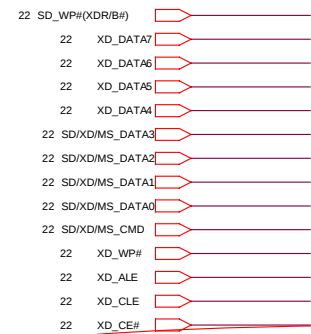
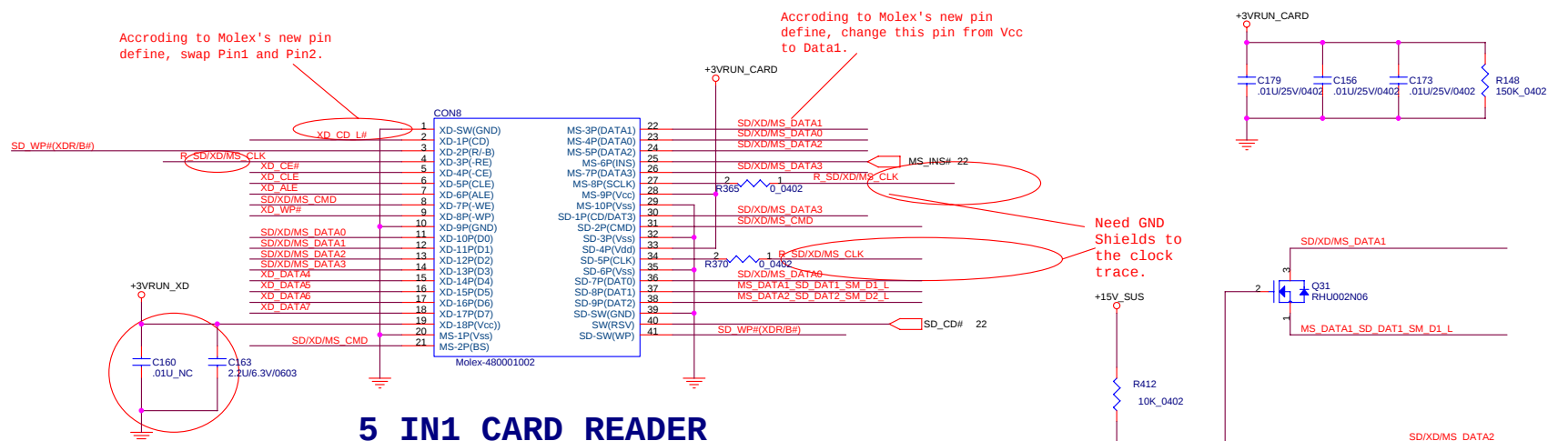






DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

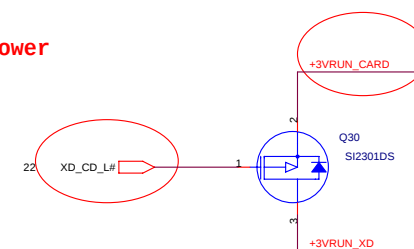
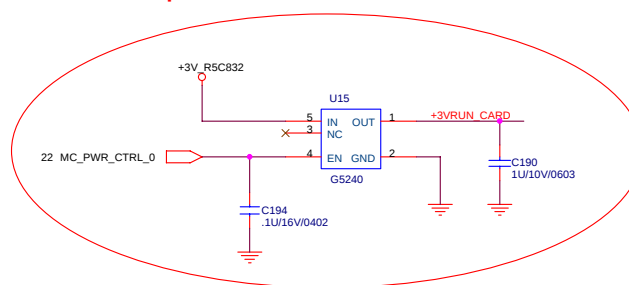
23

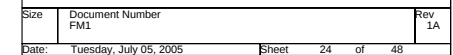


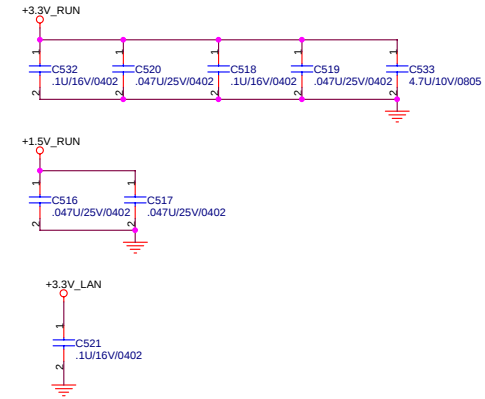
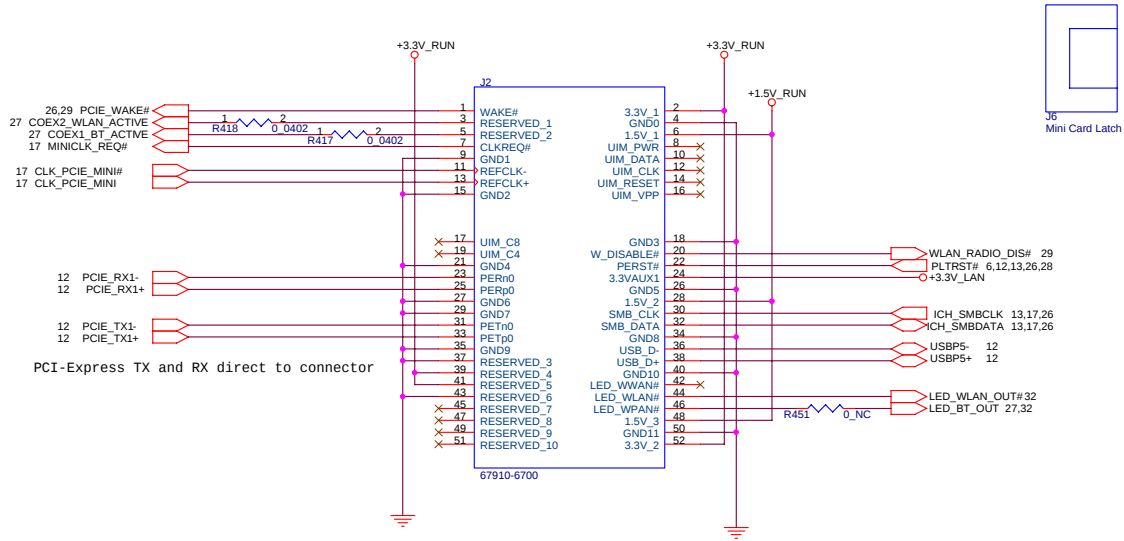
For SD/MS power

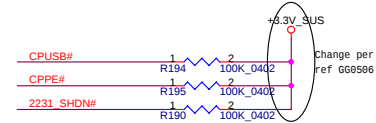
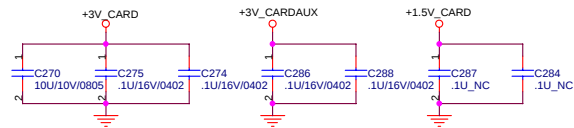
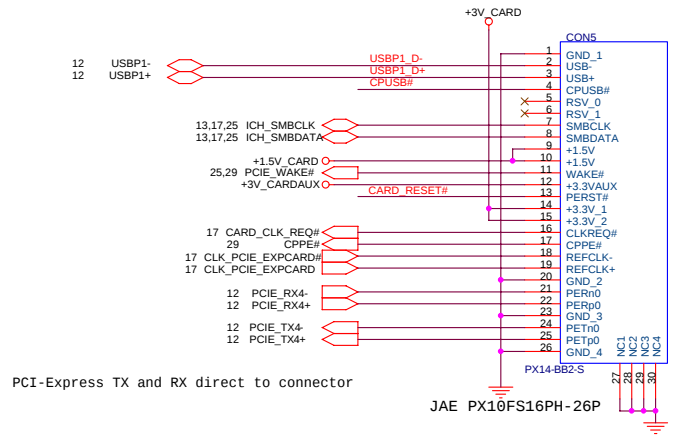
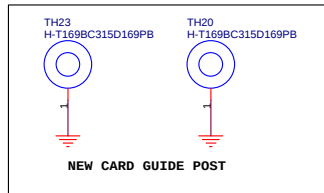
For XD power

Accroding to RICOH's suggestion, place this resistor at trident point of R_SD/XD/MS_CLK trace.

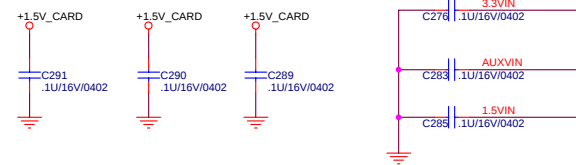
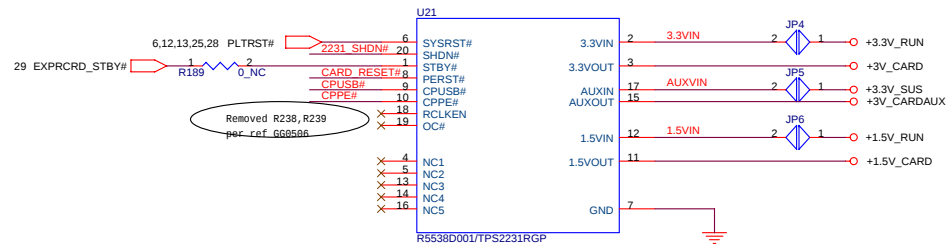






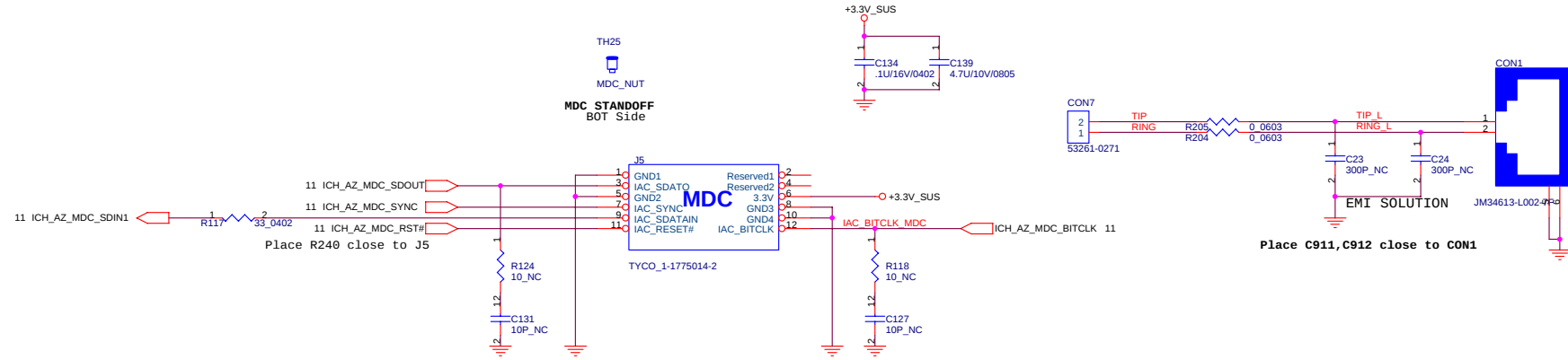


+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

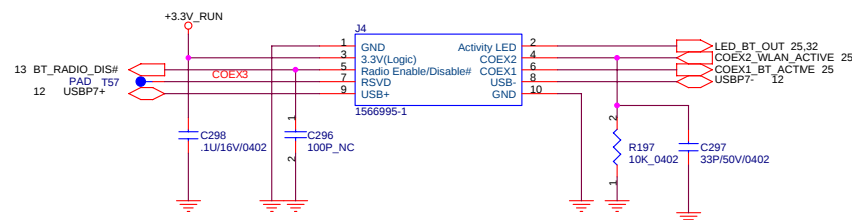


MDC Layout Notes

1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG
(stranded or twisted pair wire)



Bluetooth



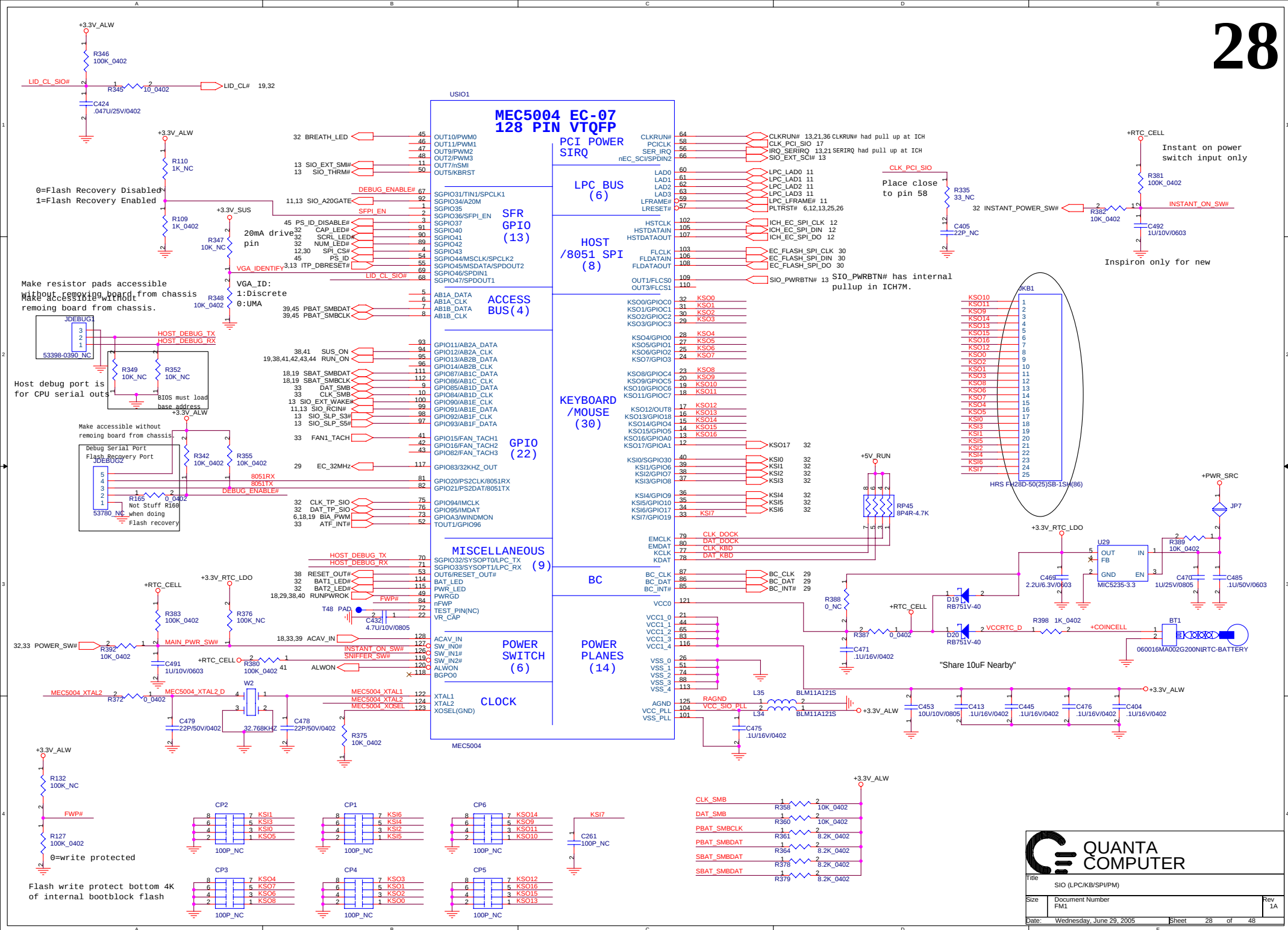
MDC CONN & BlueTooth.

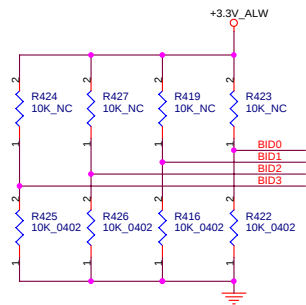
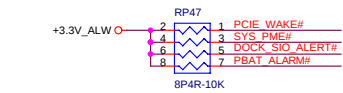
Size Document Number FM1

Date: Tuesday, June 28, 2005

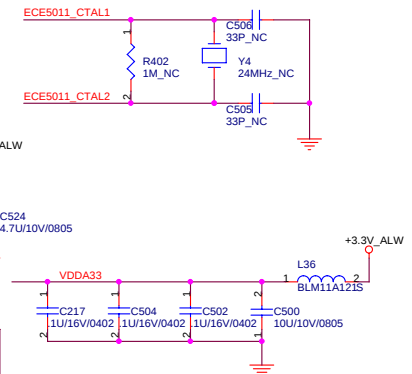
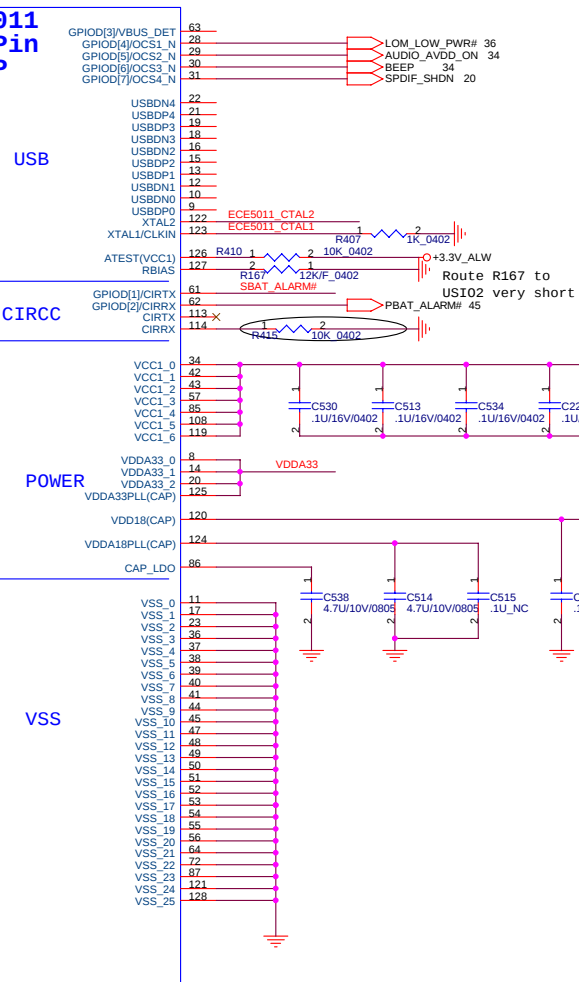
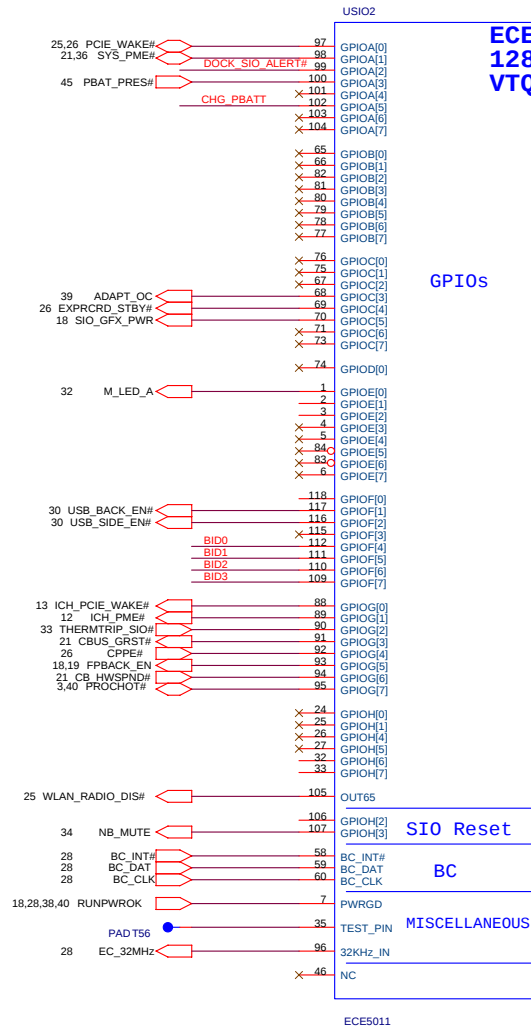
Sheet 27 of 48

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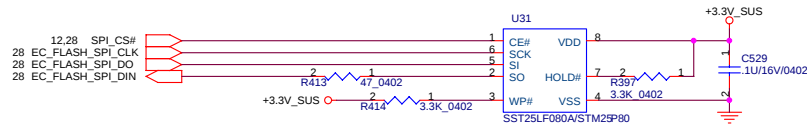


BID3	BID2	BID1	BID0	Board Revision
0	0	0	0	PROTO1 (X00)
0	0	0	1	PROTO2 (X01)
0	0	1	0	PROTO3 (X02)
0	0	1	1	QT(X03)
0	1	0	0	A00 FWB/A01 PWA

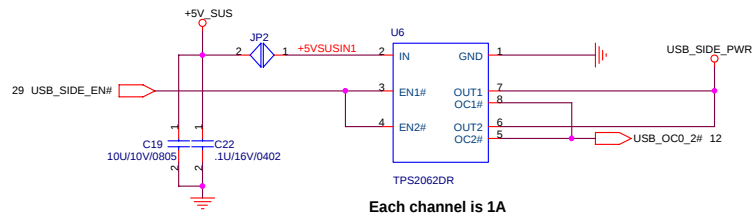


Title	SIO (GPIO/BC/USB/CIRR)
Size	Document Number FM1
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Sheet	29 of 48
Rev	1A

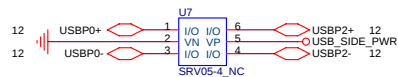
8Mbit (1M Byte), SPI



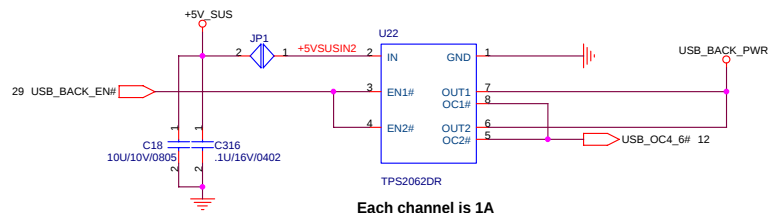
Delete UPW1, C434-436, RP53
per GG0524 item 135.



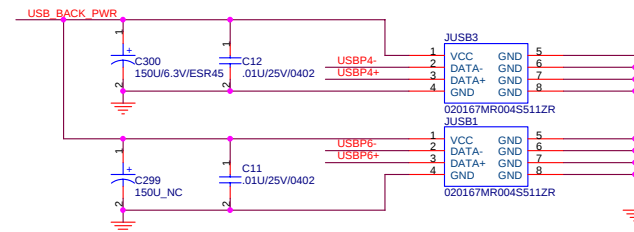
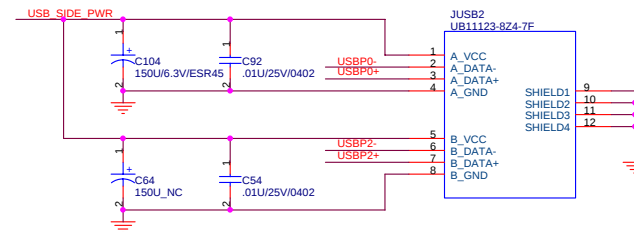
Each channel is 1A



Place ESD diodes as
close as USB connector.



Each channel is 1A



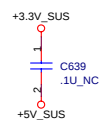
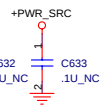
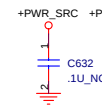
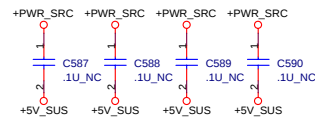
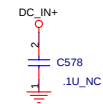
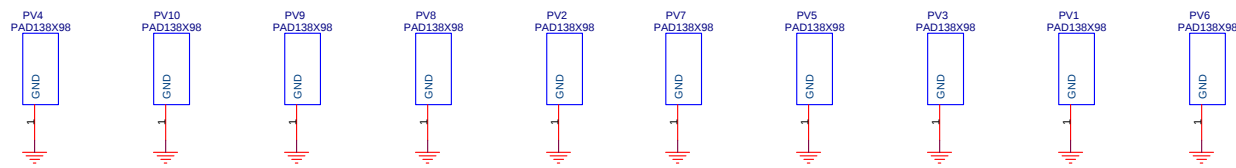
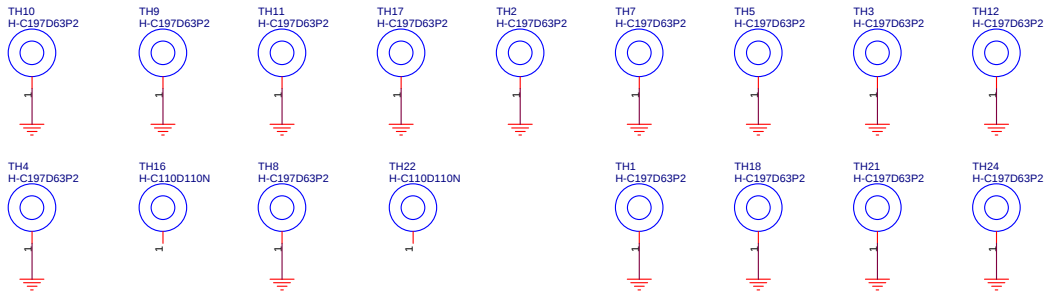
USB & Flash

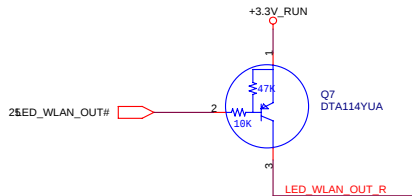
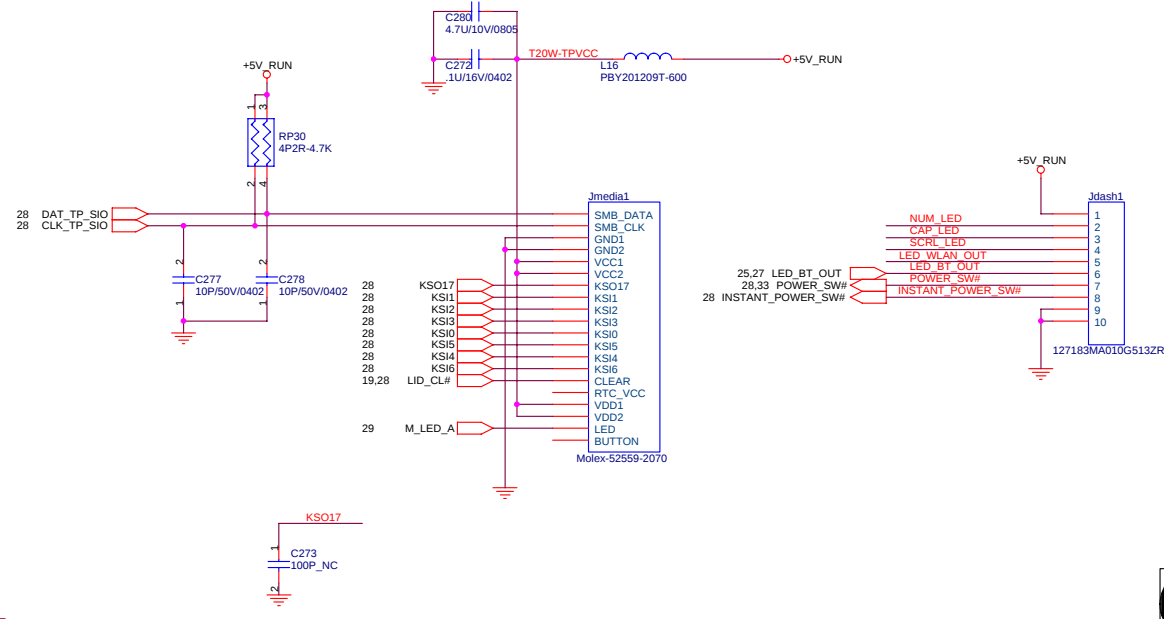
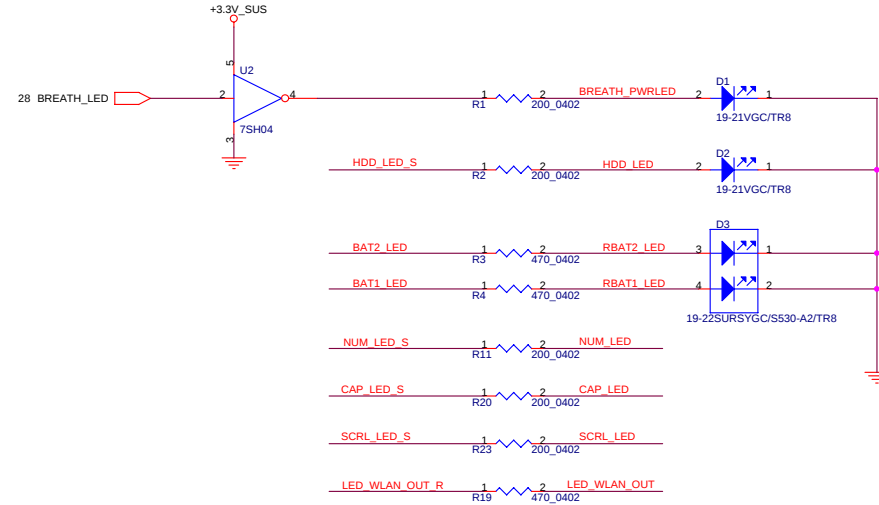
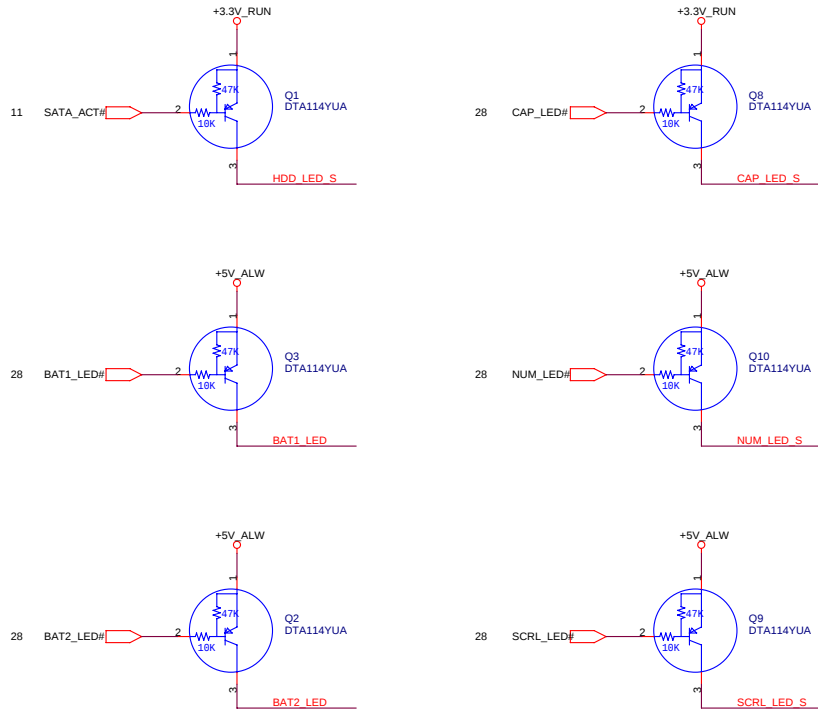
Size Document Number
FM1

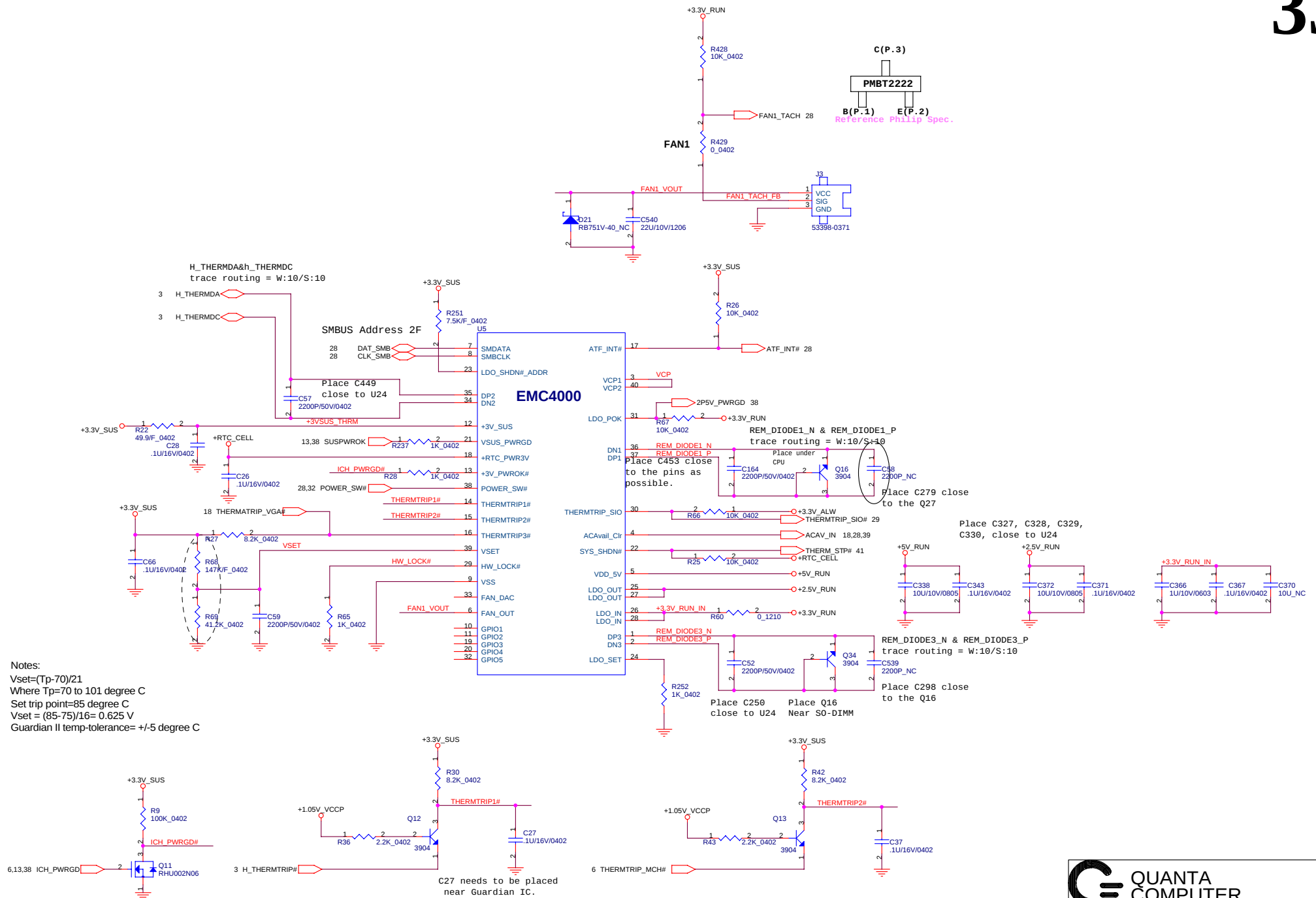
Date: Tuesday, June 28, 2005

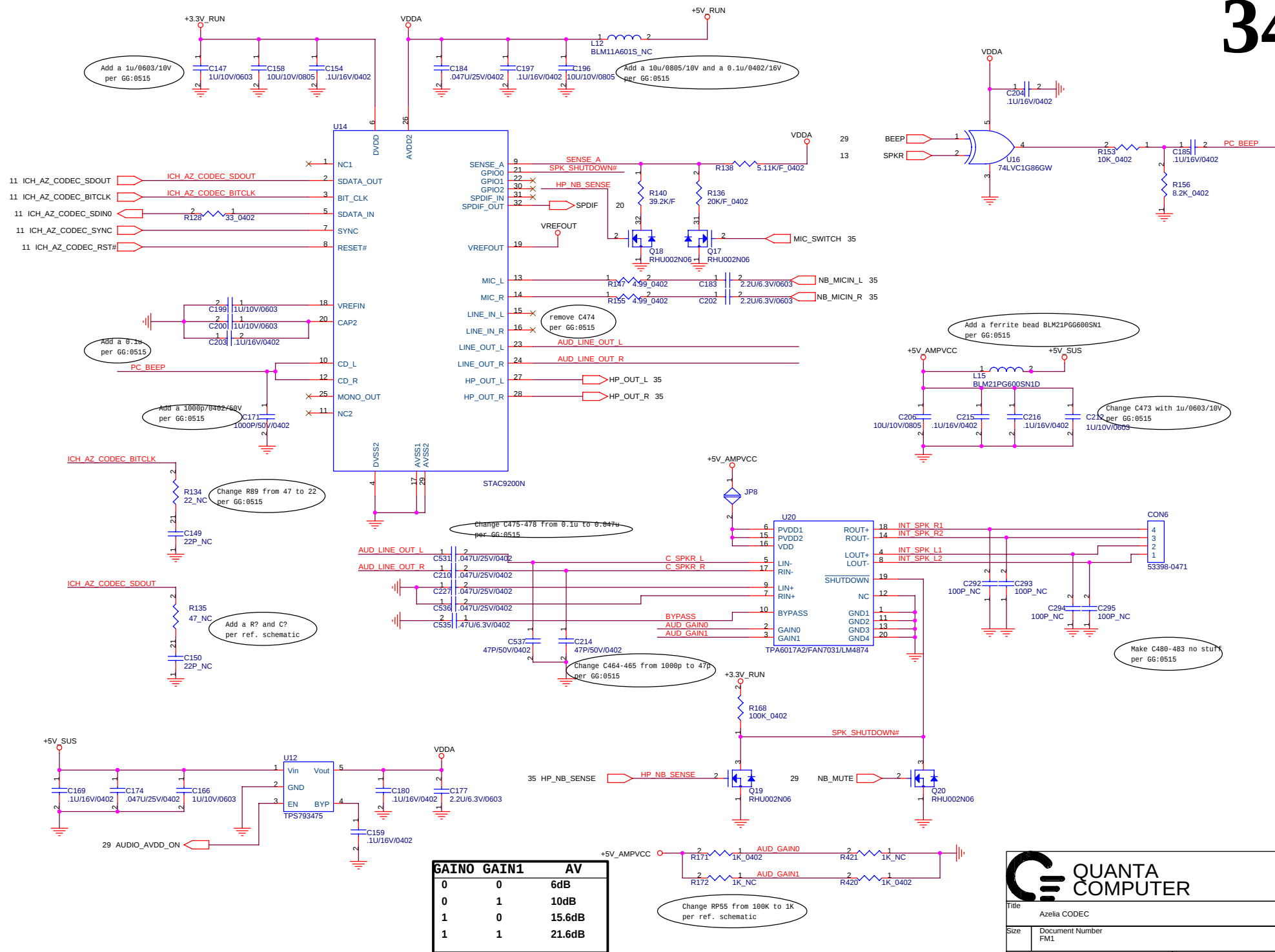
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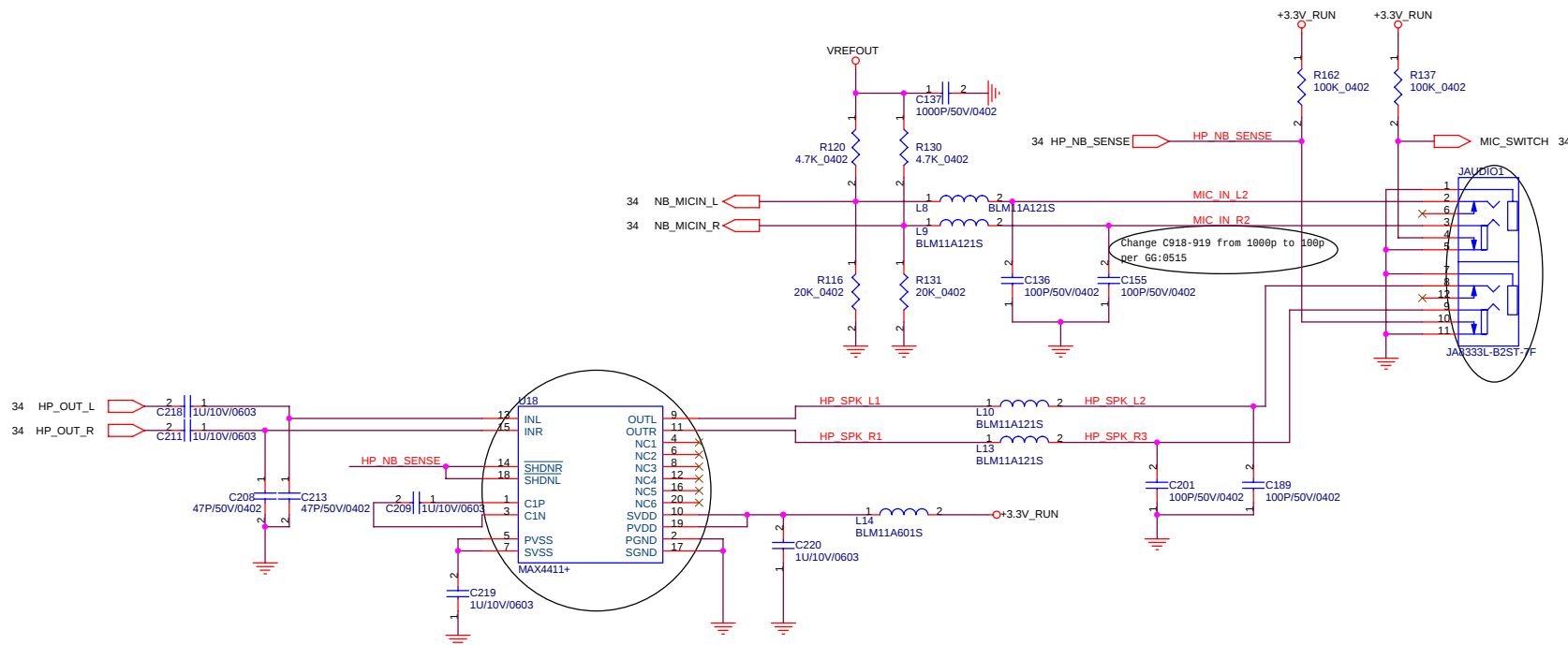
Rev
1A





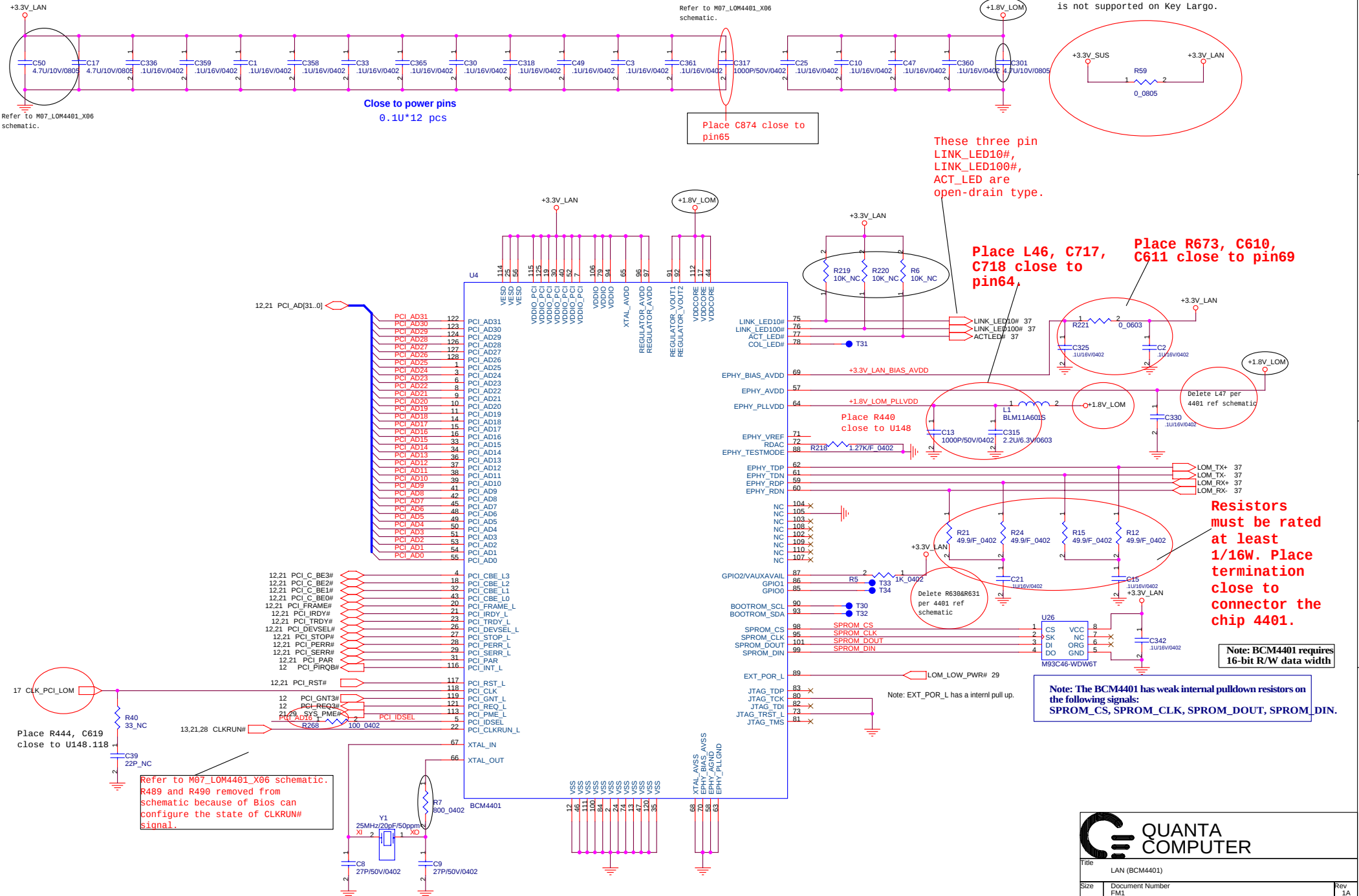


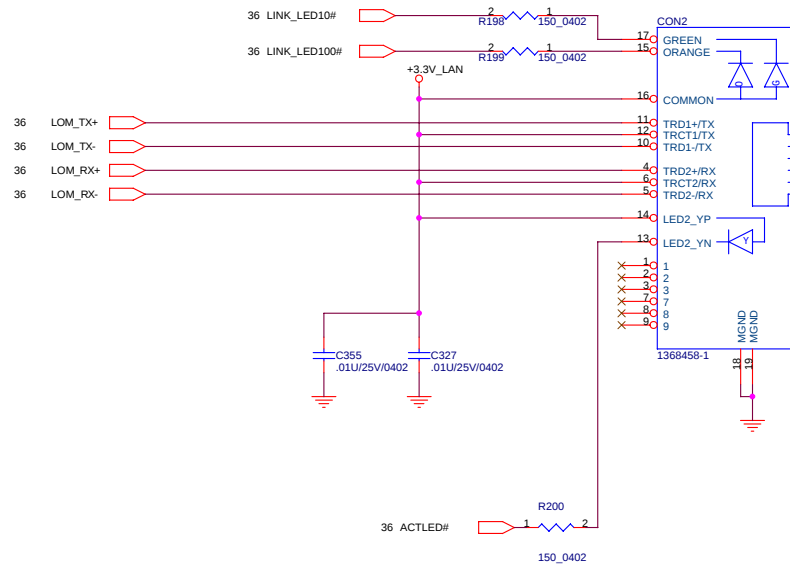


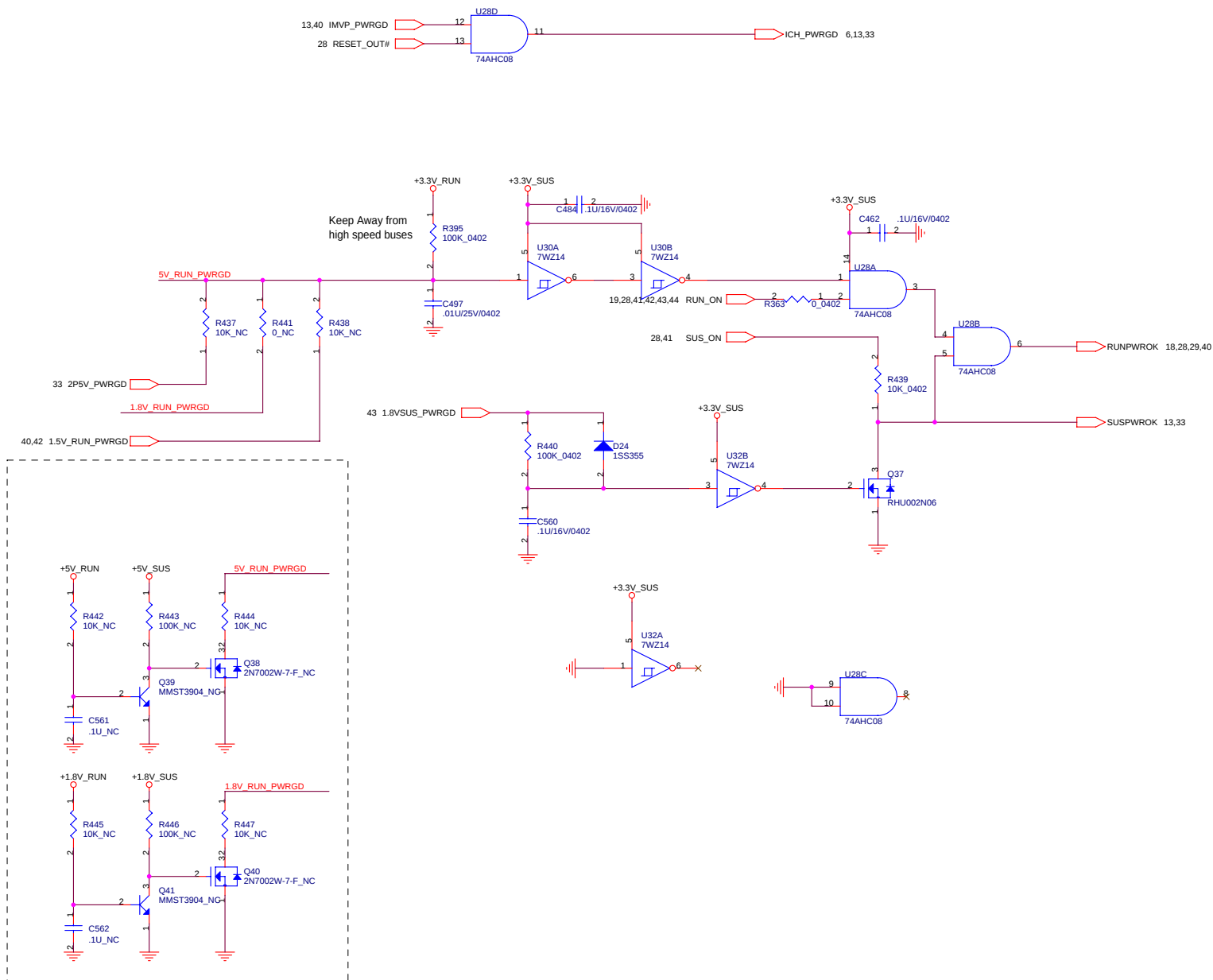


Title		AUDIO CONN	
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Refer to M07_L0M4401_X06 schematic.
'+3VLAN should be sourced from
+3VSUS instead of +3VSRG since WOL
is not supported on Key Largo.







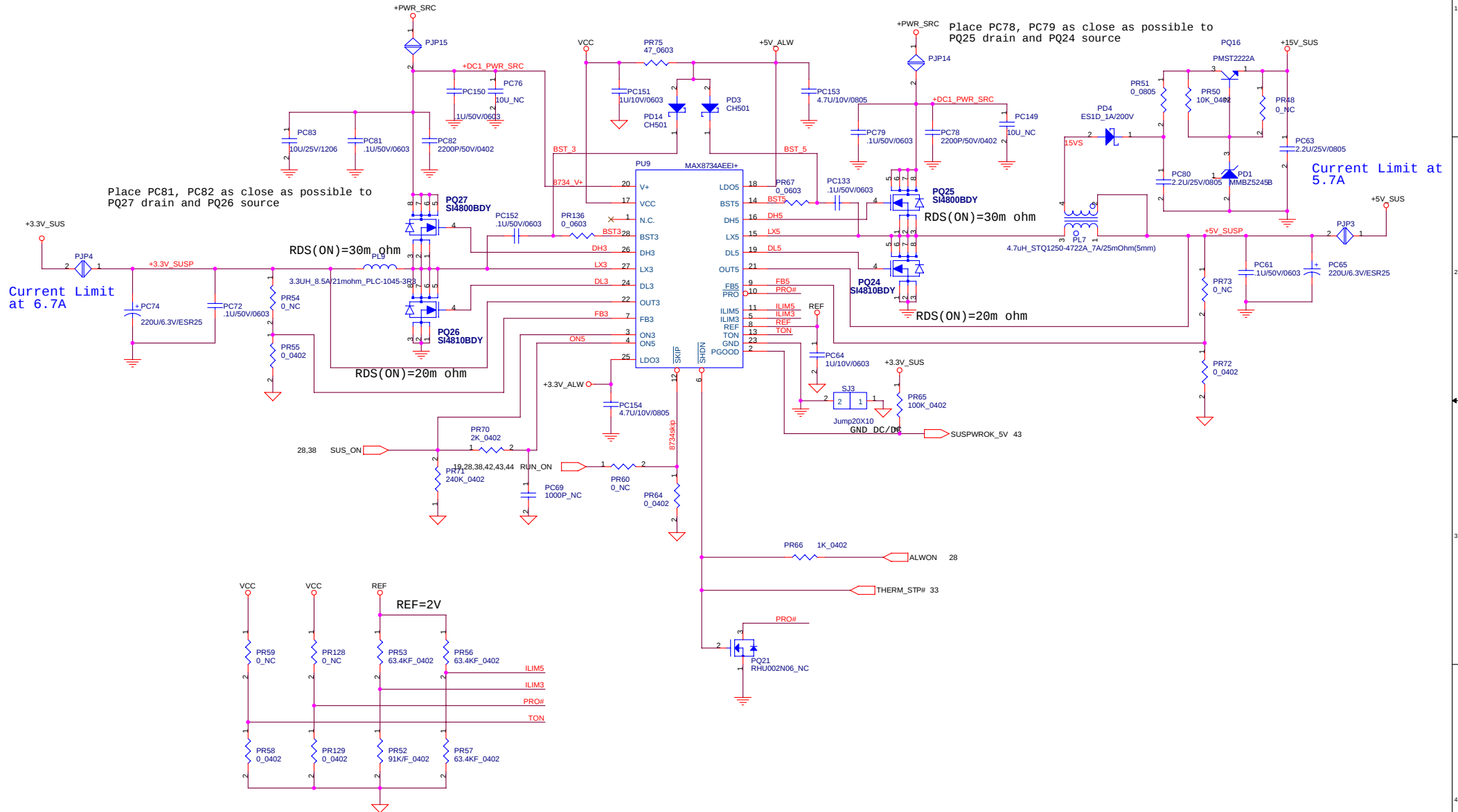
Title
System Reset Circuit

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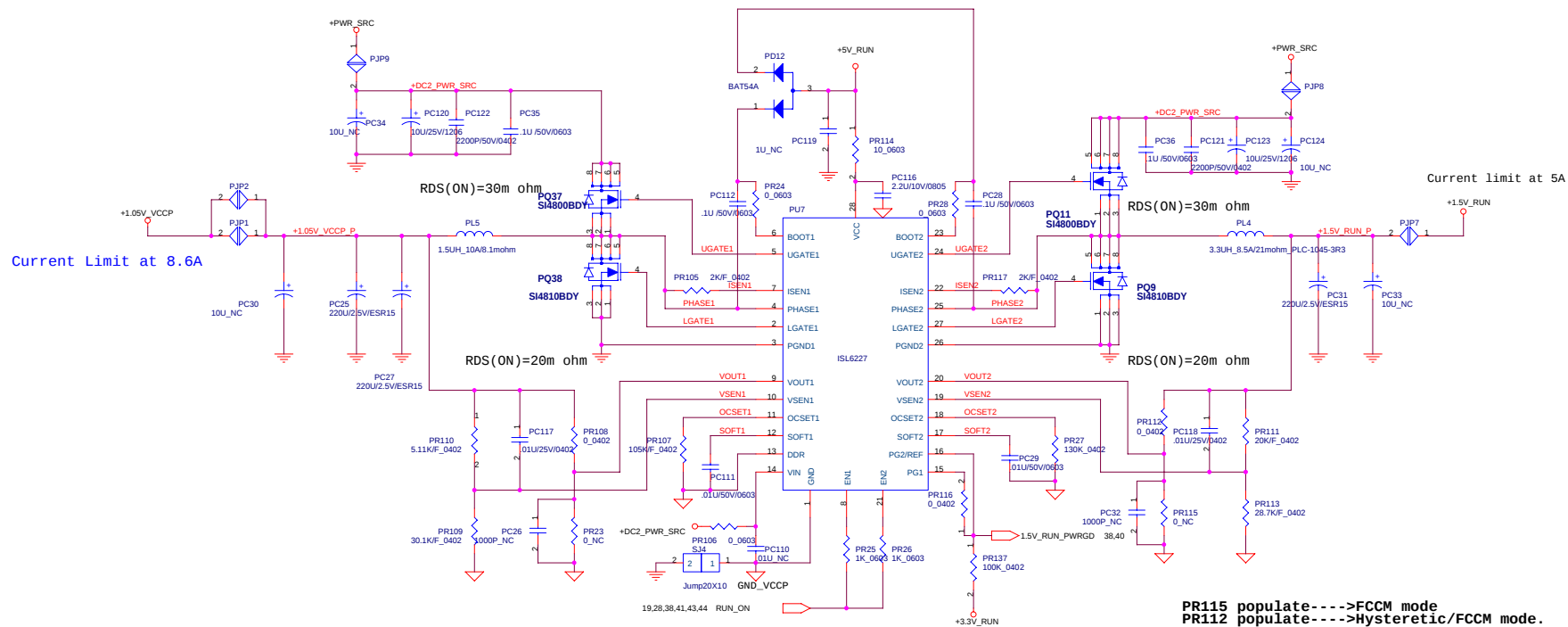
3VALW,5VALW,5V,3V

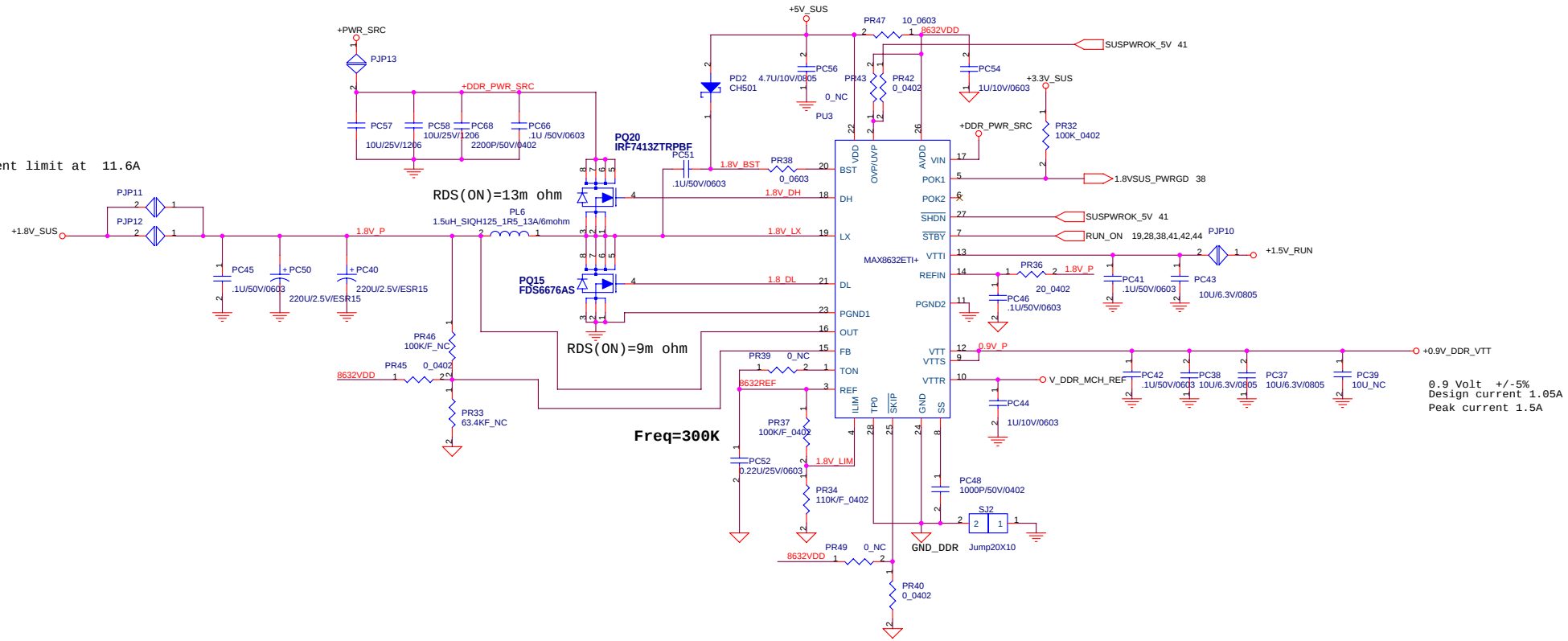
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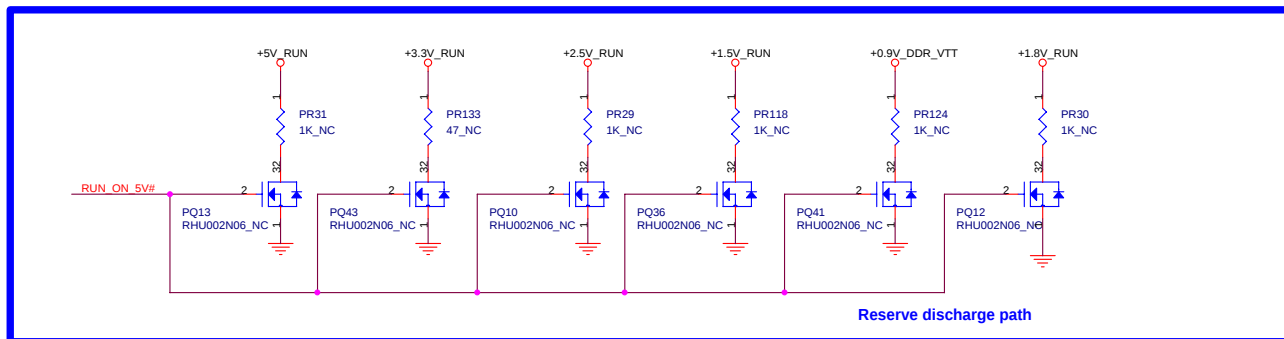
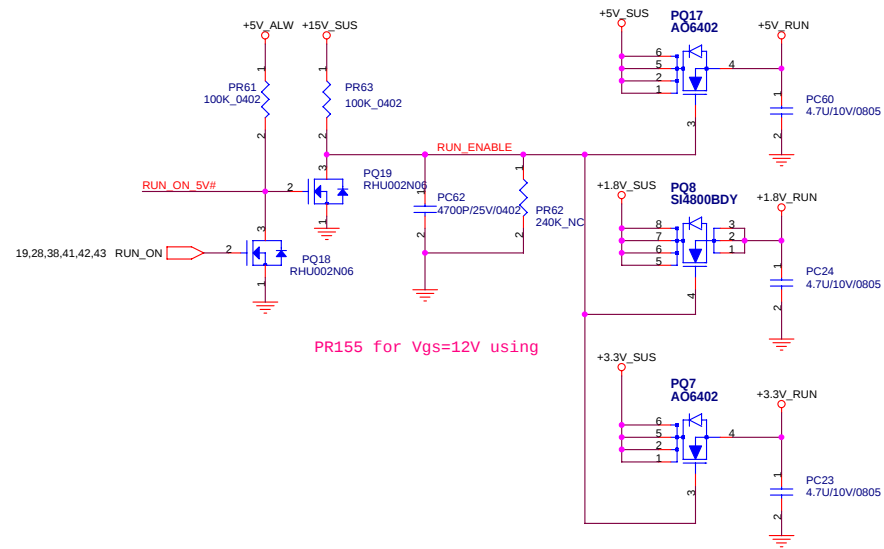
Date: 2895/4/21

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Title			RUN POWER SW
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