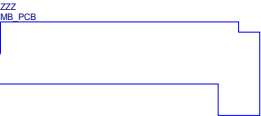


MODEL NAME : *VAZA0*
PCB NO : *LA-9262P (DAB0000I010)*
BOM P/N :

Dell/Compal Confidential

Schematic Document

Murcielgo MLK (Haswell ULT)

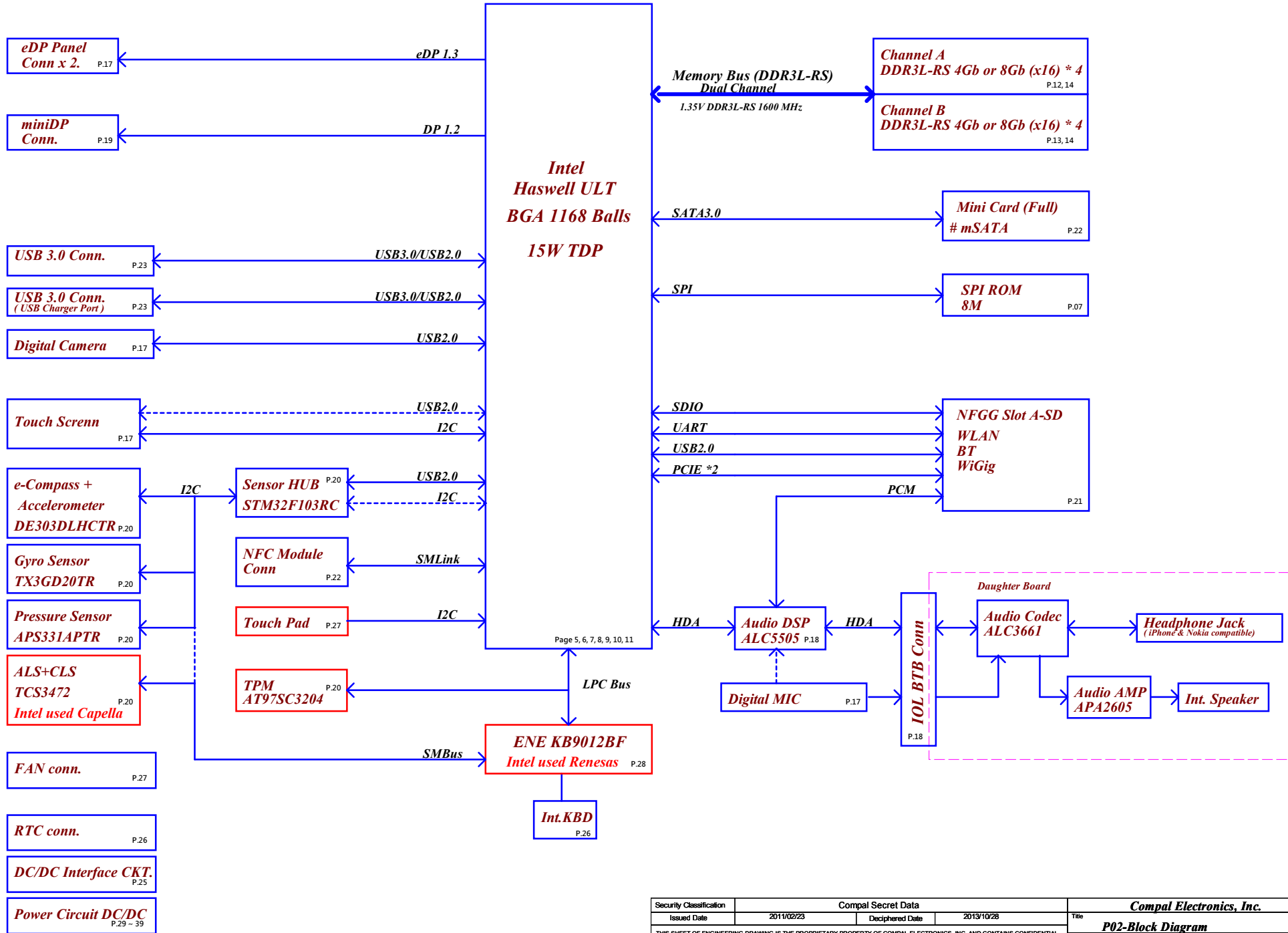


2013-04-19

Rev: 1.0

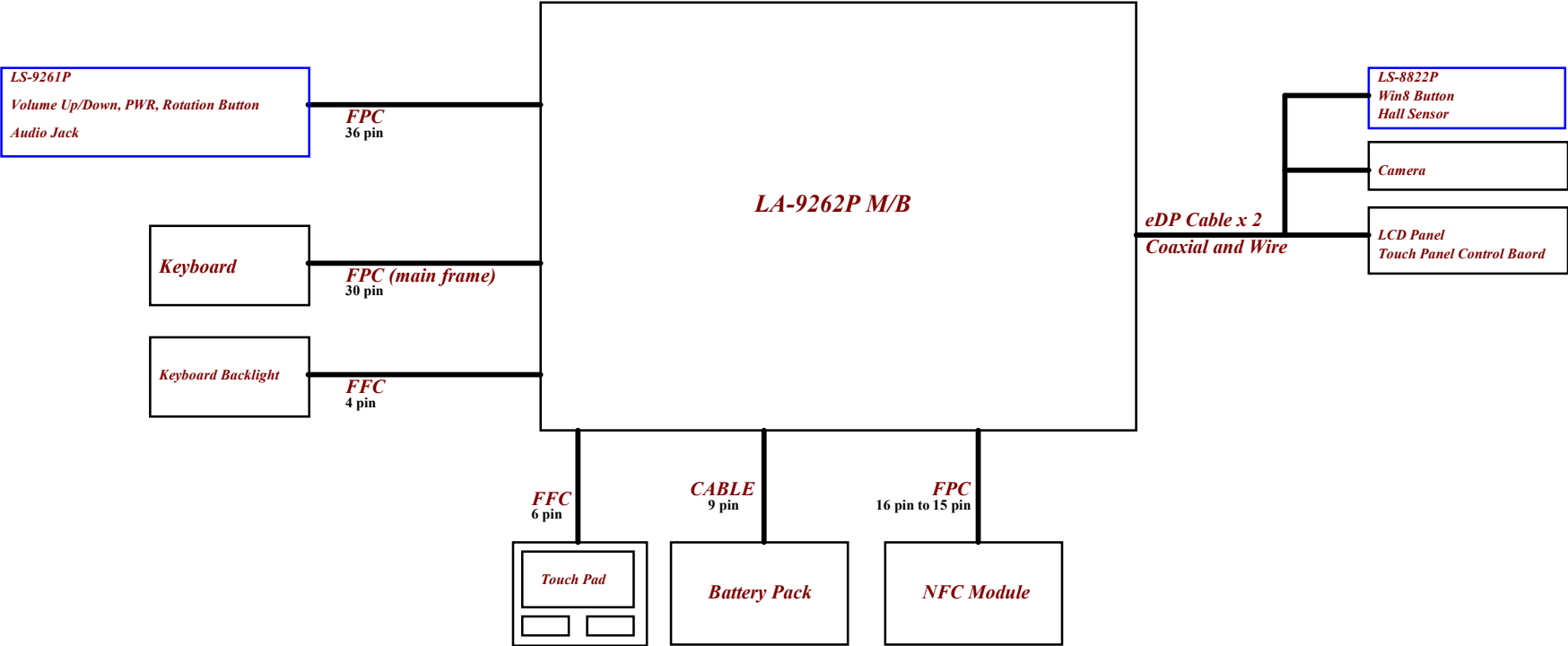
Highlight the short pad for 0 ohm

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					Size	Document Number	Rev
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Compal Confidential

Project Code : VAZA0
File Name : LA-9262P



Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0				
1	12K +/- 1%				
2	15K +/- 1%				
3	20K +/- 1%				
4	27K +/- 1%				
5	33K +/- 1%				
6	43K +/- 1%				
7	56K +/- 1%				
8	75K +/- 1%				
9	100K +/- 1%				
10	130K +/- 1%				
11	160K +/- 1%				
12	200K +/- 1%				
13	240K +/- 1%				
14	270K +/- 1%				
15	330K +/- 1%				
16	430K +/- 1%				
17	560K +/- 1%				
18	750K +/- 1%				
19	NC				

BOARD ID Table

Board ID	PCB Revision
0	CS 0.1
1	CS 0.2
2	CS 0.3
3	CS 0.4
4	CS 0.5
5	CS 1.0
6	
7	
8	
9	
10	Non-CS 0.1
11	Non-CS 0.2
12	Non-CS 0.3
13	Non-CS 0.4
14	Non-CS 1.0
15	
16	
17	
18	
19	

PCH USB Port Mapping	USB PORT#	DESTINATION
	0	External USB3
	1	External USB3
	2	NGFF CARD WLAN
	3	Touch Panel
	4	Camera
	5	Sensors HUB
	6	
	7	

SMBUS Control Table

	SOURCE	NGFF	BATT	Charger	NFC	XDP	DDR3 SPD	ALS	Touch Pad
EC_SMB_CK1 EC_SMB_DA1	KB9012		V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012							V	
PCH_SMLCLK PCH_SMLDATA	PCH	V			V				
PCH_SMLCLK PCH_SMLDATA	PCH								
MEM_SMBCLK MEM_SMBDATA	PCH					V	V		V

Link

PCH DDI Port Mapping	DDI PORT#	DESTINATION
	B	mini-DP
	C	

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0		CLKOUT_LPC_0	EC LPC
	CLKOUT_PCIE1		CLKOUT_LPC_1	TPM
	CLKOUT_PCIE2			
	CLKOUT_PCIE3	NGFF CARD WLAN		
	CLKOUT_PCIE4			
	CLKOUT_PCIE5			

SATA	DESTINATION
SATA0	m-SATA
SATA1	
SATA2	
SATA3	

PCI EXPRESS	DESTINATION
Lane 1	
Lane 2	
Lane 3	NGFF CARD WLAN
Lane 4	NGFF CARD WLAN
Lane 5	
Lane 6	

Symbol Note :

 : means Digital Ground
 : means Analog Ground

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DP

19 PCH_INV_PWM << RC147 1 2 0.0402 5% EDP_BKLCTL
RC146 2 1 0.0402 5% EDP_DISP

@RH123 1 2 100K_0402 5% ENBK1
@RH158 1 2 100K_0402 5% PCH_ENVDD
RH300 1 2 1M_0402 5% PCH_DP_HPD

+3VS
RH281 1 2 2.2K_0402 5% PCH_DP_CLK
RH282 1 2 2.2K_0402 5% PCH_DP_DAT
@RH380 1 2 100K_0402 5% TP_INT#
RP2 1 8 10K_8P4R 5% PCI_PIRQC#
2 7 PCI_PIRQD#
3 6
4 5
@RH396 1 2 10K_0402 5% AUDIO_IRQ#
@RH397 1 2 10K_0402 5% NGFF_WAKE#
@RH381 1 2 100K_0402 5% MPCIE_RST#
RH452 1 2 10K_0402 5% Sensor_RST#

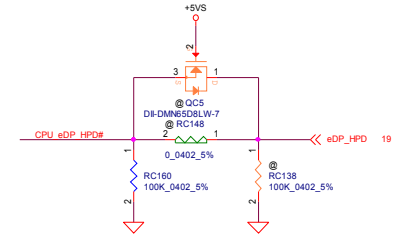
EDP_BKLCTL B8
EDP_BKLCTL A0
EDP_BKLCTL C8
19 ENBK1
19.35 PCH_ENVDD
23 MPCIE_RST# << MPCIE_RST# U6
TPM_IRQ# P4
PCI_PIRQC# N2
PCI_PIRQD# N2
AD4
@T123
29 TP_INT# << TP_INT# U7
19 TS_RST# L1
23 NGFF_WAKE# L3
22 Sensor_RST# L4
AUDIO_IRQ# L4
GPIO55
GPIO52
GPIO54
GPIO51
GPIO53

EDP_TXN0 C45
EDP_TXP0 B46
EDP_TXN1 A47
EDP_TXP1 B47
EDP_TXN2 C47
EDP_TXP2 C48
EDP_TXN3 A49
EDP_TXP3 B49
EDP_AUXN A45
EDP_AUXP B45
+VCCIOA_OUT
D20 +EDP_COM RC36 1 2 24.9 0402 1%
A43 EDP_DISP @RC158 2 1 0.0402 5%

Width 20 mils, Spacing 25 mils,
Length < 100 mil



DDPB_CTRLCLK B9
DDPB_CTRLCLK C9
DDPB_CTRLCLK D11
PCH_DP_CLK B9
PCH_DP_DAT C9
PCH_DP_CLK 21
PCH_DP_DAT 21
DDPB_AUXN C5
DDPB_AUXN B6
DDPB_AUXP B5
PCH_DP_AUXN 21
PCH_DP_AUXP 21
PCH_DP_HPD C8
CPU_eDP_HPD# A5
CPU_eDP_HPD# D6
PCH_DP_HPD 21



+1.05VS_VCCST
RC43 62 0402 5%
30 H_PECI @T2
H_CATERR# K61
H_PROCHOT# K63
H_PROCHOT# 30.32
H_PROCHOT# << RC41 2 56_0402 5%
H_CPUWGRD_R C61
H_CPUWGRD_R 10K_0402 5%
RC44 1 2



Avoid stub in the PWRGD path
while placing resistors RC44 & RC53

Width 15 mils, Spacing 25 mils, Length < 500 mil

200 0402 1% 2 RC55
121 0402 1% 2 RC58
100 0402 1% 2 RC60
H_DRAMRST# AV15
DDR_PG_CNTL AV61

SM_RCOMP0 AU60
SM_RCOMP1 AV60
SM_RCOMP2 AU61
SM_RCOMP2 AV15
SM_DRAMRST AV15
SM_PG_CNTL AV61

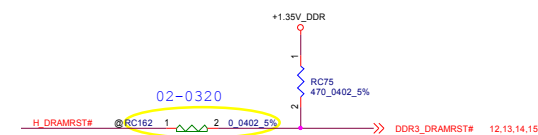
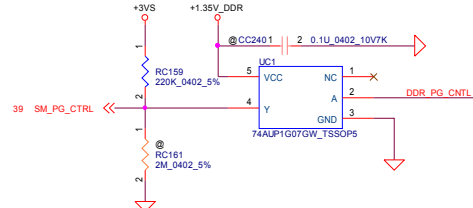
UCPU1B HSX_LUT_D0RL
PROC_DETECT K61
CATERR# N62
PROCHOT K63
H_CATERR# K61
H_PROCHOT# K63
H_CPUWGRD_R C61
PROC_PWRGD C61
PROC_TCK K62
PROC_TMS E61
PROC_TRST# F63
PROC_TDI F62
PROC_TDO F62
XDP_PRODY# J62
XDP_FREQ# K62
CPU_XDP_TCK E60
CPU_XDP_TMS E61
CPU_XDP_TRST# F63
CPU_XDP_TDI F62
CPU_XDP_TDO F62
XDP_BPMD# J60
XDP_BPMD# H60
XDP_BPMD# H61
XDP_BPMD# H62
XDP_BPMD# K59
XDP_BPMD# H63
XDP_BPMD# K60
XDP_BPMD# J61
SM_RCOMP0 AU60
SM_RCOMP1 AV60
SM_RCOMP2 AU61
SM_RCOMP2 AV15
SM_DRAMRST AV15
SM_PG_CNTL AV61

closed MCP 1000 mils

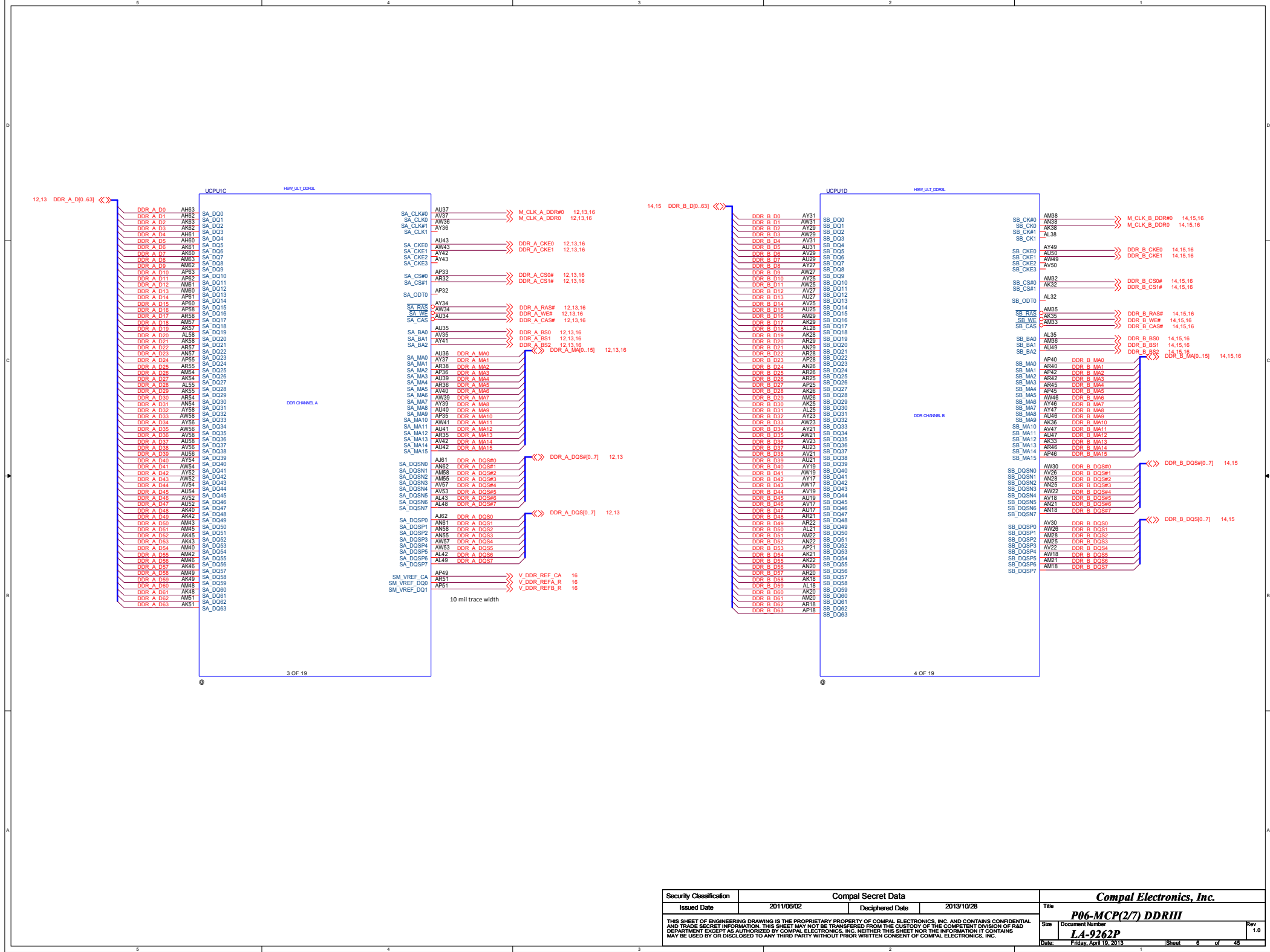
XDP_PRODY# @T263
XDP_FREQ# @T264
CPU_XDP_TCK @T265
CPU_XDP_TMS @T266
CPU_XDP_TRST# @T267
CPU_XDP_TDI @T268
CPU_XDP_TDO @T269

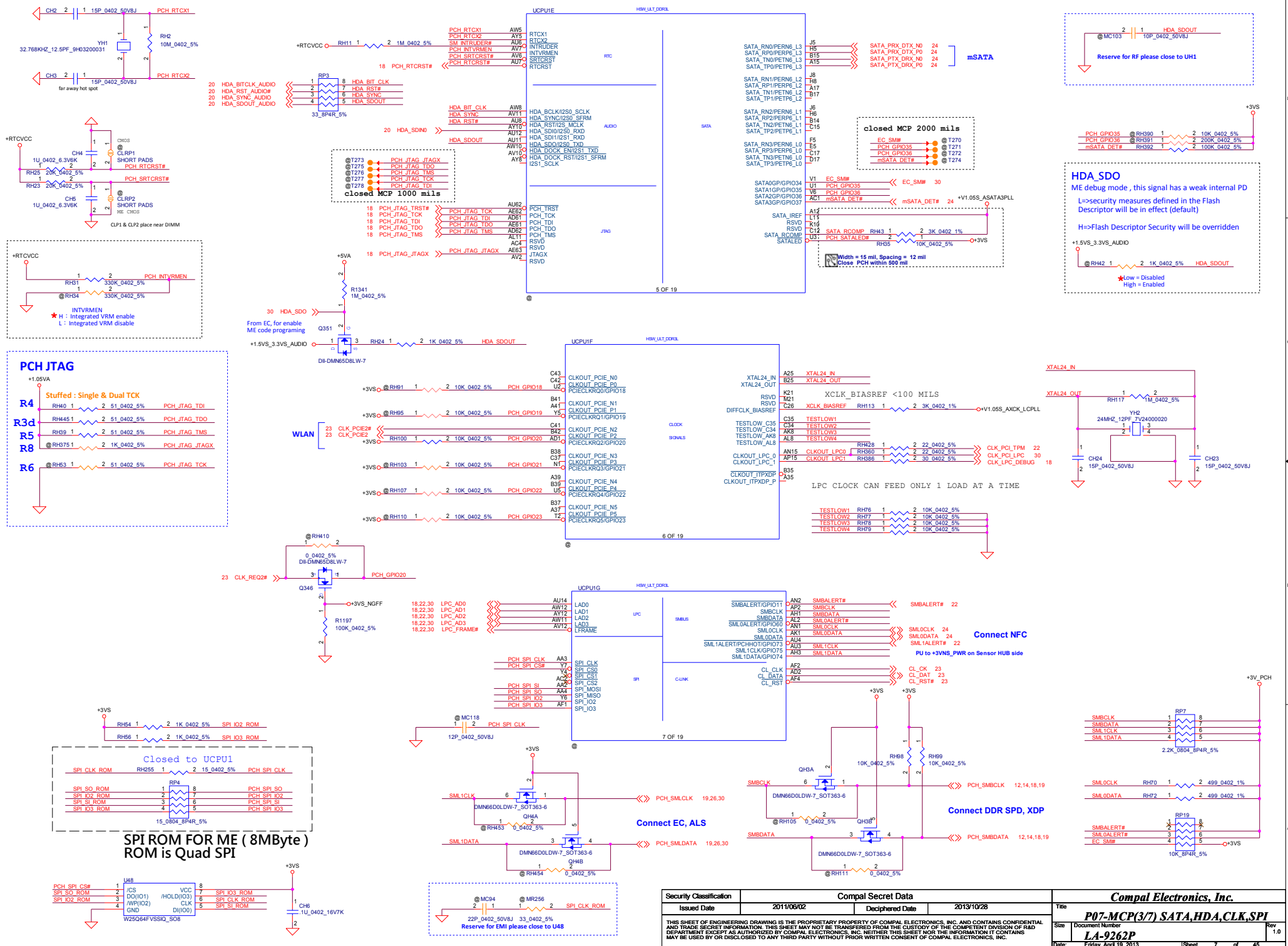
PU/PD for JTAG signals

+1.05VS_VCCST
CPU_XDP_TMS 51 0402 5% 1 2 RC45 @
CPU_XDP_TDI 51 0402 5% 1 2 RC46 @
CPU_XDP_TDO 51 0402 5% 1 2 RC48 @
R1d
Stuffed : Dual TCK
unstuffed : Singel TCK
CPU_XDP_TCK 51 0402 5% 1 2 RC52 @
CPU_XDP_TRST# 51 0402 5% 1 2 RC54 @
R2
R9

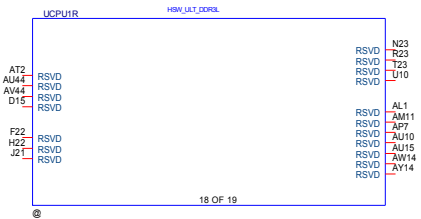
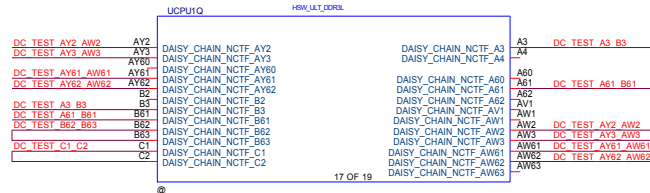
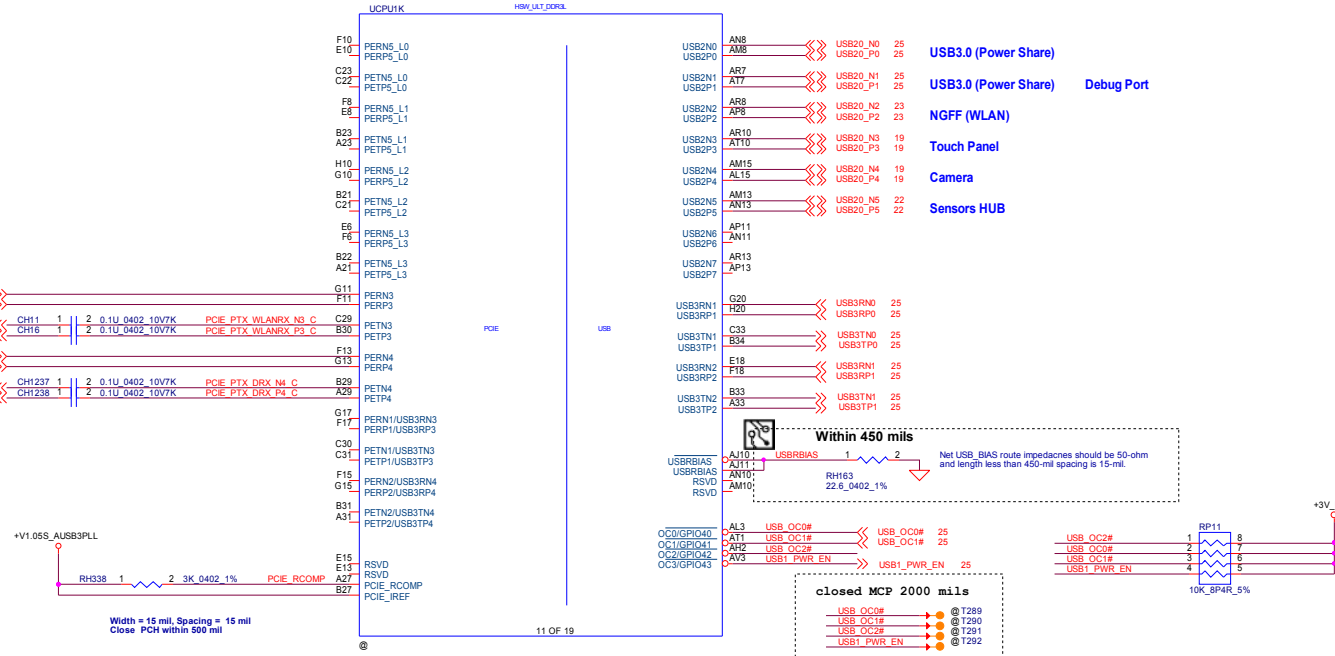


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		Rev	1.0

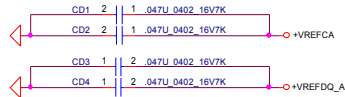




NGFF



follow INTEL PDG

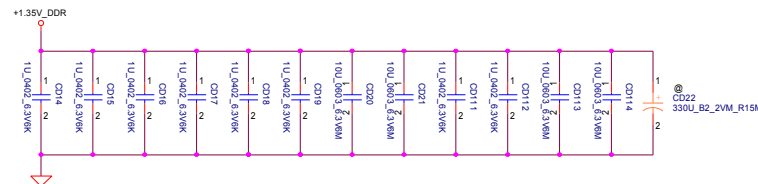
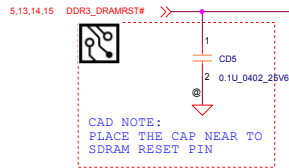
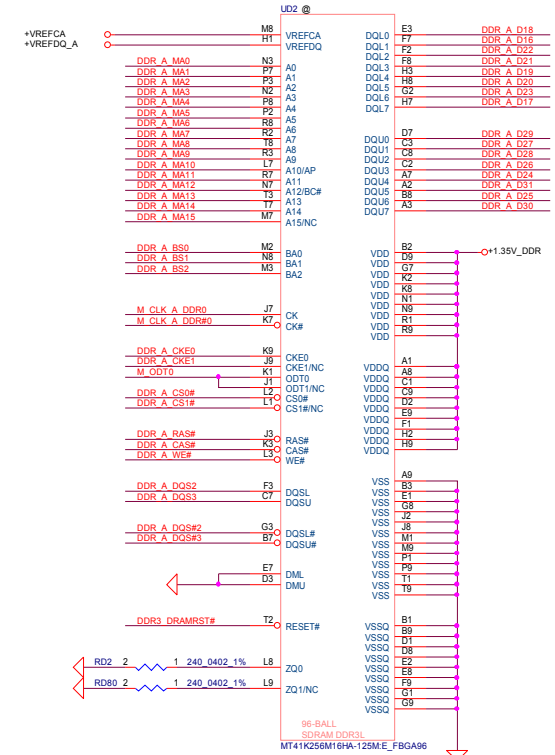
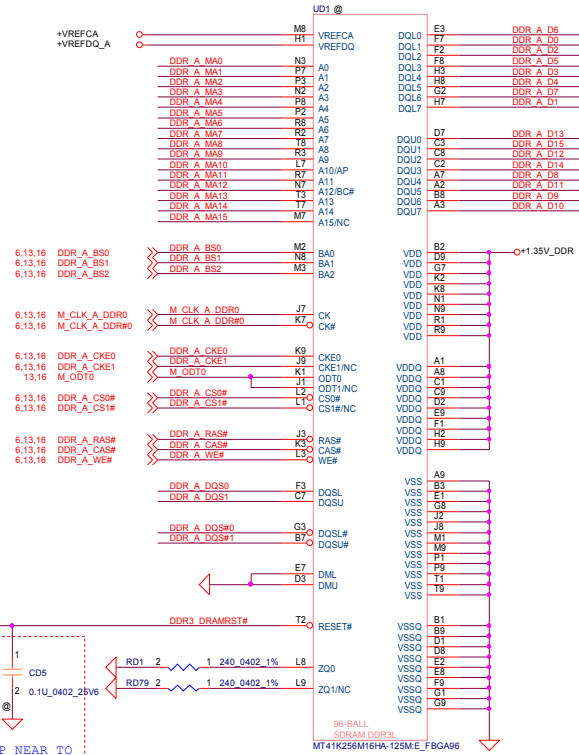


PLACE THESE CAPS
NEAR TO RESPECTIVE DIMM PINS

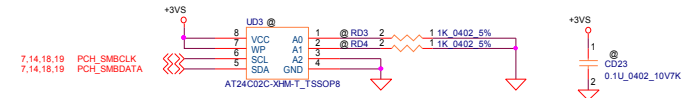


6.13 DOR_A_DQS# [0..7] <<>>
6.13 DDR_A_DQS [0..7] <<>>
6.13 DOR_A_D [0..63] <<>>
6.13.16 DOR_A_MA [0..15] <<>>

All VREF traces should
have 10 mil trace width



Memory Channel A SPD EEPROM



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Date: Friday, April 19, 2013					

follow INTEL PDG

CD24 2 1 047U_0402 16V7K

CD25 2 1 047U_0402 16V7K → VREFCA

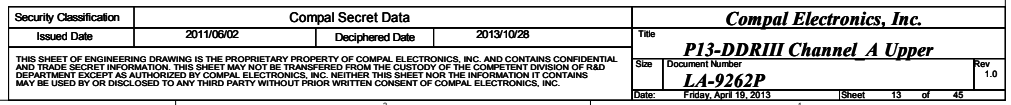
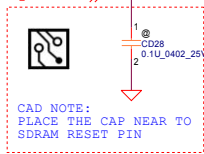
CD26 2 2 047U_0402 16V7K

CD27 2 2 047U_0402 16V7K → VREFDQ_A

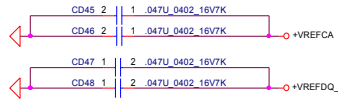
**PLACE THESE CAPS
NEAR TO RESPECTIVE DIMM PINS**



6,12	DDR_A_DQS#[0..7]	<<>>	
6,12	DDR_A_DQS[0..7]	<<>>	
6,12	DDR_A_D[0..63]	<<>>	
6,12,16	DDR_A_MA[0..15]	<<>>	



follow INTEL PDG

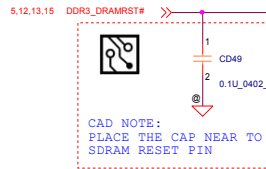


PLACE THESE CAPS
NEAR TO RESPECTIVE DIMM PINS

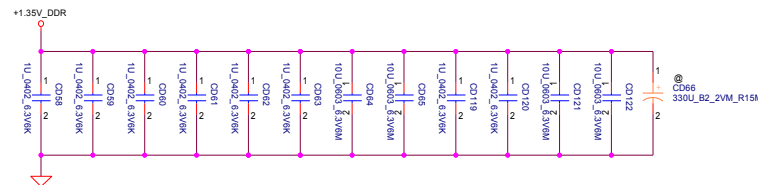


6.15 DDR_B_DQS#(0..7) <<>>
6.15 DDR_B_DQS(0..7) <<>>
6.15 DDR_B_DQ(0..63) <<>>
6.15,16 DDR_B_MA(0..15) <<>>

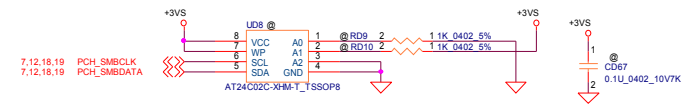
All VREF traces should
have 10 mil trace width



CAD NOTE:
PLACE THE CAP NEAR TO
SDRAM RESET PIN



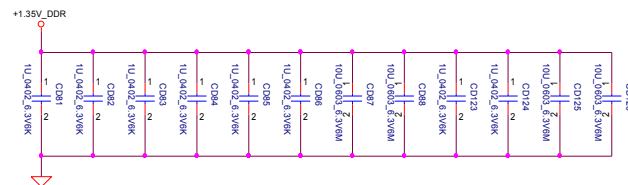
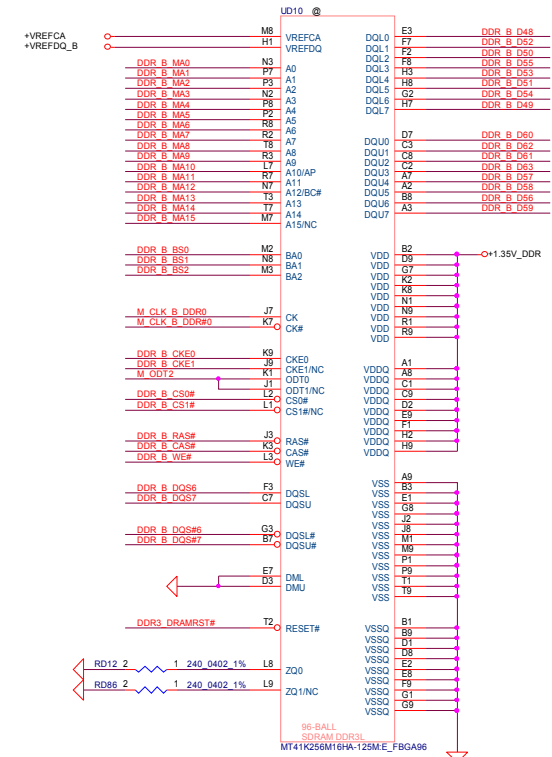
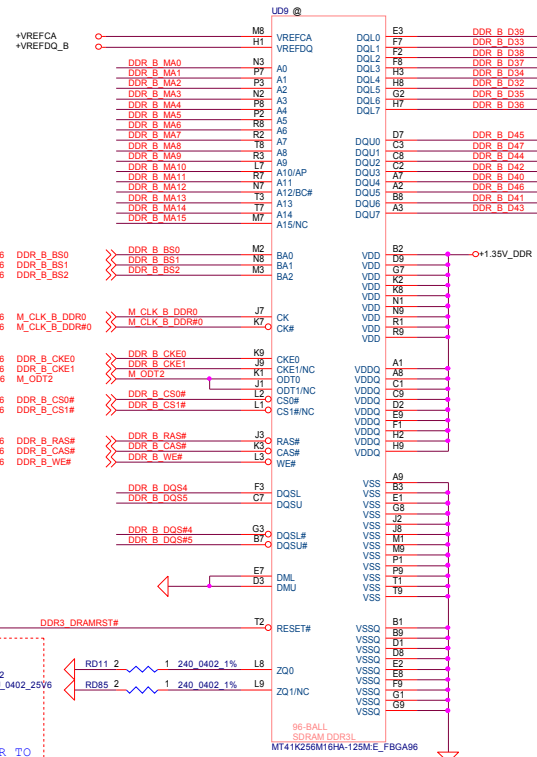
Memory Channel B SPD EEPROM



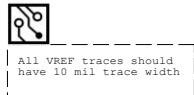
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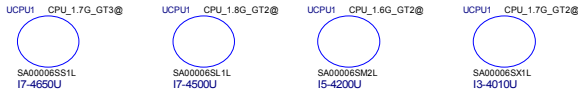
All VREF traces should have 10 mil trace width



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				Size Document Number LA-9262P	
				Date:	Friday, April 19, 2013
				Sheet	15 of 45
				Rev	1.0

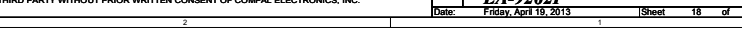
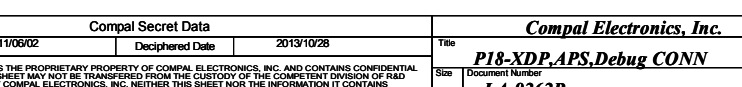
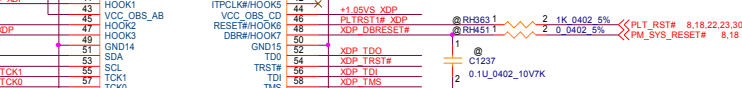
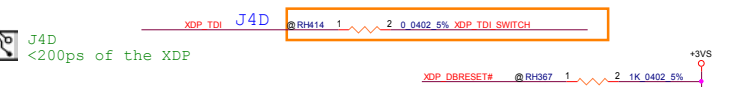
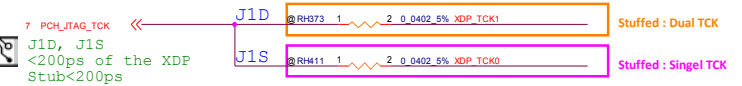
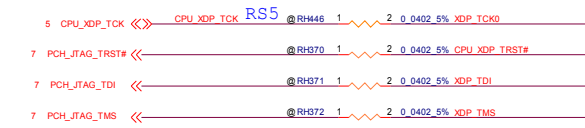
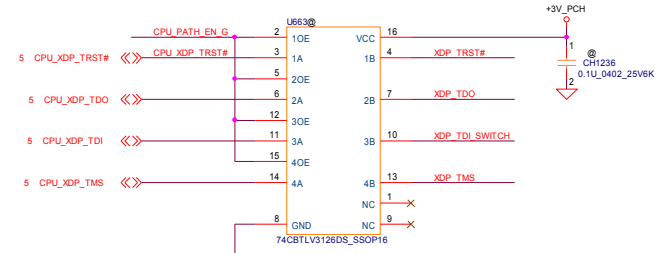
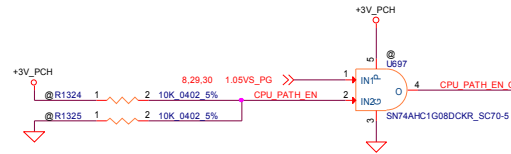


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				Date:	Friday, April 19, 2013
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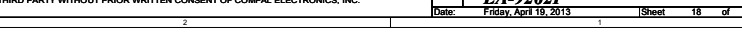
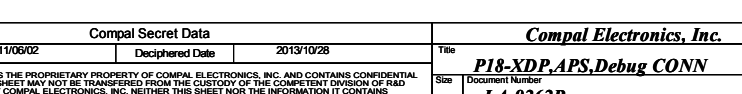
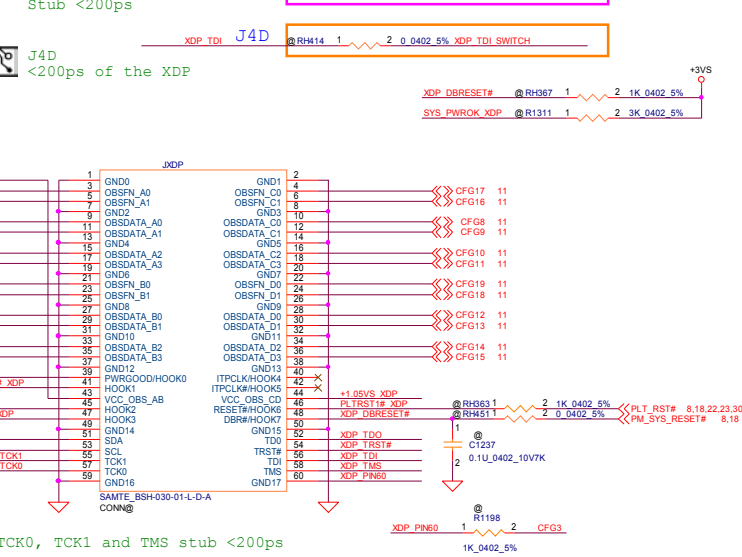
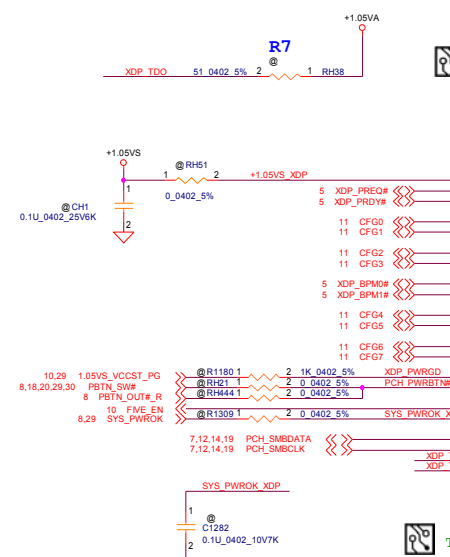
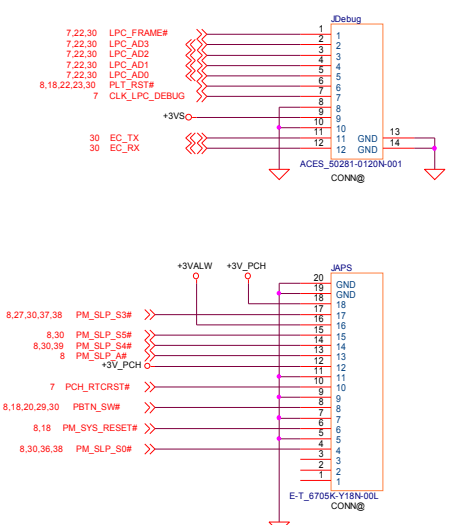


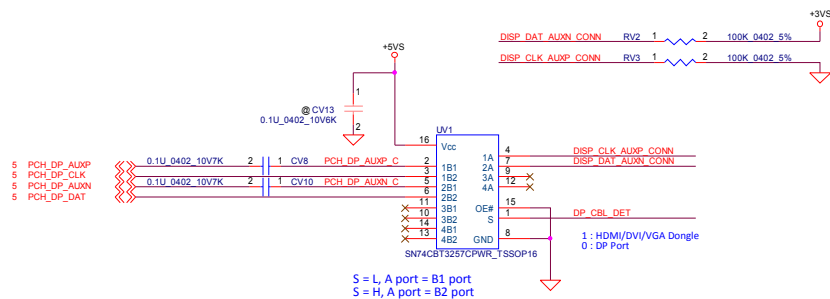
03-0320

U663 200ps of XDP

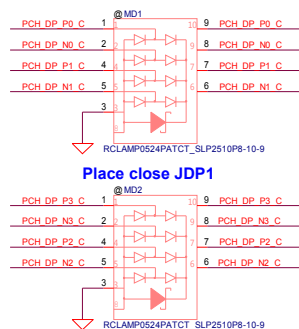


Topolog	Description	Best Use for	Resistors Stuffed	Resistors uStuffed
Default Setting: Dual TCK Scan Chains (also known as "Shared JTAG" in other document)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1, R2, J1d, J2d, J3d, J4d, R3, R4, R5	J1s, J2s, J3s
Single TCK scan chain (also known as "Common JTAG" in other document)	In this topology, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	- Boundary Scan/ Manufacturing test	J1s, J2s, J3s, J4d, R2, R3, R4, R5	R1, J1d, J2d, J3d, J4d

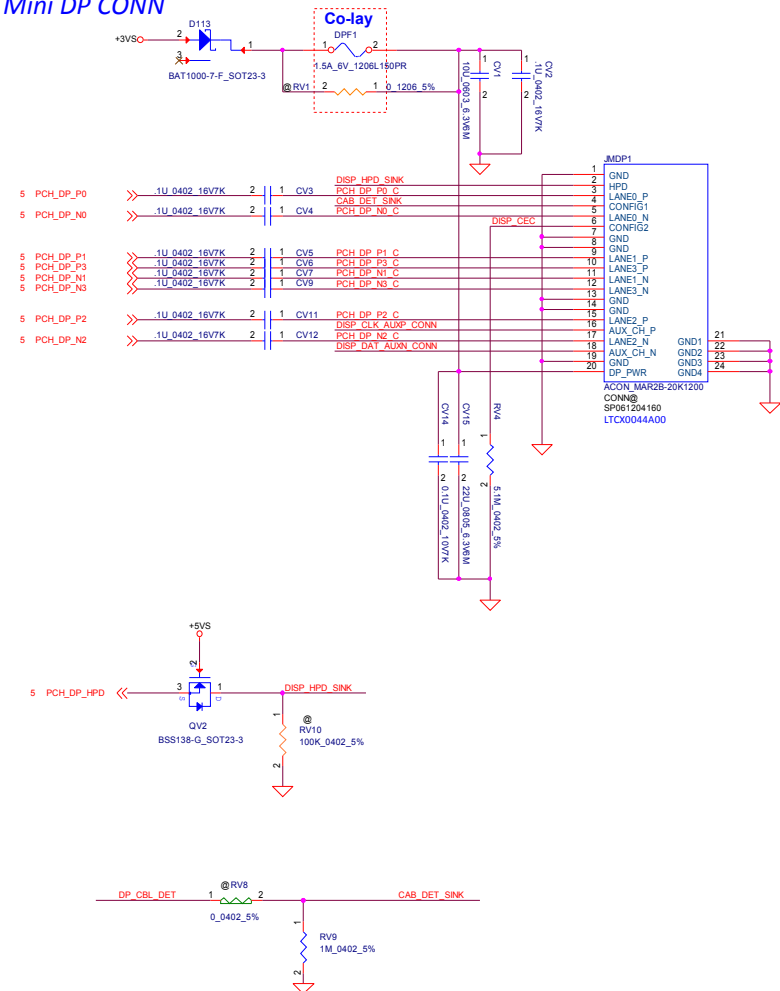




DP Signal ESD

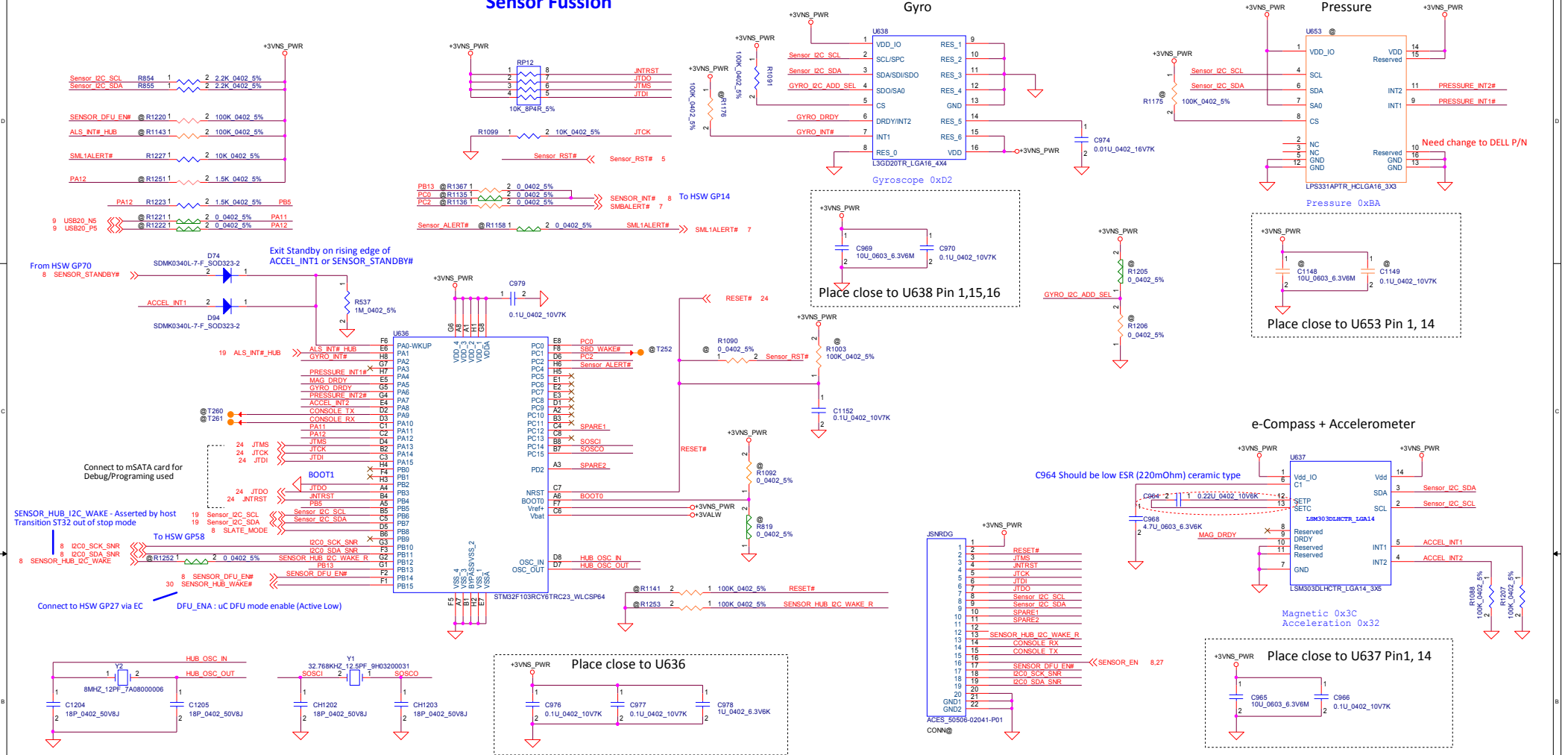
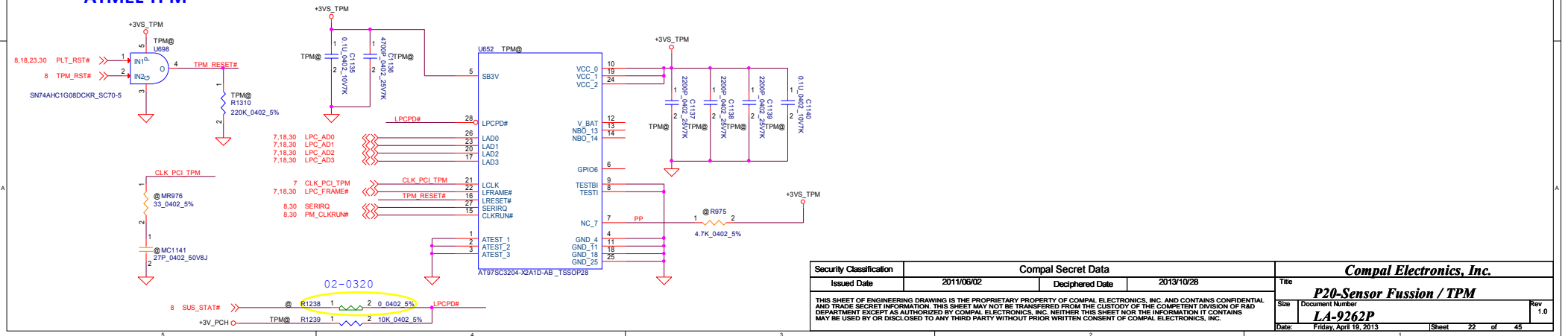


Mini DP CONN



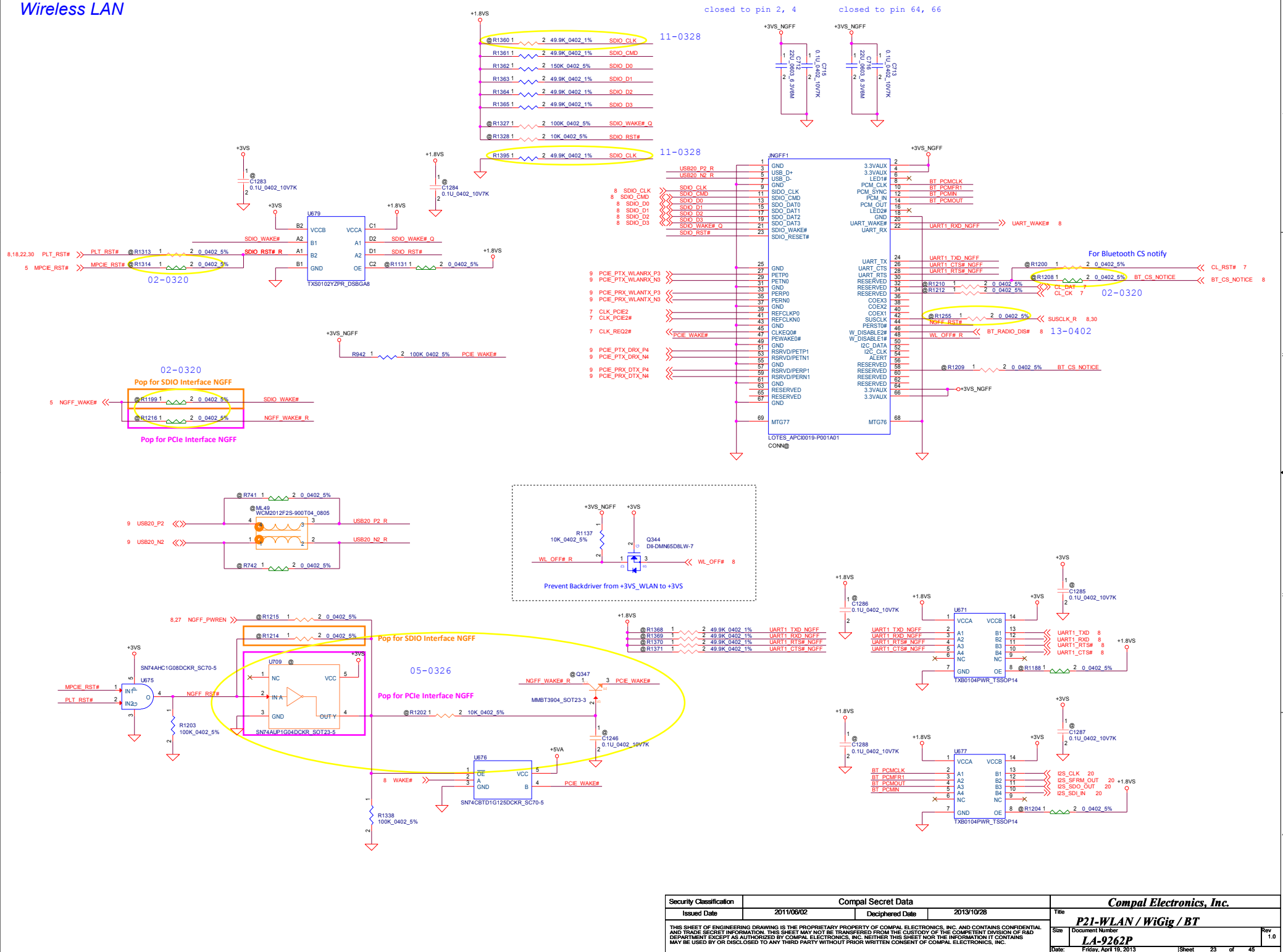
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Issued Date	2011/05/02	Deciphered Date	2013/10/28	Title	
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Size	C	Document Number	LA-9262P	Rev	1.0
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Sensor Fussion

**ATMEL TPM**

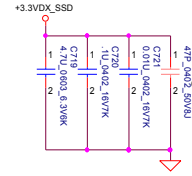
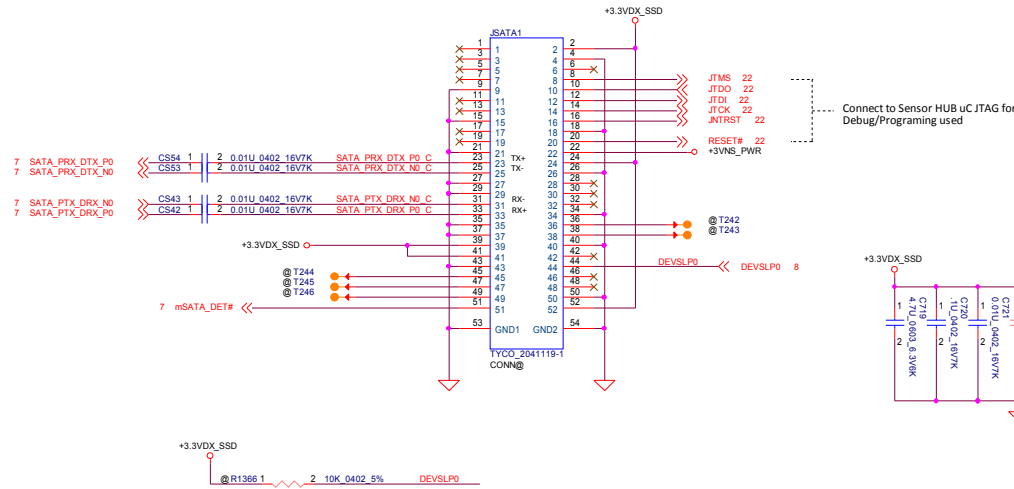
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
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				Size	Document Number
				LA-9262P	
Date:	Friday, April 19, 2013	Sheet	22	of	45

Wireless LAN

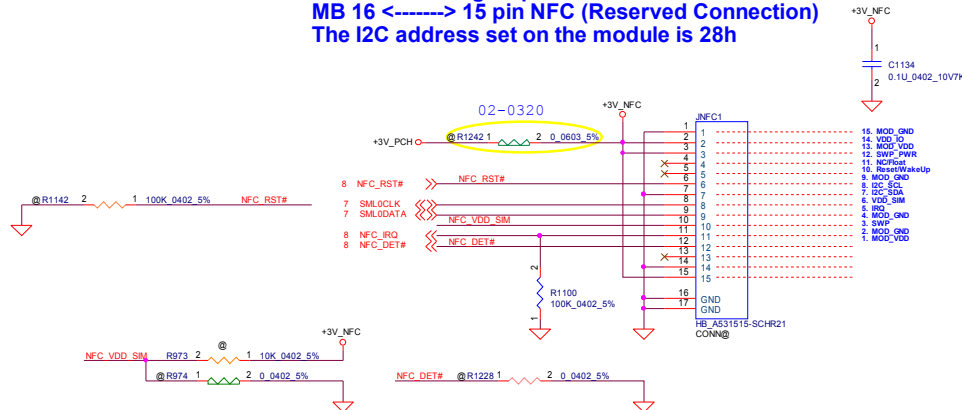


Security Classification	Compal Secret Data			Title			
Issued Date	2011/06/02	Deciphered Date	2013/10/28	P21-WLAN / WiGig / BT			
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				A-9262P Friday, July 19, 2013			1.0
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mSATA Card

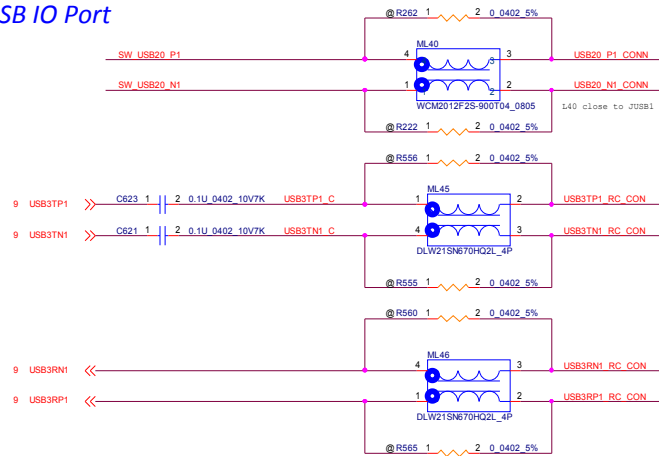


ME Decide using 16 pin conn
MB 16 <-----> 15 pin NFC (Reserved Connection)
The I2C address set on the module is 28h

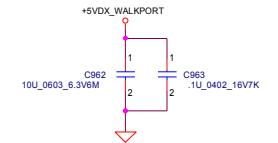
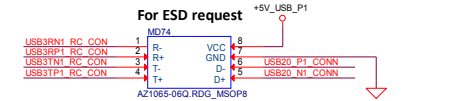
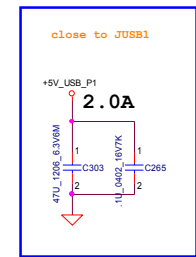
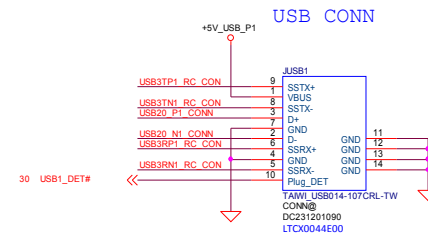
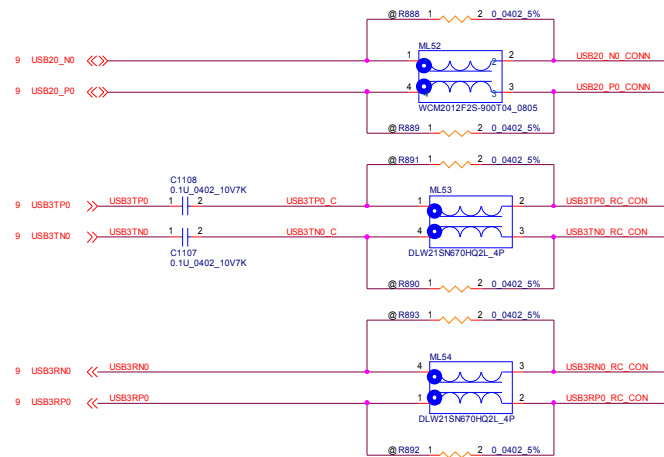


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Issued Date	2011/05/02	Deciphered Date	2013/10/28	Title	
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Size	C	Document Number	LA-9262P	Rev	1.0
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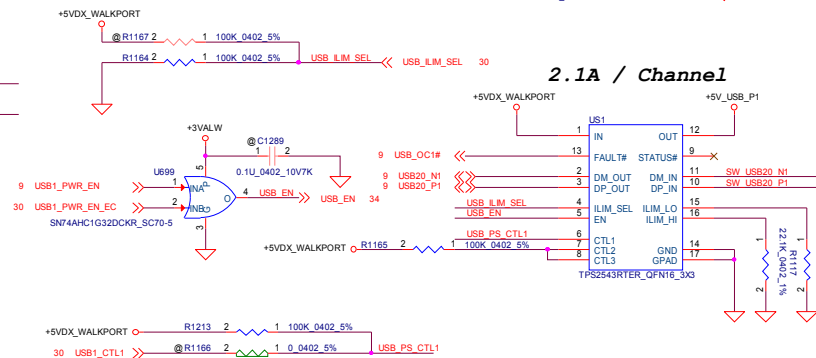
USB IO Port



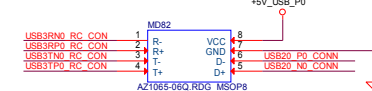
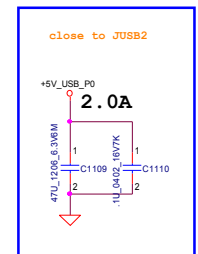
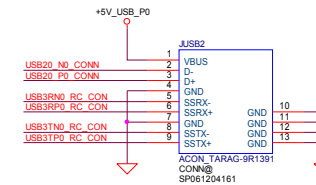
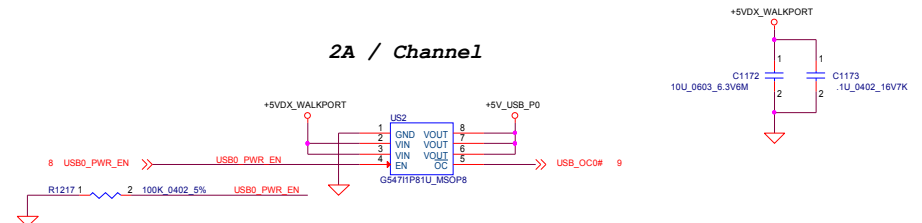
CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDF
1	1	1	1	CDP



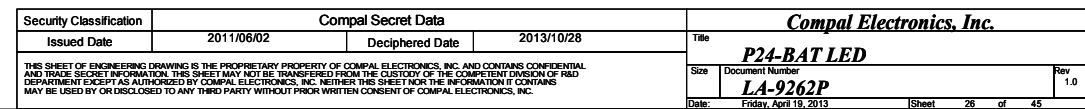
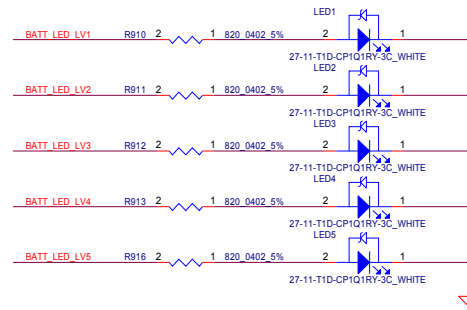
2.1A / Channel



2A / Channel



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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	<i>P23-USB 3.0 IO CONN</i>
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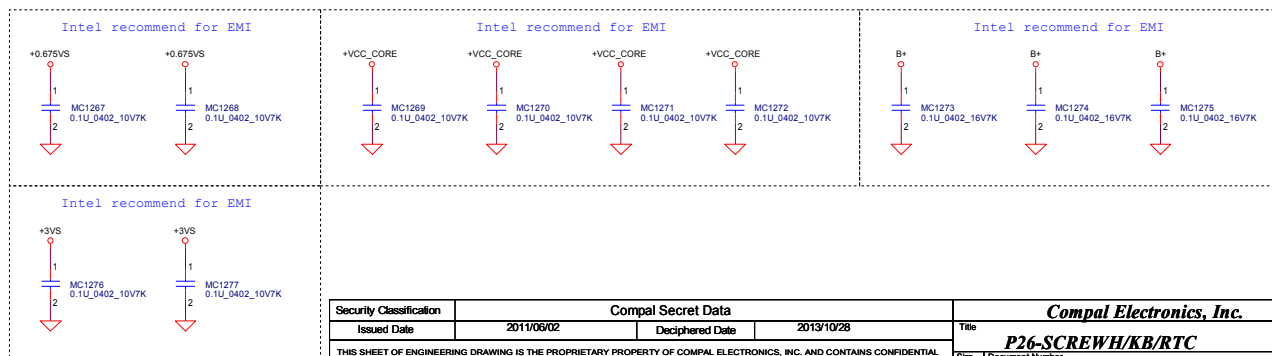
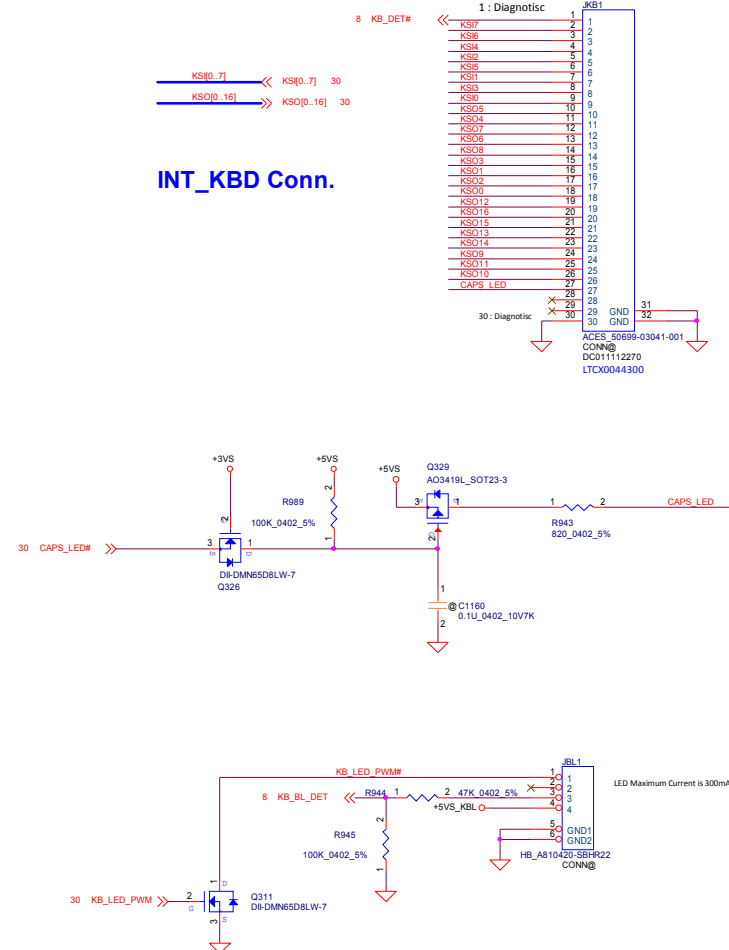
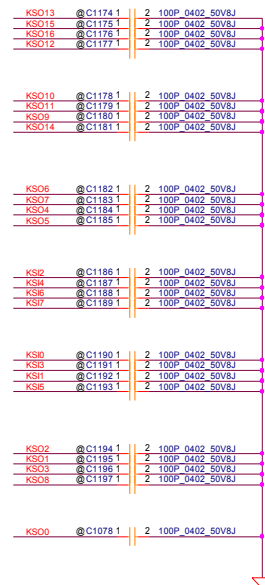
The schematic diagram illustrates a multi-channel system with the following components and connections:

- H1**: Connected to **H_2P3**, which is connected to ground.
- H5**: Connected to **H_2P3**, which is connected to ground.
- H6**: Connected to **H_2P3**, which is connected to ground.
- H8**: Connected to **H_2P3**, which is connected to ground.
- H14**: Labeled **NUT**, connected to **H_3P2**, which is connected to **CONN2** and ground.
- H16**: Connected to **H_2P0X2PSN**, which is connected to ground.
- H17**: Connected to **H_2PON**, which is connected to ground.
- H3**: Connected to **H_4P0**, which is connected to ground.

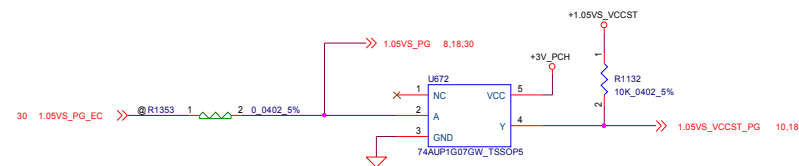
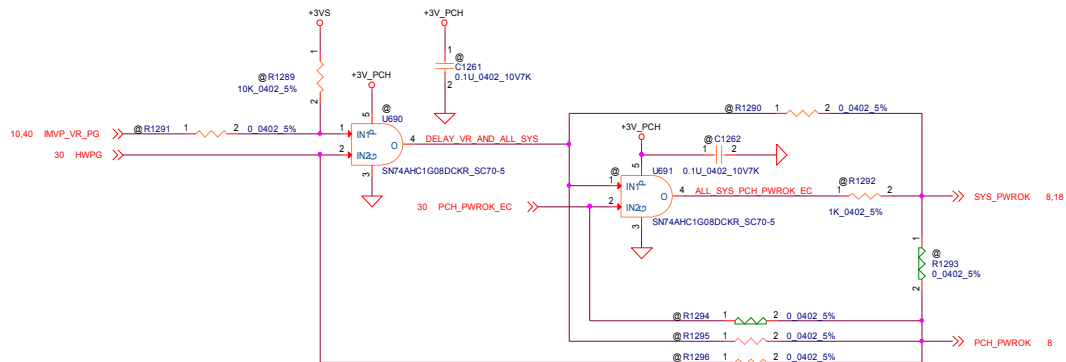
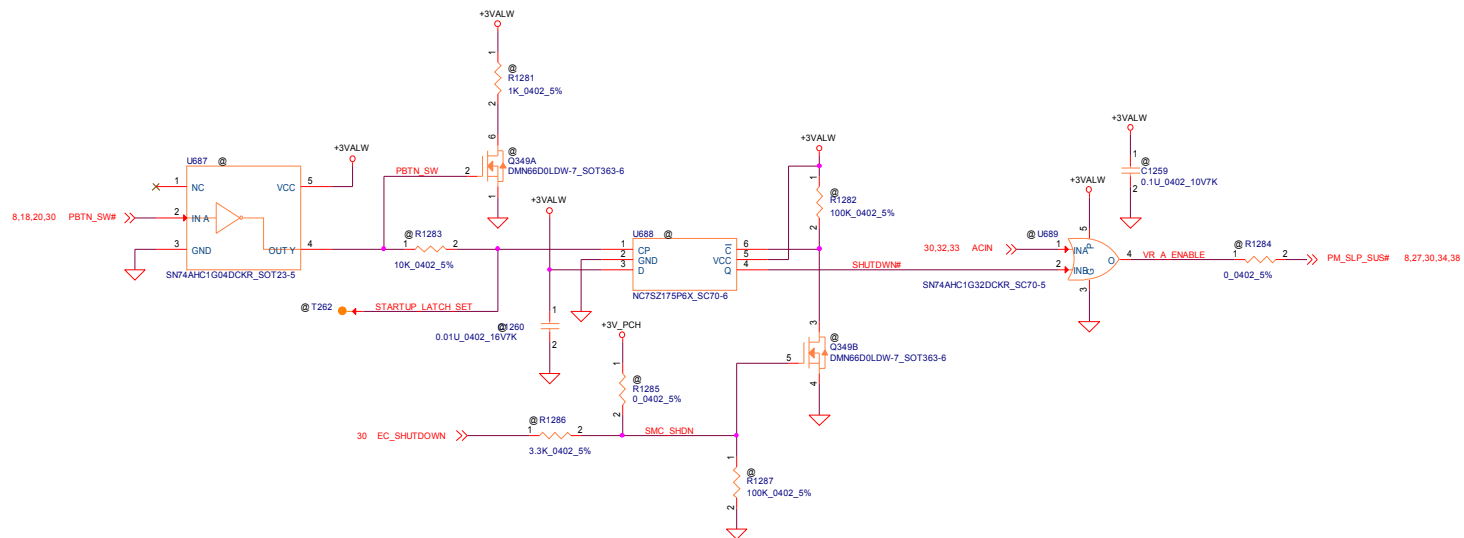
Diagram illustrating a 2x2 MIMO system with four antennas labeled H0, H10, H11, and H12. Each antenna is connected to an H_{3P2} CONN@ block, which is then connected to a red triangle representing a receiver or antenna port.

A diagram of a neuron. The cell body is a yellow circle with a black outline. Inside the cell body is a smaller yellow circle. To the right of the cell body is a long, thin, yellow axon. The axon ends in a small, yellow, bulbous structure. The labels are: H13 (above the cell body), H_4P5N (to the left of the cell body), and CONN@ (below the cell body). A red 'X' is drawn over the axon.

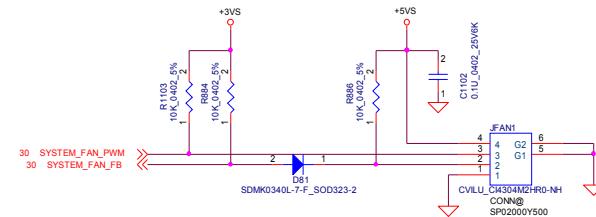
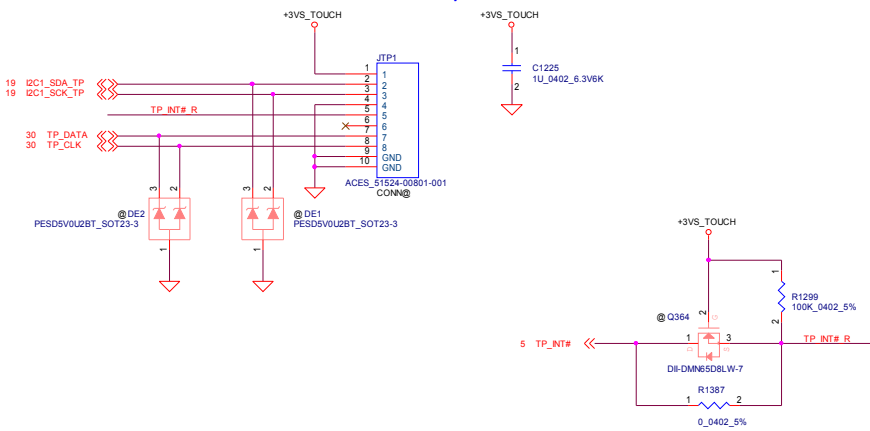
The image contains two circuit diagrams for the ACS 50271-00201-001. The left diagram shows the +RTCBATT and +3VLP inputs connected to a diode bridge, with a 1K_0402_5% resistor and a 10u_0402_6.3V8K diode. The right diagram shows the +RTCVCC input connected to a 12-0328 diode bridge, with a 10u_0402_6.3V8K diode and a 1K_0402_5% resistor. Both diagrams include a 20mils trace width and a 20mils trace length.



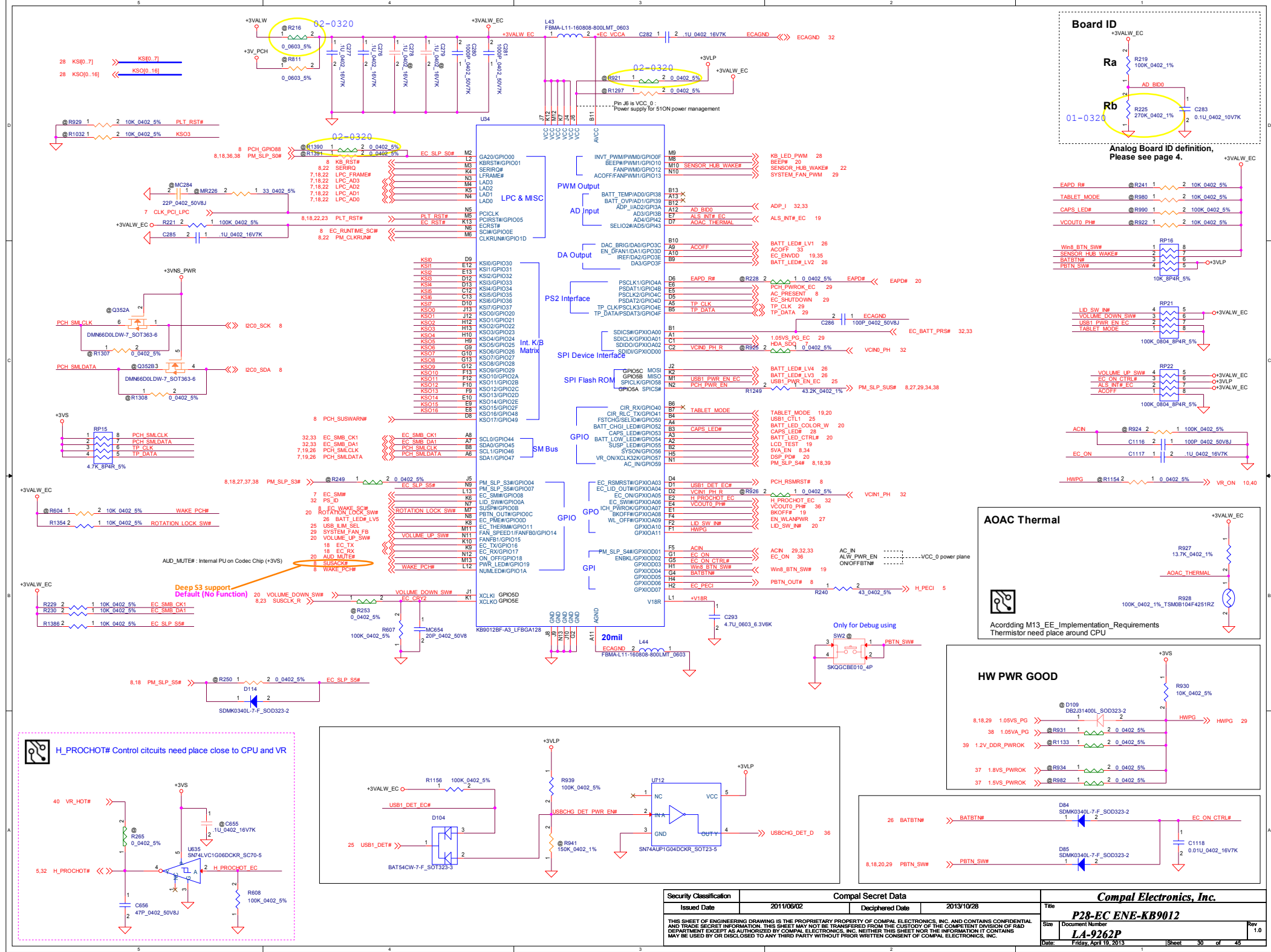
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				Size	Document Number
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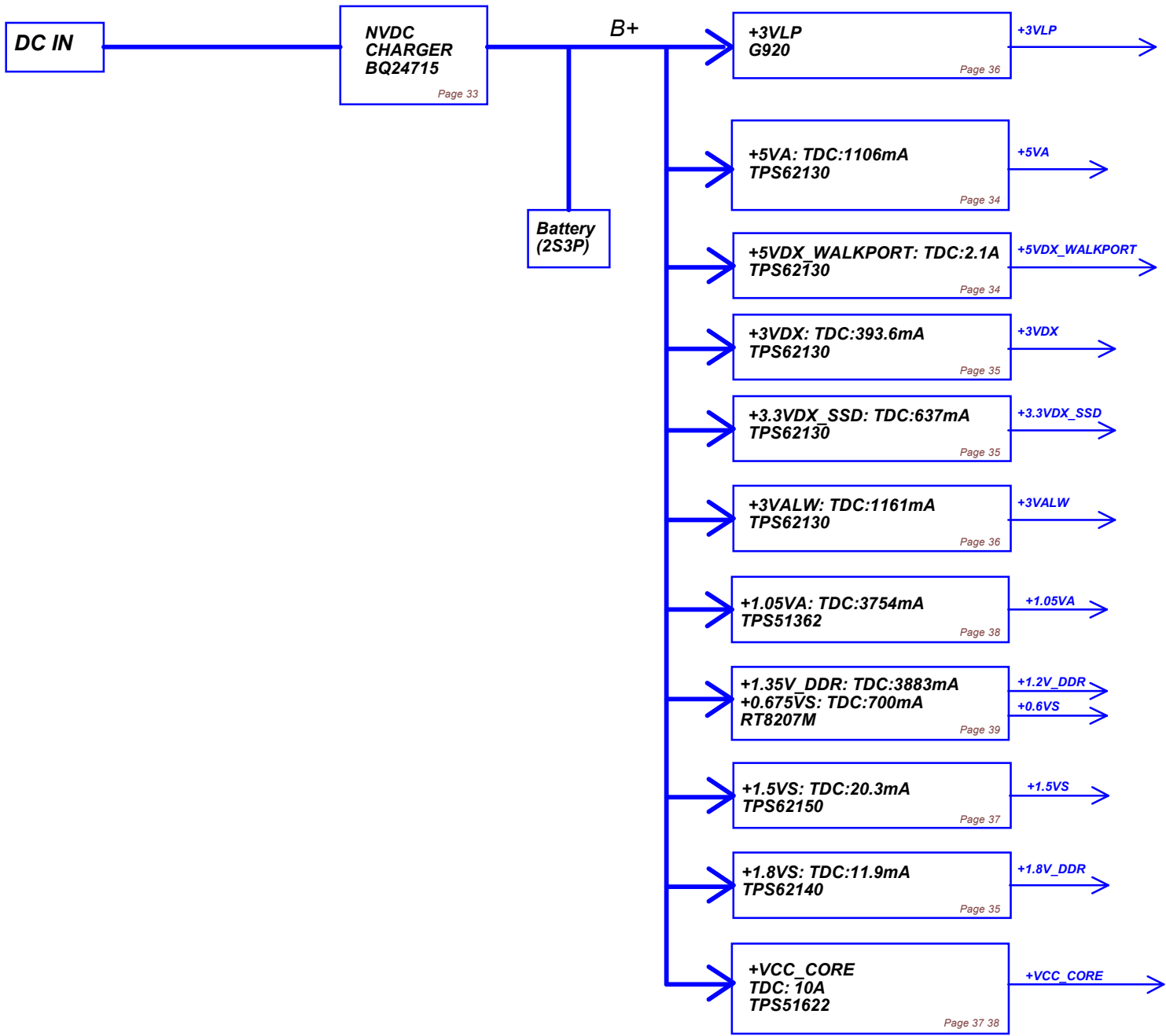


Touchpad CONN

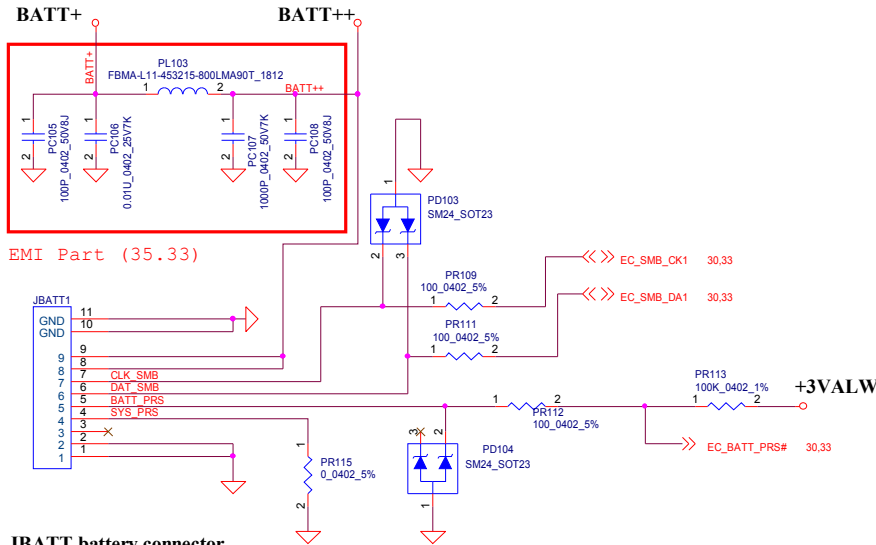
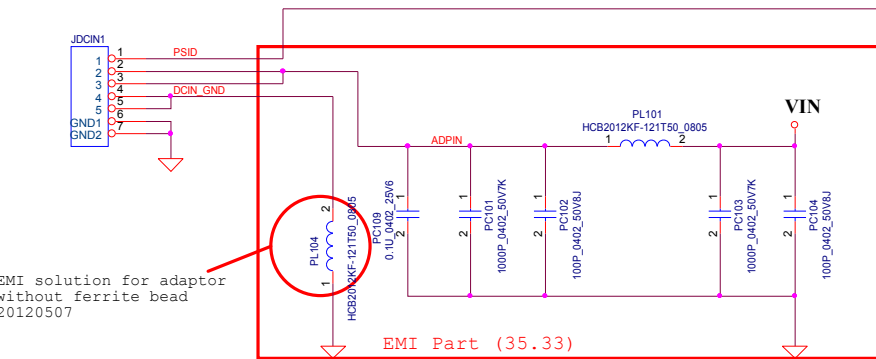


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/05/02	Deciphered Date	2013/10/28	Title	P27-TP / FAN/POWERGD
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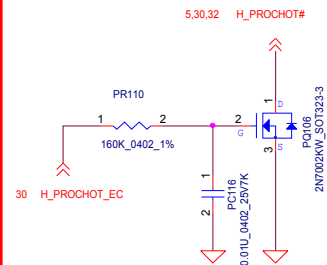
EMI solution for adaptor without ferrite bead
20120507



JBATT battery connector

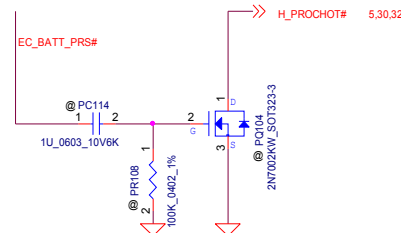
SMART Battery:
1.GND
2.GND
3.BAT_ALERT
4.SYS_PRES
5.BATT_PRS
6.DAT_SMB
7.CLK_SMB
8.BATT++
9.BATT++

Delay adaptor OC H_PROCHOT#
2ms while hybrid power transition



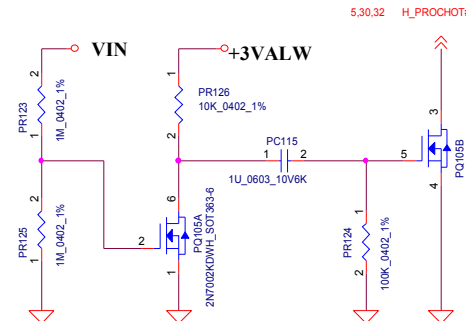
Adaptor protection:

if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep DNP in BOM since battery can not
be removed by end user



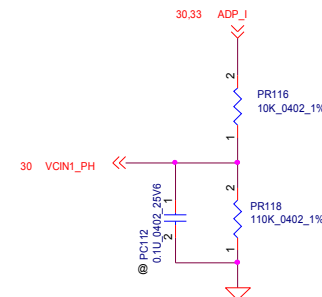
Battery protection:

asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW_PROCHOT# is issued by EC



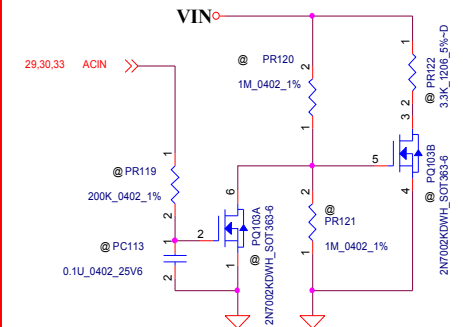
Adaptor protection:

if CP and IPCC failed, adaptor output
=rating 100% and over load 20W
then trigger the H_PROCHOT# by EC



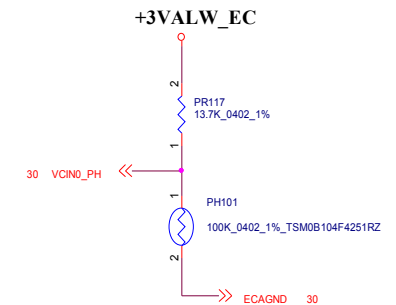
Erp lot6 Circuit

keep DNP in BOM since Dell 45W
adaptor has no hiccup mode

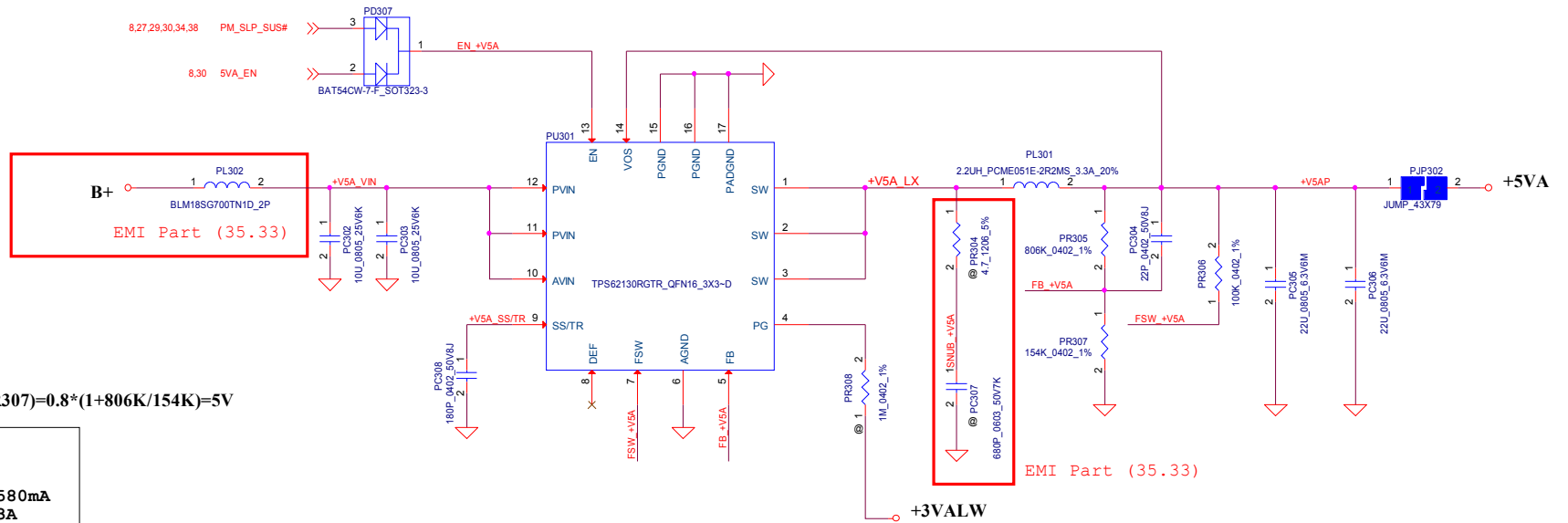


PH101 under CPU bottom side :

CPU thermal protection
@88+-3 degree C
Recovery at 80+-3 degree C

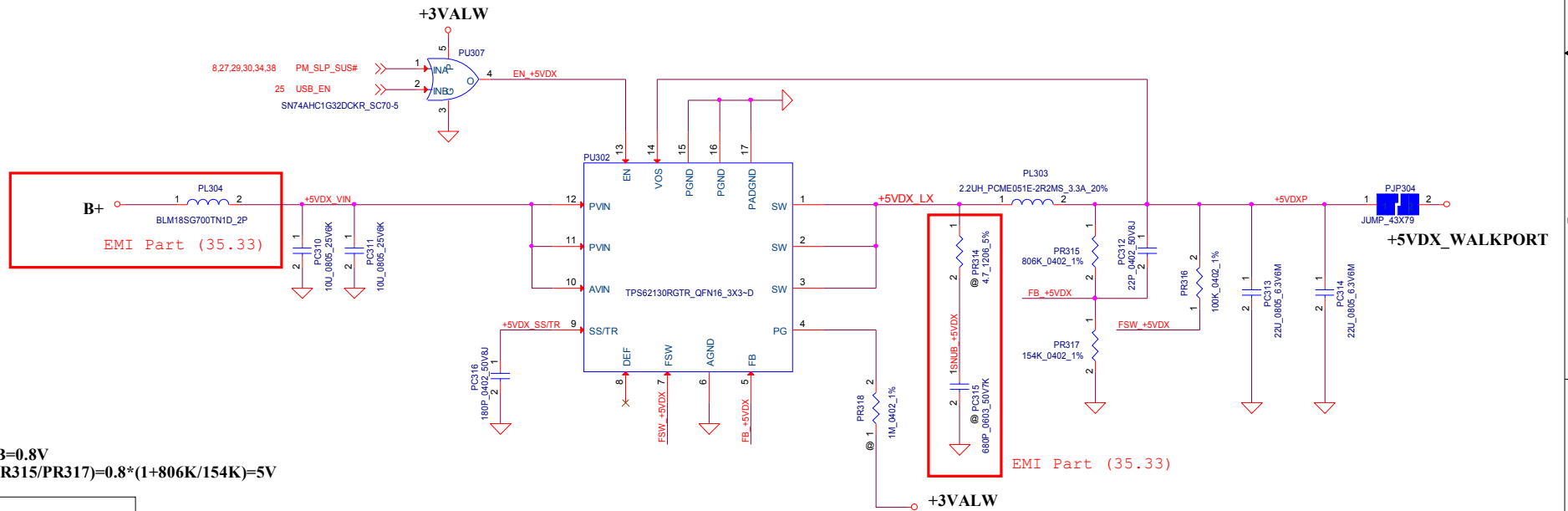


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P30-PWR DCIN/BATT CONN/OTP
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$\langle V_o=5V \rangle$ $V_{FB}=0.8V$
 $V_o = V_{FB} * (1 + PR305/PR307) = 0.8 * (1 + 806K/154K) = 5V$

+5VA
 TDC 1106mA
 Peak Current 1580mA
 OCP setting @ 3A



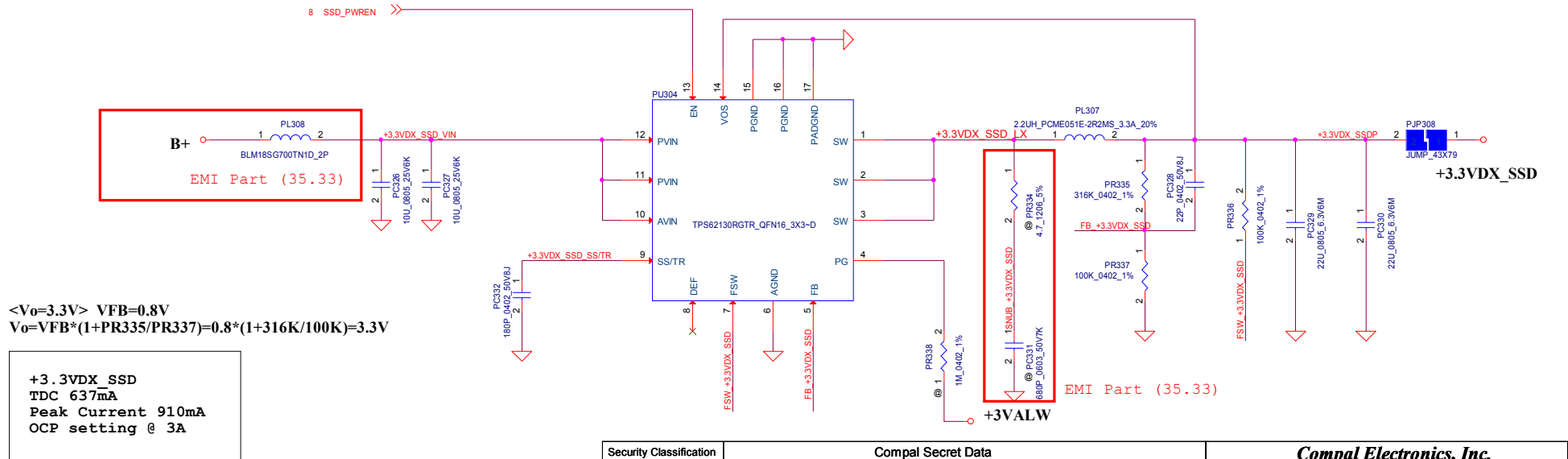
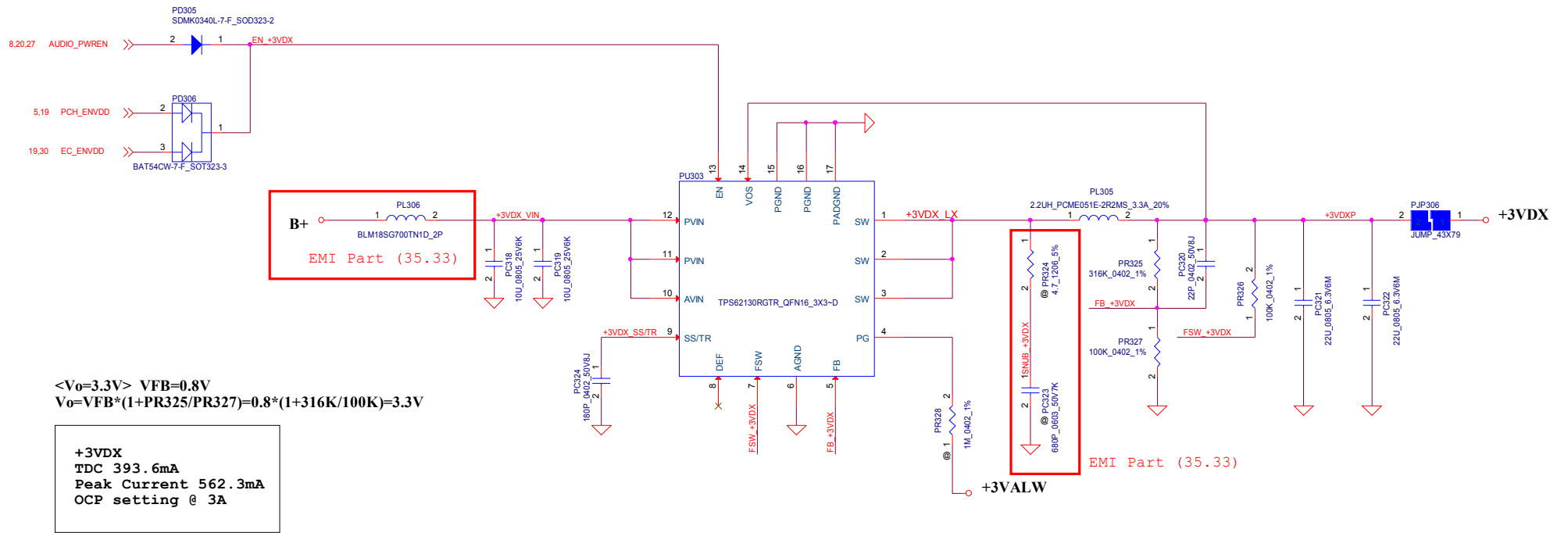
$\langle V_o=5V \rangle$ $V_{FB}=0.8V$
 $V_o = V_{FB} * (1 + PR315/PR317) = 0.8 * (1 + 806K/154K) = 5V$

+5V DX WALKPORT
 TDC 2.1A
 Peak Current 3A
 OCP setting @ 3A

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Issued Date				2011/06/02				Title			
				Deciphered Date				2013/10/28			
								Size			
								Document Number			
								LA-9262P			
								Date			
								Friday, April 19, 2013			
								Sheet			
								34 of 45			

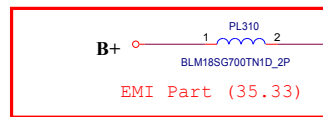
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P32-PWR +5V_VR
 Rev 1.0



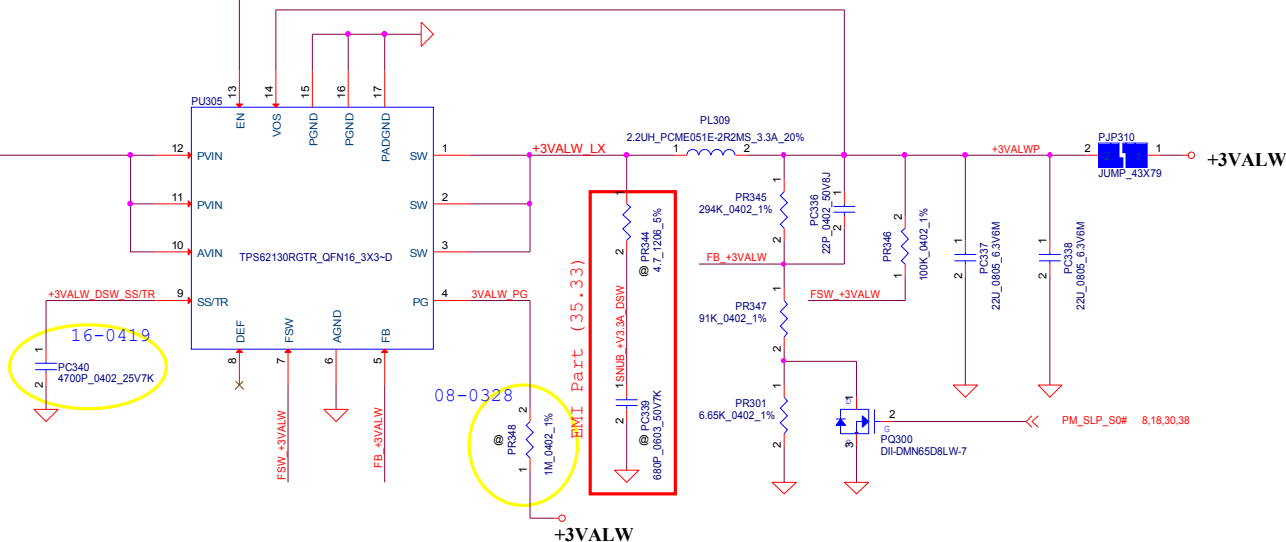
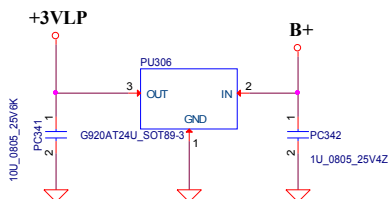
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/06/02				Title			
				Deciphered Date				P33-PWR +3.3V VR(1/2)			
								Size			
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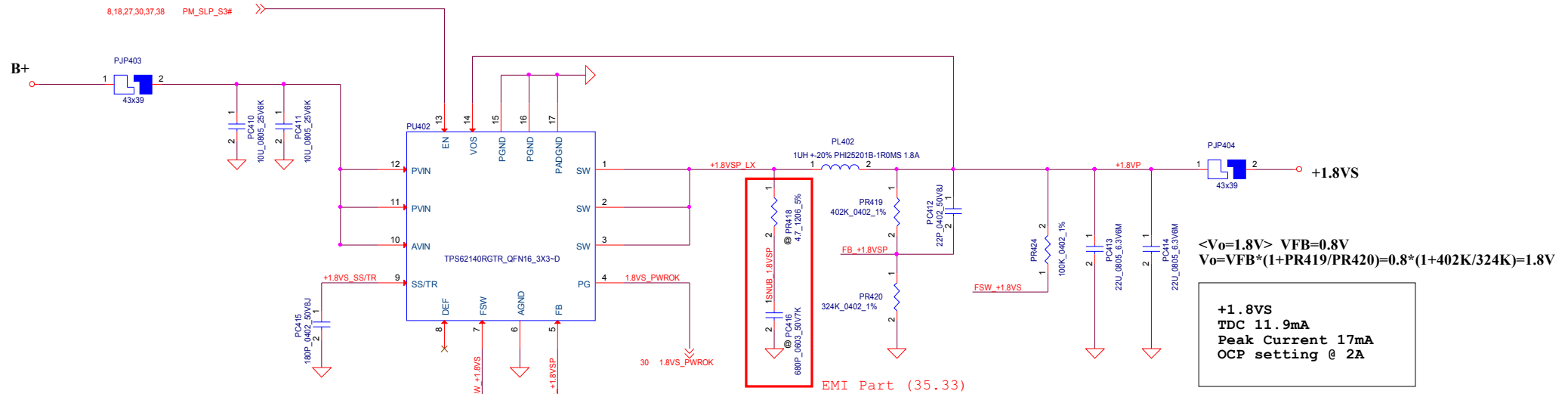
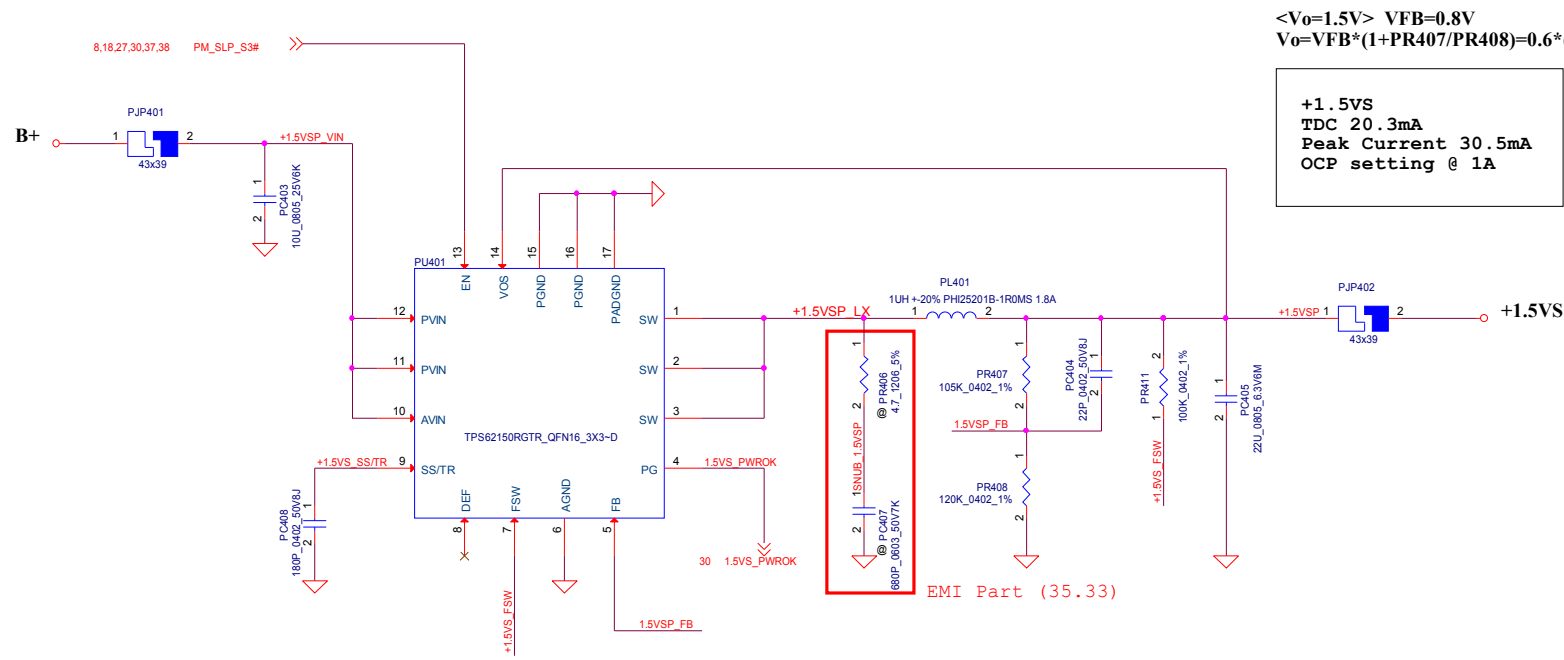


$\langle V_o = 3.3V \rangle$ $V_{FB} = 0.8V$
 $V_o = V_{FB} * (1 + PR345/PR347) = 0.8 * (1 + 316K/100K) = 3.3V$

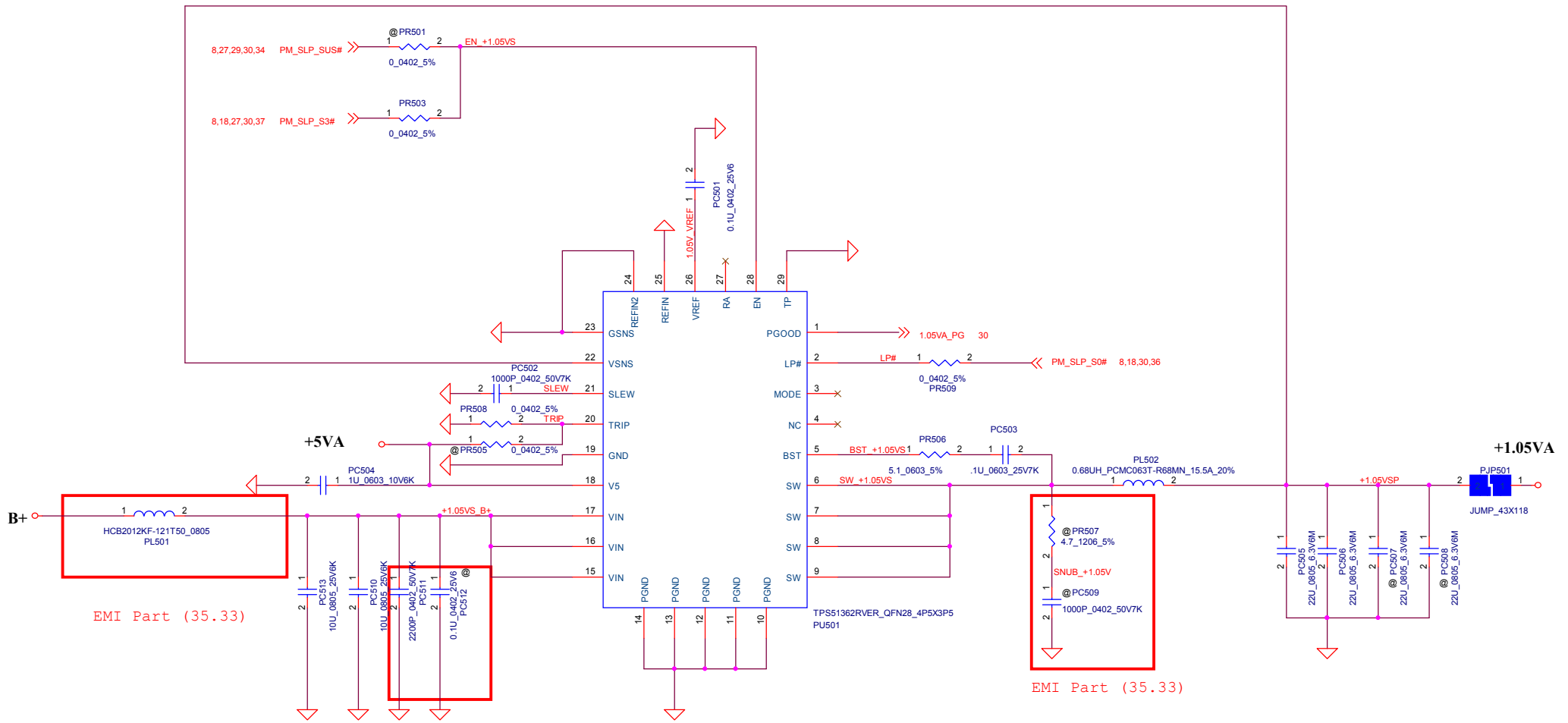
+3VALW
 TDC 161mA
 Peak Current 2301mA
 OCP setting @ 3A



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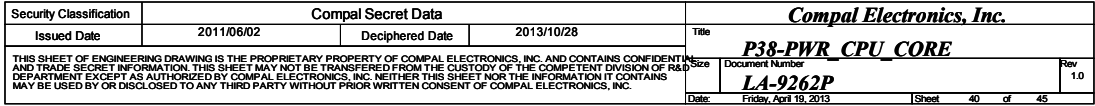


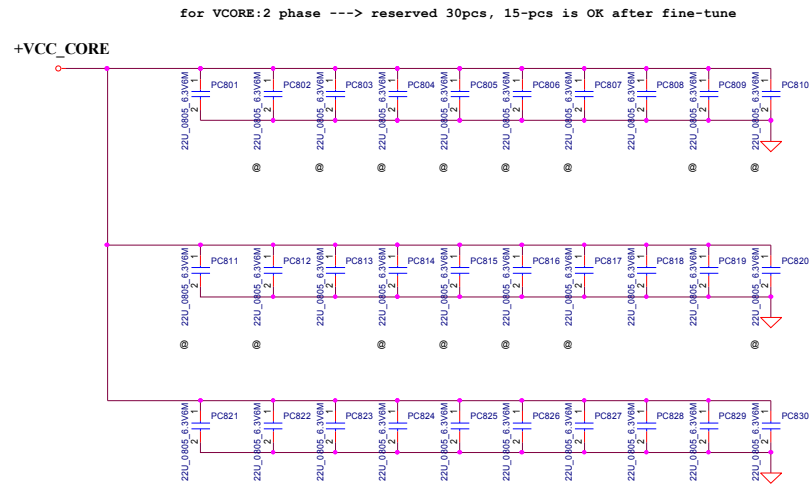
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+1.05VA
TDC 3754mA
Peak Current 3942mA
OCP setting @ 8A

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				P39-PWR PROCESSOR DECOUPLING	
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Item	Page#	Title	Date	Request Owner	Issue Description	Soluton Description	Rev.
X	XX	XXX	XX'XX/XX	Compal_XX	XXXXXX	Change PRXX from Xohm to XXKohm.	
36			20121008	Compal_Power	create one more input cap for TPS51362 Vin	add PC513_10U_0805_16V6K for TPS51362's input	
34			20121012	Compal_HW	create one more resistor for TPS62130 enable pin	add PR342_2.2K_0402_5%	
34			20121018	Compal_Power	design change, delete PU301~PU305, TPS62130 and related components, create PU301, TPS51225 for 3.3V and 5V power rails		
35							
36							
36			20121018	Compal_Power	design change, delete PU401, PU402, TPS62140 and TPS62150 and related components, create PU401and PU402, SY8003D for 1.5V and 1.8V power rails		
34			20121023	dell	reject power design change of 3.3V, 5V, 1.8V and 1.5V		
35							
36							
38			20121203	Compal_EMI	change PL501 for EMI and layout routing	change from SUPPRE_FBMA-L11-453215-800LMA90T_1812 to HCB2012KF-121T50_0805	
39			20121203	Compal_EMI	change PL601 for EMI and layout routing	change from SUPPRE_FBMA-L11-453215-800LMA90T_1812 to HCB2012KF-121T50_0805	
40			20121203	Compal_EMI	add PL703 for EMI	add PL701 HCB2012KF-121T50_0805	
38			20121203	Compal_Power	create PR509 0_0402_5% for debug	add PR509 0_0402_5%	
32			20121205	Compal_HW	create PR5107 10K_0402_1% for test	add PR107 10K_0402_1%	
40			20121213	Compal_Power	fine tune VR transient	de-pop PC714, change PR711 from 150K to be 100K	
40			20130122	Compal_Power	follow Intel's recommendation	change PR737 from 110 OHM to be 130 OHM	
33			20130131	Compal_RF	reserved a MLCC for RF consideration	create PC206 2200P_0402_50V7K	
40			20130221	Compal_RF	for RF noise reducing	pop PC703, PR719 and PC712, PR734 and PC722 for VCORE	
39			20130221	Compal_RF	for RF noise reducing	pop PR605 and PC613 for DDR	

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