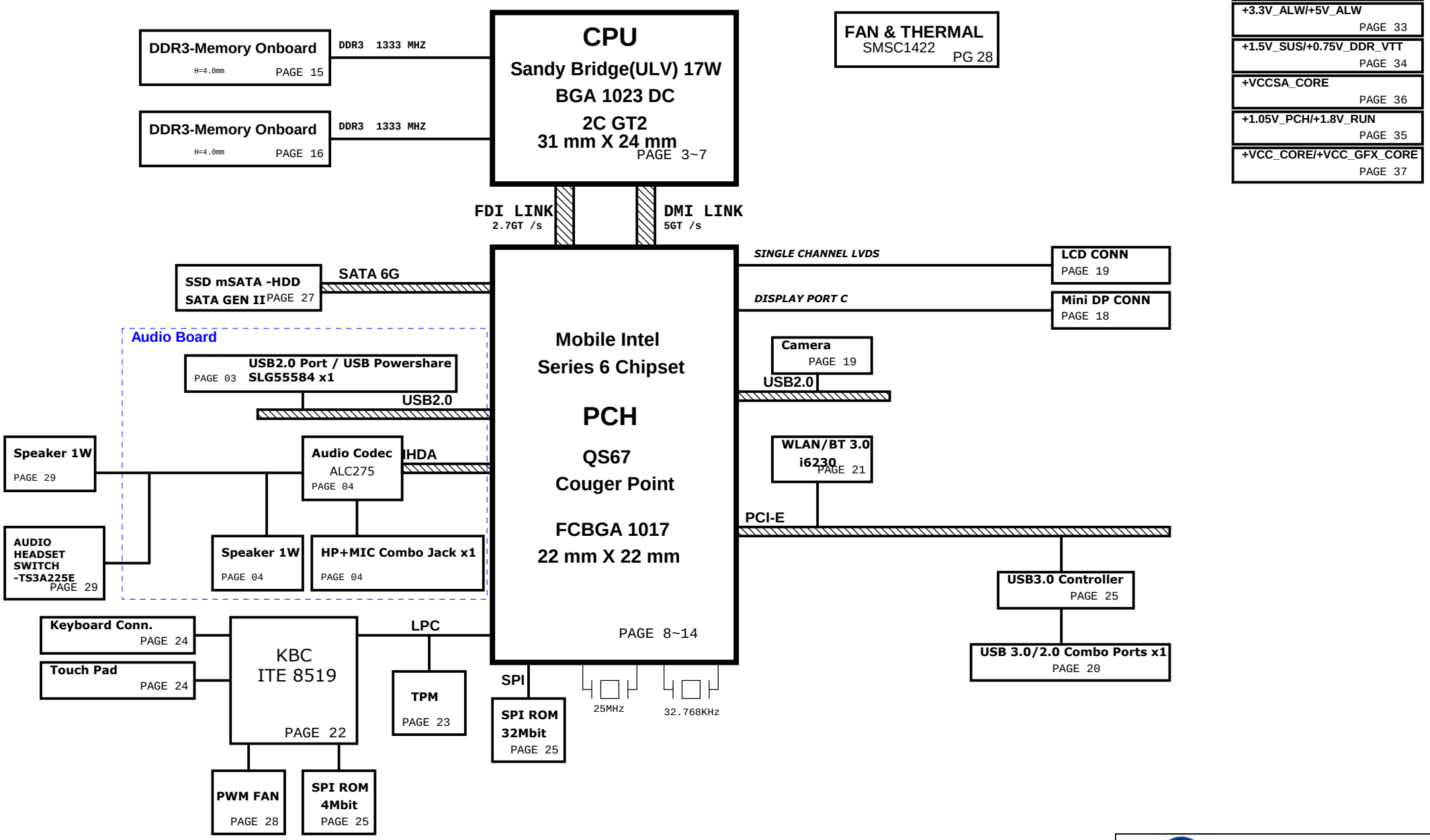
Spyder 13.3" UMA BLOCK DIAGRAM



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Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Thursday, October 13, 2011 Sheet 1 of 41

power / State	SLP_S3#	SLP_S4#	SLP_S5#	ALW_ON	+3.3V_ALW	+5V_ALW	SUS_ON	+3.3V_SUS	+5V_SUS	RUN_ON	+3.3V_RUN	+5V_RUN	AOAC flag	USB2.0 Power share USB_BAK_EN#
S0	H	H	H	H	H	H	H	H	H	H	H	H	L	L
S3	L	H	H	H	H	H	H	H	H	L	L	L	L	L
S4/S5 AC	L	L	L	H	H	H	L	L	L	L	L	L	L	L
S4/S5 DC Only	L	L	L	L	L	L	L	L	L	L	L	L	L	L
AC/DC No Exist	L	L	L	L	L	L	L	L	L	L	L	L	L	L
AOAC(S4)	L	L	L	H	H	H	H	H	H	L	L	L	H	H

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Size	Document Number	Rev
	Power Rails	1A

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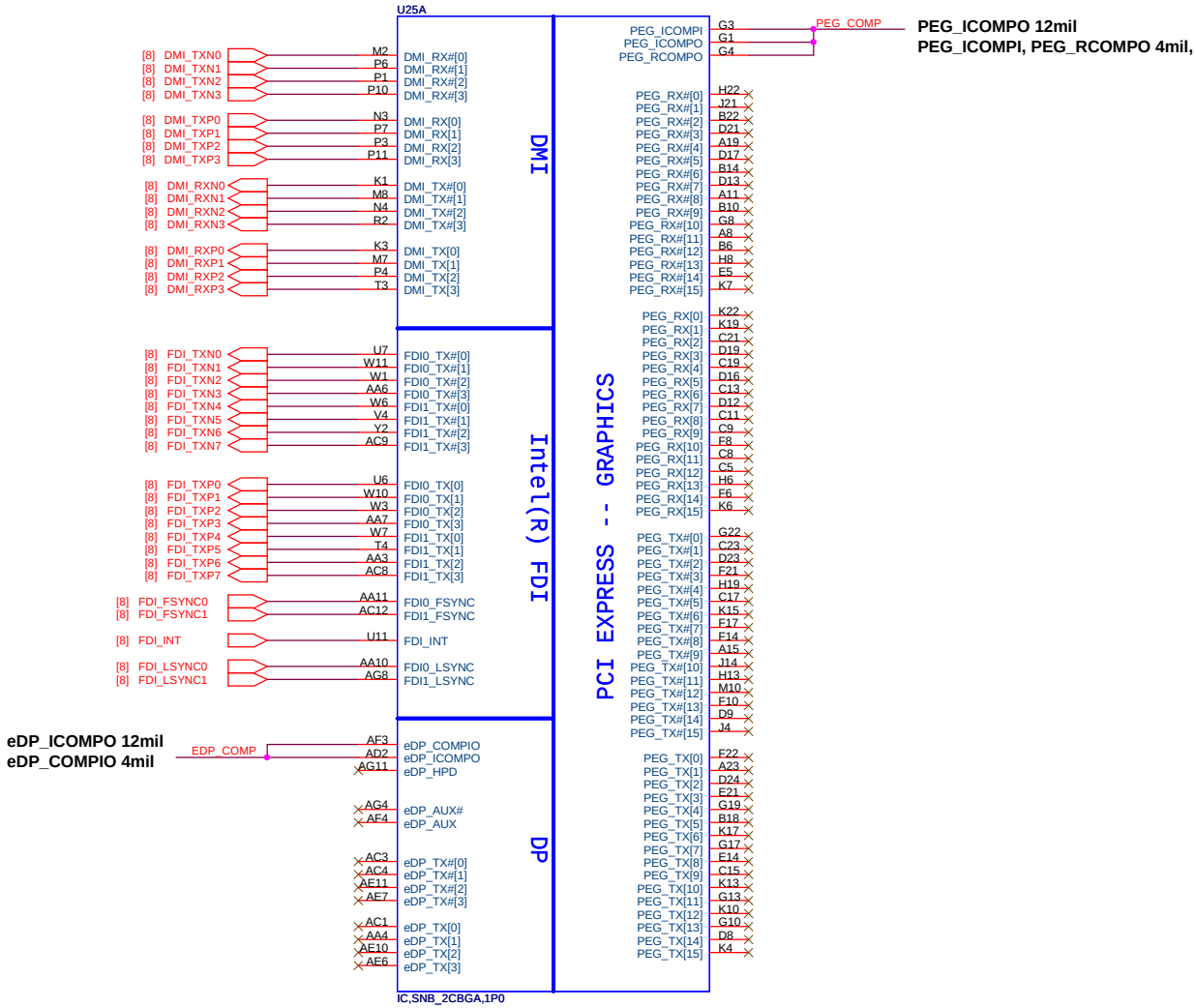
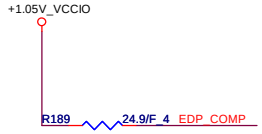
Sandy Bridge Processor (DMI,PEG,FDI)

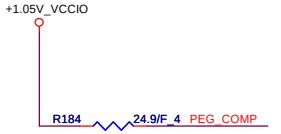
CPU is i7 in schematic



DP & PEG Compensation



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

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Size	Document Number	Rev
	Sandy Bridge 1/5	1A

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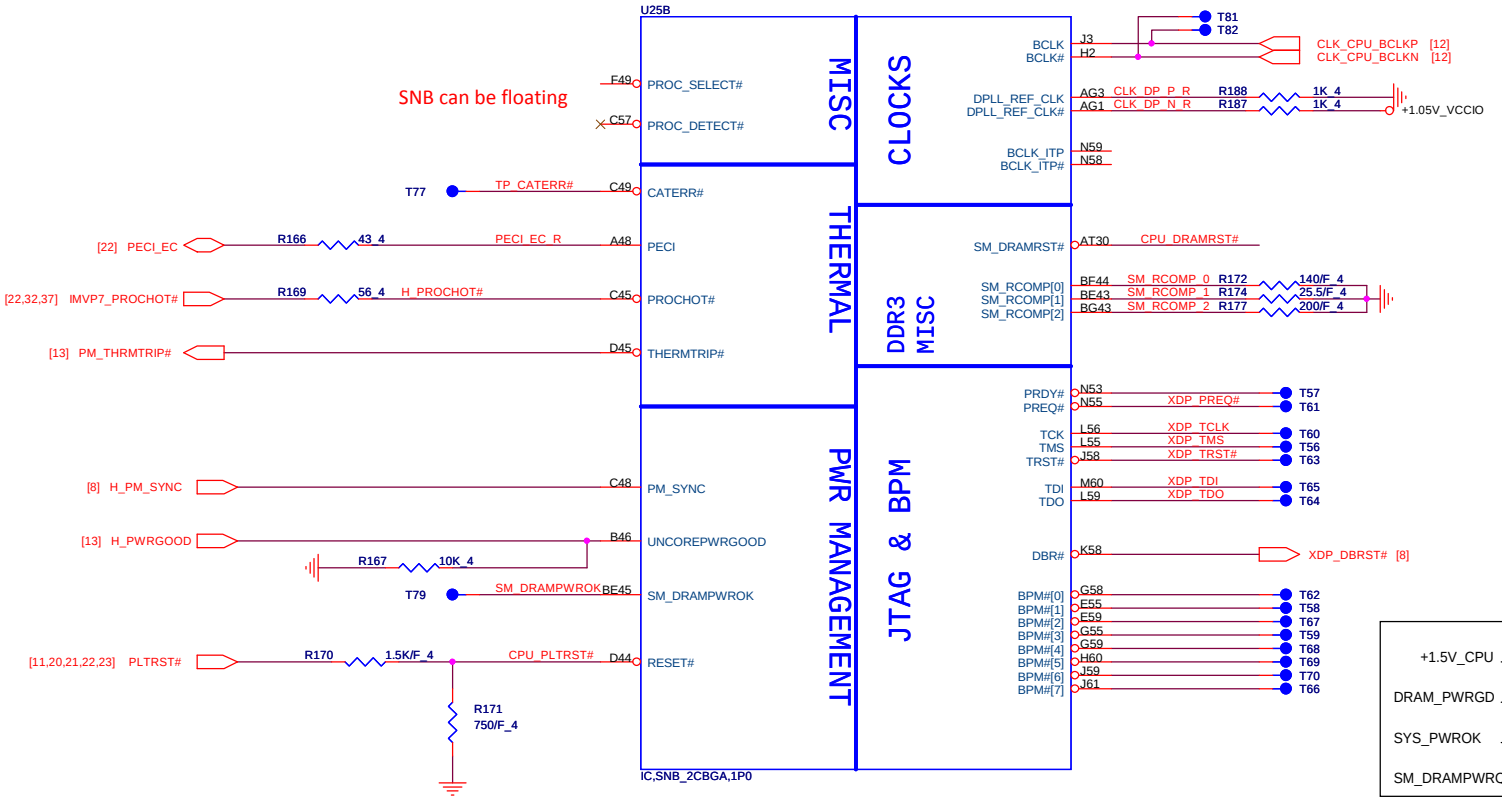
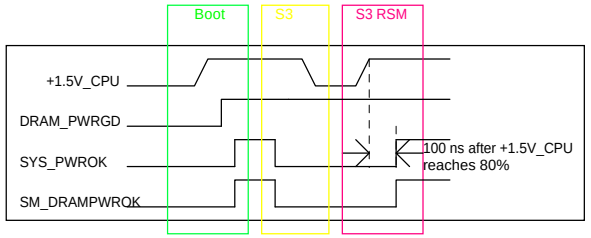
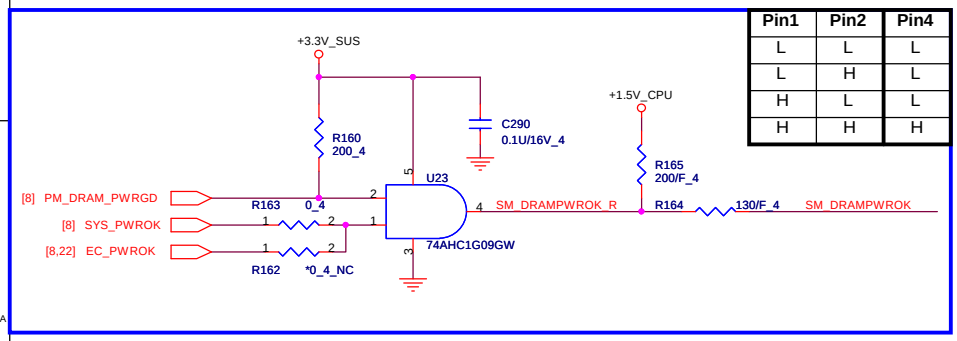
Sandy Bridge Processor (CLK,MISC,JTAG)

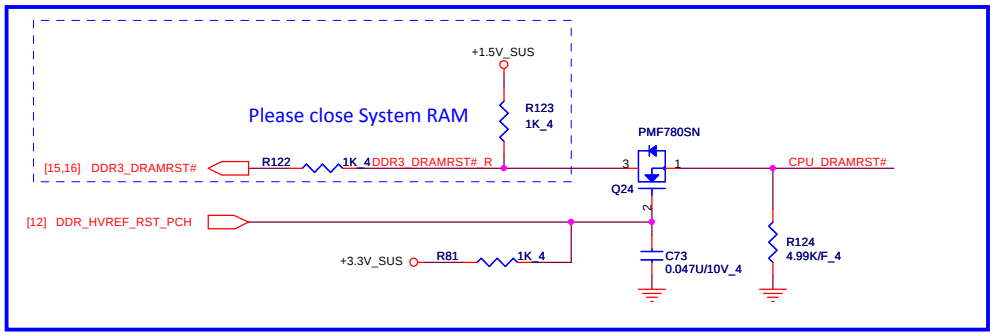
CPU is i7 in schematic







Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	H



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Size	Document Number	Rev
	Sandy Bridge 2/5	1A

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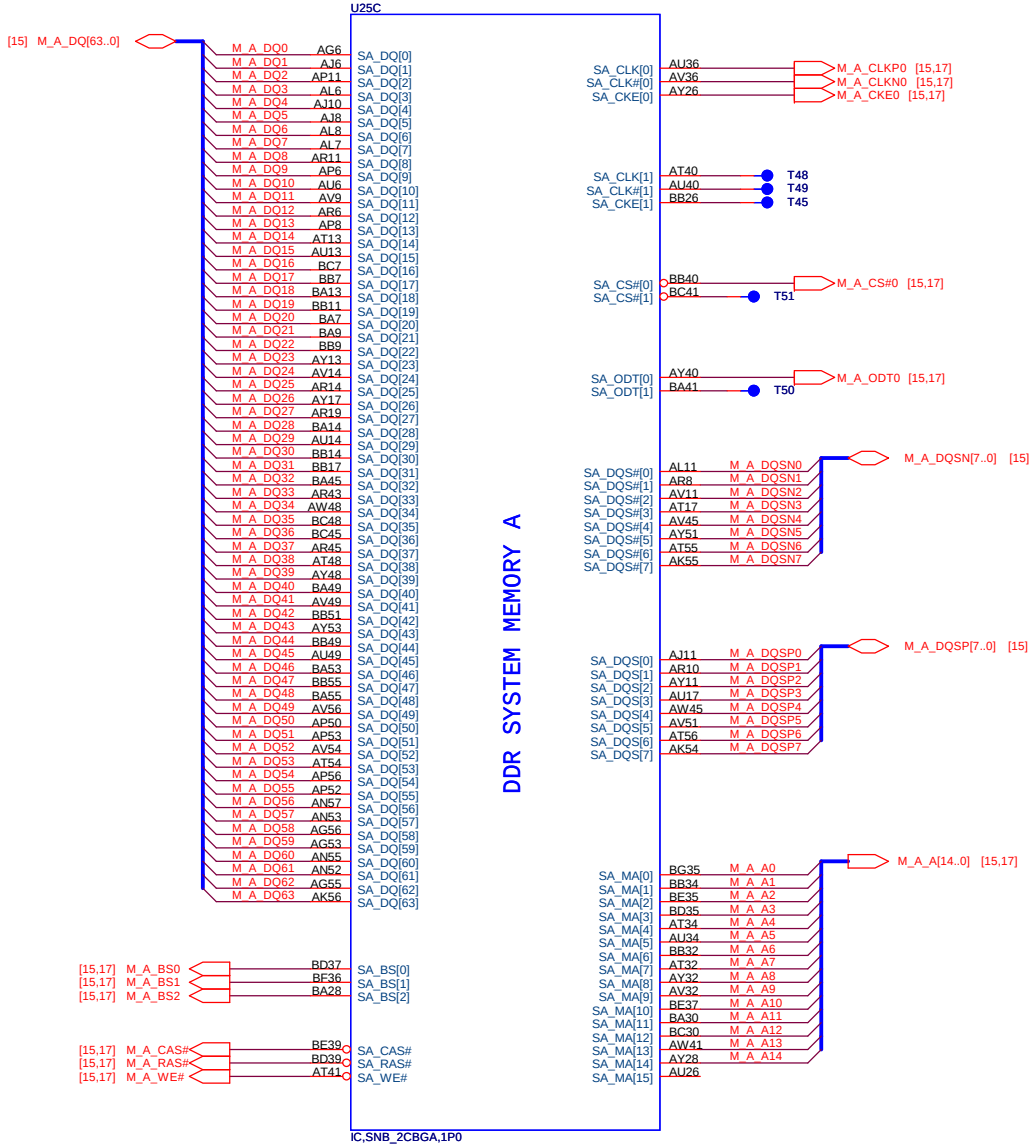
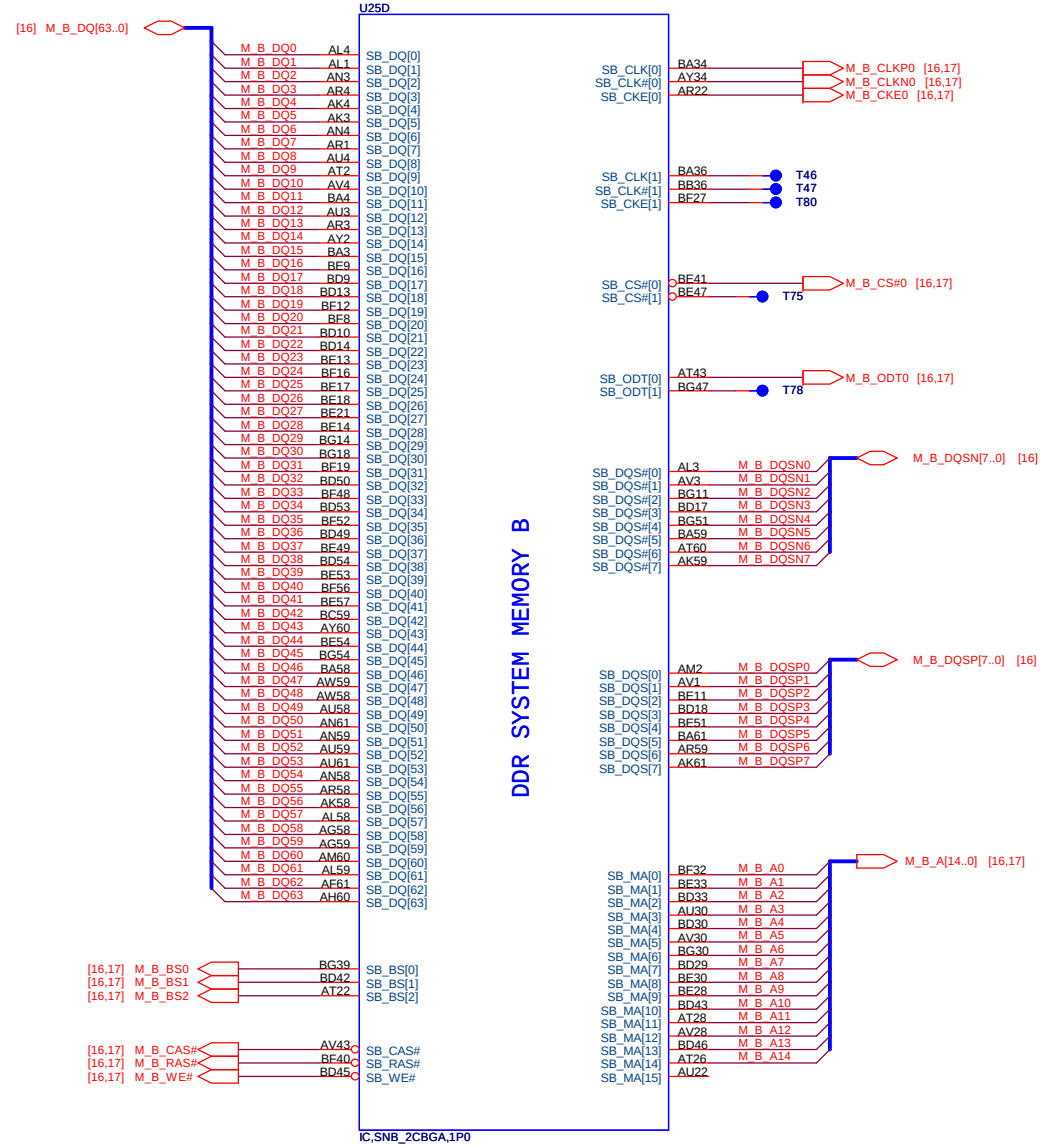
Sandy Bridge Processor (DDR3)

CPU is i7 in schematic





[15] M_A_DQ[0..7] — [15] M_A_DQ[32..39]

[15] M_A_DQ[8..15] — [15] M_A_DQ[40..47]

[15] M_A_DQ[16..23] — [15] M_A_DQ[48..55]

[15] M_A_DQ[24..31] — [15] M_A_DQ[56..63]

[16] M_B_DQ[0..7] — [16] M_B_DQ[32..39]

[16] M_B_DQ[8..15] — [16] M_B_DQ[40..47]

[16] M_B_DQ[16..23] — [16] M_B_DQ[48..55]

[16] M_B_DQ[24..31] — [16] M_B_DQ[56..63]

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Sandy Bridge Processor (POWER)

CPU is i7 in schematic

U25F

SNB:33A

+VCC_CORE

CORE SUPPLY

POWER

PEG AND DDR

8.5A

+1.05V_VCCIO

QUIET RAILS

SVID

SENSE LINES

Follow check list of Intel

IC,SNB_2CBGA,1P0

Sandy Bridge Processor (GRAPHIC POWER)

CPU is i7 in schematic

U25G

18A

+VCC_GFX_CORE

POWER

GRAPHICS

DDR3 - 1.5V RAILS

SENSE LINES

1.8V RAIL

QUIET RAILS

SA RAIL

3A

+1.8V_RUN

SNB:6A

+VCCSA_CORE

10mil

SM_VREF

+VDDR_REF_CPU

SNB:5A

+1.5V_CPU

+1.5V_SUS

5A

Q26
AON7410

check with power Andy

[8] PS_S3CNTRL_S

C241
*4700P/25V/X7R_4_NC

Follow check list of Intel

Sandy Bridge only:
VCCSA_VID[0] should be pull down
VCCSA_VID[1] should connect to SA VR

08/11
For CPU cost down plan
C151, C150

IC,SNB_2CBGA,1P0

SVID DATA

Place resistor R55 close to CPU

SVID ALERT

Place resistor R175 close to CPU

Follow check list of Intel

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	Sandy Bridge 4/5	1A

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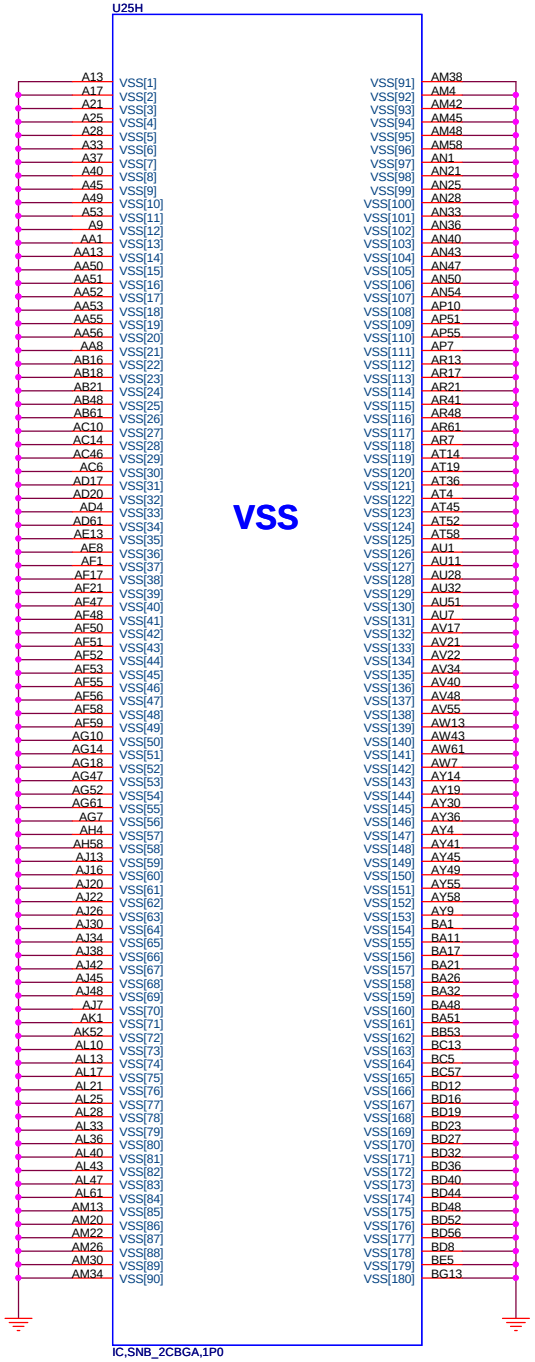
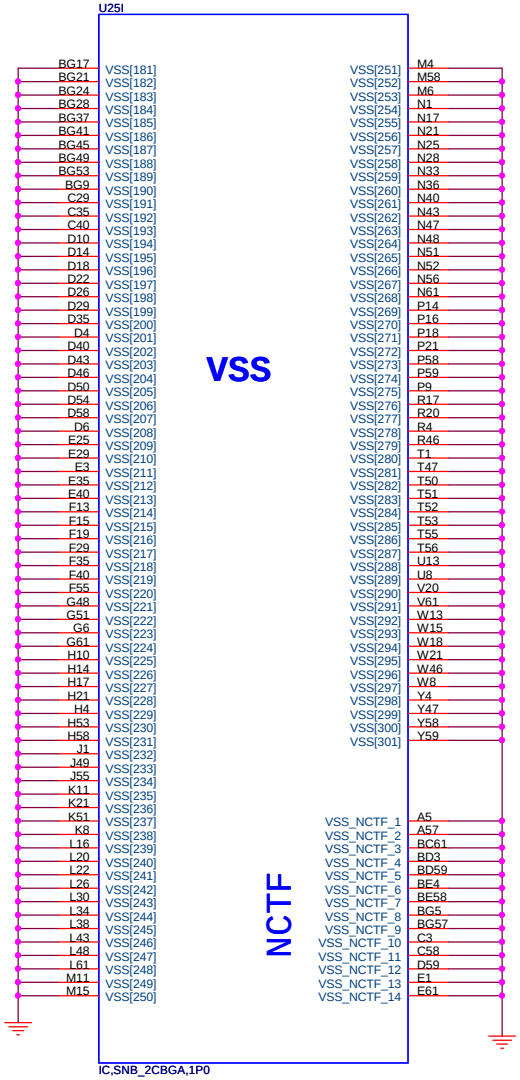
Sandy Bridge Processor (GND)

CPU is i7 in schematic

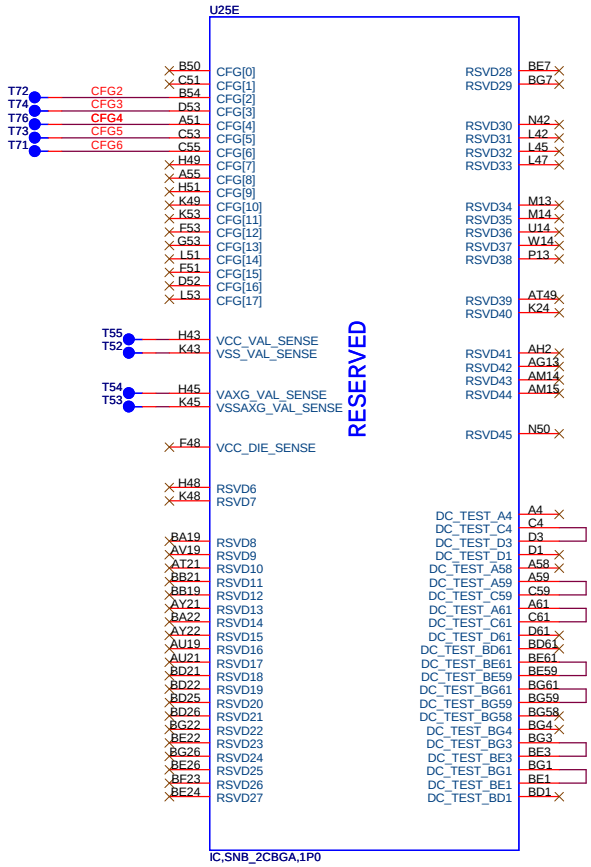


CPU is i7 in schematic



Sandy Bridge Processor (RESERVED, CFG)

CPU is i7 in schematic



PGB straping pin unused for UMA only

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

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	Sandy Bridge 5/5	1A

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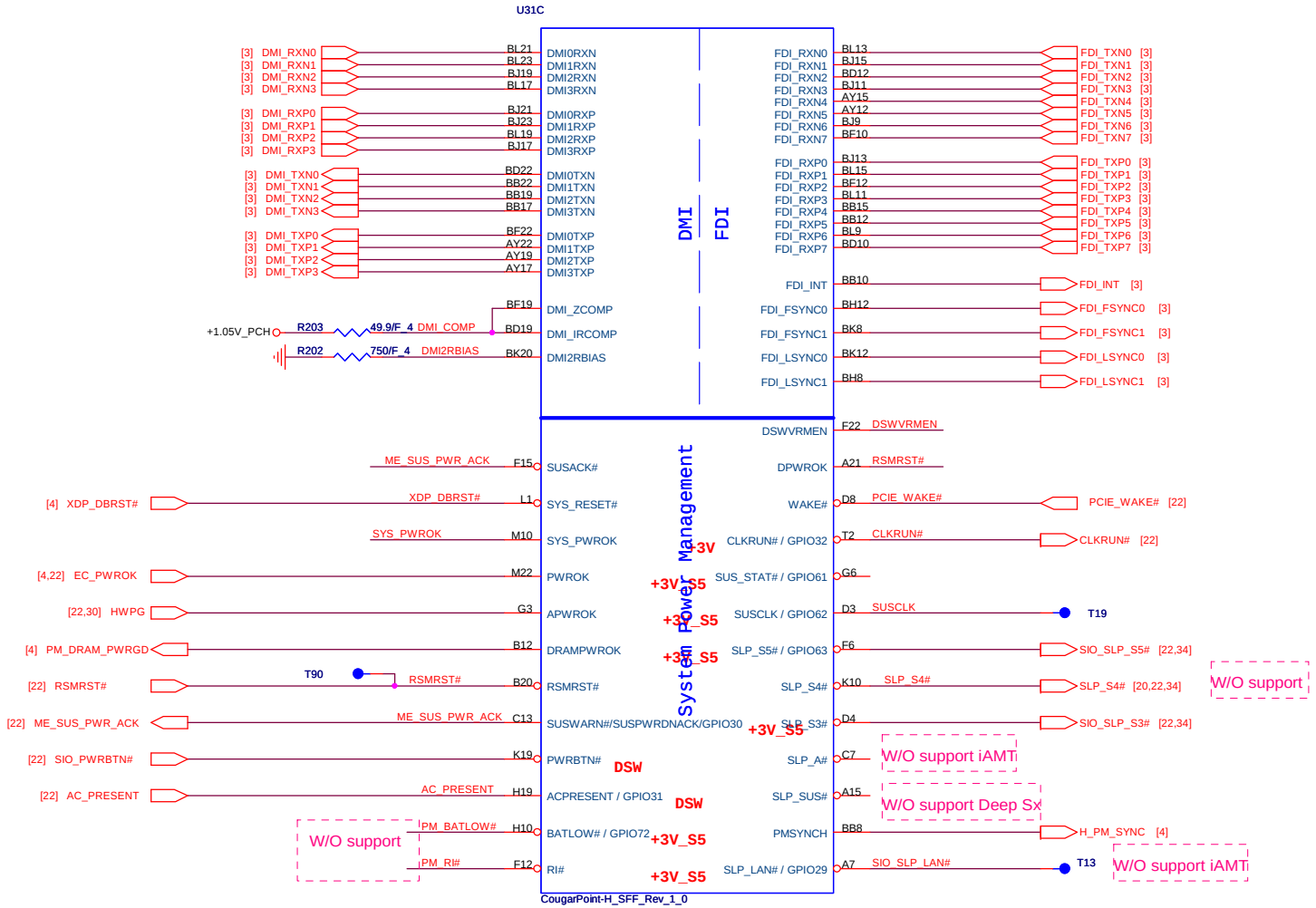
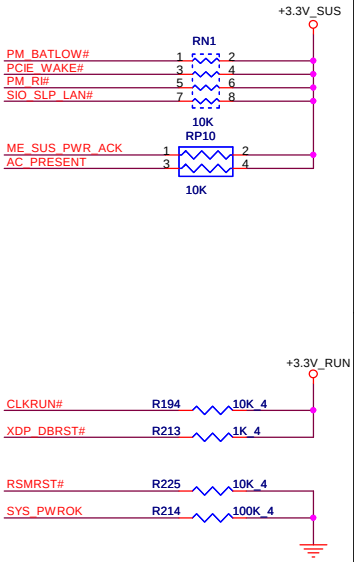
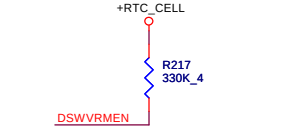
Cougar Point (DMI,FDI,PM)



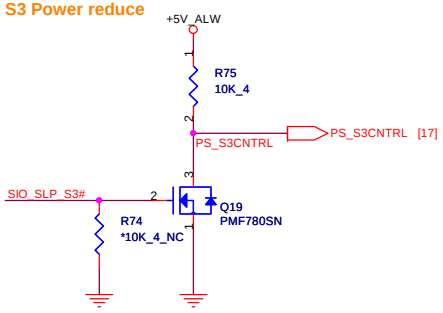
PCH Pull-high/low(CLG)





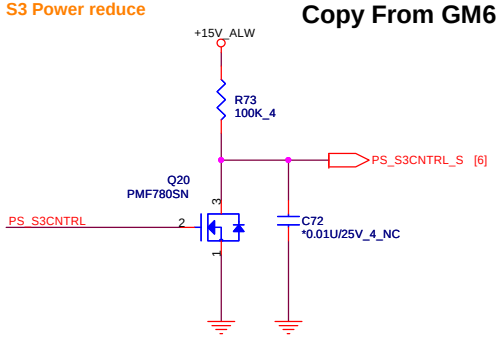
On Die DSW VR Enable
High = Enable (Default)
Low = Disable

S3 Power reduce

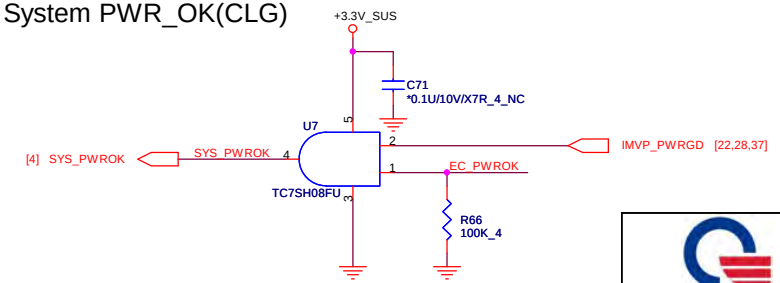


S3 Power reduce

Copy From GM6



System PWR_OK(CLG)



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	Cougar Point 1/7	1A
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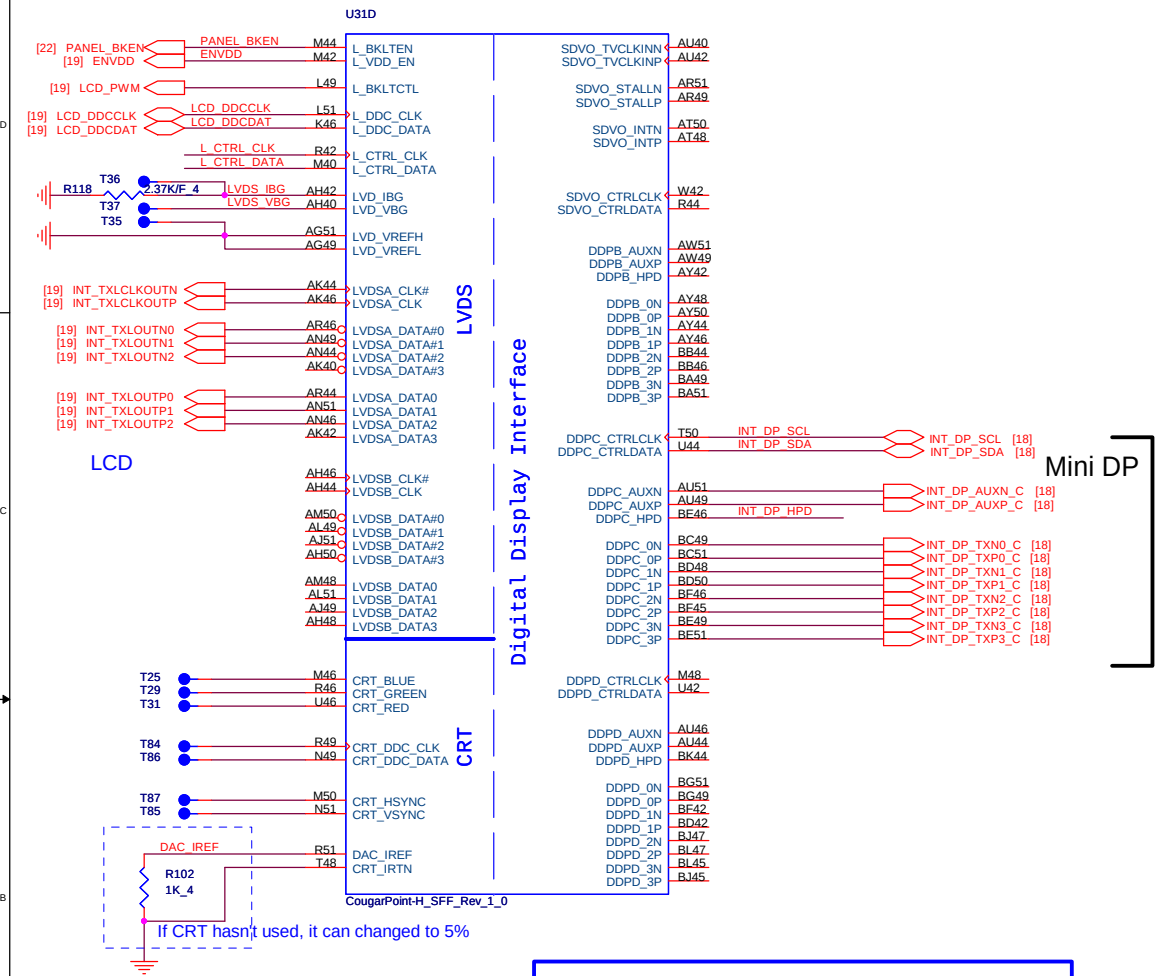
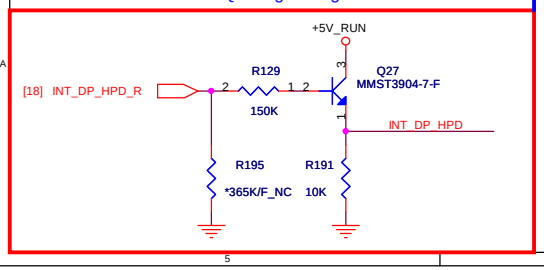
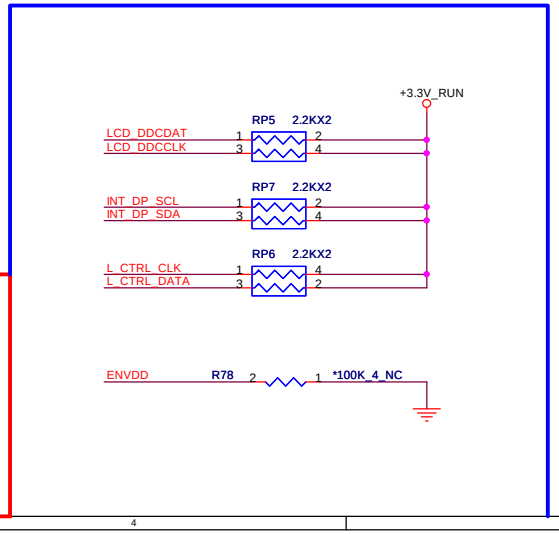
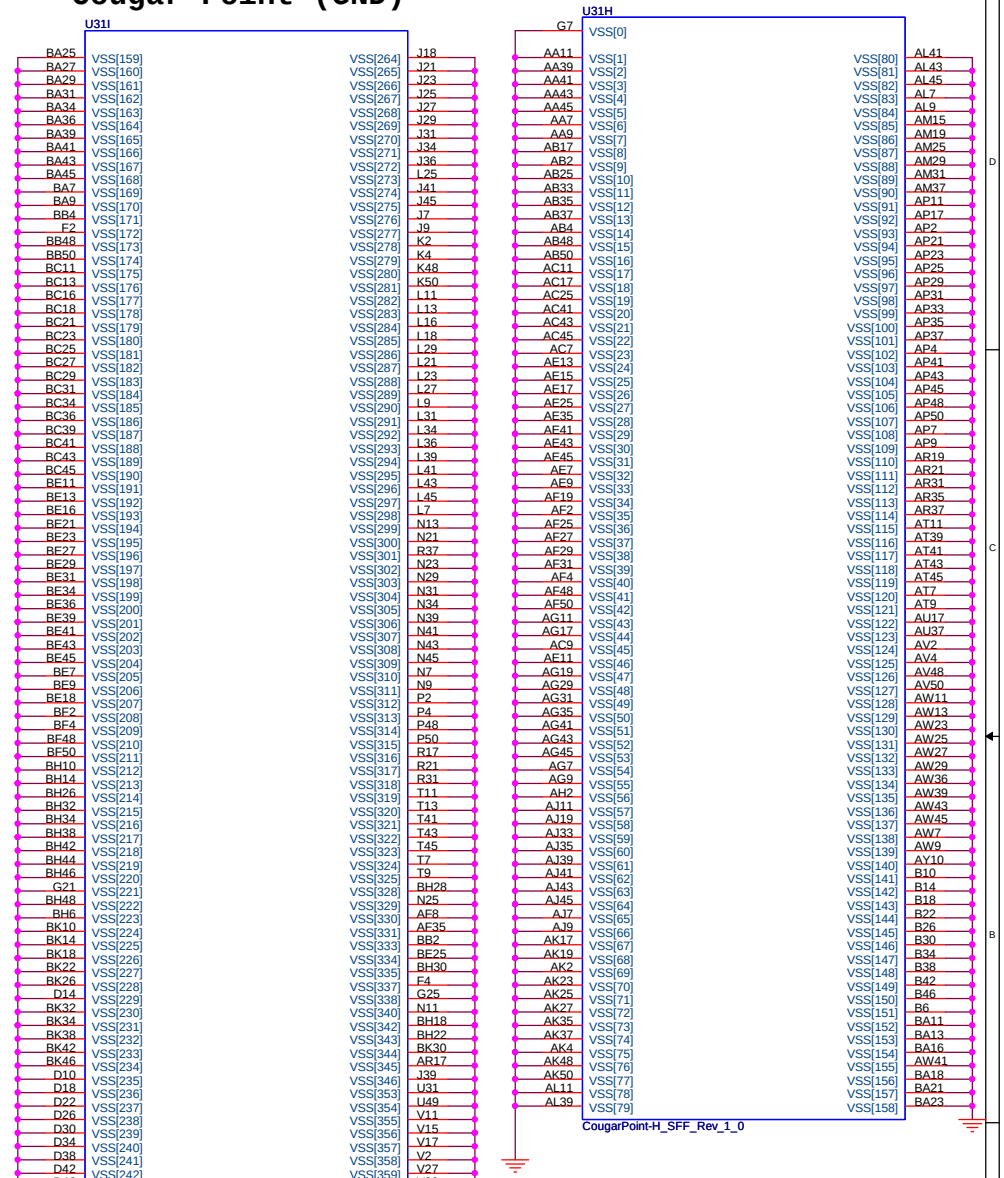
Cougar Point (LVDS,DDI)







Cougar Point (GND)



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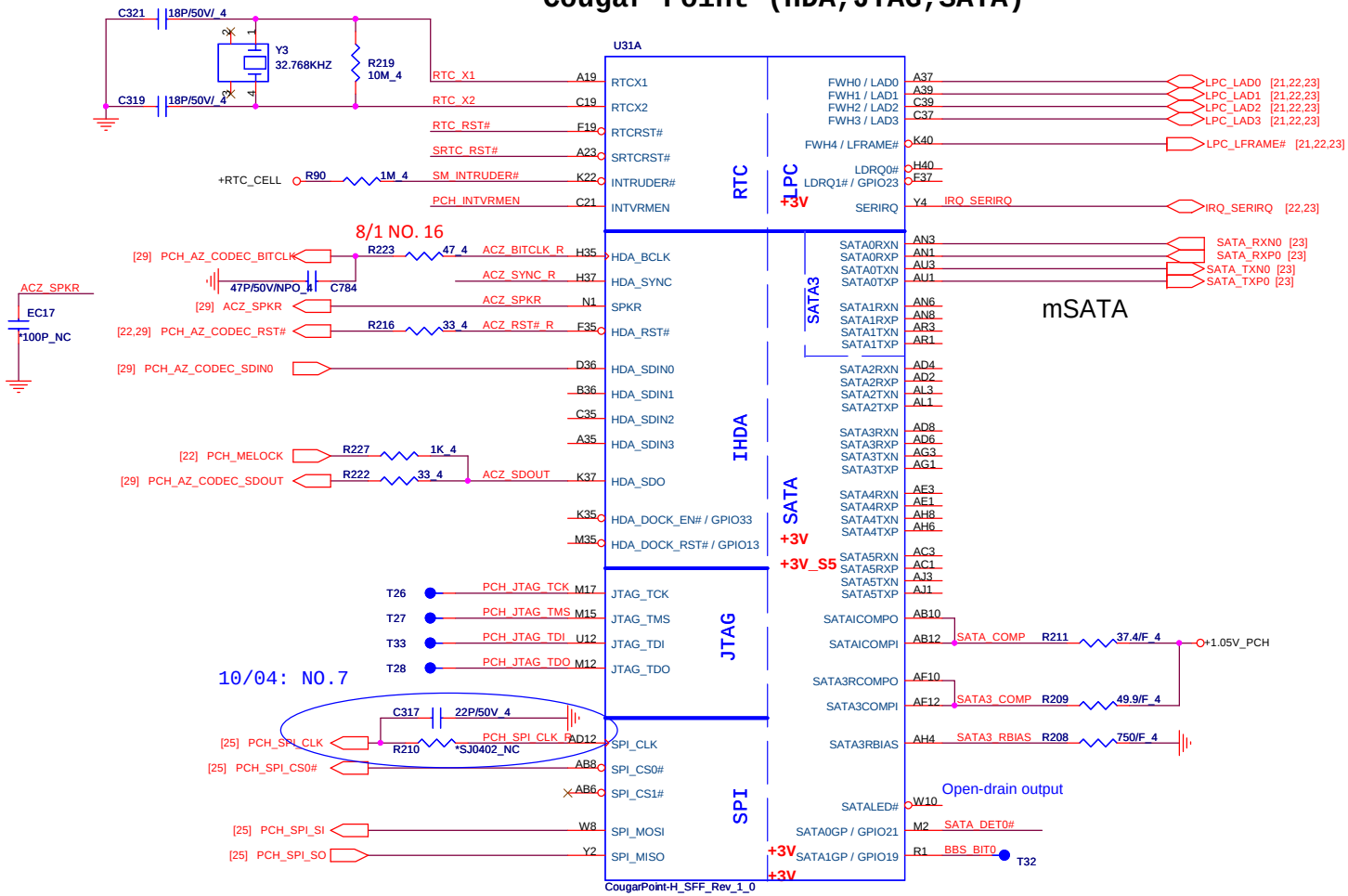
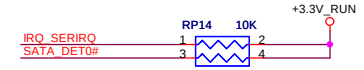
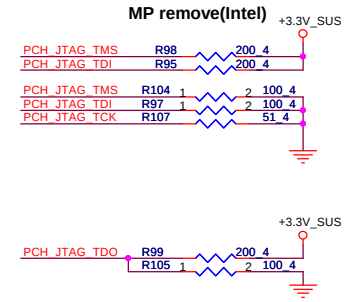
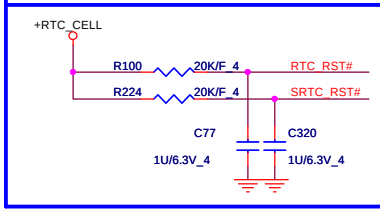
Cougar Point (HDA,JTAG,SATA)





PCH JTAG Debug (CLG)





PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	
Del 0510			**Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91**	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+RTC_CELL R96 330K_4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	[29] PCH_AZ_CODEC_SYNC R85 33_4 ACZ_SYNC_R 1K_4 R89 +3.3V_SUS

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	Cougar Point 3/7	1A
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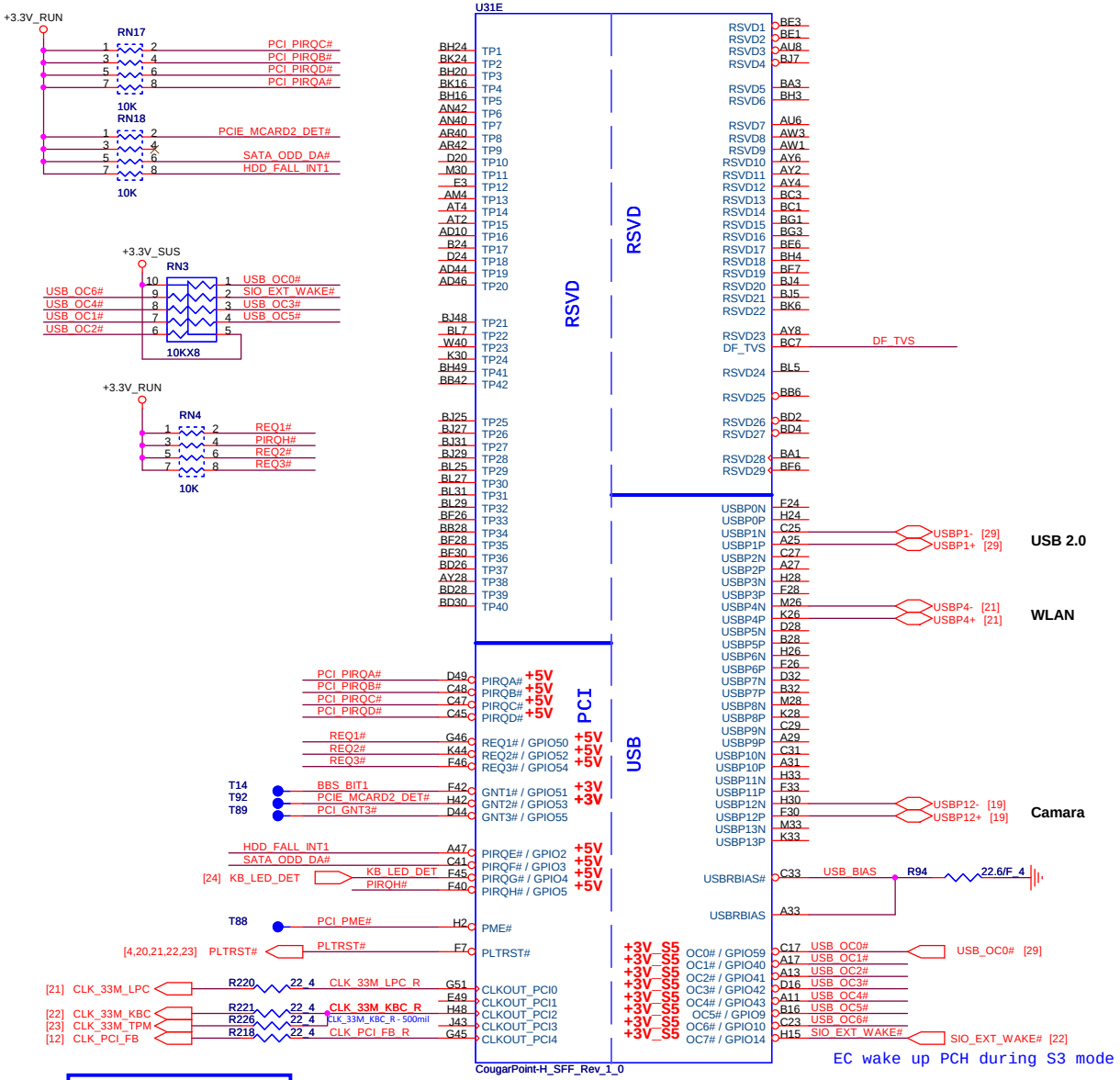
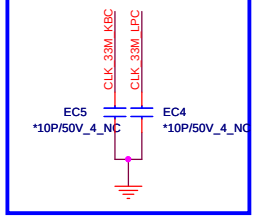
Cougar Point-M (PCI,USB,NVRAM)

PCI/USBOC# Pull-up(CLG)



Add EMC solution



Pin Name	Strap description	Sampled	Configuration
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 10K)
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 10K)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Bit 0 / Bit 1 / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
			Default weak pull-up on GNT0/1# (Internal PU)
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm

R196 2 2.2K_4 +1.8V_RUN
DF_TVS

CheckList_1.5 p72; HR_v1.5 p476

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	Cougar Point 4/7	1A
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Cougar Point-M (PCI-E,SMBUS,CLK)

U31B

For BIOS:
drop the PCH_SMB_ALERT from touchpad due to SMBUS will control it by host notify mechanism

PCI-E*

WLAN
[21] PCIE_RXN2 → BJ33 PERN1
[21] PCIE_RXP2 → BL33 PERP1
[21] PCIE_TXN2 → C313 0.1U/16V_4 → PCIE_TXN2_C → BB33 PETN1
[21] PCIE_TXP2 → C314 0.1U/16V_4 → PCIE_TXP2_C → AY33 PETP1

BJ35 PERN2
BL35 PERP2
BB30 PETN2
AY30 PETP2

BH36 PERN3
BK36 PERP3
BF33 PETN3
BD33 PETP3

USB3.0
[20] PCIE_RXN4 → BJ37 PERN4
[20] PCIE_RXP4 → BL37 PERP4
[20] PCIE_TXN4 → C312 0.1U/16V_4 → PCIE_TXN4_C → BD35 PETN4
[20] PCIE_TXP4 → C311 0.1U/16V_4 → PCIE_TXP4_C → BF35 PETP4

BJ39 PERN5
BL39 PERP5
AY35 PETN5
BB35 PETP5

BH40 PERN6
BK40 PERP6
BD37 PETN6
BF37 PETP6

BJ41 PERN7
BL41 PERP7
AY37 PETN7
BB37 PETP7

BJ43 PERN8
BL43 PERP8
AY40 PETN8
BB40 PETP8

SMBUS

+3V_S5 SMBALERT# / GPIO11 H12 PCH_SMB_ALERT# T15
SMBCLK F17 SMBCLK
SMBDATA F10 SMBDATA

+3V_S5 SML0ALERT# / GPIO60 H22 DDR_HVREF_RST_PCH [4]
SML0CLK K12 SML0CLK
SML0DATA A9 SML0DATA

+3V_S5 SML1ALERT# / PCHHOT# / GPIO74 C9 PCH_GPIO74
+3V_S5 SML1CLK / GPIO58 D12 SMB_CLK_ME1
+3V_S5 SML1DATA / GPIO75 C11 SMB_DATA_ME1

Controller Link

CL_CLK1 L3
CL_DATA1 J1
CL_RST1# M8

CLOCKS

+3V_S5 PEG_A_CLKRQ# / GPIO47 R8 PEG_CLKREQ_GPU#

AD48 CLKOUT_PCIE0N
AD50 CLKOUT_PCIE0P
PCIE_CLK_REQ0# M4 PCIECLKRQ0# / GPIO73 +3V_S5

CLKOUT_PEG_A_N AF44
CLKOUT_PEG_A_P AF46

WLAN
[21] CLK_PCIE_WLANN → AE49 CLKOUT_PCIE1N
[21] CLK_PCIE_WLANP → AE51 CLKOUT_PCIE1P
[21] PCIE_CLK_REQ1# → PCIE_CLK_REQ1# U8 PCIECLKRQ1# / GPIO18 +3V

CLKOUT_DMI_N BB24 → CLK_CPU_BCLKN [4]
CLKOUT_DMI_P AY24 → CLK_CPU_BCLKP [4]

CLKOUT_DP_N AN10
CLKOUT_DP_P AN12

AD40 CLKOUT_PCIE2N
AD42 CLKOUT_PCIE2P
PCIE_CLK_REQ2# T4 PCIECLKRQ2# / GPIO20 +3V

CLKIN_DMI_N BD17 CLK_DMIN → R199 10K_4
CLKIN_DMI_P BF17

CLKIN_GND1_N BB26 CLK_GND1 → R198 10K_4
CLKIN_GND1_P AY26

AA49 CLKOUT_PCIE3N
AA51 CLKOUT_PCIE3P
PCIE_CLK_REQ3# B8 PCIECLKRQ3# / GPIO25 +3V_S5

CLKIN_DOT_96N M24 CLK_BUF_DREFCLK → R93 10K_4
CLKIN_DOT_96P K24

USB3.0
[20] CLK_PCIE_USB30N → Y48 CLKOUT_PCIE4N
[20] CLK_PCIE_USB30P → Y50 CLKOUT_PCIE4P
[20] PCIE_CLK_REQ4# → PCIE_CLK_REQ4# M19 PCIECLKRQ4# / GPIO26 +3V_S5

CLKIN_SATA_N AK8 CLK_BUF_DREFSSCLK → R207 10K_4
CLKIN_SATA_P AK6

REFCLK14IN J49 CLK_PCH_14M → R106 10K_4

AB40 CLKOUT_PCIE5N
AB42 CLKOUT_PCIE5P
PCIE_CLK_REQ5# K8 PCIECLKRQ5# / GPIO44 +3V_S5

CLKIN_PCILOOPBACK E51 CLK_PCI_FB → CLK_PCI_FB [11]

AF40 CLKOUT_PEG_B_N
AF42 CLKOUT_PEG_B_P
PEG_B_CLKRQ# C4 PEG_B_CLKRQ# / GPIO56 +3V_S5

XTAL25_IN W49 XTAL25_IN
XTAL25_OUT W51 XTAL25_OUT
R113 1M_4
Y2 25MHz
C102 12P/50V_4
C84 12P/50V_4

AB44 CLKOUT_PCIE6N
AB46 CLKOUT_PCIE6P
PCIE_CLK_REQ6# J3 PCIECLKRQ6# / GPIO45 +3V_S5

XCLK_RCOMP AC49 XCLK_RCOMP R117 90.9/F_4 +1.05V_PCH

W44 CLKOUT_PCIE7N
W46 CLKOUT_PCIE7P
PCIE_CLK_REQ7# H4 PCIECLKRQ7# / GPIO46 +3V_S5

AR12 CLKOUT_ITPXDP_N
AR10 CLKOUT_ITPXDP_P

FLEXCLOCKS

+3V CLKOUTFLEX0 / GPIO64 H50 CLK_FLEX0 T22
+3V CLKOUTFLEX1 / GPIO65 D48 CLK_FLEX1 T20
+3V CLKOUTFLEX2 / GPIO66 G49 CLK_FLEX2 T21
+3V CLKOUTFLEX3 / GPIO67 J51 CLK_FLEX3 T24

CougarPoint-H_SFF_Rev_1_0

SMBus/Pull-up(CLG)

+3.3V_RUN
RP4 2.2KX2
Q21A DMN66D0LDW-7
SMBCLK → TP_SCLK [24]
Q21B DMN66D0LDW-7
SMBDATA → TP_SDATA [24]

+3.3V_SUS
Q22A DMN66D0LDW-7
SMB_CLK_ME1 → SMBCLK1 [22]
Q22B DMN66D0LDW-7
SMB_DATA_ME1 → SMBDAT1 [22]

CLK_REQ/Strap Pin(CLG)

+3.3V_SUS
RN2 10K
PCIE_CLK_REQ0#
PCIE_CLK_REQ3#
PCIE_CLK_REQ4#
PCIE_CLK_REQ5#
PEG_B_CLKRQ# R77 10K_4
PCIE_CLK_REQ6#
PCIE_CLK_REQ7#
RP11 10K

+3.3V_RUN
PCIE_CLK_REQ1#
PCIE_CLK_REQ2#
RP15 10K
+3.3V_SUS
PEG_CLKREQ_GPU# R92 10K_4

+3.3V_SUS
RP13 10K
PCH_GPIO74
PCH_SMB_ALERT#
RP8 2.2KX2
SMBCLK
SMBDATA
RP12 2.2KX2
SML0CLK
SML0DATA
RP9 2.2KX2
SMB_DATA_ME1
SMB_CLK_ME1

Quanta Computer Inc.
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	Cougar Point 5/7	1A

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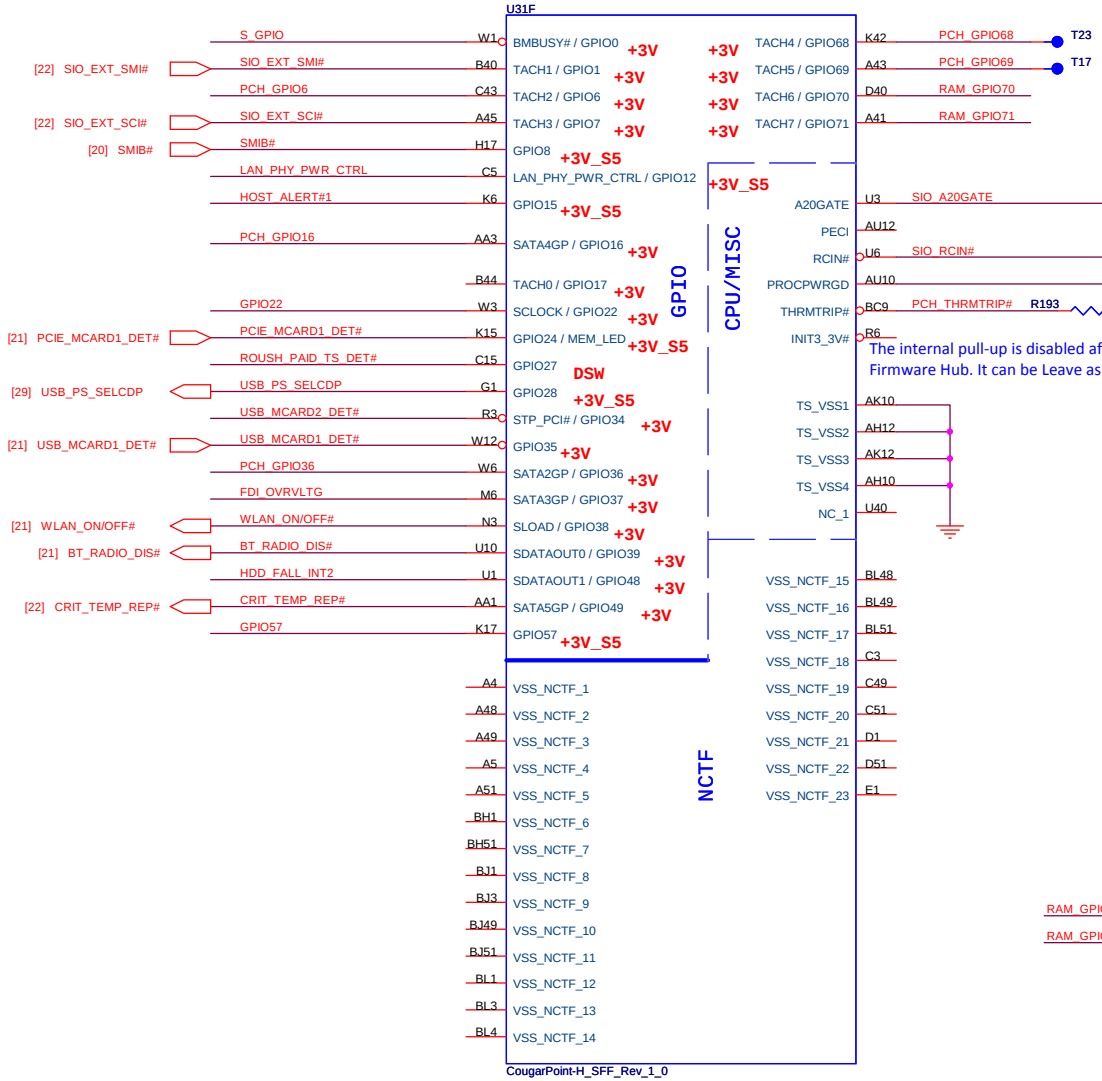
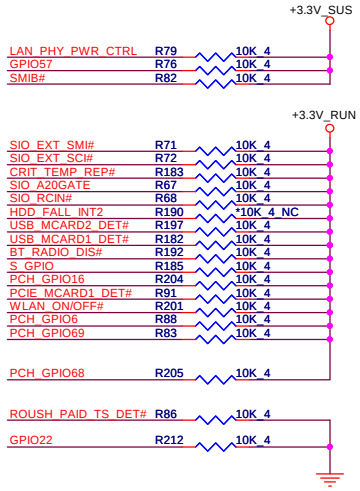
Cougar Point (GPIO,VSS_NCTF,RSVD)

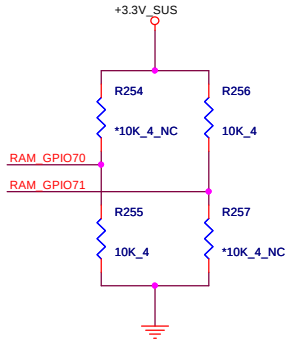
Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
Internal PU		USB_PS_SELCDP R215 *10K_4_NC	



The internal pull-up is disabled after PLTRST# deasserts. This signal is intended for Firmware Hub. It can be Leave as "No Connect". (desktop SKUs only)

GPIO Pull-up/Pull-down(CLG)





RAM Vender select

RAM_GPIO70	R254(1)	R255(0)
Samsung		V
Hynix	V	

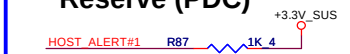
RAM size select

RAM_GPIO71	R256(1)	R257(0)
2G		V
4G	V	

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

Reserve (PDC)



Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

MFG-TEST

del 0527

Quanta Computer Inc.

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	Cougar Point 6/7	1A
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Cougar Point (POWER)

COUGAR POINT (POWER)

VccCORE =6A

need 1206?

VccADAC =1mA(8mils)

VCCDSW3_3 tie to 3.3V_SUS, when don't support Deep SX CP_v1.0 p88

VccDSW3_3= 3mA(8mil)

VccALVDS=1mA (8mils)

VccTX_LVDS=60mA (10mils)

need Indutor?

VccIO =2.925 A(120mils)

Near to AN16, AP21, AN33

Vcc3_3 = 0.266A (15mils)

Change 22U/6.3V_8 to 10U/6.3V_6 for package

01/26 power rail for VCCIO

VccDMI = 80mA (10mils)

VccCLKDMI = 20mA (8mils)

09/28: NO.3

VCCPNAND = 190 mA(15mils)

VccVRM(1.5V) =0.16 A(10mils)

VccDMI =0.042 A(10mils)

VCCSPI = 20mA(8mils)

Intel

VccASW =1.01A (50mils)

80mA(10mils)

VCCDIFFCLKN= 55mA(18mils,PDDG)

VCCSSC= 95mA(10mils)

1mA(8mils)

VCCRTC<1mA(8mils)

VCCSUS3_3 = 119mA (15mils)

VCC5REFSUS=1mA(8mil)

V5REF= 1mA(8mil)

VCCSUS3_3 = 119mA (15mils)

VCCPCORE = 28mA(10mils)

VCCVRM= 114mA(15mils)

VCCSUSHDA= 10mA(8mils)

09/28: NO.3

09/28: NO.3

Quanta Computer Inc.

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	Cougar Point 7/7	1A
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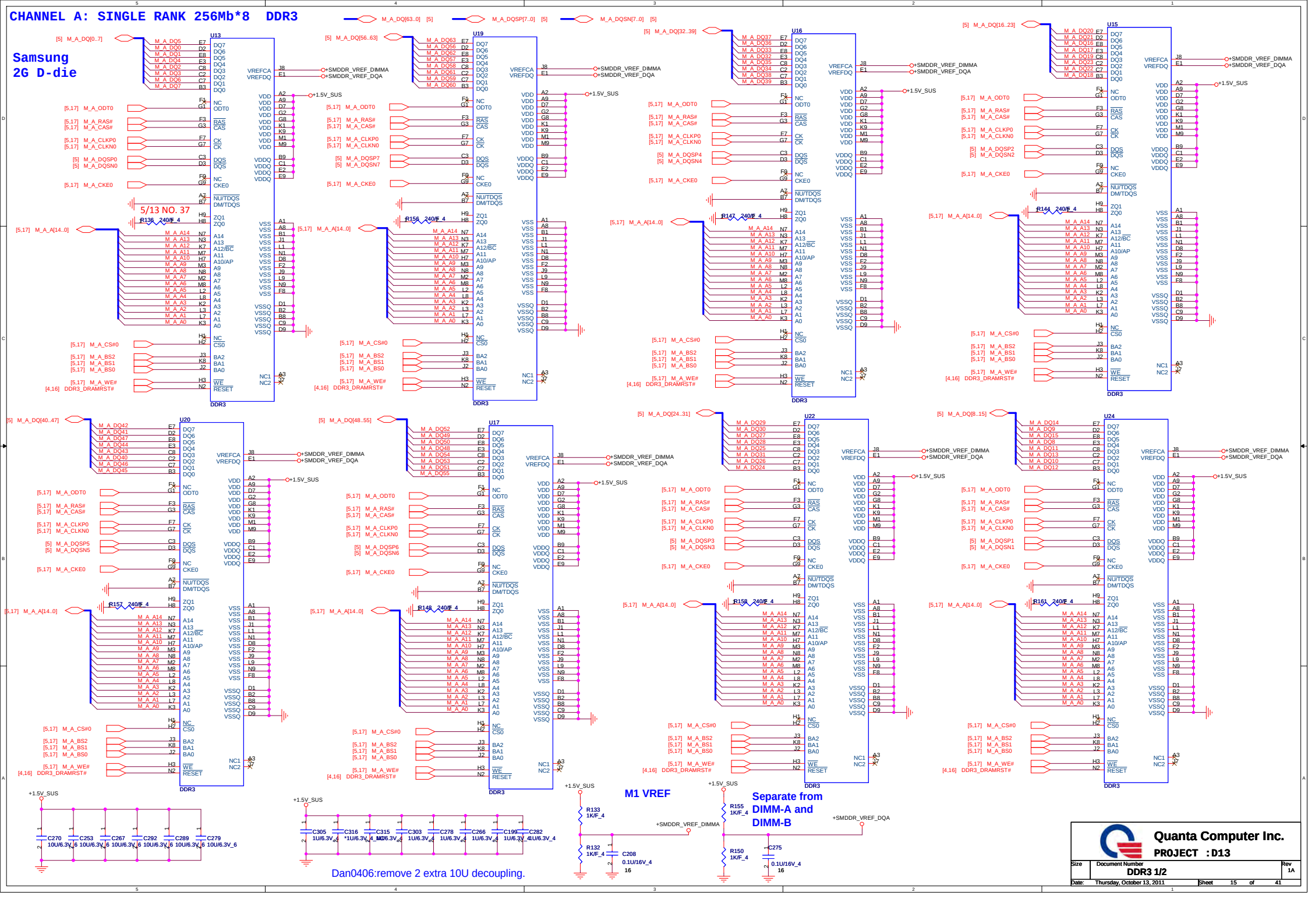
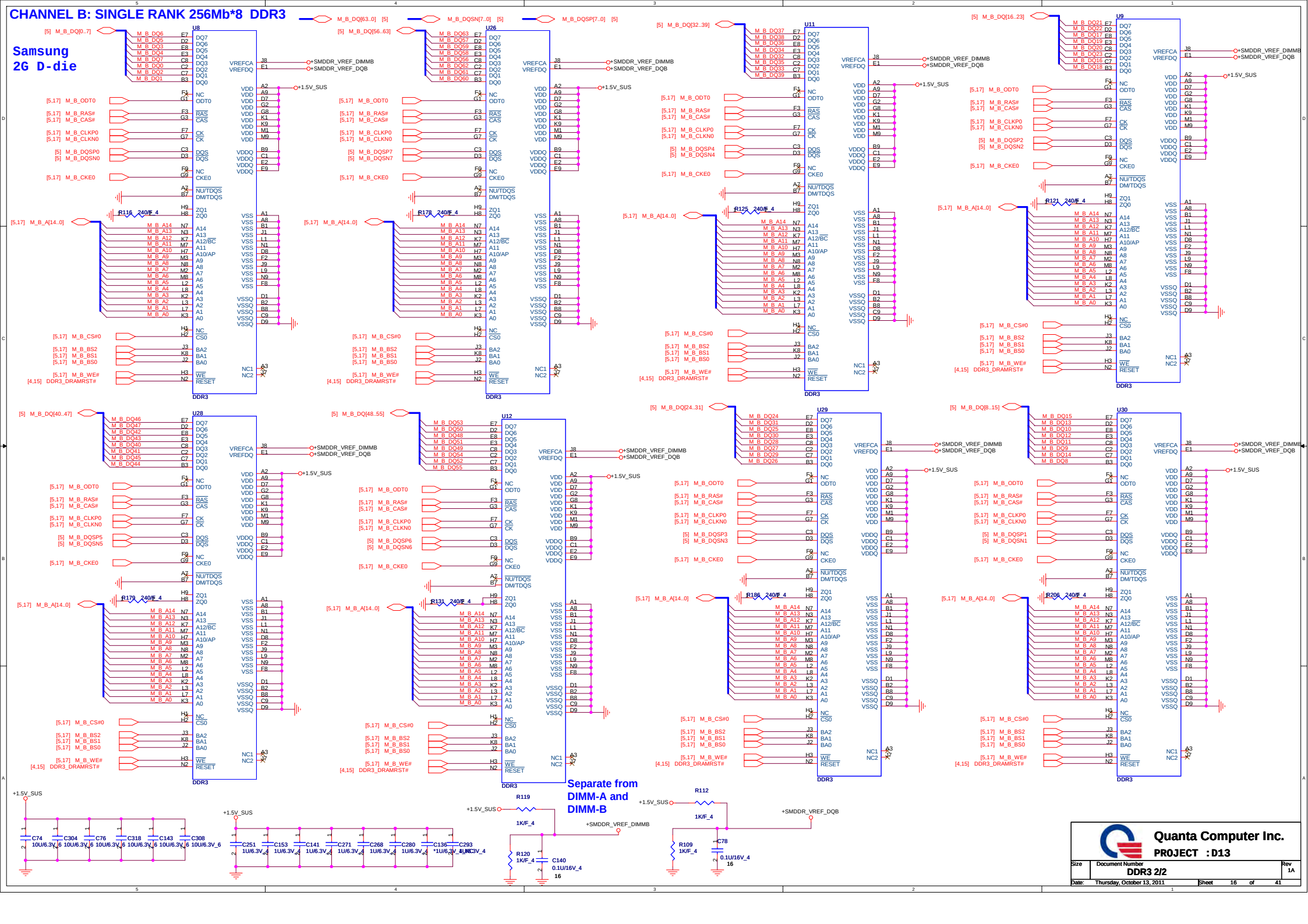
CHANNEL A: SINGLE RANK 256Mb*8 DDR3



CHANNEL B: SINGLE RANK 256Mb*8 DDR3

Samsung 2G D-die



Quanta Computer Inc.
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	DDR3 2/2	1A

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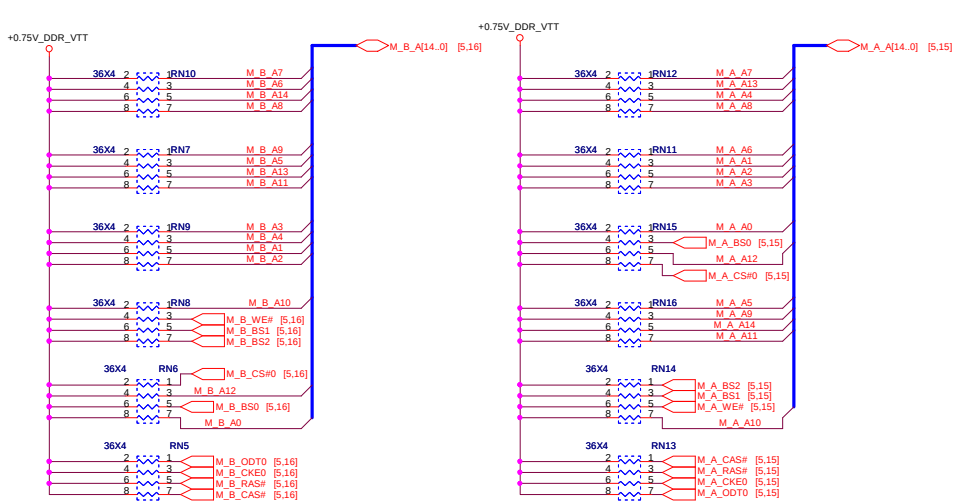

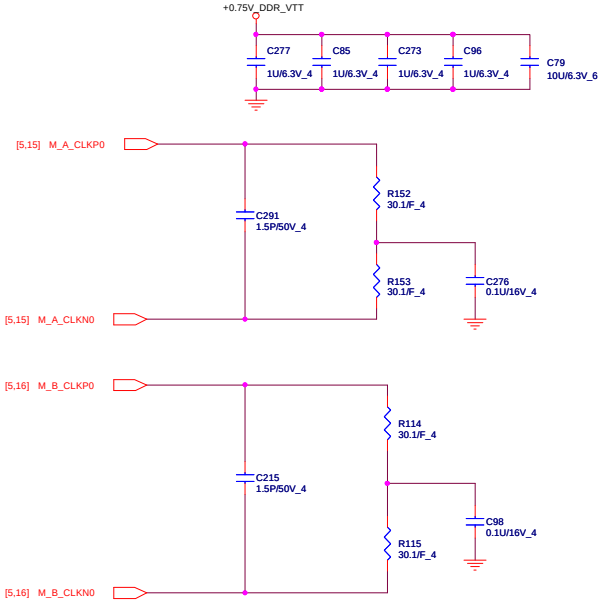

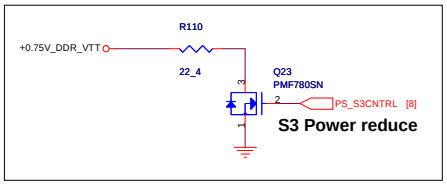

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Size	Document Number	Rev
	DDR3 TERMINATION	1A
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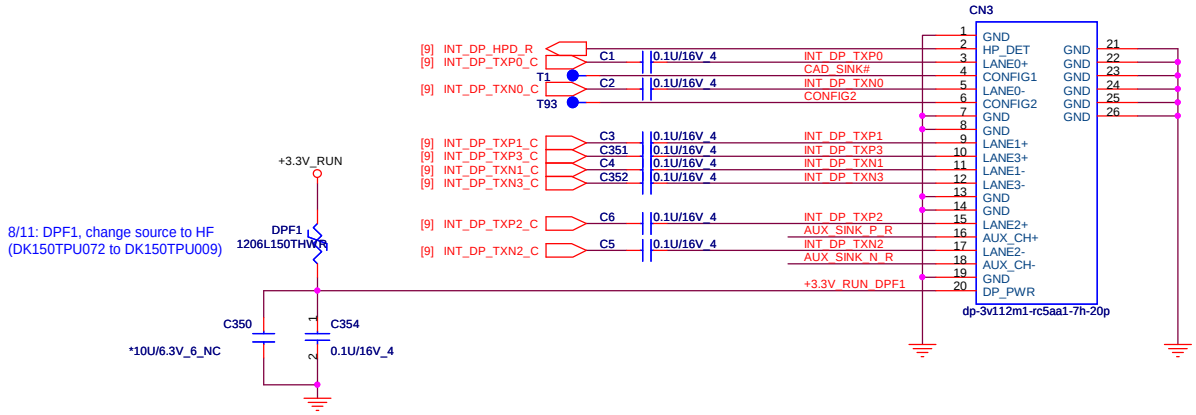
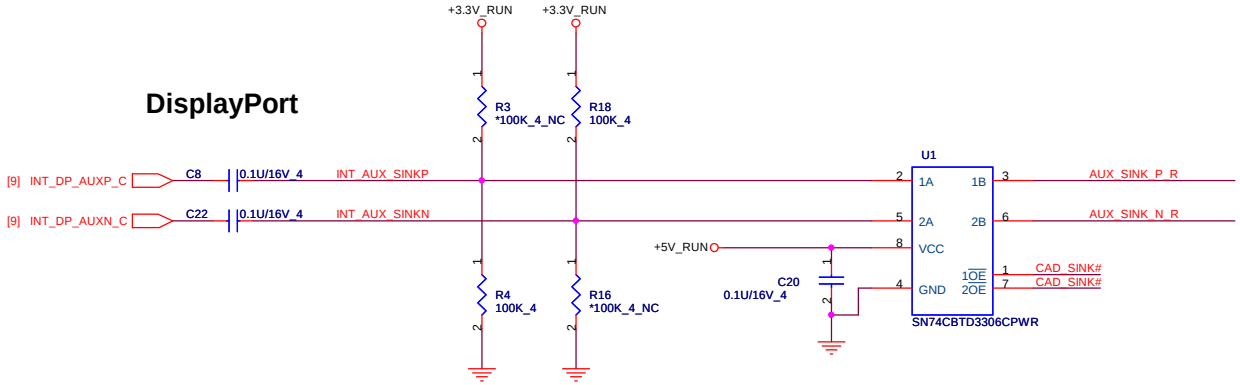
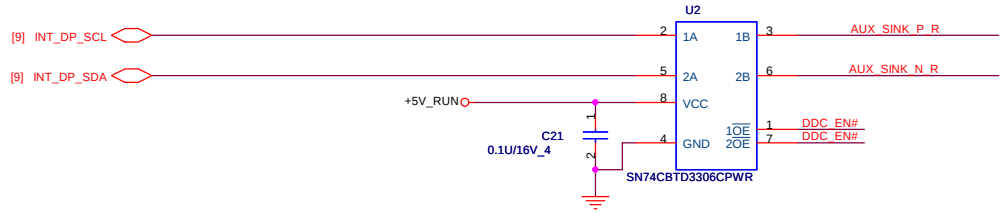
MINI DISPLAY PORT CONNECTOR

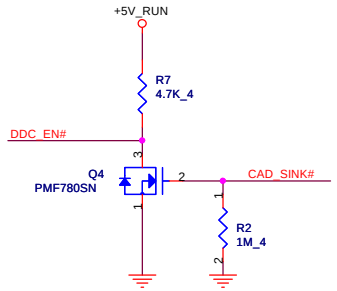


DisplayPort



HDMI





Quanta Computer Inc.		
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Size	Document Number: MINI DP CONN	Rev: 1A
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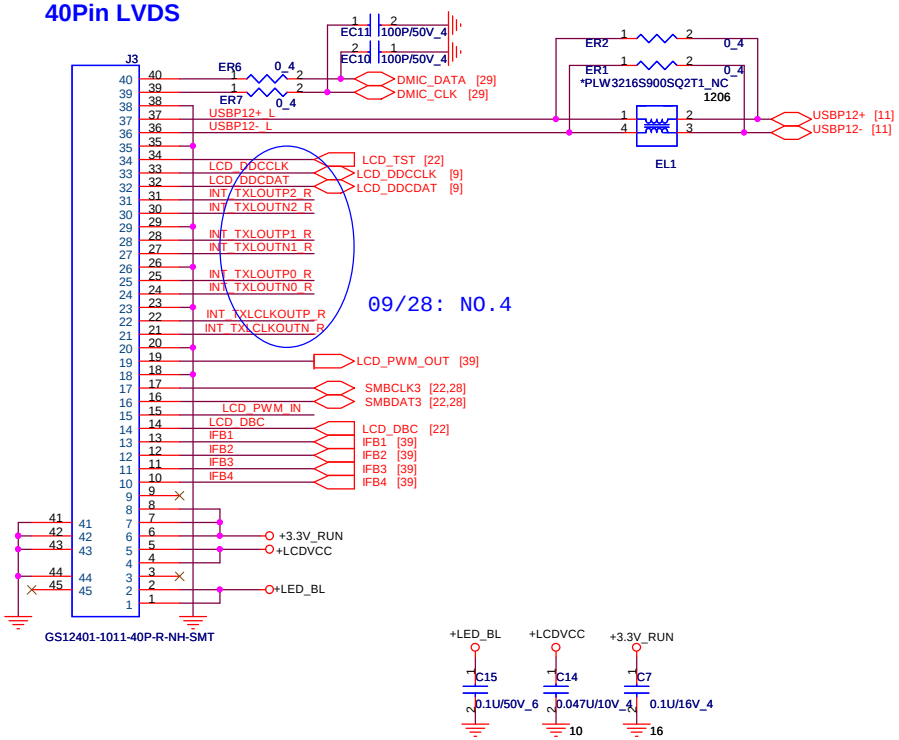
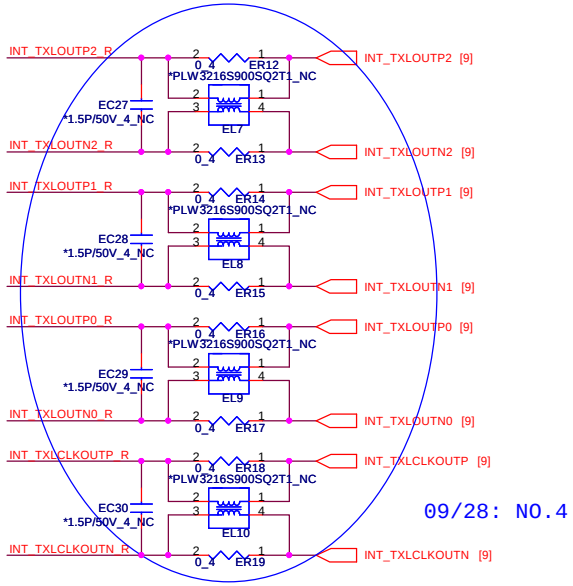
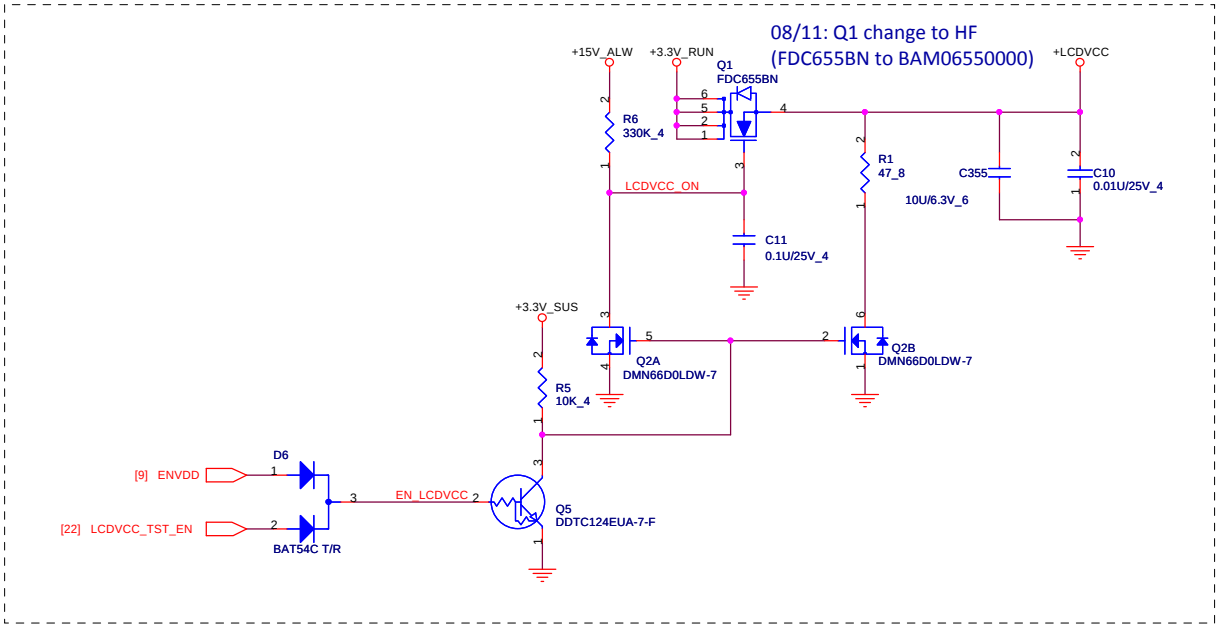
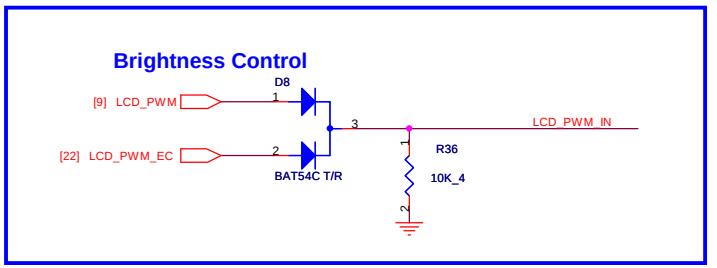
40Pin LVDS









Quanta Computer Inc.		
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Size	Document Number: LVDS CONN	Rev: 1A
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AVCC33X		
Min	Typ	Max
3.15V	3.30V	3.45V
Current = 36mA		

PVCCA33X		
Min	Typ	Max
3.15V	3.30V	3.45V
Current = 72mA		

AVCC10X		
Min	Typ	Max
1.00V	1.05V	1.10V
Current = 164mA		

AVCC10		
Min	Typ	Max
1.00V	1.05V	1.10V
Current = 9mA		

DVCC33X		
Min	Typ	Max
2.97V	3.30V	3.63V
Current = 0mA		

DVCC33		
Min	Typ	Max
2.97V	3.30V	3.63V
Current = 5mA		

DVCC10X		
Min	Typ	Max
1.00V	1.05V	1.10V
Current = 25mA		

DVCC10		
Min	Typ	Max
1.00V	1.05V	1.10V
Current = 90mA		

09/28: NO.5

TX base on FL1009

RX base on FL1009

FL1009

CANNOT floating even if it hasn't been used

10/04 NO.7

Vout=0.8*(R222+R223)/R223

Need closed to CN4

10/204 NO.7

Quanta Computer Inc.		
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	TI USB 3.0	1A
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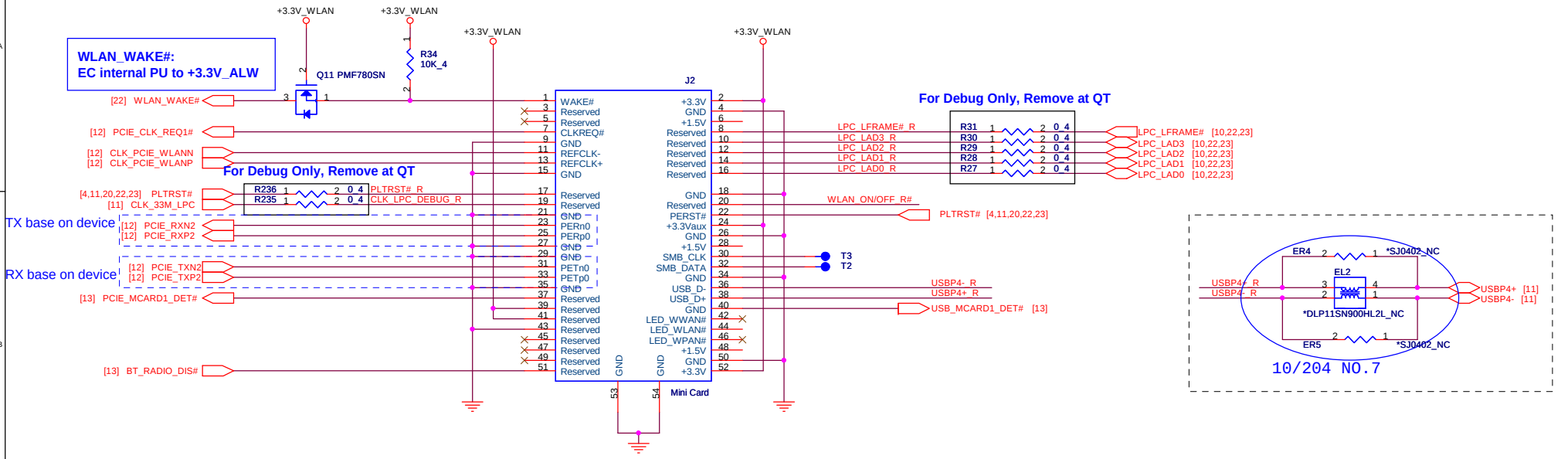
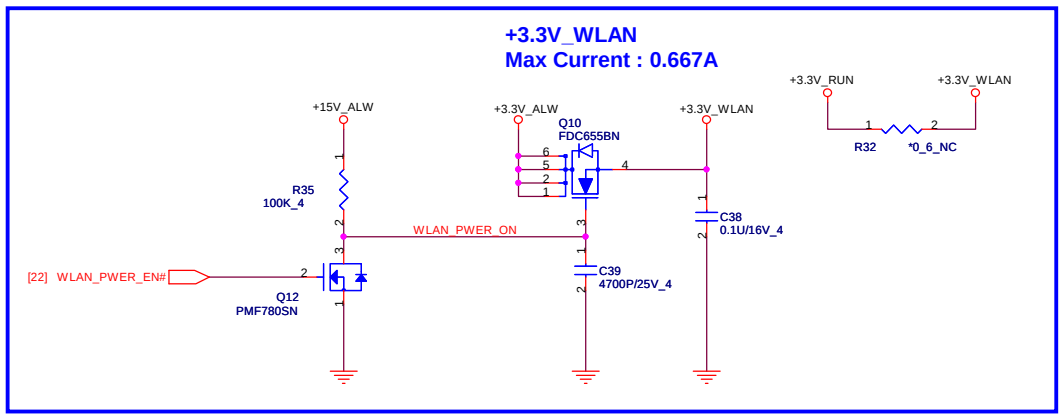
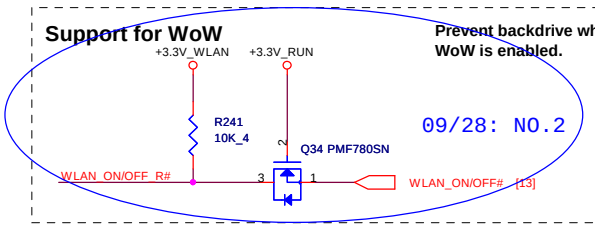
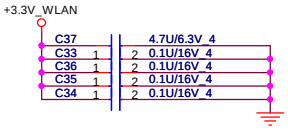
MiniCard WLAN connector



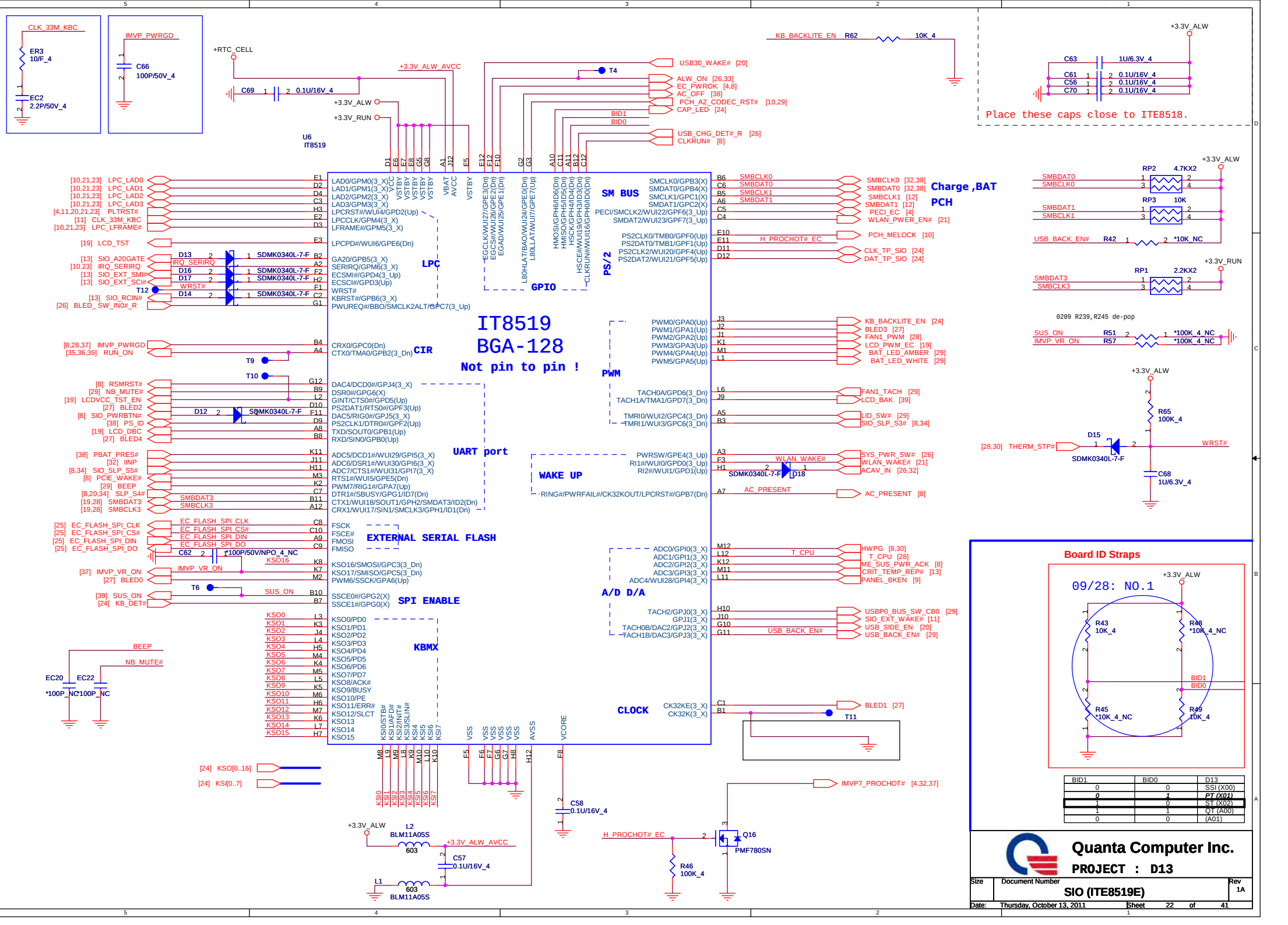






Place caps close to connector.

Quanta Computer Inc.		
PROJECT : D13		
Size	Document Number: MINI-PCI (WLAN/WPAN)	Rev: 1A
Date: Thursday, October 13, 2011	Sheet 21 of 41	


CLK_33M_KBC
ER3 10/F_4
EC2 2.2P/50V_4
IMVP_PWRGD
C66 100P/50V_4
+RTC_CELL
C69 0.1U/16V_4
+3.3V_ALW_AVCC
+3.3V_ALW
+3.3V_RUN
U6
IT8519
KB_BACKLITE_EN R62 10K_4
T4
USB30_WAKE# [20]
ALW_ON [26,33]
EC_PWROK [4,8]
AC_OFF [38]
PCH_AZ_CODEC_RST# [10,29]
CAP_LED [24]
BID1
BID0
USB_CHG_DET#_R [26]
CLKRUN# [8]
+3.3V_ALW
C63 1U/6.3V_4
C61 0.1U/16V_4
C56 0.1U/16V_4
C70 0.1U/16V_4
Place these caps close to ITE8518.
LPC
SM BUS
PS/2
GPIO
Charge ,BAT
PCH
IT8519
BGA-128
Not pin to pin !
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
SMBCLK0
SMBDAT0
SMBCLK1
SMBDAT1
PECI_EC
WLAN_PWER_EN#
H_PROCHOT# EC
PCH_MELOCK
CLK_TP_SIO
DAT_TP_SIO
KB_BACKLITE_EN
BLED3
FAN1_PWM
LCD_PWM_EC
BAT_LED_AMBER
BAT_LED_WHITE
FAN1_TACH
LCD_BAK
LID_SW#
SIO_SLP_S3#
WLAN_WAKE#
SYS_PWR_SW#
ACAV_IN
AC_PRESENT
T_CPU
HWPG
ME_SUS_PWR_ACK
CRIT_TEMP_REP#
PANEL_BKEN
USBP0_BUS_SW_CB0
SIO_EXT_WAKE#
USB_SIDE_EN
USB_BACK_EN#
BLED1
T11
IMVP7_PROCHOT#
Q16 PMF780SN
R46 100K_4
C58 0.1U/16V_4
C57 0.1U/16V_4
L2 BLM11A05S 603
L1 BLM11A05S 603
+3.3V_ALW_AVCC
RP2 4.7KX2
RP3 10K
RP1 2.2KX2
USB_BACK_EN# R42 *10K_NC
0209 R239,R245 de-pop
SUS_ON R51 *100K_4_NC
IMVP_VR_ON R57 *100K_4_NC
R65 100K_4
D15 SDMK0340L-7-F
C68 1U/6.3V_4
THERM_STP#
WRST#
Board ID Straps
09/28: NO.1
R43 10K_4
R48 *10K_4_NC
R45 *10K_4_NC
R49 10K_4
BID1
BID0
BID1 BID0 D13
0 0 SSI (X00)
0 1 PT (X01)
1 0 ST (X02)
1 1 QT (A00)
0 0 (A01)
Quanta Computer Inc.
PROJECT : D13
Size
Document Number
SIO (ITE8519E)
Rev 1A
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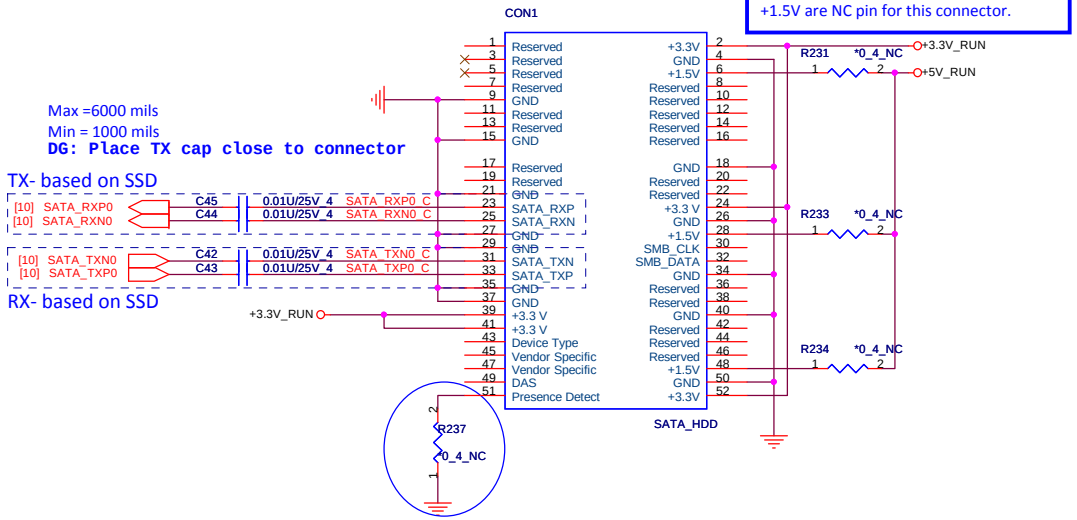
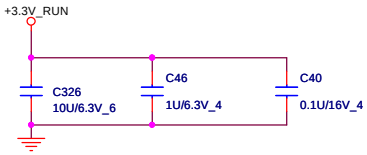
mSATA Connector

+5V_RUN is for testing mSATA by factory.
+1.5V are NC pin for this connector.

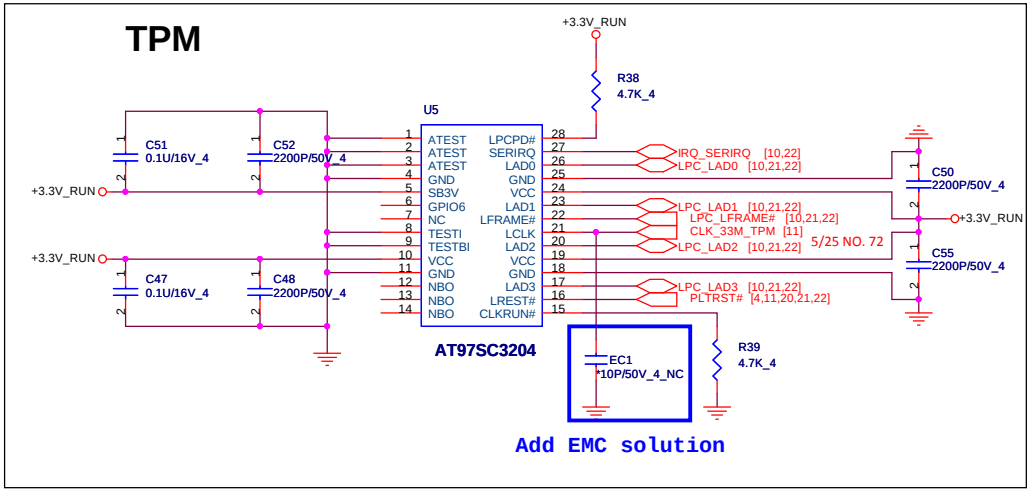


10/204 NO.7



Place caps close to connector.

TPM



Add EMC solution

Quanta Computer Inc.
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	SATA HDD/ODD	1A
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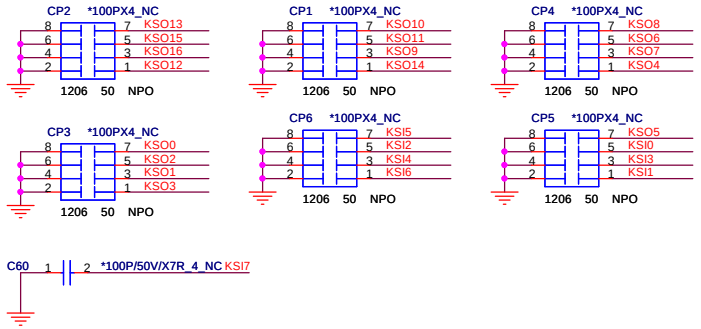
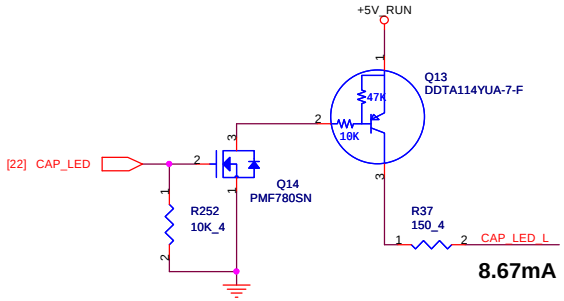
KEYBOARD CONNECTOR

03/30 Change CP1,CP2,CP3,CP4,CP5,CP6,C382 from Pop to Depop



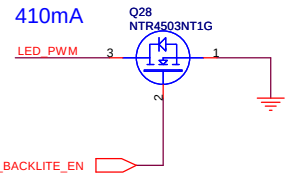
Vi(on_max)= -1.4V
Vi(off_min)=-0.3



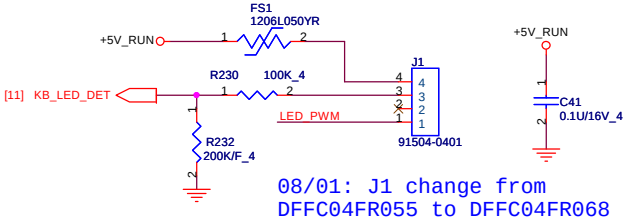
8.67mA

Key board illumination

410mA

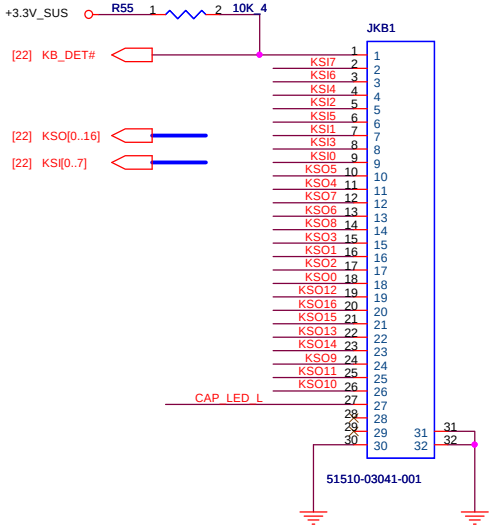


+KB_LED power trace width >10 mil



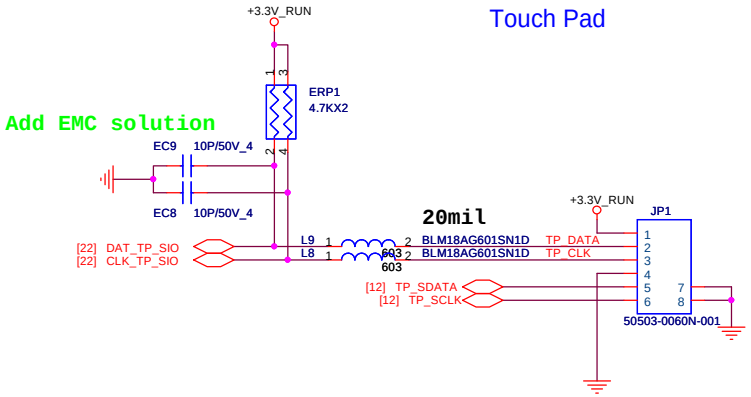
08/01: J1 change from
DFFC04FR055 to DFFC04FR068

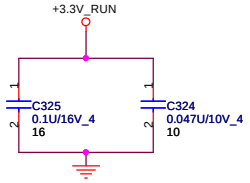
KEYBOARD CONNECTOR



Touch Pad

Add EMC solution





Quanta Computer Inc.

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	TP / KB	1A
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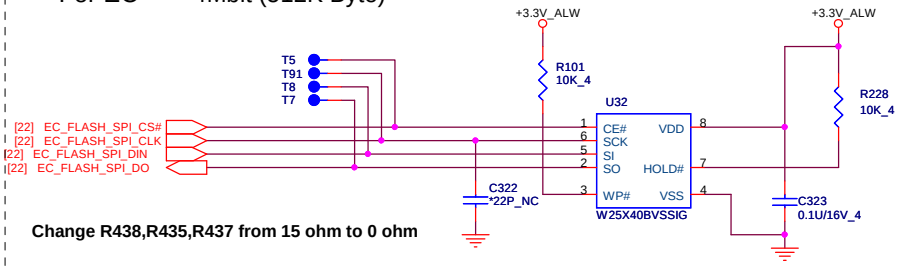
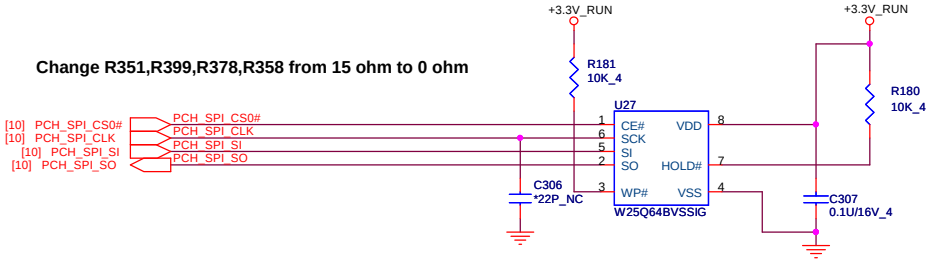
For EC 4Mbit (512K Byte)



Change R438,R435,R437 from 15 ohm to 0 ohm

For PCH 64Mbit (8M Byte)

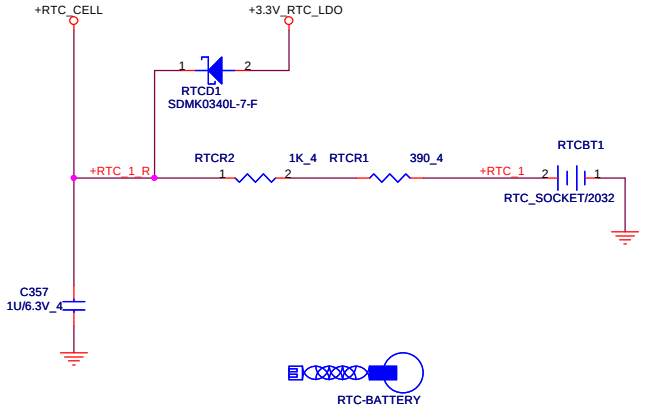


Change R351,R399,R378,R358 from 15 ohm to 0 ohm

Change SPI ROM for BIOS to AKE3EFP0N04 -0613

The max charge current is flow on charged at the end voltage of battery
2V. And the charge current is 1mA.
R >= (+RTC_CELL - 2)/1mA

RTC BATTERY



Quanta Computer Inc.
PROJECT : D13

Size	Document Number	Rev
	FLASH / RTC	1A
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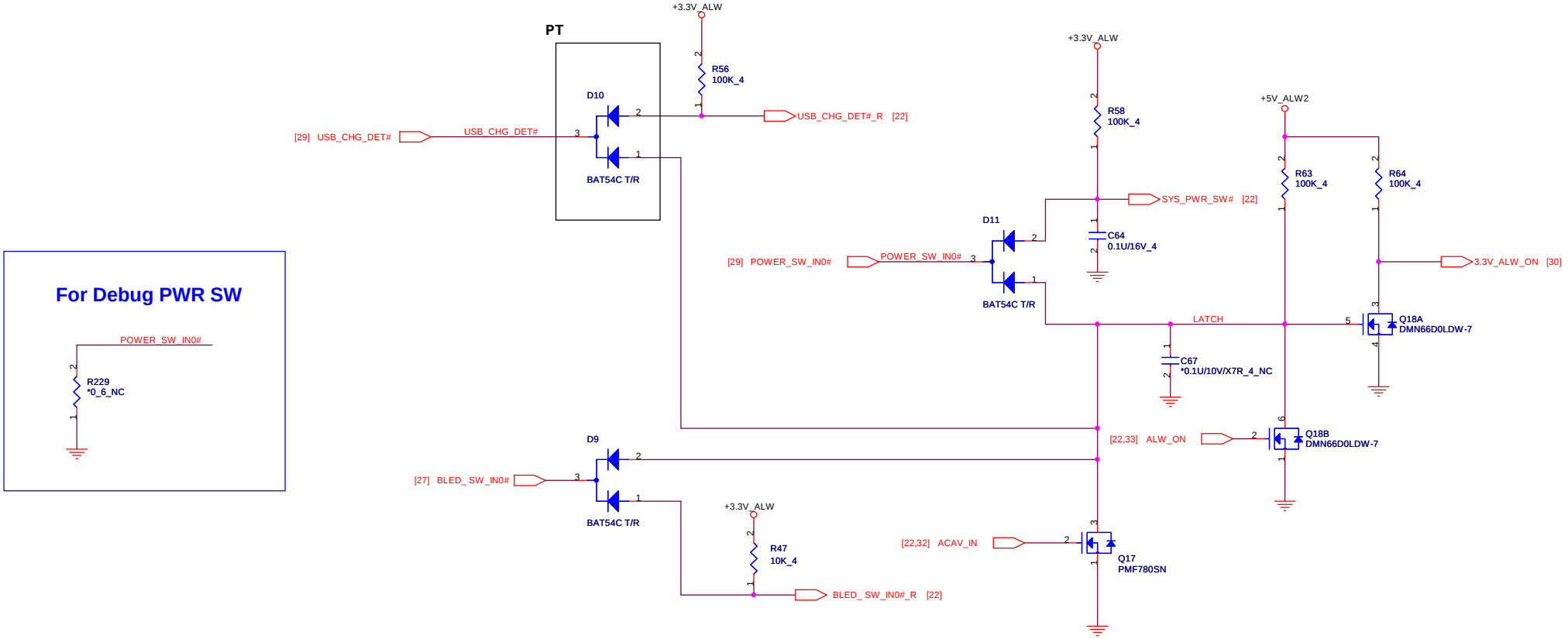
3VALW ON POWER LOGIC



Quanta Computer Inc.		
PROJECT : D13		
Size	Document Number: PWR SW/LED	Rev: 1A
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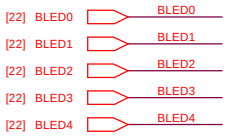
Truth table of Battery LED

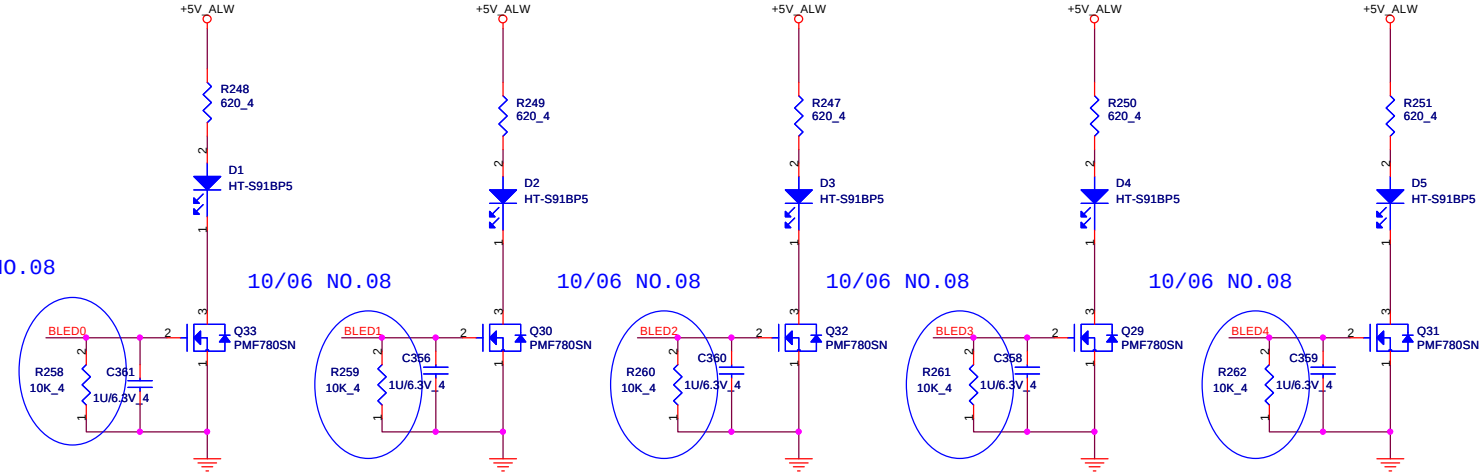
Battery Power State	BLED4	BLED3	BLED2	BLED1	BLED0	LED State
<20%	0	0	0	0	0	N/A
20%	0	0	0	0	1	D29
40%	0	0	0	1	1	D29 D30
60%	0	0	1	1	1	D29 D30 D31
80%	0	1	1	1	1	D29 D30 D31 D32
100%	1	1	1	1	1	D29 D30 D31 D32 D33

Battery Status LED



10/14, change current limit resistor from 365 ohm to 620

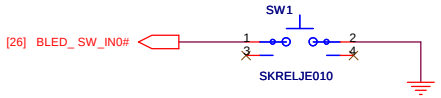
10/06 NO.08



10/06 NO.08 10/06 NO.08 10/06 NO.08 10/06 NO.08

Battery LED need to change direction

Battery LED button



Quanta Computer Inc.

PROJECT : D13

Size	Document Number	Rev
	LED SWITCH	1A

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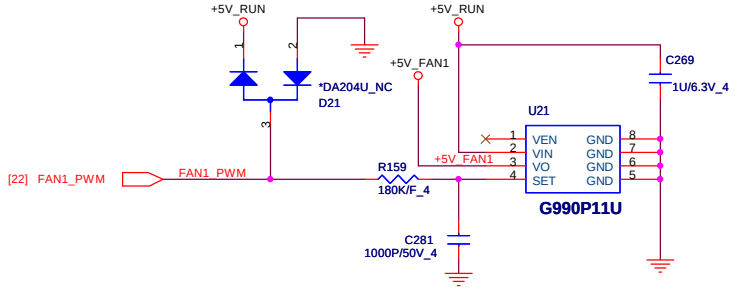
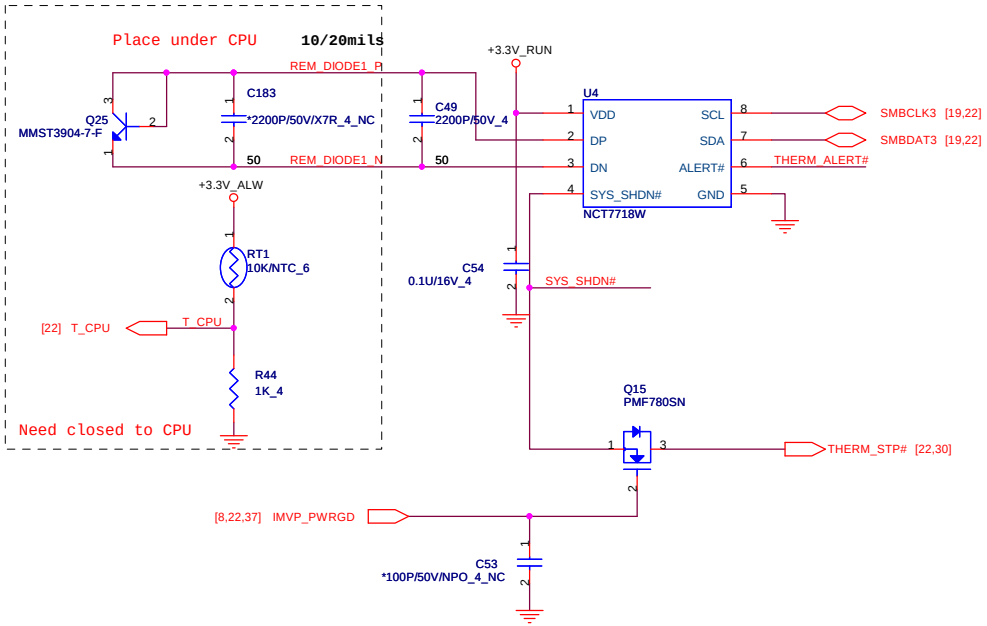
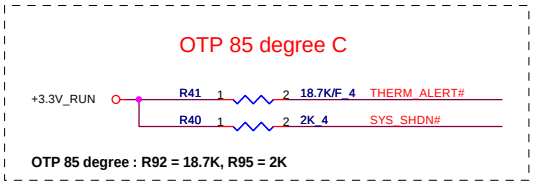


THERMAL IC



SYS_SHD# / ALERT#	2K	7.5K	10.5K	14K	18.7K
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C



Quanta Computer Inc.
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Size	Document Number	Rev
	FAN & THERMAL	1A

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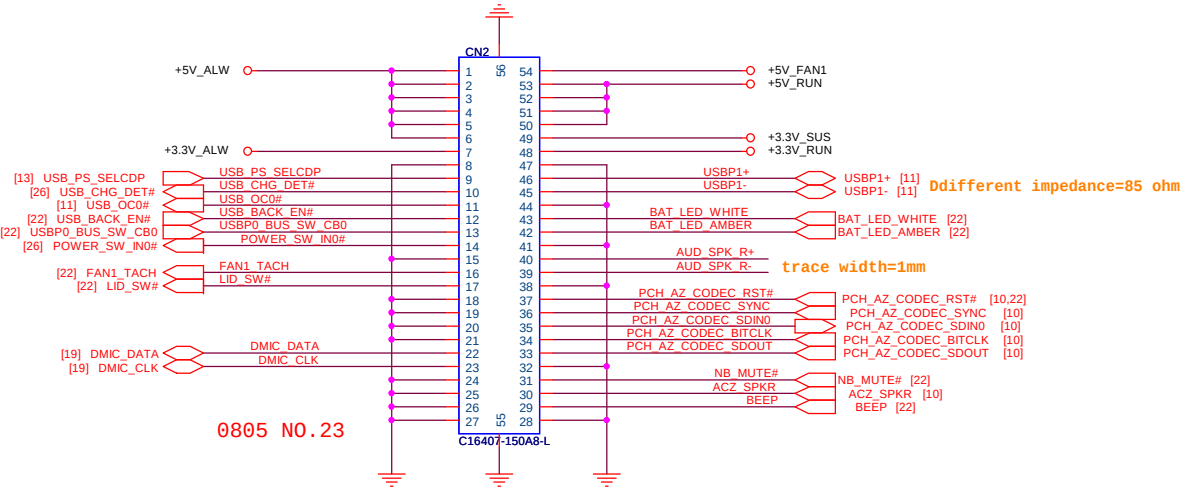
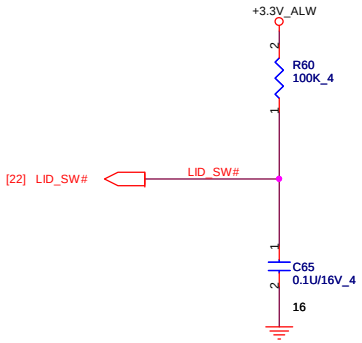
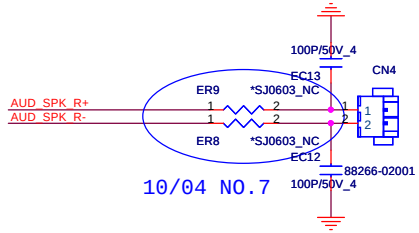
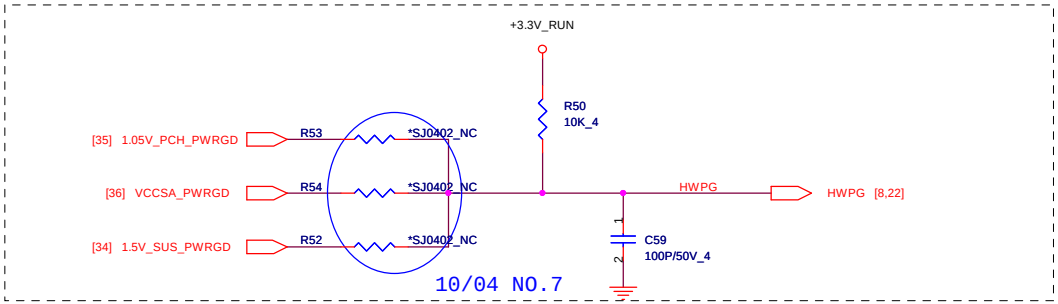


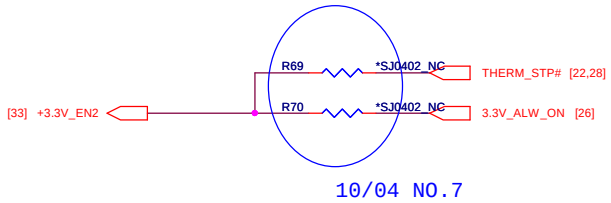


08/01: change CN4 PN from DFHD02MR401 change to DFHD02MR045



Quanta Computer Inc.		
PROJECT : D13		
Size	Document Number: BTB connector	Rev: 1A
Date: Thursday, October 13, 2011	Sheet 29 of 41	





Quanta Computer Inc.		
PROJECT : D13		
Size	Document Number: System Reset Circuit	Rev: 1A
Date: Thursday, October 13, 2011	Sheet 30 of 41	

Need to add in BOM

H7
h-tc217bc197d102p2
1
h-tc217bc197d102p2

H8
h-tc217bc197d102p2
1
h-tc217bc197d102p2

H6
h-tc217bc197d102p2
1
h-tc217bc197d102p2

H10
H-C220D142P2
1
H-C220D142P2

H11
h-tc217bc197d102p2
1
h-tc217bc197d102p2

H12
h-tc217bc197d102p2
1
h-tc217bc197d102p2

BOT-Size
Need to modify PN

TOP-Size

H4
h-tc166i131bc177d91p2
1
*h-tc166i131bc177d91p2_NC

H3
H-TC197BC221D91P2
1
*H-TC197BC221D91P2_NC

H5
H-C217D91P2
1
*H-C217D91P2_NC

H1
H-C79D79N
1
*H-C79D79N_NC

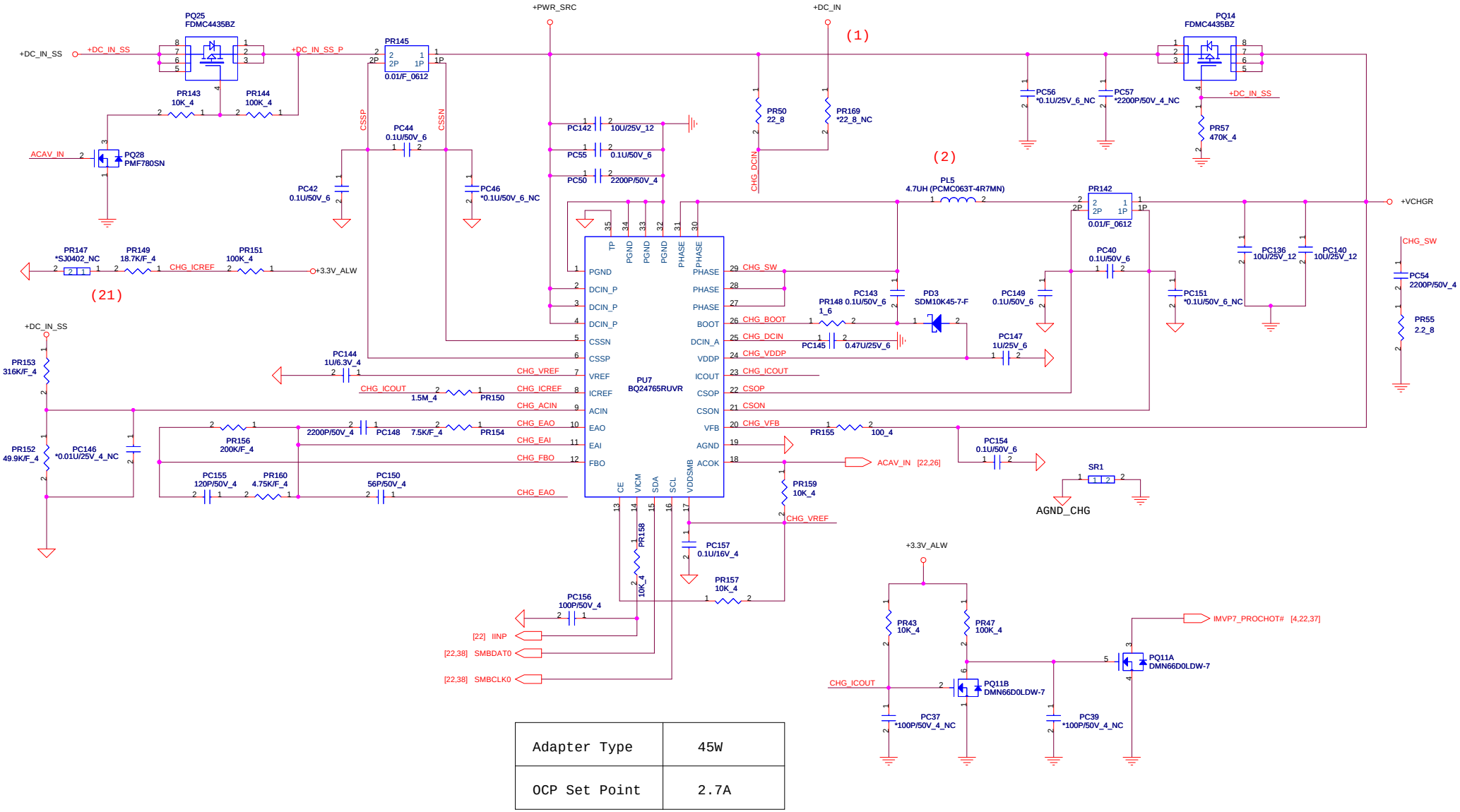
09/30: NO.6

H9
H-TC197I131BC220D91P2
1
*H-TC197I131BC220D91P2_NC

H2
h-o79x87d79x87n
1
*h-o79x87d79x87n_NC

Quanta Computer Inc.
PROJECT : D13

Size	Document Number	Rev
	SCREW PAD	1A
Date: Thursday, October 13, 2011	Sheet 31 of 41	



Adapter Type	45W
OCP Set Point	2.7A

Quanta Computer Inc.

PROJECT : D13

Size	Document Number	Rev
	Charger (BQ24765RUVR)	1A

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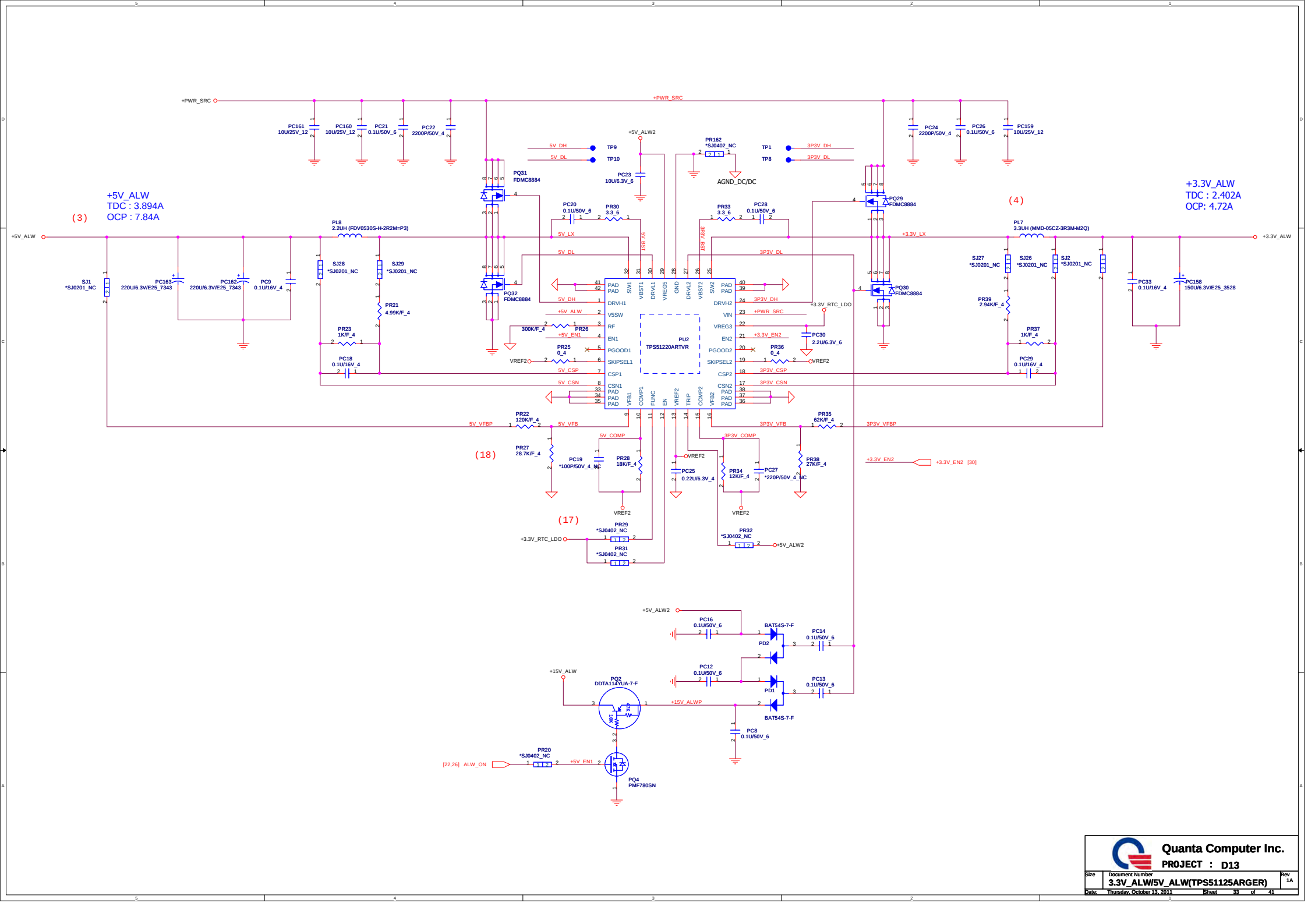
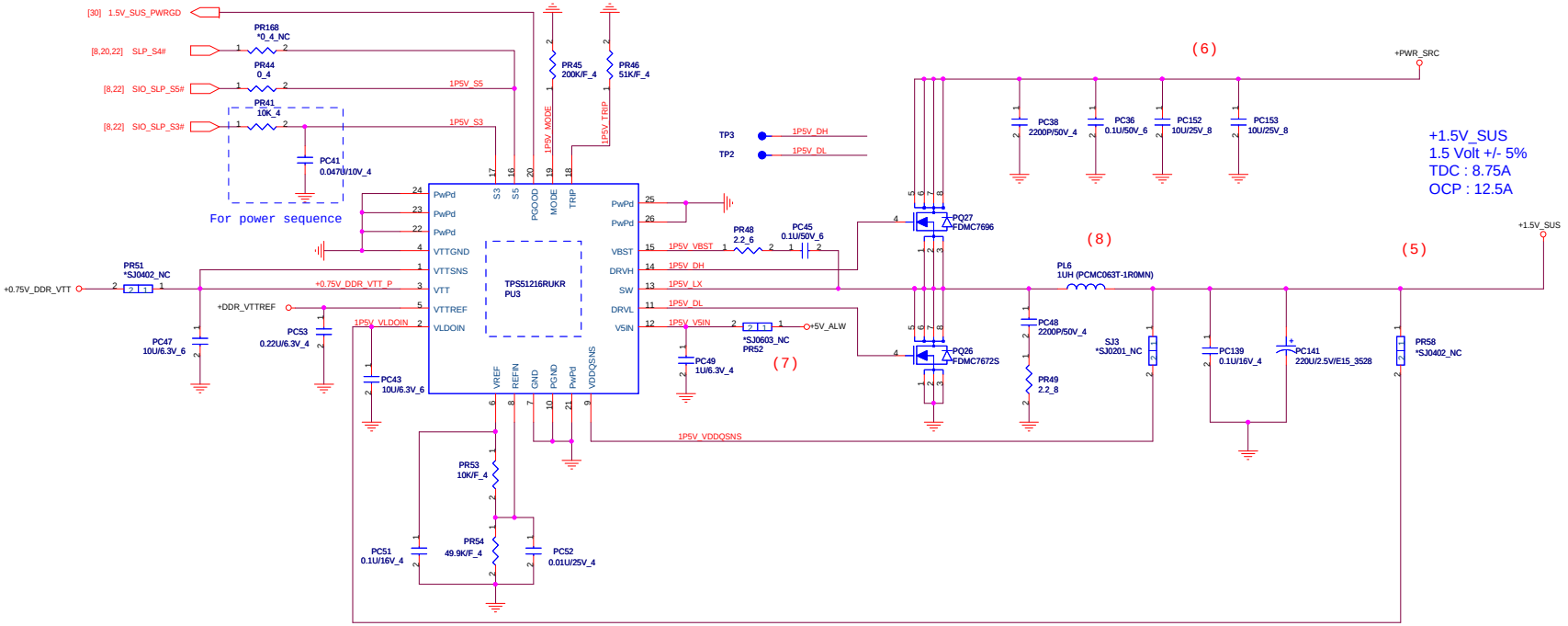


Quanta Computer Inc.			
PROJECT : D13			
Size	Document Number		Rev
	3.3V_ALW/5V_ALW(TPS51125ARGER)		1A
Date: Thursday, October 13, 2011	Sheet 33 of 41		



Quanta Computer Inc.

PROJECT : D13

Size	Document Number	Rev
	1.5_SUS/0.75_DDR_VTT	1A

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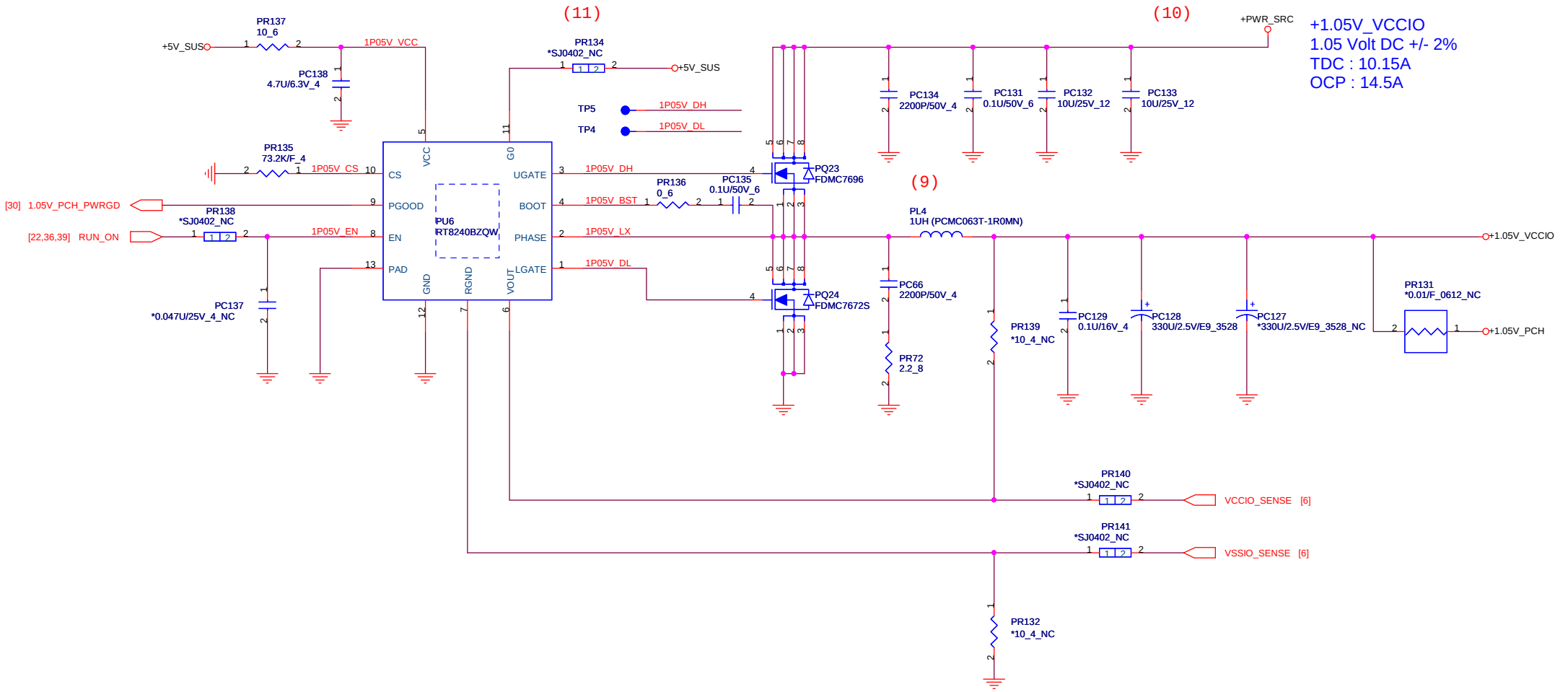
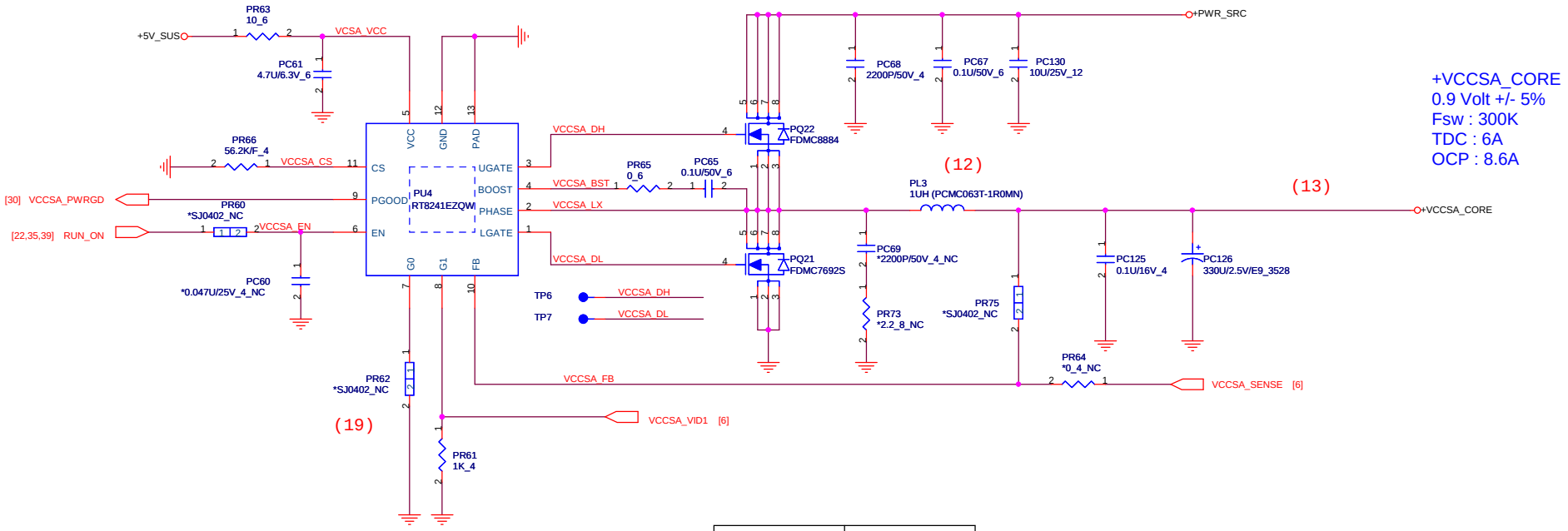
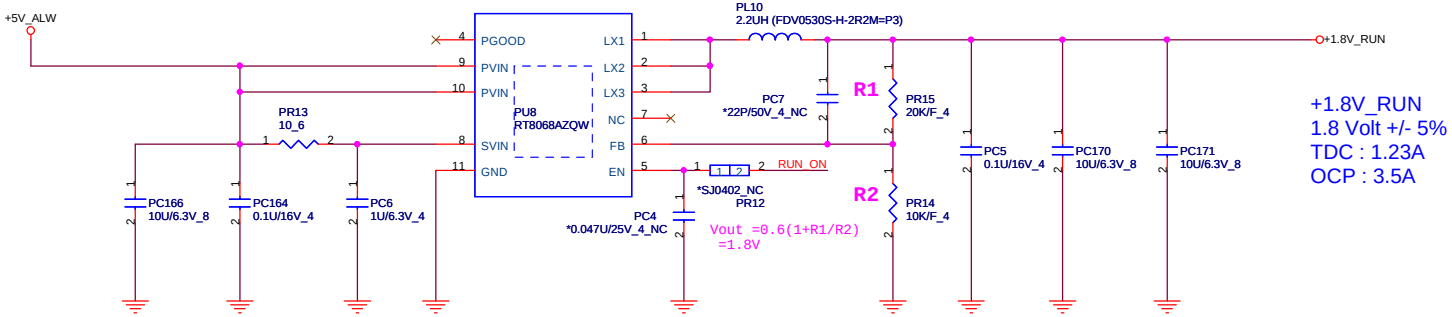


Quanta Computer Inc.		
PROJECT : D13		
Size	Document Number: 1.05V_VTT/1.05V_PCH	Rev: 1A
Date: Thursday, October 13, 2011	Sheet 35 of 41	



+VCCSA_CORE
0.9 Volt +/- 5%
Fsw : 300K
TDC : 6A
OCP : 8.6A

VCCSA_VID1	VCCSA_CORE
Low	0.9V
High	0.85V



+1.8V_RUN
1.8 Volt +/- 5%
TDC : 1.23A
OCP : 3.5A

Quanta Computer Inc.
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Size	Document Number	Rev
	VCCSA_CORE/1.8V_RUN	1A

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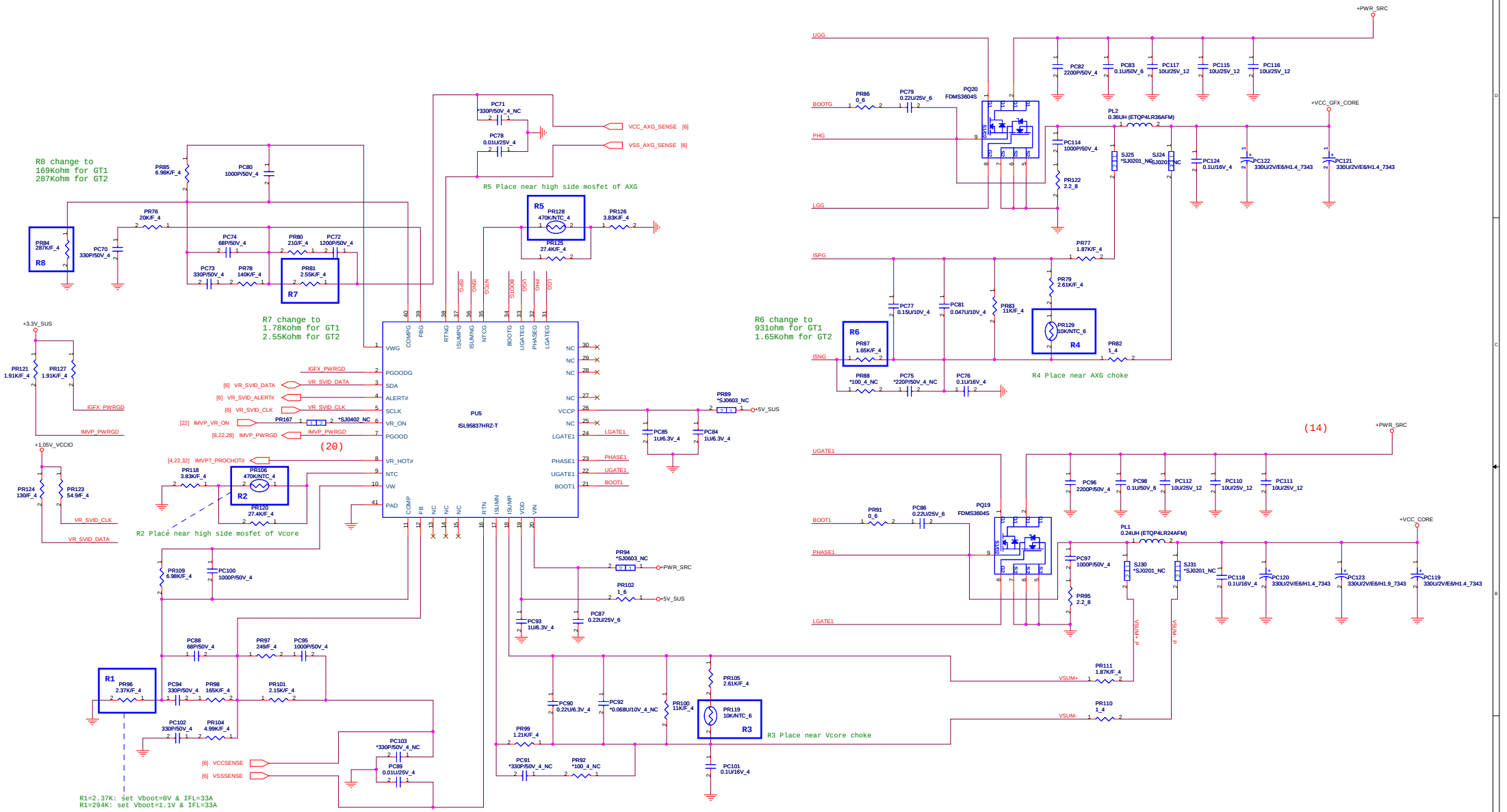

NOTE 1:
AXG Core power: Loadline ~-4.6mOhm
OCP~22A

CPU Core power: Loadline ~-2.9mOhm
OCP~40A

	GT1	GT2
R6	931 / CS19312FB11	1.65K / CS21652FB29
R7	1.78K / CS21782FB00	2.55K / CS22552FB01
R8	169K / CS41692FB12	287K / CS42872FB13

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Size	Document Number	Rev
	VCC_CORE/IGPU_CORE	1A

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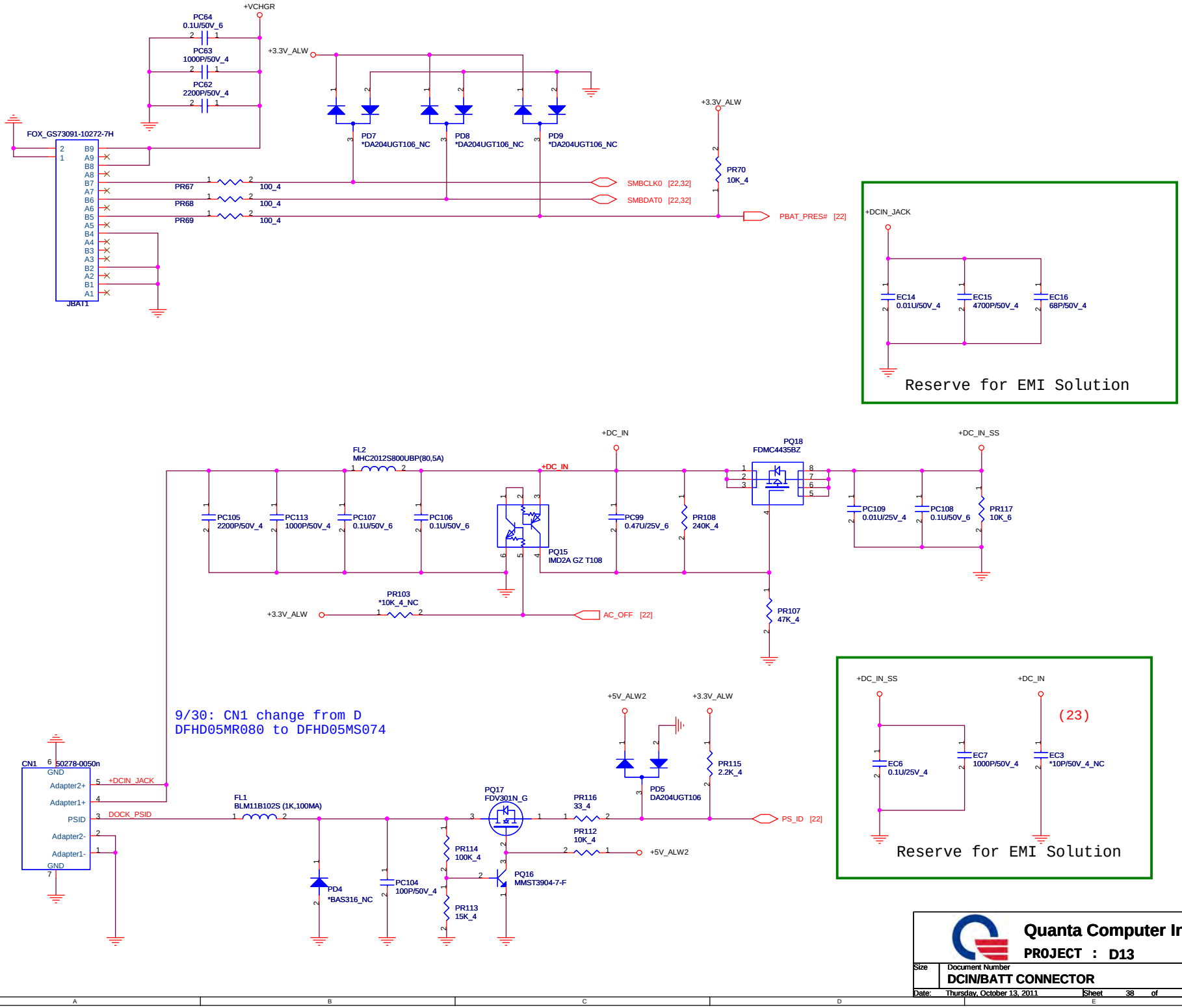
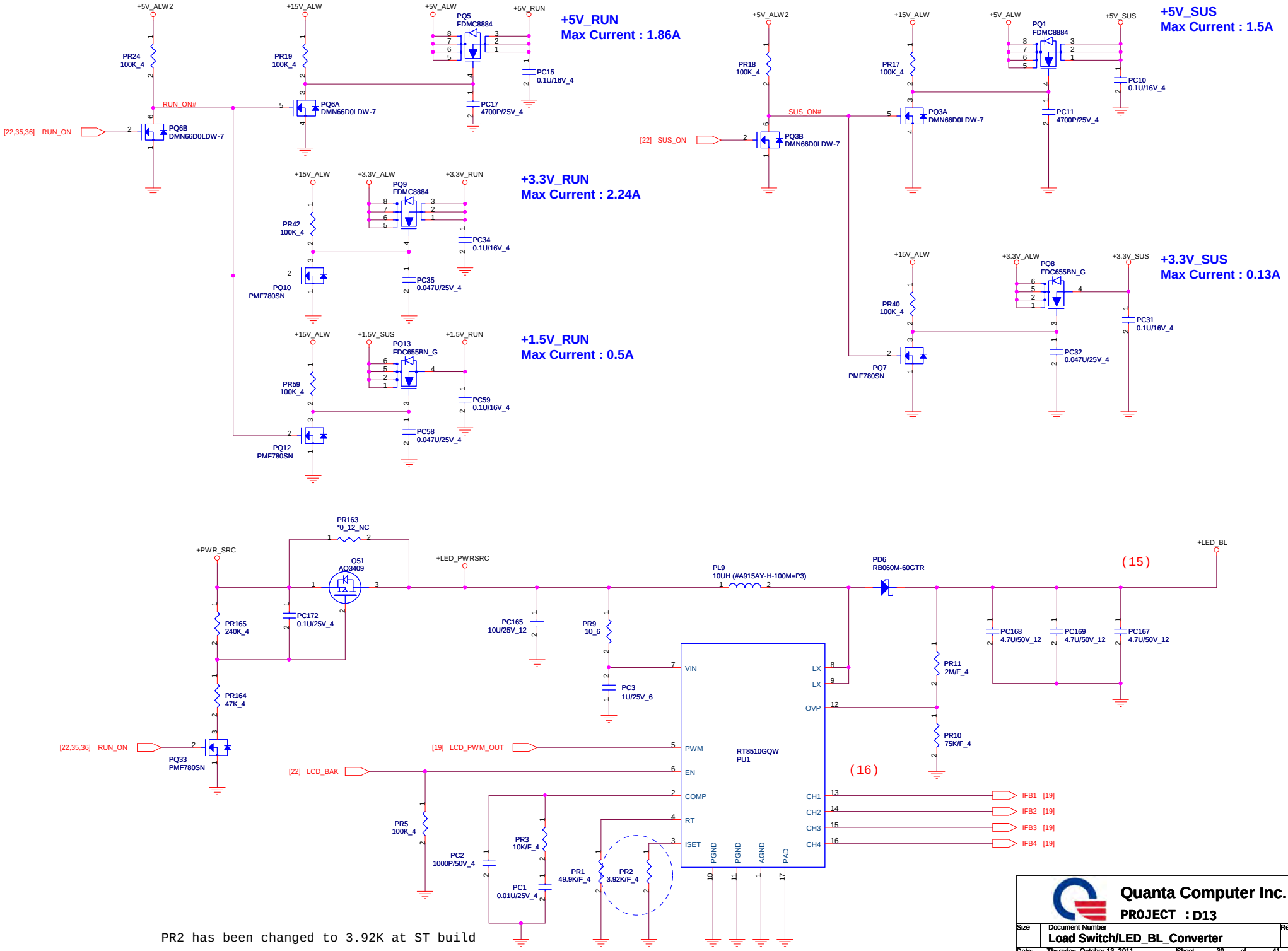


Quanta Computer Inc.		
PROJECT : D13		
Size	Document Number: DCIN/BATT CONNECTOR	Rev: 1A
Date: Thursday, October 13, 2011	Sheet 38 of 41	



PR2 has been changed to 3.92K at ST build

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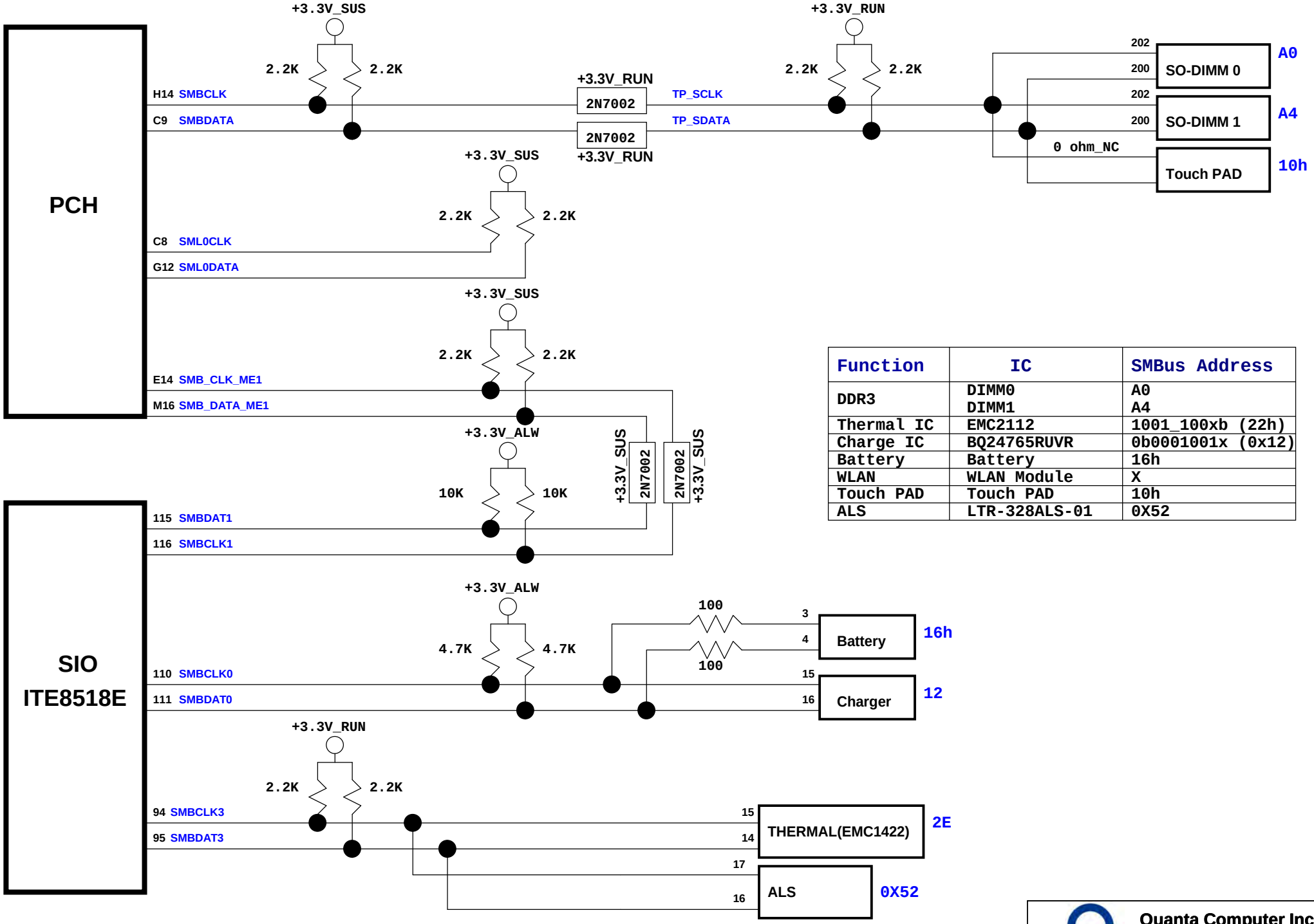
PROJECT : D13

Size	Document Number	Rev
	Load Switch/LED_BL_Converter	1A
Date: Thursday, October 13, 2011	Sheet 39 of 41	



Function	IC	SMBus Address
DDR3	DIMM0 DIMM1	A0 A4
Thermal IC	EMC2112	1001_100xb (22h)
Charge IC	BQ24765RUVR	0b0001001x (0x12)
Battery	Battery	16h
WLAN	WLAN Module	X
Touch PAD	Touch PAD	10h
ALS	LTR-328ALS-01	0X52

Quanta Computer Inc.
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Size	Document Number	Rev
	SMBUS	1A

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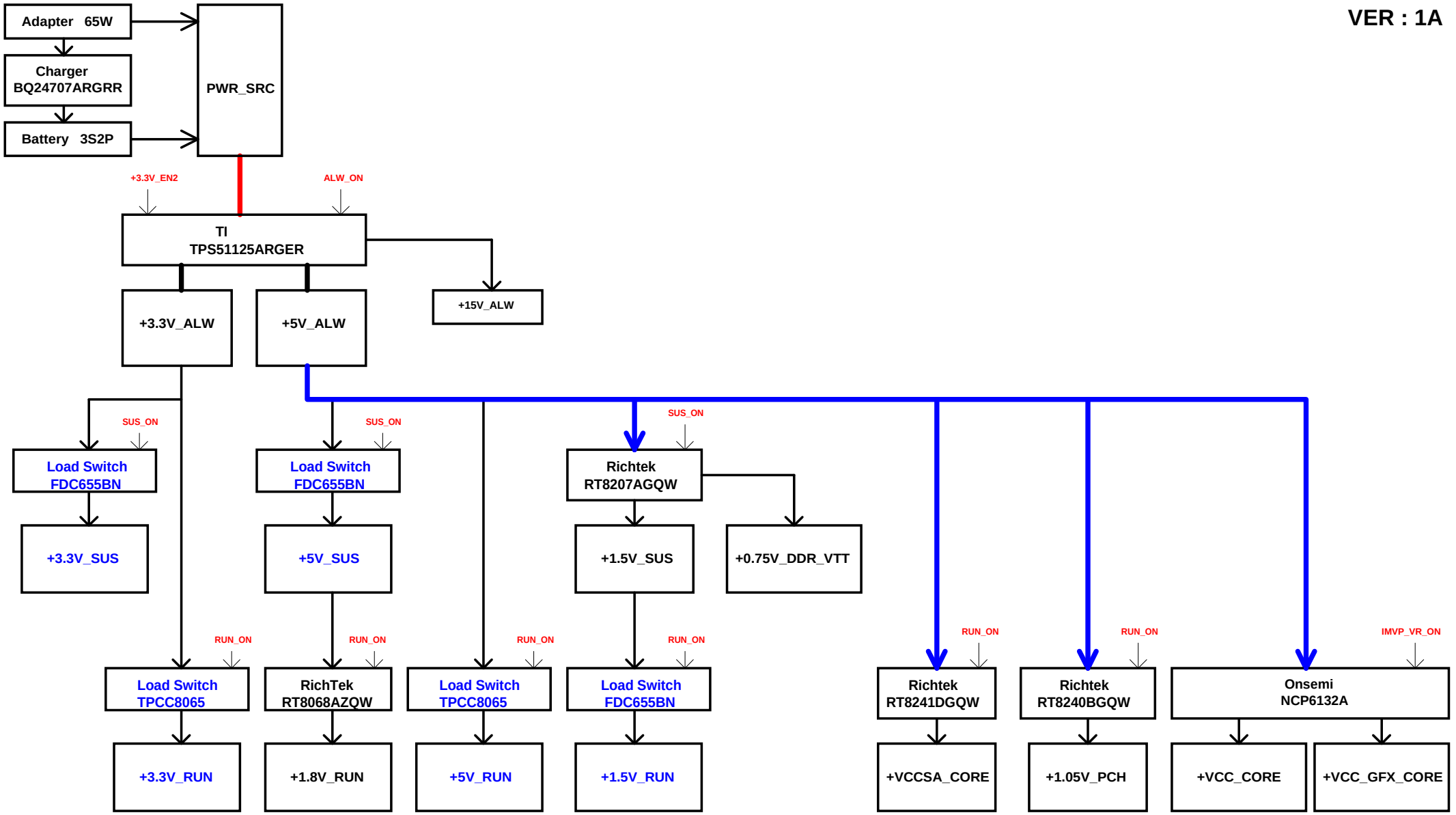
VER : 1A



Quanta Computer Inc.

PROJECT : D13

Size	Document Number	Rev
	Power Block Diagram	1A

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