

MODEL NAME : *PLW00*
PCB NO : *LA-7451P*
BOM P/N : *TBD*
TBD

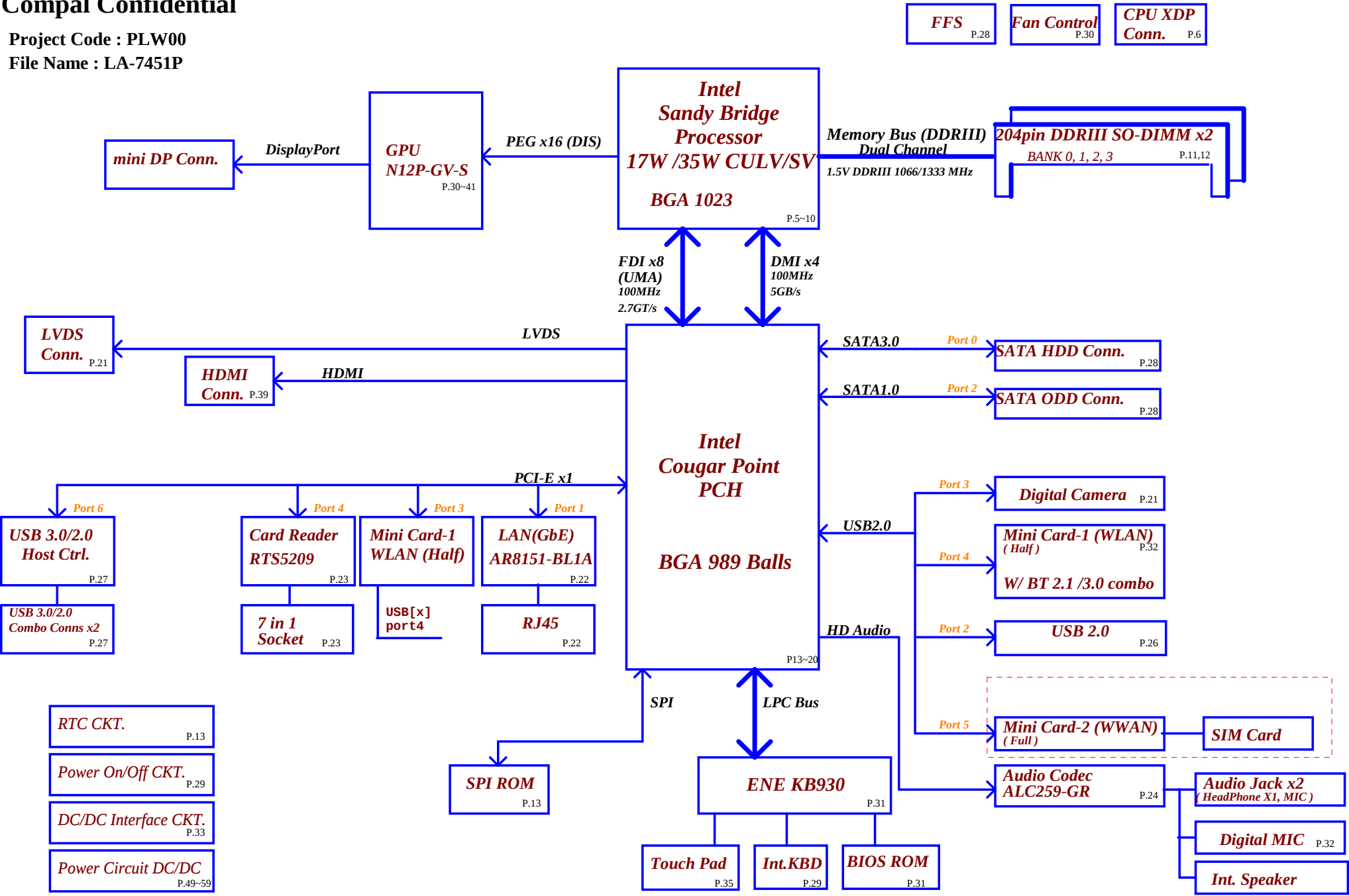
Dell/Compal Confidential
Schematic Document
Breitling (Huron River)
Sandy Bridge(BGA) + Cougar Point(standard)
DISCRETE VGA N12P-GV-S-A1 (optimus)

2011-07-12
Rev: 1.0

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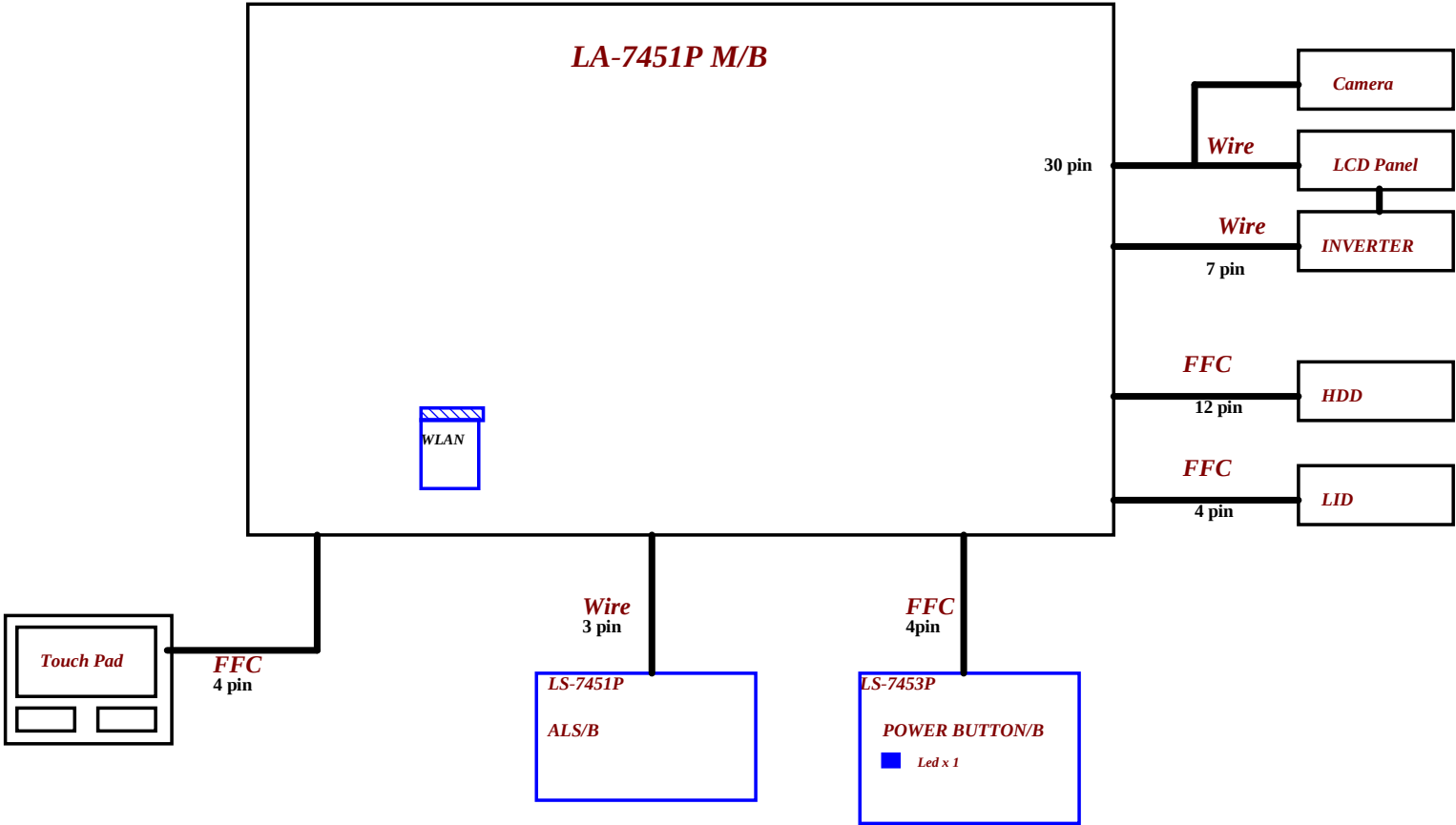
Project Code : PLW00
File Name : LA-7451P



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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC_AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

SMBUS Control Table

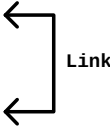
	SOURCE	BATT	SODIMM	SODIMM	FFS	VGA Thermal Sensor	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB930	V						
EC_SMB_CK2 EC_SMB_DA2	KB930							
PCH_SML0CLK PCH_SML0DATA	PCH							
PCH_SML1CLK PCH_SML1DATA	PCH						V	
MEM_SMBCLK MEM_SMBDATA	PCH		V	V	V			V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

PCH

USB PORT#	DESTINATION
0	None
1	JUSB1 (2.0 Ext UP Side)
2	None
3	CAMERA
4	JMINI1 (WLAN)
5	JMINI2 (WWAN)
6	None
7	None
8	None
9	None
10	None
11	None
12	None
13	None

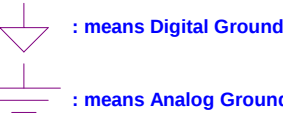


CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

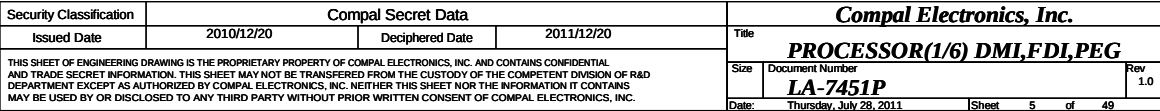
SATA	DESTINATION
SATA0	HDD
SATA1	ODD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

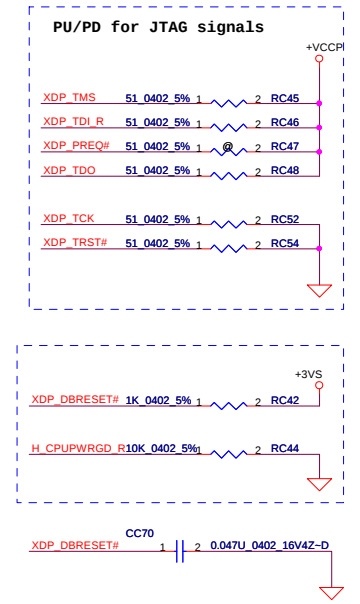
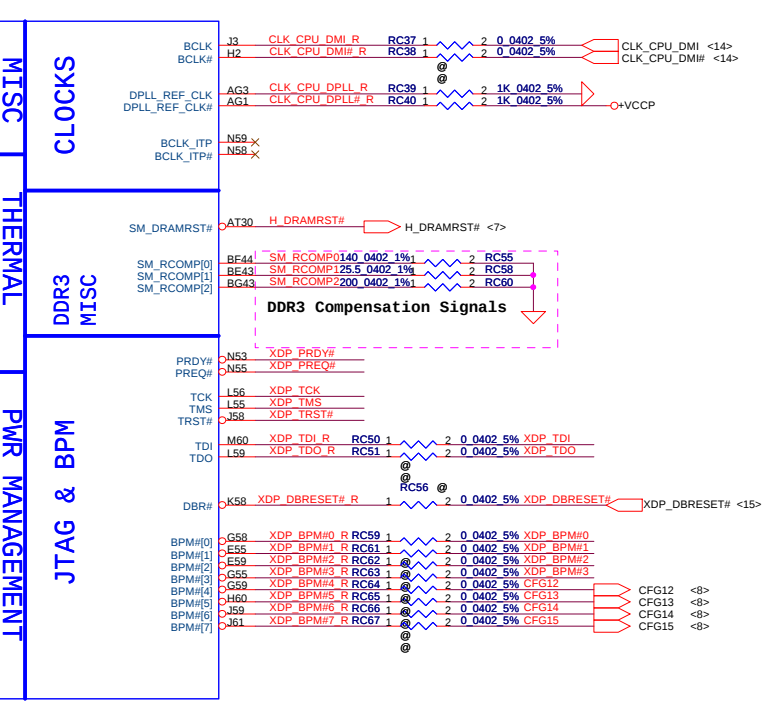
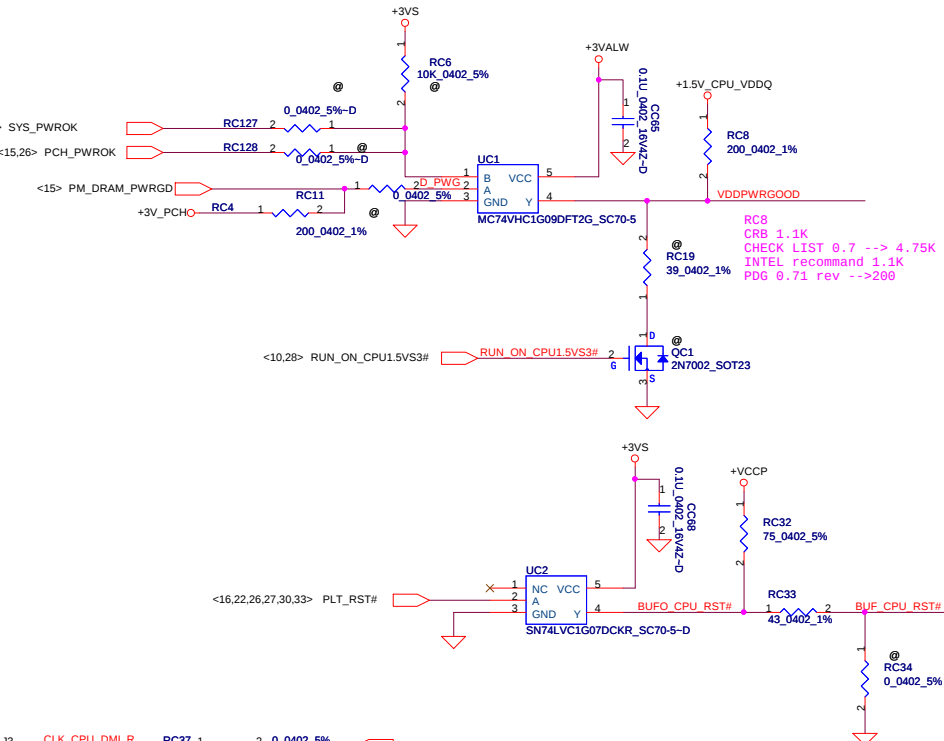
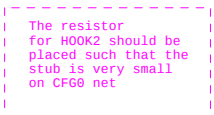
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	None
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

Symbol Note :



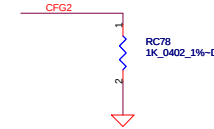
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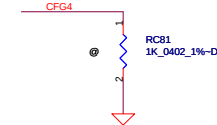


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					Size	Document Number		Rev
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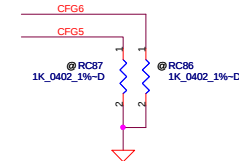
CFG Straps for Processor



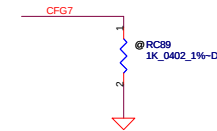
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	*1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



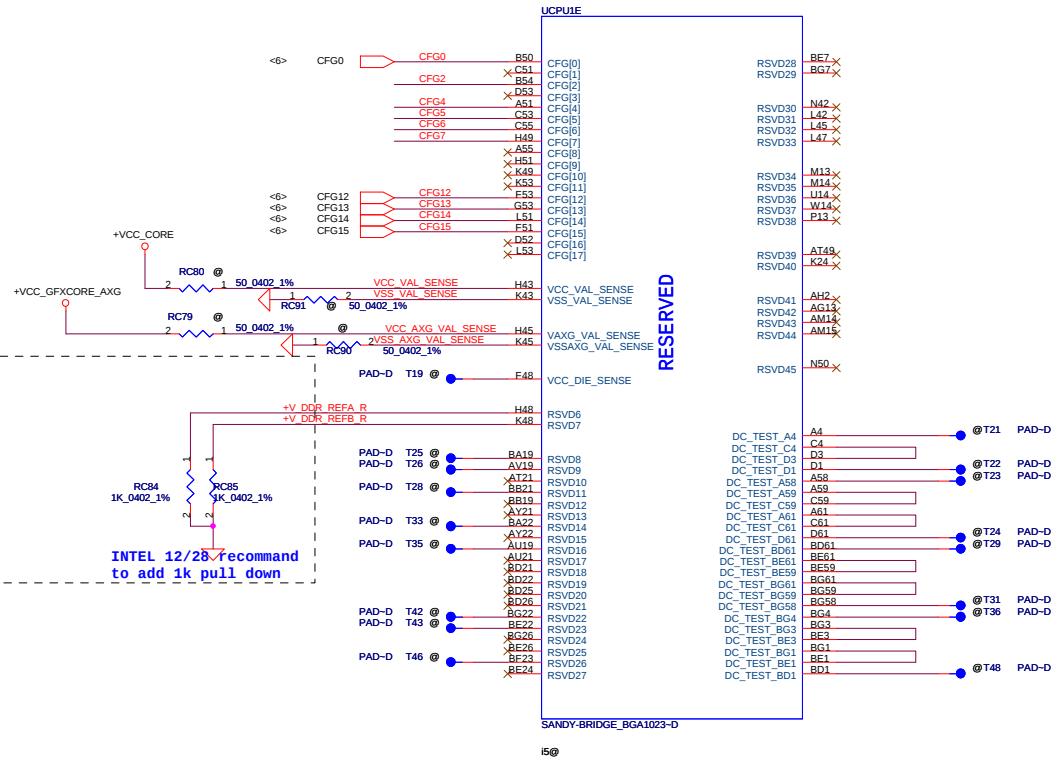
Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

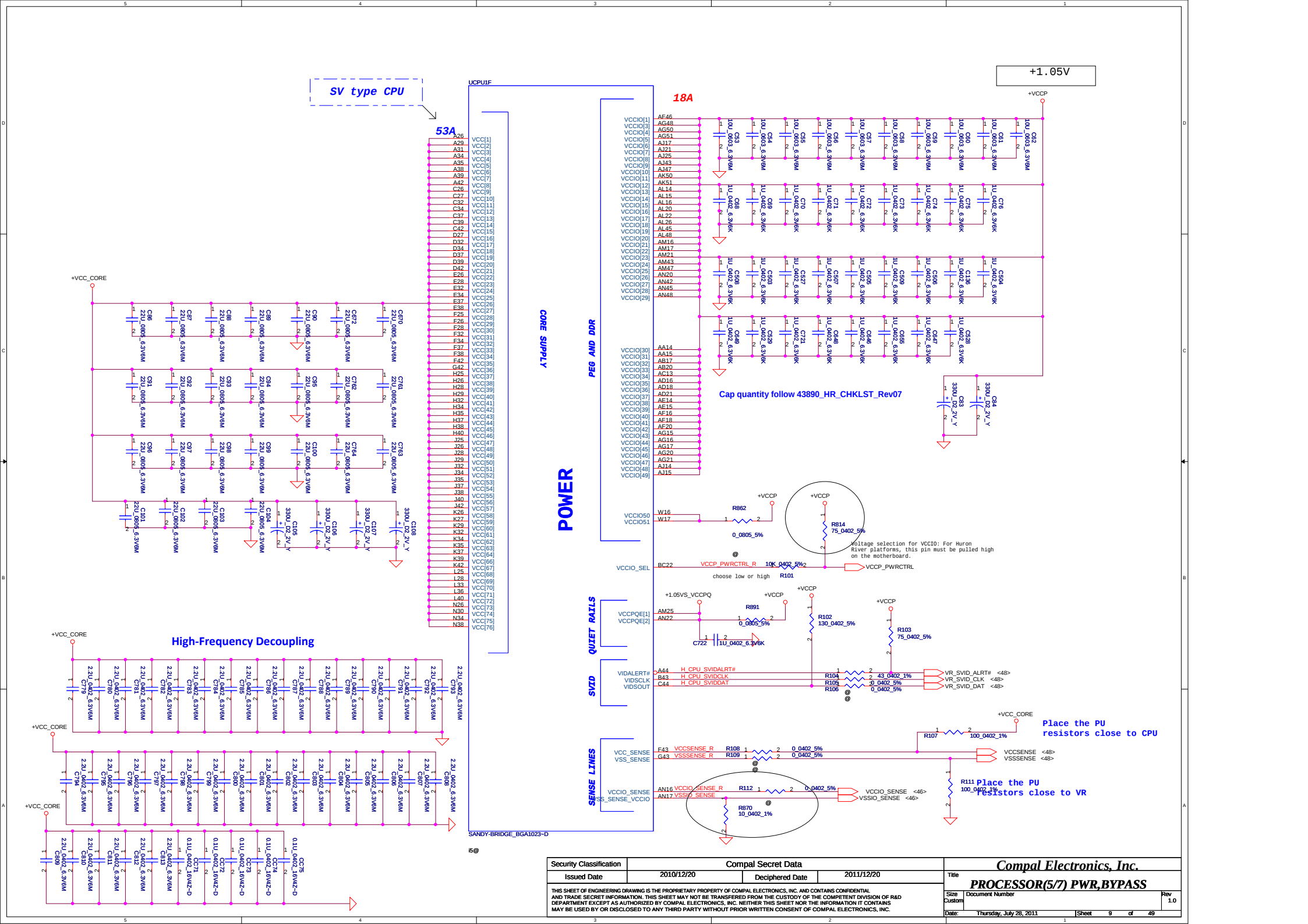


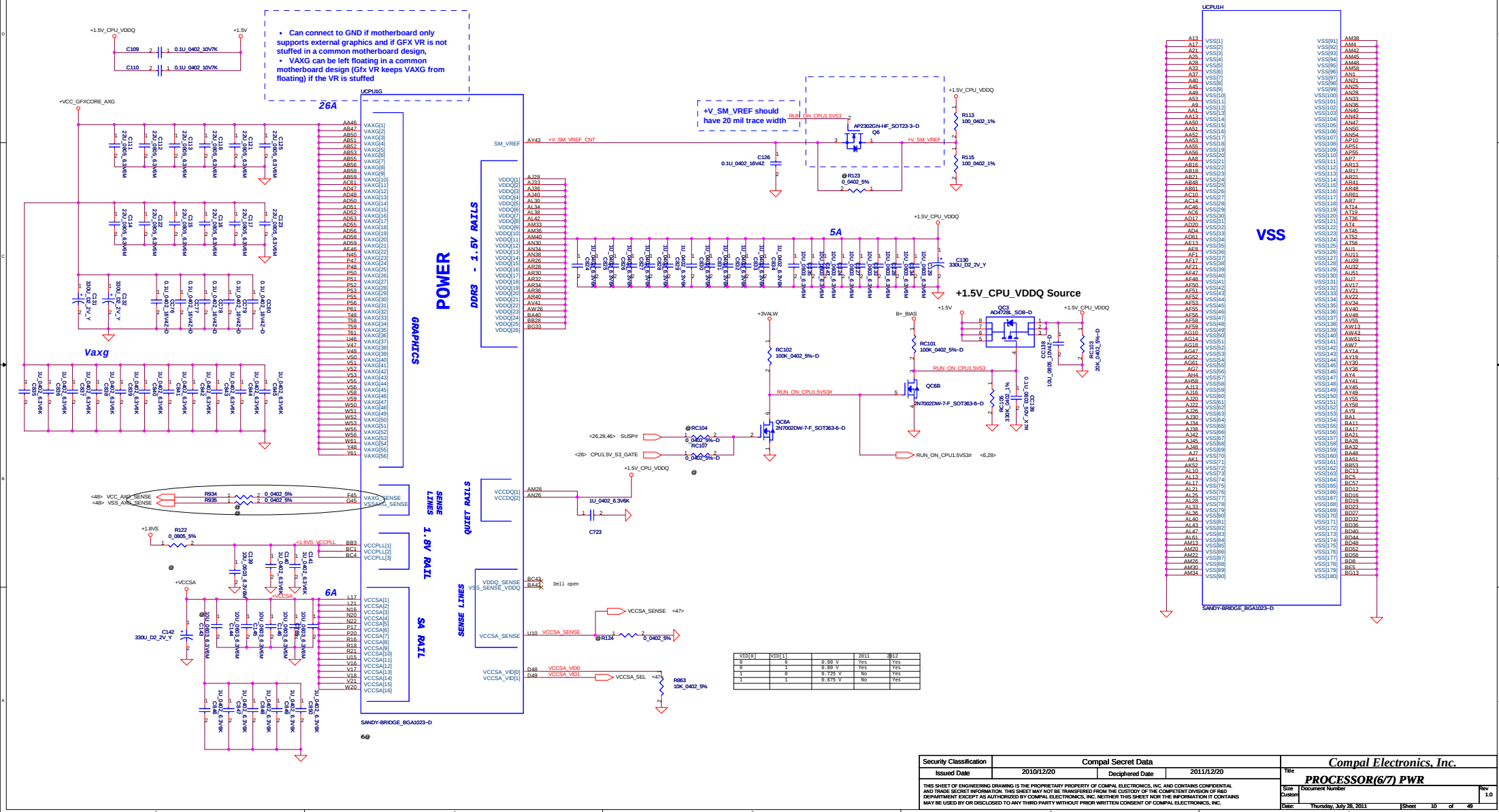
PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



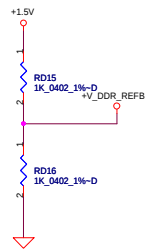




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Issued Date	2010112/20	Deciphered Date	2011112/20	Title PROCESSOR(6) PWR
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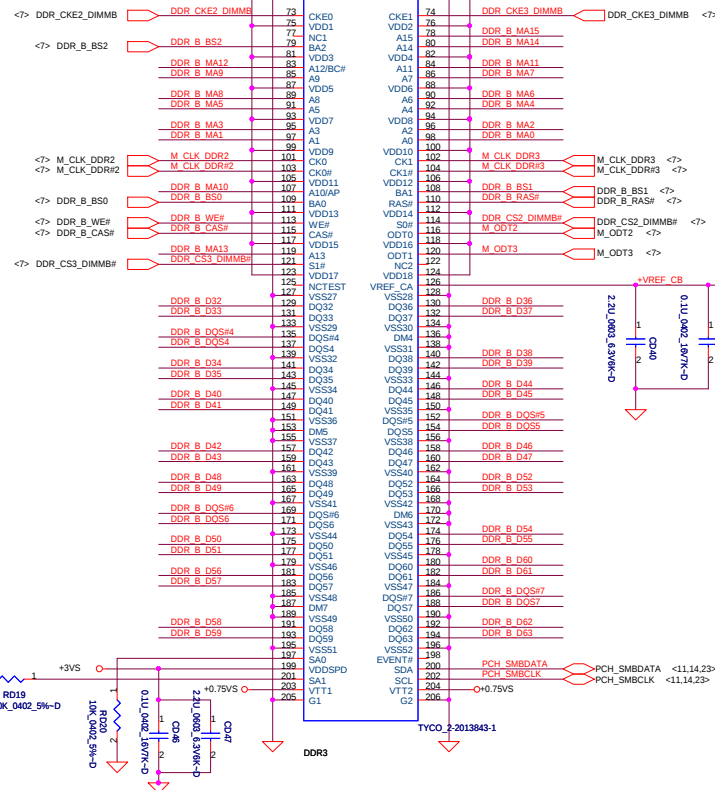
<7> DDR_B_DQS#[0..7]
<7> DDR_B_DQS#[0..7]
<7> DDR_B_DQ[0..63]
<7> DDR_B_MA[0..15]

Layout Note:
Place near JDIMMB

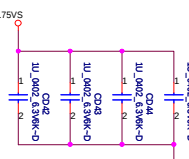


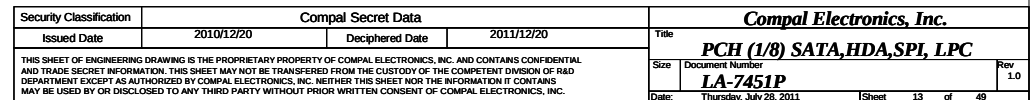
All VREF traces should
have 10 mil trace width

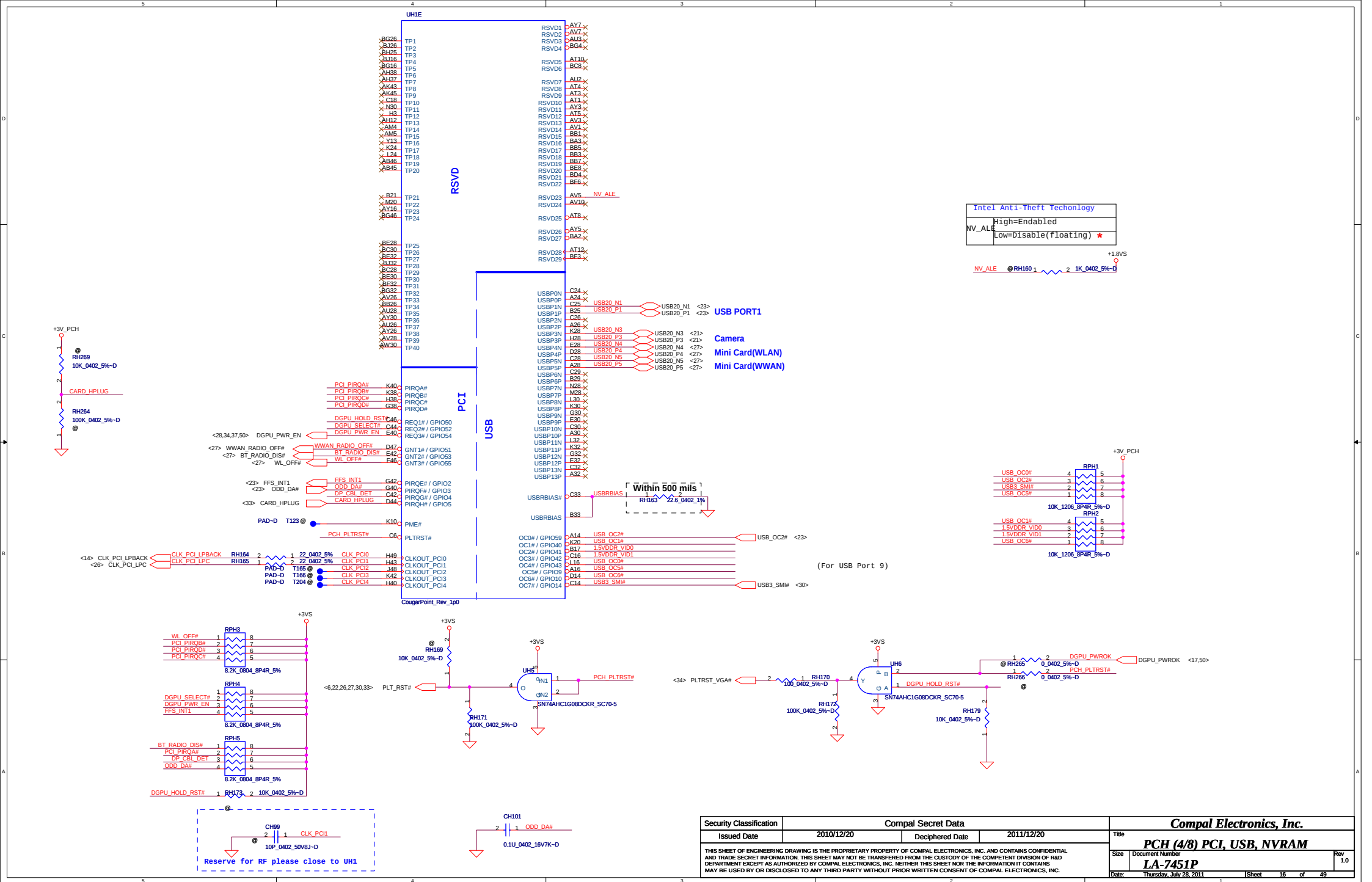
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



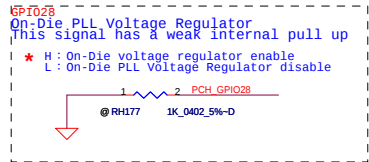
Layout Note:
Place near JDIMMB.203,204





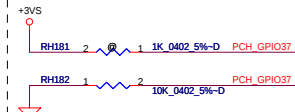


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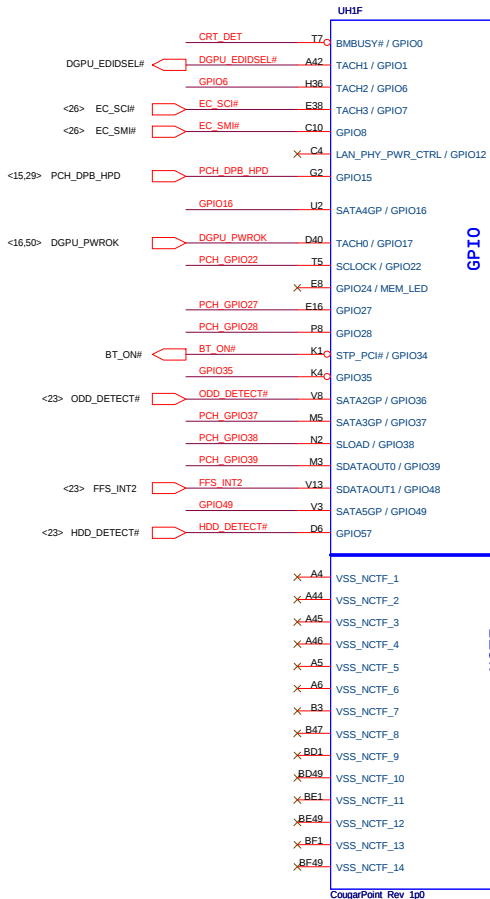
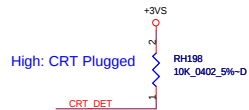
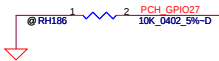
PCH_GPIO37
FDI TERMINATION VOLTAGE OVERRIDE

★ LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)



GPI027
PCH_GPIO27 (Have internal Pull-High)

★ High: VCCVRM VR Enable
Low: VCCVRM VR Disable



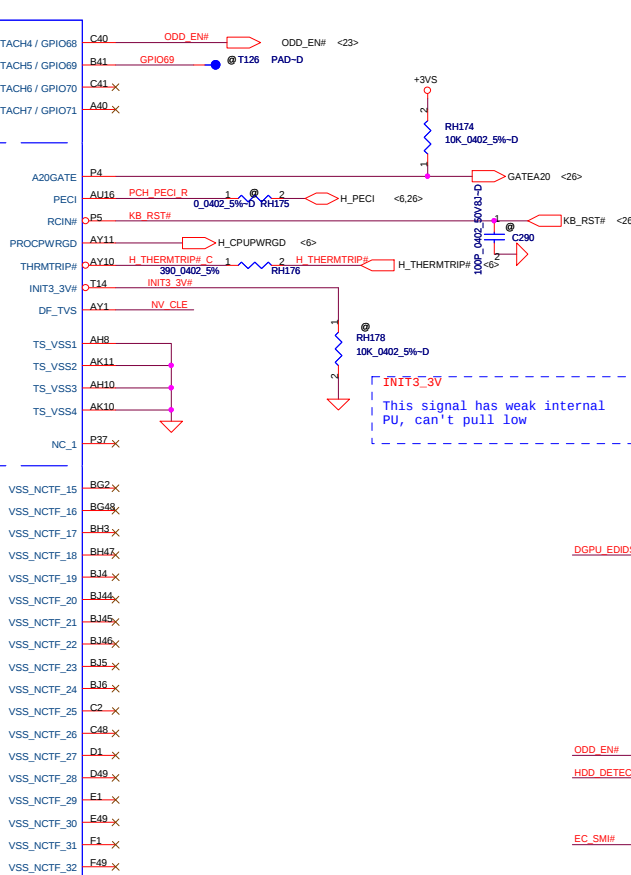
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 0.5

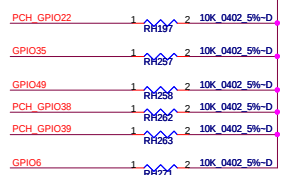
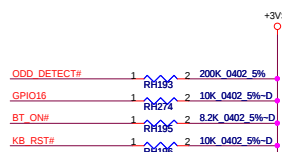
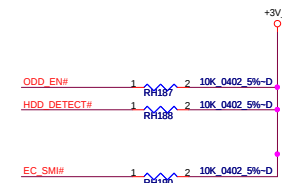
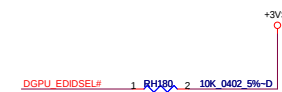
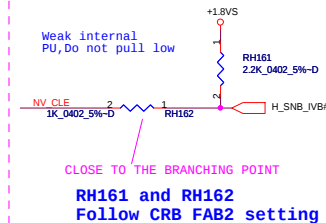
GPIO

CPU/MISC

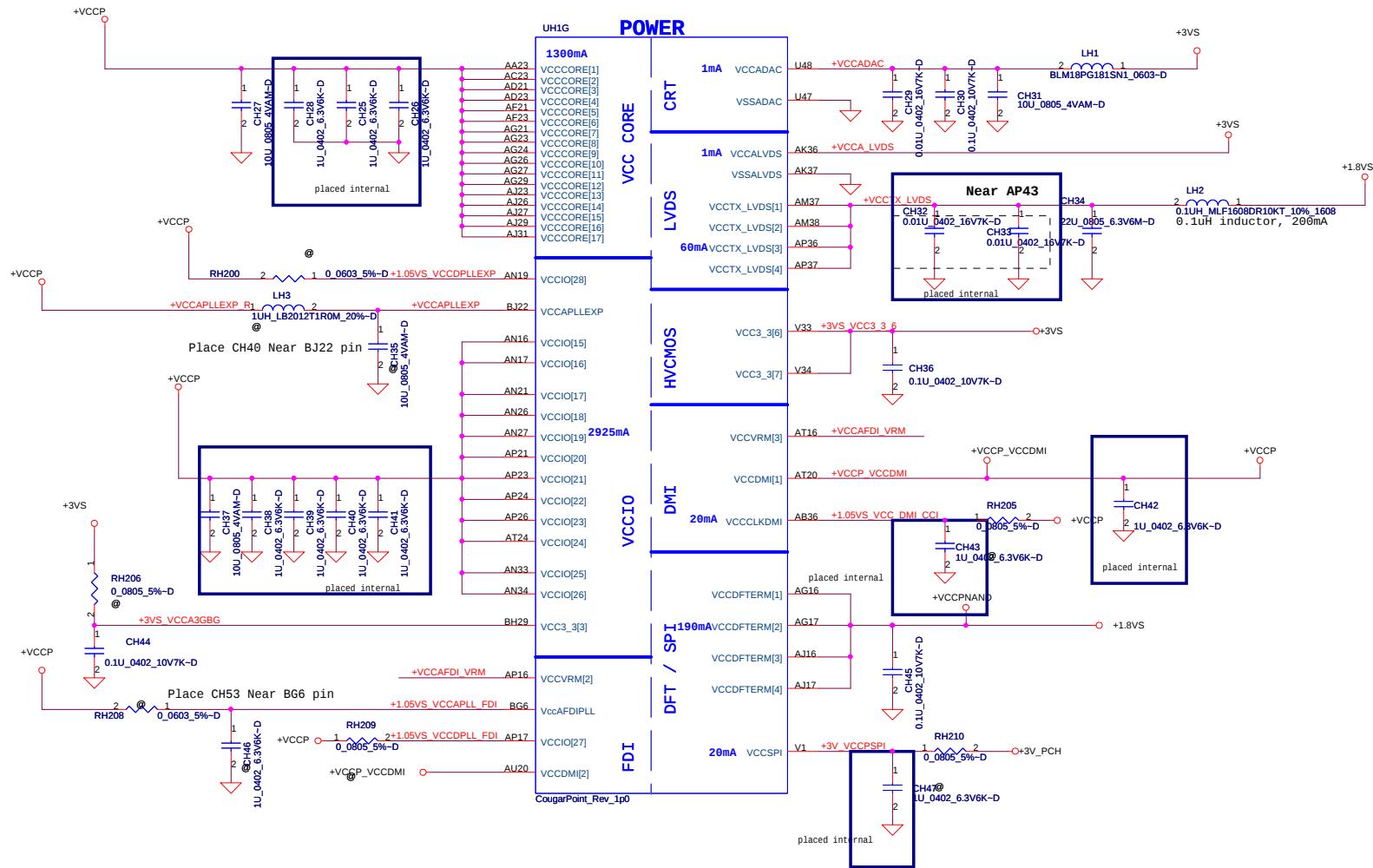
NCTF



DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

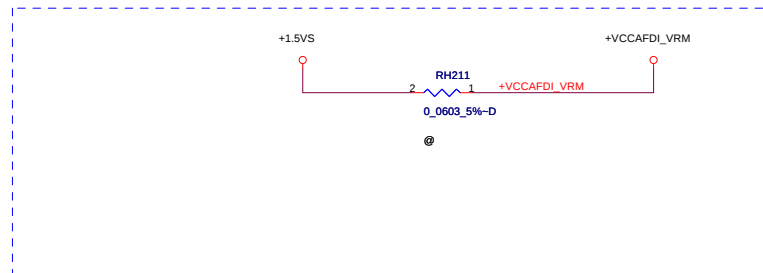


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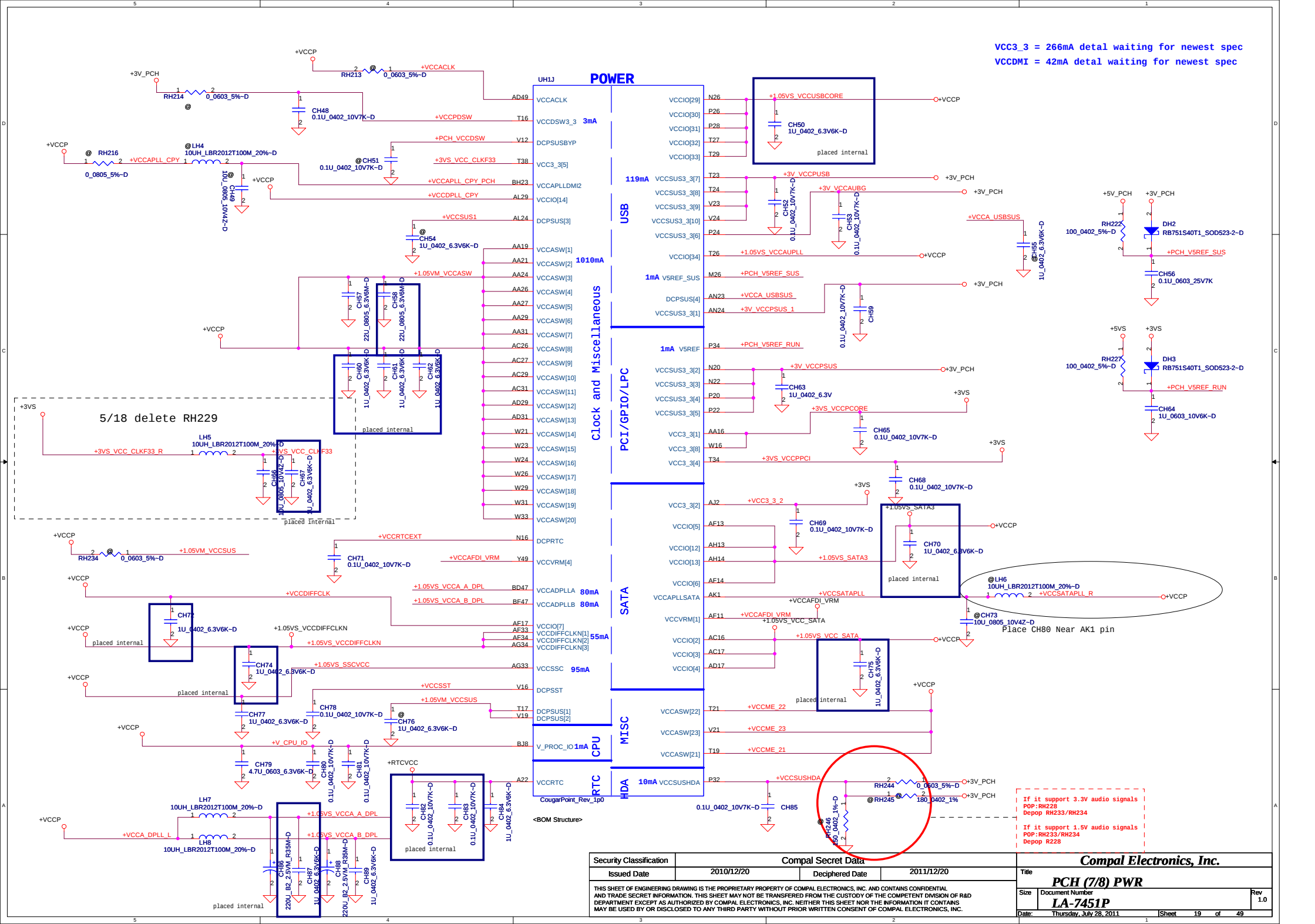


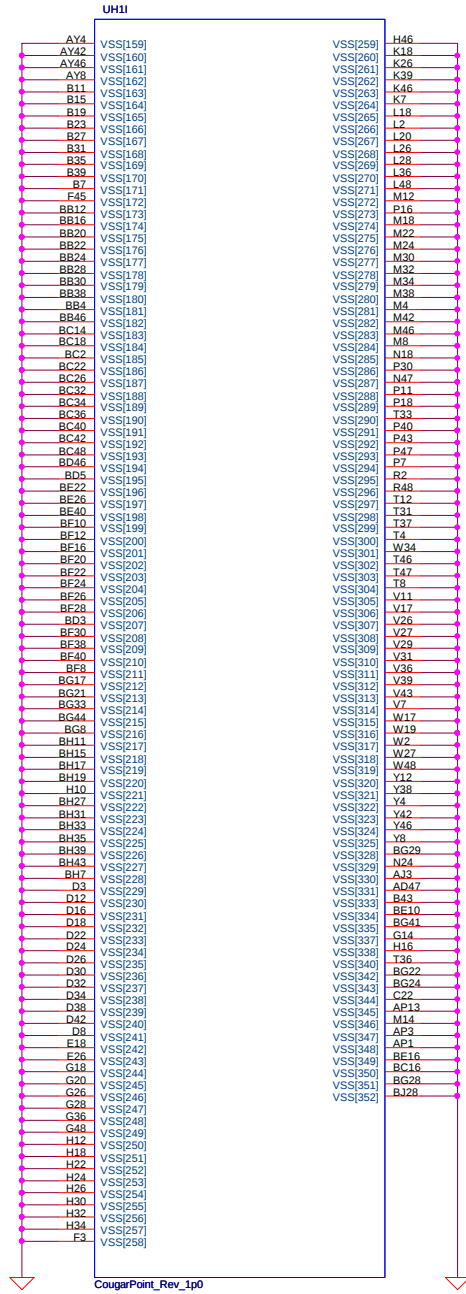
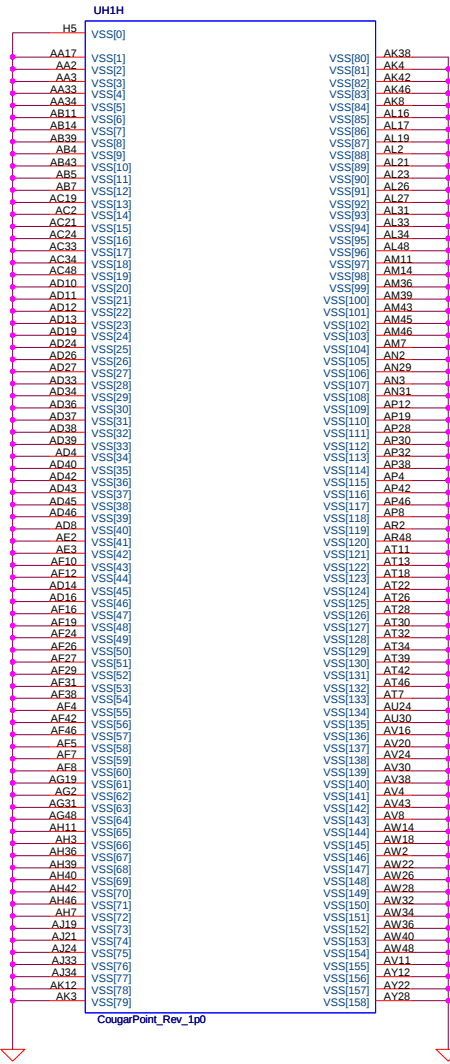
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCCVRM = 160mA detail waiting for newest spec



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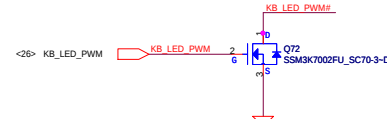
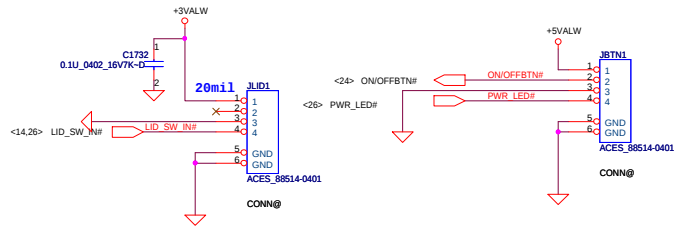




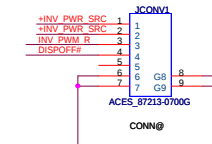
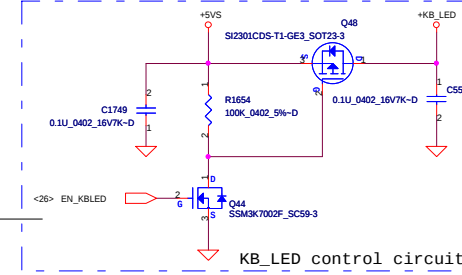
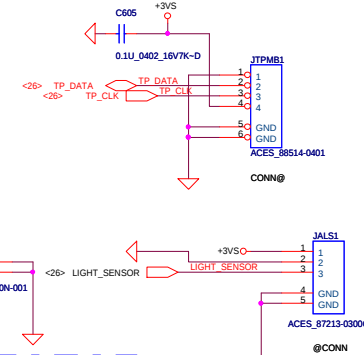
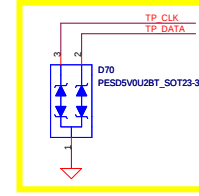
LOGO Board CONN

PWR BTN Board CONN

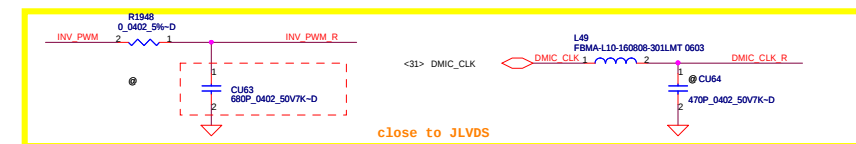
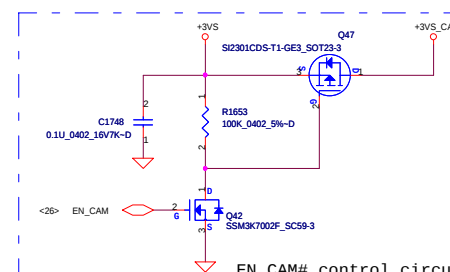
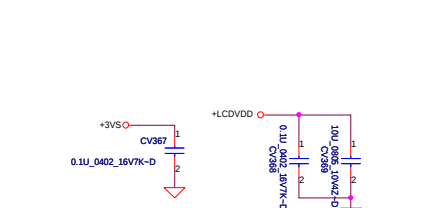
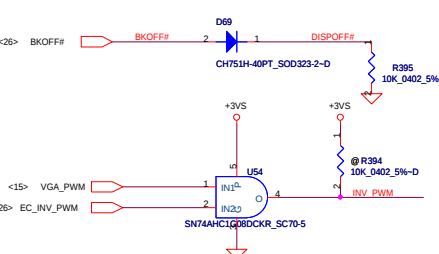
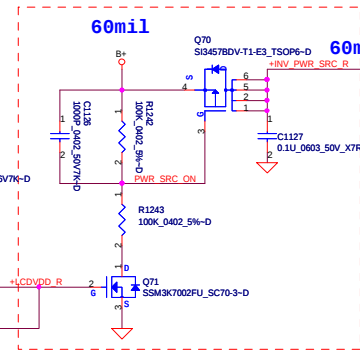
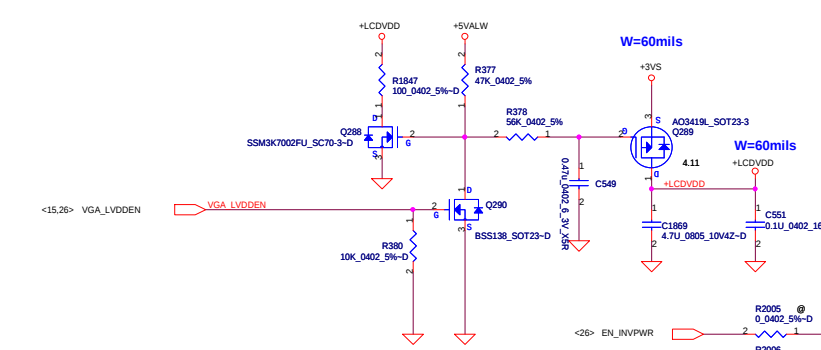
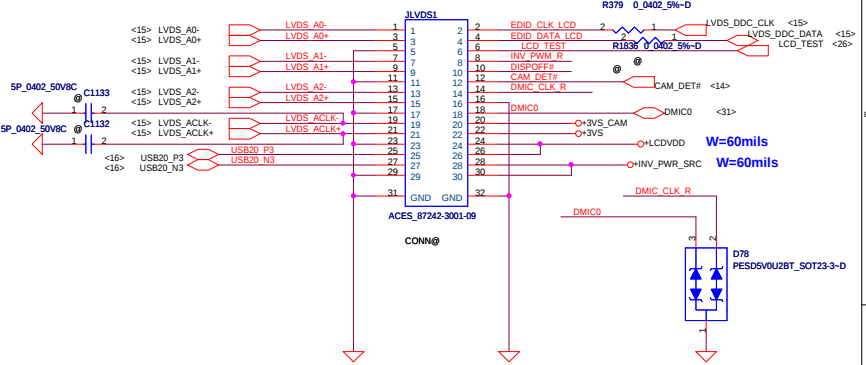
Touchpad CONN



close to JTPMB 7/26



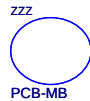
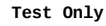
LVDS Conn.



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Issued Date	2010/12/20	Declassified Date	2011/12/20	Rev: 1.0
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Power Button



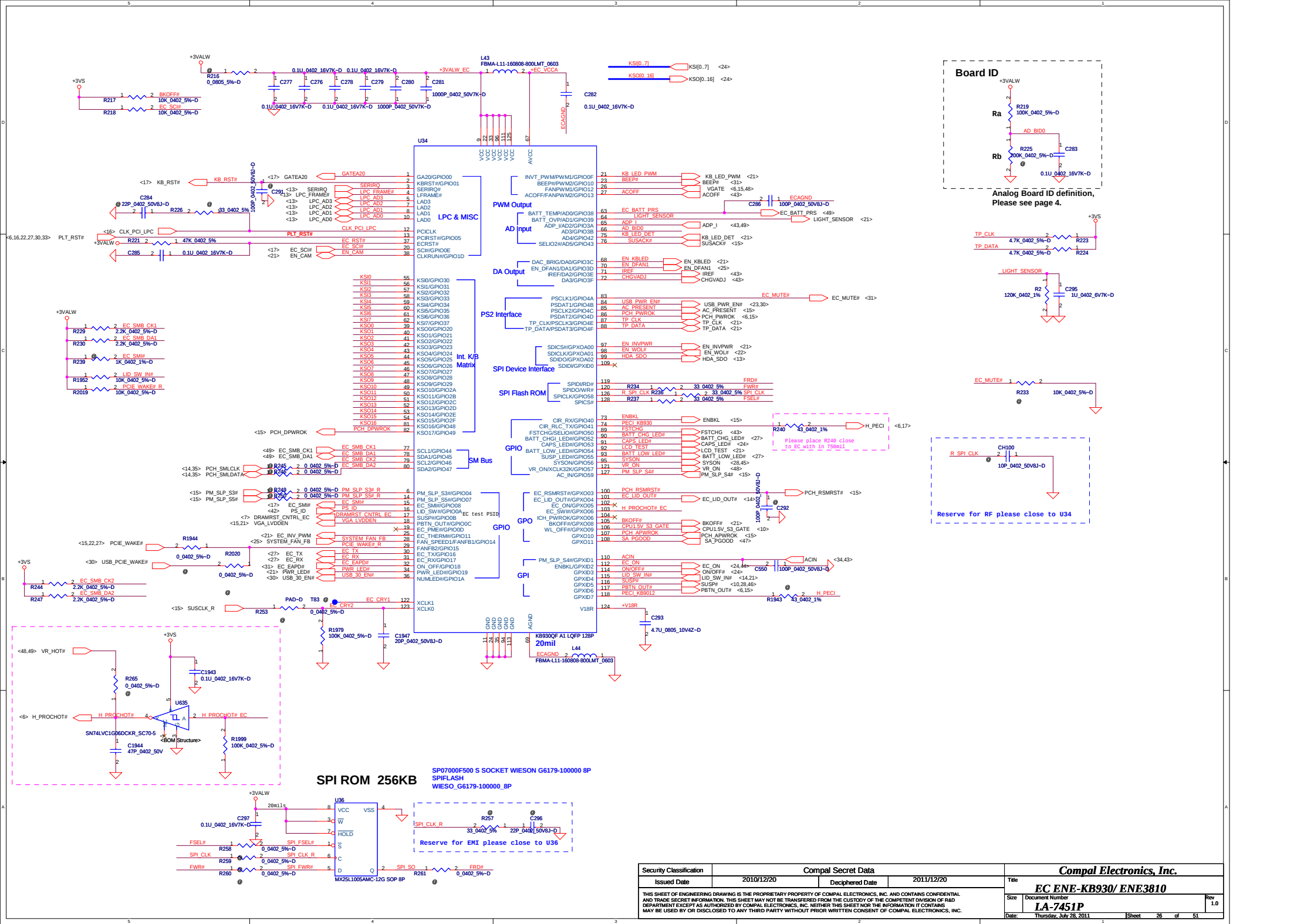
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FAN Control circuit

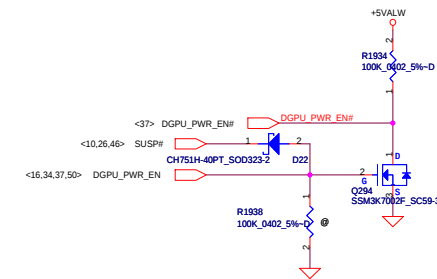
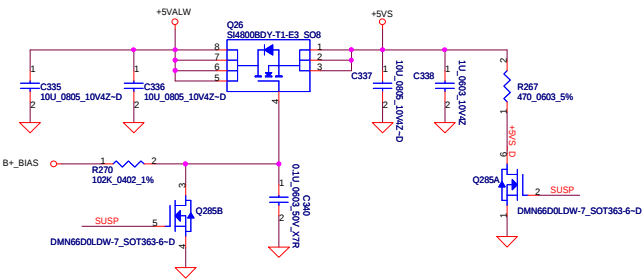
The schematic shows the following components and connections:

- Inputs:** +FAN_POWER, +5VS, +3VS.
- Capacitors:**
 - C1923: 2.2U_0603_6.3V6K-D
 - C1083: 1000P_0402_50V7K
 - C1924: 2.2U_0603_6.3V6K-D
 - C1091: 0.01U_0402_16V7K
- Resistor:** R939: 10K_0402_5%
- IC:** U30: APE8873M SO 8P
- Connectors:** JFAN1 (ACES_85204-0300N), CONN@.
- Labels:** <26> EN_DFAN1, <26> SYSTEM_FAN_FB, 40mil.

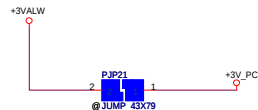
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Issued Date	2010/12/20	Deciphered Date	2011/12/20	Title FAN Controller			
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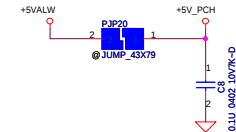
+5VALW to +5VS



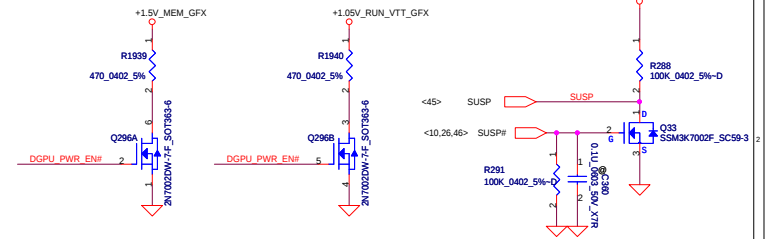
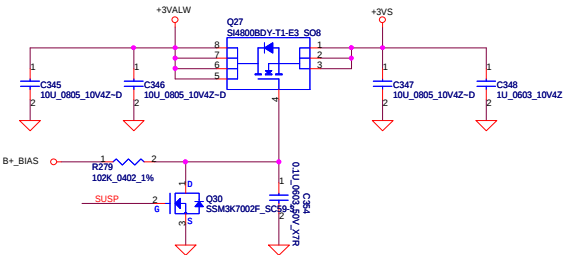
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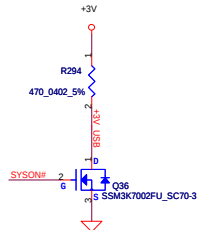
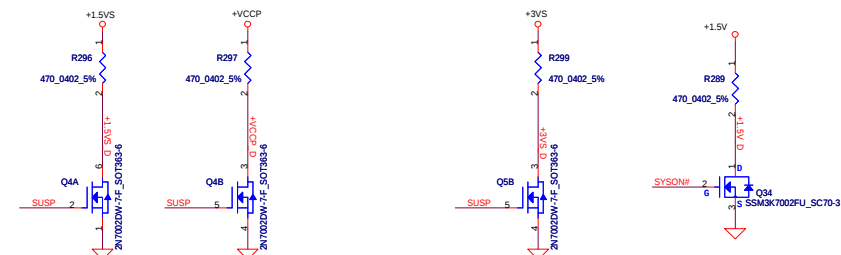
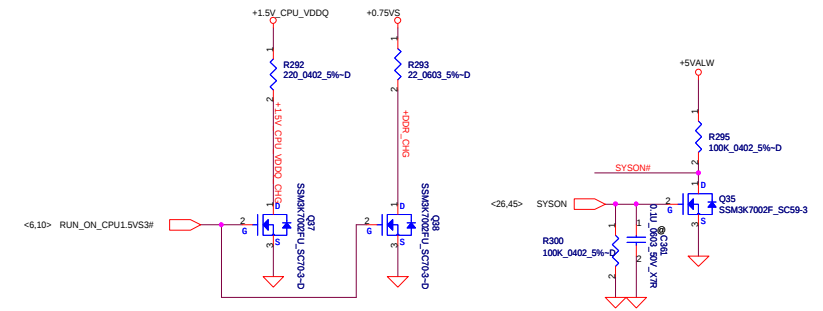
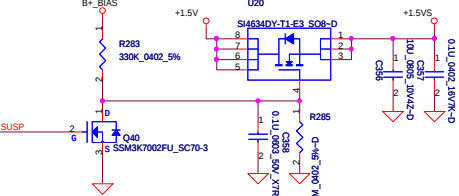
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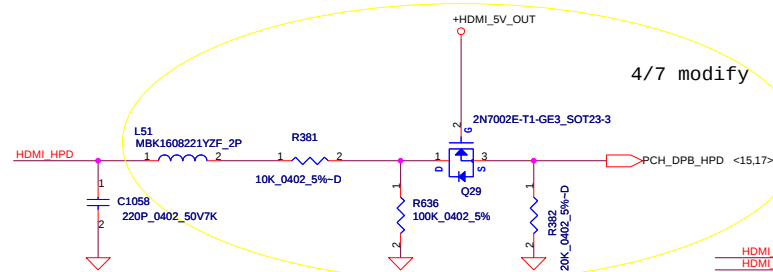
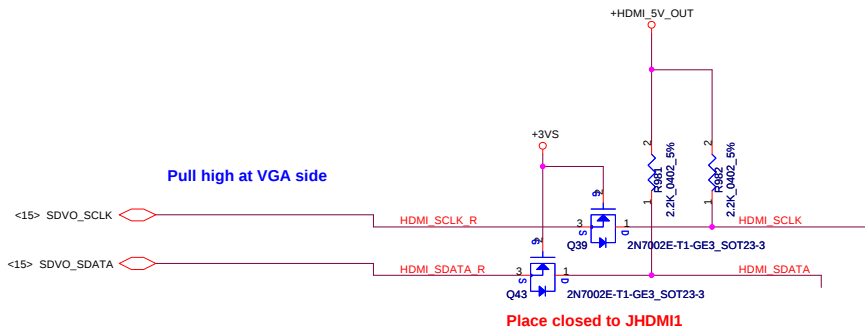
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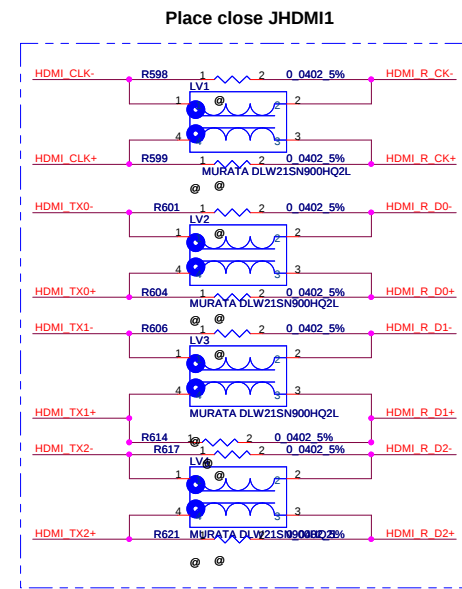
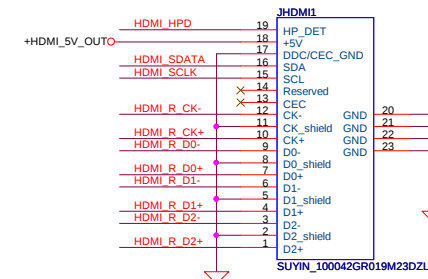
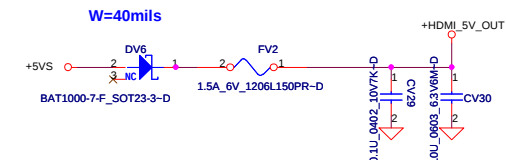
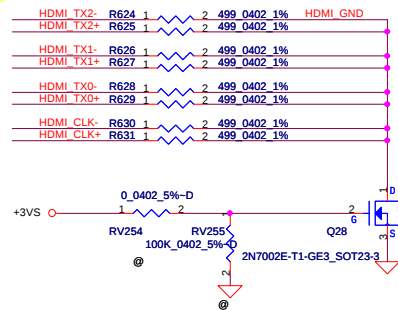
+1.5V To +1.5VS



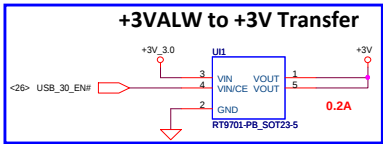
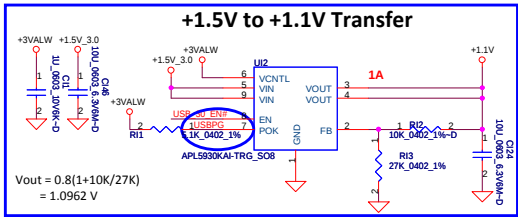
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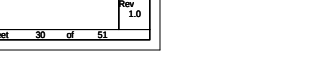
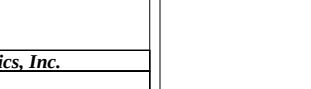
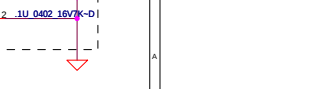
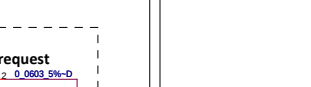
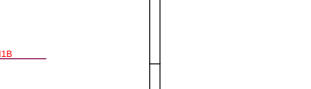
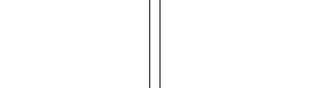
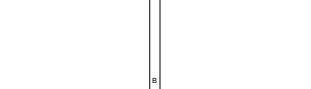
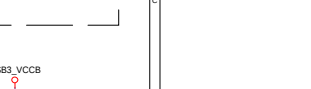
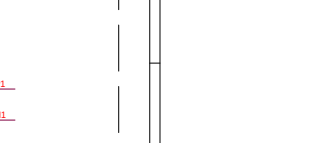
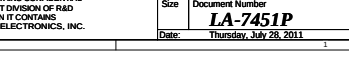
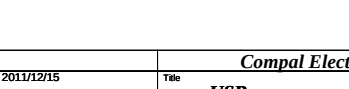
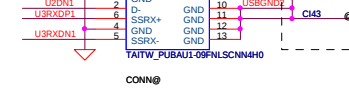
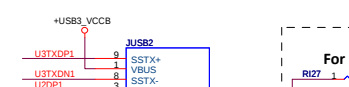
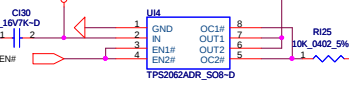
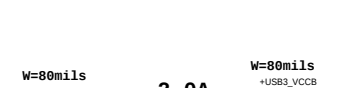
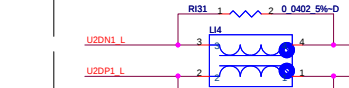
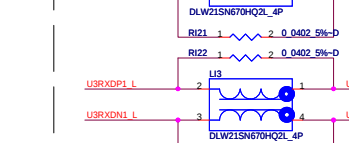
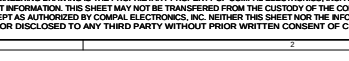
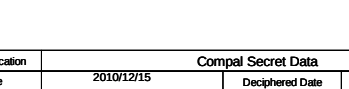
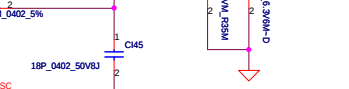
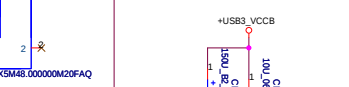
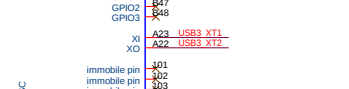
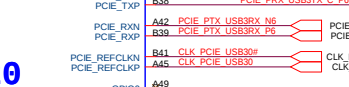
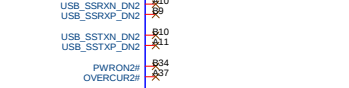
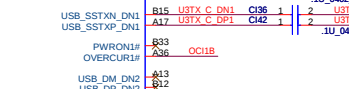
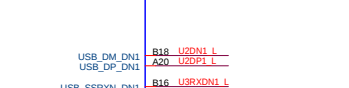
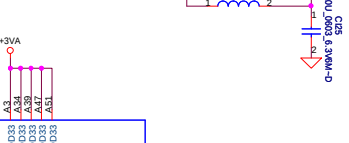
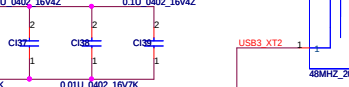
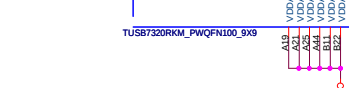
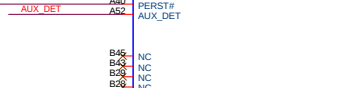
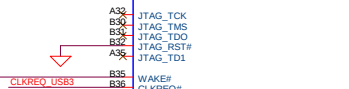
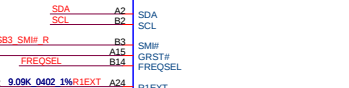
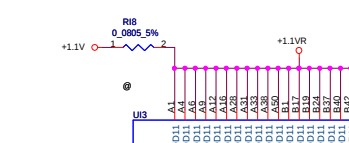
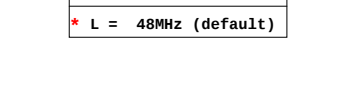
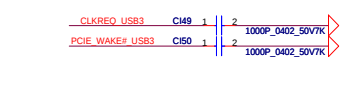
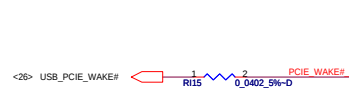
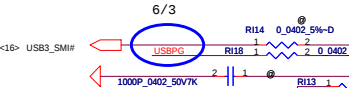
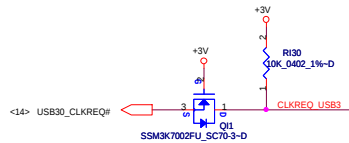
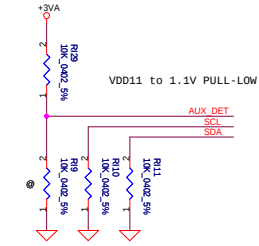
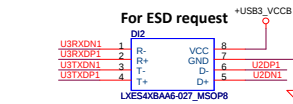
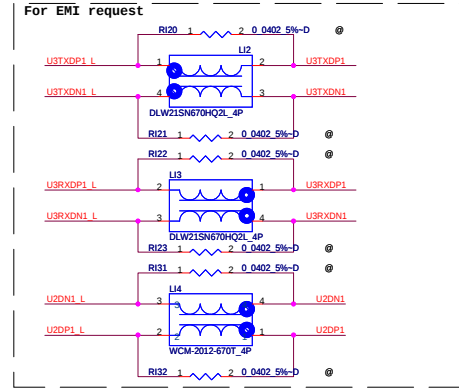
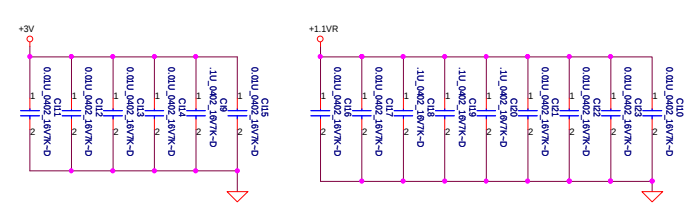
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7K for customer request, can use other kind of capacitor, like Y5V.



TUSB7320

TUSB7320RKM_PWQFN100_9x9

VSS_OSC

VSS_OSC

VSS_OSC

VSS_OSC

VSS_OSC

VSS_OSC

VSS_OSC

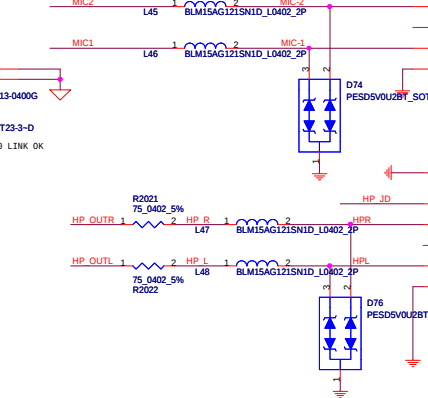
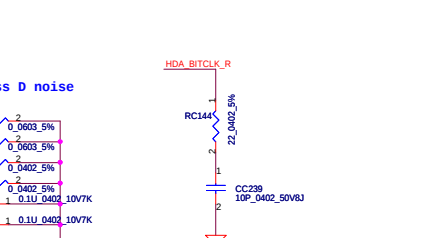
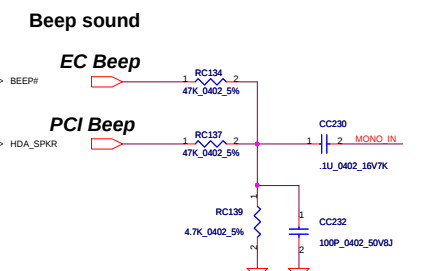
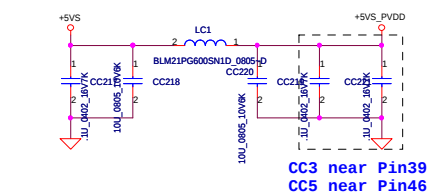
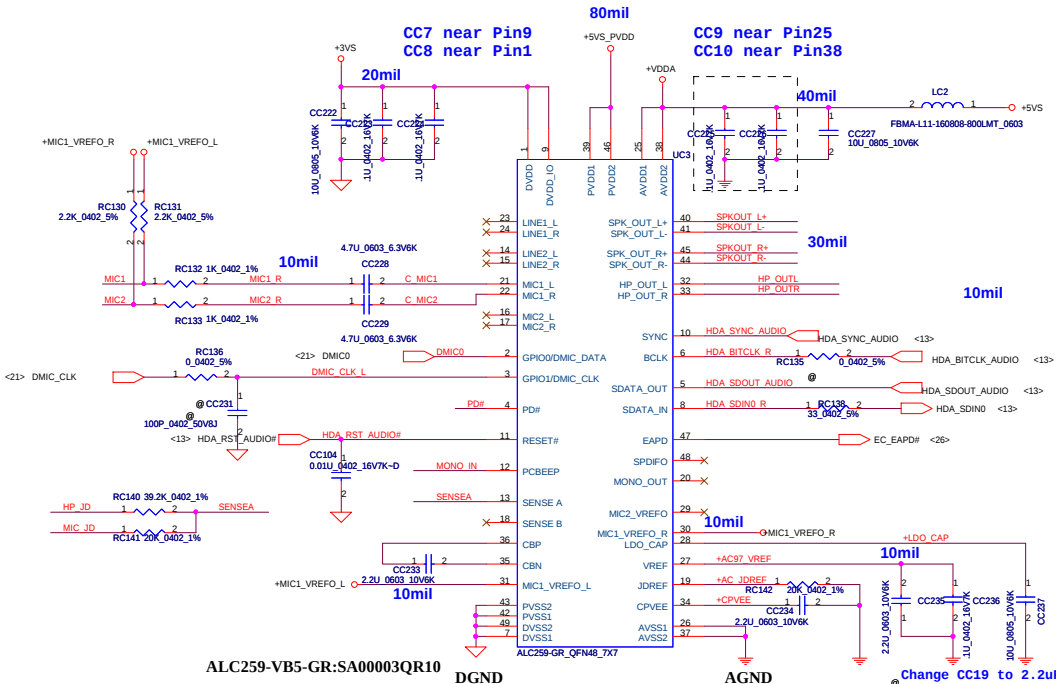
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VSS_OSC

VSS_OSC

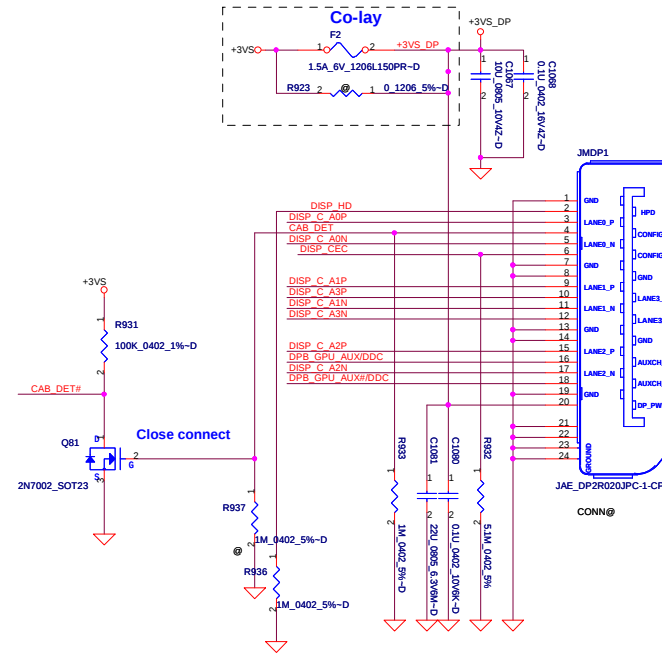
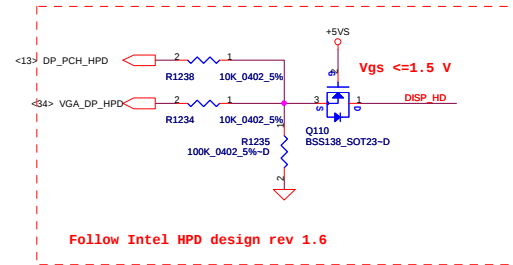
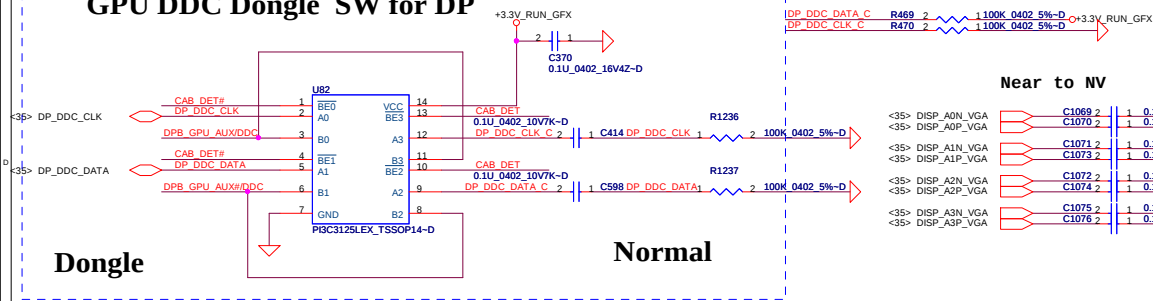
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For Power on/off de-pop circuit and system booting warning signal:
Please system BIOS Engineer Note:
1.If you want the system make warning signal after power on
Please let EC_MUTE# high first
2.When you want to exit your BIOS programming code
Please let EC_MUTE# Low.
(The programming is difference from before)

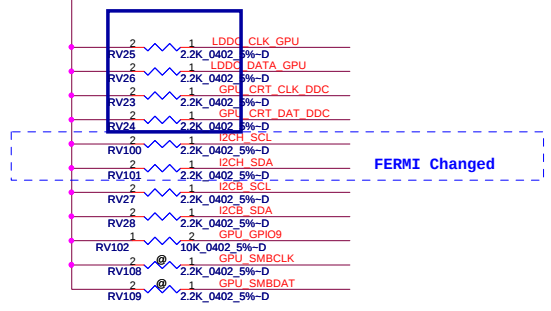
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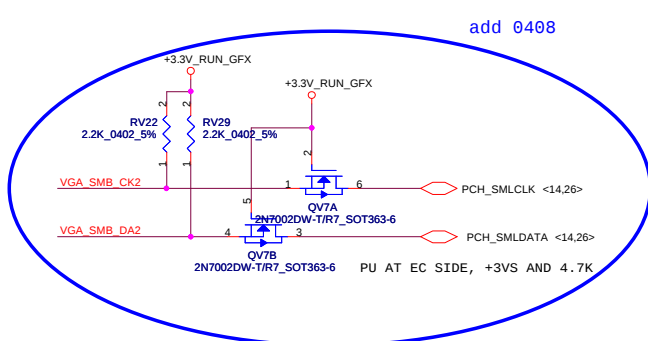
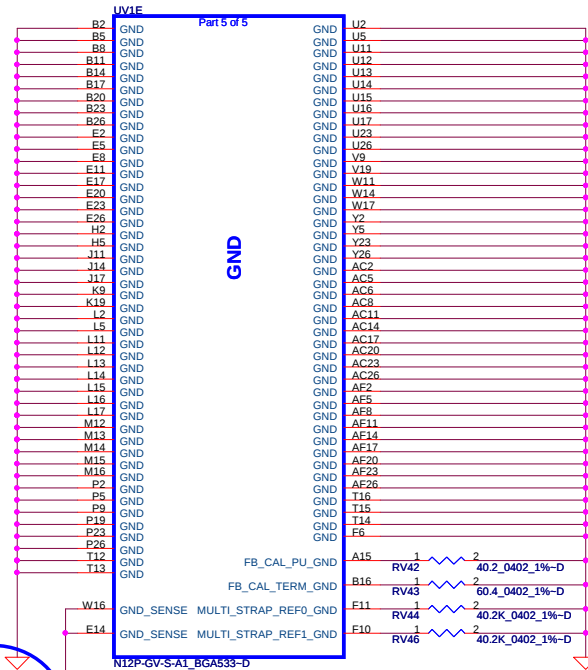
GPU DDC Dongle SW for DP



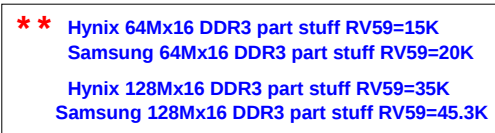
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Issued Date	2009/07/25	Deciphered Date	2011/07/06	Title	mini DP	
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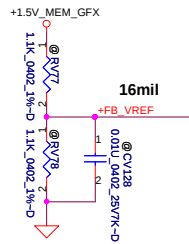




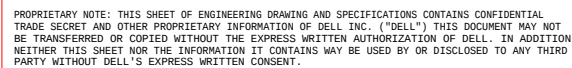
ROM_SCLK	PCIDEVID_EXT, SUB_VENDOR, SLOT_CLK, PEX_PLL_EN
ROM_SI	RAM_CFG[3:0]
ROM_SO	XLCK_417, FB_0_BAR_SIZE, ALT_AD00R, VGA_DEVICE



STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]

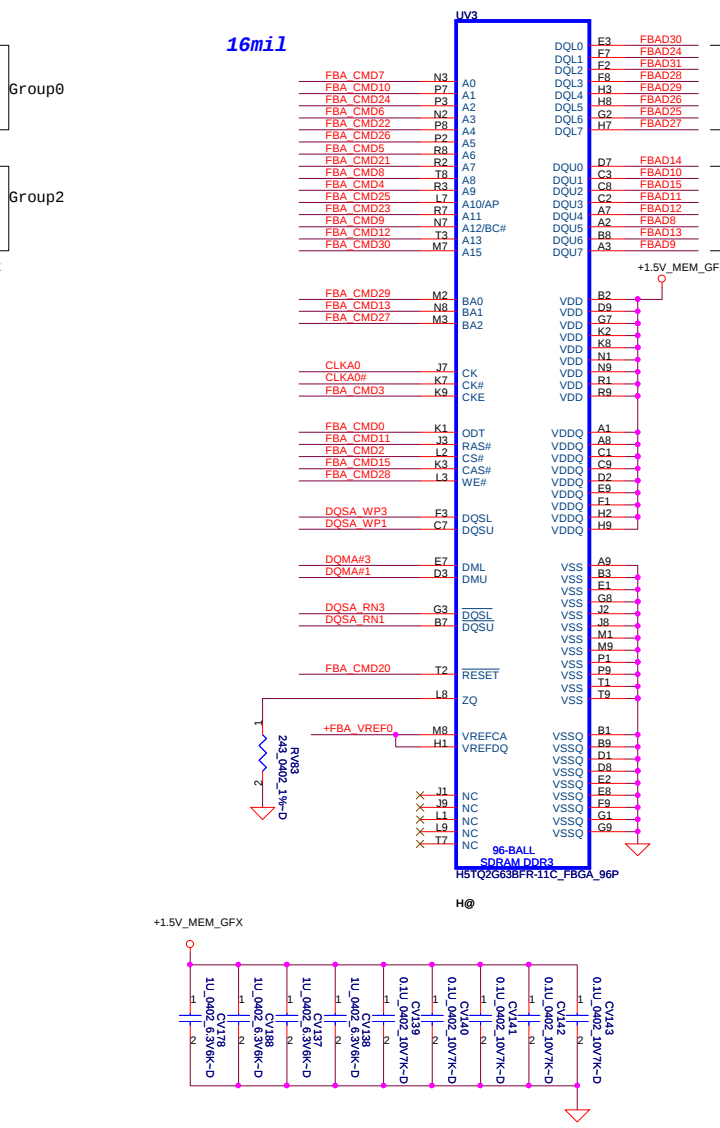
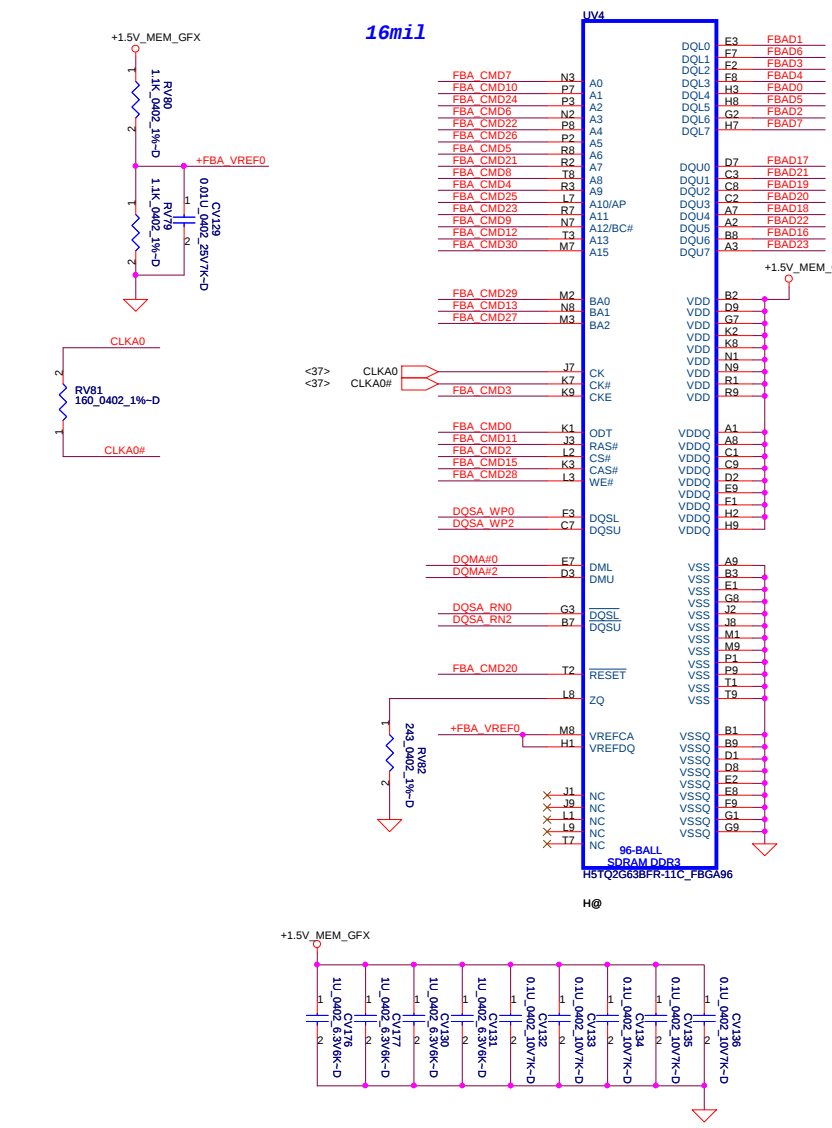


	DATA Bus	
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2



Memory Partition A - Lower 32 bits

change to Hynix



Mode E - Mirror Mode Mapping

DATA Bus	
Address	0..3132..63
CMD0	ODT_L
CMD1	CS1#_L
CMD2	CS0#_L
CMD3	CKE_L
CMD4	A9A11
CMD5	A6A7
CMD6	A3BA1
CMD7	A0A12
CMD8	A8A8
CMD9	A12A0
CMD10	A1A2
CMD11	RAS#RAS#
CMD12	A13A14
CMD13	BA1A3
CMD14	A14A13
CMD15	CAS#CAS#
CMD16	CKE_H
CMD17	CS1#_H
CMD18	CS0#_H
CMD19	ODT_H
CMD20	RST
CMD21	A7A6
CMD22	A4A5
CMD23	A11A9
CMD24	A2A1
CMD25	A10WE#
CMD26	A5A4
CMD27	BA2A15
CMD28	WE#A10
CMD29	BA0BA0
CMD30	A15BA2

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Title

VRAM A Lower

Size

Document Number

LA-7451P

Date

Thursday, July 28, 2011

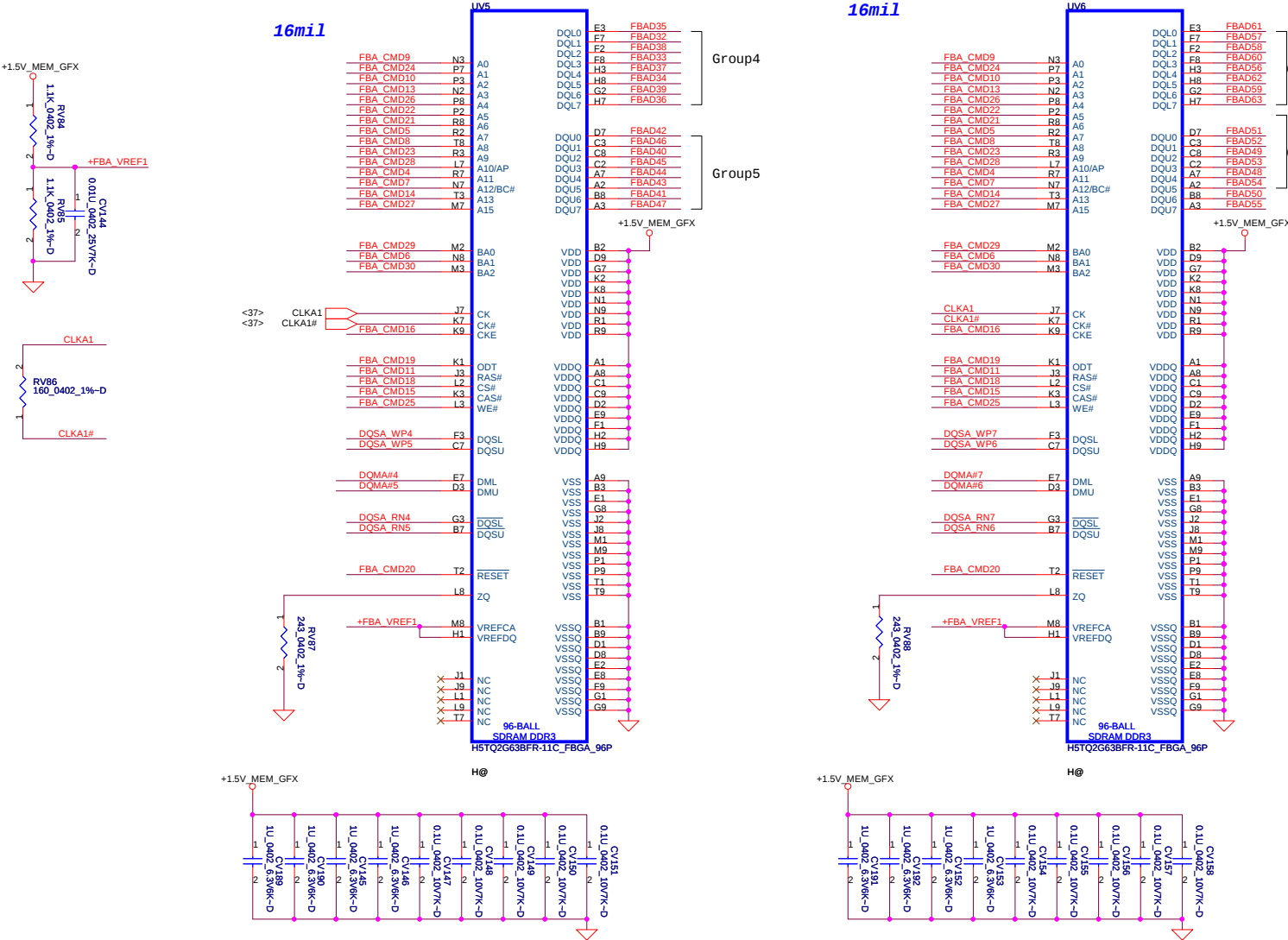
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Rev

1.0

Memory Partition A - Upper 32 bits



Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

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Version change list (P.I.R. List)

EE section

Item	Reason for change	PG#	Modify List	Date	Phase
1	SMBus signal Pull HIGH	15	Add R983, R984	2011/04/07	PT
2	SMBus signal Pull HIGH	25	Add RV22, RV29, QV7	2011/04/07	PT
3	vss pull low	35	Add RV106	2011/04/07	PT
4	Hdmi HPD	29	Add R636	2011/04/07	PT
5	GPU_CLKDOWN_R Pull HIGH	34	Add RV10	2011/04/07	PT
6	PEG_A_CLKREQ# CONTROL	34	Add RV264, RV265, RV266, RV267, QV9	2011/04/07	PT
7	sounds too small	31	Change RC134, RC137 from 47K to 560ohm	2010/10/15	PT
8	protect HDMI plug in noise	29	add CV101	2010/10/15	PT
9	Modify USB3.0 Solution	30		2010/10/15	PT
10	change Lan symbol	22	JLAN1	2010/10/15	PT
11	Power LED no light when S3	21	Change JBTN1 Pin1 from +5VS to +5VALW net	2010/10/15	PT
12	ESD request		Add CC70	2010/10/15	PT
13	ESD request		Add CHI01	2010/10/17	PT
14	ESD request		Add CC71-CC75	2010/10/17	PT
15	ESD request		Add CC76-CC80	2010/10/17	PT
16	ESD request		Del CF61,3,8,9,10,11,16,17	2010/10/20	PT
17	USB 3.0 Wake Issue	30	Del RI19, Add CI51	2010/10/20	PT
18	USB 3.0 Wake Issue	30	Change RI18 Pin1 to UI2 pin7	2010/10/22	PT
19	r		Change BOM UV2, CV107, CV108, RV108, RV109 to remove	2010/10/22	ST
20	LCD Timing		Change BOM C549 to SEI24474K80	2010/10/22	ST
21			Change BOM U48 to SA00003K80	2010/10/22	ST
22			Change BOM UV1 to SA00004Q40L	2010/10/22	ST
23				2010/10/24	
24				2010/10/24	PT
25				2010/10/26	PT
26				2010/12/1	ST
27				2010/12/1	ST
28				2010/12/1	ST
29				2010/12/1	ST
30				2010/12/1	ST
31				2010/12/6	ST
32				2010/12/6	ST
33				2010/12/6	ST
34				2010/12/6	ST
35				2010/12/8	ST
36				2010/12/8	ST
37				2010/12/8	ST
38				2010/12/8	ST
39				2010/12/9	ST
40					
41					
42					
43					
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D

C

B

A

Title			
<Title>			
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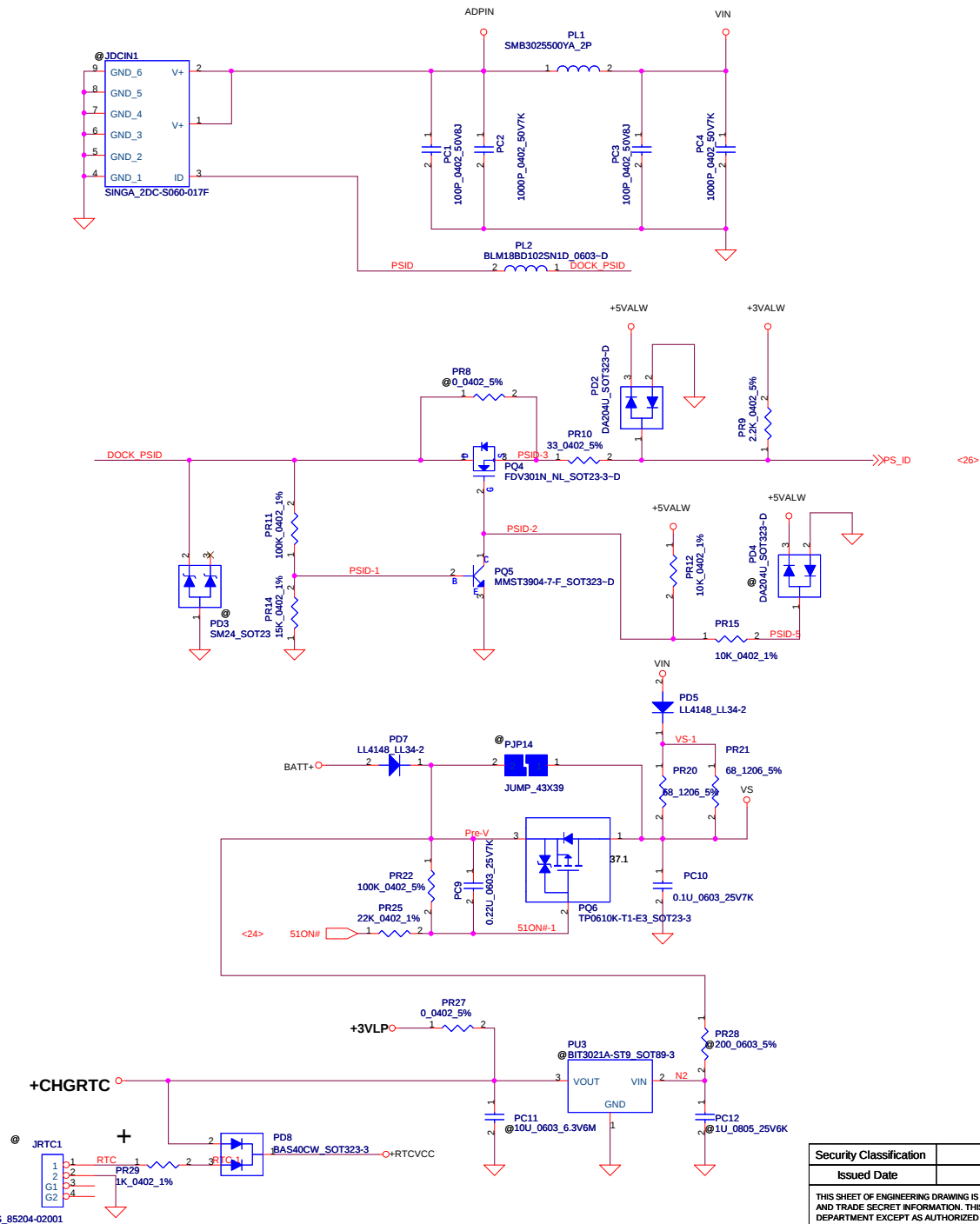
UV6
243_0402_1%-D
1 2
S@

UV5
243_0402_1%-D
1 2
S@

UV4
243_0402_1%-D
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S@

UV3
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1 2
S@

@S
1 2
D-%1_0402_K3:47
RV59

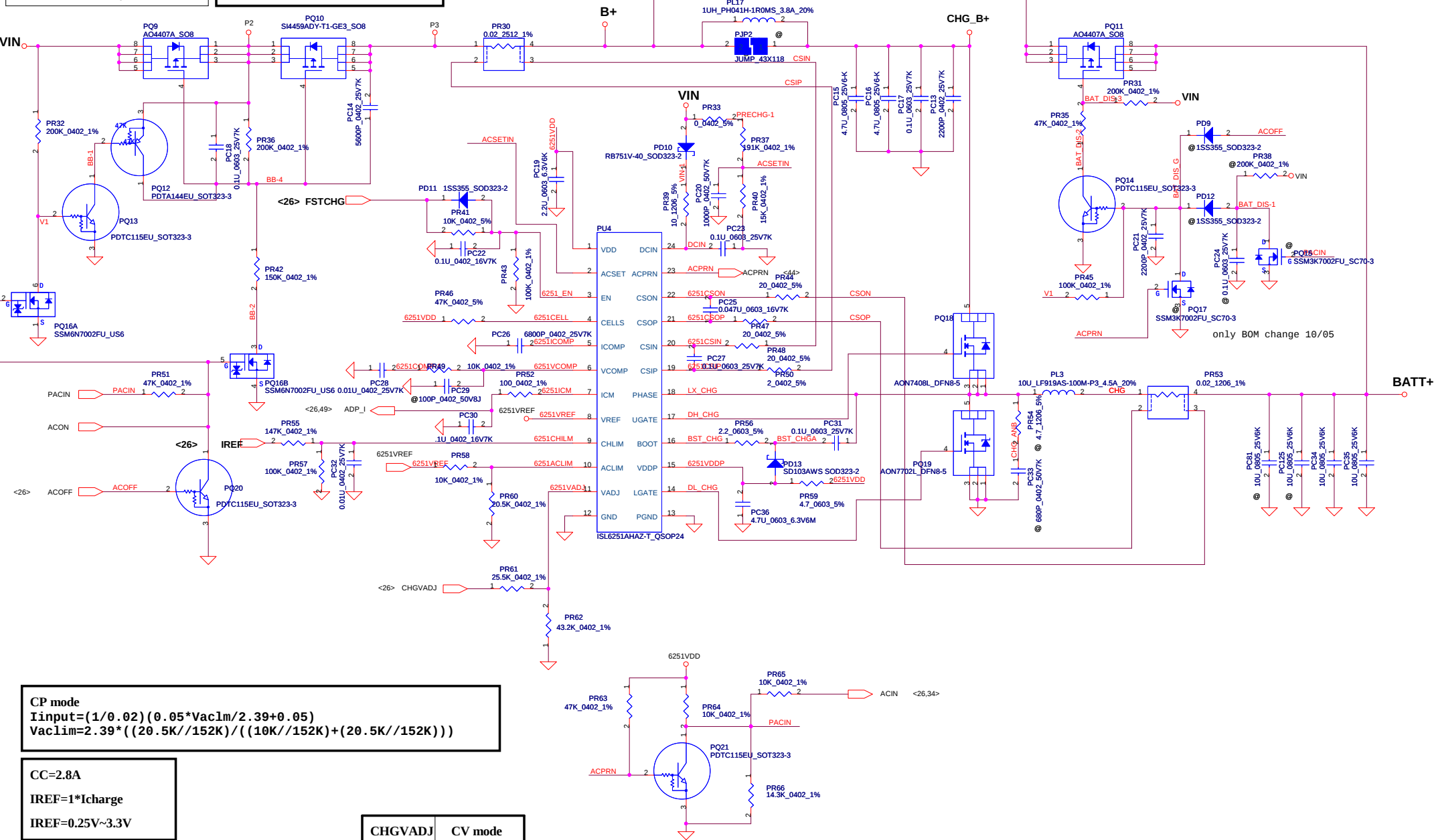


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Issued Date	2010/12/24	Deciphered Date	2011/12/24	Title	PWR-DCIN / Vin Detector	
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$I_{ada} = 0 \sim 4.615A (90W / 19.5V = 4.615A)$

$ADP_I = 19.9 * I_{adapter} * R_{sense}$

$CP = 90\% * I_{ada} ; CP = 4.15A$



CP mode
 $I_{input} = (1/0.02) (0.05 * V_{acim} / 2.39 + 0.05)$
 $V_{acim} = 2.39 * ((20.5K / 152K) / ((10K / 152K) + (20.5K / 152K)))$

CC=2.8A
 $I_{REF} = 1 * I_{charge}$
 $I_{REF} = 0.25V \sim 3.3V$

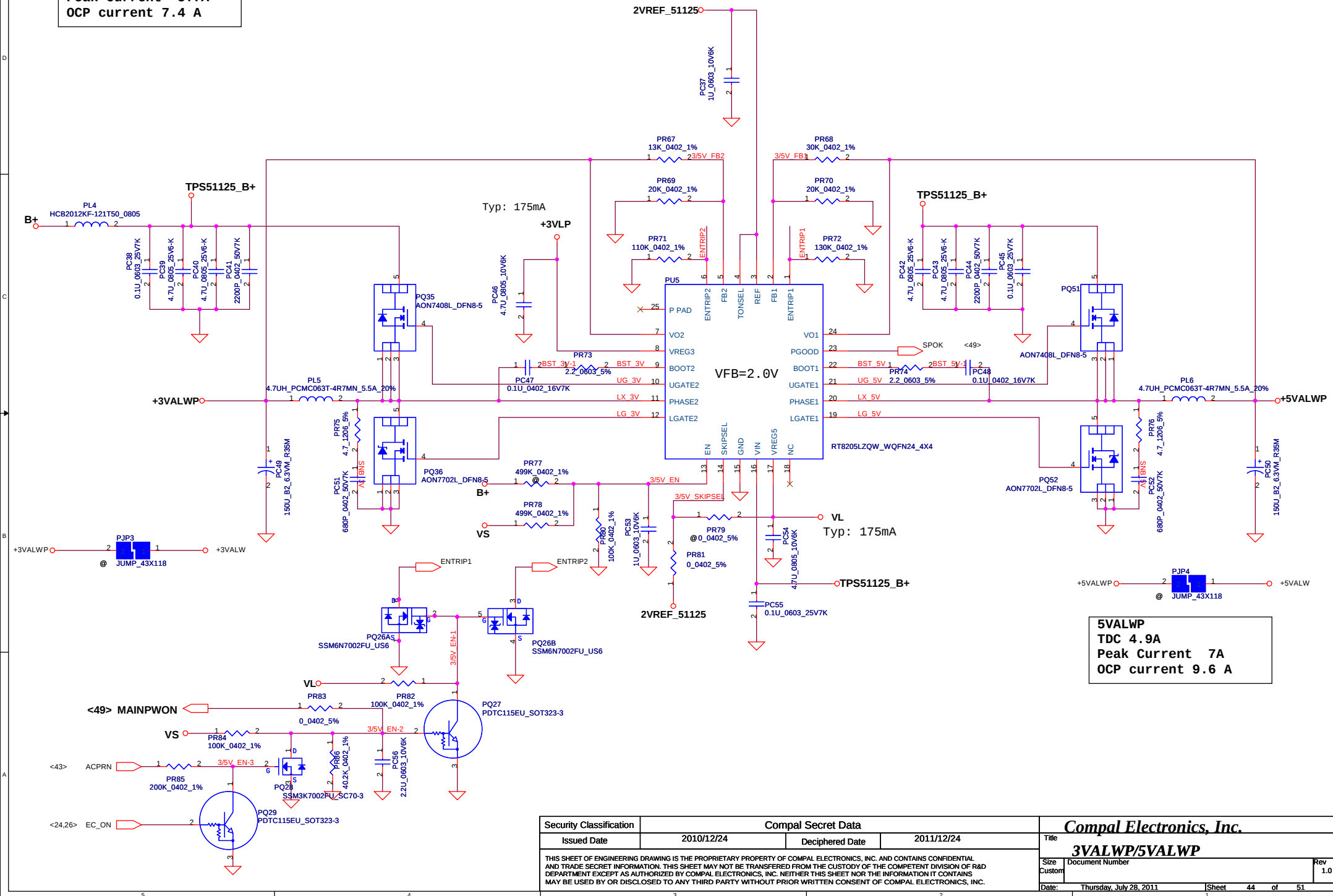
BATT Type	Charging Voltage (0x15)	CV mode
Normal 4S LI-ON Cells	14800mV	14.80V

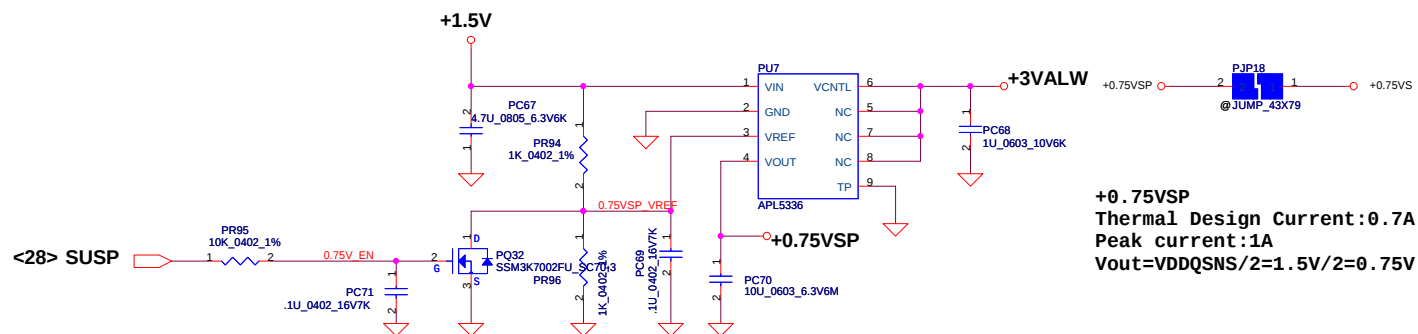
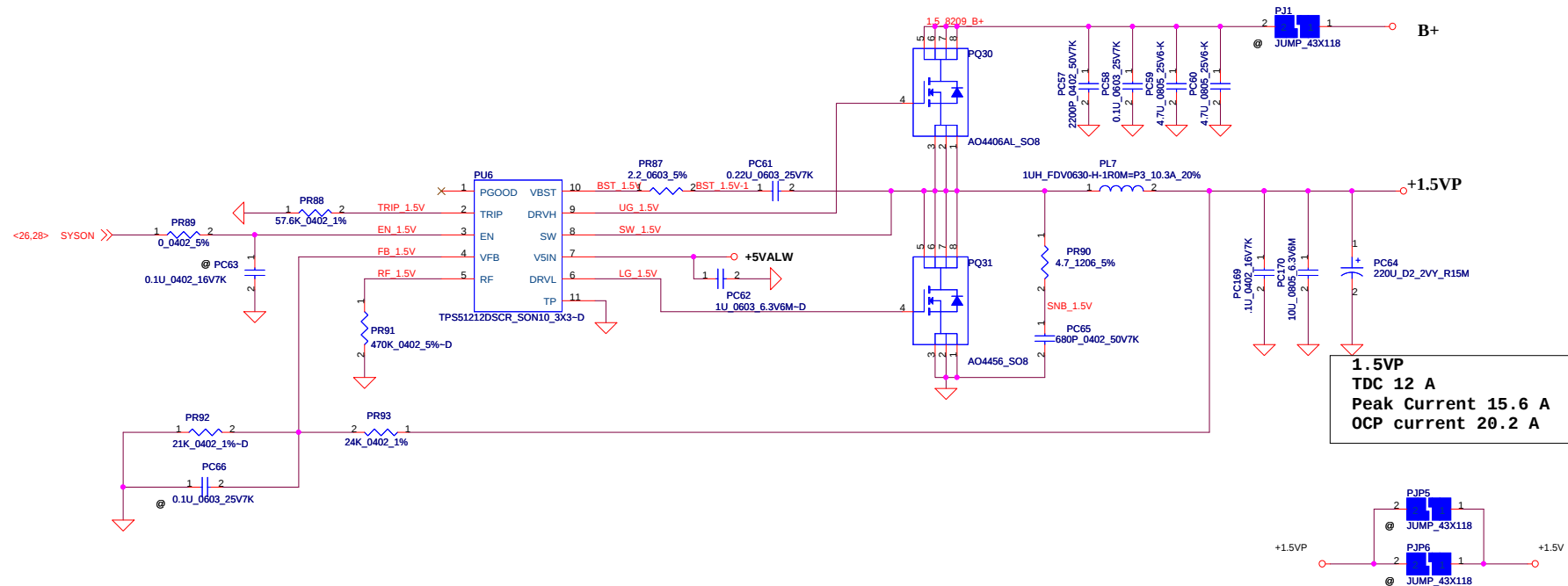
CHGVADJ	CV mode
0V	3.99V per cell
1.93V	4.2V per cell
3.3V	4.35V per cell

3.3VALWP
TDC 4.02 A
Peak Current 5.7A
OCP current 7.4 A

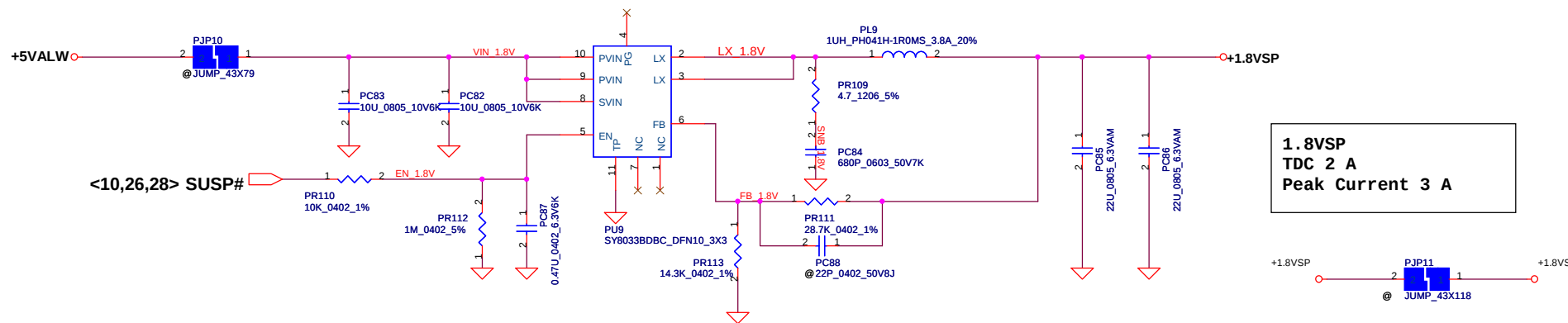
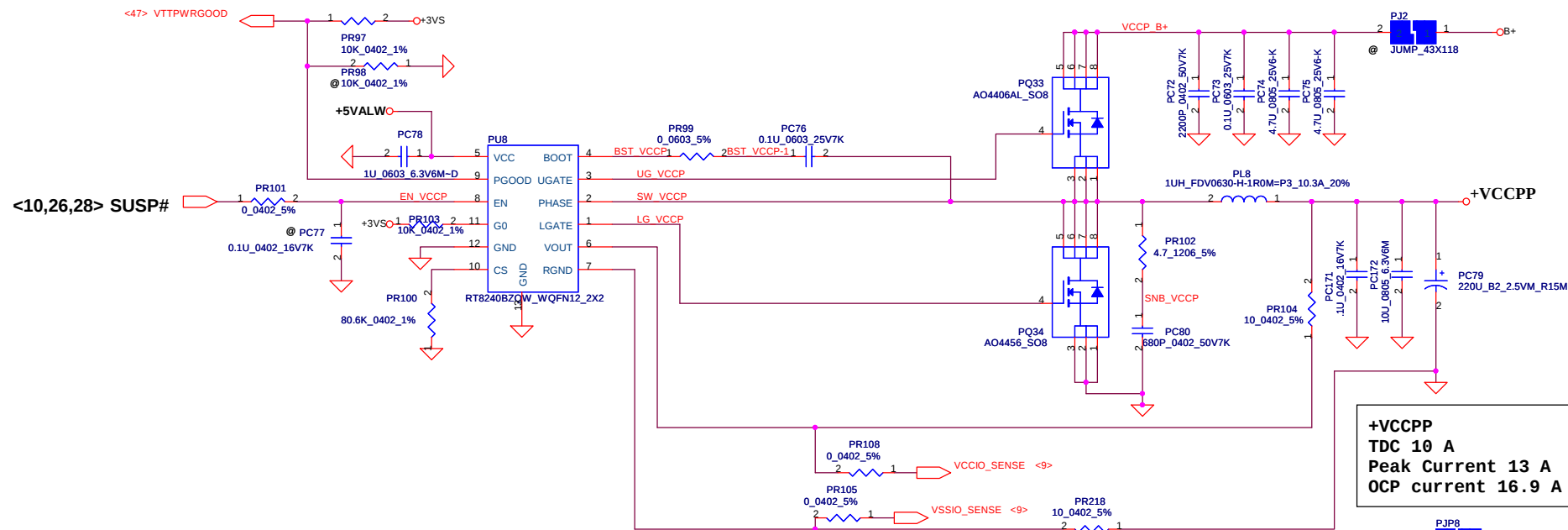
5VALWP
TDC 4.9A
Peak Current 7A
OCP current 9.6 A

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<10> VCCSA_SEL

<46> VTTTPWRGOOD

<26> SA_PGOOD

VCCSA_SEL
0
1

VCCSA Vout
0.9V
0.8V

Required on 2011 / 2012
Yes / Yes
Yes / Yes

+VCCSAP
TDC 6A
Peak Current 7.2 A
OCP current 9.36 A

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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Title			
CPU_CORE/GFX			
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Version change list (P.I.R. List)

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Item	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	modify Vcore and GFX boost resistance		P48	change PR136,PR163,PR179 to 2.2 +-5% 0603.	2011.2.10	before SSI
2	modify VGA FB resistance		P50	change PR211 to 243K +-1% 0402. PR221 to 37.4K +-1% 0402.	2011.3.24	SSI
3	modify 1.5V Enable signal		P45	change PR81 connect to SYSON.	2011.3.24	SSI
4	modify ADP_I protection		P49	change PR189 to 12.1k +-5% 0402.	2011.3.24	SSI
5	integrate mosfet		P45	change PQ53 PQ54 to AON7408L		
6	modify Vcore and GFX's loadline and OCP		P48	change PR171 to 1.62K +-1% 0402 change PR170 to 3.48K +-1% 0402 change PR149 to 1.18K +-1% 0402 change PR131 to 2.7K +-1% 0402 change PC115 to .033U 16V K X7R 0402		
7	modify VGA for HW team suggest item		P50	add PR219 100K +-5% 0402 remove PR223 10K +-5% 0402 change PR205 to 22.1K +-1% 0402		
8	integrate mosfet		P45 P47	change PQ32 to SSM3K7002FU 1N SC70-3 change PQ37 to SSM3K7002FU 1N SC70-3		
9	add capacitance for RF team suggest item		P43 P45 P46 P50	change PC81 PC125 to 10U 25V K X5R 0805 H1.25 change PC169 to .1U 16V K X7R 0402 change PC170 to 10U 6.3V M X5R 0805 H1.25 change PC171 to .1U 16V K X7R 0402 change PC172 to 10U 6.3V M X5R 0805 H1.25 change PC173 to 10U 6.3V M X5R 0805 H1.25		
10	modify 1.5V OCP resistance		P45	change PR88 to 57.6K +-1% 0402		
11	modify VCCP OCP resistance		P46	change PR100 to 80.6K +-1% 0402		
12	modify choke footprint for DFX requirement			change PL5,PL6,PL7,PL8,PL10 to TAI-T_VMPI0703AR-100M-Z01_2P		
13	modify PQ11 Vgs resistance		P43	change PR31 to 200K +-1% 0402 change PR35 to 47K +-1% 0402		
14	modify the net name of SPOK-'		P49	change the net name of PQ47 pin2 to SPOK1 change the net name of PQ47 pin1 to SPOK2 change the net name of PQ46 pin2 to SPOK3		
15	modify PU12 vcc power from +3VALW to +3VLP		P49	change PR190.1 to +3VLP change PR149.1 to +3VLP change PU12.1 to +3VLP		
16	modify OTP resistance		P49	change PR190 to 23.2K +-1% 0402 change PR194 to 10K +-1% 0402		
17	modify VCORE VCCP resistance		P48	change PR145 to 1 +-5% 0603		

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				Date: Thursday, July 28, 2011		Sheet 51 of 51