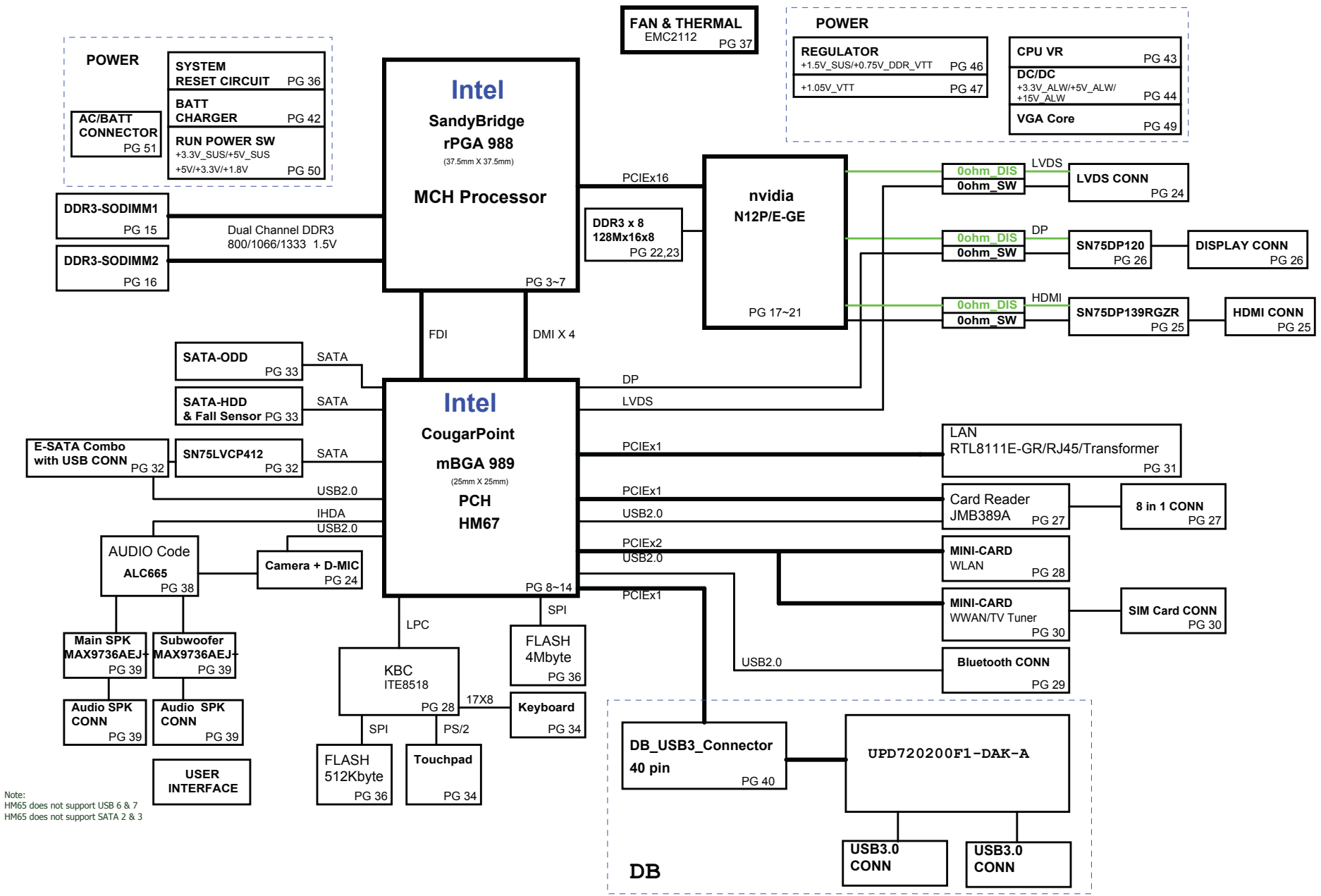
_DIS ==> Discrete Only
_SW ==> Optimus Only
_UMA ==> UMA Only

GM6C MLK Optimus, Discrete & UMA

VER : 1A
PWA:
PWB:



Note:
HM65 does not support USB 6 & 7
HM65 does not support SATA 2 & 3

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Block Diagram	1A

Date: Friday, January 07, 2011 Sheet 1 of 59

Table of Contents

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44 ,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30 ,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_ON	

GND PLANE	PAGE	DESCRIPTION
⏚ GND	ALL	

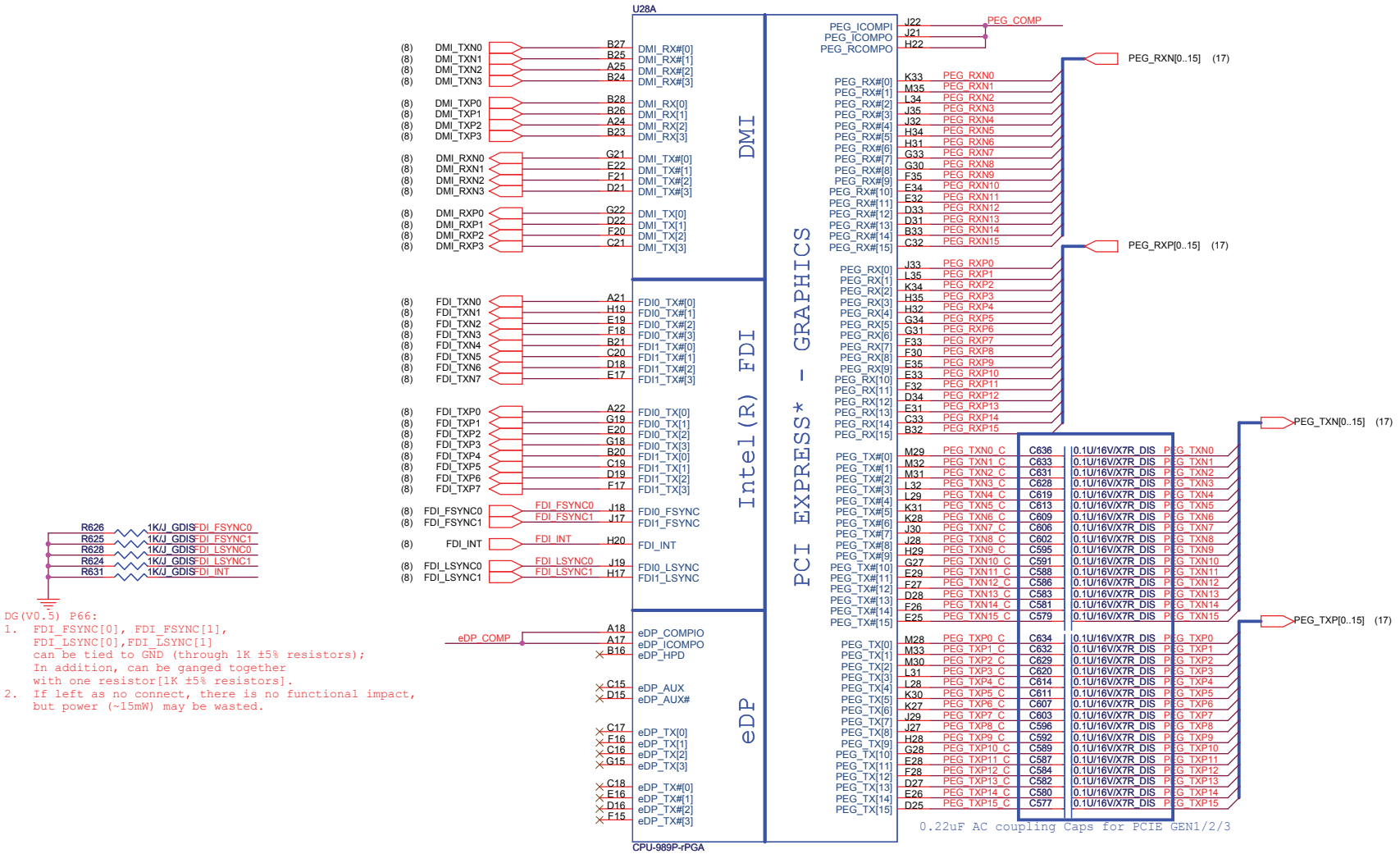
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Frontage	1A

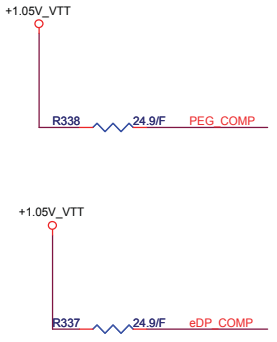
Date: Friday, January 07, 2011 Sheet 2 of 59

Sandy Bridge Processor (DMI,PEG,FDI)



DG(V0.5) P66:
1. FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0],FDI_LSYNC[1] can be tied to GND (through 1K ±5% resistors); In addition, can be ganged together with one resistor[1K ±5% resistors].
2. If left as no connect, there is no functional impact, but power (~15mW) may be wasted.

DP & PEG Compensation



Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: Sandy Bridge 1/5	Rev: 1A
Date: Friday, January 07, 2011	Sheet 3 of 59	

Sandy Bridge Processor (CLK,MISC,JTAG)

WW31.MOW Page 5 (SNB_IVB# N.A at SNB EDS #27637 0.7v1)

U28B

MISC: TP19 H_SNB_IVB# C26 PROC_SELECT#; (28) H_CPUDET# AN34 SKTOCC#

THERMAL: TP21 TP_CATERR# AL33 CATERR#; (28) EC_PECI R352 43/J H_PECI AN33 PECI; (28,42,43) VR_HOT# R358 56/J H_PROCHOT# AL32 PROCHOT#; (12) H_THERM# AN32 THERMTRIP#

shut down when asserted

Over 130 degree C will drive low

PWR MANAGEMENT: provide power management status (form PCH to CPU)

(8) PM_SYNC R372 *0/J_short_NC PM_SYNC_R AM34 PM_SYNC

(12) H_PWRGOOD R373 *0/J_short_NC PWRGOOD_R AP33 UNCOREPWRGOOD; R374 10K/J

PM_DRAM_PWRGD_R V8 SM_DRAMPWROK

+1.05V_VTT R368 *75/J_NC; CPU_PLTRST# R359 *43/J_NC CPU_PLTRST#_R AR33 RESET#

CPU-989P-rPGA

CLOCKS: BCLK A28, BCLK# A27 → CLK_CPU_BCLKP (10), CLK_CPU_BCLKN (10) DMI clock

DPLL_REF_CLK A16, DPLL_REF_CLK# A15 → CLK_DPLL_SSCLKP_R, CLK_DPLL_SSCLKN_R; R629 *0_NC; Ra; CLK_DPLL_SSCLKP (10), CLK_DPLL_SSCLKN (10) eDP clock

R627 1K/J, R630 1K/J; Rb; Rc; +1.05V_VTT

	DIS	SW
Ra	NA	0 ohm
Rb	1K ohm	NA
Rc	1K ohm	NA

DDR3 MISC: SM_DRAMRST# R8 CPU_DRAMRST# — S3 Power reduce

SM_RCOMP[0] AK1, SM_RCOMP[1] A5, SM_RCOMP[2] A4 → SM_RCOMP_0 R322 140/F, SM_RCOMP_1 R312 25.5/F, SM_RCOMP_2 R313 200/F — 26.1 change to 25 ohm

JTAG & BPM: PRDY# AP29, PREQ# AP27 XDP_PREQ# → T5

TCK AR26 XDP_TCLK, TMS AR27 XDP_TMS, TRST# AP30 XDP_TRST#

TDI AR28 XDP_TDI, TDO AP26 → T2

DBR# AL35 → T11

BPM#[0] AT28 → T3; BPM#[1] AR29 → T6; BPM#[2] AR30 → T7; BPM#[3] AT30 → T10; BPM#[4] AP32 → T9; BPM#[5] AR31 → T4; BPM#[6] AT31 → T12; BPM#[7] AR32 → T8

+1.05V_VTT

XDP_TMS R364 51/J; XDP_TDI R363 51/J; XDP_PREQ# R365 *51/J_NC; XDP_TCLK R341 51/J; XDP_TRST# R375 51/J

Option for Prochot# function
68 ohm for unused, 62 ohm for used

+1.05V_VTT

H_PROCHOT# R367 *68/J_NC; VR_HOT# R366 62/J

IN	OUT
L	L
H	High-Z

+3.3V_SUS; C414 *0.1U/16V/X7R_NC

U19 *74LVC1G07GW_NC (NC, VCC, IN, GND, OUT)

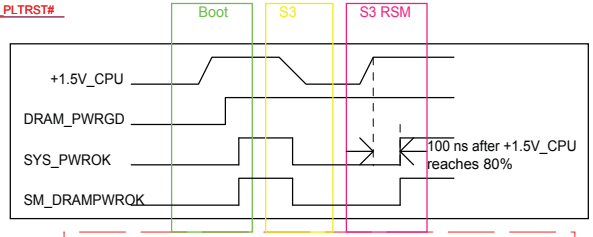
(11,17,27,28,29,30,31,40) PLTRST#

CPU_PLTRST#

level shift for reset pin(07/12)

R714 1.5K/F; CPU_PLTRST#_R; R723 750/F

Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	High-Z



+1.5V_SUS keep DDR3_DRAMRST# high to avoid CPU_DRAMRST# low when into S3 (Because can't reset DRAM when into S3)

3/16 Change topology;
Add AND gate based on DG rev0.9

+3.3V_SUS; C574 0.1U/16V/X7R; R489 200/J

(8) PM_DRAM_PWRGD, (8) SYS_PWROK → U27 74AHC1G09GW → PM_DRAM_PWRGD_Q

+1.5V_SUS_CPU

02/25 Update R8232, R8233 value and routing, Add R8583 follow PDG 0.71 #440484

R613 200/F; R615 130/F PM_DRAM_PWRGD_R

R616 *39/J_NC; Q68 *2N7002K_NC; PS_S3CNTRL (6,8,15)

S3 Power reduce

+1.5V_SUS; R293 1K/J

Q33 BSS138-7-F

CPU_DRAMRST# → DDR3_DRAMRST#_R R289 1K/J → DDR3_DRAMRST# (15,16)

R701 1K/J +3.3V_SUS; DDR_HVREF_RST_PCH (10)

R299 4.99K/F; C237 0.047U/10V/X7R 10

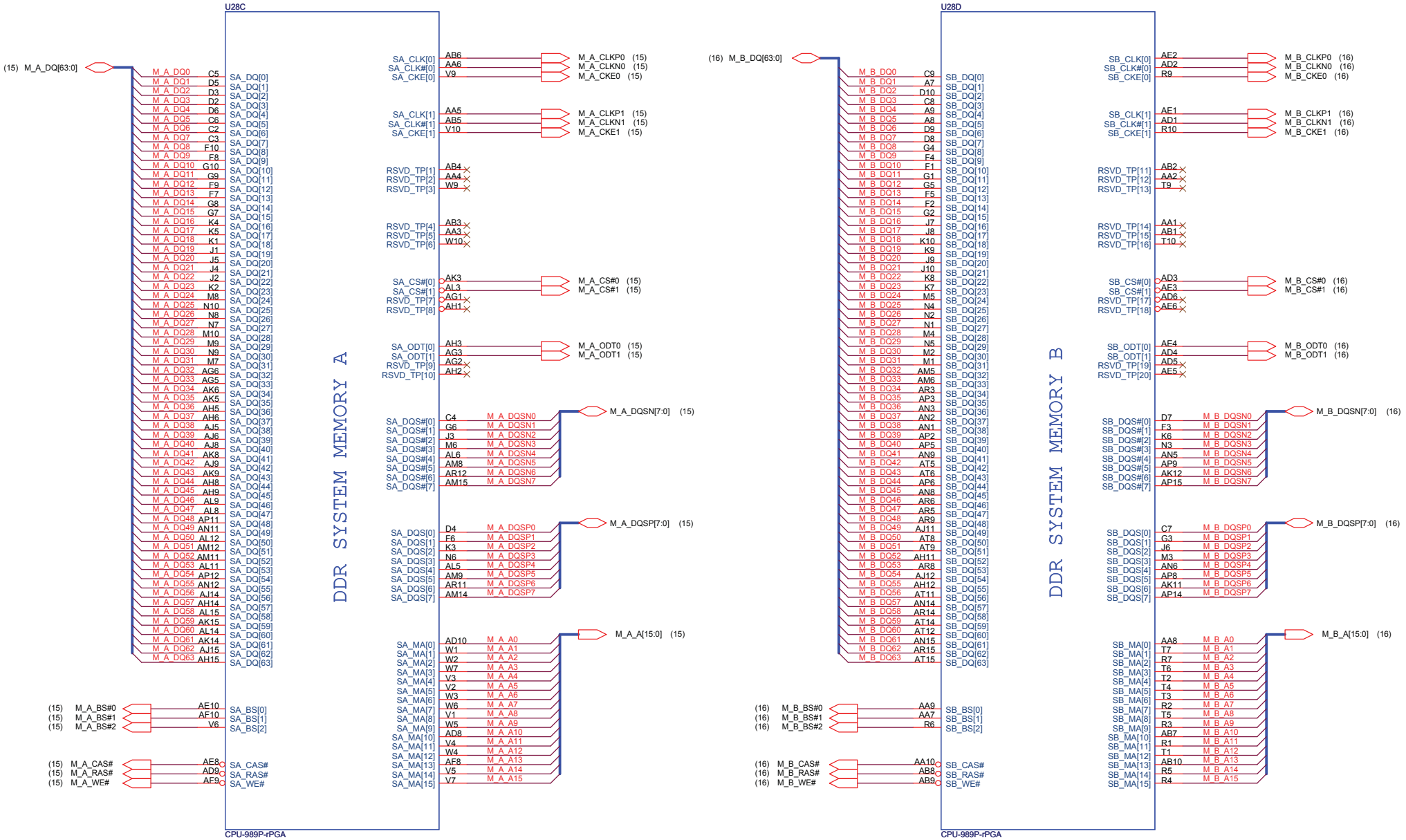
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Sandy Bridge 2/5	1A

Date: Friday, January 07, 2011 Sheet 4 of 57

Sandy Bridge Processor (DDR3)

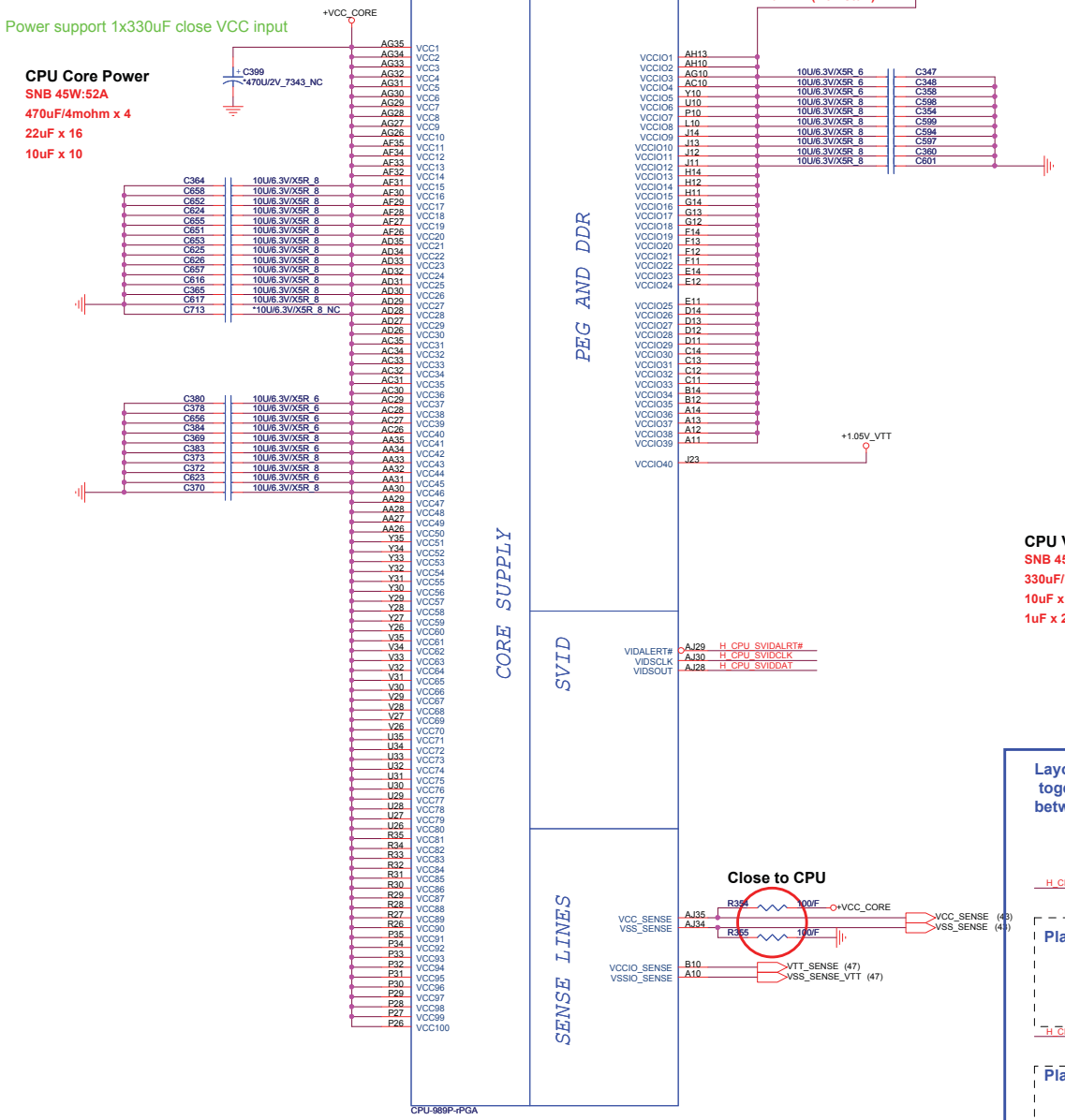


Quanta Computer Inc.

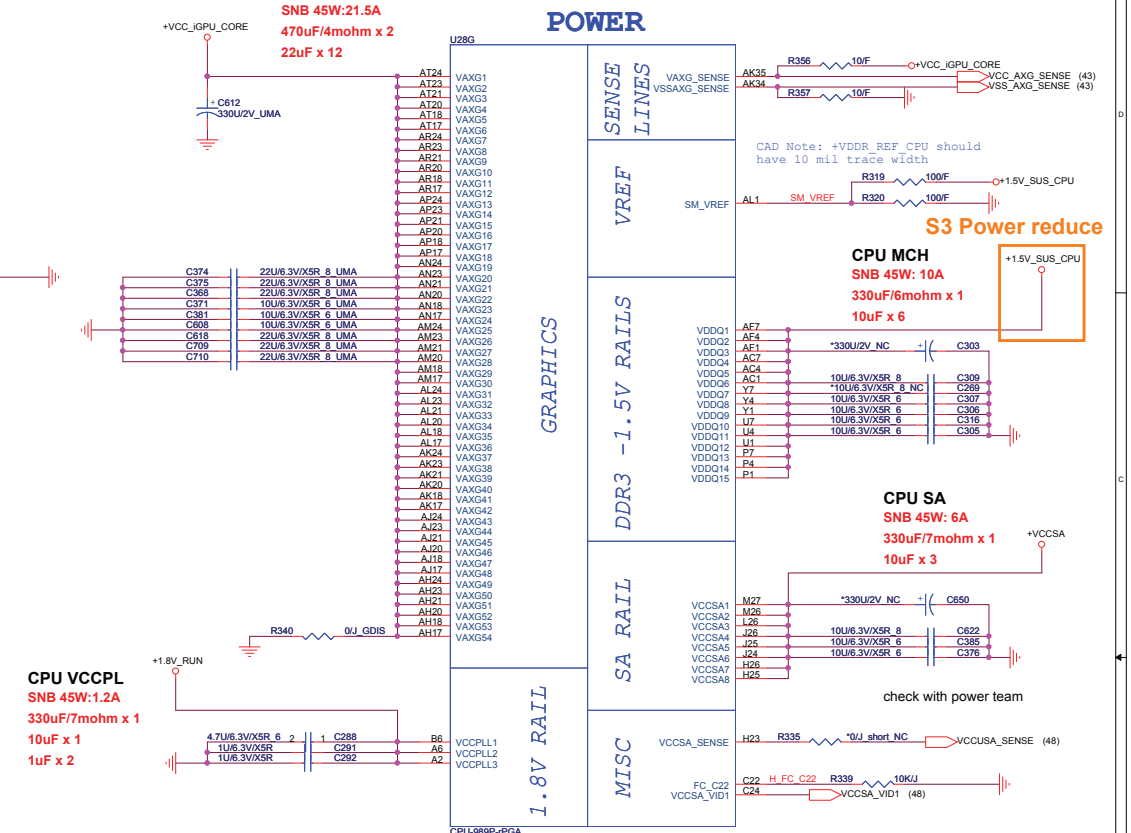
PROJECT : GM6C MLK DIS

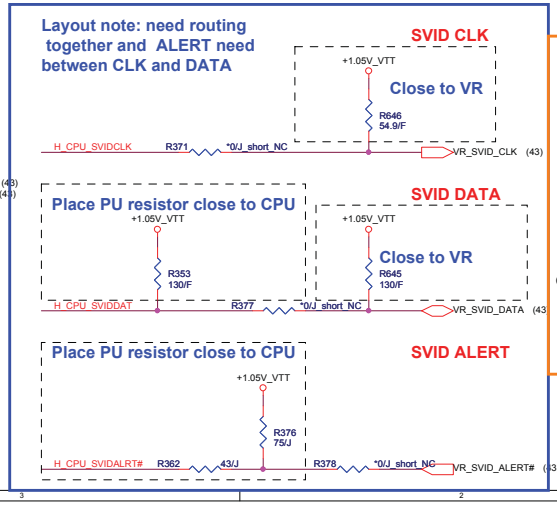
Size	Document Number	Rev
	Sandy Bridge 3/5	1A
Date: Friday, January 07, 2011	Sheet 5 of 59	

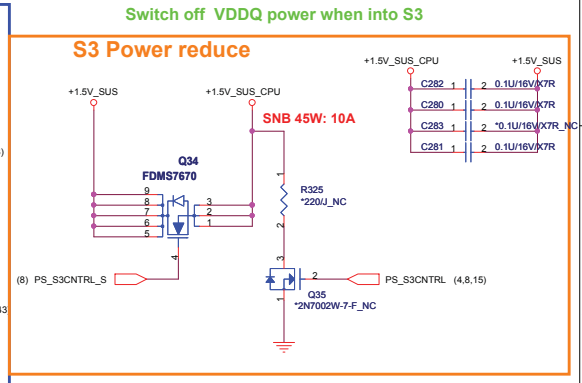
Sandy Bridge Processor (POWER)



Sandy Bridge Processor (GRAPHIC POWER)





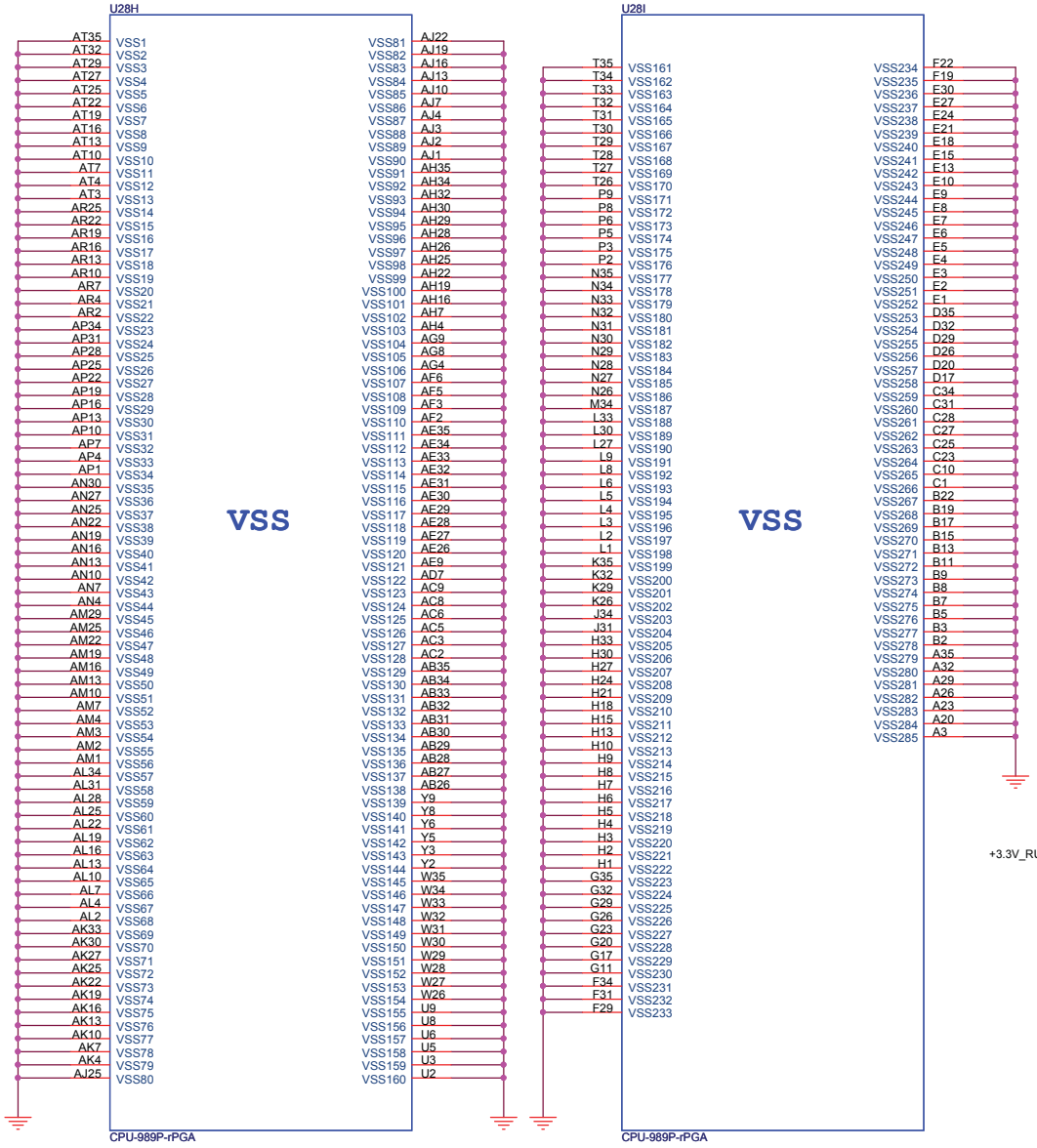


Quanta Computer Inc.

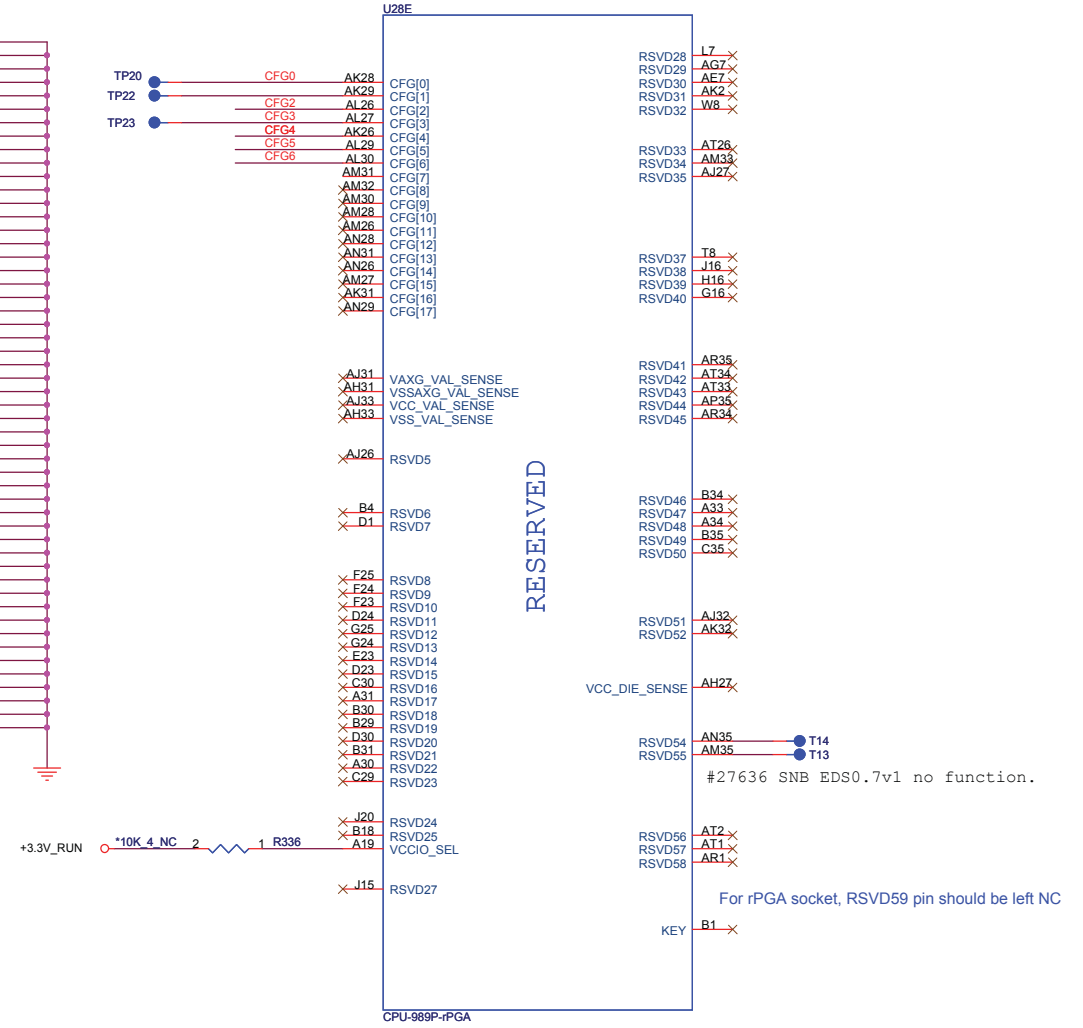
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Sandy Bridge 4/5	1A
Date: Friday, January 07, 2011	Sheet 6 of 59	

Sandy Bridge Processor (GND)



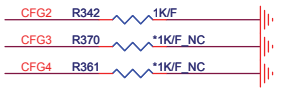
Sandy Bridge Processor (RESERVED, CFG)

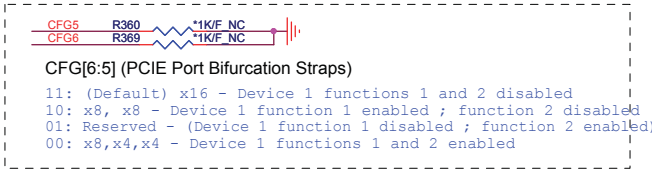


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Number Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	PCI-E Static x4 Lane Reversal	PEG wait for BIOS training
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP



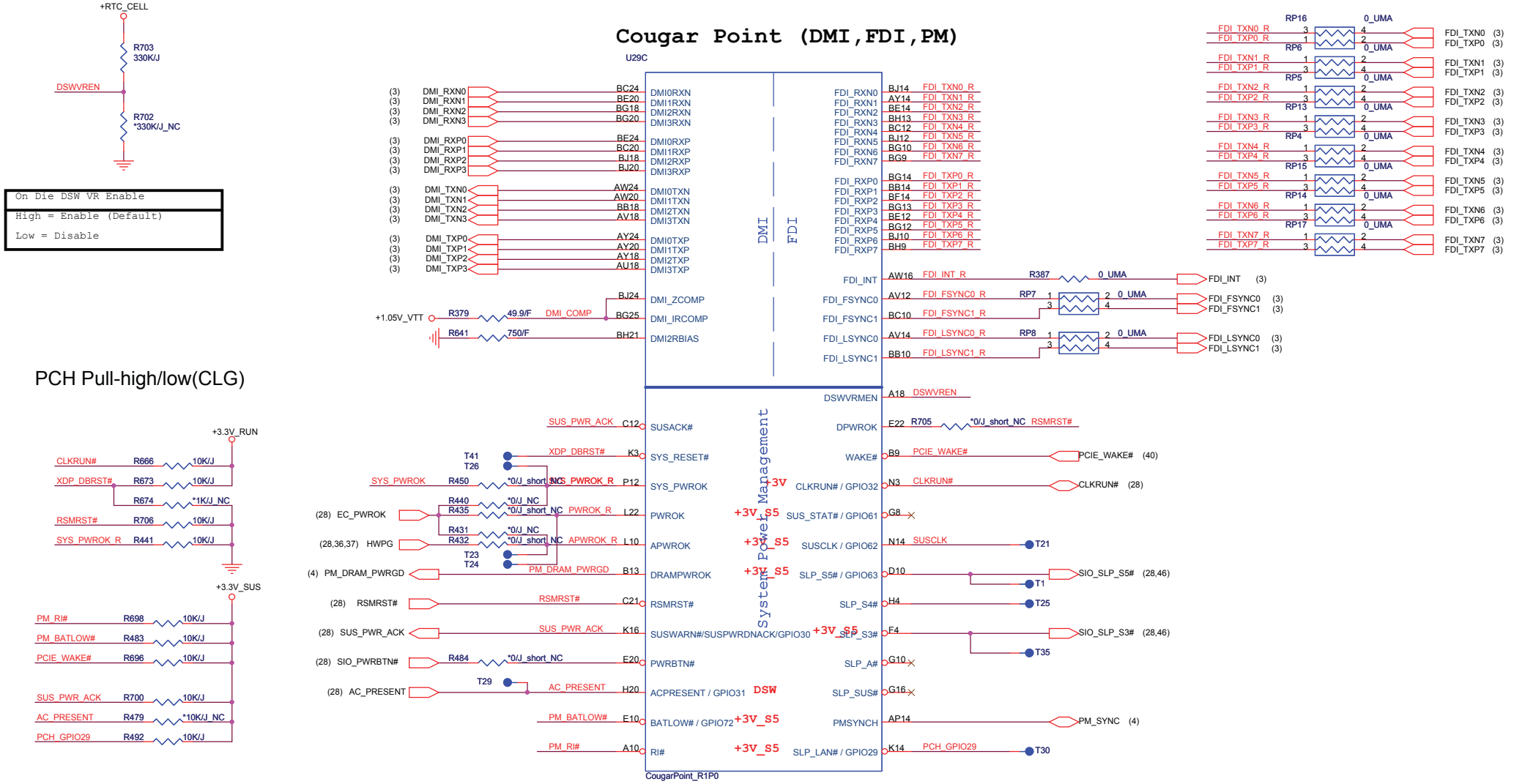


Quanta Computer Inc.

PROJECT : GM6C MLK DIS

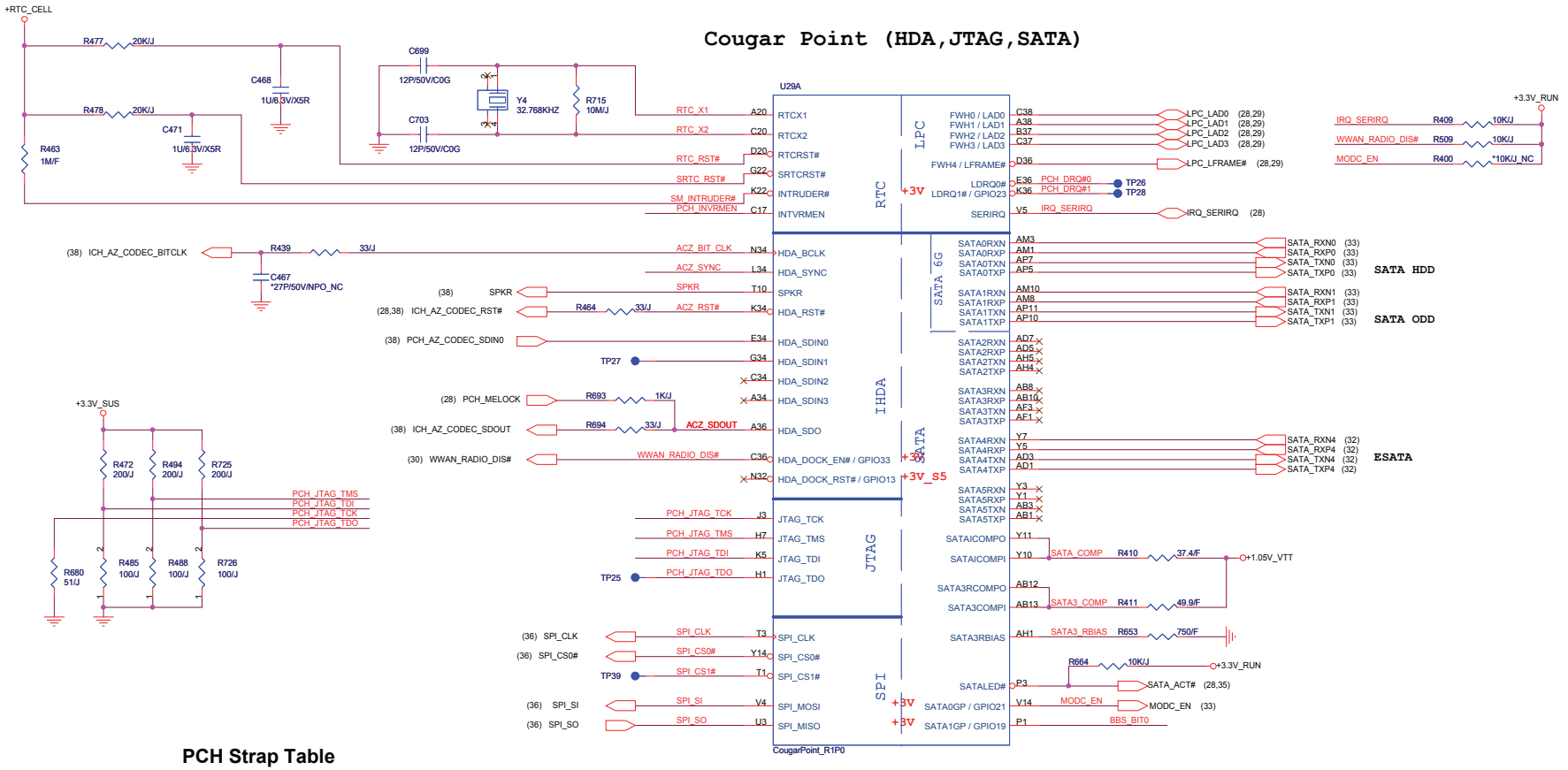
Size	Document Number	Rev
	Sandy Bridge 5/5	1A
Date: Friday, January 07, 2011	Sheet 7 of 59	

Cougar Point (DMI,FDI,PM)



Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: Cougar Point 1/7	Rev: 1A
Date: Friday, January 07, 2011	Sheet 8 of 59	

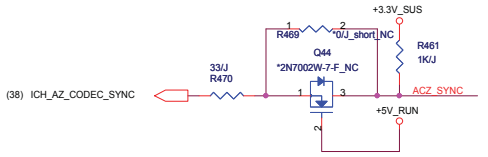
Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	**Default weak pull-up on GNT0/1#** **[Need external pull-down for LPC BIOS]**
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm **0 = Set to Vss** **1 = Set to Vcc (weak pull-down 20K)**

GNT1#	GNT0#	Boot Location
1	1	SPI *
0	0	LPC



Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Cougar Point-M (PCI-E,SMBUS,CLK)

Note:Place TX DC blocking caps close to PCH.

U29B

Mini WWAN
(30) PCIE_RXN1 — BG34 PERN1
(30) PCIE_RXP1 — BJ34 PERP1
(30) PCIE_TXN1 — C402 0.1U/16V/X7R PCIE_TXN1_C — AV32 PETN1
(30) PCIE_TXP1 — C403 0.1U/16V/X7R PCIE_TXP1_C — AU32 PETP1

Mini WLAN
(29) PCIE_RXN2 — BE34 PERN2
(29) PCIE_RXP2 — BF34 PERP2
(29) PCIE_TXN2 — C400 0.1U/16V/X7R PCIE_TXN2_C — BB32 PETN2
(29) PCIE_TXP2 — C401 0.1U/16V/X7R PCIE_TXP2_C — AY32 PETP2

BG36 PERN3
BJ36 PERP3
AV34 PETN3
AU34 PETP3

USB 3.0
(40) PCIE_RXN4 — BF36 PERN4
(40) PCIE_RXP4 — BE36 PERP4
(40) PCIE_TXN4 — C405 0.1U/16V/X7R PCIE_TXN4_C — AY34 PETN4
(40) PCIE_TXP4 — C404 0.1U/16V/X7R PCIE_TXP4_C — BB34 PETP4

Card Reader
(27) PCIE_RXN5 — BG37 PERN5
(27) PCIE_RXP5 — BH37 PERP5
(27) PCIE_TXN5 — C407 0.1U/16V/X7R PCIE_TXN5_C — AY36 PETN5
(27) PCIE_TXP5 — C406 0.1U/16V/X7R PCIE_TXP5_C — BB36 PETP5

Giga Bit LOM
(31) PCIE_RXN6 — BJ38 PERN6
(31) PCIE_RXP6 — BG38 PERP6
(31) PCIE_TXN6 — C408 0.1U/16V/X7R PCIE_TXN6_C — AU36 PETN6
(31) PCIE_TXP6 — C409 0.1U/16V/X7R PCIE_TXP6_C — AV36 PETP6

BG40 PERN7
BJ40 PERP7
AY40 PETN7
BB40 PETP7

BE38 PERN8
BC38 PERP8
AW38 PETN8
AY38 PETP8

PCI-E*

+3V_S5

SMBUS
+3V_S5 SMBALERT# / GPIO11 — E12 RSV_SMBALERT#
SMBCLK — H14 PCH_SMBCLK — PCH_SMBCLK (29)
SMBDATA — C9 PCH_SMBDATA — PCH_SMBDATA (29)
+3V_S5 SML0ALERT# / GPIO60 — A12 — DDR_HVREF_RST_PCH (4)
SML0CLK — C8 SMB_CLK_ME0
SML0DATA — G12 SMB_DATA_ME0
SML1ALERT# / PCHHOT# / GPIO74 — C13 PCH_GPIO74
+3V_S5 SML1CLK / GPIO58 — E14 SMB_CLK_ME1
+3V_S5 SML1DATA / GPIO75 — M16 SMB_DATA_ME1

Controller Link
CL_CLK1 — M7
CL_DATA1 — T11
CL_RST1# — P10

CLOCKS
+3V_S5 PEG_A_CLKRQ# / GPIO47 — M10 PEG_CLKREQ# — PEG_CLKREQ# (17)
CLKOUT_PEG_A_N — AB37 — CLK_PCIE_VGAN (17)
CLKOUT_PEG_A_P — AB38 — CLK_PCIE_VGAP (17)
CLKOUT_DMI_N — AV22 — CLK_CPU_BCLKN (4)
CLKOUT_DMI_P — AU22 — CLK_CPU_BCLKP (4)
CLKOUT_DP_N — AM12 — CLK_DPLL_SSCLKN (4)
CLKOUT_DP_P — AM13 — CLK_DPLL_SSCLKP (4)
CLKIN_DMI_N — BF18 CLK_BUF_PCIE_3GPLLN R381 10K/J
CLKIN_DMI_P — BE18 CLK_BUF_PCIE_3GPLLP R383 10K/J
CLKIN_GND1_N — BJ30 CLK_BUF_BCLKN R642 10K/J
CLKIN_GND1_P — BG30 CLK_BUF_BCLKP R643 10K/J
CLKIN_DOT_96N — G24 CLK_BUF_DREFCLKN R453 10K/J
CLKIN_DOT_96P — E24 CLK_BUF_DREFCLKP R452 10K/J
CLKIN_SATA_N — AK7 CLK_BUF_DREFSSCLKN R403 10K/J
CLKIN_SATA_P — AK5 CLK_BUF_DREFSSCLKP R402 10K/J
REFCLK14IN — K45 CLK_PCH_14M R434 10K/J
CLKIN_PCILOOPBACK — H45 CLK_PCI_FB — CLK_PCI_FB (11)
XTAL25_IN — V47 XTAL25_IN
XTAL25_OUT — V49 XTAL25_OUT
XCLK_RCOMP — Y47 XCLK_RCOMP R661 90.9/F — +1.05V_VTT

Y40 CLKOUT_PCIE0N
Y39 CLKOUT_PCIE0P
CLK_PEG0_REQ# — J2 — PCIECLKRQ0# / GPIO73 — +3V_S5

Mini WLAN
(29) CLK_PCIE_MINI1N — AB49 CLKOUT_PCIE1N
(29) CLK_PCIE_MINI1P — AB47 CLKOUT_PCIE1P
(29) MINI1CLK_REQ# — MINI1CLK_REQ# — M1 — PCIECLKRQ1# / GPIO18 — +3V

Card Reader
(27) CLK_PCIE_CRN — AA48 CLKOUT_PCIE2N
(27) CLK_PCIE_CRP — AA47 CLKOUT_PCIE2P
Enable Free-Running (confirm with BIOS) 0628
CLK_PCIE_REQ2# — V10 — PCIECLKRQ2# / GPIO20 — +3V

Mini WWAN
(30) CLK_PCIE_MINI3N — Y37 CLKOUT_PCIE3N
(30) CLK_PCIE_MINI3P — Y36 CLKOUT_PCIE3P
(30) MINI2CLK_REQ# — MINI2CLK_REQ# — A8 — PCIECLKRQ3# / GPIO25 — +3V_S5

USB3.0
(40) CLK_PCIE_USB30N — Y43 CLKOUT_PCIE4N
(40) CLK_PCIE_USB30P — Y45 CLKOUT_PCIE4P
(40) CLK_PCIE_USB30_REQ# — CLK_PCIE_USB30_REQ# — L12 — PCIECLKRQ4# / GPIO26 — +3V_S5

Giga Bit LOM
(31) CLK_PCIE_LOMN — V45 CLKOUT_PCIE5N
(31) CLK_PCIE_LOMP — V46 CLKOUT_PCIE5P
(31) LOM_CLK_REQ# — LOM_CLK_REQ# — L14 — PCIECLKRQ5# / GPIO44 — +3V_S5

AB42 CLKOUT_PEG_B_N
AB40 CLKOUT_PEG_B_P
PEG_B_CLKRQ# — E6 — PEG_B_CLKRQ# / GPIO56 — +3V_S5

T18 CLK_PCH_SRC6N — V40 CLKOUT_PCIE6N
T19 CLK_PCH_SRC6P — V42 CLKOUT_PCIE6P
CLK_PCIE_REQ6# — T13 — PCIECLKRQ6# / GPIO45 — +3V_S5

V38 CLKOUT_PCIE7N
V37 CLKOUT_PCIE7P
CLK_PCIE_REQ7# — K12 — PCIECLKRQ7# / GPIO46 — +3V_S5

T16 CLK_PCIE_XDPN — AK14 CLKOUT_ITPXDP_N
T15 CLK_PCIE_XDPP — AK13 CLKOUT_ITPXDP_P

FLEX CLOCKS
+3V CLKOUTFLEX0 / GPIO64 — K43 HDMI_PWR_CTRL — HDMI_PWR_CTRL (25)
+3V CLKOUTFLEX1 / GPIO65 — F47 CLK_VGA_27M_R R684 22/J_GDIS — CLK_VGA_27M (19)
+3V CLKOUTFLEX2 / GPIO66 — H47 TEST_WOOFER_EN — TEST_WOOFER_EN (39)
+3V CLKOUTFLEX3 / GPIO67 — K49 CLK_VGA_27M_SS_R R442 *22/J_NC — CLK_VGA_27M_SS (19)

CougarPoint_R1P0

+3V_SUS
PCH_SMBCLK 2.2K/F R482
PCH_SMBDATA 2.2K/F R697
SMB_CLK_ME0 2.2K/F R713
SMB_DATA_ME0 2.2K/F R476
SMB_CLK_ME1 2.2K/F R462
SMB_DATA_ME1 2.2K/F R457
RSV_SMBALERT# 10K/F R471
PCH_GPIO74 10K/F R712

WLAN, WWAN, DIMM0, DIMM1, 3-axis fall sensor

+3.3V_SUS
Q43 2N7002W-7-F
SMB_CLK_ME1 — SMBCLK1 (28)
+3.3V_SUS
Q42 2N7002W-7-F
SMB_DATA_ME1 — SMBDAT1 (28)

EC

PCIE Clock Request

+3.3V_SUS
R695 10K/J MINI2CLK_REQ#
R685 10K/J CLK_PEG0_REQ#
R481 10K/J LOM_CLK_REQ#
R475 10K/J PEG_B_CLKRQ#
R473 10K/J PEG_CLKREQ#
R451 10K/J CLK_PCIE_REQ6#
R467 10K/J CLK_PCIE_USB30_REQ#
R480 10K/J CLK_PCIE_REQ7#

+3.3V_RUN
R436 10K/J HDMI_PWR_CTRL
R667 10K/J MINI1CLK_REQ#
R405 10K/J CLK_PCIE_REQ2#

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

Change as big package (UM9)

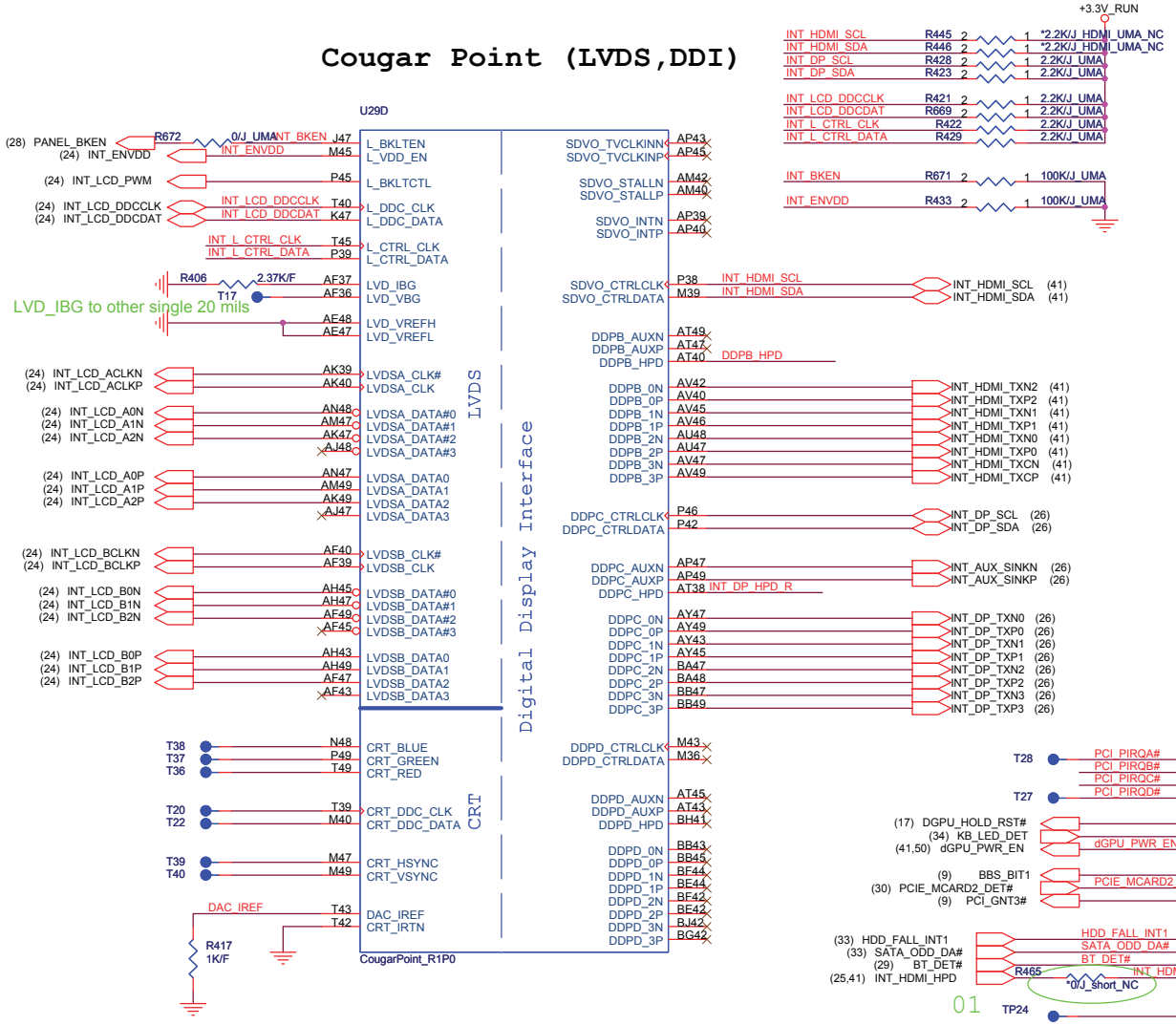
25MHz Clock for DCI Function

XTAL25_IN — R662 1M/J — XTAL25_OUT
Y3 25MHz
C683 22P/50V/NPO
C685 22P/50V/NPO

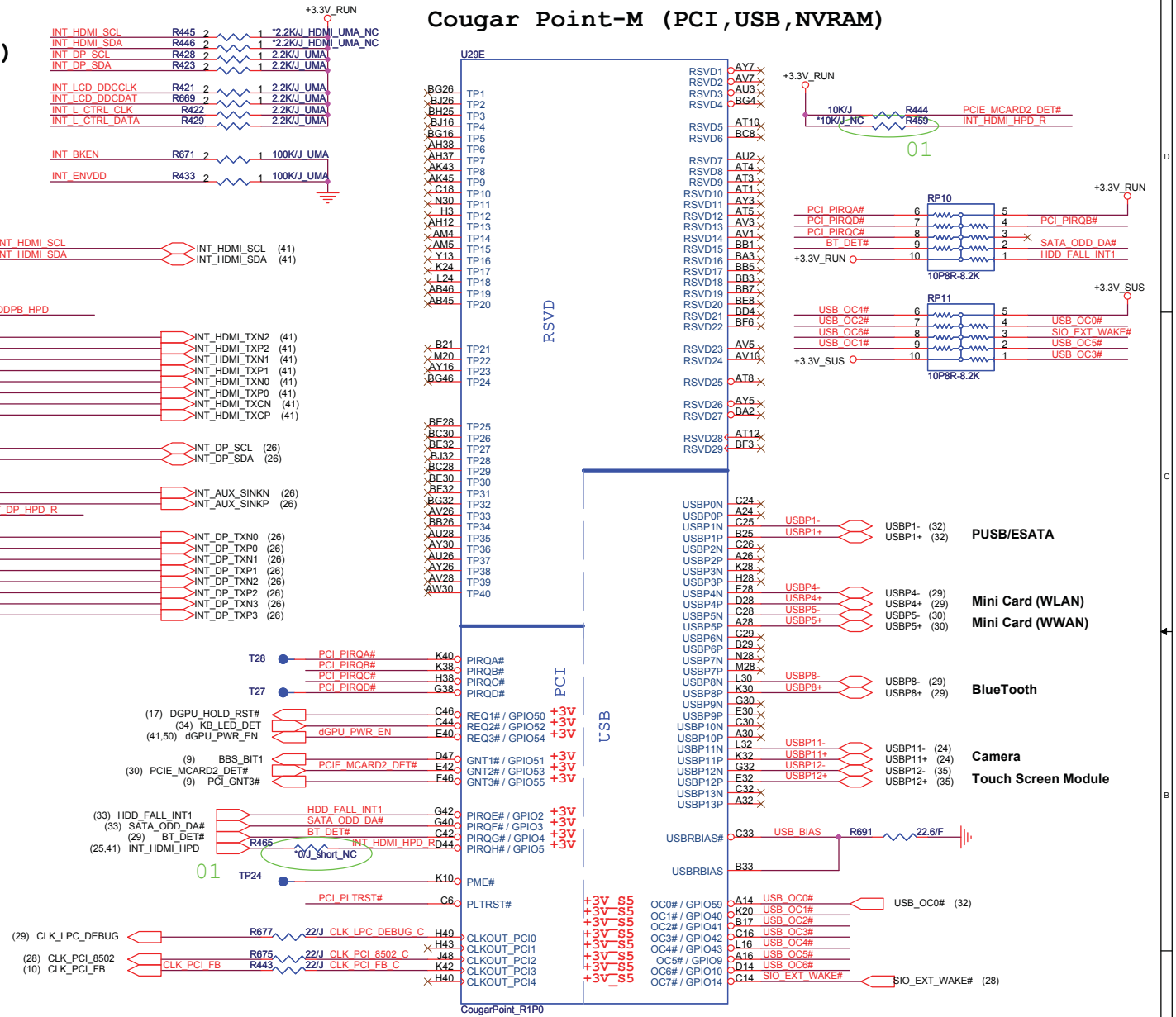
Quanta Computer Inc.
PROJECT : GM6C MLK DIS

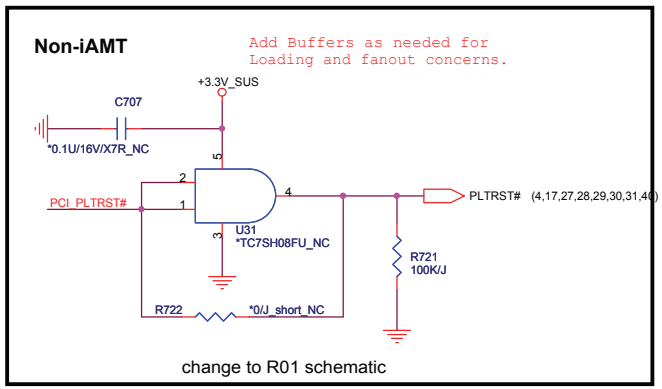
Size	Document Number	Rev
	Cougar Point 3/7	1A
Date: Friday, January 07, 2011	Sheet 10 of 59	

Cougar Point (LVDS,DDI)



Cougar Point-M (PCI,USB,NVRAM)





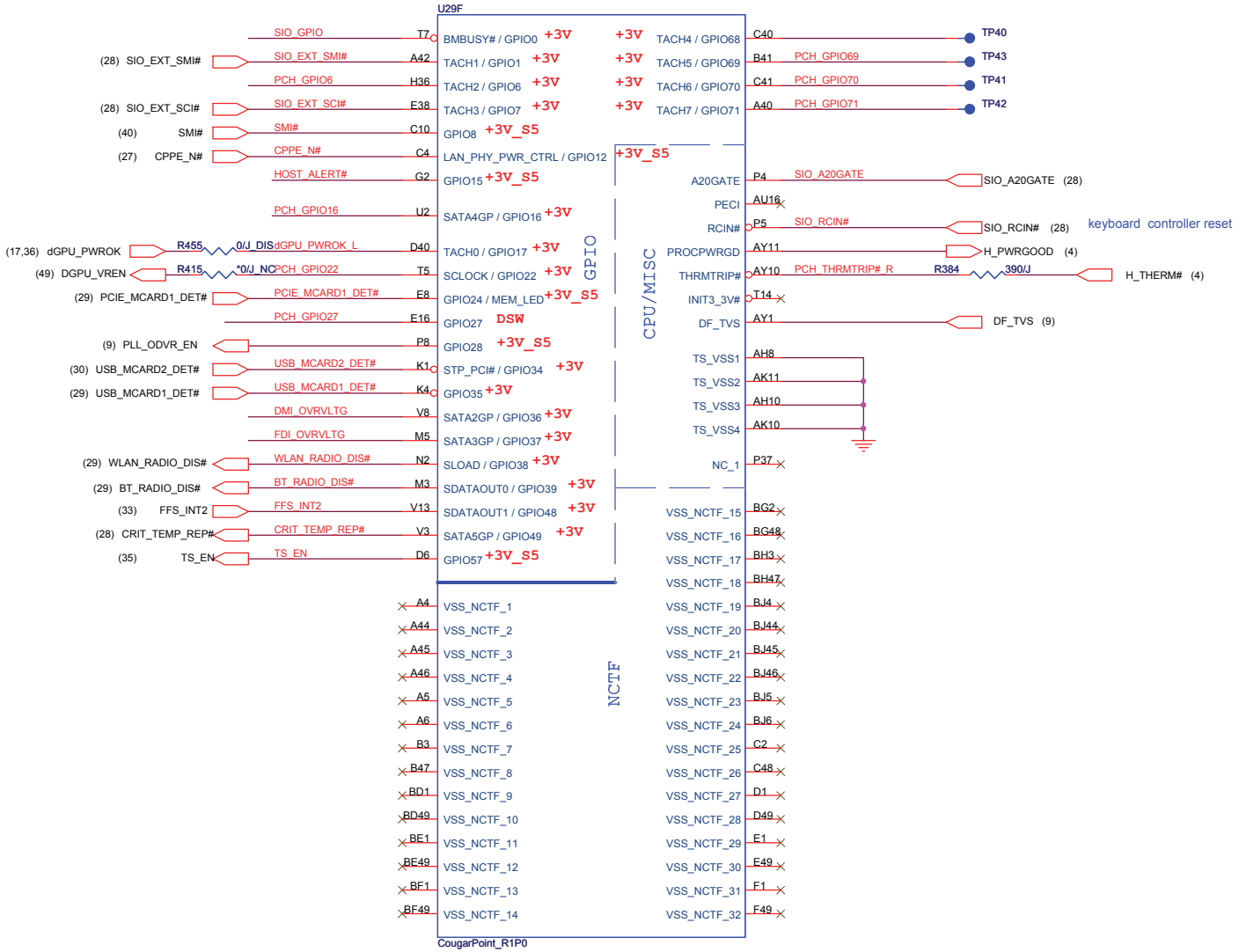
Quanta Computer Inc.

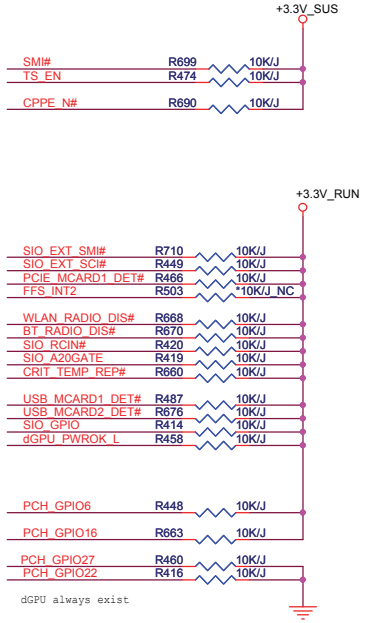
PROJECT : GM6C MLK DIS

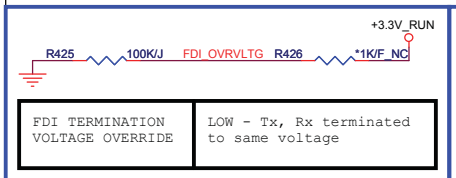
Size	Document Number	Rev
	Cougar Point 4/7	1A

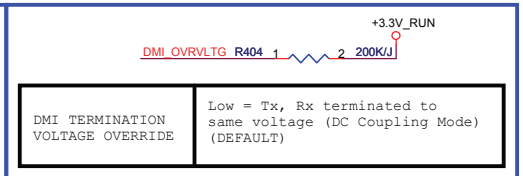
Date: Friday, January 07, 2011 Sheet 11 of 59

Cougar Point (GPIO,VSS_NCTF,RSVD)

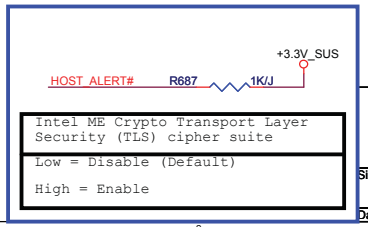








internal PD resistor 20K-ohm
To avoid voltage be divided,
please change GPIO36 PU resistor from
10K-ohm to 200K-ohm. (07/12)

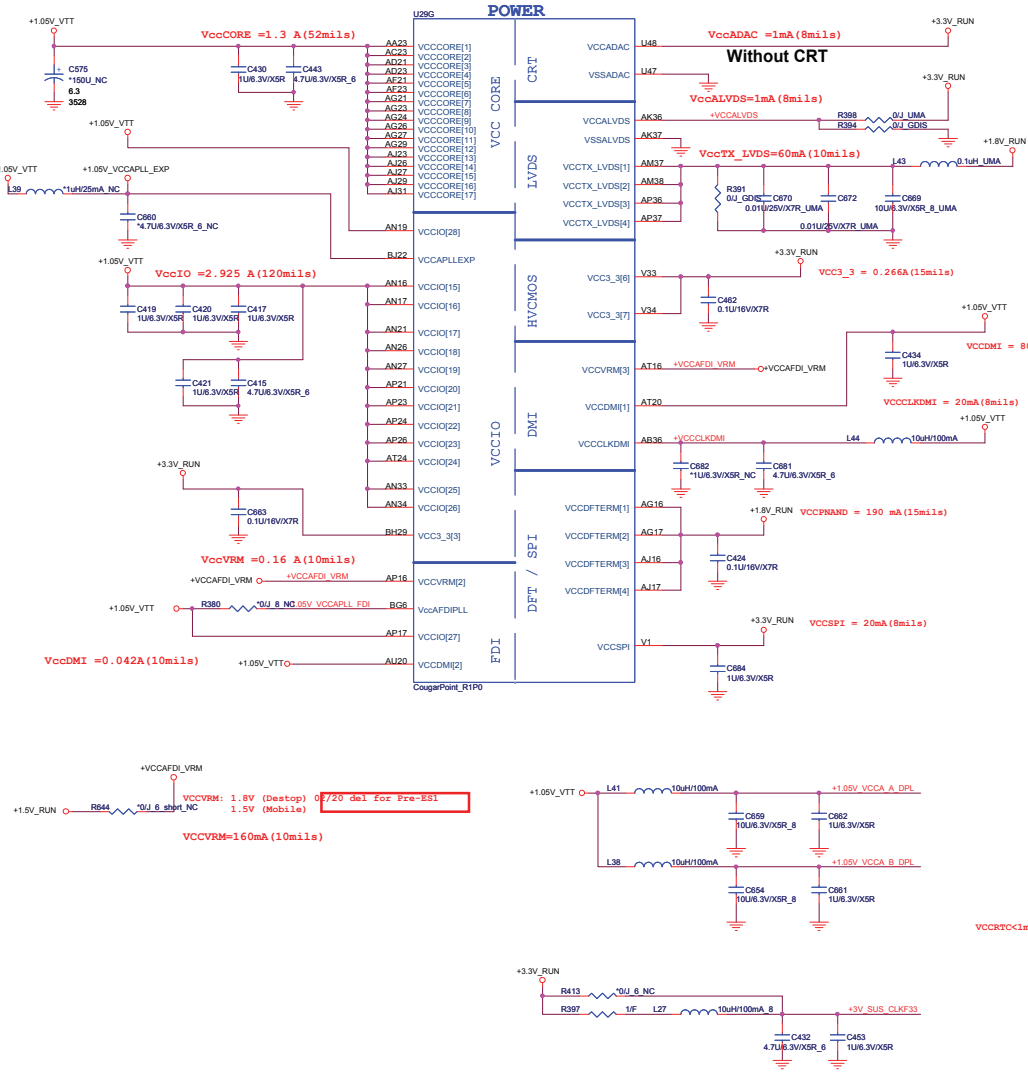


Quanta Computer Inc.
PROJECT : GM6C MLK DIS

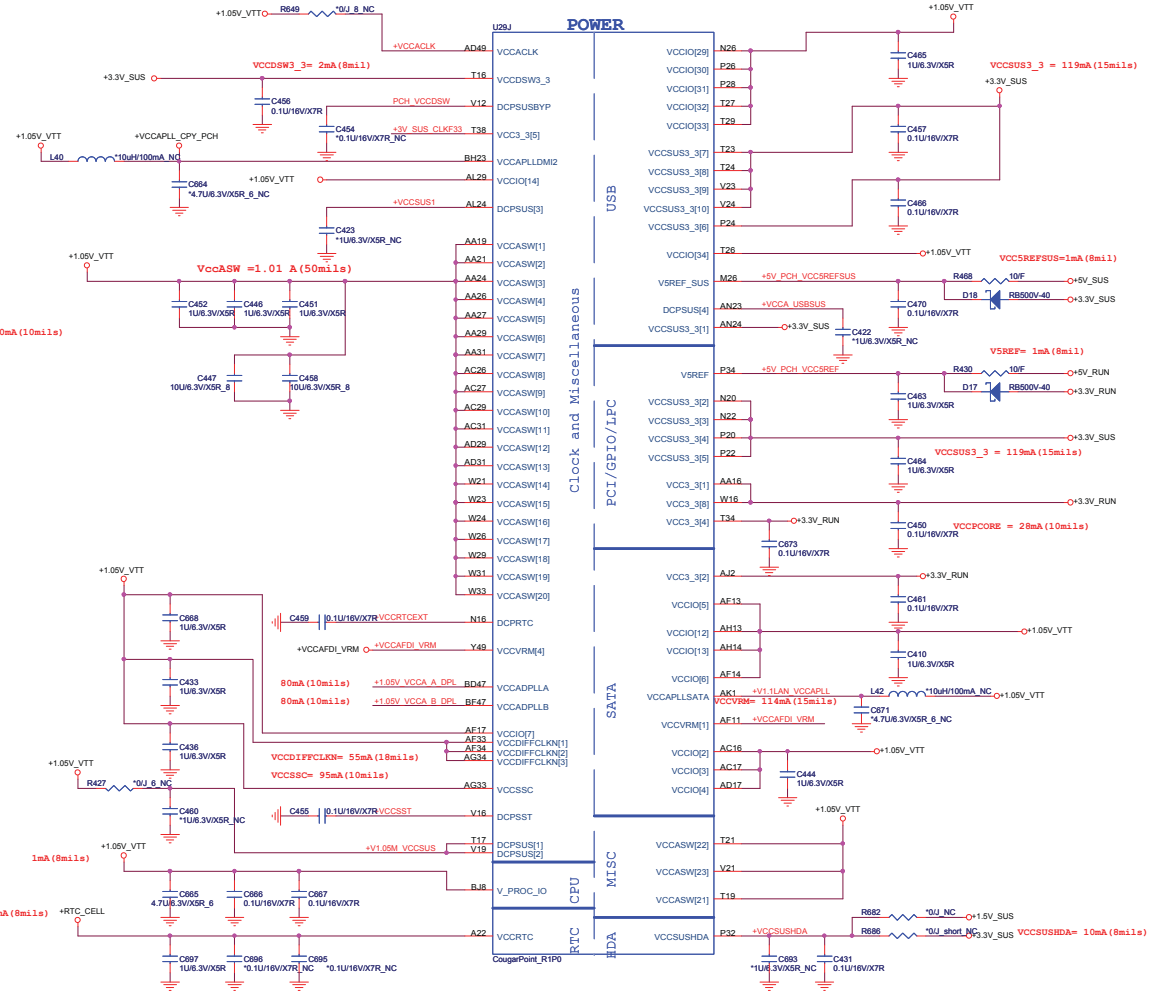
Size	Document Number	Rev
	Cougar Point 5/7	1A

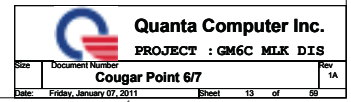
Date: Friday, January 07, 2011 Sheet 12 of 59

COUGAR POINT (POWER)

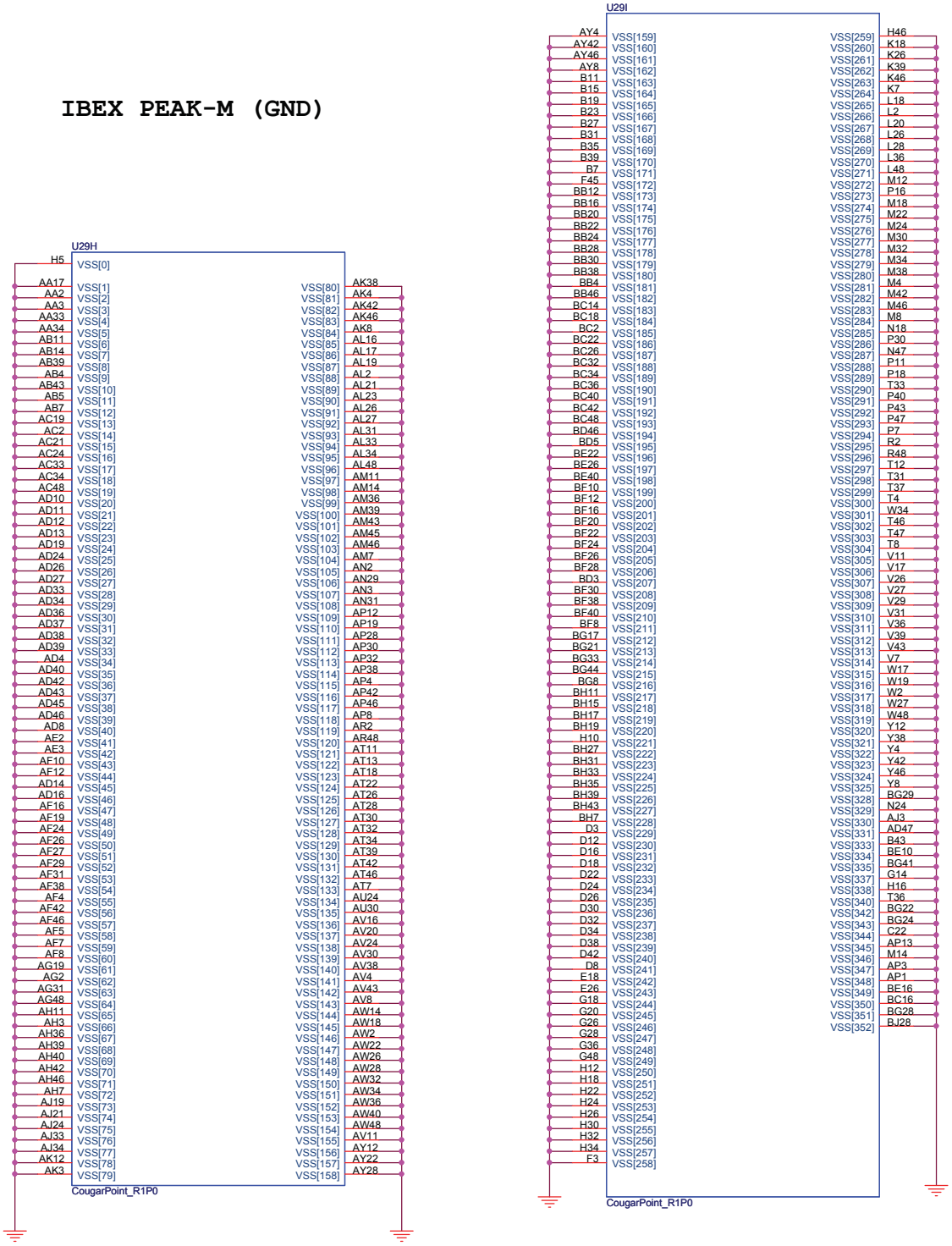


Cougar Point-M (POWER)



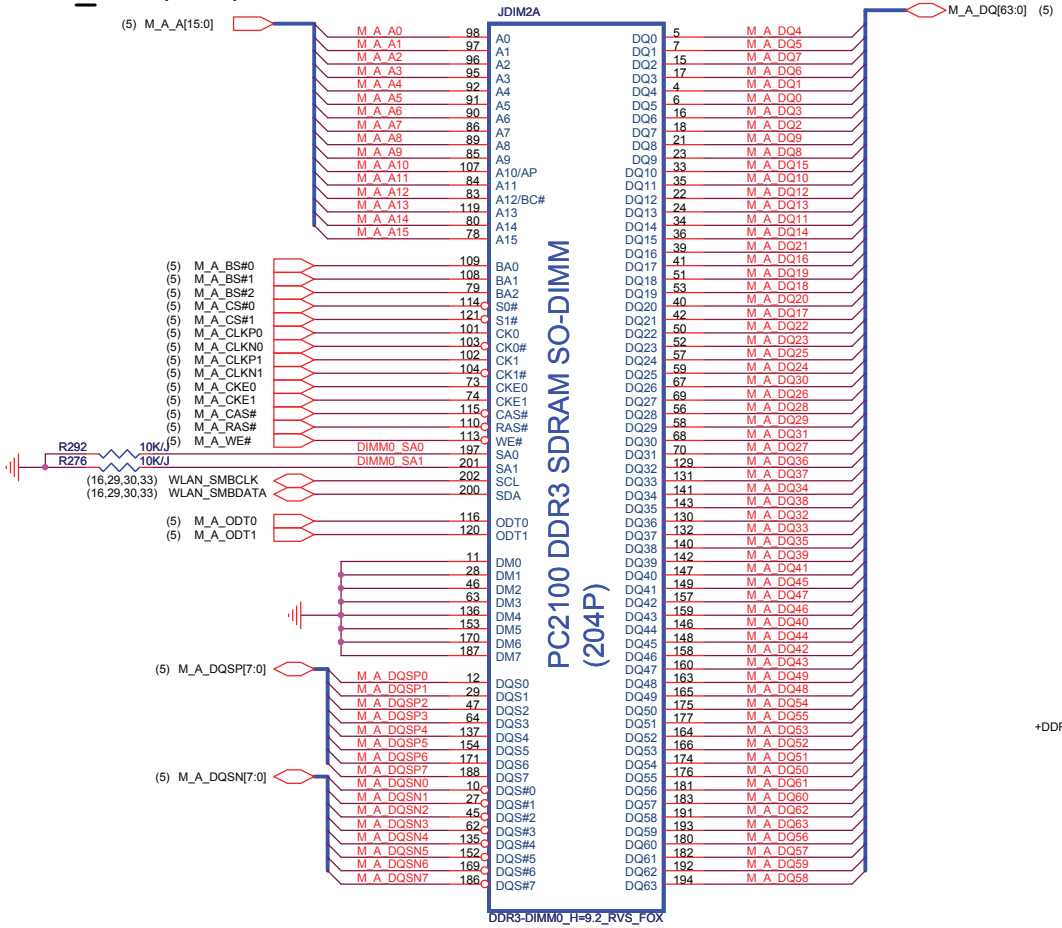


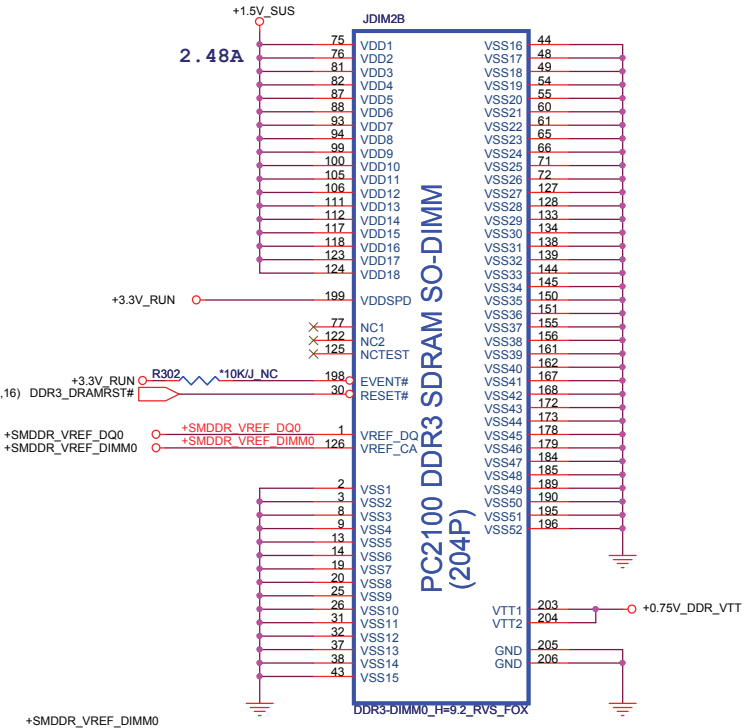
IBEX PEAK-M (GND)

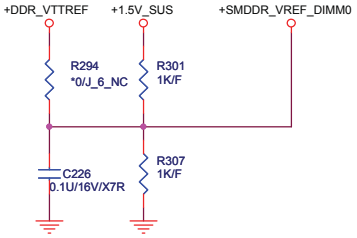


Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: Cougar Point 7/7	Rev: 1A
Date: Friday, January 07, 2011	Sheet 14 of 59	

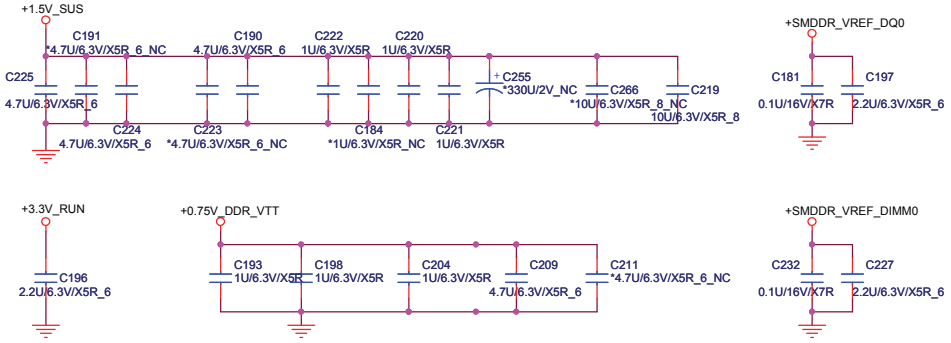
DDR_STD (DDR)



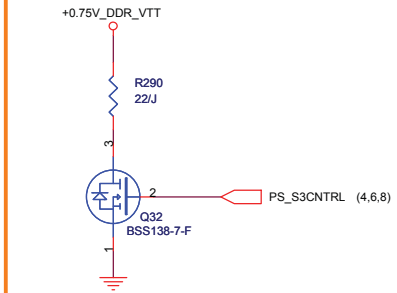




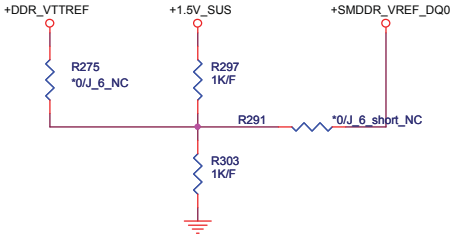
Place these Caps near So-Dimm0.



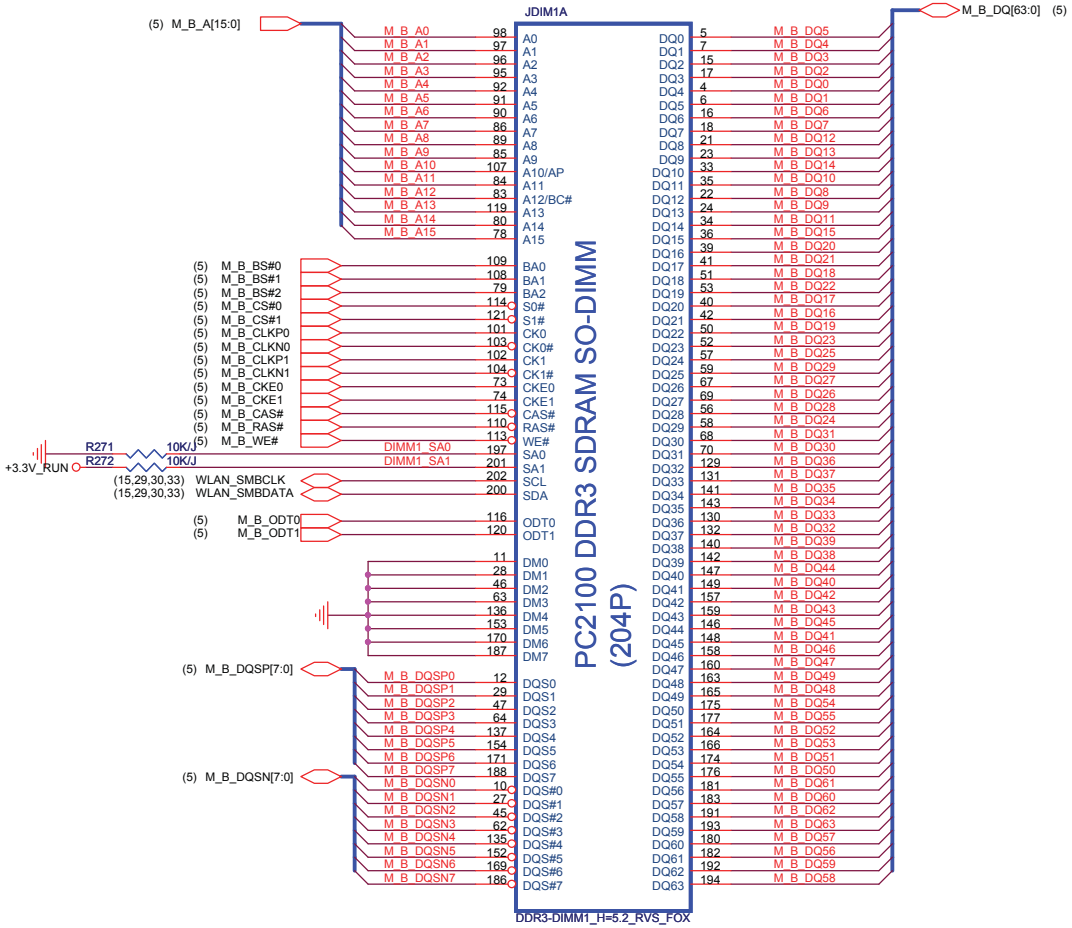
S3 Power reduce

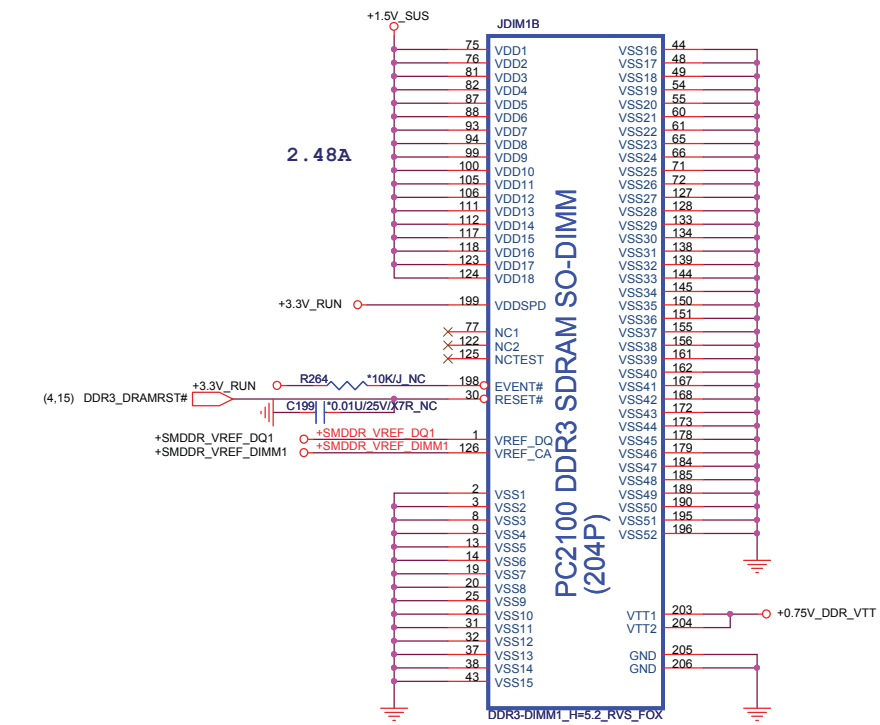


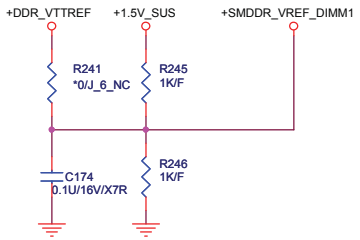
M1 VREF Solution

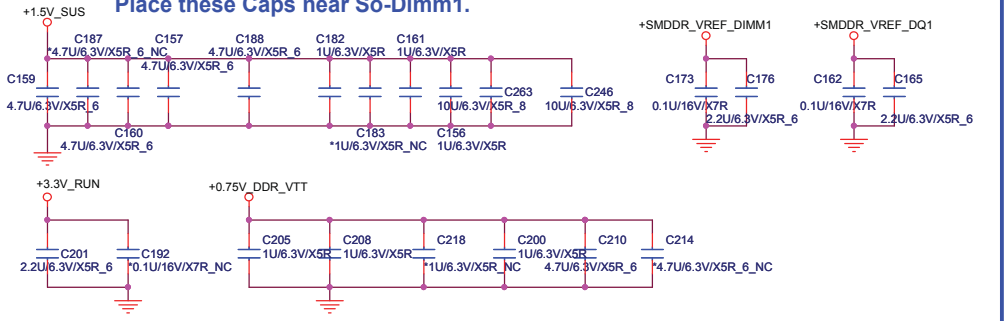


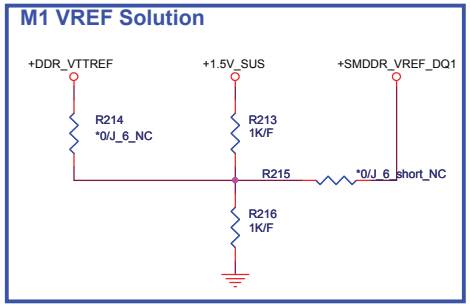
Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: DDRIII SO-DIMM-0	Rev: 1A
Date: Friday, January 07, 2011	Sheet 15 of 59	







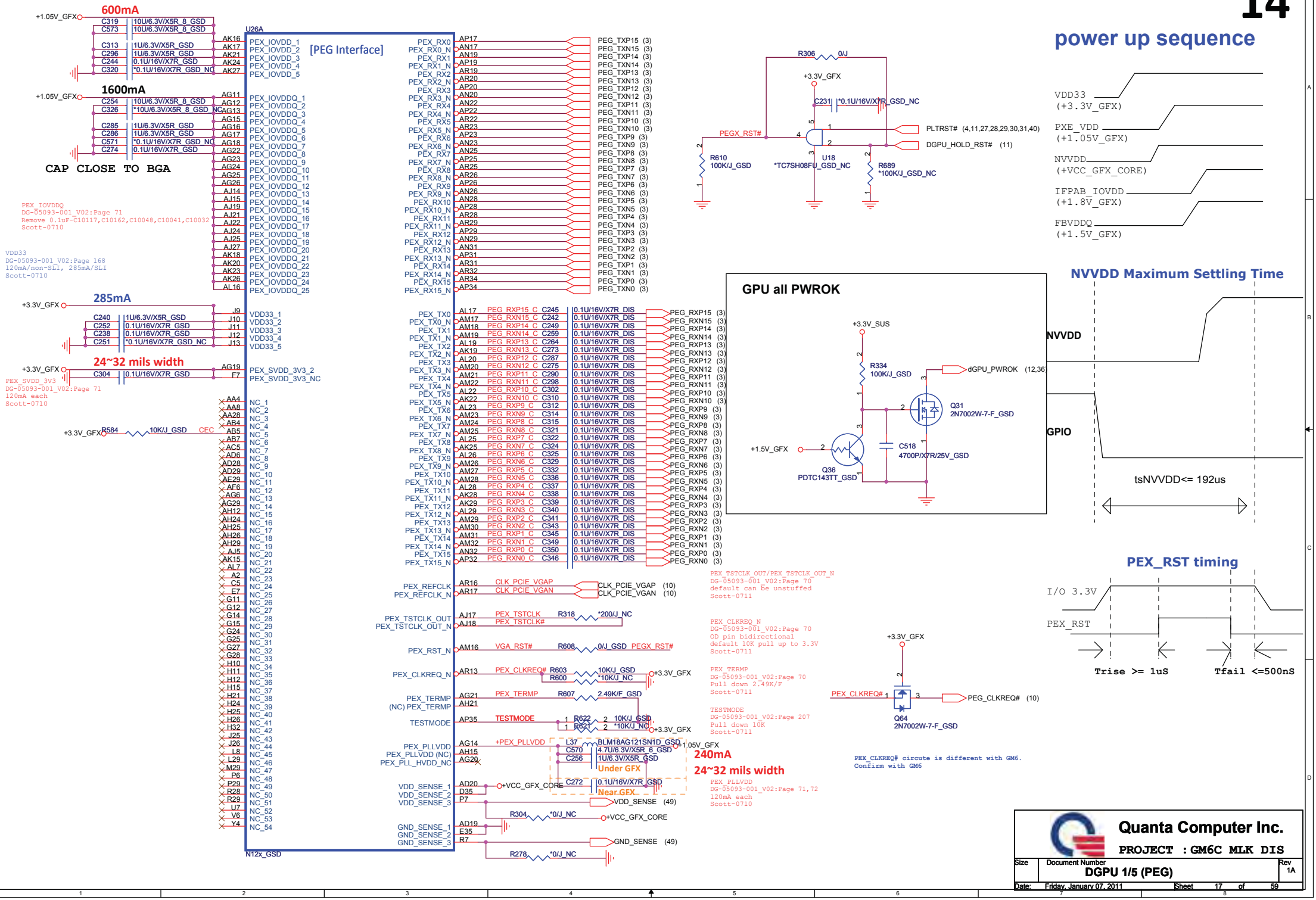




Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
Date: Friday, January 07, 2011	Sheet 16 of 59	


600mA
1600mA
CAP CLOSE TO BGA
285mA
24~32 mils width
[PEG Interface]
U26A
power up sequence
VDD33 (+3.3V_GFX)
PXE_VDD (+1.05V_GFX)
NVVDD (+VCC_GFX_CORE)
IFPAB_IOVDD (+1.8V_GFX)
FBVDDQ (+1.5V_GFX)
GPU all PWROK
NVVDD Maximum Settling Time
tsNVVDD<= 192us
PEX_RST timing
I/O 3.3V
PEX_RST
Trise >= 1uS
Tfail <=500nS
240mA
24~32 mils width
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
DGPU 1/5 (PEG)
Friday, January 07, 2011

Memory ODT,CKE,RST Termination
DG-05093-001_V02:Page 97
PRD-05272-002_v01:Page 3

U26B — [MEMORY I/F A] — N12x_GSD

U26C — MEMORY I/F C — N12x_GSD

(22) FBA_CMD[30:0] / (23) FBC_CMD[30:0]

	FBA_CMD	U26B	FBC_CMD	U26C
	FBA_CMD0	U30	FBC_CMD0	F18
	FBA_CMD1	V30	FBC_CMD1	E19
	FBA_CMD2	U31	FBC_CMD2	D18
	FBA_CMD3	V32	FBC_CMD3	C17
	FBA_CMD4	T35	FBC_CMD4	F19
	FBA_CMD5	U33	FBC_CMD5	C19
	FBA_CMD6	W32	FBC_CMD6	B17
	FBA_CMD7	W33	FBC_CMD7	E20
	FBA_CMD8	W31	FBC_CMD8	B19
	FBA_CMD9	W34	FBC_CMD9	D20
	FBA_CMD10	U34	FBC_CMD10	A19
	FBA_CMD11	U35	FBC_CMD11	D19
	FBA_CMD12	U32	FBC_CMD12	C20
	FBA_CMD13	T34	FBC_CMD13	F20
	FBA_CMD14	T33	FBC_CMD14	B20
	FBA_CMD15	W30	FBC_CMD15	G21
	FBA_CMD16	AB30	FBC_CMD16	F22
	FBA_CMD17	AA30	FBC_CMD17	F24
	FBA_CMD18	AB31	FBC_CMD18	F23
	FBA_CMD19	AA32	FBC_CMD19	C25
	FBA_CMD20	AB33	FBC_CMD20	C23
	FBA_CMD21	Y32	FBC_CMD21	F21
	FBA_CMD22	Y33	FBC_CMD22	F22
	FBA_CMD23	AB34	FBC_CMD23	D21
	FBA_CMD24	AB35	FBC_CMD24	A23
	FBA_CMD25	Y35	FBC_CMD25	D22
	FBA_CMD26	W35	FBC_CMD26	B23
	FBA_CMD27	Y34	FBC_CMD27	C22
	FBA_CMD28	Y31	FBC_CMD28	B22
	FBA_CMD29	Y30	FBC_CMD29	A22
	FBA_CMD30	W29	FBC_CMD30	A20
	FBA_CMD31 (NC)	Y29	FBC_CMD31 (NC)	G20

(22) VMA_DM[7:0] / (23) VMC_DM[7:0]

	VMA_DM	U26B	VMC_DM	U26C
	VMA_DM0	P32	VMC_DM0	A16
	VMA_DM1	H34	VMC_DM1	D10
	VMA_DM2	J30	VMC_DM2	F11
	VMA_DM3	P30	VMC_DM3	D15
	VMA_DM4	AF32	VMC_DM4	D27
	VMA_DM5	AL32	VMC_DM5	D34
	VMA_DM6	AL34	VMC_DM6	A34
	VMA_DM7	AF35	VMC_DM7	D28

(22) VMA_WDQS[7:0] / (23) VMC_WDQS[7:0]

	VMA_WDQS	U26B	VMC_WDQS	U26C
	VMA_WDQS0	L34	VMC_WDQS0	C14
	VMA_WDQS1	H35	VMC_WDQS1	A10
	VMA_WDQS2	J32	VMC_WDQS2	E10
	VMA_WDQS3	N31	VMC_WDQS3	D14
	VMA_WDQS4	AE31	VMC_WDQS4	E26
	VMA_WDQS5	AJ32	VMC_WDQS5	D32
	VMA_WDQS6	AJ34	VMC_WDQS6	A32
	VMA_WDQS7	AC33	VMC_WDQS7	B26

(22) VMA_RDQS[7:0] / (23) VMC_RDQS[7:0]

	VMA_RDQS	U26B	VMC_RDQS	U26C
	VMA_RDQS0	L35	VMC_RDQS0	B14
	VMA_RDQS1	G35	VMC_RDQS1	B10
	VMA_RDQS2	H31	VMC_RDQS2	D9
	VMA_RDQS3	N32	VMC_RDQS3	E14
	VMA_RDQS4	AD32	VMC_RDQS4	F26
	VMA_RDQS5	AJ31	VMC_RDQS5	D31
	VMA_RDQS6	AJ35	VMC_RDQS6	A31
	VMA_RDQS7	AC34	VMC_RDQS7	A26

U26B data bus:

FBA_D00	L32	VMA_DQ0	FBA_D32	AG32	VMA_DQ32
FBA_D01	N33	VMA_DQ1	FBA_D33	AG32	VMA_DQ33
FBA_D02	L33	VMA_DQ2	FBA_D34	AH31	VMA_DQ34
FBA_D03	N34	VMA_DQ3	FBA_D35	AF31	VMA_DQ35
FBA_D04	N35	VMA_DQ4	FBA_D36	AF30	VMA_DQ36
FBA_D05	P35	VMA_DQ5	FBA_D37	AE30	VMA_DQ37
FBA_D06	P33	VMA_DQ6	FBA_D38	AC32	VMA_DQ38
FBA_D07	P34	VMA_DQ7	FBA_D39	AD30	VMA_DQ39
FBA_D08	K35	VMA_DQ8	FBA_D40	AN33	VMA_DQ40
FBA_D09	K33	VMA_DQ9	FBA_D41	AL31	VMA_DQ41
FBA_D10	K34	VMA_DQ10	FBA_D42	AM33	VMA_DQ42
FBA_D11	H33	VMA_DQ11	FBA_D43	AL33	VMA_DQ43
FBA_D12	G34	VMA_DQ12	FBA_D44	AK30	VMA_DQ44
FBA_D13	G33	VMA_DQ13	FBA_D45	AK32	VMA_DQ45
FBA_D14	E34	VMA_DQ14	FBA_D46	AJ30	VMA_DQ46
FBA_D15	E33	VMA_DQ15	FBA_D47	AH30	VMA_DQ47
FBA_D16	G31	VMA_DQ16	FBA_D48	AH33	VMA_DQ48
FBA_D17	F30	VMA_DQ17	FBA_D49	AH35	VMA_DQ49
FBA_D18	G30	VMA_DQ18	FBA_D50	AH34	VMA_DQ50
FBA_D19	G32	VMA_DQ19	FBA_D51	AH32	VMA_DQ51
FBA_D20	K30	VMA_DQ20	FBA_D52	AJ33	VMA_DQ52
FBA_D21	K32	VMA_DQ21	FBA_D53	AL35	VMA_DQ53
FBA_D22	H30	VMA_DQ22	FBA_D54	AM34	VMA_DQ54
FBA_D23	K31	VMA_DQ23	FBA_D55	AM35	VMA_DQ55
FBA_D24	L31	VMA_DQ24	FBA_D56	AF33	VMA_DQ56
FBA_D25	L30	VMA_DQ25	FBA_D57	AE32	VMA_DQ57
FBA_D26	M32	VMA_DQ26	FBA_D58	AF34	VMA_DQ58
FBA_D27	N30	VMA_DQ27	FBA_D59	AE35	VMA_DQ59
FBA_D28	M30	VMA_DQ28	FBA_D60	AE34	VMA_DQ60
FBA_D29	P31	VMA_DQ29	FBA_D61	AE33	VMA_DQ61
FBA_D30	R32	VMA_DQ30	FBA_D62	AB32	VMA_DQ62
FBA_D31	R30	VMA_DQ31	FBA_D63	AC35	VMA_DQ63

U26C data bus:

FBC_D00	B13	VMC_DQ0	FBC_D32	F17	VMC_DQ31
FBC_D01	D13	VMC_DQ1	FBC_D33	D29	VMC_DQ32
FBC_D02	A13	VMC_DQ2	FBC_D34	F27	VMC_DQ33
FBC_D03	A14	VMC_DQ3	FBC_D35	F28	VMC_DQ34
FBC_D04	C16	VMC_DQ4	FBC_D36	E28	VMC_DQ35
FBC_D05	B16	VMC_DQ5	FBC_D37	D26	VMC_DQ36
FBC_D06	A17	VMC_DQ6	FBC_D38	F25	VMC_DQ37
FBC_D07	D16	VMC_DQ7	FBC_D39	D24	VMC_DQ38
FBC_D08	C13	VMC_DQ8	FBC_D40	E25	VMC_DQ39
FBC_D09	B11	VMC_DQ9	FBC_D41	E32	VMC_DQ40
FBC_D10	C11	VMC_DQ10	FBC_D42	F32	VMC_DQ41
FBC_D11	A11	VMC_DQ11	FBC_D43	D33	VMC_DQ42
FBC_D12	C10	VMC_DQ12	FBC_D44	E31	VMC_DQ43
FBC_D13	C8	VMC_DQ13	FBC_D45	C33	VMC_DQ44
FBC_D14	B8	VMC_DQ14	FBC_D46	F29	VMC_DQ45
FBC_D15	A8	VMC_DQ15	FBC_D47	D30	VMC_DQ46
FBC_D16	E8	VMC_DQ16	FBC_D48	E29	VMC_DQ47
FBC_D17	F8	VMC_DQ17	FBC_D49	B29	VMC_DQ48
FBC_D18	F10	VMC_DQ18	FBC_D50	C31	VMC_DQ49
FBC_D19	F9	VMC_DQ19	FBC_D51	C29	VMC_DQ50
FBC_D20	F12	VMC_DQ20	FBC_D52	B31	VMC_DQ51
FBC_D21	D8	VMC_DQ21	FBC_D53	C32	VMC_DQ52
FBC_D22	D11	VMC_DQ22	FBC_D54	B32	VMC_DQ53
FBC_D23	E11	VMC_DQ23	FBC_D55	B35	VMC_DQ54
FBC_D24	D12	VMC_DQ24	FBC_D56	B34	VMC_DQ55
FBC_D25	E13	VMC_DQ25	FBC_D57	A29	VMC_DQ56
FBC_D26	F13	VMC_DQ26	FBC_D58	B28	VMC_DQ57
FBC_D27	F14	VMC_DQ27	FBC_D59	C28	VMC_DQ58
FBC_D28	F15	VMC_DQ28	FBC_D60	C26	VMC_DQ59
FBC_D29	E16	VMC_DQ29	FBC_D61	D25	VMC_DQ60
FBC_D30	F16	VMC_DQ30	FBC_D62	B25	VMC_DQ61
FBC_D31	F17	VMC_DQ31	FBC_D63	A25	VMC_DQ62

FBA_CLK0 / FBA_CLK0_N / FBA_CLK1 / FBA_CLK1_N → VMA_CLK0 / VMA_CLK0# / VMA_CLK1 / VMA_CLK1# (22)

FBC_CLK0 / FBC_CLK0_N / FBC_CLK1 / FBC_CLK1_N → VMC_CLK0 / VMC_CLK0# / VMC_CLK1 / VMC_CLK1# (23)

15mils width

(FBA_DEBUG) FBA_DEBUG0 / (NC) FBA_DEBUG1 / FB_VREF_NC — FBA_DEBUG — R327 *60.4/F_NC — +1.5V_GFX

(FBC_DEBUG) FBB_DEBUG0 / (NC) FBB_DEBUG1 — FBC_DEBUG — R314 *60.4/F_NC — +1.5V_GFX

FBA_DEBUG
PRD-05272-002_v01:Page 3

+FB_VREF1 — TP16 — 15mils width

+1.5V_GFX → FBVDDQ_1 … FBVDDQ_19 (U26B)

+1.5V_GFX → FBVDDQ_20 … FBVDDQ_38 (U26C)

C388	4.7U/6.3V/X5R_6_GSD
C261	1U/6.3V/X5R_6_GSD
C262	1U/6.3V/X5R_6_GSD
C366	0.1U/16V/X7R_GSD
C300	0.1U/16V/X7R_GSD
C330	0.1U/16V/X7R_GSD
C213	0.1U/16V/X7R_GSD
C328	0.1U/16V/X7R_GSD
C344	0.1U/16V/X7R_GSD
C334	*0.1U/16V/X7R_GSD_NC
C333	0.1U/16V/X7R_GSD

FBVDDQ
DG-05093-001_V02:Page 98
DA-05206_V04:Page 21
Scott-0710

+FB_DLLAVDD — L26 BLM18PG300SN1_GSD — +1.05V_GFX

FB_DLLAVDD1 / (NC) FB_DLLAVDD2 / (NC) FB_DLLAVDD3 — R321 0/J_GSD — 12mils width

FB_PLLAVDD1 / (NC) FB_PLLAVDD2 / (NC) FB_PLLAVDD3 — R315 0/J_GSD — 12mils width

C362	2_4.7U/6.3V/X5R_6_GSD
C331	1U/6.3V/X5R_GSD
C357	0.1U/16V/X7R_GSD
C356	0.1U/16V/X7R_GSD

Near GPU / Under GPU

FB_DLLAVDD/FB_PLLAVDD
DG-05093-001_V02:Page 100
DA-05206-001_V04: Page 22

FBA_DEBUG
PRD-05272-002_v01:Page 3

FB_CAL_PD_VDDQ	R326	40.2/F_GSD
FB_CAL_PU_GND	R323	40.2/F_GSD
FB_CAL_TERM_GND	R324	60.4/F_GSD

FB_CAL_PD_VDDQ/FB_CAL_PU_GND
DG-05093-001_V02:Page 94

FB_CAL_TERM_GND
DG-05093-001_V02:Page 94
40.2/F or 60.4/F dependent on GPU SKU

For Fermi

FBA_CMD2	R348	10K/F_GSD
FBA_CMD3	R635	10K/F_GSD
FBA_CMD5	R639	10K/F_GSD
FBA_CMD18	R632	10K/F_GSD
FBA_CMD19	R350	10K/F_GSD
FBC_CMD2	R305	10K/F_GSD
FBC_CMD3	R601	10K/F_GSD
FBC_CMD5	R614	10K/F_GSD
FBC_CMD18	R618	10K/F_GSD
FBC_CMD19	R331	10K/F_GSD

VMA_DQ[63:0] → VMA_DQ[63:0] (22)

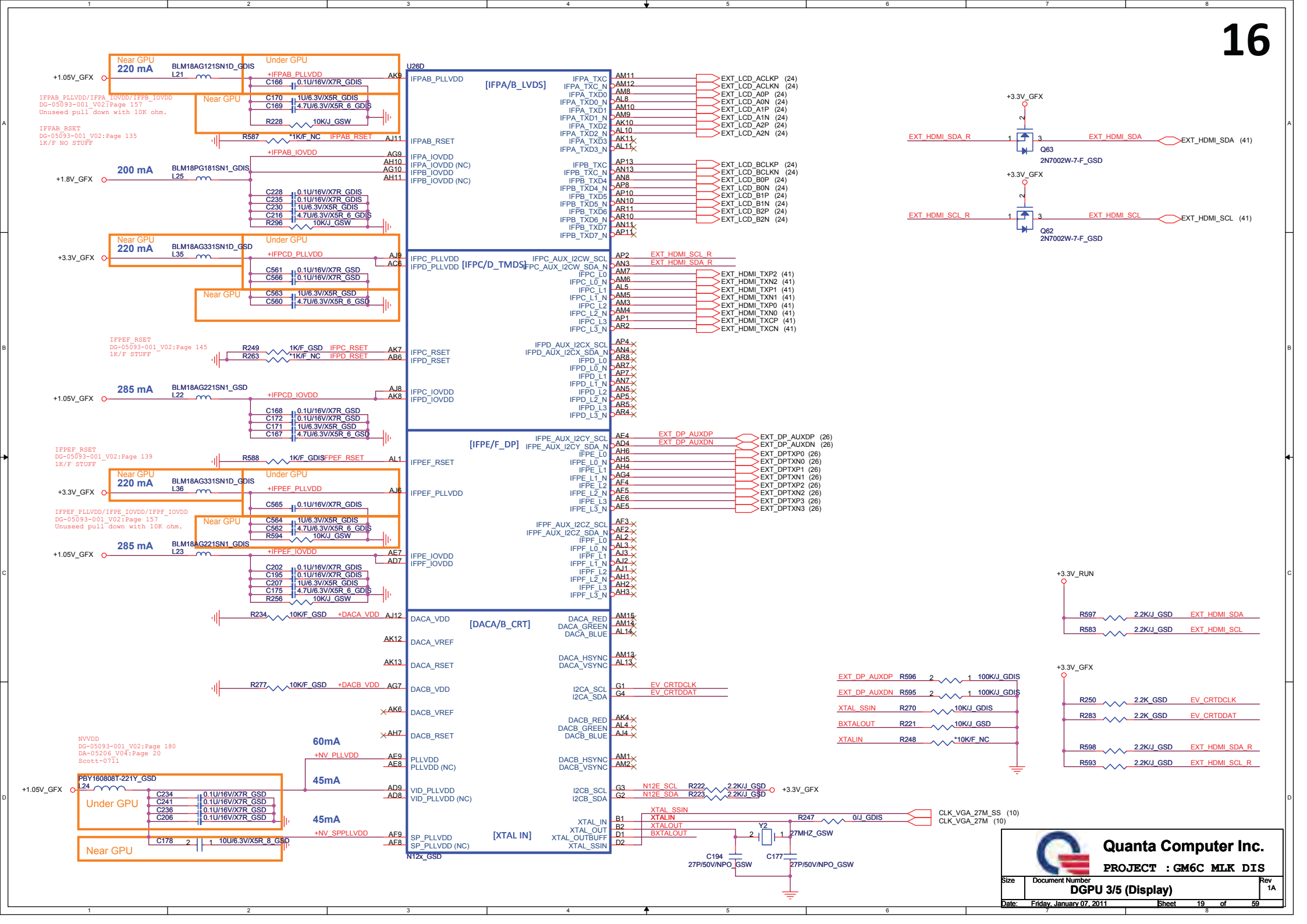
VMC_DQ[63:0] → VMC_DQ[63:0] (23)

(17,19,50) +1.05V_GFX
(17,22,23,50) +1.5V_GFX

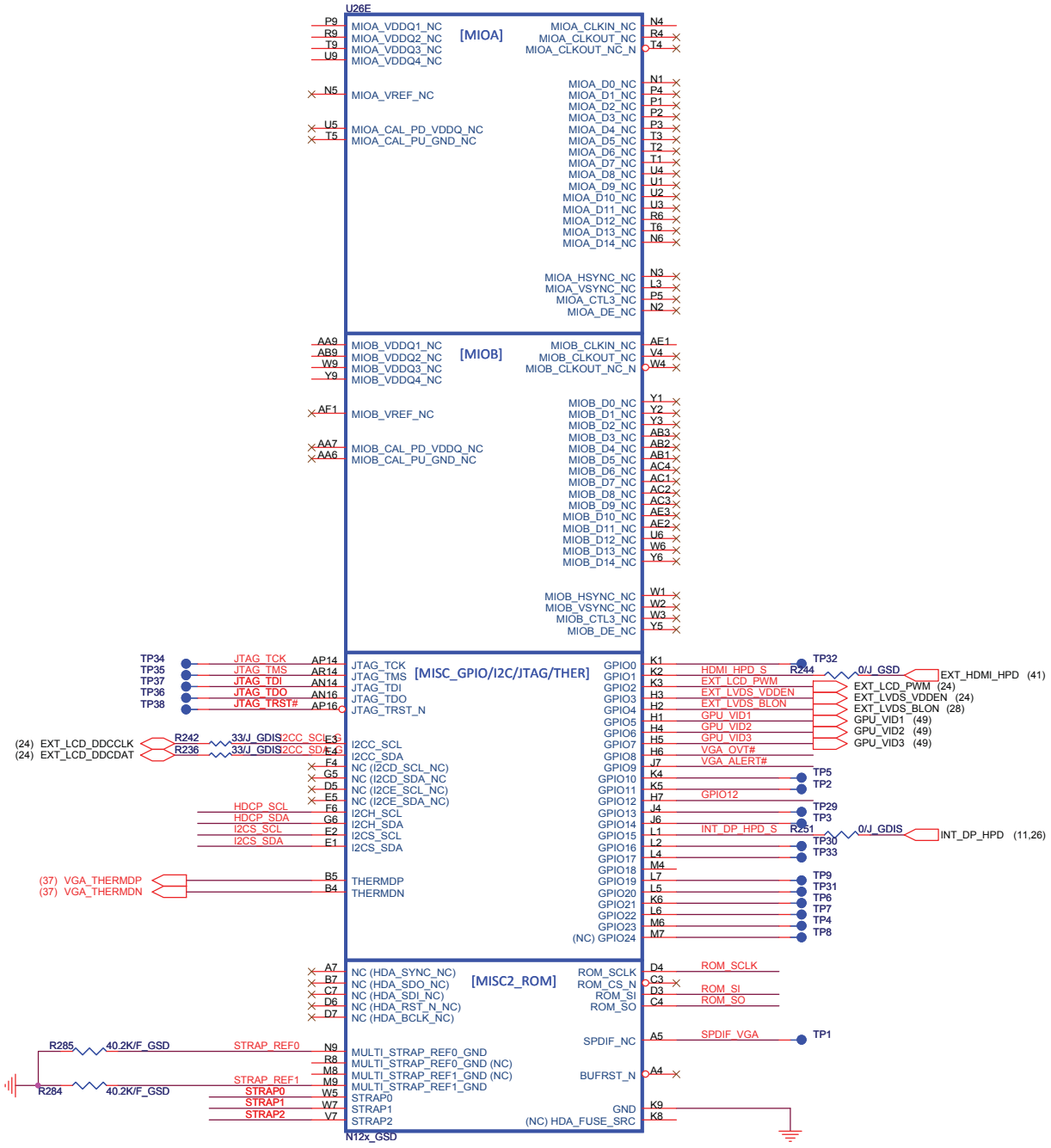
Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DGPU 2/5 (Memory)	1A

Date: Friday, January 07, 2011 Sheet 18 of 59



Quanta Computer Inc.			
PROJECT : GM6C MLK DIS			
Size	Document Number		Rev
	DGPU 3/5 (Display)		1A
Date: Friday, January 07, 2011	Sheet 19 of 59		



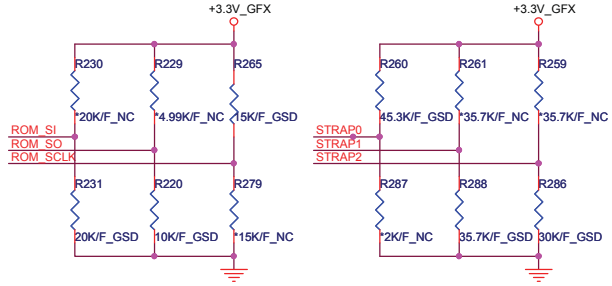
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	X010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	1110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	900MHz 512MB(64M*16) Samsung	AKD5LGHT500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKD5LZWTW02		H5TQ1G63DFR-11C
0x6(0110)	900MHz 1GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C
0x7(0111)	900MHz 1GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11

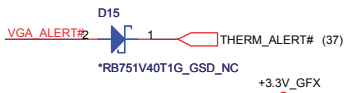
ROM_SI Strap Bit for RAM Mapping

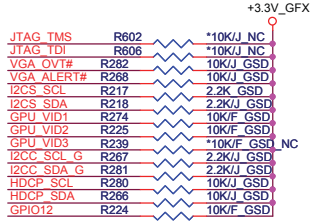
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

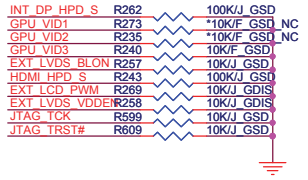


STRAP2 ROM_SCLK

N12P-GE (AJ0N12P0T02)	PD 30K	PU 15K	0xDF5	
N12P-GT (AJ0N12P0T03)	PD 35K	PU 15K	0xDF6	
N12P-GS (AJ0N12P0T04)	PD 25K	PU 15K	0xDF4	







GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI Raster Sync
12	IN	N/A	AC PWR Detect Input
13	OUT	N/A	Power Supply Control
14	OUT	N/A	Power Supply Control
15	OUT	N/A	Hot plug detect for IFP link E
16	OUT	N/A	Programmable Fan Control
17	OUT	N/A	Reserved
19	OUT	N/A	Reserved
20	OUT	N/A	Hot plug detect for IFP link D
21	OUT	N/A	Reserved
22	OUT	N/A	Hot plug detect for IFP link F
23	OUT	N/A	SLI Swap Ready single
23	OUT	N/A	

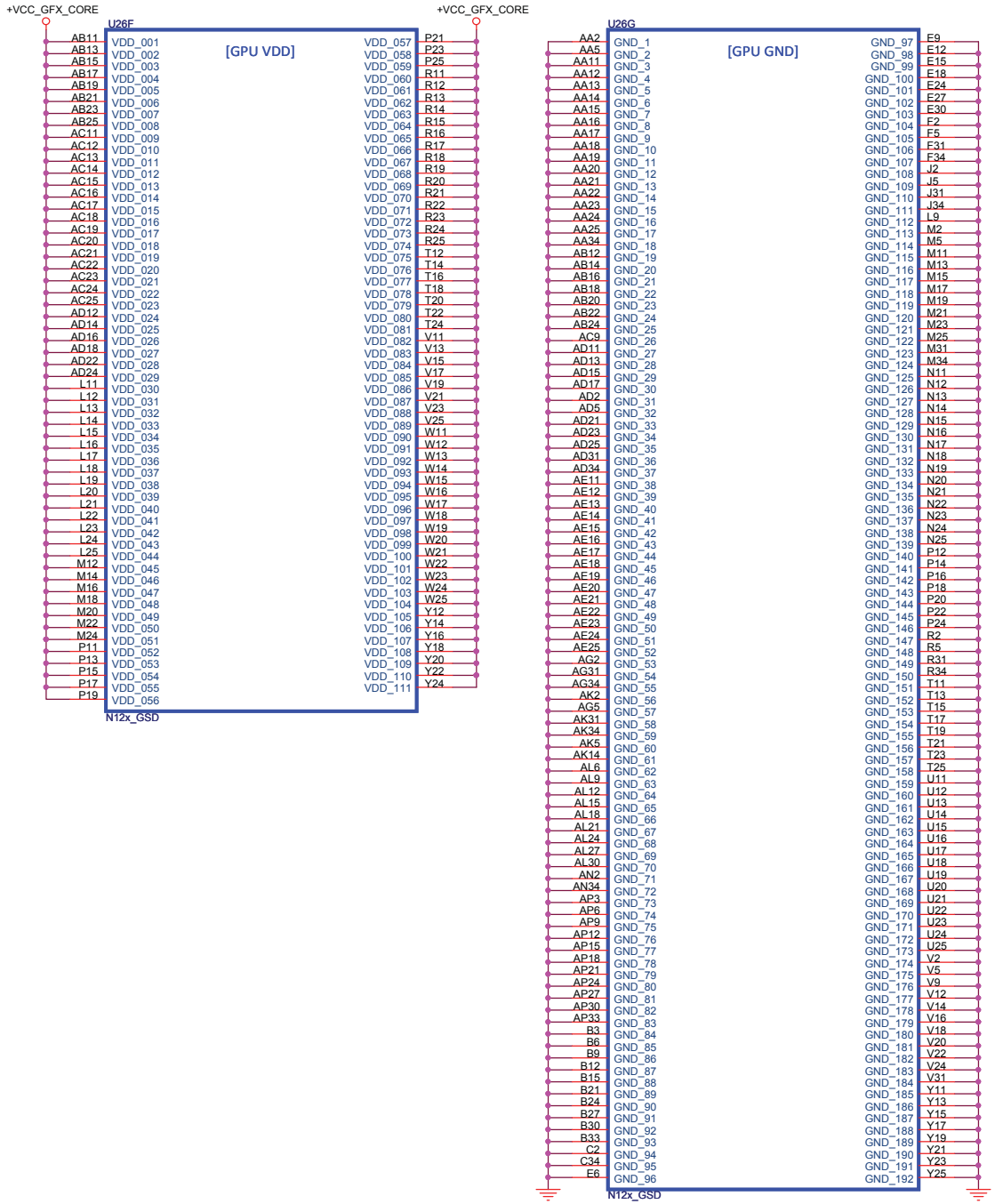
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

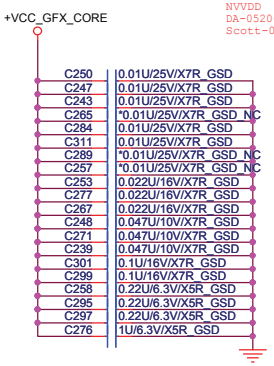
Size	Document Number	Rev
	DGPU 4/5 (MIO/GPIO)	1A

Date: Friday, January 07, 2011 Sheet 20 of 59

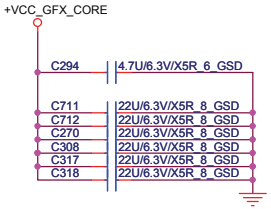
31.56A



PLACE UNDER BALLS



PLACE NEAR BALLS



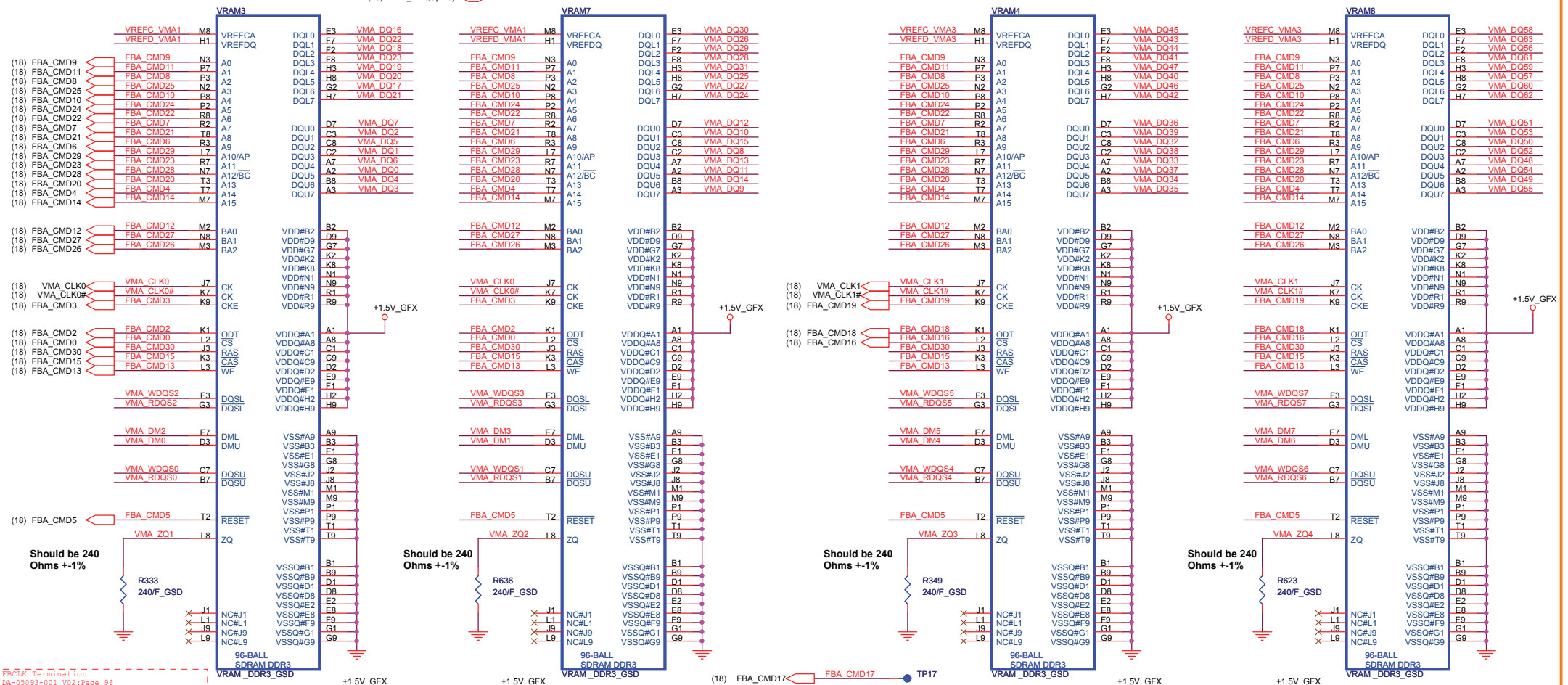
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DGPU 5/5 (Power/Ground)	1A
Date: Friday, January 07, 2011	Sheet 21 of 59	

CHANNEL A: 256MB/512MB DDR3

(18) VMA_DQ[63..0]
(18) VMA_DM[7..0]
(18) VMA_WDQS[7..0]
(18) VMA_RDQS[7..0]



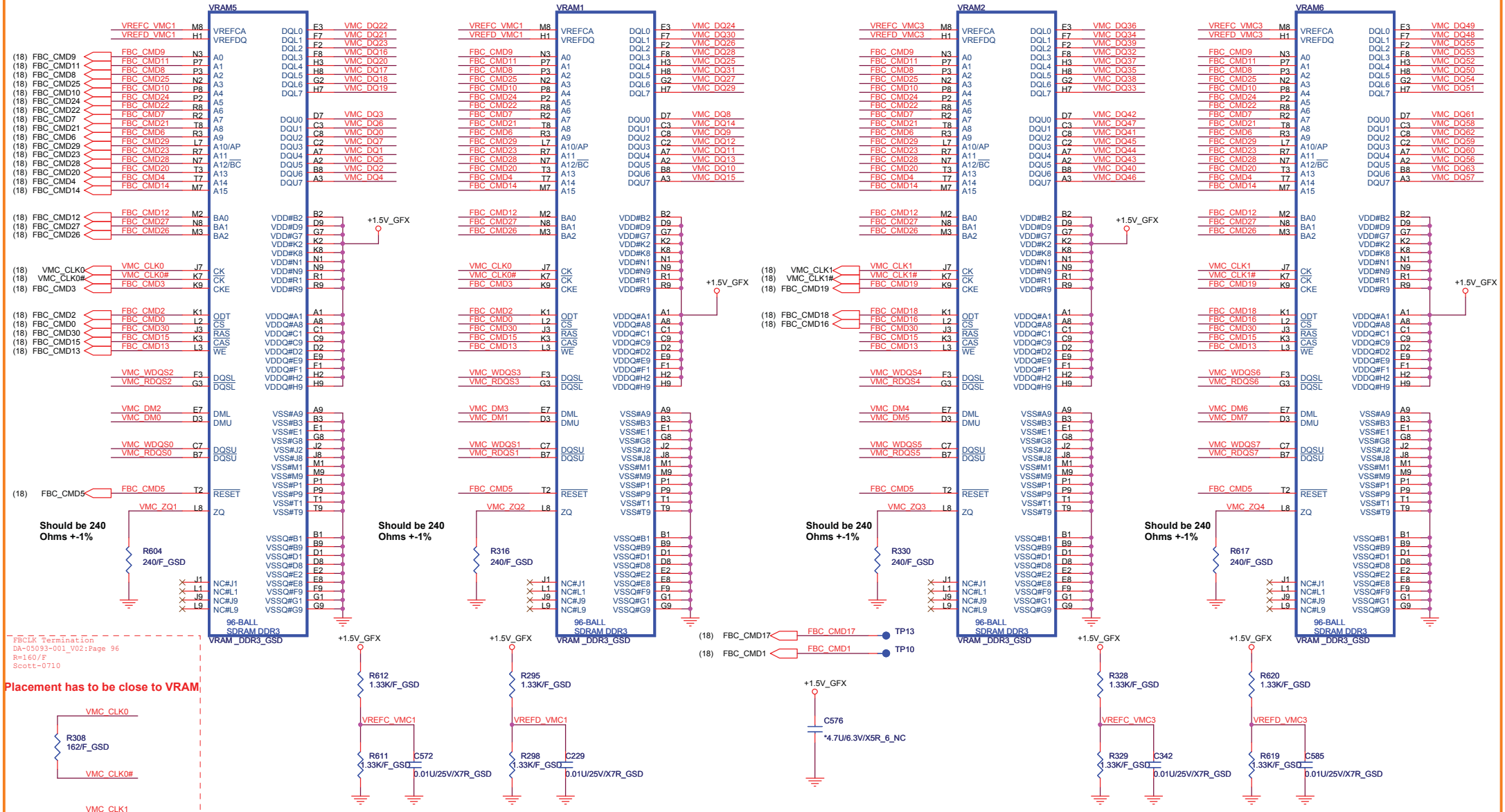
NB5

PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DGPU Memory 1/2 (DDR3)	1A
Date: Friday, January 07, 2011	Sheet 22 of 59	

CHANNEL B: 256MB/512MB DDR3

(18) VMC_DQ[63..0]
(18) VMC_DM[7..0]
(18) VMC_WDQS[7..0]
(18) VMC_RDQS[7..0]

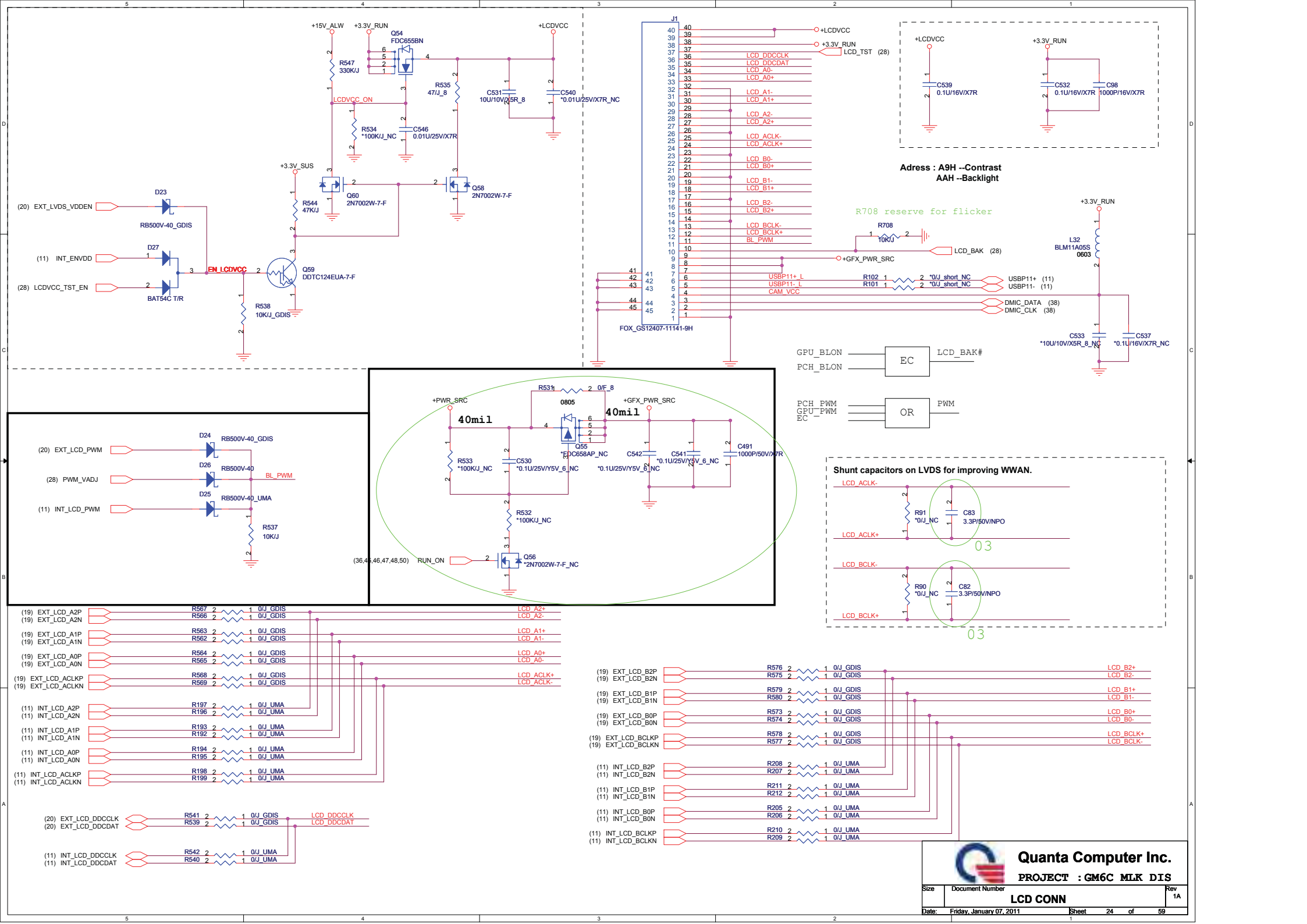


C610	10U/6.3V/X5R_8_GSD	C212	0.1U/16V/X7R_GSD
C387	10U/6.3V/X5R_8_GSD	C351	0.1U/16V/X7R_GSD
C635	10U/6.3V/X5R_8_GSD	C293	*0.1U/16V/X7R_GSD_NC
C393	1U/6.3V/X5R_GSD	C396	*0.1U/16V/X7R_GSD_NC
C646	1U/6.3V/X5R_GSD	C382	0.1U/16V/X7R_GSD
C621	1U/6.3V/X5R_GSD	C593	0.1U/16V/X7R_GSD
C278	1U/6.3V/X5R_GSD	C395	0.1U/16V/X7R_GSD
C279	*0.1U/16V/X7R_GSD_NC	C217	0.1U/16V/X7R_GSD
C647	0.1U/16V/X7R_GSD	C590	0.1U/16V/X7R_GSD
C648	0.1U/16V/X7R_GSD	C644	0.1U/16V/X7R_GSD
		C605	0.1U/16V/X7R_GSD
		C367	*0.1U/16V/X7R_GSD_NC
		C268	*0.1U/16V/X7R_GSD_NC
		C643	0.1U/16V/X7R_GSD
		C600	0.1U/16V/X7R_GSD
		C335	0.1U/16V/X7R_GSD

NB5

PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DGPU Memory 2/2 (DDR3)	1A
Date: Friday, January 07, 2011	Sheet 23 of 59	


+15V_ALW
+3.3V_RUN
Q54
FDC655BN
R547
330K/J
LCDVCC_ON
R535
47/J_8
C531
10U/10V/X5R_8
C540
*0.01U/25V/X7R_NC
R534
*100K/J_NC
C546
0.01U/25V/X7R
+LCDVCC
+3.3V_SUS
Q60
2N7002W-7-F
Q58
2N7002W-7-F
R544
47K/J
D23
RB500V-40_GDIS
(20) EXT_LVDS_VDDEN
D27
(11) INT_ENVDD
BAT54C T/R
(28) LCDVCC_TST_EN
EN_LCDVCC
Q59
DDTC124EUA-7-F
R538
10K/J_GDIS
J1
FOX_GS12407-11141-9H
+LCDVCC
+3.3V_RUN
LCD_TST (28)
LCD_DDCCLK
LCD_DDCDAT
LCD_A0-
LCD_A0+
LCD_A1-
LCD_A1+
LCD_A2-
LCD_A2+
LCD_ACLK-
LCD_ACLK+
LCD_B0-
LCD_B0+
LCD_B1-
LCD_B1+
LCD_B2-
LCD_B2+
LCD_BCLK-
LCD_BCLK+
BL_PWM
+GFX_PWR_SRC
USBP11+_L
USBP11-_L
CAM_VCC
C539
0.1U/16V/X7R
C532
0.1U/16V/X7R
C98
1000P/16V/X7R
Adress : A9H --Contrast
AAH --Backlight
R708 reserve for flicker
R708
10K/J
LCD_BAK (28)
R102
R101
*0/J_short_NC
USBP11+ (11)
USBP11- (11)
DMIC_DATA (38)
DMIC_CLK (38)
L32
BLM11A05S
0603
C533
*10U/10V/X5R_8_NC
C537
*0.1U/16V/X7R_NC
GPU_BLON
PCH_BLON
EC
LCD_BAK#
PCH_PWM
GPU_PWM
EC_
OR
PWM
+PWR_SRC
40mil
+GFX_PWR_SRC
40mil
R531
0/F_8
0805
Q55
*EDC658AP_NC
R533
*100K/J_NC
C530
*0.1U/25V/Y5V_6_NC
C542
*0.1U/25V/Y5V_6_NC
C541
*0.1U/25V/Y5V_6_NC
C491
1000P/50V/X7R
R532
*100K/J_NC
(36,45,46,47,48,50) RUN_ON
Q56
*2N7002W-7-F_NC
(20) EXT_LCD_PWM
D24
RB500V-40_GDIS
(28) PWM_VADJ
D26
RB500V-40
BL_PWM
(11) INT_LCD_PWM
D25
RB500V-40_UMA
R537
10K/J
Shunt capacitors on LVDS for improving WWAN.
LCD_ACLK-
LCD_ACLK+
R91
*0/J_NC
C83
3.3P/50V/NPO
03
LCD_BCLK-
LCD_BCLK+
R90
*0/J_NC
C82
3.3P/50V/NPO
03
(19) EXT_LCD_A2P
(19) EXT_LCD_A2N
R567
R566
0/J_GDIS
LCD_A2+
LCD_A2-
(19) EXT_LCD_A1P
(19) EXT_LCD_A1N
R563
R562
LCD_A1+
LCD_A1-
(19) EXT_LCD_A0P
(19) EXT_LCD_A0N
R564
R565
LCD_A0+
LCD_A0-
(19) EXT_LCD_ACLKP
(19) EXT_LCD_ACLKN
R568
R569
LCD_ACLK+
LCD_ACLK-
(11) INT_LCD_A2P
(11) INT_LCD_A2N
R197
R196
0/J_UMA
(11) INT_LCD_A1P
(11) INT_LCD_A1N
R193
R192
(11) INT_LCD_A0P
(11) INT_LCD_A0N
R194
R195
(11) INT_LCD_ACLKP
(11) INT_LCD_ACLKN
R198
R199
(20) EXT_LCD_DDCCLK
(20) EXT_LCD_DDCDAT
R541
R539
LCD_DDCCLK
LCD_DDCDAT
(11) INT_LCD_DDCCLK
(11) INT_LCD_DDCDAT
R542
R540
(19) EXT_LCD_B2P
(19) EXT_LCD_B2N
R576
R575
LCD_B2+
LCD_B2-
(19) EXT_LCD_B1P
(19) EXT_LCD_B1N
R579
R580
LCD_B1+
LCD_B1-
(19) EXT_LCD_B0P
(19) EXT_LCD_B0N
R573
R574
LCD_B0+
LCD_B0-
(19) EXT_LCD_BCLKP
(19) EXT_LCD_BCLKN
R578
R577
LCD_BCLK+
LCD_BCLK-
(11) INT_LCD_B2P
(11) INT_LCD_B2N
R208
R207
(11) INT_LCD_B1P
(11) INT_LCD_B1N
R211
R212
(11) INT_LCD_B0P
(11) INT_LCD_B0N
R205
R206
(11) INT_LCD_BCLKP
(11) INT_LCD_BCLKN
R210
R209
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size
Document Number
LCD CONN
Rev
1A
Date: Friday, January 07, 2011
Sheet 24 of 59

HDMI

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V
CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V
CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V

+3.3V_RUN
L9 *BLM18PG181SN1_NC
+VCC_HDMI
C46 *1U/6.3V/X5R_NC
C78 *0.1U/16V/X7R_NC
C63 *0.1U/16V/X7R_NC

U5
POWER: VCC x8 (2,11,15,21,26,33,40,46)
GND: GND x15 (1,5,12,18,24,27,31,36,37,43,49,EPAD)
CONTROL: DDC_EN, PC0, PC1, DDCBUF_EN, CFG, RT_EN#, OE#, REXT
*SN75DP139RGZR_NC

(41) HDMI_TXCP_L	HDMI_TXCP_L	C51	0.1U/16V/X7R	HDMI_TXCP_R	39 IN_D1+
(41) HDMI_TXCN_L	HDMI_TXCN_L	C49	0.1U/16V/X7R	HDMI_TXCN_R	38 IN_D1-
(41) HDMI_TXP0_L	HDMI_TXP0_L	C55	0.1U/16V/X7R	HDMI_TXP0_R	42 IN_D2+
(41) HDMI_TXN0_L	HDMI_TXN0_L	C52	0.1U/16V/X7R	HDMI_TXN0_R	41 IN_D2-
(41) HDMI_TXP1_L	HDMI_TXP1_L	C60	0.1U/16V/X7R	HDMI_TXP1_R	45 IN_D3+
(41) HDMI_TXN1_L	HDMI_TXN1_L	C56	0.1U/16V/X7R	HDMI_TXN1_R	44 IN_D3-
(41) HDMI_TXP2_L	HDMI_TXP2_L	C64	0.1U/16V/X7R	HDMI_TXP2_R	48 IN_D4+
(41) HDMI_TXN2_L	HDMI_TXN2_L	C61	0.1U/16V/X7R	HDMI_TXN2_R	47 IN_D4-

OUT_D1+ 22	HDMI_CLK+_C	HDMI_CLK+	
OUT_D1- 23	HDMI_CLK-_C	HDMI_CLK-	
OUT_D2+ 19	HDMI_TX0+_C	HDMI_TX0+	
OUT_D2- 20	HDMI_TX0-_C	HDMI_TX0-	
OUT_D3+ 16	HDMI_TX1+_C	HDMI_TX1+	
OUT_D3- 17	HDMI_TX1-_C	HDMI_TX1-	
OUT_D4+ 13	HDMI_TX2+_C	HDMI_TX2+	
OUT_D4- 14	HDMI_TX2-_C	HDMI_TX2-	
SCL_SINK 28	HDMI_CLK	HDMI_CLK	
SDA_SINK 29	HDMI_DAT	HDMI_DAT	
HPD_SINK 30	HDMI_DET_L	R38 *1K/J_NC	HDMI_DET

(41) HDMI_SCL_S — HDMI_SCL_S — 9 SCL
(41) HDMI_SDA_S — HDMI_SDA_S — 8 SDA
(11,41) INT_HDMI_HPD — INT_HDMI_HPD — 7 HPD

R388 *100K/J_NC

+3.3V_RUN
R49 *100K/J_NC
R40 *4.7K/J_NC DDC_EN
R86 *4.7K/J_NC PC0
R73 *4.7K/J_NC PC1
CFG00
(10) HDMI_PWR_CTRL — R37 *0/J_NC — OE#
R74 *3.9K/J_NC
R72 *4.7K/J_NC PC0
R47 *0/J_NC
PQ1 *2N7002W-7-F_NC
R46 *4.7K/J_NC CFG00

+5V_HDMI
R7 2.2K/J
R3 2.2K/J

CN2 LTS_ABA-HDM-024-P07

HDMI_TX2+	1 D2+	SHELL1	20
HDMI_TX2-	2 D2 Shield	SHELL2	21
HDMI_TX1+	3 D2-		
HDMI_TX1-	4 D1+		
HDMI_TX0+	5 D1 Shield		
HDMI_TX0-	6 D1-		
HDMI_CLK+	7 D0+		
HDMI_CLK-	8 D0 Shield		
	9 D0-		
HDMI_CLK	10 CK+		
HDMI_DAT	11 CK Shield		
	12 CK-		
	13 CE Remote		
	14 NC		
HDMI_DET	15 DDC CLK		
	16 DDC DATA		
	17 GND		
	18 +5V		
	19 HP DET	SHELL3	22
		SHELL4	23

+5V_RUN — HDMIF1 NANOSMDC110F-2 — +5V_HDMI
C513 *0.1U/16V/X7R_NC
C514 0.1U/16V/X7R

Reserve for EMI and close to HDMI CONN

*EXC24CG900U_NC L1: HDMI_TX2+_C / HDMI_TX2-_C ↔ HDMI_TX2+ / HDMI_TX2-
*EXC24CG900U_NC L4: HDMI_TX0+_C / HDMI_TX0-_C ↔ HDMI_TX0+ / HDMI_TX0-
*EXC24CG900U_NC L2: HDMI_TX1+_C / HDMI_TX1-_C ↔ HDMI_TX1+ / HDMI_TX1-
*EXC24CG900U_NC L3: HDMI_CLK+_C / HDMI_CLK-_C ↔ HDMI_CLK+ / HDMI_CLK-

change

HDMI_TXCP_R	HDMI_CLK+_C
HDMI_TXCN_R	HDMI_CLK-_C
HDMI_TXP0_R	HDMI_TX0+_C
HDMI_TXN0_R	HDMI_TX0-_C
HDMI_TXP1_R	HDMI_TX1+_C
HDMI_TXN1_R	HDMI_TX1-_C
HDMI_TXP2_R	HDMI_TX2+_C
HDMI_TXN2_R	HDMI_TX2-_C

UMA change to 680ohm

R736 499/F	HDMI_TX2+	
R734 499/F	HDMI_TX2-	
R737 499/F	HDMI_TX1+	
R731 499/F	HDMI_TX1-	
R729 499/F	HDMI_TX0+	
R733 499/F	HDMI_TX0-	
R735 499/F	HDMI_CLK+	
R730 499/F	HDMI_CLK-	

+3.3V_RUN — Q75 2N7002W-7-F — R732 1M

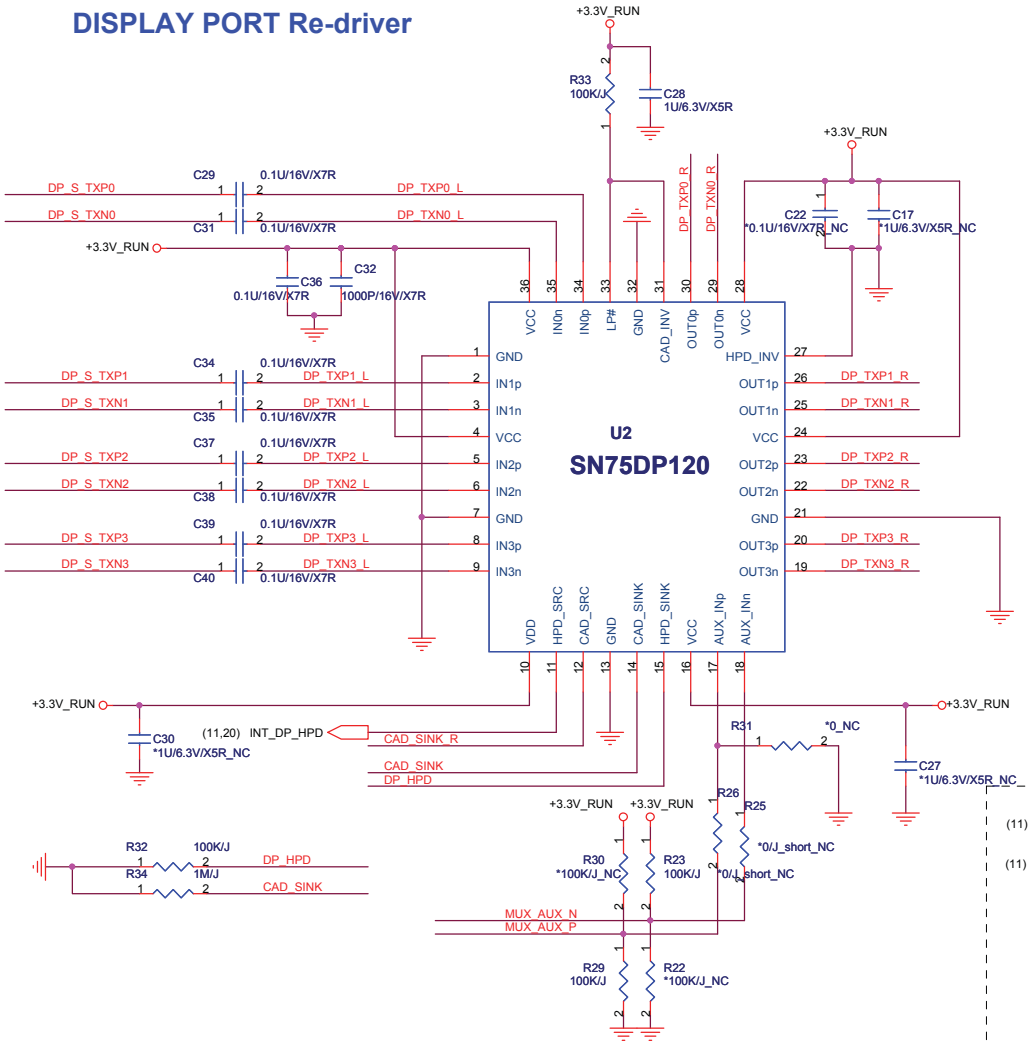
+3.3V_RUN — Q74 MMST3904-7-F — HDMI_HPD — R727 150K — HDMI_DET
(11,41) INT_HDMI_HPD — R728 10K

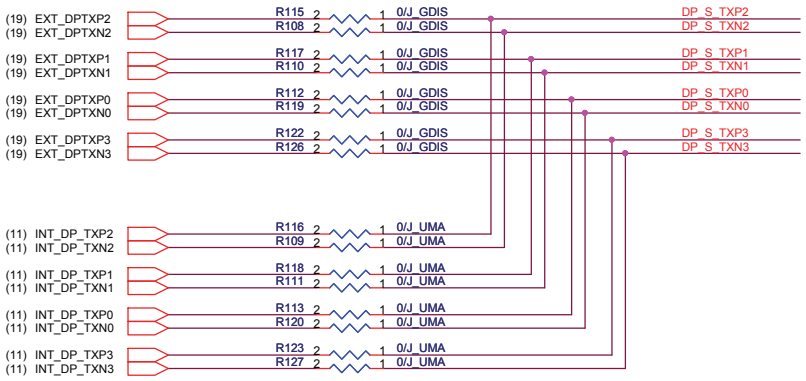
+3.3V_RUN — R709 2.2K/J — R437 2.2K/J
(41) HDMI_SCL_S — HDMI_SCL_S — Q73 FDV301N — HDMI_CLK
+3.3V_RUN
(41) HDMI_SDA_S — HDMI_SDA_S — Q72 FDV301N — HDMI_DAT

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

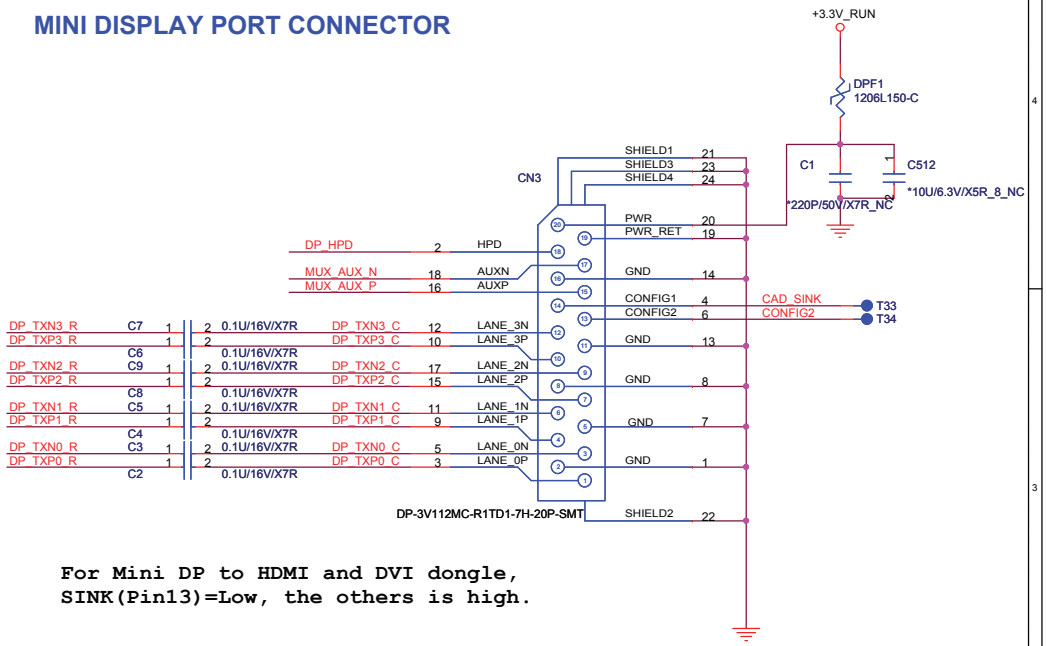
Size	Document Number	Rev
	HDMI CONN	1A
Date: Friday, January 07, 2011	Sheet 25 of 59	

DISPLAY PORT Re-driver

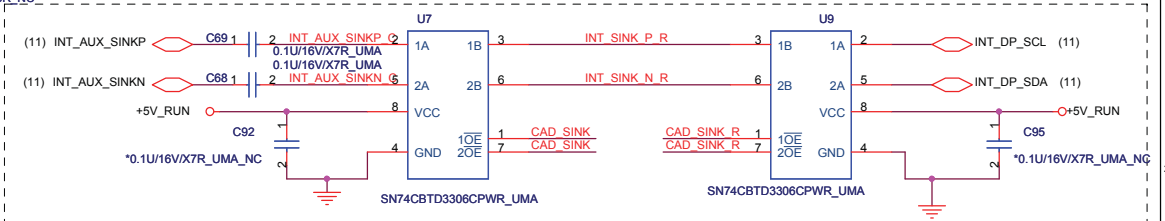


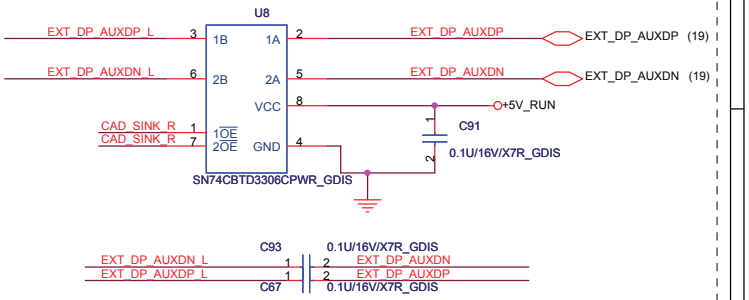


MINI DISPLAY PORT CONNECTOR

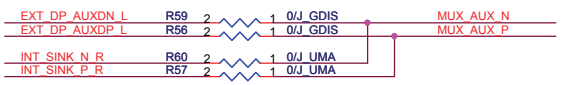


For Mini DP to HDMI and DVI dongle, SINK(Pin13)=Low, the others is high.

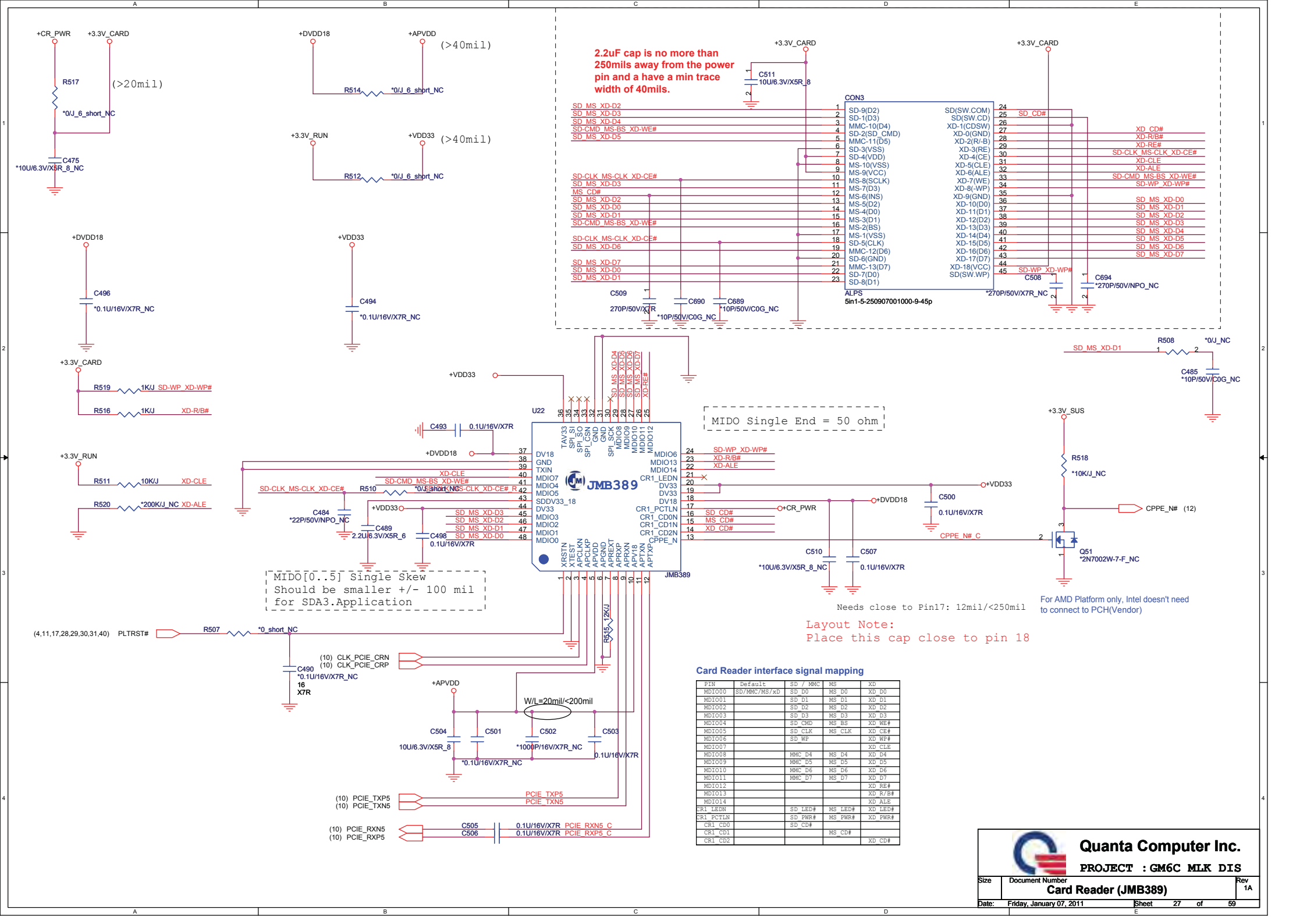




OE	Output
L	A=B
H	Z



Quanta Computer Inc.			
PROJECT : GM6C MLK DIS			
Size	Document Number		Rev
	MINI DP CONN		1A
Date: Friday, January 07, 2011		Sheet 26 of 59	



Card Reader interface signal mapping

PIN	Default	SD / MMC	MS	XD
MDIO00	SD/MMC/MS/xD	SD_D0	MS_D0	XD_D0
MDIO01		SD_D1	MS_D1	XD_D1
MDIO02		SD_D2	MS_D2	XD_D2
MDIO03		SD_D3	MS_D3	XD_D3
MDIO04		SD_CMD	MS_BS	XD_WE#
MDIO05		SD_CLK	MS_CLK	XD_CE#
MDIO06		SD_WP		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_D4	MS_D4	XD_D4
MDIO09		MMC_D5	MS_D5	XD_D5
MDIO10		MMC_D6	MS_D6	XD_D6
MDIO11		MMC_D7	MS_D7	XD_D7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE
CR1_LEDN		SD_LED#	MS_LED#	XD_LED#
CR1_PCTLN		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		
CR1_CD1			MS_CD#	
CR1_CD2				XD_CD#

Quanta Computer Inc.			
PROJECT : GM6C MLK DIS			
Size	Document Number		Rev
	Card Reader (JMB389)		1A
Date: Friday, January 07, 2011	Sheet 27 of 59		

BX1 leakage issue workaround circuit
R96,C104 no stuff,R100 stuff
BX2 will close it.
R96,C104 stuff,R100 no stuff

Layout Note: Place these caps close to ITE8502

Layout Note: Place PC169 close to ITE8502

IT8518E/CX

U11

LPC
CIR
UART port
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
GPIO
SM BUS
PS/2
PWM
WAKE UP
A/D D/A
CLOCK
BAT

Thermal, MMB

For Crystal-Free

prochot pin level shift

Board ID Straps

Config_0	Config_1	GM6/GM6C
0	0	UMA
0	1	Optimum-GE
1	0	Studio Discrete
1	1	Optimum-GS

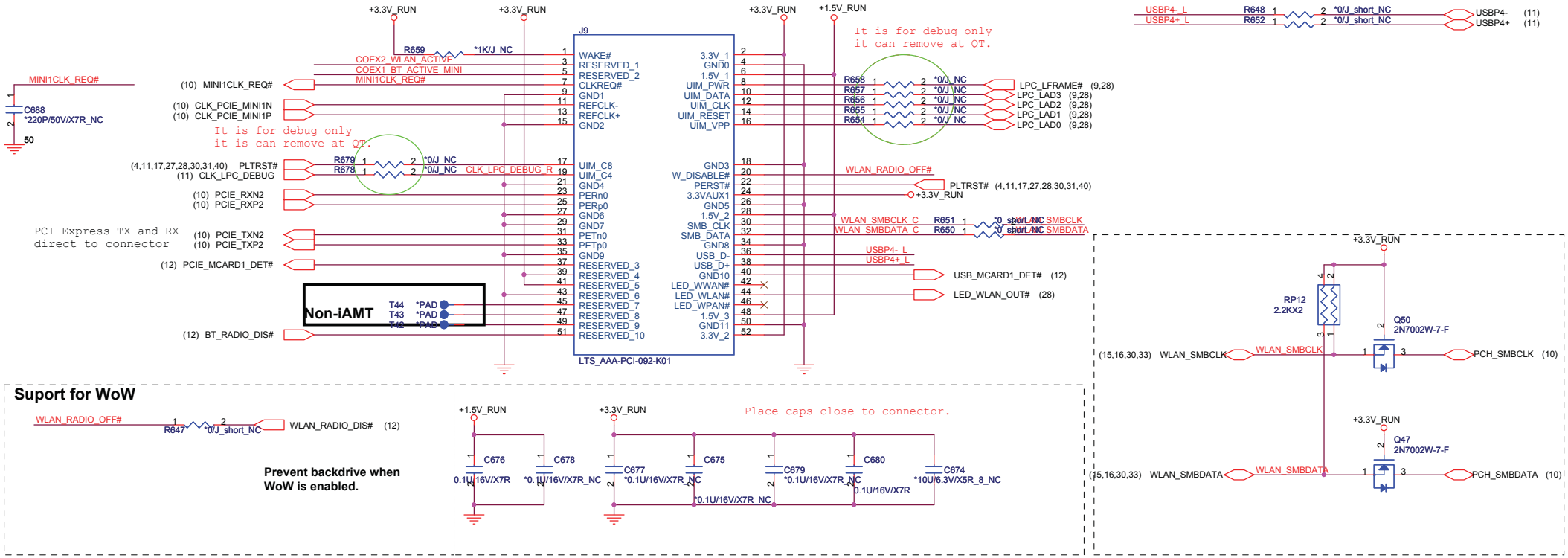
USB_BACK_EN#	BID1	GM6/GM6C
0	0	SSI (X00)
0	1	PT (X01)
1	0	ST (X02)
1	1	QT (A00)
0	0	(A01)

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

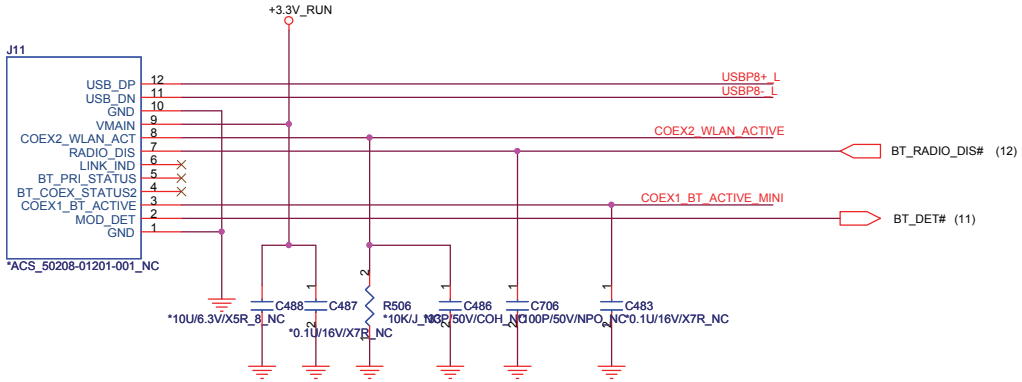
Size	Document Number	Rev
	SIO (ITE8518)	1A

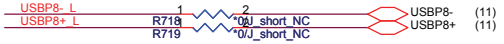
Date: Friday, January 07, 2011 Sheet 28 of 59

MiniCard WLAN connector



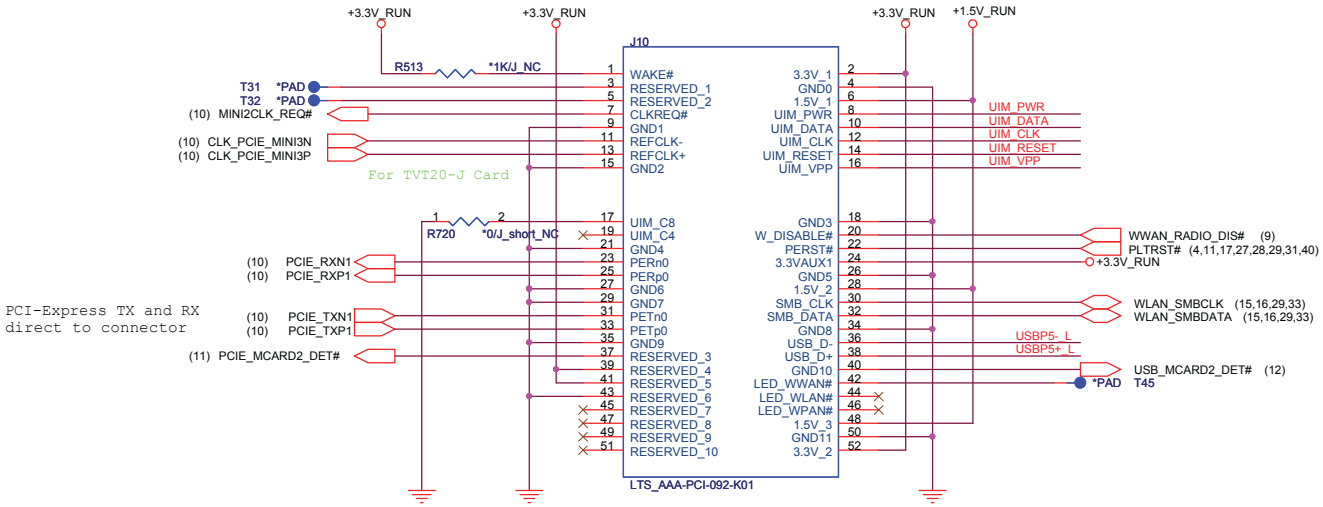
Support Dell BT375 (Little Stone) module (XPS) W TO B

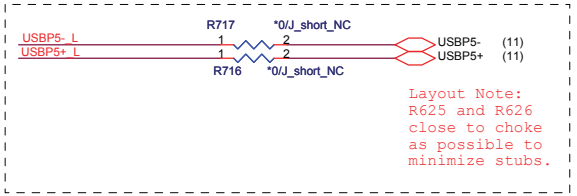


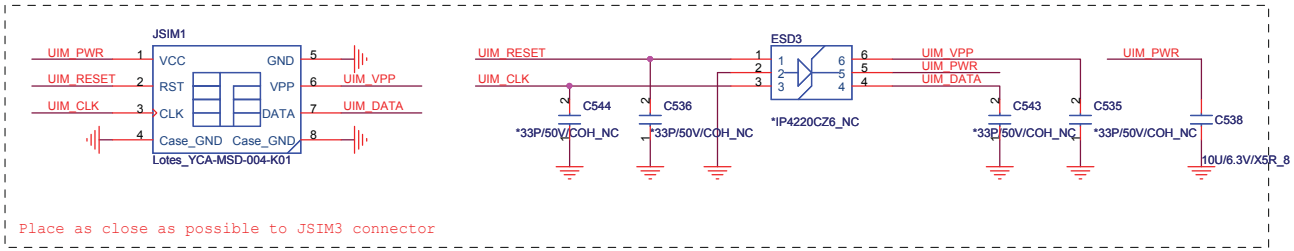


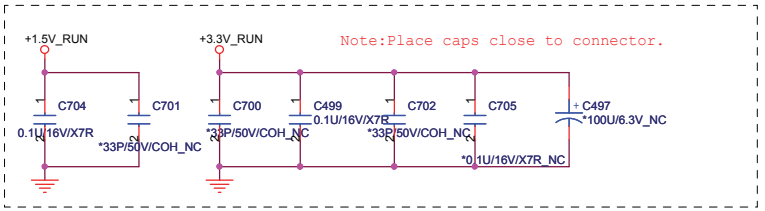
Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: MINI-Card (WLAN/WPAN)	Rev 1A
Date: Friday, January 07, 2011	Sheet 29 of 59	

MiniCard WWAN connector







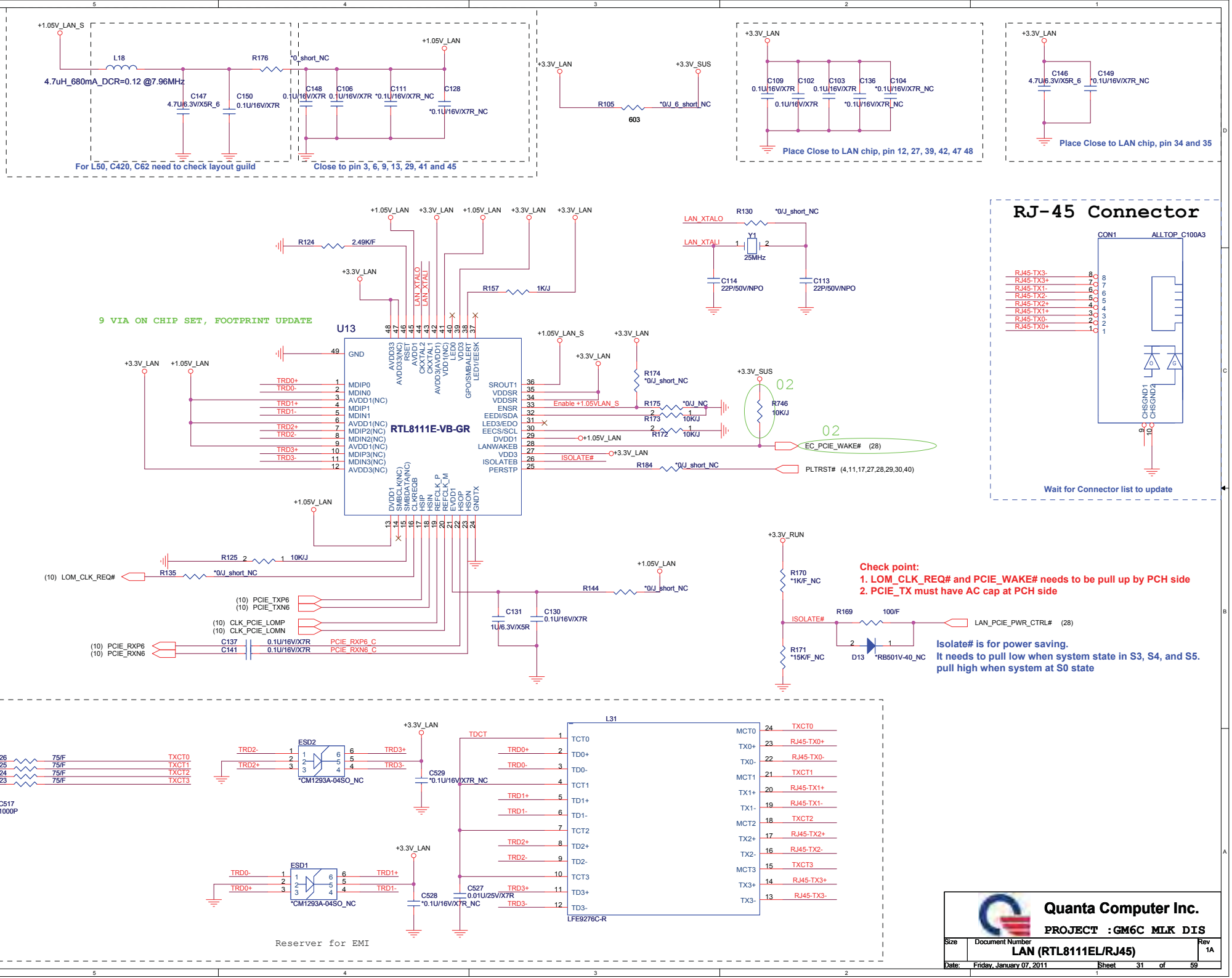


Quanta Computer Inc.

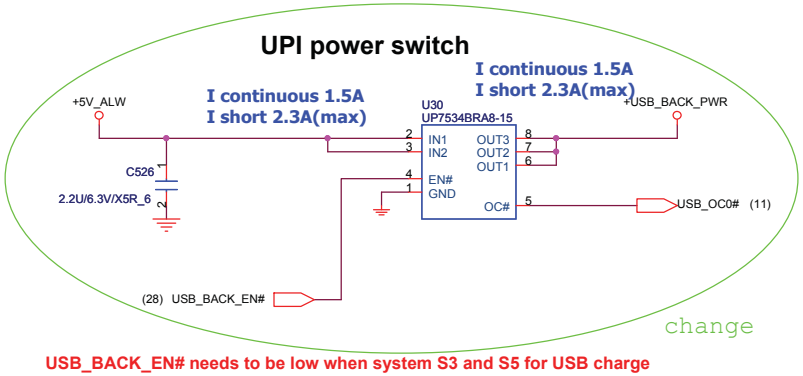
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	MINI-Card (WWAN)	1A

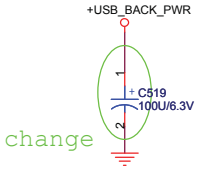
Date: Friday, January 07, 2011 Sheet 30 of 59


+1.05V_LAN_S
L18
4.7uH_680mA_DCR=0.12 @7.96MHz
R176
*0_short_NC
+1.05V_LAN
C147
4.7U/6.3V/X5R_6
C150
0.1U/16V/X7R
C148
0.1U/16V/X7R
C106
0.1U/16V/X7R
C111
*0.1U/16V/X7R_NC
C128
*0.1U/16V/X7R_NC
For L50, C420, C62 need to check layout guild
Close to pin 3, 6, 9, 13, 29, 41 and 45
+3.3V_LAN
R105
603
+3.3V_SUS
*0/J_6_short_NC
C109
0.1U/16V/X7R
C102
0.1U/16V/X7R
C103
0.1U/16V/X7R
C136
0.1U/16V/X7R
C104
*0.1U/16V/X7R_NC
Place Close to LAN chip, pin 12, 27, 39, 42, 47 48
C146
4.7U/6.3V/X5R_6
C149
*0.1U/16V/X7R_NC
Place Close to LAN chip, pin 34 and 35
9 VIA ON CHIP SET, FOOTPRINT UPDATE
U13
RTL8111E-VB-GR
GND
MDIP0
MDIN0
AVDD1(NC)
MDIP1
MDIN1
AVDD1(NC)
MDIP2(NC)
MDIN2(NC)
AVDD1(NC)
MDIP3(NC)
MDIN3(NC)
AVDD3(NC)
AVDD33
AVDD33(NC)
RSET
AVDD1
CKXTAL2
CKXTAL1
AVDD3(AVDD1)
VDD1(NC)
LED0
LED3
GPIO/SMBALERT
LED1/EESK
SROUT1
VDDSR
VDDSR
ENSR
EEDI/SDA
LED3/EDO
EECS/SCL
DVDD1
LANWAKEB
VDD3
ISOLATEB
PERSTP
DVDD1
SMBCLK(NC)
SMBDATA(NC)
CLKREQB
HSIP
HSIN
REFCLK_P
REFCLK_M
EVDD1
HSOP
HSON
GNDTX
R124
2.49K/F
R157
1K/J
LAN_XTALO
LAN_XTALI
R130
*0/J_short_NC
Y1
25MHz
C114
22P/50V/NPO
C113
22P/50V/NPO
Enable +1.05VLAN_S
ISOLATE#
R174
*0/J_short_NC
R175
*0/J_NC
R173
10K/J
R172
10K/J
R746
10K/J
02
EC_PCIE_WAKE# (28)
PLTRST# (4,11,17,27,28,29,30,40)
R184
*0/J_short_NC
RJ-45 Connector
CON1
ALLTOP_C100A3
RJ45-TX3-
RJ45-TX3+
RJ45-TX1-
RJ45-TX2-
RJ45-TX2+
RJ45-TX1+
RJ45-TX0-
RJ45-TX0+
CHSGND1
CHSGND2
Wait for Connector list to update
(10) LOM_CLK_REQ#
R125
10K/J
R135
*0/J_short_NC
(10) PCIE_TXP6
(10) PCIE_TXN6
(10) CLK_PCIE_LOMP
(10) CLK_PCIE_LOMN
(10) PCIE_RXP6
(10) PCIE_RXN6
C137
0.1U/16V/X7R
C141
0.1U/16V/X7R
PCIE_RXP6_C
PCIE_RXN6_C
C131
1U/6.3V/X5R
C130
0.1U/16V/X7R
R144
*0/J_short_NC
+3.3V_RUN
R170
*1K/F_NC
R171
*15K/F_NC
ISOLATE#
R169
100/F
LAN_PCIE_PWR_CTRL# (28)
D13
*RB501V-40_NC
Check point:
1. LOM_CLK_REQ# and PCIE_WAKE# needs to be pull up by PCH side
2. PCIE_TX must have AC cap at PCH side
Isolate# is for power saving.
It needs to pull low when system state in S3, S4, and S5.
pull high when system at S0 state
R526
R525
R524
R523
75/F
TXCT0
TXCT1
TXCT2
TXCT3
C517
1000P
ESD2
*CM1293A-04SO_NC
TRD2-
TRD2+
TRD3+
TRD3-
C529
*0.1U/16V/X7R_NC
ESD1
*CM1293A-04SO_NC
TRD0-
TRD0+
TRD1+
TRD1-
C528
*0.1U/16V/X7R_NC
C527
0.01U/25V/X7R
L31
LFE9276C-R
TDCT
TCT0
TD0+
TD0-
TCT1
TD1+
TD1-
TCT2
TD2+
TD2-
TCT3
TD3+
TD3-
MCT0
TX0+
TX0-
MCT1
TX1+
TX1-
MCT2
TX2+
TX2-
MCT3
TX3+
TX3-
TXCT0
RJ45-TX0+
RJ45-TX0-
TXCT1
RJ45-TX1+
RJ45-TX1-
TXCT2
RJ45-TX2+
RJ45-TX2-
TXCT3
RJ45-TX3+
RJ45-TX3-
Reserver for EMI
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size
Document Number
LAN (RTL8111EL/RJ45)
Rev
1A
Date: Friday, January 07, 2011
Sheet 31 of 59

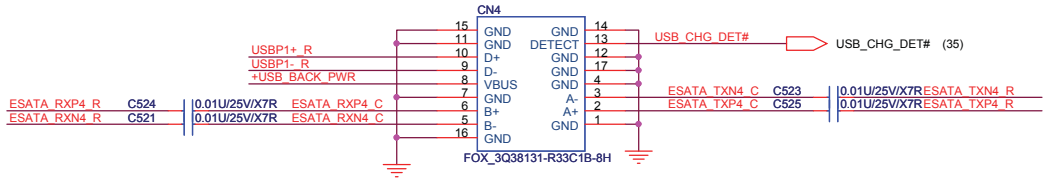
ESATA + USB Conn + Power Share

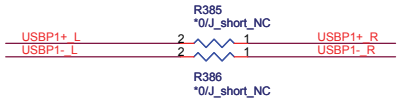


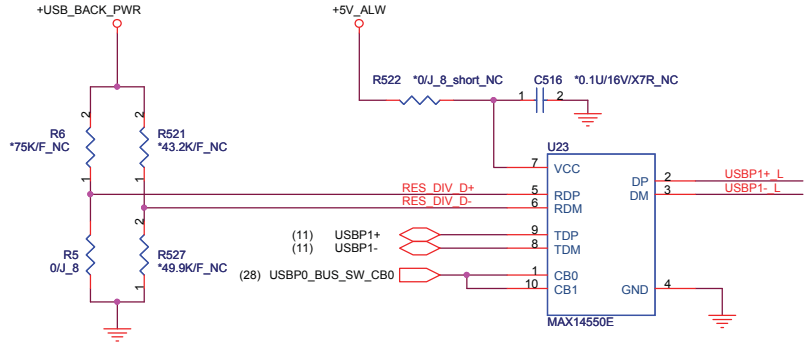
USB_BACK_EN# needs to be low when system S3 and S5 for USB charge



This pin connects to 3VALW ON POWER LOGIC







EC needs to drive CB0/CB1 pins to low when system S3/S5 and dirve high when system S0.

U49 PN and Footprint needs to double check

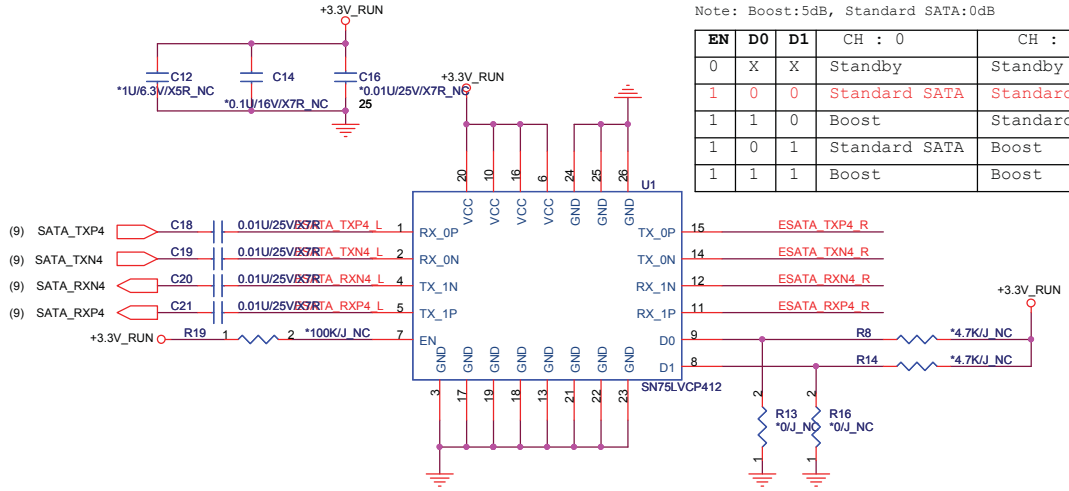
R15 needs to be 49.9K_F if we use external resisters.

CB0	CB1	Function
0	0	Auto Detection active
1	1	USB Function only

(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB



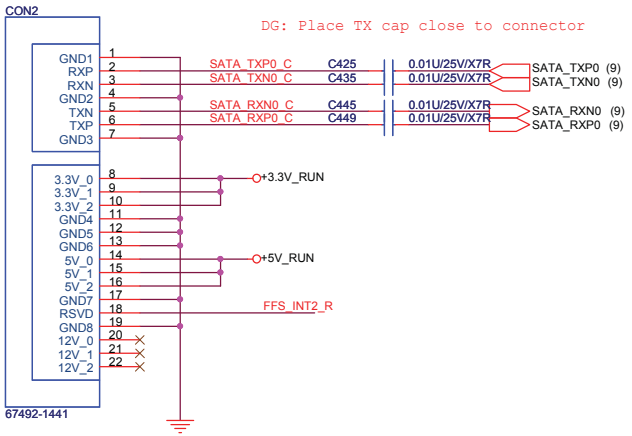
Note: Boost:5dB, Standard SATA:0dB

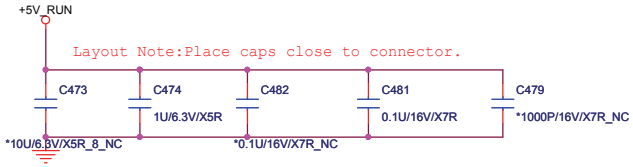
EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

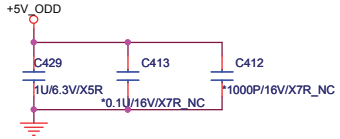
Size	Document Number	Rev
	Righ PUSB/ESATA	1A
Date: Friday, January 07, 2011	Sheet 32 of 59	

SATA Connector.

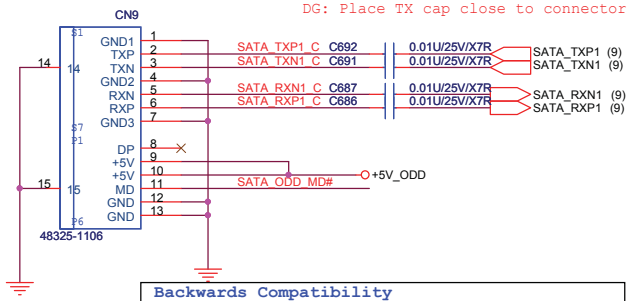




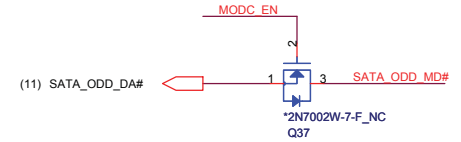
ODD Connector



Layout Note:Place caps close to connector.

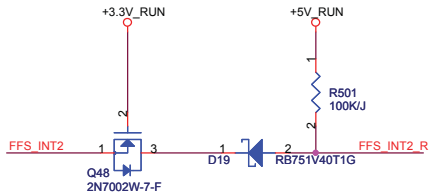


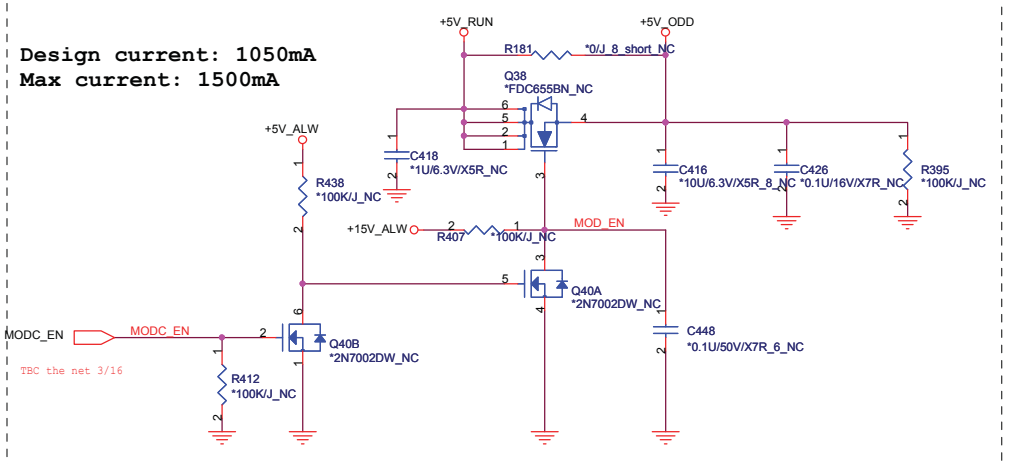
Backwards Compatibility



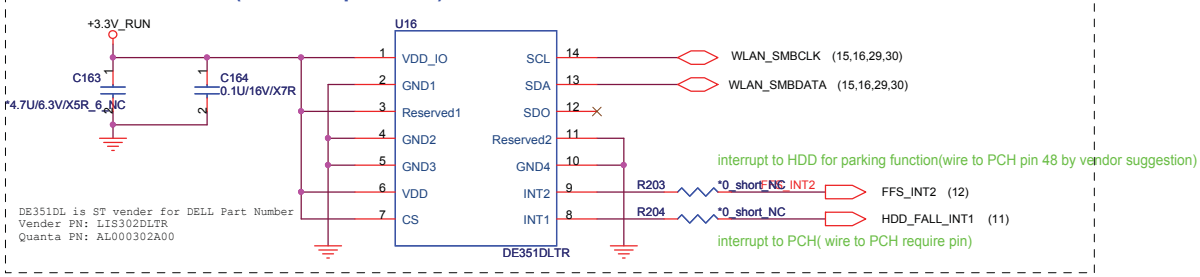
Drive powered on, MD# is High
Drive powered off, MD# is Low

Because the drive does not support ZPODD, the driver never powers off the power FET and never connects the MD/DA pin to the drive





3-axis Fall Sensor (HDD data protector)



Quanta Computer Inc.

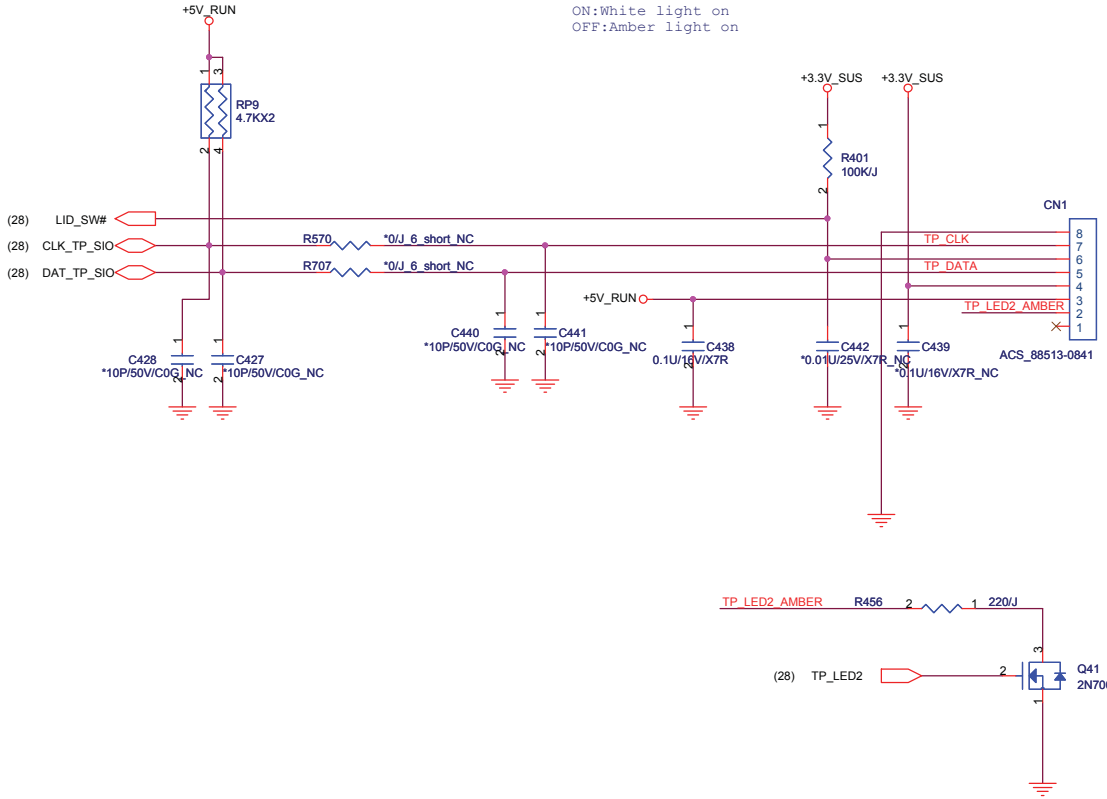
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	SATA (HDD&ODD)	1A

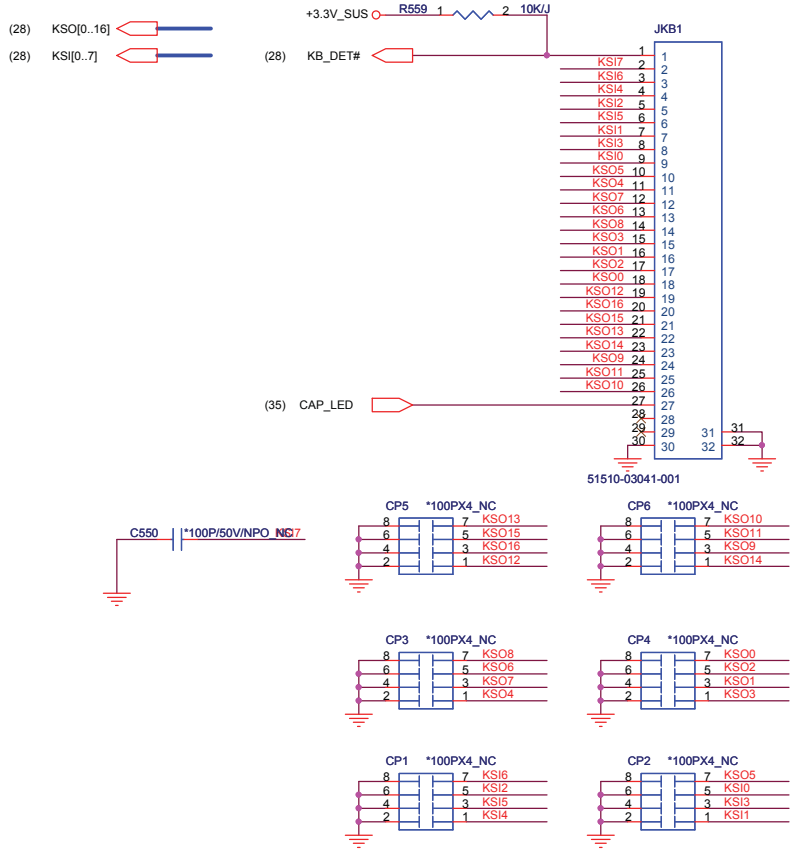
Date: Friday, January 07, 2011 Sheet 33 of 59

Touch Pad

ON:White light on
OFF:Amber light on



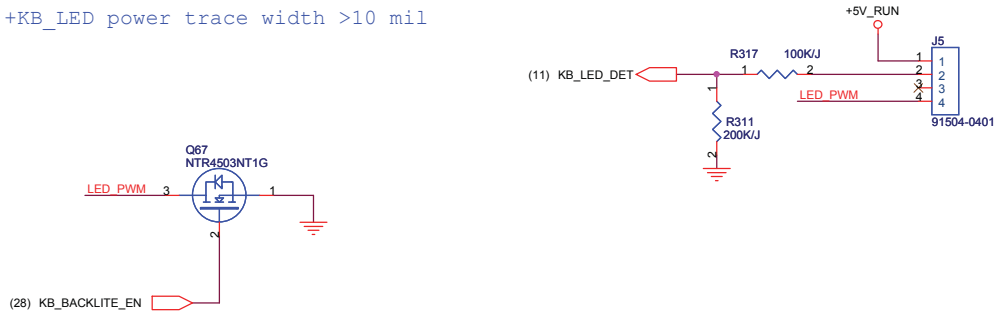
KEYBOARD CONNECTOR



Layout Note: 100P CAPS CLOSE TO JKB3

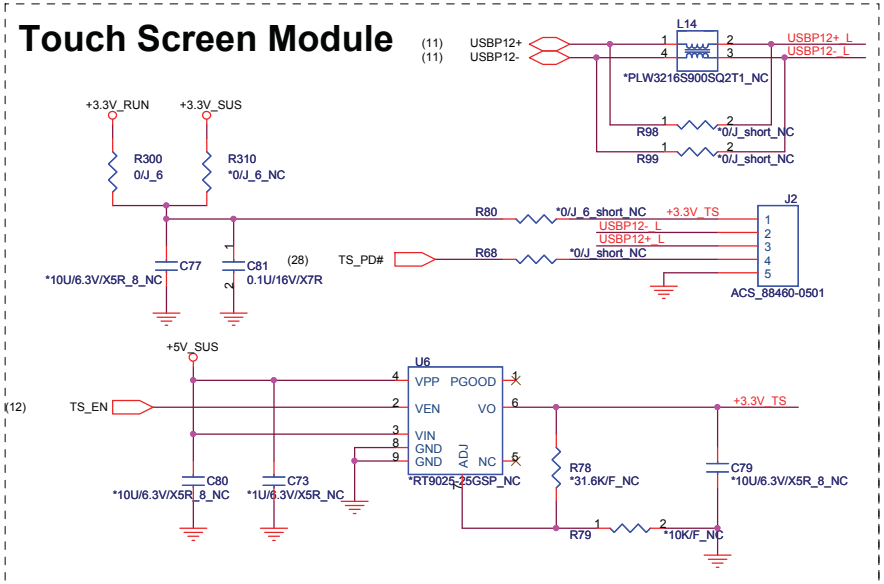
Key board illumination

+KB_LED power trace width >10 mil

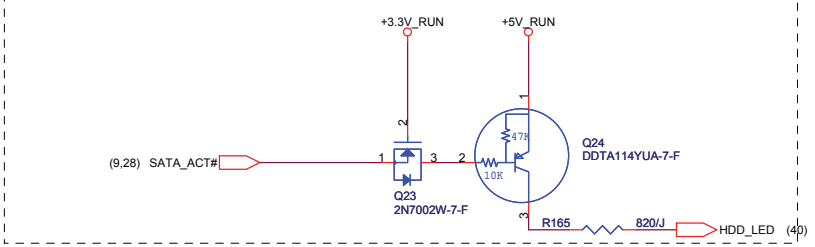


Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: TP/KB	Rev: 1A
Date: Friday, January 07, 2011	Sheet 34 of 59	

Touch Screen Module

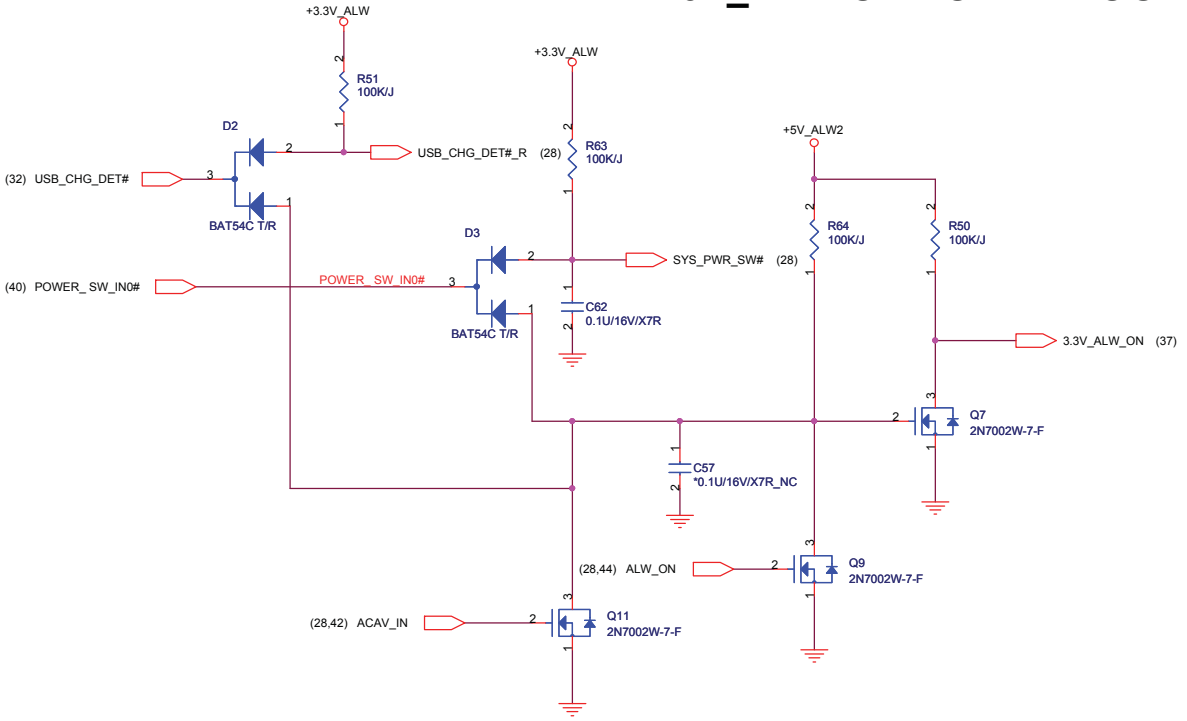


HDD activity LED.

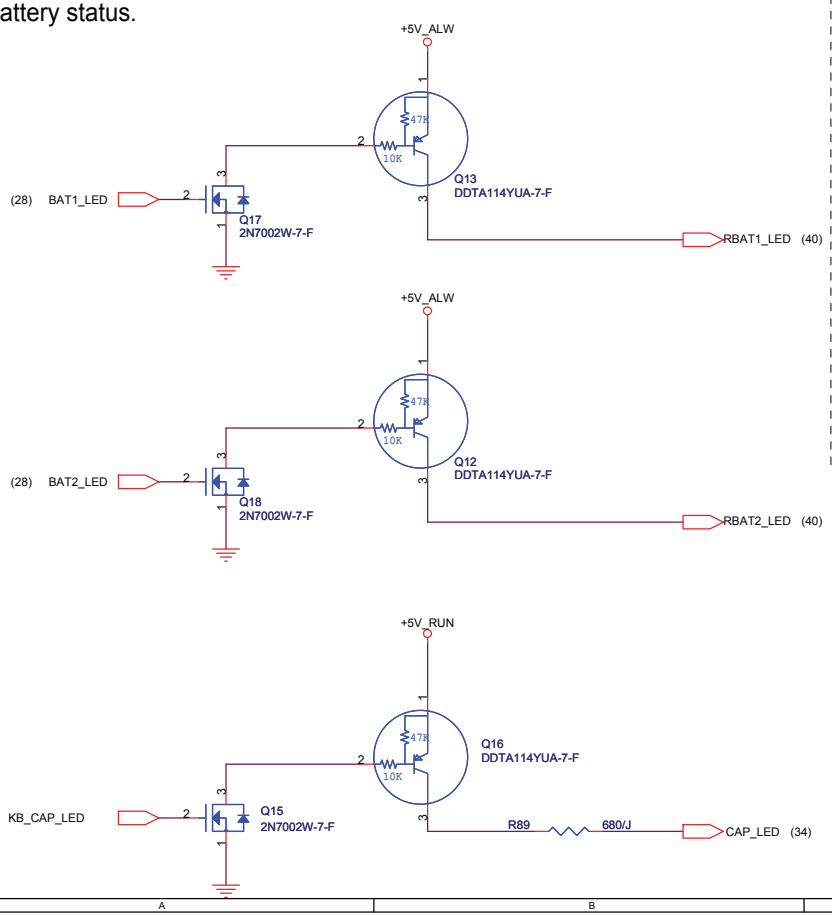


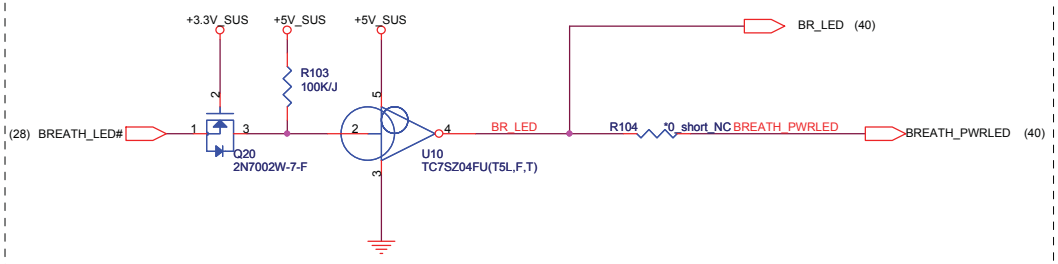
Power button for Engineer

3V_ALW ON POWER LOGIC



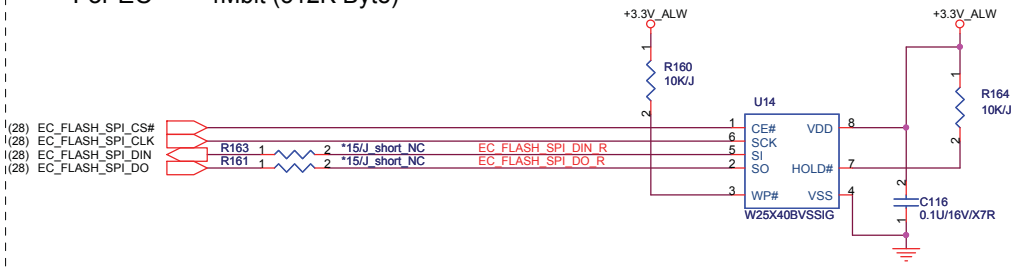
Battery status.



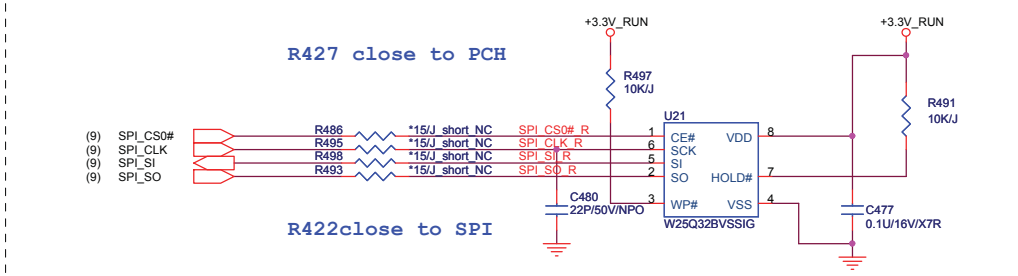


Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: SWITCH/LED/T-Screen	Rev: 1A
Date: Friday, January 07, 2011	Sheet 35 of 59	

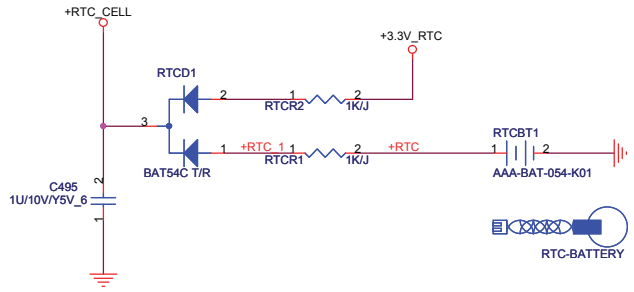
For EC 4Mbit (512K Byte)



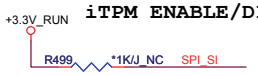
For PCH 32Mbit (4M Byte)



RTC BATTERY

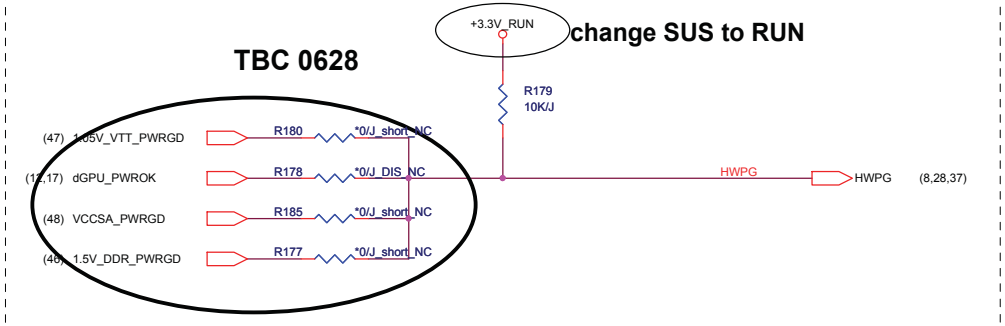


iTPM ENABLE/DISABLE

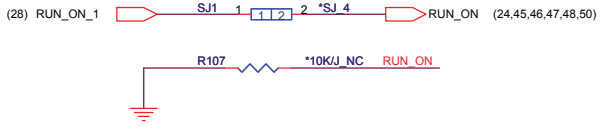


TPM Function	R428
Enable	Mount
Disable	NC (Default)

RESET CIRCUIT



delet VTT_POWERGOOD(07/12)

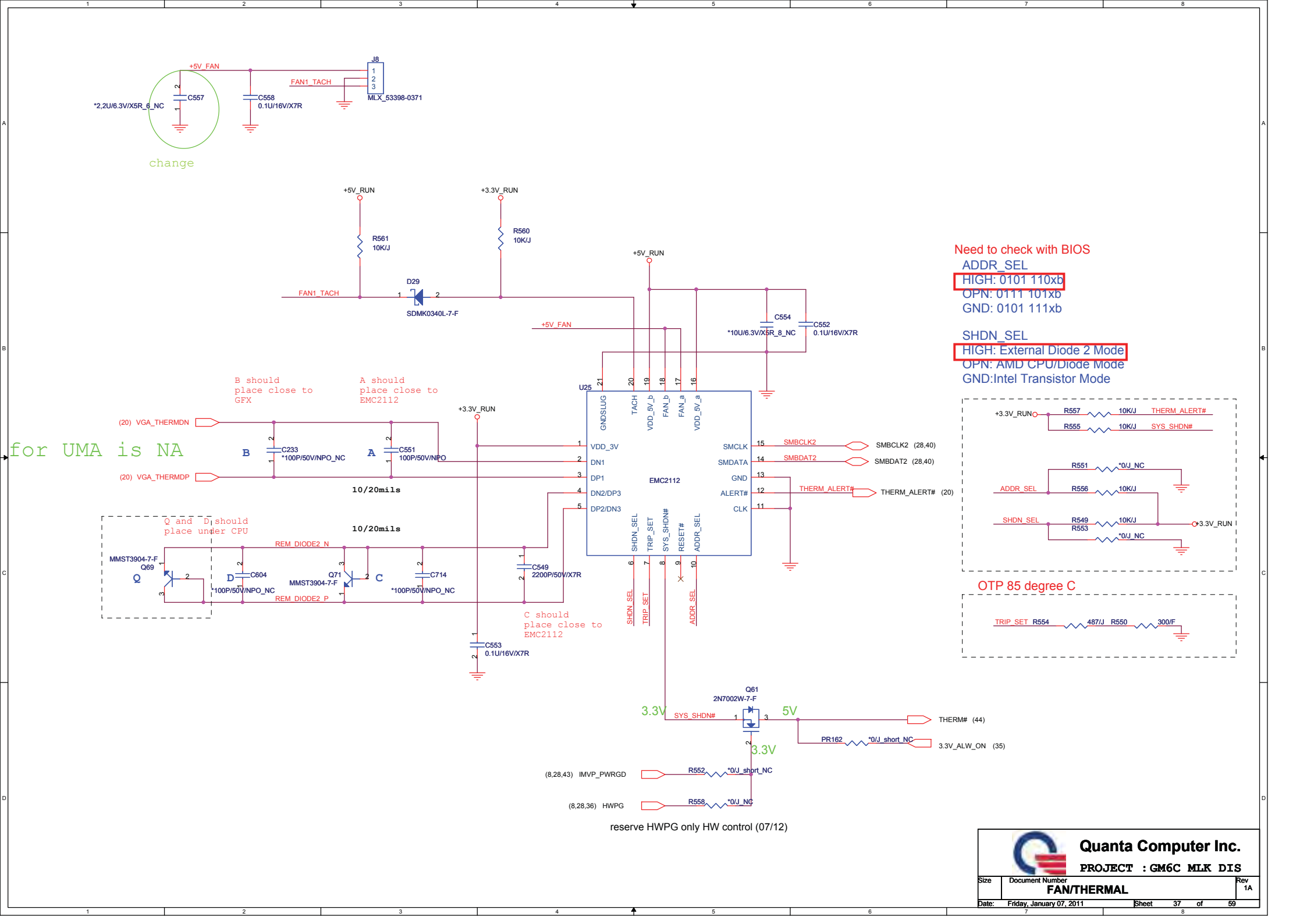


Quanta Computer Inc.

PROJECT : GM6C MLK DIS

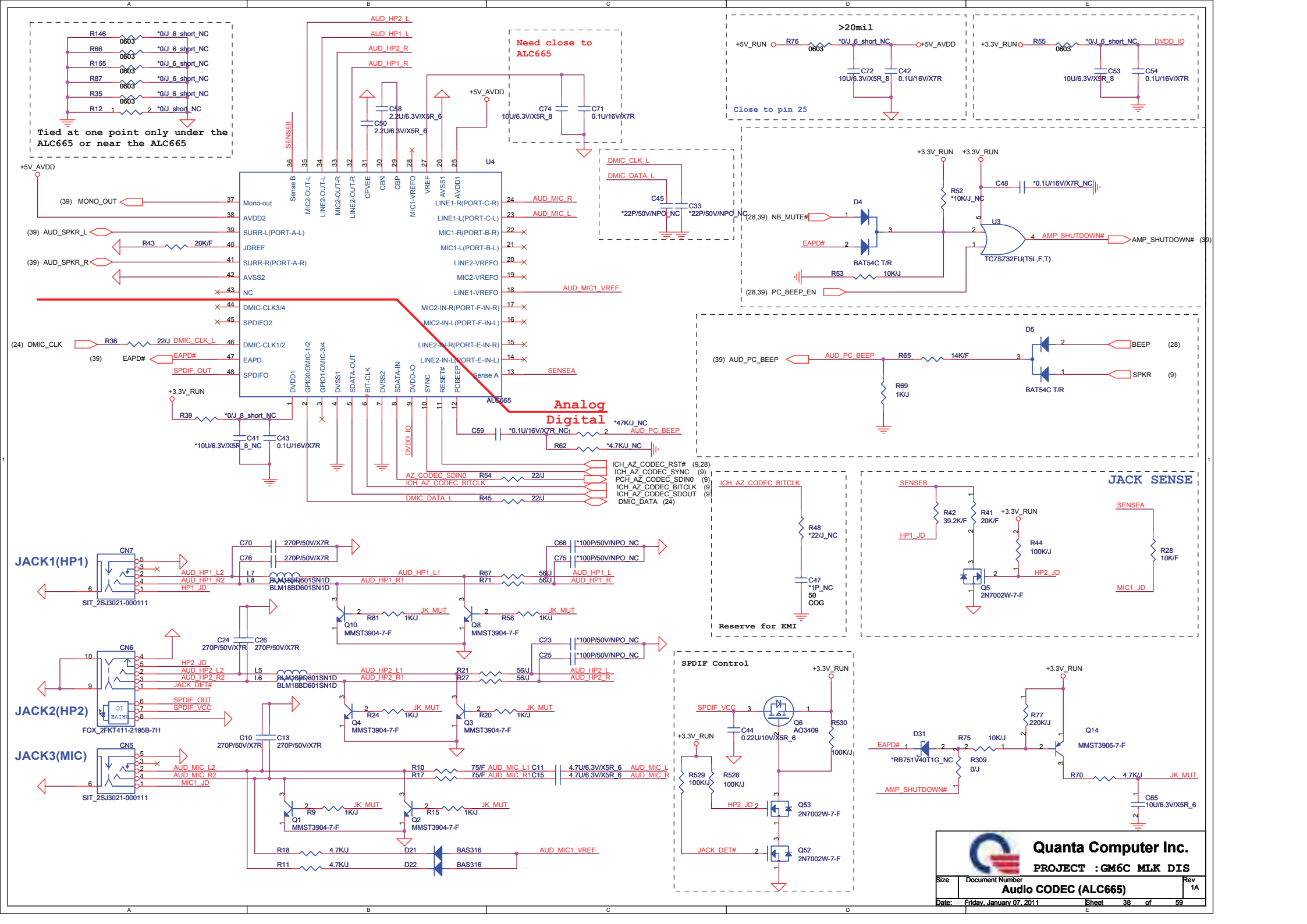
Size	Document Number	Rev
	FLASH/RTC/RESET CIRCUIT	1A

Date: Friday, January 07, 2011 Sheet 36 of 59

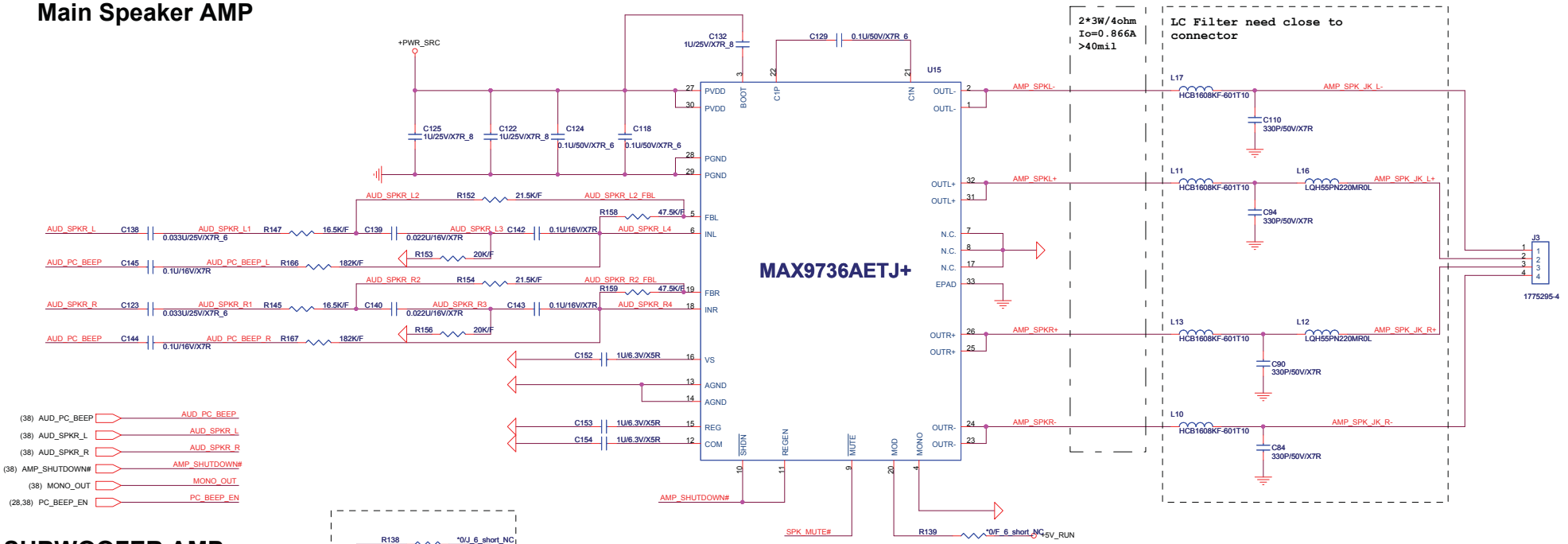


reserve HWPG only HW control (07/12)

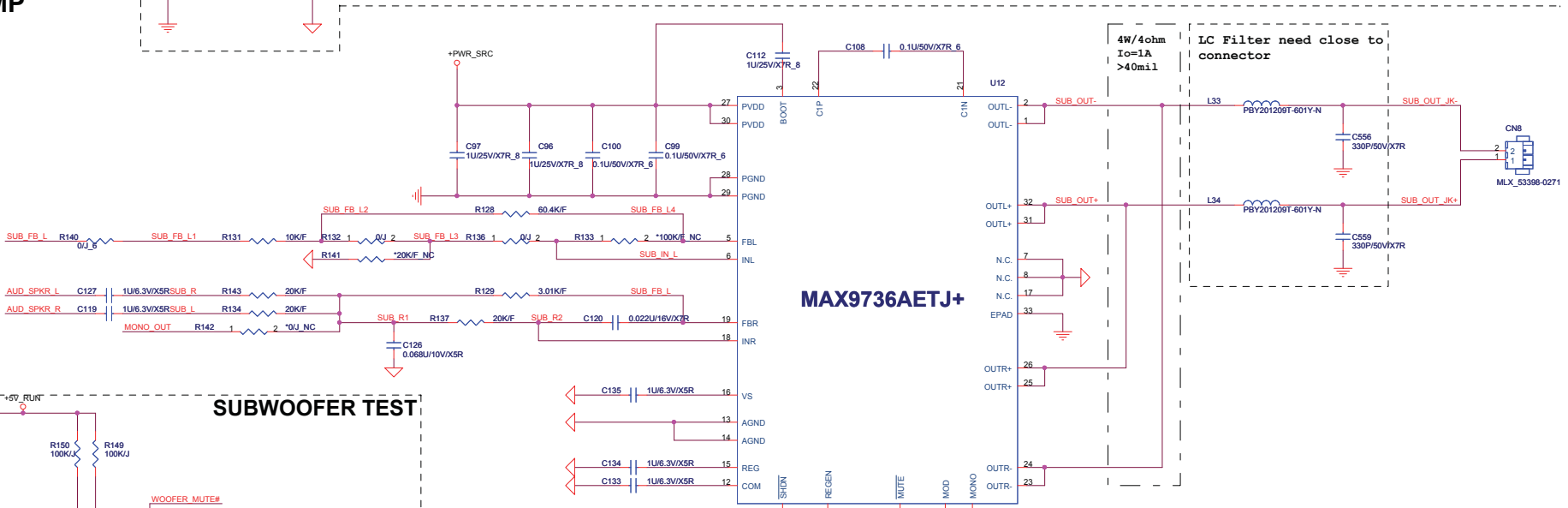
Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: FAN/THERMAL	Rev: 1A
Date: Friday, January 07, 2011	Sheet 37 of 59	


Tied at one point only under the ALC665 or near the ALC665
Need close to ALC665
>20mil
Close to pin 25
U4
ALC665
Analog
Digital
JACK1(HP1)
JACK2(HP2)
JACK3(MIC)
JACK SENSE
SPDIF Control
Reserve for EMI
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Audio CODEC (ALC665)
Date: Friday, January 07, 2011
Sheet 38 of 59

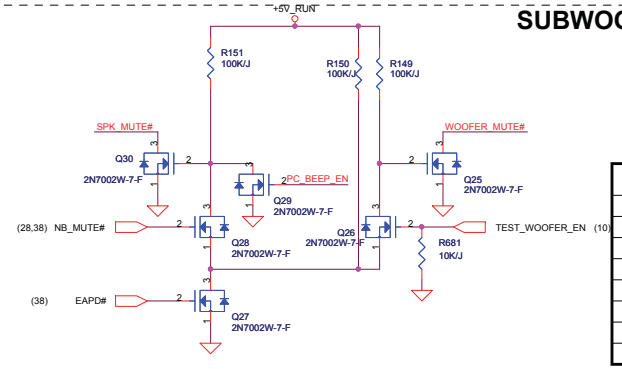
Main Speaker AMP



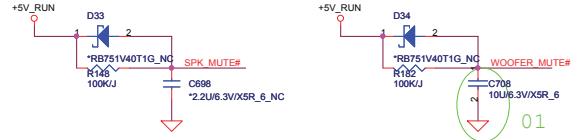
SUBWOOFER AMP



SUBWOOFER TEST



EAPD#	NB_MUTE#	TEST_WOOFER_EN	SPK_MUTE#	WOOFER_MUTE#
0	0	0	L	L
0	0	1	L	L
0	1	0	L	L
0	1	1	L	L
1	0	0	L	L
1	0	1	L(Disable SPK)	H(Test Woofer)
1	1	0	H(Test SPK)	L(Disable Woofer)
1	1	1	H	H

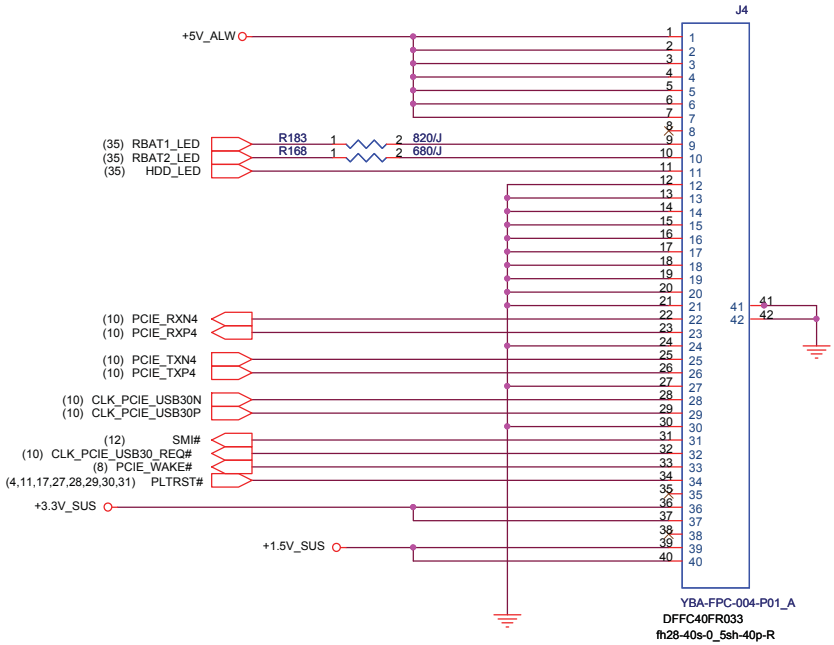


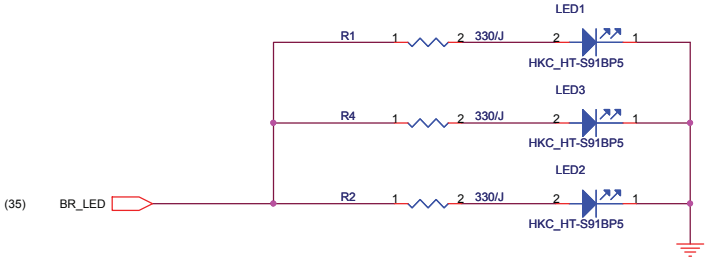
Quanta Computer Inc.

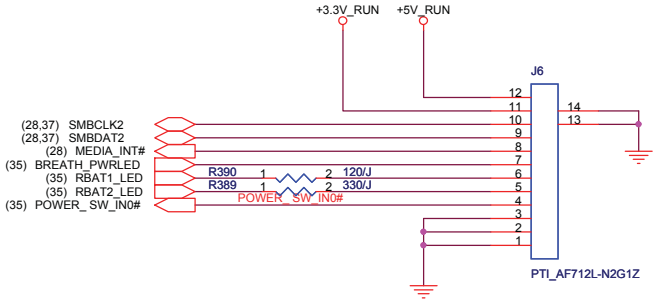
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Audio AMP (MAX9736A)	1A
Date: Friday, January 07, 2011	Sheet 39 of 59	

01





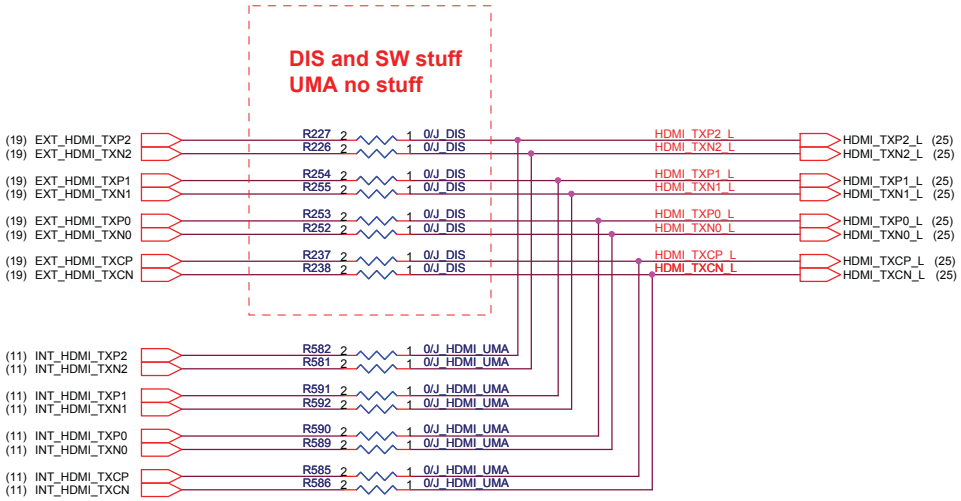


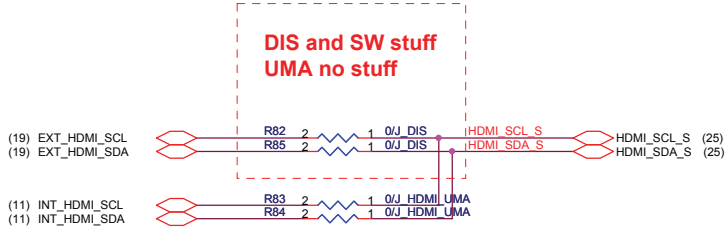
Quanta Computer Inc.

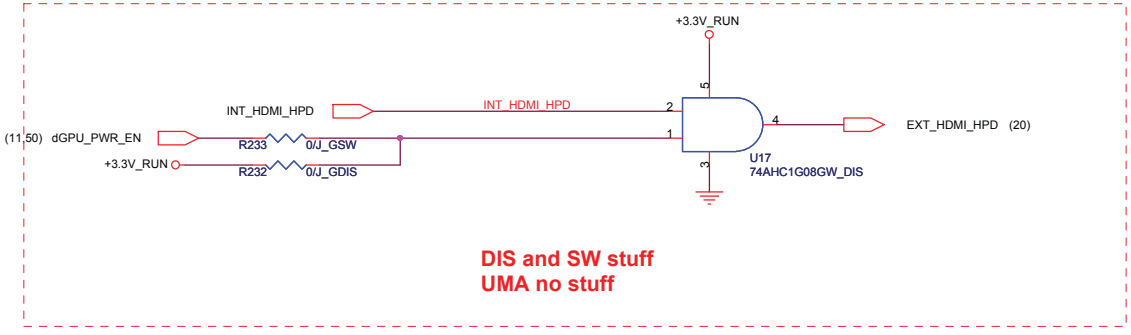
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Left USB/MMB CONN	1A
Date: Friday, January 07, 2011	Sheet 40 of 59	

HDMI Switch





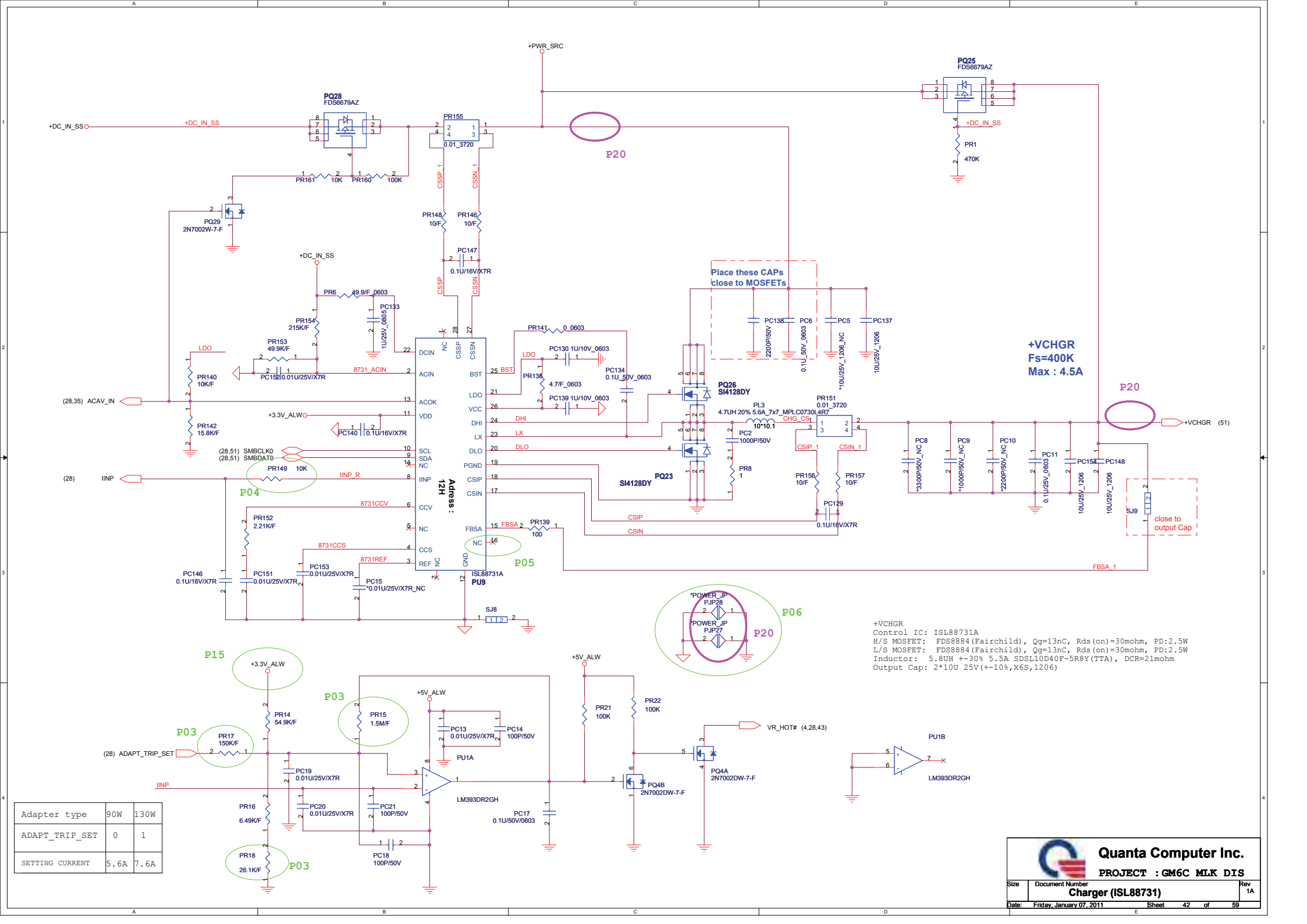


Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	BLANK	1A

Date: Friday, January 07, 2011 Sheet 41 of 59



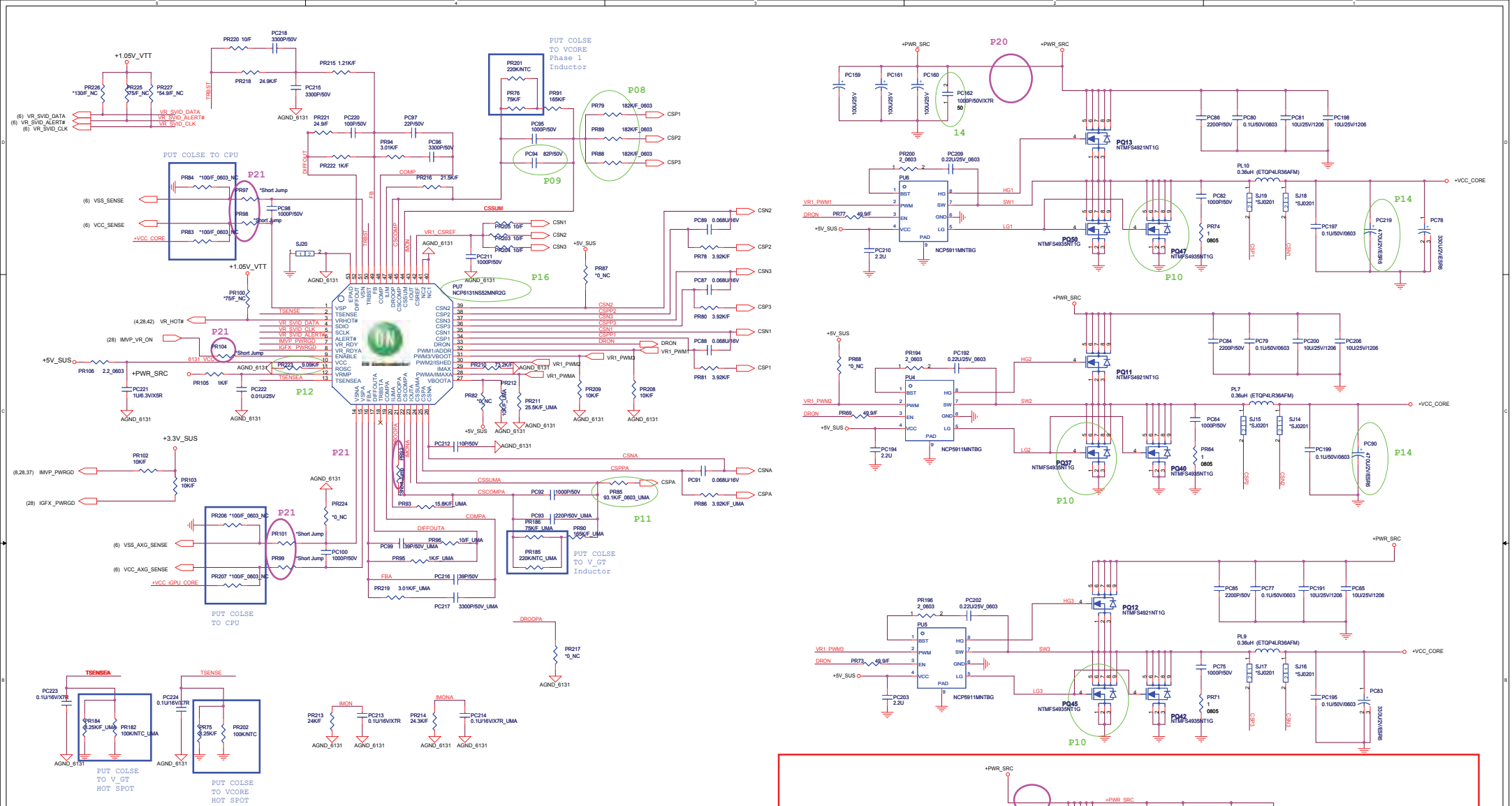
Adapter type	90W	130W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	5.6A	7.6A

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Charger (ISL88731)	1A

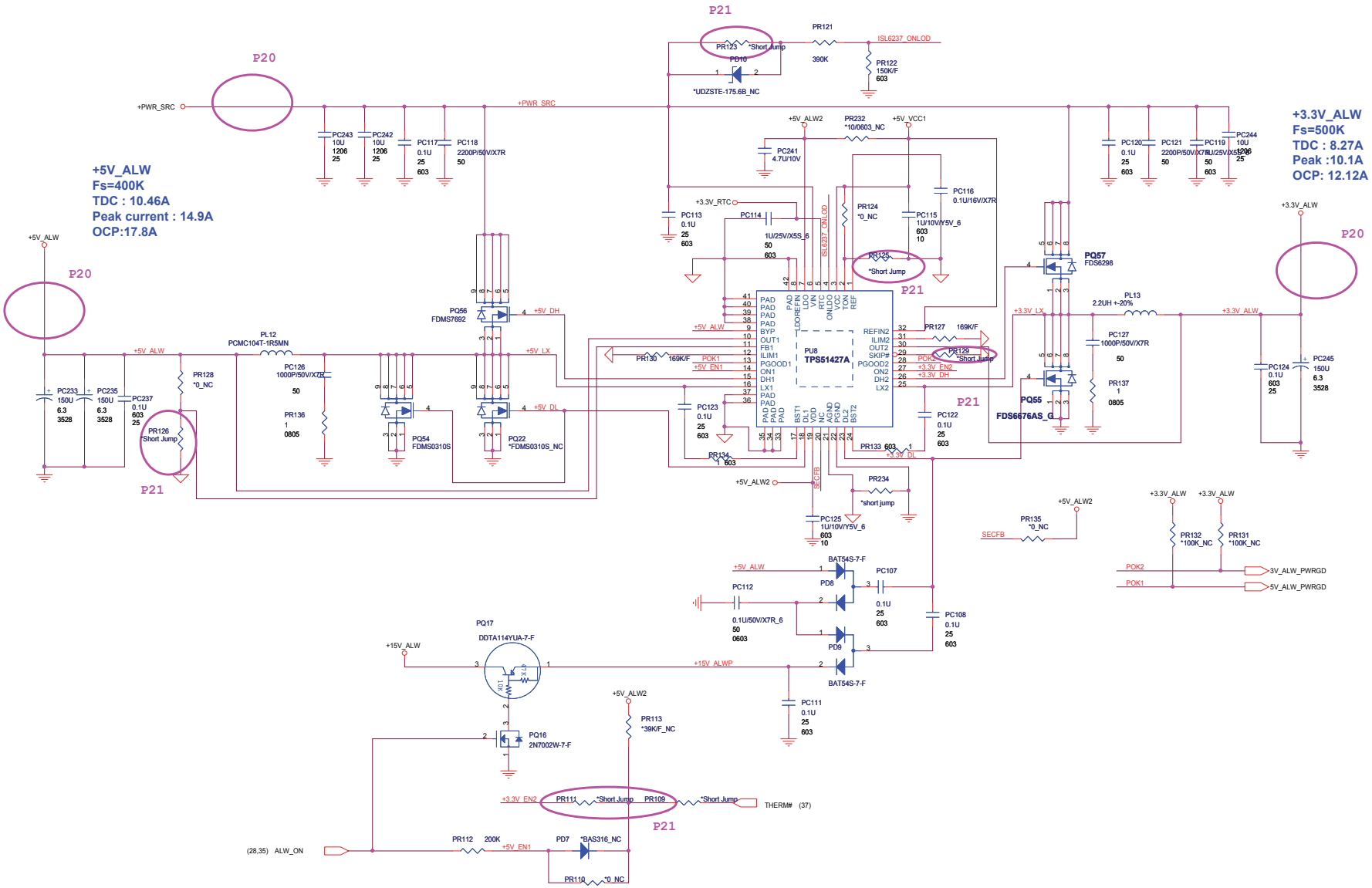
Date: Friday, January 07, 2011 Sheet 42 of 59



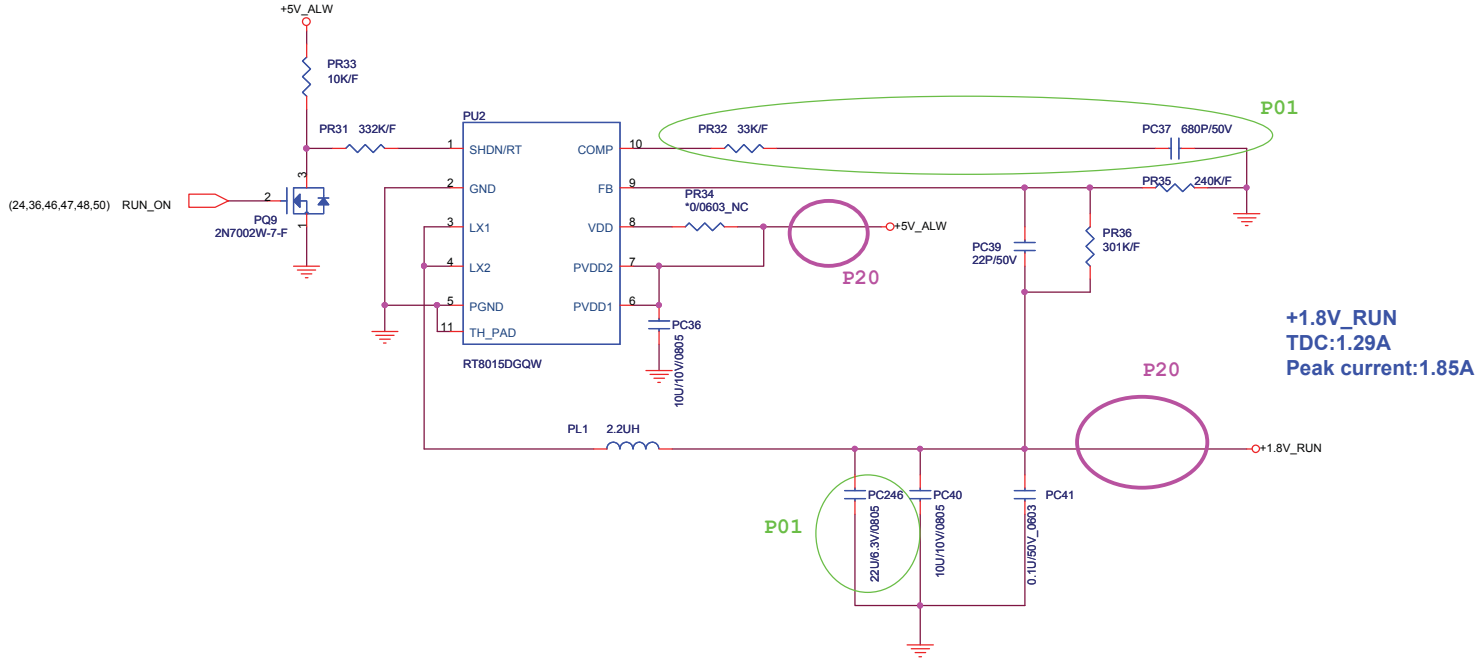
Reference	Discrete	UMA	Optimus
PR82	0(CS00002JB38)	NC	NC
PC91	0(CS00002JB38)	0.068U/16V(CH3683K1B09)	0.068U/16V(CH3683K1B09)
PC92	0(CS00002JB38)	1000P/50V(CH21006JB10)	1000P/50V(CH21006JB10)
PC212	0(CS00002JB38)	10P/50V(CH01006JB08)	10P/50V(CH01006JB08)
PR217	0(CS00002JB38)	NC	NC
PC216	0(CS00002JB38)	39P/50V(CH03906JB06)	39P/50V(CH03906JB06)
PC100	0(CS00002JB38)	1000P/50V(CH21006JB10)	1000P/50V(CH21006JB10)
PR224	0(CS00002JB38)	NC	NC
PR214	0(CS00002JB38)	24.3K/F(CS32432FB19)	24.3K/F(CS32432FB19)
PC223	0(CS00002JB38)	0.1U/10V(CH4102K1B03)	0.1U/10V(CH4102K1B03)

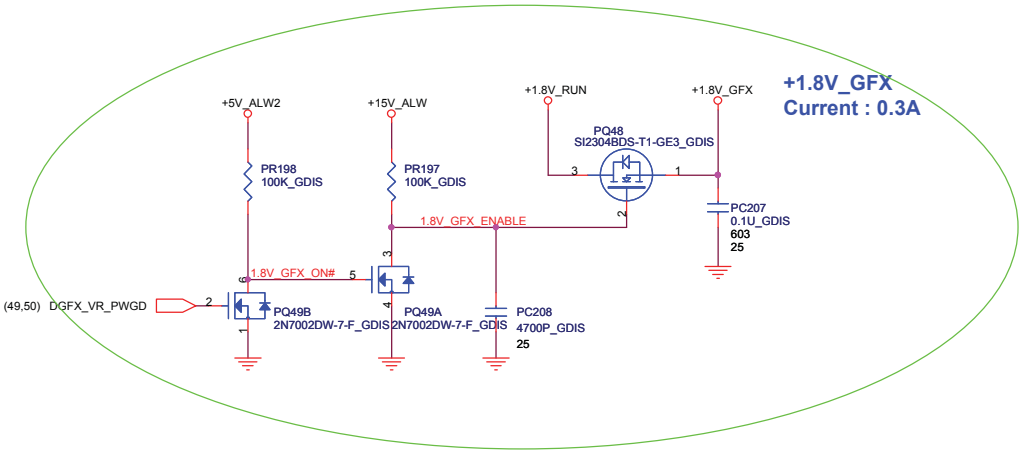
	UMA	Optimus
PC180, C612	470uF CH747RM8800	330uF CH733RM8831

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: CPU_VCORE (NCP6131S) | Rev: 1A
Date: Friday, January 07, 2011 | Sheet 43 of 59



Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: 3.3V_ALW / 5V_ALW(TPS51427A)	Rev: 1A
Date: Friday, January 07, 2011	Sheet 44 of 59	



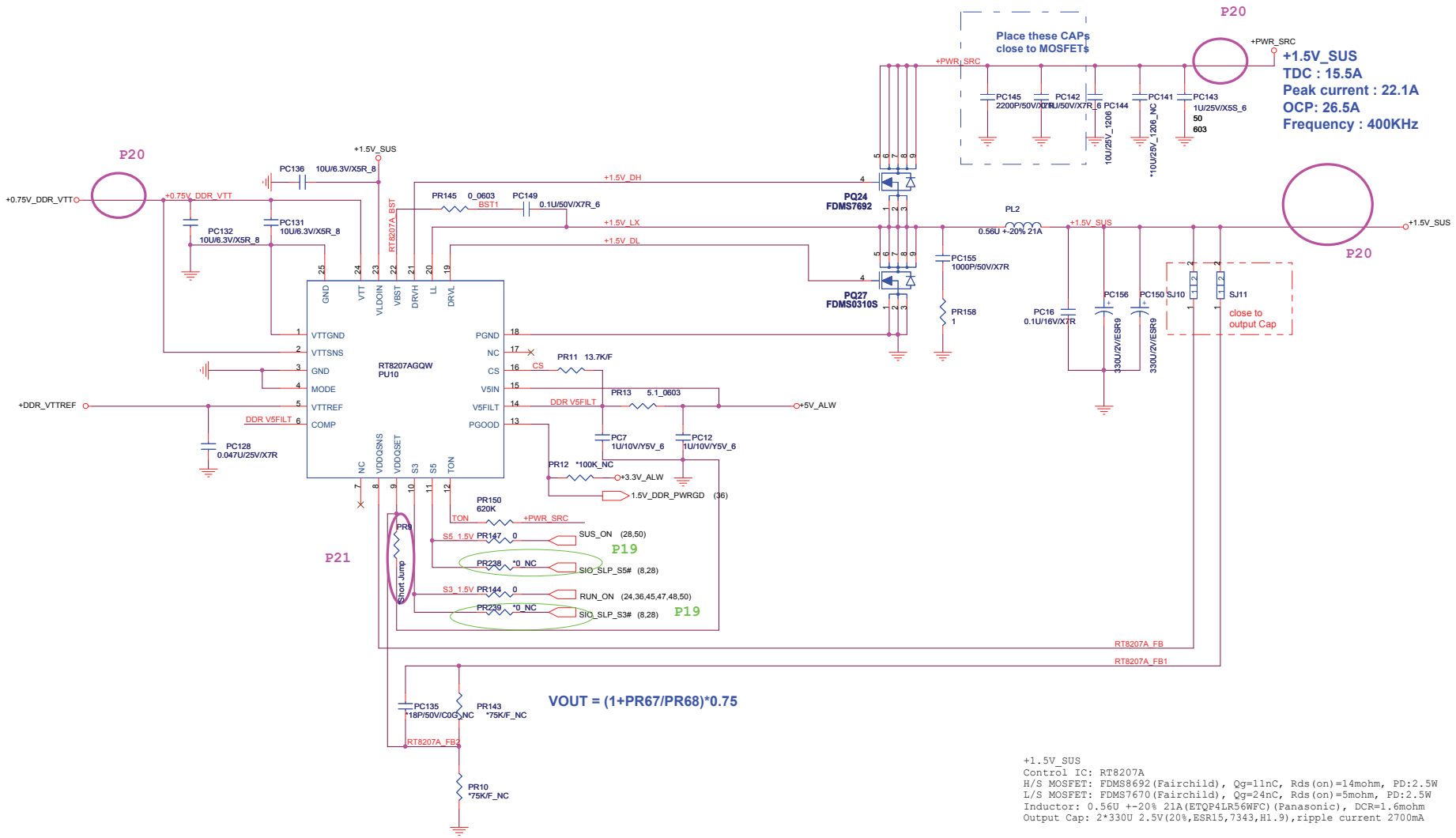


Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	1.8V_RUN & 1.8V_RUN_GFX	1A

Date: Friday, January 07, 2011 Sheet 45 of 59



+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.56U +-20% 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
Output Cap: 2*330U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

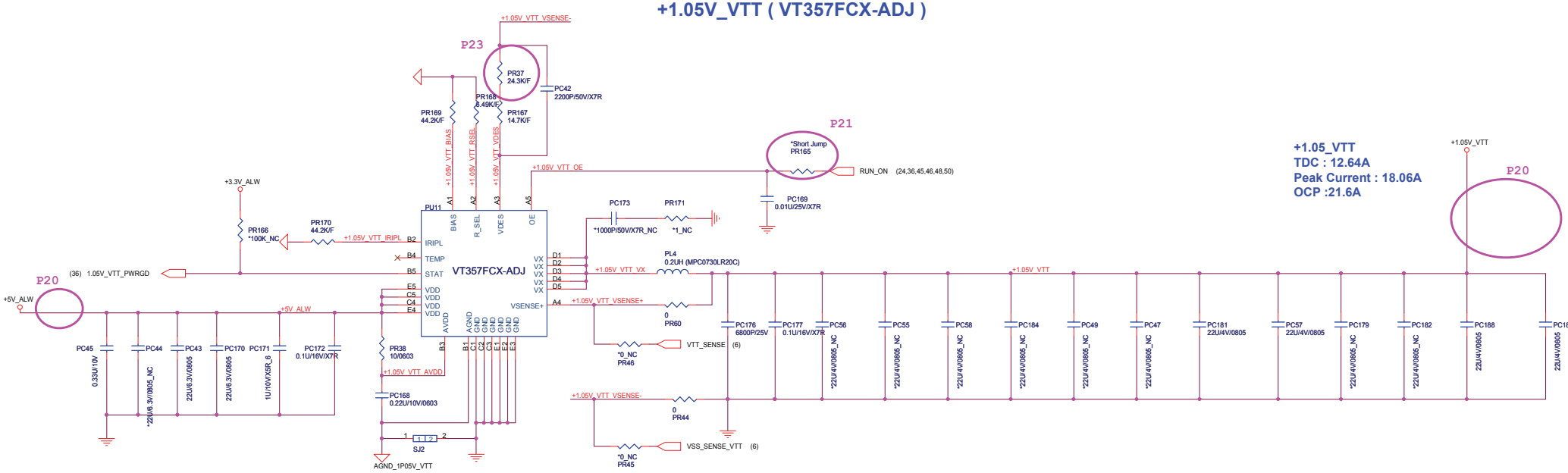
VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: 1.5V_SUS & 0.75_DDR_VTT (RT8207) | Rev: 1A
Date: Friday, January 07, 2011 | Sheet 46 of 59

+1.05V_VTT (VT357FCX-ADJ)

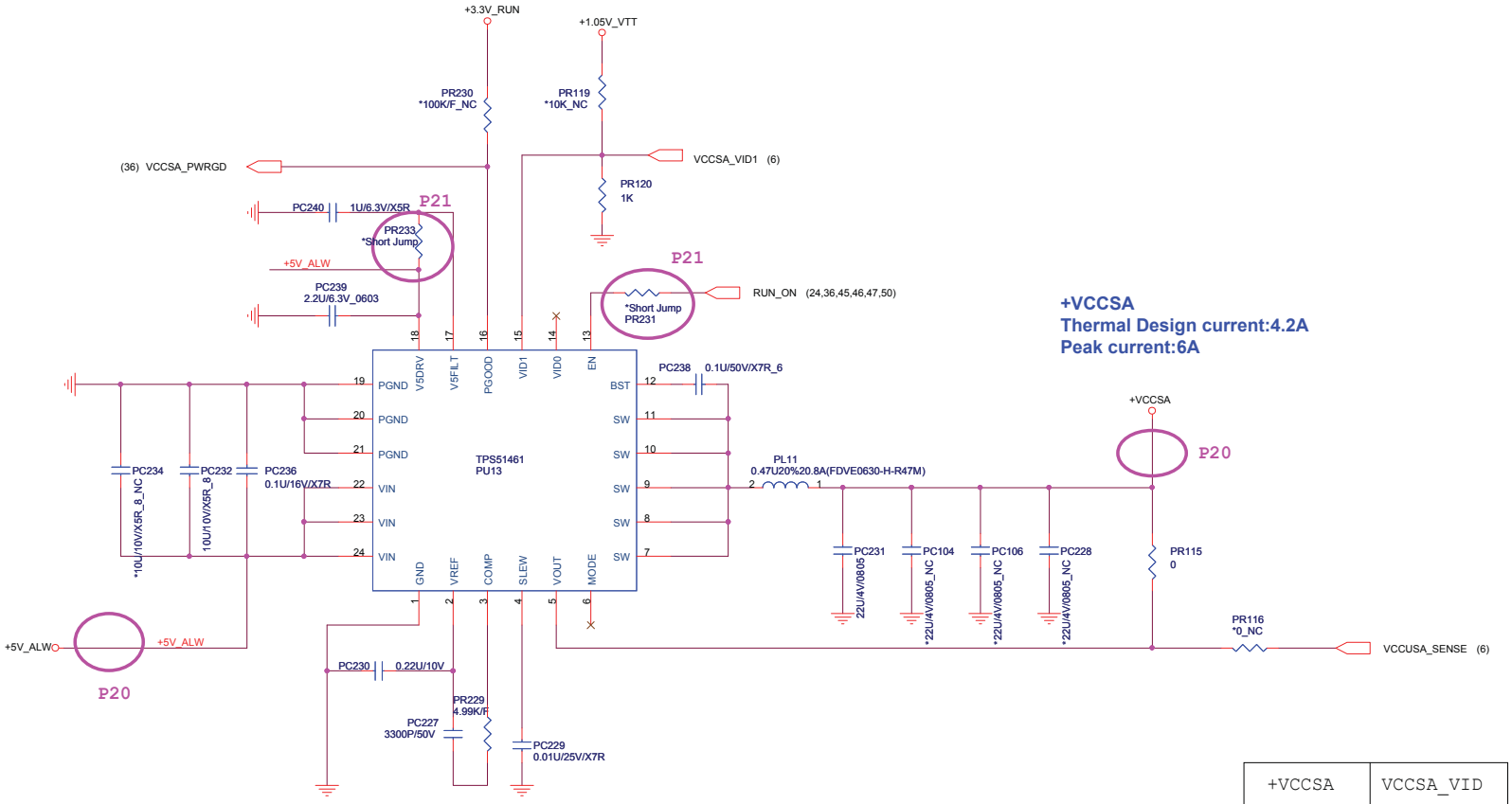


Route +1.05V_VTT_VSENSE+ and +1.05V_VTT_VSENSE-
as differential pair

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	1.05V_VTT	1A
Date: Friday, January 07, 2011	Sheet 47 of 59	



+VCCSA	VCCSA_VID
0.8V	High
0.9V	Low

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	VCCSA (TPS51461)	1A

Date: Friday, January 07, 2011 Sheet 48 of 59

N12P-GE:

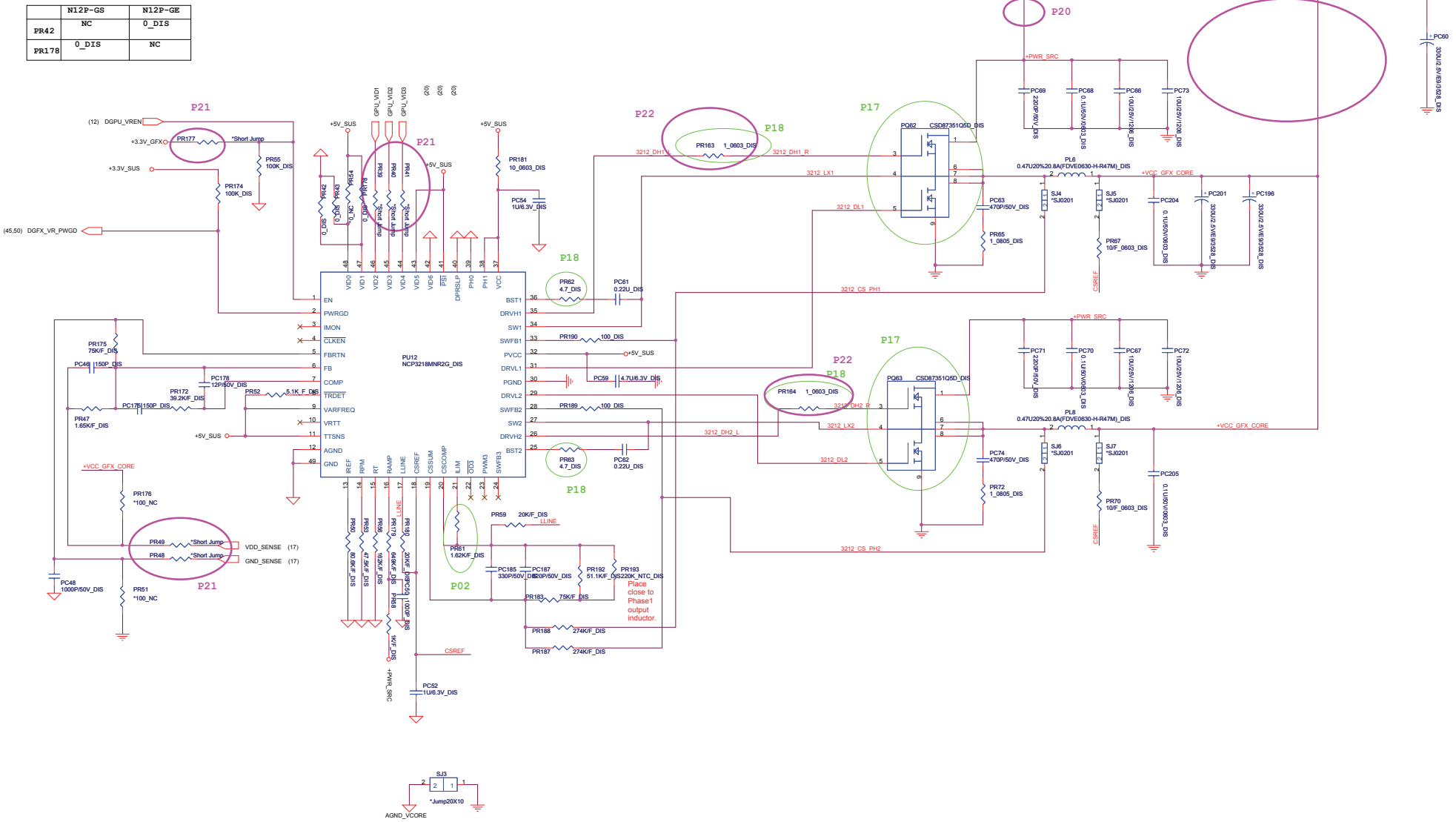
	GPU_VID3	GPU_VID2	GPU_VID1
0.85V	1	0	1
0.95V	0	1	1
1.0V	0	1	0

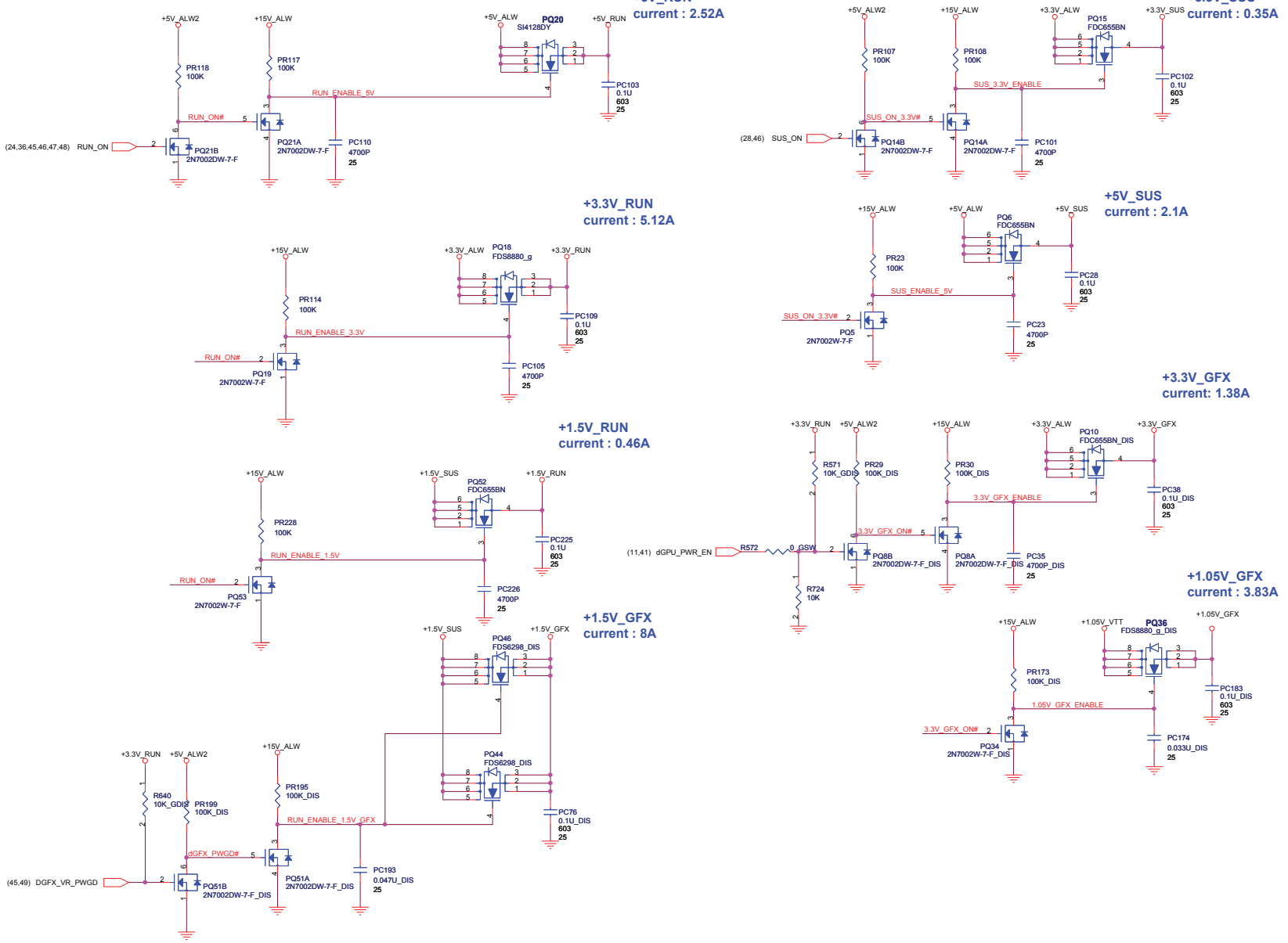
N12P-GS:

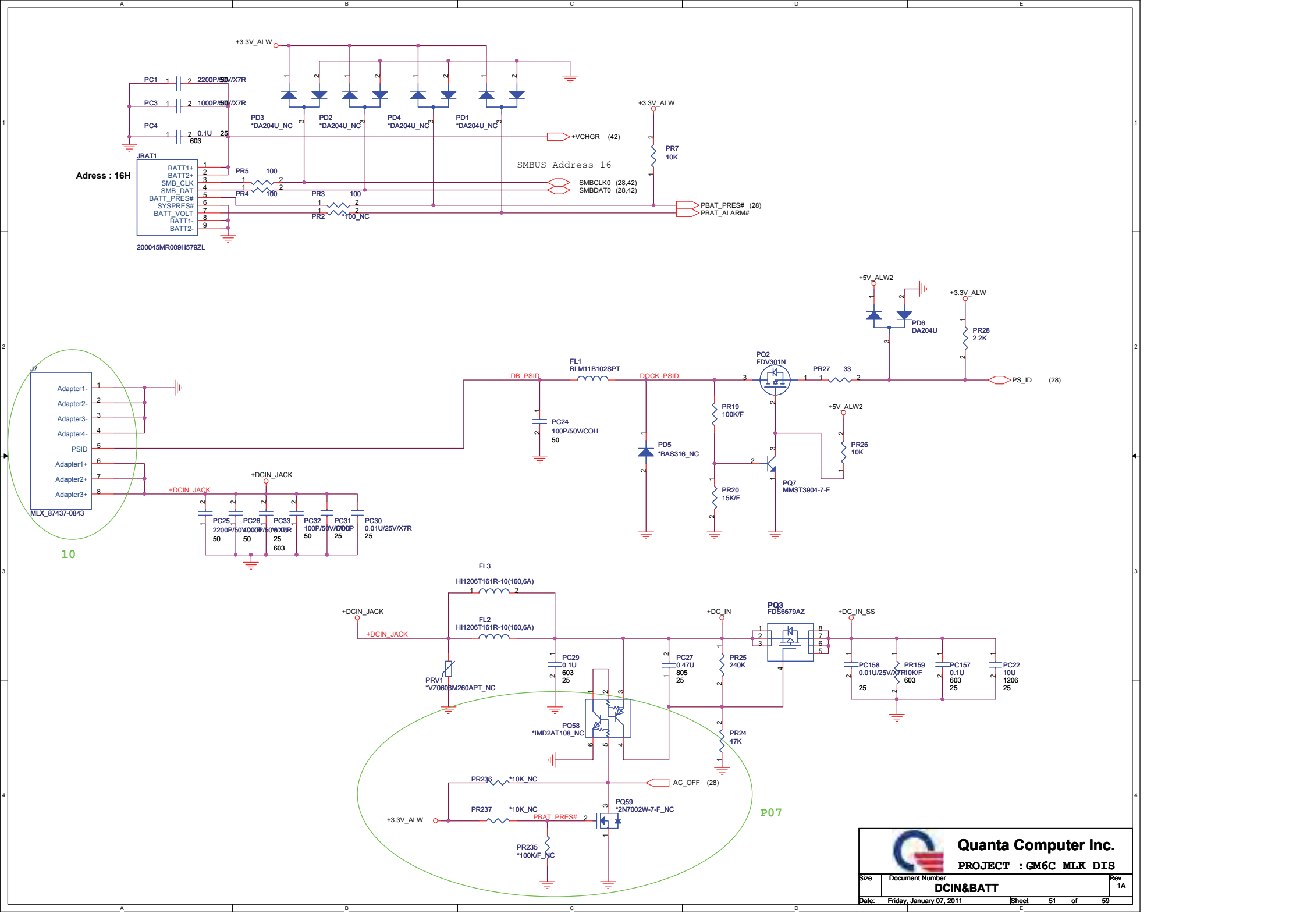
	GPU_VID3	GPU_VID2	GPU_VID1
0.825V	1	0	1
0.975V	0	1	0
1.0V	0	0	1

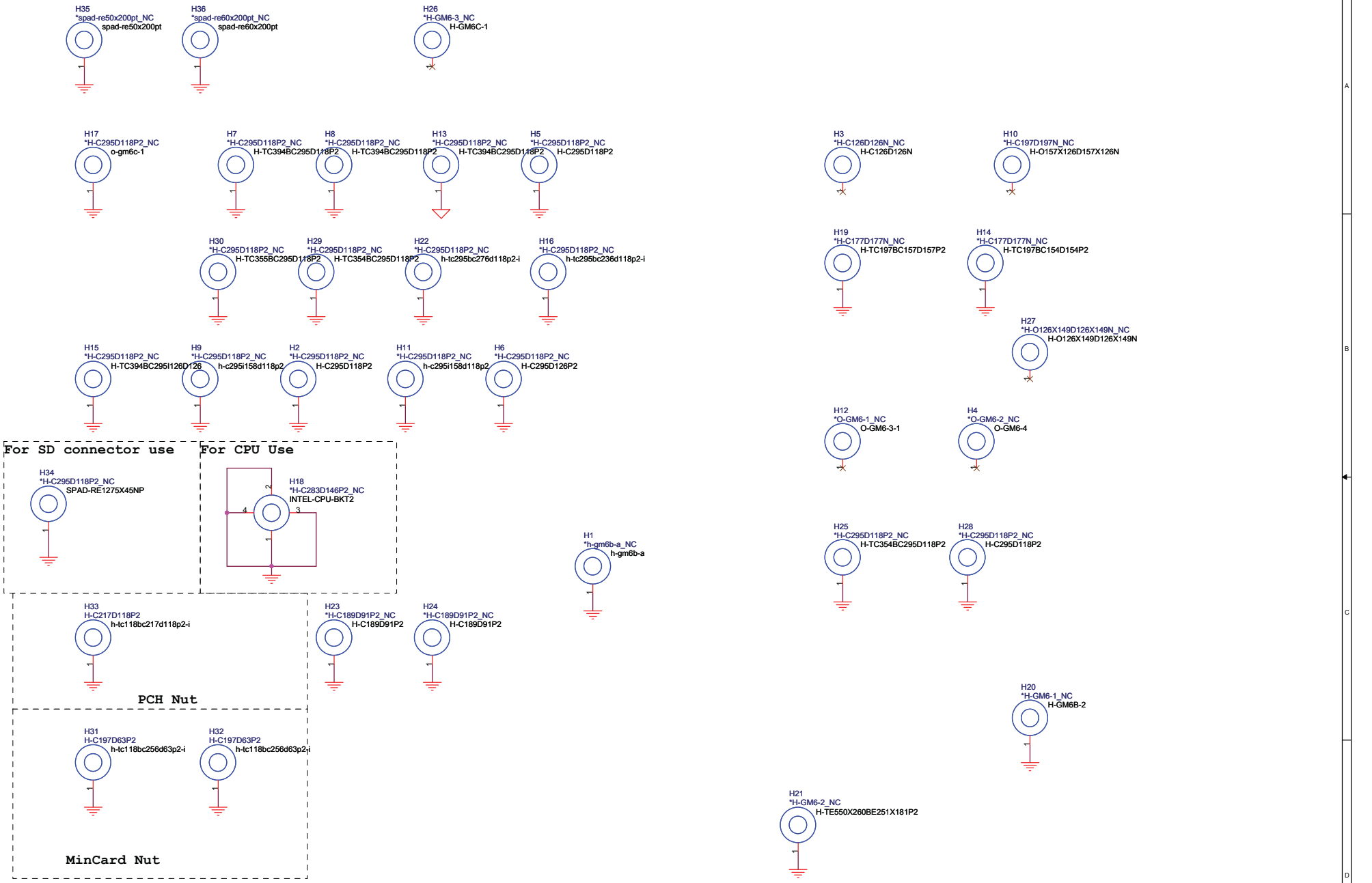
	N12P-GS	N12P-GE
PR42	NC	0_DIS
PR178	0_DIS	NC

+VCC_GFX_CORE
Fs=300K
Current:21.81A
OCP:52A




+5V_RUN
current : 2.52A
+3.3V_SUS
current : 0.35A
+3.3V_RUN
current : 5.12A
+5V_SUS
current : 2.1A
+3.3V_GFX
current: 1.38A
+1.5V_RUN
current : 0.46A
+1.05V_GFX
current : 3.83A
+1.5V_GFX
current : 8A
Reserve discharge path
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Run Power Switch
Rev 1A
Friday, January 07, 2011
Sheet 50 of 59

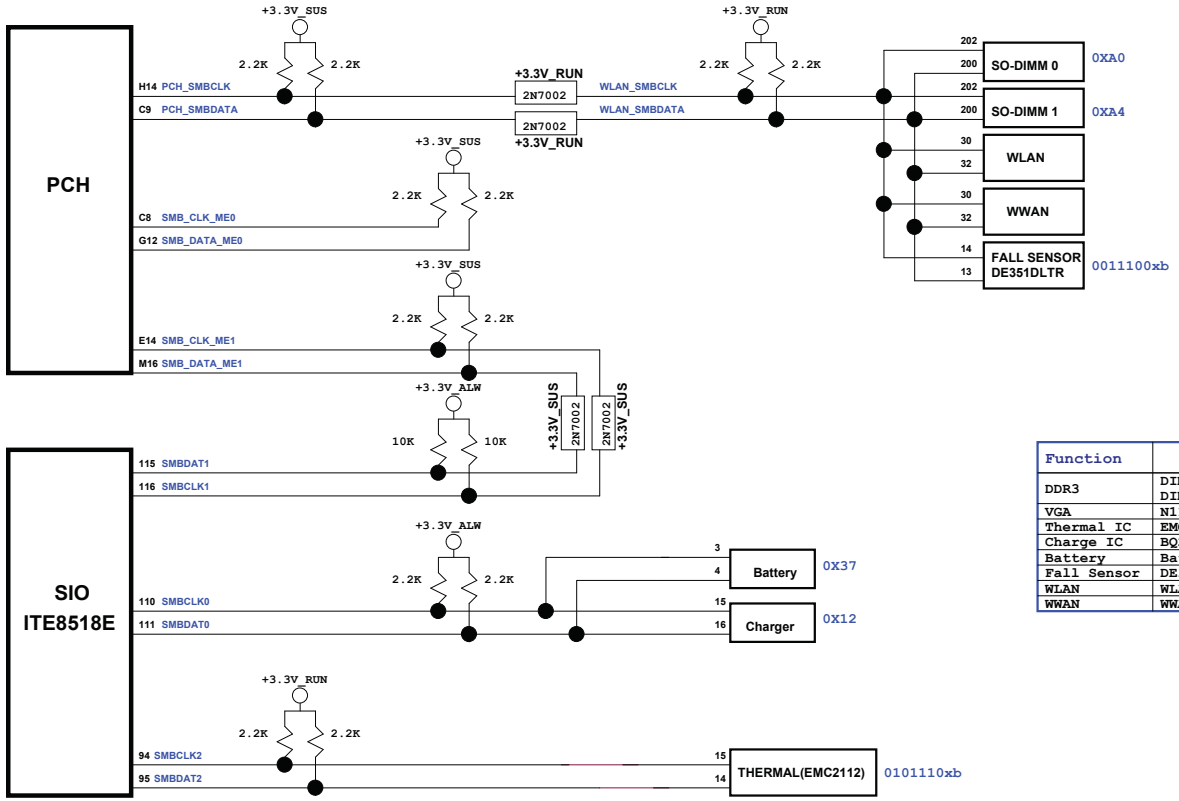

+3.3V_ALW
PC1 2200P/50V/X7R
PC3 1000P/50V/X7R
PC4 0.1U 25 603
PD3 *DA204U_NC
PD2 *DA204U_NC
PD4 *DA204U_NC
PD1 *DA204U_NC
+VCHGR (42)
JBAT1
Adress : 16H
BATT1+
BATT2+
SMB_CLK
SMB_DAT
BATT_PRES#
SYSPRES#
BATT_VOLT
BATT1-
BATT2-
PR5 100
PR4 100
PR3 100
PR2 *100_NC
SMBUS Address 16
SMBCLK0 (28,42)
SMBDAT0 (28,42)
PR7 10K
PBAT_PRES# (28)
PBAT_ALARM#
200045MR009H579ZL
J7
Adapter1-
Adapter2-
Adapter3-
Adapter4-
PSID
Adapter1+
Adapter2+
Adapter3+
MLX_87437-0843
10
+DCIN_JACK
PC25 2200P/50V/X7R 50
PC26 1000P/50V/X7R 50
PC33 0.1U 25 603
PC32 100P/50V/COH 50
PC31 470P 25
PC30 0.01U/25V/X7R 25
DB_PSID
FL1 BLM11B102SPT
DOCK_PSID
PC24 100P/50V/COH 50
PD5 *BAS316_NC
PR19 100K/F
PR20 15K/F
PQ2 FDV301N
PQ7 MMST3904-7-F
PR26 10K
+5V_ALW2
PD6 DA204U
PR27 33
PR28 2.2K
PS_ID (28)
FL3 HI1206T161R-10(160,6A)
FL2 HI1206T161R-10(160,6A)
PRV1 *VZ0603M260APT_NC
PC29 0.1U 603 25
PC27 0.47U 805 25
PR25 240K
PQ3 FDS6679AZ
+DC_IN
+DC_IN_SS
PC158 0.01U/25V/X7R 25
PR159 10K/F 603
PC157 0.1U 603 25
PC22 10U 1206 25
PQ58 *IMD2AT108_NC
PR24 47K
PR236 *10K_NC
AC_OFF (28)
PR237 *10K_NC
PBAT_PRES#
PQ59 *2N7002W-7-F_NC
PR235 *100K/F_NC
P07
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size
Document Number
DCIN&BATT
Rev 1A
Date: Friday, January 07, 2011
Sheet 51 of 59



Quanta Computer Inc.

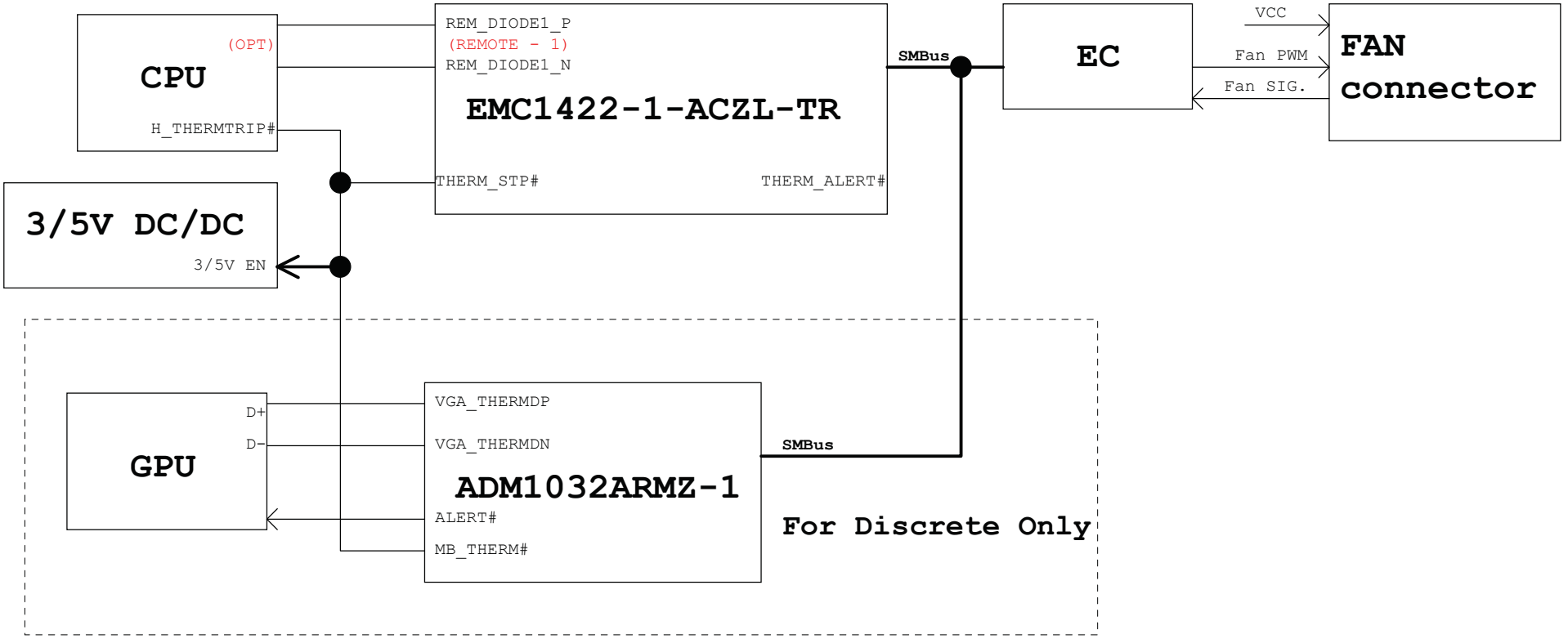
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	PAD & SCREW	1A
Date: Friday, January 07, 2011	Sheet 52 of 59	



Function	IC	SMBus Address
DDR3	DIMM0 DIMM1	A0 A4
VGA	N11P	9E
Thermal IC	EMC2112	0011100xb
Charge IC	BQ24765RUVR	0x12
Battery	Battery	0X37
Fall Sensor	DE351DLTR	0101110xb
WLAN	WLAN Module	X
WWAN	WWAN Module	X

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: SMBUS | Rev: 1A
Date: Friday, January 07, 2011 | Sheet 53 of 59



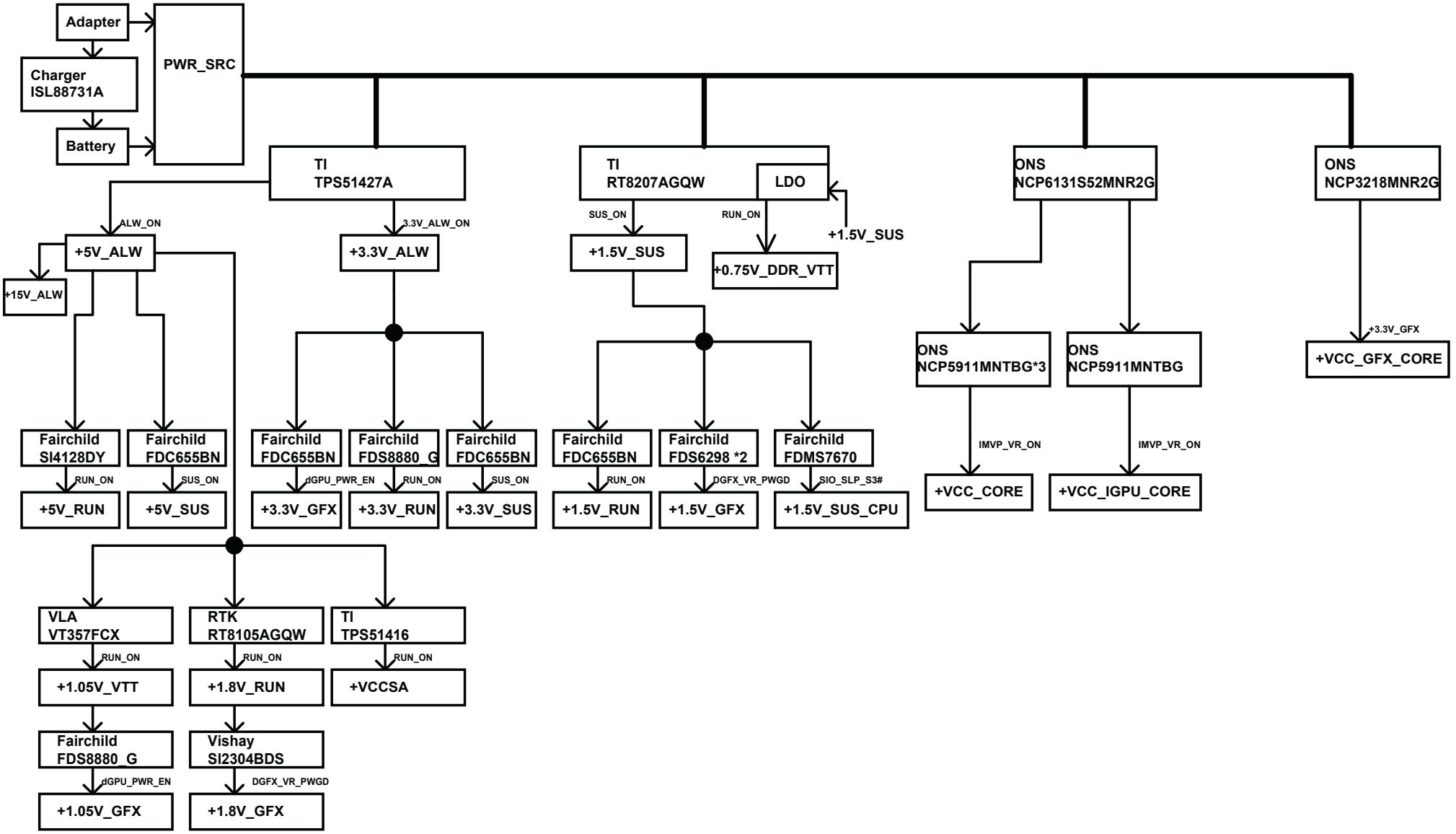
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	THERMAL MAP	1A

Date: Friday, January 07, 2011 Sheet 54 of 59

VER : 1A



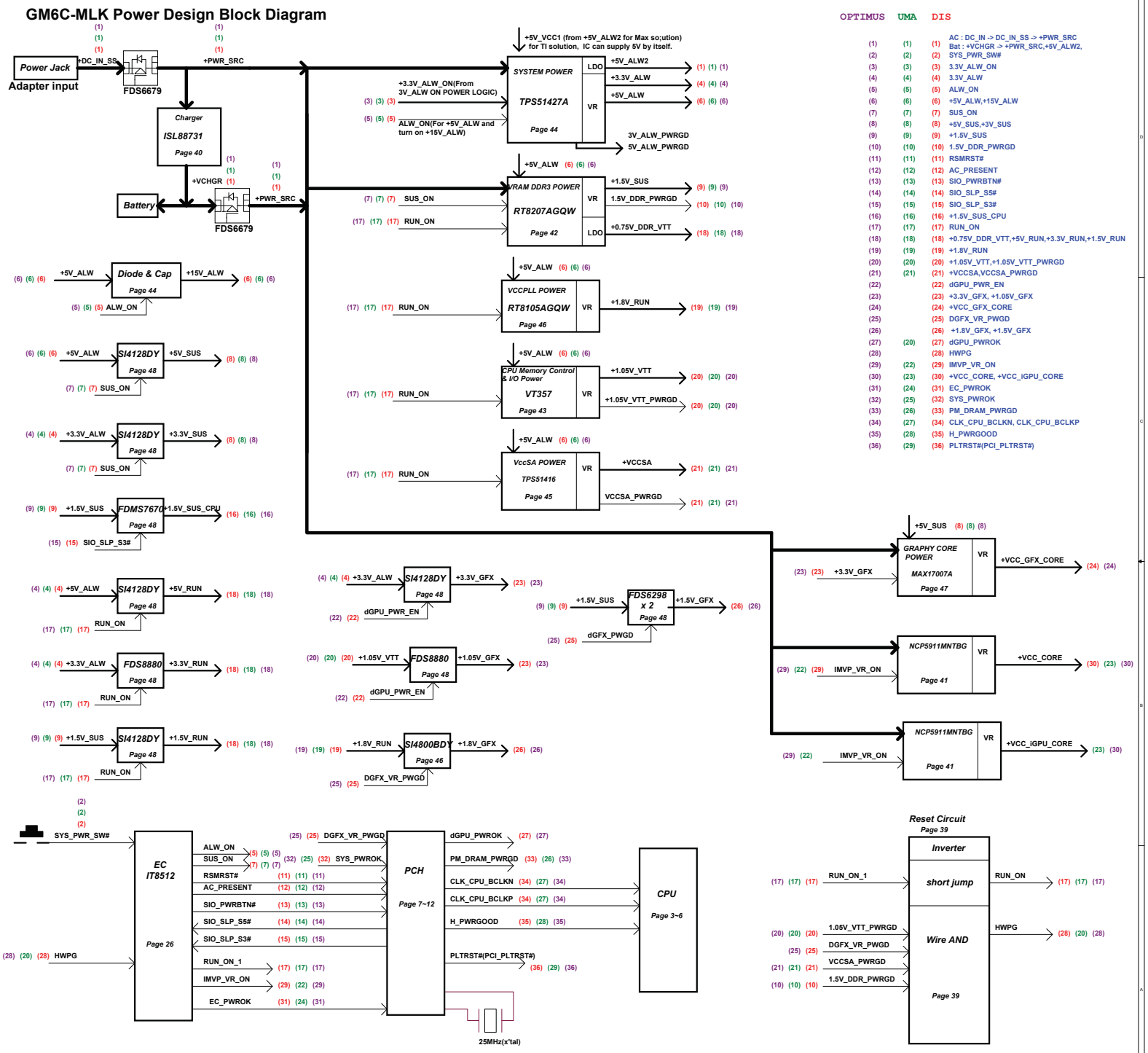
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Power Block Diagram	1A

Date: Friday, January 07, 2011 Sheet 55 of 59

GM6C-MLK Power Design Block Diagram



OPTIMUS	UMA	DIS	
(1)	(1)	(1)	AC : DC_IN -> DC_IN_SS -> +PWR_SRC Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2)	(2)	(2)	SYS_PWR_SW#
(3)	(3)	(3)	3.3V_ALW_ON
(4)	(4)	(4)	3.3V_ALW
(5)	(5)	(5)	ALW_ON
(6)	(6)	(6)	+5V_ALW,+15V_ALW
(7)	(7)	(7)	SUS_ON
(8)	(8)	(8)	+5V_SUS,+3V_SUS
(9)	(9)	(9)	+1.5V_SUS
(10)	(10)	(10)	1.5V_DDR_PWRGD
(11)	(11)	(11)	RSMRST#
(12)	(12)	(12)	AC_PRESENT
(13)	(13)	(13)	SIO_PWRBTN#
(14)	(14)	(14)	SIO_SLP_S5#
(15)	(15)	(15)	SIO_SLP_S3#
(16)	(16)	(16)	+1.5V_SUS_CPU
(17)	(17)	(17)	RUN_ON
(18)	(18)	(18)	+0.75V_DDR_VTT,+5V_RUN,+3.3V_RUN,+1.5V_RUN
(19)	(19)	(19)	+1.8V_RUN
(20)	(20)	(20)	+1.05V_VTT,+1.05V_VTT_PWRGD
(21)	(21)	(21)	+VCCSA,VCCSA_PWRGD
(22)		(22)	dGPU_PWR_EN
(23)		(23)	+3.3V_GFX, +1.05V_GFX
(24)		(24)	+VCC_GFX_CORE
(25)		(25)	DGFX_VR_PWGD
(26)		(26)	+1.8V_GFX, +1.5V_GFX
(27)	(20)	(27)	dGPU_PWROK
(28)		(28)	HWPG
(29)	(22)	(29)	IMVP_VR_ON
(30)	(23)	(30)	+VCC_CORE, +VCC_iGPU_CORE
(31)	(24)	(31)	EC_PWROK
(32)	(25)	(32)	SYS_PWROK
(33)	(26)	(33)	PM_DRAM_PWRGD
(34)	(27)	(34)	CLK_CPU_BCLKN, CLK_CPU_BCLKP
(35)	(28)	(35)	H_PWRGOOD
(36)	(29)	(36)	PLTRST#(PCI_PLTRST#)

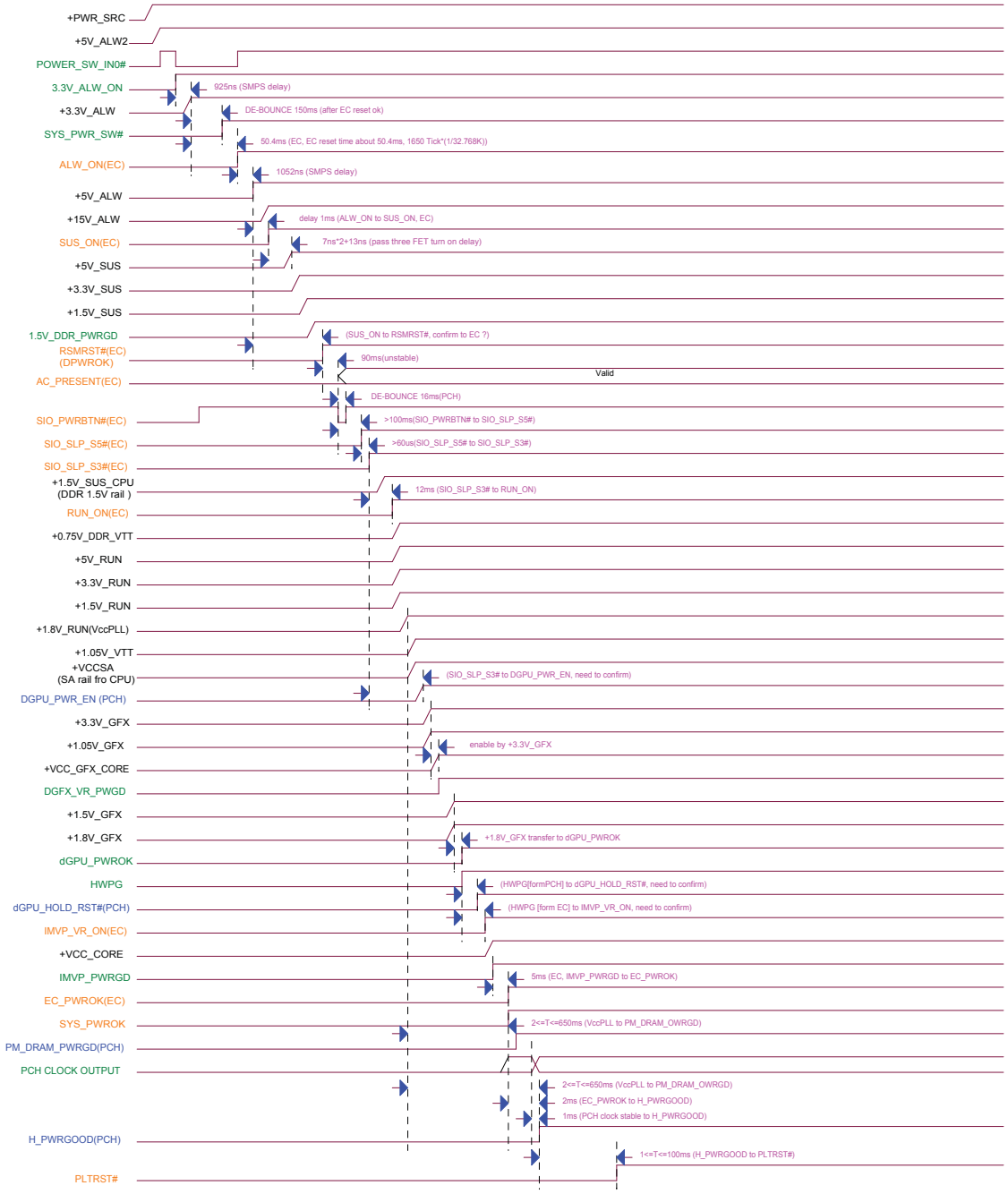
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size: | Document Number: Power sequence Block | Rev: 1A

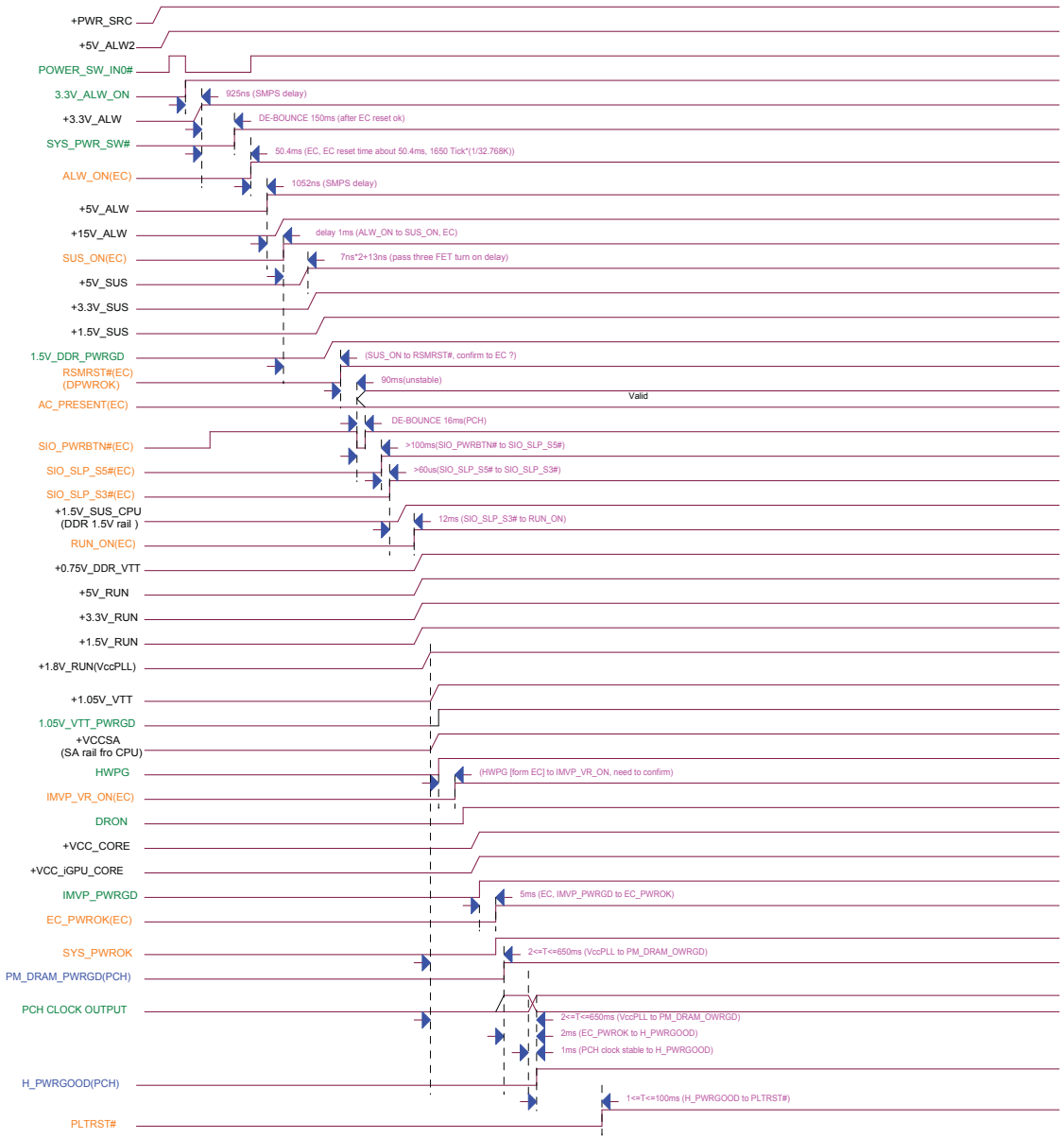
Date: Friday, January 07, 2011 | Sheet 56 of 59

GM6C_MLK_DIS Power on Timing(BATTERY MODE)



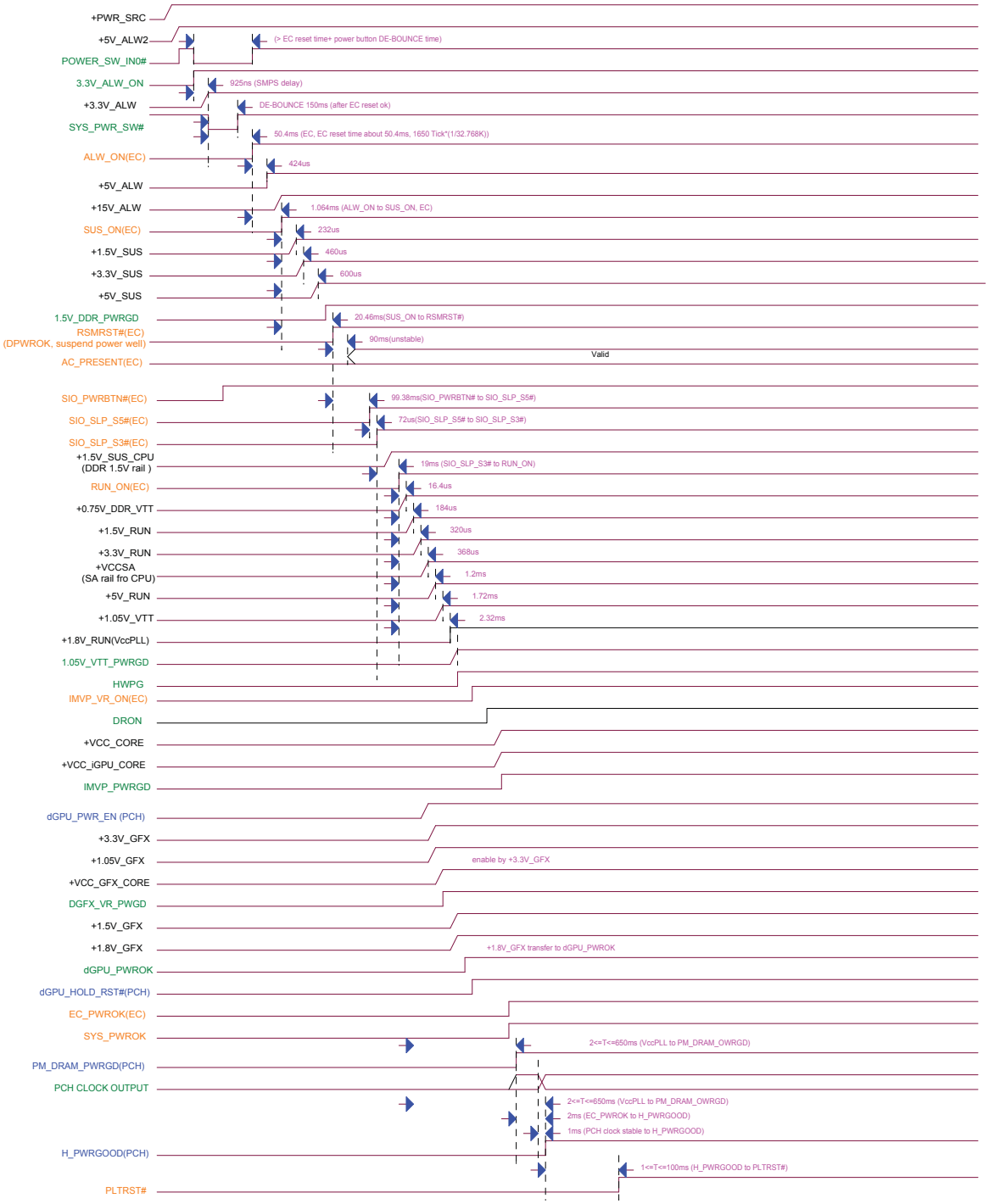
Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: POWER SEQUENCE(DIS)	Rev: 1A
Date: Friday, January 07, 2011	Sheet 57 of 59	

GM6C_MLK_UMA Power on Timing(BATTERY MODE)



Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: POWER SEQUENCE(UMA)	Rev: 1A
Date: Friday, January 07, 2011	Sheet 58 of 59	

GM6C_MLK_OPTIMUS Power on Timing(BATTERY MODE)



Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	POWER SEQUENCE(OPTIMUS)	1A
Date: Friday, January 07, 2011	Sheet 59 of 59	