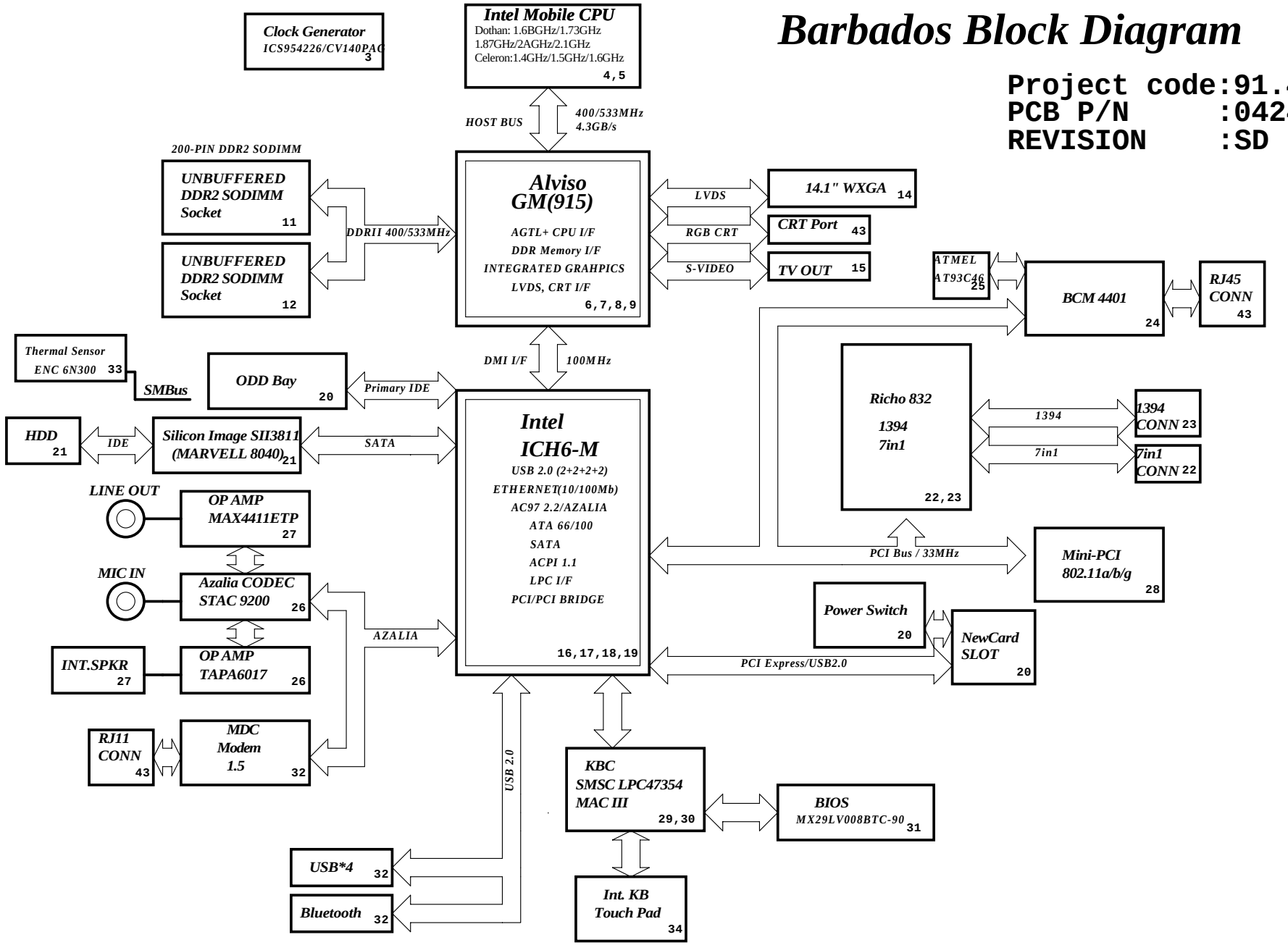
Barbados Block Diagram

Project code:91.4C401.001
PCB P/N :04242
REVISION :SD



System DC/DC MAX8734A 39	
INPUTS	OUTPUTS
PWR_SRC	+5VSUS +3VSRC
Battery Charger MAX1909 42	
PWR_SRC	BATT+
System DC/DC MAX8743 40	
PWR_SRC	+1.05VRUN +1.5VSUS
CPU DC/DC ISL6217 38	
PWR_SRC	VCC_CORE
DDR2 DC/DC TI 51116 41	
PWR_SRC	+1.8VSUS +0.9VRUN +0.9VSUS_DDR2VREF

PCB LAYER
L1:TOP
L2:Signal
L3:GND
L4:Signal
L5:Signal
L6:VCC
L7:GND
L8:BOT

Wistron/Dell confidential

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Alviso Strapping Signals and Configuration

Pin Name	Strap Description	Configuration page 7
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott **1 = Dothan** (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled** (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V** (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

For Dothan B stepping

	CPU		NB			CLOCK		
	BSEL1	BSEL0	CFG2	CFG1	CFG0	FS_C	FS_B	FS_A
100MHZ	0	1	1	0	1	1	0	1
133MHZ	0	0	0	0	1	0	0	1

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
LAN Broadcom BCM4401/BCM5507	AD16	PIRQC#	REQ4# / GNT4#
MINIPCI SLOT	AD19	PIRQB# PIRQD#	REQ3# / GNT3#
R5C832	AD17	PIRQA# PIRQC#	REQ1# / GNT1#

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

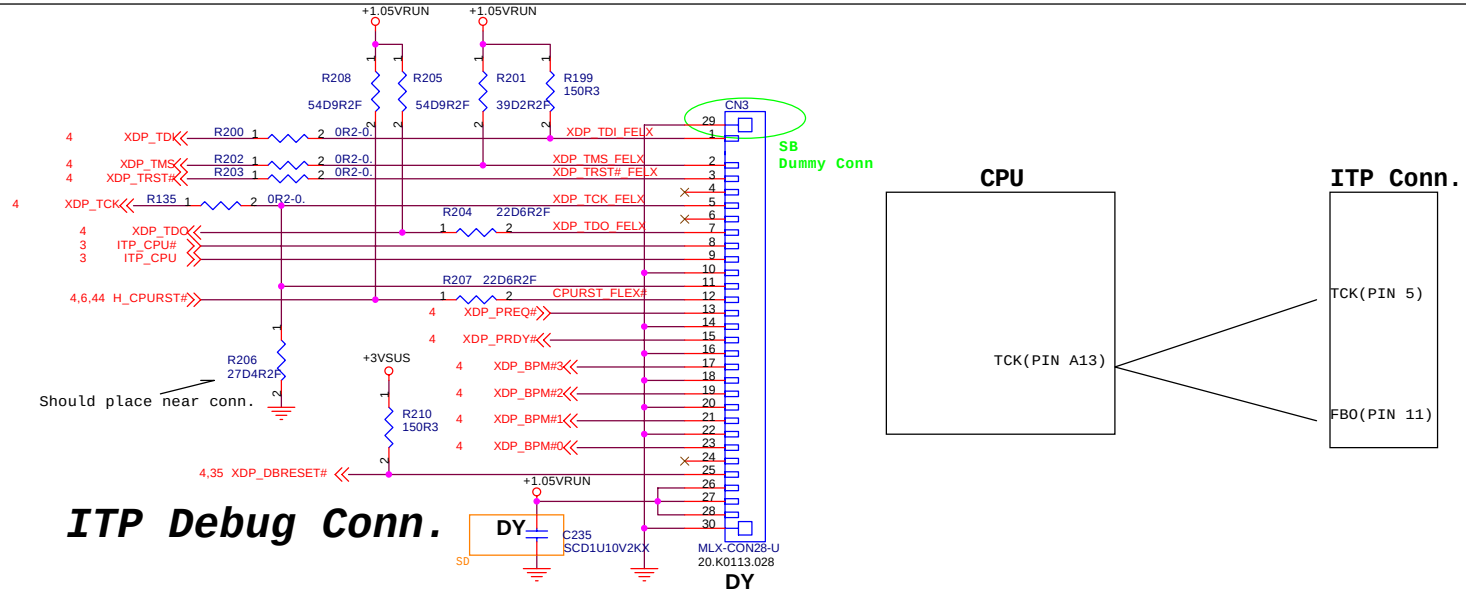
ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH6-M Strapping Signals and Configuration

Pin Name	Strap Description	Note
ACZ_SDOUT	0=Normal(default) 1=XOR Test mode	
ACZ_SYNC	0=Normal(default)	1=Reserved
DPRSLPVR	0=Normal	1=Reserved
EE_CS	0=Normal	1=Reserved
EE_DOUT	0=Normal	1=Reserved
GNT[5]#/GPO[17]#	0=PCI cycles to FWH 1=PCI cycles to LPC (default)	Selects memory range to FWD to out of PCI
GNT(6)#/GPO(16)#	0="Top block swap" mode 1=Normal(default)	"Top block swap" inverts A16 on cycles to FWH
GPIO[25]	0=Internal 2.5V DISEN(default) 1=ENABLE Internal Vcc2_5VRM	
INTVRMEN	0=Internal VccSus1.5V DISEN (default) 1=ENABLE Internal VccSus1.5VRM	
LINKALERT#	1=Normal(requires external PU)	0=Reserved
REQ[4:1]	XOR Test Chain Selection	Requires external resistors
SATALED#	0=Normal(default)	1=Reserved
SPKR	0=Normal(default) 1=NO Reboot	
TP[3]	0=Enter XOR Test mode 1=Normal(default)	

NOTE: All strap signals are sampled on the rising edge of the ICH6-M's PWROK signal.



BATT+ BATT+ 42,43
DC_IN+ DC_IN+ 42,43,44
PWR_SRC PWR_SRC 14,29,38,39,40,41,42,43,44
VCCRTC VCCRTC 16,18,29,33

+0.9VSUS_DDR2VREF +0.9VSUS_DDR2VREF 7,11,12,41,44
+5VSUS +5VSUS 18,26,27,32,33,36,39,40,41,43,44
+3VSUS +3VSUS 14,17,18,19,20,24,25,27,28,32,33,35,36,39,40,41,43,44
+1.5VSUS +1.5VSUS 18,36,40,44

+2.5VRUN +2.5VRUN 7,9,14,15,18,36,43,44
+5VRUN +5VRUN 14,15,18,20,21,26,28,30,33,34,36,38,43,44
+12V +12V 14,23,33,36,43,44
+1.5VRUN +1.5VRUN 5,7,9,17,18,20,36,44
VCC_CORE VCC_CORE 5,36,38,44
+1.05VRUN +1.05VRUN 3,4,5,6,7,9,10,16,18,33,36,40,44
LCDVDD LCDVDD 14,44
+3VRUN +3VRUN 3,4,9,11,12,14,15,17,18,19,20,21,22,23,26,27,28,29,30,32,33,35,36,38,43,44

+5VALW +5VALW 14,30,36,39,43,44
+3VALW +3VALW 4,14,20,22,29,30,31,33,34,39,43,44

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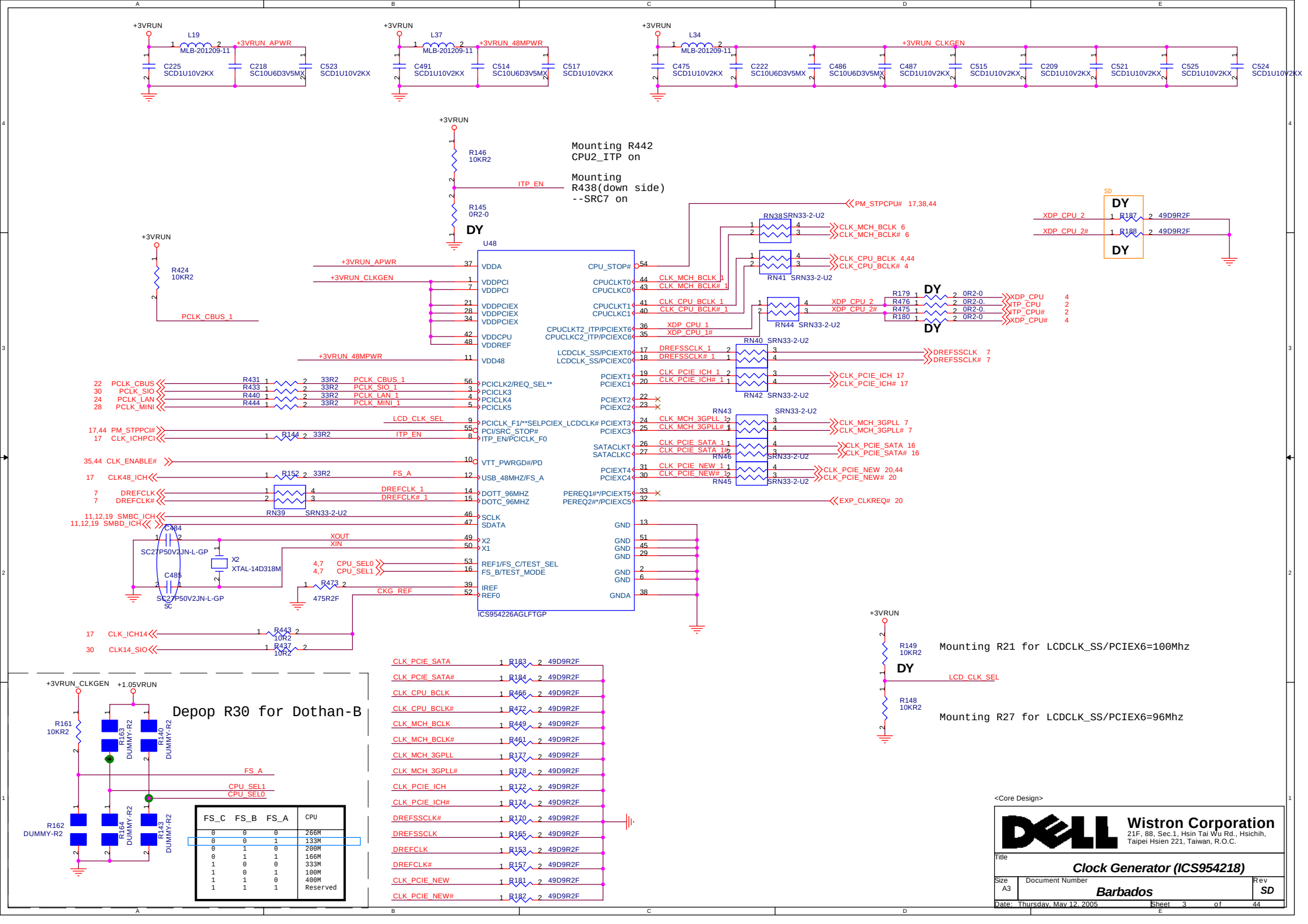
+3VRUN
L19
MLB-201209-11
+3VRUN_APWR
C225 SCD1U10V2KX
C218 SC10U6D3V5MX
C523 SCD1U10V2KX
L37
MLB-201209-11
+3VRUN_48MPWR
C491 SCD1U10V2KX
C514 SC10U6D3V5MX
C517 SCD1U10V2KX
L34
MLB-201209-11
+3VRUN_CLKGEN
C475 SCD1U10V2KX
C222 SC10U6D3V5MX
C486 SC10U6D3V5MX
C487 SCD1U10V2KX
C515 SCD1U10V2KX
C209 SCD1U10V2KX
C521 SCD1U10V2KX
C525 SCD1U10V2KX
C524 SCD1U10V2KX
R146 10KR2
ITP_EN
R145 0R2-0
DY
Mounting R442
CPU2_ITP on
Mounting
R438(down side)
--SRC7 on
R424 10KR2
PCLK_CBUS_1
U48
+3VRUN_APWR
+3VRUN_CLKGEN
+3VRUN_48MPWR
VDDA
VDDPCI
VDDPCIEX
VDDCPU
VDDREF
VDD48
PCICLK2/REQ_SEL**
PCICLK3
PCICLK4
PCICLK5
PCICLK_F1/**SELPCIEX_LCDCLK#
PCI/SRC_STOP#
ITP_EN/PCICLK_F0
VTT_PWRGD#/PD
USB_48MHZ/FS_A
DOTT_96MHZ
DOTC_96MHZ
SCLK
SDATA
X2
X1
REF1/FS_C/TEST_SEL
FS_B/TEST_MODE
IREF
REF0
CPU_STOP#
CPUCLKT0
CPUCLKC0
CPUCLKT1
CPUCLKC1
CPUCLKT2_ITP/PCIEXT6
CPUCLKC2_ITP/PCIEXC6
LCDCLK_SS/PCIEXT0
LCDCLK_SS/PCIEXC0
PCIEXT1
PCIEXC1
PCIEXT2
PCIEXC2
PCIEXT3
PCIEXC3
SATACLKT
SATACLKC
PCIEXT4
PCIEXC4
PEREQ1#*/PCIEXT5
PEREQ2#*/PCIEXC5
GND
GNDA
ICS954226AGLFTGP
PCLK_CBUS
PCLK_SIO
PCLK_LAN
PCLK_MINI
PM_STPPCI#
CLK_ICHPCI
CLK_ENABLE#
CLK48_ICH
DREFCLK
DREFCLK#
SMBC_ICH
SMBD_ICH
LCD_CLK_SEL
ITP_EN
FS_A
DREFCLK_1
DREFCLK#_1
SC27P50V2JN-L-GP
XOUT
XIN
XTAL-14D318M
CPU_SEL0
CPU_SEL1
CKG_REF
475R2F
CLK_ICH14
CLK14_SIO
PM_STPCPU# 17,38,44
RN38 SRN33-2-U2
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
CLK_CPU_BCLK 4,44
CLK_CPU_BCLK# 4
RN41 SRN33-2-U2
CLK_MCH_BCLK_1
CLK_MCH_BCLK#_1
CLK_CPU_BCLK_1
CLK_CPU_BCLK#_1
XDP_CPU_1
XDP_CPU_1#
RN44 SRN33-2-U2
XDP_CPU_2
XDP_CPU_2#
R179 0R2-0
R476 0R2-0
R475 0R2-0
R180 0R2-0
XDP_CPU
ITP_CPU
ITP_CPU#
XDP_CPU#
RN40 SRN33-2-U2
DREFSSCLK_1
DREFSSCLK#_1
DREFSSCLK 7
DREFSSCLK# 7
RN42 SRN33-2-U2
CLK_PCIE_ICH_1
CLK_PCIE_ICH#_1
CLK_PCIE_ICH 17
CLK_PCIE_ICH# 17
RN43 SRN33-2-U2
CLK_MCH_3GPLL_1
CLK_MCH_3GPLL#_1
CLK_MCH_3GPLL 7
CLK_MCH_3GPLL# 7
RN46 SRN33-2-U2
CLK_PCIE_SATA_1
CLK_PCIE_SATA#_1
CLK_PCIE_SATA 16
CLK_PCIE_SATA# 16
RN45 SRN33-2-U2
CLK_PCIE_NEW_1
CLK_PCIE_NEW#_1
CLK_PCIE_NEW 20,44
CLK_PCIE_NEW# 20
EXP_CLKREQ# 20
SD
DY
XDP_CPU_2
XDP_CPU_2#
R187 49D9R2F
R188 49D9R2F
R149 10KR2
R148 10KR2
LCD_CLK_SEL
Mounting R21 for LCDCLK_SS/PCIEX6=100Mhz
Mounting R27 for LCDCLK_SS/PCIEX6=96Mhz
+3VRUN_CLKGEN
+1.05VRUN
R161 10KR2
R163 DUMMY-R2
R140 DUMMY-R2
R162 DUMMY-R2
R164 DUMMY-R2
R143 DUMMY-R2
Depop R30 for Dothan-B
FS_C FS_B FS_A CPU
0 0 0 266M
0 0 1 133M
0 1 0 200M
0 1 1 166M
1 0 0 333M
1 0 1 100M
1 1 0 400M
1 1 1 Reserved
CLK_PCIE_SATA R183 49D9R2F
CLK_PCIE_SATA# R184 49D9R2F
CLK_CPU_BCLK R466 49D9R2F
CLK_CPU_BCLK# R472 49D9R2F
CLK_MCH_BCLK R449 49D9R2F
CLK_MCH_BCLK# R461 49D9R2F
CLK_MCH_3GPLL R177 49D9R2F
CLK_MCH_3GPLL# R178 49D9R2F
CLK_PCIE_ICH R172 49D9R2F
CLK_PCIE_ICH# R174 49D9R2F
DREFSSCLK# R170 49D9R2F
DREFSSCLK R165 49D9R2F
DREFCLK R153 49D9R2F
DREFCLK# R157 49D9R2F
CLK_PCIE_NEW R181 49D9R2F
CLK_PCIE_NEW# R182 49D9R2F
<Core Design>
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Title
Clock Generator (ICS954218)
Size A3
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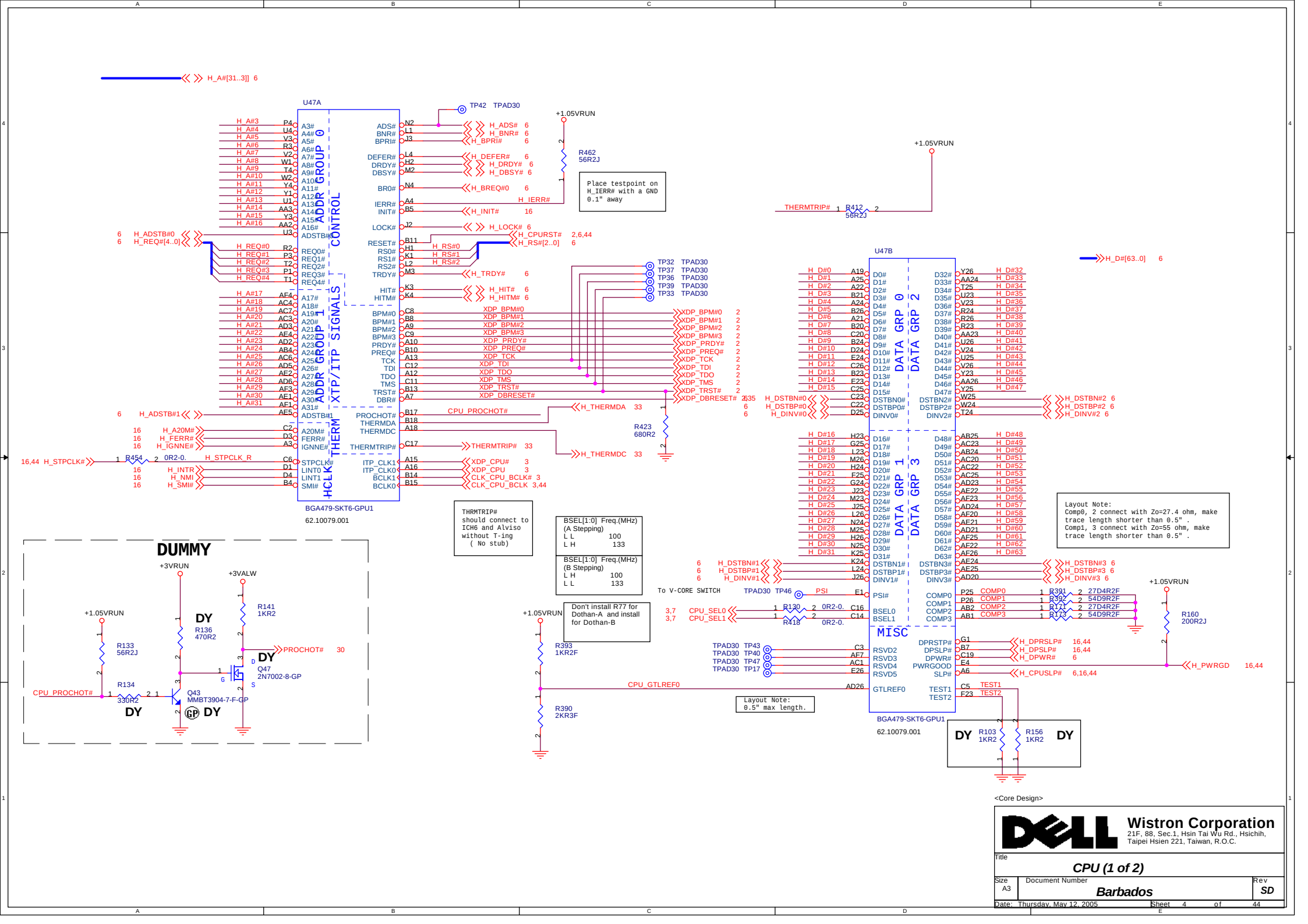
H_A#[31..3] 6
U47A
ADDR GROUP 0
ADDR GROUP 1
XTP/ITP SIGNALS
THERM
CLK
CONTROL
BGA479-SKT6-GPU1
62.10079.001
TP42 TPAD30
+1.05VRUN
R462 56R2J
Place testpoint on H_IERR# with a GND 0.1" away
THERMTRIP# R412 56R2J
U47B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
H_D#[63..0] 6
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
THRMTRIP# should connect to ICH6 and Alviso without T-ing (No stub)
BSEL[1:0] Freq.(MHz) (A Stepping) L L 100 L H 133
BSEL[1:0] Freq.(MHz) (B Stepping) L H 100 L L 133
To V-CORE SWITCH
Don't install R77 for Dothan-A and install for Dothan-B
Layout Note: 0.5" max length.
DUMMY
+3VRUN
+3VALW
+1.05VRUN
DY
R133 56R2J
R134 330R2
R136 470R2
R141 1KR2
Q43 MMBT3904-7-F-GP
Q47 2N7002-8-GP
PROCHOT# 30
CPU_PROCHOT#
R393 1KR2F
R390 2KR3F
CPU_GTLREF0
R103 1KR2
R156 1KR2
R160 200R2J
H_PWRGD 16,44
<Core Design>
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At Dothan 400Mhz CPU application, POWER is 1.8V.
At Dothan 533Mhz CPU application, POWER is 1.5V.
At Celeron CPU .13 application, POWER is 1.8V.
At Celeron CPU .09 application, POWER is 1.5V.

U47C

BGA479-SKT6-GPU1
62.10079.001

U47D

BGA479-SKT6-GPU1
62.10079.001

Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

Dummy 2 by layout

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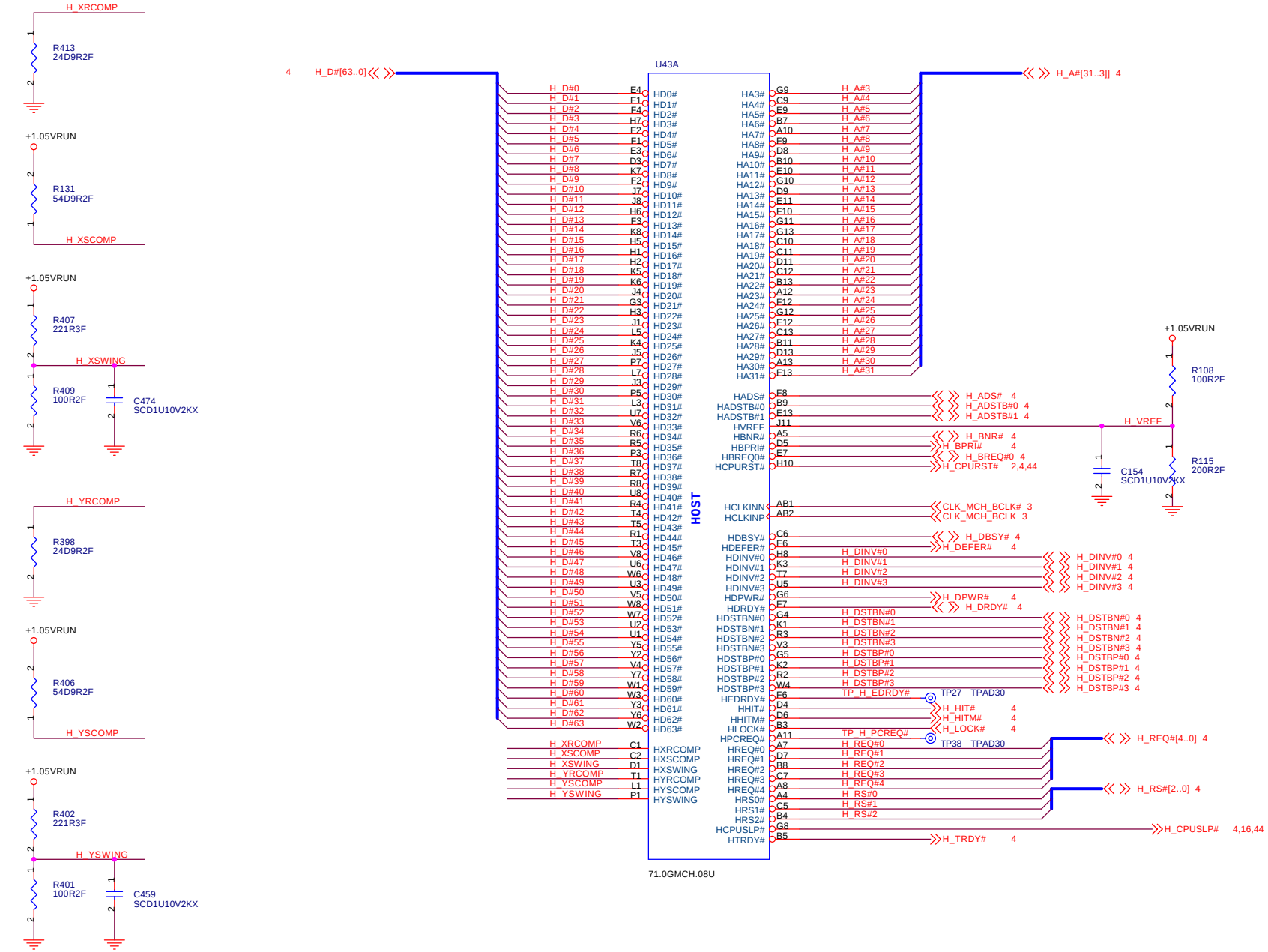

Place them near to the chip

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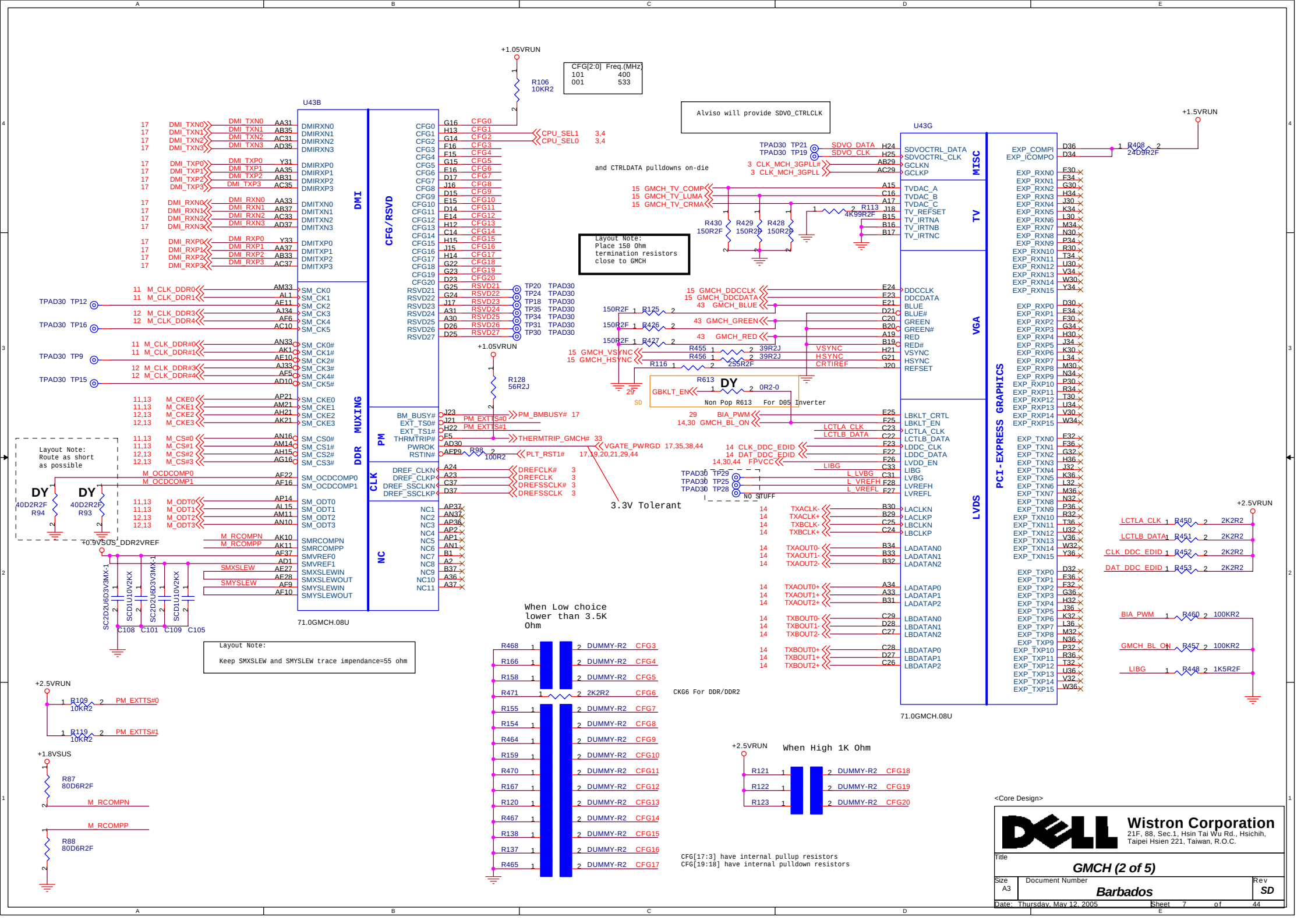
U43B
DMI
CFG/RSVD
DDR MUXING
PM
CLK
NC
DMIRXN0
DMIRXN1
DMIRXN2
DMIRXN3
DMIRXP0
DMIRXP1
DMIRXP2
DMIRXP3
DMITXN0
DMITXN1
DMITXN2
DMITXN3
DMITXP0
DMITXP1
DMITXP2
DMITXP3
SM_CK0
SM_CK1
SM_CK2
SM_CK3
SM_CK4
SM_CK5
SM_CK0#
SM_CK1#
SM_CK2#
SM_CK3#
SM_CK4#
SM_CK5#
SM_CKE0
SM_CKE1
SM_CKE2
SM_CKE3
SM_CS0#
SM_CS1#
SM_CS2#
SM_CS3#
SM_OCDCOMP0
SM_OCDCOMP1
SM_ODT0
SM_ODT1
SM_ODT2
SM_ODT3
SMRCOMPN
SMRCOMPP
SMVREF0
SMVREF1
SMXSLEWIN
SMXSLEWOUT
SMYSLEWIN
SMYSLEWOUT
BM_BUSY#
EXT_TS0#
EXT_TS1#
THRMTRIP#
PWROK
RSTIN#
DREF_CLKN
DREF_CLKP
DREF_SSCLKN
DREF_SSCLKP
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
71.0GMCH.08U
U43G
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
SDVOCTRL_DATA
SDVOCTRL_CLK
GCLKN
GCLKP
TVDAC_A
TVDAC_B
TVDAC_C
TV_REFSET
TV_IRTNA
TV_IRTNB
TV_IRTNC
DDCCLK
DDCDATA
BLUE
BLUE#
GREEN
GREEN#
RED
RED#
VSYNC
HSYNC
REFSET
LBKLT_CRTL
LBKLT_EN
LCTLA_CLK
LCTLB_CLK
LCTLB_DATA
LDDC_CLK
LDDC_DATA
LVDD_EN
LIBG
LVBG
LVREFH
LVREFL
LACLKN
LACLKP
LBCLKN
LBCLKP
LADATAN0
LADATAN1
LADATAN2
LADATAP0
LADATAP1
LADATAP2
LBDATAN0
LBDATAN1
LBDATAN2
LBDATAP0
LBDATAP1
LBDATAP2
EXP_COMPI
EXP_ICOMPO
EXP_RXN0
EXP_RXN1
EXP_RXN2
EXP_RXN3
EXP_RXN4
EXP_RXN5
EXP_RXN6
EXP_RXN7
EXP_RXN8
EXP_RXN9
EXP_RXN10
EXP_RXN11
EXP_RXN12
EXP_RXN13
EXP_RXN14
EXP_RXN15
EXP_RXP0
EXP_RXP1
EXP_RXP2
EXP_RXP3
EXP_RXP4
EXP_RXP5
EXP_RXP6
EXP_RXP7
EXP_RXP8
EXP_RXP9
EXP_RXP10
EXP_RXP11
EXP_RXP12
EXP_RXP13
EXP_RXP14
EXP_RXP15
EXP_TXN0
EXP_TXN1
EXP_TXN2
EXP_TXN3
EXP_TXN4
EXP_TXN5
EXP_TXN6
EXP_TXN7
EXP_TXN8
EXP_TXN9
EXP_TXN10
EXP_TXN11
EXP_TXN12
EXP_TXN13
EXP_TXN14
EXP_TXN15
EXP_TXP0
EXP_TXP1
EXP_TXP2
EXP_TXP3
EXP_TXP4
EXP_TXP5
EXP_TXP6
EXP_TXP7
EXP_TXP8
EXP_TXP9
EXP_TXP10
EXP_TXP11
EXP_TXP12
EXP_TXP13
EXP_TXP14
EXP_TXP15
71.0GMCH.08U
+1.05VRUN
+1.5VRUN
+2.5VRUN
+1.8VSUS
+0.9VSUS_DDR2VREF
CFG[2:0] Freq.(MHz)
101 400
001 533
Alviso will provide SDVO_CTRLCLK
and CTRLDATA pulldowns on-die
Layout Note:
Place 150 Ohm
termination resistors
close to GMCH
Layout Note:
Route as short
as possible
Layout Note:
Keep SMXSLEW and SMYSLEW trace impendance=55 ohm
DY
Non Pop R613 For D05 Inverter
3.3V Tolerant
When Low choice
lower than 3.5K
Ohm
When High 1K Ohm
CKG6 For DDR/DDR2
CFG[17:3] have internal pullup resistors
CFG[19:18] have internal pulldown resistors
<Core Design>
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
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GMCH (2 of 5)
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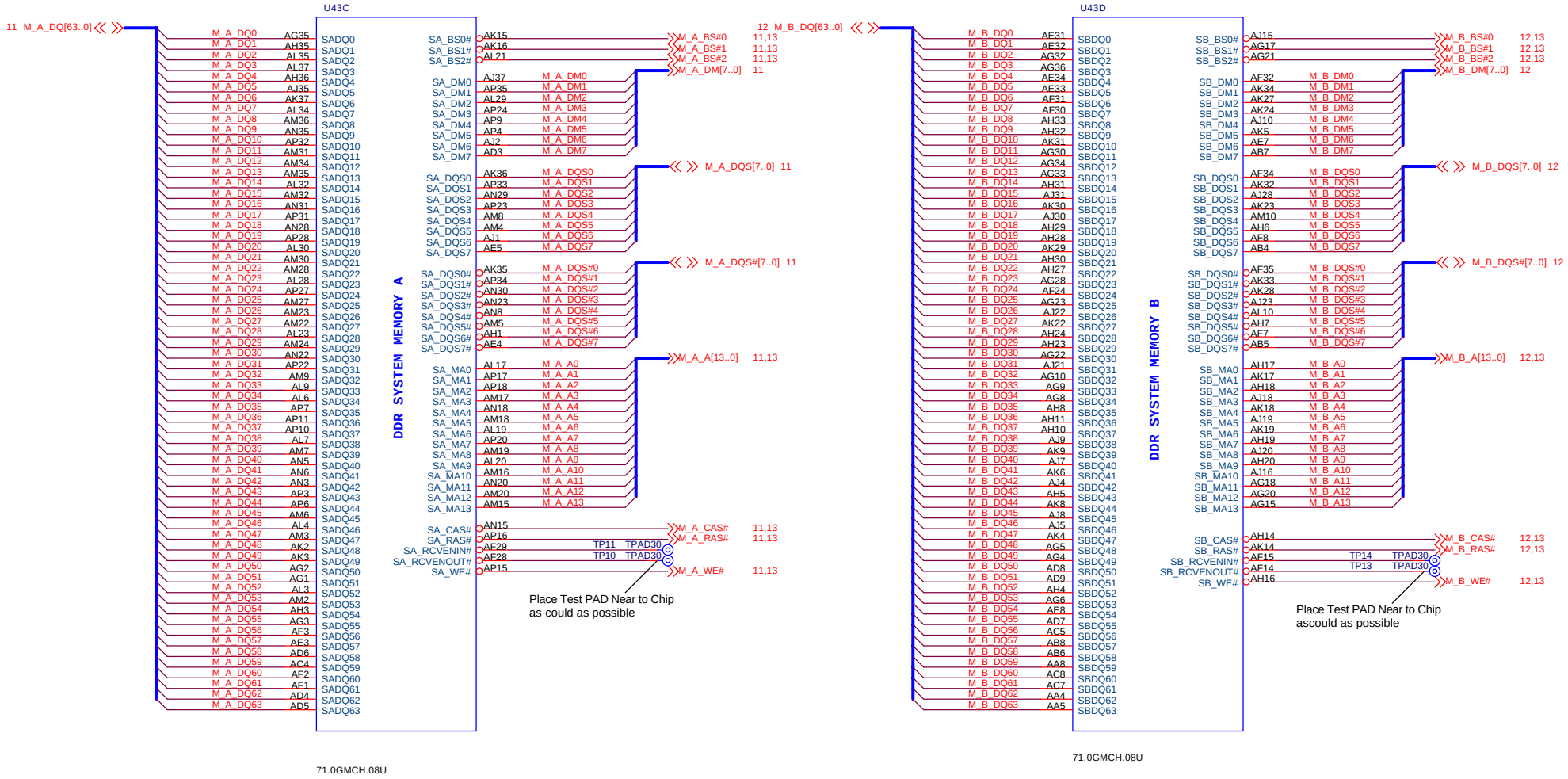

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Title: ***GMCH (3 of 5)***

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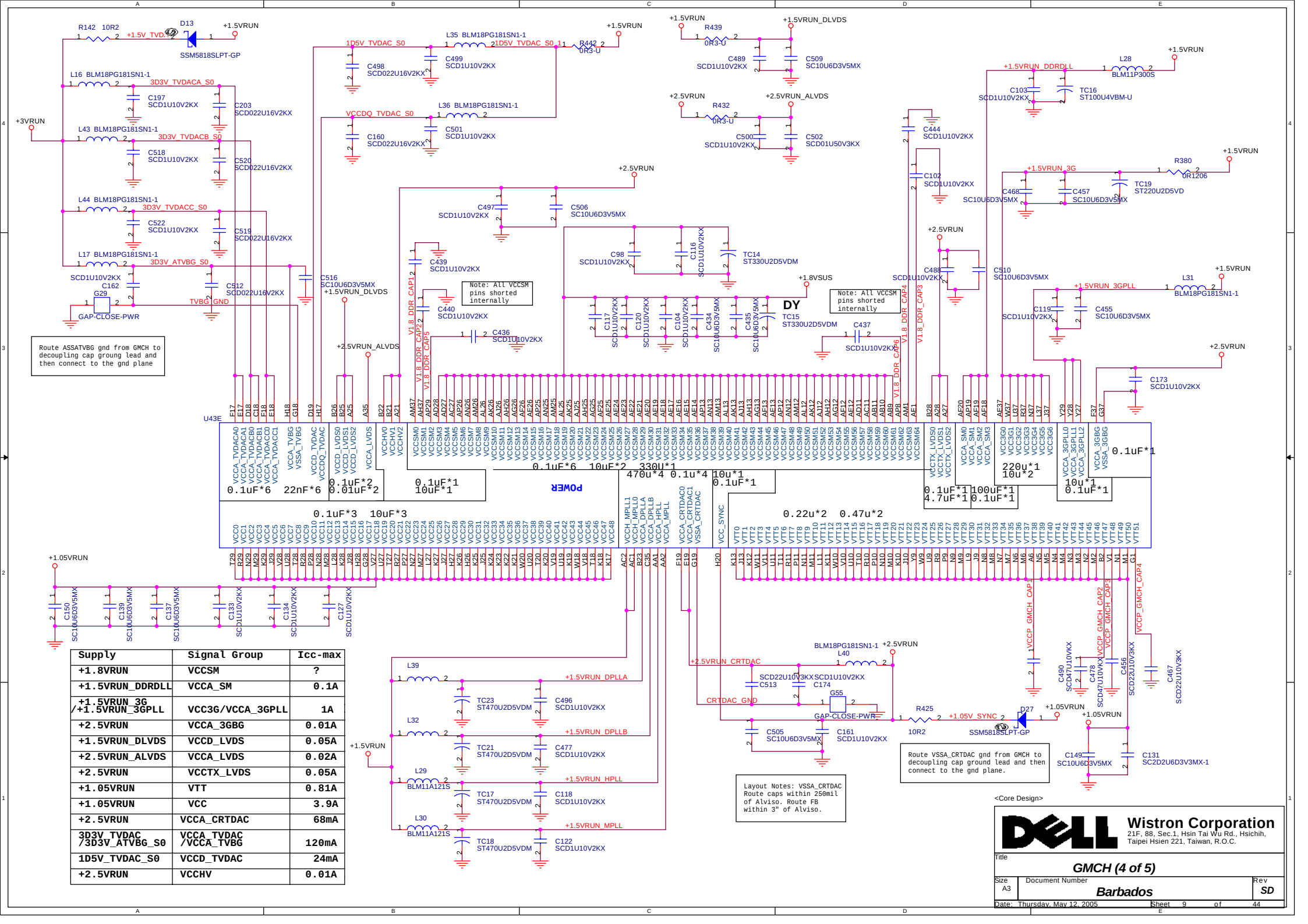

Supply	Signal Group	Icc-max
+1.8VRUN	VCCSM	?
+1.5VRUN_DDRDLL	VCCA_SM	0.1A
+1.5VRUN_3G /+1.5VRUN_3GPLL	VCC3G/VCCA_3GPLL	1A
+2.5VRUN	VCCA_3GBG	0.01A
+1.5VRUN_DLVDS	VCCD_LVDS	0.05A
+2.5VRUN_ALVDS	VCCA_LVDS	0.02A
+2.5VRUN	VCCTX_LVDS	0.05A
+1.05VRUN	VTT	0.81A
+1.05VRUN	VCC	3.9A
+2.5VRUN	VCCA_CRTDAC	68mA
3D3V_TVDAC /3D3V_ATVBG_S0	VCCA_TVDAC /VCCA_TVBG	120mA
1D5V_TVDAC_S0	VCCD_TVDAC	24mA
+2.5VRUN	VCCHV	0.01A

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<Core Design>
Title: GMCH (4 of 5)
Size: A3
Document Number: Barbados
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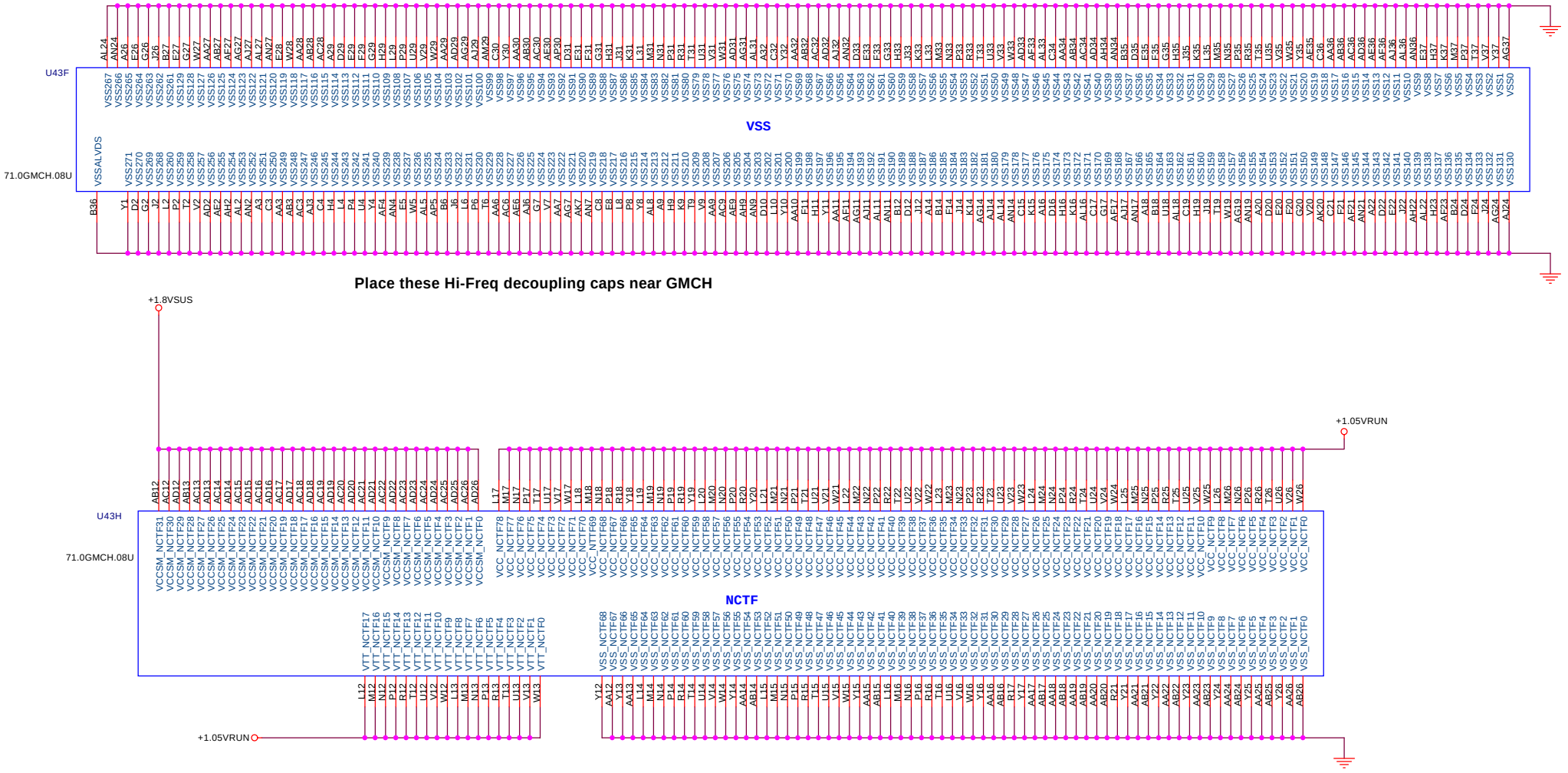
Date: Thursday, May 12, 2005
Sheet 9 of 44



<Core Design>

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Title: *GMCH (5 of 5)*

Size: A3 | Document Number: *Barbados* | Rev: *SD*

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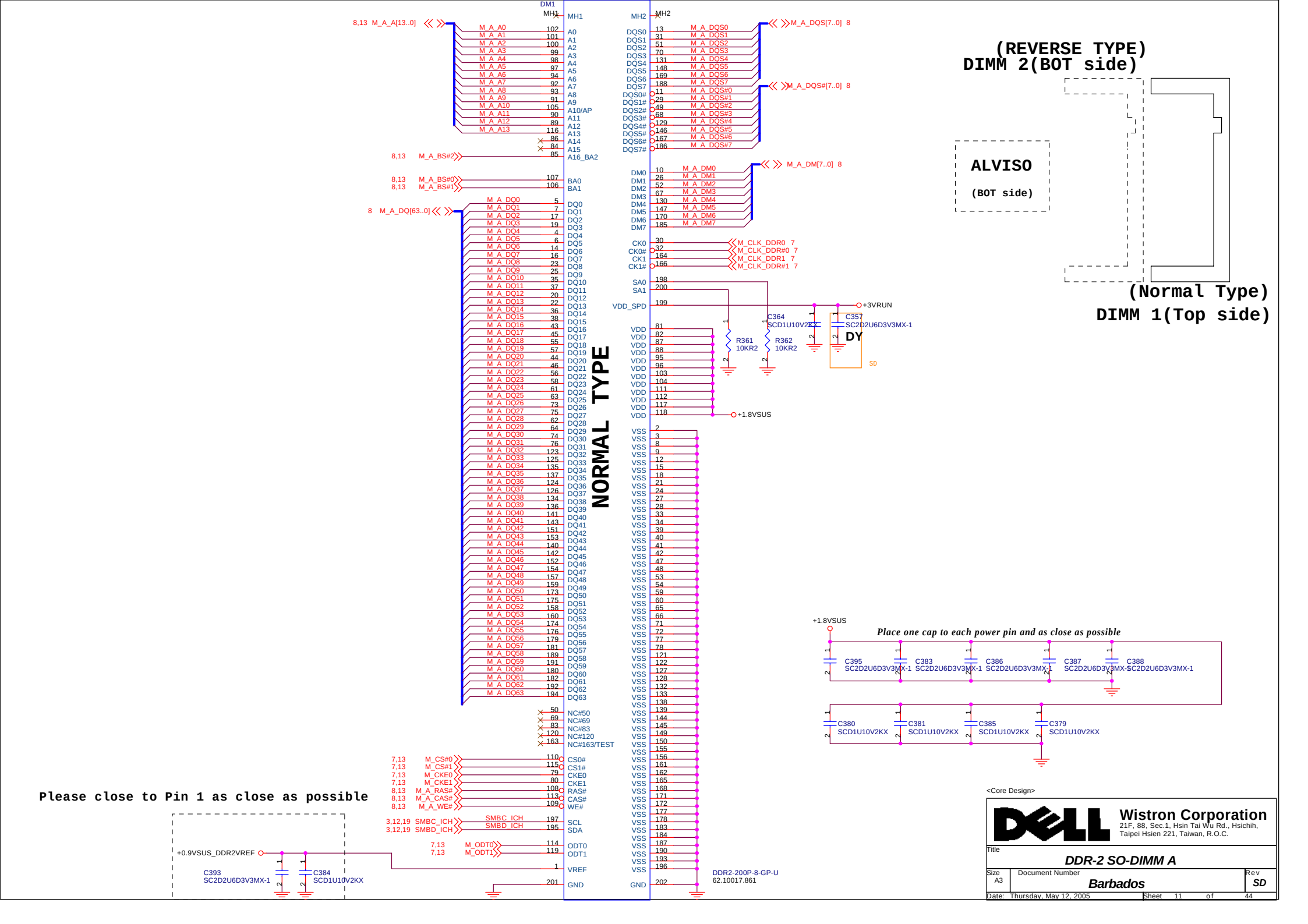
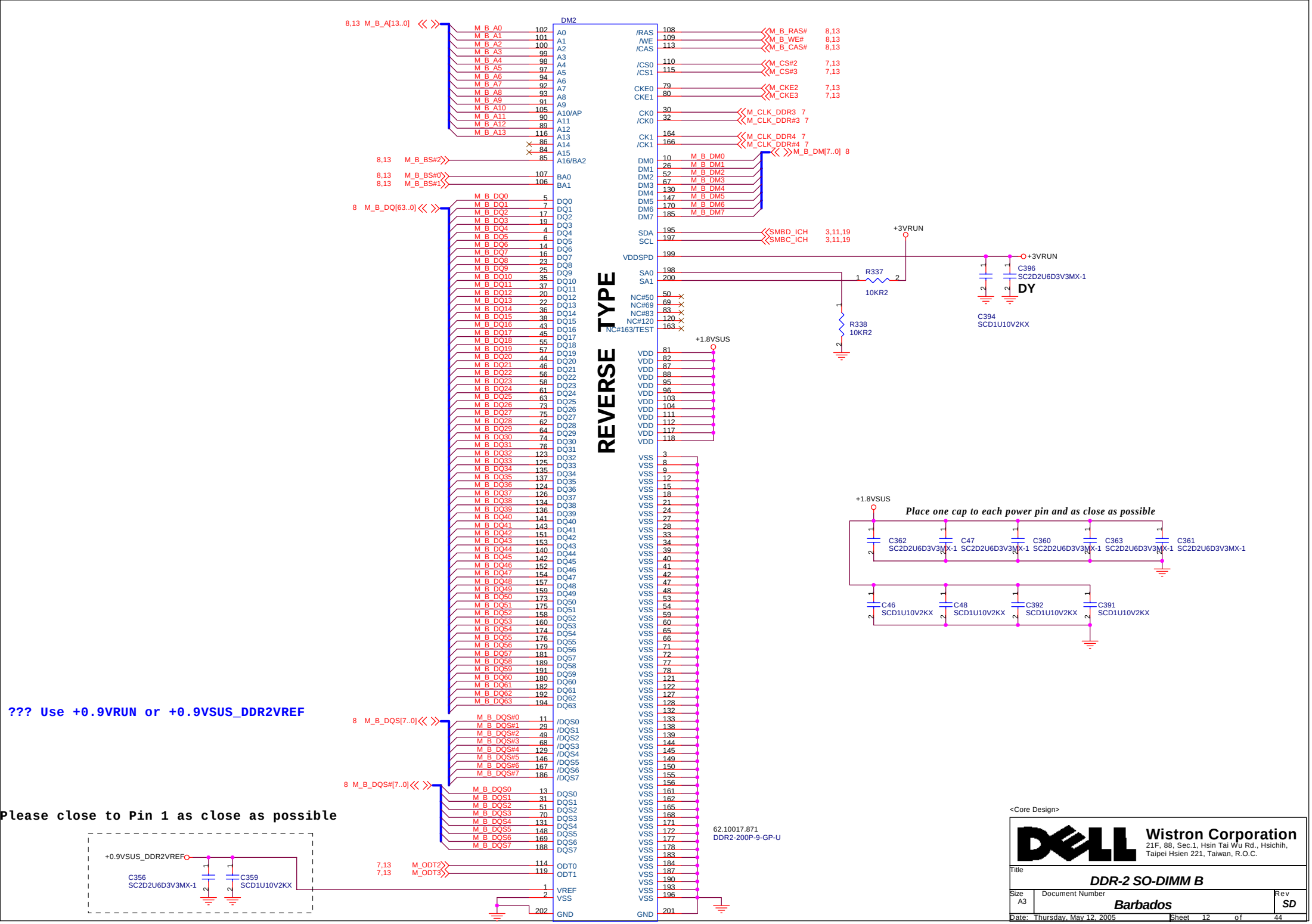

DM1
NORMAL TYPE
(REVERSE TYPE)
DIMM 2(BOT side)
ALVISO
(BOT side)
(Normal Type)
DIMM 1(Top side)
Please close to Pin 1 as close as possible
Place one cap to each power pin and as close as possible
DY
SD
+3VRUN
+1.8VSUS
+0.9VSUS_DDR2VREF
DDR2-200P-8-GP-U
62.10017.861
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR-2 SO-DIMM A
Size
A3
Document Number
Barbados
Rev
SD
Date: Thursday, May 12, 2005
Sheet 11 of 44


DM2
REVERSE TYPE
8,13 M_B_A[13..0]
M_B_A0 102
M_B_A1 101
M_B_A2 100
M_B_A3 99
M_B_A4 98
M_B_A5 97
M_B_A6 94
M_B_A7 92
M_B_A8 93
M_B_A9 91
M_B_A10 105
M_B_A11 90
M_B_A12 89
M_B_A13 116
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2
8,13 M_B_BS#2 85
8,13 M_B_BS#0 107
8,13 M_B_BS#1 106
BA0 BA1
8 M_B_DQ[63..0]
M_B_DQ0 5
M_B_DQ1 7
M_B_DQ2 17
M_B_DQ3 19
M_B_DQ4 4
M_B_DQ5 6
M_B_DQ6 14
M_B_DQ7 16
M_B_DQ8 23
M_B_DQ9 25
M_B_DQ10 35
M_B_DQ11 37
M_B_DQ12 20
M_B_DQ13 22
M_B_DQ14 36
M_B_DQ15 38
M_B_DQ16 43
M_B_DQ17 45
M_B_DQ18 55
M_B_DQ19 57
M_B_DQ20 44
M_B_DQ21 46
M_B_DQ22 56
M_B_DQ23 58
M_B_DQ24 61
M_B_DQ25 63
M_B_DQ26 73
M_B_DQ27 75
M_B_DQ28 62
M_B_DQ29 64
M_B_DQ30 74
M_B_DQ31 76
M_B_DQ32 123
M_B_DQ33 125
M_B_DQ34 135
M_B_DQ35 137
M_B_DQ36 124
M_B_DQ37 126
M_B_DQ38 134
M_B_DQ39 136
M_B_DQ40 141
M_B_DQ41 143
M_B_DQ42 151
M_B_DQ43 153
M_B_DQ44 140
M_B_DQ45 142
M_B_DQ46 152
M_B_DQ47 154
M_B_DQ48 157
M_B_DQ49 159
M_B_DQ50 173
M_B_DQ51 175
M_B_DQ52 158
M_B_DQ53 160
M_B_DQ54 174
M_B_DQ55 176
M_B_DQ56 179
M_B_DQ57 181
M_B_DQ58 189
M_B_DQ59 191
M_B_DQ60 180
M_B_DQ61 182
M_B_DQ62 192
M_B_DQ63 194
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63
8 M_B_DQS[7..0]
M_B_DQS#0 11
M_B_DQS#1 29
M_B_DQS#2 49
M_B_DQS#3 68
M_B_DQS#4 129
M_B_DQS#5 146
M_B_DQS#6 167
M_B_DQS#7 186
/DQS0 /DQS1 /DQS2 /DQS3 /DQS4 /DQS5 /DQS6 /DQS7
8 M_B_DQS#[7..0]
M_B_DQS0 13
M_B_DQS1 31
M_B_DQS2 51
M_B_DQS3 70
M_B_DQS4 131
M_B_DQS5 148
M_B_DQS6 169
M_B_DQS7 188
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
7,13 M_ODT2 114
7,13 M_ODT3 119
ODT0 ODT1
VREF 1
VSS 2
GND 202
/RAS 108
/WE 109
/CAS 113
M_B_RAS# 8,13
M_B_WE# 8,13
M_B_CAS# 8,13
/CS0 110
/CS1 115
M_CS#2 7,13
M_CS#3 7,13
CKE0 79
CKE1 80
M_CKE2 7,13
M_CKE3 7,13
CK0 30
/CK0 32
M_CLK_DDR3 7
M_CLK_DDR#3 7
CK1 164
/CK1 166
M_CLK_DDR4 7
M_CLK_DDR#4 7
M_B_DM[7..0] 8
DM0 10 M_B_DM0
DM1 26 M_B_DM1
DM2 52 M_B_DM2
DM3 67 M_B_DM3
DM4 130 M_B_DM4
DM5 147 M_B_DM5
DM6 170 M_B_DM6
DM7 185 M_B_DM7
SDA 195
SCL 197
SMBD_ICH 3,11,19
SMBC_ICH 3,11,19
VDDSPD 199
SA0 198
SA1 200
NC#50 50
NC#69 69
NC#83 83
NC#120 120
NC#163/TEST 163
+1.8VSUS
VDD 81 82 87 88 95 96 103 104 111 112 117 118
VSS 3 8 9 12 15 18 21 24 27 28 33 34 39 40 41 42 47 48 53 54 59 60 65 66 71 72 77 78 121 122 127 128 132 133 138 139 144 145 149 150 155 156 161 162 165 168 171 172 177 178 183 184 187 190 193 196 201
GND
62.10017.871
DDR2-200P-9-GP-U
+3VRUN
R337 10KR2
R338 10KR2
C396 SC2D2U6D3V3MX-1
DY
C394 SCD1U10V2KX
+1.8VSUS
Place one cap to each power pin and as close as possible
C362 SC2D2U6D3V3MX-1
C47 SC2D2U6D3V3MX-1
C360 SC2D2U6D3V3MX-1
C363 SC2D2U6D3V3MX-1
C361 SC2D2U6D3V3MX-1
C46 SCD1U10V2KX
C48 SCD1U10V2KX
C392 SCD1U10V2KX
C391 SCD1U10V2KX
??? Use +0.9VRUN or +0.9VSUS_DDR2VREF
Please close to Pin 1 as close as possible
+0.9VSUS_DDR2VREF
C356 SC2D2U6D3V3MX-1
C359 SCD1U10V2KX
<Core Design>
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR-2 SO-DIMM B
Size A3
Document Number
Barbados
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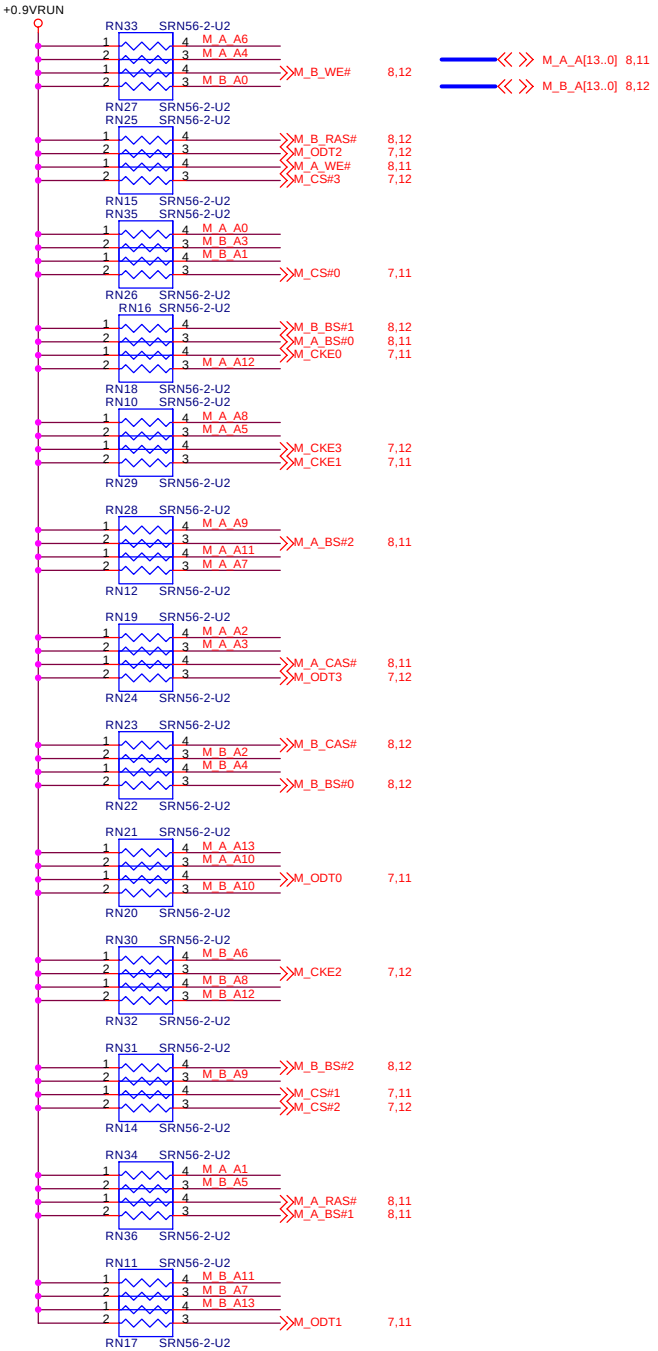
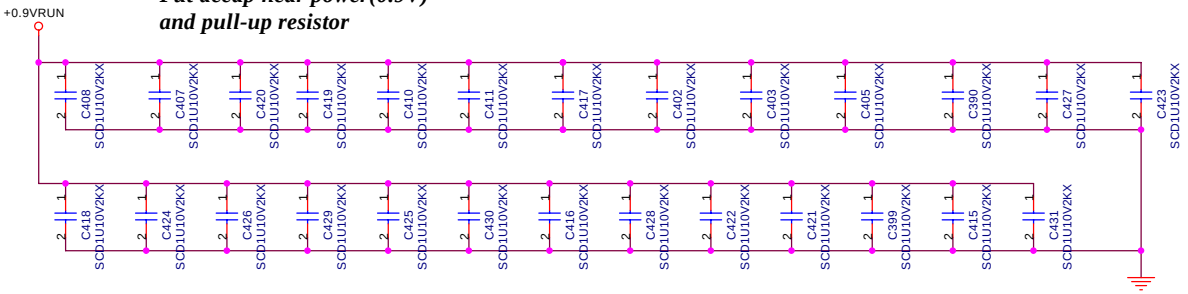
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



<Core Design>

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Title: ***DDR-2 TERMINATION / STRAPS***

Size	Document Number	Rev
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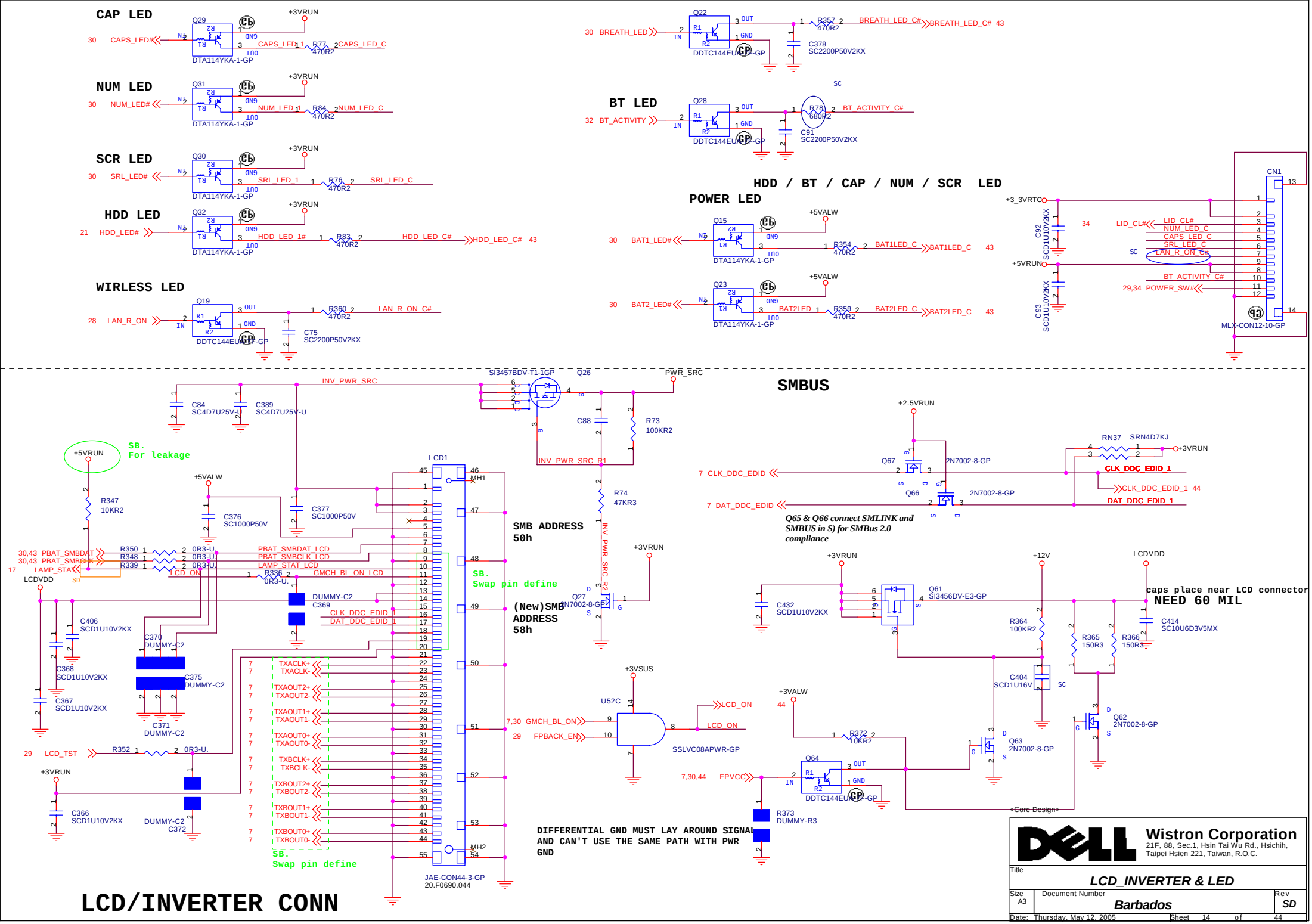
CAP LED
NUM LED
SCR LED
HDD LED
WIRLESS LED
BT LED
POWER LED
HDD / BT / CAP / NUM / SCR LED
SMBUS
SB. For leakage
SB. Swap pin define
SB. Swap pin define
SMB ADDRESS 50h
(New)SMB ADDRESS 58h
DIFFERENTIAL GND MUST LAY AROUND SIGNAL AND CAN'T USE THE SAME PATH WITH PWR GND
Q65 & Q66 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance
caps place near LCD connector NEED 60 MIL
<Core Design>
LCD/INVERTER CONN
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LCD_INVERTER & LED
Barbados
SD
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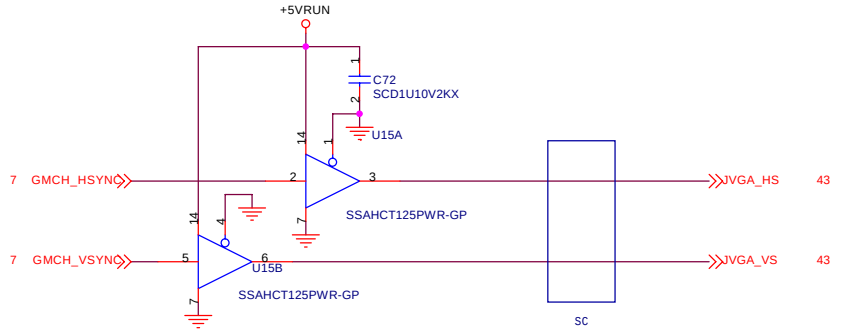
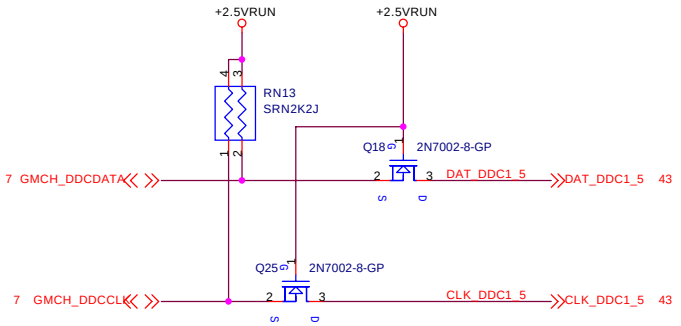
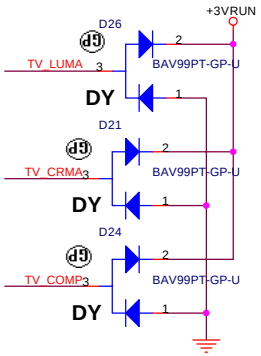
14
44



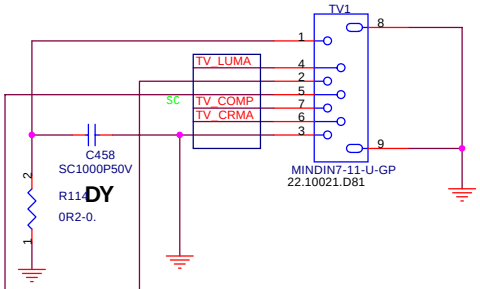
DDC_CLK & DATE LEVEL SHIFT

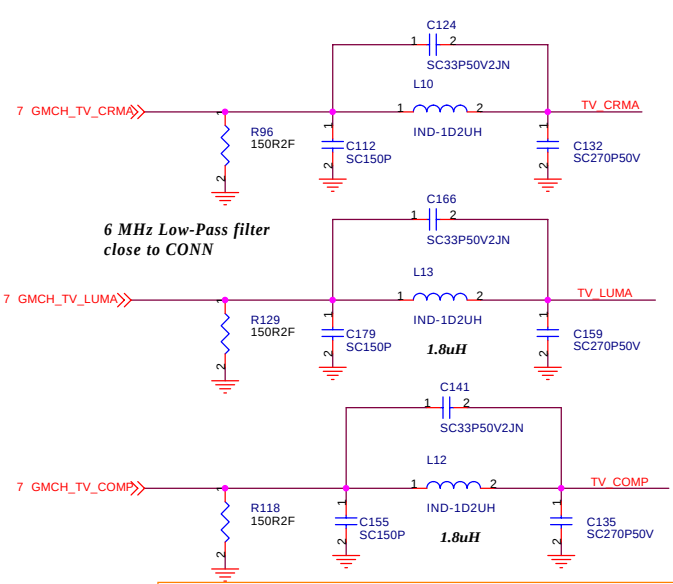


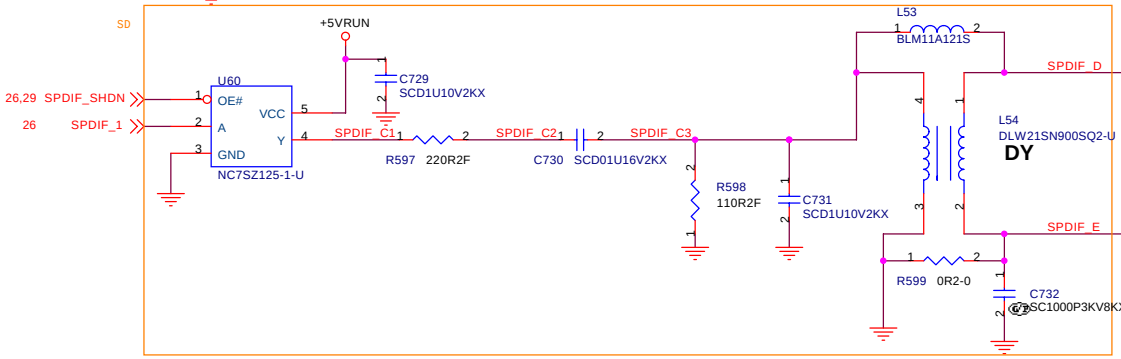
ESD Protection Diode



TVOUT CONN







<Core Design>

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Title	***TV CONN.***	
Size A3	Document Number ***Barbados***	Rev ***SD***
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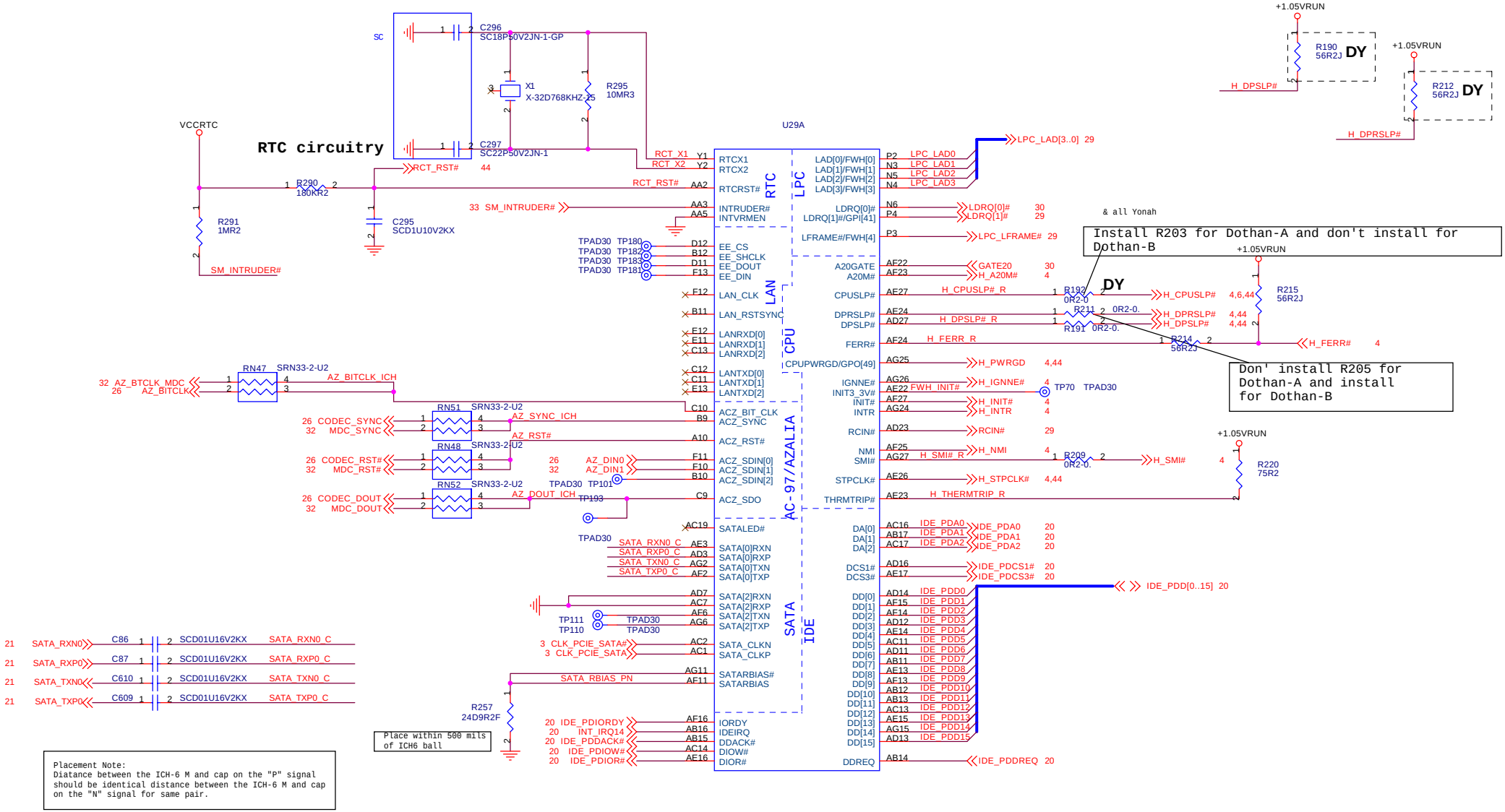

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Title: ICH6-M (1 of 4)

Size: A3 | Document Number: Barbados | Rev: SD

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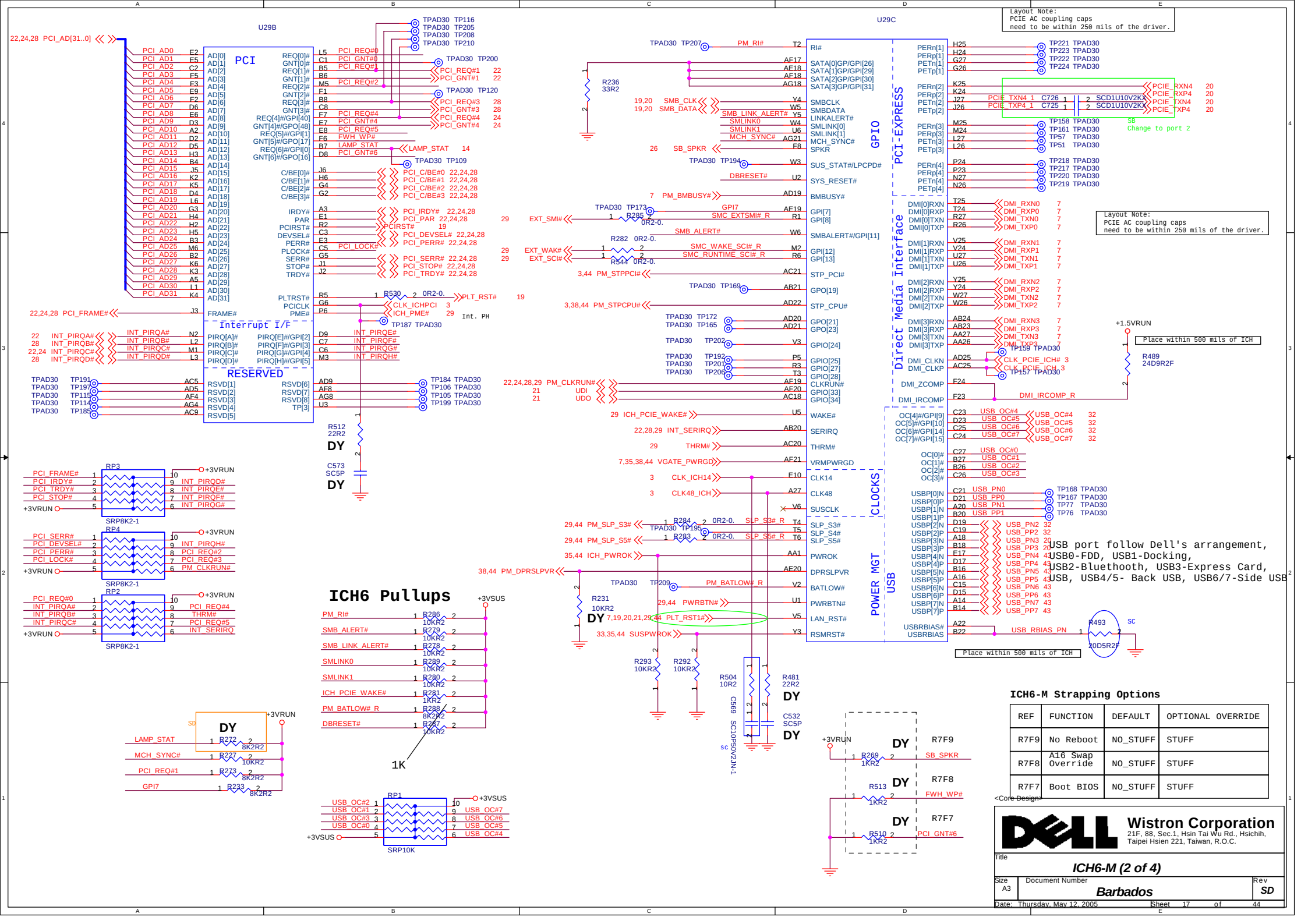
U29B
PCI
Interrupt I/F
RESERVED
U29C
GPIO
PCI-EXPRESS
Direct Media Interface
CLOCKS
USB
POWER MGT
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
Place within 500 mils of ICH
SB
Change to port 2
USB port follow Dell's arrangement,
USB0-FDD, USB1-Docking,
USB2-Bluethooth, USB3-Express Card,
USB, USB4/5- Back USB, USB6/7-Side USB
ICH6 Pullups
1K
SRP8K2-1
SRP8K2-1
SRP8K2-1
SRP10K
DY
ICH6-M Strapping Options
REF
FUNCTION
DEFAULT
OPTIONAL OVERRIDE
R7F9
No Reboot
NO_STUFF
STUFF
R7F8
A16 Swap Override
NO_STUFF
STUFF
R7F7
Boot BIOS
NO_STUFF
STUFF
<Core Design>
Wistron Corporation
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Title
ICH6-M (2 of 4)
Size
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Supply	Signal Group	Icc-max
V5REF_S0	V5REF	0.001A
V5REF_S5	V5REF_SUS	0.01A
+3VRUN	VCC3_3	0.19A
+3VRUN	VCCSUS3_3 /VCCLAN3_3	0.39A
+2.5VRUN	VCC2_5	0.01A
+1.5VRUN	VCC1_5	2.95A
+1.5VSUS	VCCSUS1_5 /VCCLAN1_5	0.27A
+1.05VRUN	V_CPU_IO	0.014A
VCCRTC	VCCRTC	5uA

ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

<Core Design>

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Title: ICH6-M (3 of 4)

Size: A3 | Document Number: Barbados | Rev: SD

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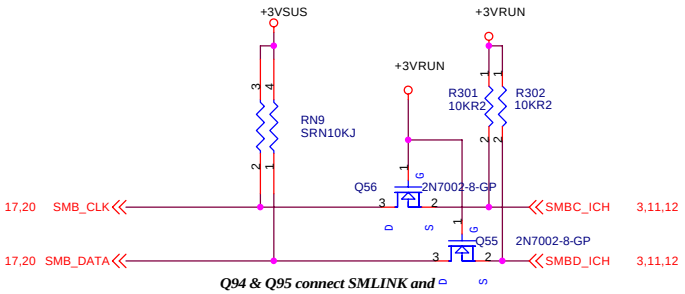
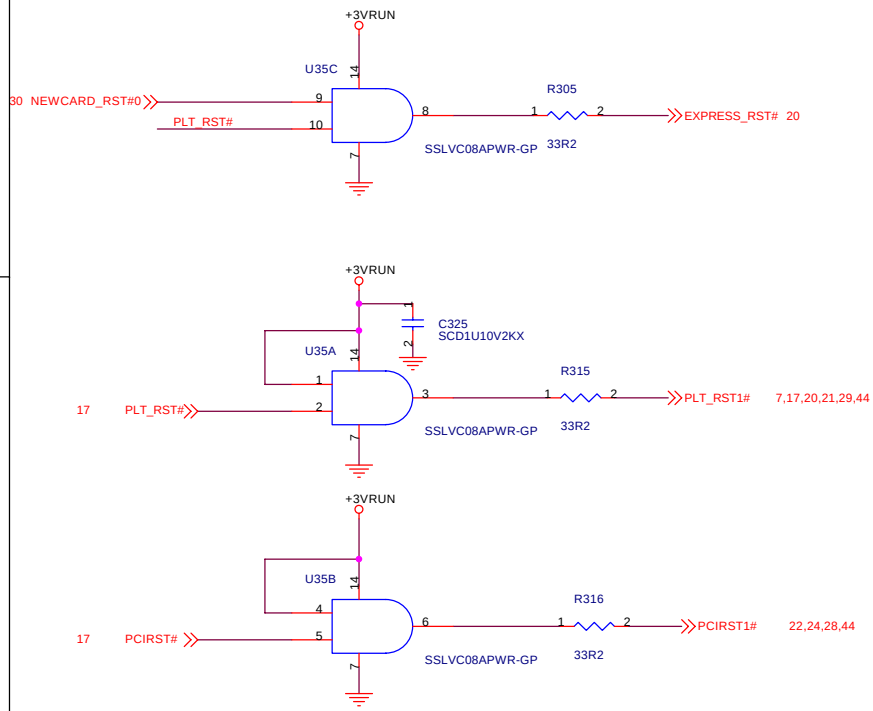
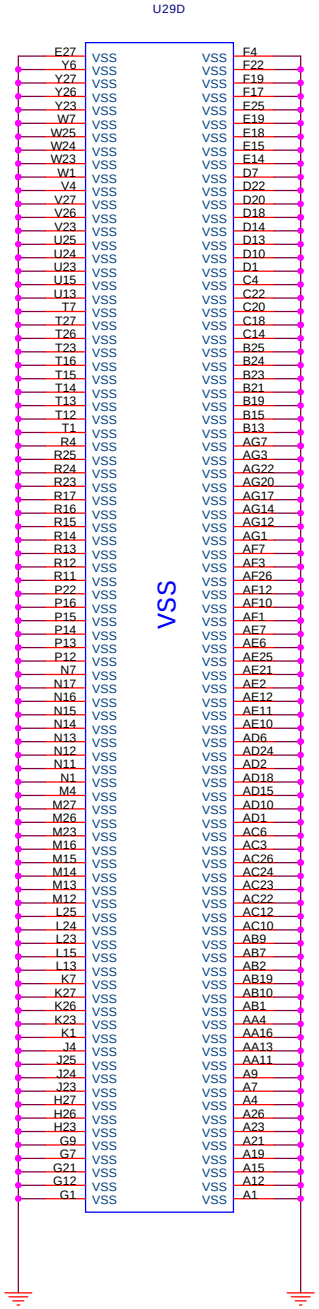
SMBUS



Q94 & Q95 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance





<Core Design>

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Title: *ICH6-M (4 of 4)*

Size: A3 | Document Number: *Barbados* | Rev: *SD*

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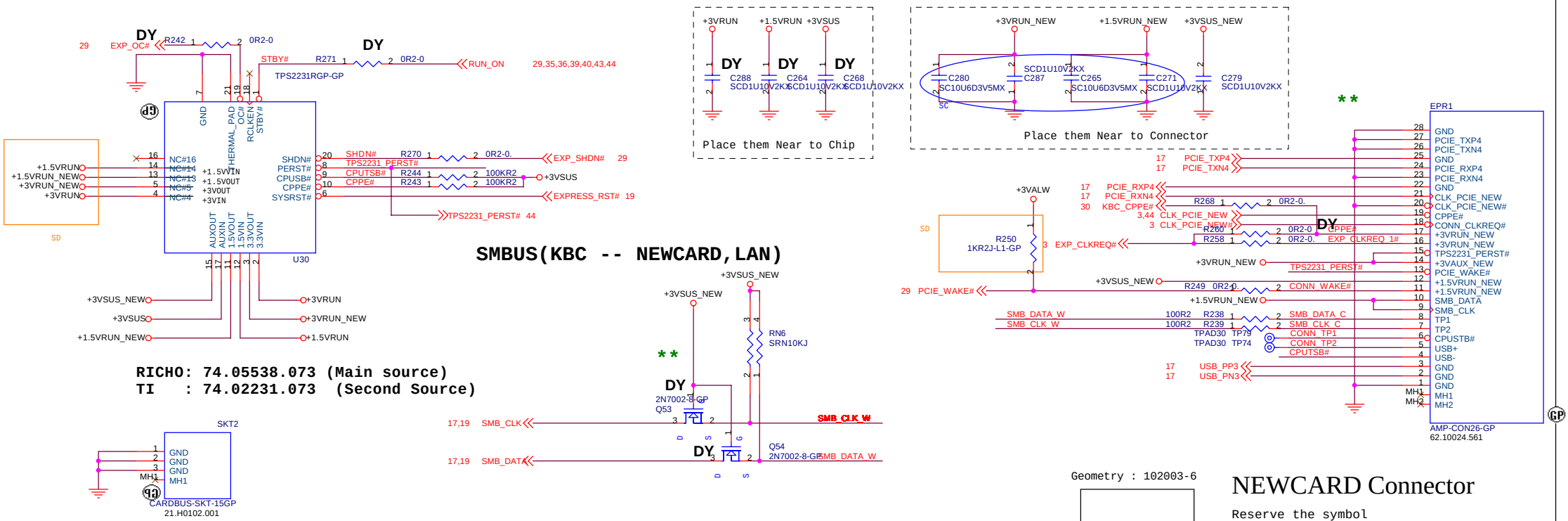

<Core Design>

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Title: **CDROM/NEWCARD**

Size	Document Number	Rev
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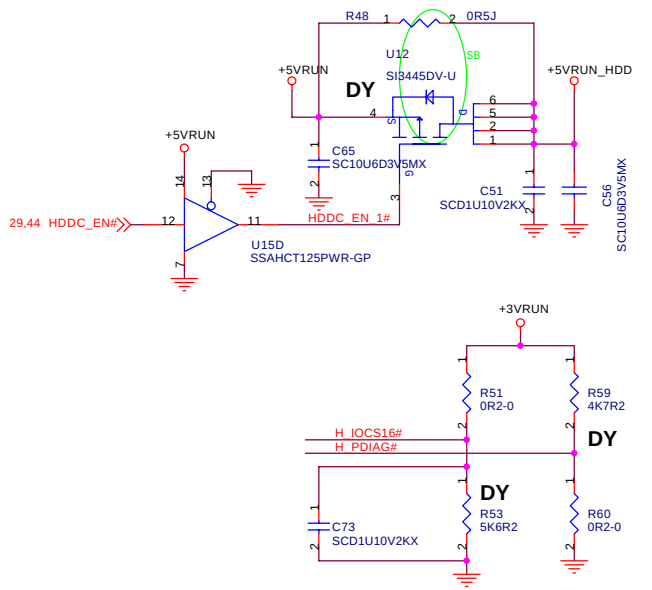
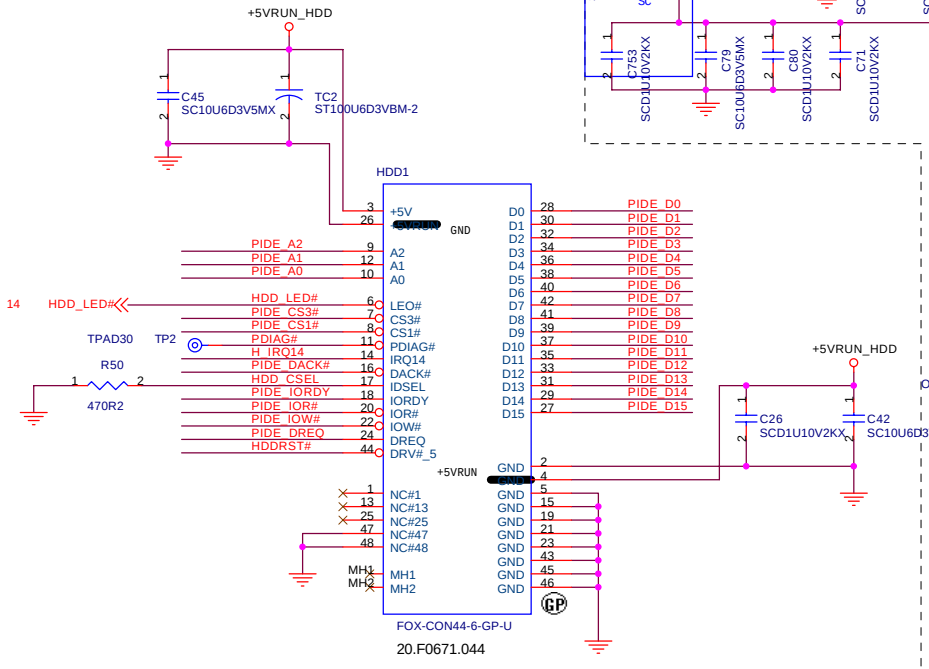
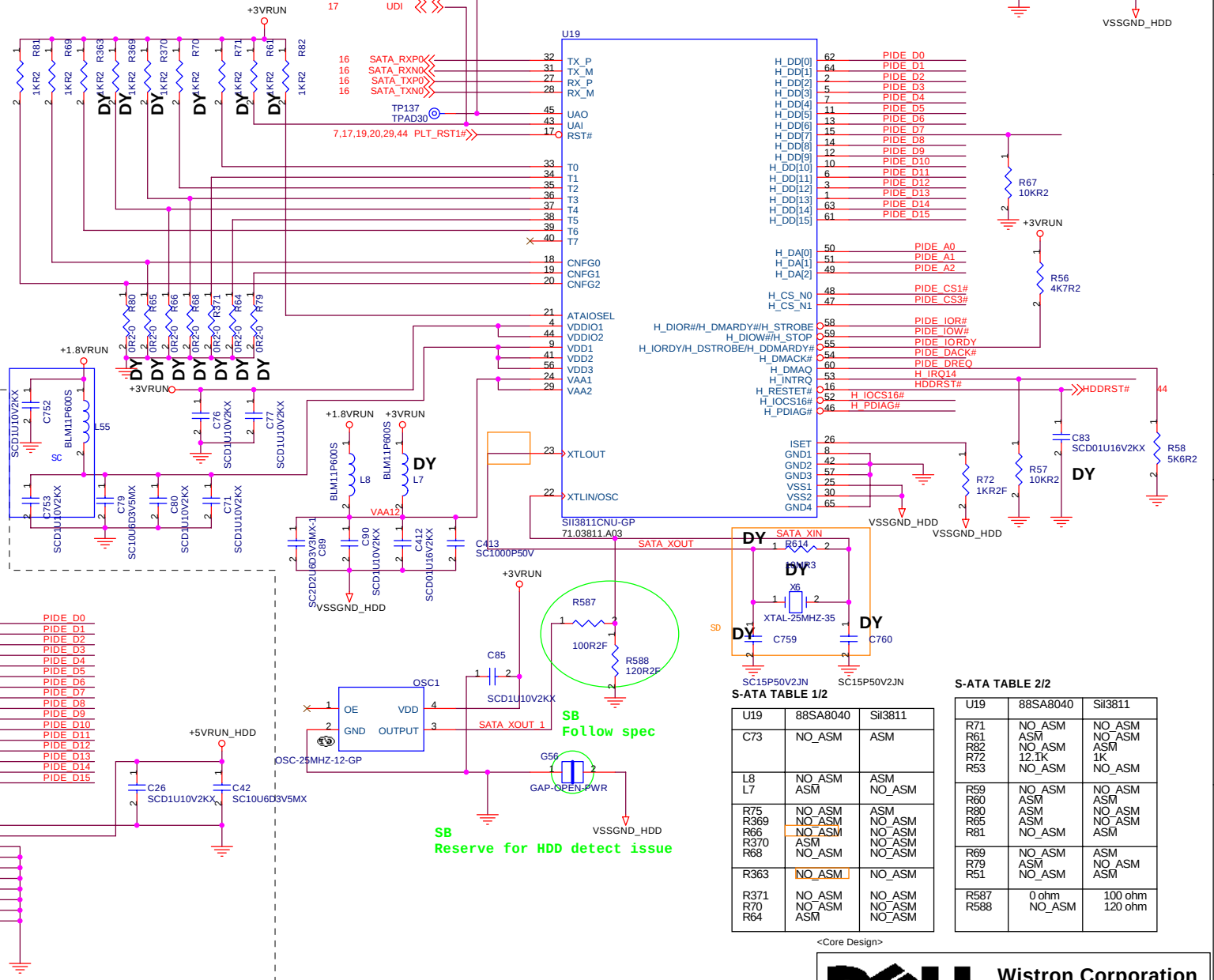
HDD power



HDD CONN





S-ATA TABLE 1/2

U19	88SA8040	SiI3811
C73	NO_ASM	ASM
L8 L7	NO_ASM ASM	ASM NO_ASM
R75 R369 R66 R370 R68	NO_ASM NO_ASM NO_ASM ASM NO_ASM	ASM NO_ASM NO_ASM NO_ASM NO_ASM
R363	NO_ASM	NO_ASM
R371 R70 R64	NO_ASM NO_ASM ASM	NO_ASM NO_ASM NO_ASM

S-ATA TABLE 2/2

U19	88SA8040	SiI3811
R71 R61 R82 R72 R53	NO_ASM ASM NO_ASM 12.1K NO_ASM	NO_ASM NO_ASM ASM 1K NO_ASM
R59 R60 R80 R65 R81	NO_ASM ASM NO_ASM ASM NO_ASM	NO_ASM ASM NO_ASM NO_ASM ASM
R69 R79 R51	NO_ASM ASM NO_ASM	ASM NO_ASM ASM
R587 R588	0 ohm NO_ASM	100 ohm 120 ohm

<Core Design>

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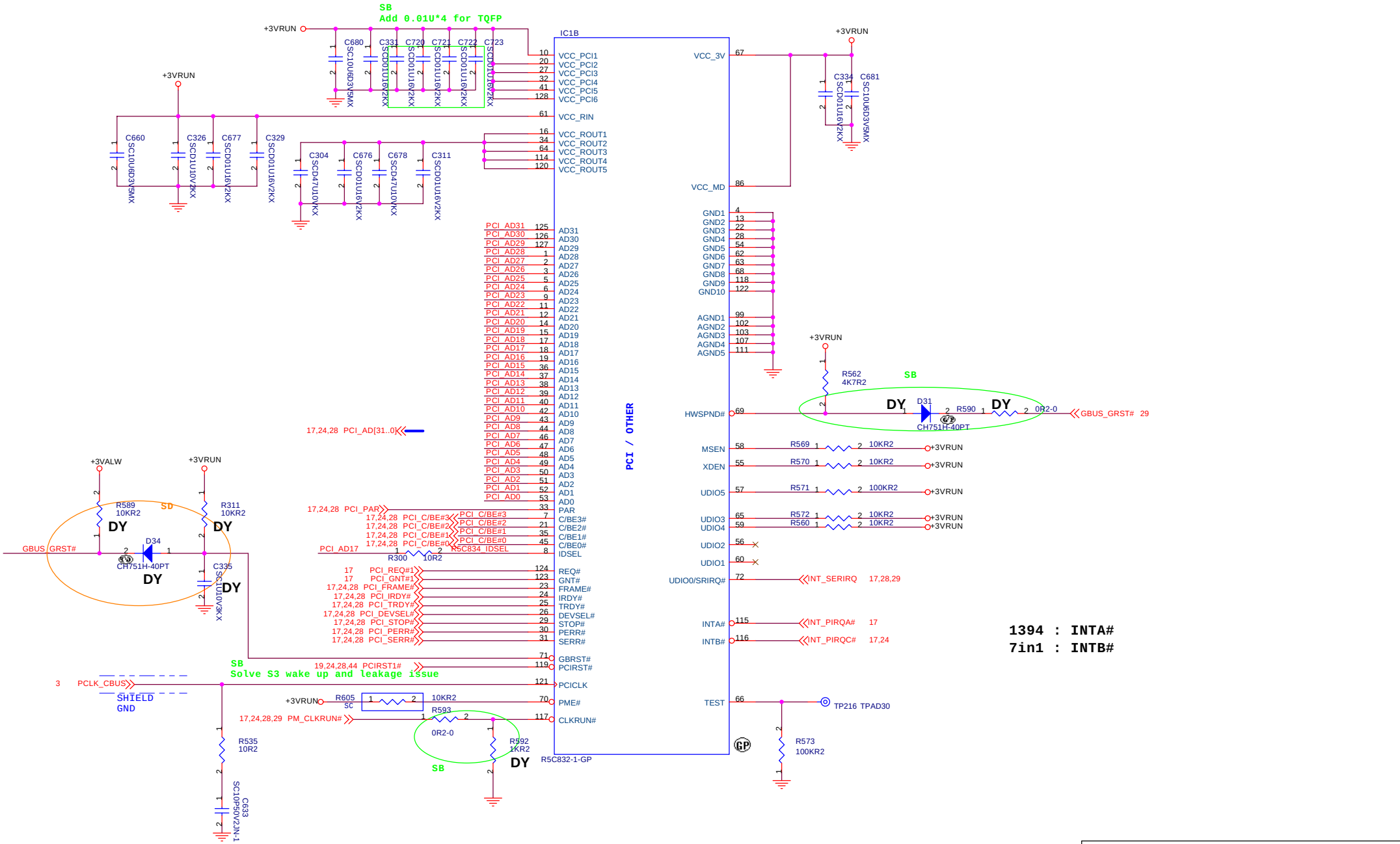
Title: SATA HDD/CD ROM

Size: A3 | Document Number: Barbados | Rev: SD

Date: Thursday, May 12, 2005 | Sheet 21 of 44



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: *R5C832_PCI(1/2)*			
Size: A3	Document Number: *Barbados*		Rev: *SD*
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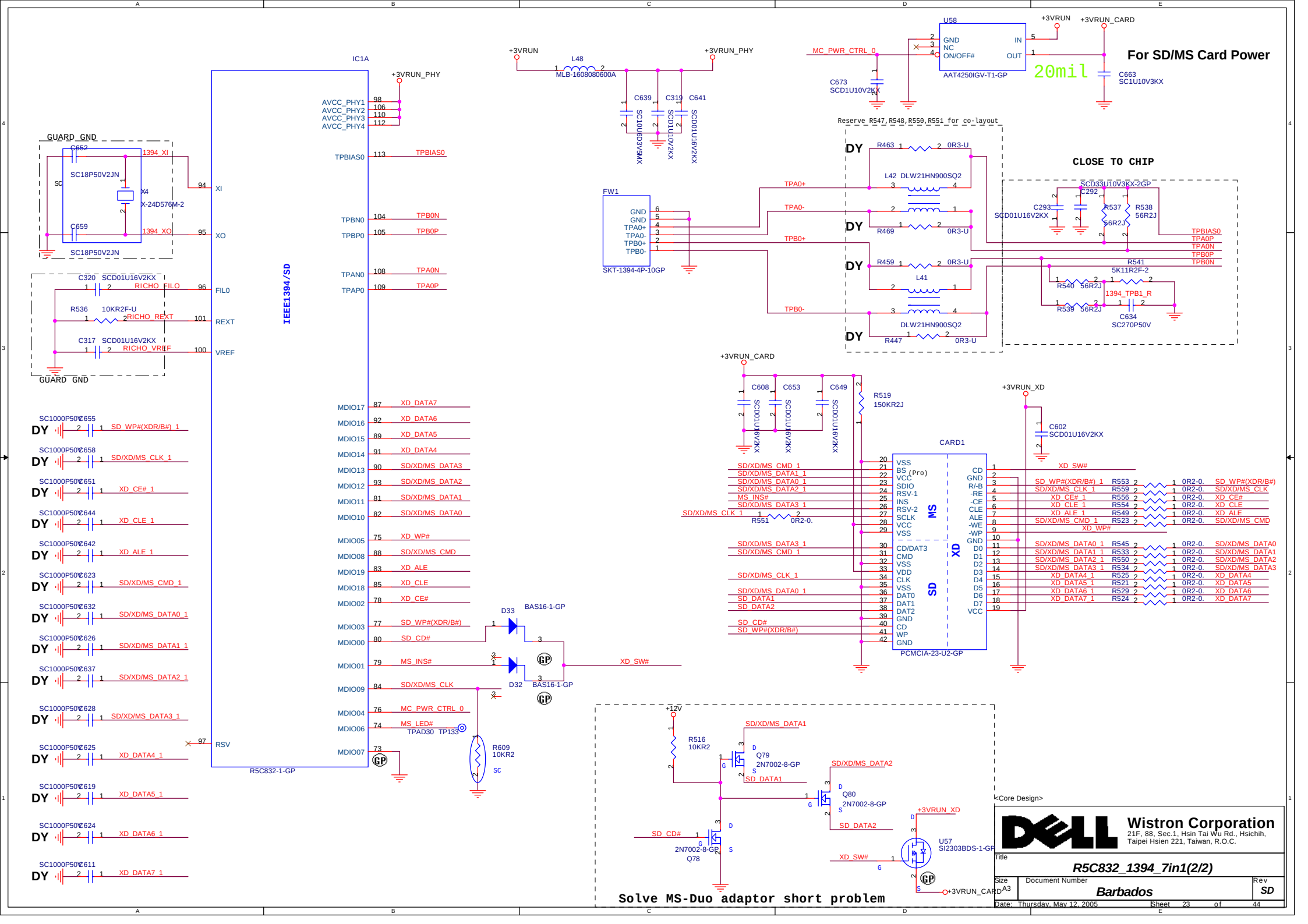
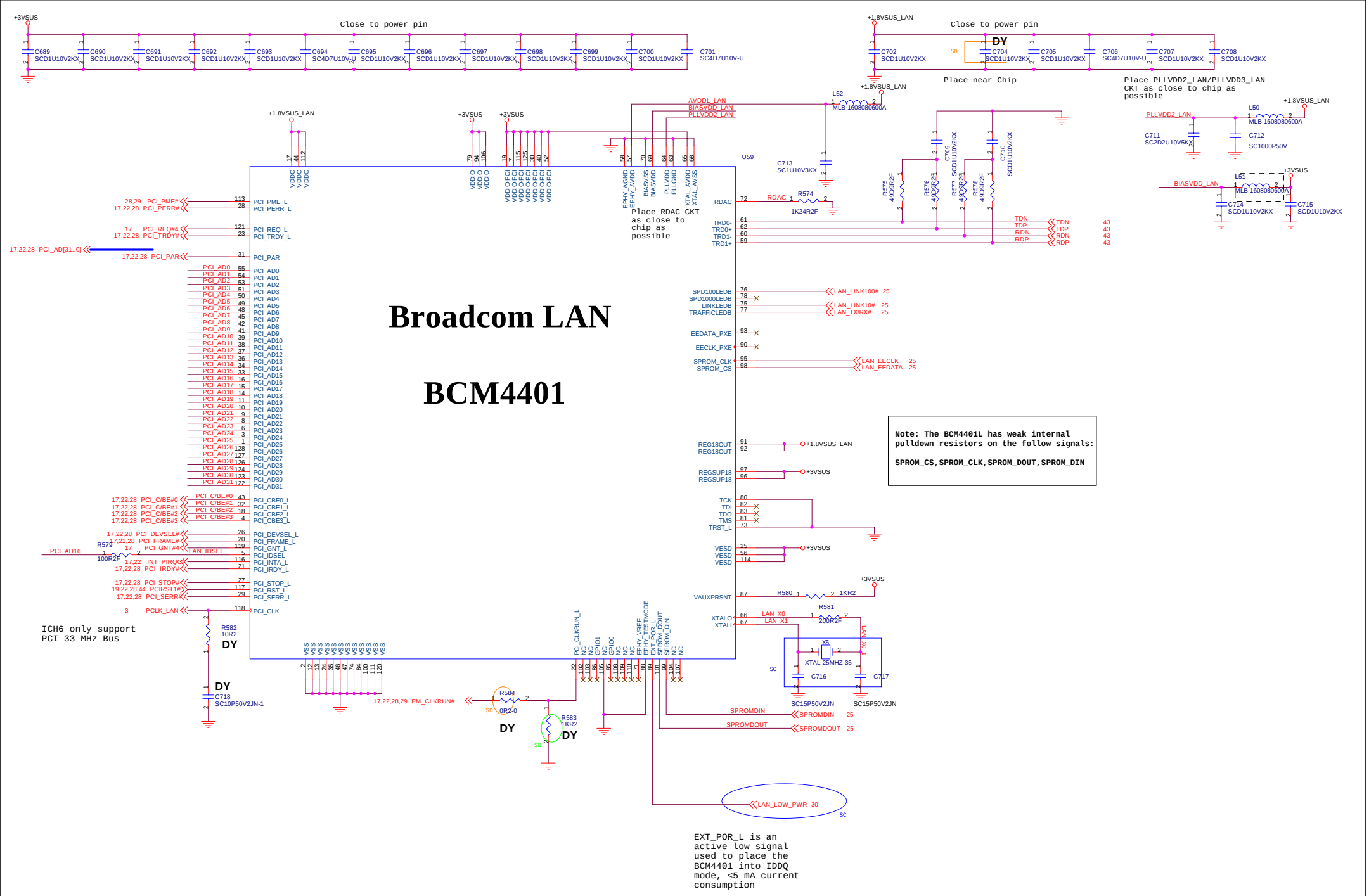

For SD/MS Card Power
CLOSE TO CHIP
Reserve R547,R548,R550,R551 for co-layout
IC1A
IEEE1394/SD
GUARD_GND
CARD1
PCMCIA-23-U2-GP
SKT-1394-4P-10GP
R5C832-1-GP
Solve MS-Duo adaptor short problem
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
R5C832_1394_7in1(2/2)
Barbados
Thursday, May 12, 2005



<Core Design>

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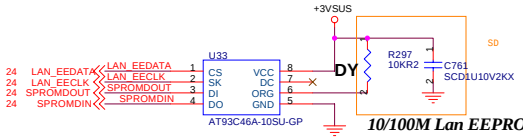
Title: BCM4401 10/100 LAN

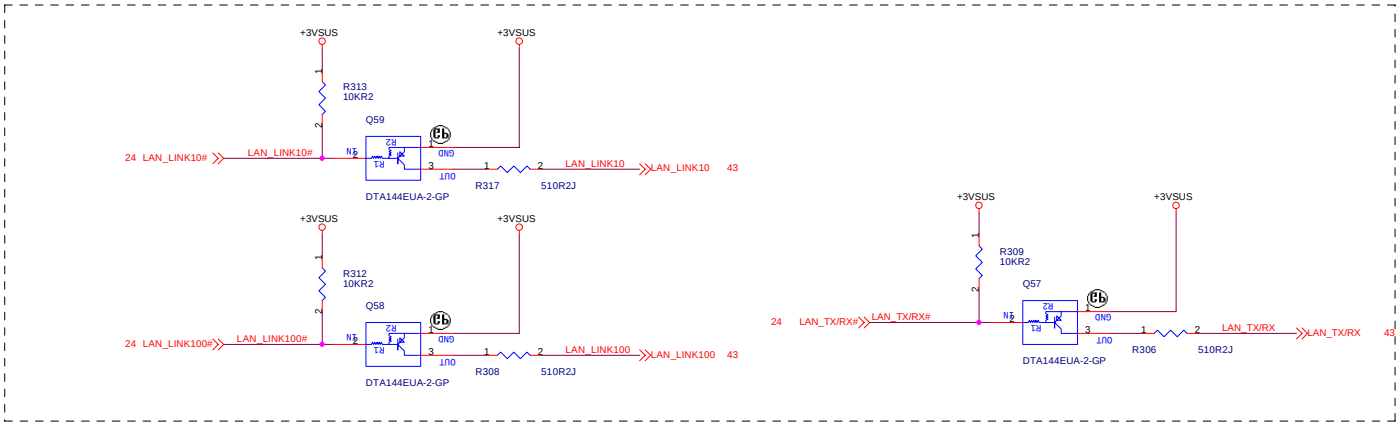
Size: Custom | Document Number: Barbados | Rev: SD

Date: Thursday, May 12, 2005 | Sheet 24 of 44



10/100M Lan EEPROM

Atmal: AT93C46-10SI "72.93C46.K01" (Main source)
ST : M93C46-W "72.93C46.E01" (2nd source)



<Core Design>

Wistron Corporation
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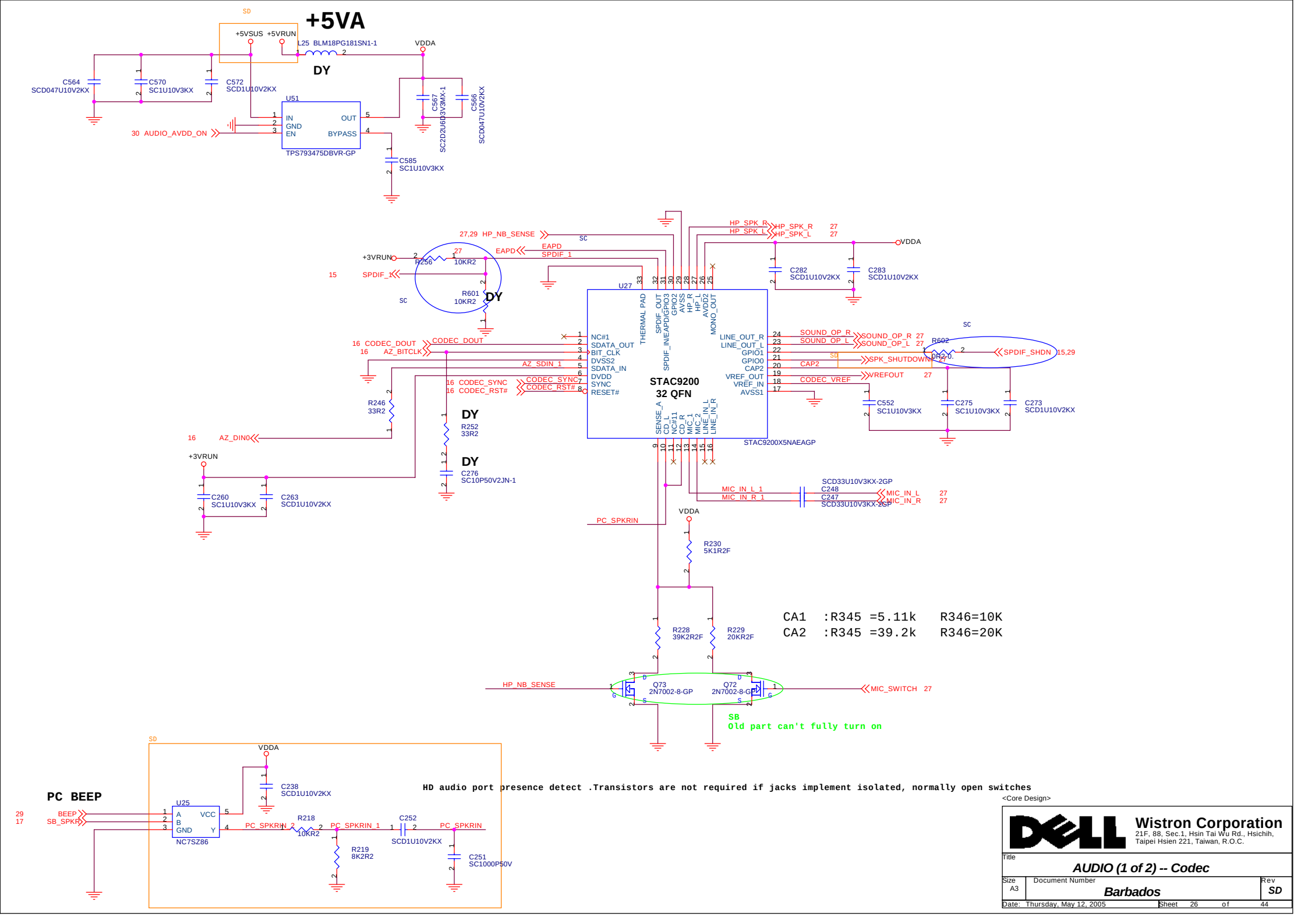
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN Transformer***

Size: Custom | Document Number: ***Barbados*** | Rev: ***SD***

Date: Thursday, May 12, 2005 | Sheet 25 of 44



<Core Design>

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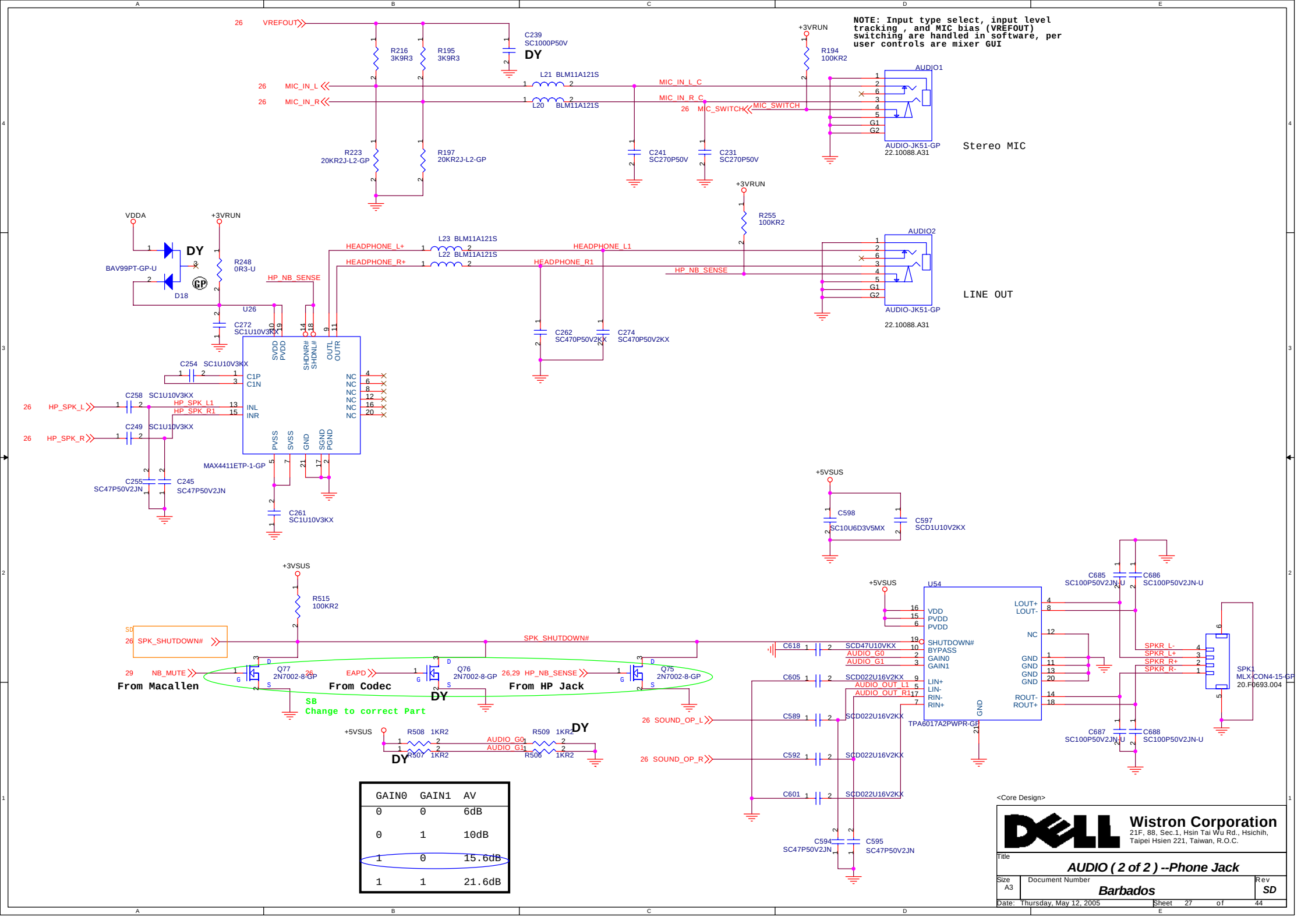
Title: ***AUDIO (1 of 2) -- Codec***

Size	Document Number	Rev
A3	***Barbados***	***SD***

Date: Thursday, May 12, 2005 Sheet 26 of 44


NOTE: Input type select, input level tracking , and MIC bias (VREFOUT) switching are handled in software, per user controls are mixer GUI
Stereo MIC
LINE OUT
From Macallen
From Codec
From HP Jack
SB
Change to correct Part
DY
GAIN0 GAIN1 AV
0 0 6dB
0 1 10dB
1 0 15.6dB
1 1 21.6dB
<Core Design>
Wistron Corporation
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Title
AUDIO (2 of 2) --Phone Jack
Size A3
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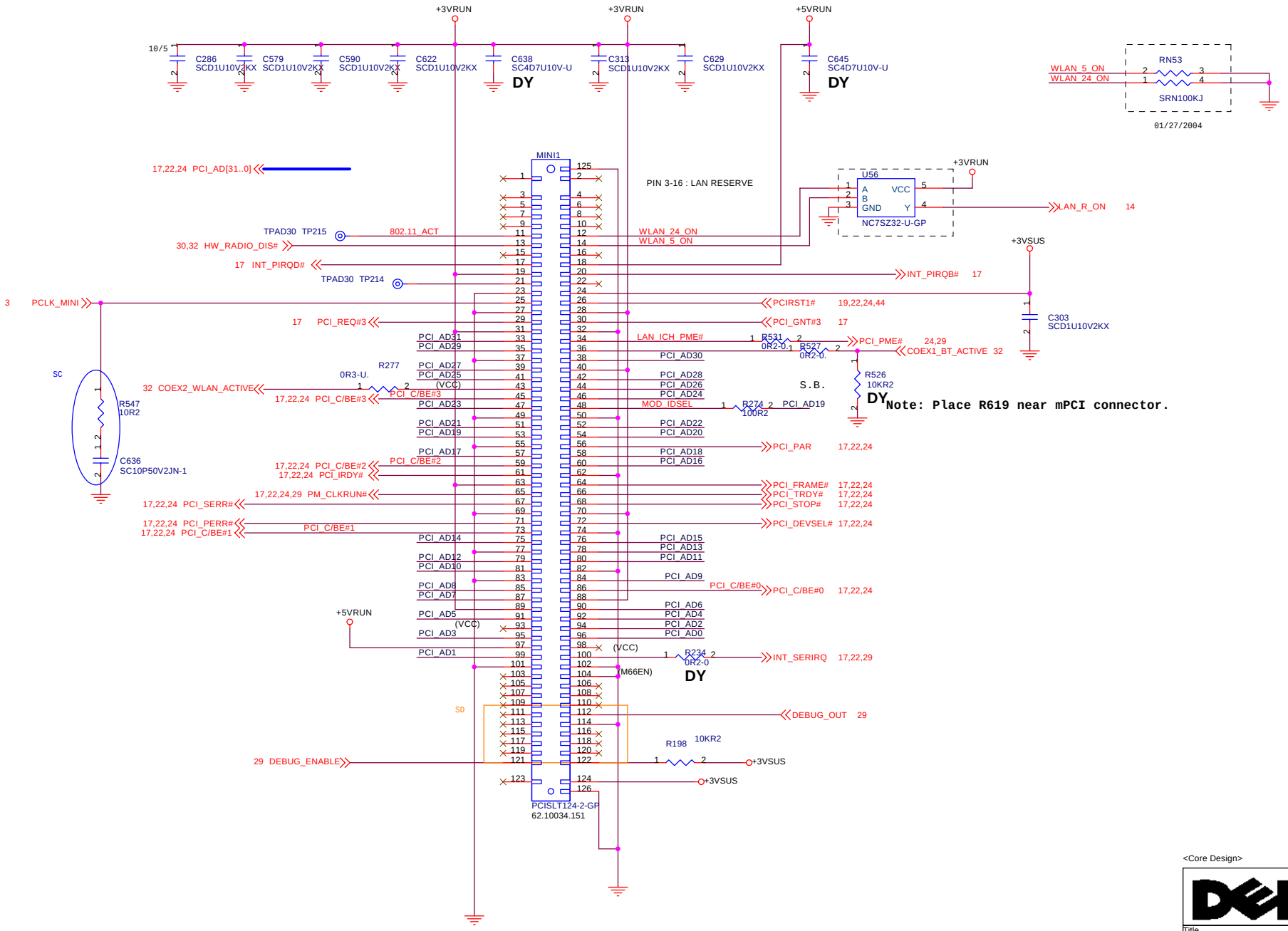
MINI PCI



<Core Design>

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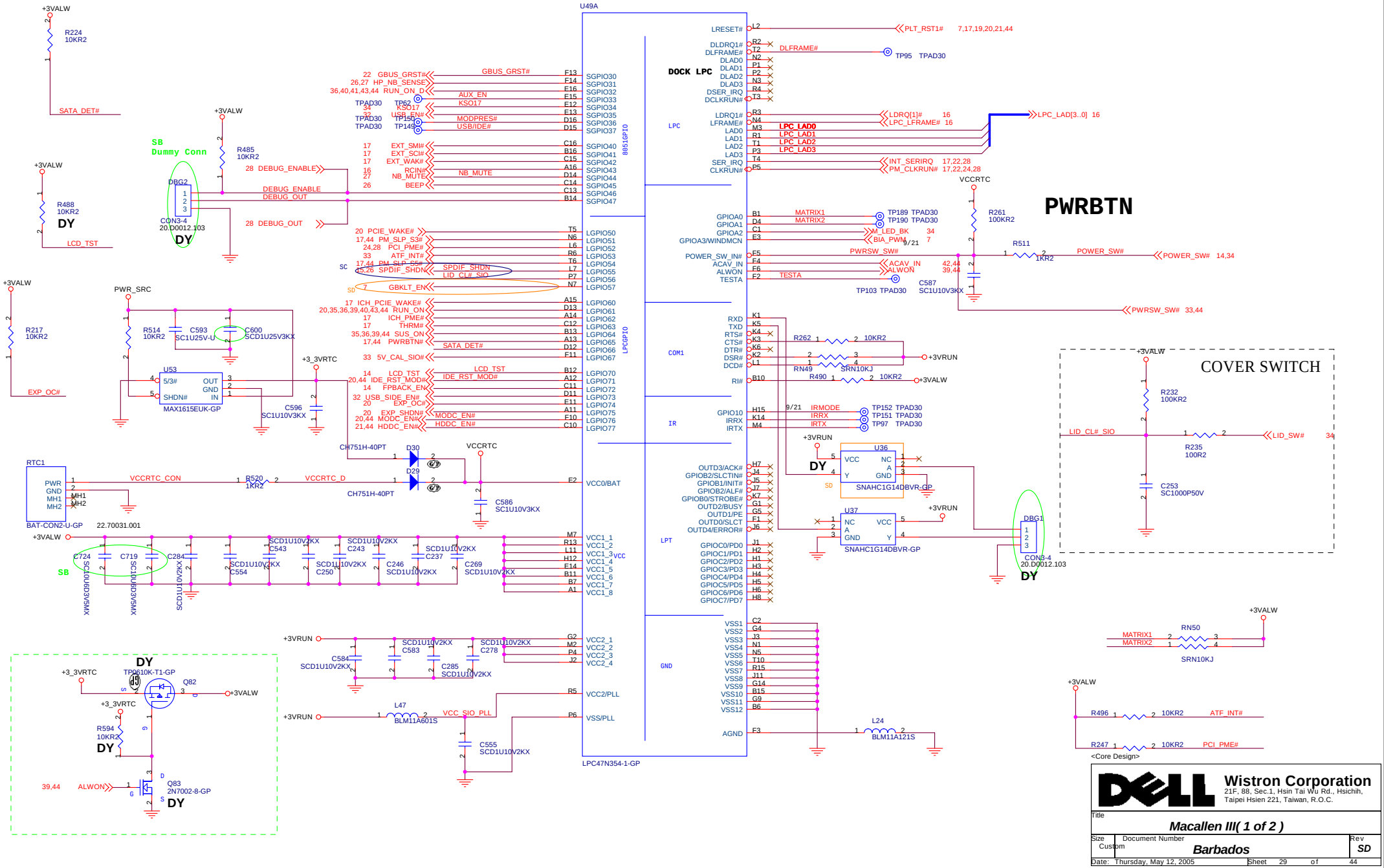
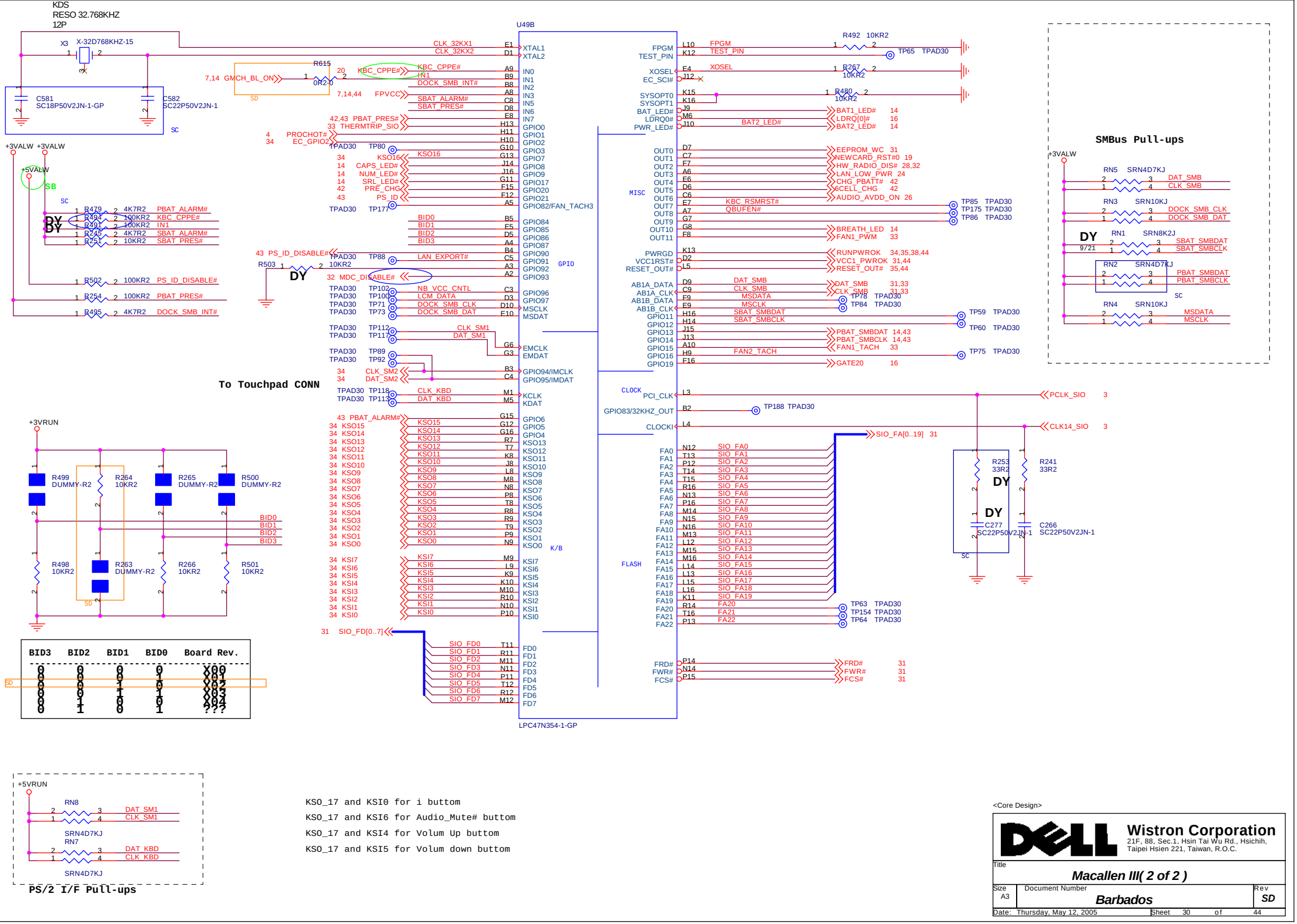
Title	***MINI-PCI***	
Size A3	Document Number ***Barbados***	Rev ***SD***
Date: Thursday, May 12, 2005	Sheet 28 of 44	



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*Macallen III(1 of 2)*
Size: Custom	Document Number: *Barbados*
Rev	*SD*
Date: Thursday, May 12, 2005	Sheet 29 of 44


KDS
RESO 32.768KHZ
12P
X3 X-32D768KHZ-15
C581 SC18P50V2JN-1-GP
C582 SC22P50V2JN-1
SC
+3VALW +3VALW
+5VALW
SB
SC
R479 4K7R2 PBAT_ALARM#
R494 100KR2 KBC_CPPE#
R491 100KR2 IN1
R245 4K7R2 SBAT_ALARM#
R251 10KR2 SBAT_PRES#
DY
R502 100KR2 PS_ID_DISABLE#
R254 100KR2 PBAT_PRES#
R495 4K7R2 DOCK_SMB_INT#
U49B
CLK_32KX1
CLK_32KX2
R615 0R2-0
7,14 GMCH_BL_ON
KBC_CPPE#
7,14,44 FPVCC
SBAT_ALARM#
SBAT_PRES#
42,43 PBAT_PRES#
33 THERMTRIP_SIO
4 PROCHOT#
34 EC_GPIO2
TPAD30 TP80 KSO16
34 KSO16
14 CAPS_LED#
14 NUM_LED#
14 SRL_LED#
42 PRE_CHG
43 PS_ID
TPAD30 TP177
BID0
BID1
BID2
BID3
43 PS_ID_DISABLE#
R503 10KR2
TPAD30 TP88 LAN_EXPORT#
32 MDC_DISABLE#
TPAD30 TP102 NB_VCC_CNTL
TPAD30 TP104 LCM_DATA
TPAD30 TP71 DOCK_SMB_CLK
TPAD30 TP73 DOCK_SMB_DAT
TPAD30 TP112 CLK_SM1
TPAD30 TP117 DAT_SM1
TPAD30 TP89
TPAD30 TP92
34 CLK_SM2
34 DAT_SM2
TPAD30 TP118 CLK_KBD
TPAD30 TP113 DAT_KBD
43 PBAT_ALARM#
34 KSO15
34 KSO14
34 KSO13
34 KSO12
34 KSO11
34 KSO10
34 KSO9
34 KSO8
34 KSO7
34 KSO6
34 KSO5
34 KSO4
34 KSO3
34 KSO2
34 KSO1
34 KSO0
34 KSI7
34 KSI6
34 KSI5
34 KSI4
34 KSI3
34 KSI2
34 KSI1
34 KSI0
31 SIO_FD[0..7]
SIO_FD0
SIO_FD1
SIO_FD2
SIO_FD3
SIO_FD4
SIO_FD5
SIO_FD6
SIO_FD7
XTAL1
XTAL2
IN0
IN1
IN2
IN3
IN5
IN6
IN7
GPIO0
GPIO1
GPIO2
GPIO3
GPIO7
GPIO8
GPIO9
GPIO17
GPIO20
GPIO21
GPIO82/FAN_TACH3
GPIO84
GPIO85
GPIO86
GPIO87
GPIO90
GPIO91
GPIO92
GPIO93
GPIO96
GPIO97
MSCLK
MSDAT
EMCLK
EMDAT
GPIO94/IMCLK
GPIO95/IMDAT
KCLK
KDAT
GPIO6
GPIO5
GPIO4
KSO13
KSO12
KSO11
KSO10
KSO9
KSO8
KSO7
KSO6
KSO5
KSO4
KSO3
KSO2
KSO1
KSO0
K/B
KSI7
KSI6
KSI5
KSI4
KSI3
KSI2
KSI1
KSI0
FD0
FD1
FD2
FD3
FD4
FD5
FD6
FD7
LPC47N354-1-GP
FPGM TEST_PIN
XOSEL EC_SCI#
SYSOPT0
SYSOPT1
BAT_LED#
LDRQ0#
PWR_LED#
R492 10KR2
TP65 TPAD30
R267 10KR2
R480 10KR2
BAT1_LED# 14
LDRQ[0]# 16
BAT2_LED# 14
MISC
EEPROM_WC 31
NEWCARD_RST#0 19
HW_RADIO_DIS# 28,32
LAN_LOW_PWR 24
CHG_PBATT# 42
BCELL_CHG 42
AUDIO_AVDD_ON 26
KBC_RSMRST#
QBUFEN#
TP85 TPAD30
TP175 TPAD30
TP86 TPAD30
BREATH_LED 14
FAN1_PWM 33
PWRGD
VCC1RST#
RESET_OUT#
RUNPWROK 34,35,38,44
VCC1_PWROK 31,44
RESET_OUT# 35,44
AB1A_DATA
AB1A_CLK
AB1B_DATA
AB1B_CLK
DAT_SMB 31,33
CLK_SMB 31,33
MSDATA
MSCLK
TP78 TPAD30
TP84 TPAD30
GPIO11
GPIO12
SBAT_SMBDAT
SBAT_SMBCLK
TP59 TPAD30
TP60 TPAD30
GPIO13
GPIO14
GPIO15
GPIO16
GPIO19
PBAT_SMBDAT 14,43
PBAT_SMBCLK 14,43
FAN1_TACH 33
FAN2_TACH
TP75 TPAD30
GATE20 16
CLOCK
PCI_CLK
GPIO83/32KHZ_OUT
CLOCKI
TP188 TPAD30
PCLK_SIO 3
CLK14_SIO 3
SIO_FA[0..19] 31
FLASH
FA0
FA1
FA2
FA3
FA4
FA5
FA6
FA7
FA8
FA9
FA10
FA11
FA12
FA13
FA14
FA15
FA16
FA17
FA18
FA19
FA20
FA21
FA22
SIO_FA0
SIO_FA1
SIO_FA2
SIO_FA3
SIO_FA4
SIO_FA5
SIO_FA6
SIO_FA7
SIO_FA8
SIO_FA9
SIO_FA10
SIO_FA11
SIO_FA12
SIO_FA13
SIO_FA14
SIO_FA15
SIO_FA16
SIO_FA17
SIO_FA18
SIO_FA19
FA20
FA21
FA22
TP63 TPAD30
TP154 TPAD30
TP64 TPAD30
FRD#
FWR#
FCS#
FRD# 31
FWR# 31
FCS# 31
R253 33R2
R241 33R2
C277 SC22P50V2JN-1
C266 SC22P50V2JN-1
SMBus Pull-ups
+3VALW
RN5 SRN4D7KJ DAT_SMB CLK_SMB
RN3 SRN10KJ DOCK_SMB_CLK DOCK_SMB_DAT
DY 9/21
RN1 SRN8K2J SBAT_SMBDAT SBAT_SMBCLK
RN2 SRN4D7KJ PBAT_SMBDAT PBAT_SMBCLK
RN4 SRN10KJ MSDATA MSCLK
To Touchpad CONN
+3VRUN
R499 DUMMY-R2
R264 10KR2
R265 DUMMY-R2
R500 DUMMY-R2
R498 10KR2
R263 DUMMY-R2
R266 10KR2
R501 10KR2
SD
BID3 BID2 BID1 BID0 Board Rev.
0 0 0 0 X00
0 0 0 1 X01
0 0 1 0 X02
0 0 1 1 X03
0 1 0 0 X04
0 1 0 1 ???
+5VRUN
RN8 DAT_SM1 CLK_SM1
SRN4D7KJ
RN7 DAT_KBD CLK_KBD
SRN4D7KJ
PS/2 I/F Pull-ups
KSO_17 and KSI0 for i buttom
KSO_17 and KSI6 for Audio_Mute# buttom
KSO_17 and KSI4 for Volum Up buttom
KSO_17 and KSI5 for Volum down buttom
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
Macallen III(2 of 2)
Size A3
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Barbados
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Date: Thursday, May 12, 2005
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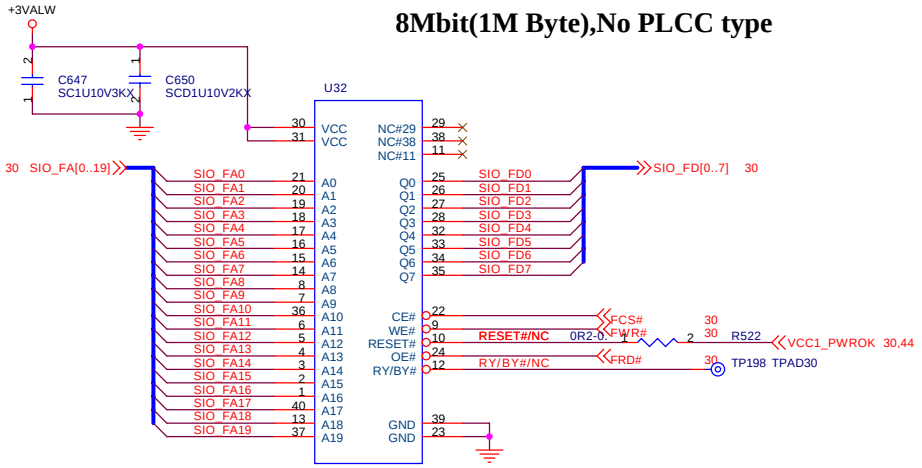
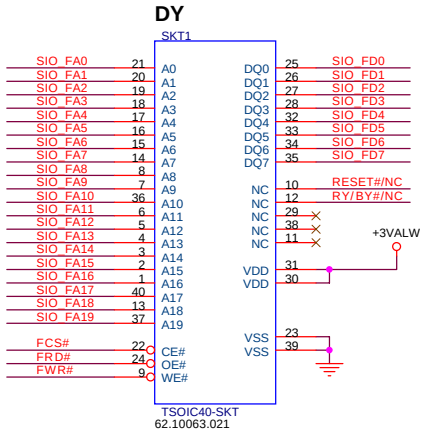
8Mbit(1M Byte),No PLCC type



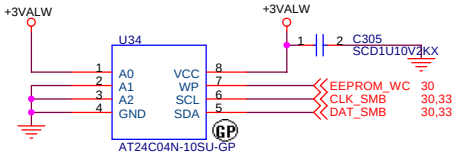


TSOIC 40 pin SOCKET
Co_layout with U28

MXIC: MX29LV008CTTI-90G "72.29008.G09"(Main sorce,LF,bottom boot block)
ST: M29W008AB-90 "72.29008.C09" (2nd sorce)

SMBus address A2

User Password



Atmel: AT24C04N-10SI "72.24C04.D01" (Main sorce)
ST : M24C04 "72.24C04.B01" (2nd sorce)

<Core Design>

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Title: BIOS

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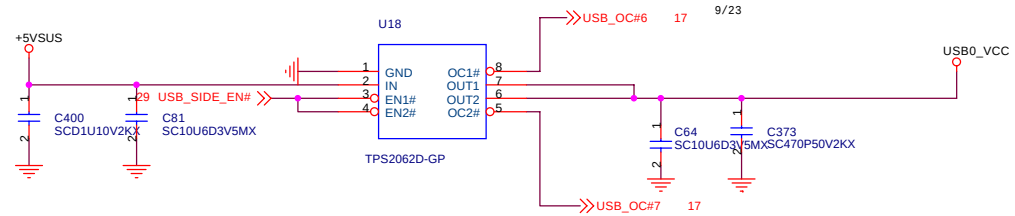
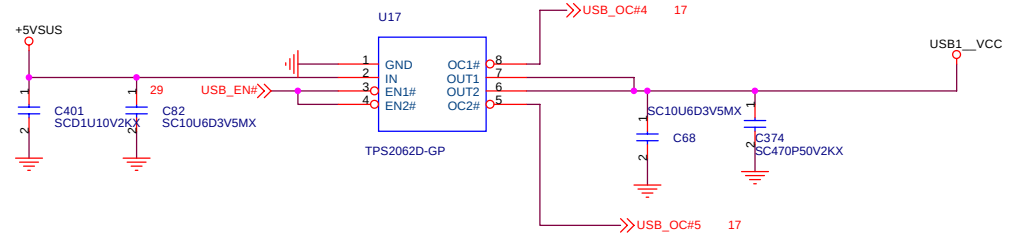
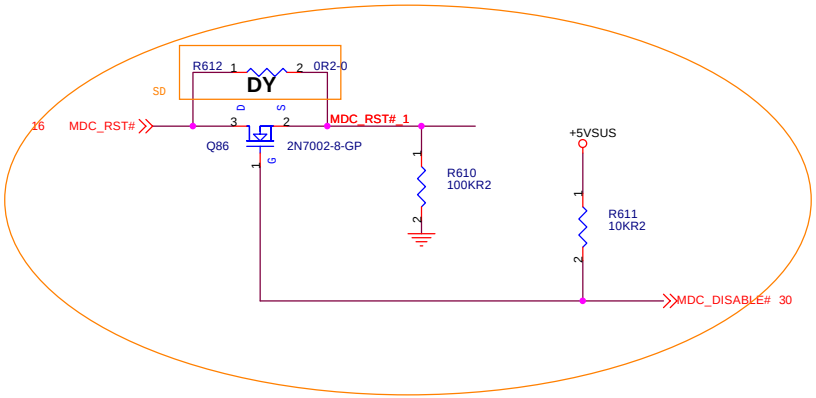
Dual USB0_VCC switch for USB6/USB7

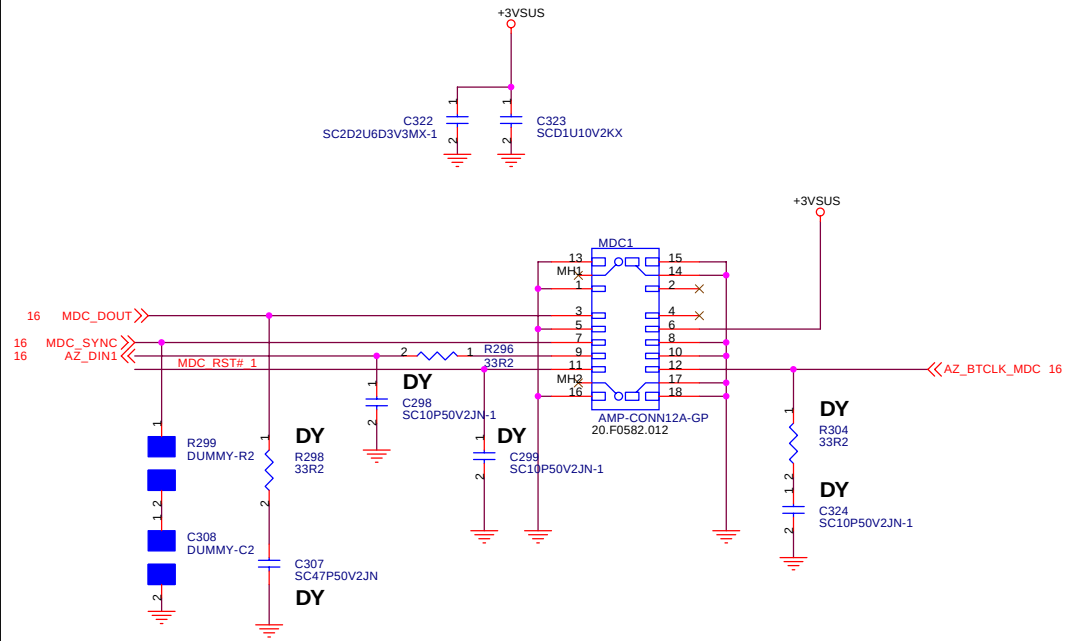


Dual USB1_VCC switch for USB4/USB5

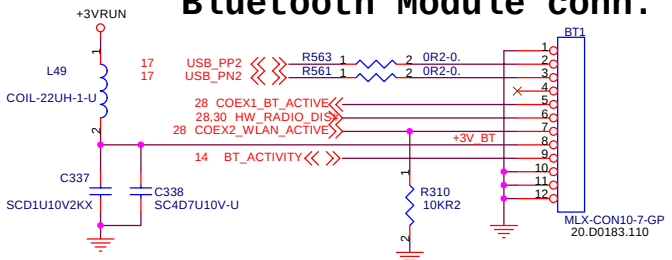




Modem Connector (Not Standard Type)



Bluetooth Module conn.



Note:Place R621 near CN13.

<Core Design>

Wistron Corporation
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Title: USB / MDC /BT/FIR		
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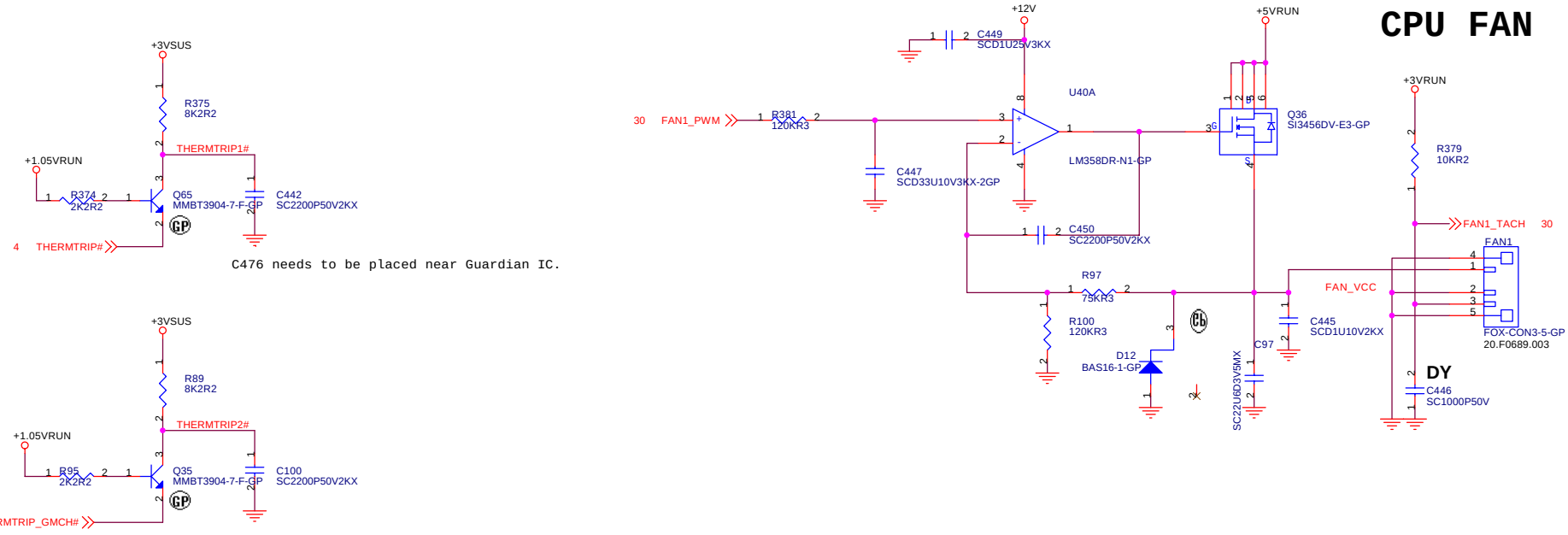
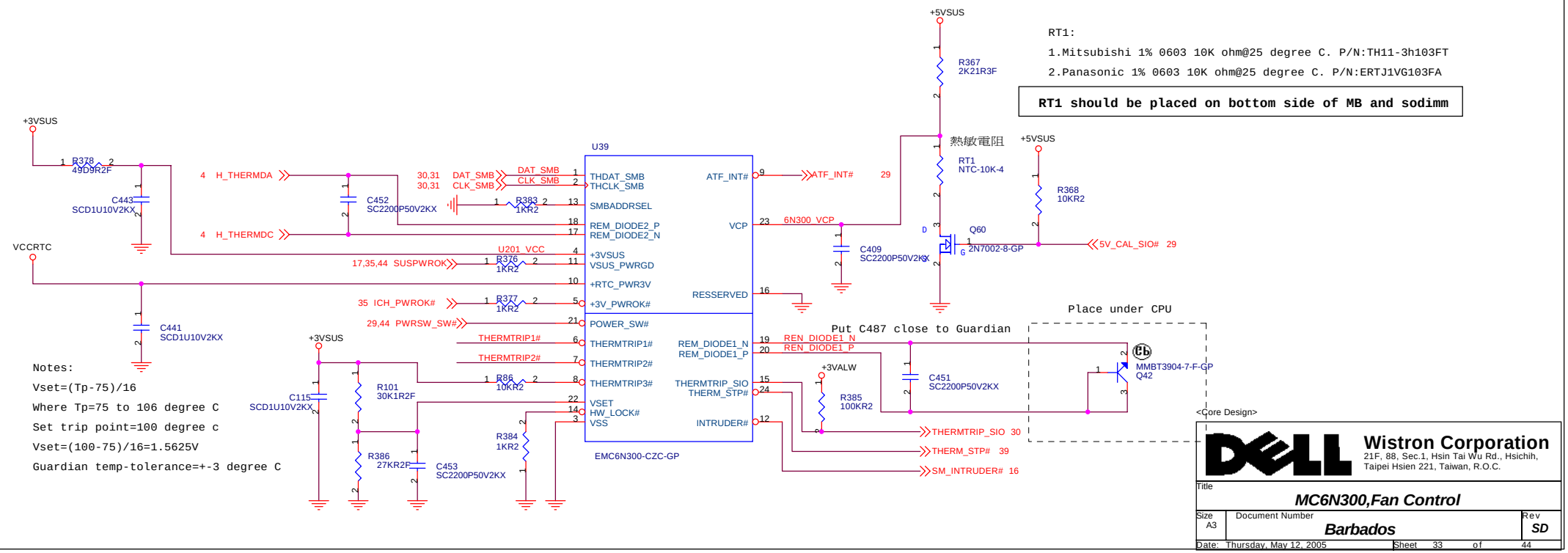
CPU FAN





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<Core Design>

Title: MC6N300,Fan Control

Size: A3 | Document Number: Barbados | Rev: SD

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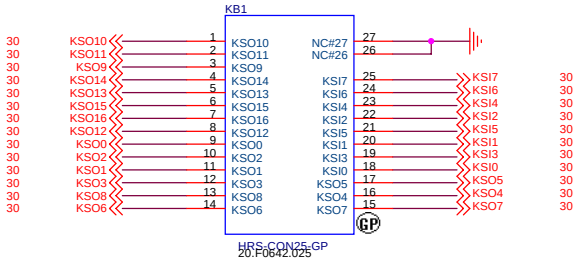
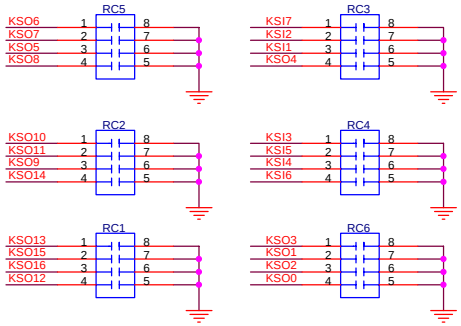
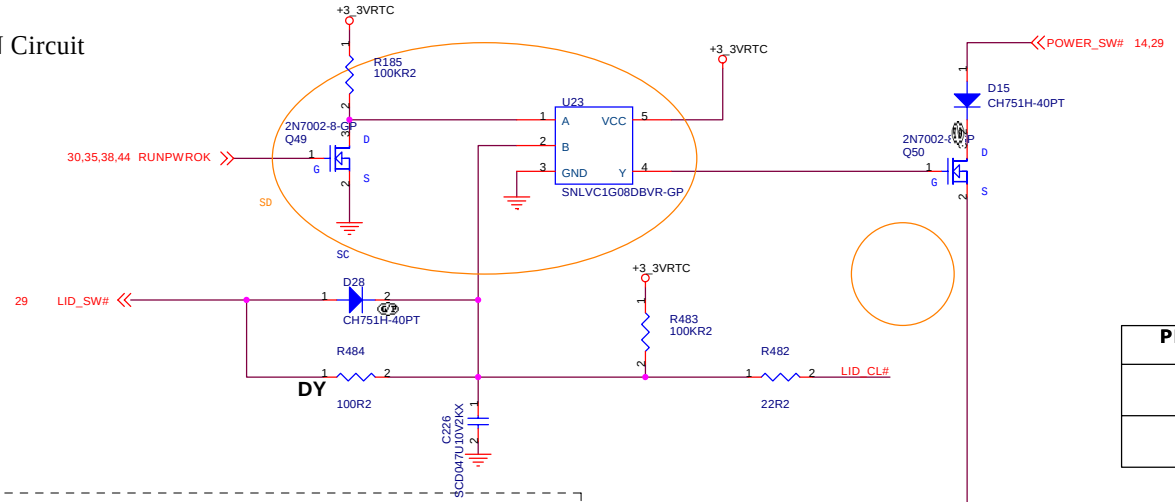
KB CONN

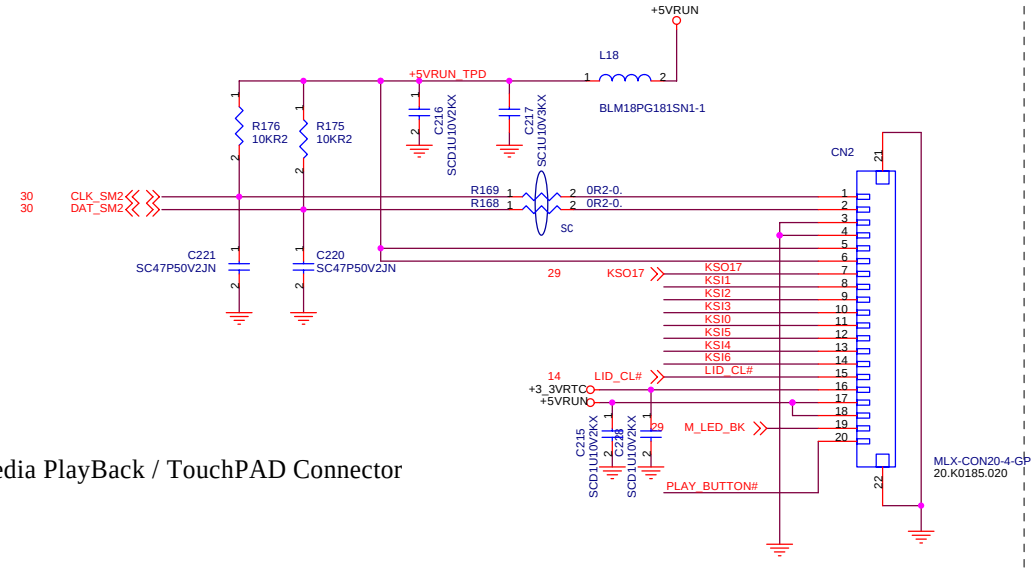


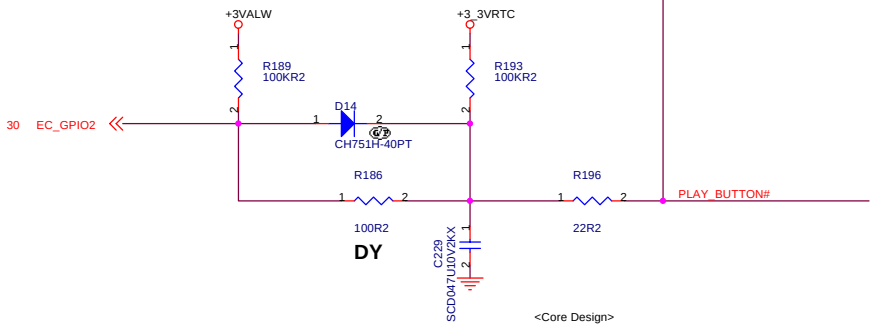


Instant ON Circuit



PLAY_PWR	PLAY_Button#
LOW	Regular Play Function
HIGH	Power On Function





Media PlayBack / TouchPAD Connector

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: KB/TPAD/Media_Playback_Conn

Size: Custom | Document Number: Barbados | Rev: SD

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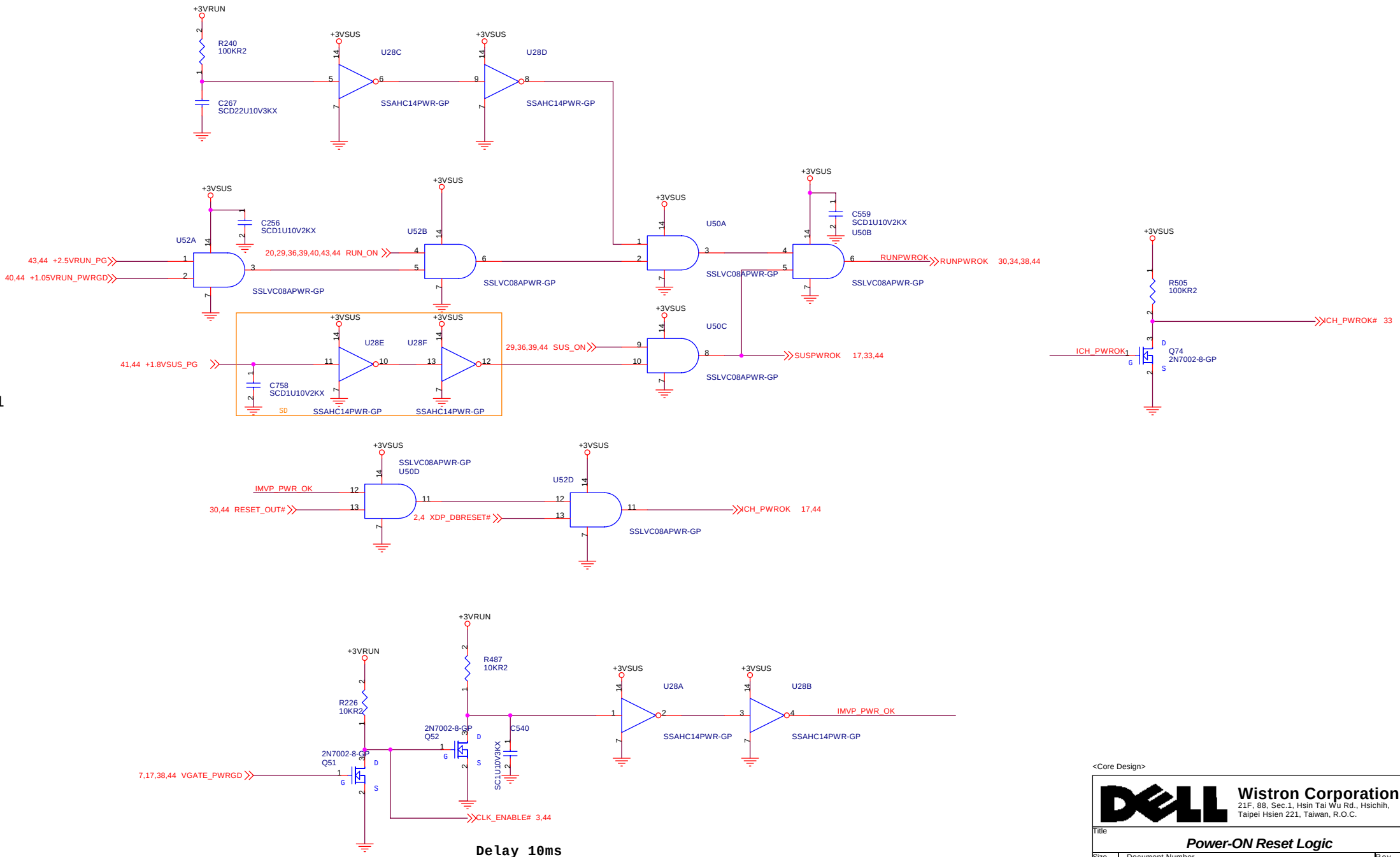

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power-ON Reset Logic***

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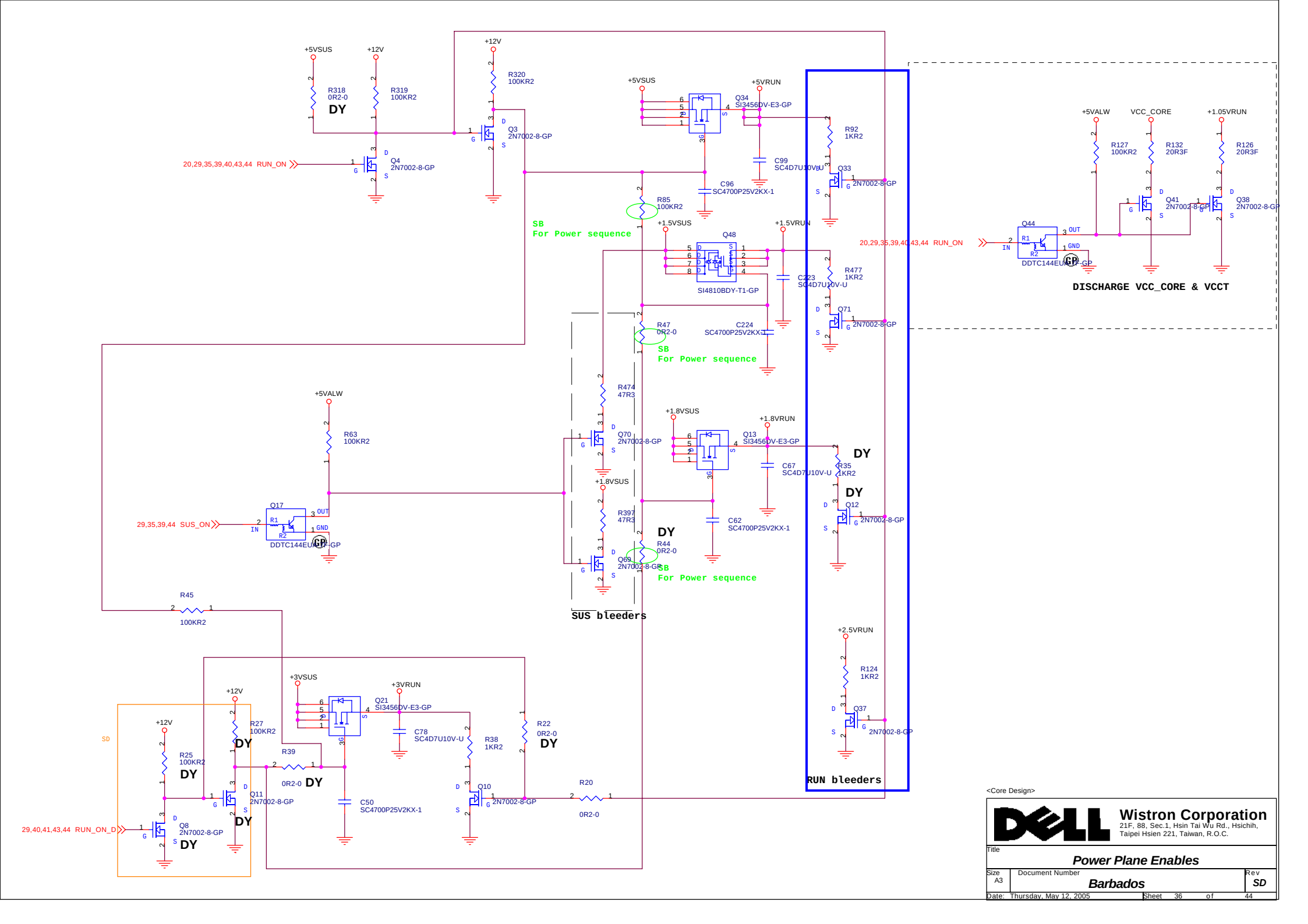

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enables

Size: A3 | Document Number: Barbados | Rev: SD

Date: Thursday, May 12, 2005 | Sheet 36 of 44

CPU_CORE ISL6217A

VID Setting
- H_VID0 — VID0(I / 1.05V)
- H_VID1 — VID1(I / 1.05V)
- H_VID2 — VID2(I / 1.05V)
- H_VID3 — VID3(I / 1.05V)
- H_VID4 — VID4(I / 1.05V)
- H_VID5 — VID5(I / 1.05V)

Output Signal
- PGOOD(OD / 3.3V) — VGATE_PWRGD

Output Power
- VCC_CORE(O) — VCC_CORE (27A)

Input Signal
- RUNPWROK — EN(I / 3.3V)
- PM_DPRSLPVR — DRSEN(I / 3.3V)
- PM_STPCPU# — DSEN# (I / 3.3V)

Voltage Sense
- VCC_CORE — VSEN(I / 1.55V / 1.35V)

Input Power
- PWR_SRC_6217 — VCC(I)
- +5VRUN — VCC(I)

Max8734A 5V/3D3V

Input Signal
- SUS_ON — ON3
- ON5
- ALWON/THERM_STP# — SHDN#
- +5VALW — SKIP#

Output Signal
- PGOOD(OD / 3.3V) — SUSPWROK_5V

Output Power
- 5V(O) — +5VSUS(5.336A)
- 3D3V(O) — +3VSUS(4.9A)
- LDO5(O) — +5VALW(30mA)
- LDO3 (O) — +3VALW(30mA)

Input Power
- PWR_SRC_1999 — V+

Max8743 1.5V/1.05V

Input Signal
- RUN_ON_D — ON1
- SUSPWROK_5V — ON2

Output Signal
- PGOOD(OD / 3.3V) — +1.05VRUN_PWRGD

Output Power
- 1.5V(O) — +1.5VSUS(4.3A)
- +1.05V(O) — +1.05VRUN(5A)

Input Power
- +5VSUS — VCC(I)
- PWR_SRC — V+

Adapter

Input Signal
- PS_ID_CONN — (I)

Output Signal
- (O) — PS_ID

Input Power
- CHG_DC_IN — VCC(I)

Output Power
- VCC(O) — DC_IN+

Charger MAX1909

Input Signal
- CHG_PBATT — CHG_OFF(I / 3.3V)
- PBAT_SMBCLK — BT_SCL(IO / 5V)
- PBAT_SMBDAT — BT_SDA(IO / 5V)

Output Signal
- BT_TH(O / 5V) — PBAT_THEM#

Input Power
- DC_IN+ — VCC(I)

Output Power
- VCC(O) — PWR_SRC
- VCC(O) — BATT+

TI51116 1.8V / 0.9V

Input Signal
- SUSPWROK_5V — S5
- RUN_ON_D — S3

Output Signal
- PGOOD(OD / 3.3V) — +1.8VSUS_PG

Input Power
- +5VSUS — VCC(I)
- PWR_SRC — VCC(I)

Output Power
- VCC(O) — +1.8VSUS(7.4A)
- VCC(O) — +0.9VRUN(1.2A)
- VCC(O) — +0.9VSUS_DDRVREF

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power Block Diagram*

Size: A3 | Document Number: *Barbados* | Rev: *SD*

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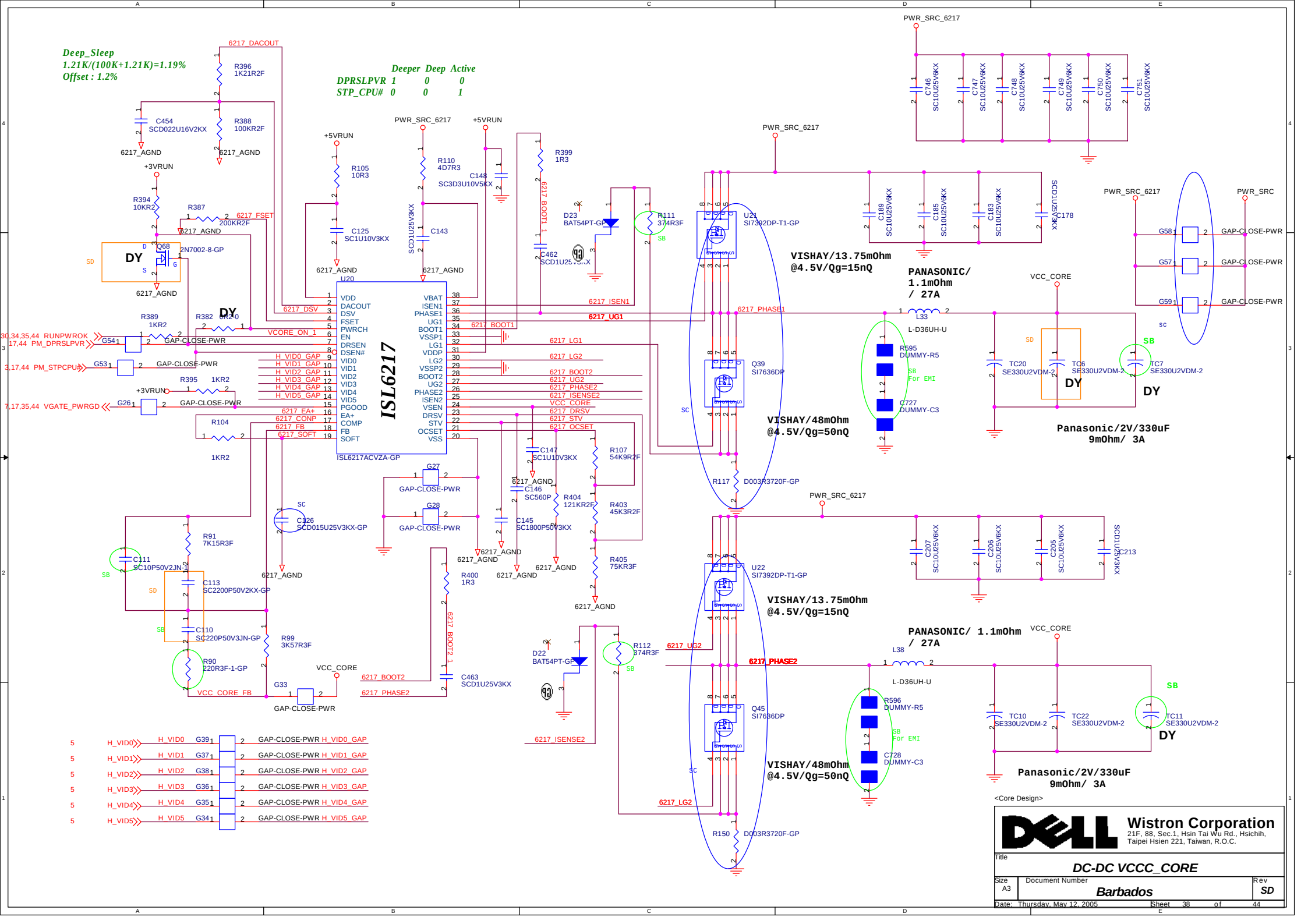
Deep_Sleep
1.21K/(100K+1.21K)=1.19%
Offset : 1.2%
Deeper Deep Active
DPRSLPVR 1 0 0
STP_CPU# 0 0 1
ISL6217
ISL6217ACVZA-GP
VISHAY/13.75mOhm
@4.5V/Qg=15nQ
VISHAY/48mOhm
@4.5V/Qg=50nQ
PANASONIC/
1.1mOhm
/ 27A
Panasonic/2V/330uF
9mOhm/ 3A
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Taipei Hsien 221, Taiwan, R.O.C.
DC-DC VCCC_CORE
Barbados
Date: Thursday, May 12, 2005
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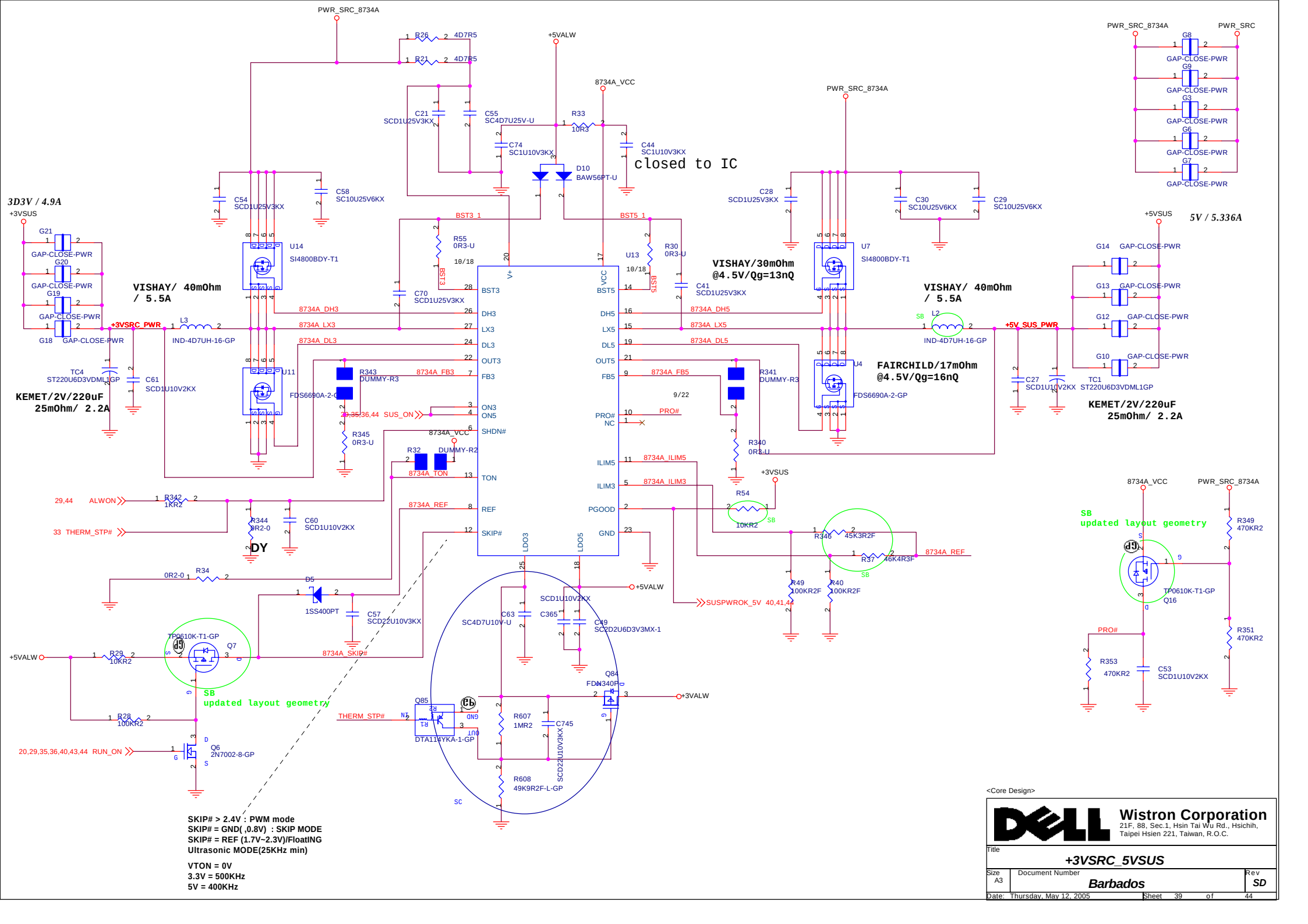
3D3V / 4.9A
+3VSUS
VISHAY/ 40mOhm / 5.5A
+3VSRC_PWR
KEMET/2V/220uF 25mOhm/ 2.2A
VISHAY/30mOhm @4.5V/Qg=13nQ
FAIRCHILD/17mOhm @4.5V/Qg=16nQ
5V / 5.336A
+5VSUS
+5V_SUS_PWR
closed to IC
SB updated layout geometry
DY
SKIP# > 2.4V : PWM mode
SKIP# = GND(,0.8V) : SKIP MODE
SKIP# = REF (1.7V~2.3V)/FloatING
Ultrasonic MODE(25KHz min)
VTON = 0V
3.3V = 500KHz
5V = 400KHz
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
+3VSRC_5VSUS
Size A3
Document Number
Barbados
Rev SD
Date: Thursday, May 12, 2005
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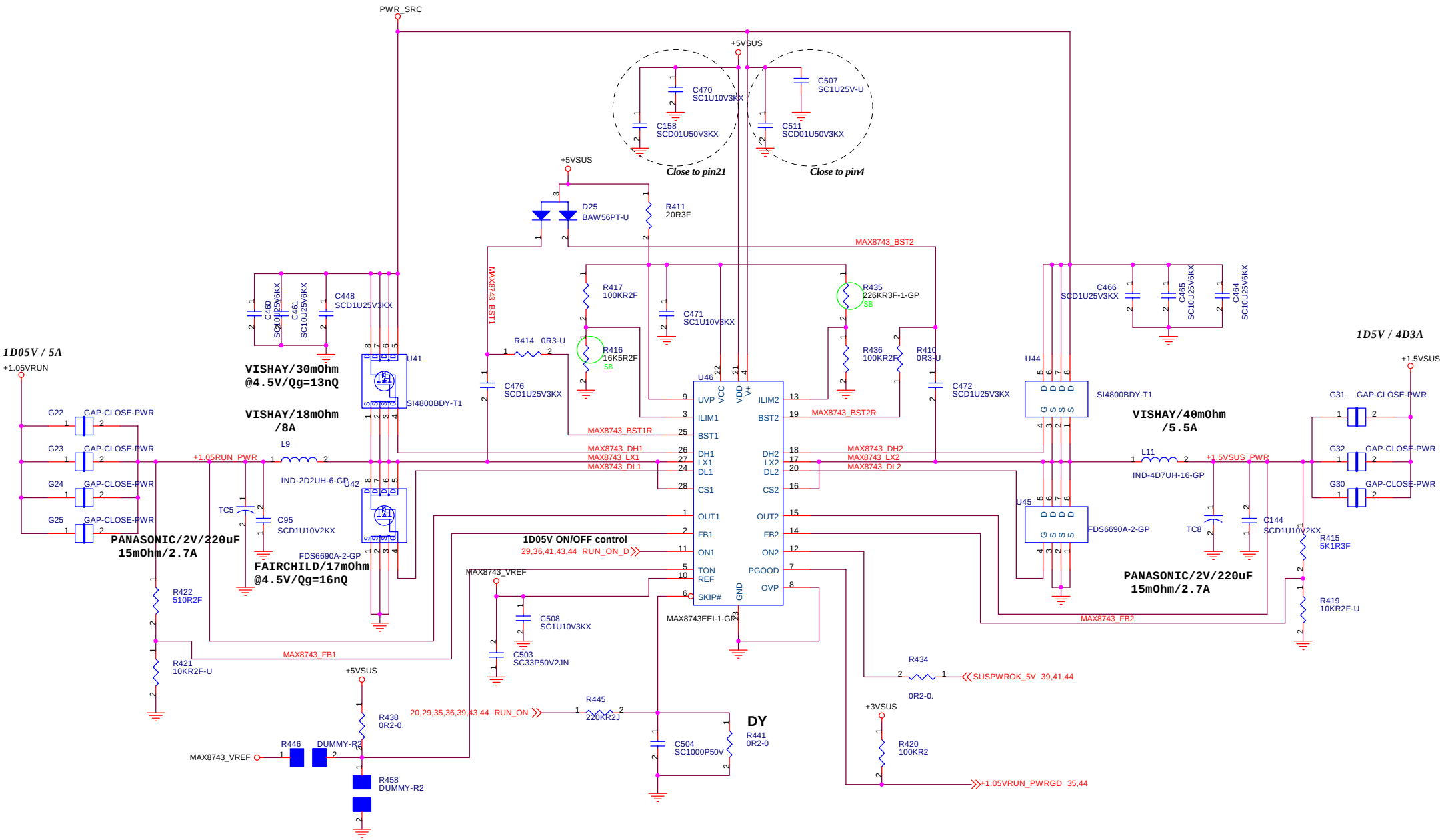

<Core Design>

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Title: +1.5VSUS_1.05VRUN

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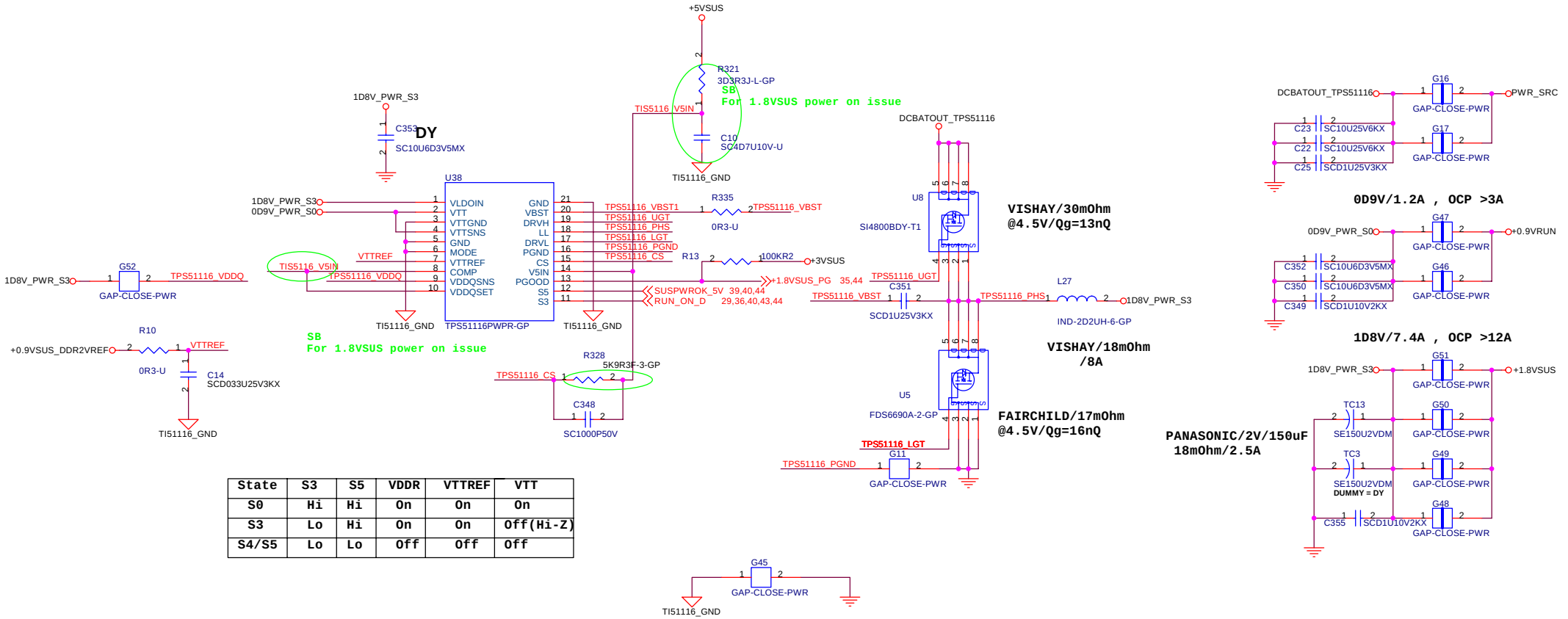
TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *+1.8VSUS&0.9VRUN&DDR2_VREF*

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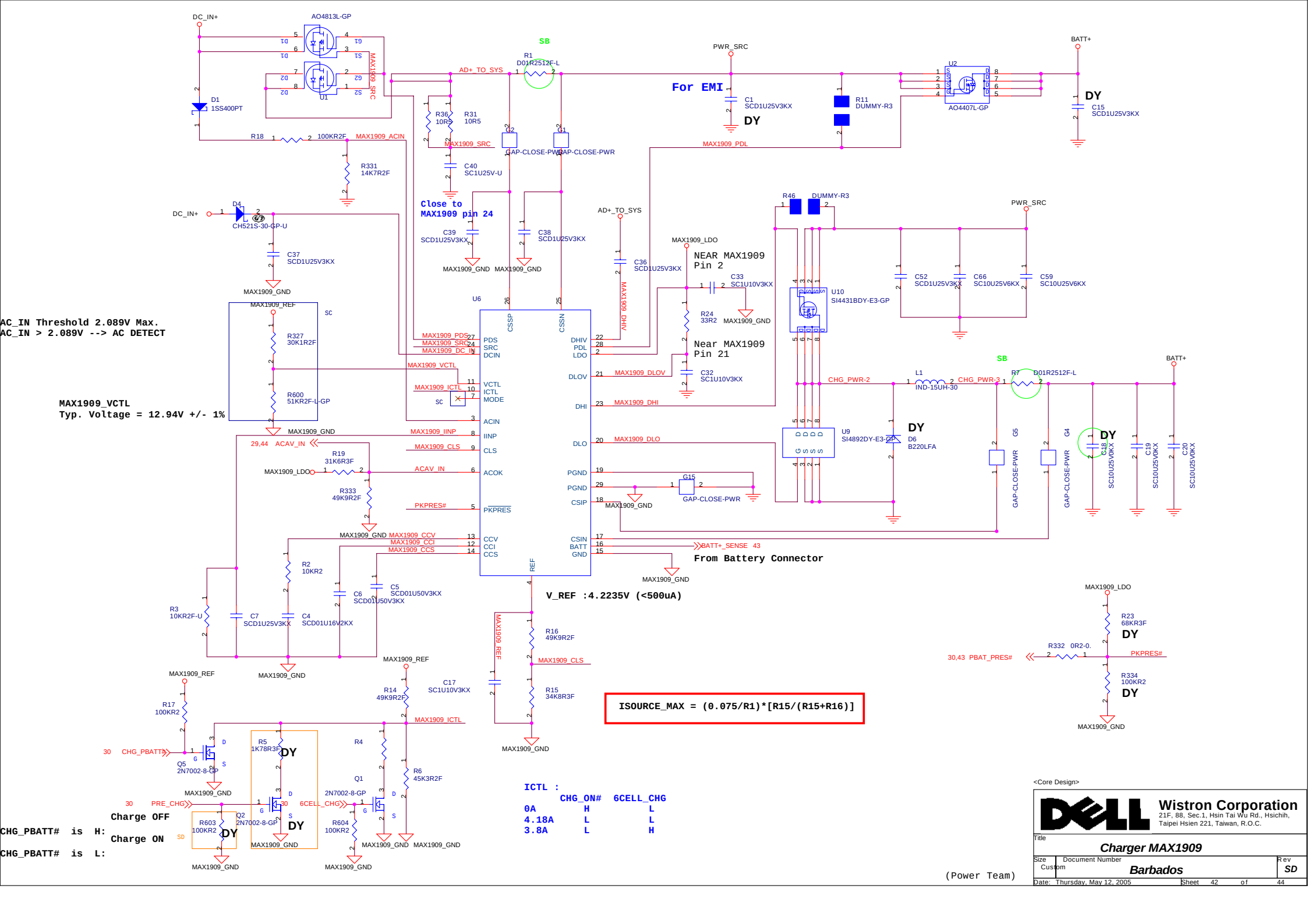
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
MAX1909_VCTL
Typ. Voltage = 12.94V +/- 1%
V_REF :4.2235V (<500uA)
From Battery Connector
ISOURCE_MAX = (0.075/R1)*[R15/(R15+R16)]
ICTL :
CHG_ON# 6CELL_CHG
0A H L
4.18A L L
3.8A L H
Charge OFF
Charge ON
CHG_PBATT# is H:
CHG_PBATT# is L:
For EMI
Close to MAX1909 pin 24
NEAR MAX1909 Pin 2
Near MAX1909 Pin 21
SB
DY
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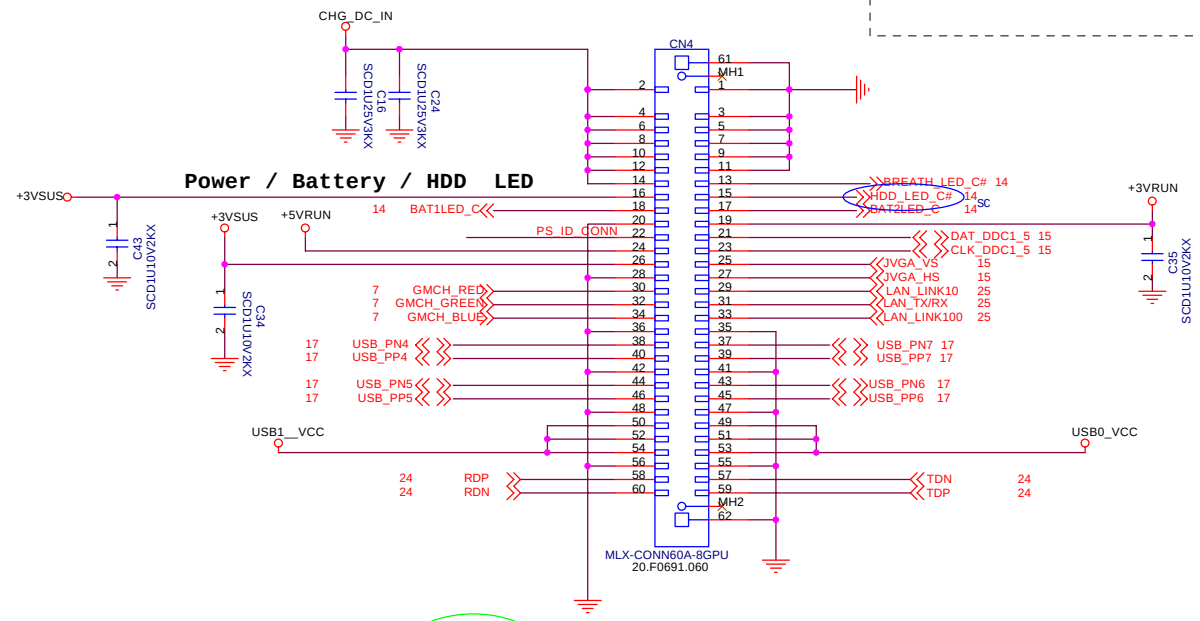
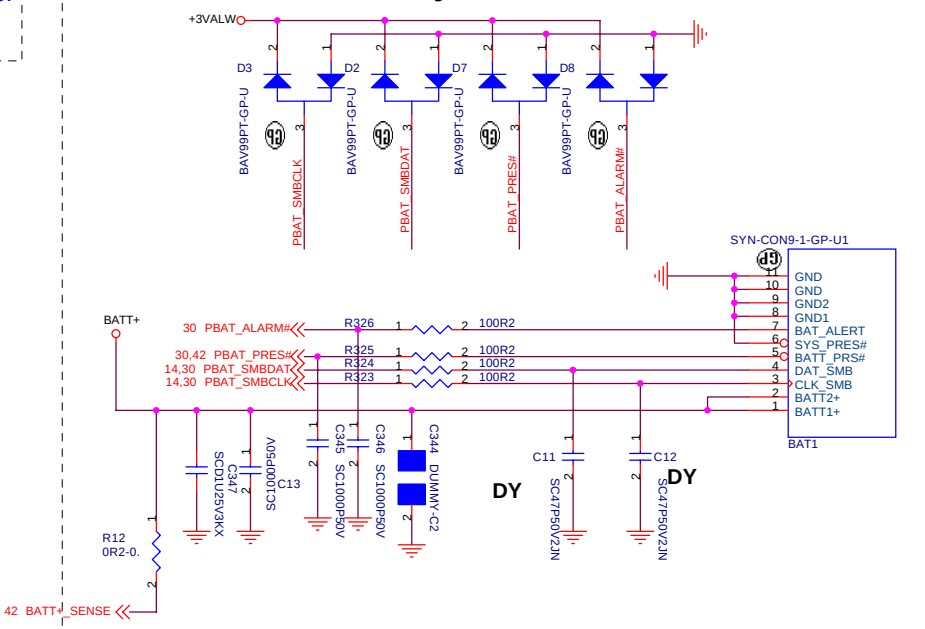
Charger MAX1909
Barbados
(Power Team)
Thursday, May 12, 2005

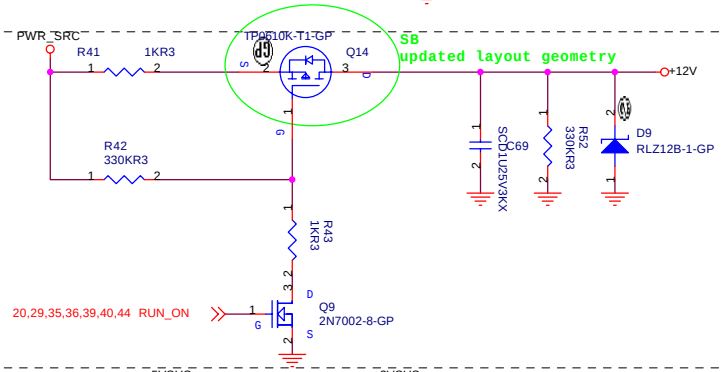
TV BD Conn

Layout Note:
Must be a ground return path for
CRT_R,CRT_G,CRT_B

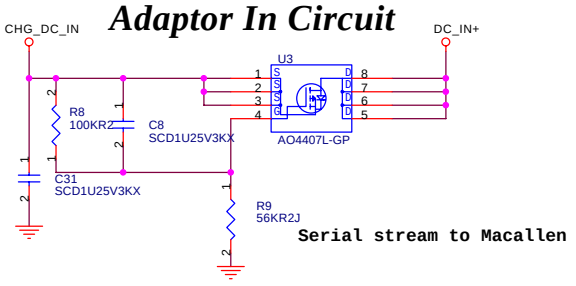


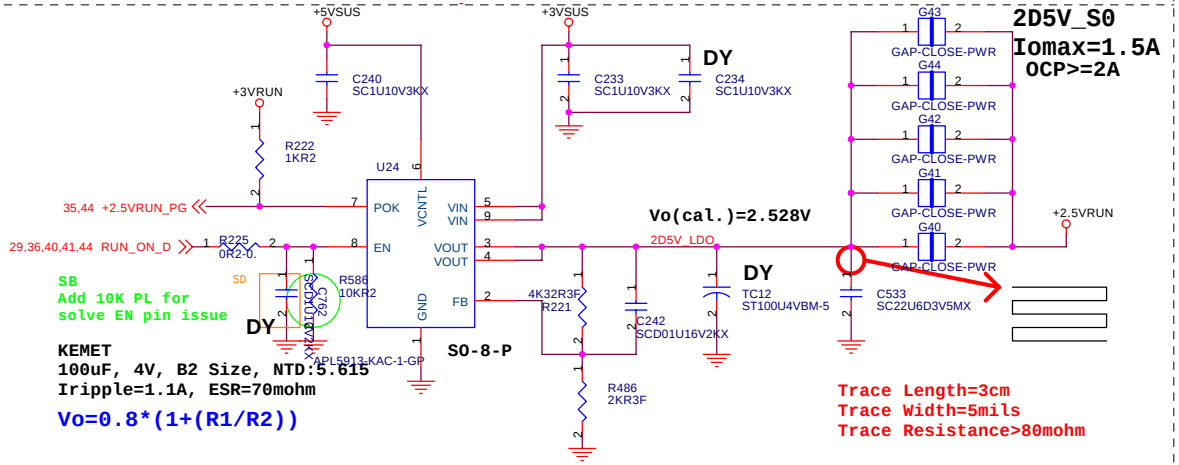
Battery Conn

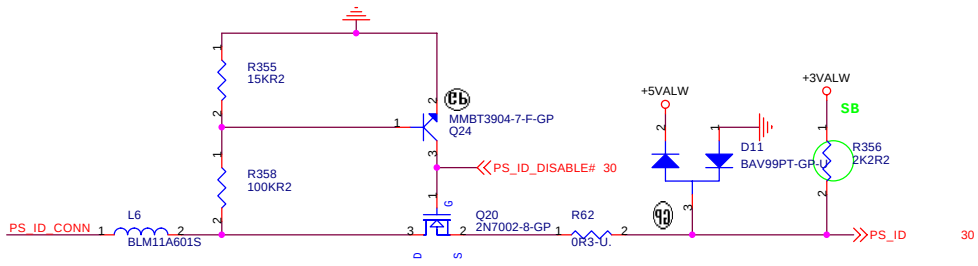




Adaptor In Circuit







<Core Design>

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Title: Battery/TV/Adaptor Conn/+2.5VSUS

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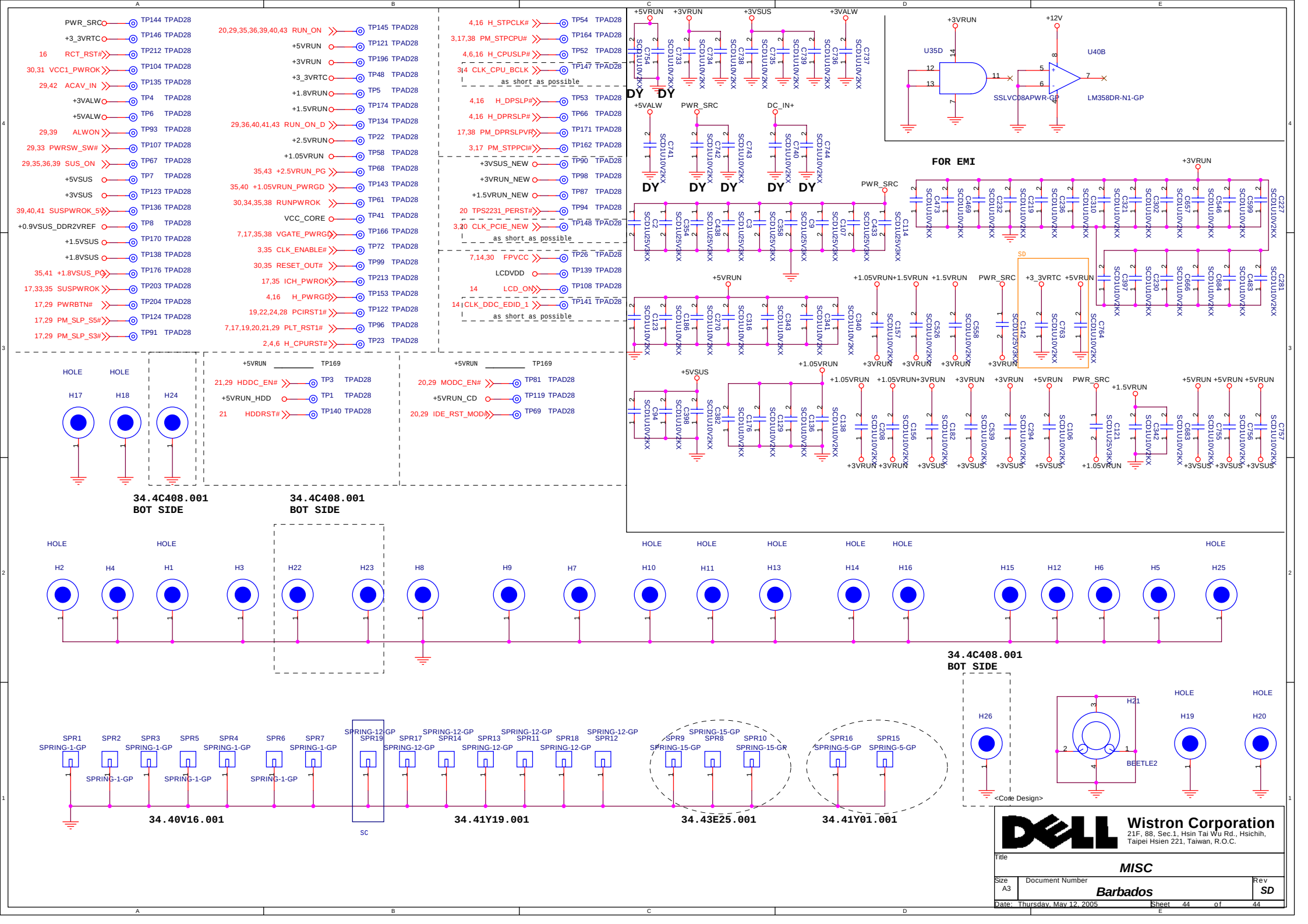
PWR_SRC TP144 TPAD28
+3_3VRTC TP146 TPAD28
16 RCT_RST# TP212 TPAD28
30,31 VCC1_PWROK TP104 TPAD28
29,42 ACAV_IN TP135 TPAD28
+3VALW TP4 TPAD28
+5VALW TP6 TPAD28
29,39 ALWON TP93 TPAD28
29,33 PWRSW_SW# TP107 TPAD28
29,35,36,39 SUS_ON TP67 TPAD28
+5VSUS TP7 TPAD28
+3VSUS TP123 TPAD28
39,40,41 SUSPWROK_5V TP136 TPAD28
+0.9VSUS_DDR2VREF TP8 TPAD28
+1.5VSUS TP170 TPAD28
+1.8VSUS TP138 TPAD28
35,41 +1.8VSUS_PG TP176 TPAD28
17,33,35 SUSPWROK TP203 TPAD28
17,29 PWRBTN# TP204 TPAD28
17,29 PM_SLP_S5# TP124 TPAD28
17,29 PM_SLP_S3# TP91 TPAD28
20,29,35,36,39,40,43 RUN_ON TP145 TPAD28
+5VRUN TP121 TPAD28
+3VRUN TP196 TPAD28
+3_3VRTC TP48 TPAD28
+1.8VRUN TP5 TPAD28
+1.5VRUN TP174 TPAD28
29,36,40,41,43 RUN_ON_D TP134 TPAD28
+2.5VRUN TP22 TPAD28
+1.05VRUN TP58 TPAD28
35,43 +2.5VRUN_PG TP68 TPAD28
35,40 +1.05VRUN_PWRGD TP143 TPAD28
30,34,35,38 RUNPWROK TP61 TPAD28
VCC_CORE TP41 TPAD28
7,17,35,38 VGATE_PWRGD TP166 TPAD28
3,35 CLK_ENABLE# TP72 TPAD28
30,35 RESET_OUT# TP99 TPAD28
17,35 ICH_PWROK TP213 TPAD28
4,16 H_PWRGD TP153 TPAD28
19,22,24,28 PCIRST1# TP122 TPAD28
7,17,19,20,21,29 PLT_RST1# TP96 TPAD28
2,4,6 H_CPURST# TP23 TPAD28
4,16 H_STPCLK# TP54 TPAD28
3,17,38 PM_STPCPU# TP164 TPAD28
4,6,16 H_CPUSLP# TP52 TPAD28
3,4 CLK_CPU_BCLK TP147 TPAD28
as short as possible
4,16 H_DPSLP# TP53 TPAD28
4,16 H_DPRSLP# TP66 TPAD28
17,38 PM_DPRSLPVR TP171 TPAD28
3,17 PM_STPPCI# TP162 TPAD28
+3VSUS_NEW TP90 TPAD28
+3VRUN_NEW TP98 TPAD28
+1.5VRUN_NEW TP87 TPAD28
20 TPS2231_PERST# TP94 TPAD28
3,20 CLK_PCIE_NEW TP148 TPAD28
as short as possible
7,14,30 FPVCC TP26 TPAD28
LCDVDD TP139 TPAD28
14 LCD_ON TP108 TPAD28
14 CLK_DDC_EDID_1 TP141 TPAD28
as short as possible
HOLE H17
HOLE H18
H24
+5VRUN TP169
21,29 HDDC_EN# TP3 TPAD28
+5VRUN_HDD TP1 TPAD28
21 HDDRST# TP140 TPAD28
+5VRUN TP169
20,29 MODC_EN# TP81 TPAD28
+5VRUN_CD TP119 TPAD28
20,29 IDE_RST_MOD# TP69 TPAD28
34.4C408.001
BOT SIDE
34.4C408.001
BOT SIDE
+5VRUN +3VRUN +3VSUS +3VALW
DY DY
+5VALW PWR_SRC DC_IN+
DY DY DY DY DY
PWR_SRC
FOR EMI
+3VRUN
SD
+5VRUN
+1.05VRUN +1.5VRUN +1.5VRUN
PWR_SRC +3_3VRTC +5VRUN
+5VSUS
+1.05VRUN
+1.05VRUN +1.05VRUN +3VRUN
+3VRUN +3VRUN +3VRUN +5VRUN
PWR_SRC +1.5VRUN
+5VRUN +5VRUN +5VRUN
U35D
U40B
SSLVC08APWR-GP
LM358DR-N1-GP
HOLE H2
HOLE H4
H1
H3
H22
H23
H8
H9
H7
HOLE H10
HOLE H11
H13
HOLE H14
HOLE H16
H15
H12
H6
H5
HOLE H25
34.4C408.001
BOT SIDE
SPR1 SPRING-1-GP
SPR2 SPRING-1-GP
SPR3 SPRING-1-GP
SPR5 SPRING-1-GP
SPR4 SPRING-1-GP
SPR6 SPRING-1-GP
SPR7 SPRING-1-GP
SPR19 SPRING-12-GP
SPR17 SPRING-12-GP
SPR14 SPRING-12-GP
SPR13 SPRING-12-GP
SPR11 SPRING-12-GP
SPR18 SPRING-12-GP
SPR12 SPRING-12-GP
SPR9 SPRING-15-GP
SPR8 SPRING-15-GP
SPR10 SPRING-15-GP
SPR16 SPRING-5-GP
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SC
34.41Y19.001
34.43E25.001
34.41Y01.001
H26
<Core Design>
H21
BEETLE2
HOLE H19
HOLE H20
Wistron Corporation
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Title
MISC
Size A3
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