

SULLIVAN

REV : X01

@ : Depop Component for All

Dothan Schematic with Capture CIS and Function field

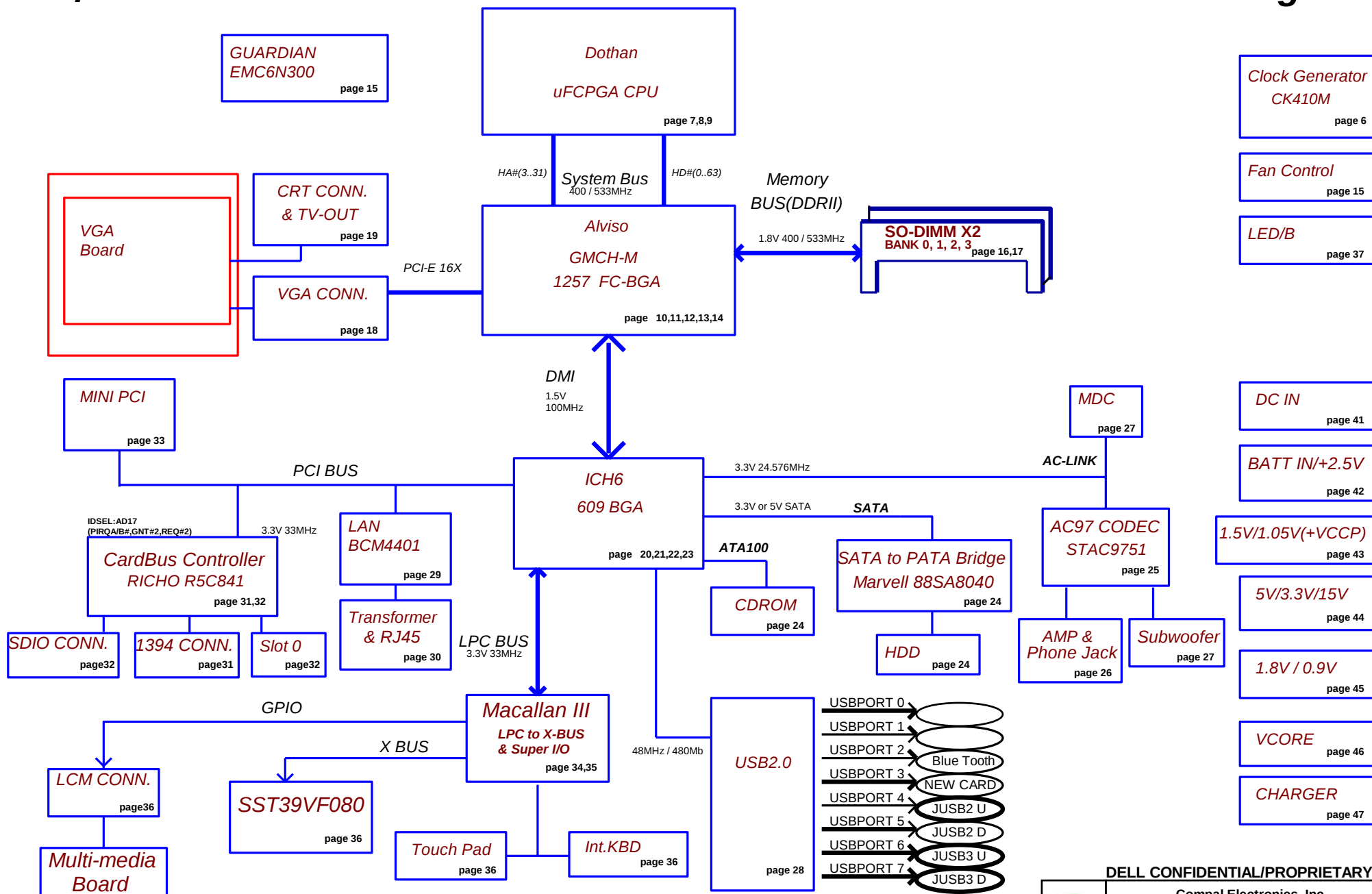
uFCPGA Dothan
02-11-2004
REV: 0.2

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Title			Cover Sheet	
Size	Document Number	Rev		
	LA-2171	0.2		
Date	12/2004	Sheet	1	of 50



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Block Diagram

Size	Document Number	Rev
	LA-2171	0.2

Date: 12/2004 Sheet: 2 of 50

PM TABLE

State \ power plane	+3VALW +5VALW	+3VSUS +5VSUS +1.8VSUS +1.5VSUS	+5VRUN +3VRUN +0.9V_DDR_VTT +2.5VRUN +1.8VRUN +1.5VRUN +VCC_CORE +VCCP +15V
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	1	D,C
MINI PCI	AD19	3	D,B
LAN	AD16	4	C

USB TABLE

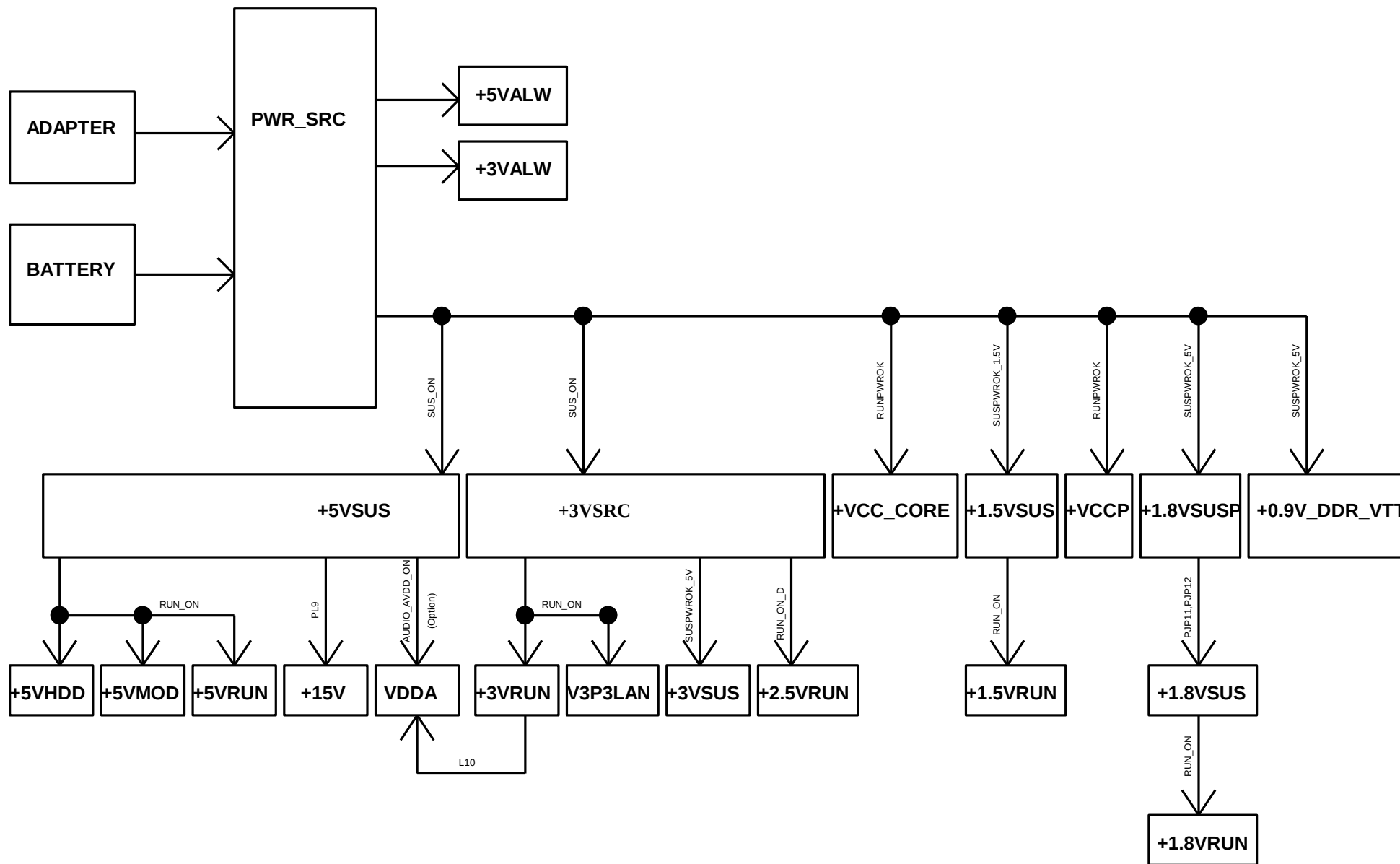
USB PORT#	DESTINATION
0	
1	
2	Blue Tooth
3	NEW CARD
4	JUSB2 (Top)
5	JUSB2 (Bottom)
6	
7	

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Title		Index and Config.	
Size	Document Number	Rev	
	LA-2171	0.2	
Date	12/2004	Sheet	3 of 50

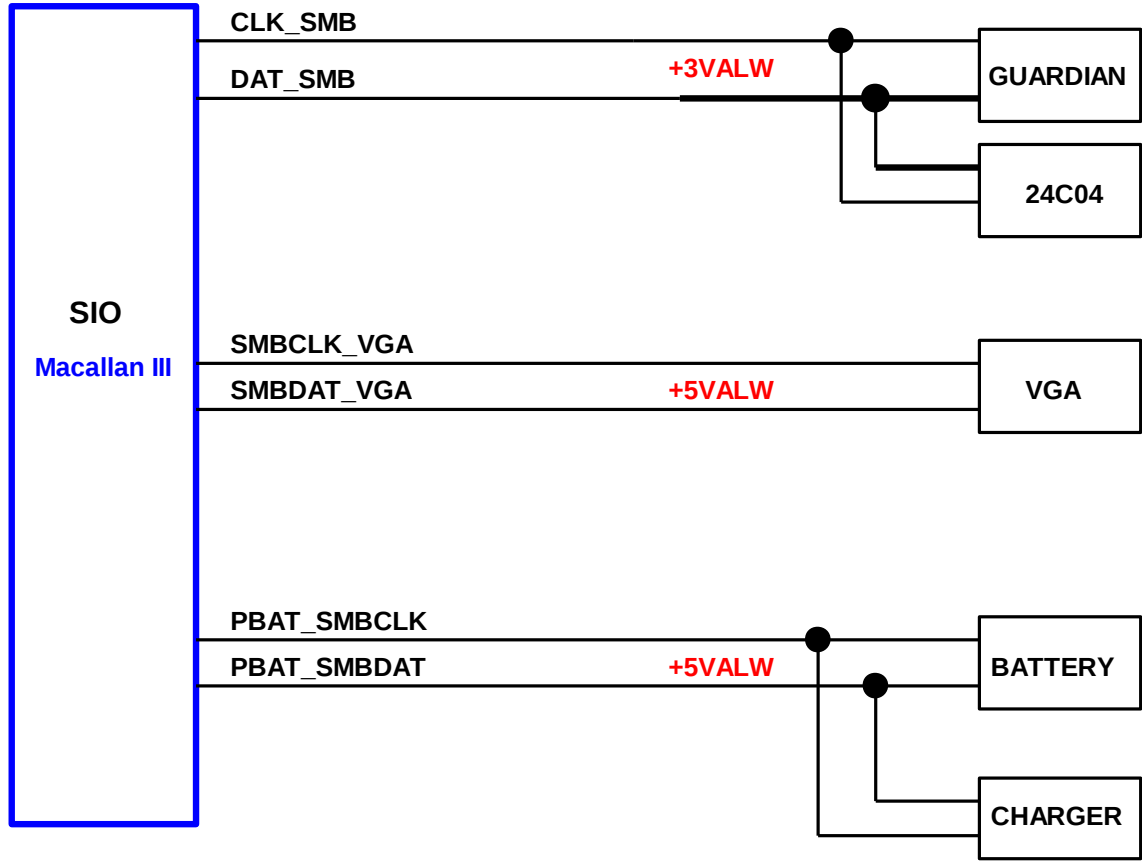
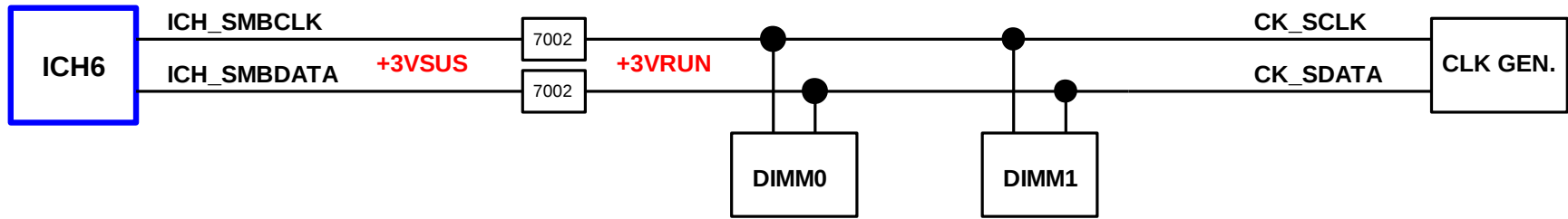


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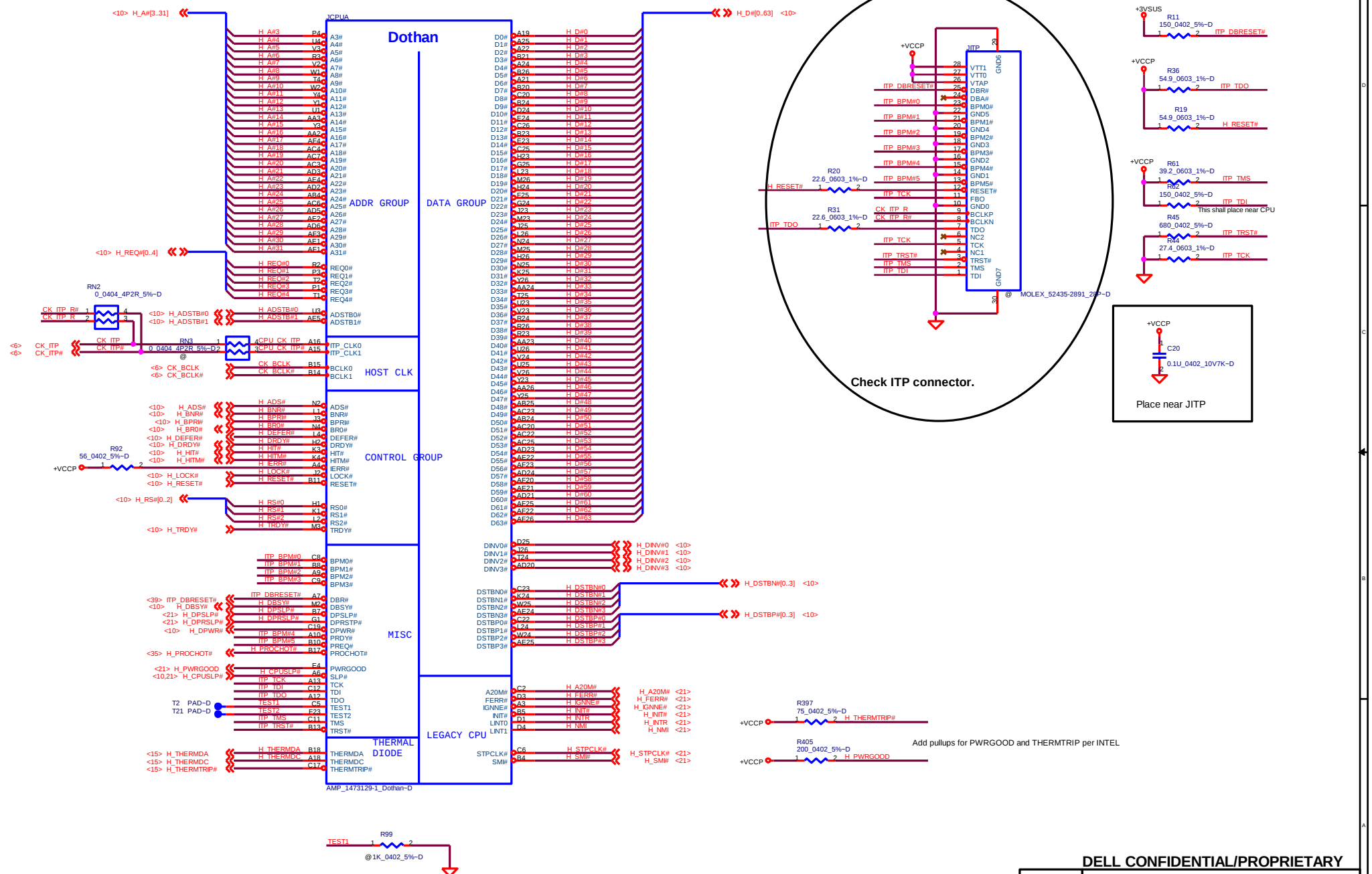
Title		Power Rail	
Size	Document Number	Rev	
	LA-2171	0.2	
Date	12/2004	Sheet	4 of 50



	Device	Address
	DIM0	A0h
	DIM1	A2h
	CLK GEN.	D2h
	GUARDIAN	5Eh
	24C04	A2h
	VGA	58h
	Battery	16h
	Charger	12h

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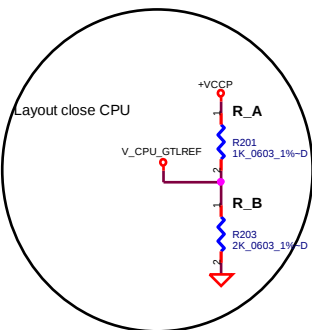
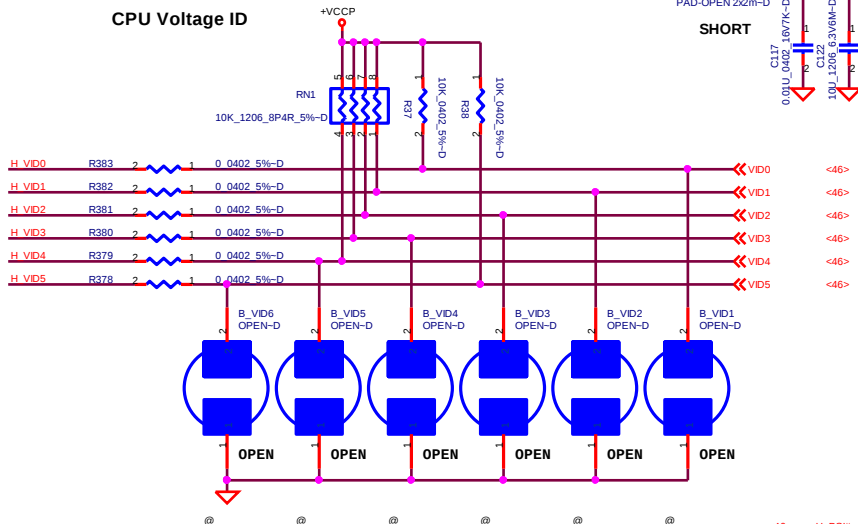
Dothan Processor(1/2)

Size	Document Number	Rev
LA-2171	LA-2171	0.2
Date	12/2004	Sheet 7 of 50

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For test only ,Cmos output

CPU Voltage ID



Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.

Layout Note:
500 mil max length

V_CPU_GTLREF

CPU_BSEL0 CPU_BSEL1

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

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COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

COMP0 COMP1 COMP2 COMP3

Dothan

POWER, GROUND, RESERVED SIGNALS AND NC

Dothan

POWER, GROUND

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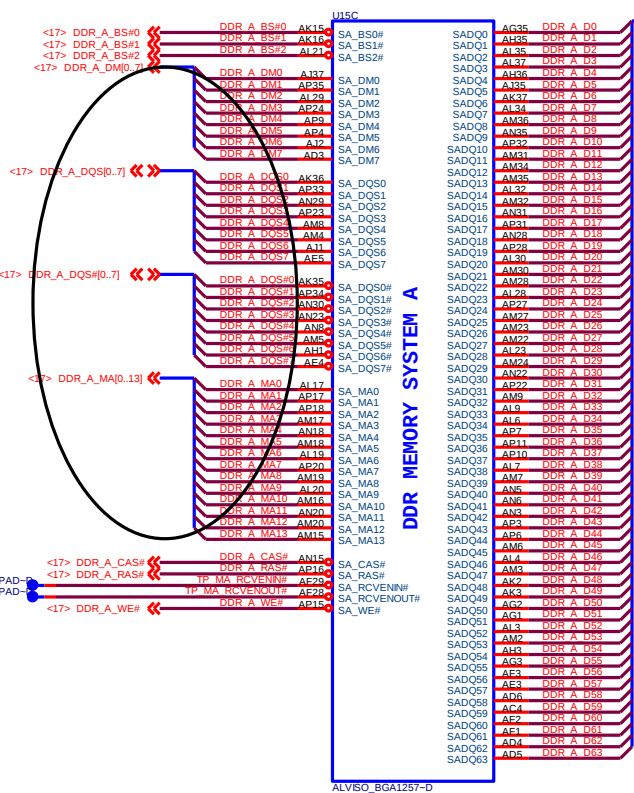
Dothan Processor(2/2)

LA-2171

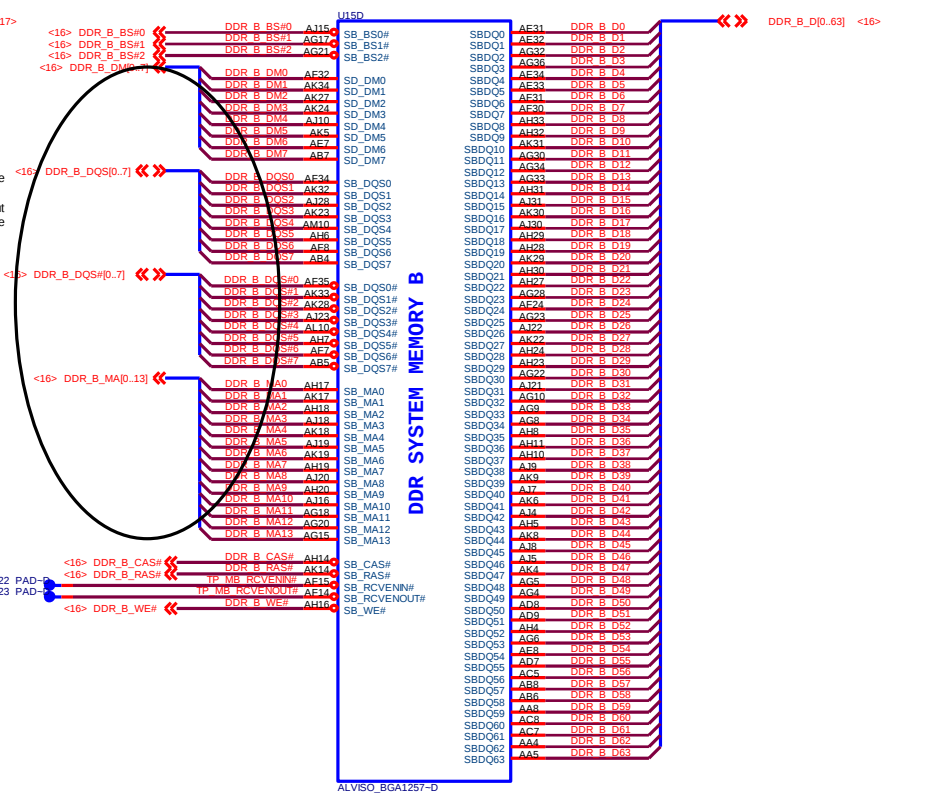
12/2004 8 of 50

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This Symbol as same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.



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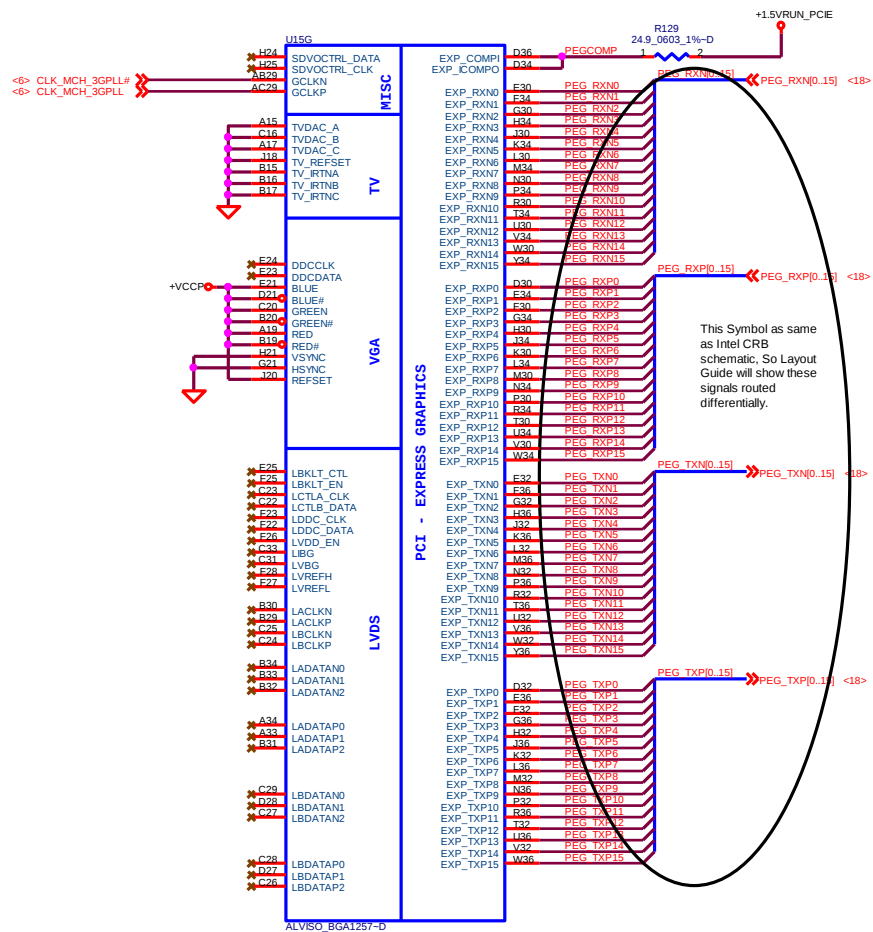
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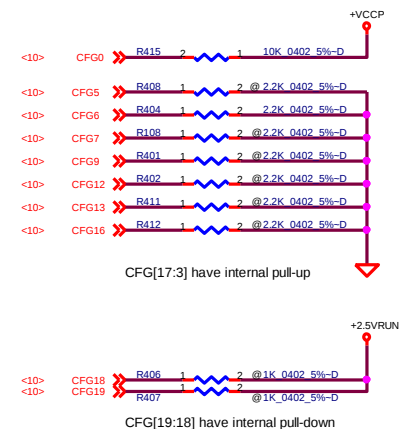


Title		Alviso(2 of 5)	
Size	LA-2171	Rev	0.2
Date	12/2004	Sheet	11 of 50

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CFG[2:0]	Refer to sheet 6 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II * High = DDR-I
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V



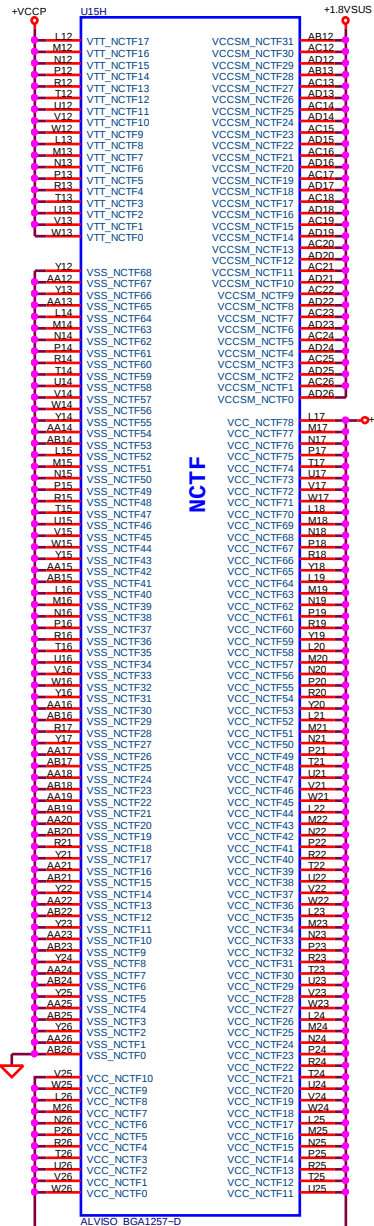
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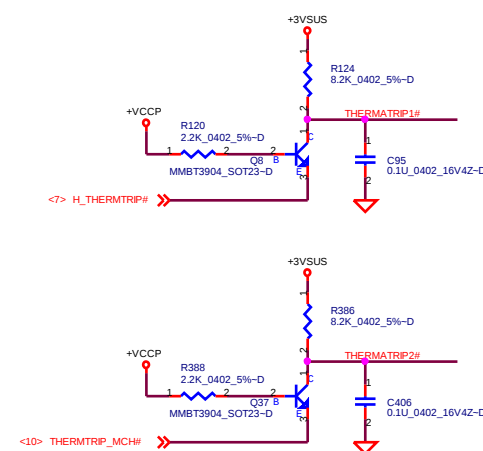
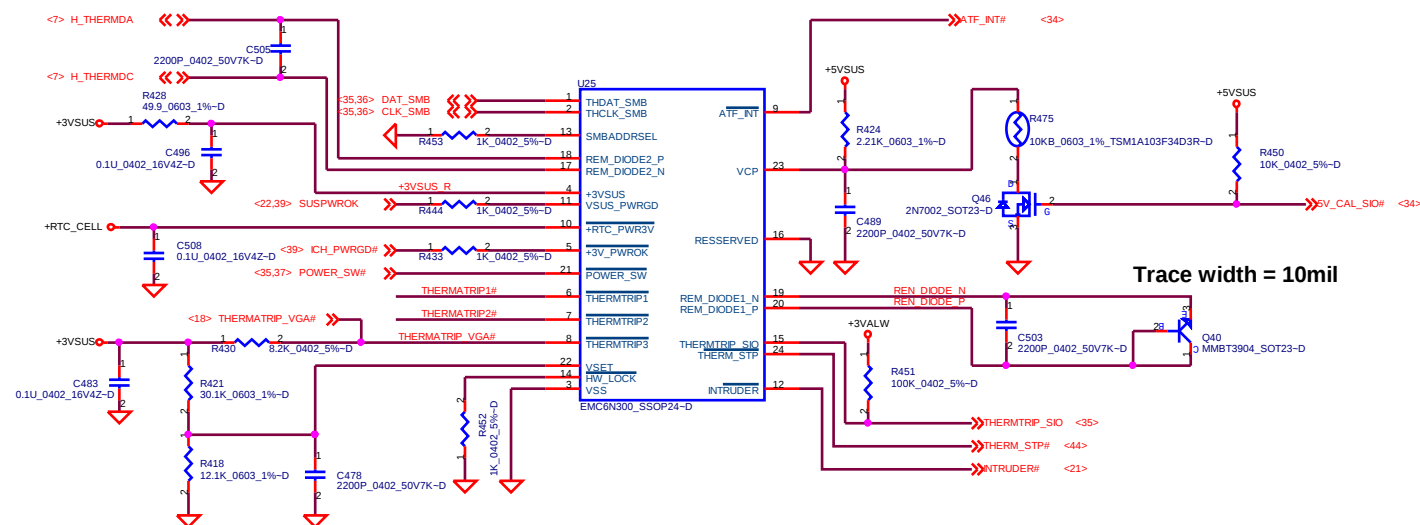
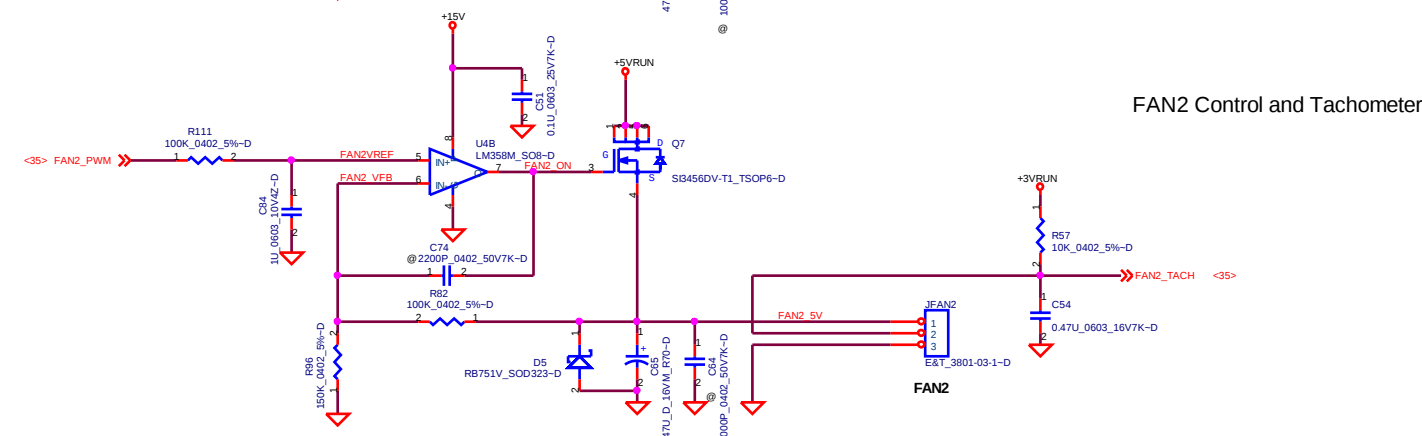
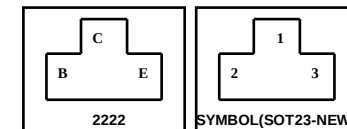
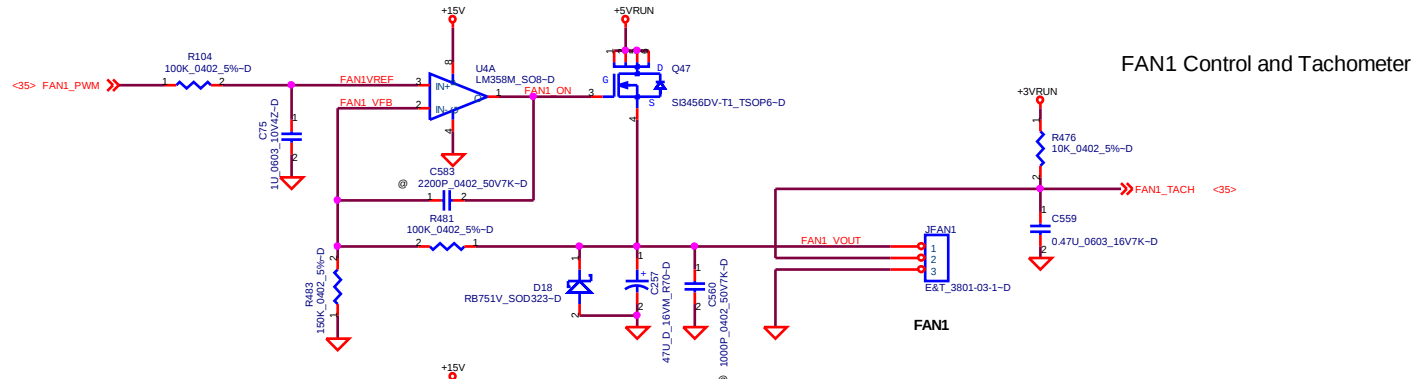
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Alviso(3 of 5)

Title	Document Number	Rev
LA-2171	LA-2171	0.2
Date	12/2004	Sheet 12 of 50

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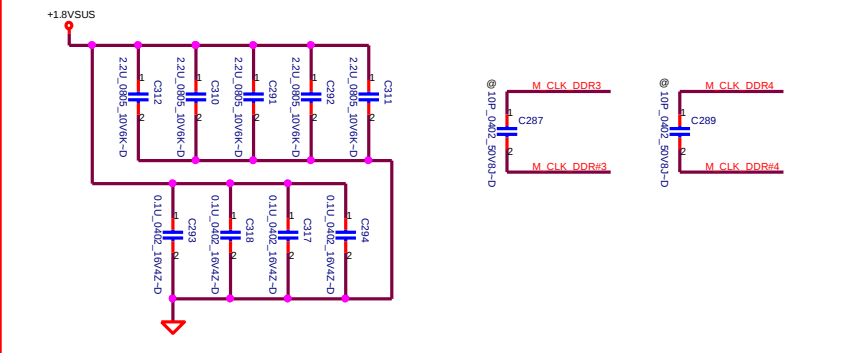
Thermal sensor and Fan

Size	Document Number	Rev
12	LA-2171	0.2

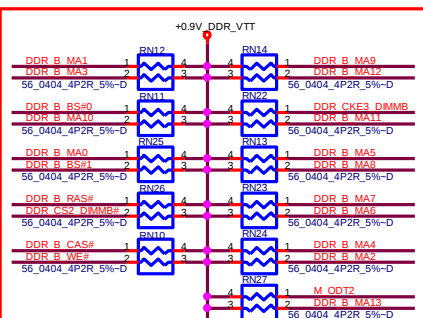
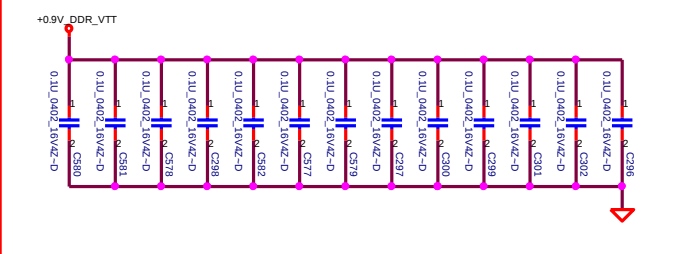
Date: 12/2004 Sheet: 15 of 50

<11> DDR_B_DQS[0..7] <<>>
 <11> DDR_B_D[0..63] <<>>
 <11> DDR_B_DM[0..7] <<>>
 <11> DDR_B_DQS[0..7] <<>>
 <11> DDR_B_MA[0..13] <<>>

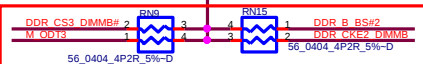
Layout Note:
Place near JDIM1



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT



Layout Note:
Place these resistor
closely JDIM1,all
trace length<750 mil



Layout Note:
Place these resistor
closely JDIM1,all
trace length
Max<1.3"



DIMM
STANDARD

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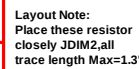
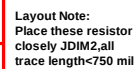
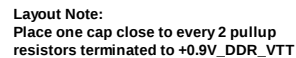
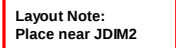
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DDR-II-SODIMM SLOT1

Size Document Number
LA-2171

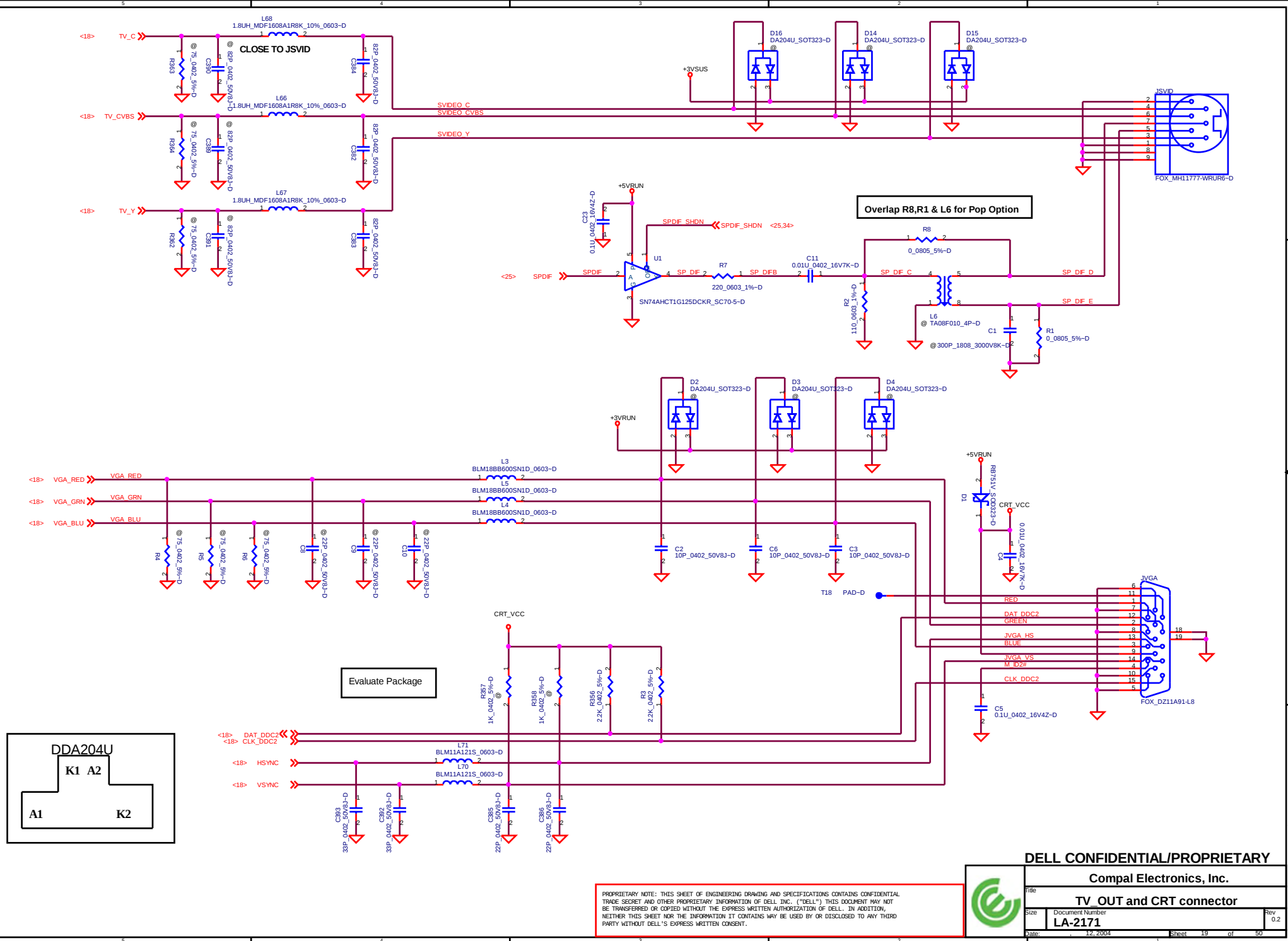
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LA-2171				
Date: 12/20/04	Sheet: 17	of	50	

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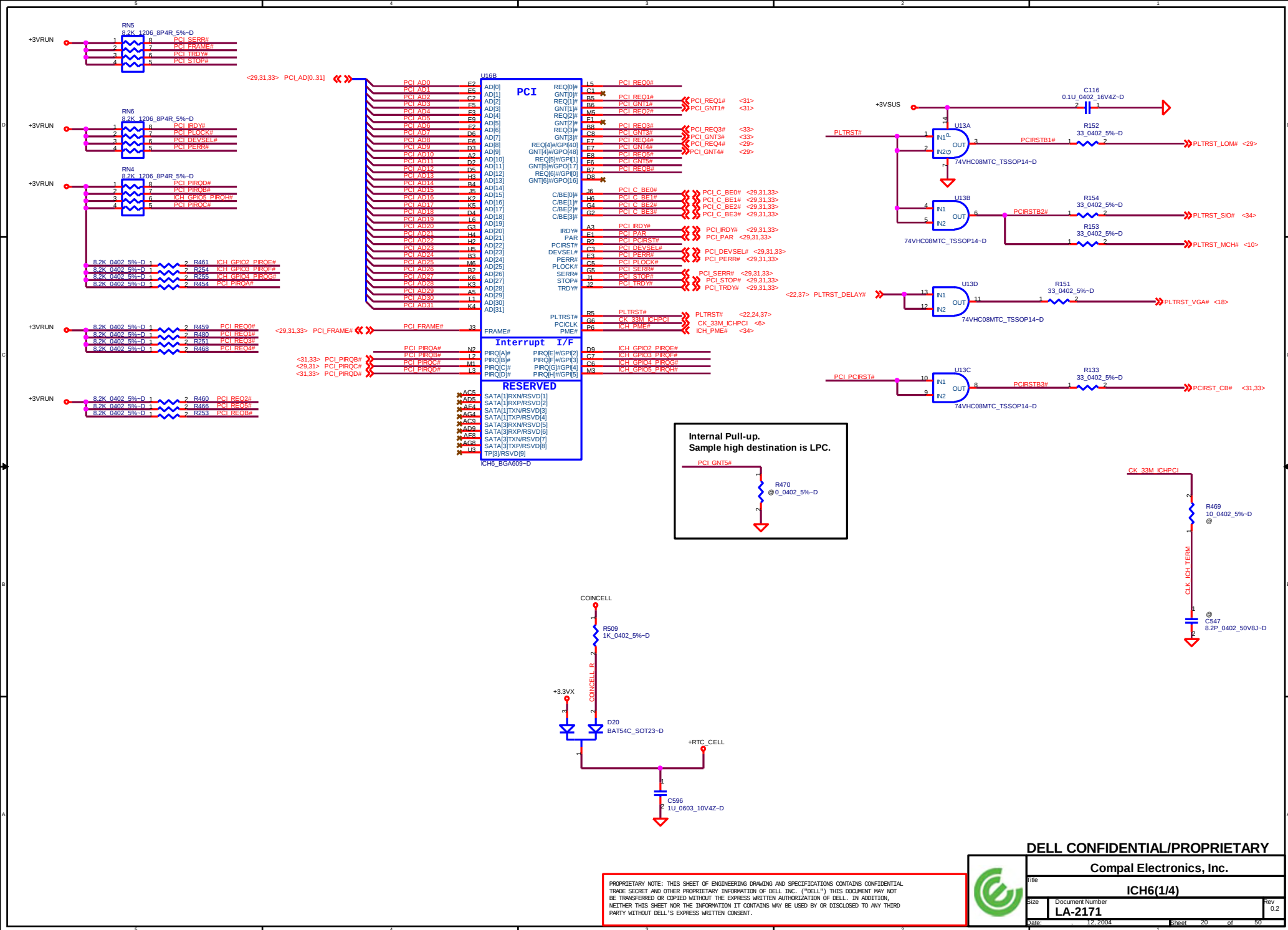
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TV OUT and CRT connector

Document Number
LA-2171

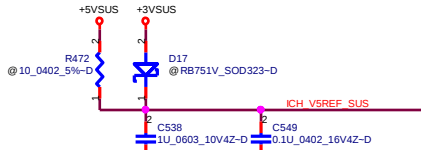
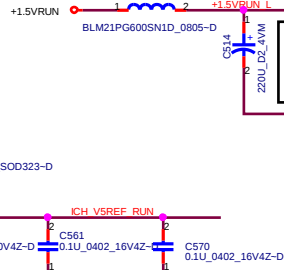
Rev 0.1

Date: 12.2004 Sheet 19 of 50



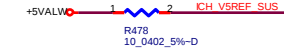
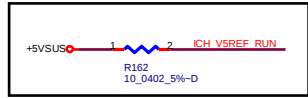
Title: ICH6(3/4)
 Size: Document Number
 LA-2171
 Date: 12, 2004 Sheet 22 of 50

Near PIN F27(C968),
P27(C949), AB27(C950)



Replacing by this circuit?

Note: Intel will update design guide.



Near PIN AG5

Near PIN AG9

Near PIN E26, E27

Near PIN AE1

Near PIN A17

Near PIN AC27

CODE

IDE

PCI

USB

USB CORE

PCI/IDE RBP

VCC1_5[98]

VCC1_5[97]

VCC1_5[96]

VCC1_5[95]

VCC1_5[94]

VCC1_5[93]

VCC1_5[92]

VCC1_5[91]

VCC1_5[90]

VCC1_5[89]

VCC1_5[88]

VCC1_5[87]

VCC1_5[86]

VCC1_5[85]

VCC1_5[84]

VCC1_5[83]

VCC1_5[82]

VCC1_5[81]

VCC1_5[80]

VCC1_5[79]

VCC1_5[78]

VCC1_5[77]

VCC1_5[76]

VCC1_5[75]

VCC1_5[74]

VCC1_5[73]

VCC1_5[72]

VCC1_5[71]

VCC1_5[70]

VCC1_5[69]

VCC1_5[68]

VCC1_5[67]

VCC1_5[66]

VCC1_5[65]

VCC1_5[64]

VCC1_5[63]

VCC1_5[62]

VCC1_5[61]

VCC1_5[60]

VCC1_5[59]

VCC1_5[58]

VCC1_5[57]

VCC1_5[56]

VCC1_5[55]

VCC1_5[54]

VCC1_5[53]

VCC1_5[52]

VCC1_5[51]

VCC1_5[50]

VCC1_5[49]

VCC1_5[48]

VCC1_5[47]

VCC1_5[46]

VCC1_5[45]

VCC1_5[44]

VCC1_5[43]

VCC1_5[42]

VCC1_5[41]

VCC1_5[40]

VCC1_5[39]

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VCC1_5[9]

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VCC1_5[6]

VCC1_5[5]

VCC1_5[4]

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VCC1_5[-1]

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VCC1_5[-132]

VCC1_5[-133]

VCC1_5[-134]

VCC1_5[-135]

VCC1_5[-136]

VCC1_5[-137]

VCC1_5[-138]

VCC1_5[-139]

VCC1_5[-140]

VCC1_5[-141]

VCC1_5[-142]

VCC1_5[-143]

VCC1_5[-144]

VCC1_5[-145]

VCC1_5[-146]

VCC1_5[-147]

VCC1_5[-148]

VCC1_5[-149]

VCC1_5[-150]

VCC1_5[-151]

VCC1_5[-152]

VCC1_5[-153]

VCC1_5[-154]

VCC1_5[-155]

VCC1_5[-156]

VCC1_5[-157]

VCC1_5[-158]

VCC1_5[-159]

VCC1_5[-160]

VCC1_5[-161]

VCC1_5[-162]

VCC1_5[-163]

VCC1_5[-164]

VCC1_5[-165]

VCC1_5[-166]

VCC1_5[-167]

VCC1_5[-168]

VCC1_5[-169]

VCC1_5[-170]

VCC1_5[-171]

VCC1_5[-172]

VCC1_5[-173]

VCC1_5[-174]

VCC1_5[-175]

VCC1_5[-176]

VCC1_5[-177]

The schematic diagram illustrates the signal path of a SATA to SATA-Express adapter. It starts with a SATA connector on the left, showing pins for XTALIN, XTALOUT, GND, and VSS_SATA. The signal path includes a 25MHz 20pF load capacitor (X7), a 0.0402 5% resistor (R493), a 1M 0.402 5% resistor (R494), a 33pF 0.402 50V B3-D capacitor (C593), and a 33 0.402 5% resistor (R499). The signal then passes through a parallel ATA controller (U28) and a SATA-Express connector (88SAB040_TQFP64-D). The SATA-Express connector pins are labeled with their respective signals: HD00, HD01, HD02, HD03, HD04, HD05, HD06, HD07, HD08, HD09, HD10, HD11, HD12, HD13, HD14, HD15, HDA0, HDA1, HCS0#, HCS1#, HCS1#, HINTRQ#, HDMACK#, HICRDY#, HD0R#, HD0RW#, HD0RQ#, HRESSET#, HPMQ#, and UA0, UA1.

T4	T3	
0	0	20MHz
0	1	25MHz
1	0	30MHz
1	1	40MHz

Pin Name	Pin No.	Int. PU/PD	Settings
SATATEST0	33	PD	NC
SATATEST1	34	PU	NC
SATATEST2	35	PD	NC
SATATEST3	36	PD	1
SATATEST4	37	PD	NC
SATATEST5	38	PU	0
SATATEST6	39	PD	1
SATATEST7	40	PD	NC
CFG0	20	PD	NC
CFG1	19	PU	0
CFG2	18	PD	NC

Diagram illustrating the configuration of the SATA RXN0 and RXPO registers. The RXN0 register (C482) and RXPO register (C486) are shown with their respective bit fields. The RXN0 register has a value of 0x01U_0402_16V7K-D, and the RXPO register has a value of 0x01U_0402_16V7K-D. The RXN0 register has a bit 2 set to 1, and the RXPO register has a bit 2 set to 0. The RXN0 register is labeled SATA_RXN0_C <21> and the RXPO register is labeled SATA_RXPO_C <21>.

The diagram shows the pinout for the SUNV_B0095AR050G1T-D component, which is a 50-pin device. The pins are numbered 1 to 50. The connections are as follows:

- Pin 1:** C350, 47P_0402_50V8J3-D
- Pin 2:** JMOD
- Pin 3:** IDE DD7
- Pin 4:** IDE DD8
- Pin 5:** IDE DD9
- Pin 6:** IDE DD10
- Pin 7:** IDE DD11
- Pin 8:** IDE DD12
- Pin 9:** IDE DD13
- Pin 10:** IDE DD14
- Pin 11:** IDE DD15
- Pin 12:** IDE DD16
- Pin 13:** IDE DD17
- Pin 14:** IDE DD18
- Pin 15:** IDE DD19
- Pin 16:** IDE DD20
- Pin 17:** IDE DD21
- Pin 18:** IDE DD22
- Pin 19:** IDE DD23
- Pin 20:** IDE DD24
- Pin 21:** IDE DD25
- Pin 22:** IDE DD26
- Pin 23:** IDE DD27
- Pin 24:** IDE DD28
- Pin 25:** IDE DD29
- Pin 26:** IDE DD30
- Pin 27:** IDE DD31
- Pin 28:** IDE DD32
- Pin 29:** IDE DD33
- Pin 30:** IDE DD34
- Pin 31:** IDE DD35
- Pin 32:** IDE DD36
- Pin 33:** IDE DD37
- Pin 34:** IDE DD38
- Pin 35:** IDE DD39
- Pin 36:** IDE DD40
- Pin 37:** IDE DD41
- Pin 38:** IDE DD42
- Pin 39:** IDE DD43
- Pin 40:** IDE DD44
- Pin 41:** IDE DD45
- Pin 42:** IDE DD46
- Pin 43:** IDE DD47
- Pin 44:** IDE DD48
- Pin 45:** IDE DD49
- Pin 46:** IDE DD50
- Pin 47:** IDE DD51
- Pin 48:** IDE DD52
- Pin 49:** IDE DD53
- Pin 50:** IDE DD54

Other connections include:

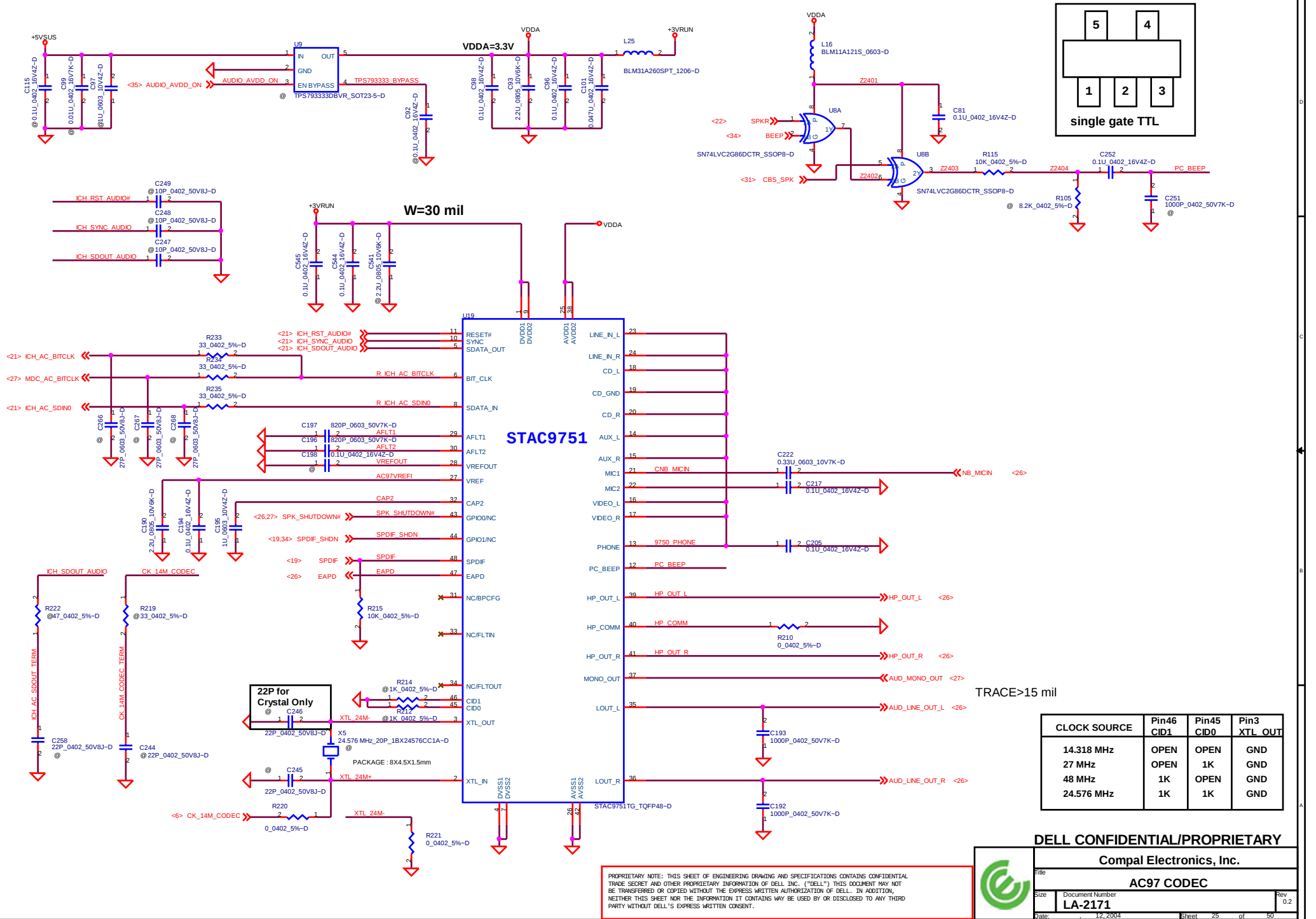
- Pin 1:** SEC_CSEL
- Pin 2:** RDREQ, IDE_DIOR#, +5VMOD
- Pin 3:** RPDACK#
- Pin 4:** PDIA#
- Pin 5:** RD_DA2, RD_DCS3#
- Pin 6:** RD_DA2, RD_DCS3#
- Pin 7:** RD_DA2, RD_DCS3#
- Pin 8:** RD_DA2, RD_DCS3#
- Pin 9:** RD_DA2, RD_DCS3#
- Pin 10:** RD_DA2, RD_DCS3#
- Pin 11:** RD_DA2, RD_DCS3#
- Pin 12:** RD_DA2, RD_DCS3#
- Pin 13:** RD_DA2, RD_DCS3#
- Pin 14:** RD_DA2, RD_DCS3#
- Pin 15:** RD_DA2, RD_DCS3#
- Pin 16:** RD_DA2, RD_DCS3#
- Pin 17:** RD_DA2, RD_DCS3#
- Pin 18:** RD_DA2, RD_DCS3#
- Pin 19:** RD_DA2, RD_DCS3#
- Pin 20:** RD_DA2, RD_DCS3#
- Pin 21:** RD_DA2, RD_DCS3#
- Pin 22:** RD_DA2, RD_DCS3#
- Pin 23:** RD_DA2, RD_DCS3#
- Pin 24:** RD_DA2, RD_DCS3#
- Pin 25:** RD_DA2, RD_DCS3#
- Pin 26:** RD_DA2, RD_DCS3#
- Pin 27:** RD_DA2, RD_DCS3#
- Pin 28:** RD_DA2, RD_DCS3#
- Pin 29:** RD_DA2, RD_DCS3#
- Pin 30:** RD_DA2, RD_DCS3#
- Pin 31:** RD_DA2, RD_DCS3#
- Pin 32:** RD_DA2, RD_DCS3#
- Pin 33:** RD_DA2, RD_DCS3#
- Pin 34:** RD_DA2, RD_DCS3#
- Pin 35:** RD_DA2, RD_DCS3#
- Pin 36:** RD_DA2, RD_DCS3#
- Pin 37:** RD_DA2, RD_DCS3#
- Pin 38:** RD_DA2, RD_DCS3#
- Pin 39:** RD_DA2, RD_DCS3#
- Pin 40:** RD_DA2, RD_DCS3#
- Pin 41:** RD_DA2, RD_DCS3#
- Pin 42:** RD_DA2, RD_DCS3#
- Pin 43:** RD_DA2, RD_DCS3#
- Pin 44:** RD_DA2, RD_DCS3#
- Pin 45:** RD_DA2, RD_DCS3#
- Pin 46:** RD_DA2, RD_DCS3#
- Pin 47:** RD_DA2, RD_DCS3#
- Pin 48:** RD_DA2, RD_DCS3#
- Pin 49:** RD_DA2, RD_DCS3#
- Pin 50:** RD_DA2, RD_DCS3#

Additional components and labels include:

- SEC_CSEL** (Pin 1)
- RDREQ** (Pin 2)
- IDE_DIOR#** (Pin 2)
- +5VMOD** (Pin 2)
- RPDACK#** (Pin 3)
- PDIA#** (Pin 4)
- RD_DA2** (Pin 5)
- RD_DCS3#** (Pin 5)
- RD_DA2** (Pin 6)
- RD_DCS3#** (Pin 6)
- RD_DA2** (Pin 7)
- RD_DCS3#** (Pin 7)
- RD_DA2** (Pin 8)
- RD_DCS3#** (Pin 8)
- RD_DA2** (Pin 9)
- RD_DCS3#** (Pin 9)
- RD_DA2** (Pin 10)
- RD_DCS3#** (Pin 10)
- RD_DA2** (Pin 11)
- RD_DCS3#** (Pin 11)
- RD_DA2** (Pin 12)
- RD_DCS3#** (Pin 12)
- RD_DA2** (Pin 13)
- RD_DCS3#** (Pin 13)
- RD_DA2** (Pin 14)
- RD_DCS3#** (Pin 14)
- RD_DA2** (Pin 15)
- RD_DCS3#** (Pin 15)
- RD_DA2** (Pin 16)
- RD_DCS3#** (Pin 16)
- RD_DA2** (Pin 17)
- RD_DCS3#** (Pin 17)
- RD_DA2** (Pin 18)
- RD_DCS3#** (Pin 18)
- RD_DA2** (Pin 19)
- RD_DCS3#** (Pin 19)
- RD_DA2** (Pin 20)
- RD_DCS3#** (Pin 20)
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- RD_DCS3#** (Pin 21)
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- RD_DCS3#** (Pin 22)
- RD_DA2** (Pin 23)
- RD_DCS3#** (Pin 23)
- RD_DA2** (Pin 24)
- RD_DCS3#** (Pin 24)
- RD_DA2** (Pin 25)
- RD_DCS3#** (Pin 25)
- RD_DA2** (Pin 26)
- RD_DCS3#** (Pin 26)
- RD_DA2** (Pin 27)
- RD_DCS3#** (Pin 27)
- RD_DA2** (Pin 28)
- RD_DCS3#** (Pin 28)
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- RD_DCS3#** (Pin 29)
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- RD_DCS3#** (Pin 42)
- RD_DA2** (Pin 43)
- RD_DCS3#** (Pin 43)
- RD_DA2** (Pin 44)
- RD_DCS3#** (Pin 44)
- RD_DA2** (Pin 45)
- RD_DCS3#** (Pin 45)
- RD_DA2** (Pin 46)
- RD_DCS3#** (Pin 46)
- RD_DA2** (Pin 47)
- RD_DCS3#** (Pin 47)
- RD_DA2** (Pin 48)



Size	Document Number	Rev
	LA-2171	0.2
Date:	12, 2004	Sheet 24 of 50



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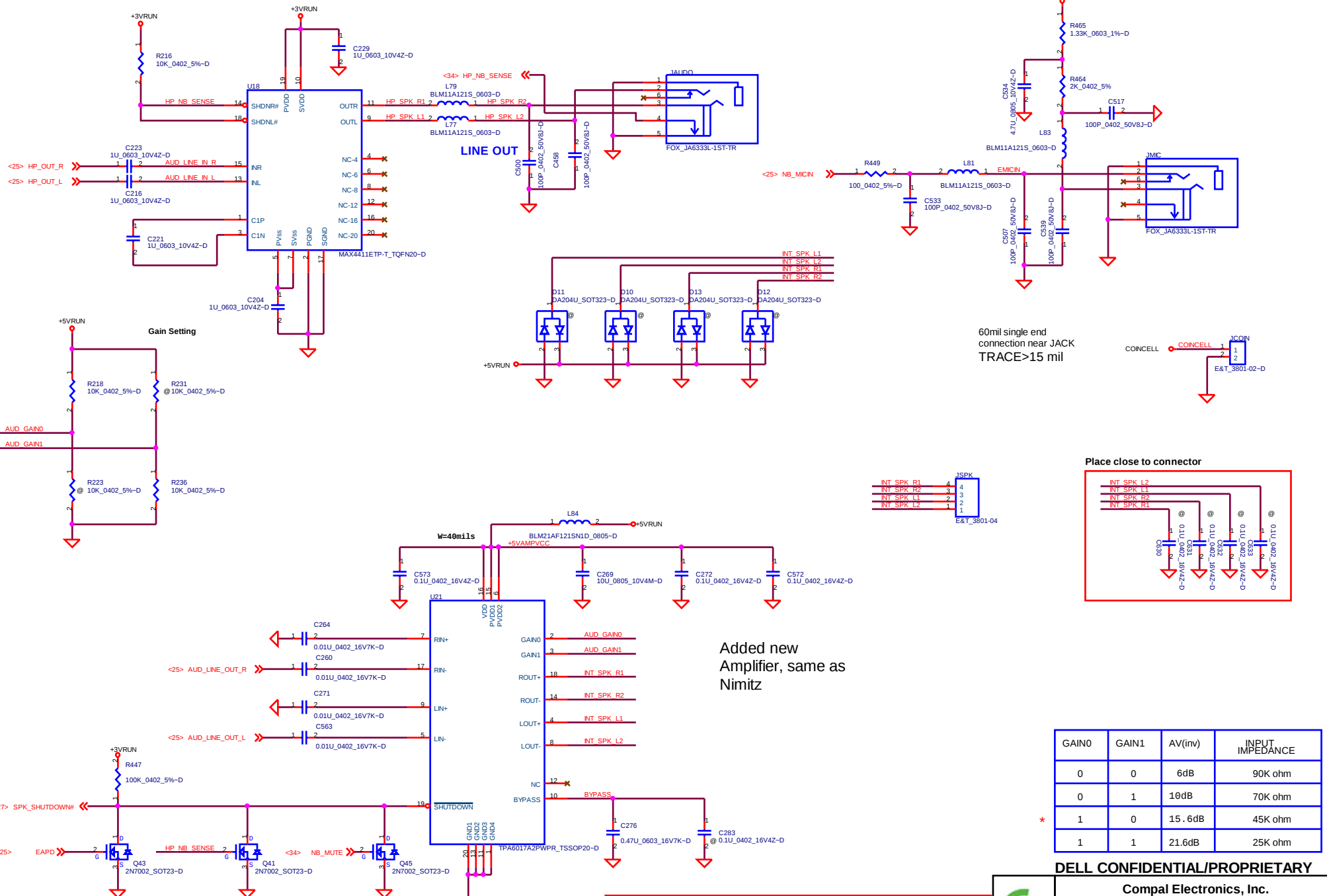
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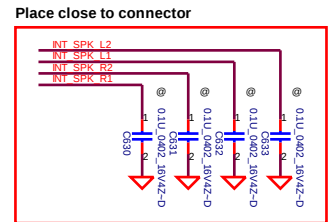
AC97 CODEC

Size	Document Number	Rev
LA-2171		0.2

Date: 12/2004 Sheet: 25 of 50



60mil single end
connection near JACK
TRACE>15 mil



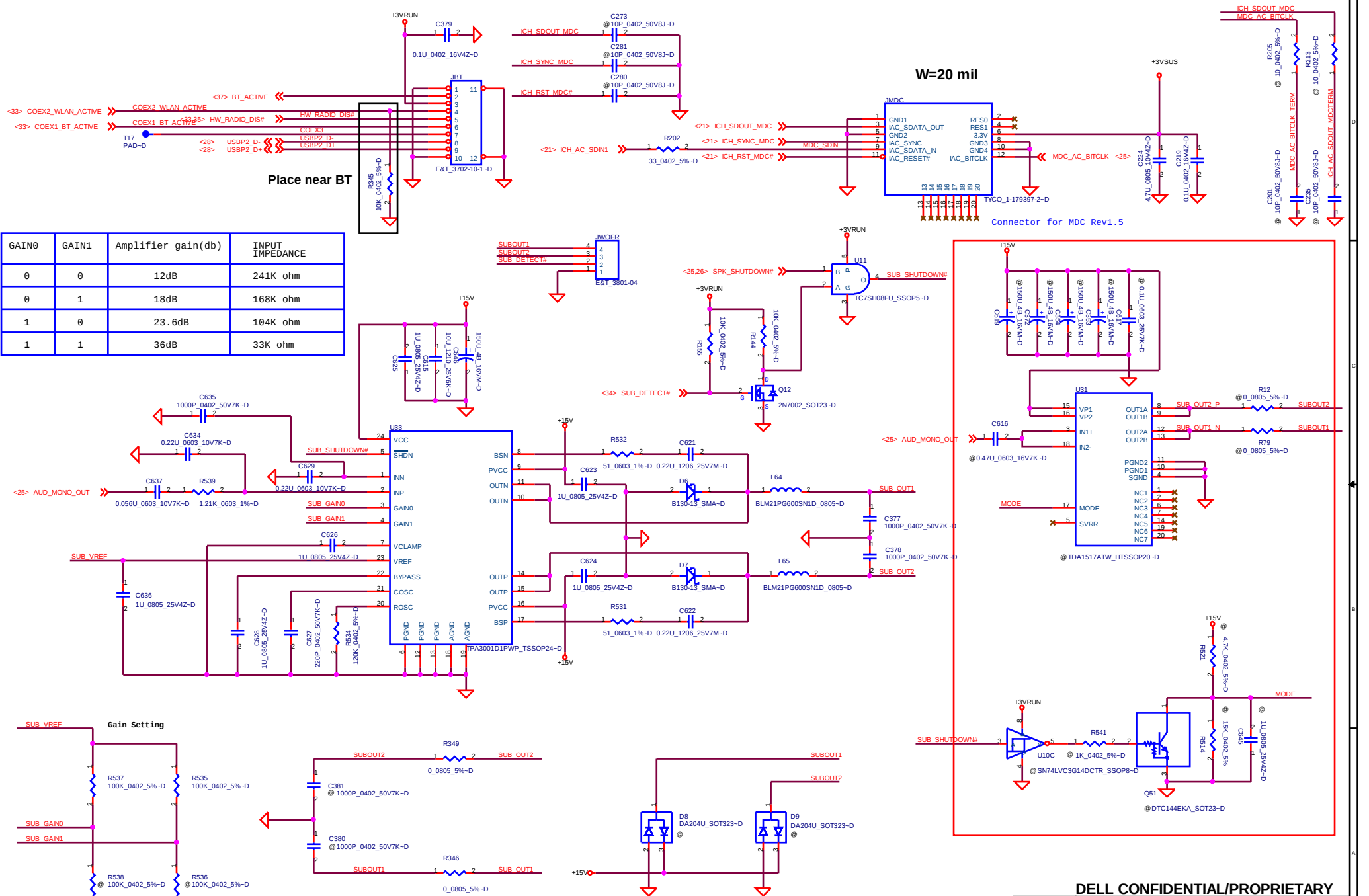
GAIN0	GAIN1	AV(inv)	INPUT IMPEDANCE
0	0	6dB	90K ohm
0	1	10dB	70K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	25K ohm

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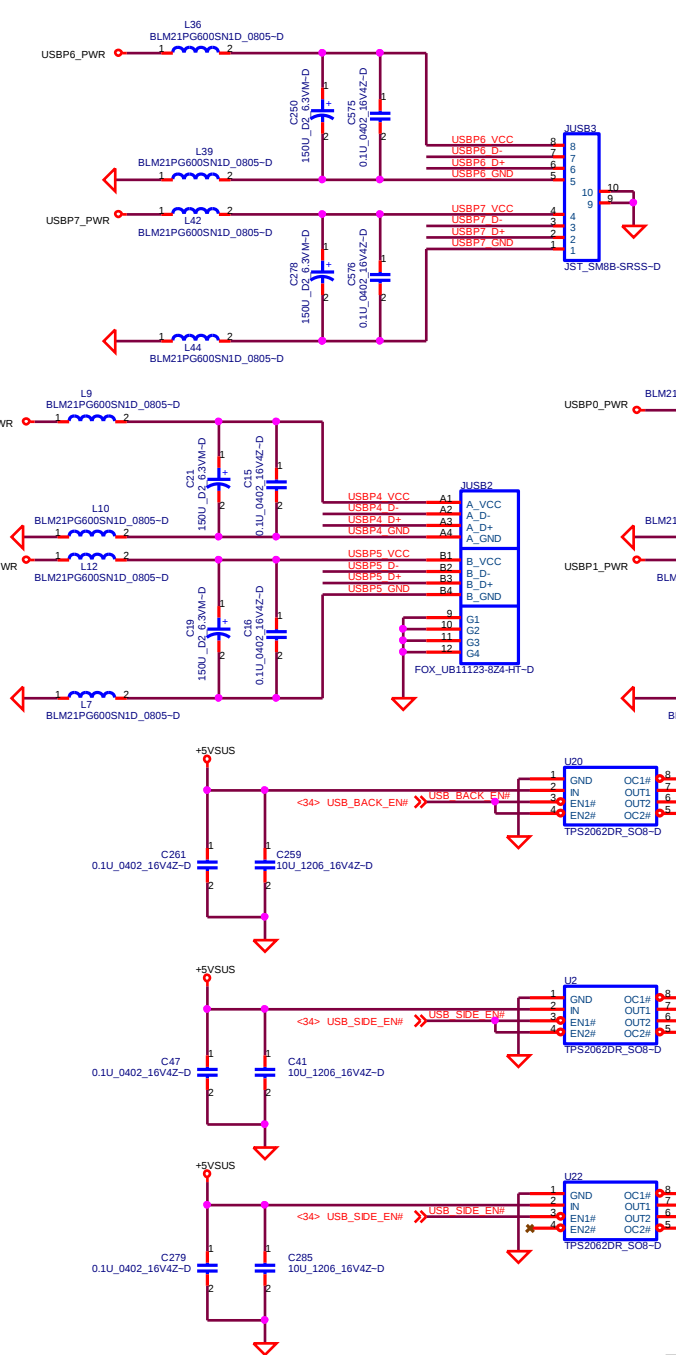
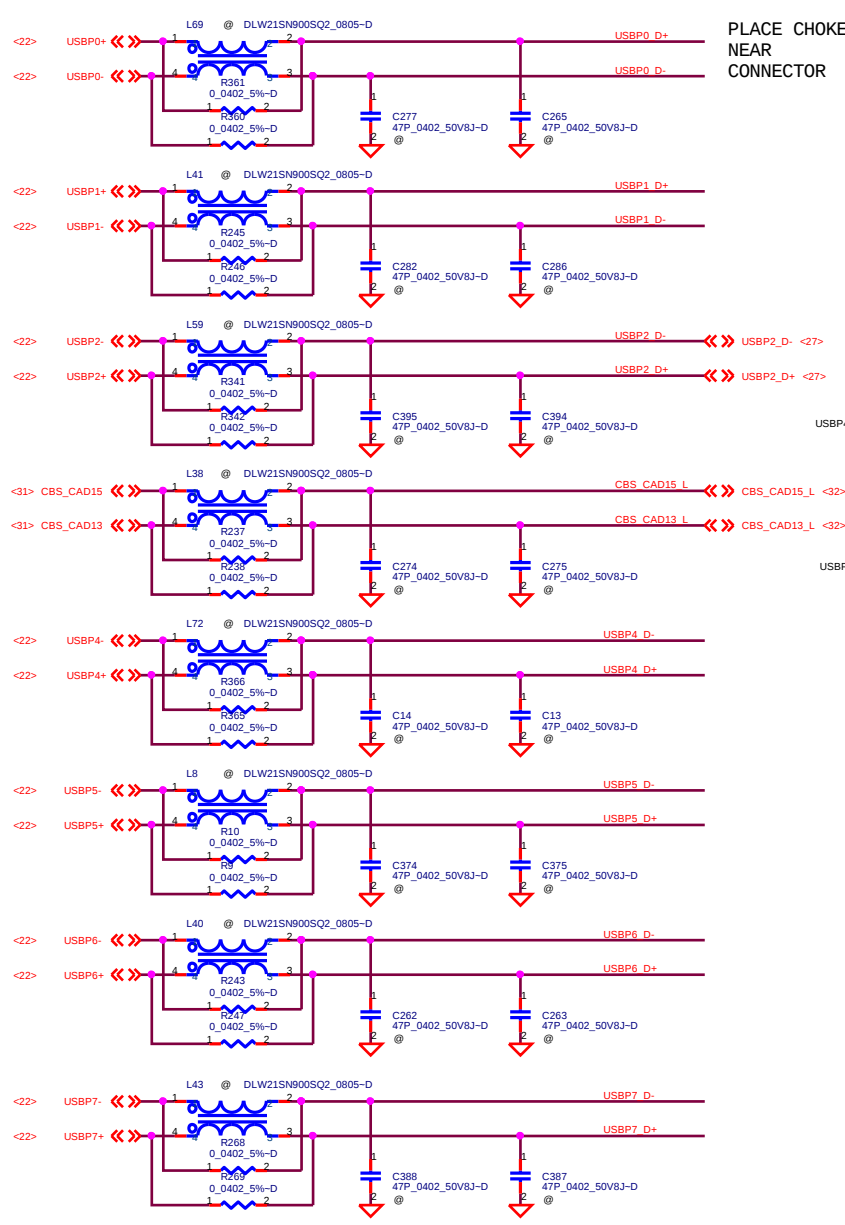
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Amplifier and Phone Jack	
LA-2171	Rev 0.2
Date: 12, 2004	Sheet: 26 of 50

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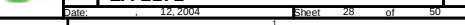
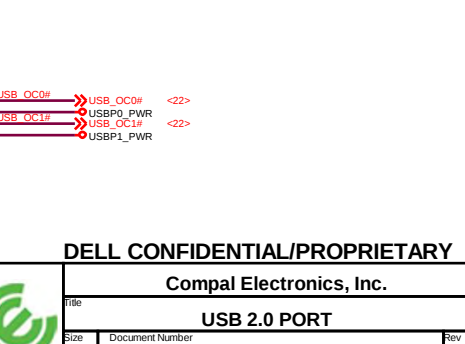
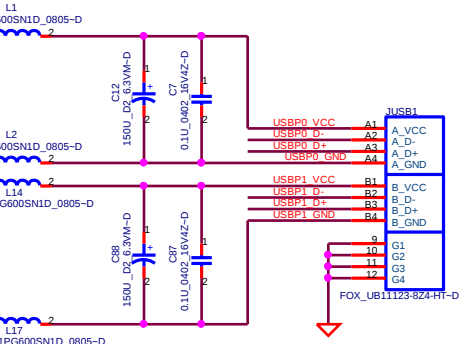


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USB PORT#	DESTINATION
0	JUSB1 (Top)
1	JUSB1 (Bottom)
2	BlueTooth
3	NEW CARD
4	JUSB2 (Top)
5	JUSB2 (Bottom)
6	JUSB3 (Top)
7	JUSB3 (Bottom)



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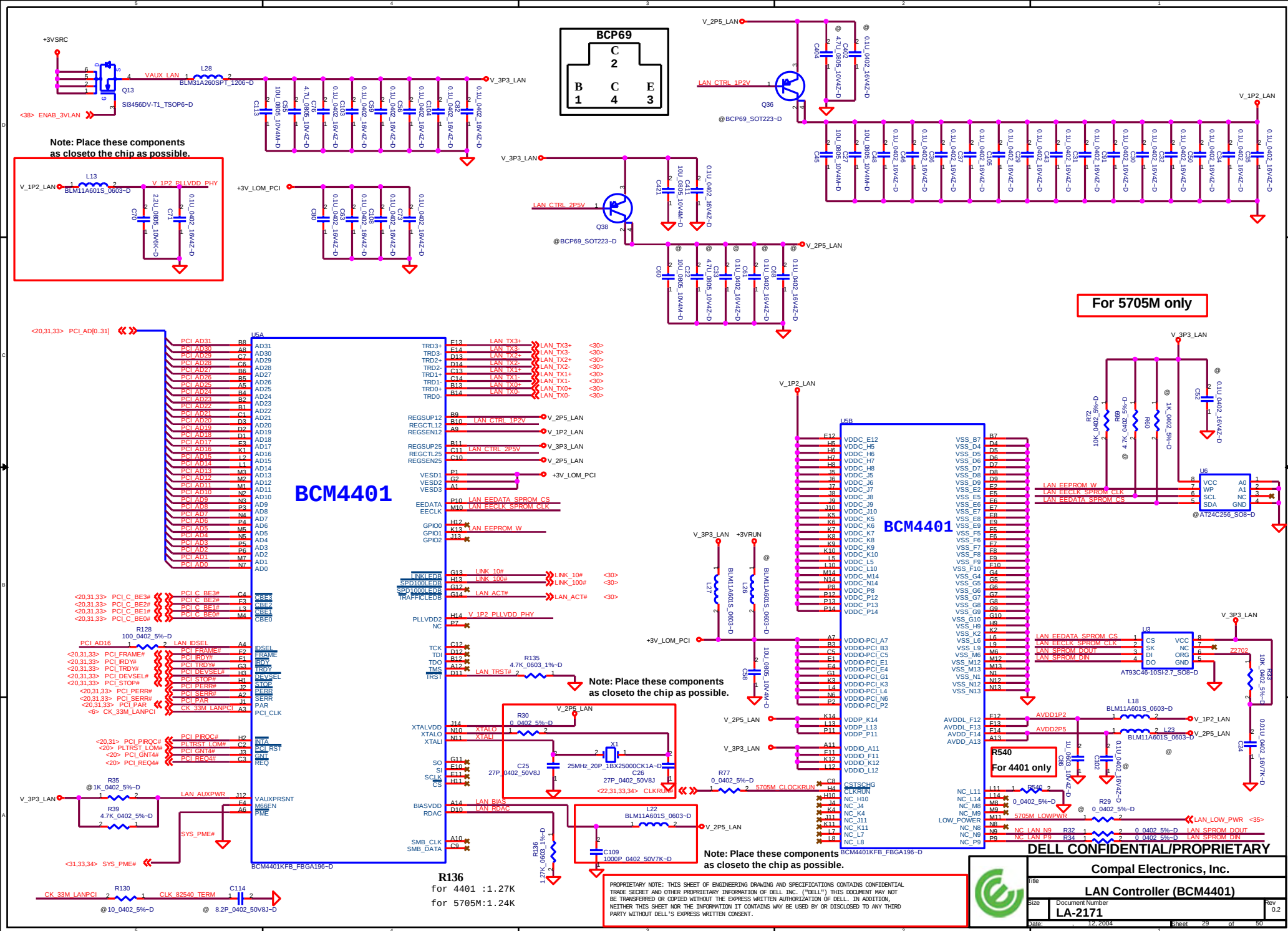
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USB 2.0 PORT

Size: Document Number
LA-2171

Date: 12, 2004 Sheet: 28 of 50



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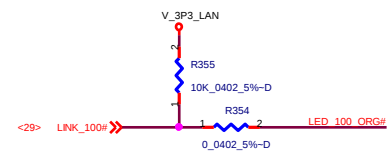
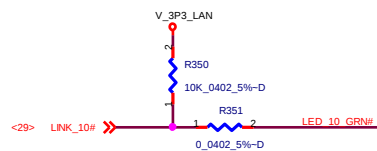
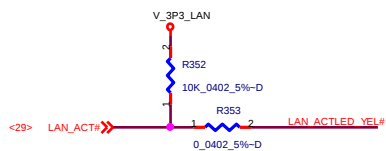
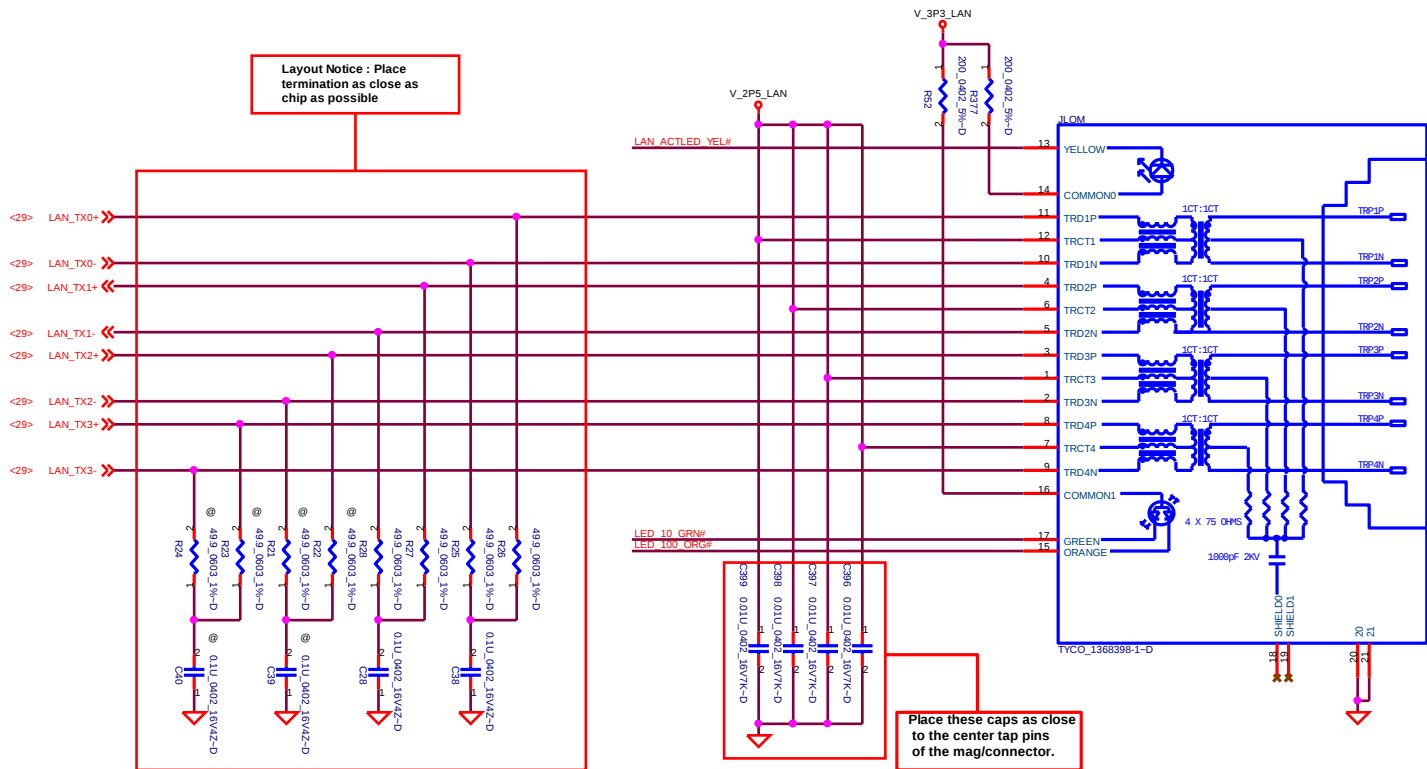
LAN Controller (BCM4401)

Size	Document Number
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LA-2171

Rev
0.2

Date: 12.2004 Sheet 29 of 50



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LAN Transfomer and RJ45

Document Number

LA-2171

Rev

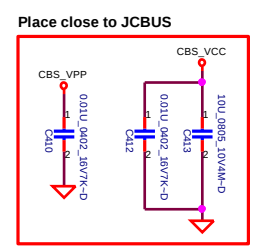
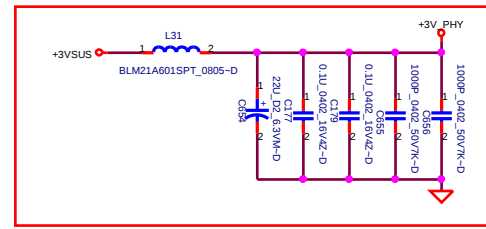
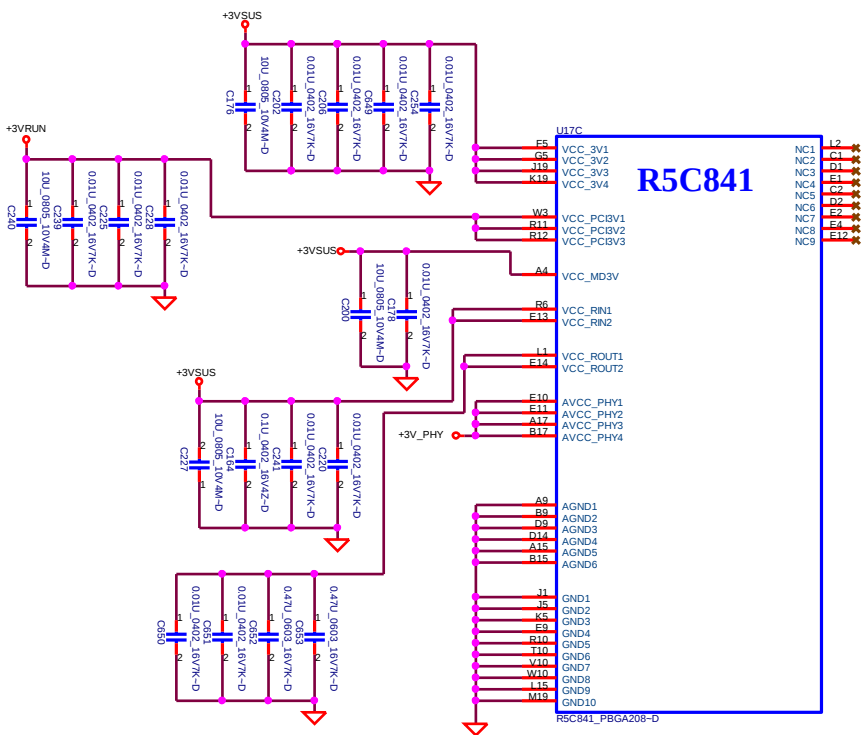
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Date 12/2004

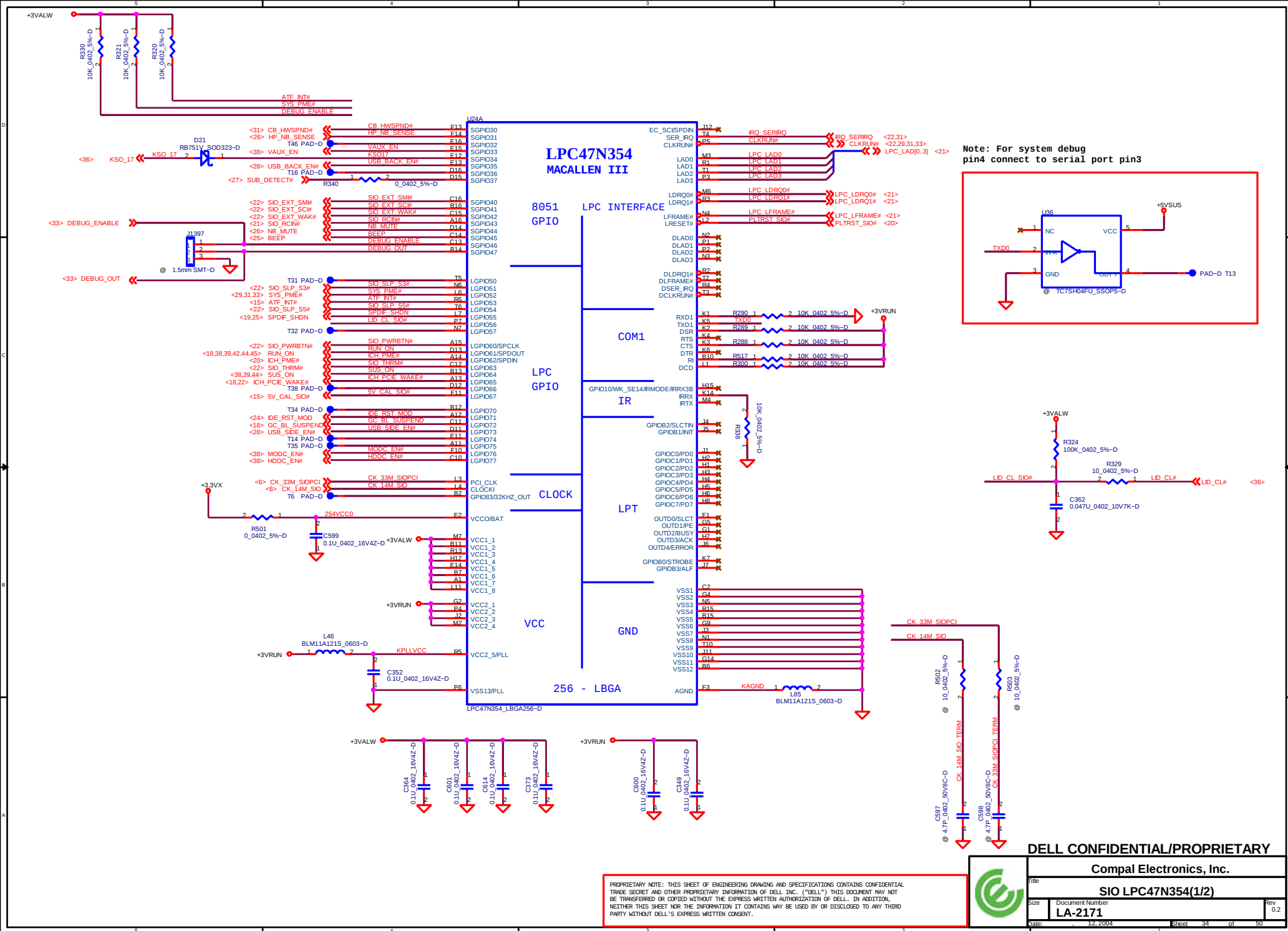
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Title		MINIPCI		Rev	0.2
Size	Document Number				
	LA-2171				
Date	12/2004	Sheet	33	of	50



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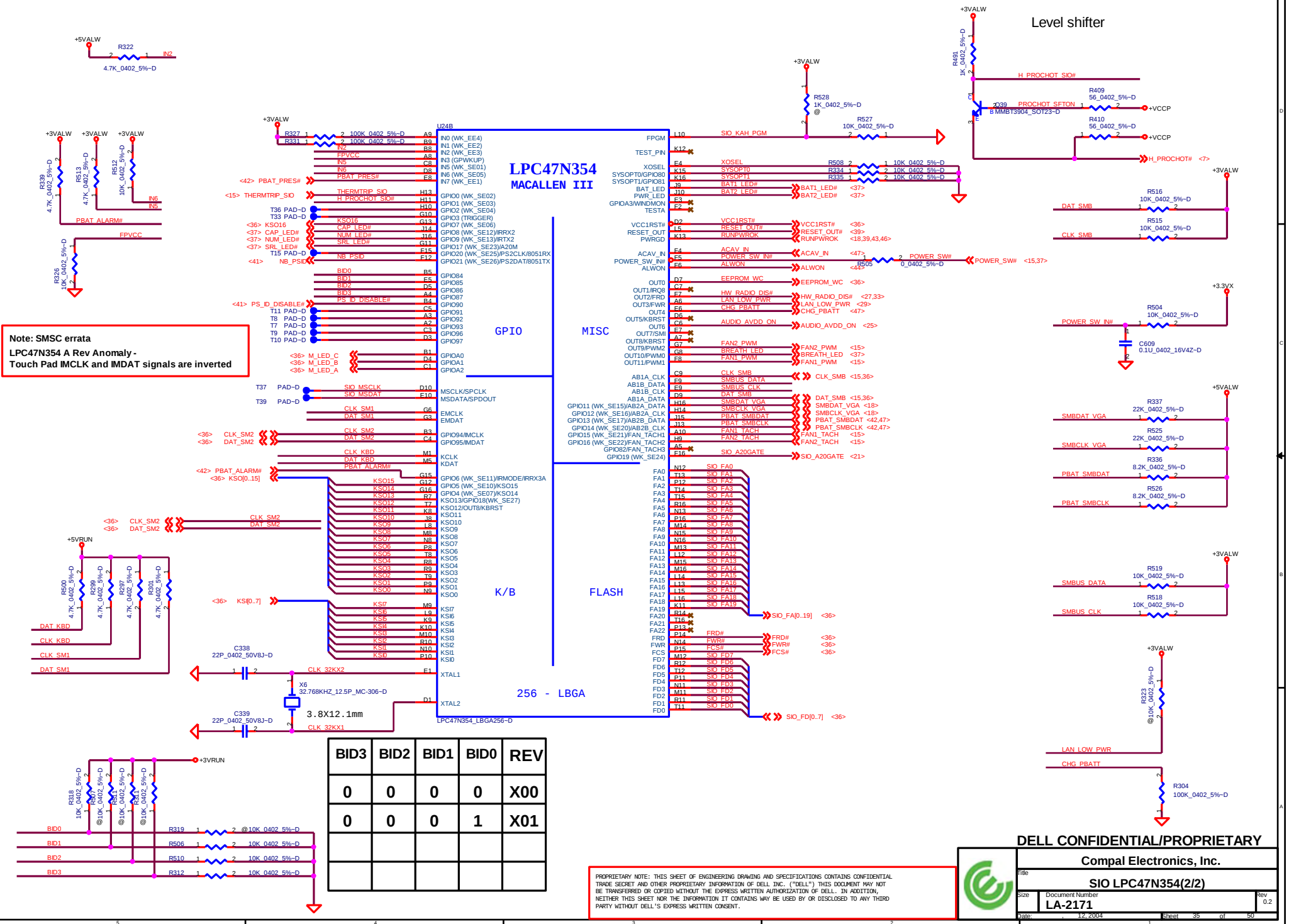
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SIO LPC47N354(1/2)

Size	Document Number	Rev
	LA-2171	0.2
Date	12/2004	Sheet 34 of 50

Note: SMSC errata
LPC47N354 A Rev Anomaly -
Touch Pad IMCLK and IMDAT signals are inverted



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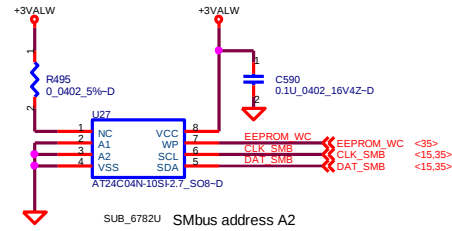
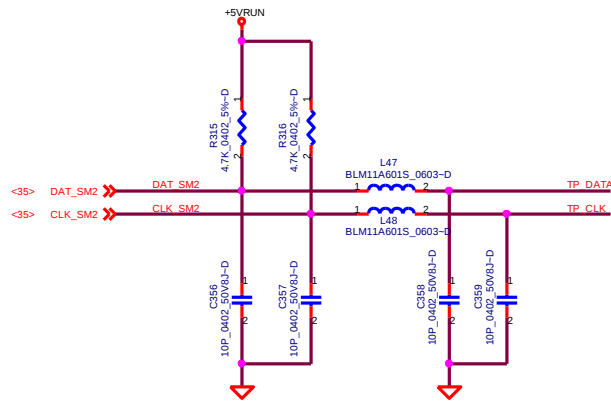
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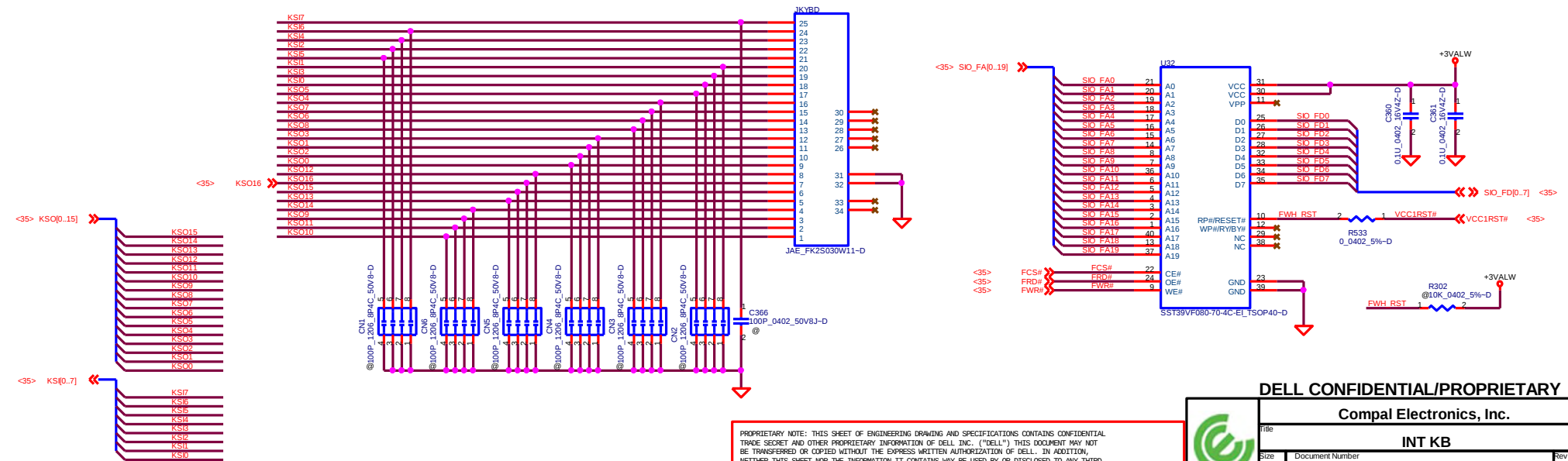
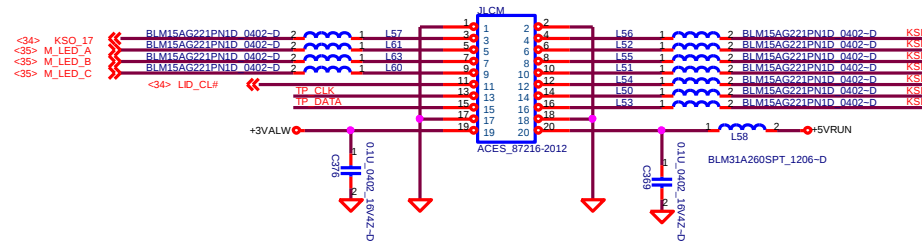
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Note: SMSC errata
LPC47N354 A Rev Anomaly - Touch Pad IMCLK and IMDAT signals are inverted



LCM & Direct play SW & T PAD



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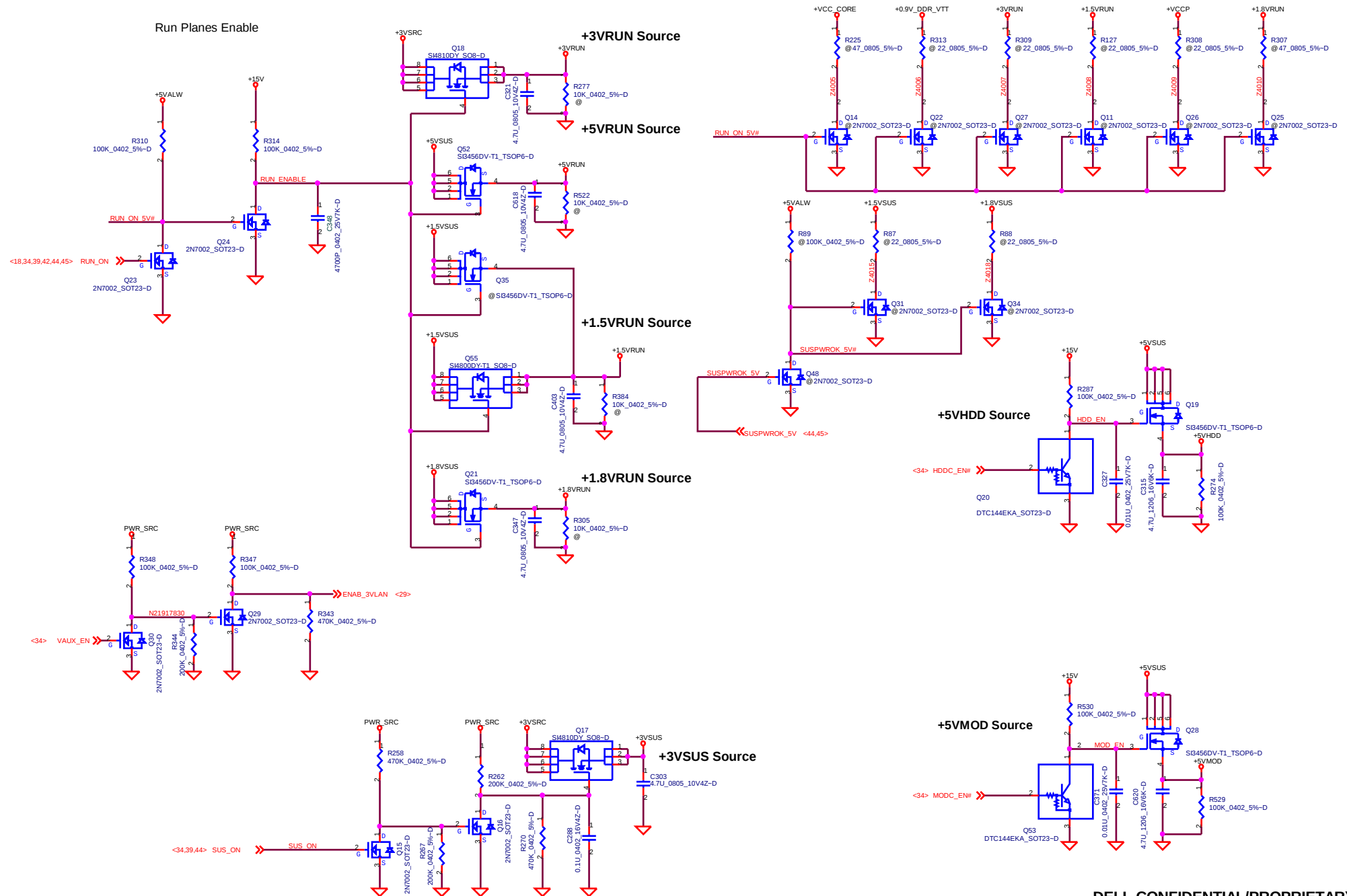
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Size	Document Number	Rev
	LA-2171	0.2
Date	12/2004	Sheet 36 of 50

Run Planes Enable



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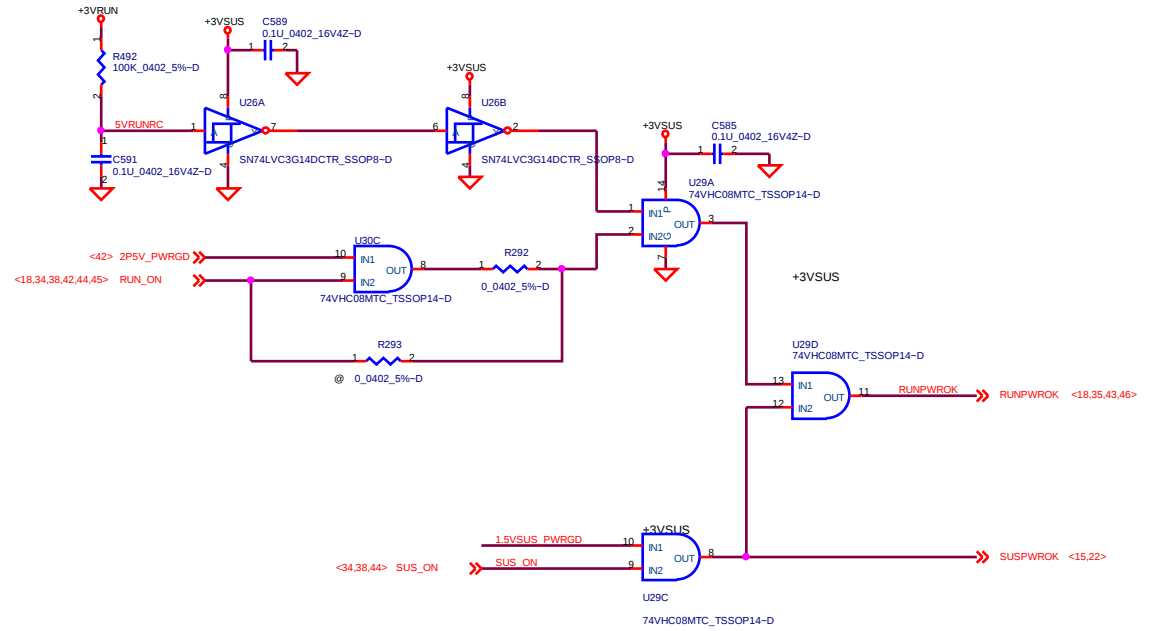
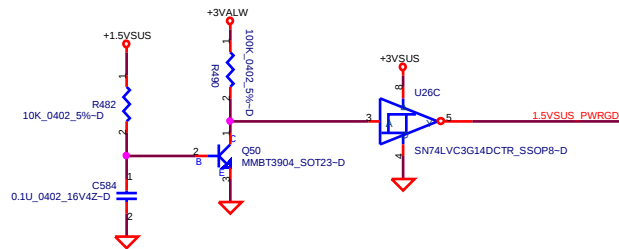
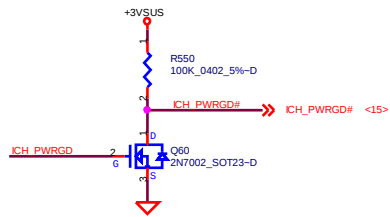
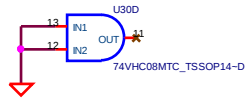
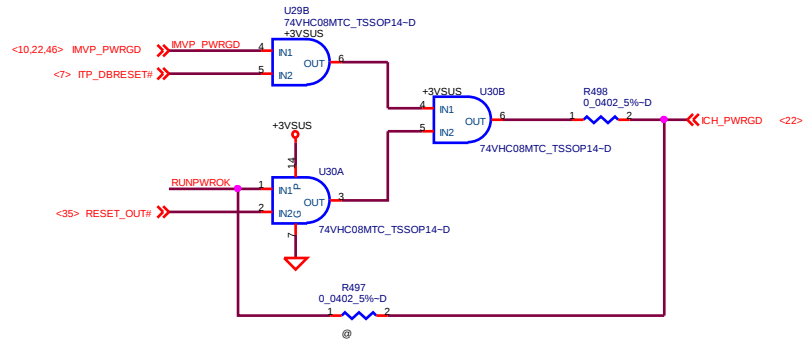
POWER CONTROL

LA-2171

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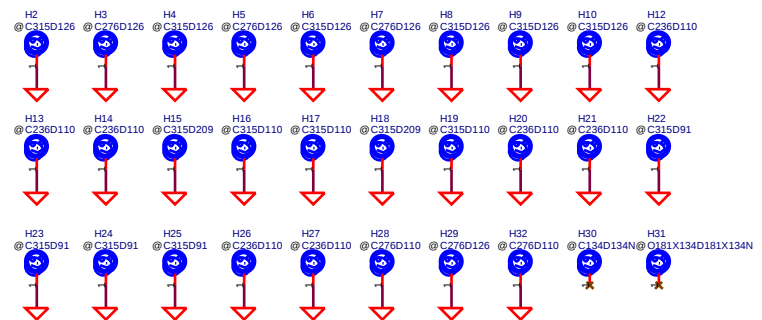
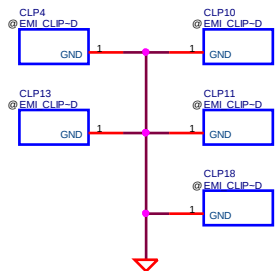
Rev 0.2



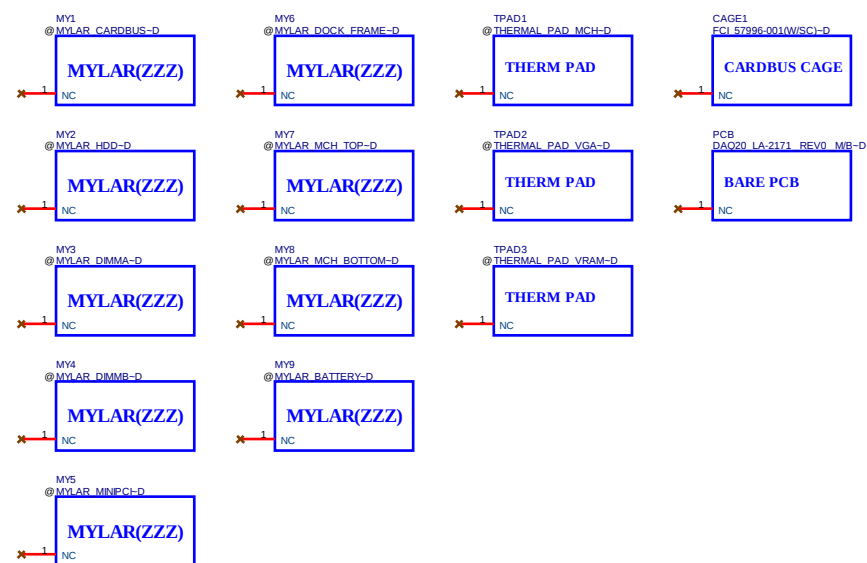
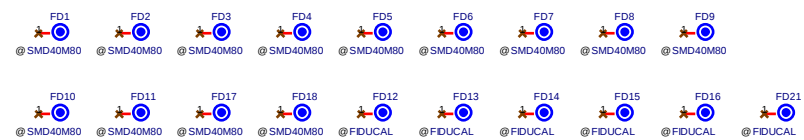
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Title		Power Good	
Size	Document Number	Rev	
	LA-2171	0.2	
Date	12/2004	Sheet	39 of 50



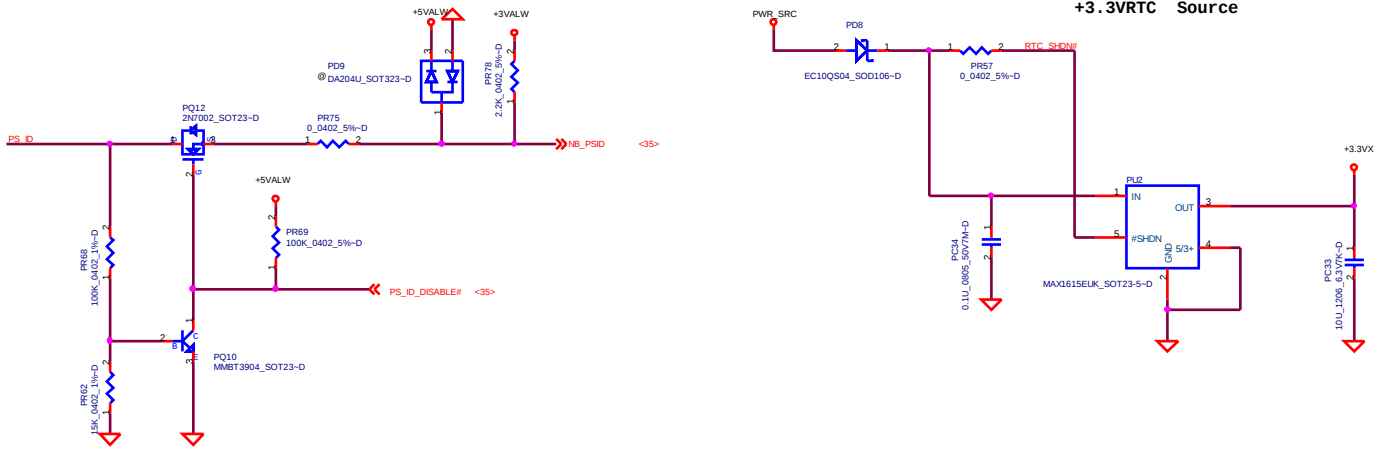
Fiducial Mark



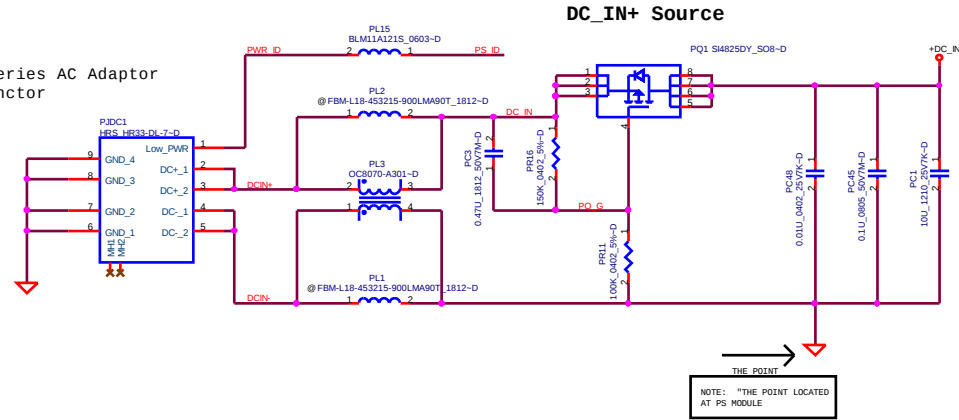
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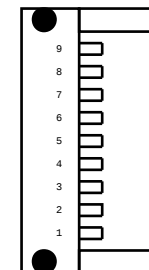
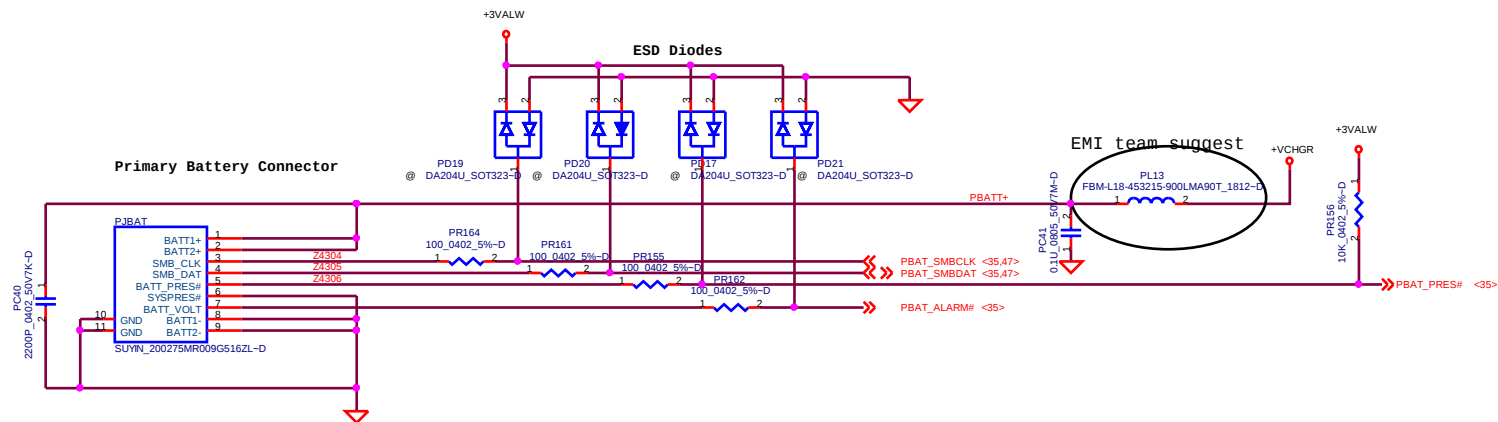


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Title			
PAD and Standoff			
Size	Document Number	Rev	
LA-2171	LA-2171	0.2	
Date	12/2004	Sheet	40 of 50



Z-series AC Adaptor
Connector

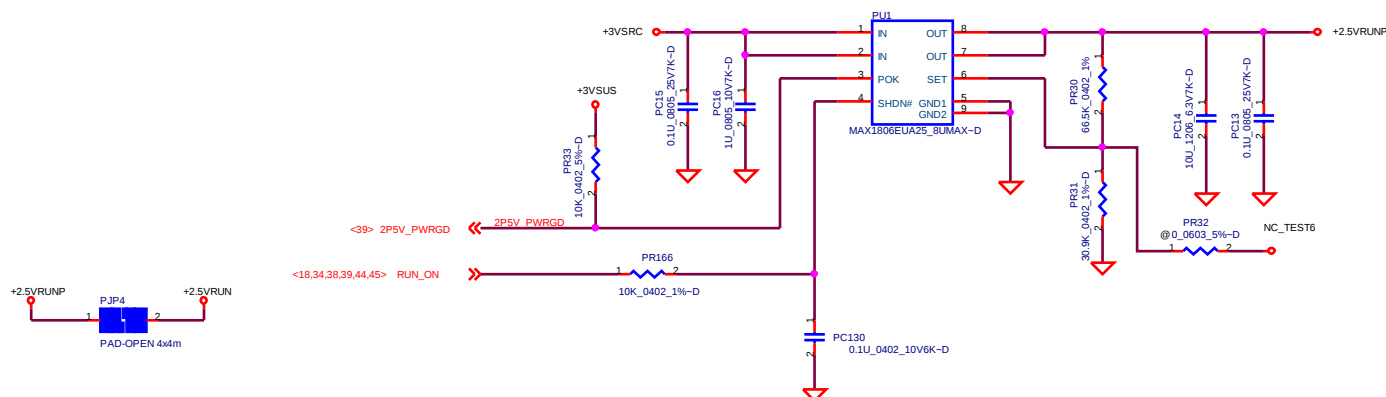




SUYIN_20175A-09G1
TOP view

+2.5V RUN

$$R1 = R2 * (V_o / 0.8 - 1), R2: 25K-100K.$$



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Battery Conn./+2.5V

Size Document Number
LA-2171

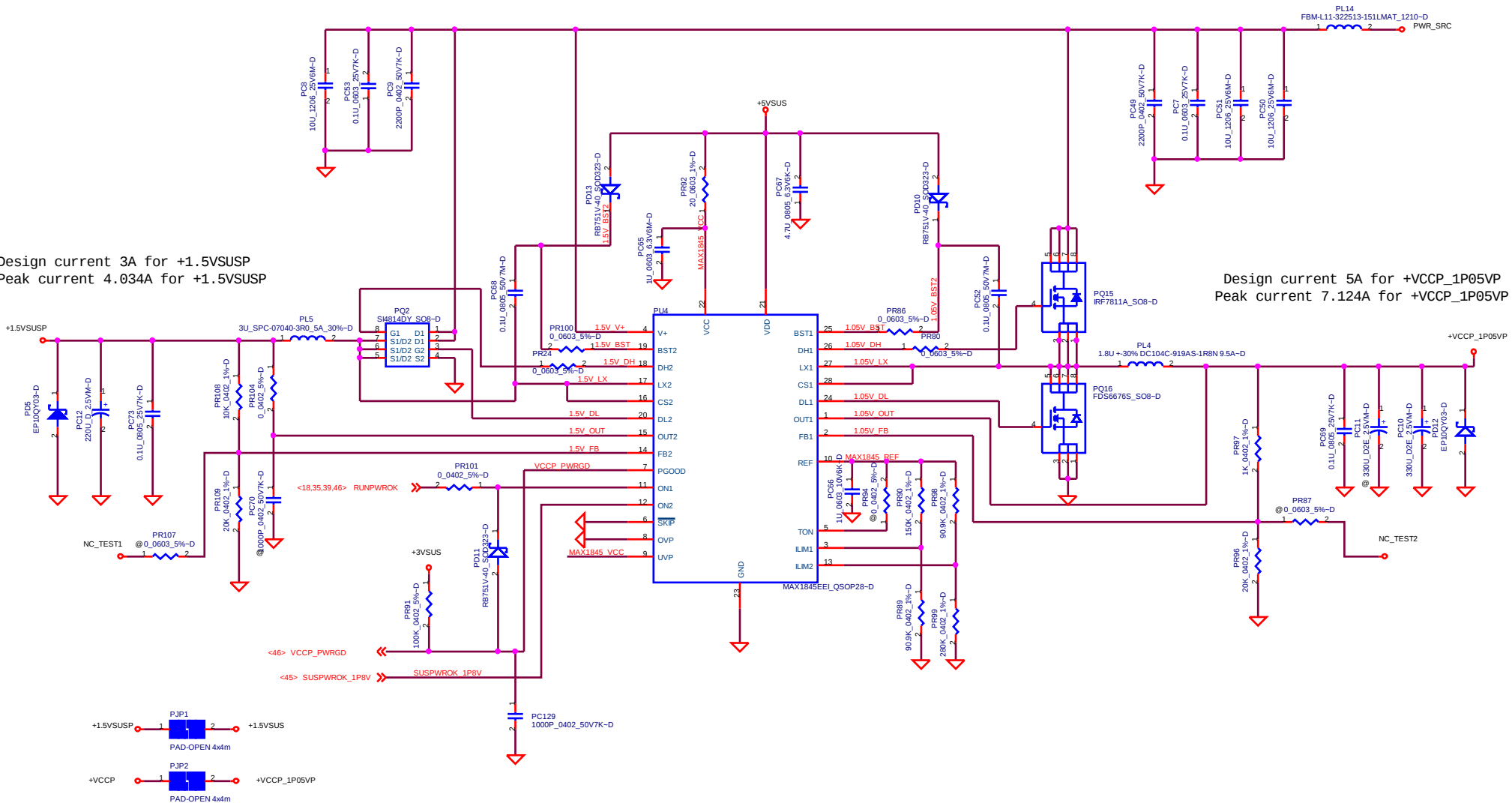
Date 12/2004 Sheet 42 of 50 Rev 0.2

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+1.5VSUSP / +VCCP_1P05VP

Design current 3A for +1.5VSUSP
Peak current 4.034A for +1.5VSUSP

Design current 5A for +VCCP_1P05VP
Peak current 7.124A for +VCCP_1P05VP



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+1.5VSUSP /+VCCP_1P05VP



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File	LA-2171	Rev	0.2
Size	Document Number	Date	12/2004
Sheet	43	of	50

DC/DC +3V/ +5V/ +15V

Design current 3.4A for +3.3VSRCP
Peak current 4.758A for +3VSRCP

Design current 4A for +5VSUSP
Peak current 5.7A for +5VSUSP

Place these CAPS
close to FETs

Place these CAPS
close to FETs

Adding SKIP control

Note: check the power consumption of +15V plane

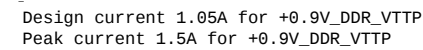
- +15VP (150mA, Via NO.= 2)
- +5VSUSP (6A, 240mils, Via NO.= 12)
- +3VSRCP (4A, 160mils, Via NO.= 8)

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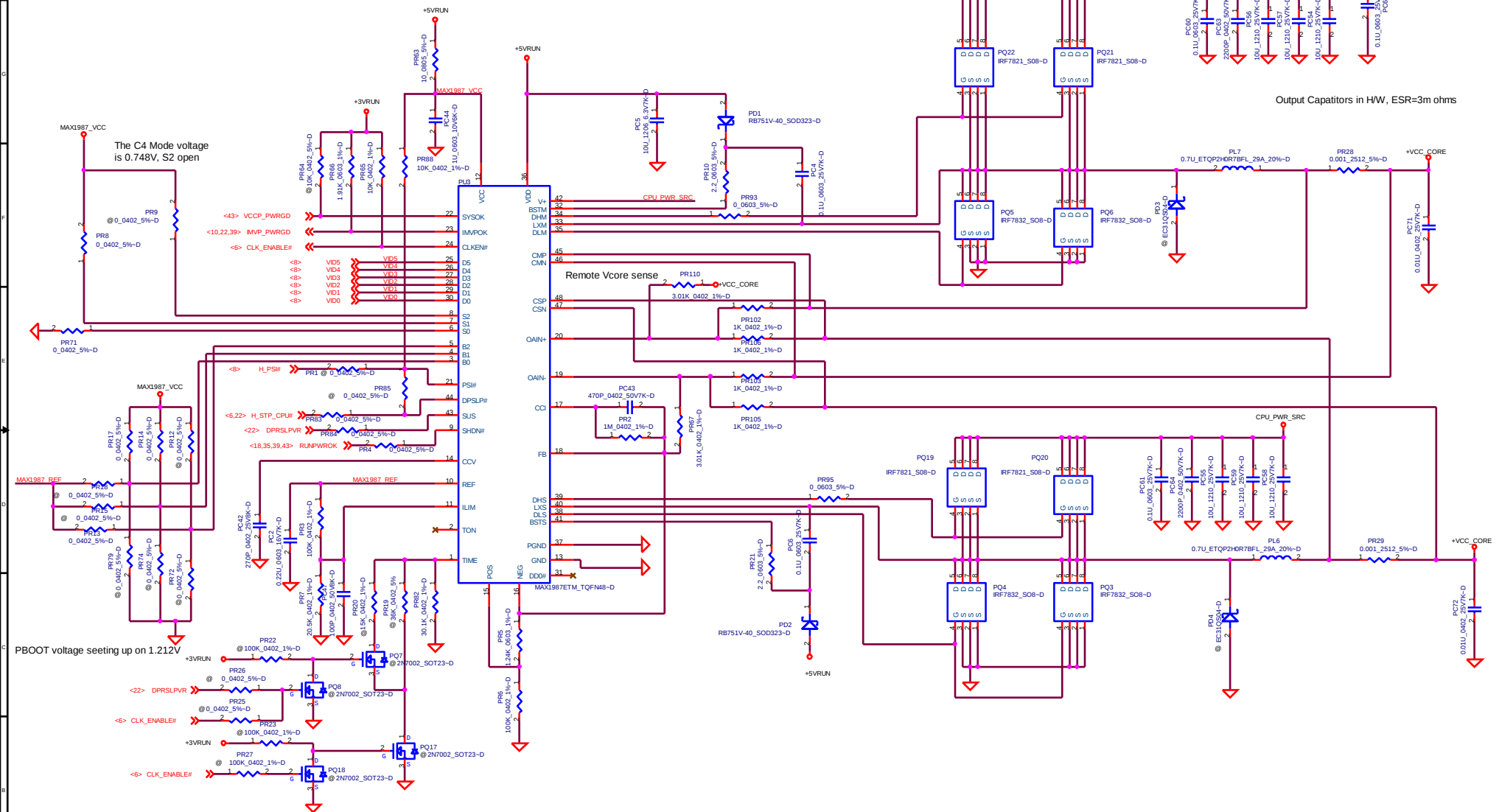
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+3.3V/+5V/+15V			
Doc	Document Number	LA-2171	
Date	12/2004	Sheet	44 of 50

DDR2 Termination




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 Title **+1.8VSUSP/ +0.9V_DDR_VT**
 Size Document Number Board Number LA2111 Rev D.1
 Date 12/2004 Sheet 45 of 50

V I D								Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V		
0	1	1	1	1	0	1.484		
0	1	1	0	0	1	1.308		
1	0	1	1	1	1	0.956		
1	1	1	1	0	0	0.748		



Change PR62 30.1k. Delete PR22/PQ8/PQ17/PQ7/PQ18/PR20/PR26/PR23 and PR19 for BANIAS and DOTHAN
 PR22/PQ8/PQ17/PQ7/PQ18/PR20/PR26/PR23 and PR19 are only for YONAH CPU.
 TRANSITION TIMING:
 (a): START-UP and SHUTDOWN (SUS=LOW, RUNPWROK=LOW): 2mV/us
 (b): ENTER SUSPEND (SUS=HIGH, RUNPWROK=HIGH): 8.6mV/us
 (c): EXIT SUSPEND (SUS=LOW, RUNPWROK=HIGH): 24.7mV/us

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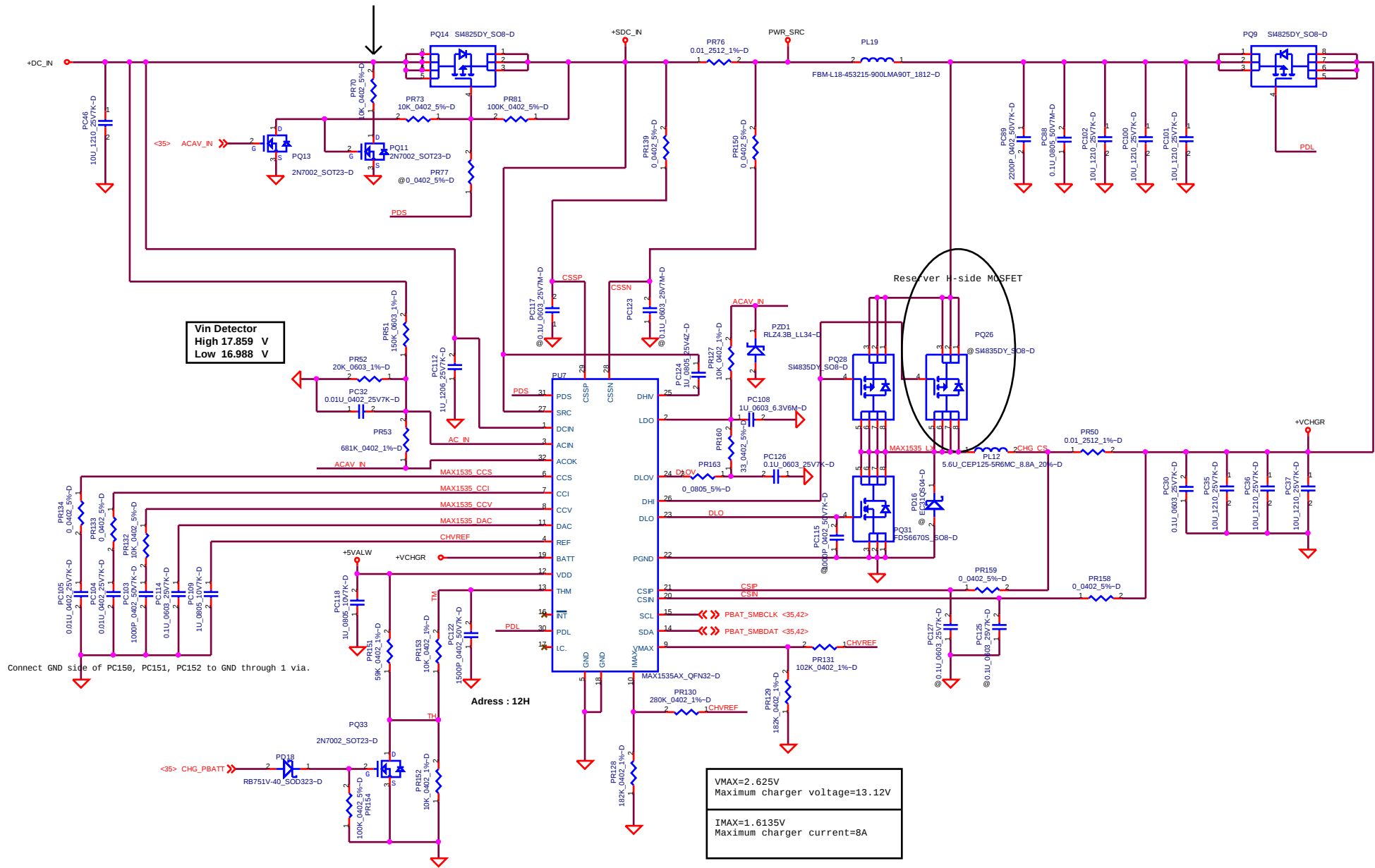
+VCORE

Document Number

LA-2171

Rev 0.2

+DC_IN discharge path



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Charger

Document Number
LA-2171

Rev
0.2

Date 12/2004

Sheet 47 of 50

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	31&32	Cardbus	10/15/03	Dell	Change cardbus controller to TI PCI4515.	Change U162	M00
2	18	VGA/B & DVI CONN.	10/16/03	Dell	Add DVI connector.	Add JDVI	M00
3	25	SATA Bridge	10/16/03	Dell	Add SATA to PATA circuit.	Add page 25	M00
4	28	Subwoofer	10/16/03	Dell	Add subwoofer circuit.	Add page 28	M00
5	40	LED/B	10/16/03	Dell	Removed IR circuit.	Delete U52	M00
6	27	Amplifier & Phone JACK	10/17/03	Dell	Removed internal MIC circuit.		X00
7	31&32	LOM	10/17/03	Dell	Change LAN controller (U164) from 5751M to 4401. Add pop option for the 5705 like Kapalua/Lindbergh board.		X00
8	33	Cardbus	10/17/03	Dell	Depop 1394 choke, L142 and pop bypass resistors, R1025, R1026, R1027, R1028		X00
9	1	Cover page	10/17/03	Dell	Change schematic revision from M00 to X00.		X00
10	40	PAD & ME & spare parts	01/07/04	Compal	For EMI requirement.	Pop CLP4,5,10,11,13 and depop CLP18	X01
11	22	ICH6(3/4)	01/08/04	Dell	Connected PCIE channel 1 to TV-Tuner connector.	Delete T4,T5,T29,T30 and add C661,C662	X01
12	37	LED/B & TV TUNER	01/08/04	Dell	Connected TV tuner signals.	Add C663,C664	X01
13	40	PAD & ME & spare parts	01/08/04	Compal	Added ME standoff.	Pop H12,H13,H14,H17,H20,H21,H26,H27	X01
14	32	CardBus(2/2)	01/28/04		Fixed SD card issue.	The pin11 of JSD need to be connected to GND and pin 12 need to be connected to U17 pin b3.	X01
15	10	Alviso(1/5)	01/28/04	Dell			
16	6	Clock Generator	01/28/04	Dell			
17	7&10	Dothan(1/2) &Alviso(1/5)	01/28/04	Dell			
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Changed-List History



Size	Document Number	Rev
	LA-2171	0.2

Date: 12/2004 Sheet: 48 of 50

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Version Change List (P. I. R. List)

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File	Changed-List History
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Size	Document Number	Rev
	LA-2171	0.2
Date:	12, 2004	Sheet 49 of 50

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	49	Charger selector	2003/10/14	Compal	Modify charger selector circuit.	Need to discuss.	0.0
2	42	PSID & +3VX	2003/10/15	Compal	Modify PSID circuit same as Nimitas. And add current limit resistor on RTC charger.	Add ESD solution on PSID, and limit RTC charge current.	0.0
3	44	+15VP	2003/11/4	Compal	+15VP current rating is not enough for subwoofer	Use MB3800 Boost IC to generate +15VP from +5VSUSP	X00
4	47	Charger	2003/11/5	Compal	That has leakage current from battery goes through PQ22 and PQ44 to DC_IN.	Move Adaptor current sense PR144 after PQ24 and before PWR_SRC. That is same as Nimitaz.	X00
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Size	Document Number	Rev
	LA-2171	0.2