Siberia / Converse Block Diagram

Project code:91.4Q601.001
PCB P/N :48.4Q601.0SA
REVISION :06226-SA

Clock Generator CY28547LFXC 4

Intel Mobile CPU Merom 4M FSB:667/ 800 Mhz 5,6

HOST BUS | FSB 667/800MHz

200-PIN DDR2 SODIMM

UNBUFFERED DDR2 SODIMM Socket 13 — DDRII 533/667MHz

UNBUFFERED DDR2 SODIMM Socket 14 — DDRII 533/667MHz

Crestline-PM 7,8,9,10,11,12
- AGTL+ CPU I/F
- DDR Memory I/F
- EXTERNAL GRAHPICS

PCI-e x16 → Graphic CONN. 15
- DVI-Out → DVI Port 16
- RGB CRT → CRT Port 17
- S-Video → TV-Out 17

Thermal Sensor EMC4001 22 — SMBus

DMI x4 | C-LINK0

PCI BUS | PCI Express (5)

Intel ICH8-M Enhanced 18,19,20,21
- USB 2.0/1.1 ports (10)
- PCI Express ports (6)
- ETHERNET (10/100/1000Mb)
- High Definition Audio
- ATA 66/ 100
- SATA (3)
- LPC I/F
- SPI
- ACPI 1.1
- PCI/PCI BRIDGE

SATA HDD 23 — SATA (2)

SATA HDD 23 — SATA (2)

ODD Bay 23 — PATA IDE

Ricoh R5C833 8 in 1 card reader 1394 24
- 1394 → 1394 CONN 24
- 8 in1 → 8 in1 CONN 25

Power Switch 30 → Express Card Slot 54mm 31

Buletooth 2.1 29

USB2.0 (10)

USB2.0 (5) → USB*6 33

Mini-Card Buletooth 2.1/UWB 32

Mini-Card 802.11a/g/n 31

Mini-Card WWAN 32 → SIM CONN 32

INT.Subwoofer 5W 30 — Subwoofer AMP. MAX9713 30

LINE OUT — Headphone AMP. MAX4411 29

MIC IN — Azalia CODEC STAC 9230 28 — AZALIA

Array MIC 28

USB Hub (4) USB2504 40

USB2.0 (4)

BCM5756ME Giga LAN 26 → RJ45 CONN 27

TPM 1.2 26

LPC

LINE OUT — Speaker AMP. Headphone AMP. MAX9789A 29

INT.SPKR 2W x 2 29

BIOS SPI FLASH 16Mb 40 — SPI

SPI

EC SMSC MEC5025 37

SIO Expander SMSC ECE5032 38

Smart Card OZ77CR6LN 34 → Smart Card CONN 34

Camera 39

Gaming LCD/ Biometric 39

PCI Q-Switch 35

RJ11 CONN 30 — MDC Modem 1.5 30

KBC SMSC ECE1077 39

CIR 39

Touch Pad 39

Int. KB Numpad

USB Mux 36

SPDIF

PS/2

SMBus

LPC D

SPDIF MODEM PS/2 SMBus LPC BUS USB 2.0 RJ45 PCI BUS S-video CRT DVI

D- Dock 36

System DC/DC TPS51120 50

INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW +5V_SUS +3.3V_SUS +3.3V_RTC_LDO

System DC/DC SN0508073 48

+PWR_SRC	+1.05V_VCCP +1.5V_RUN

DDR2 DC/DC SN0508073 49

+PWR_SRC	+1.8V_SUS +1.25V_RUN

LDO TPS51100 51

+1.8V_SUS	+0.9V_DDR_VTT

LDO MAX668 51

+PWR_SRC	+12V_S

Battery Charger ISL88731 45

INPUTS	OUTPUTS
+PWR_SRC	+VCHGR

CPU DC/DC ISL6260C 46,47

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

PCB LAYER

L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Signal
L7:GND
L8:BOT

SA5032

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Title: BLOCK DIAGRAM

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CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 10

Bit5 S1	Bit4 S0	Spread Spectrum S[1:0]
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

BYTE 15
IO_VOUT[2,1,0]

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order) ★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reversed	Normal Operation ★	Lane Reversed
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation ★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	BT/UWB/Robson
LANE4	Express Card
LANE5	No use
LANE6	Giba Bit LOM

PCI ROUTING

	IDSEL	INT	REQ	GNT
Dock	AD24	A	0	0
1394/ MediaCard	AD17	C D	1	1

USB TABLE

ICH

USB0	Ext Side (Left)
USB1	Ext Side (Right)
USB2	Ext I/O BD Side (Top)
USB3	Ext I/O BD Side (Bottom)
USB4	Ext Back (Bottom)
USB5	Dock/Ext Back (Top)
USB6	Express Card
USB7	BT
USB8	3rd mini card
USB9	USB Hub

USB Hub

USB1	SmartCard
USB2	Gaming LCD/Biometric
USB3	Camera
USB4	WWAN

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved. Rising Edge of PWROK.	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD/tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR	LOW = Defaule High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST0#	PULL-UP 13K

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Title: *Table of Content*

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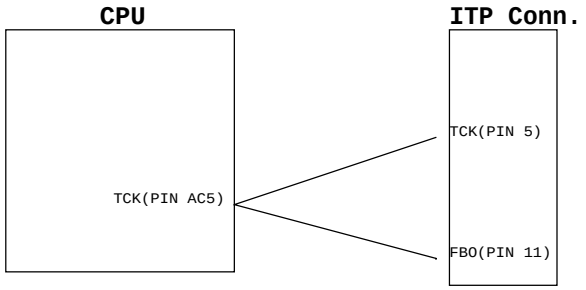

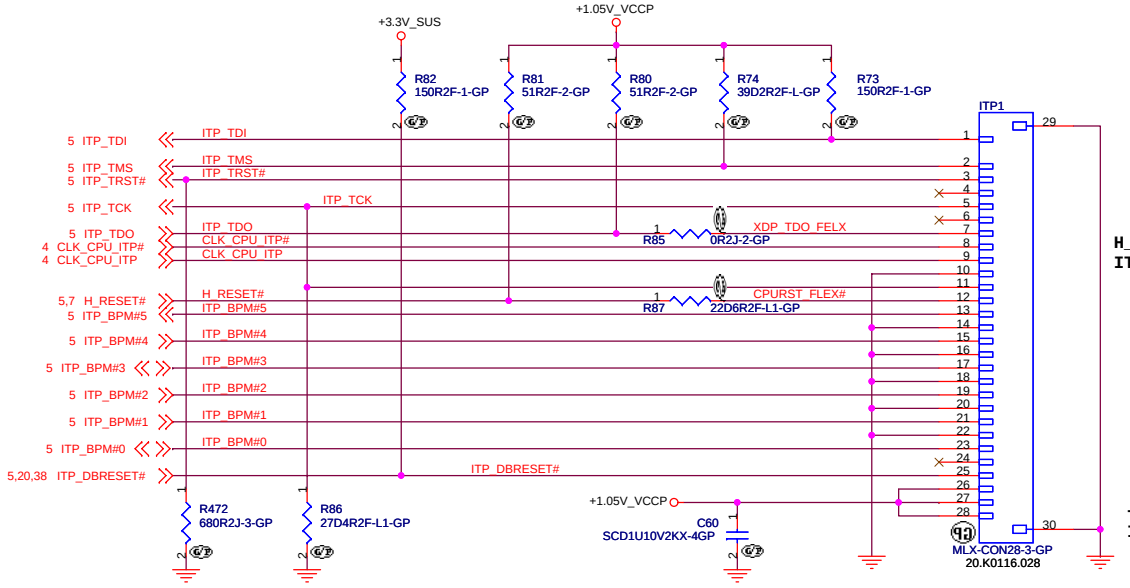

H_CPURST# use pull-up Resistor close ITP connector 500 mil (max)

+1.05VRUN use Decoupling Capacitor close ITP connector 100 mil (max)

ITP Debug Conn.

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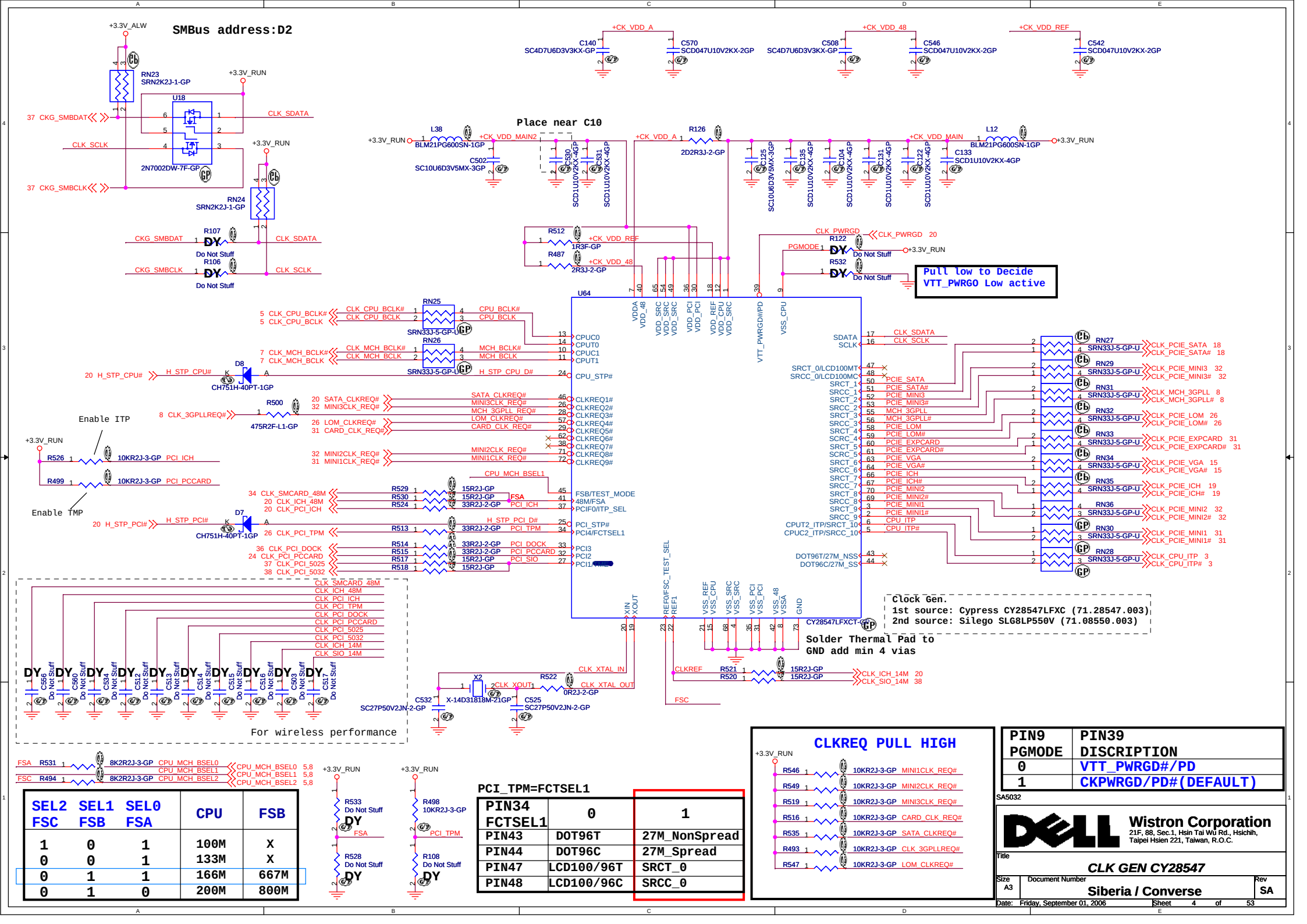
SMBus address:D2
Place near C10
Pull low to Decide
VTT_PWRGO Low active
Enable ITP
Enable TMP
Clock Gen.
1st source: Cypress CY28547LFXC (71.28547.003)
2nd source: Silego SLG8LP550V (71.08550.003)
Solder Thermal Pad to
GND add min 4 vias
For wireless performance
CLKREQ PULL HIGH
PCI_TPM=FCTSEL1
SEL2 FSC | SEL1 FSB | SEL0 FSA | CPU | FSB
1 | 0 | 1 | 100M | X
0 | 0 | 1 | 133M | X
0 | 1 | 1 | 166M | 667M
0 | 1 | 0 | 200M | 800M
PIN34 FCTSEL1 | 0 | 1
PIN43 | DOT96T | 27M_NonSpread
PIN44 | DOT96C | 27M_Spread
PIN47 | LCD100/96T | SRCT_0
PIN48 | LCD100/96C | SRCC_0
PIN9 PGMODE | PIN39 DISCRIPTION
0 | VTT_PWRGD#/PD
1 | CKPWRGD/PD#(DEFAULT)
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CLK GEN CY28547
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H_D#[63..0] H_D#[63..0] 7
H_A#[35..3] H_A#[35..3] 7
H_REQ#[4..0] H_REQ#[4..0] 7
H_RS#[2..0] H_RS#[2..0] 7

U16A 1 OF 4

ADDR GROUP 0 / CONTROL / ADDR GROUP 1 / XDP/ITP SIGNALS / THERMAL / ICH / HCLK / RESERVED

H_A#3 J4 A3#
H_A#4 L5 A4#
H_A#5 L4 A5#
H_A#6 K5 A6#
H_A#7 M3 A7#
H_A#8 N2 A8#
H_A#9 J1 A9#
H_A#10 N3 A10#
H_A#11 P5 A11#
H_A#12 P2 A12#
H_A#13 L2 A13#
H_A#14 P4 A14#
H_A#15 P1 A15#
H_A#16 R1 A16#
7 H_ADSTB#0 H_ADSTB#0 M1 ADSTB0#

H_REQ#0 K3 REQ0#
H_REQ#1 H2 REQ1#
H_REQ#2 K2 REQ2#
H_REQ#3 J3 REQ3#
H_REQ#4 L1 REQ4#

H_A#17 Y2 A17#
H_A#18 U5 A18#
H_A#19 R3 A19#
H_A#20 W6 A20#
H_A#21 U4 A21#
H_A#22 Y5 A22#
H_A#23 U1 A23#
H_A#24 R4 A24#
H_A#25 T5 A25#
H_A#26 T3 A26#
H_A#27 W2 A27#
H_A#28 W5 A28#
H_A#29 Y4 A29#
H_A#30 U2 A30#
H_A#31 V4 A31#
H_A#32 W3 A32#
H_A#33 AA4 A33#
H_A#34 AB2 A34#
H_A#35 AA3 A35#
7 H_ADSTB#1 H_ADSTB#1 V1 ADSTB1#

18 H_A20M# H_A20M# A6 A20M#
18 H_FERR# H_FERR# A5 FERR#
18 H_IGNNE# H_IGNNE# C4 IGNNE#

18 H_STPCLK# H_STPCLK# D5 STPCLK#
18 H_INTR# H_INTR# C6 LINT0
18 H_NMI# H_NMI# B4 LINT1
18 H_SMI# H_SMI# A3 SMI#

Do Not Stuff TP65 CPU_RSVD01 M4 RSVD#M4
Do Not Stuff TP66 CPU_RSVD02 N5 RSVD#N5
Do Not Stuff TP59 CPU_RSVD03 T2 RSVD#T2
Do Not Stuff TP62 CPU_RSVD04 V3 RSVD#V3
Do Not Stuff TP61 CPU_RSVD05 B2 RSVD#B2
Do Not Stuff TP63 CPU_RSVD06 C3 RSVD#C3
Do Not Stuff TP60 CPU_RSVD07 D2 RSVD#D2
Do Not Stuff TP68 CPU_RSVD08 D22 RSVD#D22
Do Not Stuff TP64 CPU_RSVD09 D3 RSVD#D3
Do Not Stuff TP67 CPU_RSVD10 F6 RSVD#F6

B1 KEY_NC

SKT-CPU478P-GP
62.10079.021

ADS# H1 H_ADS# H_ADS# 7 H_ADS# 7
BNR# E2 H_BNR# H_BNR# 7 H_BNR# 7
BPRI# G5 H_BPRI# H_BPRI# 7 H_BPRI# 7

+1.05V_VCCP
R131 56R2J-4-GP

DEFER# H5 H_DEFER# H_DEFER# 7 H_DEFER# 7
DRDY# F21 H_DRDY# H_DRDY# 7 H_DRDY# 7
DBSY# E1 H_DBSY# H_DBSY# 7 H_DBSY# 7

BR0# F1 H_BR0# H_BR0# 7 H_BR0# 7

IERR# D20 H_IERR#
INIT# B3 H_INIT# H_INIT# 18

LOCK# H4 H_LOCK# H_LOCK# 7

RESET# C1 H_RESET# H_RESET# 3,7
RS0# E3 H_RS#0
RS1# E4 H_RS#1
RS2# G3 H_RS#2
TRDY# G2 H_TRDY# H_TRDY# 7

HIT# G6 H_HIT# H_HIT# 7 H_HIT# 7
HITM# E4 H_HITM# H_HITM# 7 H_HITM# 7

BPM0# AD4 ITP_BPM#0 ITP_BPM#0 3
BPM1# AD3 ITP_BPM#1 ITP_BPM#1 3
BPM2# AD1 ITP_BPM#2 ITP_BPM#2 3
BPM3# AC4 ITP_BPM#3 ITP_BPM#3 3
PRDY# AC2 ITP_BPM#4 ITP_BPM#4 3
PREQ# AC1 ITP_BPM#5 ITP_BPM#5 3
TCK AC5 ITP_TCK ITP_TCK 3
TDI AA6 ITP_TDI ITP_TDI 3
TDO AB3 ITP_TDO ITP_TDO 3
TMS AB5 ITP_TMS ITP_TMS 3
TRST# AB6 ITP_TRST# ITP_TRST# 3
DBR# C20 ITP_DBRESET# ITP_DBRESET# 3,20,38

EC_CPU_PROCHOT# 37
PROCHOT# D21
THRMDA A24 H_THERMDA H_THERMDA 22
THRMDC B25 H_THERMDC H_THERMDC 22
C158 Do Not Stuff DY

THERMTRIP# C7 H_THERMTRIP# H_THERMTRIP# 22

BCLK0 A22 CLK_CPU_BCLK CLK_CPU_BCLK 4
BCLK1 A21 CLK_CPU_BCLK# CLK_CPU_BCLK# 4

+1.05V_VCCP
R150 1KR2F-3-GP
V_CPU_GTLREF
R149 2KR2F-3-GP

layout note:Zo =55 ohm , 0.5" MAX for GTLREF

U16B 2 OF 4

DATA GRP0 / DATA GRP2 / DATA GRP3 / DATA GRP1 / MISC

H_D#0 E22 D0# D32# Y22 H_D#32
H_D#1 F24 D1# D33# AB24 H_D#33
H_D#2 E26 D2# D34# V24 H_D#34
H_D#3 G22 D3# D35# V26 H_D#35
H_D#4 F23 D4# D36# Y23 H_D#36
H_D#5 G25 D5# D37# T22 H_D#37
H_D#6 E25 D6# D38# U25 H_D#38
H_D#7 E23 D7# D39# U23 H_D#39
H_D#8 K24 D8# D40# Y25 H_D#40
H_D#9 G24 D9# D41# W22 H_D#41
H_D#10 J24 D10# D42# Y23 H_D#42
H_D#11 J23 D11# D43# W24 H_D#43
H_D#12 H22 D12# D44# W25 H_D#44
H_D#13 F26 D13# D45# AA23 H_D#45
H_D#14 K22 D14# D46# AA24 H_D#46
H_D#15 H23 D15# D47# AB25 H_D#47

7 H_DSTBN#0 H_DSTBN#0 J26 DSTBN0# DSTBN2# Y26 H_DSTBN#2 H_DSTBN#2 7
7 H_DSTBP#0 H_DSTBP#0 H26 DSTBP0# DSTBP2# AA26 H_DSTBP#2 H_DSTBP#2 7
7 H_DINV#0 H_DINV#0 H25 DINV0# DINV2# U22 H_DINV#2 H_DINV#2 7

H_D#16 N22 D16# D48# AE24 H_D#48
H_D#17 K25 D17# D49# AD24 H_D#49
H_D#18 P26 D18# D50# AA21 H_D#50
H_D#19 R23 D19# D51# AB22 H_D#51
H_D#20 L23 D20# D52# AB21 H_D#52
H_D#21 M24 D21# D53# AC26 H_D#53
H_D#22 L22 D22# D54# AD20 H_D#54
H_D#23 M23 D23# D55# AE22 H_D#55
H_D#24 P25 D24# D56# AF23 H_D#56
H_D#25 P23 D25# D57# AC25 H_D#57
H_D#26 P22 D26# D58# AE21 H_D#58
H_D#27 T24 D27# D59# AD21 H_D#59
H_D#28 R24 D28# D60# AC22 H_D#60
H_D#29 L25 D29# D61# AD23 H_D#61
H_D#30 T25 D30# D62# AE22 H_D#62
H_D#31 N25 D31# D63# AC23 H_D#63

7 H_DSTBN#1 H_DSTBN#1 L26 DSTBN1# DSTBN3# AE25 H_DSTBN#3 H_DSTBN#3 7
7 H_DSTBP#1 H_DSTBP#1 M26 DSTBP1# DSTBP3# AF24 H_DSTBP#3 H_DSTBP#3 7
7 H_DINV#1 H_DINV#1 N24 DINV1# DINV3# AC20 H_DINV#3 H_DINV#3 7

GTLREF AD26 COMP0 R26 COMP0 R148 1 27D4R2F-L1-GP
TEST1 C23 COMP1 U26 COMP1 R147 1 54D9R2F-L1-GP
TEST2 D25 COMP2 AA1 COMP2 R484 1 27D4R2F-L1-GP
TEST3 C24 COMP3 Y1 COMP3 R483 1 54D9R2F-L1-GP
TEST4 AF26
TEST5 AF1
TEST6 A26

DPRSTP# E5 H_DPRSTP# H_DPRSTP# 8,18,46
DPSLP# B5 H_DPSLP# H_DPSLP# 18
DPWR# D24 H_DPWR# H_DPWR# 7
PWRGOOD D6 H_PWRGOOD H_PWRGOOD 18
SLP# D7 H_CPUSLP# H_CPUSLP# 7
PSI# AE6 H_PSI# H_PSI# 46

BSEL0 B22
BSEL1 B23
BSEL2 C21

SKT-CPU478P-GP

R136 1 Do Not Stuff DY
R143 1 Do Not Stuff DY
C177 Do Not Stuff DY
R139 1 Do Not Stuff DY

4,8 CPU_MCH_BSEL0 CPU_MCH_BSEL0
4,8 CPU_MCH_BSEL1 CPU_MCH_BSEL1
4,8 CPU_MCH_BSEL2 CPU_MCH_BSEL2

Note:
H_DPRSTP# need to daisy chain from ICH8 to IMVP6 to CPU

Use old Symbol replace New P/N
original value:SKT-CPU478P-GP

PLACE C117 close to the TEST4 PIN, make sure TEST4 PIN routing is reference to GND and away from other noisy signals

Do Not Stuff TP69 TEST3
Do Not Stuff TP58 TEST5

For the purpose of testability, route thes signals through a ground referenced Zo=55ohm trace thatends in a via that is near a GND via and is accessible through an oscilloscope connection.

Make COMP[3..0] traces length shorter than 0.5". Trace should be at least 25 mils away from any other toggling signal.
COMP 0,2 connect Zo=27.4ohm.
COMP 1,3 connect Zo=55ohm.

+1.05V_VCCP
R100 1 DY Do Not Stuff H_PWRGOOD
R102 1 56R2J-4-GP H_THERMTRIP#
R132 1 56R2J-4-GP EC_CPU_PROCHOT#
R97 1 56R2J-4-GP H_FERR#
R485 1 DY Do Not Stuff ITP_BPM#4

SA5032

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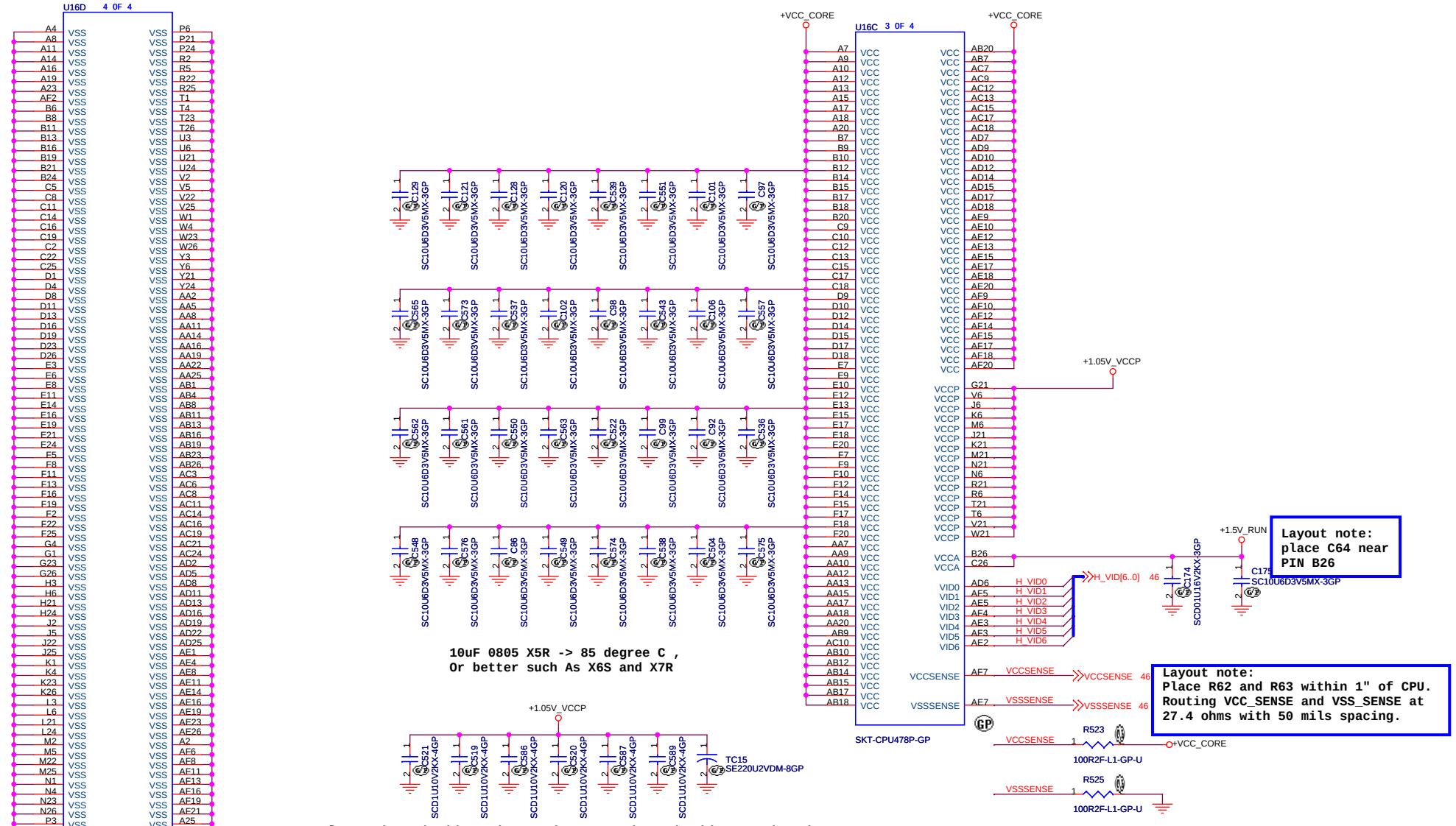

SA5032

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU-POWER (2/2)***

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H_D#[63..0] H_D#[63..0] 5

H_A#[35..3] H_A#[35..3] 5

H_REQ#[4..0] H_REQ#[4..0] 5

H_RS#[2..0] H_RS#[2..0] 5

U34A 1 OF 10

HOST

H_D#0 E2 H_D#1 G2 H_D#2 G7 H_D#3 M6 H_D#4 H7 H_D#5 H3 H_D#6 G4 H_D#7 F3 H_D#8 N8 H_D#9 H2 H_D#10 M10 H_D#11 N12 H_D#12 N9 H_D#13 H5 H_D#14 P13 H_D#15 K9 H_D#16 M2 H_D#17 W10 H_D#18 Y8 H_D#19 V4 H_D#20 M3 H_D#21 J1 H_D#22 N5 H_D#23 N3 H_D#24 W6 H_D#25 W9 H_D#26 N2 H_D#27 Y7 H_D#28 Y9 H_D#29 P4 H_D#30 W3 H_D#31 N1 H_D#32 AD12 H_D#33 AE3 H_D#34 AD9 H_D#35 AC9 H_D#36 AC7 H_D#37 AC14 H_D#38 AD11 H_D#39 AC11 H_D#40 AB2 H_D#41 AD7 H_D#42 AB1 H_D#43 Y3 H_D#44 AC6 H_D#45 AE2 H_D#46 AC5 H_D#47 AG3 H_D#48 AJ9 H_D#49 AH8 H_D#50 AJ14 H_D#51 AE9 H_D#52 AE11 H_D#53 AH12 H_D#54 AJ5 H_D#55 AH5 H_D#56 AJ6 H_D#57 AE7 H_D#58 AJ7 H_D#59 AJ2 H_D#60 AE5 H_D#61 AJ3 H_D#62 AH2 H_D#63 AH13

H_A#3 J13 H_A#4 B11 H_A#5 C11 H_A#6 M11 H_A#7 C15 H_A#8 F16 H_A#9 L13 H_A#10 G17 H_A#11 C14 H_A#12 K16 H_A#13 B13 H_A#14 L16 H_A#15 J17 H_A#16 B14 H_A#17 K19 H_A#18 P15 H_A#19 R17 H_A#20 B16 H_A#21 H20 H_A#22 L19 H_A#23 D17 H_A#24 M17 H_A#25 N16 H_A#26 J19 H_A#27 B18 H_A#28 E19 H_A#29 B17 H_A#30 B15 H_A#31 E17 H_A#32 C18 H_A#33 A19 H_A#34 B19 H_A#35 N19

H_ADS# G12 H_ADSTB#0 H17 H_ADSTB#1 G20 H_BNR# C8 H_BPRI# E8 H_BR0# E12 H_DEFER# D6 H_DBSY# C10 HPLL_CLK AM5 HPLL_CLK# AM7 H_DPWR# H8 H_DRDY# K7 H_HIT# E4 H_HITM# C6 H_LOCK# G10 H_TRDY# B7

H_ADS# 5 H_ADSTB#0 5 H_ADSTB#1 5 H_BNR# 5 H_BPRI# 5 H_BR0# 5 H_DEFER# 5 H_DBSY# 5 CLK_MCH_BCLK 4 CLK_MCH_BCLK# 4 H_DPWR# 5 H_DRDY# 5 H_HIT# 5 H_HITM# 5 H_LOCK# 5 H_TRDY# 5

H_DINV#0 K5 H_DINV#1 L2 H_DINV#2 AD13 H_DINV#3 AE13

H_DINV#0 5 H_DINV#1 5 H_DINV#2 5 H_DINV#3 5

H_DSTBN#0 M7 H_DSTBN#1 K3 H_DSTBN#2 AD2 H_DSTBN#3 AH11

H_DSTBN#0 5 H_DSTBN#1 5 H_DSTBN#2 5 H_DSTBN#3 5

H_DSTBP#0 L7 H_DSTBP#1 K2 H_DSTBP#2 AC2 H_DSTBP#3 AJ10

H_DSTBP#0 5 H_DSTBP#1 5 H_DSTBP#2 5 H_DSTBP#3 5

H_SWING B3 H_RCOMP C2

H_SCOMP W1 H_SCOMP# W2

H_RESET# B6 H_CPUSLP# E5

H_CPURST# H_CPUSLP#

H_REQ#0 M14 H_REQ#1 E13 H_REQ#2 A11 H_REQ#3 H13 H_REQ#4 B12

H_RS#0 E12 H_RS#1 D7 H_RS#2 D8

H_AVREF B9 H_DVREF A9

3,5 H_RESET#
5 H_CPUSLP#

H_REF

CRESTLINE-GP-U

H_REF Decoupling Crestline close Crestline 100 mil

+1.05V_VCCP

R171 1KR2F-3-GP

R170 2KR2F-3-GP

C191 SCD1U10V2KX-4GP

CRB v0.9 REQUEST

H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close Caliistoga 500 mil (MAX)

From Schematic Design Checklit v.1201

221 1% pull high 100

1% pull low

+1.05V_VCCP

R186 221R2F-2-GP

H_SWING

C197 SCD1U10V2KX-4GP

R183 100R2F-L1-GP-U

H_SCOMP and H_SCOMP# Resistors and Capacitors close Caliistoga 500 mil (MAX)

Zo=55ohms

+1.05V_VCCP

R207 54D9R2F-L1-GP H_SCOMP

+1.05V_VCCP

R209 54D9R2F-L1-GP H_SCOMP#

H_RCOMP routing Trace width and Spacing use 10 / 20 mil

R188 24D9R2F-L-GP H_RCOMP

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Title: GMCH-FSB LIBC (1/6)

Size: A3 | Document Number: Siberia / Converse | Rev: SA

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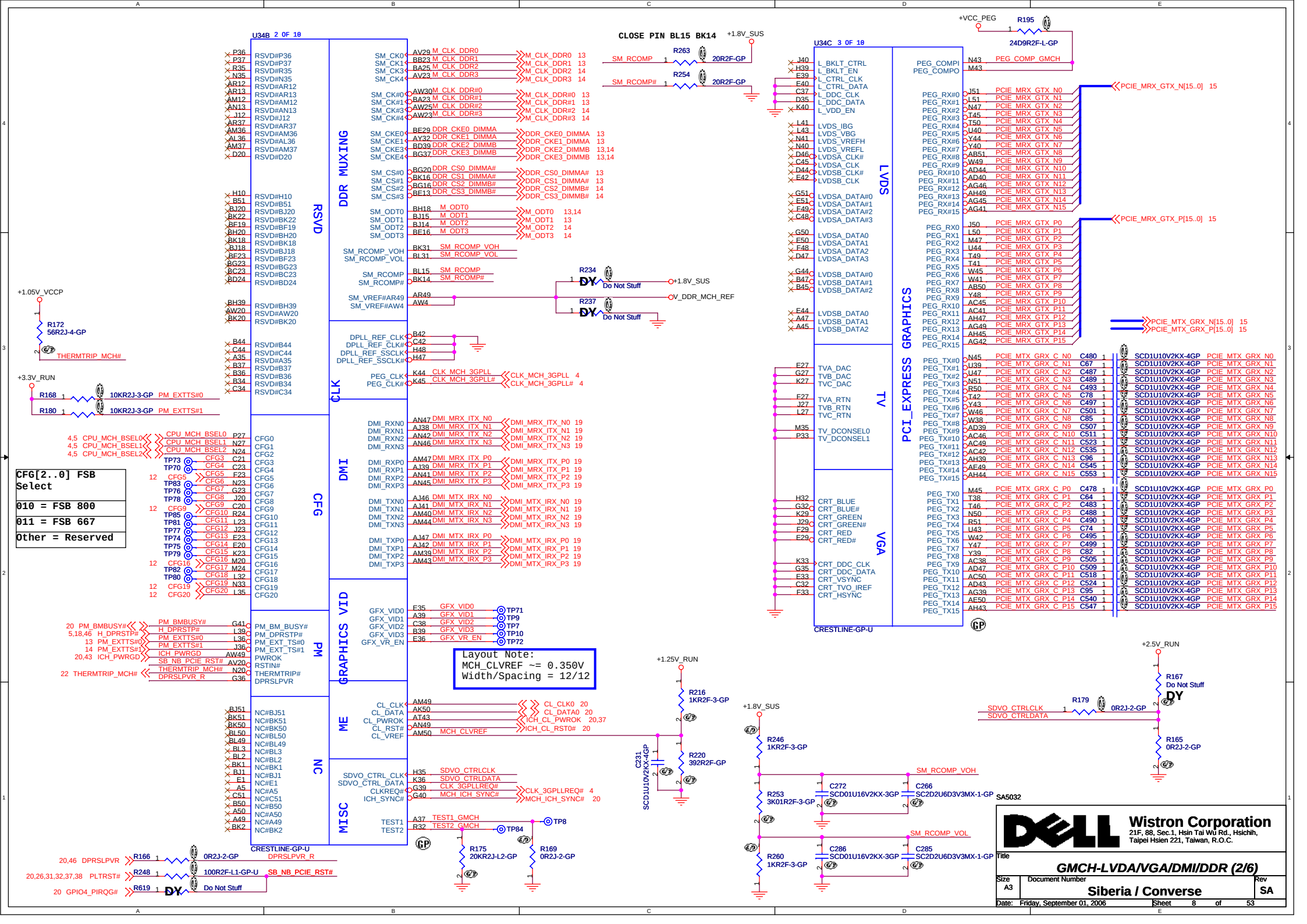
U34B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
CRESTLINE-GP-U
U34C 3 OF 10
LVDS
PCI_EXPRESS GRAPHICS
TV
VGA
CRESTLINE-GP-U
CLOSE PIN BL15 BK14
CFG[2..0] FSB Select
010 = FSB 800
011 = FSB 667
Other = Reserved
Layout Note:
MCH_CLVREF ~= 0.350V
Width/Spacing = 12/12
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
GMCH-LVDA/VGA/DMI/DDR (2/6)
SA5032
Siberia / Converse
Size A3
Rev SA
Date: Friday, September 01, 2006
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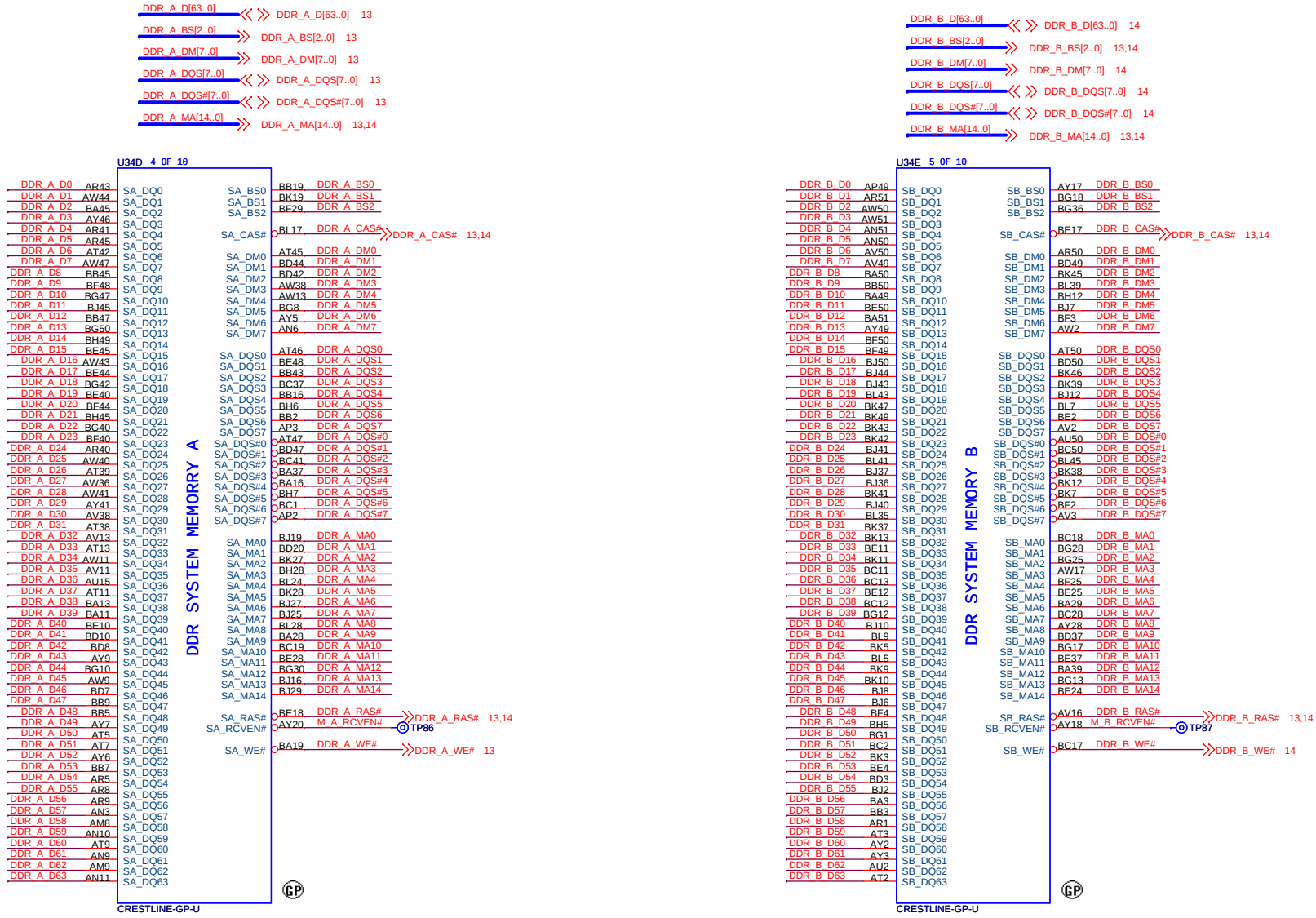

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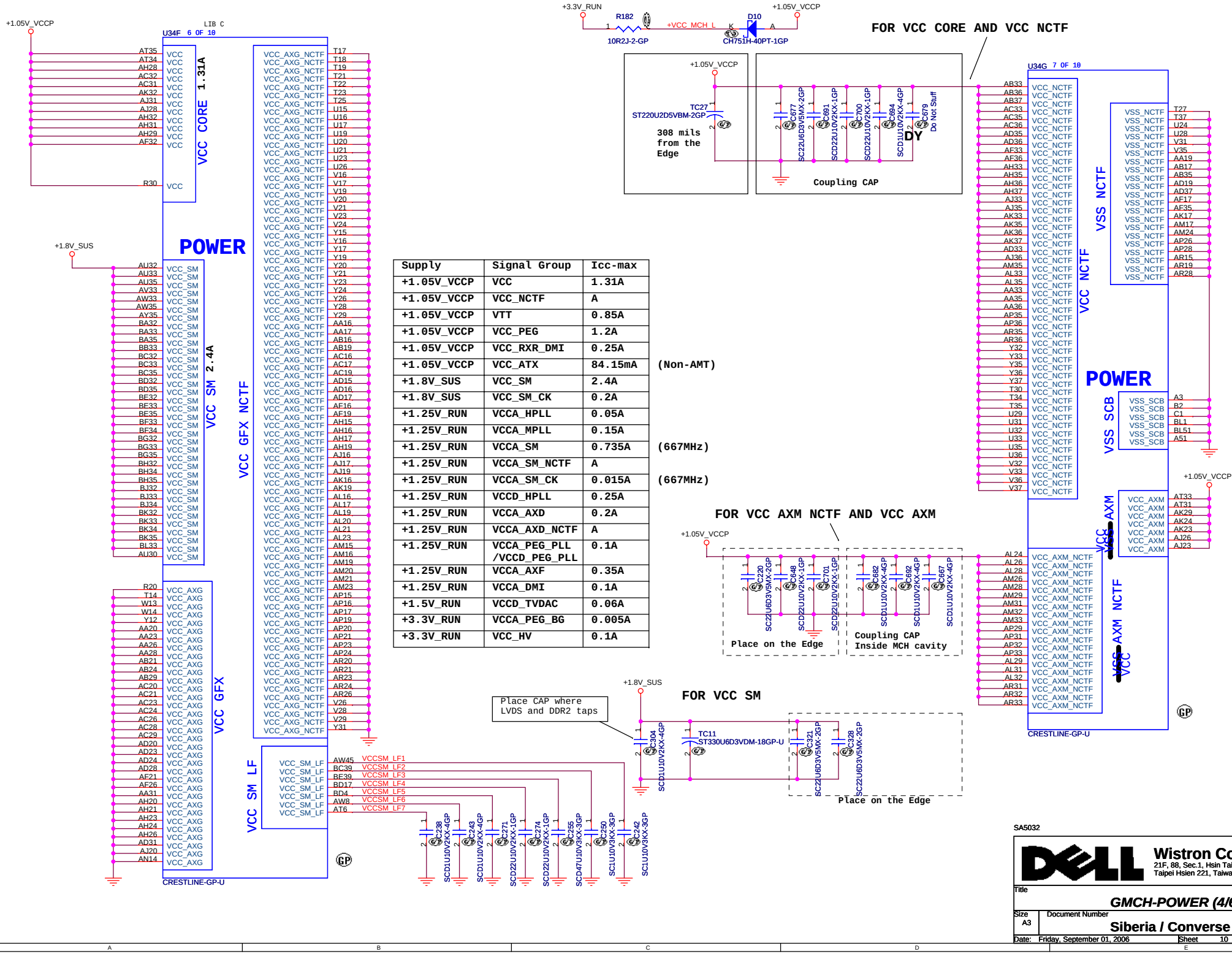
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GMCH-DDR (3/6)***

Size	Document Number	Rev
A3	Siberia / Converse	SA

Date: Friday, September 01, 2006 Sheet 9 of 53



Supply	Signal Group	Icc-max	
+1.05V_VCCP	VCC	1.31A	
+1.05V_VCCP	VCC_NCTF	A	
+1.05V_VCCP	VTT	0.85A	
+1.05V_VCCP	VCC_PEG	1.2A	
+1.05V_VCCP	VCC_RXR_DMI	0.25A	
+1.05V_VCCP	VCC_ATX	84.15mA	(Non-AMT)
+1.8V_SUS	VCC_SM	2.4A	
+1.8V_SUS	VCC_SM_CK	0.2A	
+1.25V_RUN	VCCA_HPLL	0.05A	
+1.25V_RUN	VCCA_MPLL	0.15A	
+1.25V_RUN	VCCA_SM	0.735A	(667MHz)
+1.25V_RUN	VCCA_SM_NCTF	A	
+1.25V_RUN	VCCA_SM_CK	0.015A	(667MHz)
+1.25V_RUN	VCCD_HPLL	0.25A	
+1.25V_RUN	VCCA_AXD	0.2A	
+1.25V_RUN	VCCA_AXD_NCTF	A	
+1.25V_RUN	VCCA_PEG_PLL /VCCD_PEG_PLL	0.1A	
+1.25V_RUN	VCCA_AXF	0.35A	
+1.25V_RUN	VCCA_DMI	0.1A	
+1.5V_RUN	VCCD_TVDAC	0.06A	
+3.3V_RUN	VCCA_PEG_BG	0.005A	
+3.3V_RUN	VCC_HV	0.1A	

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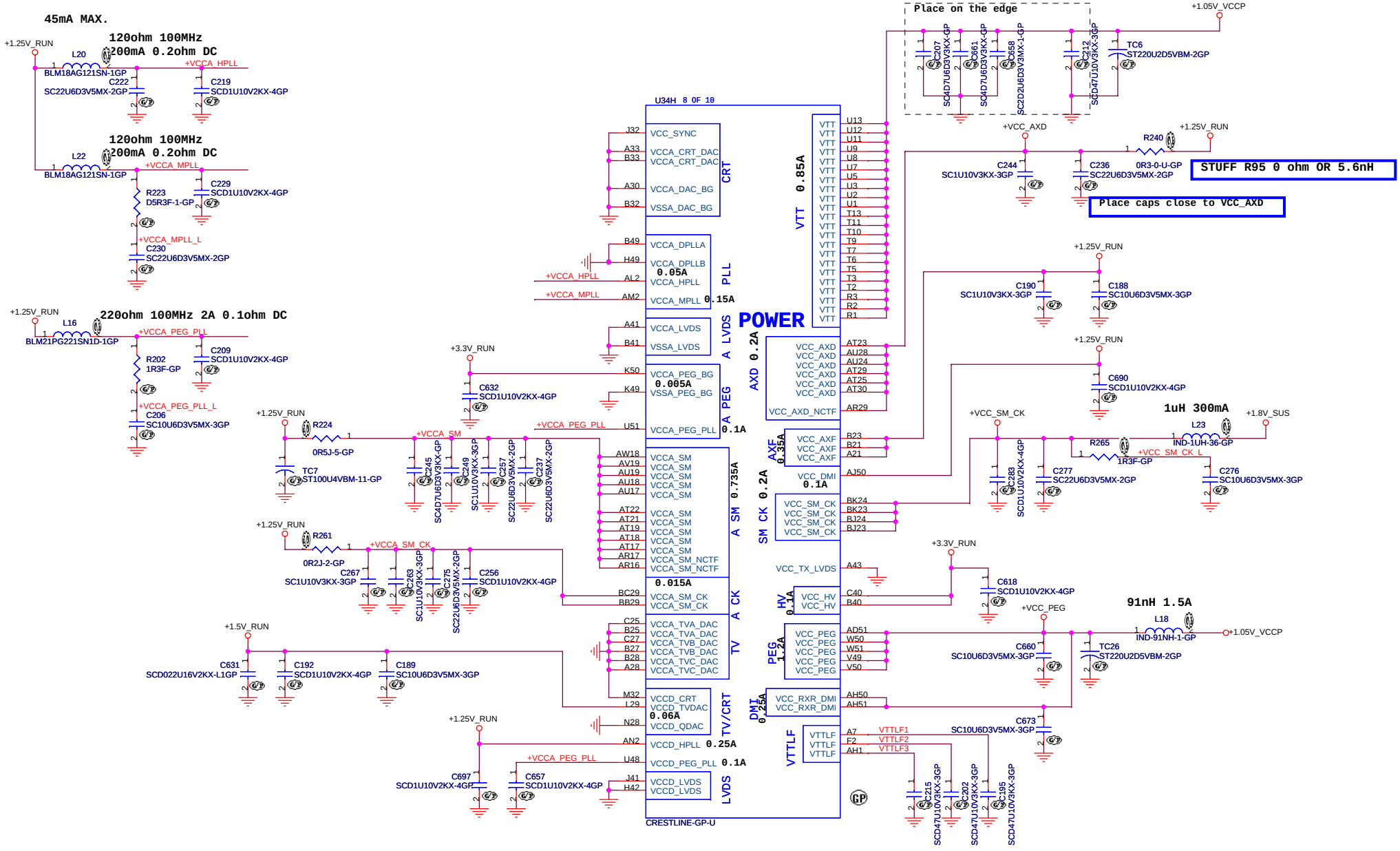
Title: *GMCH-POWER (4/6)*

Size: A3 | Document Number: Siberia / Converse | Rev: SA

Date: Friday, September 01, 2006 | Sheet 10 of 53



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Title: GMCH-POWER/FILTERR (5/6)

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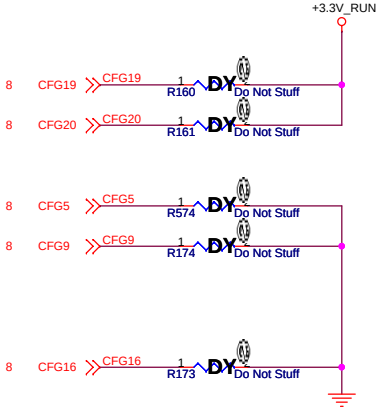
Layout Note:
Location of all MCH CFG strap resistors need to be close to trace to minimize stub



CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	★ DMI X 4
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	★ Normal Mode(Lanes number in order)
CFG 16 FSB Dynamic ODT	Disabled	★ Enabled
CFG 18 VCC select	★ 1.05V	1.5V
CFG 19 DMI Lane Reversed	★ Normal Operation	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	★ Only PCIE or SDVO is operation	PCIE and SDVO are operation simultaneous

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation ★

9 OF 10

U34I

VSS

CRESTLINE-GP-U

10 OF 10

U34J

VSS

CRESTLINE-GP-U

T29	MCH_GND1	R162 1 0 0R2J-2-GP
T31	MCH_GND2	R163 1 0 0R2J-2-GP
T33	MCH_GND3	R159 1 0 0R2J-2-GP
R28	MCH_GND4	R594 1 0 0R2J-2-GP

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Title: GMCH-GND (6/6)

Size: A3 | Document Number: Siberia / Converse | Rev: SA

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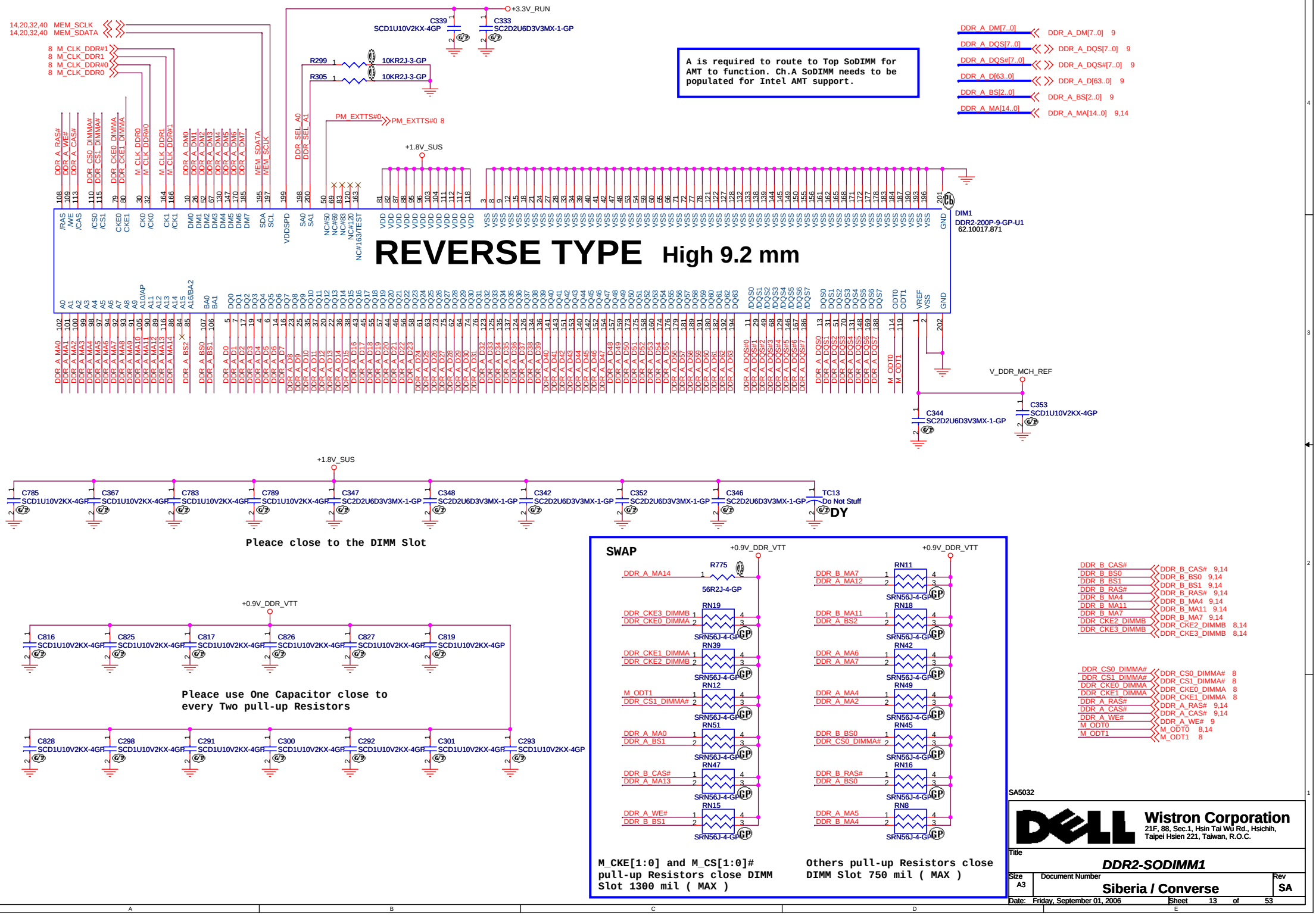
A is required to route to Top SoDIMM for AMT to function. Ch.A SoDIMM needs to be populated for Intel AMT support.
REVERSE TYPE High 9.2 mm
DIM1
DDR2-200P-9-GP-U1
62.10017.871
+3.3V_RUN
+1.8V_SUS
+0.9V_DDR_VTT
V_DDR_MCH_REF
Please close to the DIMM Slot
Please use One Capacitor close to every Two pull-up Resistors
SWAP
M_CKE[1:0] and M_CS[1:0]# pull-up Resistors close DIMM Slot 1300 mil (MAX)
Others pull-up Resistors close DIMM Slot 750 mil (MAX)
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SA5032
DDR2-SODIMM1
Siberia / Converse
SA
Date: Friday, September 01, 2006
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M_CLK_DDR3 and M_CLK_DDR#3
can map to Row/Rank 2

13,20,32,40 MEM_SCLK
13,20,32,40 MEM_SDATA
8 M_CLK_DDR#3
8 M_CLK_DDR3
8 M_CLK_DDR#2
8 M_CLK_DDR2

R277 10KR2J-3-GP
R281 10KR2J-3-GP
C781 SCD1U10V2KX-4GP
C791 SC2D2U6D3V3MX-1-GP
+3.3V_RUN
PM_EXTTS#1
PM_EXTTS#1 8
+1.8V_SUS

DDR_B_DM[7..0] DDR_B_DM[7..0] 9
DDR_B_DQS[7..0] DDR_B_DQS[7..0] 9
DDR_B_DQS#[7..0] DDR_B_DQS#[7..0] 9
DDR_B_D[63..0] DDR_B_D[63..0] 9
DDR_B_BS[2..0] DDR_B_BS[2..0] 9,13
DDR_B_MA[14..0] DDR_B_MA[14..0] 9,13

DIM2
DDR2-200P-8-GP-U1
62.10017.861

NORMAL TYPE High 4mm

C792 SC2D2U6D3V3MX-1-GP
C788 SCD1U10V2KX-4GP
V_DDR_MCH_REF

+1.8V_SUS
C782 SCD1U10V2KX-4GP
C370 SCD1U10V2KX-4GP
C786 SCD1U10V2KX-4GP
C784 SCD1U10V2KX-4GP
C350 SC2D2U6D3V3MX-1-GP
C351 SC2D2U6D3V3MX-1-GP
C374 SC2D2U6D3V3MX-1-GP
C349 SC2D2U6D3V3MX-1-GP
C364 SC2D2U6D3V3MX-1-GP
TC10 Do Not Stuff
DY

Please close to the DIMM Slot

+0.9V_DDR_VTT
C829 SCD1U10V2KX-4GP
C821 SCD1U10V2KX-4GP
C820 SCD1U10V2KX-4GP
C818 SCD1U10V2KX-4GP
C823 SCD1U10V2KX-4GP
C824 SCD1U10V2KX-4GP

Please use One Capacitor close to
every Two pull-up Resistors

C815 SCD1U10V2KX-4GP
C297 SCD1U10V2KX-4GP
C302 SCD1U10V2KX-4GP
C295 SCD1U10V2KX-4GP
C296 SCD1U10V2KX-4GP
C303 SCD1U10V2KX-4GP
C289 SCD1U10V2KX-4GP

SWAP

+0.9V_DDR_VTT
R272 56R2J-4-GP
RN48 SRN56J-4-GP
RN46 SRN56J-4-GP
RN50 SRN56J-4-GP
RN43 SRN56J-4-GP
RN41 SRN56J-4-GP
RN14 SRN56J-4-GP

+0.9V_DDR_VTT
RN17 SRN56J-4-GP
RN44 SRN56J-4-GP
RN7 SRN56J-4-GP
RN9 SRN56J-4-GP
RN10 SRN56J-4-GP
RN13 SRN56J-4-GP
RN40 SRN56J-4-GP

M_CKE[3:2] and M_CS[3:2]#
pull-up Resistors close DIMM
Slot 1300 mil (MAX)

Others pull-up Resistors close
DIMM Slot 750 mil (MAX)

DDR_A_MA3 DDR_A_MA3 9,13
DDR_A_MA1 DDR_A_MA1 9,13
DDR_A_MA8 DDR_A_MA8 9,13
DDR_A_MA9 DDR_A_MA9 9,13
DDR_A_MA11 DDR_A_MA11 9,13
DDR_A_MA10 DDR_A_MA10 9,13
DDR_A_CAS# DDR_A_CAS# 9,13
DDR_A_RAS# DDR_A_RAS# 9,13
M_ODT0 M_ODT0 8,13

DDR_CS2_DIMMB# DDR_CS2_DIMMB# 8
DDR_CS3_DIMMB# DDR_CS3_DIMMB# 8
DDR_CKE2_DIMMB DDR_CKE2_DIMMB 8,13
DDR_CKE3_DIMMB DDR_CKE3_DIMMB 8,13
DDR_B_RAS# DDR_B_RAS# 9,13
DDR_B_CAS# DDR_B_CAS# 9,13
DDR_B_WE# DDR_B_WE# 9
M_ODT2 M_ODT2 8
M_ODT3 M_ODT3 8

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2-SODIMM2
Size: A3
Document Number: Siberia / Converse
Rev: SA
Date: Friday, September 01, 2006
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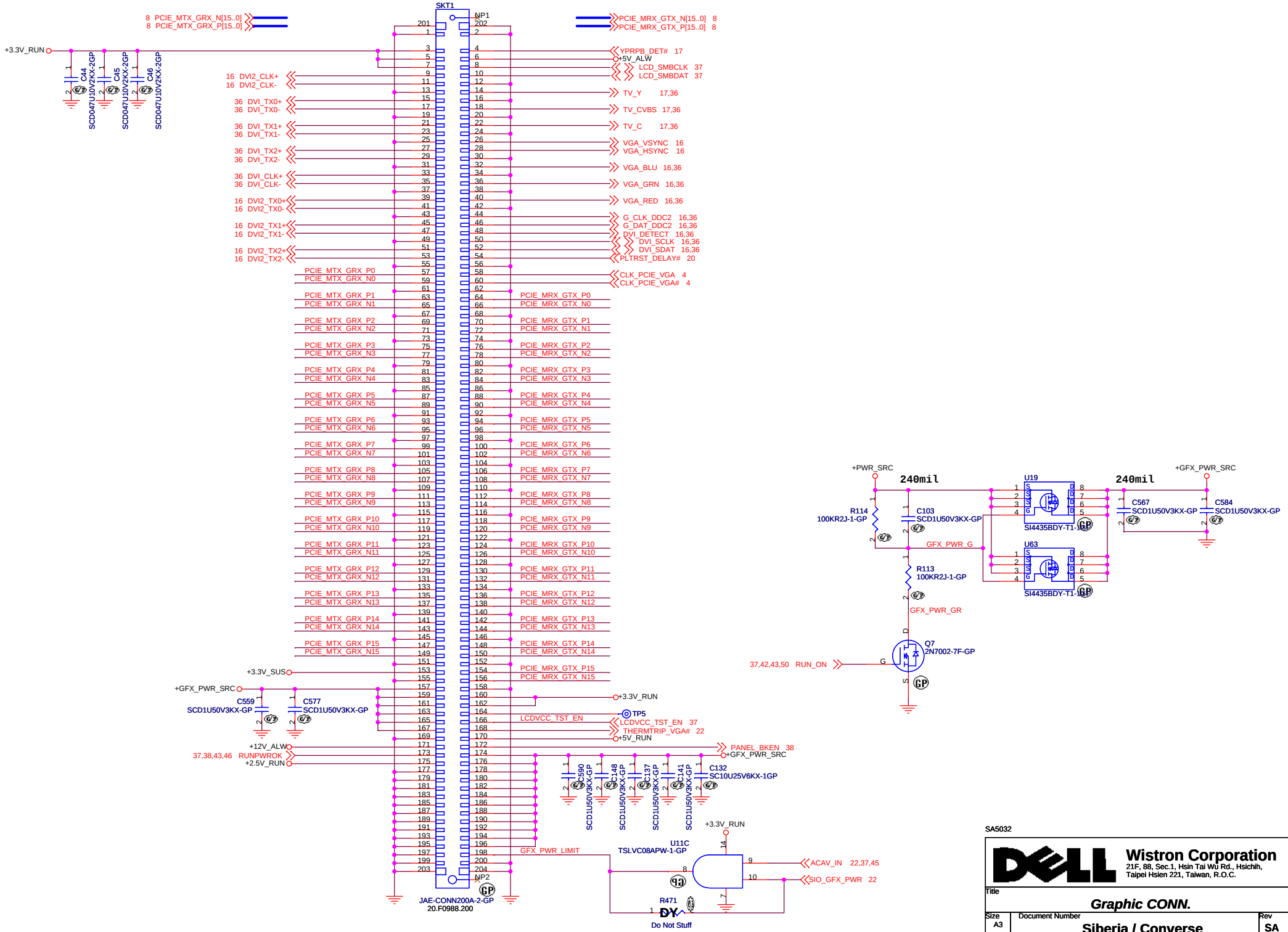

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Graphic CONN.***

Size	Document Number	Rev
A3	**Siberia / Converse**	SA

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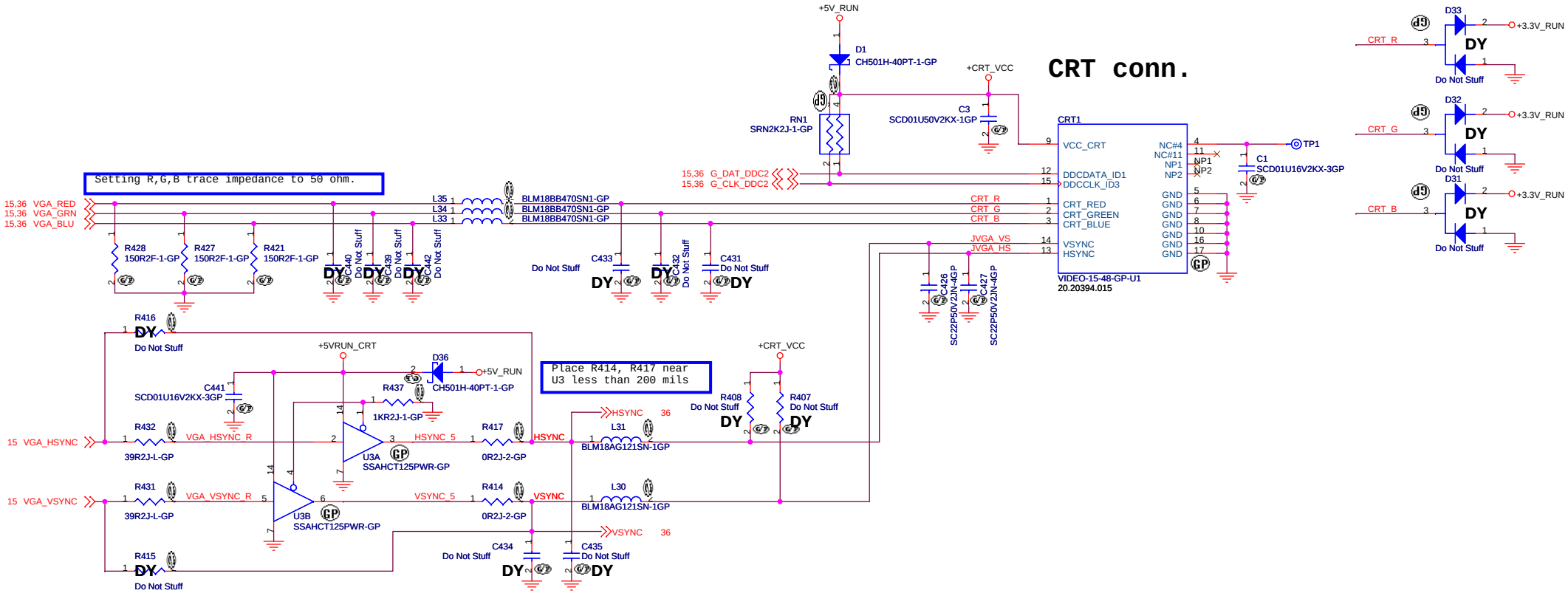

SA5032

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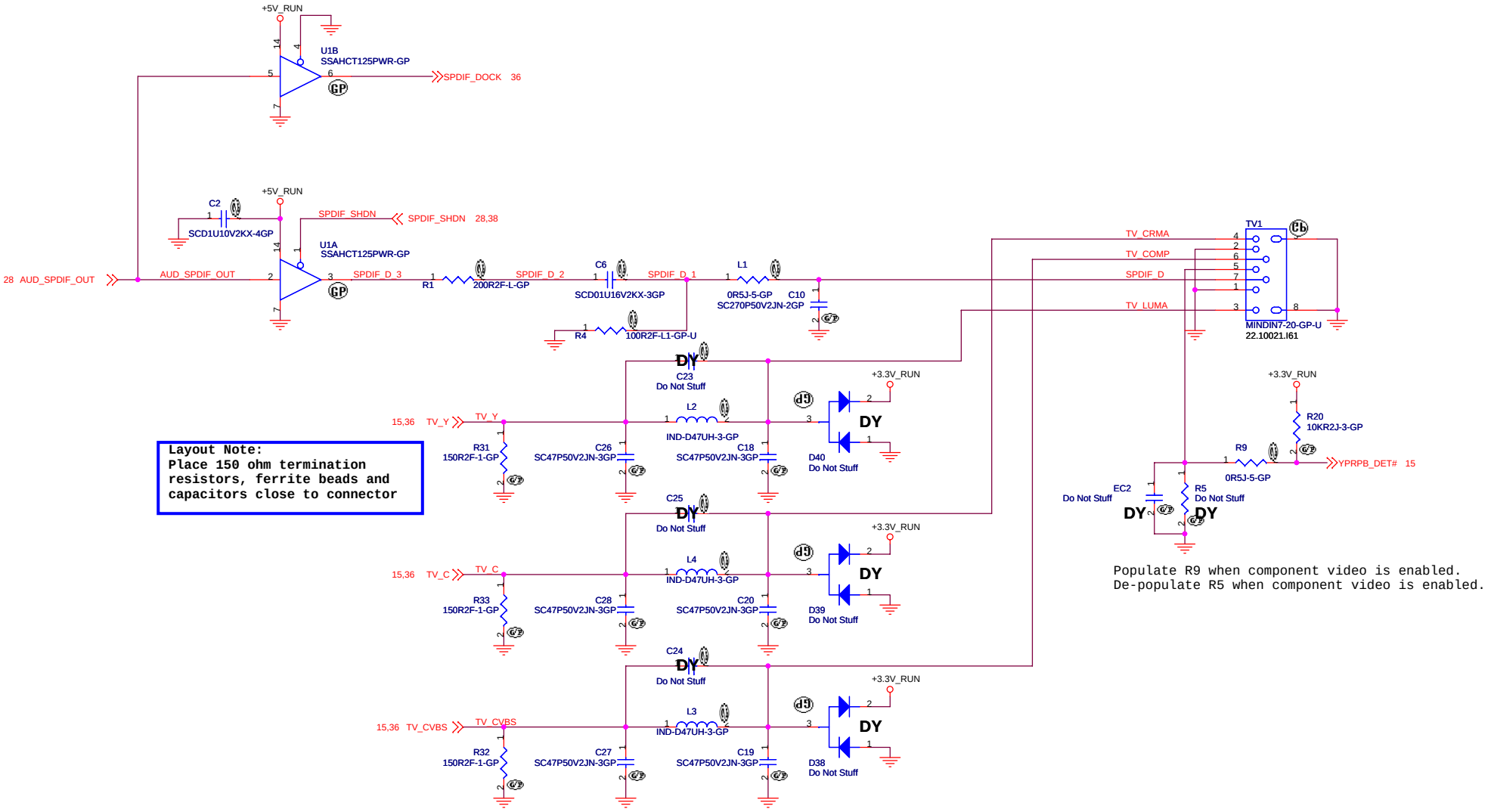
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT / DVI OUT***

Size	Document Number	Rev
A3	Siberia / Converse	SA

Date: Friday, September 01, 2006 Sheet 16 of 53



Layout Note:
Place 150 ohm termination resistors, ferrite beads and capacitors close to connector

Populate R9 when component video is enabled.
De-populate R5 when component video is enabled.

SA5032

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TV OUT***

Size	Document Number	Rev
A3	**Siberia / Converse**	SA

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RTC circuitry

+PWR_SRC
U14
SHDN# IN
GND
5/3#(FB) OUT
Do Not Stuff
DY
C70
Do Not Stuff
DY
+3.3V_RTC_LDO
C738
SC2D2U6D3V3MX-1-GP
D45
CH751H-40PT-1GP
+RTC_CELL
C315
SC1U10V3KX-3GP
RTC1
PWR
GND
MH1
MH2
BAT-CON2-U2-GP
22.70031.001
+RTC
+RTC_VCC
R284
1KR2J-1-GP
D16
CH751H-40PT-1GP
R677
20KR2J-L2-GP
ICH_RTCRST#
R682
1MR2J-1-GP
C742
SC1U10V3KX-3GP
ICH_INTRUDER#
R73
10MR3J-L1-GP
ICH_RTC_X2
R711
0R2J-2-GP
X5
X-32D768KHZ-39GP
C756
SC3D3P50V2CN-GP
C765
SC3D3P50V2CN-GP

Place all series terms close to ICH8 except for SDIN input lines, which shoud be close to source. Placement of R698, R699, R7138 & R723 should equal distance to th T split trace point as R693, R694, R710 & R722 respective. Basically, keep the same distance from T for all series termination resistors.

28 ICH_AZ_CODEC_BITCLK
30 ICH_AZ_MDC_BITCLK
ICH_AZ_CODEC_BITCLK R722 33R2J-2-GP
ICH_AZ_MDC_BITCLK R723 33R2J-2-GP
28 ICH_AZ_CODEC_SYNC
30 ICH_AZ_MDC_SYNC
ICH_AZ_CODEC_SYNC R710 33R2J-2-GP
ICH_AZ_MDC_SYNC R713 33R2J-2-GP
28 ICH_AZ_CODEC_RST#
30 ICH_AZ_MDC_RST#
ICH_AZ_CODEC_RST# R693 33R2J-2-GP
ICH_AZ_MDC_RST# R698 33R2J-2-GP
28 ICH_AZ_CODEC_SDOUT
30 ICH_AZ_MDC_SDOUT
ICH_AZ_CODEC_SDOUT R694 33R2J-2-GP
ICH_AZ_MDC_SDOUT R699 33R2J-2-GP

+1.5V_PCIE_ICH
R628 24D9R2F-L-GP
GLAN_COMP place within 500 mil of ICH8M

This circuit is only needed if the platform has the SNIFFER

+3.3V_RUN
32,38 LED_MASK#
R681 10KR2J-3-GP
41 SATA_ACT#
SATA_ACT# R
Q74 2N7002-7F-GP
R679 DY Do Not Stuff

23 SATA_RX0-
23 SATA_RX0+
23 SATA_TX0-
23 SATA_TX0+
C759 SC3900P50V3KX-GP
C760 SC3900P50V3KX-GP
23 SATA_RX2-
23 SATA_RX2+
23 SATA_TX2-
23 SATA_TX2+
C758 SC3900P50V3KX-GP
C757 SC3900P50V3KX-GP
Distance between the ICH8-M and cap on the "P" signal should be identical distance between the ICH8-M and cap on the "N" signal for same pair.

4 CLK_PCIE_SATA#
4 CLK_PCIE_SATA
R691 24D9R2F-L-GP
SM_SATASB Place within 500 mil of ICH8-M

1 OF 6
ICH8-M-1-GP-U
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
RTC
LPC
LAN/GLAN
CPU
IHDA
SATA
IDE

U85A
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LPC_LAD0 26,37,38
LPC_LAD1 26,37,38
LPC_LAD2 26,37,38
LPC_LAD3 26,37,38
LPC_FRAME# 26,37,38
LPC_DRQ0# 38
LPC_DRQ1# 38
SIO_A20GATE 37
H_A20M# 5
H_DPRSTP# 5,8,46
H_DPSLP# 5
H_FERR# 5
H_PWRGOOD 5
H_IGNNE# 5
H_INIT# 5
H_INTR# 5
SIO_RCIN# 37
H_NMI# 5
H_SMI# 5
H_STPCLK# 5
THERMTRIP# ICH
TP21
IDE_DD[15..0] 23
IDE_DA0 23
IDE_DA1 23
IDE_DA2 23
IDE_DCS1# 23
IDE_DCS3# 23
IDE_DIOR# 23
IDE_DIOW# 23
IDE_DDACK# 23
IDE_IRQ 23
IDE_DIORDY 23
IDE_DDREQ 23

+1.05V_VCCP
R675 56R2J-4-GP
56 ohm must be place within 2"of stub
R678 Do Not Stuff DY
R670 Do Not Stuff DY
H_DPRSTP#
H_DPSLP#

SIO_A20GATE
SIO_RCIN#
R707 10KR2J-3-GP
R728 10KR2J-3-GP
+3.3V_RUN

ICH8-Strap PIN

+3.3V_RUN
20,28 SPKR
SPKR R714 DY Do Not Stuff
ACZ_DOUT R702 DY Do Not Stuff
20 ICH_RSVD
ICH_RSVD R726 DY Do Not Stuff

No Reboot Strap	
SPKR	LOW = Defaule High=No Reboot

XOR Chain Entrance Strap

ICH_RSVD	ACZ_DOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

+RTC_CELL
R684 330KR2F-L-GP
ICH_INTVRMEN
R683 Do Not Stuff DY
+RTC_CELL
R665 330KR2F-L-GP
ICH_LAN100_SLP
R669 Do Not Stuff DY

integrated VccSus1_05,VccSus1_5,VccCL1_5		
ICH_INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
ICH_LAN100_SLP	High=Enable	Low=Disable

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8M-RTC/IDE/LPC/DHI (1/4)
Size: A3
Document Number: Siberia / Converse
Rev: SA
Date: Thursday, September 07, 2006
Sheet 18 of 53

PCIE Interface Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	MiniCard WPAN
LANE4	Express Card
LANE5	No use
LANE6	Giba Bit LOM

PCIE TX dc blocking
Capacitors close to ICH8-M

U85B 2 OF 6

PCI-Express / Direct Media Interface

PCIE_RX1- P27 PERN1
PCIE_RX1+ P26 PERP1
PCIE_TX1- C723 SCD1U10V2KX-4GP PCIE_TXN1_C N29 PETN1
PCIE_TX1+ C719 SCD1U10V2KX-4GP PCIE_TXP1_C N28 PETP1

PCIE_RX2- M27 PERN2
PCIE_RX2+ M26 PERP2
PCIE_TX2- C717 SCD1U10V2KX-4GP PCIE_TXN2_C L29 PETN2
PCIE_TX2+ C715 SCD1U10V2KX-4GP PCIE_TXP2_C L28 PETP2

PCIE_RX3- K27 PERN3
PCIE_RX3+ K26 PERP3
PCIE_TX3- C711 SCD1U10V2KX-4GP PCIE_TXN3_C J29 PETN3
PCIE_TX3+ C713 SCD1U10V2KX-4GP PCIE_TXP3_C J28 PETP3

PCIE_RX4- H27 PERN4
PCIE_RX4+ H26 PERP4
PCIE_TX4- C708 SCD1U10V2KX-4GP PCIE_TXN4_C G29 PETN4
PCIE_TX4+ C705 SCD1U10V2KX-4GP PCIE_TXP4_C G28 PETP4

E27 PERN5
E26 PERP5
E29 PETN5
E28 PETP5

PCIE_RX6-/GLAN_RX- D27 PERN6/GLAN_RXN
PCIE_RX6+/GLAN_RX+ D26 PERP6/GLAN_RXP
PCIE_TX6-/GLAN_TX- C702 SCD1U10V2KX-4GP GLAN_TXN_C C29 PETN6/GLAN_TXN
PCIE_TX6+/GLAN_TX+ C698 SCD1U10V2KX-4GP GLAN_TXP_C C28 PETP6/GLAN_TXP

DMI0RXN V27 DMI_MTX_IRX_N0 → DMI_MTX_IRX_N0 8
DMI0RXP V26 DMI_MTX_IRX_P0 → DMI_MTX_IRX_P0 8
DMI0TXN U29 DMI_MRX_ITX_N0 → DMI_MRX_ITX_N0 8
DMI0TXP U28 DMI_MRX_ITX_P0 → DMI_MRX_ITX_P0 8

DMI1RXN Y27 DMI_MTX_IRX_N1 → DMI_MTX_IRX_N1 8
DMI1RXP Y26 DMI_MTX_IRX_P1 → DMI_MTX_IRX_P1 8
DMI1TXN W29 DMI_MRX_ITX_N1 → DMI_MRX_ITX_N1 8
DMI1TXP W28 DMI_MRX_ITX_P1 → DMI_MRX_ITX_P1 8

DMI2RXN AB26 DMI_MTX_IRX_N2 → DMI_MTX_IRX_N2 8
DMI2RXP AB25 DMI_MTX_IRX_P2 → DMI_MTX_IRX_P2 8
DMI2TXN AA29 DMI_MRX_ITX_N2 → DMI_MRX_ITX_N2 8
DMI2TXP AA28 DMI_MRX_ITX_P2 → DMI_MRX_ITX_P2 8

DMI3RXN AD27 DMI_MTX_IRX_N3 → DMI_MTX_IRX_N3 8
DMI3RXP AD26 DMI_MTX_IRX_P3 → DMI_MTX_IRX_P3 8
DMI3TXN AC29 DMI_MRX_ITX_N3 → DMI_MRX_ITX_N3 8
DMI3TXP AC28 DMI_MRX_ITX_P3 → DMI_MRX_ITX_P3 8

DMI_CLKN T26 CLK_PCIE_ICH# → CLK_PCIE_ICH# 4
DMI_CLKP T25 CLK_PCIE_ICH → CLK_PCIE_ICH 4

DMI_ZCOMP Y23 DMI_COMP — R266 1 24D9R2F-L-GP — +1.5V_PCIE_ICH
DMI_IRCOMP Y24

DMI_COMP R158 place within 500 mil of ICH8M

SPI

37 ICH_EC_SPI_CLK — R625 1 15R2J-GP — ICH_EC_SPI_CLK_R C23 SPI_CLK
ICH_SPI_CS# B23 SPI_CS0#
ICH_SPI_CS1#_R E22 SPI_CS1#

37 ICH_EC_SPI_DO — R624 1 15R2J-GP — ICH_EC_SPI_DO_R D23 SPI_MOSI
37 ICH_EC_SPI_DIN ICH_EC_SPI_DIN F21 SPI_MISO

USB

33 USB_OC0_1# — USB_OC0_1# AJ19 OC0#
AG16 OC1#/GPIO40
AG15 OC2#/GPIO41
29 USB_OC2_3# — USB_OC2_3# AE15 OC3#/GPIO42
33 USB_OC4_5# — USB_OC4_5# AF15 OC4#/GPIO43
AG17 OC5#/GPIO29
USB_OC6# AD12 OC6#/GPIO30
USB_OC7# AJ18 OC7#/GPIO31
USB_OC8# AD14 OC8#
USB_OC9# AH18 OC9#

USBP0N G3 ICH_USBP0- 33
USBP0P G2 ICH_USBP0+ 33
USBP1N H5 ICH_USBP1- 33
USBP1P H4 ICH_USBP1+ 33
USBP2N H2 ICH_USBP2- 29
USBP2P H1 ICH_USBP2+ 29
USBP3N J3 ICH_USBP3- 29
USBP3P J2 ICH_USBP3+ 29
USBP4N K5 ICH_USBP4- 33
USBP4P K4 ICH_USBP4+ 33
USBP5N K2 ICH_USBP5- 36
USBP5P K1 ICH_USBP5+ 36
USBP6N L3 ICH_USBP6- 31
USBP6P L2 ICH_USBP6+ 31
USBP7N M5 ICH_USBP7- 29
USBP7P M4 ICH_USBP7+ 29
USBP8N M2 ICH_USBP8- 32
USBP8P M1 ICH_USBP8+ 32
USBP9N N3 ICH_USBP9- 40
USBP9P N2 ICH_USBP9+ 40

USBRBIAS# E2
USBRBIAS F3 — R238 1 22D6R2F-L1-GP

GP

ICH8-M-1-GP-U

USBRBIAS close to ICH8M 500 mils and Trace impedance should be 60 ohm +/- 15%

Layout Note:
Place R624, R625 and R626 within 500 mils from ICH.

ICH8-Strap PIN

BOOT BIOS Strap

PCI_GNT#0 (R617)	SPI_CS#1 (R623)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

A16 swap override strap

PCI_GNT#3 (R620)	
	low = A16 swap override enable high = default

20,35 PCI_GNT#0 — PCI_GNT#0 — R617 1 1KR2J-1-GP
ICH_SPI_CS1#_R — R623 1 DY Do Not Stuff
20 PCI_GNT#3 — PCI_GNT#3 — R620 1 DY Do Not Stuff

R601 1 0R2J-2-GP — ICH_SPI_CS0# — +3.3V_ALW
R600 1 Do Not Stuff DY — SPI_CS0#_R
40 SPI_CS0#
U75 (VCC 5, Y 4, B 1, A 2, GND 3)
R626 1 15R2J-GP — ICH_SPI_CS#
SIO_SPI_CS# 37
Do Not Stuff DY

USB OC# PULL HIGH

+3.3V_SUS
RP4 SRN10KJ-L3-GP
USB_OC9# 1
USB_OC6# 2
USB_OC7# 3
+3.3V_SUS 4
5
10 USB_OC2_3#
9 USB_OC8#
8 USB_OC4_5#
7 USB_OC0_1#
6

ICH

USB0	Ext Side (Left)
USB1	Ext Side (Right)
USB2	Ext I/O BD Side (Top)
USB3	Ext I/O BD Side (Bottom)
USB4	Ext Back (Bottom)
USB5	Dock/Ext Back (Top)
USB6	Express Card
USB7	BT
USB8	3rd mini card
USB9	USB Hub

USB Hub

USB1	SmartCard
USB2	Gaming LCD/Biometric
USB3	Camera
USB4	WWAN

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Taipei Hsien 221, Taiwan, R.O.C.

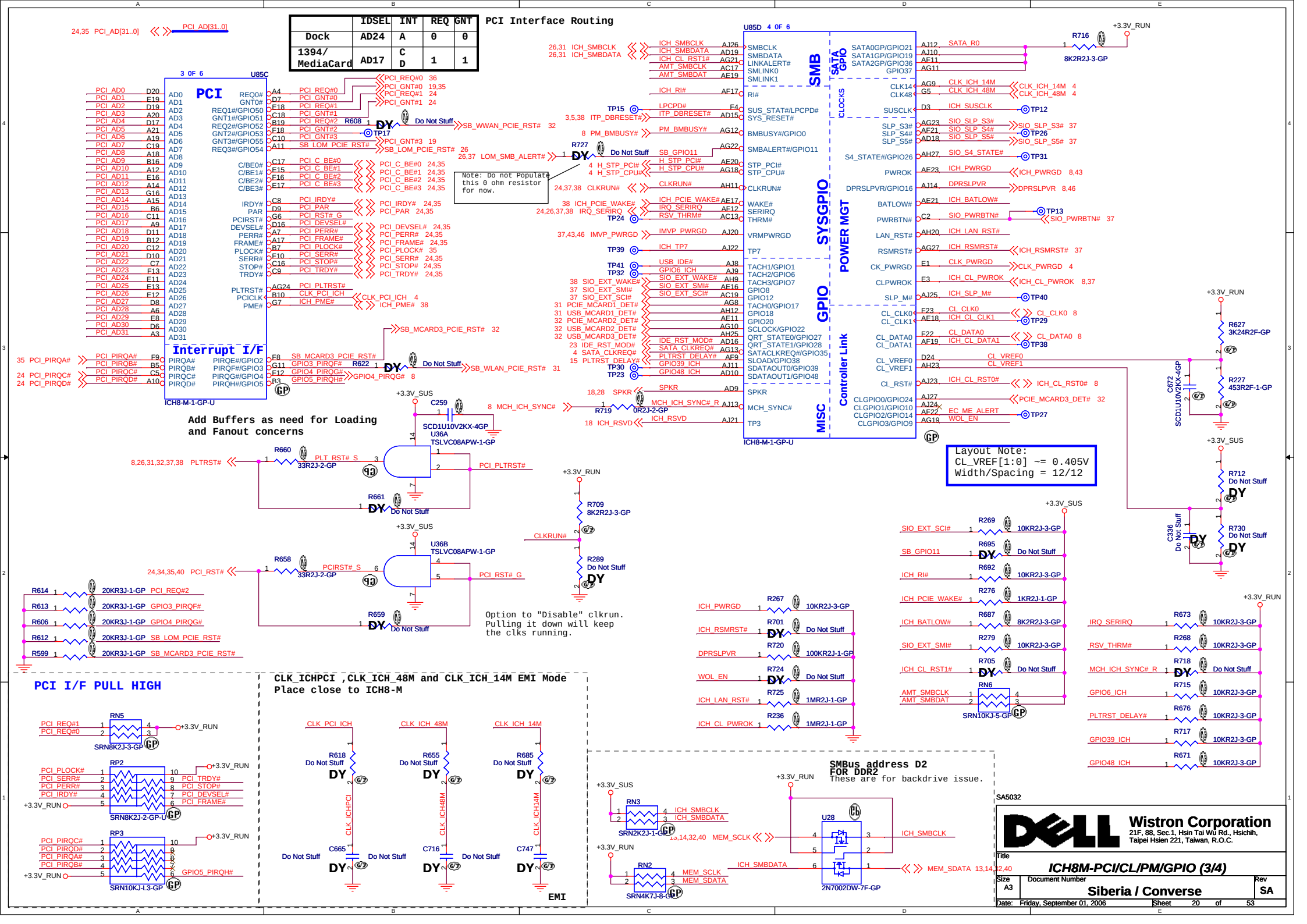
Title: ICH8M-PCIE/USB/SPI/DMI (2/4)

Size	Document Number	Rev
A3	Siberia / Converse	SA

Date: Friday, September 01, 2006 Sheet 19 of 53

	IDSEL	INT	REQ	GNT
Dock	AD24	A	0	0
1394/ MediaCard	AD17	C D	1	1

PCI Interface Routing



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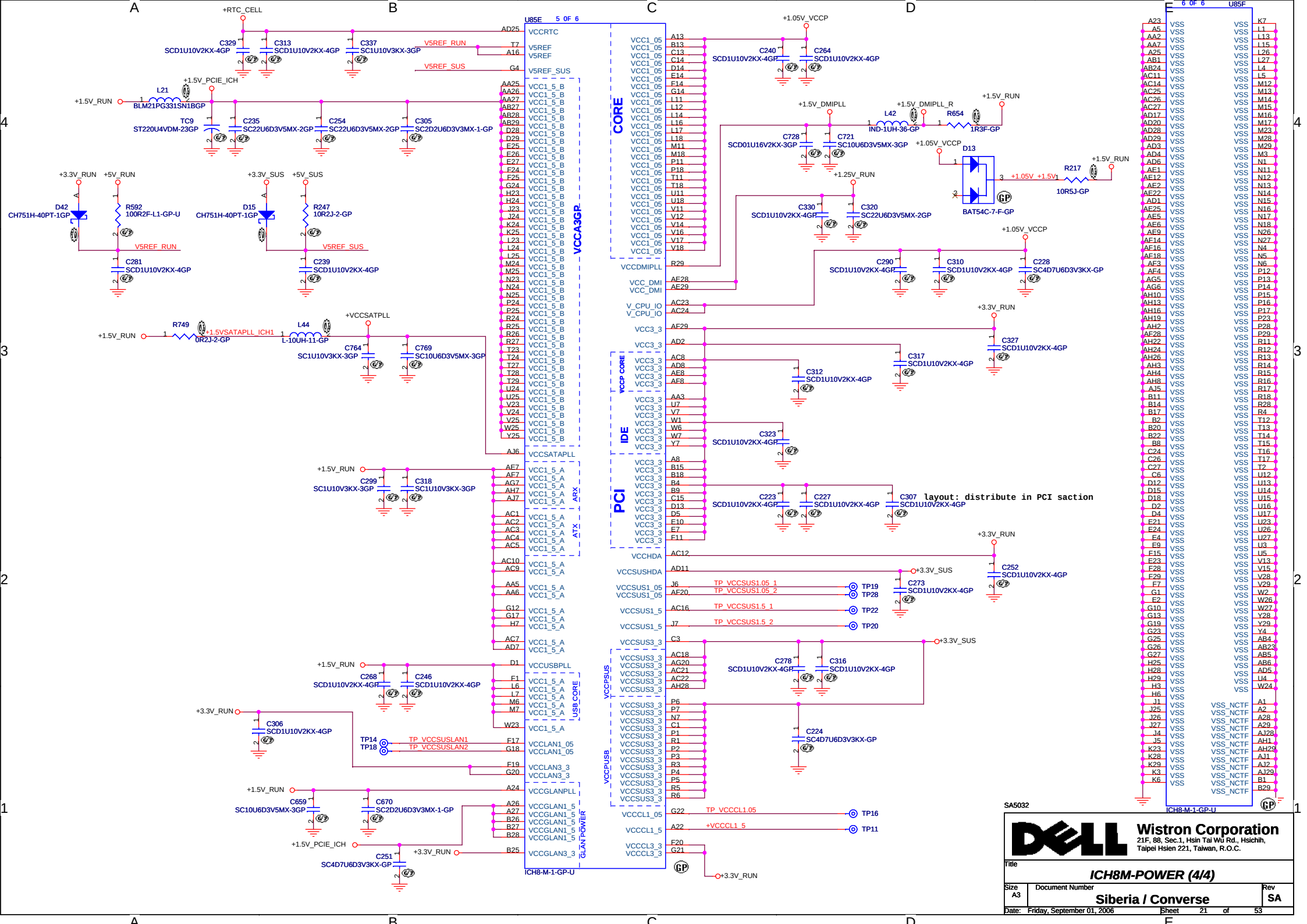
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ICH8M-PCI/CL/PM/GPIO (3/4)*

Size: A3 | Document Number: Siberia / Converse | Rev: SA

Date: Friday, September 01, 2006 | Sheet 20 of 53


U85E 5 OF 6
VCCRTC
V5REF
V5REF_SUS
VCC1_5_B
VCCA3GP
VCCSATAPLL
VCC1_5_A
ARX
ATX
VCCUSBPLL
USB_CORE
VCCLAN1_05
VCCLAN3_3
VCCGLANPLL
GLAN_POWER
CORE
VCCDMIPLL
VCC_DMI
V_CPU_IO
VCC3_3
VCCP CORE
IDE
PCI
VCCHDA
VCCSUSHDA
VCCSUS1_05
VCCSUS1_5
VCCSUS3_3
VCCPSUS
VCCPUSB
VCCCL1_05
VCCCL1_5
VCCCL3_3
ICH8-M-1-GP-U
U85F 6 OF 6
VSS
VSS_NCTF
ICH8-M-1-GP-U
+RTC_CELL
C329 SCD1U10V2KX-4GP
C313 SCD1U10V2KX-4GP
C337 SC1U10V3KX-3GP
V5REF_RUN
V5REF_SUS
+1.5V_PCIE_ICH
+1.5V_RUN
L21 BLM21PG331SN1BGP
TC9 ST220U4VDM-23GP
C235 SC22U6D3V5MX-2GP
C254 SC22U6D3V5MX-2GP
C305 SC2D2U6D3V3MX-1-GP
+3.3V_RUN
+5V_RUN
D42 CH751H-40PT-1GP
R592 100R2F-L1-GP-U
C281 SCD1U10V2KX-4GP
+3.3V_SUS
+5V_SUS
D15 CH751H-40PT-1GP
R247 10R2J-2-GP
C239 SCD1U10V2KX-4GP
+VCCSATPLL
R749 0R2J-2-GP
+1.5VSATAPLL_ICH1
L44 L-10UH-11-GP
C764 SC1U10V3KX-3GP
C769 SC10U6D3V5MX-3GP
C299 SC1U10V3KX-3GP
C318 SC1U10V3KX-3GP
C268 SCD1U10V2KX-4GP
C246 SCD1U10V2KX-4GP
C306 SCD1U10V2KX-4GP
TP14
TP18
TP_VCCSUSLAN1
TP_VCCSUSLAN2
C659 SC10U6D3V5MX-3GP
C670 SC2D2U6D3V3MX-1-GP
C251 SC4D7U6D3V3KX-GP
+1.05V_VCCP
C240 SCD1U10V2KX-4GP
C264 SCD1U10V2KX-4GP
+1.5V_DMIPLL
+1.5V_DMIPLL_R
L42 IND-1UH-36-GP
R654 1R3F-GP
C728 SCD01U16V2KX-3GP
C721 SC10U6D3V5MX-3GP
+1.25V_RUN
C330 SCD1U10V2KX-4GP
C320 SC22U6D3V5MX-2GP
D13 BAT54C-7-F-GP
+1.05V +1.5V
R217 10R5J-GP
C290 SCD1U10V2KX-4GP
C310 SCD1U10V2KX-4GP
C228 SC4D7U6D3V3KX-GP
C327 SCD1U10V2KX-4GP
C317 SCD1U10V2KX-4GP
C312 SCD1U10V2KX-4GP
C323 SCD1U10V2KX-4GP
C223 SCD1U10V2KX-4GP
C227 SCD1U10V2KX-4GP
C307 SCD1U10V2KX-4GP
layout: distribute in PCI saction
C252 SCD1U10V2KX-4GP
C273 SCD1U10V2KX-4GP
TP_VCCSUS1.05_1
TP_VCCSUS1.05_2
TP_VCCSUS1.5_1
TP_VCCSUS1.5_2
TP19
TP28
TP22
TP20
C278 SCD1U10V2KX-4GP
C316 SCD1U10V2KX-4GP
C224 SC4D7U6D3V3KX-GP
TP_VCCCL1.05
+VCCCL1_5
TP16
TP11
SA5032
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8M-POWER (4/4)
Size A3
Document Number
Siberia / Converse
Rev SA
Date: Friday, September 01, 2006
Sheet 21 of 53

SSID = THERMAL

REM_DIODE1_N and REM_DIODE1_P routing Trace width and Spacing use 10 / 10 mil

Place inside CPU socket

Locate C371 near Guardian

H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil

Place near the bottom SODIMM CONN

should be placed TOP Side under mini Card

should be placed Bot Side under Graphic Card

should be placed TOP Side under ODD

Note :

VSET = (Tp - 70) / 21
3.3 * (R411/ R406 + R411) = (Tp - 70) / 21
Where Tp = 70 to 101 degrees C
Tp set at 88 degrees C
Guardian temp tolerance = +/- 3 degrees C

pull up on SIO

pull up on SIO

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Taipei Hsien 221, Taiwan, R.O.C.

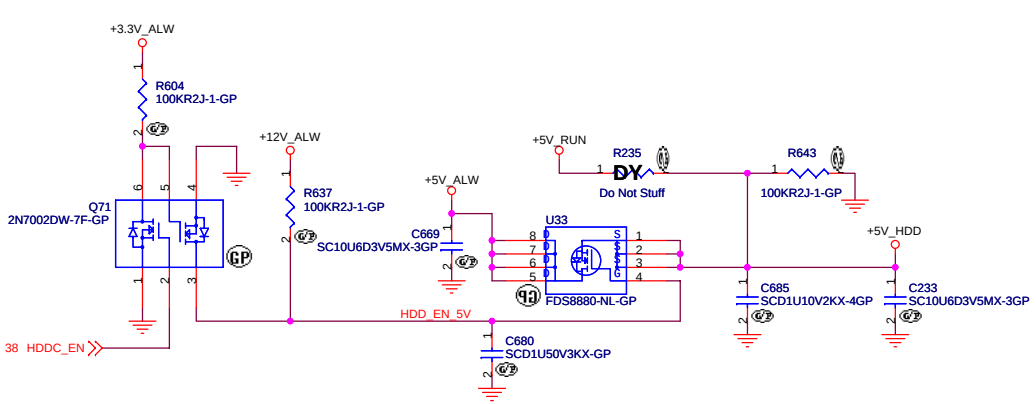
Title: FAN, EMC4001

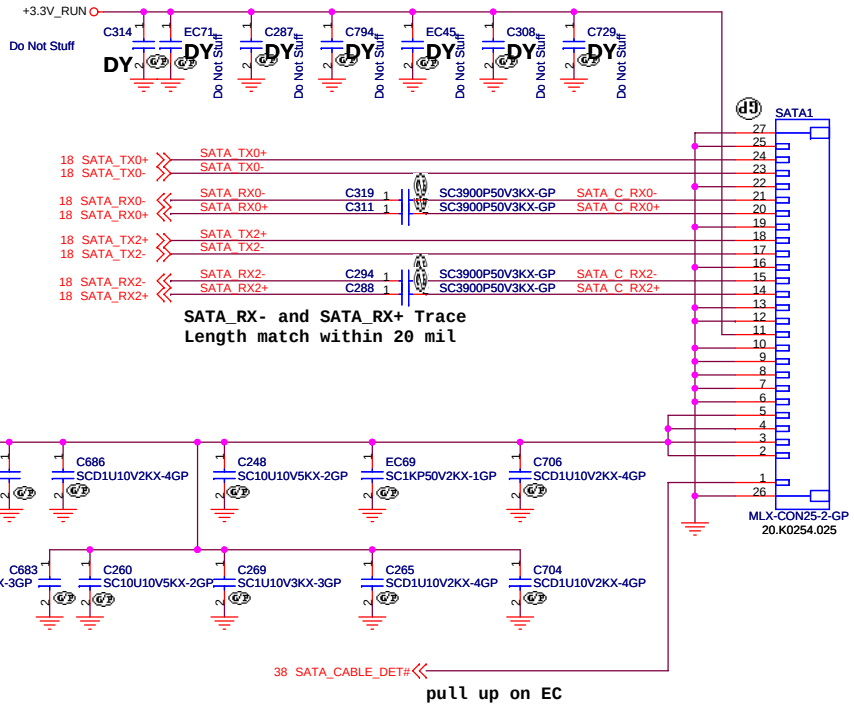
Size: A3 | Document Number: Siberia / Converse | Rev: SA

Date: Friday, September 01, 2006 | Sheet 22 of 53

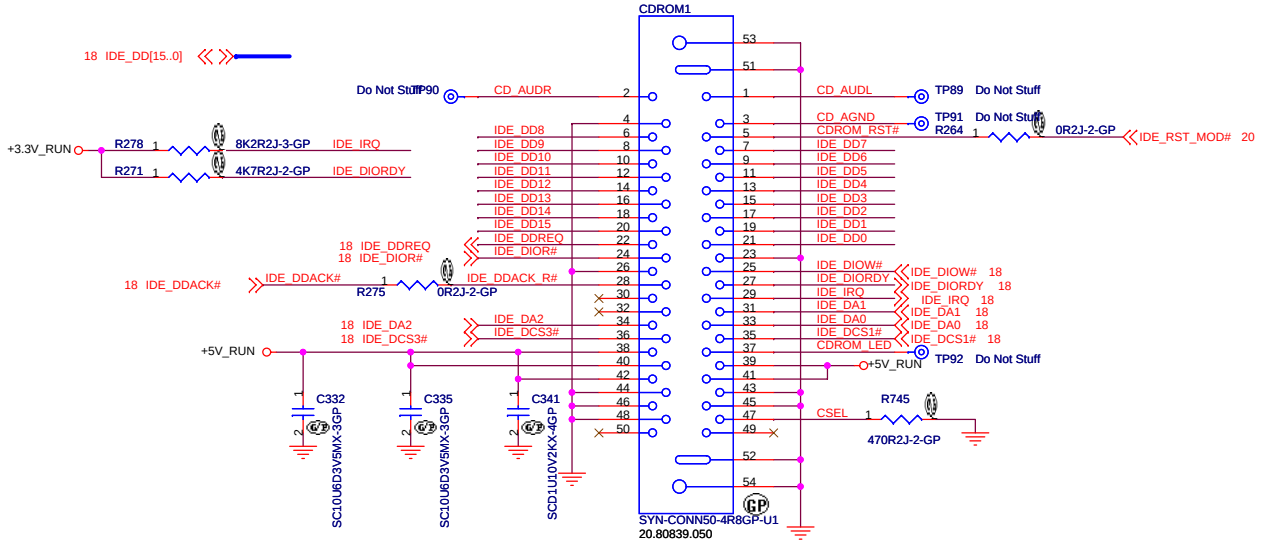
SSID = IDE & SATA

SATA HDD Connector





ODD Connector



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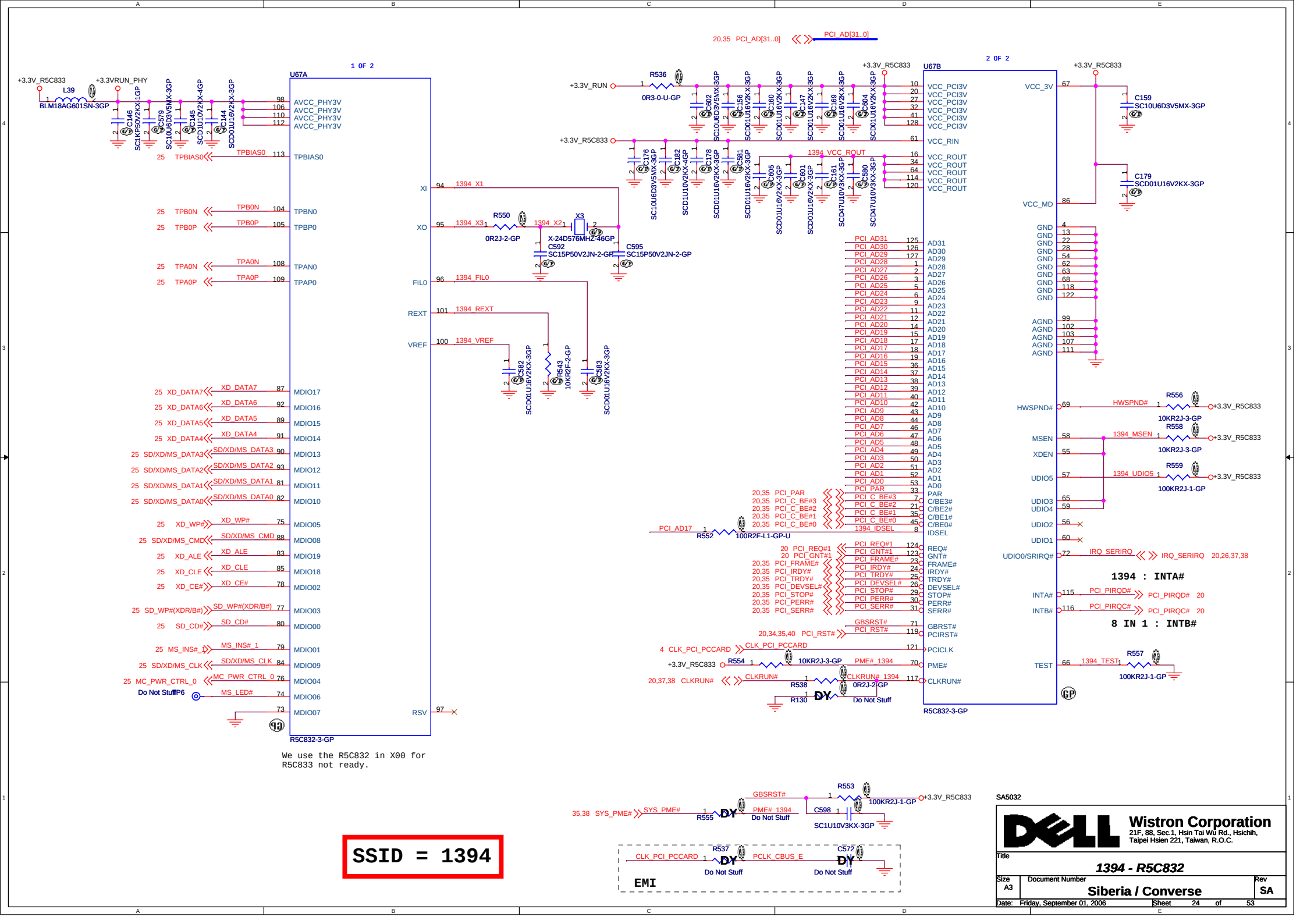
Title: ***HDD&ODD***

Size	Document Number	Rev
A3	**Siberia / Converse**	SA

Date: Friday, September 01, 2006 Sheet 23 of 53



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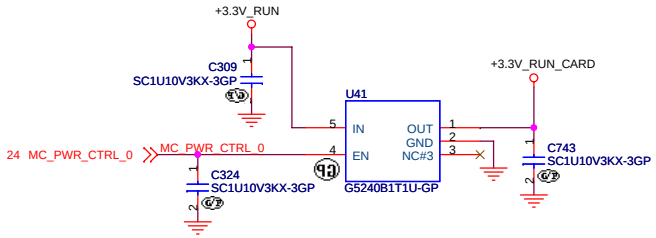
Taipei Hsien 221, Taiwan, R.O.C.

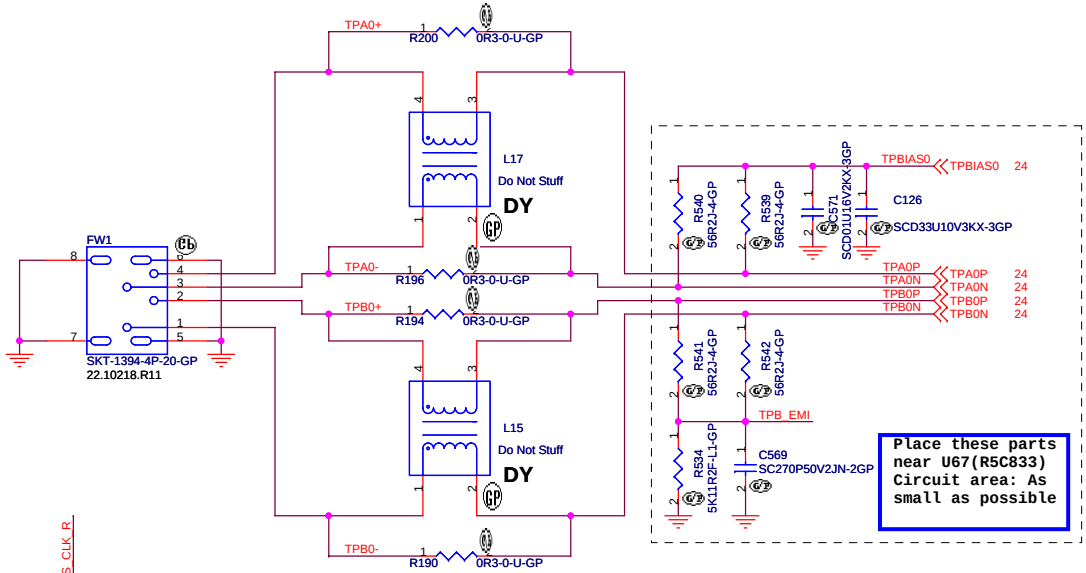
Title: *1394 - R5C832*

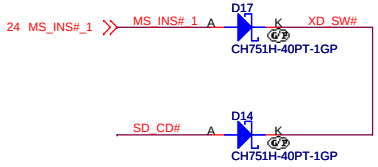
Size: A3 | Document Number: Siberia / Converse | Rev: SA

Date: Friday, September 01, 2006 | Sheet 24 of 53

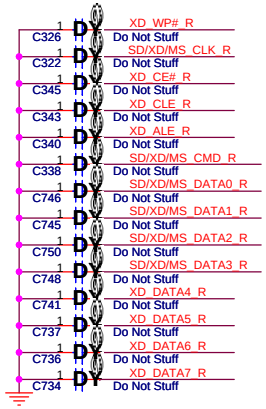
SSID = 1394







These 1394 signalsare high speed differential pairs and must be kept equal length with a differential impedance(Zo) of 110 ohms.



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *1394 - 8 IN 1 Connector*

Size	Document Number	Rev
A3	Siberia / Converse	SA

Date: Friday, September 01, 2006 Sheet 25 of 53

Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

Place one cap close to each of the pins, D9 and E10.

Populate R503 = BLM18AG601SN, C506, C510 if nosie margin on SDSVDD pin above spec

Populate resister for debug

Place resister as close as possible to the ASIC. Pad is needed to measure 125MHz clock for debugging.

Important Layout Note for Dual footprint design:
Atmel part is available in standard package size, where as ST-Micro part is available in narrow package size. Ensure that pads are laid out for bath footprints.
Recommendation: Pads for pins 1 (reference) through 4 can be standard and identically located for both packages. Pads for pins 5-8 need to be larger to accommodate both packages.

	NV_STRAP1	NVSTRAP0	SO	SI	CS#	SCLK
Ato-Sense Mode	0	0	0	0	0	0
ST M45PE20	0	1	1	0	0	1
Atmel AT45BCM021B	0	0	1	0	1	1

Place crystal less than 0.75" (~1.9cm) from LAN Controller

Logic High Voltage must be 0.7V to 2.75V

DOCKED
SEL 0:RJ45.
SEL 1:Dock.

LOM_CABLE_DETECT goes to an input on a system microcontroller that can poll this signal periodically and can de-assert the LOM_LOM_PWR when LOM_CABLE_DETECT signal is high. Connect to an EC GPIO defined by th GPIO mapping.

Layout Note:
PNP Q60 and Q61 needs 0.5 inch by 0.5 inch thermal relief pad.

REGSEN12 and REGSEN25 should be routed using a trace from the load (PNP) back to the controller. Do not use a direct connection to the power plane.

Use 8mils trace width for these signals

Place high-freqency decoupling cpas close to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side ofthe cap to the ground via should also be minimized.

VDDIOPower Decoupling

VDDP Power Decoupling

Core Power Decoupling

Reserve for EMI

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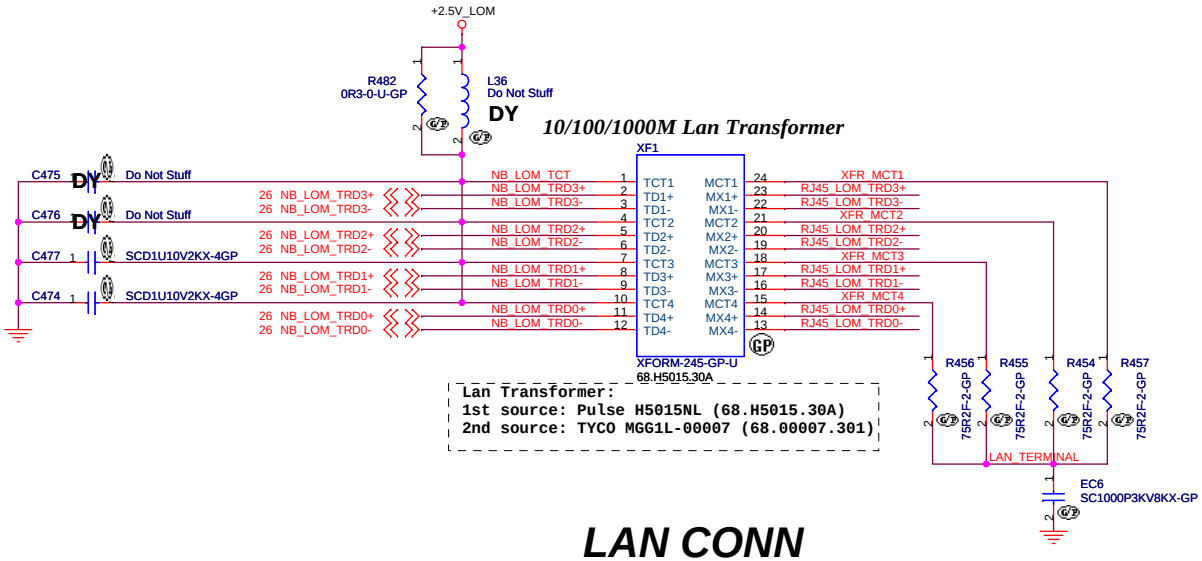
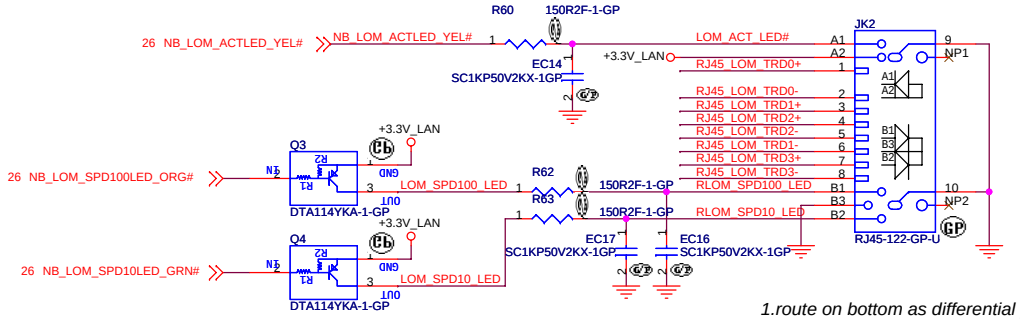
Title: **LAN BCM5756ME**

Size: C | Document Number: Siberia / Converse | Rev: SA

Date: Friday, September 01, 2006 | Sheet 26 of 53



LAN CONN



Yellow LED:TX/RX
Orange LED:Speed 100
Green LED:Speed 10

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

The blowout from the LAN magnetics to the RJ45 connector maintining the distance between the two to be within 1 inch.

Hipot layout guide line update space > 50mil

Rj11 layout guide line update > 100mil

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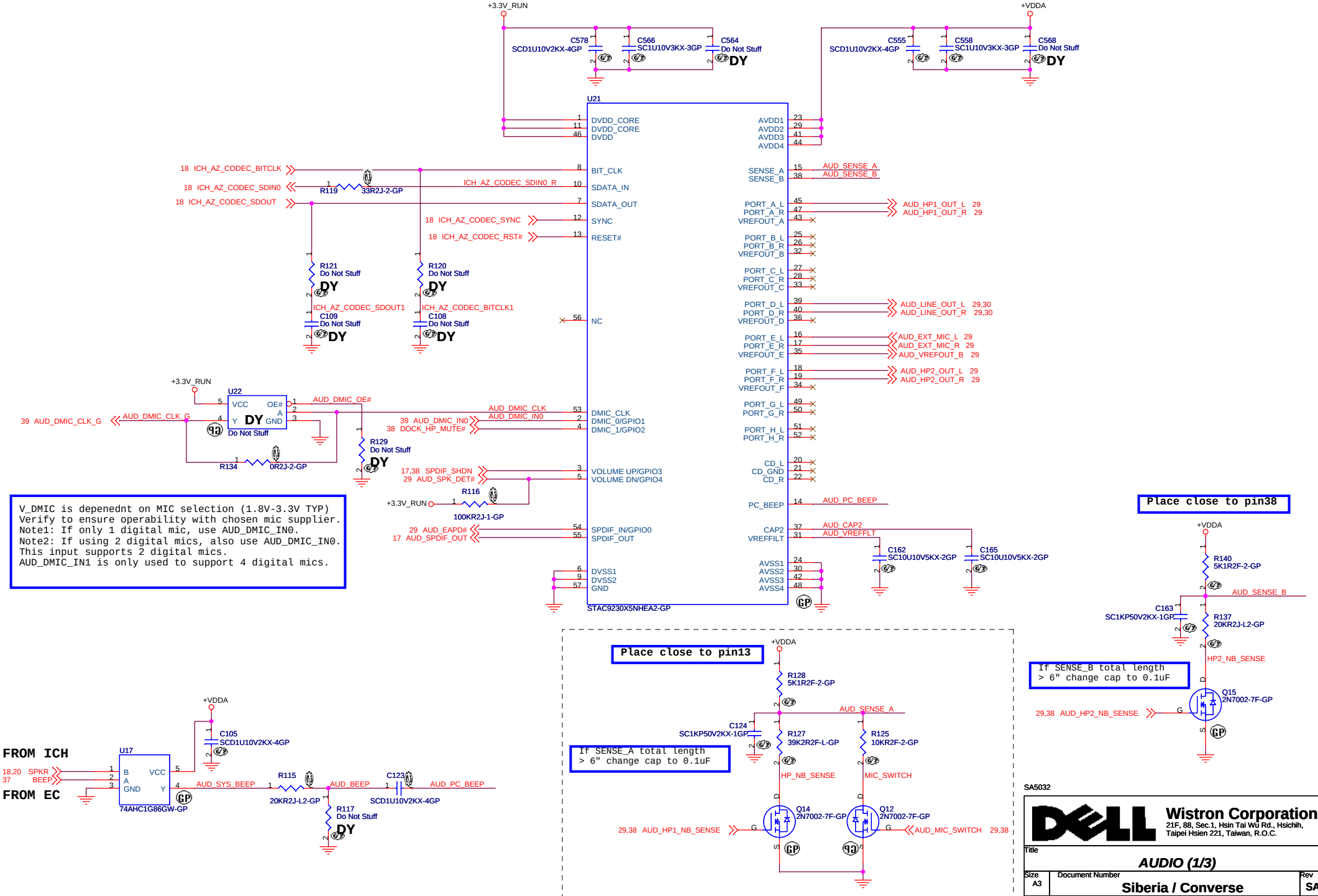
Title: *LAN Connector*

Size	Document Number	Rev
A3	Siberia / Converse	SA

Date: Friday, September 01, 2006 Sheet 27 of 53



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Title: **AUDIO (1/3)**

Size	Document Number	Rev
A3	Siberia / Converse	SA

Date: Friday, September 01, 2006 Sheet 28 of 53

I/O Board / Bluetooth CONN

Speaker

Place just befor +5V_SPK_AMP crosses MOAT.

Place caps close to pin17

Place caps close to pin9

Place caps close to pin8

Place caps close to pin18

R138 used to all low-pass filter for better analog performance.

Close to I/O Board CONN

R359 close to CN6 pin5

parallel with R359

Signal Inverter for Speaker Shutdown. Allows speakers to work while class driver is installed.

This pin should be FLOAT. Do NOT connect to GND.

Need to adjust EMI cap values as necessary.

Close to SPK1

From EC

pull up on EC

pull up on codec.

100 mil

GAIN SETTING RESISTORS

GAIN1	GAIN2	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

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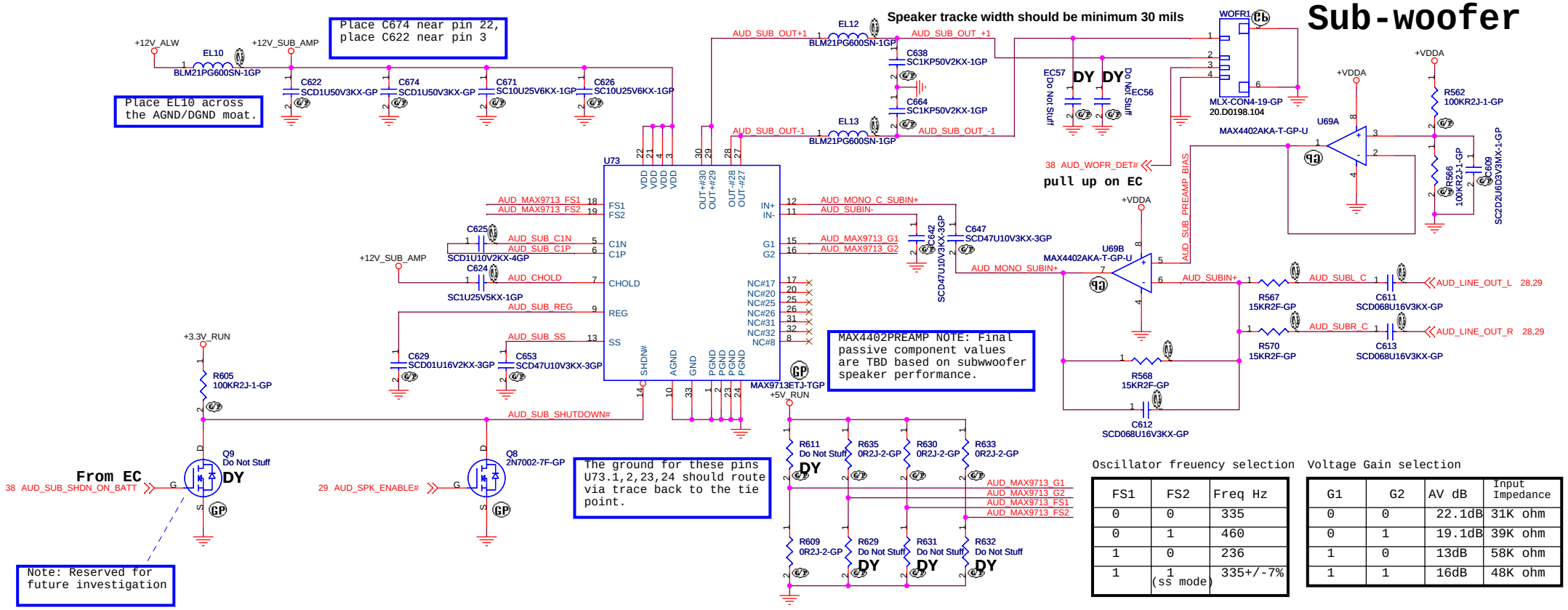
Title: AUDIO (2/3) / Bluetooth

Size: A3 | Document Number: Siberia / Converse | Rev: SA

Date: Friday, September 01, 2006 | Sheet 29 of 53

Sub-woofer



Oscillator freuency selection

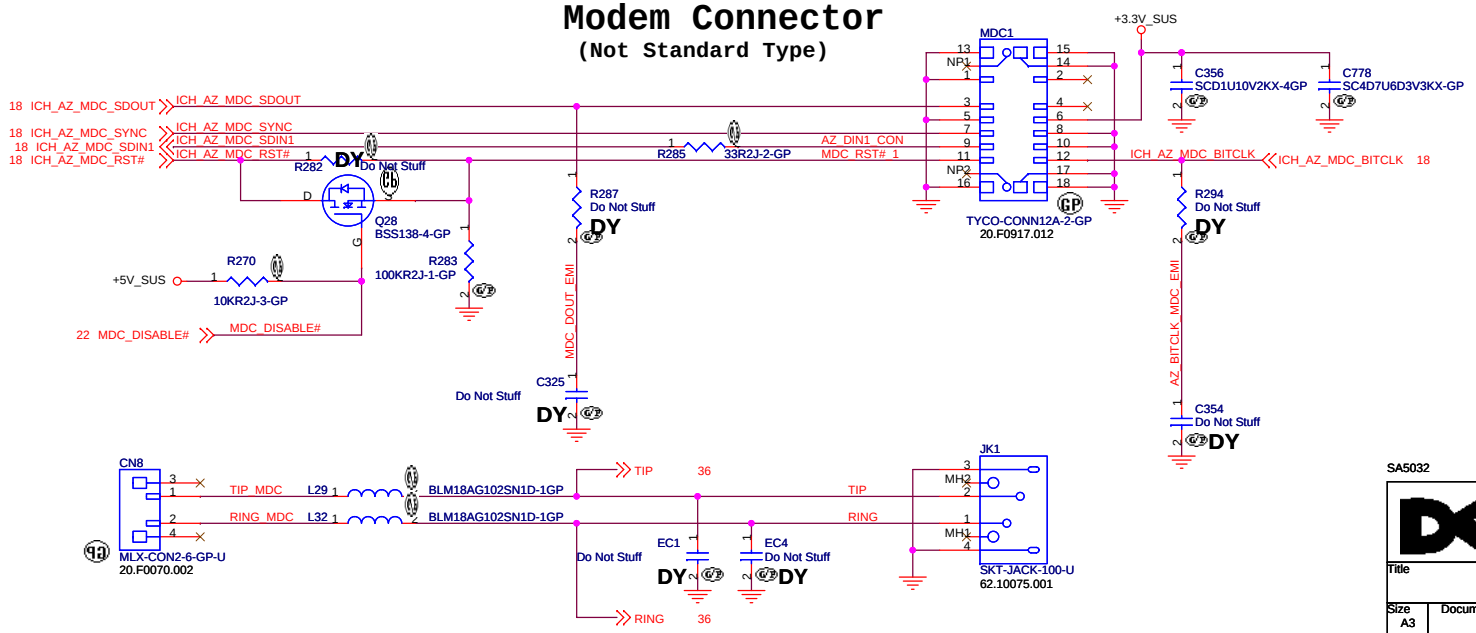
FS1	FS2	Freq Hz
0	0	335
0	1	460
1	0	236
1	1 (ss mode)	335+/-7%

Voltage Gain selection

G1	G2	AV dB	Input Impedance
0	0	22.1dB	31K ohm
0	1	19.1dB	39K ohm
1	0	13dB	58K ohm
1	1	16dB	48K ohm

Modem Connector

(Not Standard Type)



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Title: **AUDIO (3/3) / MDC**

Size: A3 | Document Number: Siberia / Converse | Rev: SA

Date: Friday, September 01, 2006 | Sheet 30 of 53

Please Near the U99

+3.3V_SUS C836 SCD1U10V2KX-4GP
+3.3V_RUN C842 SCD1U10V2KX-4GP
+1.5V_RUN C844 SCD1U10V2KX-4GP
+3.3V_CARDAUX C840 SCD1U10V2KX-4GP
+3.3V_CARD C846 SCD1U10V2KX-4GP
+1.5V_CARD C848 SCD1U10V2KX-4GP

STBY# R787 DY Do Not Stuff EXPRCRD_STDBY# EXPRCRD_STDBY# 38

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

U99 TPS2231RGP-GP
GND THERMAL_PAD OC# RCLKEN# STBY#
NC#16 NC#14 NC#13 NC#5 NC#4 +1.5VIN +1.5VOUT +3VOUT +3VIN
SHDN# PERST# CPUSB# CPPE# SYSRST#
AUXOUT AUXIN 1.5VOUT 1.5VIN 3.3VOUT 3.3VIN

+1.5V_RUN +1.5V_CARD +3.3V_CARD +3.3V_RUN
+3.3V_CARDAUX +3.3V_SUS +1.5V_CARD
+3.3V_RUN +3.3V_CARD +1.5V_RUN

SHDN# R788 100KR2J-1-GP +3.3V_SUS
CARD_RESET# CPUSB# R798 100KR2J-1-GP
EXPRCRD_PWREN# R799 100KR2J-1-GP
NRST R797 0R2J-2-GP PLTRST# PLTRST# 8,20,26,32,37,38

Test circuit
Use Card and No Card

+3.3V_CARD C851 SC10U6D3V5MX-3GP
+3.3V_CARD C838 SCD1U10V2KX-4GP
+1.5V_CARD C853 SC10U6D3V5MX-3GP
+1.5V_CARD C850 SCD1U10V2KX-4GP
Please Near the EPR1

19 ICH_USBP6+ R340 0R3-0-U-GP USBP6D+
EL8 Do Not Stuff DY
19 ICH_USBP6- R341 0R3-0-U-GP USBP6D-

Close EPR1

EXPRESS CARD

EPR1 FOX-CONN30A-5GP 20.F0965.030
+1.5V_CARD +1_5V +1_5V
+3.3V_CARDAUX +3.3V_CARD +3_3VAUX +3_3V +3_3V
SBMDATA SMBCLK
CPUSB# WAKE# PESET# CLKREQ# CPPE#
REFCLK- REFCLK+
USB- USB+
PER0- PER0+
PET0- PET0+
NP1 NP2
GND

ICH_SMBDATA 20,26
ICH_SMBCLK 20,26
CPUSB#
PCIE_WAKE# C
CARD_RESET#
R793 0R2J-2-GP PCIE_WAKE# 26,32,38
CARD_CLK_REQ# 4
EXPRCRD_PWREN# 38
4 CLK_PCIE_EXPCARD#
4 CLK_PCIE_EXPCARD
USBP6D-
USBP6D+
19 PCIE_RX4-
19 PCIE_RX4+
19 PCIE_TX4-
19 PCIE_TX4+
EXPCARD_CABLE_DET# 38

DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

MiniCard WLAN connector

+3.3V_RUN RN37 SRN100KJ-6-GP
20 PCIE_MCARD1_DET#
20 USB_MCARD1_DET#
PCIE_MCARD1_DET#
USB_MCARD1_DET#

+1.5V_RUN C753 SCD047U10V2KX-2GP C763 SCD047U10V2KX-2GP

MINICARD3 SKT-MINI52P-8-GP 62.10043.391
1.5V 3.3V +1.5V +1.5V +3.3V +3.3VAUX
REFCLK+ REFCLK-
PERN0 PERP0
PETN0 PETP0
USB_D- USB_D+
SMB_CLK SMB_DATA
WAKE# CLKREQ# PERST#
GND
RESERVED#3 RESERVED#5 RESERVED#8 RESERVED#10 RESERVED#12 RESERVED#14 RESERVED#16 RESERVED#17 RESERVED#19 RESERVED#20 RESERVED#37 RESERVED#39 RESERVED#41 RESERVED#43 RESERVED#45 RESERVED#47 RESERVED#49 RESERVED#51
LED_WWAN# LED_WLAN# LED_WPAN#

CLK_PCIE_MINI1 CLK_PCIE_MINI1 4
CLK_PCIE_MINI1# CLK_PCIE_MINI1# 4
PCIE_RX2- PCIE_RX2- 19
PCIE_RX2+ PCIE_RX2+ 19
PCIE_TX2- PCIE_TX2- 19
PCIE_TX2+ PCIE_TX2+ 19
MINI1_USBPN TP33 Do Not Stuff
MINI1_USBPP TP36 Do Not Stuff
WLAN_SCLK
WLAN_SDATA
PCIE_WAKE#
MINI1CLK_REQ#
PLTRST# 8,20,26,32,37,38
SB_WLAN_PCIE_RST# 20
GND
USB_MCARD1_DET#

+3.3V_WLAN C331 SC4D7U6D3V3KX-GP C334 SCD1U10V2KX-4GP C751 SCD1U10V2KX-4GP C777 SCD047U10V2KX-2GP C755 SCD047U10V2KX-2GP
+3.3V_WLAN C752 SCD1U10V2KX-4GP
C752 Please Near the MINICARD1/Pin24

29,32 COEX2_WLAN_ACTIVE COEX2_WLAN_ACTIVE R743 0R2J-2-GP COEX2_WLAN_ACTIVE_1
29,32 COEX1_BT_ACTIVE COEX1_BT_ACTIVE R744 0R2J-2-GP COEX1_BT_ACTIVE_1

37 HOST_DEBUG_TX
37 HOST_DEBUG_RX
37 8051_TX
38 WLAN_RADIO_DIS#
WLAN_RADIO_DIS# R703 DY Do Not Stuff WLAN_RADIO_OFF#
PCIE_MCARD1_DET#
D47 CH751H-40PT-1GP
Prevent backdrive when WoW is enabled.

+5V_RUN R748 0R3-0-U-GP +5V_DBG_RUN
+3.3V_ALW R747 0R3-0-U-GP +3.3V_DBG_ALW
For Debug card used only.

37 8051_RX
41 LED_WLAN_OUT#
LED_WLAN_OUT#
29,32 BT_ACTIVE_K#
R733 DY Do Not Stuff BT_ACTIVE_WLAN#

+3.3V_WLAN RN20 SRN4K7J-8-GP
ICH_SMBCLK
ICH_SMBDATA
U42 2N7002DW-7F-GP
WLAN_SCLK
WLAN_SDATA

+12V_ALW
R164 100KR2J-1-GP
R155 100KR2J-1-GP
+3.3V_ALW
+3.3V_WLAN
U91 SI3456BDV-T1-GP
R157 200KR2J-L1-GP
C801 SC4700P50V2KX-1GP
U27 2N7002DW-7F-GP
37 AUX_EN_WOWL
R153 100KR2J-1-GP

SKT2 SKT-MINIPCI-4P-1GP 62.10043.401
NP1 NP2

SA5032

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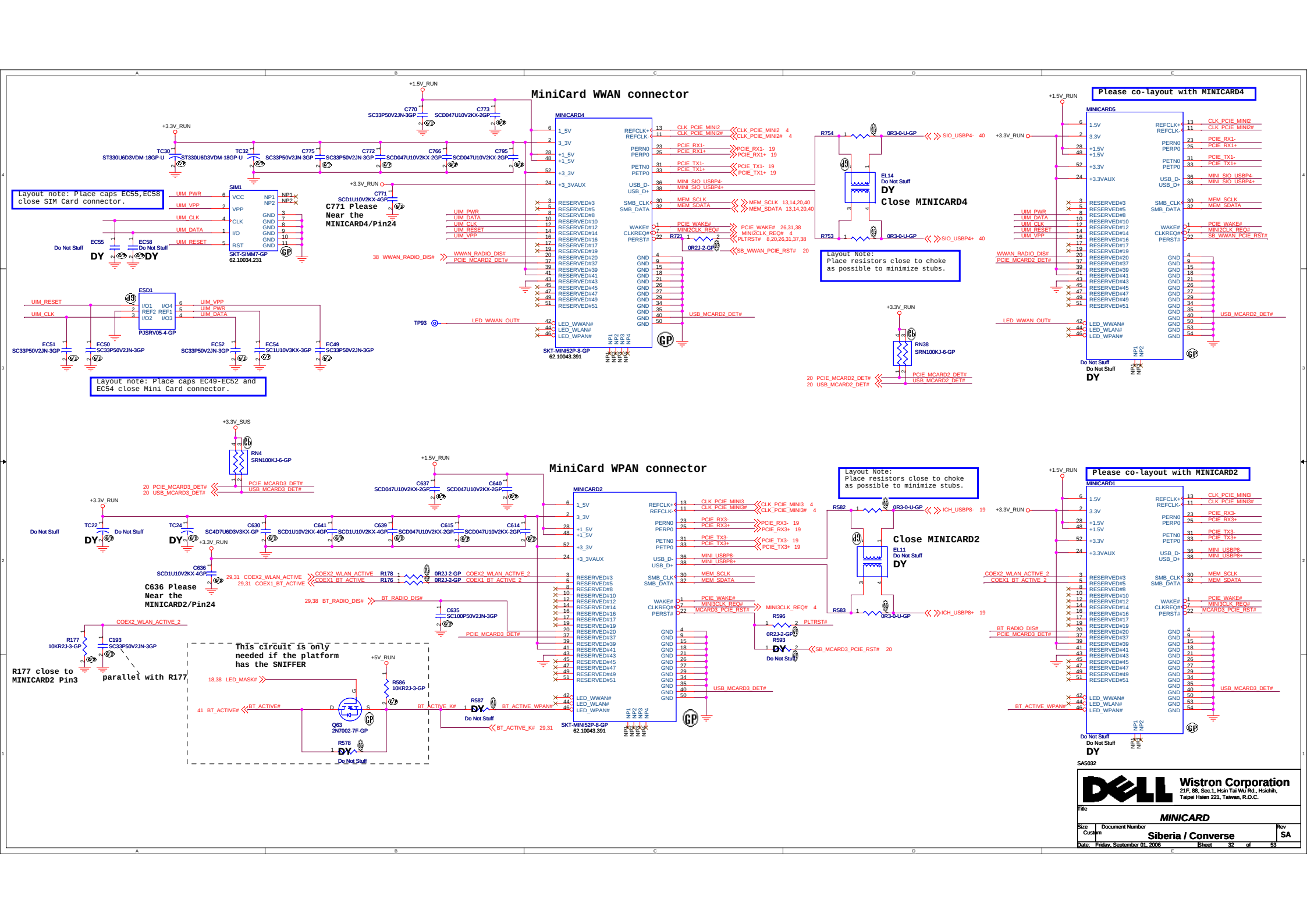
Title: EXPRESS CARD & MINICARD
Size: A3
Document Number: Siberia / Converse
Rev: SA
Date: Friday, September 01, 2006
Sheet 31 of 53


MiniCard WWAN connector
Please co-layout with MINICARD4
Layout note: Place caps EC55,EC58 close SIM Card connector.
C771 Please Near the MINICARD4/Pin24
Layout Note: Place resistors close to choke as possible to minimize stubs.
Close MINICARD4
Layout note: Place caps EC49-EC52 and EC54 close Mini Card connector.
MiniCard WPAN connector
Please co-layout with MINICARD2
C636 Please Near the MINICARD2/Pin24
R177 close to MINICARD2 Pin3
parallel with R177
This circuit is only needed if the platform has the SNIFFER
Close MINICARD2
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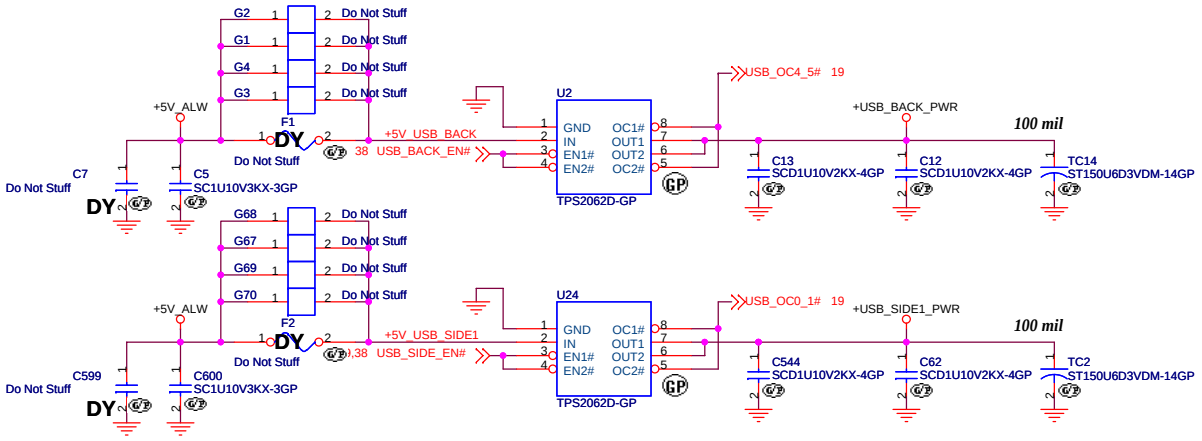
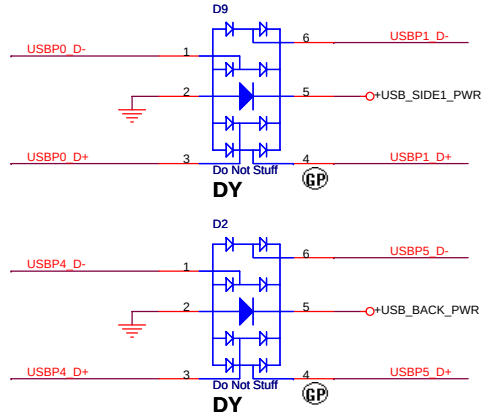
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
MINICARD
Siberia / Converse
SA
Friday, September 01, 2006
32
53

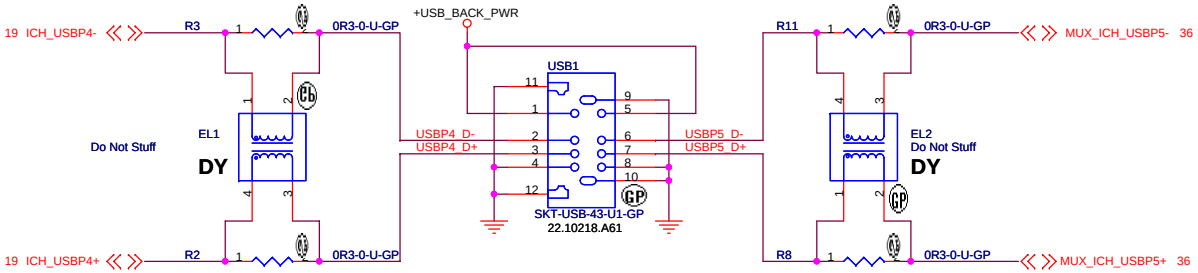
USB POWER



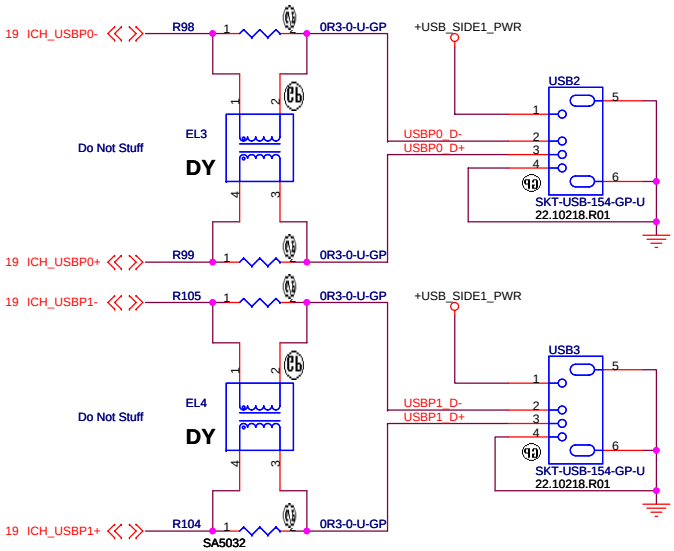


Place ESD diodes as close to the connector as passible.

USB PORT(BACK Port)



USB PORT(SIDE Port)



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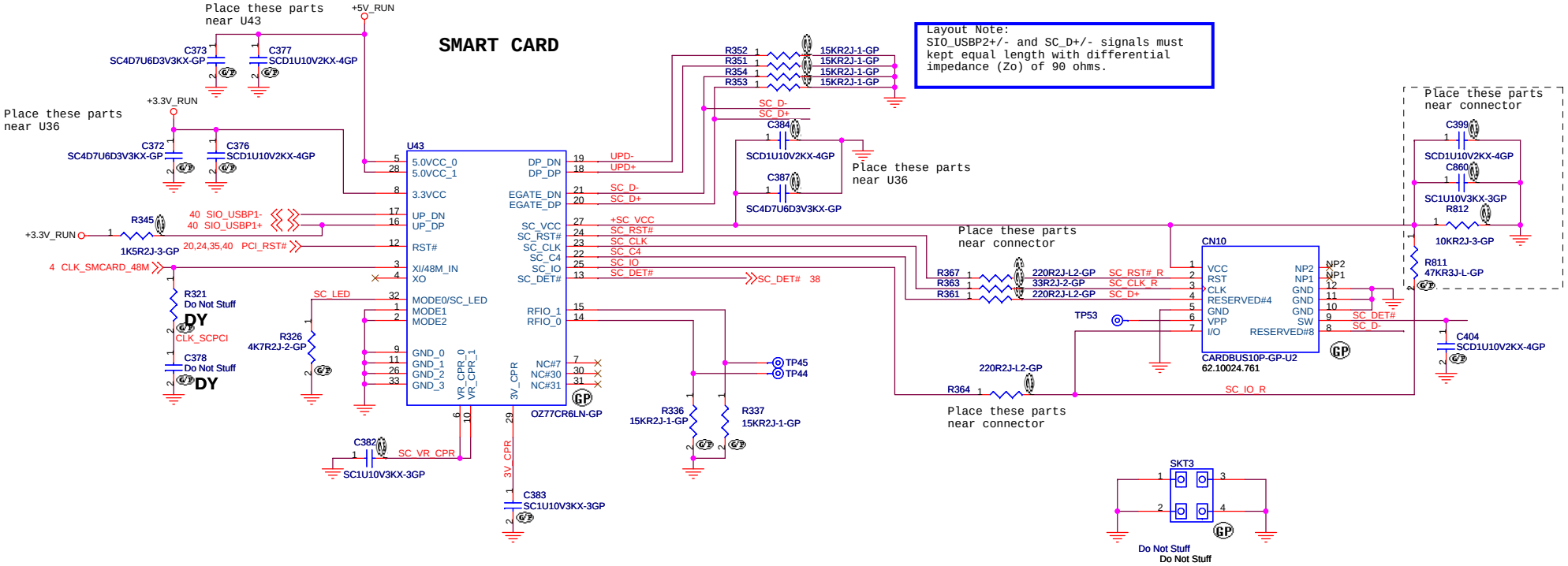
Title: *USB PORT*		
Size: A3	Document Number: Siberia / Converse	Rev: SA
Date: Friday, September 01, 2006	Sheet 33 of 53	



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Title: ***Smart Card***

Size	Document Number	Rev
A3	**Siberia / Converse**	SA

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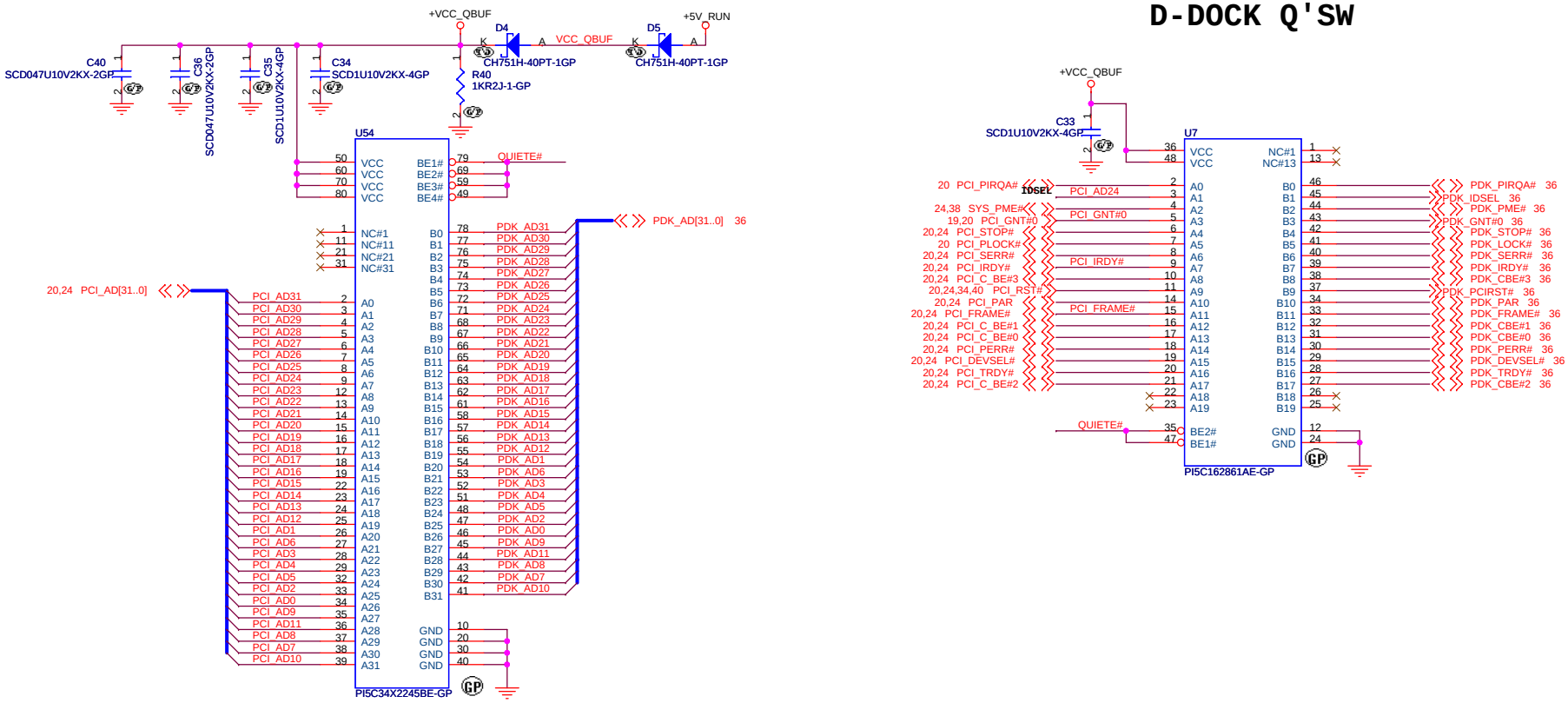
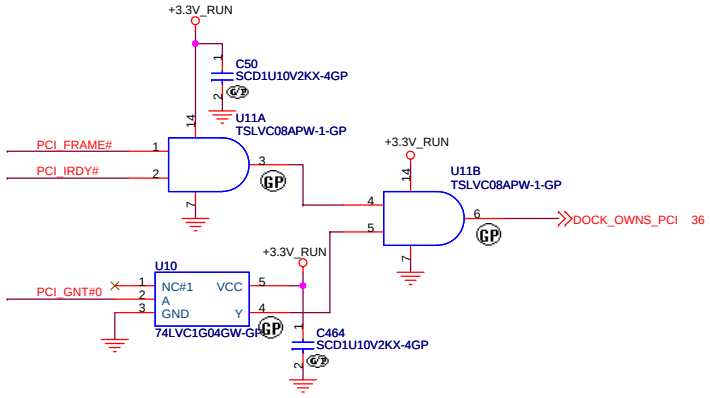
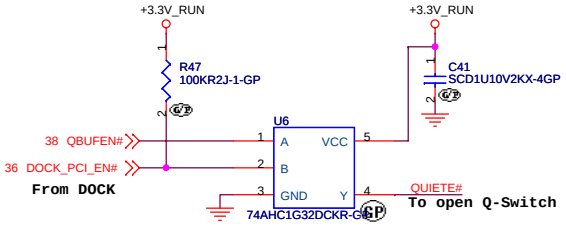
D-DOCK Q'SW







Dock on sequence

* BIOS requests through SMB to connect to PCI bus in the dock
* D-dock state machine generates REQ 0
* ICH8 generates GNT0
* Notbook waits for next Idle bus cycle (IORDY# and FRAME#)
* DOCK_QWNS_PCI is generated
* on rising edge of PCI clock REQ0 is deasserted and DOCK_PCI_EN# is asserted
* now Q-switch is enabled and PCI goes through to the dock
* D-dock reports connection through SMB
* re-enumeration is done by BIOS

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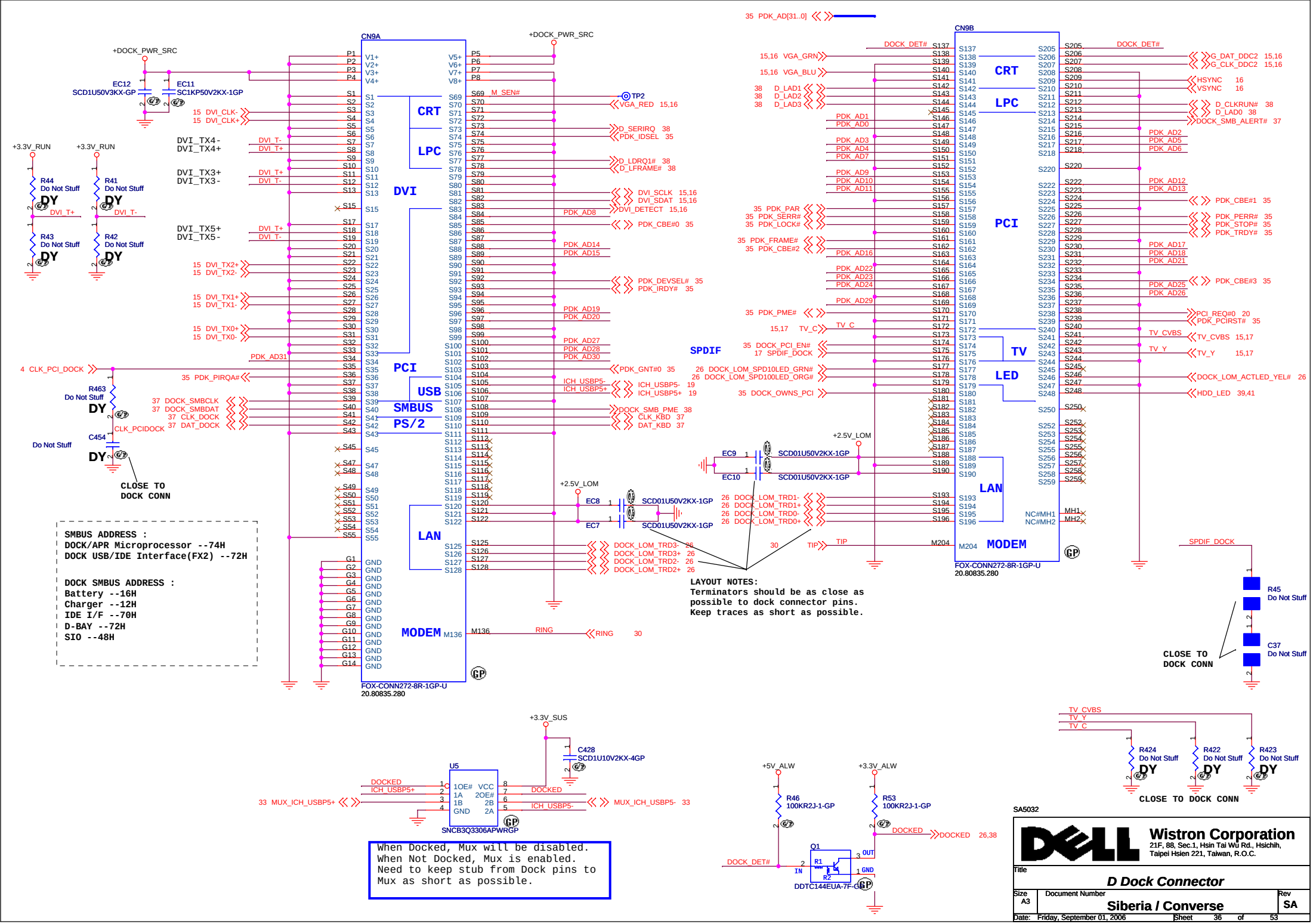
Title: D Dock Buffer

Size	Document Number	Rev
A3	Siberia / Converse	SA

Date: Friday, September 01, 2006 Sheet 35 of 53


CN9A
CN9B
CRT
LPC
DVI
PCI
USB
SMBUS
PS/2
LAN
MODEM
SPDIF
TV
LED
+DOCK_PWR_SRC
+3.3V_RUN
+2.5V_LOM
+3.3V_SUS
+5V_ALW
+3.3V_ALW
FOX-CONN272-8R-1GP-U
20.80835.280
CLOSE TO DOCK CONN
SMBUS ADDRESS :
DOCK/APR Microprocessor --74H
DOCK USB/IDE Interface(FX2) --72H
DOCK SMBUS ADDRESS :
Battery --16H
Charger --12H
IDE I/F --70H
D-BAY --72H
SIO --48H
LAYOUT NOTES:
Terminators should be as close as possible to dock connector pins.
Keep traces as short as possible.
When Docked, Mux will be disabled.
When Not Docked, Mux is enabled.
Need to keep stub from Dock pins to Mux as short as possible.
SNCB3Q3306APWRGP
DDTC144EUA-7F-G
SA5032
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
D Dock Connector
Siberia / Converse
Size A3
Rev SA
Date: Friday, September 01, 2006
Sheet 36 of 53

Place these caps close to MEC5025.

Place cap close to pin 121.

Note: MEC5025 KSO3/GPIOC3 pin 29 was 3V_5V_SUS_PWRGD, M08 platforms already had 3V_5V_SUS_PWRGD from the discrete component.

Flash Recovery.
1=Enabled
0=Disabled

Low=
Write Protected.

Flash Write Protect bottom 4K of internal bootblock flash.

Not Stuff R839 0 ohm when doing Flash recovery.

Debug Serial Port Flash Recovery port.

SA5032

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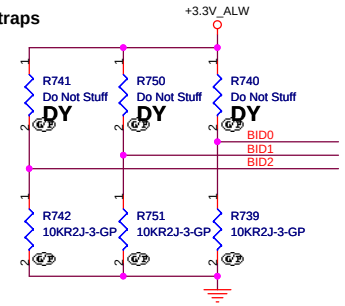
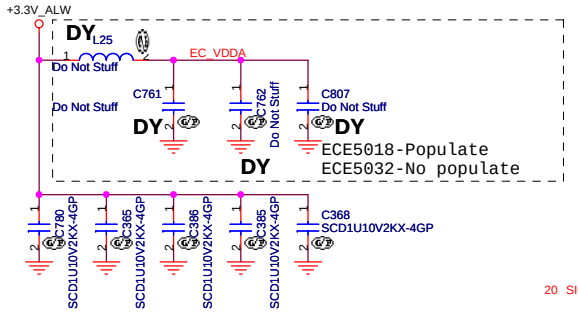
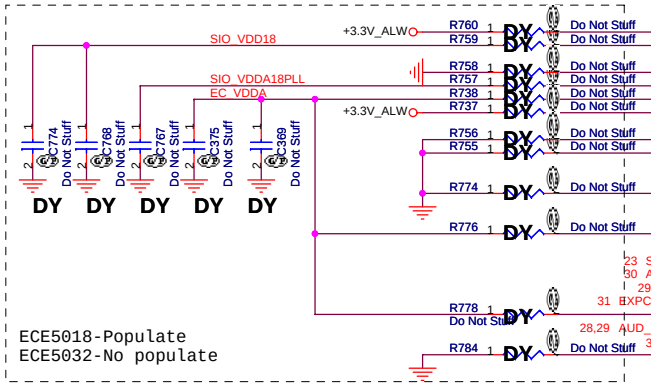
Title: KBC MEC5025		
Size: A3	Document Number: Siberia / Converse	Rev: SA
Date: Friday, September 01, 2006	Sheet 37 of 53	

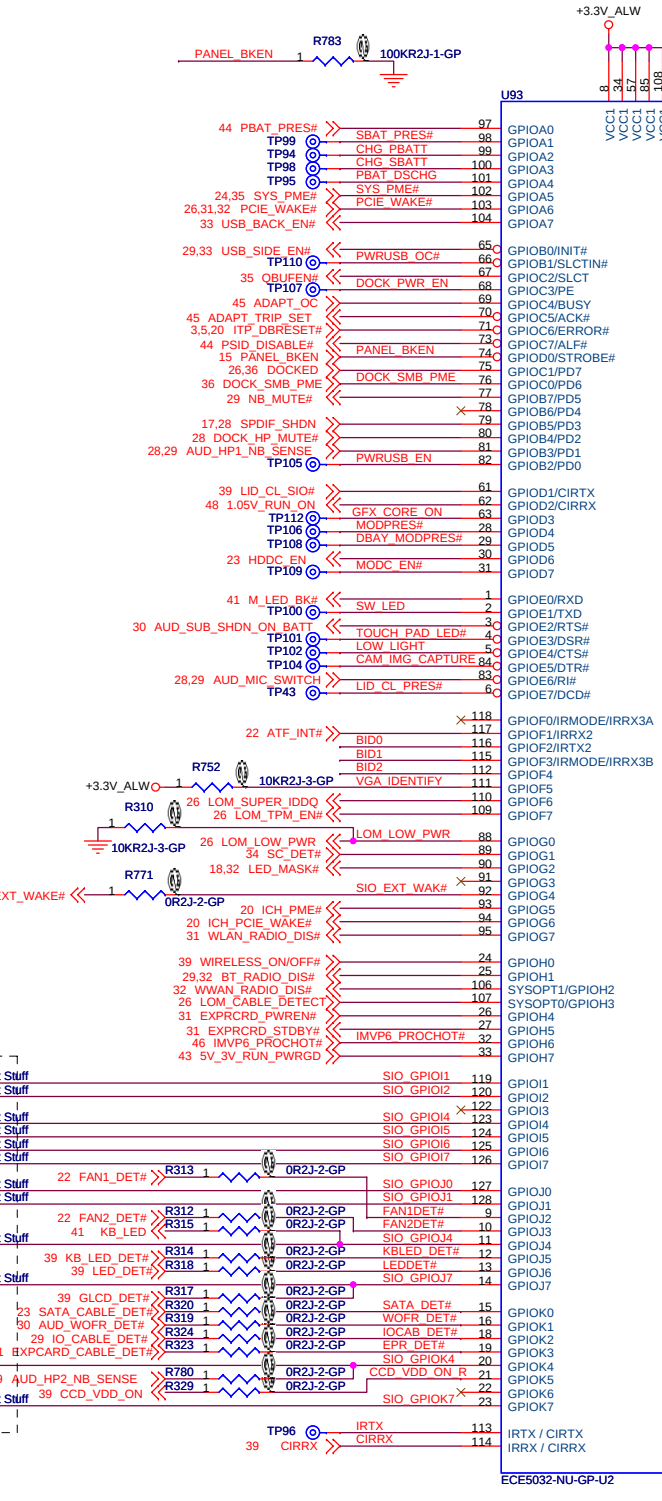
Board ID Straps

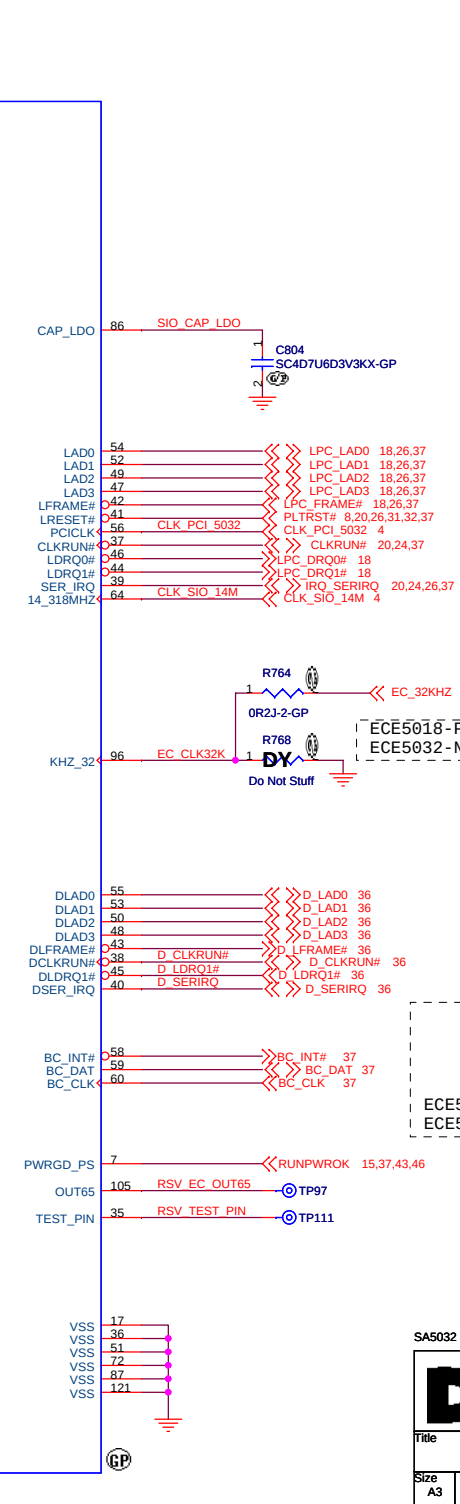


BID2	BID1	BID0	Board Rev.
0	0	0	ENG1(M00)
0	0	1	ENG2(X00)
0	1	0	ENG3(X01)
0	1	1	ENG4(X02)
1	0	0	QT (X03)
1	0	1	RAMP(A00)
1	1	0	









SA5032

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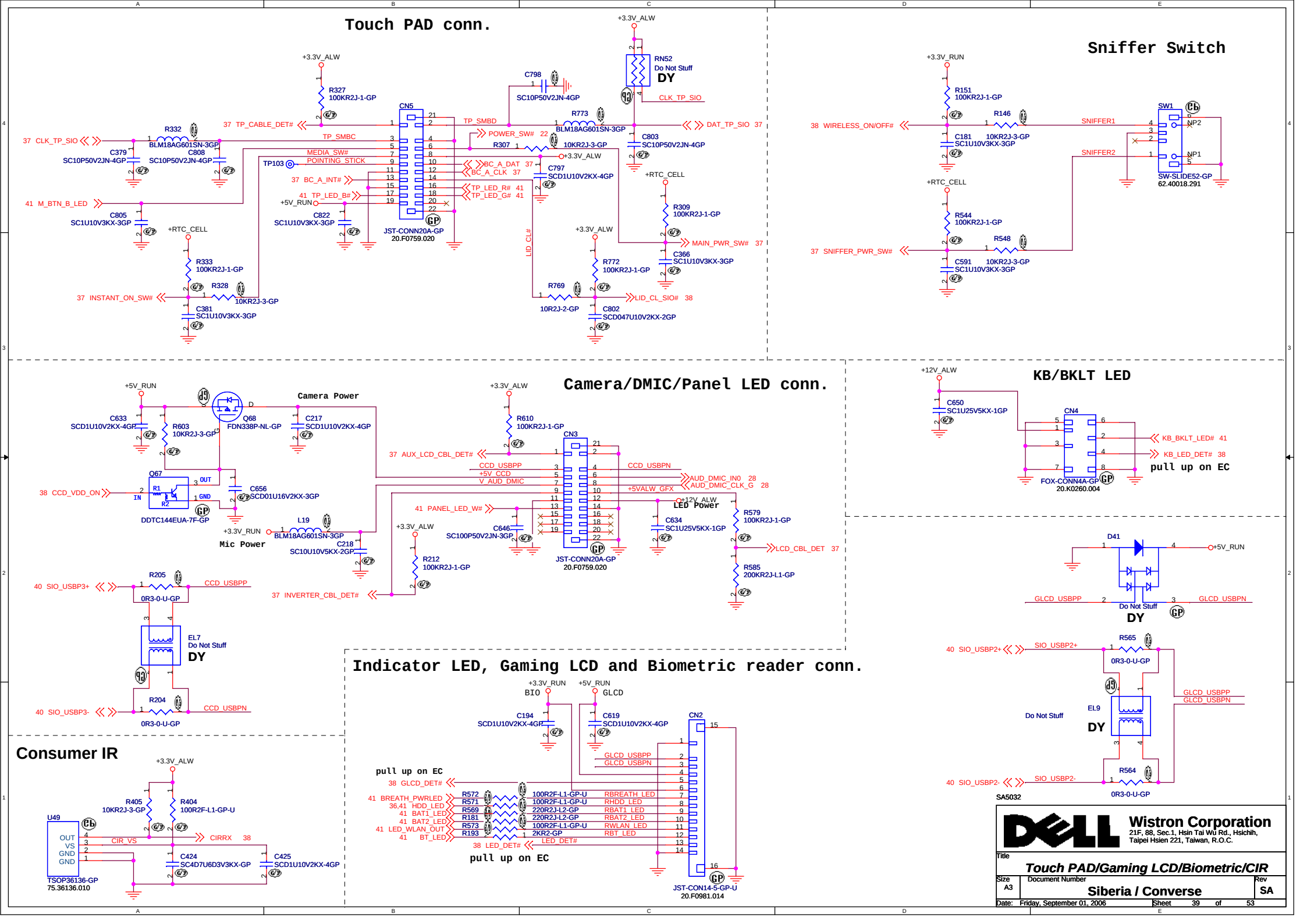
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SIO ECE5032***

Size	Document Number	Rev
A3	Siberia / Converse	SA

Date: Friday, September 01, 2006 Sheet 38 of 53


Touch PAD conn.
Sniffer Switch
Camera/DMIC/Panel LED conn.
KB/BKLT LED
Indicator LED, Gaming LCD and Biometric reader conn.
Consumer IR
Camera Power
Mic Power
LED Power
pull up on EC
DY
Do Not Stuff
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Touch PAD/Gaming LCD/Biometric/CIR
Size A3
Document Number
Siberia / Converse
Rev SA
Date: Friday, September 01, 2006
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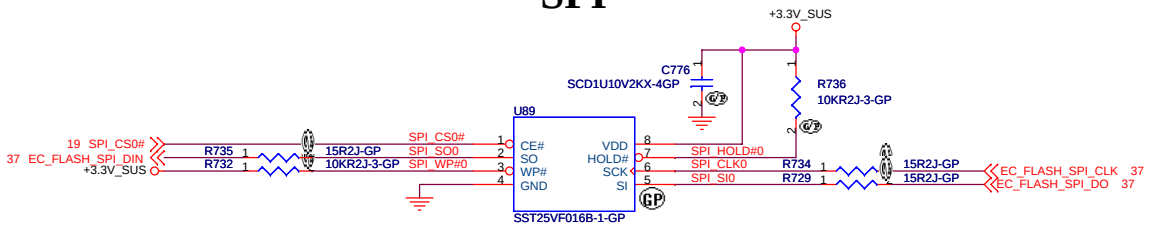
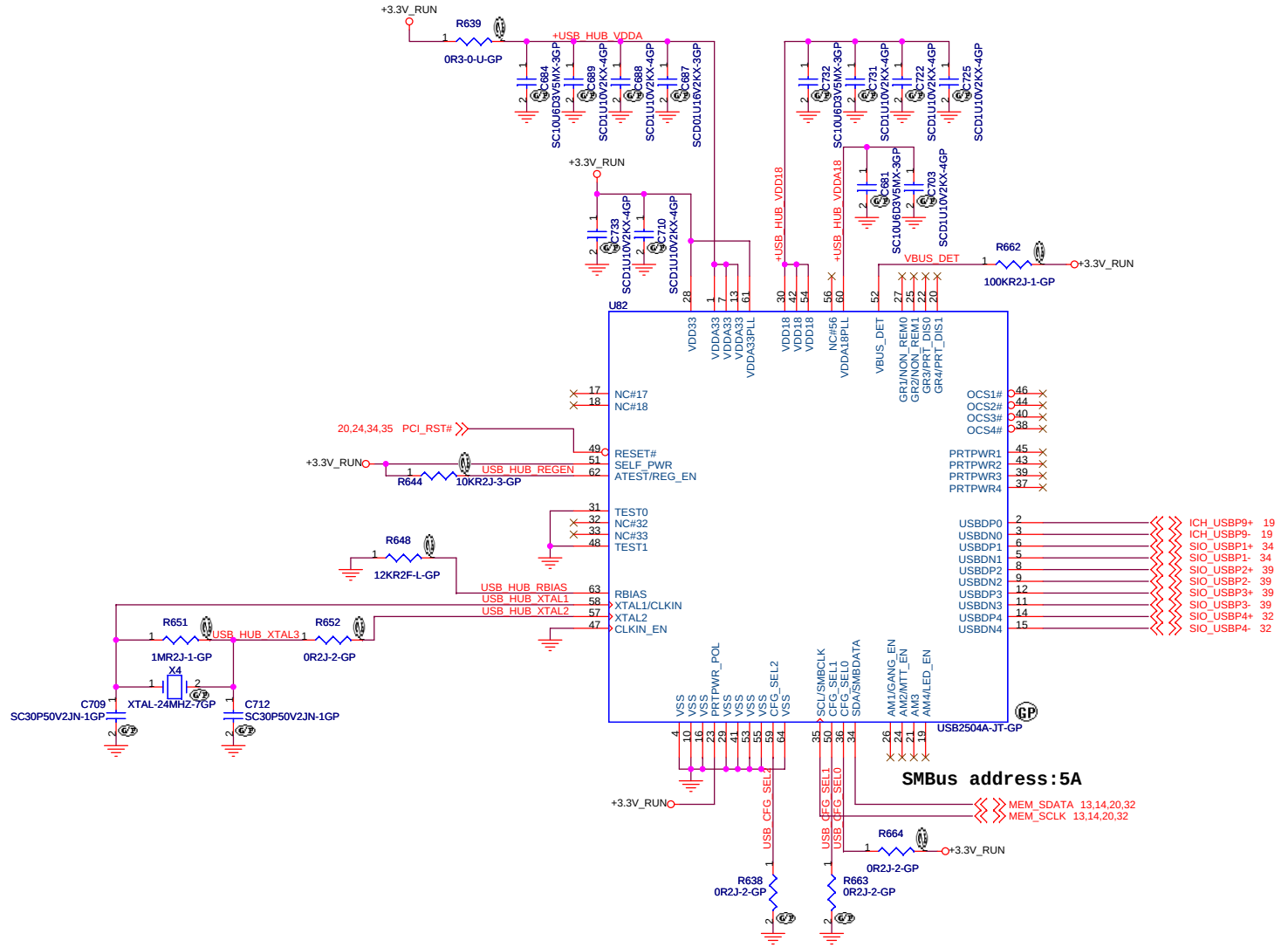
SPI





SA5032

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SPI FLASH/USB HUB***

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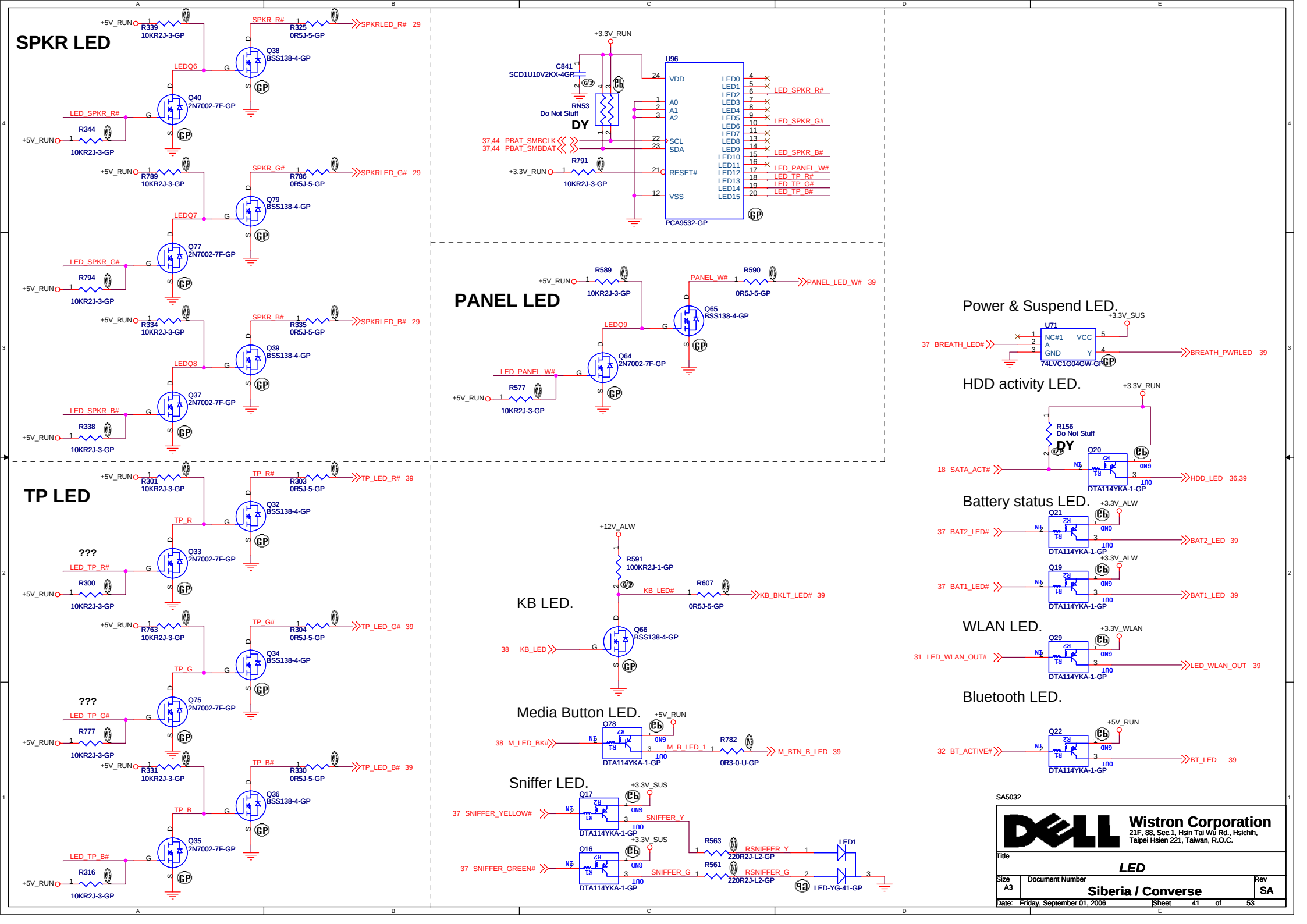
SPKR LED
+5V_RUN
R339
10KR2J-3-GP
SPKR_R#
R325
0R5J-5-GP
SPKRLED_R# 29
Q38
BSS138-4-GP
LEDQ6
Q40
2N7002-7F-GP
LED_SPKR_R#
R344
10KR2J-3-GP
R789
10KR2J-3-GP
SPKR_G#
R786
0R5J-5-GP
SPKRLED_G# 29
Q79
BSS138-4-GP
LEDQ7
Q77
2N7002-7F-GP
LED_SPKR_G#
R794
10KR2J-3-GP
R334
10KR2J-3-GP
SPKR_B#
R335
0R5J-5-GP
SPKRLED_B# 29
Q39
BSS138-4-GP
LEDQ8
Q37
2N7002-7F-GP
LED_SPKR_B#
R338
10KR2J-3-GP
+3.3V_RUN
C841
SCD1U10V2KX-4GP
U96
VDD
A0
A1
A2
SCL
SDA
RESET#
VSS
LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
LED9
LED10
LED11
LED12
LED13
LED14
LED15
LED_SPKR_R#
LED_SPKR_G#
LED_SPKR_B#
LED_PANEL_W#
LED_TP_R#
LED_TP_G#
LED_TP_B#
RN53
Do Not Stuff
DY
37,44 PBAT_SMBCLK
37,44 PBAT_SMBDAT
R791
10KR2J-3-GP
PCA9532-GP
PANEL LED
R589
10KR2J-3-GP
PANEL_W#
R590
0R5J-5-GP
PANEL_LED_W# 39
Q65
BSS138-4-GP
LEDQ9
Q64
2N7002-7F-GP
LED_PANEL_W#
R577
10KR2J-3-GP
Power & Suspend LED.
U71
NC#1
A
GND
VCC
Y
74LVC1G04GW-GP
+3.3V_SUS
37 BREATH_LED#
BREATH_PWRLED 39
HDD activity LED.
R156
Do Not Stuff
DY
Q20
DTA114YKA-1-GP
18 SATA_ACT#
HDD_LED 36,39
Battery status LED.
+3.3V_ALW
Q21
37 BAT2_LED#
BAT2_LED 39
Q19
37 BAT1_LED#
BAT1_LED 39
WLAN LED.
Q29
+3.3V_WLAN
31 LED_WLAN_OUT#
LED_WLAN_OUT 39
Bluetooth LED.
Q22
32 BT_ACTIVE#
BT_LED 39
TP LED
TP_R#
R301
10KR2J-3-GP
R303
0R5J-5-GP
TP_LED_R# 39
Q32
BSS138-4-GP
TP_R
Q33
2N7002-7F-GP
LED_TP_R#
R300
10KR2J-3-GP
???
TP_G#
R763
10KR2J-3-GP
R304
0R5J-5-GP
TP_LED_G# 39
Q34
BSS138-4-GP
TP_G
Q75
2N7002-7F-GP
LED_TP_G#
R777
10KR2J-3-GP
???
TP_B#
R331
10KR2J-3-GP
R330
0R5J-5-GP
TP_LED_B# 39
Q36
BSS138-4-GP
TP_B
Q35
2N7002-7F-GP
LED_TP_B#
R316
10KR2J-3-GP
KB LED.
+12V_ALW
R591
100KR2J-1-GP
KB_LED#
R607
0R5J-5-GP
KB_BKLT_LED# 39
Q66
BSS138-4-GP
38 KB_LED
Media Button LED.
Q78
DTA114YKA-1-GP
38 M_LED_BK#
M_B_LED_1
R782
0R3-0-U-GP
M_BTN_B_LED 39
Sniffer LED.
Q17
37 SNIFFER_YELLOW#
SNIFFER_Y
Q16
37 SNIFFER_GREEN#
SNIFFER_G
R563
220R2J-L2-GP
RSNIFFER_Y
R561
220R2J-L2-GP
RSNIFFER_G
LED1
LED-YG-41-GP
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LED
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A3
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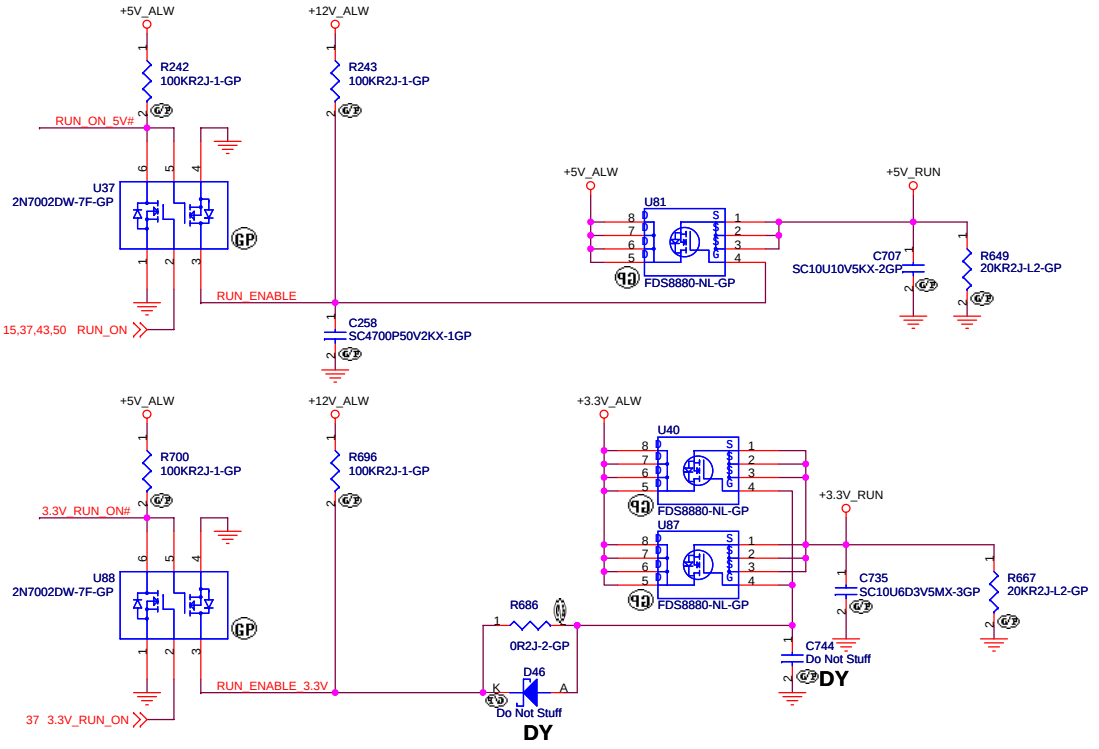

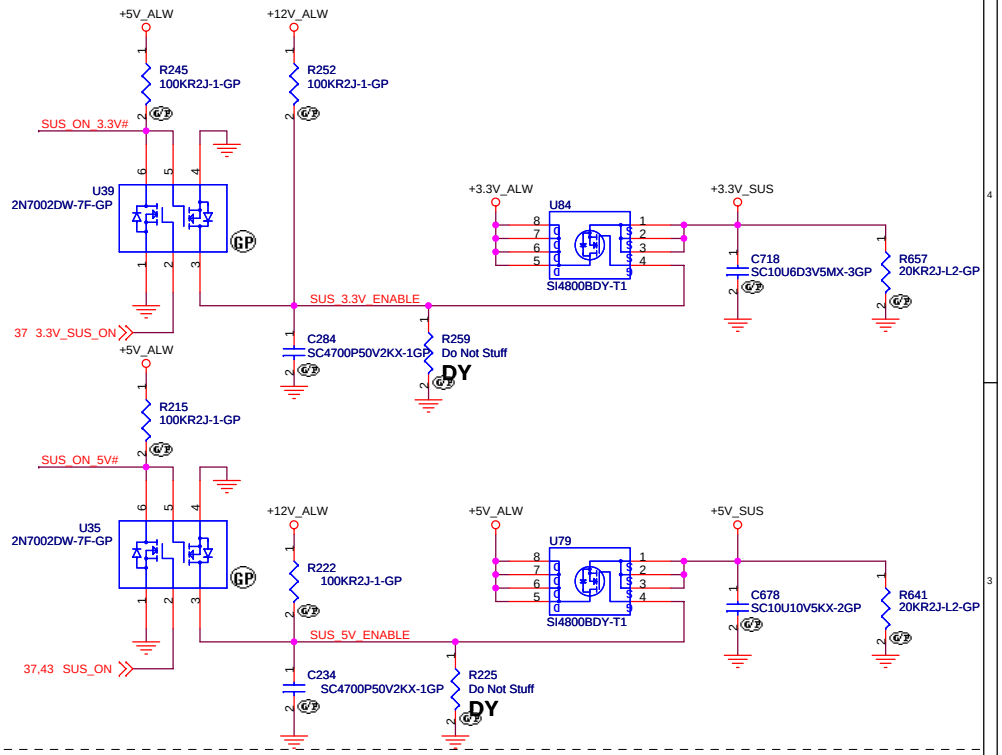

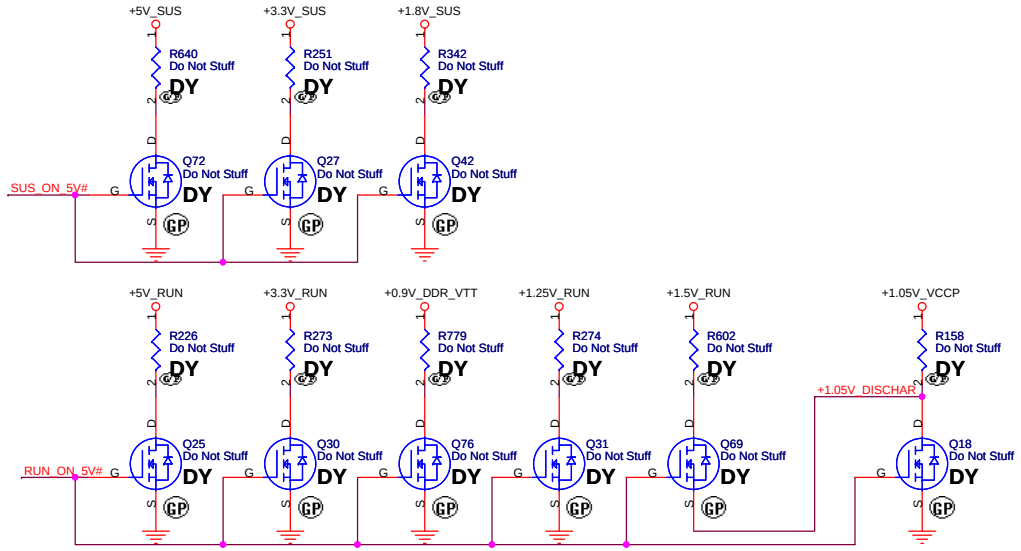

Reserve discharge path

CRB 0.95:
Insures that +1.05_VCCP and +1.5_RUN ramp down together by discharing +1.5V_RUN into +1.05V_VCCP

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Plane Enable***

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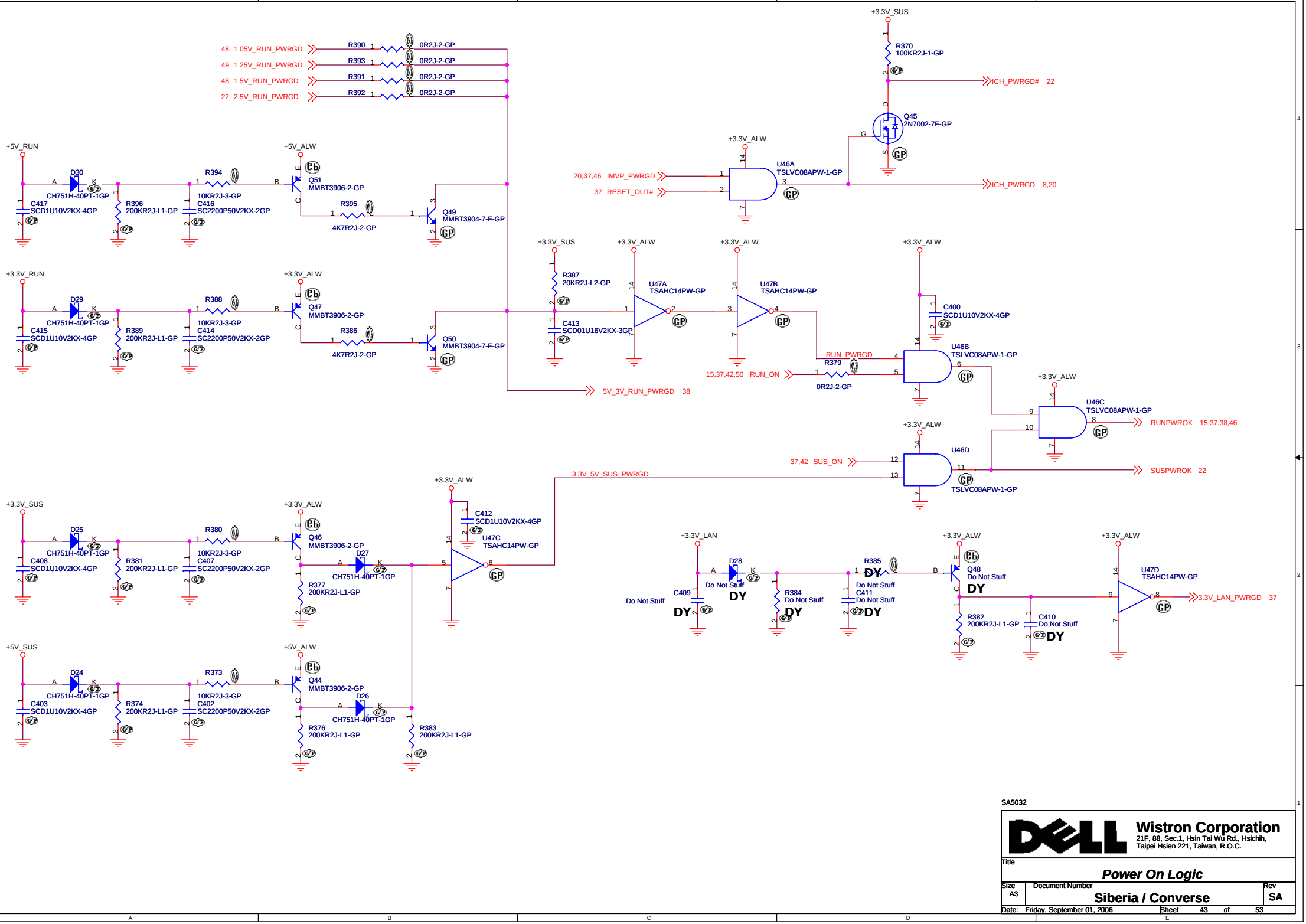

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power On Logic***

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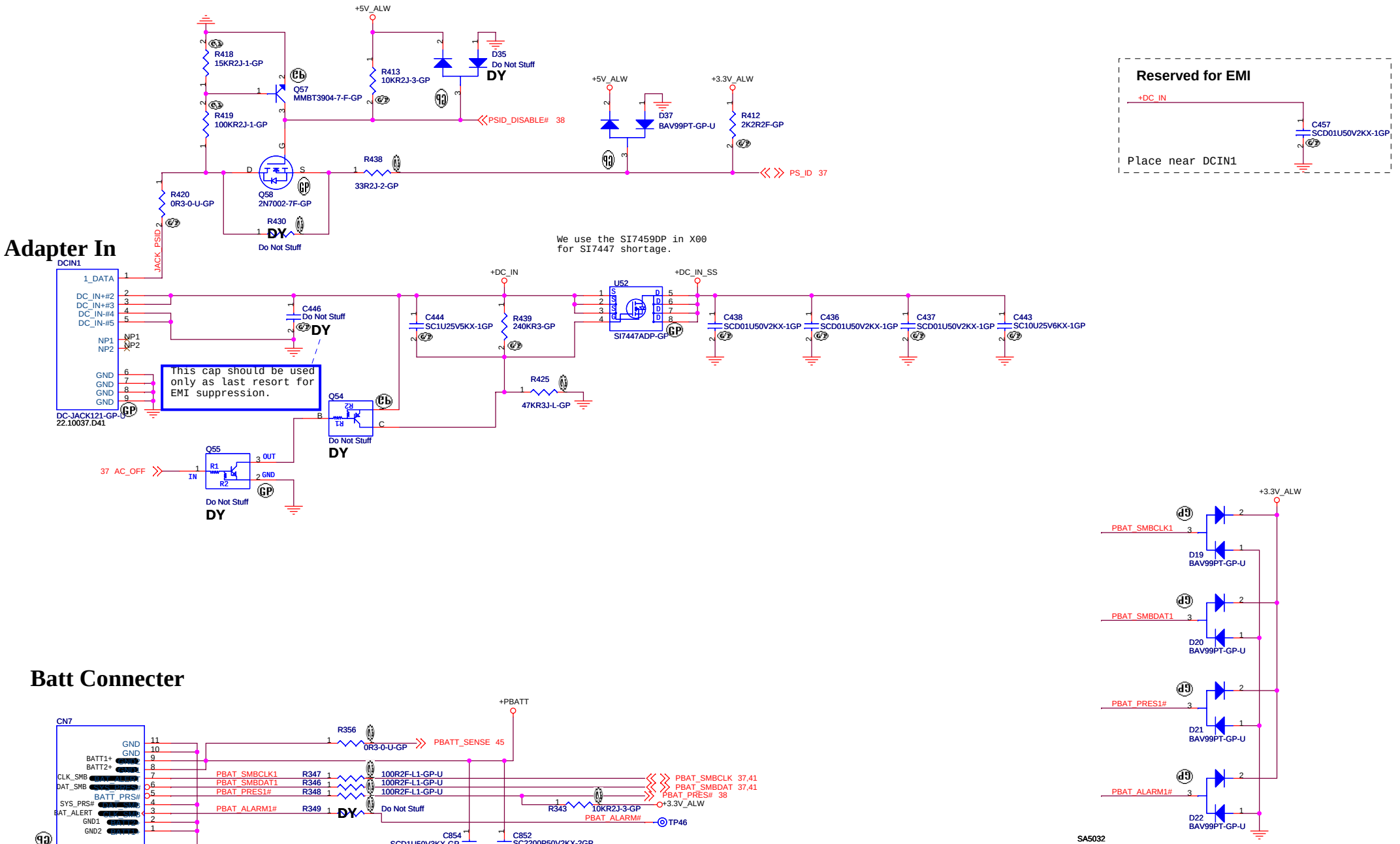

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN / BATT CONN.

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PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

"NC" means no-connect

We use the SI7459DP in X00 for SI7447 shortage.

We use the SI7459DP in X00 for SI7447 shortage.

This Resistor must be 1% tolerance.

TABLE

MAXIM & INTERSIL BOM DIFFERENCES

REF DES	MAXIM	INTERSIL
R831	8.45K 1%	16K 1%
C422	0.01uF	DUMMY
C873	0.1uF 10V	DUMMY
C882	1uF 10V	DUMMY
R836	365K 1%	215K 1%
R823	0 5%	10 5%
R833	0 5%	10 5%
C865	DUMMY	0.22uF
C877	DUMMY	0.22uF
C879	0.01uF	DUMMY
C875	0.1uF 10V	DUMMY
C872	220pF 50V	DUMMY
D48	1SS400	DUMMY
C866	3.3nF	DUMMY
R828	1 1%	0 5%
R824	100 5%	0 5%
R834	4.7K 5%	4.7K 5%
C880	0.01uF	0.01uF
C878	0.01uF	0.01uF

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Title: Charger

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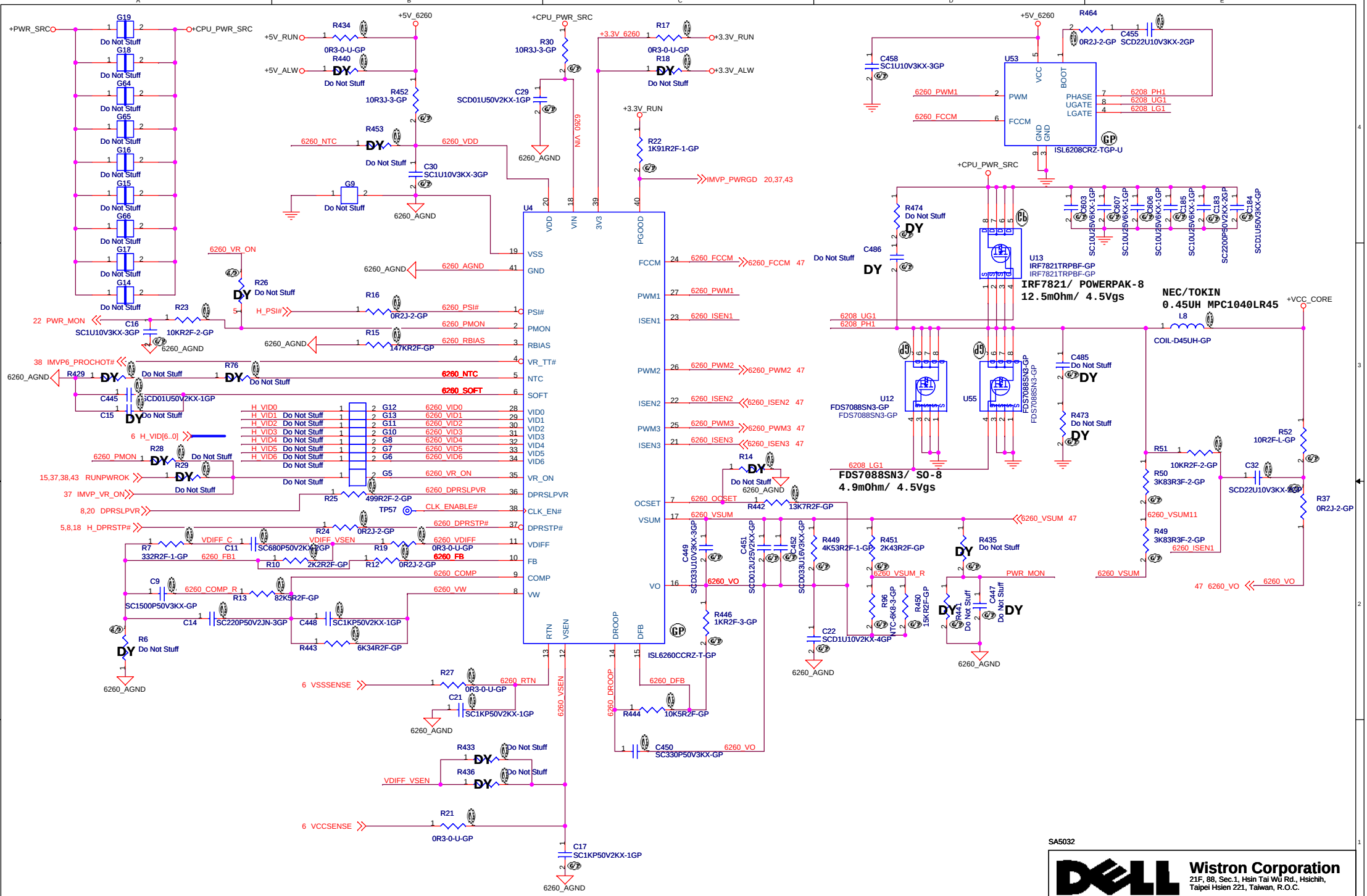
+PWR_SRC
+CPU_PWR_SRC
G19
G18
G64
G65
G16
G15
G66
G17
G14
Do Not Stuff
+5V_RUN
+5V_ALW
+5V_6260
R434
R440
R452
10R3J-3-GP
0R3-0-U-GP
R453
C30
SC1U10V3KX-3GP
G9
6260_AGND
6260_NTC
6260_VDD
+CPU_PWR_SRC
R30
C29
SCD01U50V2KX-1GP
+3.3V_6260
+3.3V_RUN
+3.3V_ALW
R17
R18
R22
1K91R2F-1-GP
IMVP_PWRGD 20,37,43
U4
VDD
VIN
3V3
PGOOD
VSS
GND
PSI#
PMON
RBIAS
VR_TT#
NTC
SOFT
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VR_ON
DPRSLPVR
CLK_EN#
DPRSTP#
VDIFF
FB
COMP
VW
RTN
VSEN
DROOP
DFB
FCCM
PWM1
ISEN1
PWM2
ISEN2
PWM3
ISEN3
OCSET
VSUM
VO
ISL6260CCRZ-T-GP
6260_VR_ON
R26
H_PSI#
R16
0R2J-2-GP
6260_PSI#
6260_PMON
6260_RBIAS
R15
147KR2F-GP
22 PWR_MON
R23
C16
10KR2F-2-GP
38 IMVP6_PROCHOT#
R429
R76
6260_NTC
6260_SOFT
C445
C15
SCD01U50V2KX-1GP
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
G12
G13
G11
G10
G8
G7
G6
G5
6260_VID0
6260_VID1
6260_VID2
6260_VID3
6260_VID4
6260_VID5
6260_VID6
6260_VR_ON
6 H_VID[6..0]
6260_PMON
R28
R29
15,37,38,43 RUNPWROK
37 IMVP_VR_ON
8,20 DPRSLPVR
R25
499R2F-2-GP
6260_DPRSLPVR
TP57
CLK_ENABLE#
5,8,18 H_DPRSTP#
R24
0R2J-2-GP
6260_DPRSTP#
VDIFF_C
R7
332R2F-1-GP
C11
SC680P50V2KX-2GP
VDIFF_VSEN
R19
0R3-0-U-GP
6260_VDIFF
6260_FB1
R10
2K2R2F-GP
R12
0R2J-2-GP
6260_FB
6260_COMP
C9
SC1500P50V3KX-GP
6260_COMP_R
R13
82K5R2F-GP
6260_VW
C14
SC220P50V2JN-3GP
C448
SC1KP50V2KX-1GP
R443
6K34R2F-GP
R6
6260_AGND
6 VSSSENSE
R27
0R3-0-U-GP
6260_RTN
C21
SC1KP50V2KX-1GP
R433
R436
VDIFF_VSEN
6 VCCSENSE
R21
0R3-0-U-GP
C17
SC1KP50V2KX-1GP
R14
R442
13K7R2F-GP
6260_OCSET
6260_VSUM
6260_VO
C449
SCD33U10V3KX-3GP
C451
SCD012U25V2KX-GP
C452
SCD033U16V3KX-GP
R449
4K53R2F-1-GP
R451
2K43R2F-GP
6260_VSUM_R
R96
6K8-3-GP
NTC-6K8-3-GP
R450
15K2F-GP
C22
SCD1U10V2KX-4GP
R435
PWR_MON
R445
C447
R446
1K2R2F-3-GP
R444
10K5R2F-GP
6260_DFB
C450
SC330P50V3KX-GP
6260_VSUM 47
6260_FCCM 47
6260_PWM1
6260_PWM2 47
6260_ISEN1
6260_ISEN2 47
6260_PWM3 47
6260_ISEN3 47
R464
0R2J-2-GP
C455
SCD22U10V3KX-2GP
C458
SC1U10V3KX-3GP
U53
VCC
BOOT
PWM
PHASE
UGATE
LGATE
FCCM
GND
6260_PWM1
6260_FCCM
6208_PH1
6208_UG1
6208_LG1
ISL6208CRZ-TGP-U
R474
Do Not Stuff
C486
C603
C607
C606
C185
C183
C184
SC10U25V6KX-1GP
SC2200P50V2KX-2GP
SCD1U50V3KX-GP
U13
IRF7821TRPBF-GP
IRF7821/ POWERPAK-8
12.5mOhm/ 4.5Vgs
NEC/TOKIN
0.45UH MPC1040LR45
+VCC_CORE
L8
COIL-D45UH-GP
6208_UG1
6208_PH1
6208_LG1
U12
U55
FDS7088SN3-GP
FDS7088SN3/ SO-8
4.9mOhm/ 4.5Vgs
C485
R473
R51
10KR2F-GP
R50
3K83R3F-2-GP
R52
10R2F-L-GP
C32
SCD22U10V3KX-2GP
R37
0R2J-2-GP
R49
3K83R3F-2-GP
6260_VSUM11
6260_ISEN1
47 6260_VO
SA5032
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU Vcore Power_1
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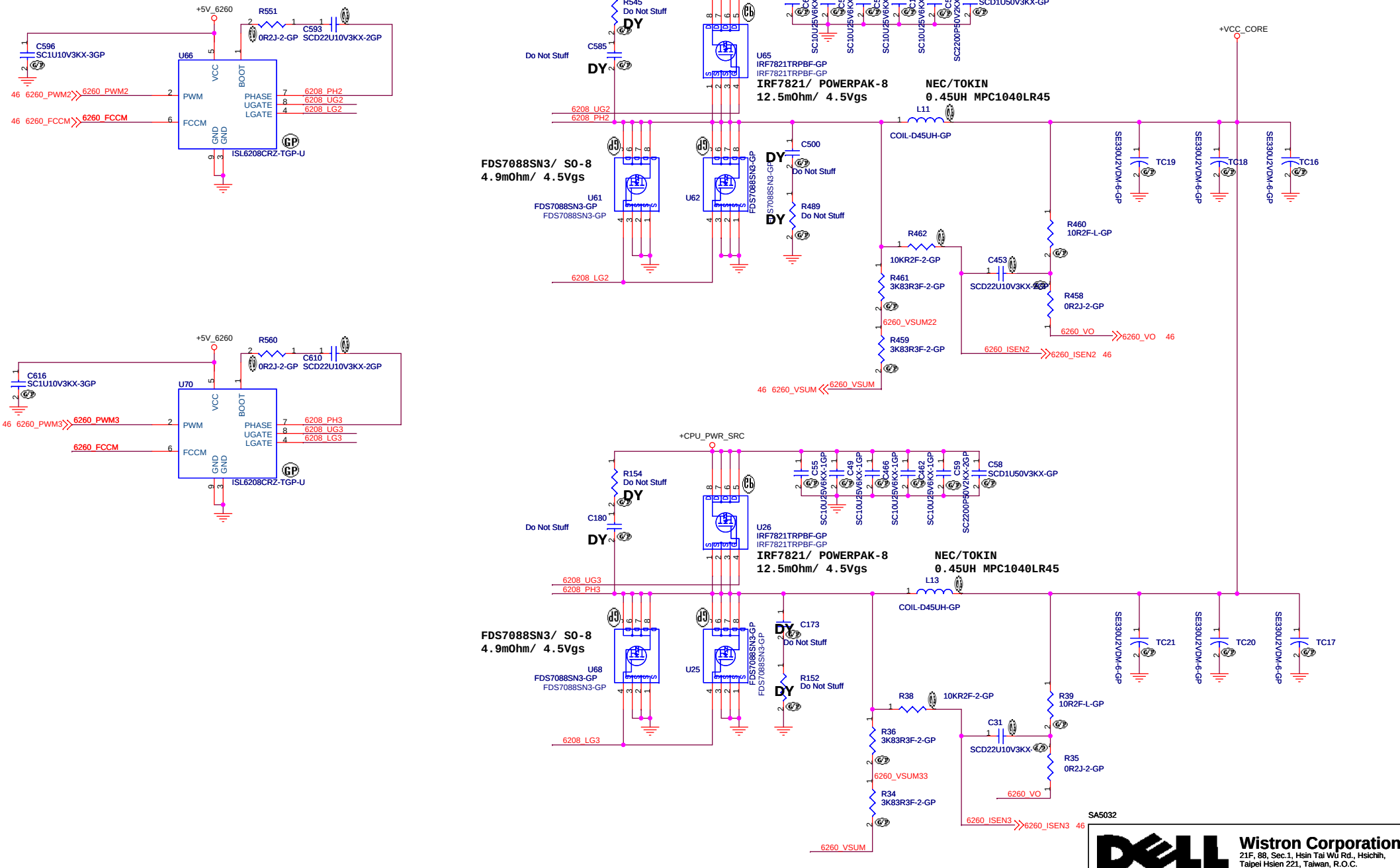
+5V_6260
R551
0R2J-2-GP
C593
SCD22U10V3KX-2GP
C596
SC1U10V3KX-3GP
U66
VCC
BOOT
PWM
FCCM
GND
GND
PHASE
UGATE
LGATE
46 6260_PWM2
6260_PWM2
46 6260_FCCM
6260_FCCM
6208_PH2
6208_UG2
6208_LG2
ISL6208CRZ-TGP-U
+CPU_PWR_SRC
R545
Do Not Stuff
DY
C585
U65
IRF7821TRPBF-GP
IRF7821TRPBF-GP
IRF7821/ POWERPAK-8
12.5mOhm/ 4.5Vgs
NEC/TOKIN
0.45UH MPC1040LR45
C608
C588
C594
C186
C554
SC10U25V6KX-1GP
SC2200P50V2KX-2GP
C552
SCD1U50V3KX-GP
6208_UG2
6208_PH2
L11
COIL-D45UH-GP
+VCC_CORE
FDS7088SN3/ SO-8
4.9mOhm/ 4.5Vgs
U61
FDS7088SN3-GP
U62
C500
R489
6208_LG2
SE330U2VDM-6-GP
TC19
TC18
TC16
R462
10KR2F-2-GP
R461
3K83R3F-2-GP
C453
SCD22U10V3KX-GP
R460
10R2F-L-GP
R458
0R2J-2-GP
6260_VSUM22
R459
3K83R3F-2-GP
6260_VO
6260_VO 46
6260_ISEN2
6260_ISEN2 46
46 6260_VSUM
6260_VSUM
+5V_6260
R560
0R2J-2-GP
C610
SCD22U10V3KX-2GP
C616
SC1U10V3KX-3GP
U70
46 6260_PWM3
6260_PWM3
6260_FCCM
6208_PH3
6208_UG3
6208_LG3
ISL6208CRZ-TGP-U
+CPU_PWR_SRC
R154
Do Not Stuff
DY
C180
U26
IRF7821TRPBF-GP
IRF7821TRPBF-GP
IRF7821/ POWERPAK-8
12.5mOhm/ 4.5Vgs
NEC/TOKIN
0.45UH MPC1040LR45
C55
C49
C466
C462
C59
SC10U25V6KX-1GP
SC2200P50V2KX-2GP
C58
SCD1U50V3KX-GP
6208_UG3
6208_PH3
L13
COIL-D45UH-GP
FDS7088SN3/ SO-8
4.9mOhm/ 4.5Vgs
U68
FDS7088SN3-GP
U25
C173
R152
6208_LG3
SE330U2VDM-6-GP
TC21
TC20
TC17
R38
10KR2F-2-GP
R36
3K83R3F-2-GP
C31
SCD22U10V3KX-GP
R39
10R2F-L-GP
R35
0R2J-2-GP
6260_VSUM33
R34
3K83R3F-2-GP
6260_VO
6260_ISEN3
6260_ISEN3 46
6260_VSUM
SA5032
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU Vcore Power_2
Size
A3
Document Number
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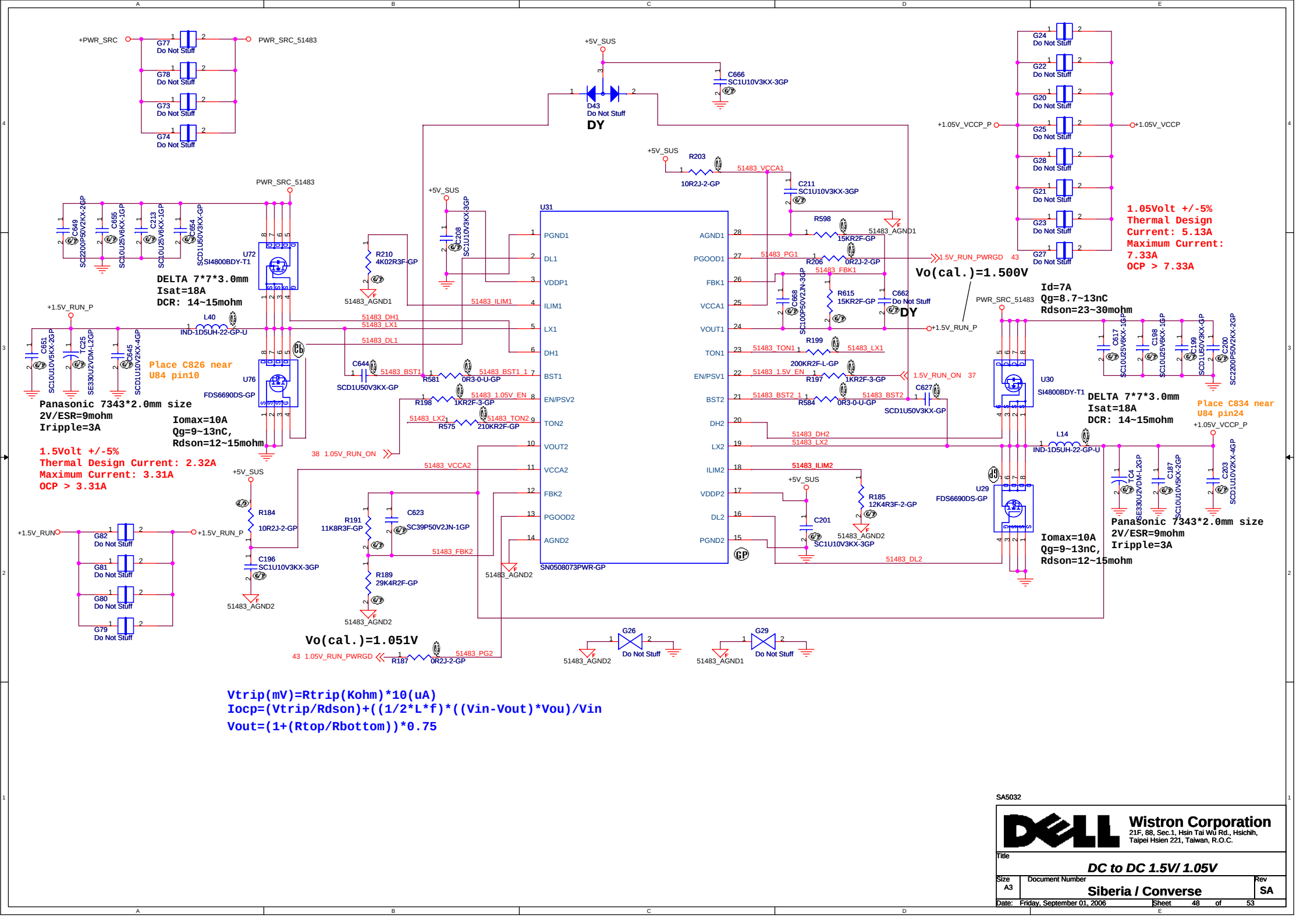

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.5V/ 1.05V

Size	Document Number	Rev
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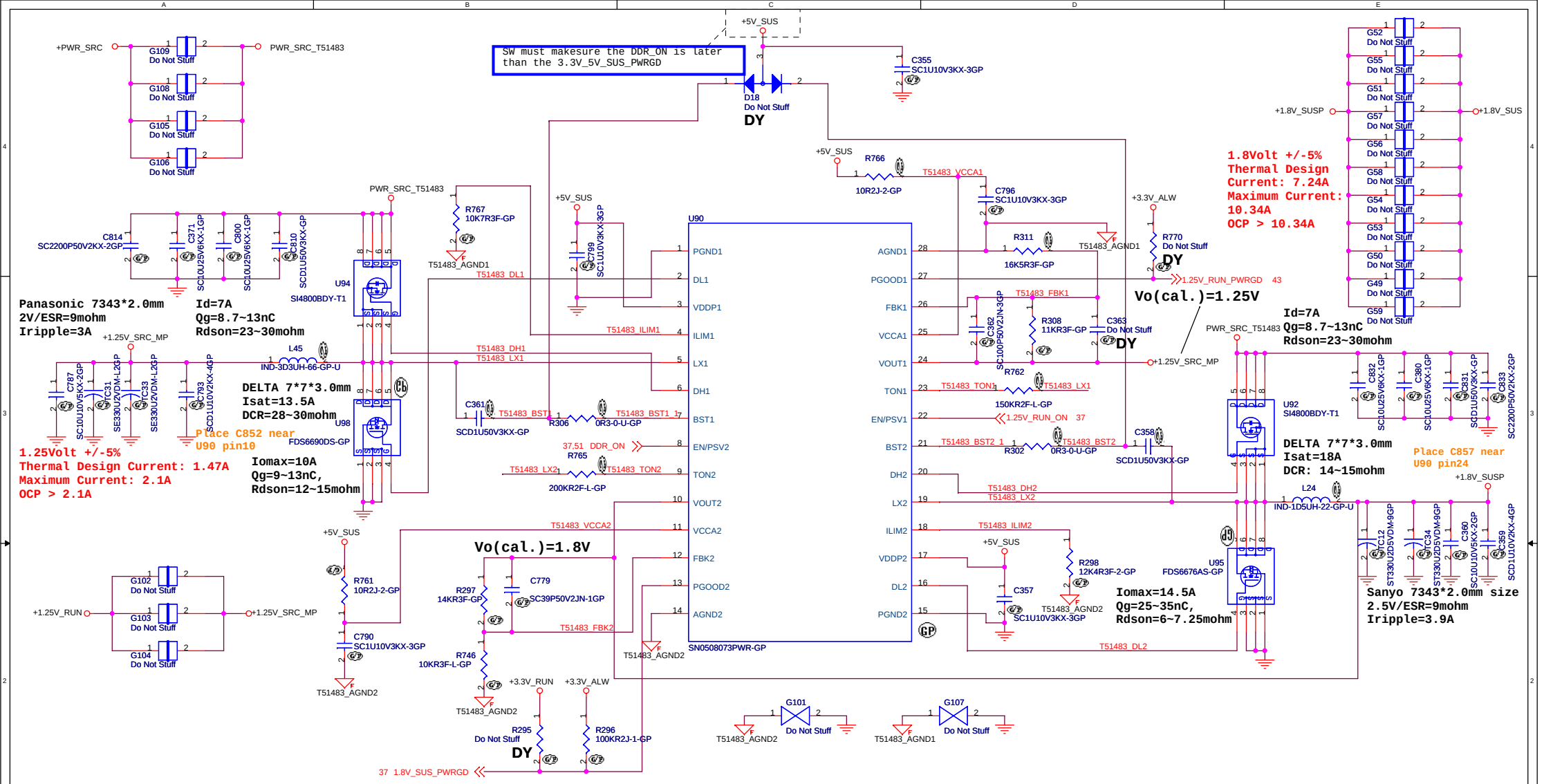

Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/2*L*f)*((Vin-Vout)*Vou)/Vin
Vout=(1+(Rtop/Rbottom))*0.75

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DC to DC 1.8V/ 1.25V*

Size: A3 | Document Number: Siberia / Converse | Rev: SA

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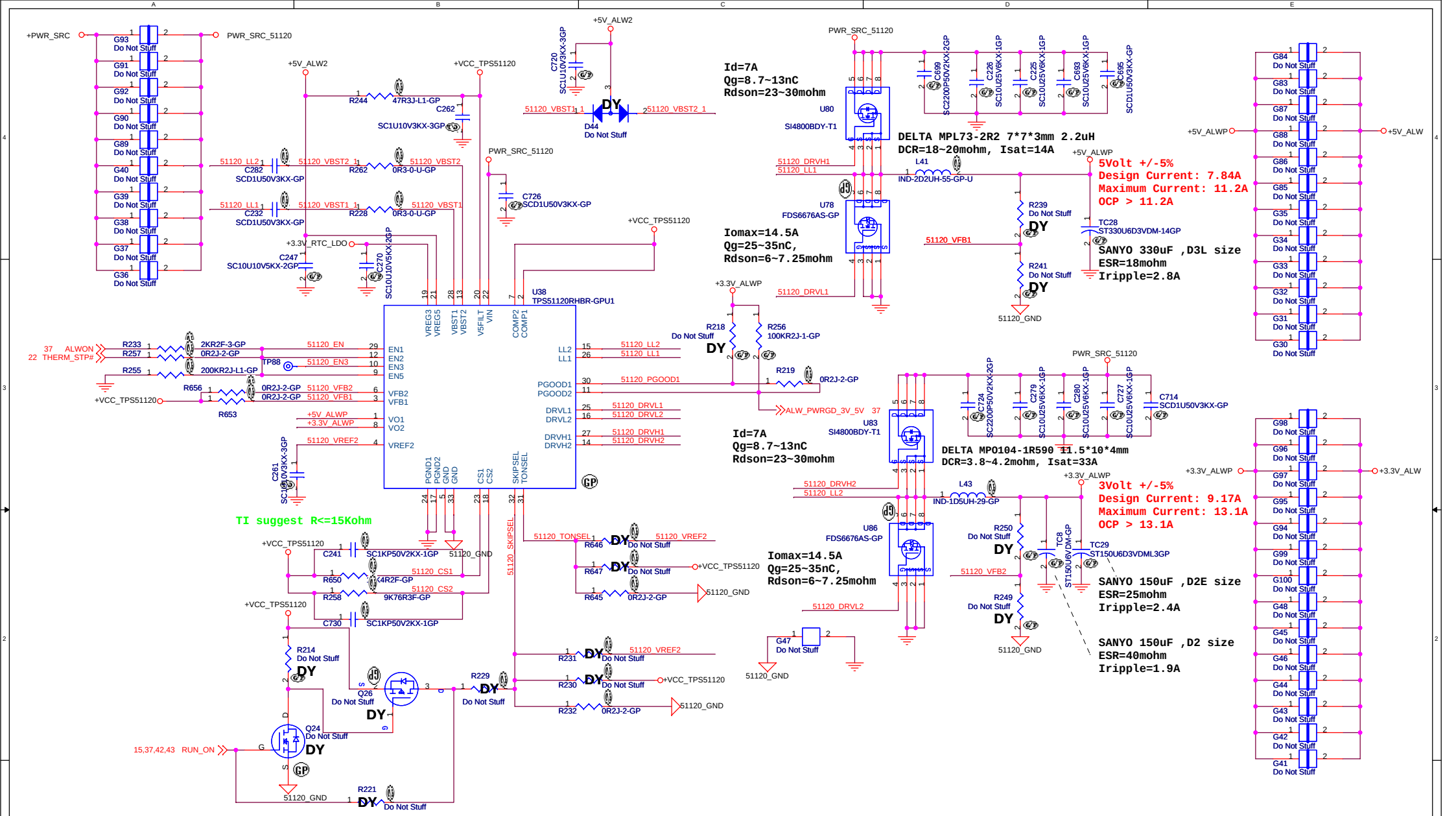

	GND	VREF2	FLOAT	VSFILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 580k/CH2	**280k/CH1 430k/CH2**	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 ON

Vout=1V*(R1+R2)/R2

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Title: **DC to DC 3.3V / 5V**

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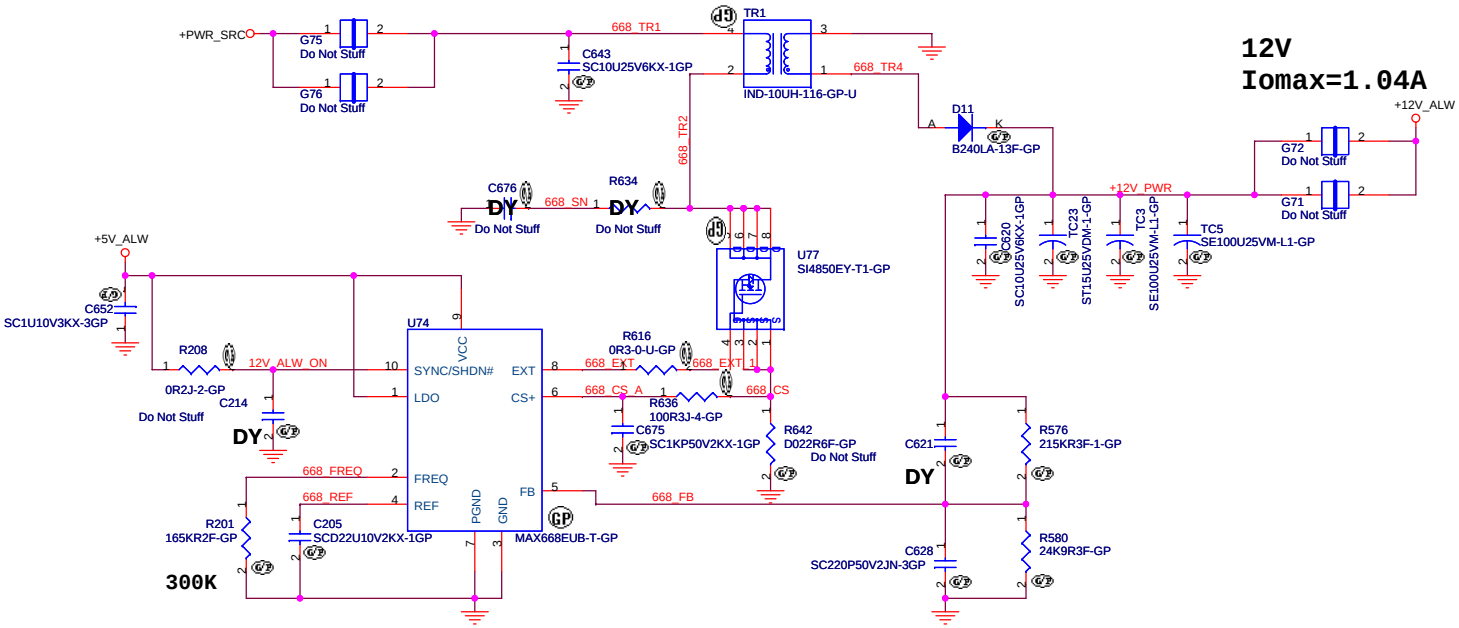

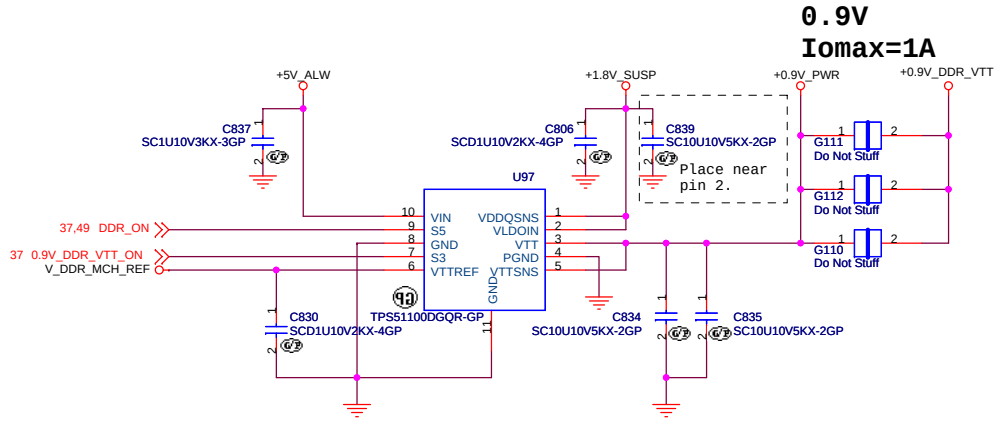

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Title: ***DC to DC 12V / 0.9V***

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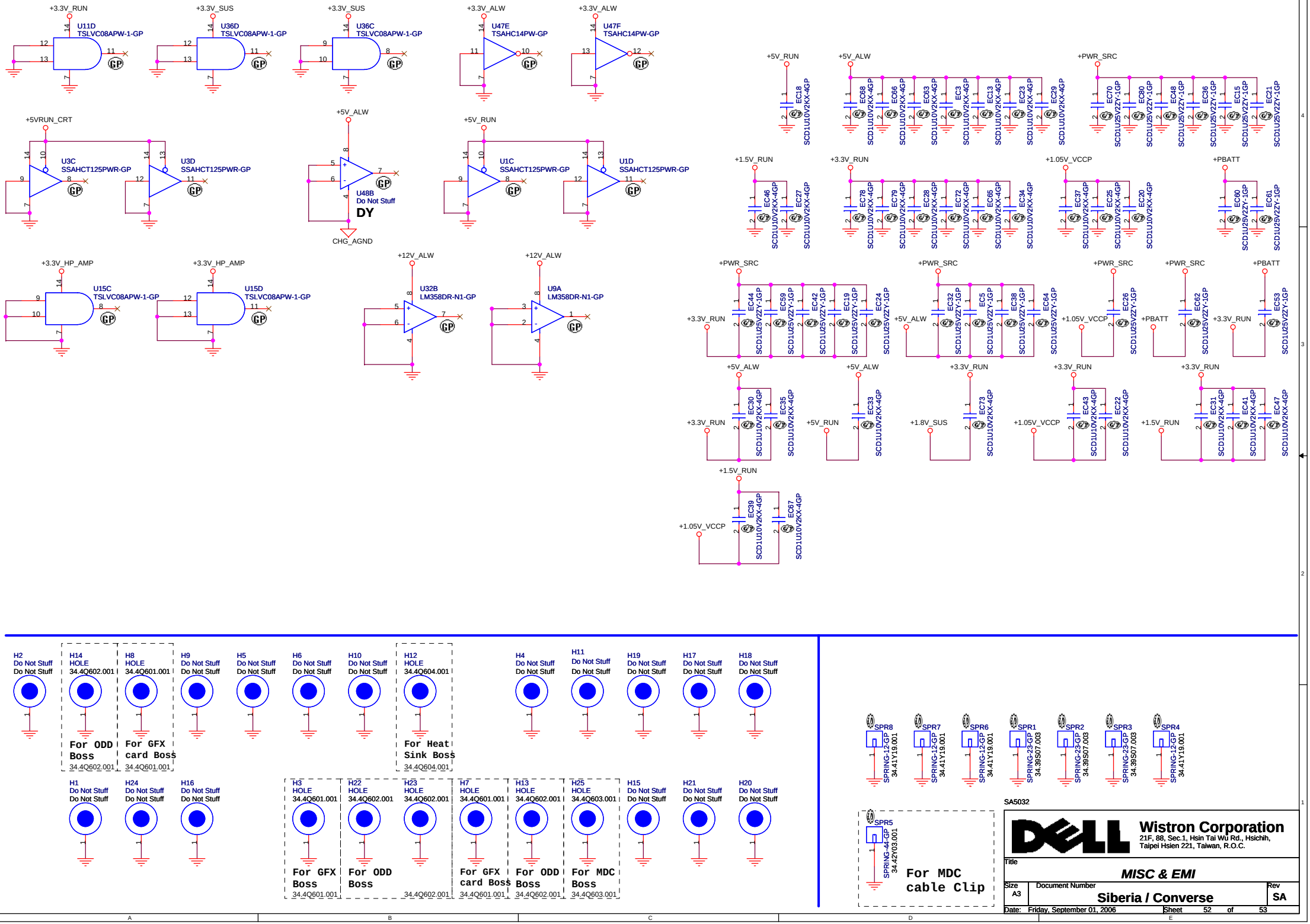
+3.3V_RUN
U11D
TSLVC08APW-1-GP
+3.3V_SUS
U36D
TSLVC08APW-1-GP
+3.3V_SUS
U36C
TSLVC08APW-1-GP
+3.3V_ALW
U47E
TSAHC14PW-GP
+3.3V_ALW
U47F
TSAHC14PW-GP
+5VRUN_CRT
U3C
SSAHCT125PWR-GP
U3D
SSAHCT125PWR-GP
+5V_ALW
U48B
Do Not Stuff
DY
CHG_AGND
+5V_RUN
U1C
SSAHCT125PWR-GP
U1D
SSAHCT125PWR-GP
+3.3V_HP_AMP
U15C
TSLVC08APW-1-GP
+3.3V_HP_AMP
U15D
TSLVC08APW-1-GP
+12V_ALW
U32B
LM358DR-N1-GP
+12V_ALW
U9A
LM358DR-N1-GP
+5V_RUN
+5V_ALW
+PWR_SRC
+1.5V_RUN
+3.3V_RUN
+1.05V_VCCP
+PBATT
+1.8V_SUS
H2 Do Not Stuff Do Not Stuff
H14 HOLE 34.4Q602.001 For ODD Boss 34.4Q602.001
H8 HOLE 34.4Q601.001 For GFX card Boss 34.4Q601.001
H9 Do Not Stuff Do Not Stuff
H5 Do Not Stuff Do Not Stuff
H6 Do Not Stuff Do Not Stuff
H10 Do Not Stuff Do Not Stuff
H12 HOLE 34.4Q604.001 For Heat Sink Boss 34.4Q604.001
H4 Do Not Stuff Do Not Stuff
H11 Do Not Stuff Do Not Stuff
H19 Do Not Stuff Do Not Stuff
H17 Do Not Stuff Do Not Stuff
H18 Do Not Stuff Do Not Stuff
H1 Do Not Stuff Do Not Stuff
H24 Do Not Stuff Do Not Stuff
H16 Do Not Stuff Do Not Stuff
H3 HOLE 34.4Q601.001 For GFX Boss 34.4Q601.001
H22 HOLE 34.4Q602.001 For ODD Boss 34.4Q602.001
H23 HOLE 34.4Q602.001
H7 HOLE 34.4Q601.001 For GFX card Boss 34.4Q601.001
H13 HOLE 34.4Q602.001 For ODD Boss 34.4Q602.001
H25 HOLE 34.4Q603.001 For MDC Boss 34.4Q603.001
H15 Do Not Stuff Do Not Stuff
H21 Do Not Stuff Do Not Stuff
H20 Do Not Stuff Do Not Stuff
SPR8 SPRING-12-GP 34.41Y19.001
SPR7 SPRING-12-GP 34.41Y19.001
SPR6 SPRING-12-GP 34.41Y19.001
SPR1 SPRING-23-GP 34.39S07.003
SPR2 SPRING-23-GP 34.39S07.003
SPR3 SPRING-23-GP 34.39S07.003
SPR4 SPRING-12-GP 34.41Y19.001
SPR5 SPRING-44-GP 34.42Y03.001 For MDC cable Clip
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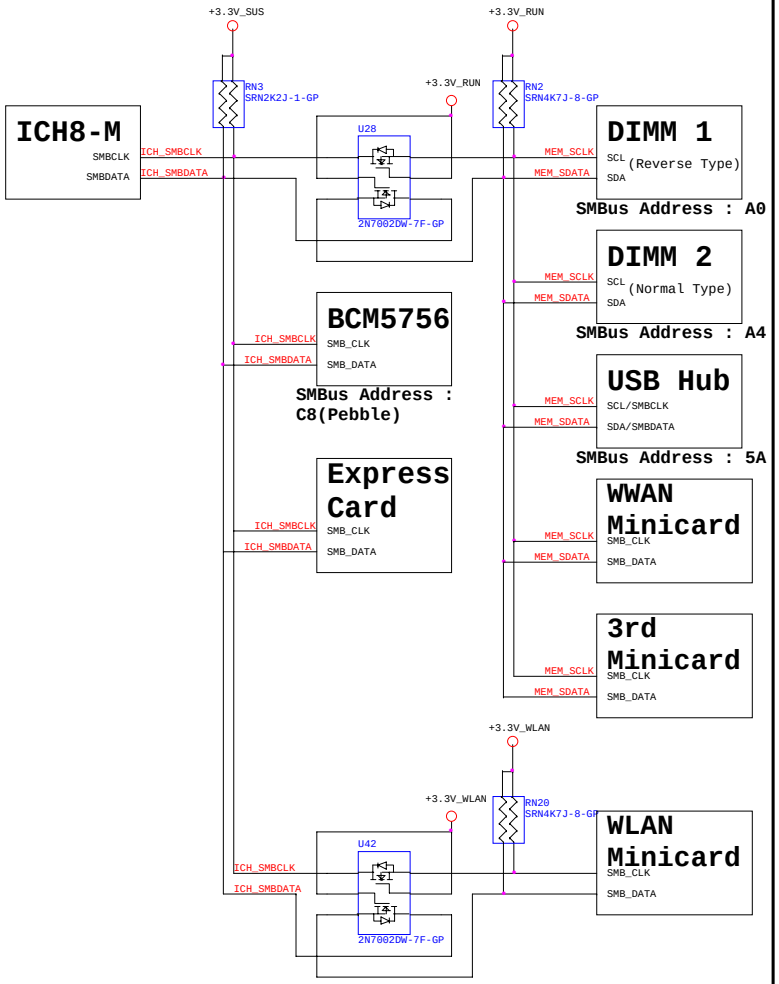
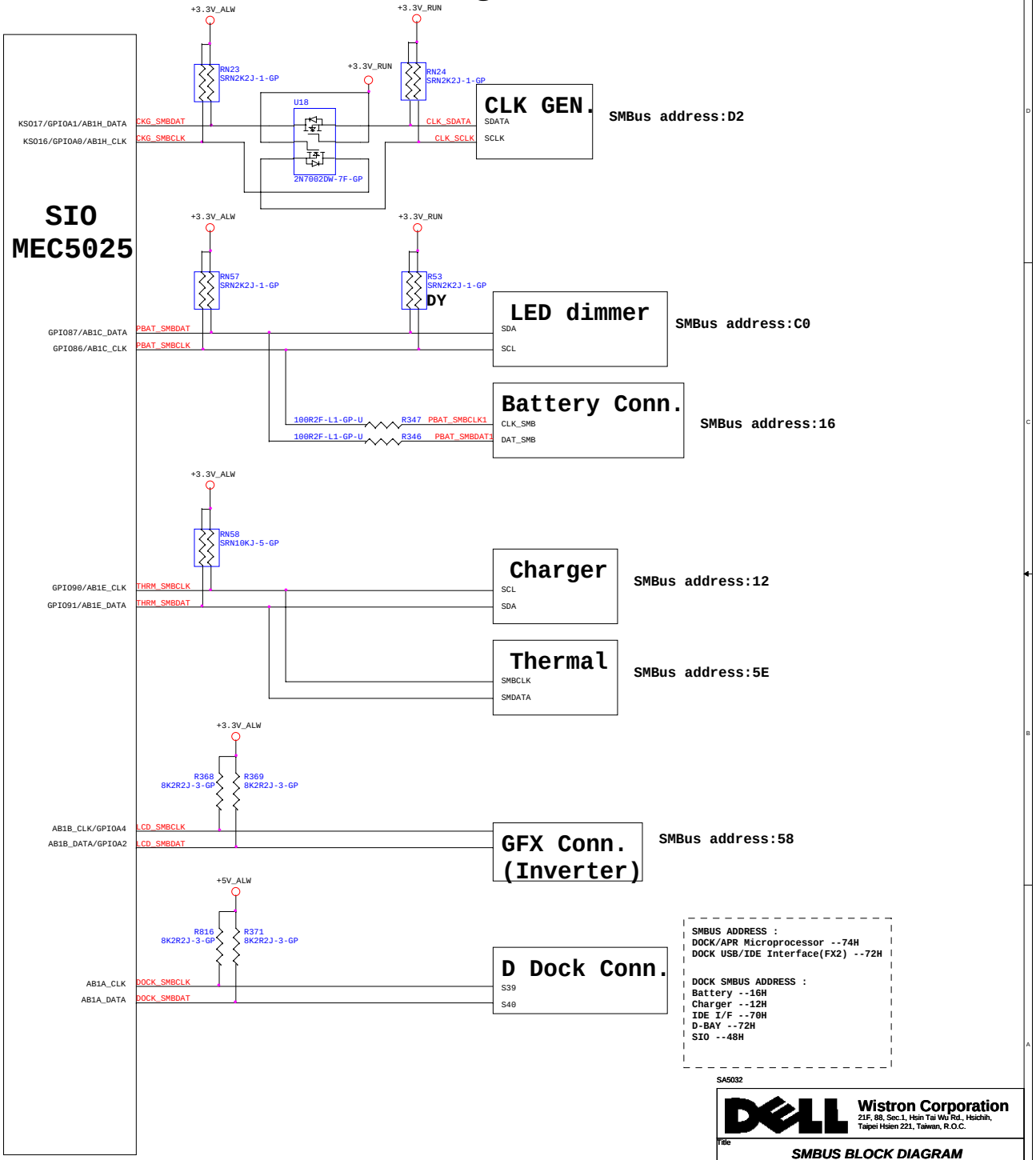
ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



SMBUS ADDRESS :
DOCK/APR Microprocessor --74H
DOCK USB/IDE Interface(FX2) --72H

DOCK SMBUS ADDRESS :
Battery --16H
Charger --12H
IDE I/F --70H
D-BAY --72H
SIO --48H

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Title: SMBUS BLOCK DIAGRAM

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