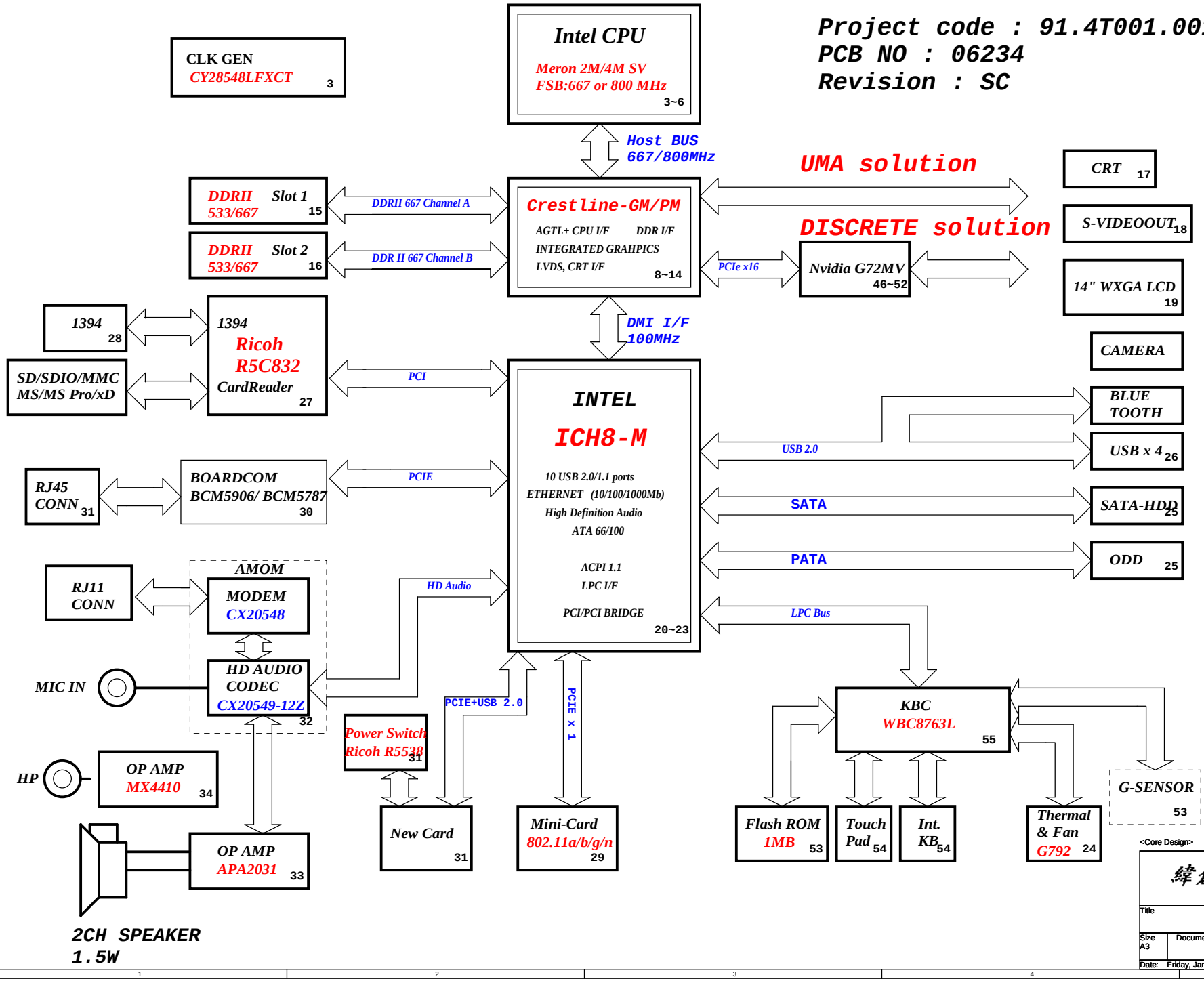
Anote2.0 Block Diagram

Project code : 91.4T001.001
PCB NO : 06234
Revision : SC



SYSTEM DC/D TPS51120	
INPUTS	OUTP
DCBATOUT	5V_S3 3D3V_S

SYSTEM DC/D ISL6268CAZ	
INPUTS	OUTPU
DCBATOUT	1D05V_

SYSTEM DC/D TPS51116	
INPUTS	OUTPU
DCBATOUT	1D8V_S 0D9V_S

CHARGER ISL6255	
INPUTS	OUTPU
DCBATOUT	BT+ 20V 3. 5V 1

CPU DC/DC ISL6262ACRZ	
INPUTS	OUTPU
DCBATOUT	VCC_C

PCB LAYE

L1: Signal 1
L2: VCC
L3: Signal 2
L4: GND
L5: GND
L6: Signal 4

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C

Title: **Block Diagram**
Size: A3
Document Number: Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 1 of

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD	tp3	AZ_DOUT_ICH	Description
0		0	RSVD
0		1	Enter XOR Chain
1		0	Normal Operation(default)
1		1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3	
low	= A16 swap override enable
high	= default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order) ★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation ★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

<21,23> +RTCVCC +RTCVCC
<4,5,6,7,8,11,12,13,21,23,39> 1D05V_S0 1D05V_S
<3,10,12,23,42> 1D25V_S0 1D25V_S
<30> 1D2V_LAN_S5 1D2V_LA
<31,57> 1D5V_NEW_S0 1D5V_NE
<10,12,13,15,16,40,42,45> 1D8V_S3 1D8V_S3
<30,31> 2D5V_LAN_S5 2D5V_LA
<24,38,44,53,54,55> 3D3V_AUX_S5 3D3V_AU
<30,31> 3D3V_LAN_S5 3D3V_LA
<3,10,11,12,13,15,16,17,18,19,20,21,22,23,24,25,27,28,29,30,31,32,34,35,36,38,39,41,42,45,46,47,50,52,53,54,55,56,57,58> 3D3V_S0 3D3V_S0
<19,20,21,22,23,26,29,30,31,32,38,40,43,45,53,54,55,58> 3D3V_S5 3D3V_S5
<29,38,43> 5V_AUX_S5 5V_AUX_
<17,19,22,23,24,25,33,35,36,39,41,42,45,46,54,56,57> 5V_S0 5V_S0
<23,26,38,40,45,56> 5V_S5 5V_S5
<43,44> AD+ AD+
<19,36,37,38,39,40,41,43,45,56> DCBATOUT DCBATOU
<10,15,16,40> DDR_VREF_S3 DDR_VRE
<19> LCDVDD_S0 LCDVDD_
<5,6,37> VCC_CORE_S0 VCC_COR

<Core Design>

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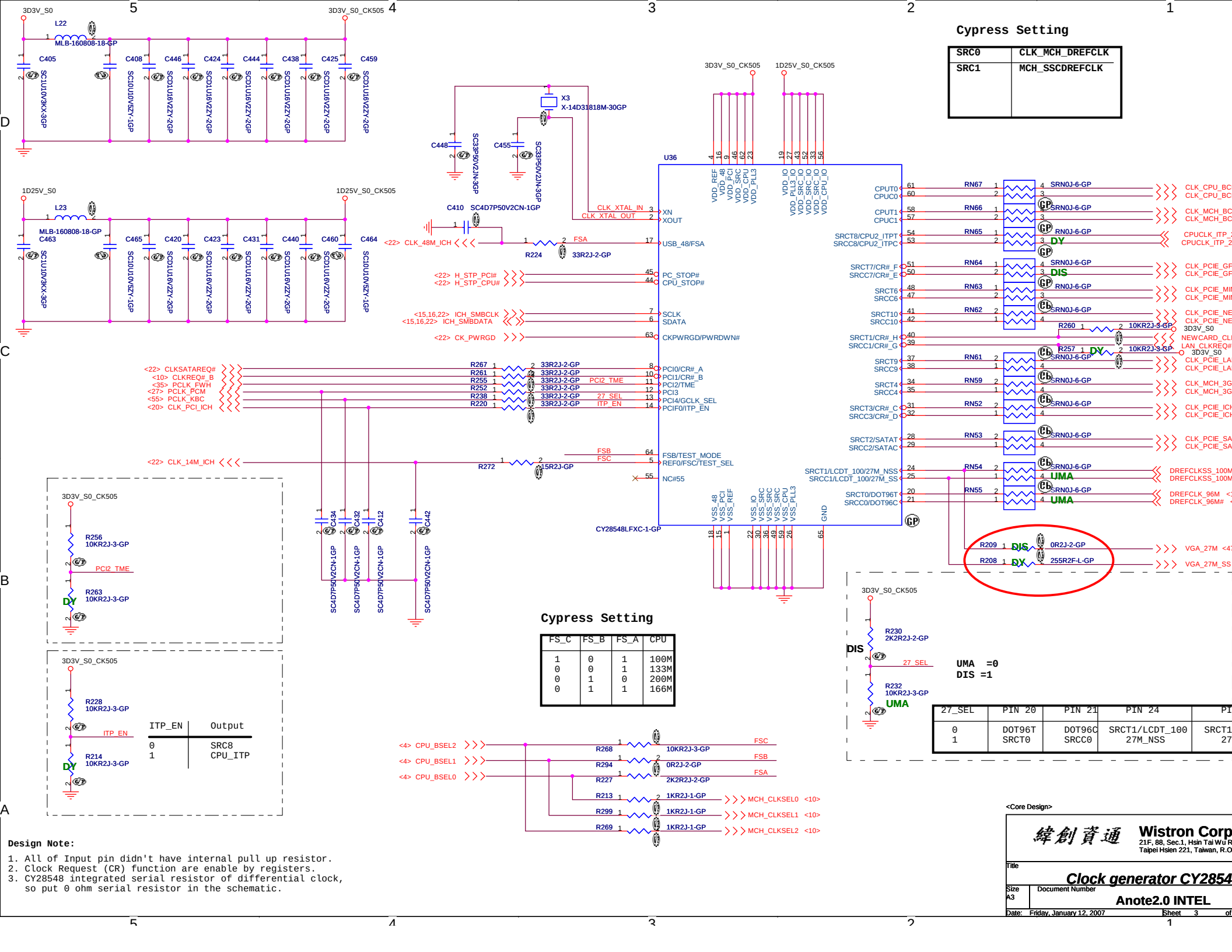
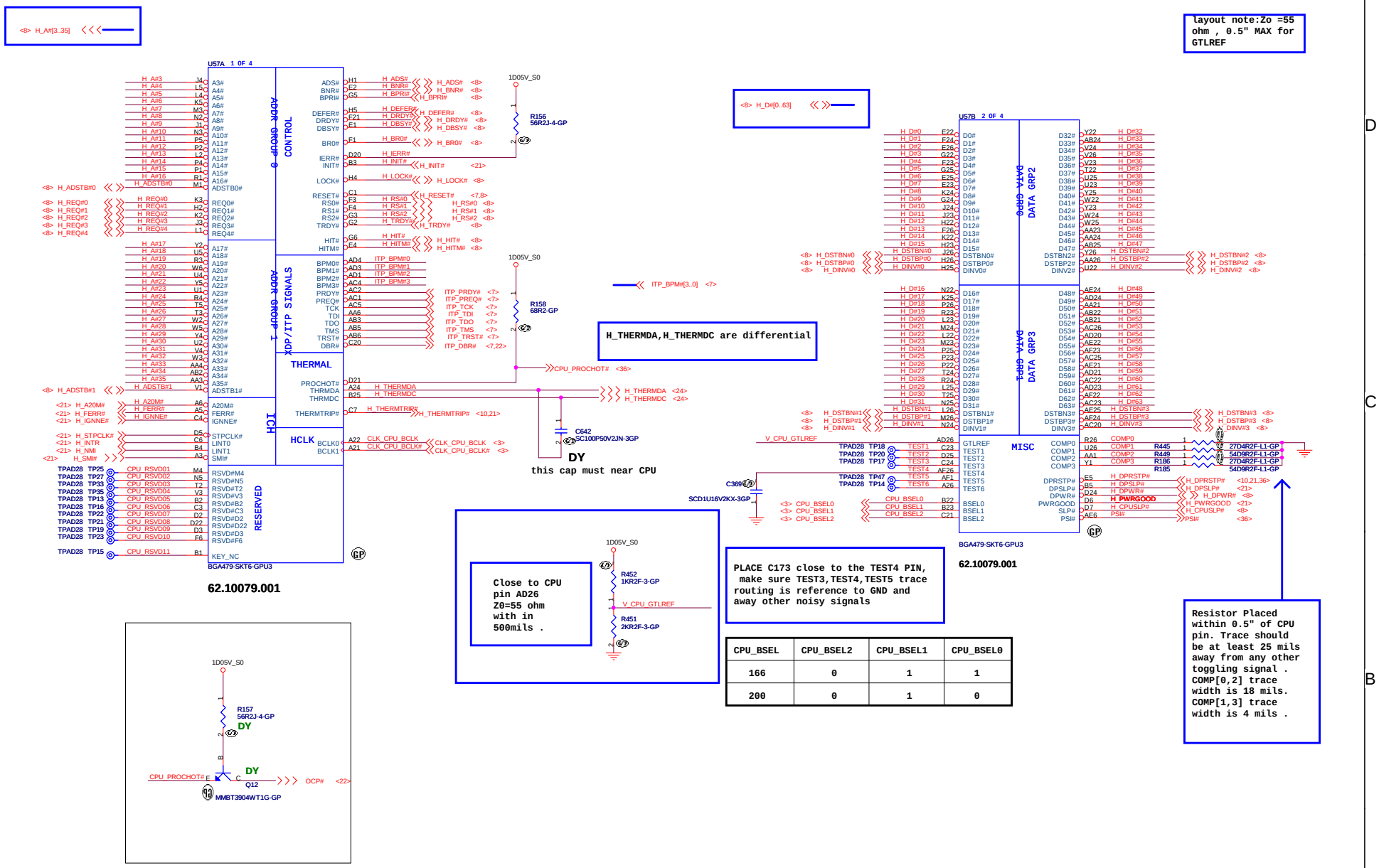
Title: Table of Content

Size: A3 | Document Number: Anote2.0 INTE

Date: Friday, January 12, 2007 | Sheet 2 of


Cypress Setting
SRC0 CLK_MCH_DREFCLK
SRC1 MCH_SSCDREFCLK
U36
CY28548LFXC-1-GP
Cypress Setting
FS_C FS_B FS_A CPU
1 0 1 100M
0 0 1 133M
0 1 0 200M
0 1 1 166M
UMA =0
DIS =1
27_SEL PIN 20 PIN 21 PIN 24
0 DOT96T DOT96C SRCT1/LCDT_100 27M_NSS
1 SRCT0 SRCC0 SRCT1
ITP_EN Output
0 SRC8
1 CPU_ITP
Design Note:
1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.
<Core Design>
Wistron Corp
Clock generator CY2854
Anote2.0 INTEL
Date: Friday, January 12, 2007


layout note:Zo =55 ohm , 0.5" MAX for GTLREF
U57A 1 OF 4
ADDR GROUP 0
CONTROL
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
ICH
HCLK
RESERVED
BGA479-SKT6-GPU3
62.10079.001
U57B 2 OF 4
DATA GRP2
DATA GRP3
MISC
BGA479-SKT6-GPU3
62.10079.001
H_THERMDA,H_THERMDC are differential
this cap must near CPU
Close to CPU pin AD26 Z0=55 ohm with in 500mils .
PLACE C173 close to the TEST4 PIN, make sure TEST3,TEST4,TEST5 trace routing is reference to GND and away other noisy signals
Resistor Placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal . COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils .
CPU_BSEL | CPU_BSEL2 | CPU_BSEL1 | CPU_BSEL0
166 | 0 | 1 | 1
200 | 0 | 1 | 0
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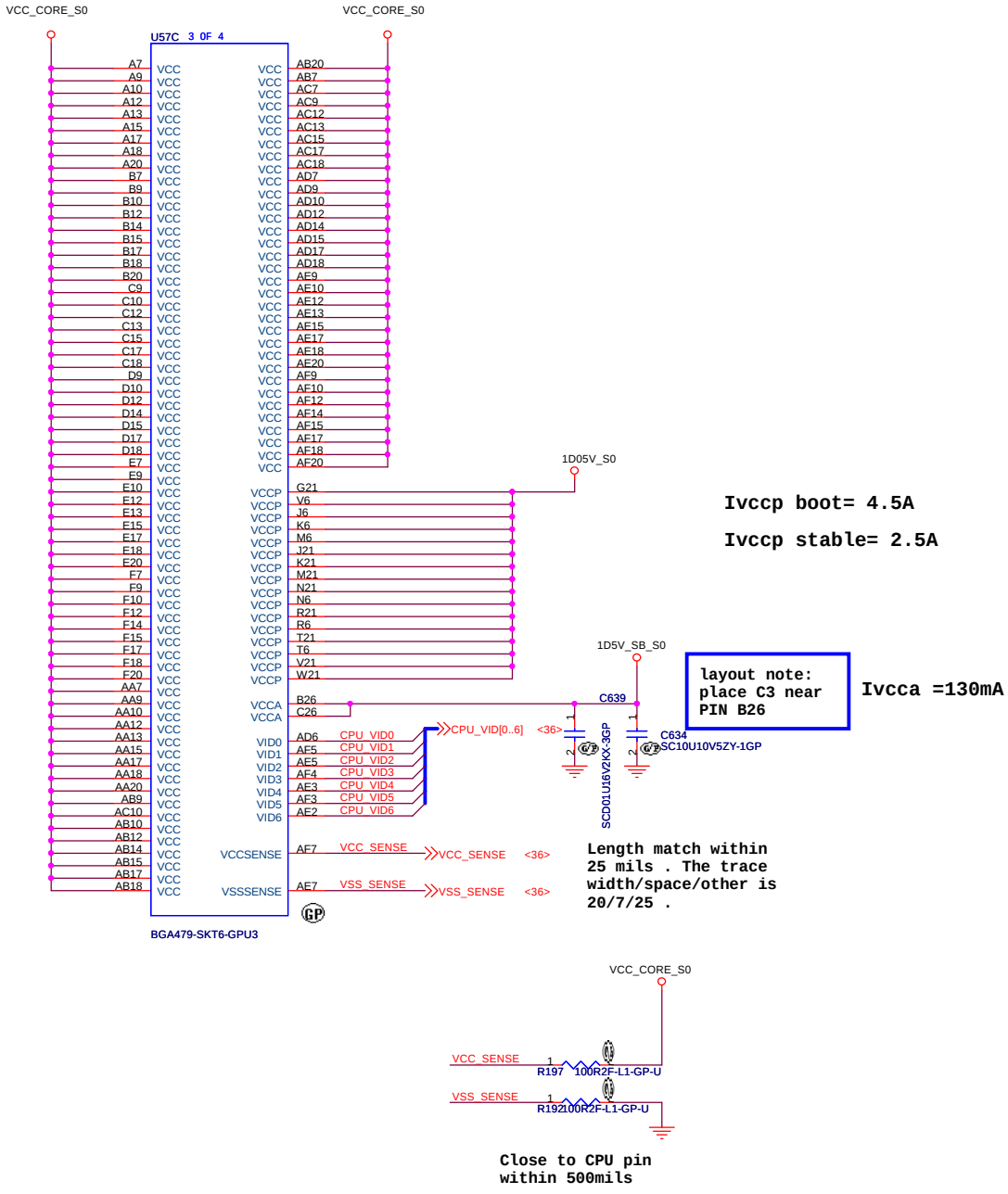
Meron(1/3)-AGTL+/XDP
Anote2.0 INTEL
SC
Friday, January 12, 2007
Sheet 4 of 58



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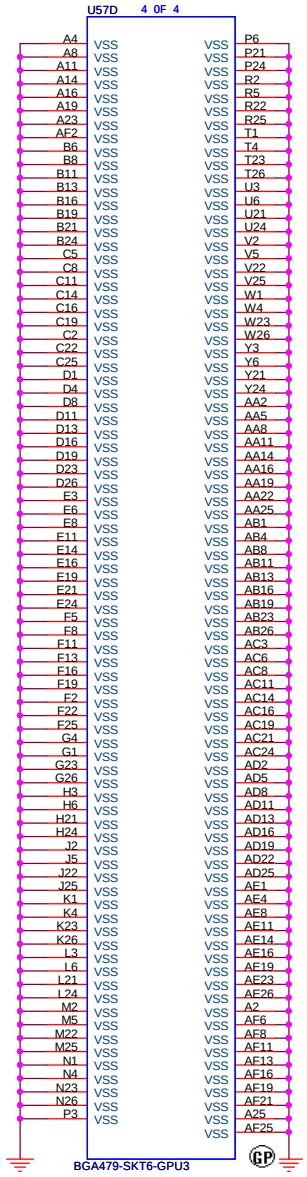
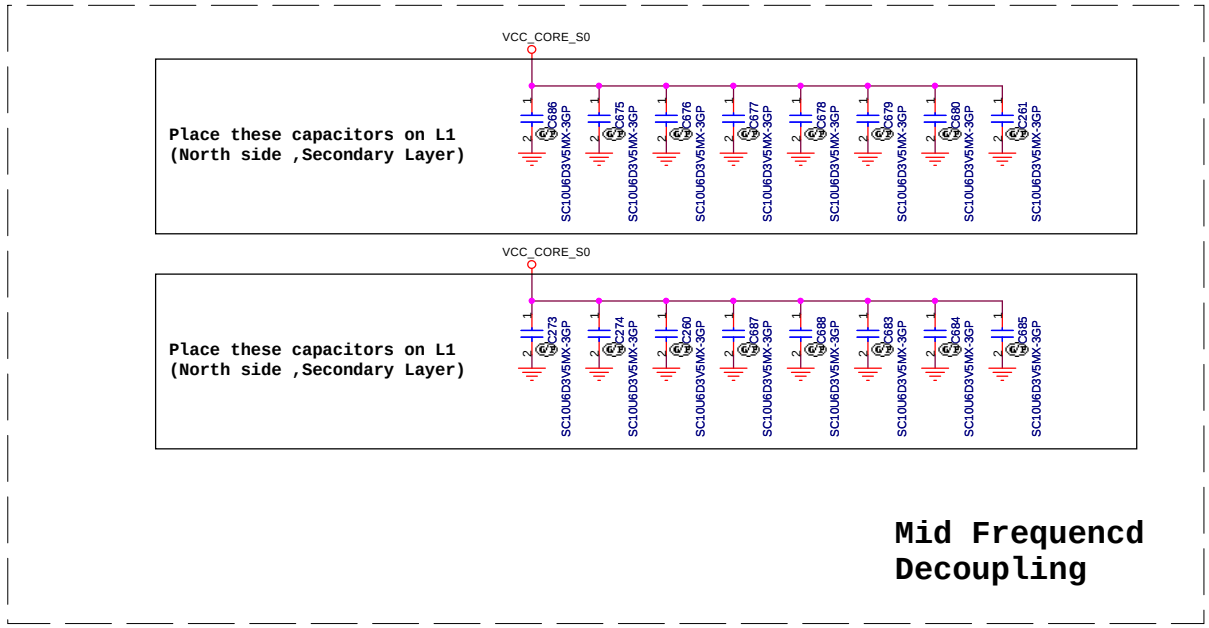
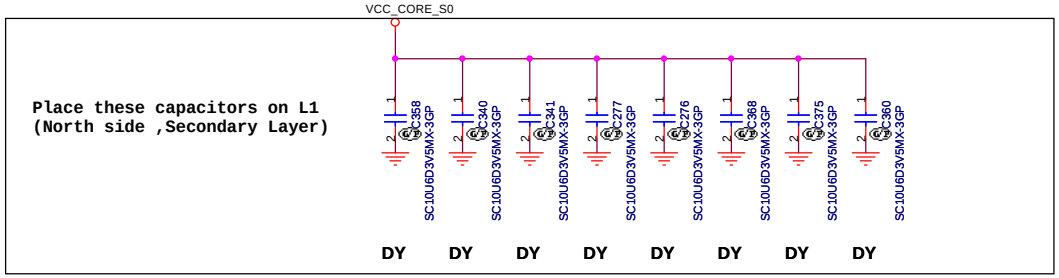
Title
Meron(2/3)-AGTL+/PWR

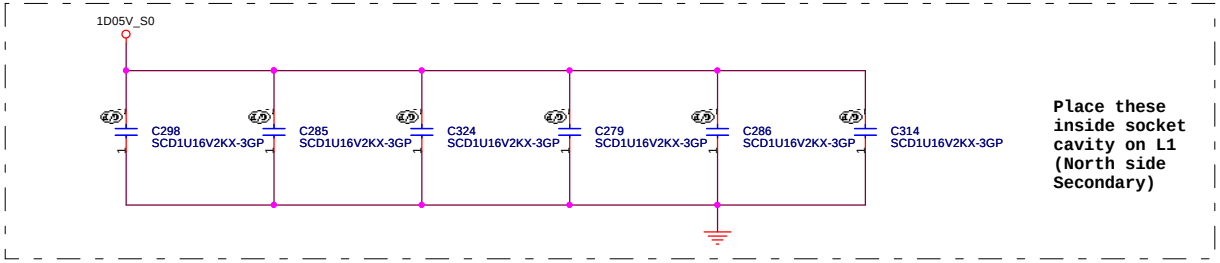
Size A3 | Document Number Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 5 of









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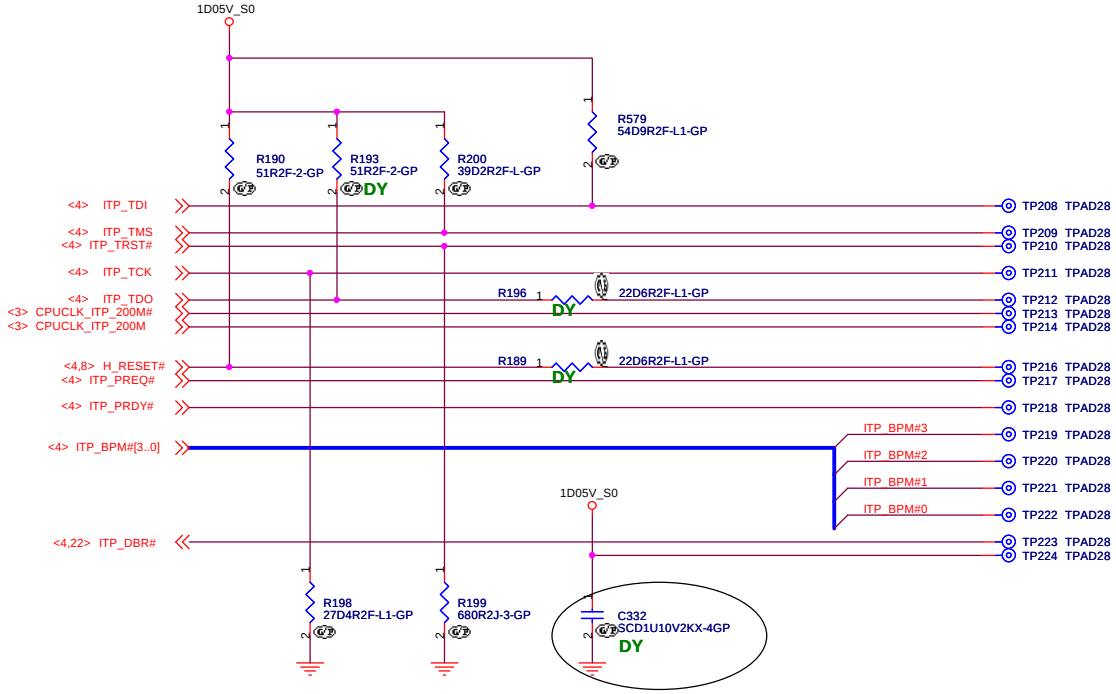
Title: Meron(3/3)-GND&Bypass

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 6 of

ITP Connector



<Core Design>

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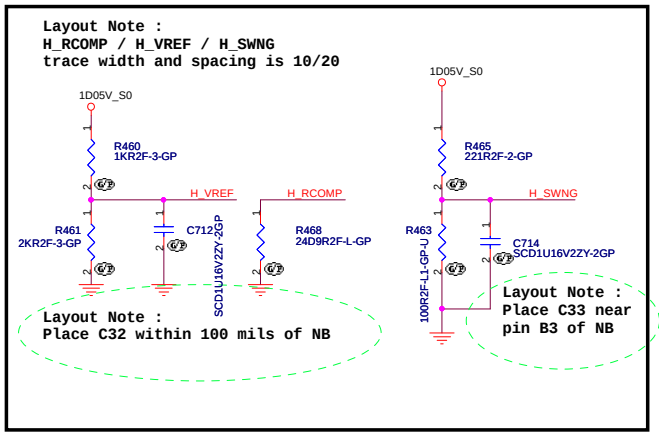
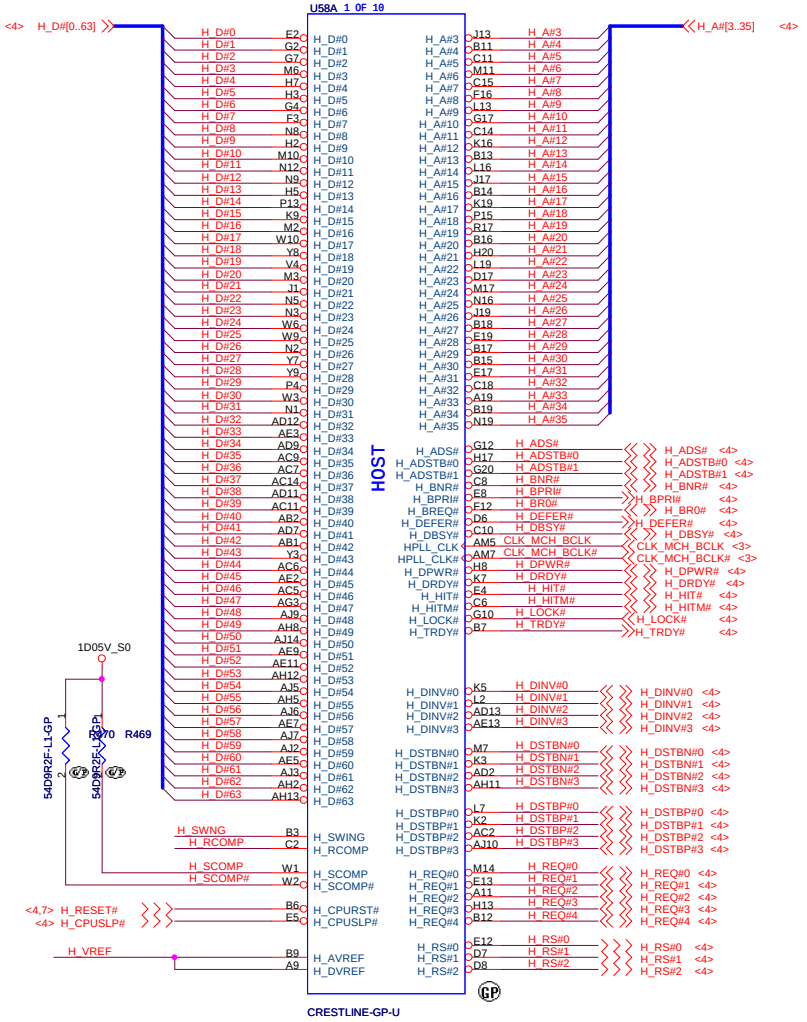
Title: *Meron(3/3)-GND&Bypass*

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 7 of

layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing
and impedance (55 ohm) same as FSB data traces





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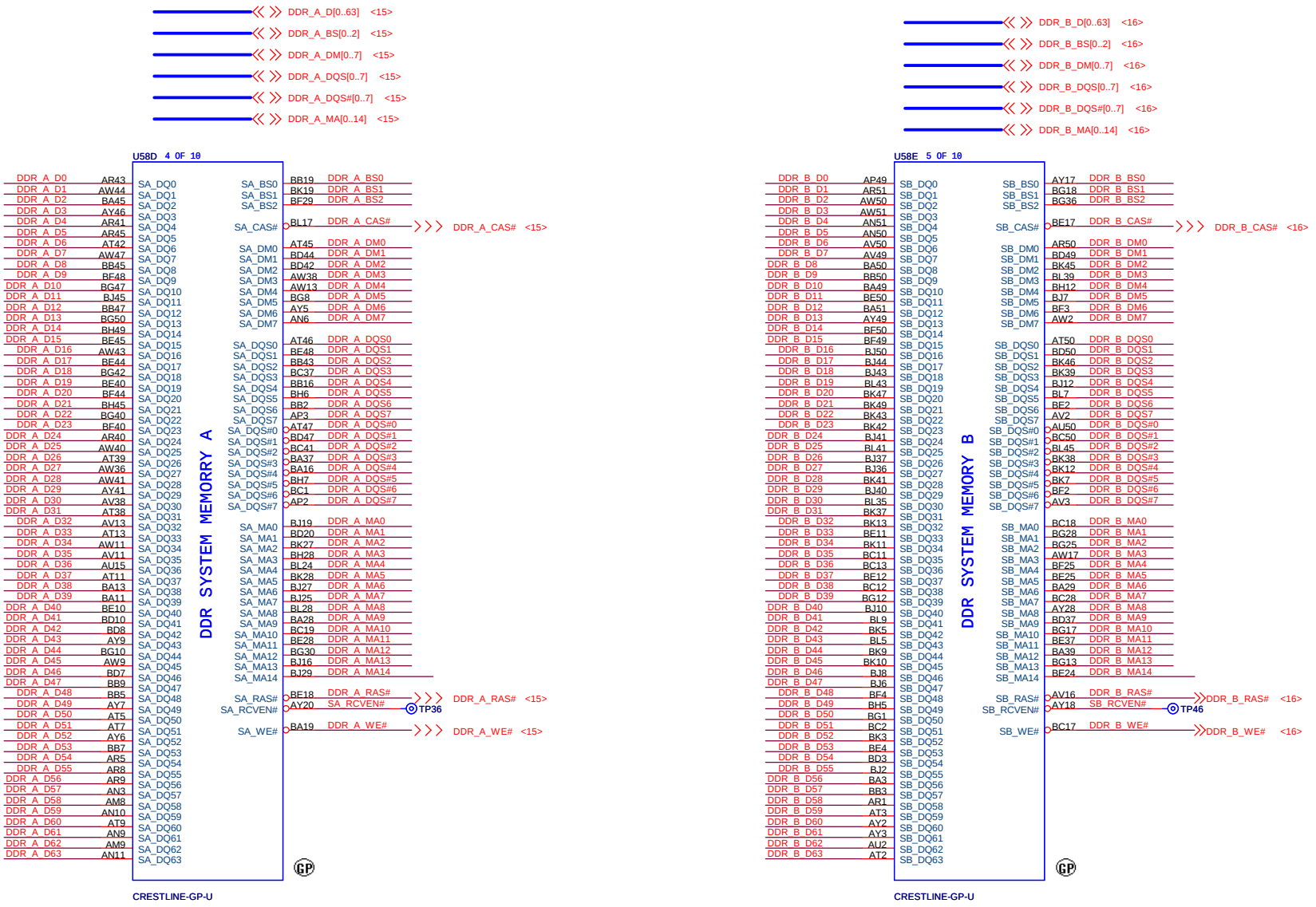
Title: CRESTLINE(1/7)-AGTL+/DMI/DDR2

Size	Document Number	Rev
Custom	Anote2.0 INTEL	SC

Date: Friday, January 12, 2007 Sheet 8 of 58



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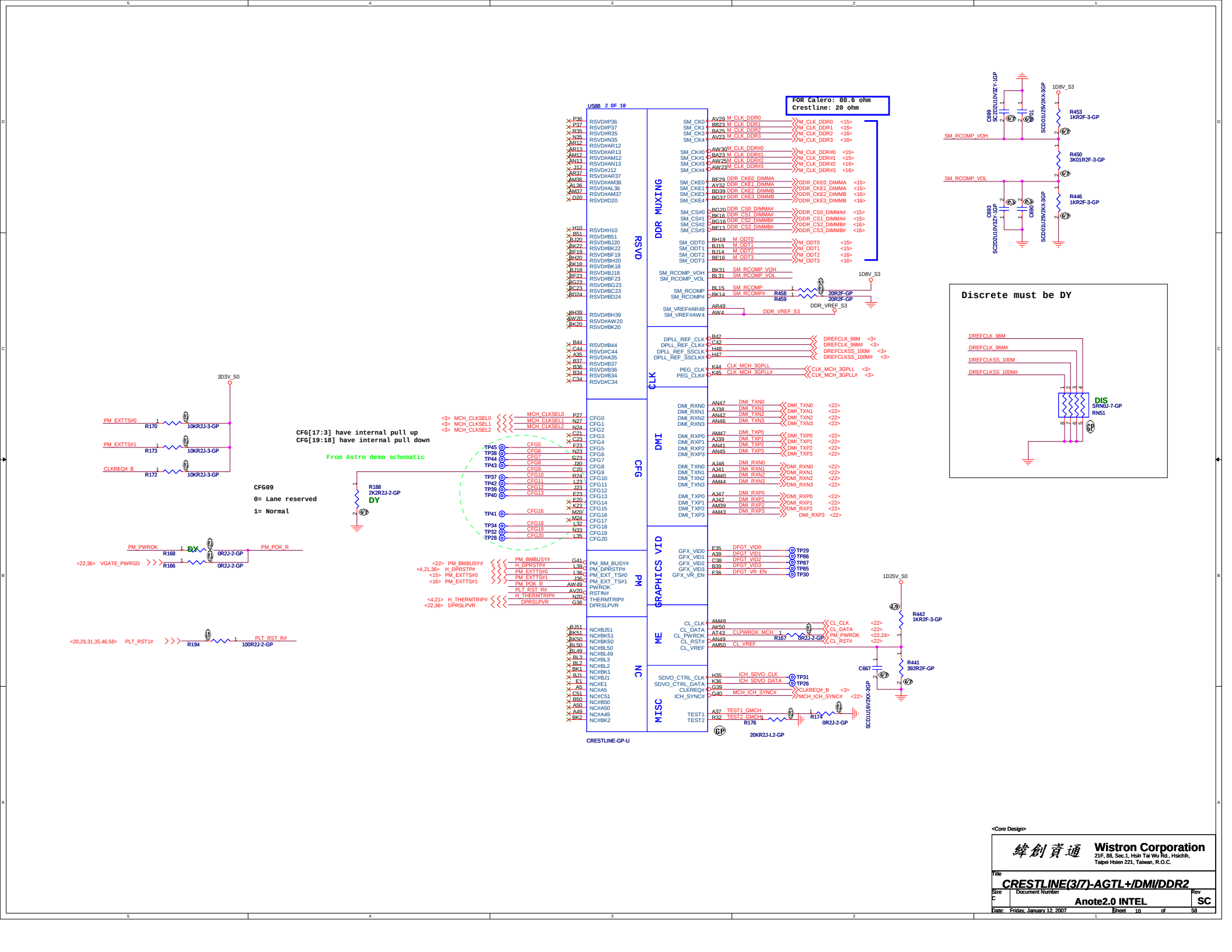
Title
CRESTLINE(2/7)-DDR2 A/B CH

Size A3 | Document Number Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 9 of


FOR Calero: 80.6 ohm
Crestline: 20 ohm
CFG[17:3] have internal pull up
CFG[19:18] have internal pull down
From Astro demo schematic
CFG09
0= Lane reserved
1= Normal
Discrete must be DY
CRESTLINE-GP-U
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CRESTLINE(3/7)-AGTL+/DMI/DDR2
Anote2.0 INTEL
Friday, January 12, 2007

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operationa 1 = PCIE/SDVO are operating simu.

PEGCOMP trace width and spacing is 20/25 mils.

For Crestline : 2.4 Kohm
For Calero : 1.5Kohm

FOR Calero: 255 ohm
Crestline: 1.3k ohm

U58C 3 OF 10

CRESTLINE-GP-U

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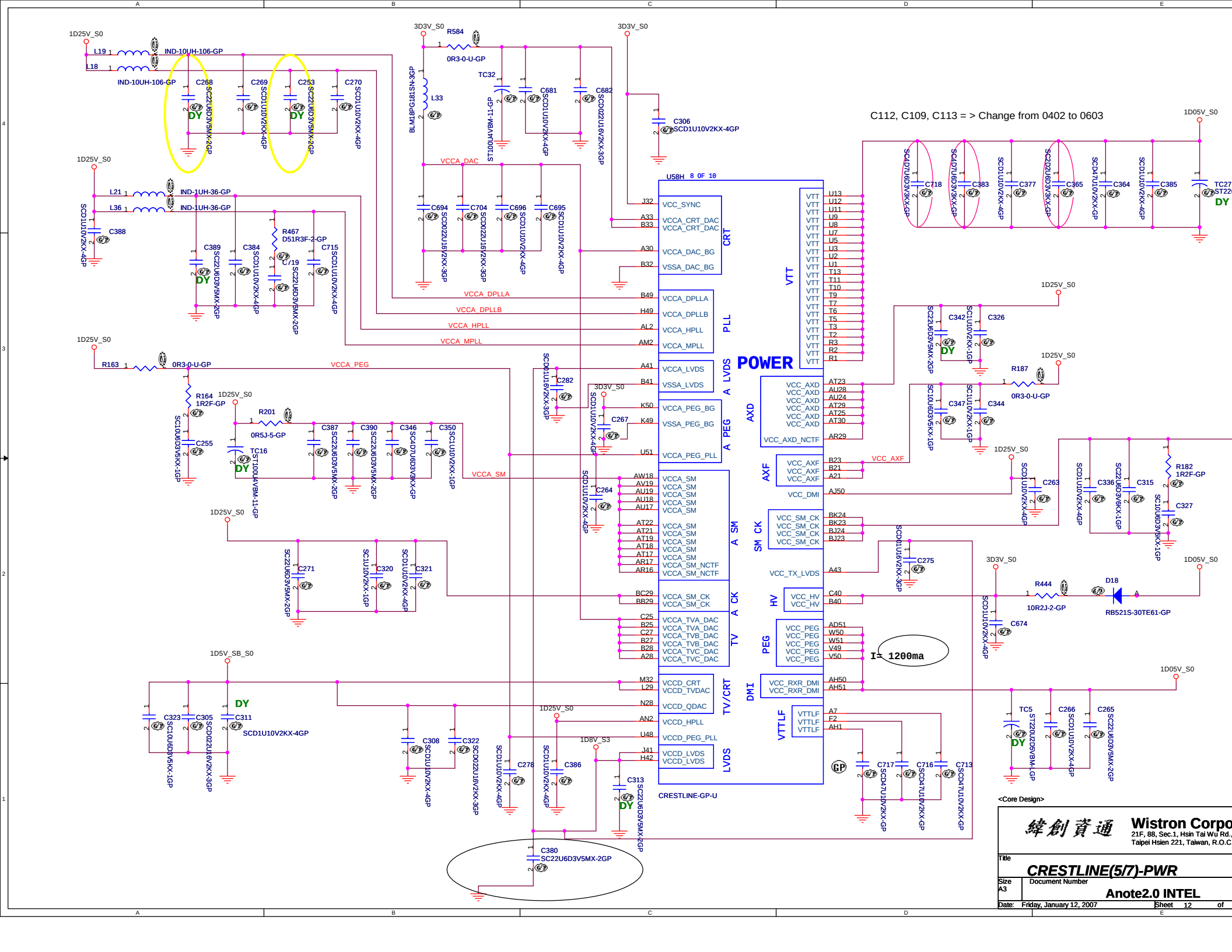
Title: CRESTLINE(4/7)-VGA/LVDS/

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 11 of


C112, C109, C113 = > Change from 0402 to 0603
POWER
CRESTLINE-GP-U
I= 1200ma
VCCA_DAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_PEG
VCCA_SM
VCC_AXF
VCC_TX_LVDS
VCC_DMI
VTT
AXD
AXF
SM CK
HV
PEG
DMI
VTTLF
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
TV/CRT
LVDS
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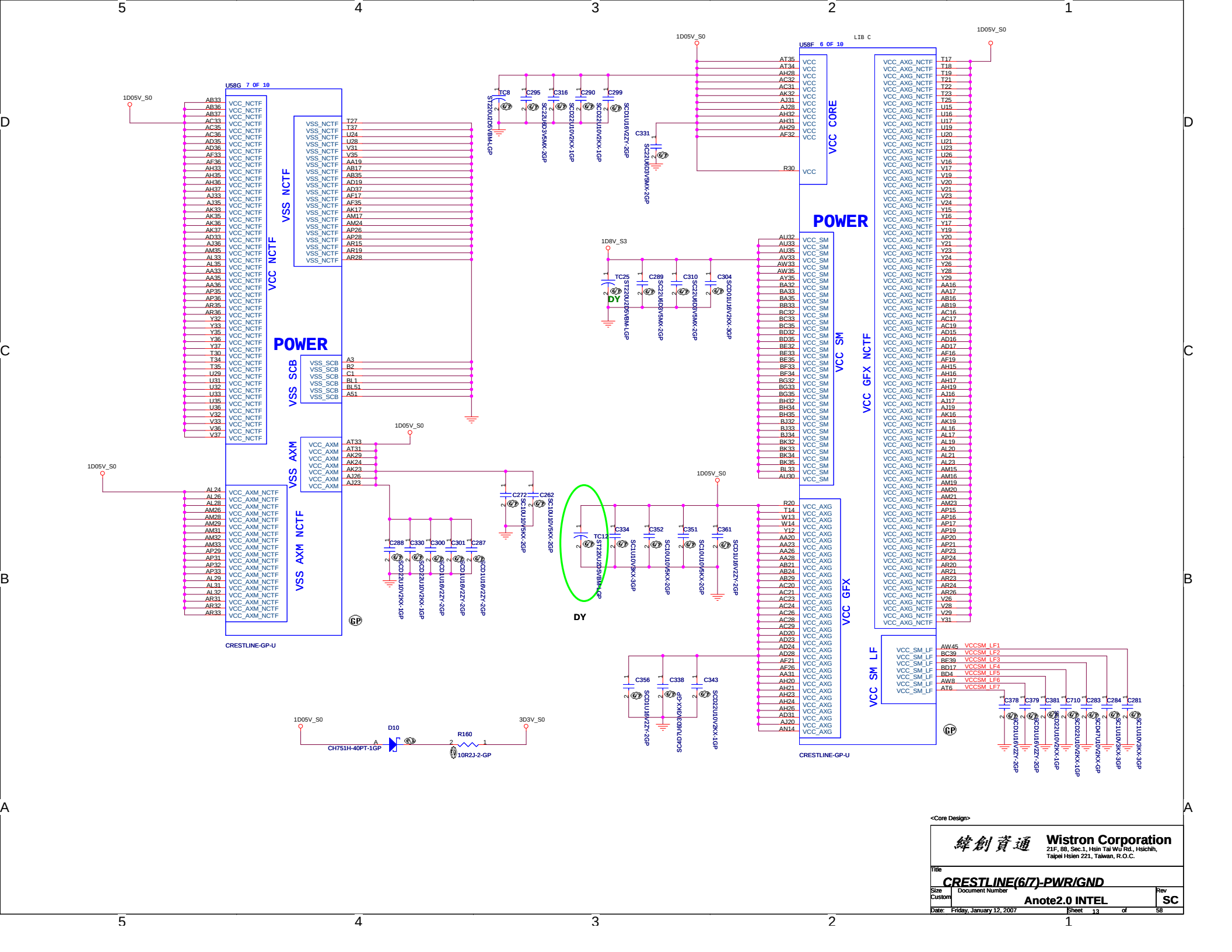
CRESTLINE(5/7)-PWR
Anote2.0 INTEL
Friday, January 12, 2007



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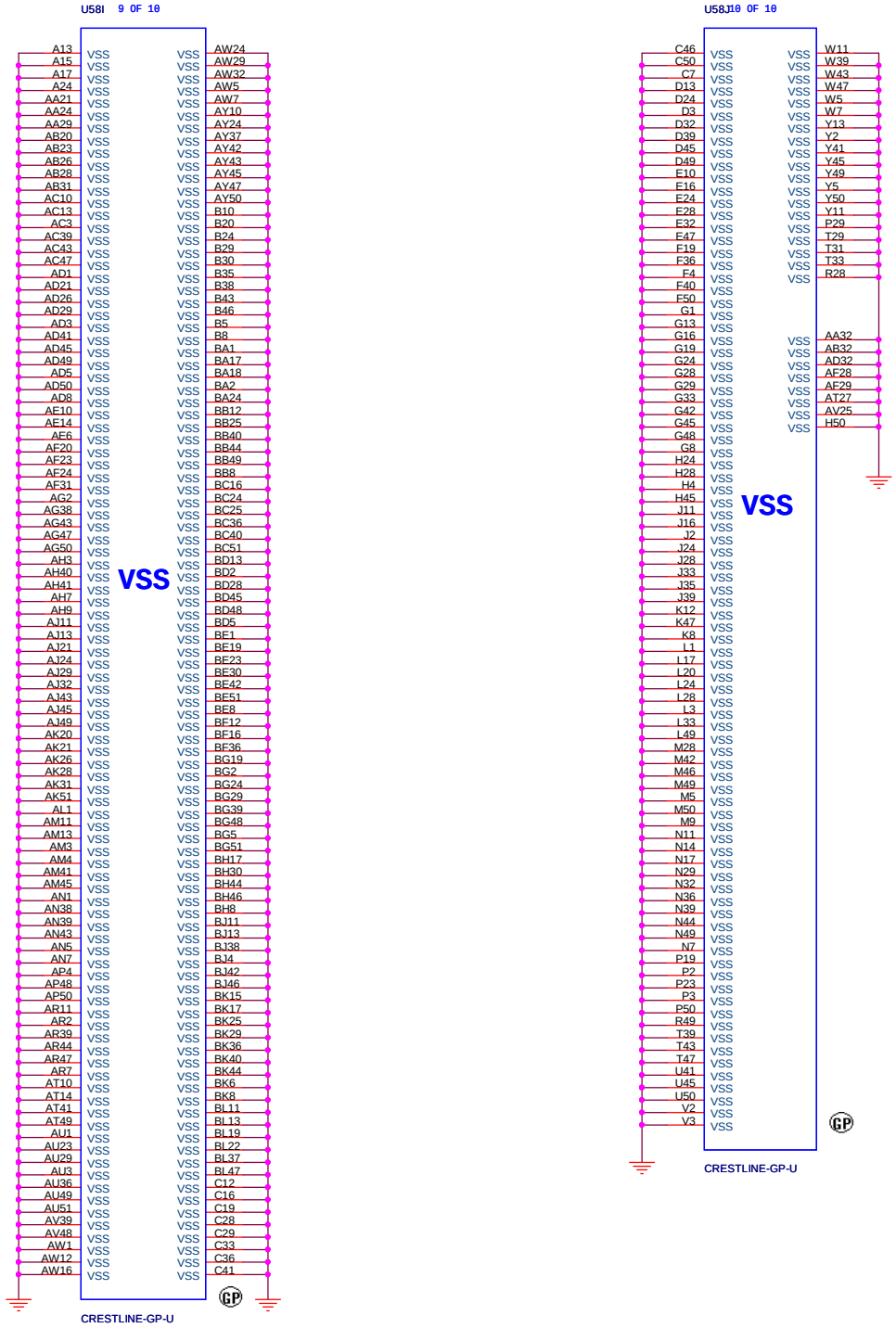
Title: CRESTLINE(6/7)-PWR/GND

Size: Custom | Document Number: Anote2.0 INTEL | Rev: SC

Date: Friday, January 12, 2007 | Sheet 13 of 58



<Core Design>

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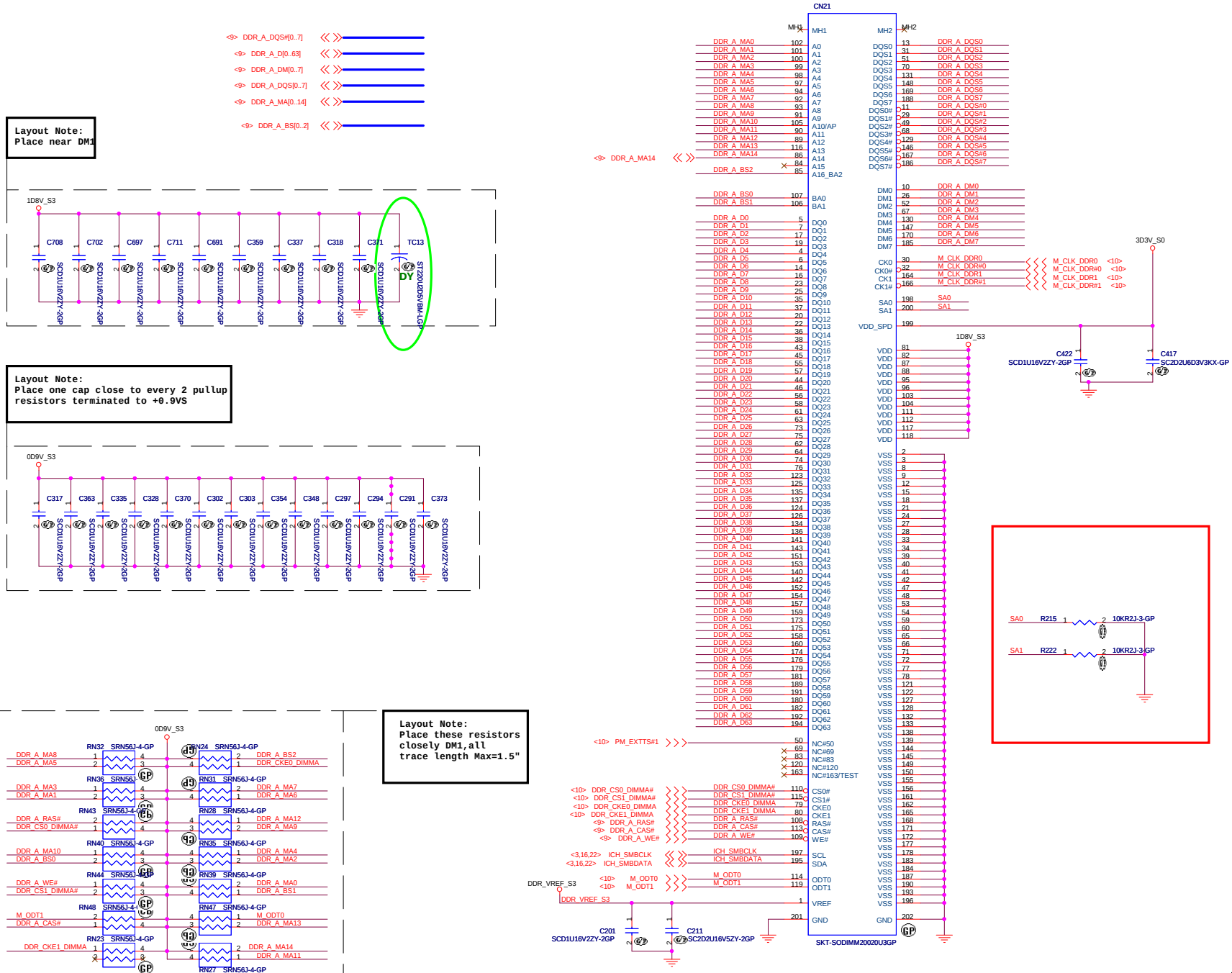
Title
CRESTLINE(7/7)-PWR/GND

Size A3 | Document Number Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 14 of



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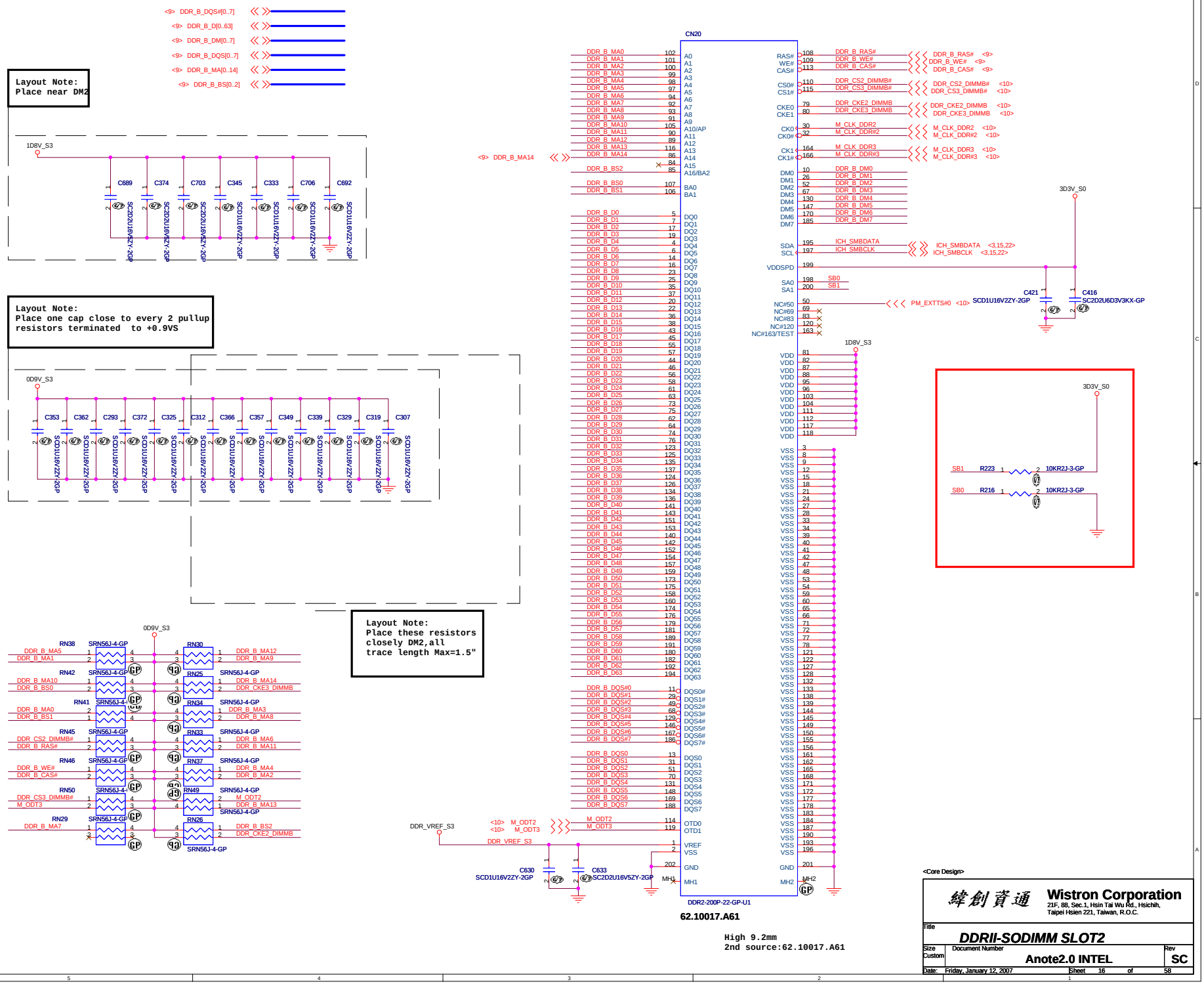
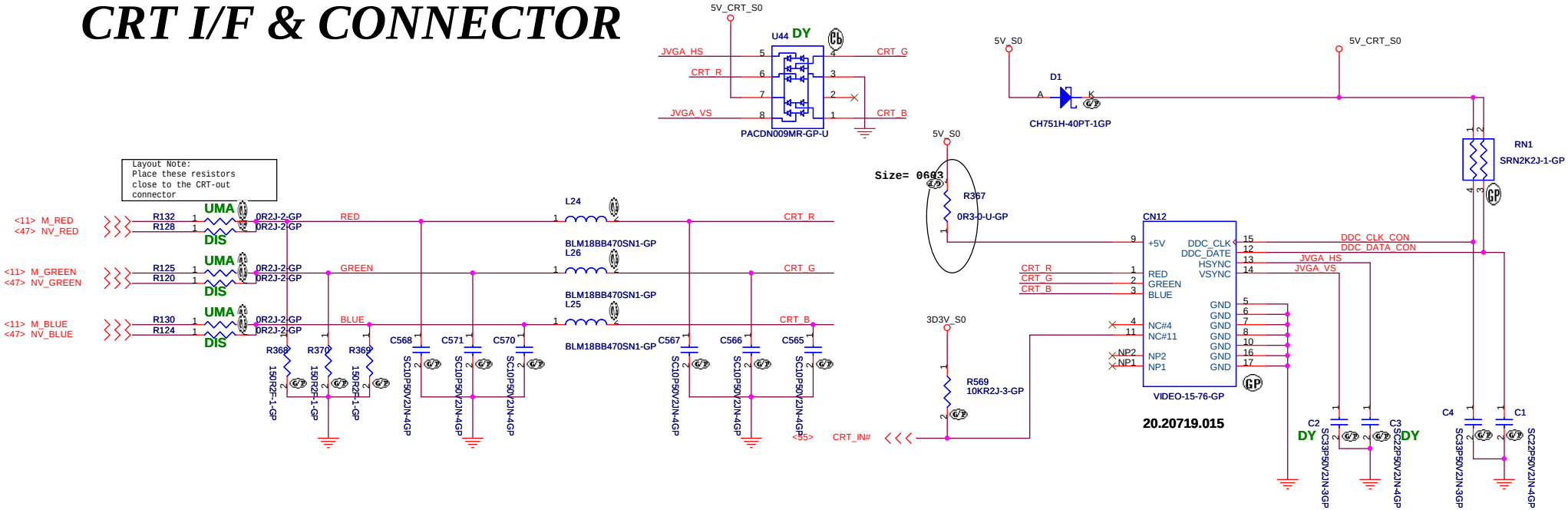
Title: **DDRII-SODIMM SLOT1**

Size: Custom | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 15 of

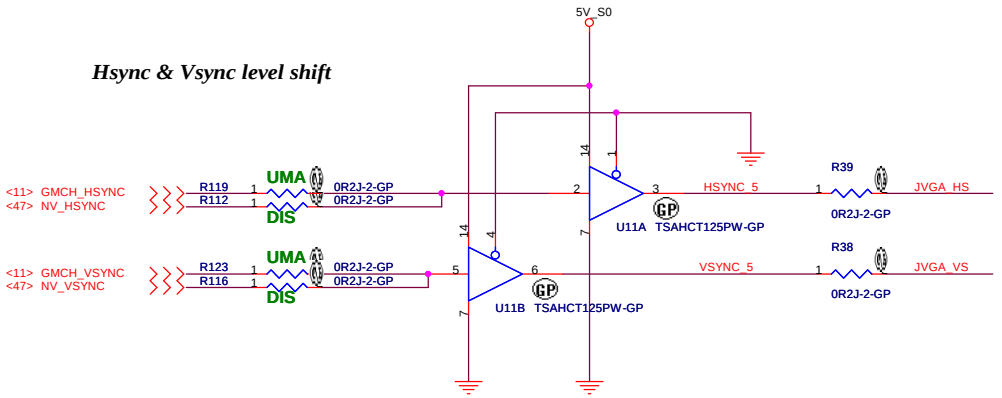

Layout Note:
Place near DM2
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
CN20
DDR2-200P-22-GP-U1
62.10017.A61
High 9.2mm
2nd source:62.10017.A61
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDRII-SODIMM SLOT2
Anote2.0 INTEL
Friday, January 12, 2007

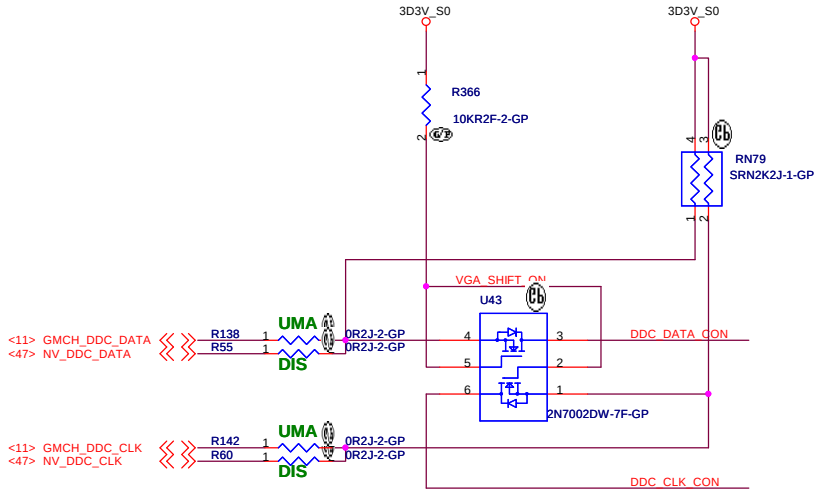
CRT I/F & CONNECTOR



Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift





<Core Design>

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Title	**CRT Connector**	
Size A3	Document Number **Anote2.0 INTEL**	
Date: Friday, January 12, 2007	Sheet 17	of

TV OUT PORT

<57> TV_LUMA
<57> TV_CRMA

<11> M_CRMA
<47> NV_CRMA

R145 UMA 0R2J-2-GP TV_CRMA_R
R64 DIS 0R2J-2-GP

L28
C572 BLM18BB470SN1-GP C573
R372 150R2F-1-GP
SC10P50V2JN-4GP
SC10P50V2JN-4GP

TV_LUMA
TV_CRMA

CN14
5 GND
1 GND
3 LUMA
4 CRMA
2 GND
6 GND
MINDIN4-41-GP

22.10021.J11

<11> M_LUMA
<47> NV_LUMA

R143 UMA 0R2J-2-GP TV_LUMA_R
R62 DIS 0R2J-2-GP

L27
C575 BLM18BB470SN1-GP C574
R373 150R2F-1-GP
SC10P50V2JN-4GP
SC10P50V2JN-4GP

Place this 2 resistors close to the TV-out connector

D14
3D3V_S0
TV_LUMA
DY
BAV99-7-F-GP
C6 SCD1U16V2ZY-2GP DY

D3
3D3V_S0
TV_CRMA
DY
BAV99-7-F-GP
C7 SCD1U16V2ZY-2GP DY

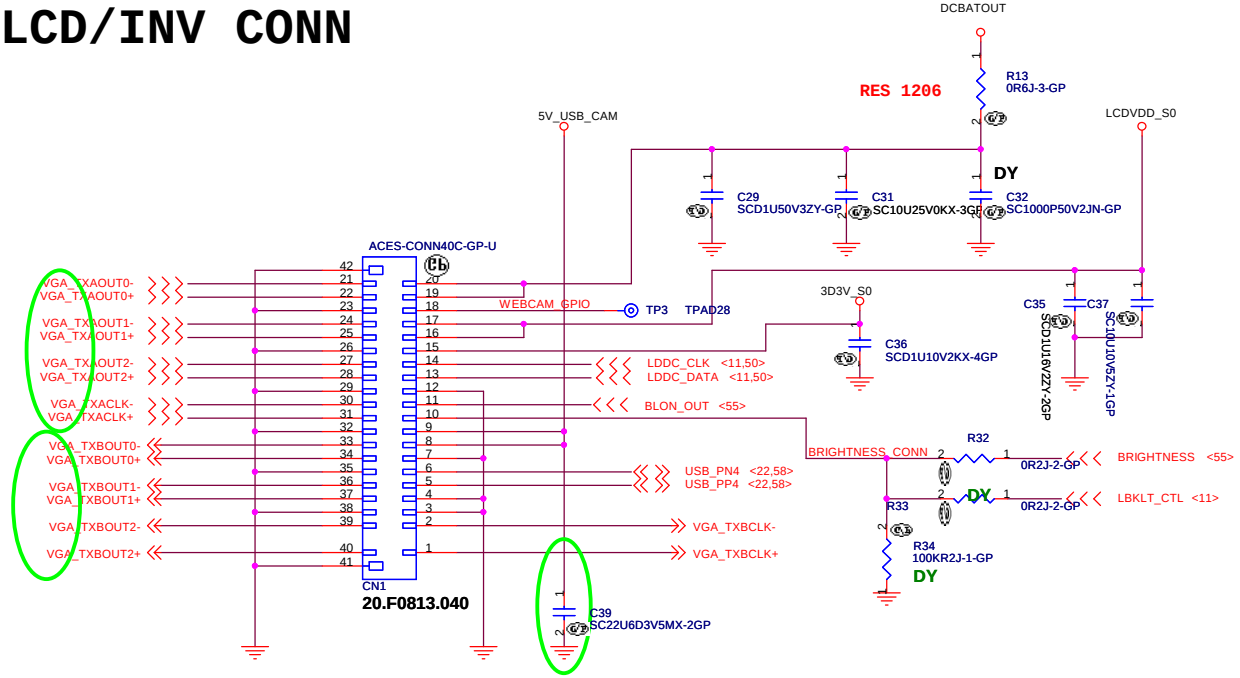
<Core Design>

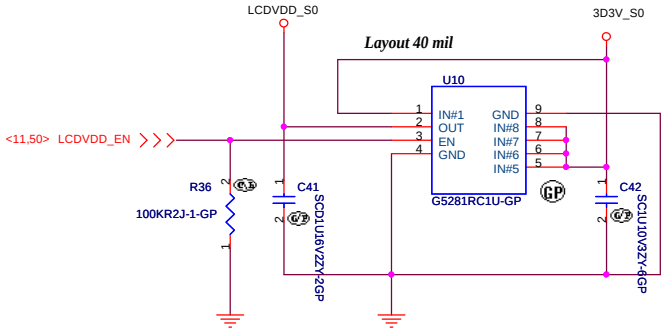
緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

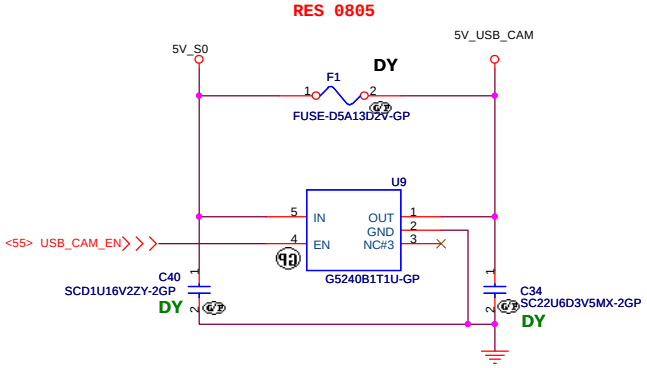
Title: TV Connector
Size: A4
Document Number: Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 18 of

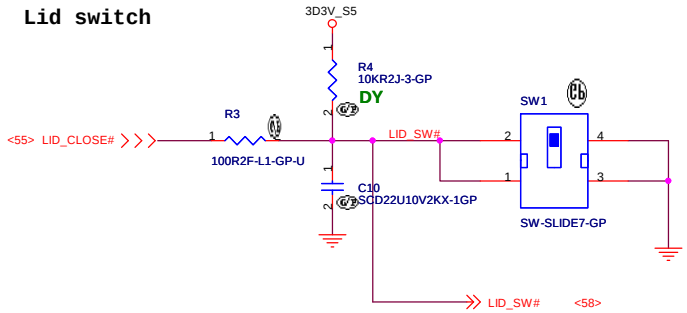
LED / INVERTER INTERFACE

LCD/INV CONN

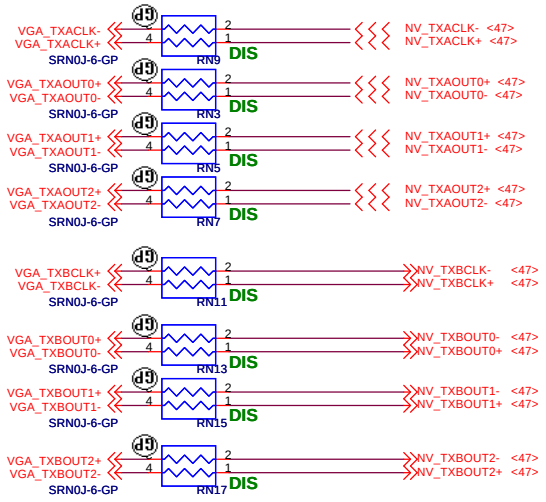




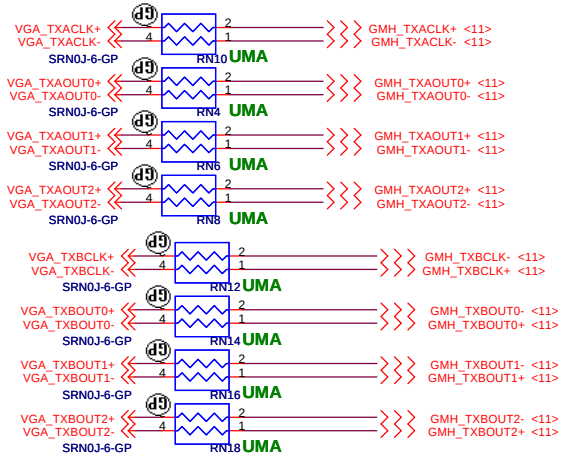




ATI LVDS INTERFACE



UMA LVDS INTERFACE



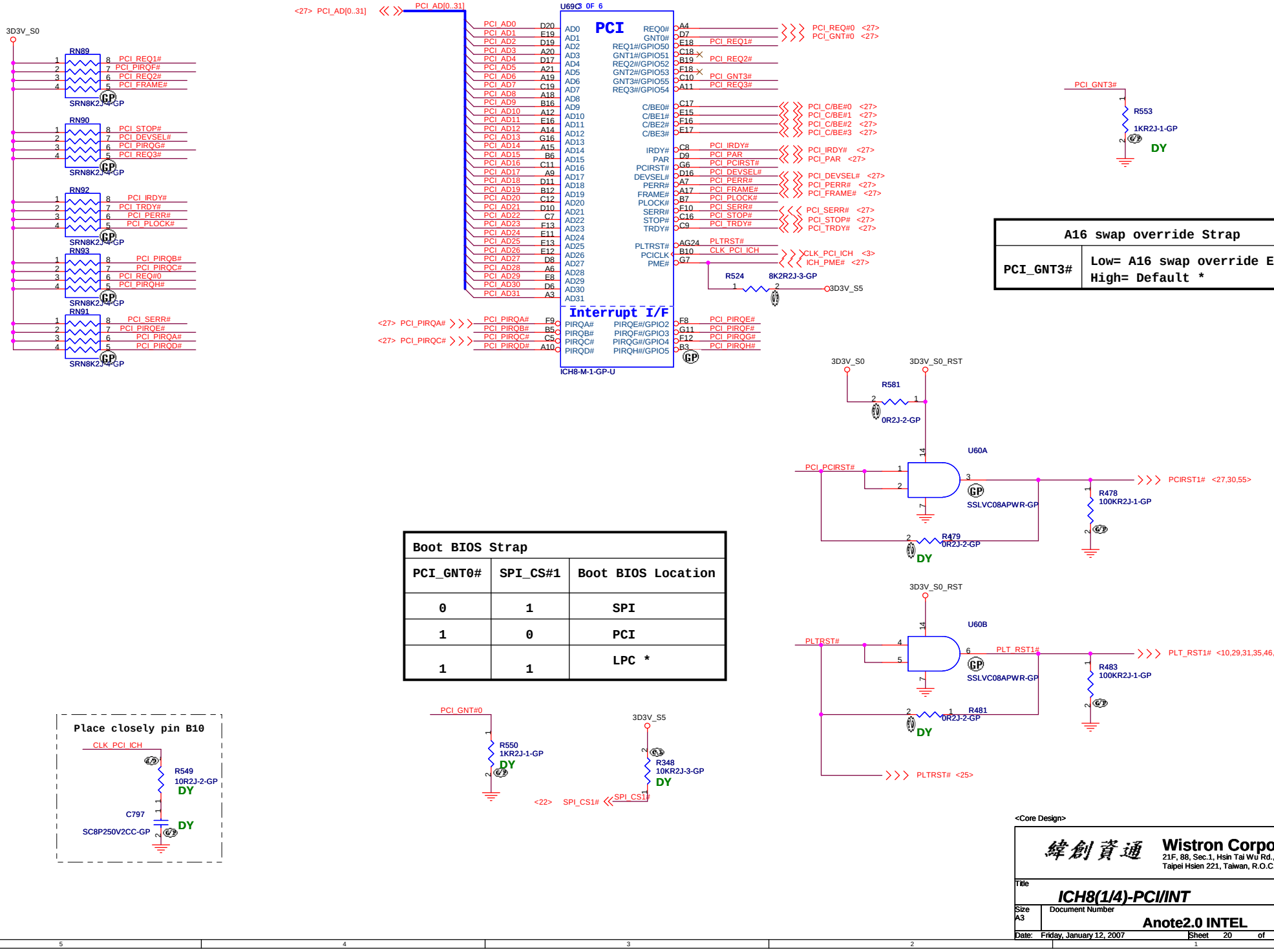
<Core Design>

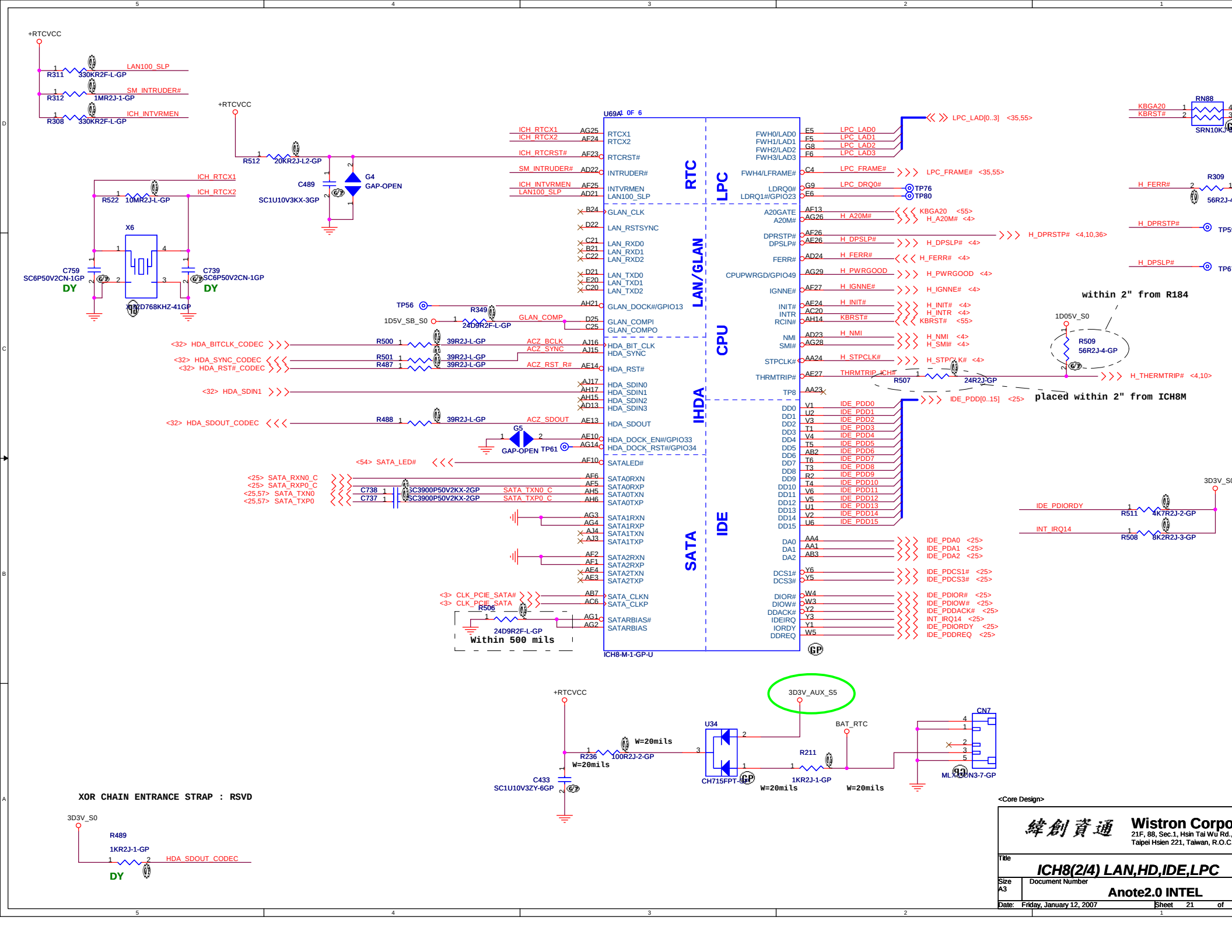
緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

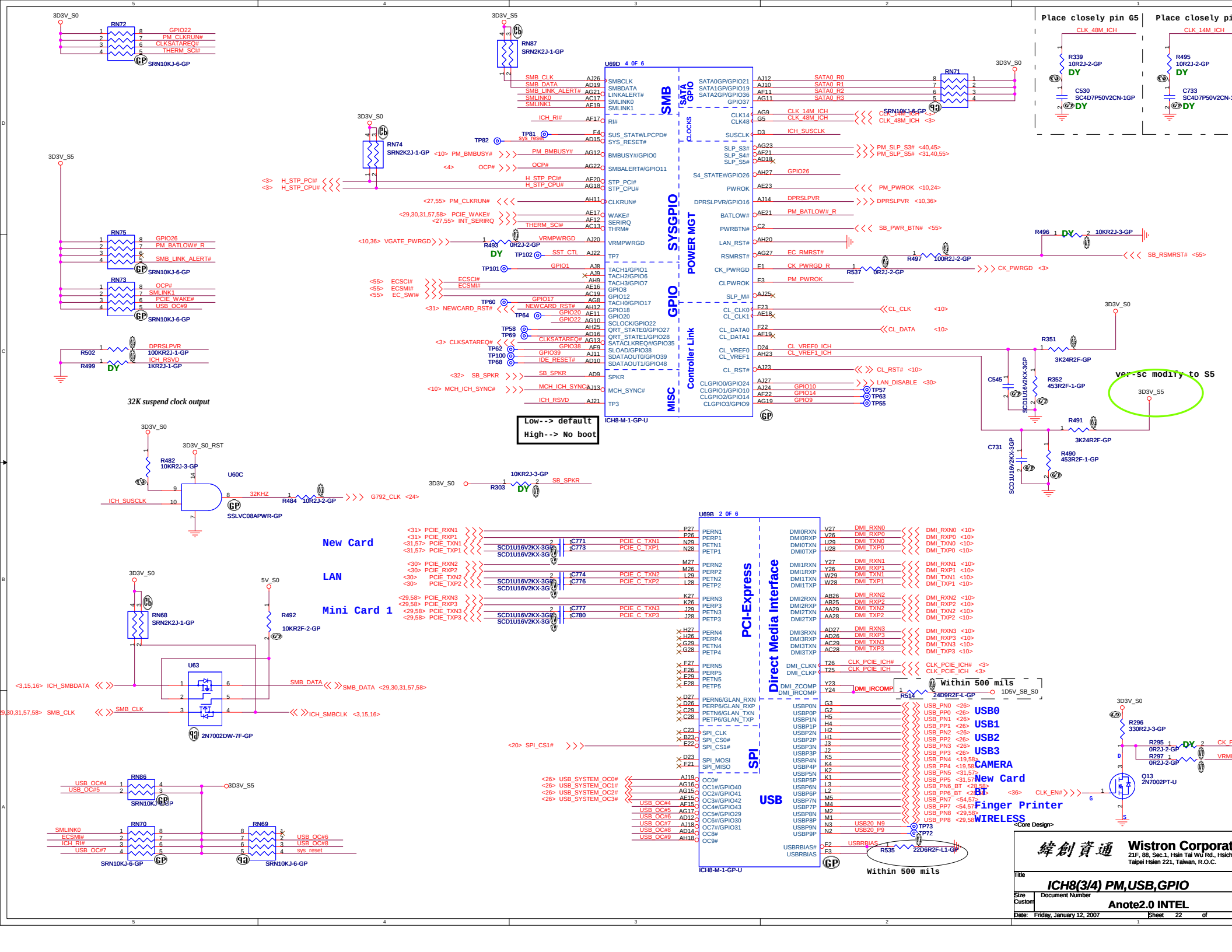
Title: LCD/Inverter Connector

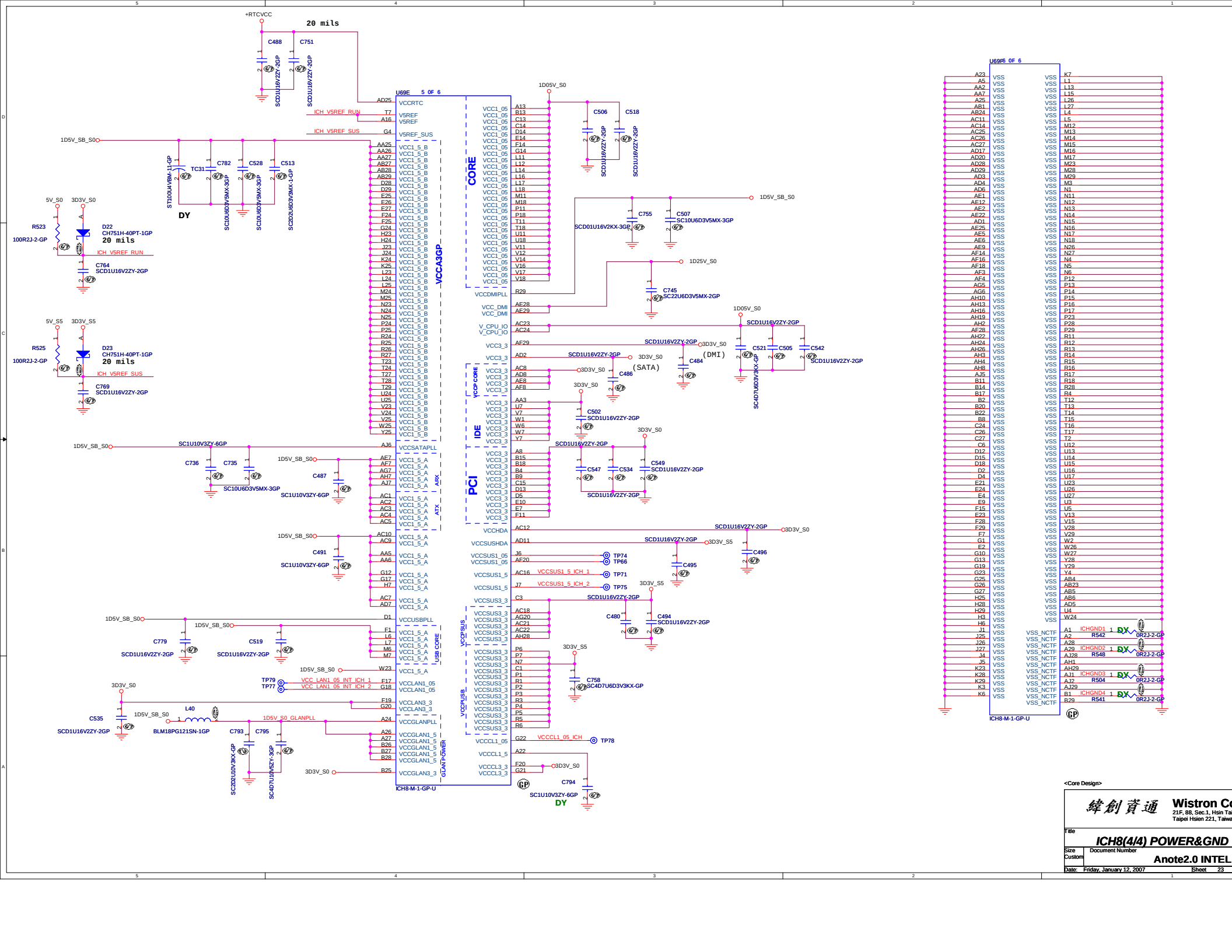
Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 19 of


3D3V_S0
RN89
PCI_REQ1#
PCI_PIRQF#
PCI_REQ2#
PCI_FRAME#
SRN8K2J-1-GP
RN90
PCI_STOP#
PCI_DEVSEL#
PCI_PIRQG#
PCI_REQ3#
SRN8K2J-1-GP
RN92
PCI_IRDY#
PCI_TRDY#
PCI_PERR#
PCI_PLOCK#
SRN8K2J-1-GP
RN93
PCI_PIRQB#
PCI_PIRQC#
PCI_REQ#0
PCI_PIRQH#
SRN8K2J-1-GP
RN91
PCI_SERR#
PCI_PIRQE#
PCI_PIRQA#
PCI_PIRQD#
SRN8K2J-1-GP
<27> PCI_AD[0..31]
PCI_AD[0..31]
U69C3 0F 6
PCI
PCI_AD0 D20
PCI_AD1 E19
PCI_AD2 D19
PCI_AD3 A20
PCI_AD4 D17
PCI_AD5 A21
PCI_AD6 A19
PCI_AD7 C19
PCI_AD8 A18
PCI_AD9 B16
PCI_AD10 A12
PCI_AD11 E16
PCI_AD12 A14
PCI_AD13 G16
PCI_AD14 A15
PCI_AD15 B6
PCI_AD16 C11
PCI_AD17 A9
PCI_AD18 D11
PCI_AD19 B12
PCI_AD20 C12
PCI_AD21 D10
PCI_AD22 C7
PCI_AD23 F13
PCI_AD24 E11
PCI_AD25 F13
PCI_AD26 E12
PCI_AD27 D8
PCI_AD28 A6
PCI_AD29 E8
PCI_AD30 D6
PCI_AD31 A3
REQ0# A4
GNT0# D7
REQ1#/GPIO50 E18
GNT1#/GPIO51 C18
REQ2#/GPIO52 B19
GNT2#/GPIO53 E18
GNT3#/GPIO55 C10
REQ3#/GPIO54 A11
C/BE0# C17
C/BE1# E15
C/BE2# F16
C/BE3# E17
IRDY# C8
PAR D9
PCIRST# G6
DEVSEL# D16
PERR# A7
FRAME# A17
PLOCK# B7
SERR# F10
STOP# C16
TRDY# C9
PLTRST# AG24
PCICLK B10
PME# G7
PCI_REQ#0 <27>
PCI_GNT#0 <27>
PCI_REQ1#
PCI_REQ2#
PCI_GNT3#
PCI_REQ3#
PCI_C/BE#0 <27>
PCI_C/BE#1 <27>
PCI_C/BE#2 <27>
PCI_C/BE#3 <27>
PCI_IRDY# <27>
PCI_PAR <27>
PCI_PCIRST#
PCI_DEVSEL# <27>
PCI_PERR# <27>
PCI_FRAME# <27>
PCI_PLOCK#
PCI_SERR# <27>
PCI_STOP# <27>
PCI_TRDY# <27>
CLK_PCI_ICH <3>
ICH_PME# <27>
R524 8K2R2J-3-GP
3D3V_S5
Interrupt I/F
<27> PCI_PIRQA#
<27> PCI_PIRQC#
PIRQA# F9
PIRQB# B5
PIRQC# C5
PIRQD# A10
PIRQE#/GPIO2 F8
PIRQF#/GPIO3 G11
PIRQG#/GPIO4 F12
PIRQH#/GPIO5 B3
PCI_PIRQE#
PCI_PIRQF#
PCI_PIRQG#
PCI_PIRQH#
ICH8-M-1-GP-U
PCI_GNT3#
R553
1KR2J-1-GP
DY
A16 swap override Strap
PCI_GNT3#
Low= A16 swap override E
High= Default *
3D3V_S0
3D3V_S0_RST
R581
0R2J-2-GP
U60A
PCI_PCIRST#
SSLVC08APWR-GP
PCIRST1# <27,30,55>
R478
100KR2J-1-GP
R479
0R2J-2-GP
DY
3D3V_S0_RST
U60B
PLTRST#
PLT_RST1#
SSLVC08APWR-GP
PLT_RST1# <10,29,31,35,46,
R483
100KR2J-1-GP
R481
0R2J-2-GP
DY
PLTRST# <25>
Boot BIOS Strap
PCI_GNT0#
SPI_CS1#
Boot BIOS Location
0
1
SPI
1
0
PCI
1
1
LPC *
PCI_GNT#0
R550
1KR2J-1-GP
DY
3D3V_S5
R348
10KR2J-3-GP
DY
<22> SPI_CS1#
SPI_CS1#
Place closely pin B10
CLK_PCI_ICH
R549
10R2J-2-GP
DY
C797
SC8P250V2CC-GP
DY
<Core Design>
緯創資通
Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(1/4)-PCI/INT
Size
A3
Document Number
Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 20 of


+RTCVCC
R311 330KR2F-L-GP
LAN100_SLP
R312 1MR2J-1-GP
SM_INTRUDER#
R308 330KR2F-L-GP
ICH_INTVRMEN
R512 20KR2J-L2-GP
C489 SC1U10V3KX-3GP
G4 GAP-OPEN
ICH_RTCX1
ICH_RTCX2
R522 10MR2J-L-GP
X6
X32D768KHZ-41GP
C759 SC6P50V2CN-1GP DY
C739 SC6P50V2CN-1GP DY
U69A 1 OF 6
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
RTC
LAN/GLAN
IHDA
SATA
LPC
CPU
IDE
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
ICH8-M-1-GP-U
LPC_LAD[0..3] <35,55>
LPC_FRAME# <35,55>
TP76
TP80
KBGA20 <55>
H_A20M# <4>
H_DPRSTP# <4,10,36>
H_DPSLP# <4>
H_FERR# <4>
H_PWRGOOD <4>
H_IGNNE# <4>
H_INIT# <4>
H_INTR <4>
KBRST# <55>
H_NMI <4>
H_SMI# <4>
H_STPCLK# <4>
H_THERMTRIP# <4,10>
IDE_PDD[0..15] <25>
IDE_PDA0 <25>
IDE_PDA1 <25>
IDE_PDA2 <25>
IDE_PDCS1# <25>
IDE_PDCS3# <25>
IDE_PDIOR# <25>
IDE_PDIOW# <25>
IDE_PDDACK# <25>
INT_IRQ14 <25>
IDE_PDIORDY <25>
IDE_PDDREQ <25>
RN88
SRN10KJ-6-GP
R309 56R2J-4-GP
TP5
TP6
within 2" from R184
1D05V_S0
R509 56R2J-4-GP
R507 24R2J-GP
placed within 2" from ICH8M
3D3V_S0
R511 4K7R2J-2-GP
R508 8K2R2J-3-GP
<32> HDA_BITCLK_CODEC
<32> HDA_SYNC_CODEC
<32> HDA_RST#_CODEC
<32> HDA_SDIN1
<32> HDA_SDOUT_CODEC
R500 39R2J-L-GP
R501 39R2J-L-GP
R487 39R2J-L-GP
R488 39R2J-L-GP
ACZ_BCLK
ACZ_SYNC
ACZ_RST_R#
ACZ_SDOUT
TP56
R349 24D9R2F-L-GP
1D5V_SB_S0
GLAN_COMP
G5 GAP-OPEN
TP61
<54> SATA_LED#
<25> SATA_RXN0_C
<25> SATA_RXP0_C
<25,57> SATA_TXN0
<25,57> SATA_TXP0
C738 SC3900P50V2KX-2GP
C737 SC3900P50V2KX-2GP
SATA_TXN0_C
SATA_TXP0_C
<3> CLK_PCIE_SATA#
<3> CLK_PCIE_SATA
R506 24D9R2F-L-GP
Within 500 mils
+RTCVCC
3D3V_AUX_S5
R236 100R2J-2-GP
W=20mils
C433 SC1U10V3ZY-6GP
U34 CH715FPT-GP
R211 1KR2J-1-GP
BAT_RTC
CN7
MLX-SDN3-7-GP
XOR CHAIN ENTRANCE STRAP : RSVD
3D3V_S0
R489 1KR2J-1-GP
HDA_SDOUT_CODEC
DY
<Core Design>
緯創資通
Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(2/4) LAN,HD,IDE,LPC
Size A3
Document Number
Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 21 of


Place closely pin G5
Place closely pi
CLK_48M_ICH
CLK_14M_ICH
R339 10R2J-2-GP DY
C530 SC4D7P50V2CN-1GP DY
R495 10R2J-2-GP DY
C733 SC4D7P50V2CN-1
3D3V_S0
3D3V_S5
RN72 GPIO22 PM_CLKRUN# CLKSATAREQ# THERM_SCI# SRN10KJ-6-GP
RN87 SRN2K2J-1-GP
U69D 4 OF 6
SMB_CLK AJ26 SMBCLK
SMB_DATA AD19 SMBDATA
SMB_LINK_ALERT# AG21 LINKALERT#
SMLINK0 AC17 SMLINK0
SMLINK1 AE19 SMLINK1
SMB
SATA GPIO
SATA0GP/GPIO21 AJ12 SATA0_R0
SATA1GP/GPIO19 AJ10 SATA0_R1
SATA2GP/GPIO36 AF11 SATA0_R2
GPIO37 AG11 SATA0_R3
RN71 SRN10KJ-6-GP
ICH_RI# AF17 RI#
RN74 SRN2K2J-1-GP
TP81 F4
sys_reset AD15
TP82
PM_BMBUSY# AG12 BMBUSY#/GPIO0
OCP# AG22 SMBALERT#/GPIO11
H_STP_PCI# AE20 STP_PCI#
H_STP_CPU# AG18 STP_CPU#
CLOCKS
CLK14 AG9 CLK_14M_ICH
CLK48 G5 CLK_48M_ICH
SUSCLK D3 ICH_SUSCLK
SLP_S3# AG23 PM_SLP_S3# <40,45>
SLP_S4# AF21 PM_SLP_S5# <31,40,55>
SLP_S5# AD18
S4_STATE#/GPIO26 AH27 GPIO26
PWROK AE23 PM_PWROK <10,24>
DPRSLPVR/GPIO16 AJ14 DPRSLPVR <10,36>
BATLOW# AE21 PM_BATLOW#_R
PWRBTN# C2 SB_PWR_BTN# <55>
LAN_RST# AH20
RSMRST# AG27 EC_RMRST#
CK_PWRGD E1 CK_PWRGD_R
CLPWROK E3 PM_PWROK
SLP_M# AJ25
CL_CLK0 F23 CL_CLK <10>
CL_CLK1 AE18
CL_DATA0 F22 CL_DATA <10>
CL_DATA1 AF19
CL_VREF0 D24 CL_VREF0_ICH
CL_VREF1 AH23 CL_VREF1_ICH
CL_RST# AJ23 CL_RST# <10>
CLGPIO0/GPIO24 AJ27 LAN_DISABLE <30>
CLGPIO1/GPIO10 AJ24 GPIO10
CLGPIO2/GPIO14 AF22 GPIO14
CLGPIO3/GPIO9 AG19 GPIO9
TP57 TP63 TP55
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
ICH8-M-1-GP-U
RN75 GPIO26 PM_BATLOW# R SMB_LINK_ALERT# SRN10KJ-6-GP
RN73 OCP# SMLINK1 PCIE_WAKE# USB_OC#9 SRN10KJ-6-GP
R502 100KR2J-1-GP DPRSLPVR
R499 1KR2J-1-GP DY ICH_RSVD
32K suspend clock output
TP101 GPIO1 AJ8
TP102 SST_CTL AJ22
R493 0R2J-2-GP DY VRMPWRGD AJ20
TP60 GPIO17 AG8
TP64 GPIO20 AE11
GPIO22 AG10
TP58 AH25
TP69 AD16
CLKSATAREQ# AG13
TP62 GPIO38 AF9
TP100 GPIO39 AJ11
TP68 IDE_RESET# AD10
SB_SPKR AD9
MCH_ICH_SYNC# AJ13 MCH_SYNC#
ICH_RSVD AJ21 TP3
ECSCI# AJ9
ECSMI# AE16
EC_SWI# AC19
GPIO12
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
Low--> default
High--> No boot
R496 DY 10KR2J-3-GP
R497 100R2J-2-GP
R537 0R2J-2-GP
SB_RSMRST# <55>
CK_PWRGD <3>
R351 3K24R2F-GP
C545 SCD1U16V2KX-3GP
R352 453R2F-1-GP
ver:Sc modify to S5
R491 3K24R2F-GP
C731 SCD1U16V2KX-3GP
R490 453R2F-1-GP
3D3V_S0_RST
R482 10KR2J-3-GP
U60C
ICH_SUSCLK
32KHZ
R484 10R2J-2-GP
G792_CLK <24>
SSLVC08APWR-GP
R303 DY 10KR2J-3-GP SB_SPKR
U69B 2 OF 6
PCI-Express
Direct Media Interface
New Card
LAN
Mini Card 1
PCIE_RXN1 P27
PCIE_RXP1 P26
PCIE_TXN1 N29
PCIE_TXP1 N28
C771 PCIE_C_TXN1
C773 PCIE_C_TXP1
SCD1U16V2KX-3GP
PCIE_RXN2 M27
PCIE_RXP2 M26
PCIE_TXN2 L29
PCIE_TXP2 L28
C774 PCIE_C_TXN2
C776 PCIE_C_TXP2
PCIE_RXN3 K27
PCIE_RXP3 K26
PCIE_TXN3 J29
PCIE_TXP3 J28
C777 PCIE_C_TXN3
C780 PCIE_C_TXP3
PERN4 H27
PERP4 H26
PETN4 G29
PETP4 G28
PERN5 F27
PERP5 F26
PETN5 E29
PETP5 E28
PERN6/GLAN_RXN D27
PERP6/GLAN_RXP D26
PETN6/GLAN_TXN C29
PETP6/GLAN_TXP C28
DMI0RXN V27 DMI_RXN0
DMI0RXP V26 DMI_RXP0
DMI0TXN U29 DMI_TXN0
DMI0TXP U28 DMI_TXP0
DMI1RXN Y27 DMI_RXN1
DMI1RXP Y26 DMI_RXP1
DMI1TXN W29 DMI_TXN1
DMI1TXP W28 DMI_TXP1
DMI2RXN AB26 DMI_RXN2
DMI2RXP AB25 DMI_RXP2
DMI2TXN AA29 DMI_TXN2
DMI2TXP AA28 DMI_TXP2
DMI3RXN AD27 DMI_RXN3
DMI3RXP AD26 DMI_RXP3
DMI3TXN AC29 DMI_TXN3
DMI3TXP AC28 DMI_TXP3
DMI_CLKN T26 CLK_PCIE_ICH#
DMI_CLKP T25 CLK_PCIE_ICH
DMI_ZCOMP Y23
DMI_IRCOMP Y24 DMI_IRCOMP
R514 24D9R2F-L-GP
Within 500 mils
1D5V_SB_S0
USB0
USB1
USB2
USB3
CAMERA
New Card
BT
Finger Printer
WIRELESS
USBP0N G3 USB_PN0
USBP0P G2 USB_PP0
USBP1N H5 USB_PN1
USBP1P H4 USB_PP1
USBP2N H2 USB_PN2
USBP2P H1 USB_PP2
USBP3N J3 USB_PN3
USBP3P J2 USB_PP3
USBP4N K5 USB_PN4
USBP4P K4 USB_PP4
USBP5N K2 USB_PN5
USBP5P K1 USB_PP5
USBP6N L3 USB_PN6_BT
USBP6P L2 USB_PP6_BT
USBP7N M5 USB_PN7
USBP7P M4 USB_PP7
USBP8N M2 USB_PN8
USBP8P M1 USB_PP8
USBP9N N3 USB20_N9
USBP9P N2 USB20_P9
TP73 TP72
USBRBIAS F2
USBRBIAS# F3
R535 22D6R2F-L1-GP
Within 500 mils
SPI_CLK C23
SPI_CS0# B23
SPI_CS1# E22
SPI_MOSI D23
SPI_MISO F21
SPI
USB
OC0# AJ19
OC1#/GPIO40 AG16
OC2#/GPIO41 AG15
OC3#/GPIO42 AE15
OC4#/GPIO43 AF15
OC5#/GPIO29 AG17
OC6#/GPIO30 AD12
OC7#/GPIO31 AJ18
OC8# AD14
OC9# AH18
USB_OC#4
USB_OC#5
USB_OC#6
USB_OC#7
USB_OC#8
USB_OC#9
ICH8-M-1-GP-U
R492 10KR2F-2-GP
RN68 SRN2K2J-1-GP
U63 2N7002DW-7F-GP
ICH_SMBDATA
SMB_DATA
ICH_SMBCLK
SMB_CLK
RN86 SRN10KJ-6-GP
RN70 SRN10KJ-6-GP
RN69 SRN10KJ-6-GP
SMLINK0
ECSMI#
ICH_RI#
USB_OC#7
sys_reset
R296 330R2J-3-GP
R295 0R2J-2-GP DY
R297 0R2J-2-GP
CK_P
VRMI
Q13 2N7002PT-U
CLK_EN#
<Core Design>
緯創資通
Wistron Corporat
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsich
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(3/4) PM,USB,GPIO
Size Custom
Document Number
Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 22 of



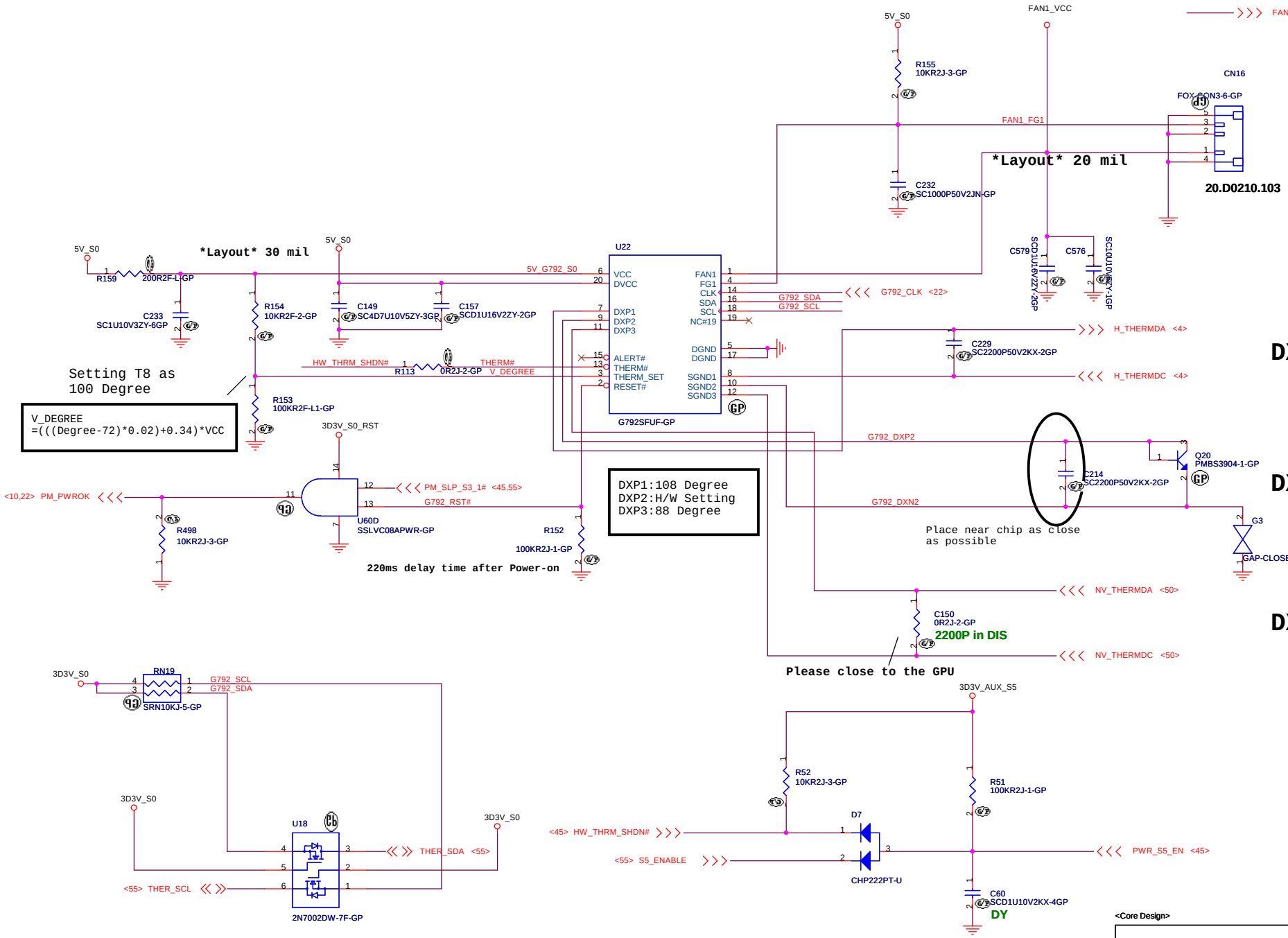
<Core Design>

Wistron Co
21F, 88, Sec.1, Hsin Ta
Taipei Hsien 221, Taiwa

Title: ICH8(4/4) POWER&GND

Size: Custom | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 23



<Core Design>

緯創資通 Wistron Corp

21F, 88, Sec.1, Hsin Tai Wu R
Taipei Hsien 221, Taiwan, R.O

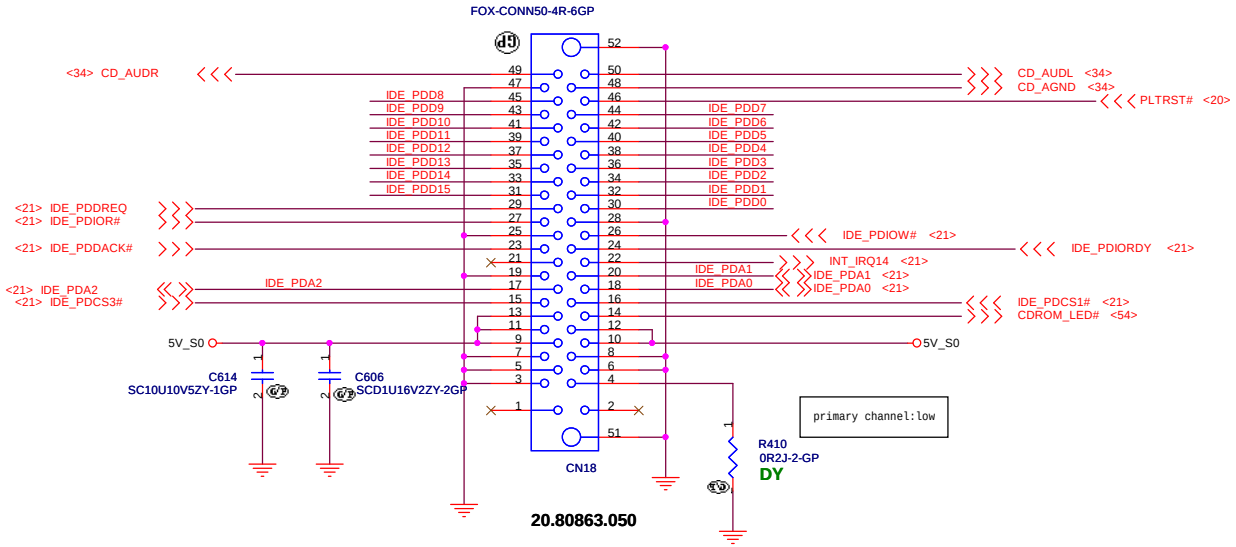
Title: Thermal/Fan Controllor G7

Size: Custom | Document Number: Anote2.0 INTEL

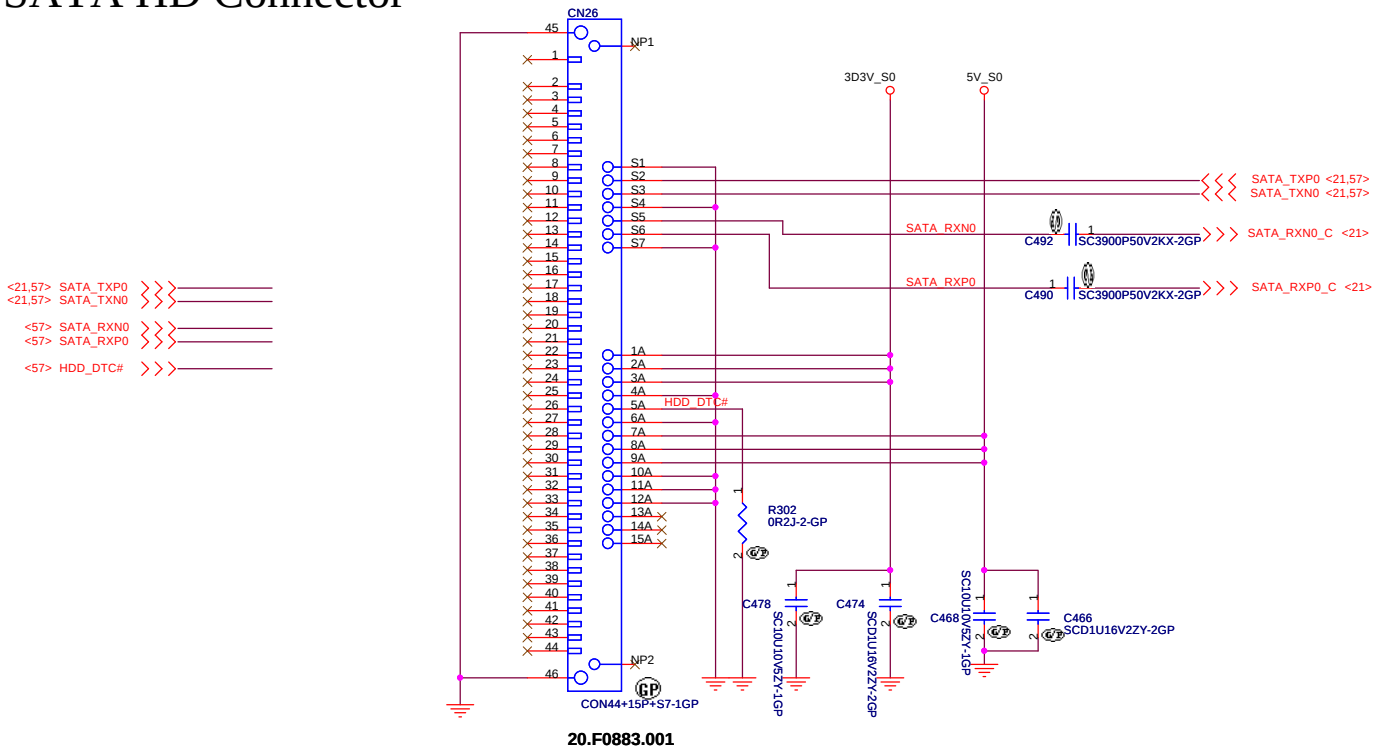
Date: Friday, January 12, 2007 | Sheet 24 of

CD-ROM CONNECTOR

Lab1 20.80346.050
Lab2 20.80863.050



SATA HD Connector



<Core Design>

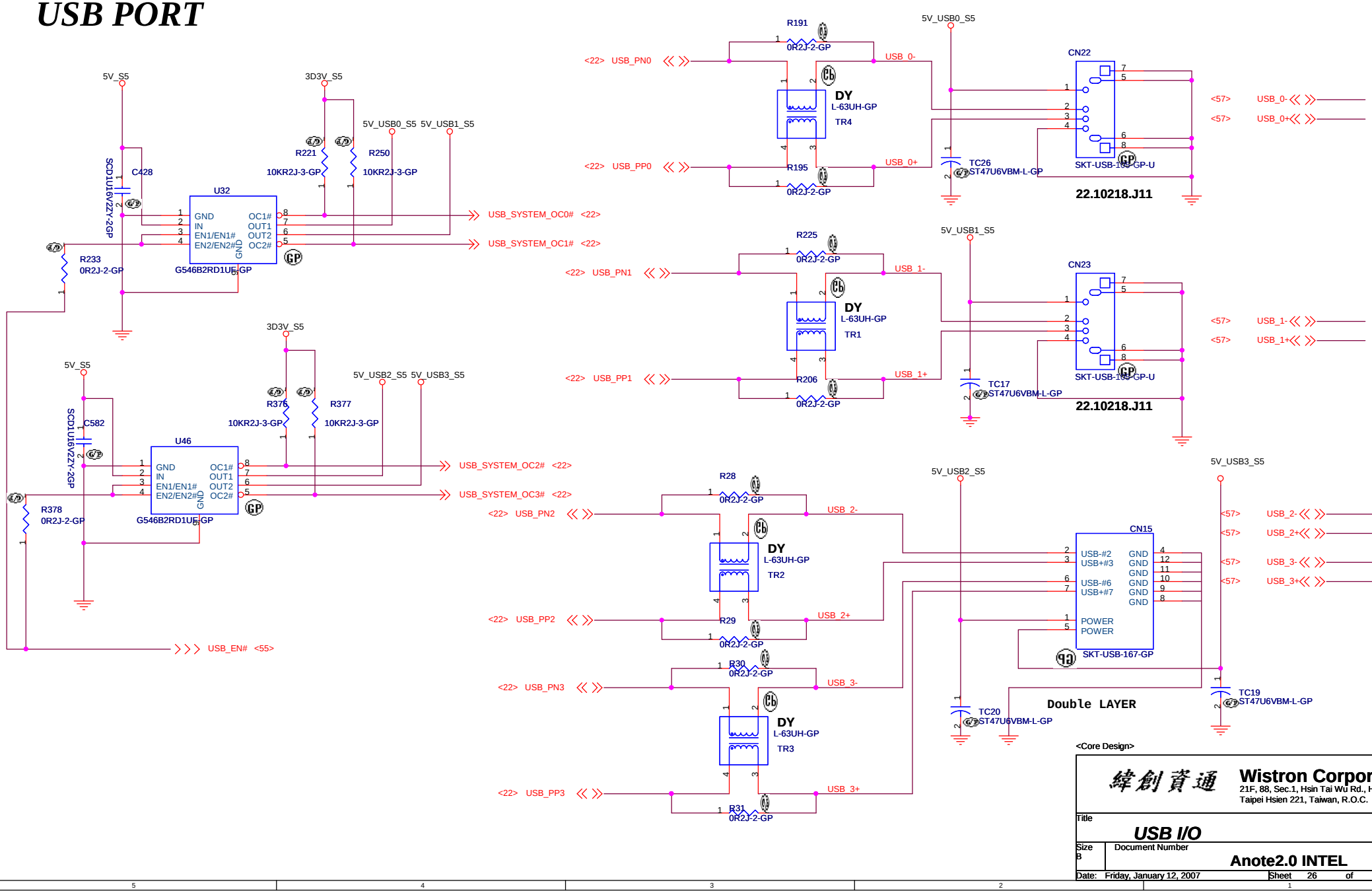
緯創資通 Wistron Corp
21F, 88, Sec.1, Hsin Tai Wu R
Taipei Hsien 221, Taiwan, R.O

Title: HD/CDROM/USB

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 25 of

USB PORT

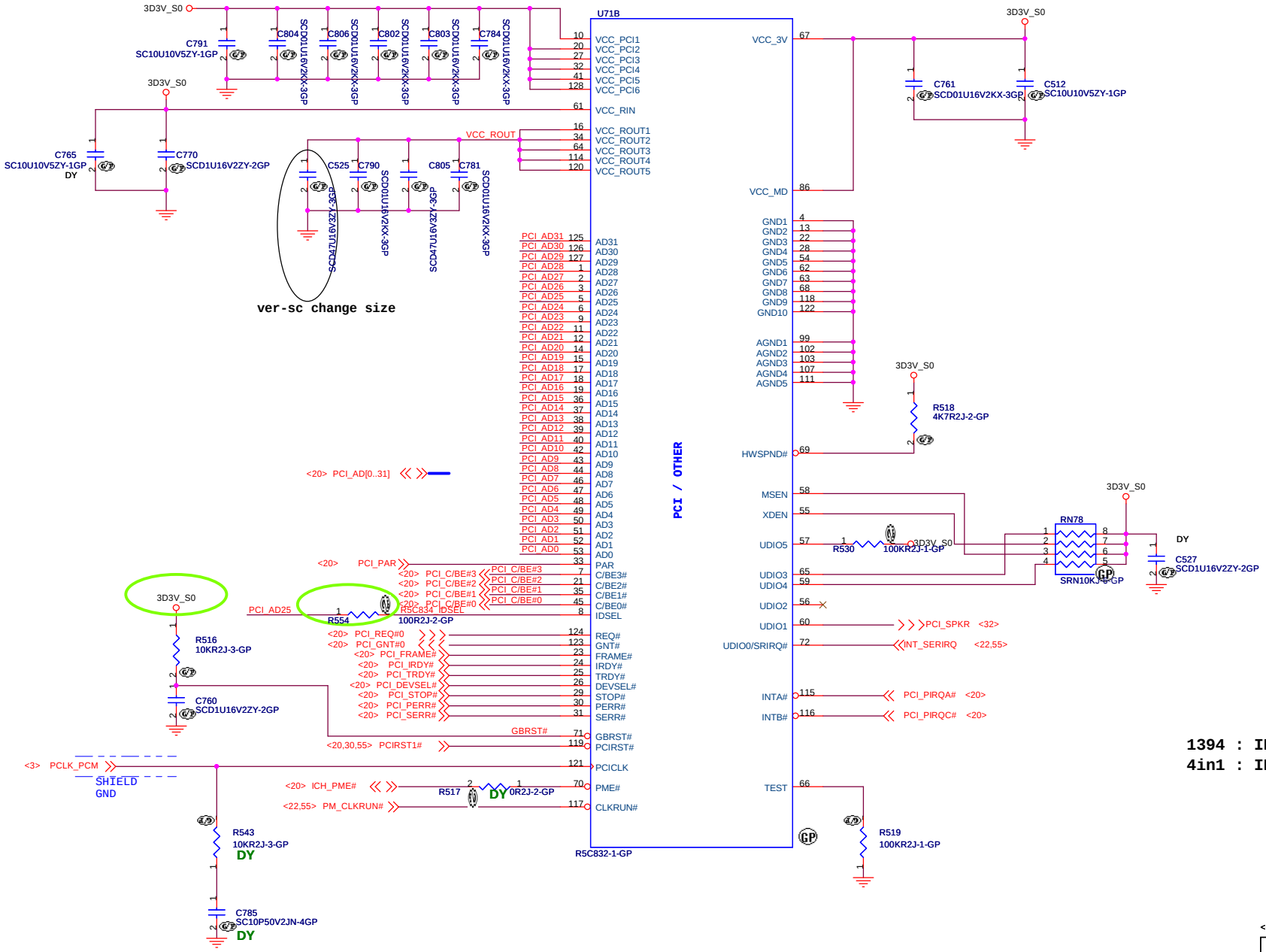


<Core Design>

緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB I/O

Size	Document Number	
B		Anote2.0 INTEL
Date: Friday, January 12, 2007	Sheet 26	of



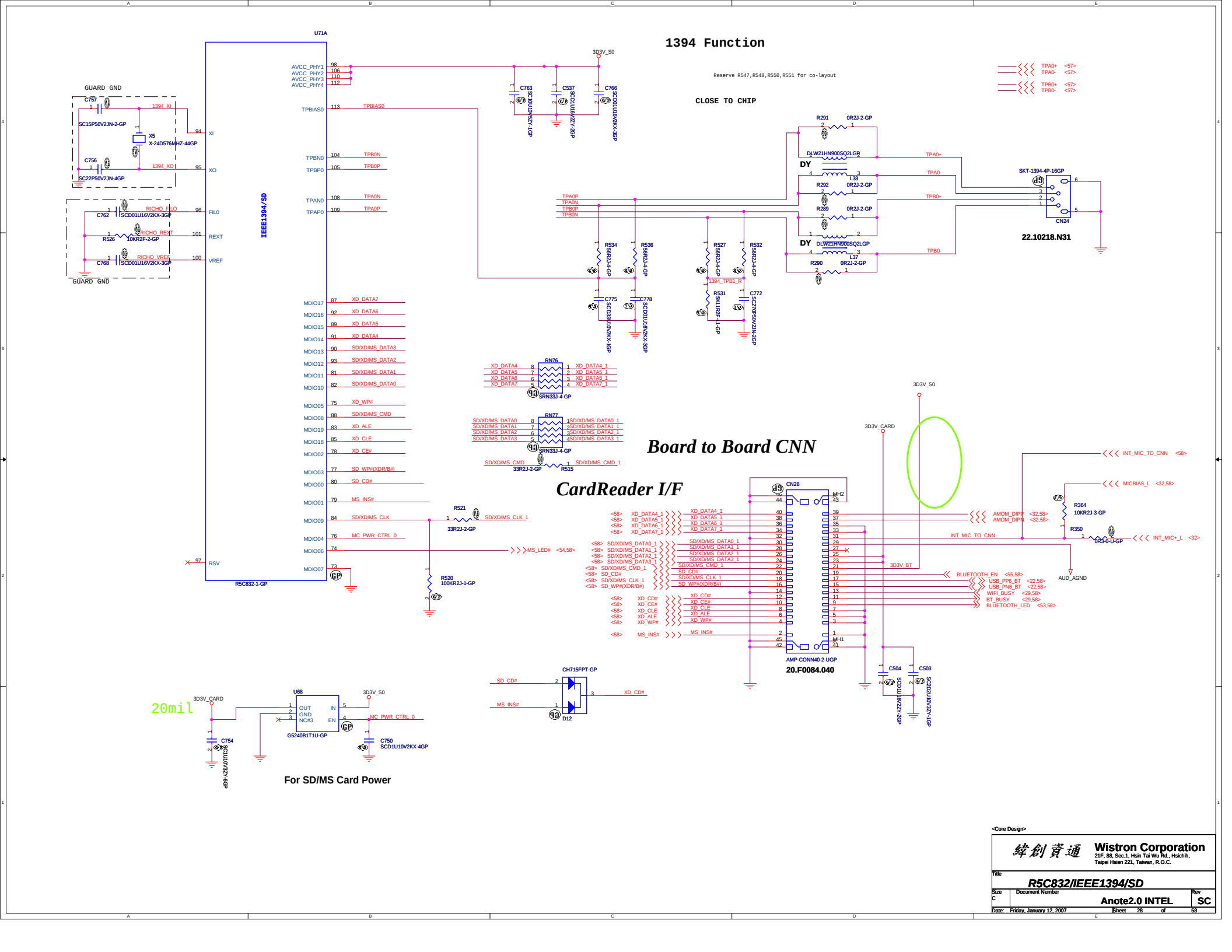
<Core Design>

Wistron Corp
21F, 88, Sec.1, Hsin Tai Wu R
Taipei Hsien 221, Taiwan, R.O

Title: R5C832/PCI

Size: A3 | Document Number: Anote2.0 INTEL

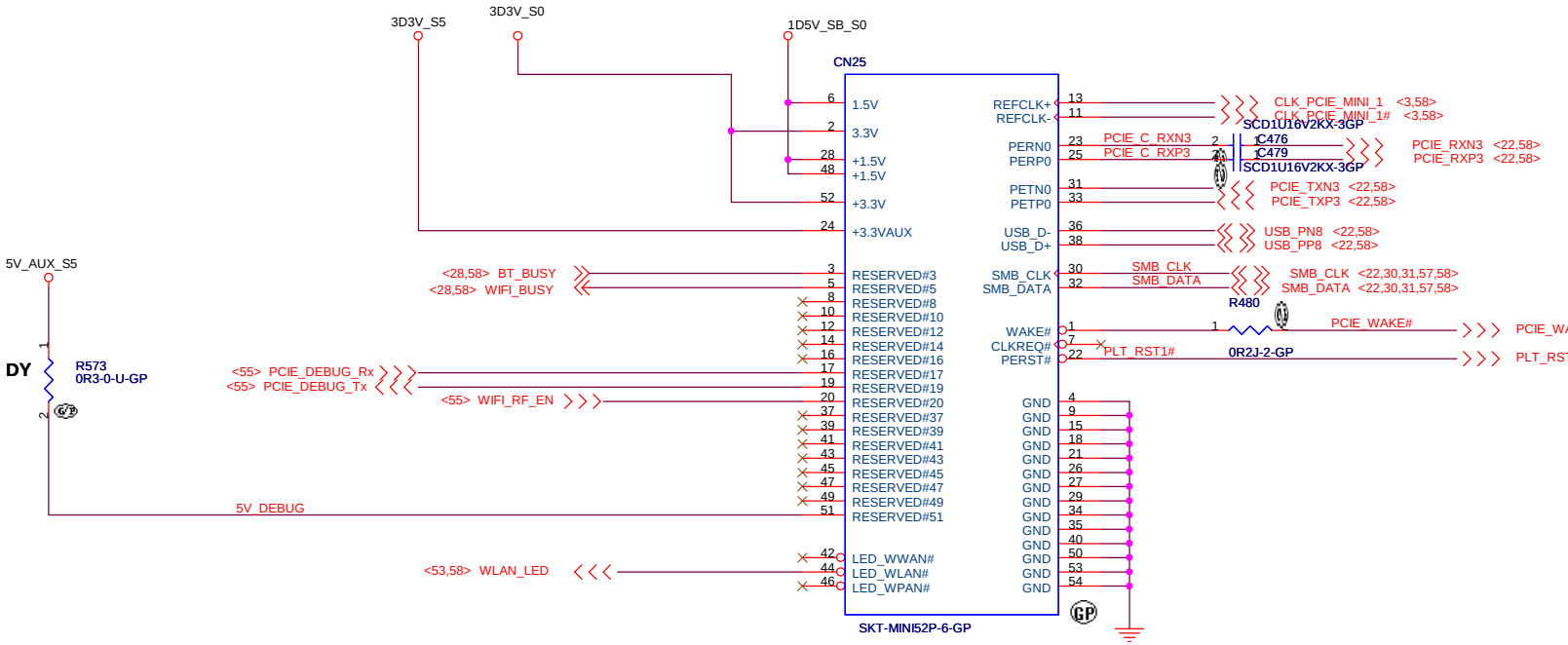
Date: Friday, January 12, 2007 | Sheet 27 of


1394 Function
Reserve R547,R548,R550,R551 for co-layout
CLOSE TO CHIP
U71A
IEEE1394/SD
R5C832-1-GP
GUARD GND
C757
1394_XI
SC15P50V2JN-2-GP
X5
X-24D576MHZ-44GP
C756
1394_XO
SC22P50V2JN-4GP
C762
RICHO_FIL0
SCD01U16V2KX-3GP
R526
10KR2F-2-GP
RICHO_REXT
C768
RICHO_VREF
SCD01U16V2KX-3GP
AVCC_PHY1
AVCC_PHY2
AVCC_PHY3
AVCC_PHY4
TPBIAS0
TPBN0
TPBP0
TPAN0
TPAP0
C763
C537
C766
SC1D0U10V2ZY-4GP
SCD01U10V2KX-3GP
R291
R292
R289
R290
0R2J-2-GP
DLW21HN900SQ2LGP
DLW21HN900SQ2LGP
DY
L38
L37
TPA0+
TPA0-
TPB0+
TPB0-
SKT-1394-4P-16GP
CN24
22.10218.N31
R534
R536
R527
R532
56R2J-4-GP
1394_TPB1_R
R531
56R1J2F-1-GP
C775
C778
C772
SC2700P50V2JN-2GP
RN76
RN77
SRN33J-4-GP
XD_DATA4_1
XD_DATA5_1
XD_DATA6_1
XD_DATA7_1
SD/XD/MS_DATA0_1
SD/XD/MS_DATA1_1
SD/XD/MS_DATA2_1
SD/XD/MS_DATA3_1
SD/XD/MS_CMD
SD/XD/MS_CMD_1
33R2J-2-GP
R515
R521
R520
100KR2J-1-GP
Board to Board CNN
CardReader I/F
3D3V_S0
3D3V_CARD
3D3V_BT
CN28
AMP-CONN40-2-UGP
20.F0084.040
INT_MIC_TO_CNN
MICBIAS_L
R364
10KR2J-3-GP
R350
0R3-0-U-GP
INT_MIC+_L
AUD_AGND
AMOM_DIPP
AMOM_DIPN
BLUETOOTH_EN
USB_PP6_BT
USB_PN6_BT
WIFI_BUSY
BT_BUSY
BLUETOOTH_LED
C504
C503
SCD1U16V2ZY-2GP
SCD1U10V2ZY-1GP
CH715FPT-GP
D12
SD_CD#
MS_INS#
XD_CD#
20mil
U68
G5240B1T1U-GP
C754
C750
SCD1U10V2KX-4GP
SCD1U10V2ZY-6GP
MC_PWR_CTRL_0
For SD/MS Card Power
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
R5C832/IEEE1394/SD
Size
C
Document Number
Anote2.0 INTEL
Rev
SC
Date: Friday, January 12, 2007
Sheet 28 of 58

Mini PCI-E Connector

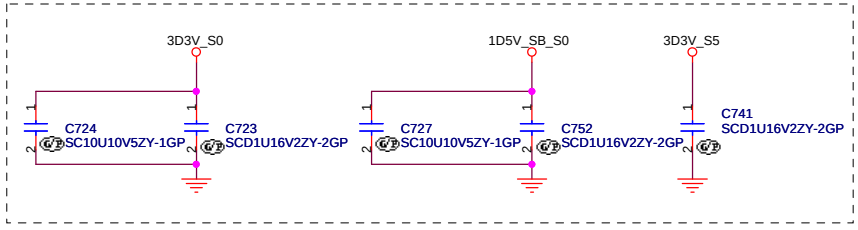
Port-1

Only port-1 support USB



62.10043.261

Note: 9/5 ME updata



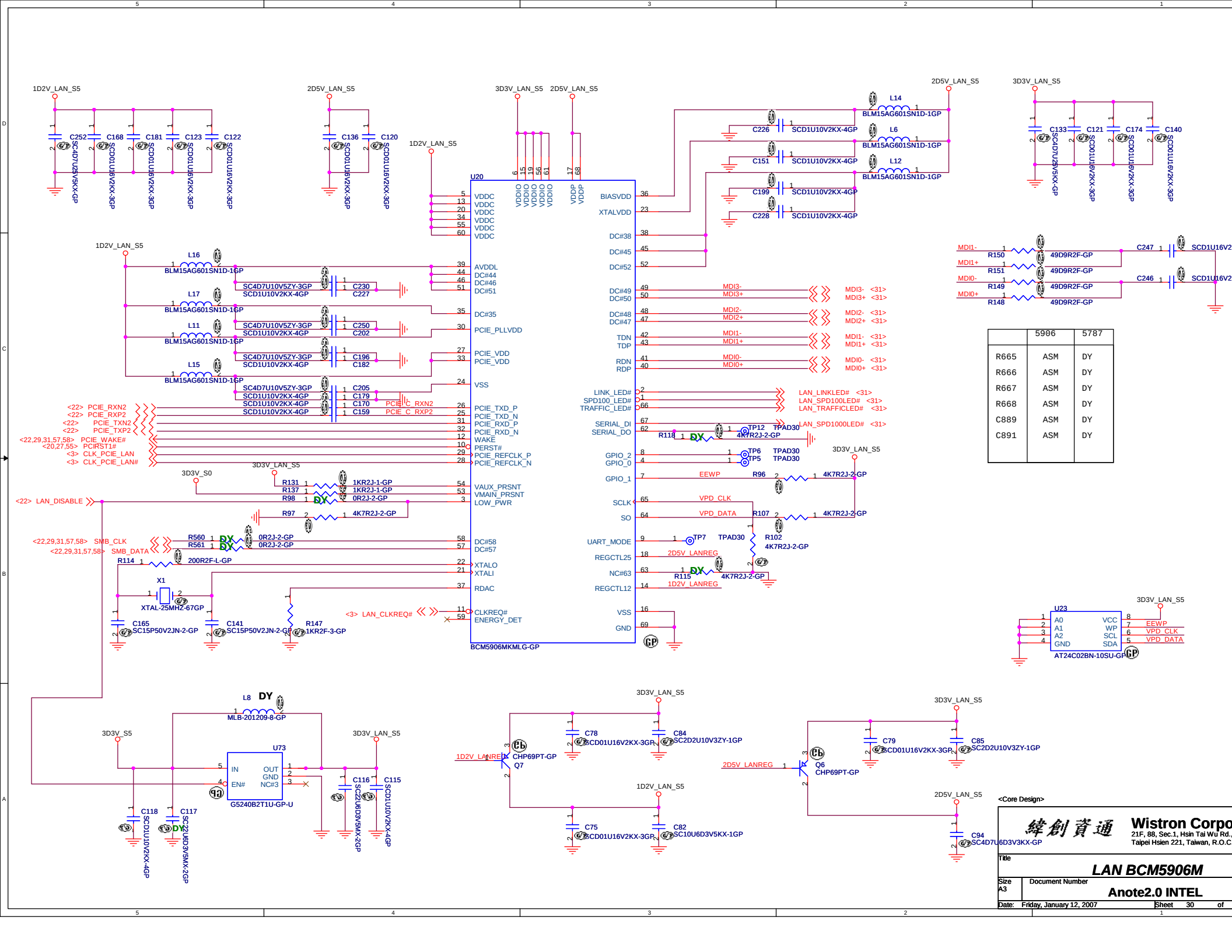
<Core Design>

緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN .

Size: B | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 29 of



	5906	5787
R665	ASM	DY
R666	ASM	DY
R667	ASM	DY
R668	ASM	DY
C889	ASM	DY
C891	ASM	DY

<Core Design>

緯創資通 Wistron Corpo

21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C.

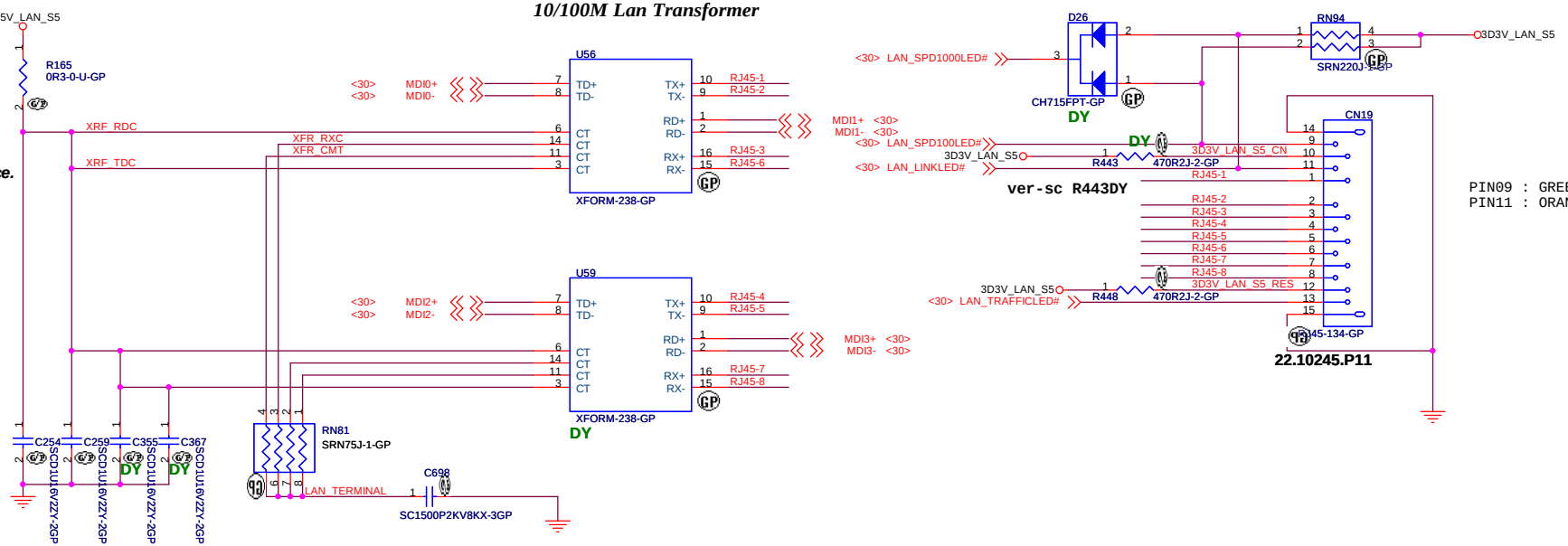
Title: LAN BCM5906M

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 30 of

10/100M Lan Transformer

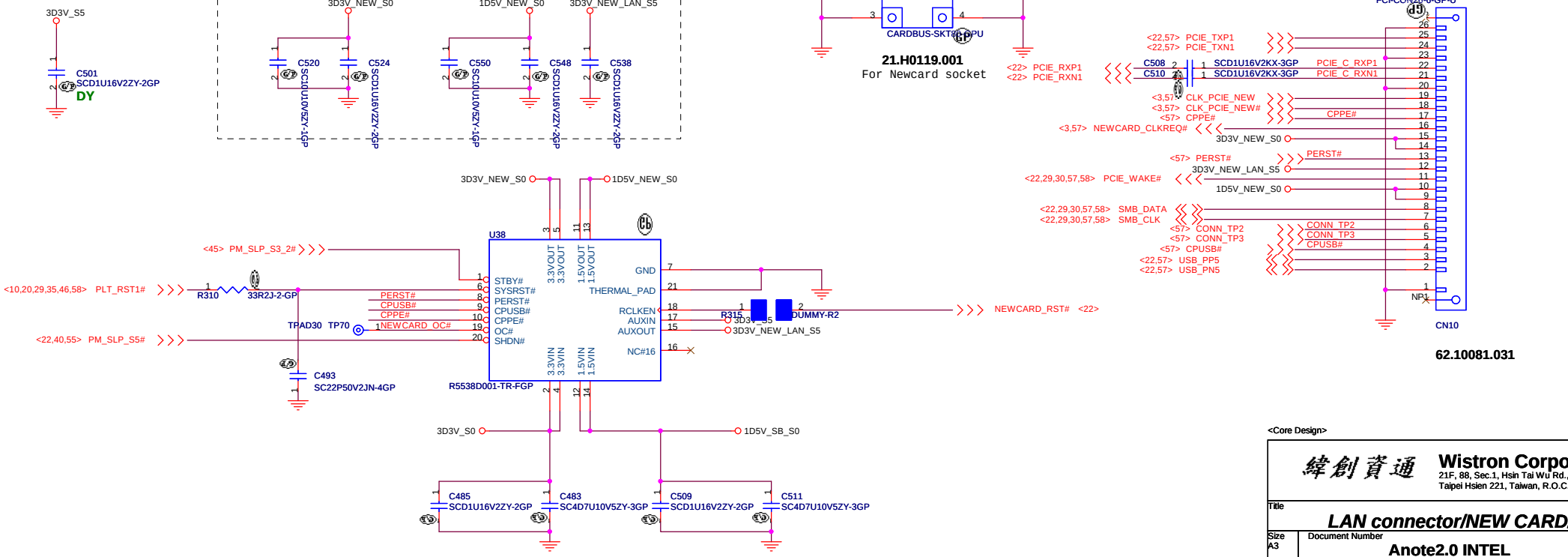
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



NEWCARD Connector

Place them Near to Chip

Place them Near to Connector



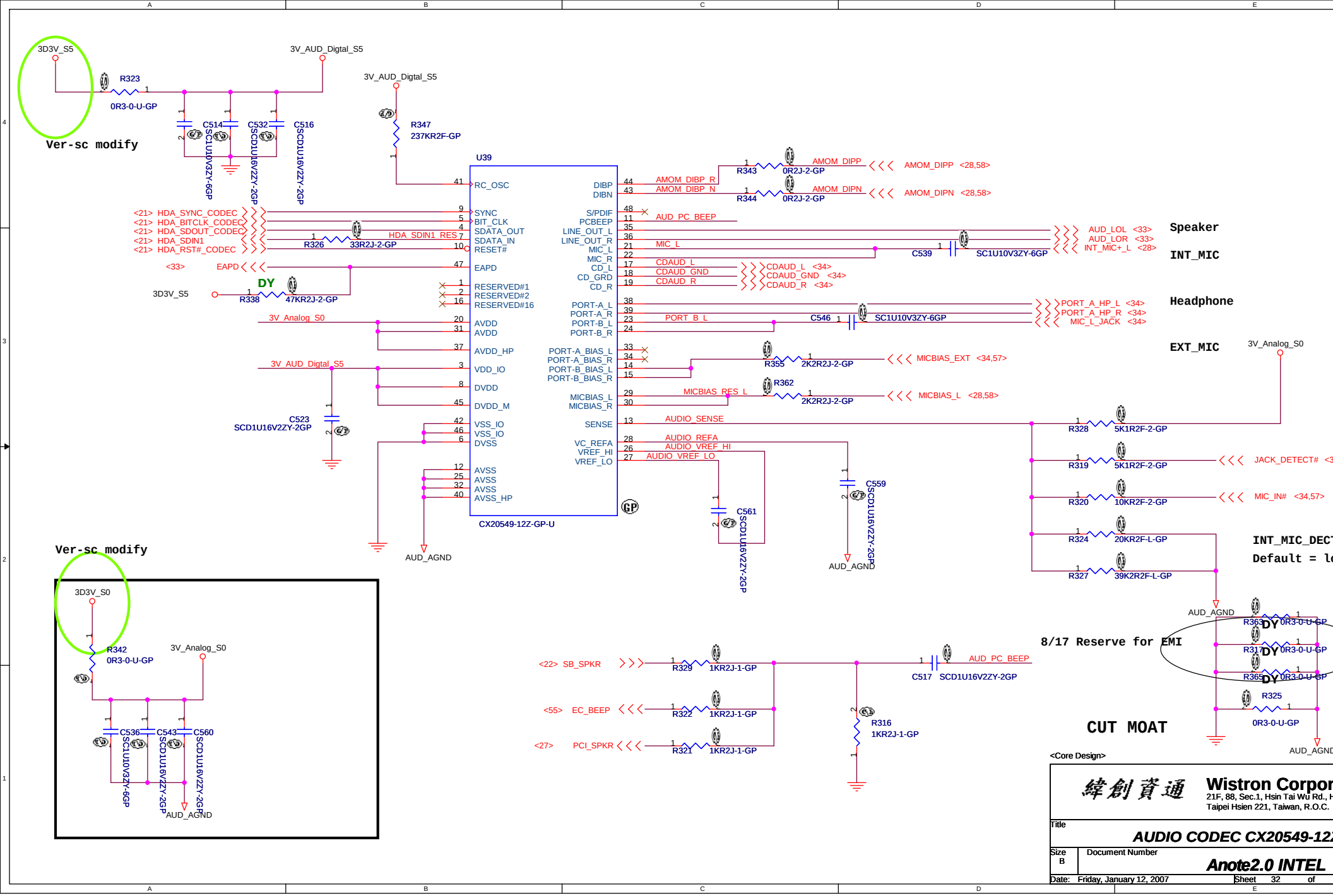
<Core Design>

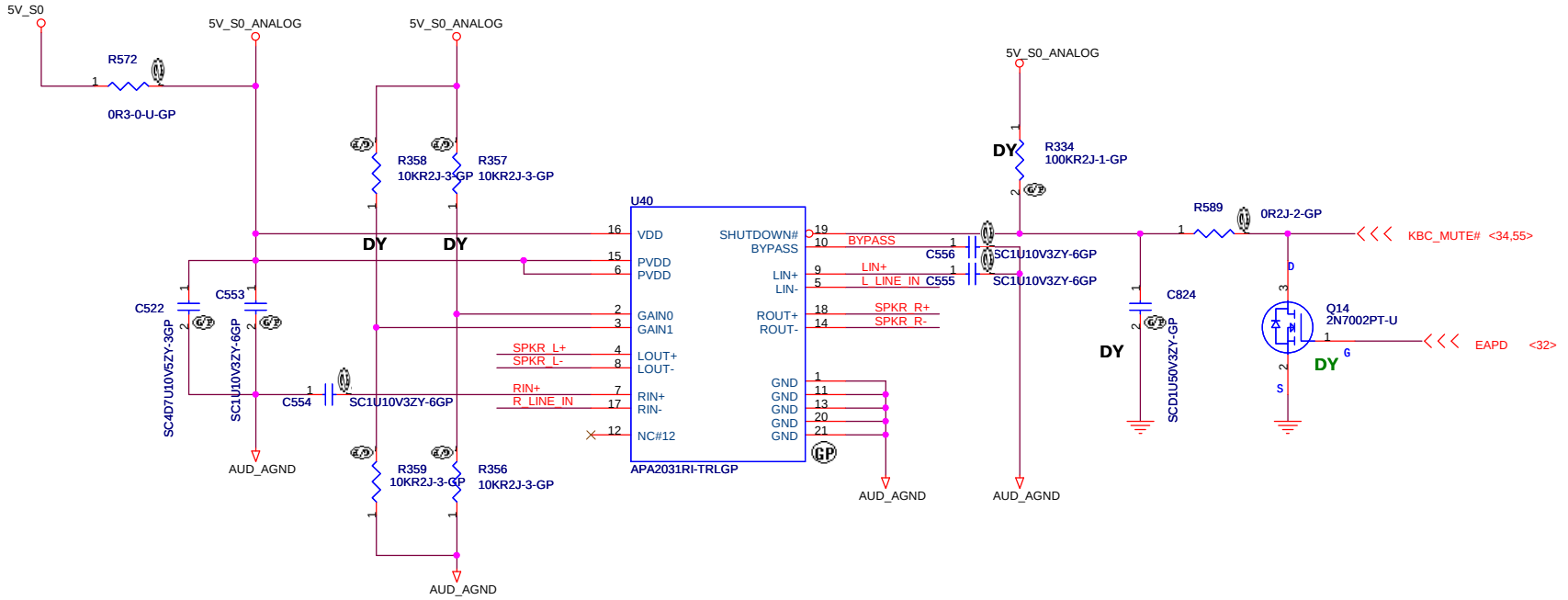
緯創資通 Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C.

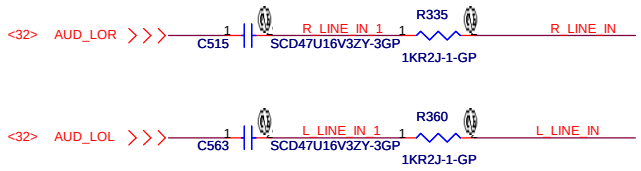
Title: LAN connector/NEW CARD

Size: A3 | Document Number: Anote2.0 INTEL

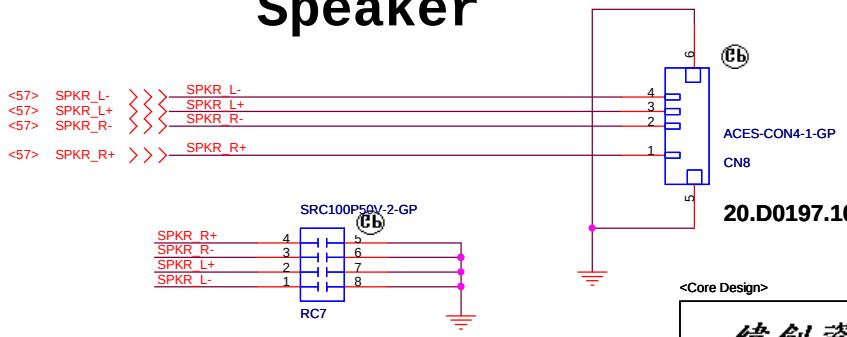
Date: Friday, January 12, 2007 | Sheet 31 of


3D3V_S5
3V_AUD_Digtal_S5
R323
0R3-0-U-GP
Ver-sc modify
C514
SC1U10V3ZY-6GP
C532
SCD1U16V2ZY-2GP
C516
SCD1U16V2ZY-2GP
R347
237KR2F-GP
U39
RC_OSC
SYNC
BIT_CLK
SDATA_OUT
SDATA_IN
RESET#
EAPD
RESERVED#1
RESERVED#2
RESERVED#16
AVDD
AVDD
AVDD_HP
VDD_IO
DVDD
DVDD_M
VSS_IO
VSS_IO
DVSS
AVSS
AVSS
AVSS
AVSS_HP
DIBP
DIBN
S/PDIF
PCBEEP
LINE_OUT_L
LINE_OUT_R
MIC_L
MIC_R
CD_L
CD_GRD
CD_R
PORT-A_L
PORT-A_R
PORT-B_L
PORT-B_R
PORT-A_BIAS_L
PORT-A_BIAS_R
PORT-B_BIAS_L
PORT-B_BIAS_R
MICBIAS_L
MICBIAS_R
SENSE
VC_REFA
VREF_HI
VREF_LO
CX20549-12Z-GP-U
<21> HDA_SYNC_CODEC
<21> HDA_BITCLK_CODEC
<21> HDA_SDOUT_CODEC
<21> HDA_SDIN1
<21> HDA_RST#_CODEC
HDA_SDIN1_RES
R326
33R2J-2-GP
<33>
EAPD
DY
R338
47KR2J-2-GP
3V_Analog_S0
3V_AUD_Digtal_S5
C523
SCD1U16V2ZY-2GP
AUD_AGND
AMOM_DIPP
AMOM_DIPN
R343
0R2J-2-GP
R344
0R2J-2-GP
AMOM_DIPP <28,58>
AMOM_DIPN <28,58>
AMOM_DIBP_R
AMOM_DIBP_N
AUD_PC_BEEP
MIC_L
CDAUD_L
CDAUD_GND
CDAUD_R
CDAUD_L <34>
CDAUD_GND <34>
CDAUD_R <34>
C539
SC1U10V3ZY-6GP
AUD_LOL <33>
AUD_LOR <33>
INT_MIC+_L <28>
Speaker
INT_MIC
PORT_B_L
C546
SC1U10V3ZY-6GP
PORT_A_HP_L <34>
PORT_A_HP_R <34>
MIC_L_JACK <34>
Headphone
EXT_MIC
R355
2K2R2J-2-GP
MICBIAS_EXT <34,57>
R362
2K2R2J-2-GP
MICBIAS_RES_L
MICBIAS_L <28,58>
AUDIO_SENSE
AUDIO_REFA
AUDIO_VREF_HI
AUDIO_VREF_LO
C561
SCD1U16V2ZY-2GP
C559
SCD1U16V2ZY-2GP
R328
5K1R2F-2-GP
R319
5K1R2F-2-GP
JACK_DETECT# <3
R320
10KR2F-2-GP
MIC_IN# <34,57>
R324
20KR2F-L-GP
R327
39K2R2F-L-GP
INT_MIC_DEC
Default = lo
8/17 Reserve for EMI
R363
0R3-0-U-GP
R317
0R3-0-U-GP
R365
0R3-0-U-GP
DY
R325
0R3-0-U-GP
CUT MOAT
<22> SB_SPKR
<55> EC_BEEP
<27> PCI_SPKR
R329
1KR2J-1-GP
R322
1KR2J-1-GP
R321
1KR2J-1-GP
R316
1KR2J-1-GP
C517
SCD1U16V2ZY-2GP
AUD_PC_BEEP
Ver-sc modify
3D3V_S0
R342
0R3-0-U-GP
3V_Analog_S0
C536
SC1U10V3ZY-6GP
C543
SCD1U16V2ZY-2GP
C560
SCD1U16V2ZY-2GP
AUD_AGND
<Core Design>
緯創資通
Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC CX20549-12
Size
B
Document Number
Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 32 of





Speaker



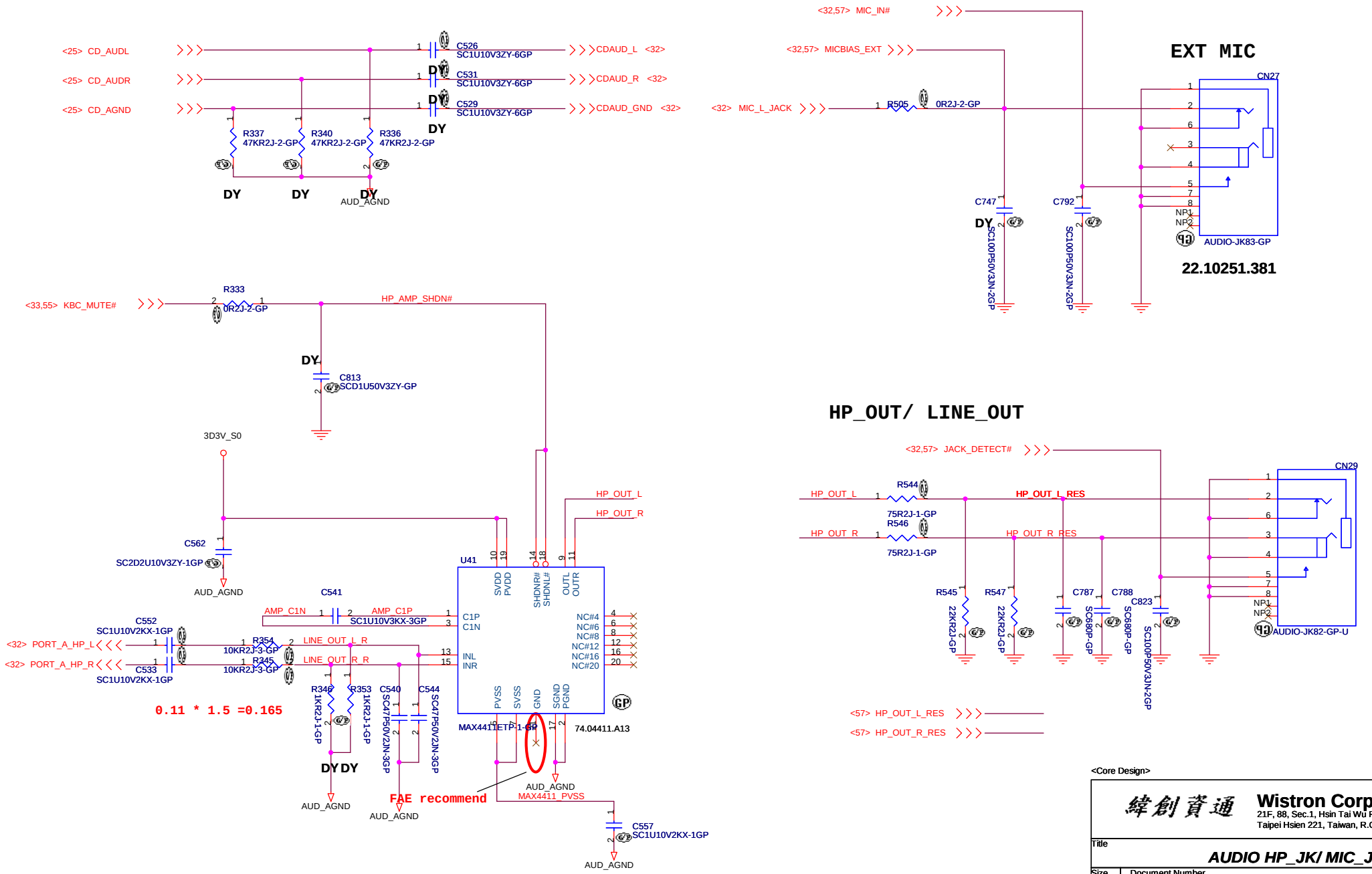
<Core Design>

緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP/SPEAKER

Size: B | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 33 of



<Core Design>

緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO HP_JK/ MIC_JK

Size: B | Document Number: Anote2.0 INTEL

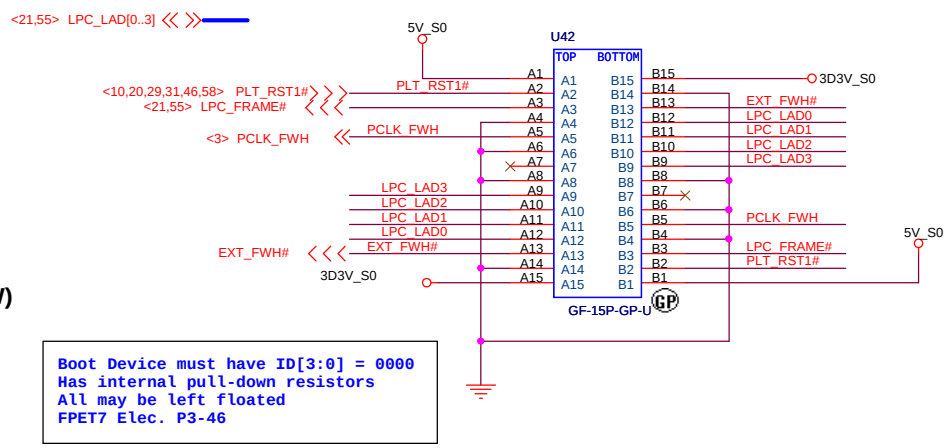
Date: Friday, January 12, 2007 | Sheet 34 of

GOLDEN FINGER FOR DEBUG BOARD

TOP VIEW

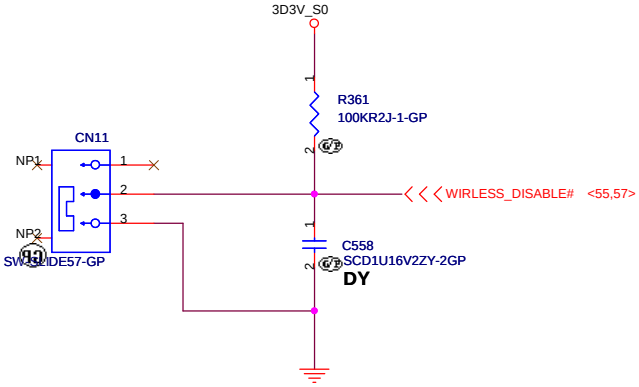
A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

WIRELESS SWITCH



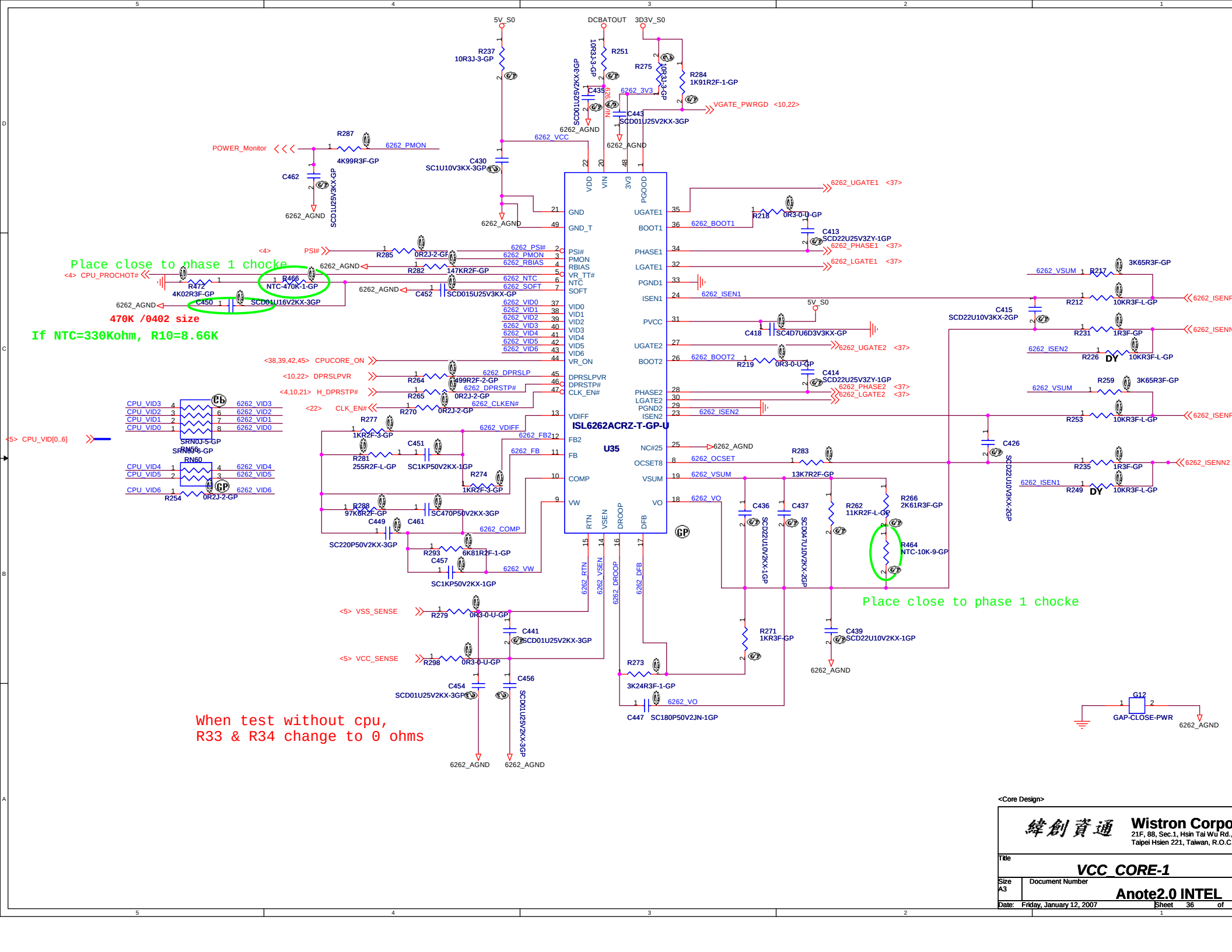
<Core Design>

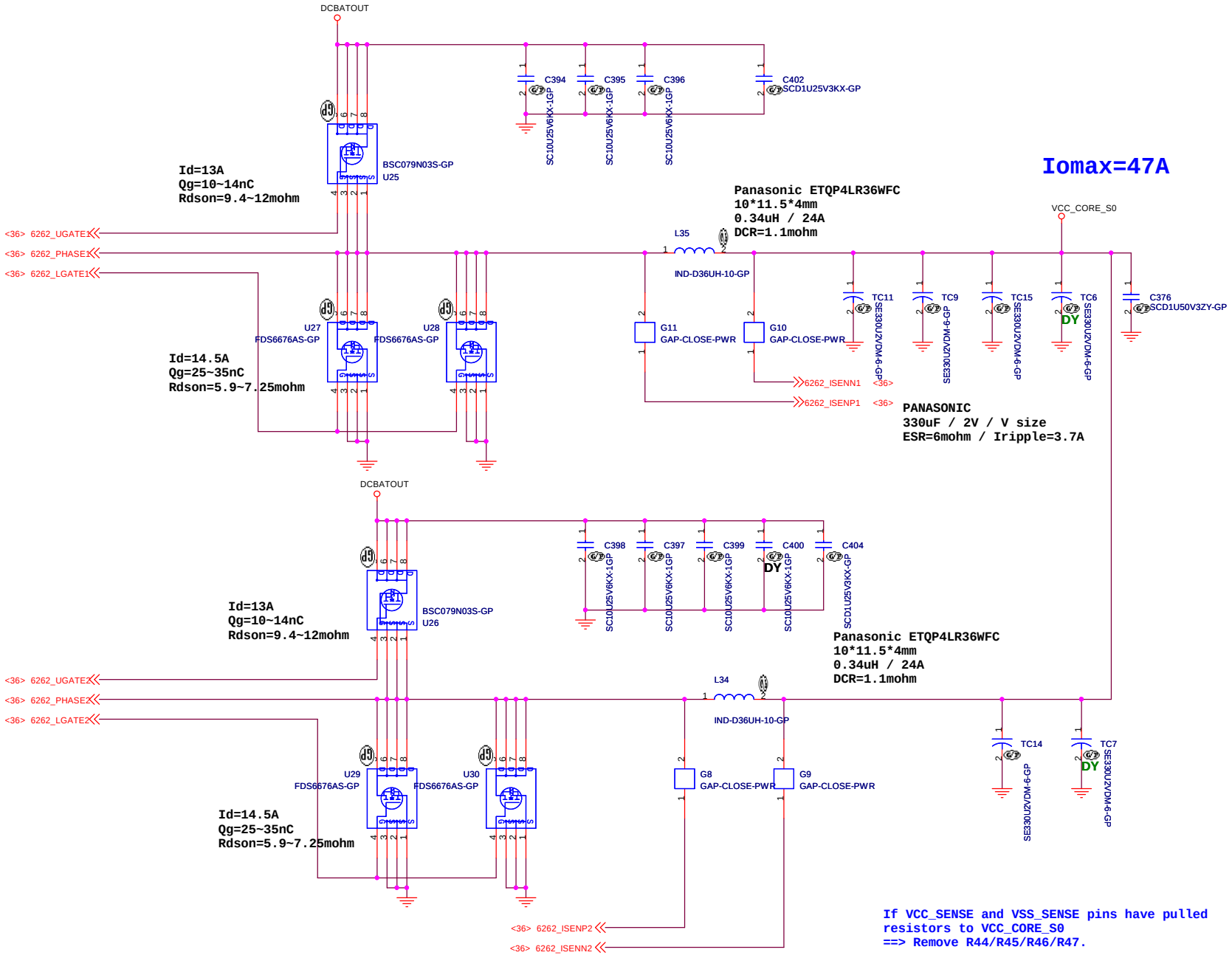
緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

Title: FWH and Debug

Size: B | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 35 of


Place close to phase 1 chocke
470K /0402 size
If NTC=330Kohm, R10=8.66K
ISL6262ACRZ-T-GP-U
U35
Place close to phase 1 chocke
When test without cpu,
R33 & R34 change to 0 ohms
<Core Design>
Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C
Title
VCC_CORE-1
Size
A3
Document Number
Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 36 of



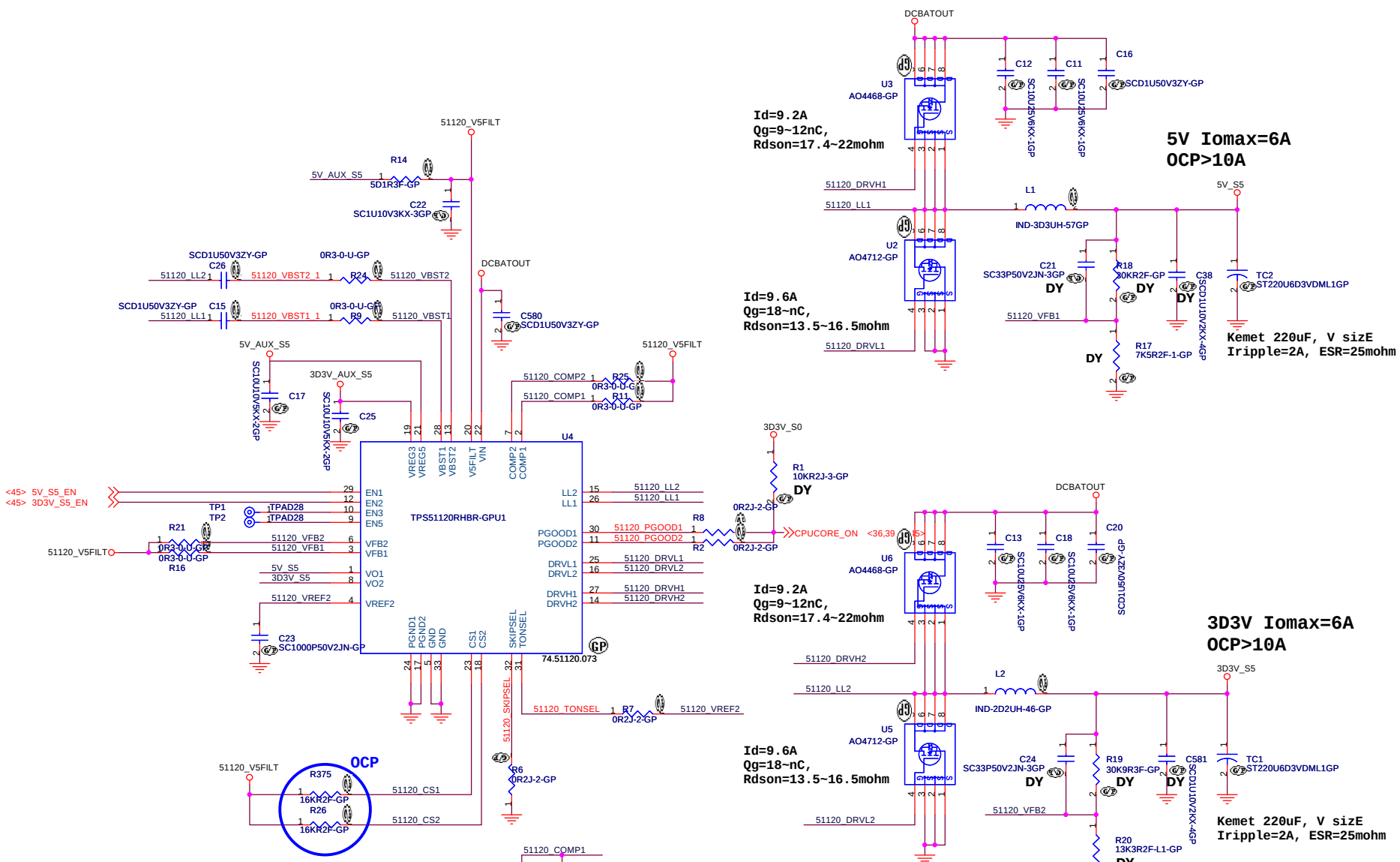
<Core Design>

緯創資通 Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VCC_CORE_2

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 37 of



Pin	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current Mode (apply R-C network)	D-CAP. Mode
TONSEL (CH1/CH2) [kHz]	380 / 580	280 / 430	220 / 330	180 / 270
VFB1	Adjustable output (connect to the resistor divider)			5V fixed output
VFB2	Adjustable output (connect to the resistor divider)			3.3 V fixed output
SKIPSEL	AUTO-SKIP	AUTO-SKIP (FAULTS OFF)	PWM	PWM
EN1, EN2	Switcher Off	Not used	Switcher on	Switcher on
EN3, EN5	LDO Off	Not used	LDO on	LDO on (EN3 only)

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

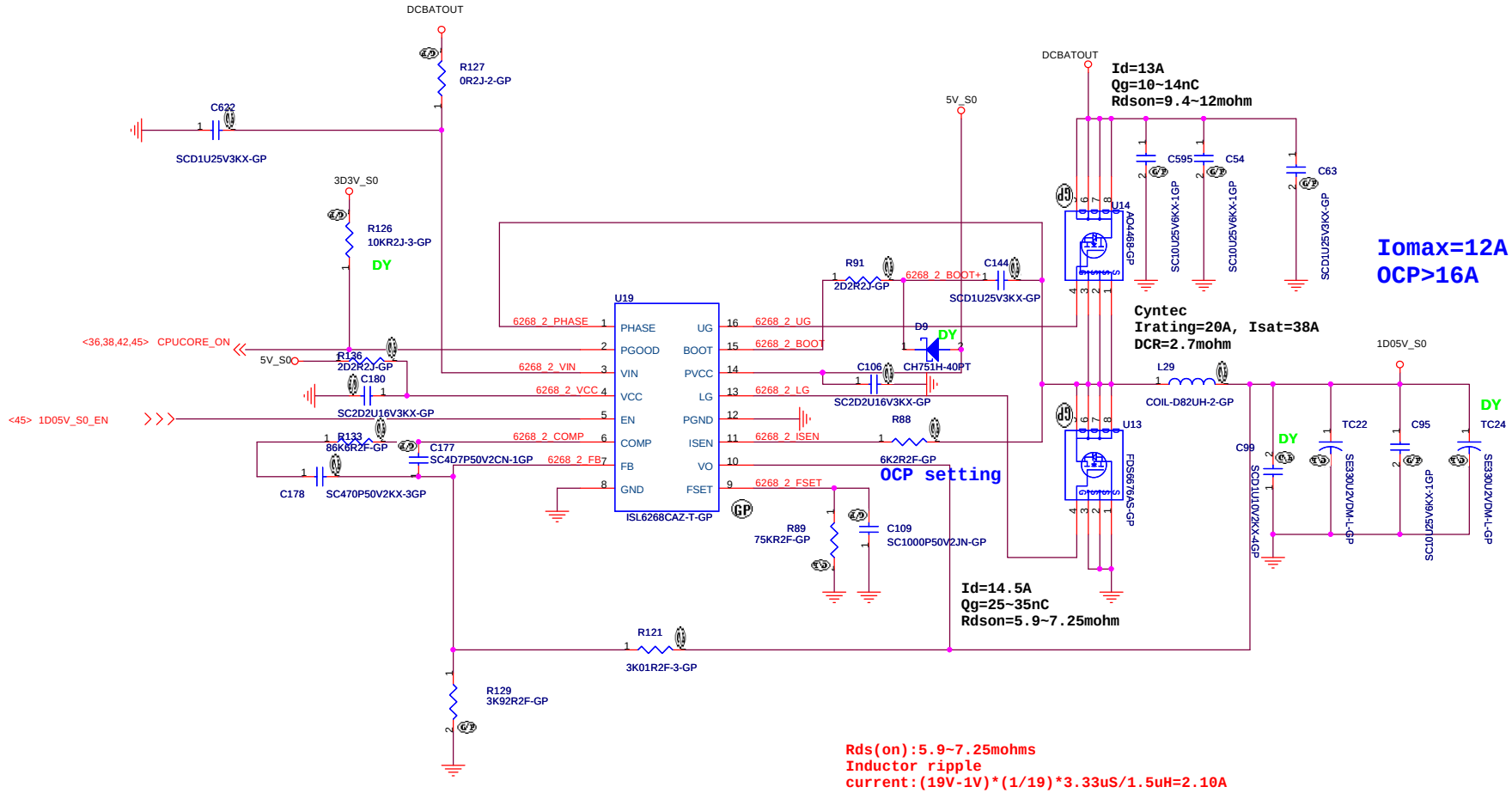
<Core Design>

緯創資通 Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51120 5V / 3D3V

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 38 of



<Core Design>

緯創資通 Wistron Corpo

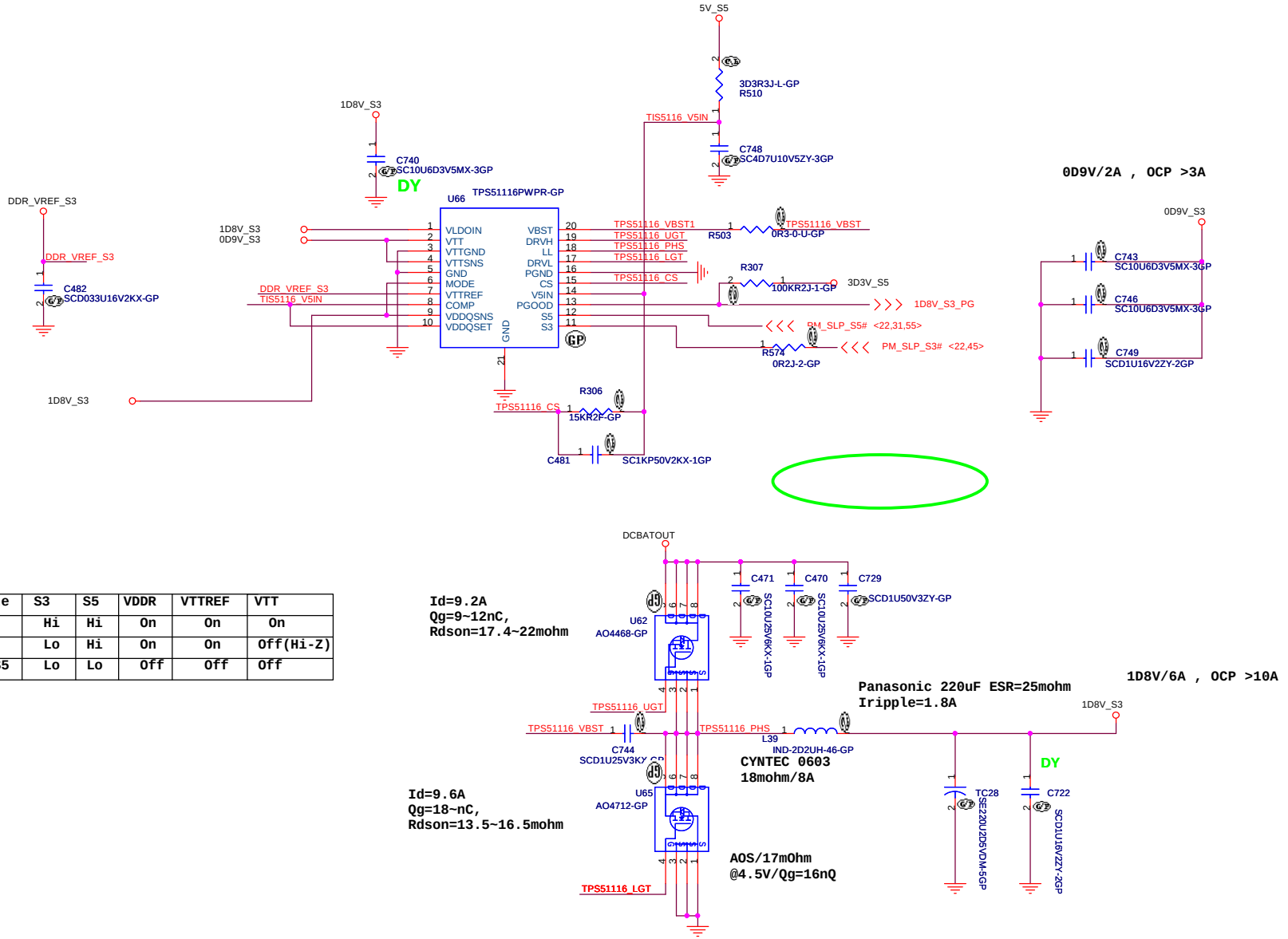
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D05V_S0_ISL6268

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 39 of

TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

<Core Design>

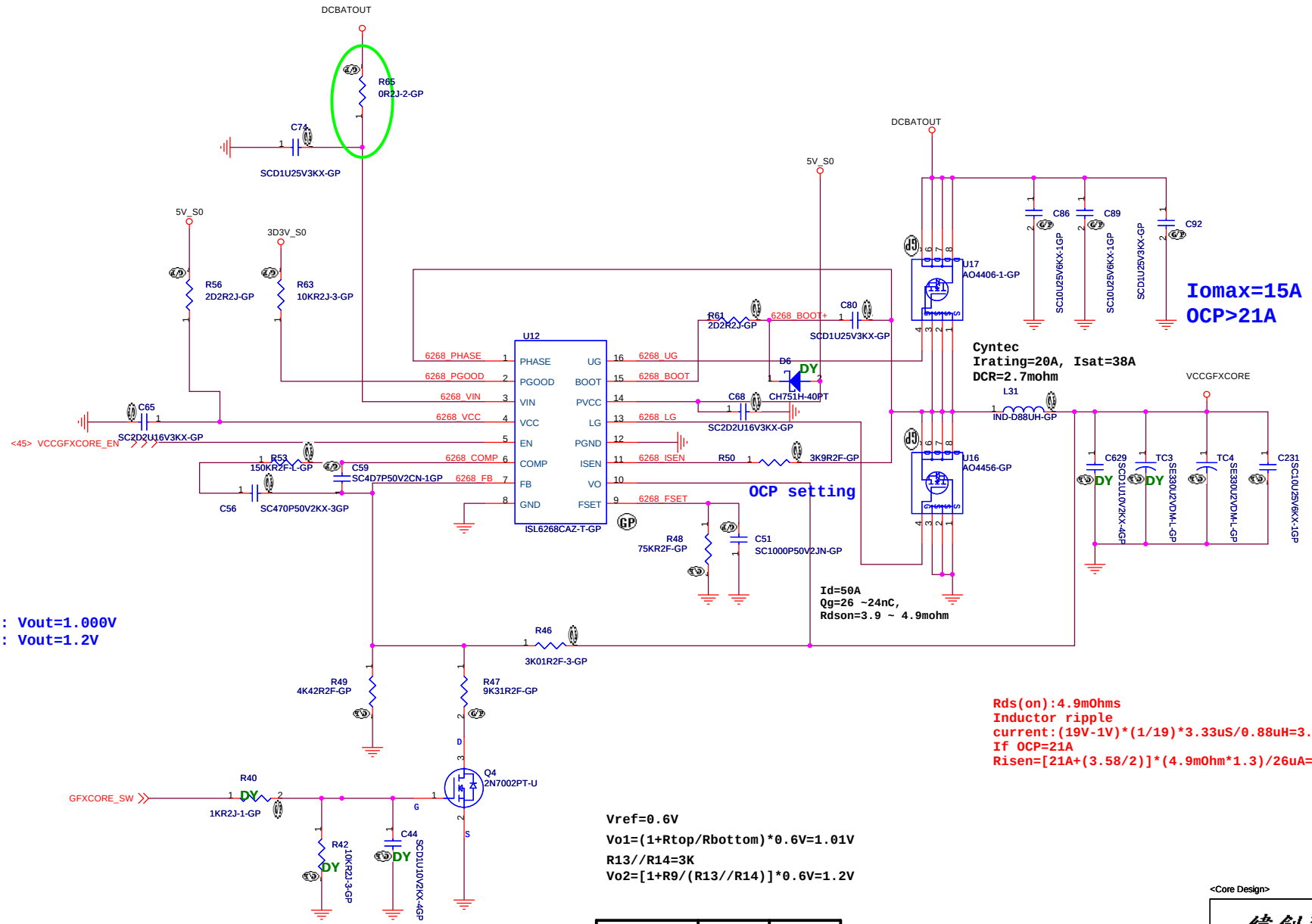
緯創資通 Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116 1D8V/0D9V

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 40 of

reserve for cost down



Vo_Select	Hi	Lo
Vout	1.2V	1.01V

<Core Design>

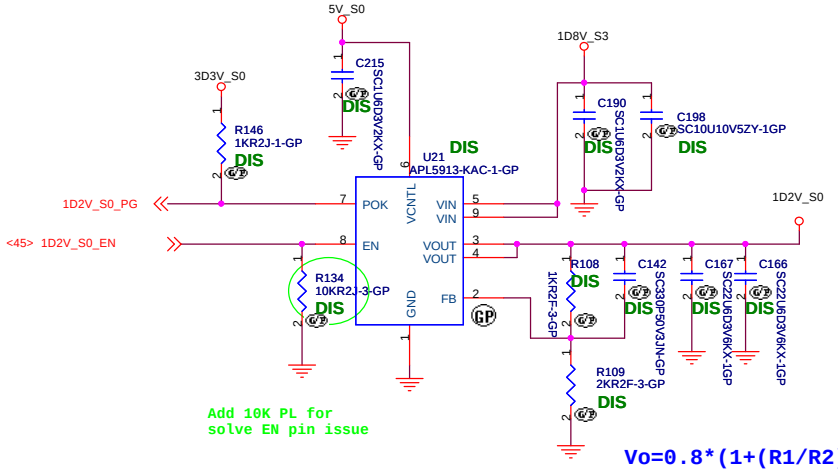
緯創資通 Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C

Title: DC/DC VCCGFXCORE(ISL6268)

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 41 of

VGA 1.2V Power

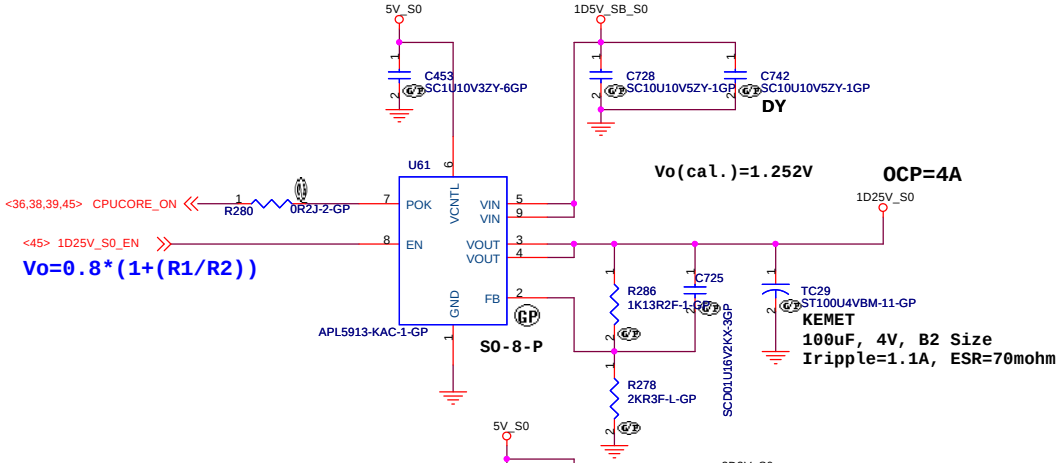


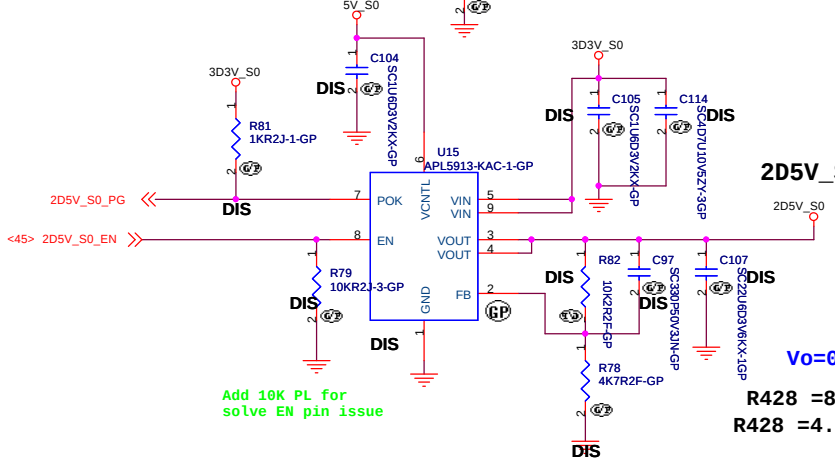
1D2V_S0
only for DISCRETE

1D5V_NB

PS: SB del

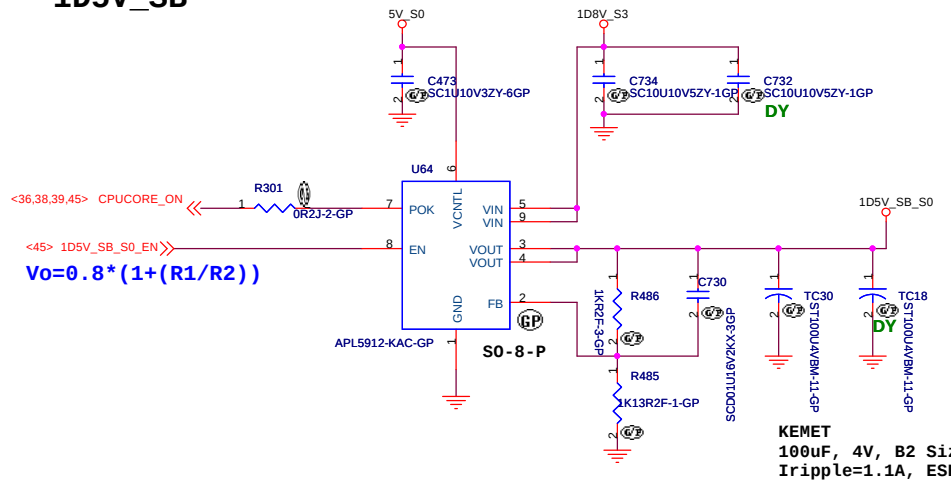
1D25V_S0
Iomax=2.0A





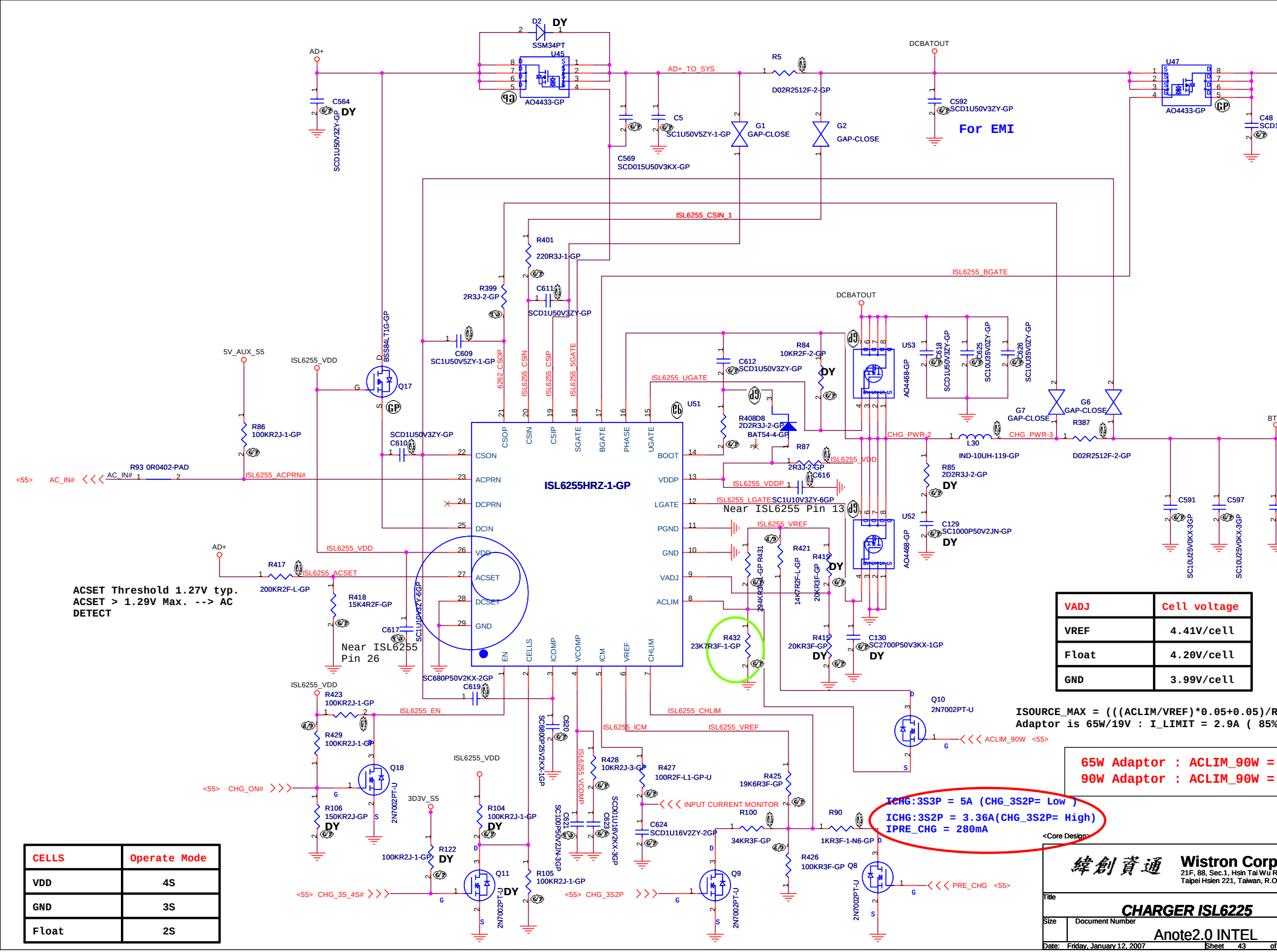
2D5V_S0
only for DISCRETE

1D5V_SB



<Core Design>

緯創資通	Wistron Corpo 21F, 88, Sec.1, Hsin Tai Wu Rd., Taipei Hsien 221, Taiwan, R.O.C
Title	*1D2V_VGA/2D5V/1D25V/1D5V LDO*
Size	Document Number: Anote2.0 INTEL
Date: Friday, January 12, 2007	Sheet 42 of



VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

65W Adaptor : ACLIM_90W = LOW
90W Adaptor : ACLIM_90W = HIGH

Adaptor in to generate DCBATOUT

BATTERY CONNECT

CN13
SKT-JACK-201-GP
22.10037.D51
Lab1 22.10037.B41
Lab2 22.10037.D51

AD_DATA
R12 0R3-0-U-GP
ACDC_ID <55>
C816 SC1000P50V2JN-GP
EMI
D4 UCLAMP3301D-GP
DY
R575 0R6J-3-GP
R576 0R6J-3-GP
AD_IN
AD_JK
C815 SCD1U50V3ZY-GP
EMI
D13 P4SSMJ24PT-GP
U1 AO4433-GP
AD+_2
AD+
C8 SCD1U50V3ZY-GP
R374 100KR2J-1-GP
C9 SC1U50V5ZY-1-GP
PDTA124EU-1-GP
Q16
R371 56KR3F-GP
Q1 CHDTC124EU-1GP
<55> AD_OFF
R15 1KR2J-1-GP
3D3V_AUX_S5
D16 BAV99PT-GP-U
DY
D15 BAV99PT-GP-U
DY
<55> BAT_SCL
<55> BAT_SDA
<55,57> BAT_IN#
BT+
R379 27R3F-GP
R380 27R3F-GP
BATA_SCL_1
BATA_SDA_1
R577 0R6J-3-GP
R578 0R6J-3-GP
BAT_VCC_IN
C50
C590
C589
C821 SCD1U50V3ZY-GP
SC270P50V2JN-2GP
CN17
SYN-C
20.80

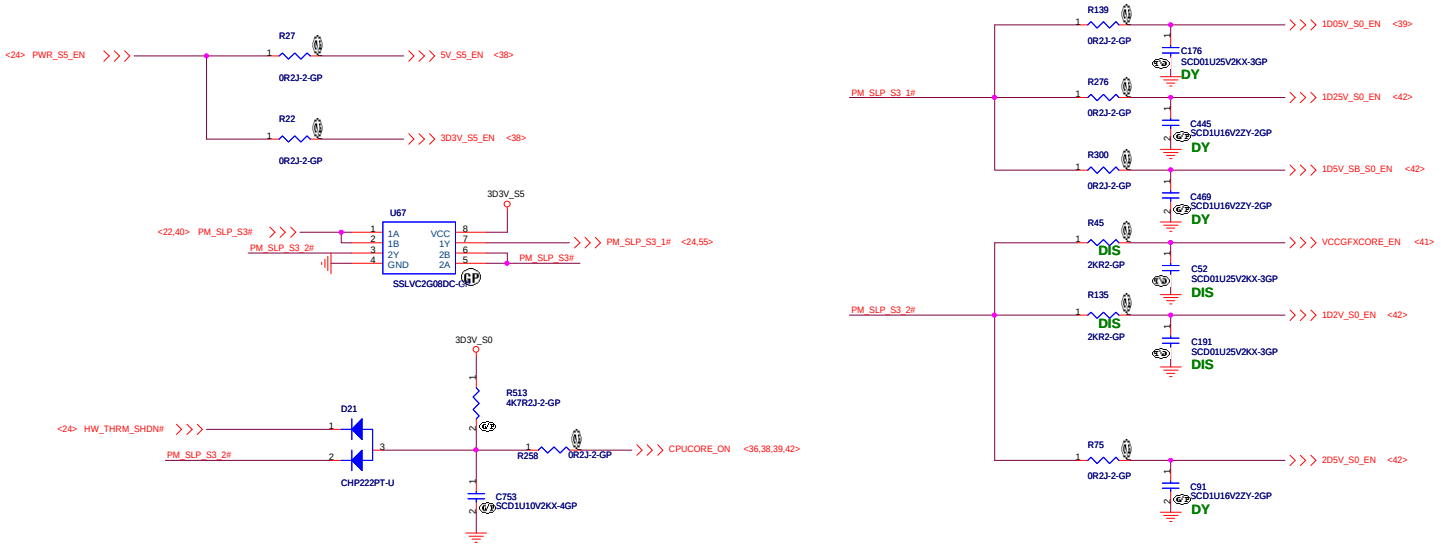
<57> AD_IN
<57> AD_DATA

<57> BATA_SCL_1
<57> BATA_SDA_1
<55,57> BAT_IN#
<57> BAT_VCC_IN

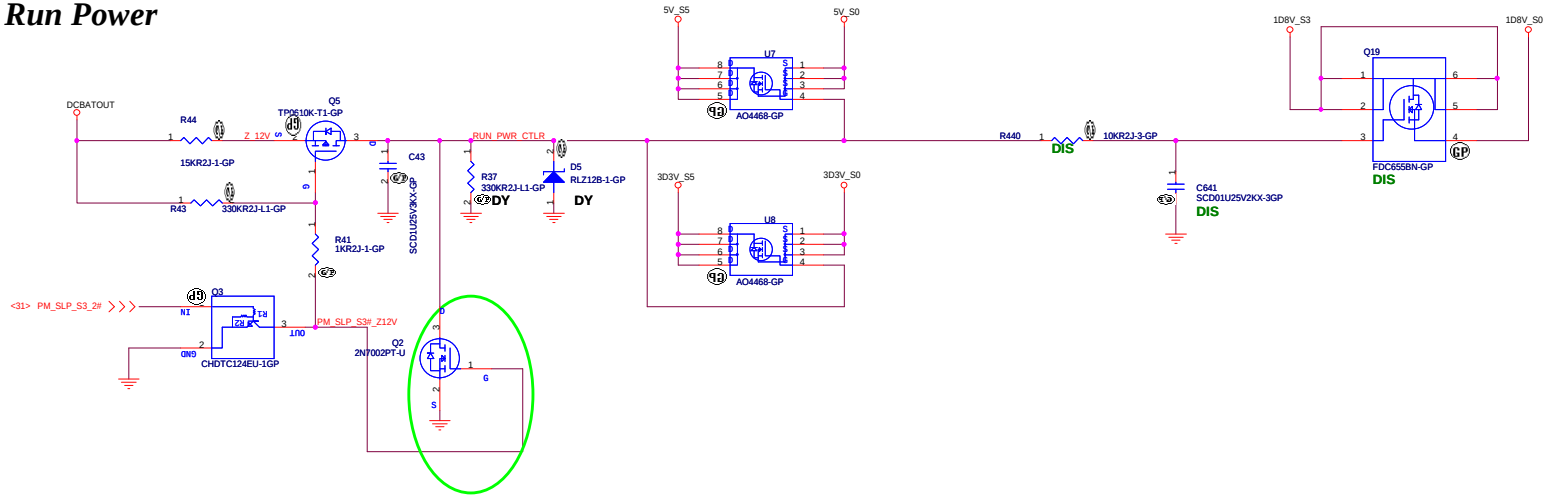
<Core Design>

緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN
Size:
Document Number: Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 44 of

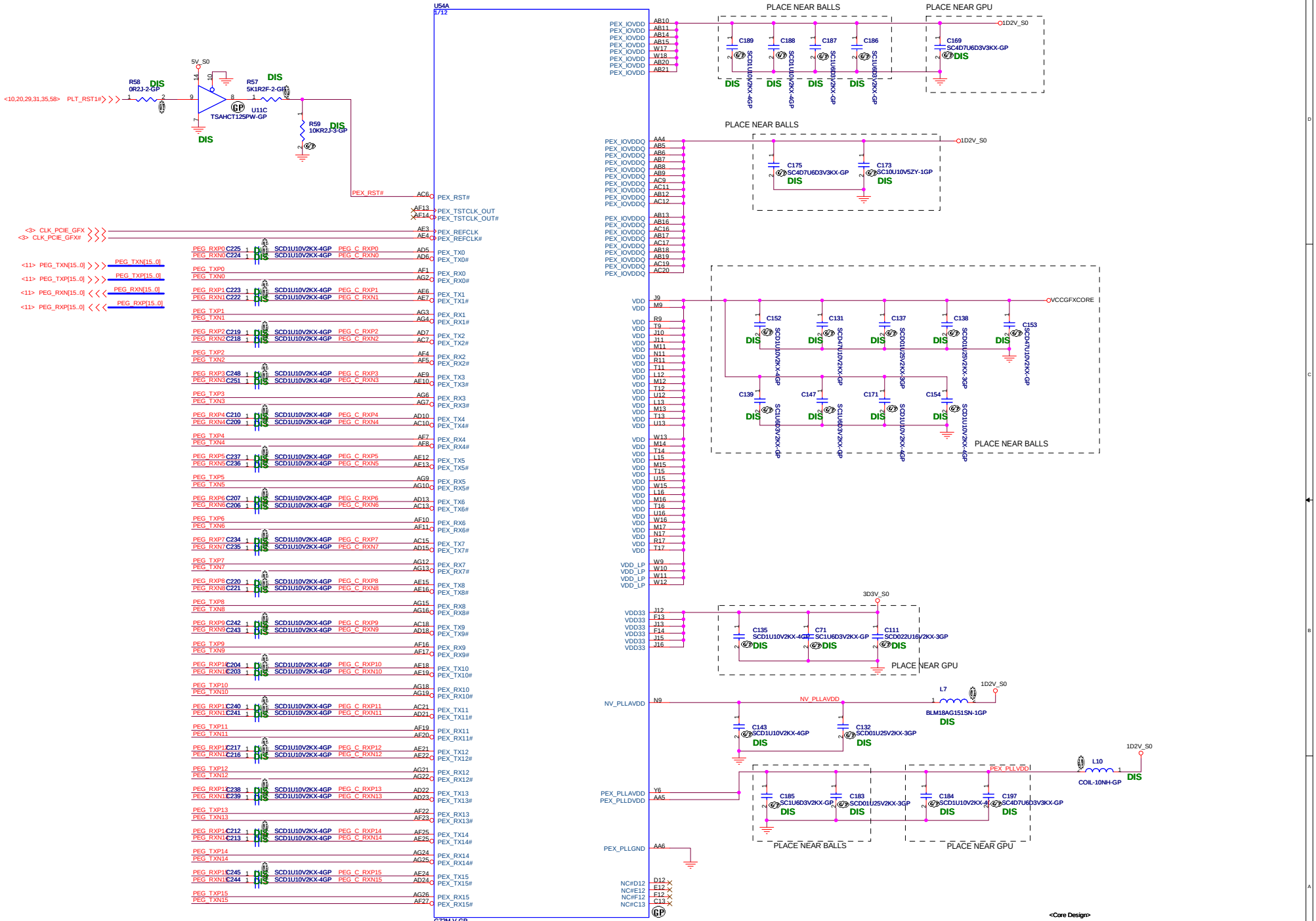


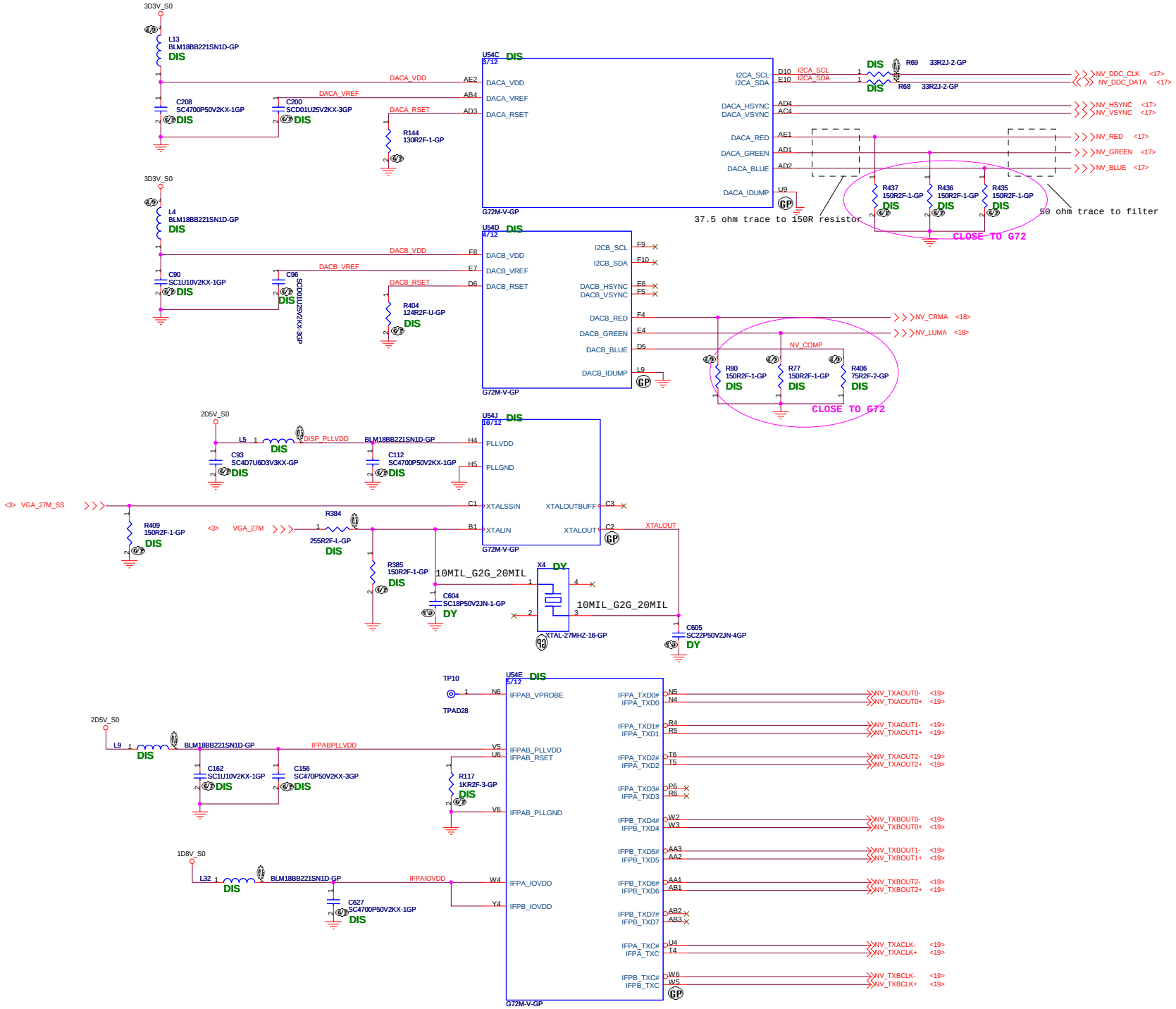
Run Power



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PWRPLANE&RESET LOGIC***	
Size: C	Document Number: Anote2.0 INTEL	Rev: SC
Date: Friday, January 12, 2007	Sheet 45 of 58	


U54A
1/12
G72M-V-GP
DIS
71.0G72M.B0U
PLACE NEAR BALLS
PLACE NEAR GPU
VCCGFXCORE
1D2V_S0
3D3V_S0
5V_S0
TSAHCT125PW-GP
U11C
PLT_RST1#
PEX_RST#
CLK_PCIE_GFX
CLK_PCIE_GFX#
PEG_TXN[15..0]
PEG_TXP[15..0]
PEG_RXN[15..0]
PEG_RXP[15..0]
NV_PLLAVDD
PEX_PLLAVDD
PEX_PLLDVDD
PEX_PLLGND
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
G72M PCIE
Anote2.0 INTEL
Friday, January 12, 2007
46
58



<Core Design>

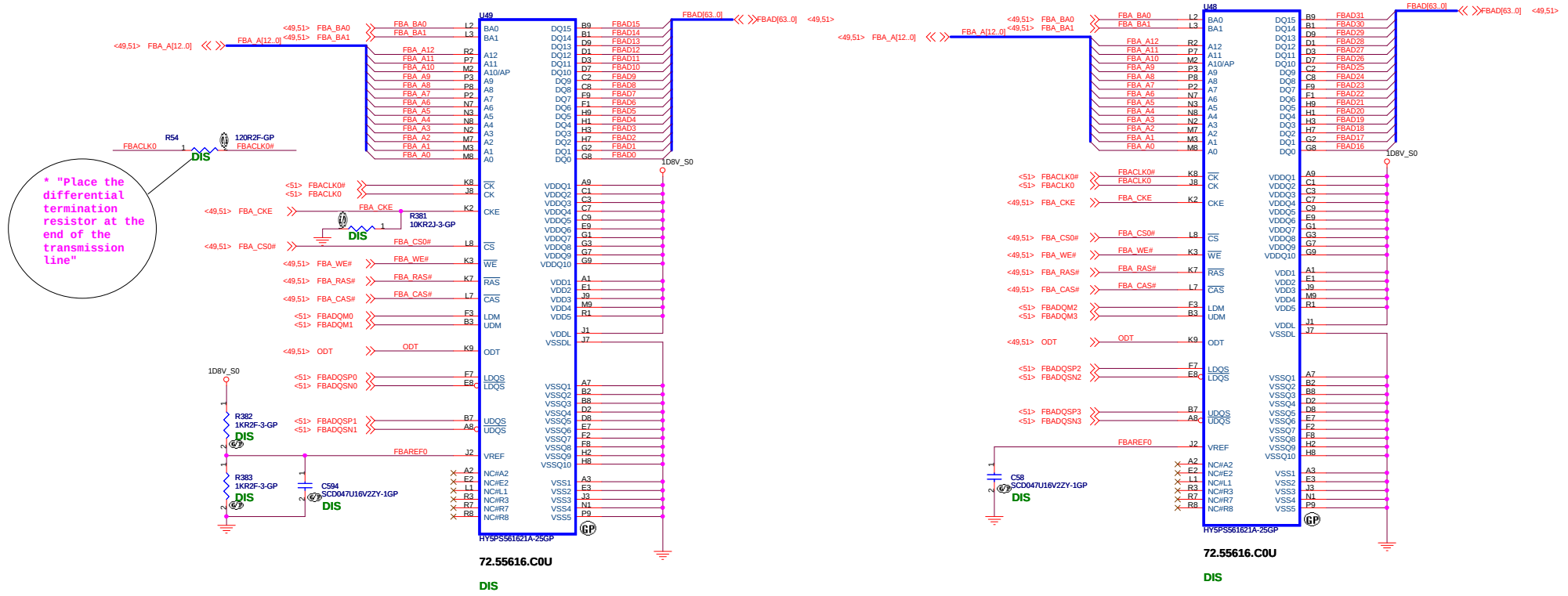
緯創資通 Wistron Co

21F, 88, Sec.1, Hsin Tai W
Taipei Hsien 221, Taiwan,

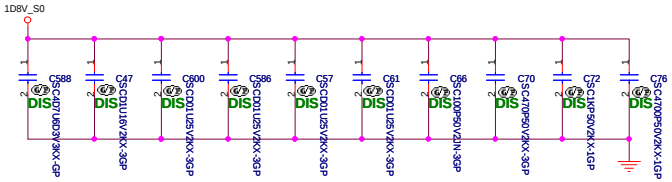
Title: G72M CRT & TV OUT

Size | Document Number: Anote2.0 INTEL

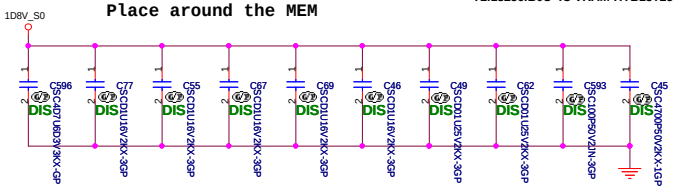
Date: Friday, January 12, 2007 | Sheet 47



Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



72.51216.D0U IC VRAM HY5PS121621BFP-25 FBGA(32M*16, 400Mhz)
72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGAby Hynix (16M*16, 400Mhz)
72.18512.A0U IC VRAM HY5PS121621BFP-25 FBGA by Infineon (32M*16, 400Mhz)
72.18256.B0U IC VRAM HYB18T256161AFL25 BGA, by Infineon(16M*16, 400Mhz)

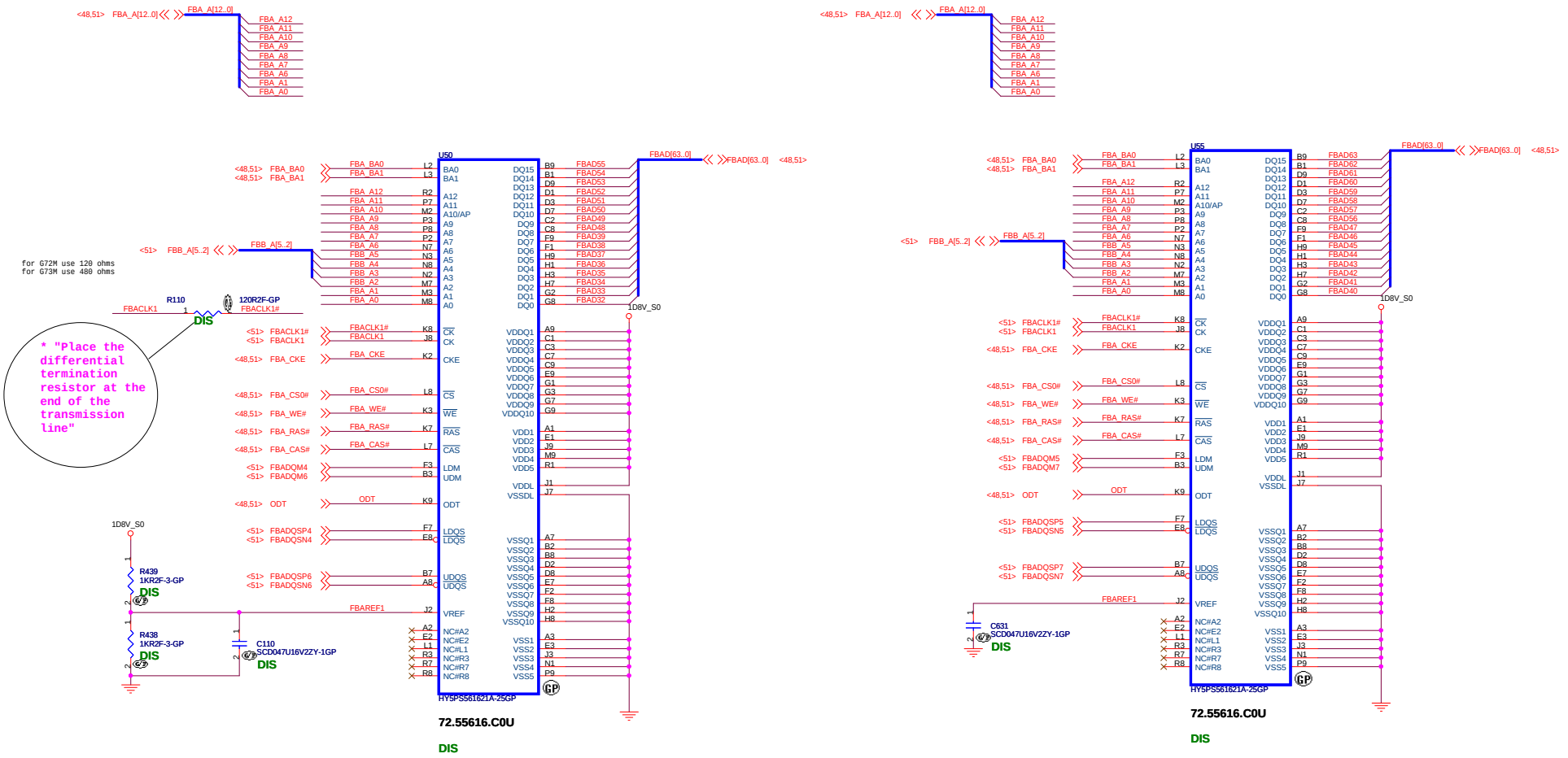
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

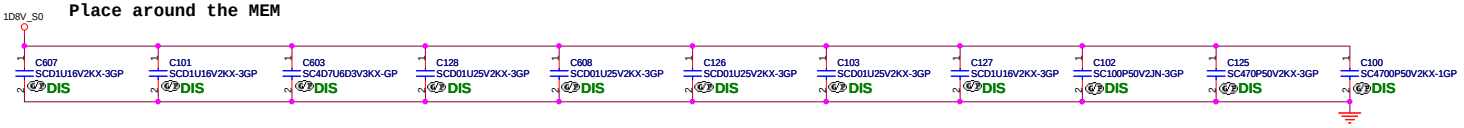
Title: G72M VRAM (1ST 1/2)

Size	Document Number	Rev
	Anote2.0 INTEL	SC

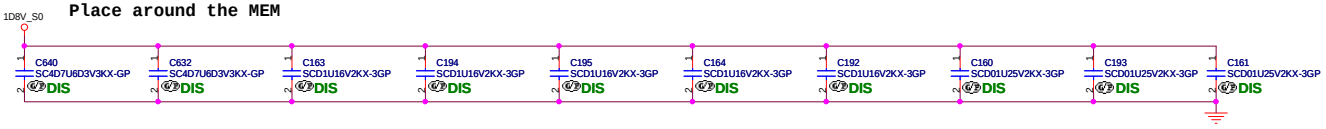
Date: Friday, January 12, 2007 Sheet 48 of 58



Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



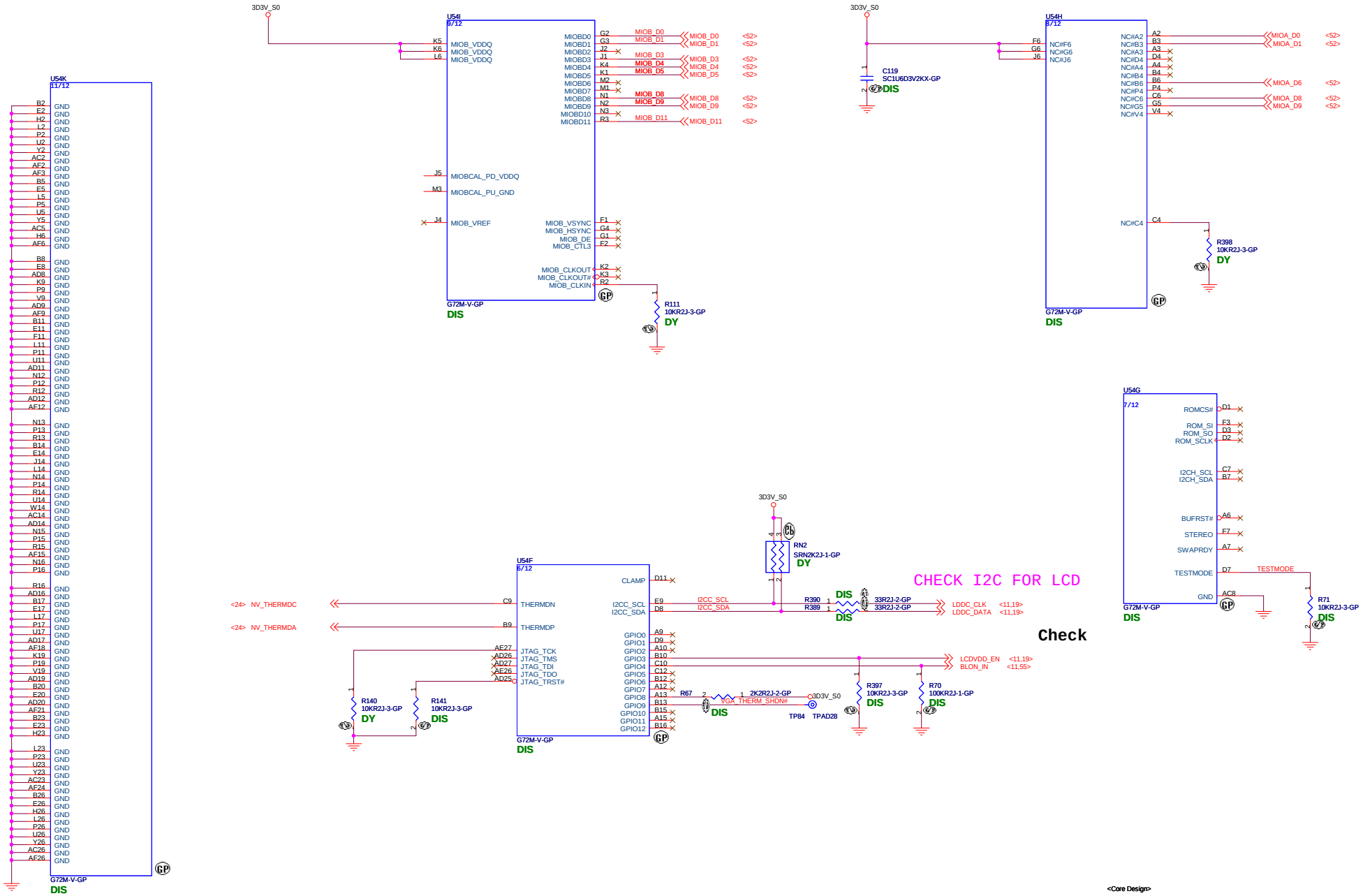
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M VRAM (1ST 2/2)

Size | Document Number: Anote2.0 INTEL | Rev: SC

Date: Friday, January 12, 2007 | Sheet 49 of 58



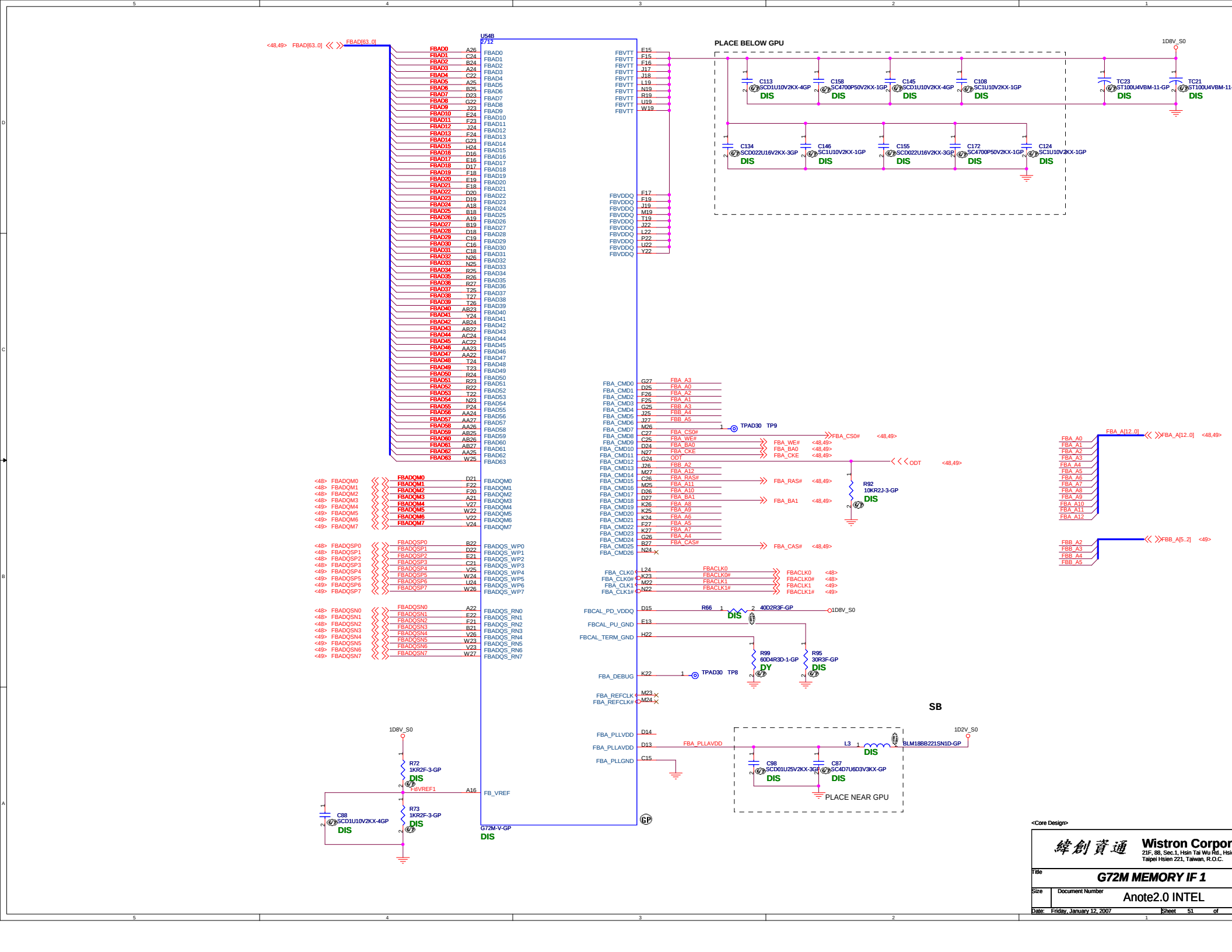
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M ROM & Spread Specturm

Size	Document Number	Rev
	Anote2.0 INTEL	SC

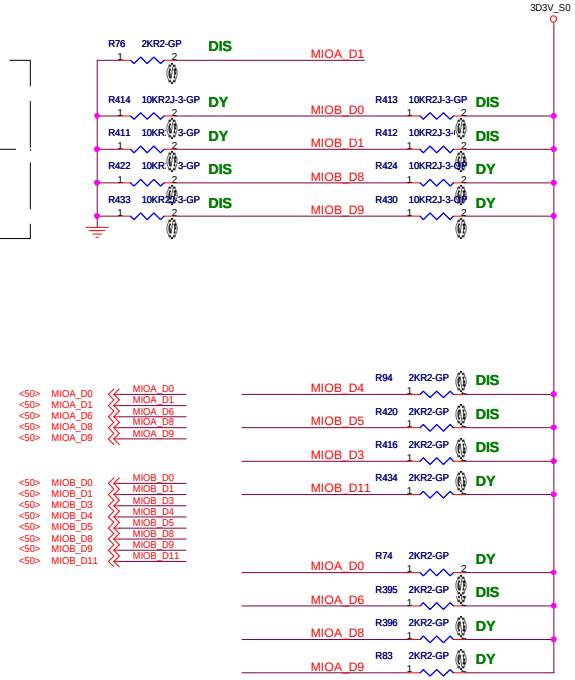
Date: Friday, January 12, 2007 Sheet 50 of 58


U54B
2/12
G72M-V-GP
DIS
PLACE BELOW GPU
1D8V_S0
C113 SCD1U10V2KX-4GP DIS
C158 SC4700P50V2KX-1GP DIS
C145 SCD1U10V2KX-4GP DIS
C108 SC1U10V2KX-1GP DIS
TC23 ST100U4VBM-11-GP DIS
TC21 ST100U4VBM-11- DIS
C134 SCD022U16V2KX-3GP DIS
C146 SC1U10V2KX-1GP DIS
C155 SCD022U16V2KX-3GP DIS
C172 SC4700P50V2KX-1GP DIS
C124 SC1U10V2KX-1GP DIS
FBAD[63..0]
FBADQM[7..0]
FBADQSP[7..0]
FBADQSN[7..0]
FBVTT
FBVDDQ
FBA_CMD0
FBA_CMD1
FBA_CMD2
FBA_CMD3
FBA_CMD4
FBA_CMD5
FBA_CMD6
FBA_CMD7
FBA_CMD8
FBA_CMD9
FBA_CMD10
FBA_CMD11
FBA_CMD12
FBA_CMD13
FBA_CMD14
FBA_CMD15
FBA_CMD16
FBA_CMD17
FBA_CMD18
FBA_CMD19
FBA_CMD20
FBA_CMD21
FBA_CMD22
FBA_CMD23
FBA_CMD24
FBA_CMD25
FBA_CMD26
TPAD30 TP9
TPAD30 TP8
FBA_CS0#
FBA_WE#
FBA_BA0
FBA_CKE
ODT
FBA_RAS#
FBA_BA1
FBA_CAS#
FBA_CLK0
FBA_CLK0#
FBA_CLK1
FBA_CLK1#
FBACLK0
FBACLK0#
FBACLK1
FBACLK1#
R92 10KR2J-3-GP DIS
R66 40D2R3F-GP DIS
R99 60D4R3D-1-GP DY
R95 30R3F-GP DIS
FBCAL_PD_VDDQ
FBCAL_PU_GND
FBCAL_TERM_GND
FBA_DEBUG
FBA_REFCLK
FBA_REFCLK#
FBA_A[12..0]
FBA_A0
FBA_A1
FBA_A2
FBA_A3
FBA_A4
FBA_A5
FBA_A6
FBA_A7
FBA_A8
FBA_A9
FBA_A10
FBA_A11
FBA_A12
FBB_A[5..2]
FBB_A2
FBB_A3
FBB_A4
FBB_A5
SB
1D2V_S0
FBA_PLLVDD
FBA_PLLGND
FBA_PLLAVDD
L3 BLM18BB221SN1D-GP DIS
C98 SCD01U25V2KX-3GP DIS
C87 SC4D7U6D3V3KX-GP DIS
PLACE NEAR GPU
R72 1KR2F-3-GP DIS
R73 1KR2F-3-GP DIS
C88 SCD1U10V2KX-4GP DIS
FBVREF1
FB_VREF
<Core Design>
緯創資通
Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsi
Taipei Hsien 221, Taiwan, R.O.C.
Title
G72M MEMORY IF 1
Size
Document Number
Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 51 of

STRAPS, Mechanical Parts

Check

Hynix256MB :	R825_0	R824_1	R822_1	R820_1
Hynix128MB :	R825_0	R823_0	R822_1	R820_1
Hynix64MB :	R826_1	R823_0	R822_1	R820_1
Infineon256MB :	R825_0	R824_1	R822_1	R819_0
Infineon128MB :	R825_0	R823_0	R822_1	R819_0
Infineon64MB :	R826_1	R823_0	R822_1	R819_0



Bit	Signal	Values
MIOA_D1:	SUB_VENDOR	0 NO_BIOS 1 READ FROM BIOS

For MEM strapping, Please use below table:

RAM_CFG[9.8.1.0] RAM_CFG[3..0]	Config	FB Bus Width	Definitions
0000			
0001	16Mx16 DDR2	64-bit	Samsung
0010	16Mx16 DDR2	64-bit	Infineon
0011	16Mx16 DDR2	64-bit	Hynix
0100			
0101	32Mx16 DDR2	64-bit	Samsung
0110	32Mx16 DDR2	64-bit	Infineon
0111	32Mx16 DDR2	64-bit	Hynix

MIOB_D4:	PCI_DEVID_0	
MIOB_D5:	PCI_DEVID_1	1000 (default 0x00FC)
MIOB_D3:	PCI_DEVID_2	
MIOB_D11:	PCI_DEVID_3	0111 G72MV **G72MZ=6,G73=8**

MIOA_D0:	PEX_PLL_EN_TERM100	0 ENABLED 1 DISABLED
MIOA_D6:	3GIO_PADCFG_LUT_ADDR[0]	
MIOA_D8:	3GIO_PADCFG_LUT_ADDR[1]	
MIOA_D9:	3GIO_PADCFG_LUT_ADDR[2]	001 DEFAULT

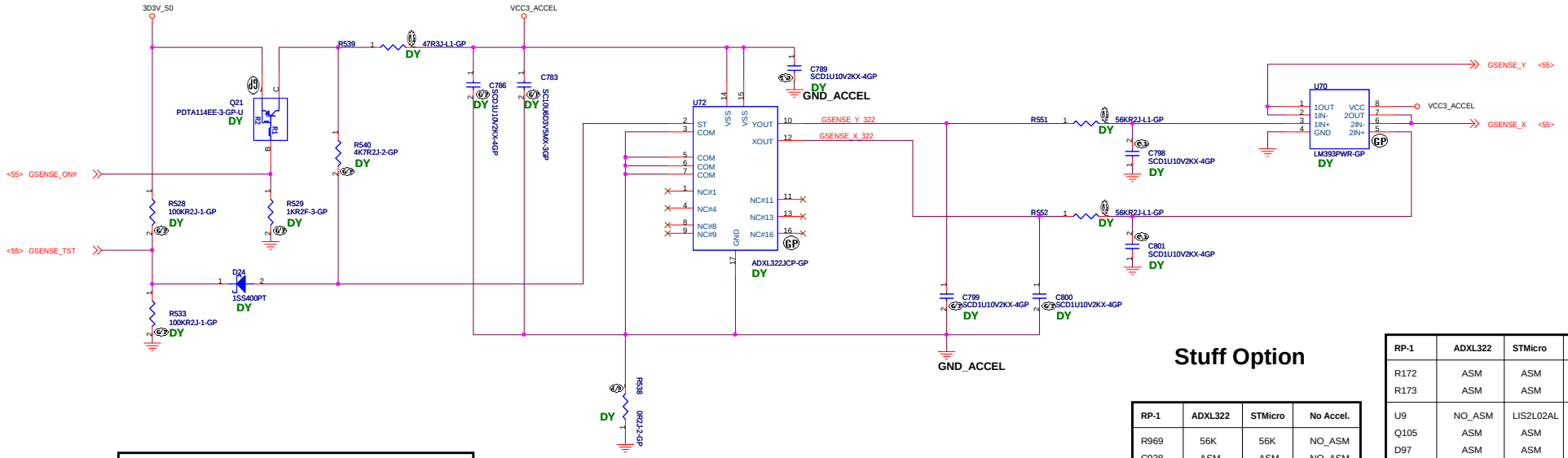
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G72M STRAPPING***

Size	Document Number	Rev
	Anote2.0 INTEL	SC

Date: Friday, January 12, 2007 Sheet 52 of 58



Stuff Option

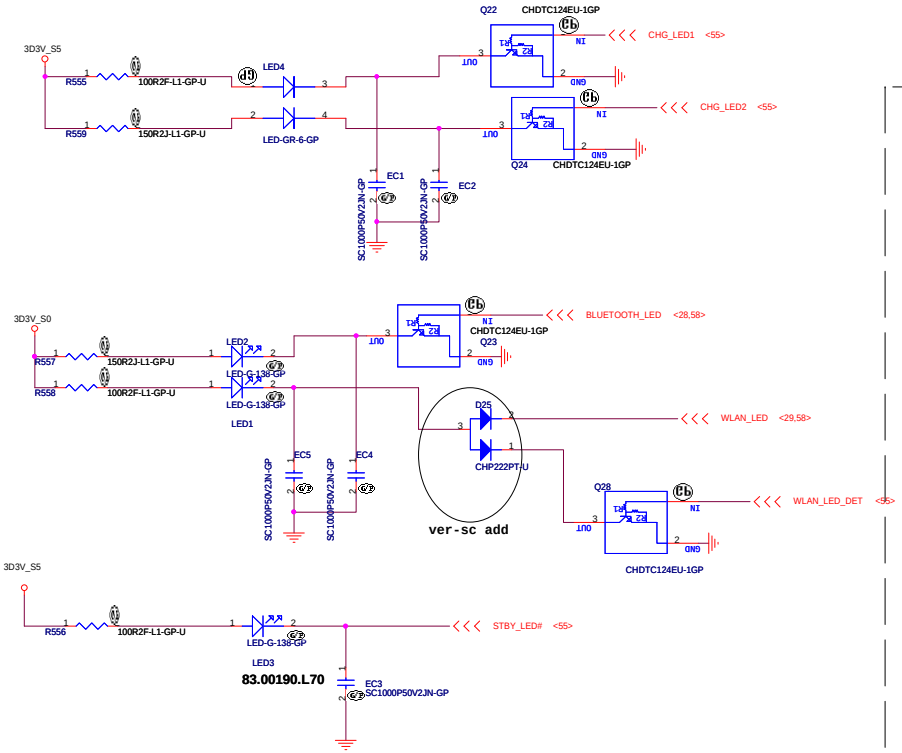
RP-1	ADXL322	STMicro	No Accel.
R969	56K	56K	NO_ASM
C938	ASM	ASM	NO_ASM
R970	56K	56K	NO_ASM
C956	ASM	ASM	NO_ASM
U66	ADXL322	NO_ASM	NO_ASM
C170	ASM	NO_ASM	NO_ASM
C178	ASM	NO_ASM	NO_ASM
C190	ASM	NO_ASM	NO_ASM
R31	ASM	NO_ASM	NO_ASM

RP-1	ADXL322	STMicro	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C830	NO_ASM	0.033UF	NO_ASM
C847	NO_ASM	0.033UF	NO_ASM

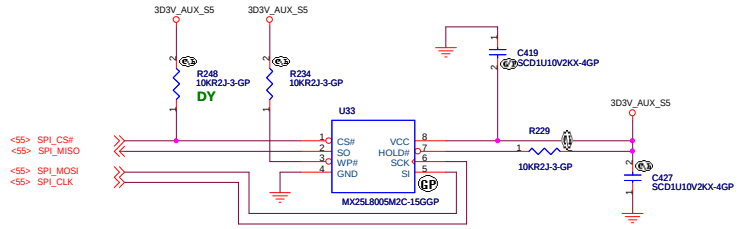
A-note 2.0 LED's Location and Sequence

Left side — Right side

WLAN Bluetooth Battery Suspend



SPI ROM for System & KBC



1. MXIC MX25L8005M2C
2. WINBOND W25X80
3. SST 8Mbit72.25080.G01

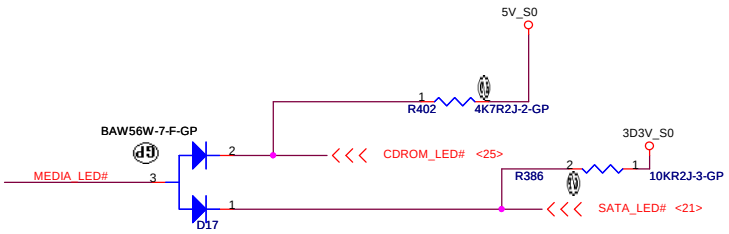
<Core Design>

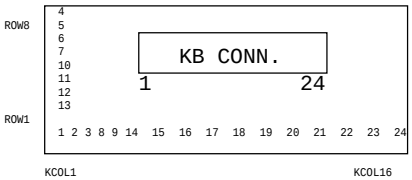
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G-sensor / SPI / LEDs

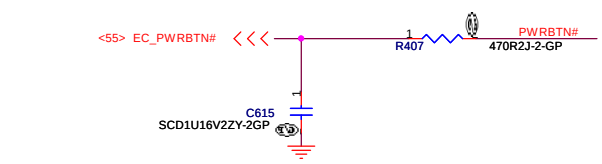
Size: C | Document Number: Anote2.0 INTEL | Rev: SC

Date: Friday, January 12, 2007 | Sheet 53 of 58

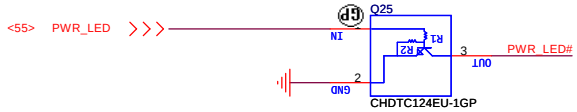


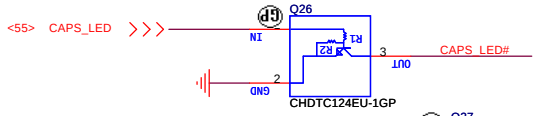


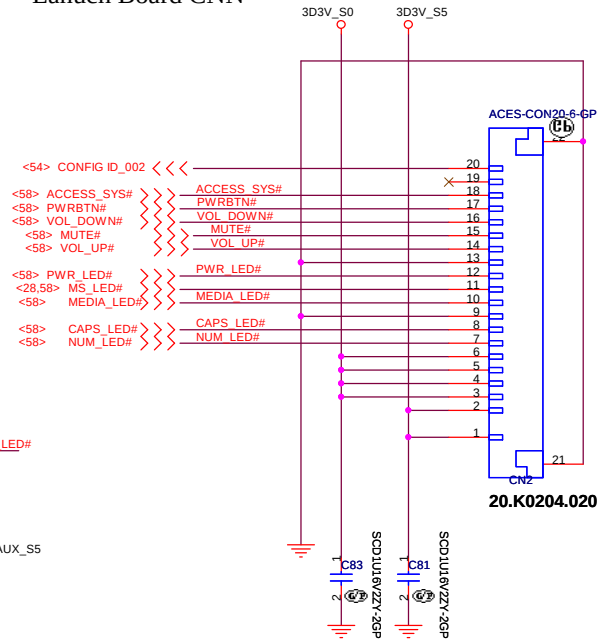
Internal KeyBoard Connector



Lanuch Board CNN

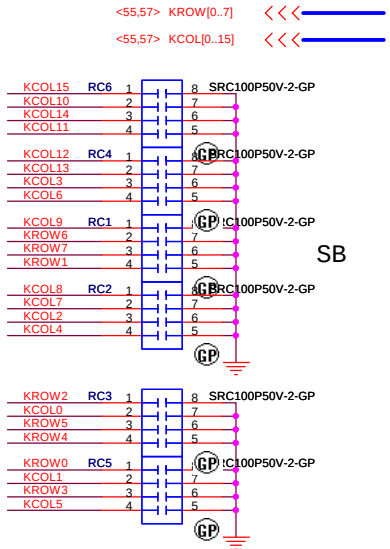


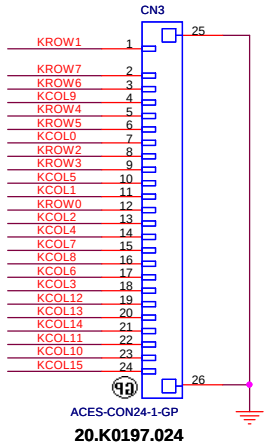




20.K0204.020

LAB2 20.K0204.020





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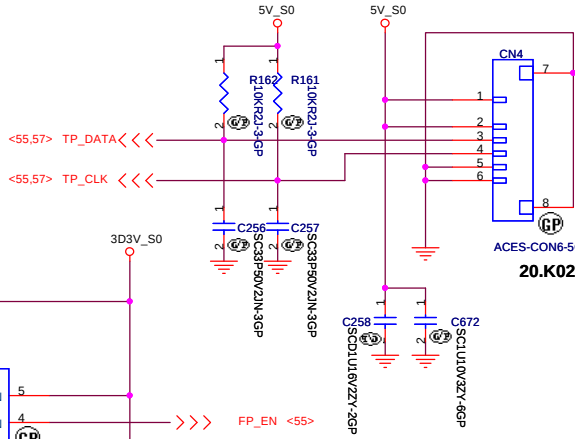
TouchPad Connector



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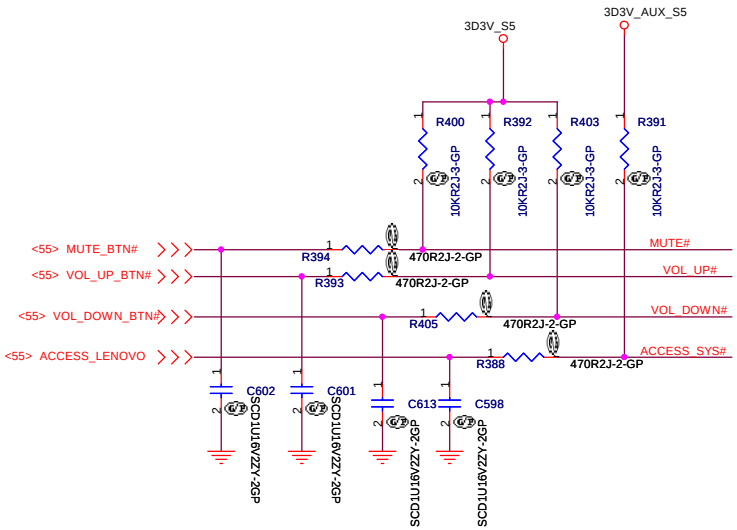
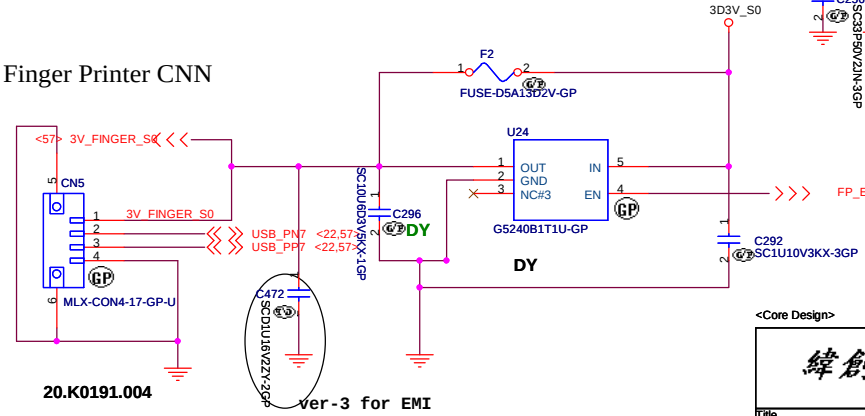


Finger Printer CNN



20.K0191.004

ver-3 for EMI

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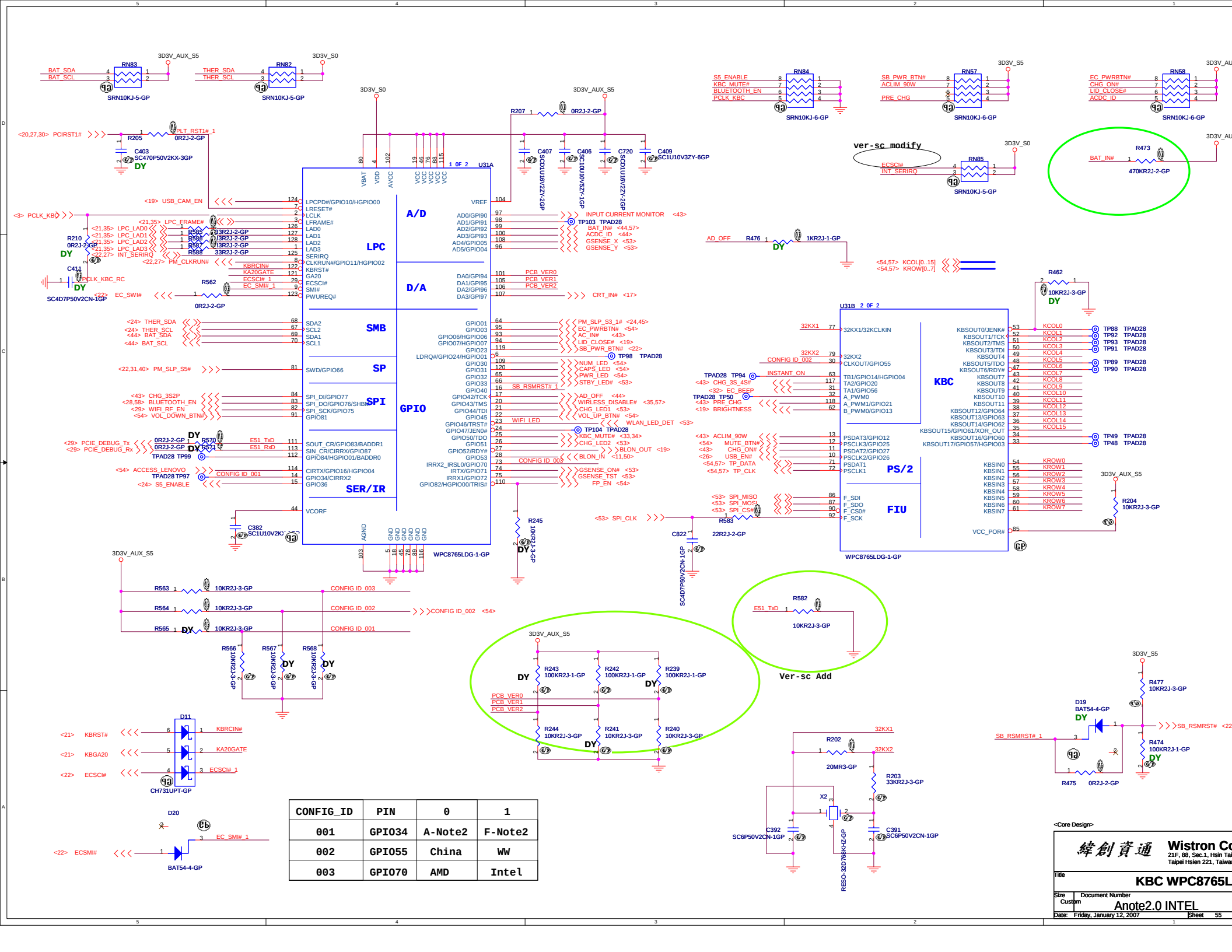
Taipei Hsien 221, Taiwan, R.O.C.

Title: Keyboard /Touch Pad

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 54 of



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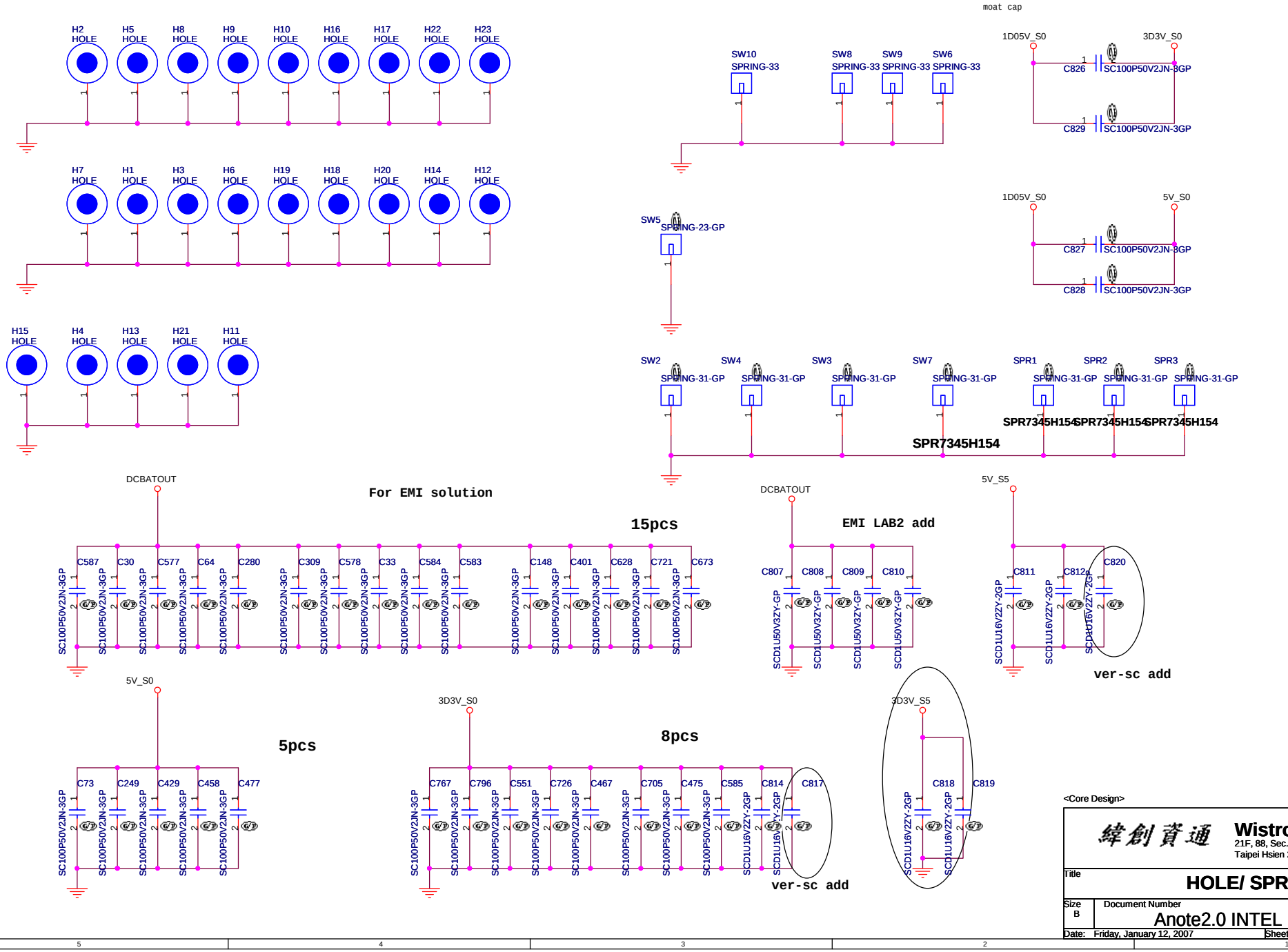
002	GPIO55	China	WW
003	GPIO70	AMD	Intel



<Core Design>

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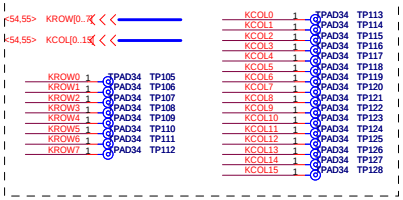
Taipei Hsien 221, Taiwan, R.O.C.

Title: HOLE/ SPRING

Size: B | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 56 of

Near CN3 KB



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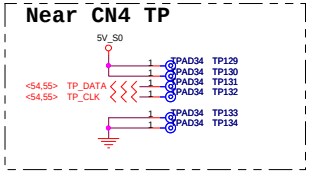

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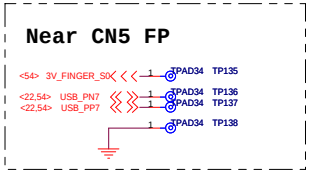

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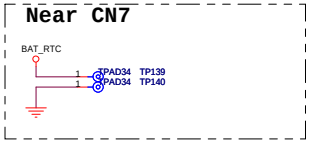

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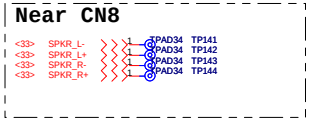

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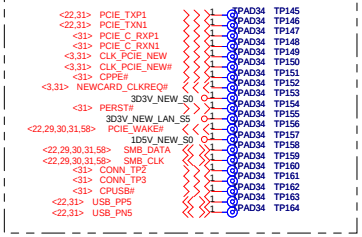
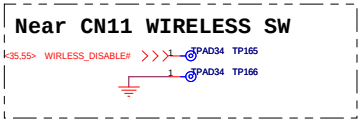
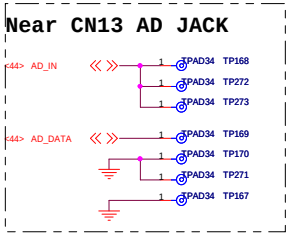


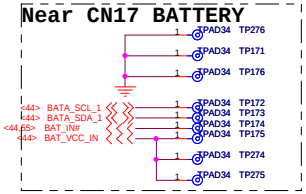
Near CN11 WIRELESS SW



Near CN13 AD JACK



Near CN17 BATTERY



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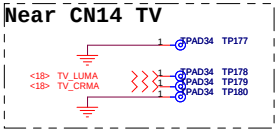

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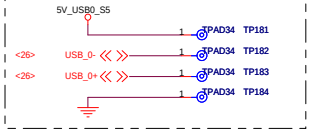

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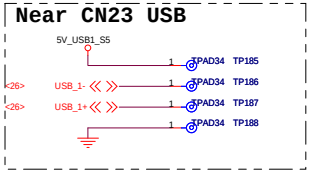

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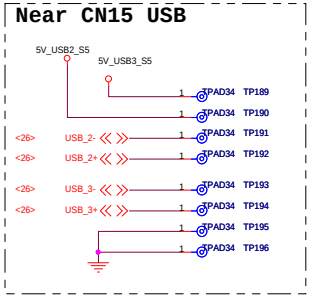

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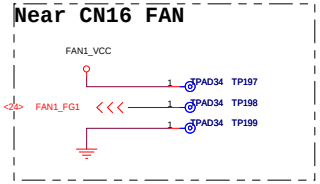

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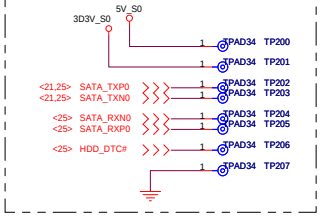
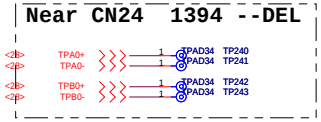
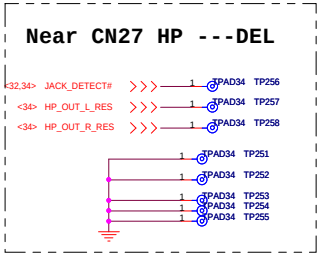


Near CN24 1394 --DEL



Near CN27 HP ---DEL



Near CN27 EXT MIC---DEL

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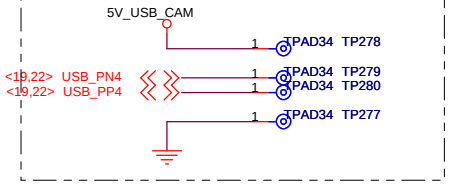
Size: C | Document Number: Anote2.0 INTEL | Rev: SC

Date: Friday, January 12, 2007 | Sheet 57 of 58

Near LCD CNN--CAM



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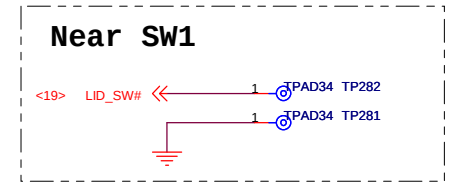

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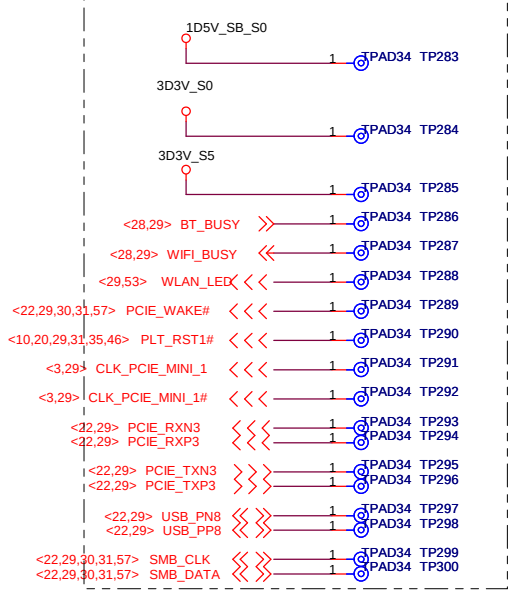
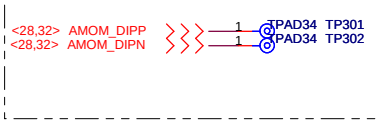
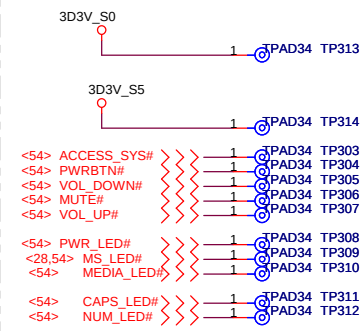


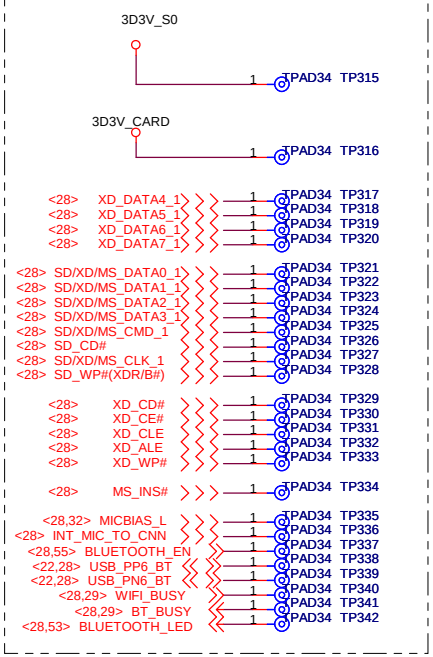
Modem



Launch-BD



Daughter-BD



<Core Design>

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Date: Friday, January 12, 2007 | Sheet 58 of