Compal confidential

Schematics Document
Mobile Merom uFCPGA with Satna Rosa Platform

2007-07-24

REV:0.3

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: *Cover Sheet*

Size: Custom | Document Number: *LA-3821P* | Rev: 0.3

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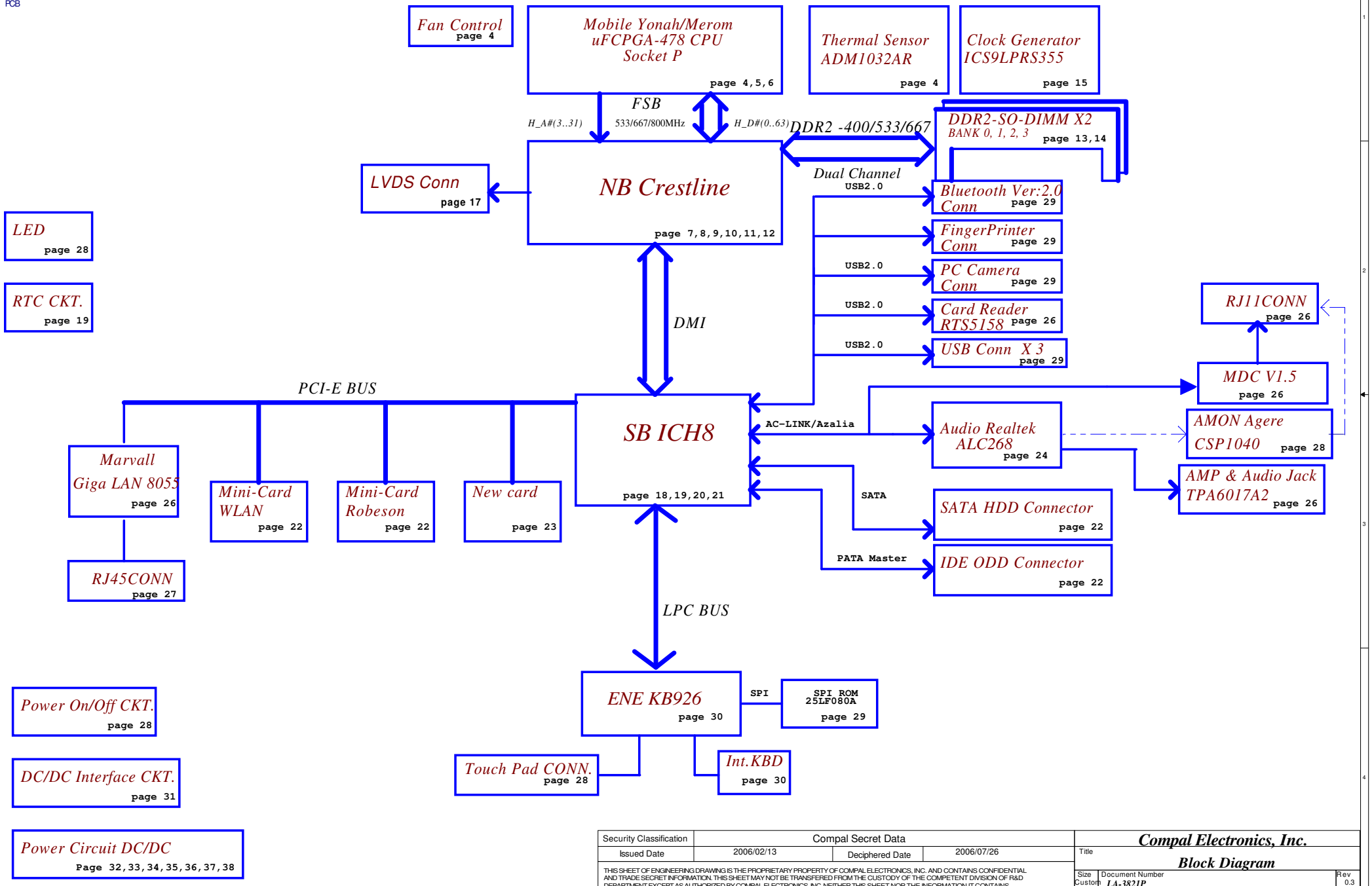
Compal confidential

File Name : LA-3821P

Supra 1.0 (Merom +Crestline+ICH8) 12"

ZZZ1

PCB



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Title: Block Diagram

Size	Document Number	Rev
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Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

BOM: 43XXXXXX

Jump-Short: PJP?

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Title: *Notes List*

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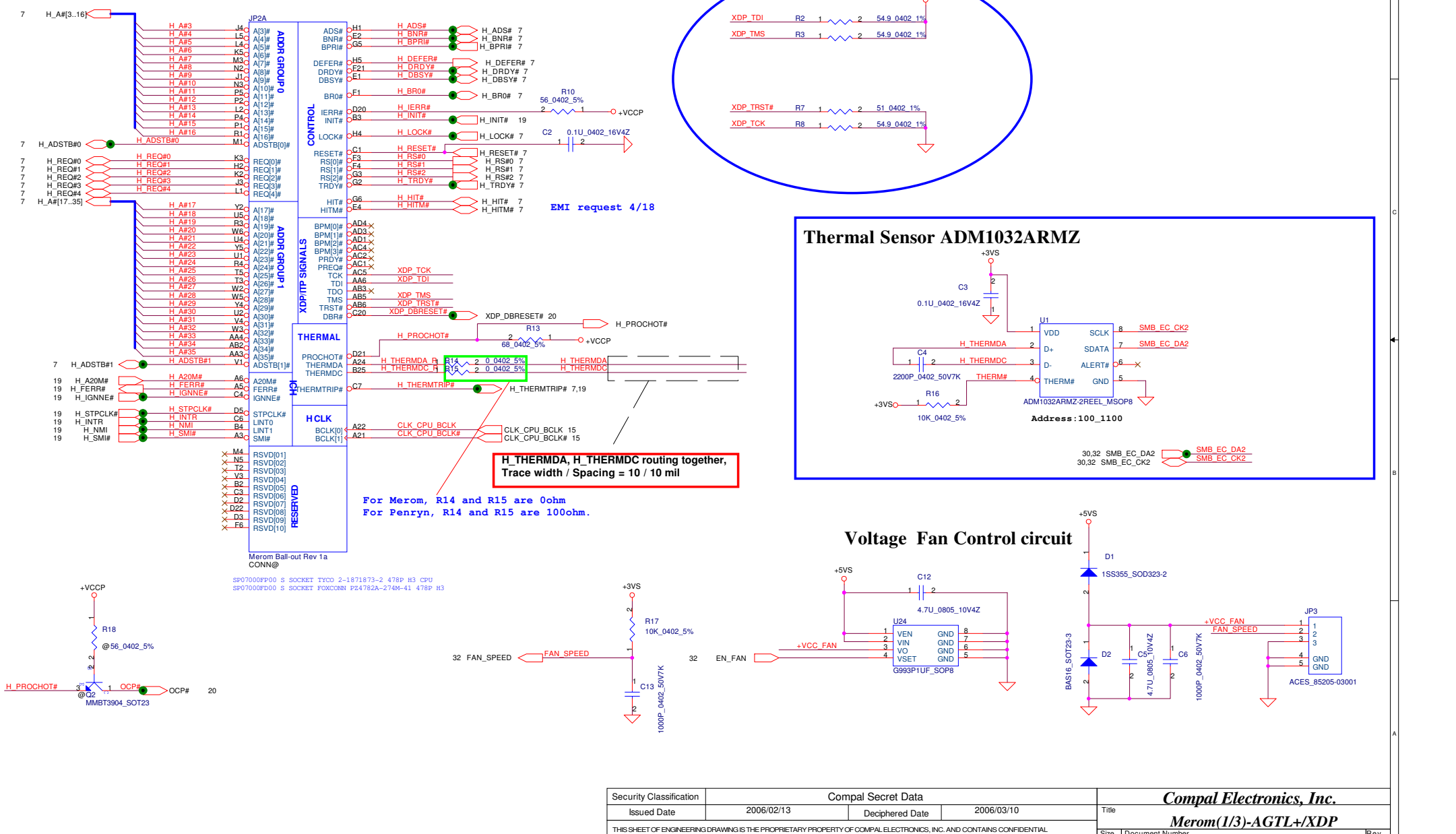

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.	
Title	Merom(1/3)-AGTL+/XDP
Size: Custom	Document Number: LA-3821P
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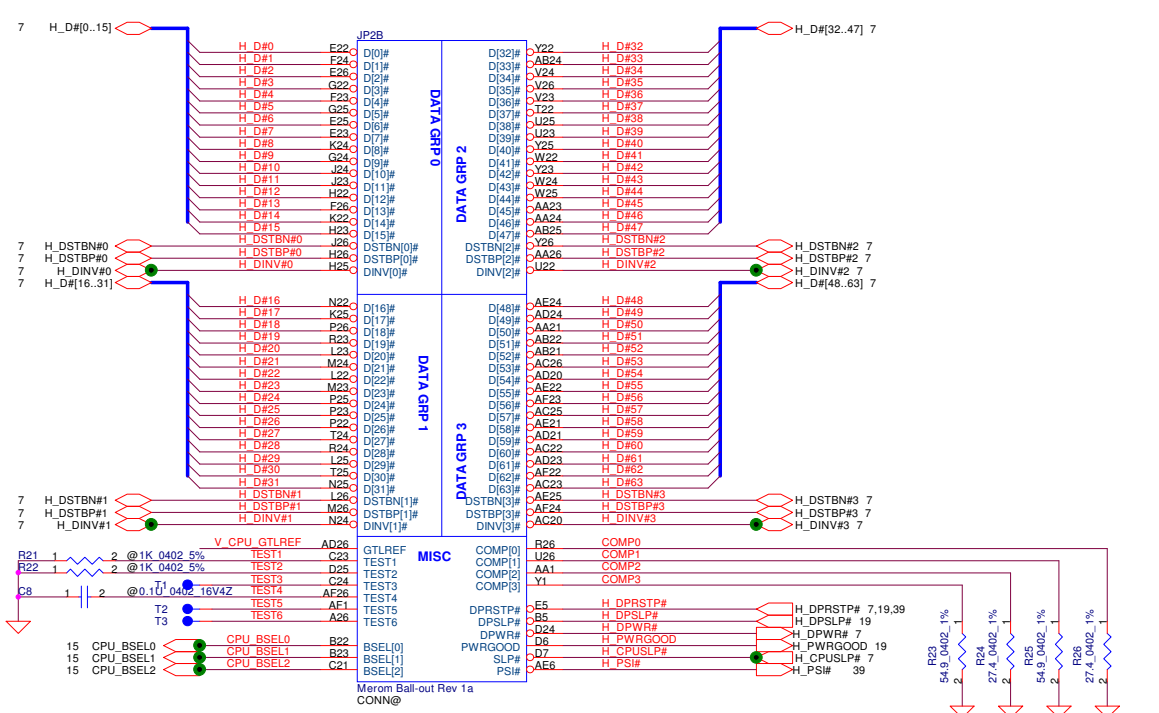
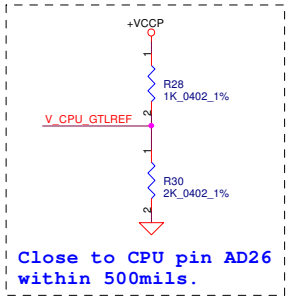


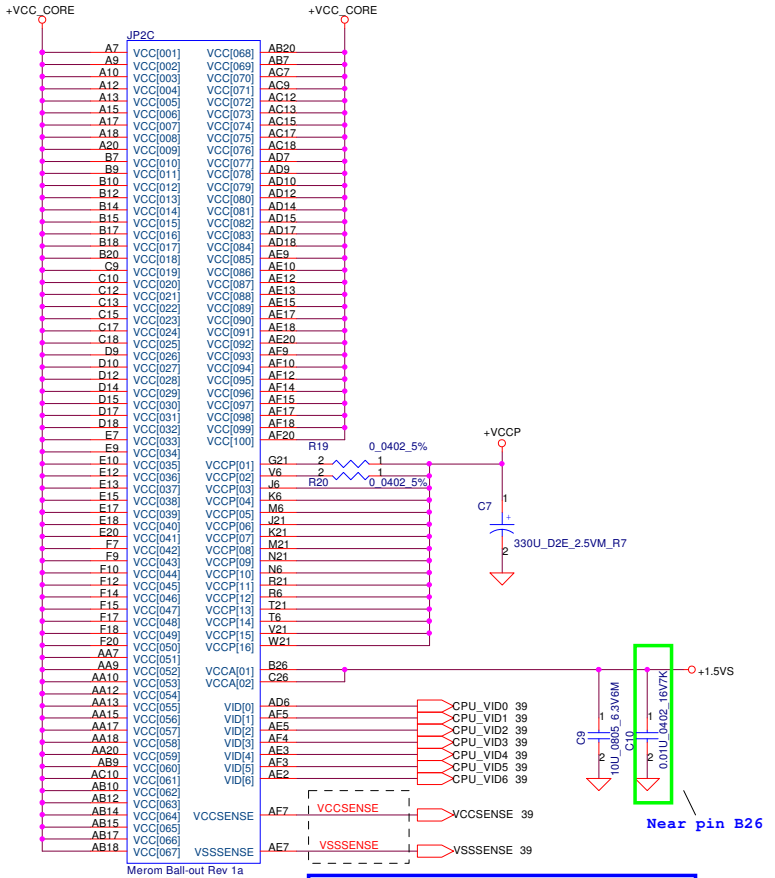
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

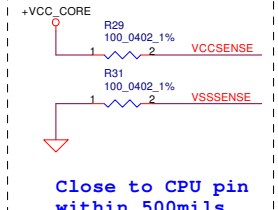
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal.
COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Close to CPU pin AD26 within 500mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

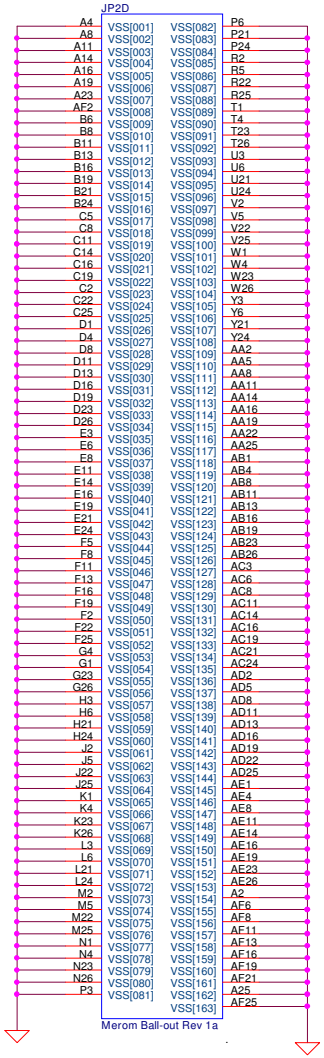
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

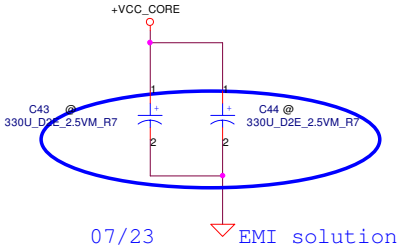
Title: Merom(2/3)-AGTL+/PWR

Size	Document Number	Rev
Custom	LA-3821P	0.3

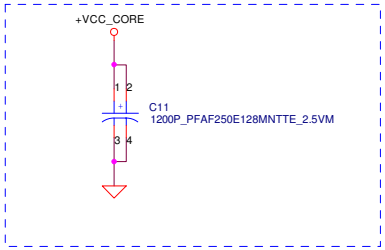
Date: Tuesday, July 31, 2007 Sheet 5 of 43



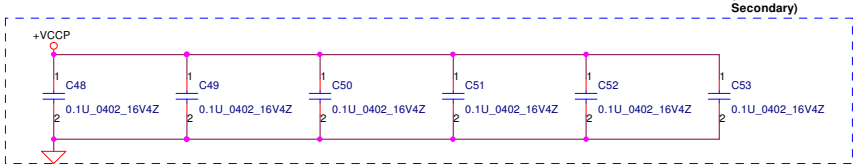
Near CPU CORE regulator



Proadlizer



Place these inside socket cavity on L8 (North side Secondary)



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.			
Title: Merom(3/3)-GND&Bypass			
Size: Custom	Document Number: LA-3821P		Rev: 0.3
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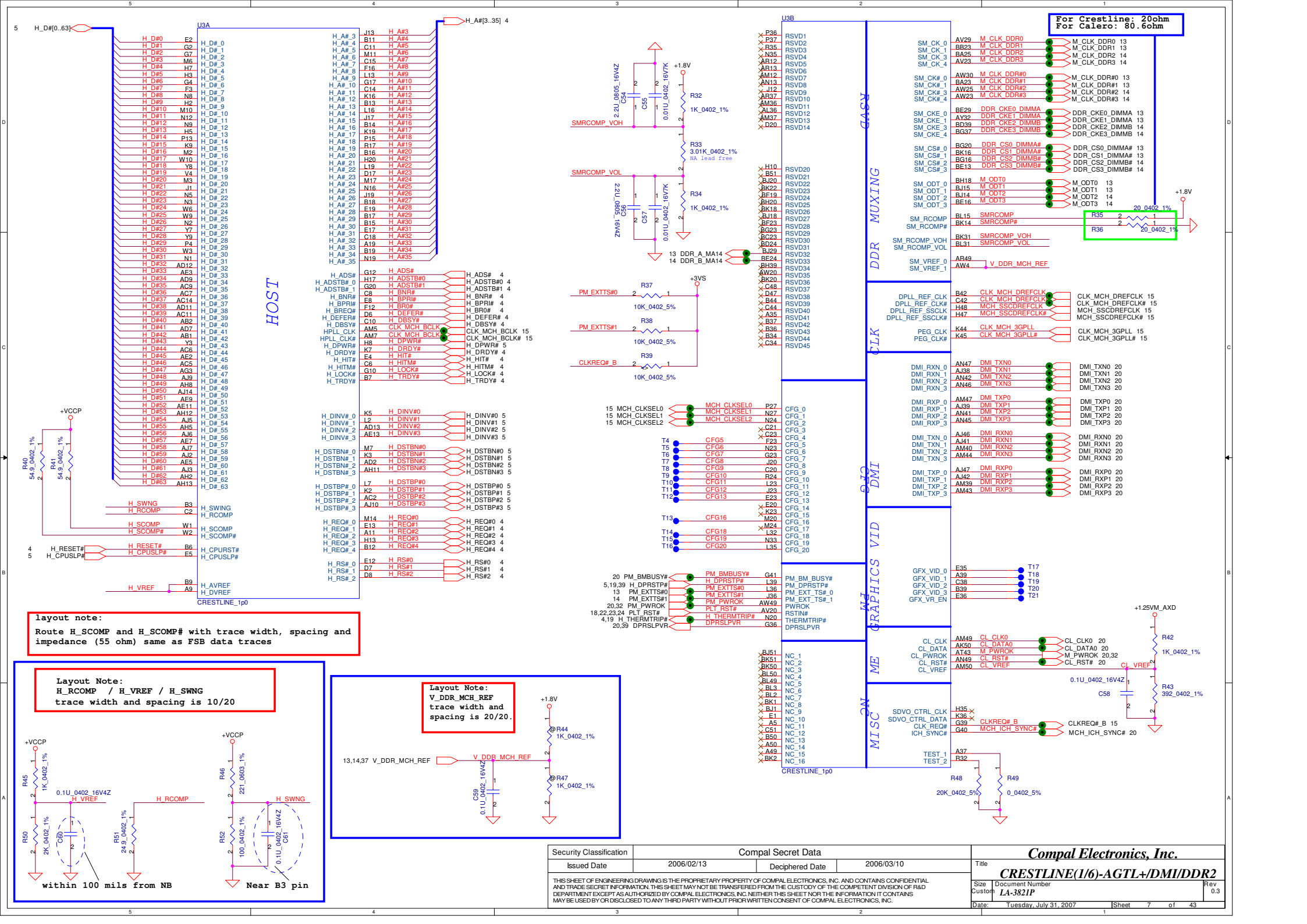
For Crestline: 20ohm
For Calero: 80.6ohm
HOST
CRESTLINE_1p0
DDR MUXING
CLK
DMI
GRAPHICS VID
MISC
PWR
layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces
Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20
within 100 mils from NB
Near B3 pin
Layout Note:
V_DDR_MCH_REF
trace width and
spacing is 20/20.
Security Classification
Compal Secret Data
Issued Date
2006/02/13
Deciphered Date
2006/03/10
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Title
CRESTLINE(1/6)-AGTL+/DMI/DDR2
Size
Custom
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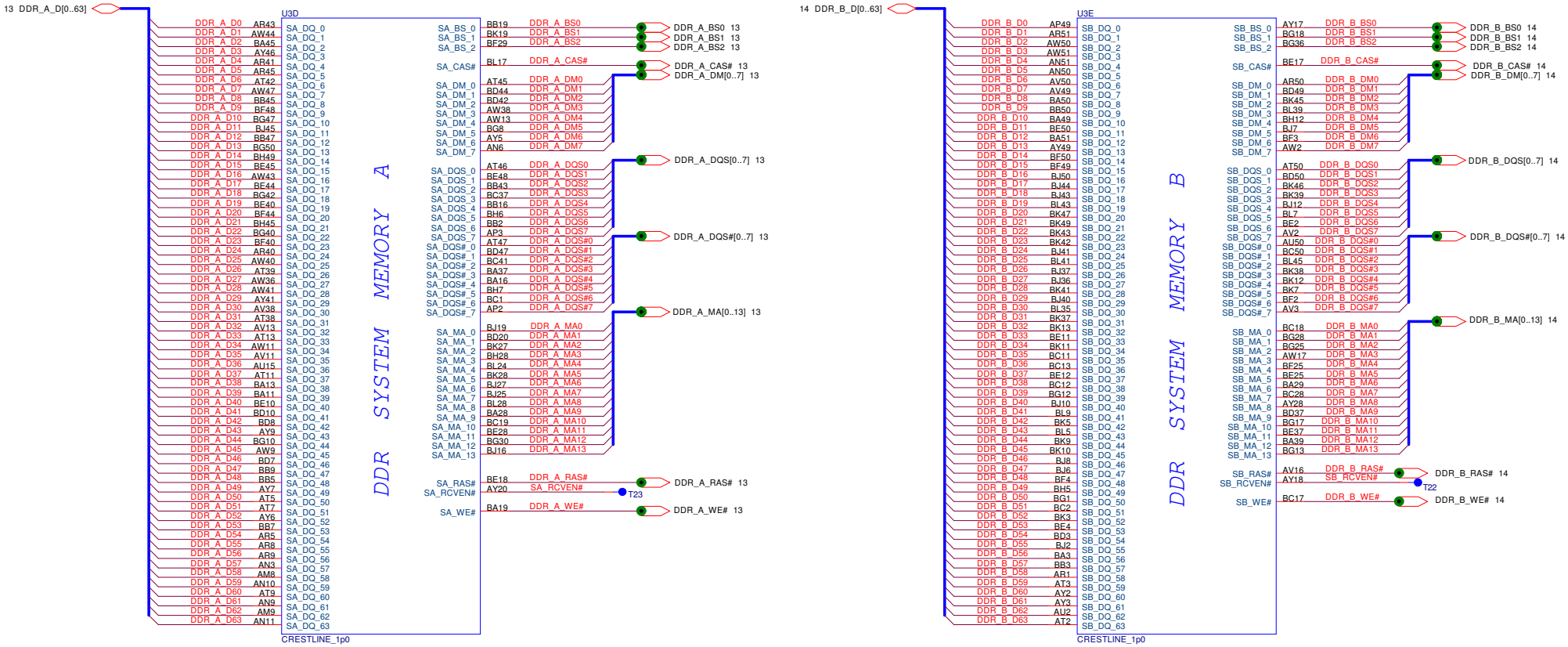

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **CRESTLINE((2/6)-DDR2 A/B CH**

Size	Document Number	Rev
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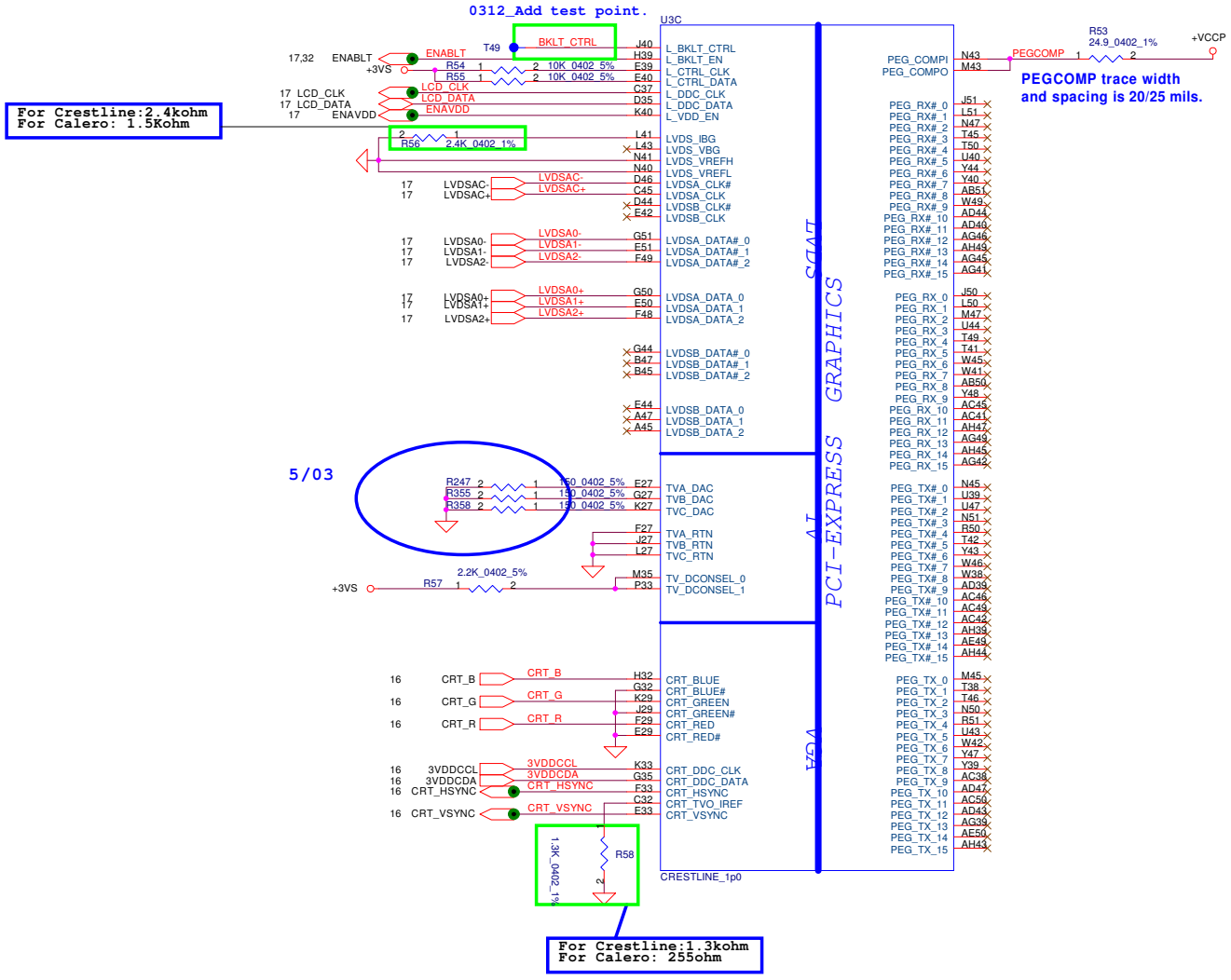

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

CFG[17:3] have internal pull up

CFG[19:18] have internal pull down

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Compal Electronics, Inc.

Title: CRESTLINE((3/6)-VGA/LVDS/TV

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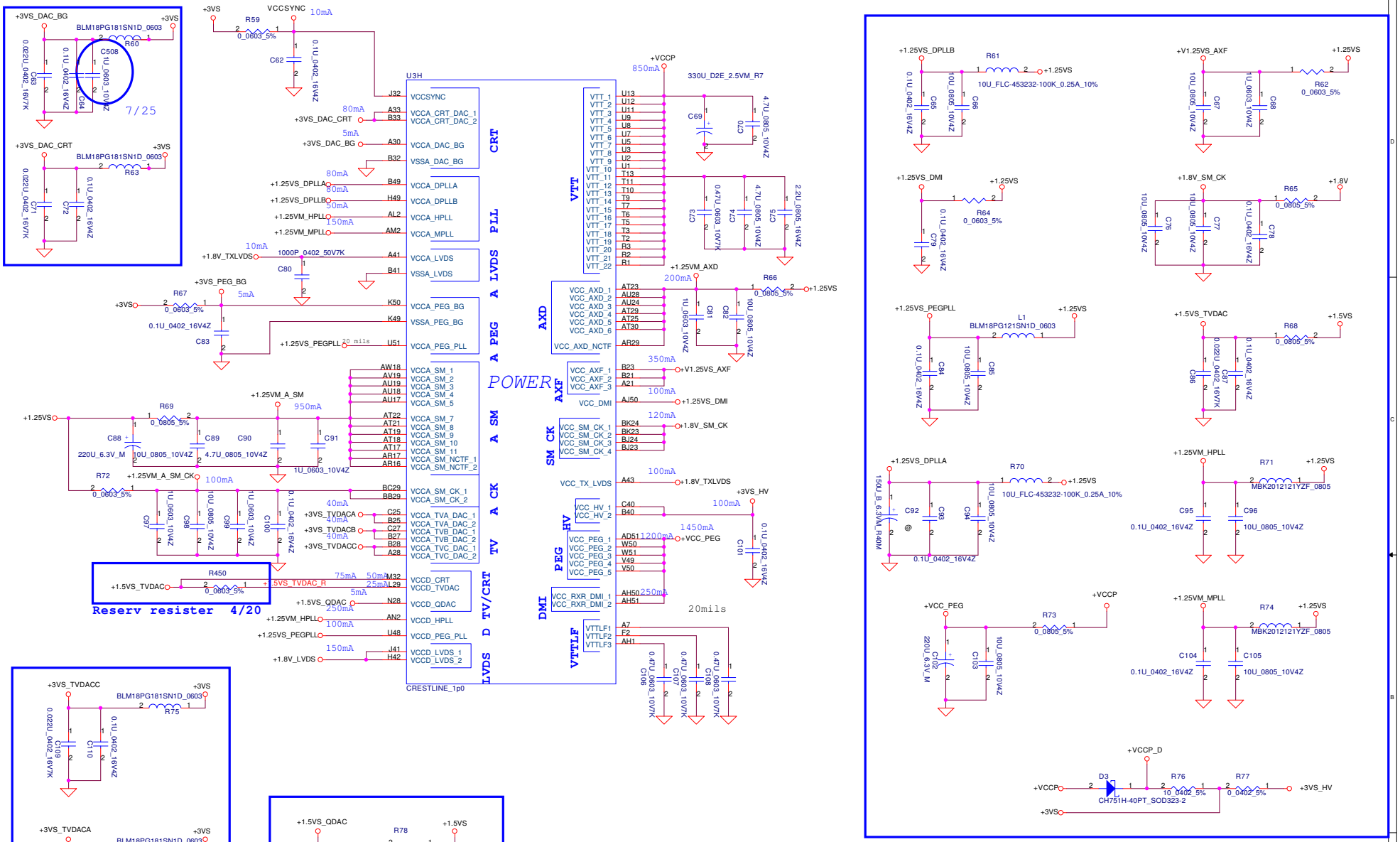

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Title	*Compal Electronics, Inc.*
	CRESTLINE(4/6)-PWR
Size: Custom	Document Number: *LA-3821P*
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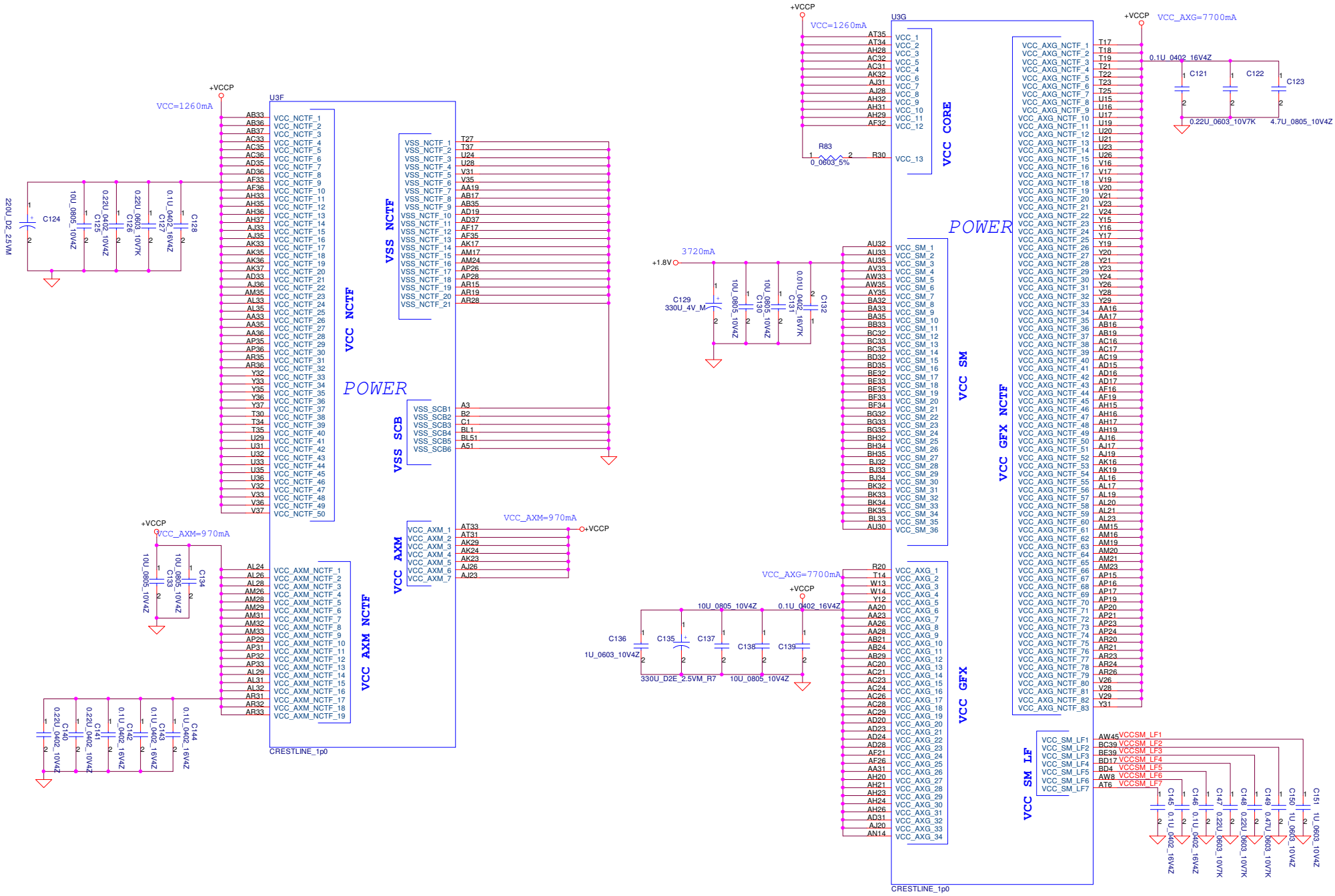

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Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **CRESTLINE((5/6)-PWR/GND**

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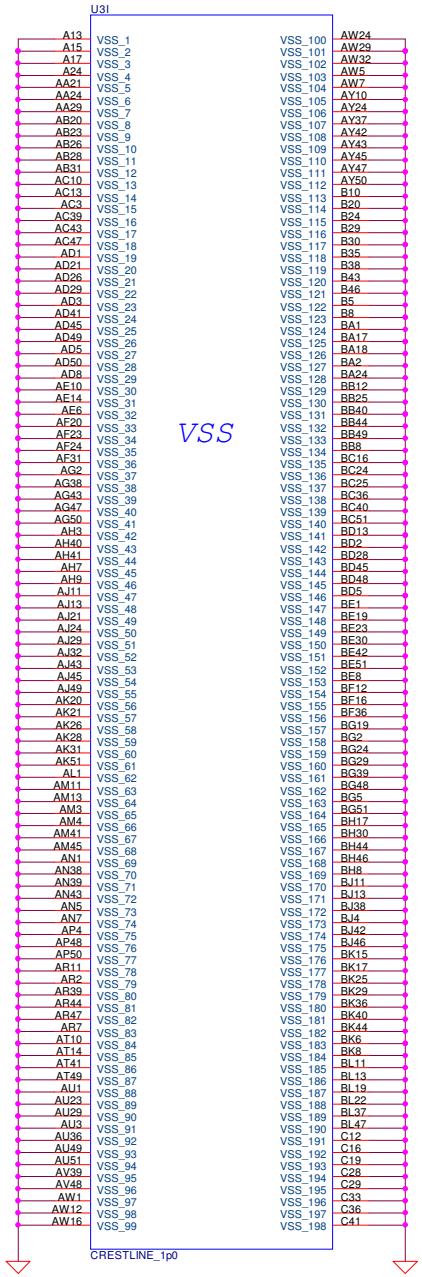

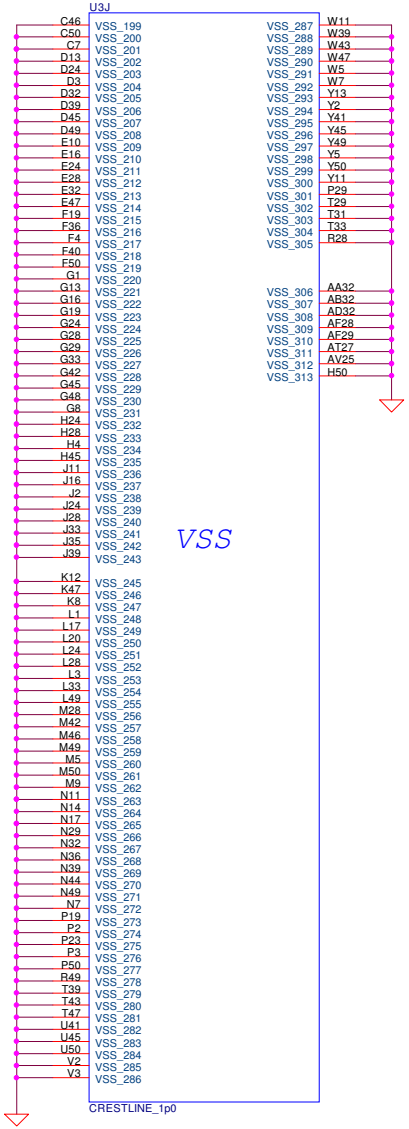

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Compal Electronics, Inc.

Title: **CRESTLINE((6/6)-PWR/GND**

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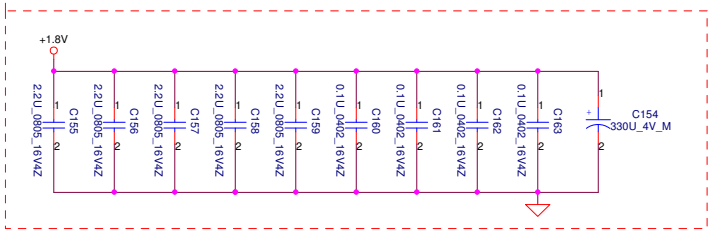
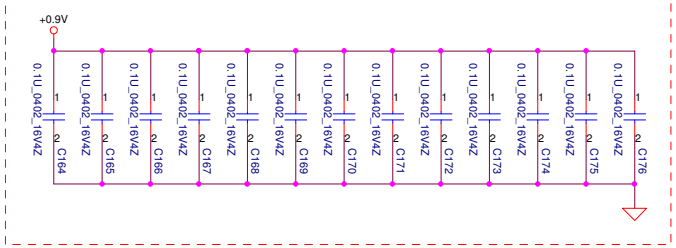
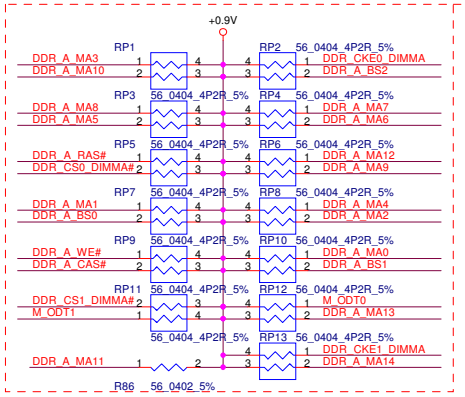
8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
7,8 DDR_A_MA[0..14]

Layout Note:
Place near JP34

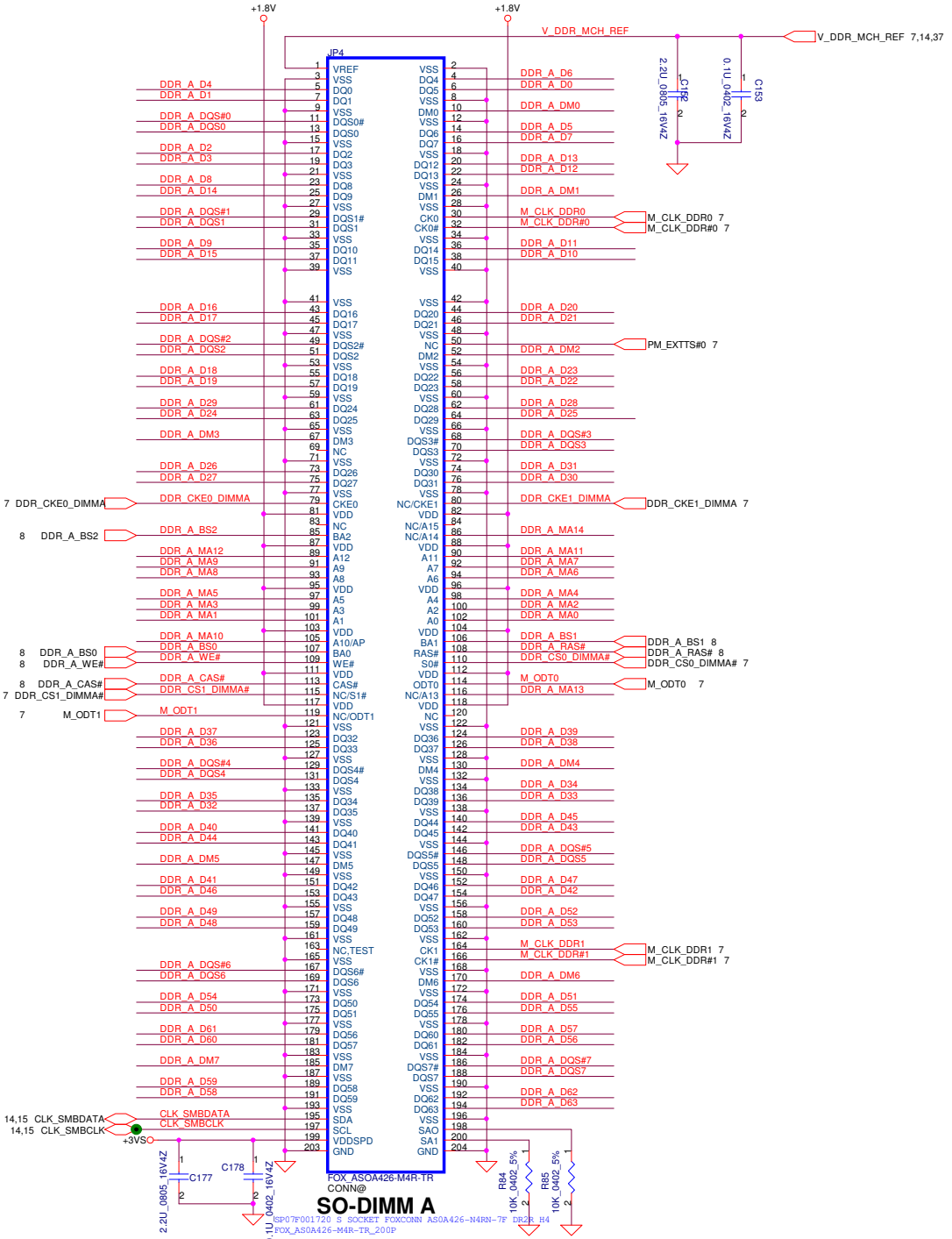


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS





Layout Note:
Place these resistor closely JP34,all trace length Max=1.5"



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Title	*Compal Electronics, Inc.*		
	DDRII-SODIMM SLOT1		
Size: Custom	Document Number: *LA-3821P*		Rev: 0.3
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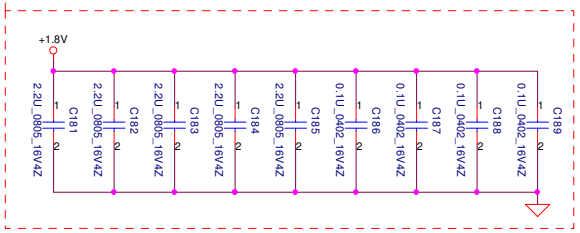
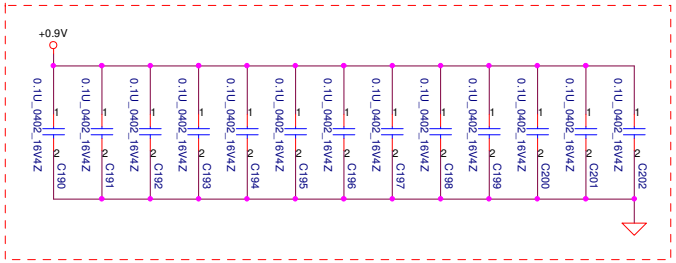
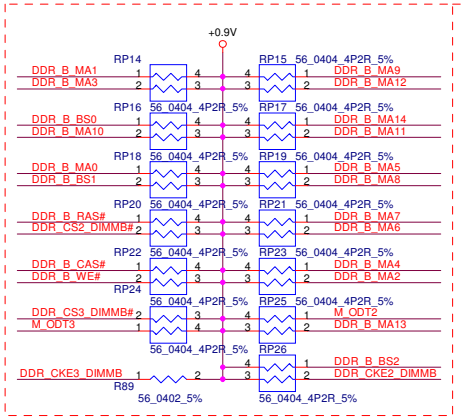
8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
7,8 DDR_B_MA[0..14]

Layout Note:
Place near JP10

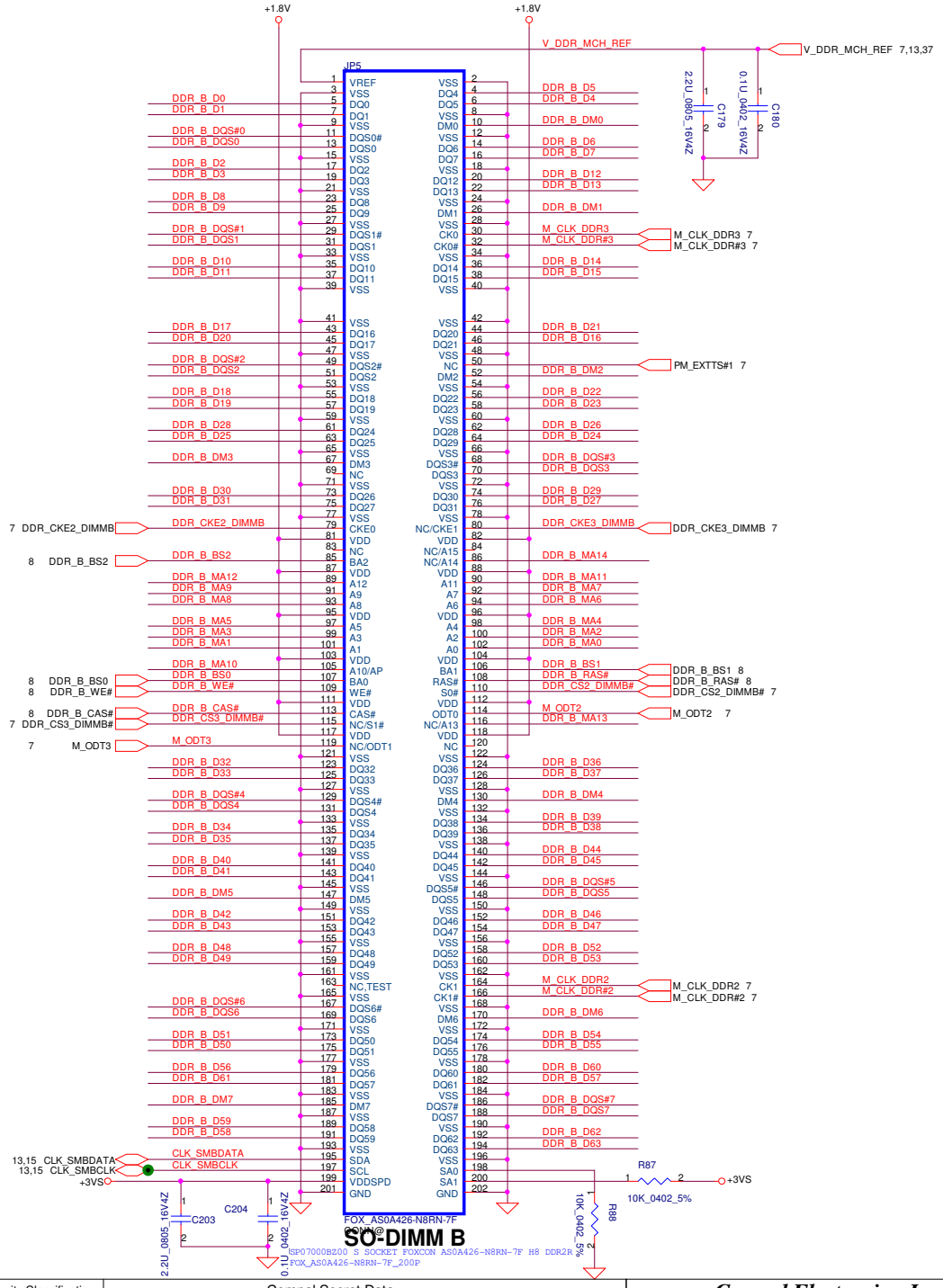


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS





Layout Note:
Place these resistor closely JP10,all trace length Max=1.5"



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Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT2

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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R1107	R1135	R1083			
*(Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139
667MHz	Stuff	R1086	R1139	R1135	R1074	R1139	R1135
	No Stuff	R1083	R1107	R1128			
		R1113	R1098				
800MHz	Stuff	R1135	R1139				
	No Stuff	R1083	R1086	R1098	R1128		
		R1074	R1107	R1113			

Place close to U4

0308_Change R89 and R92 form 0 ohm to bead, C209, C211, C216, C218 from 0.1uF to 680pF.

SB, MINI PCI

CLRP4,CLRP5 for 667/800 FSB select
SHORT CLRP5, NO SHORT CLRP4 -- CPU option
SHORT CLRP4, NO SHORT CLRP5 -- FSB 667

0301_Change R105 from 22 ohm to 0 ohm.
0312_Change R106, 107, 109 from 22 to 33 ohm.

Routing the trace at least 10mil

New card WLAN clock REQ

Mini card Robeson clock REQ

Mini card WLAN clock REQ

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1= Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

For Layout request:
1. Change MINI_CLKREQ# from pin 32 to pin 43.
2. Change CLK_PCIE_MCARD from SRC9 to SRC6.

* Internal Pull-Up Resistor
** Internal Pull-Down Resistor

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Compal Electronics, Inc.

Title: Clock generator

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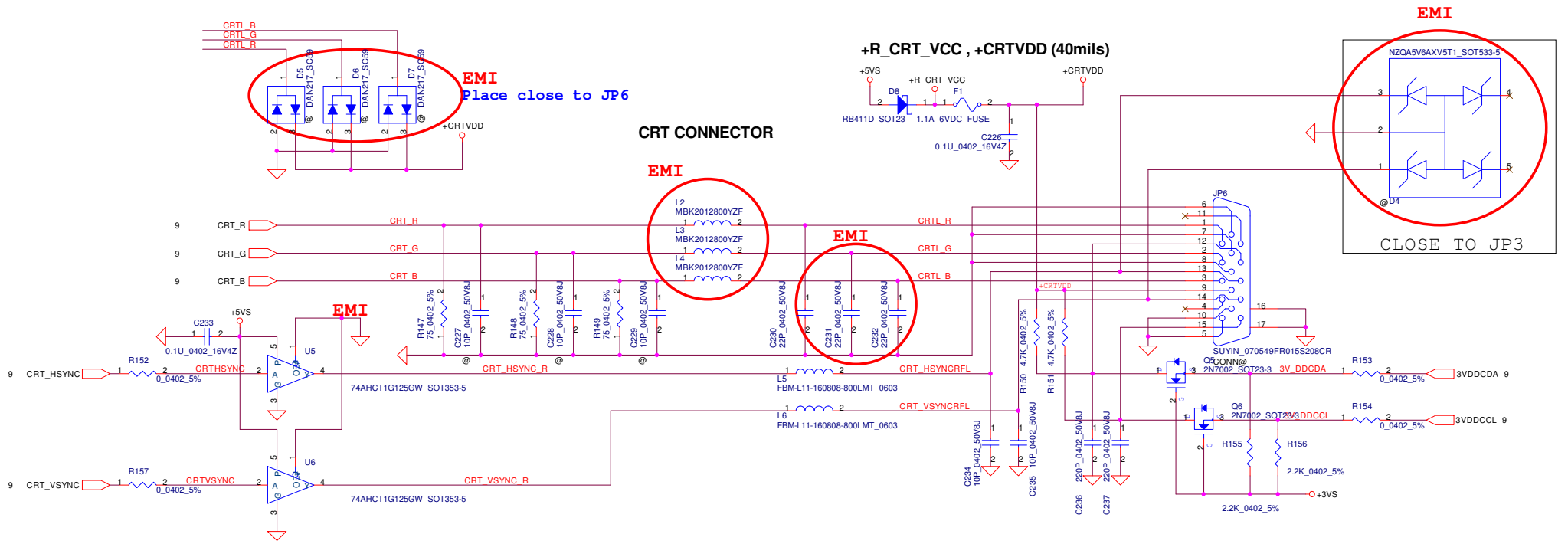

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Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: CRT & TVout Connector			
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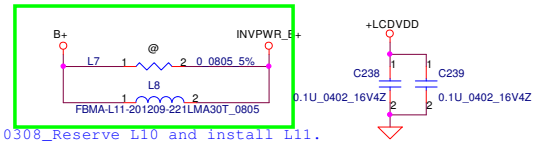
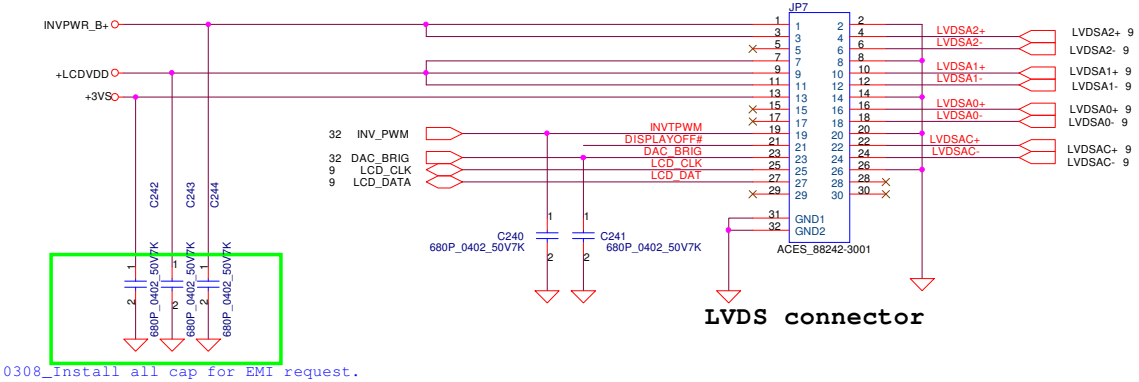
LVDS CONN

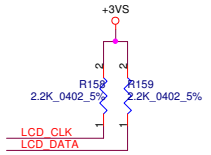


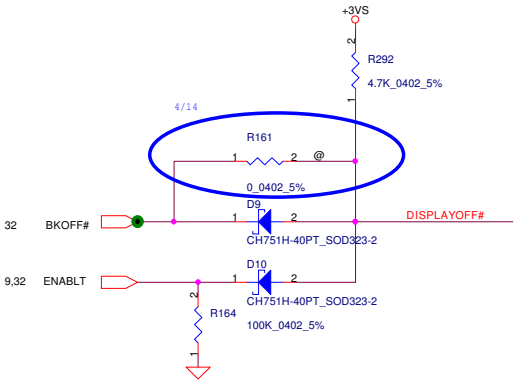
0308_Reserve L10 and install L11.

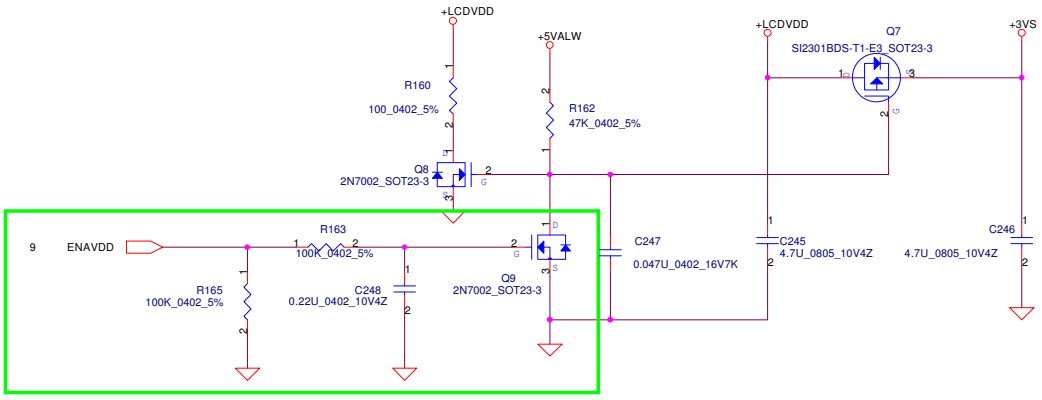


LVDS connector

0308_Install all cap for EMI request.







Avoid Panel display garbage after power on.

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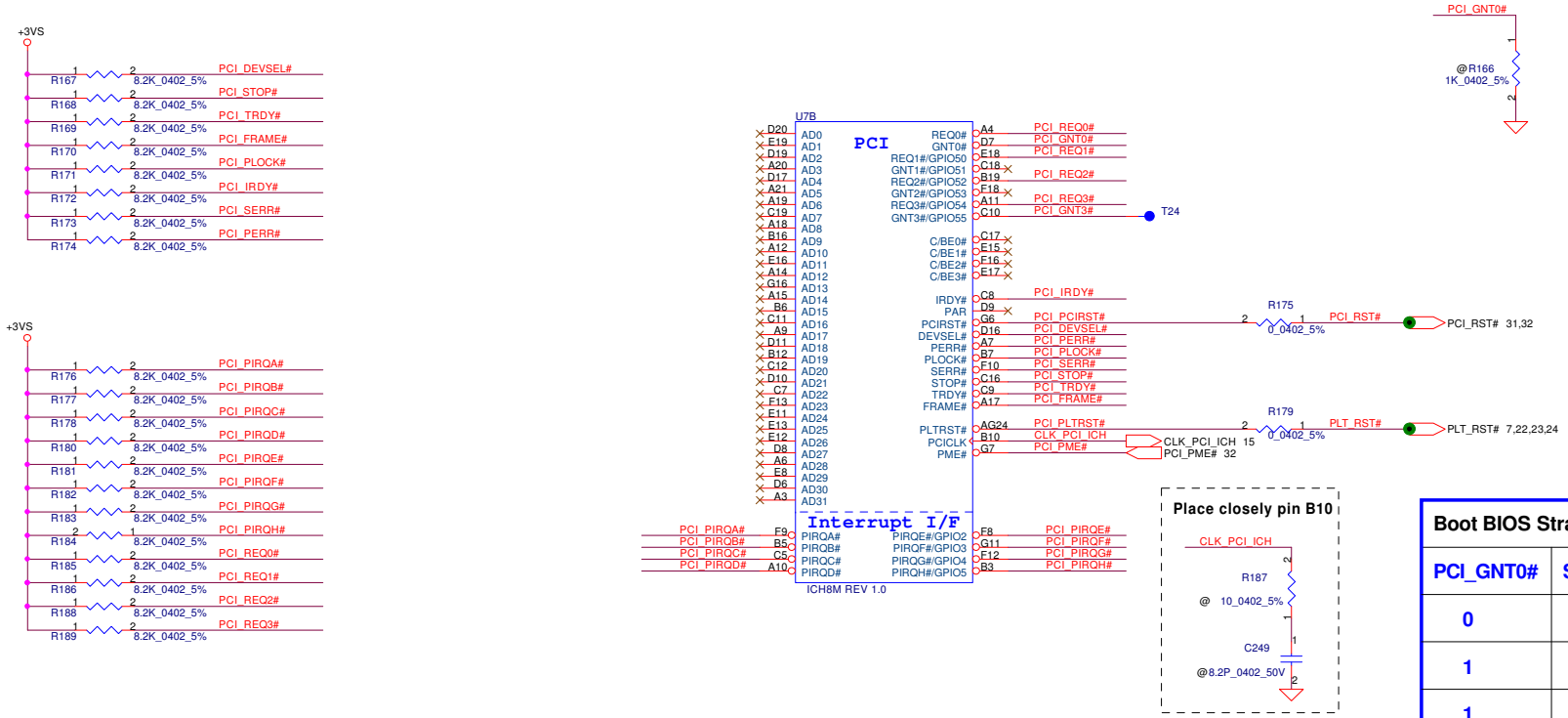
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: LCD CONN.			
Size	Document Number: LA-3821P		Rev: 0.3
Date: Tuesday, July 31, 2007	Sheet 17 of 43		



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

A16 swap override Strap	
PCI_GNT3#	*Low= A16 swap override Enble High= Default

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.			
Title: ICH8(1/4)-PCI/INT			
Size	Document Number: LA-3821P		Rev: 0.3
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ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)

ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

0205_Change Crystal type.

0420_Change RTC battery to power part

within 2" from R1557

placed within 2" from ICH8M

All trace 20mils

Within 500 mils

ICH8M REV 1.0

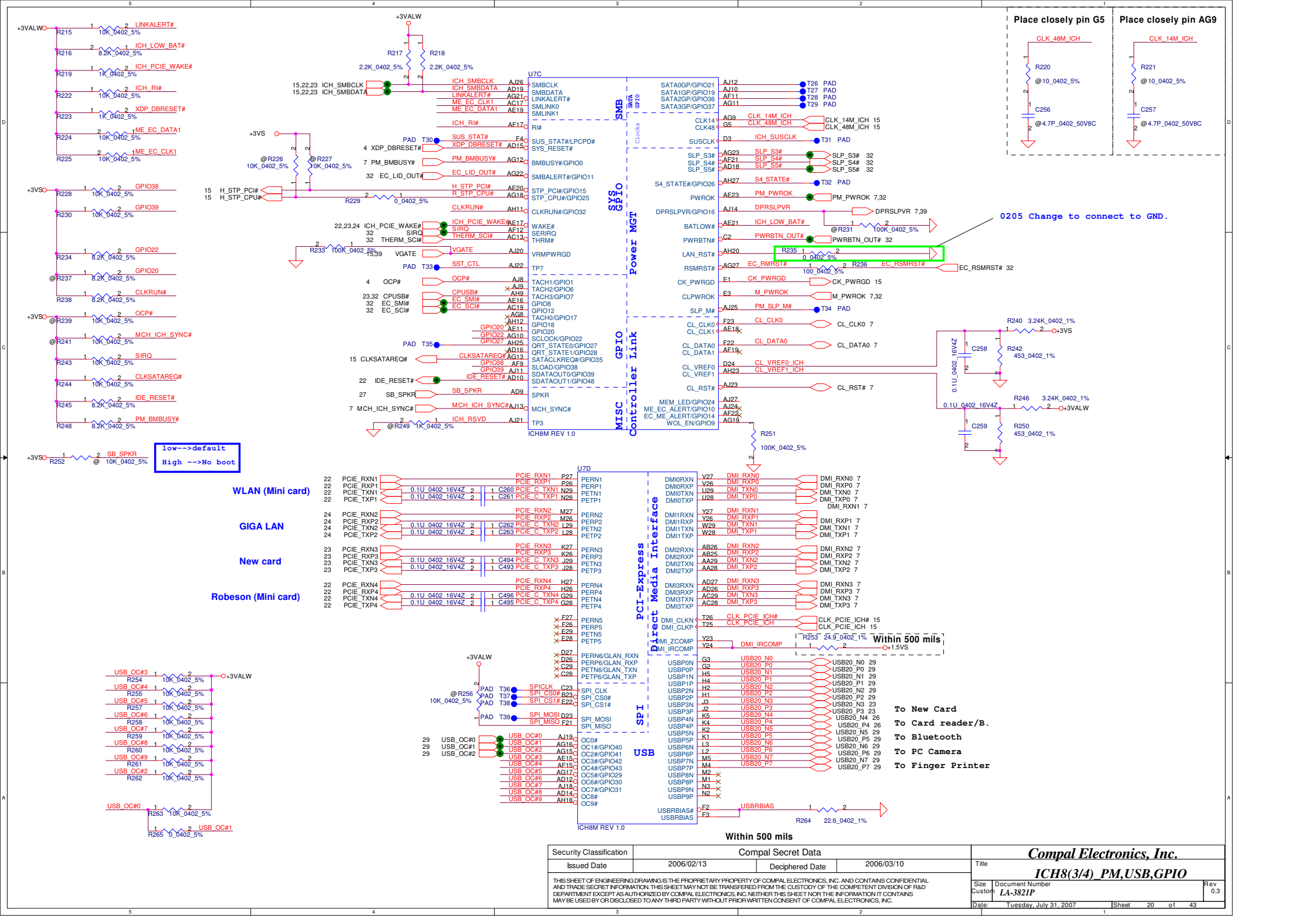
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: ICH8(2/4)_LAN,HD,IDE,LPC

Size: Custom | Document Number: LA-3821P | Rev: 0.3

Date: Tuesday, July 31, 2007 | Sheet 19 of 43



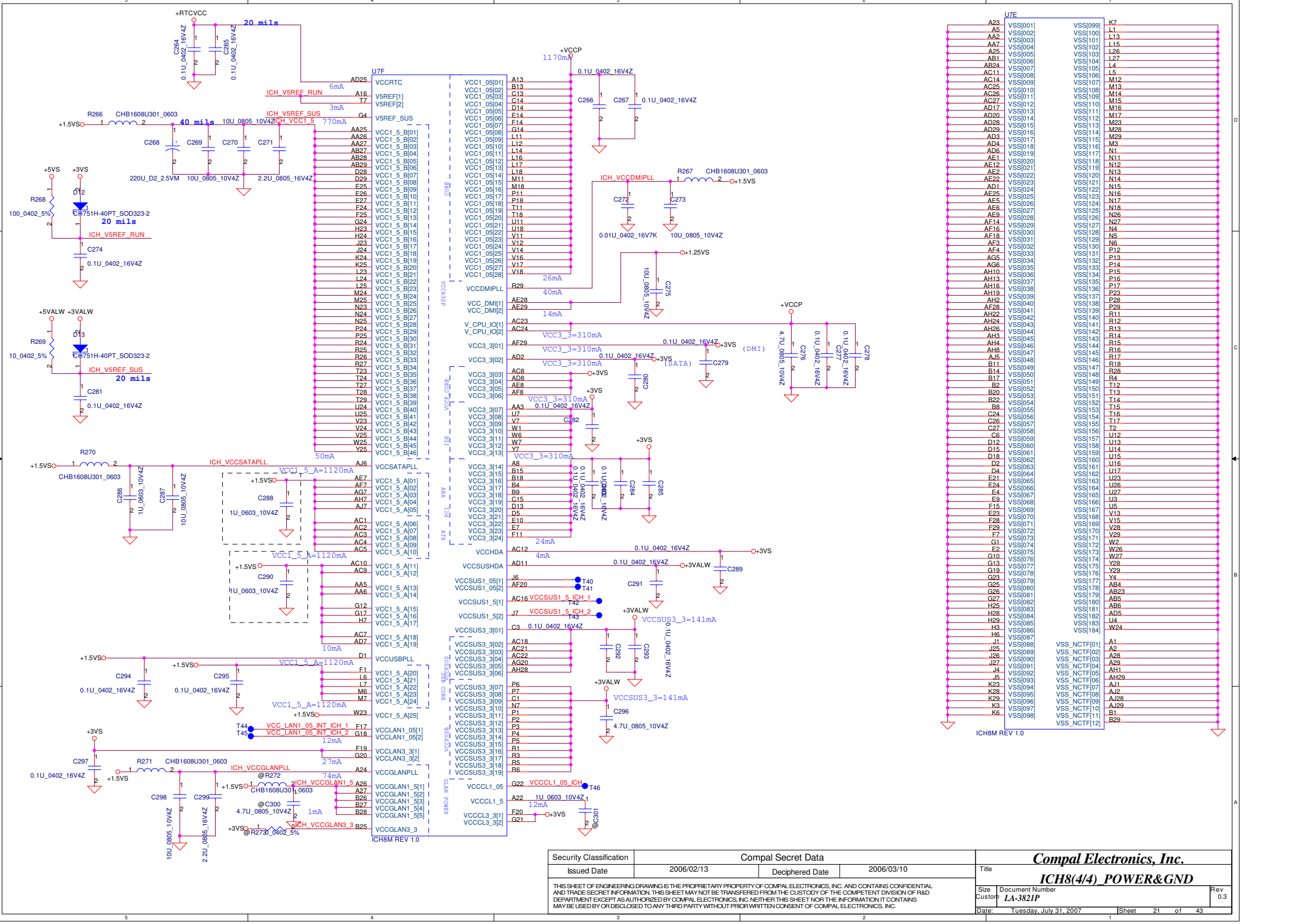
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **ICH8(3/4)_PM,USB,GPIO**

Size	Document Number	Rev
Custom	LA-3821P	0.3

Date: Tuesday, July 31, 2007 Sheet 20 of 43



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

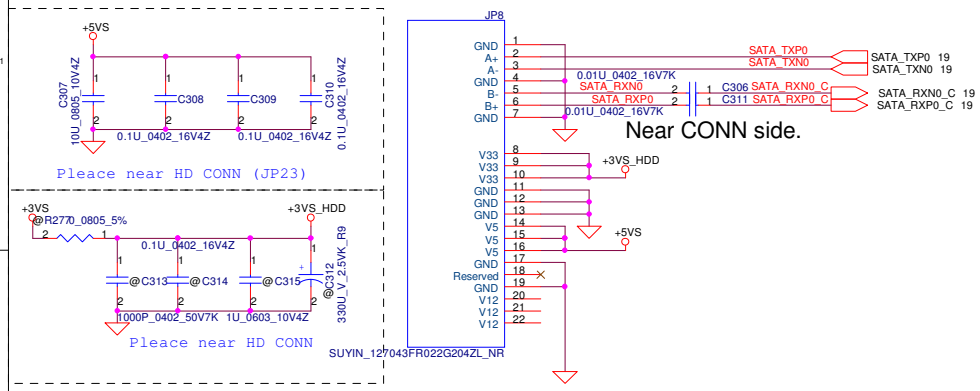
Compal Electronics, Inc.

Title: **ICH8(4/4)_POWER&GND**

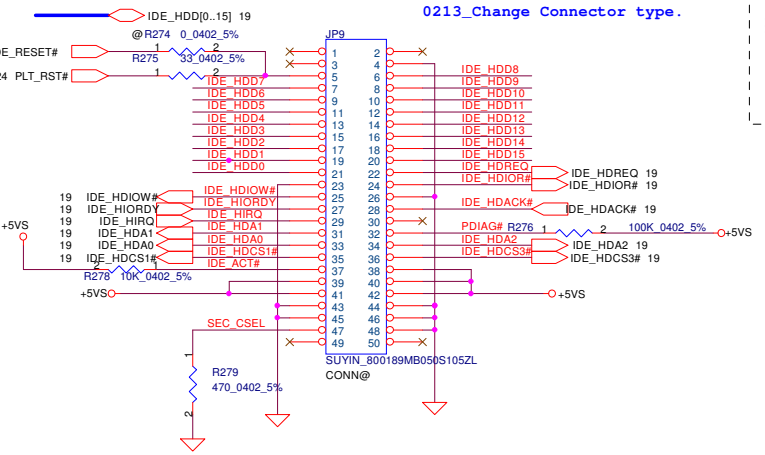
Size	Document Number	Rev
Custom	LA-3821P	0.3

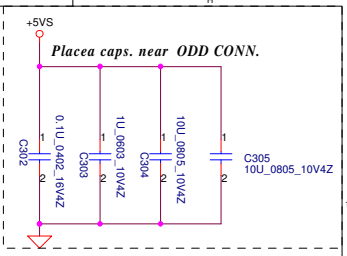
Date: Tuesday, July 31, 2007 Sheet 21 of 43

HDD Connector



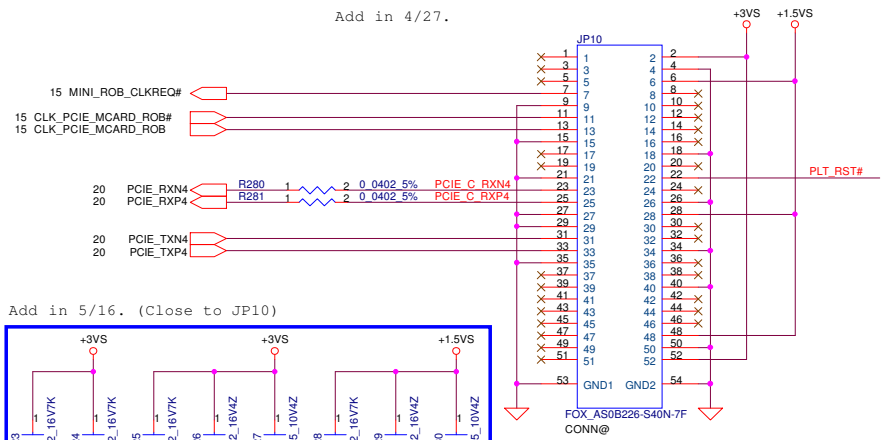
CD-ROM Connector



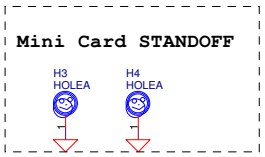


NAND mini Card(Robson support)

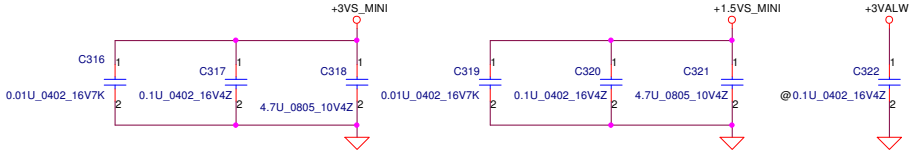
Add in 4/27.

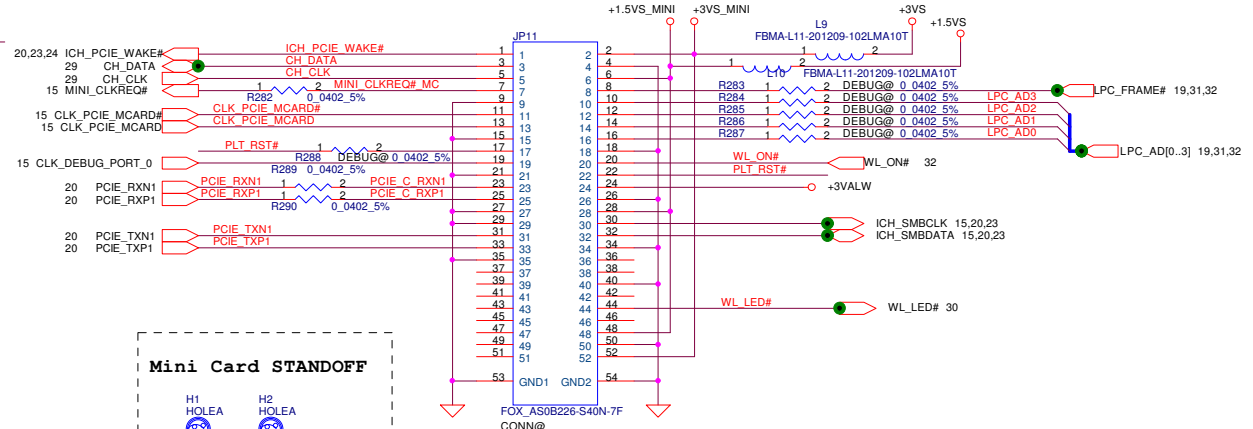


Add in 5/16. (Close to JP10)



Mini-Express Card---WLAN

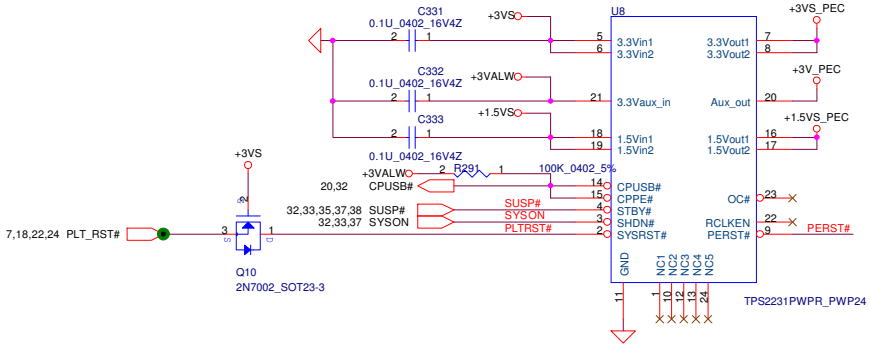


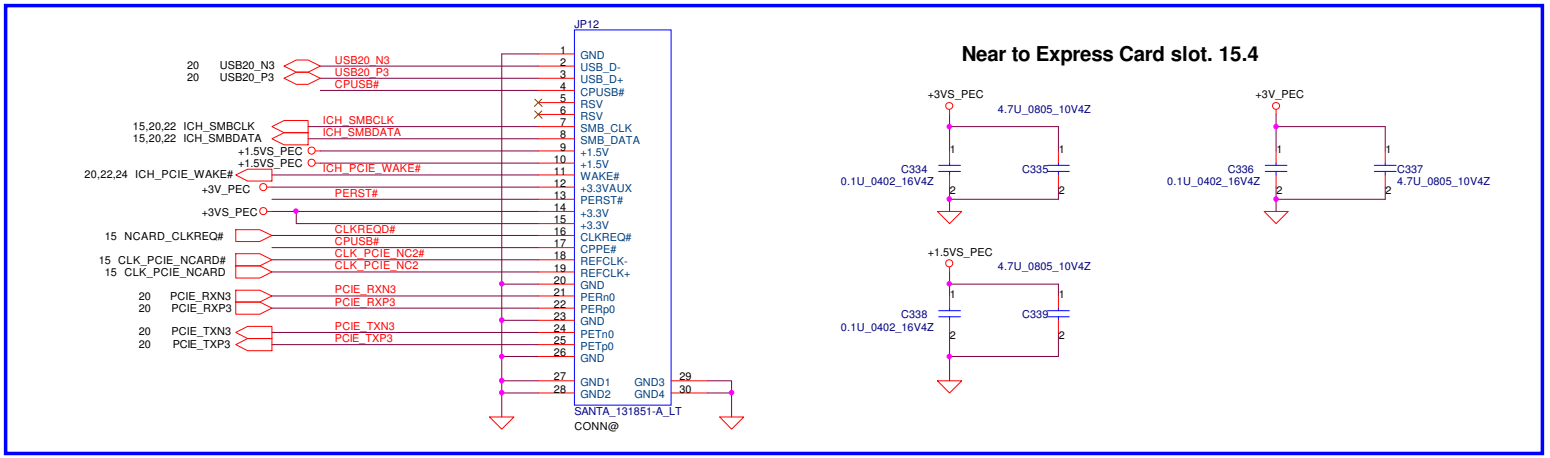


Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2007/08/29

Compal Electronics, Inc.			
Title: HDD/ODD/Mini Card CONN.			
Size	Document Number: LA-3821P		Rev: 0.3
Date: Tuesday, July 31, 2007		Sheet 22 of 43	

Express Card Power Switch





Near to Express Card slot. 15.4

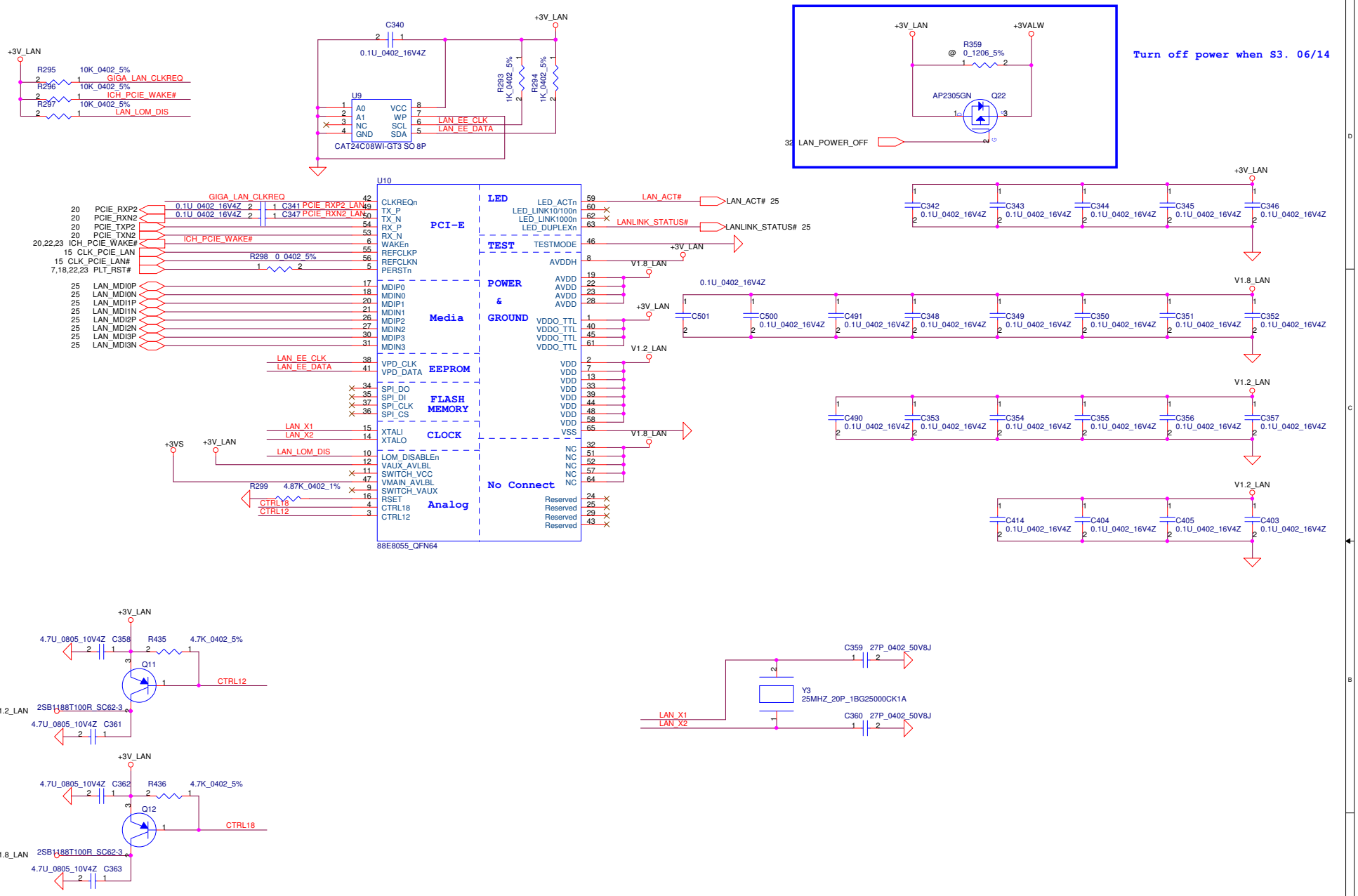
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Express Card**

Size	Document Number	Rev
Custom	LA-3821P	0.3

Date: Tuesday, July 31, 2007 | Sheet 23 of 43



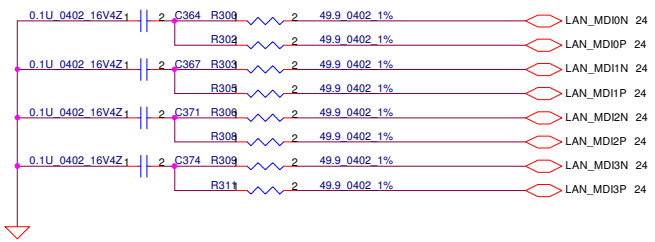
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2007/08/29

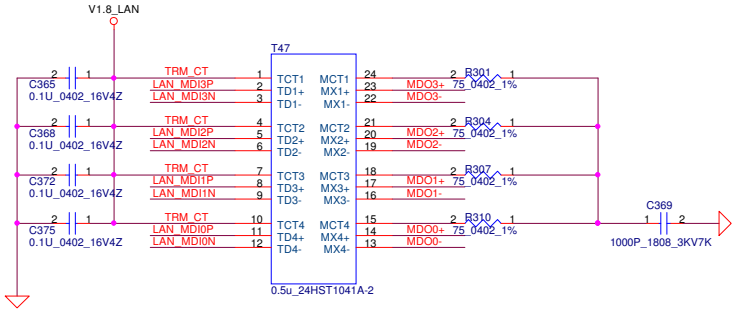
Compal Electronics, Inc.

Title: **LAN-8100CL**

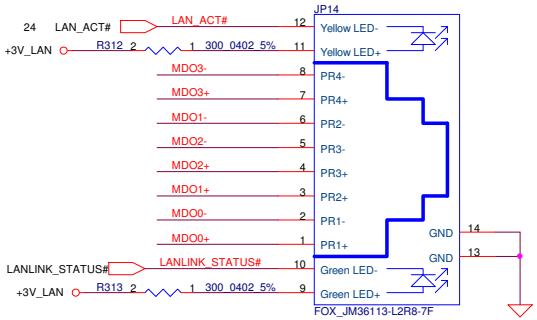
Size	Document Number	Rev
	LA-3821P	0.3

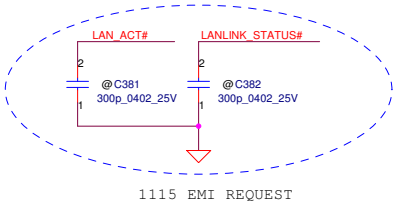
Date: Tuesday, July 31, 2007 | Sheet 24 of 43



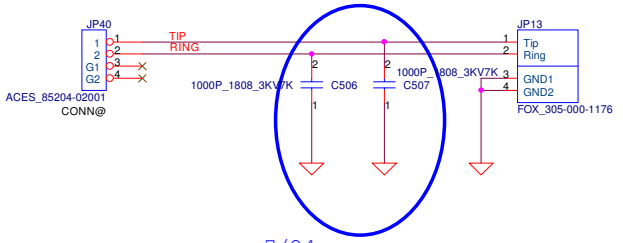


Note: MDO[3..0]+/- signals should route to JP13 first then to JP30.





1115 EMI REQUEST

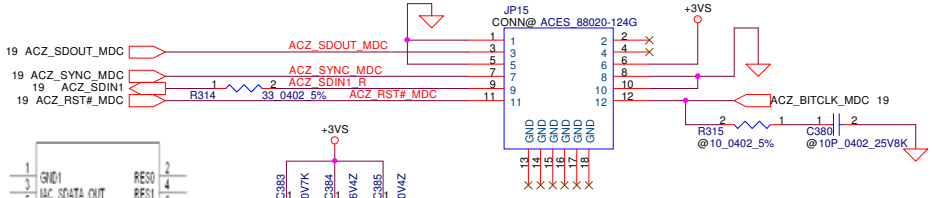


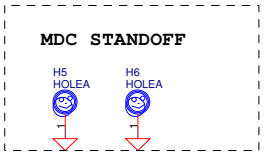
RJ11

7/24

MDC 1.5 Conn.

Change type 4/25





Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: Magnetic & RJ45/RJ11			
Size	Document Number: LA-3821P		Rev: 0.3
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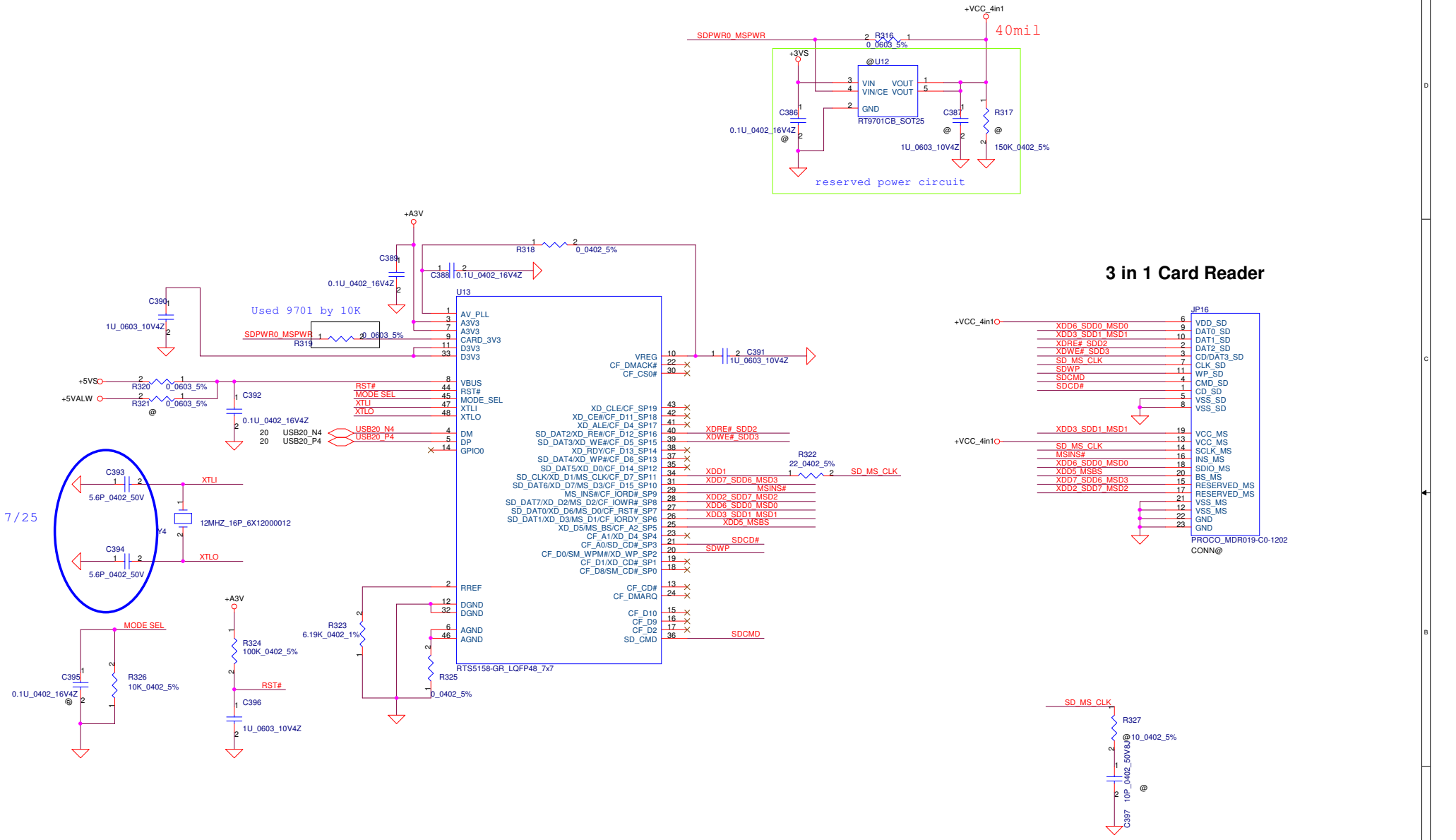
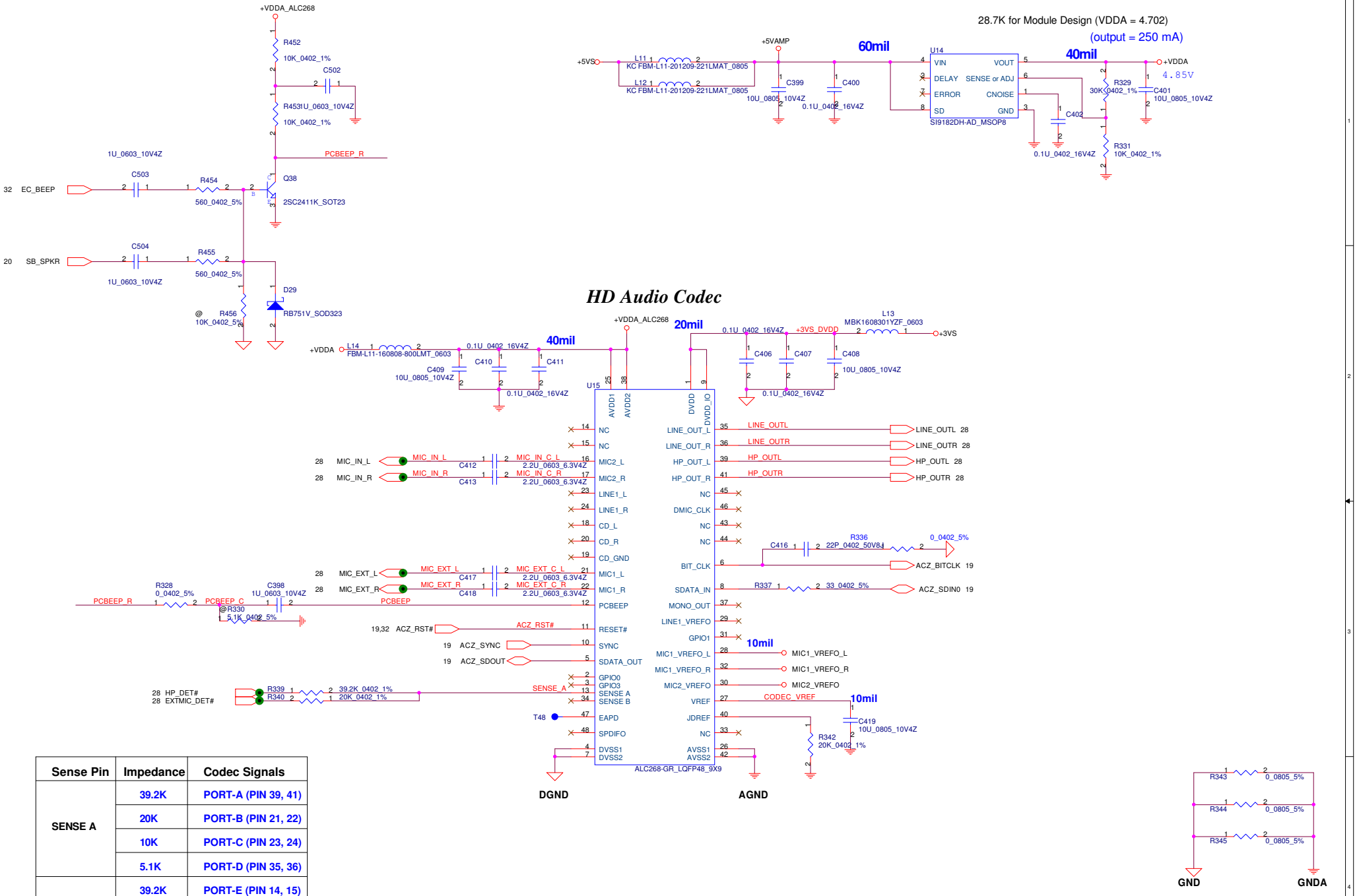


Compal Electronics, Inc.		
Title: Card reader board		
Size	Document Number: LA-3821P	Rev: 0.3
Date: Tuesday, July 31, 2007	Sheet 26 of 43	



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: HD Audio Codec ALC268

Size	Document Number	Rev
B	LA-3821P	0.3

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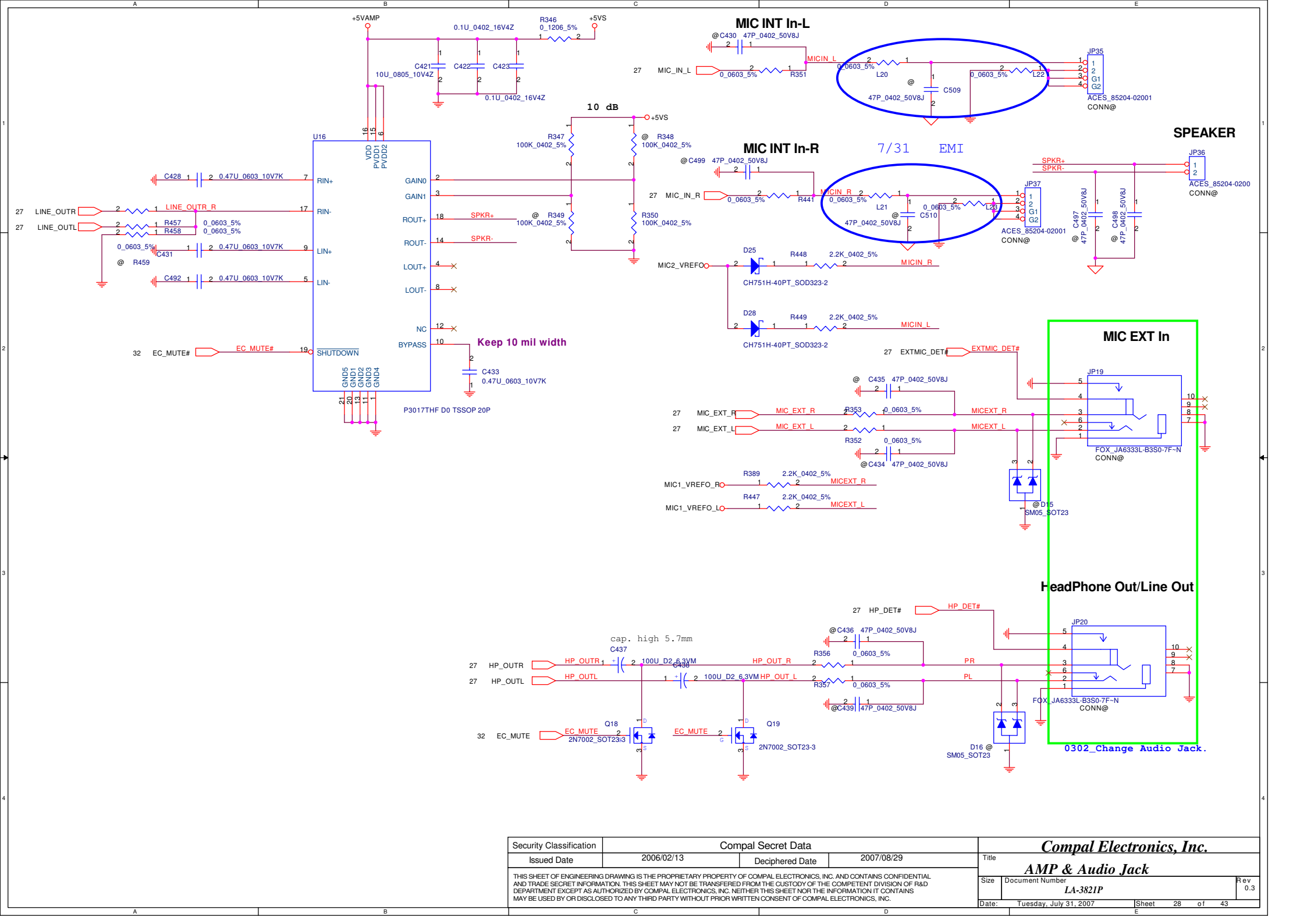

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2007/08/29

Compal Electronics, Inc.

Title: **AMP & Audio Jack**

Size	Document Number	Rev
	LA-3821P	0.3

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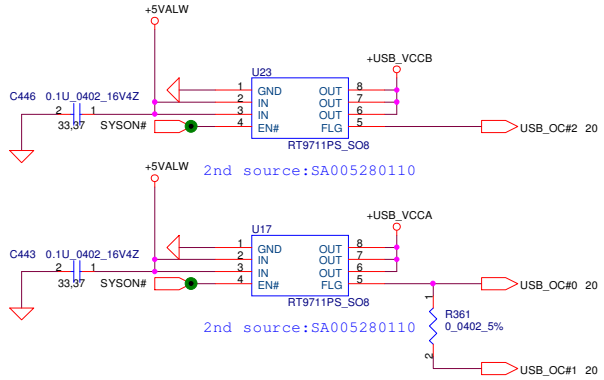
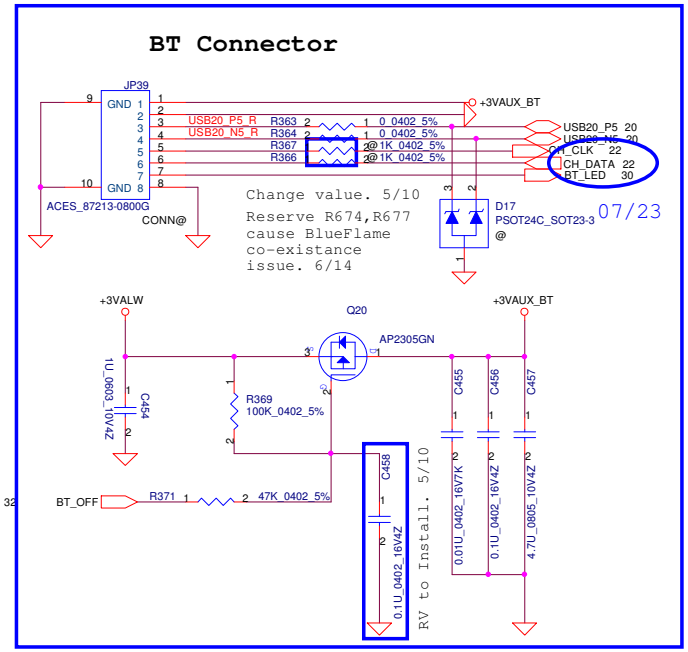
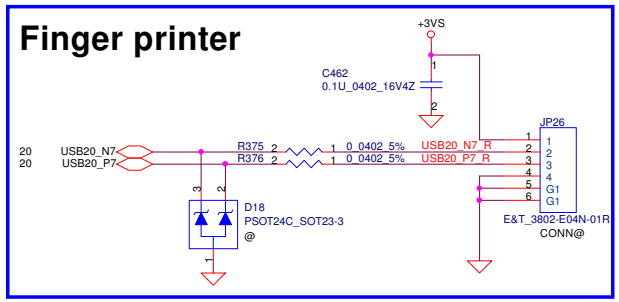


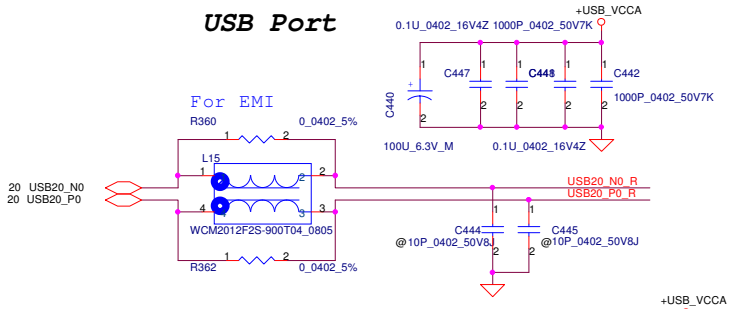
BT Connector

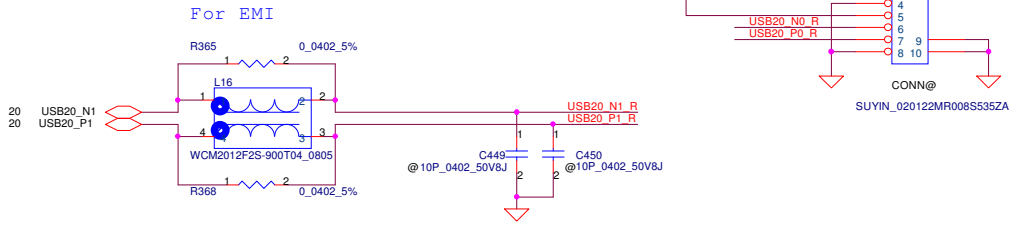


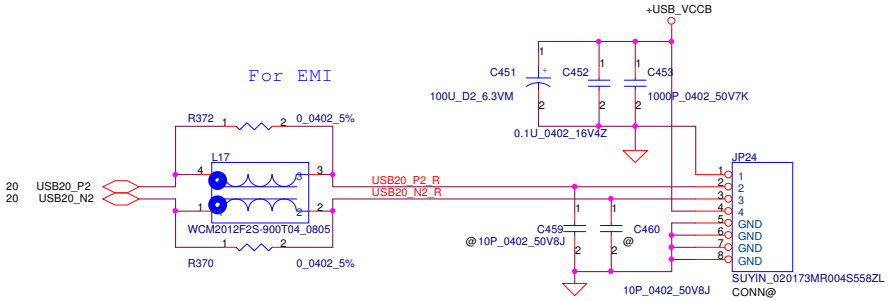
Finger printer



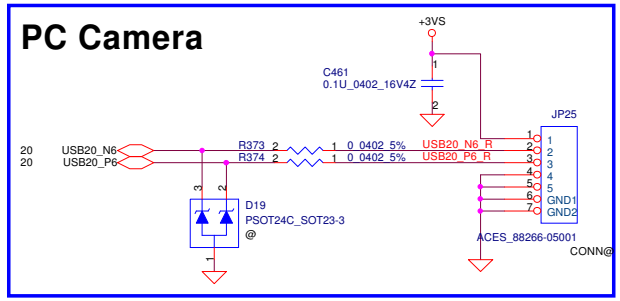
USB Port







PC Camera



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: USB CONN.			
Size	Document Number: LA-3821P		Rev: 0.3
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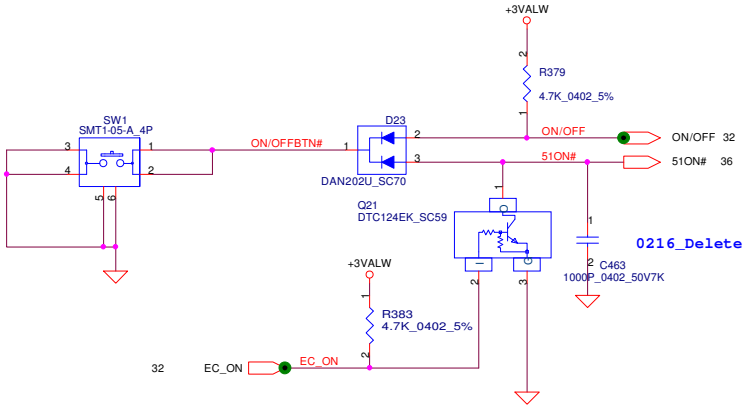
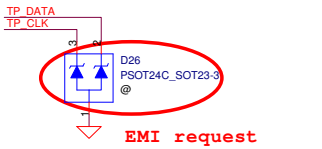
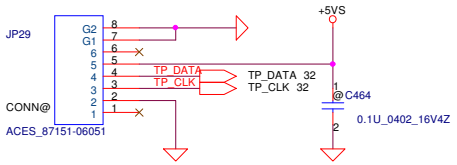
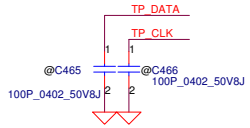
Power ON/OFF

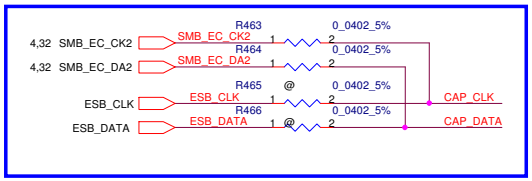


T/P Board

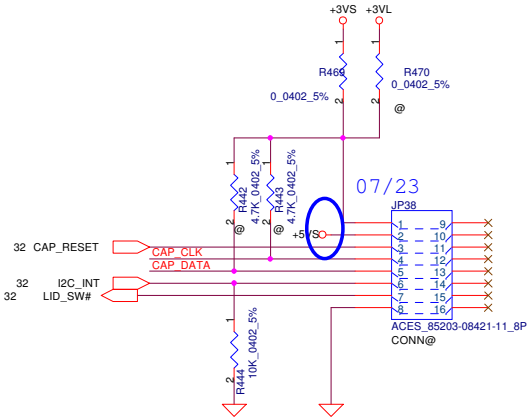




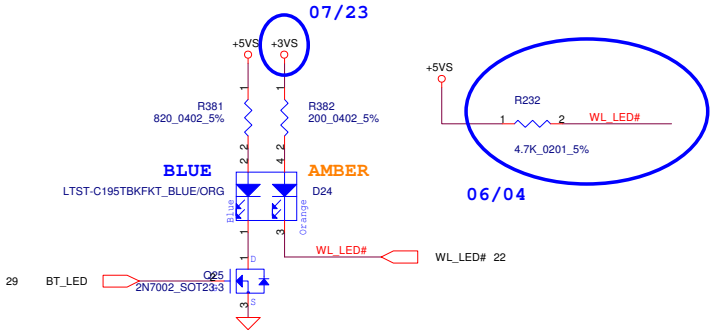




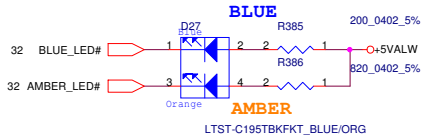
06/15 Change pin define for try ENE cap bottom



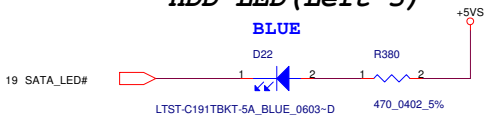
Wireless ON Amber
Bluethooth ON Blue



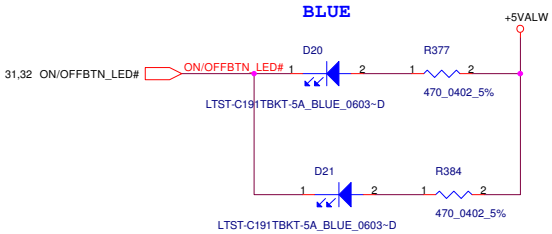
Battery Charge LED(Left 2)



HDD LED(Left 3)



POWER LED1



POWER LED2

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: LED/SW

Size	Document Number	Rev
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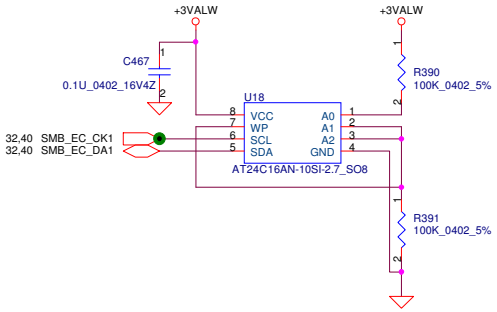
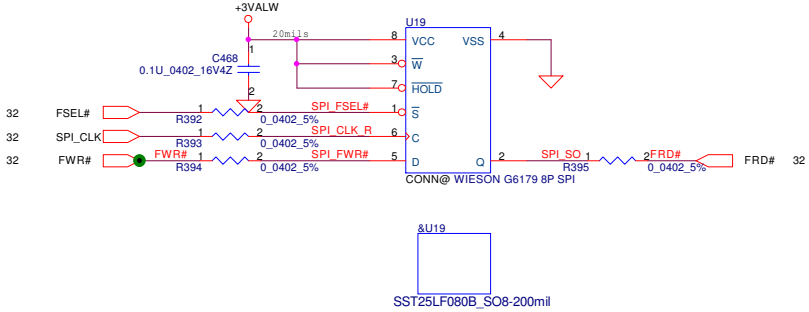
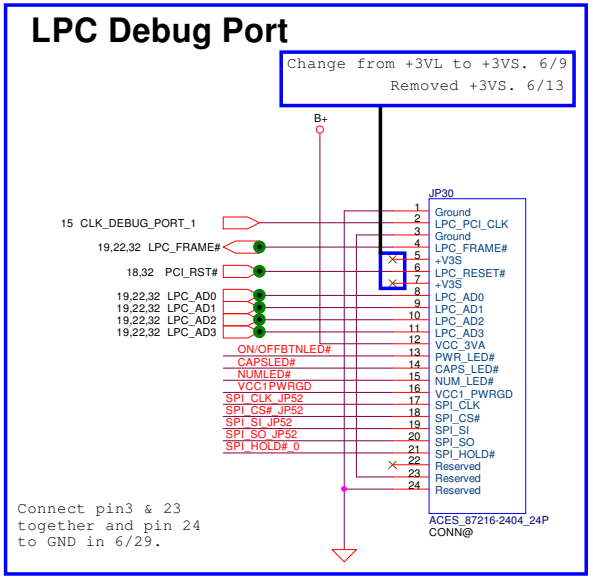
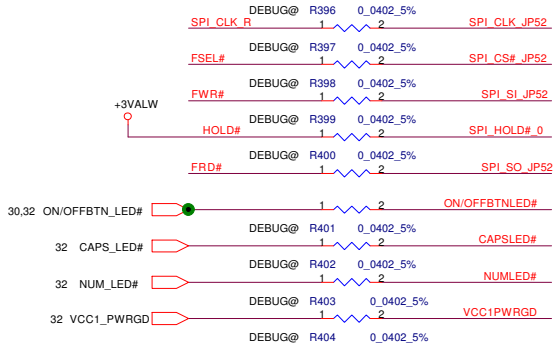


SPI ROM



B-Test remove SPI ROM socket





Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: BIOS ROM			
Size	Document Number: LA-3821P		Rev: 0.3
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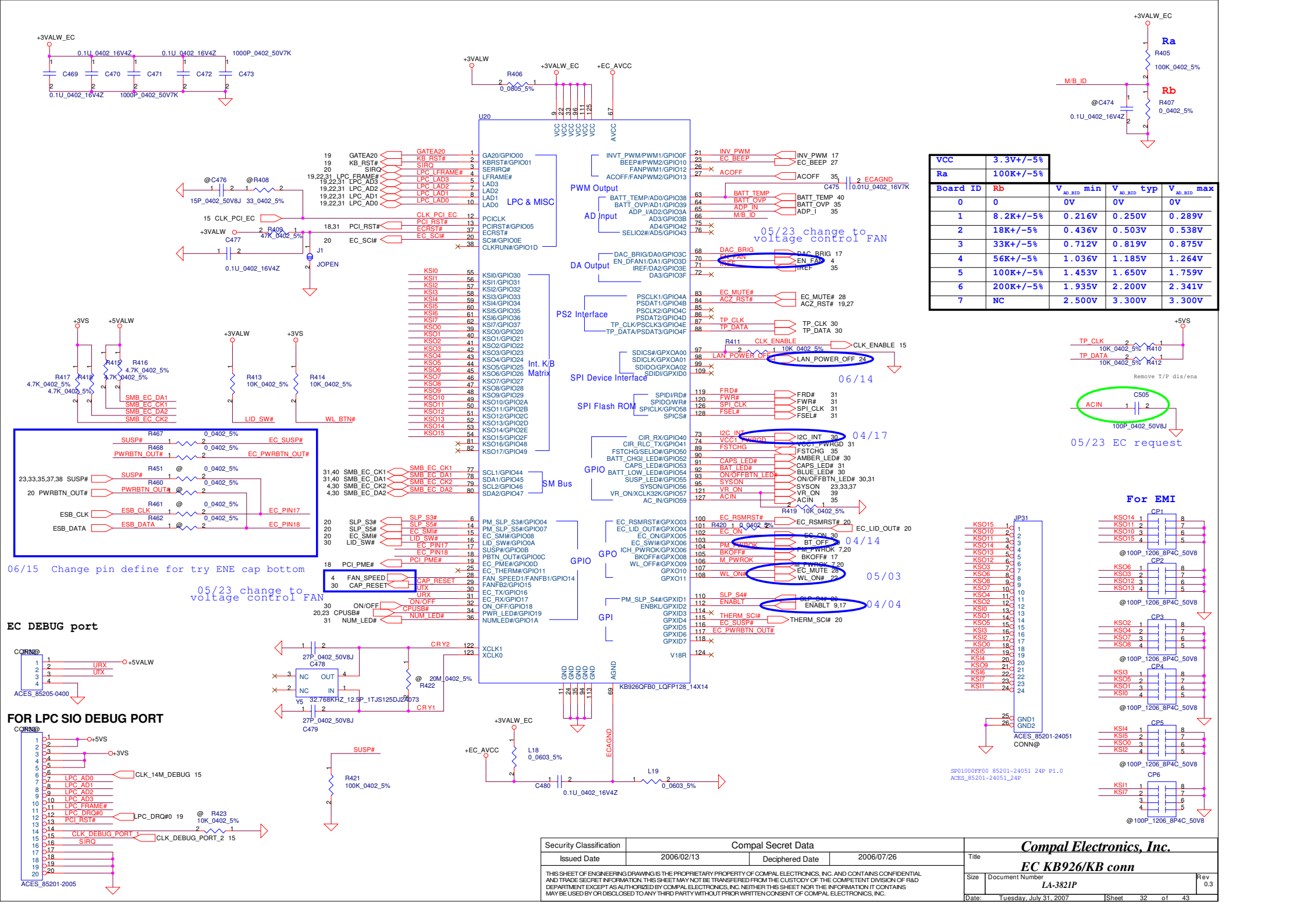
+3VALW_EC
0.1U_0402_16V4Z
1000P_0402_50V7K
C469
C470
C471
C472
C473
+3VALW
R406
0_0805_5%
+EC_AVCC
U20
VCC
AVCC
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
GATEA20
KB_RST#
SIRQ
LPC_LFRAME#
LPC_LAD3
LPC_LAD2
LPC_LAD1
LPC_LAD0
CLK_PCI_EC
PCI_RST#
ECRST#
EC_SCI#
J1
JOPEN
@C476
@R408
15P_0402_50V8J
33_0402_5%
@R409
47K_0402_5%
C477
0.1U_0402_16V4Z
KSI0
KSI1
KSI2
KSI3
KSI4
KSI5
KSI6
KSI7
KSO0
KSO1
KSO2
KSO3
KSO4
KSO5
KSO6
KSO7
KSO8
KSO9
KSO10
KSO11
KSO12
KSO13
KSO14
KSO15
SMB_EC_CK1
SMB_EC_DA1
SMB_EC_CK2
SMB_EC_DA2
INV_PWM
EC_BEEP
ACOFF
BATT_TEMP
BATT_OVP
ADP_IN
M/B_ID
DAC_BRIG
EN_FAN
IREF
EC_MUTE#
ACZ_RST#
TP_CLK
TP_DATA
CLK_ENABLE
LAN_POWER_OFF
FRD#
FWR#
SPI_CLK
FSEL#
I2C_INT
VCC1_PWRGD
FSTCHG
AMBER_LED#
CAPS_LED#
BLUE_LED#
ON/OFFBTN_LED#
SYSON
VR_ON
ACIN
EC_RSMRST#
EC_ON
BT_OFF
PM_PWROK
BKOFF#
WL_ON#
SLP_S4#
ENABLT
THERM_SCI#
EC_SUSP#
EC_PWRBTN_OUT#
ECAGND
C475
0.01U_0402_16V7K
05/23 change to voltage control FAN
06/14
04/17
04/14
05/03
04/04
R467
R468
R451
R460
R461
R462
SUSP#
PWRBTN_OUT#
ESB_CLK
ESB_DATA
EC_SUSP#
EC_PWRBTN_OUT#
EC_PIN17
EC_PIN18
06/15 Change pin define for try ENE cap bottom
05/23 change to voltage control FAN
SLP_S3#
SLP_S5#
EC_SMI#
LID_SW#
PCI_PME#
CAP_RESET
UTX
URX
ON/OFF
CPUSB#
NUM_LED#
FAN_SPEED
CAP_RESET
XCLK1
XCLK0
CRY2
CRY1
27P_0402_50V8J
C478
C479
Y5
32.768KHZ_12.5P_1TJS125DJ2073
@ 20M_0402_5%
R422
KB926QFB0_LQFP128_14X14
V18R
AGND
GND
+3VS
+5VALW
R412
R416
4.7K_0402_5%
R417
R418
4.7K_0402_5%
R413
10K_0402_5%
R414
10K_0402_5%
LID_SW#
WL_BTN#
R411
10K_0402_5%
R419
10K_0402_5%
R420
0_0402_5%
EC DEBUG port
CONN@
ACES_85205-0400
FOR LPC SIO DEBUG PORT
ACES_85201-2005
CLK_14M_DEBUG
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
LPC_DRQ#0
PCI_RST#
CLK_DEBUG_PORT_1
SIRQ
LPC_DRQ#0 19
CLK_DEBUG_PORT_2 15
@ R423
10K_0402_5%
SUSP#
R421
100K_0402_5%
+EC_AVCC
L18
0_0603_5%
L19
0_0603_5%
C480
0.1U_0402_16V4Z
+3VALW_EC
Ra
R405
100K_0402_5%
Rb
R407
0_0402_5%
@C474
0.1U_0402_16V4Z
M/B_ID
VCC 3.3V+/-5%
Ra 100K+/-5%
Board ID | Rb | V_AD_BID min | V_AD_BID typ | V_AD_BID max
0 | 0 | 0V | 0V | 0V
1 | 8.2K+/-5% | 0.216V | 0.250V | 0.289V
2 | 18K+/-5% | 0.436V | 0.503V | 0.538V
3 | 33K+/-5% | 0.712V | 0.819V | 0.875V
4 | 56K+/-5% | 1.036V | 1.185V | 1.264V
5 | 100K+/-5% | 1.453V | 1.650V | 1.759V
6 | 200K+/-5% | 1.935V | 2.200V | 2.341V
7 | NC | 2.500V | 3.300V | 3.300V
+5VS
TP_CLK
TP_DATA
10K_0402_5%
R410
R412
Remove T/P dis/ena
C505
ACIN
100P_0402_50V8J
05/23 EC request
For EMI
JP31
KSO15
KSO10
KSO11
KSO14
KSO13
KSO12
KSO3
KSO6
KSO8
KSO7
KSO4
KSO2
KSI0
KSO1
KSO5
KSI3
KSI2
KSO0
KSI5
KSI4
KSO9
KSI6
KSI7
KSI1
GND1
GND2
ACES_85201-24051
CONN@
SP01000FF00 85201-24051 24P P1.0
ACES_85201-24051_24P
CP1
CP2
CP3
CP4
CP5
CP6
@100P_1206_8P4C_50V8
Security Classification: Compal Secret Data
Issued Date: 2006/02/13
Deciphered Date: 2006/07/26
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Title: EC KB926/KB conn
Size: Document Number: LA-3821P
Rev: 0.3
Date: Tuesday, July 31, 2007
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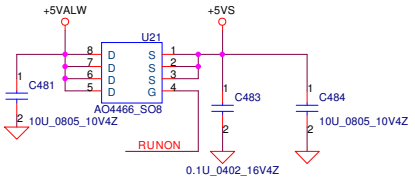
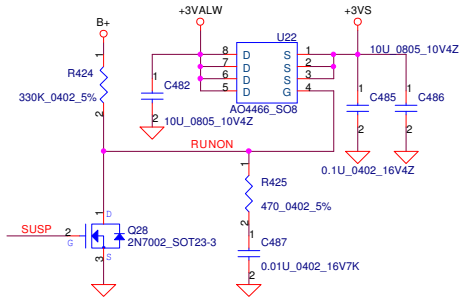
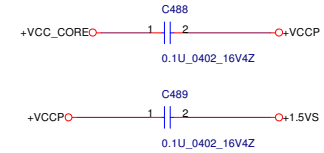
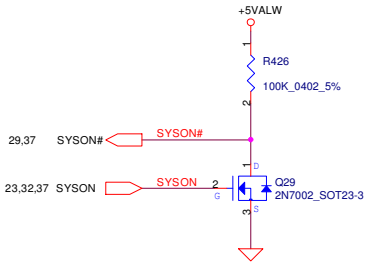
+5VALW to +5VS Transfer

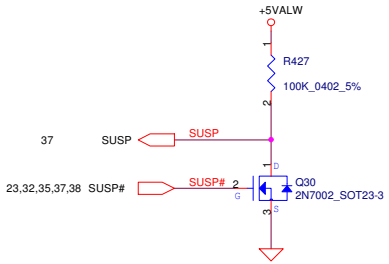


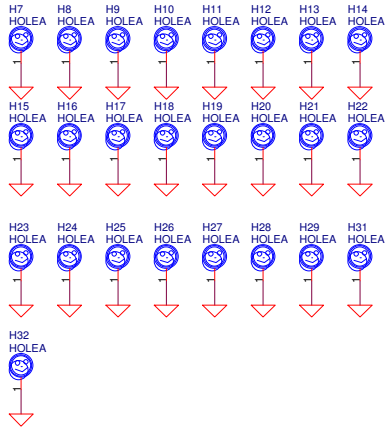
+3VALW to +3VS Transfer



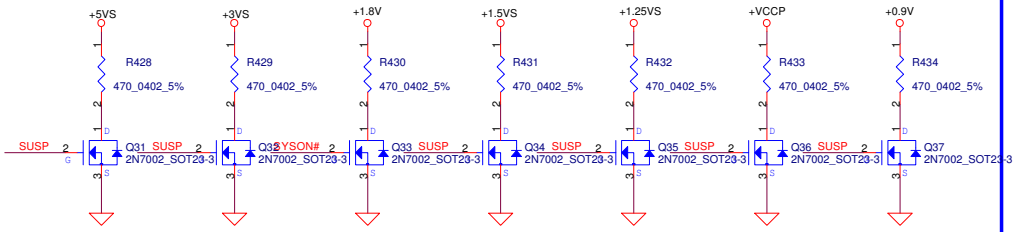








Discharge circuit



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **DC/DC Interface**

Size | Document Number: *LA-3821P* | Rev: 0.3

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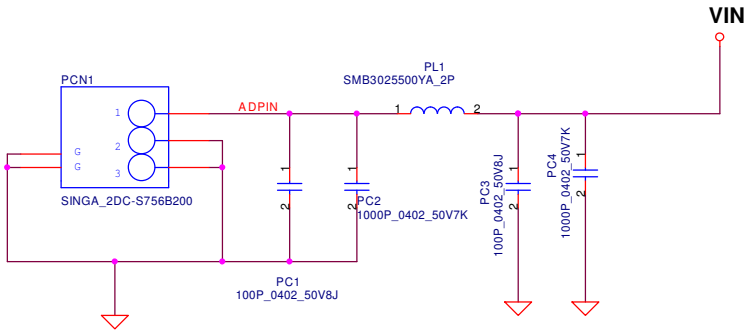

Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Title: ***DC CONN***

Size	Document Number	Rev
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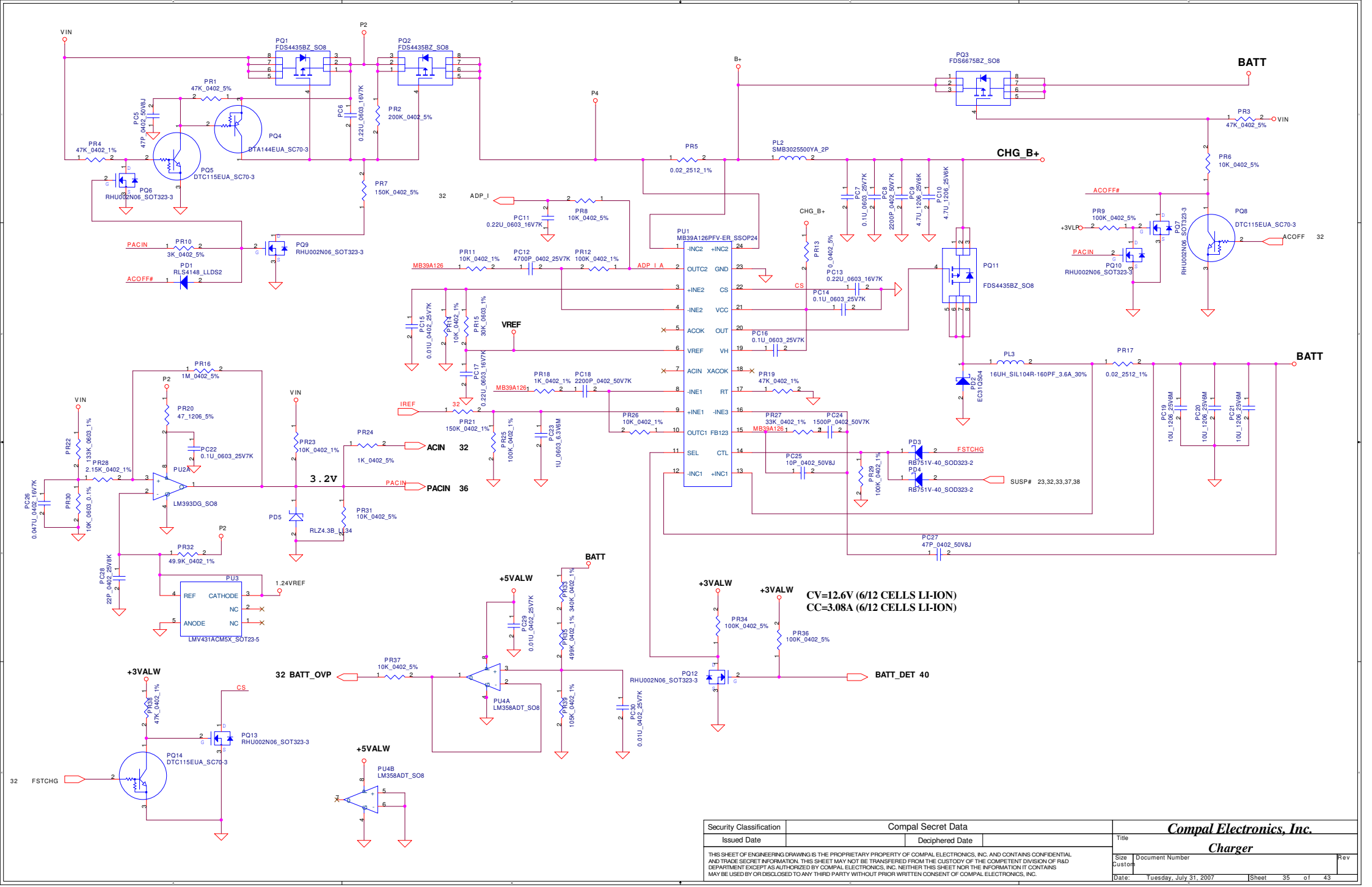

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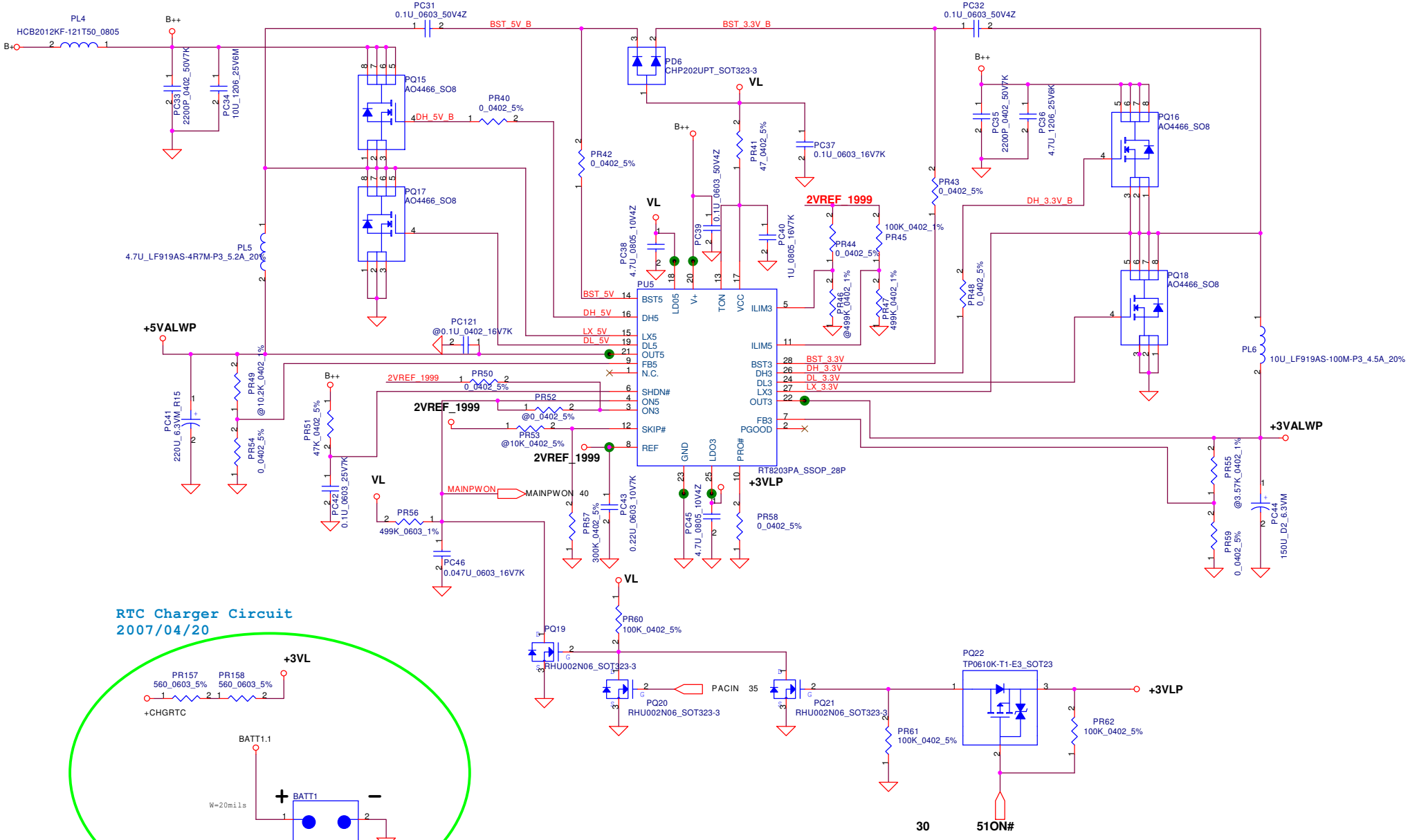
Issued Date		Deciphered Date	

Compal Electronics, Inc.		
Title: Charger		
Size: Custom	Document Number	Rev
Date: Tuesday, July 31, 2007	Sheet 35 of 43	



Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.

Title: **3.3VALWP / 5VALWP**

Size	Document Number	Rev

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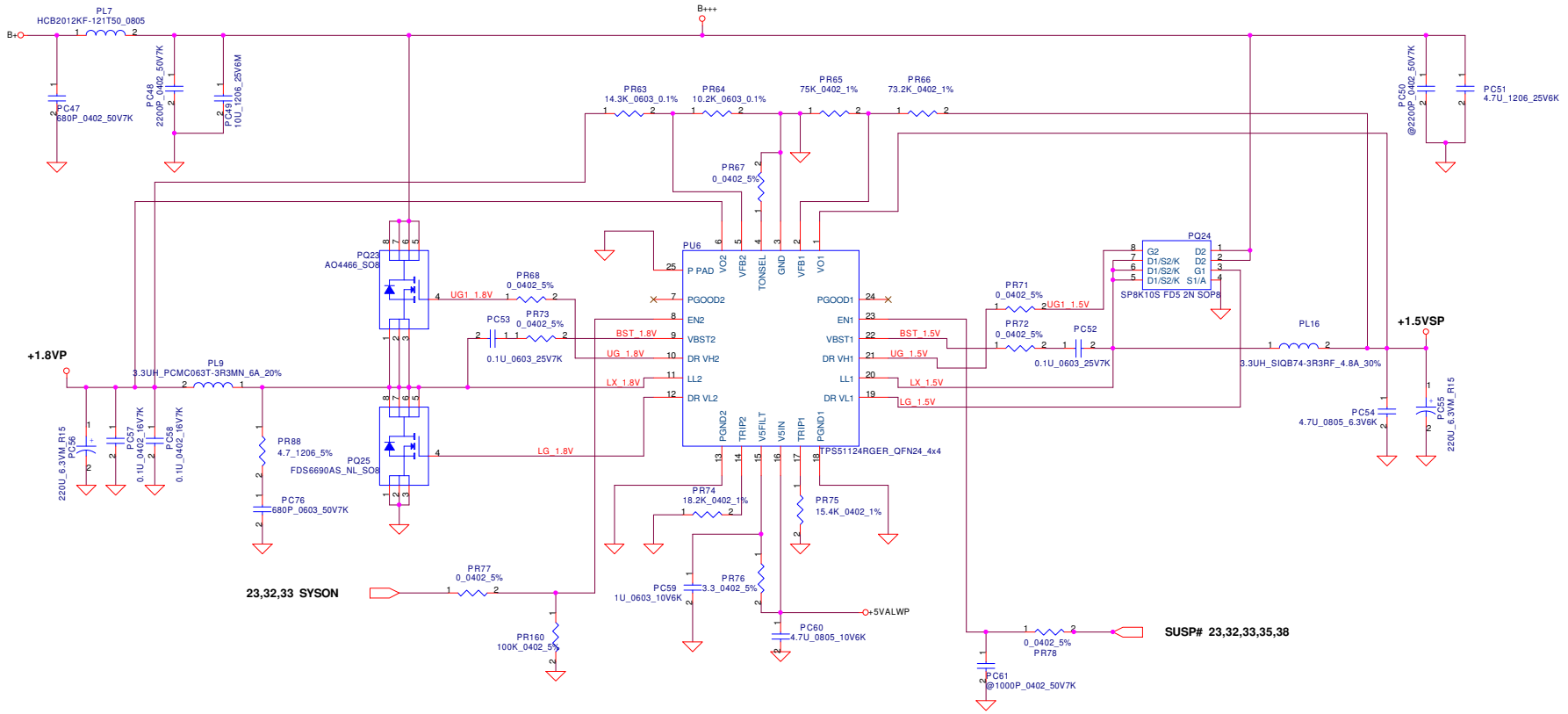

Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: *1.8VP/0.9VP/1.5VSP*

Size	Document Number	Rev
	LA-3821P	0.2

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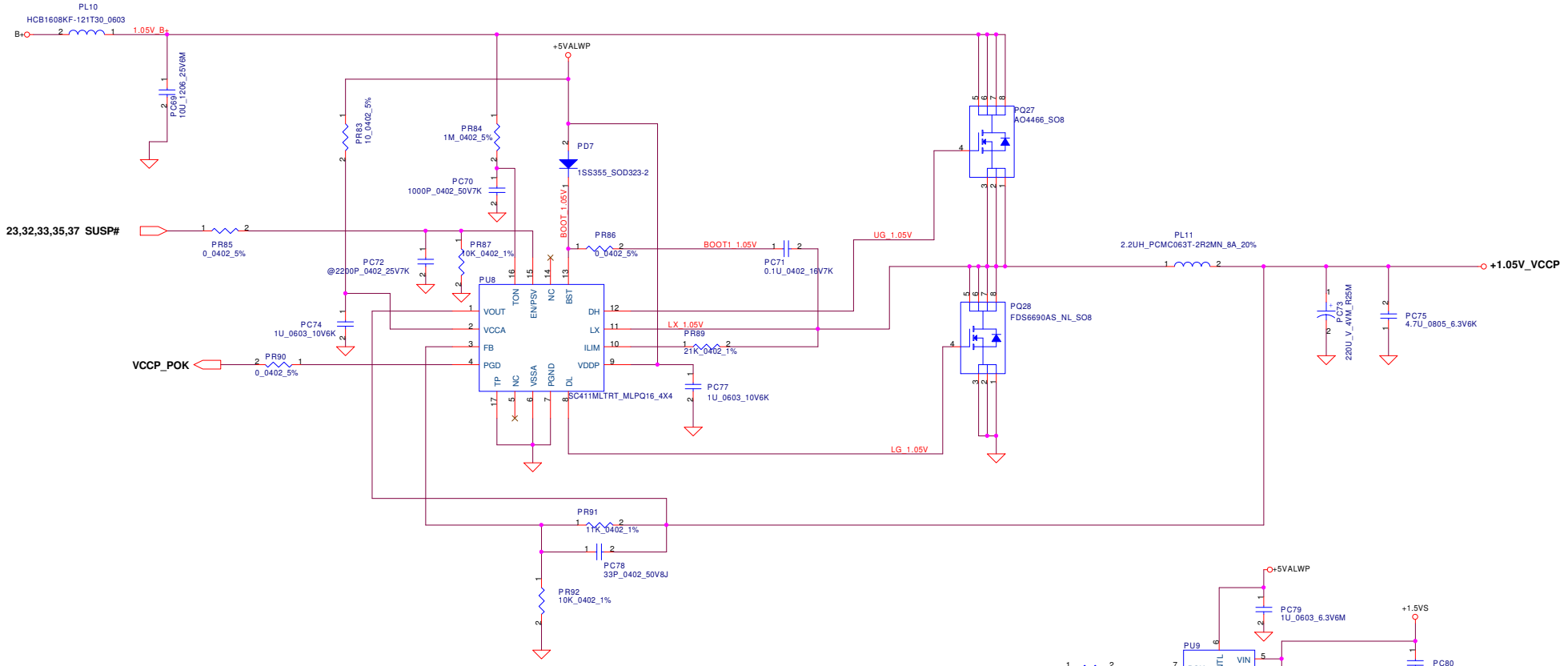
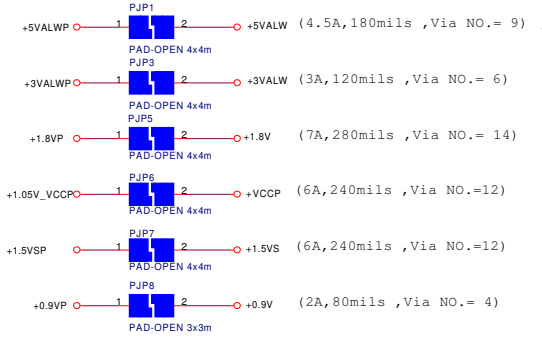
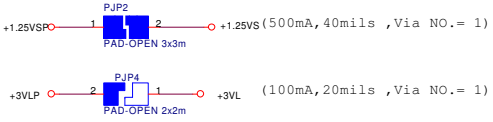
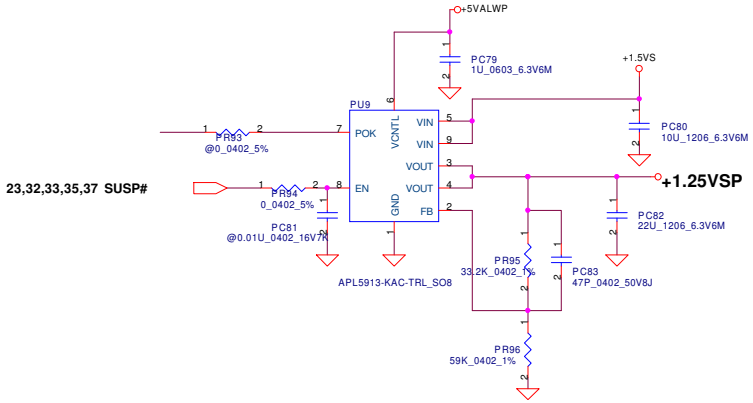








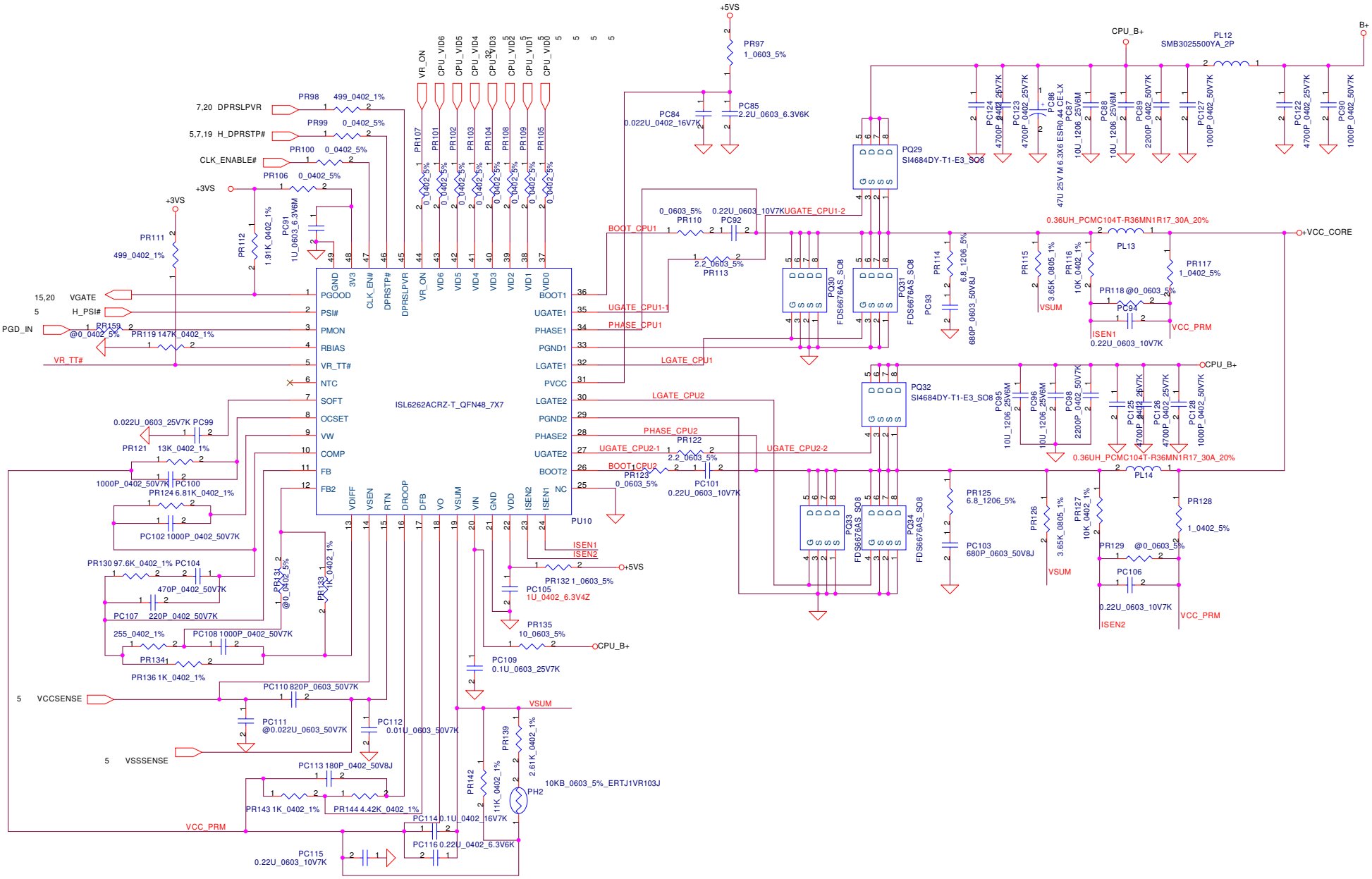
Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.

Title: *1.05V_VCCP/2.5VSP*

Size	Document Number	Rev
	LA-3821P	0.2

Date: Tuesday, July 31, 2007 | Sheet 38 of 43



Compal Electronics, Inc.

Title: +CPU_CORE

Size: Custom | Document Number | Rev: 0.2

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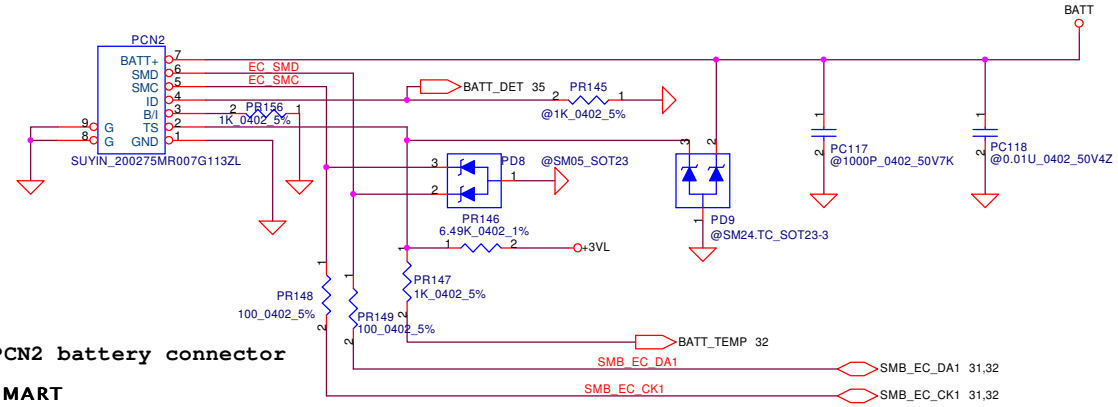
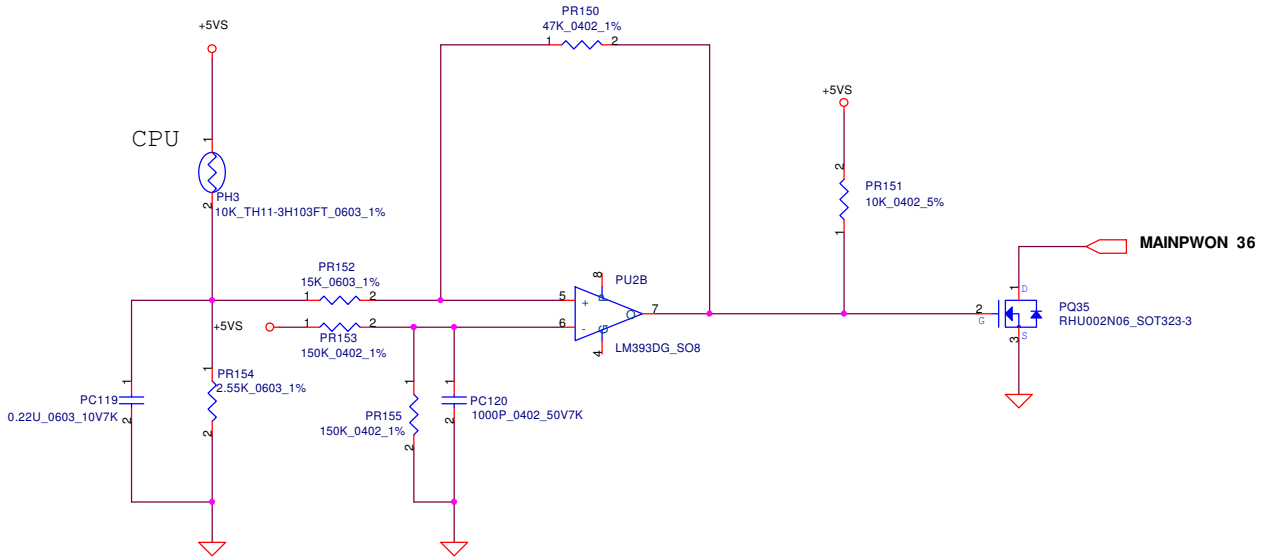


PCN2 battery connector

SMART Battery:
7.BATT+
6.SMD
5.SMC
4.ID
3.B/I
2.TS
1.GND

PH3 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C



Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.

Title: **BATTERY CONN**

Size: Custom | Document Number: LA-3821P | Rev:

Date: Tuesday, July 31, 2007 | Sheet 40 of 43

Version change list (P.I.R. List)

Power section

Item	Reason for change	PG#	Modify List	Date	Phase
1	RT8203 crosstalk issue	37	add PC121 and 0.1uF	2007/05/24	SI
2	PU6 pin8 add a resistor to GND	38	add PR160 100K_ohm	2007/05/24	SI
3	remove PL15	36	remove PL15	2007/06/12	SI
4	EMI request	39	add PC122,PC123,PC124,PC125,PC126,PC127,PC128	2007/07/23	PV
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					

Compal Electronics, Inc.
Title: PWR PIR
Size: Custom | Document Number | Rev: 0.2
Date: Tuesday, July 31, 2007 | Sheet 41 of 43

Version change list (P.I.R. List)

Power section

Item	Reason for change	PG#	Modify List	Date	Phase
1	EC team request	32	ACIN add 100P (C505) to GND	2007/05/30	SI
2	Change Board ID	32	R407 from 0 Ohm to 8.2K,R405 install 100K	2007/05/30	SI
3	USB power switch fail	29	U23 & U17 change pin 4 from SLP_S5# to SYSON#	2007/05/30	SI
4	FAN use voltage control	4	del U2,Q1;add U24,C13 for 3 pin FAN	2007/05/30	SI
5	USB JP24 fail	29	Change pin define	2007/05/30	SI
6	Speaker output fail	28	Add R457,R458,R459 for Line_out	2007/05/30	SI
7	MS Pro fail	26	Add MS_D1,MS_D2,MS_D3 net	2007/06/06	SI
8	WLAN LED fail when disable WLAN	30	Add R232 pull high +5VS	2007/06/06	SI
9	+3VALW leakage	30	Del R387	2007/06/06	SI
10	Capacitor board fail	32	Add net CAP_RESET for Capacitor board reset	2007/06/06	SI
11	XDP fail	15	XDP clock share in robeson card	2007/06/06	SI
12	LAN power consumption is too large when S3	24	Add Q22	2007/06/14	SI
13	RJ11' cap is duplicate MDC module.	25	Delete C378,C379	2007/06/14	SI
14	Reverse some resister for tring ENE cap board	30 32	Add R460~R468,R451	2007/06/14	SI
15	+LCDVDD over current when diplay.	17	Change R163 from 47K to 100K Change C248 from 0.1U to 0.22U	2007/06/21	SI
16	LAN fail	24	Change JP14 pin define	2007/06/06	SI
17	WLAN LED (Amber led) issue	30	WLAN LED need change from +5VS to +3VS	2007/07/23	PV
18	030 project Bluetooth module issue	29	Swap pin5 & pin7	2007/07/23	PV
19	change Cap board LED supply voltage	30	from +3VS to +5VS	2007/07/23	PV
20	CMOS timing can't reset	19	SHORT PAD (CLRP3) connect between +RTCVCC and GND	2007/07/23	PV
20	EMI issue (CPU core)	5	add C43 & C44 (330U)	2007/07/23	PV
21	EMI/ESD issue (XDO connector)	4	delete XDP connector	2007/07/23	PV
22	EMI/ESD issue (RJ11 connector)	25	add 1000P at RJ11 RING & TIP	2007/07/23	PV

Compal Electronics, Inc.
Title: PWR PIR
Size: Custom | Document Number | Rev: 0.3
Date: Tuesday, July 31, 2007 | Sheet 42 of 43

Version change list (P.I.R. List)

Power section

Item	Reason for change	PG#	Modify List	Date	Phase
23	card reader RTL5158 chip issue	26	change C393, C394 from 27p to 5.6p	2007/07/25	PV
24	monitor wave riple issue	10	add C508	2007/07/25	PV
25	MIC issue for EMI solution	28	add L20, L21, L22, L23, C509, C510	2007/07/31	PV

Compal Electronics, Inc.
Title: PWR PIR
Size: Custom | Document Number | Rev: 0.3
Date: Tuesday, July 31, 2007 | Sheet 43 of 43