



M/B PCB

12.1" AM3 Low Rider Block Diagram

VER : C3A

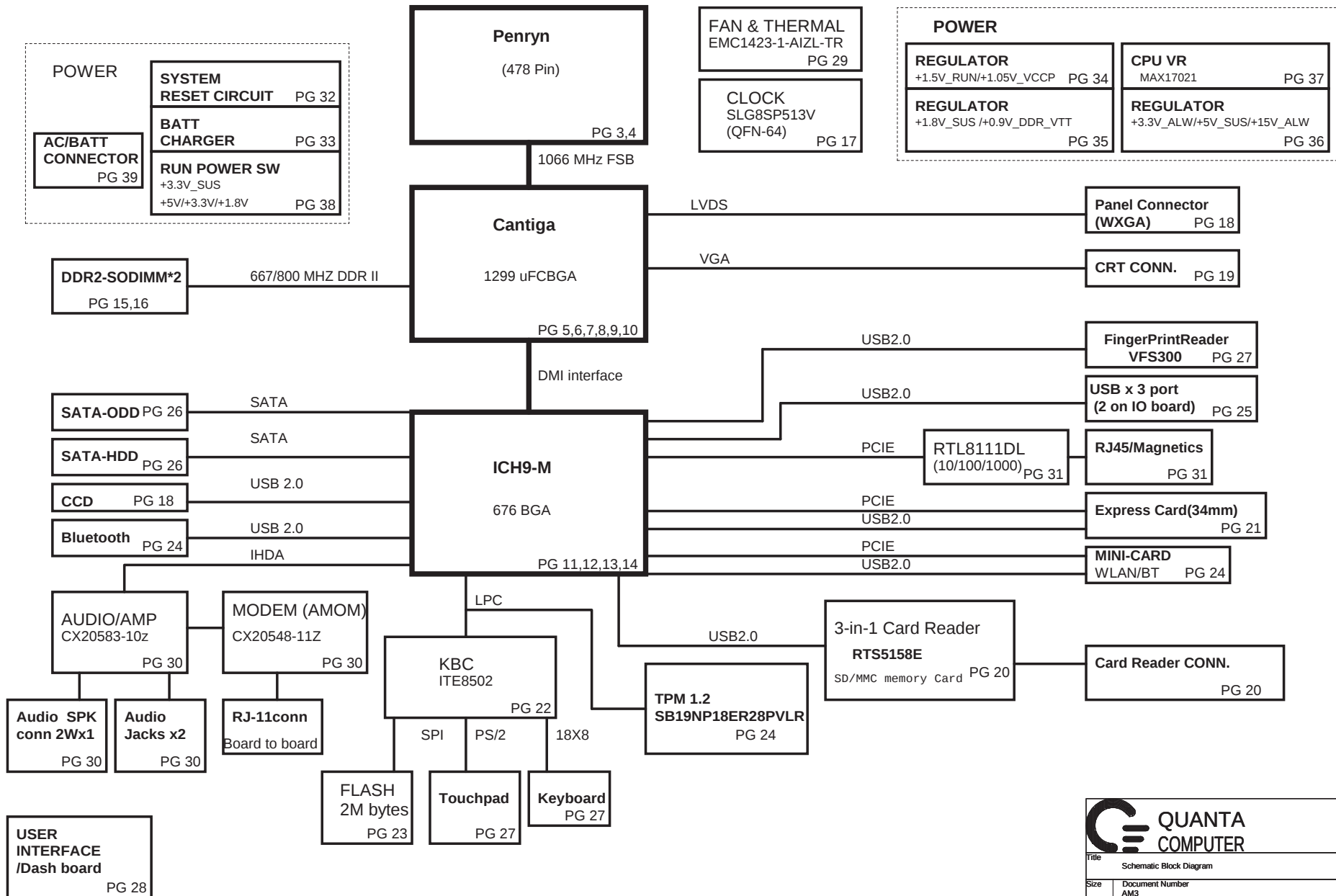


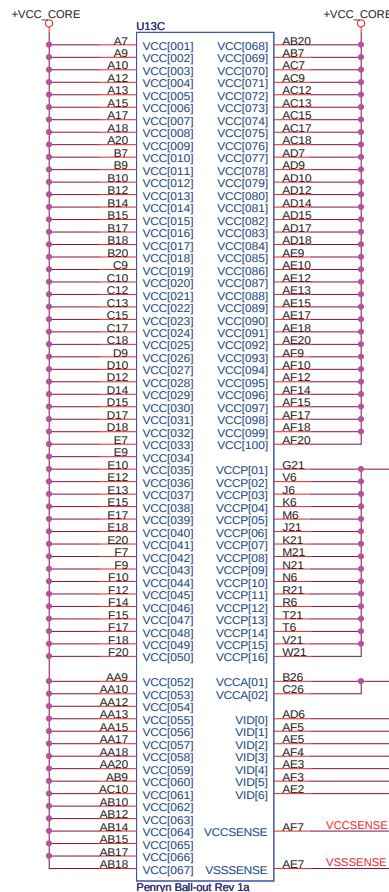
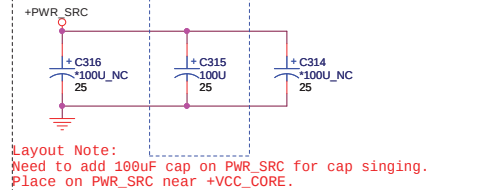
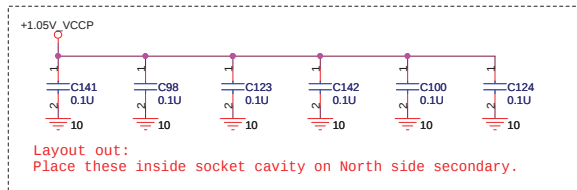
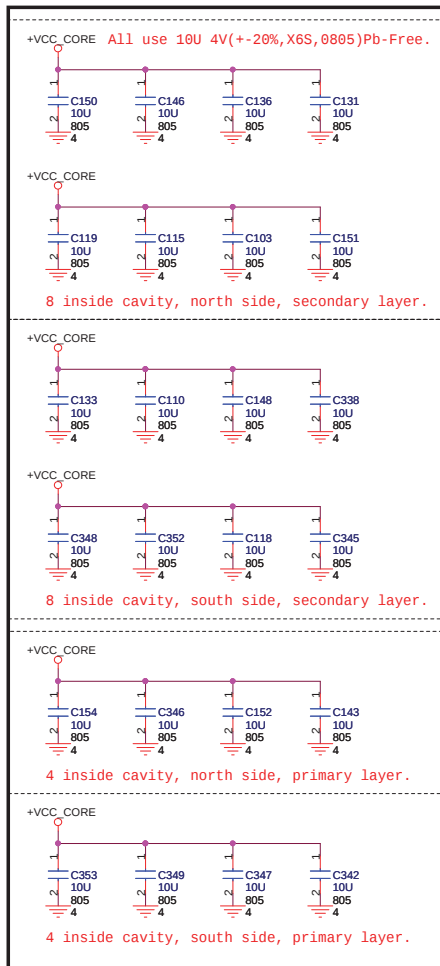
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	PAD& SCREW
	EMI CAP
	SMBUS BLOCK

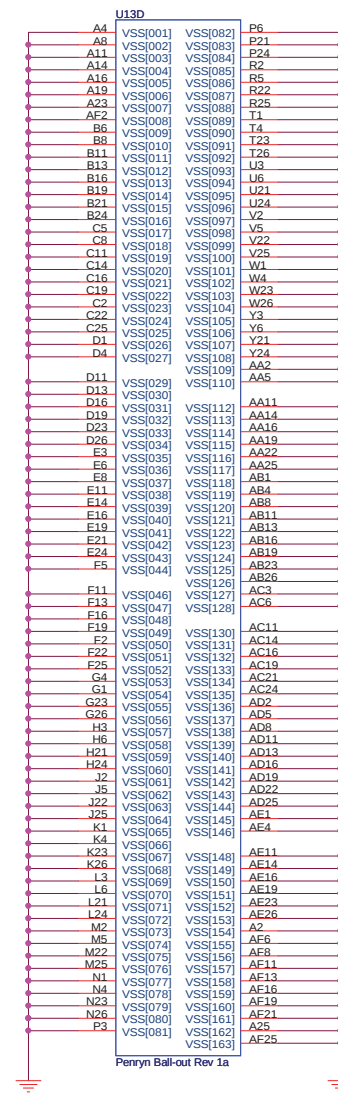
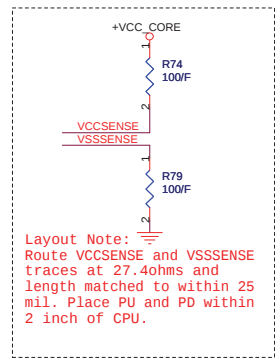
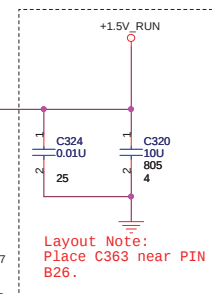
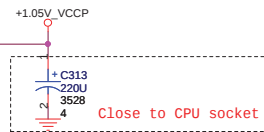
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,51,52,56	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,26,30,37,38,43,48,49,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,53	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,18,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	14,18,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,53,56	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48,56	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51,56	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+PBATT	+10V~+17V		MAIN BATTERY	CHG_PBATT	
+SBATT	+10V~+17V		SECOND BATTERY	CHG_SBATT	

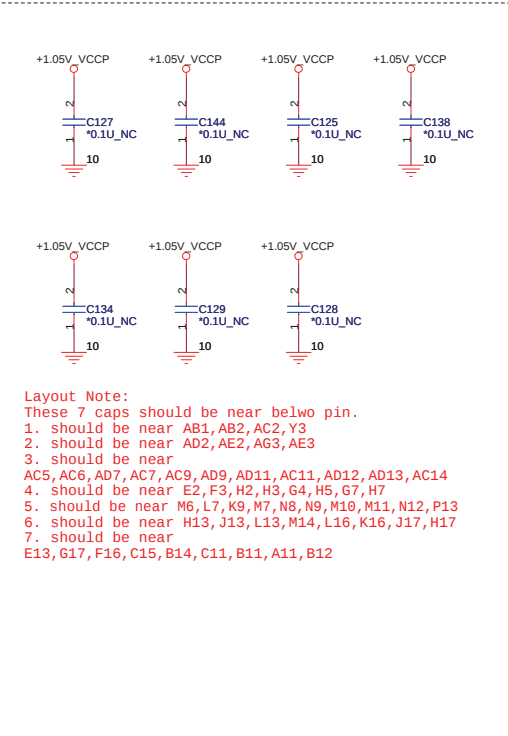
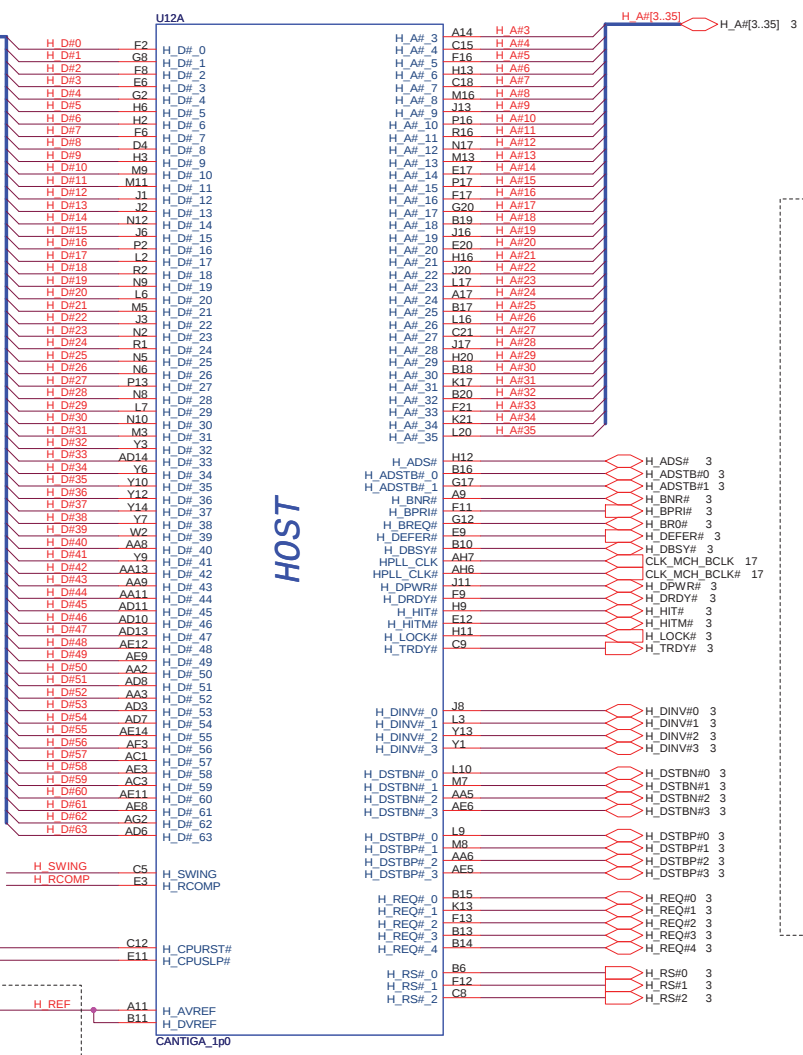
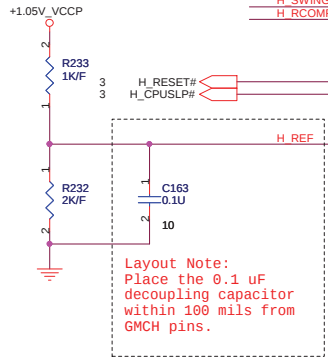
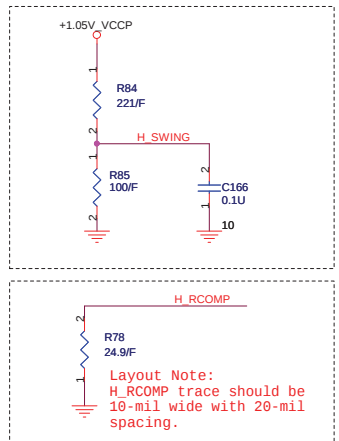
GND PLANE	PAGE	DESCRIPTION
 GND	ALL	

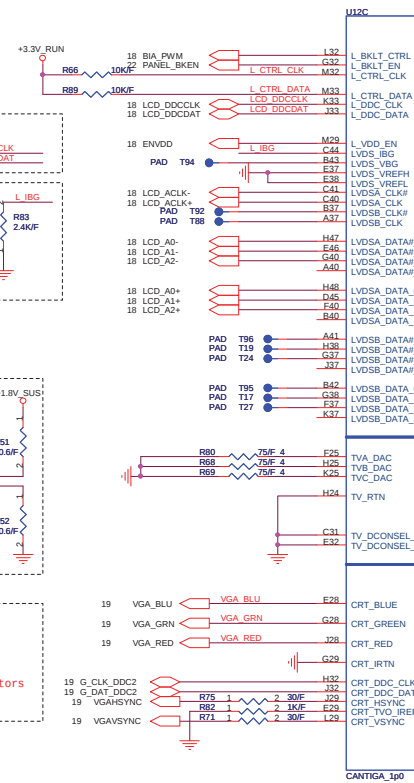
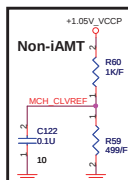
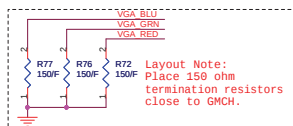
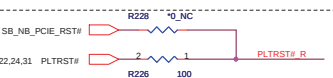


Add those caps for EMI solution No3 0318



Add C315 for Acoustic No1 0220





CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIe1 is operational (default) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present.	Low=No SDVO Device Present (default) High=SDVO Device Present

DDR SYSTEM MEMORY A

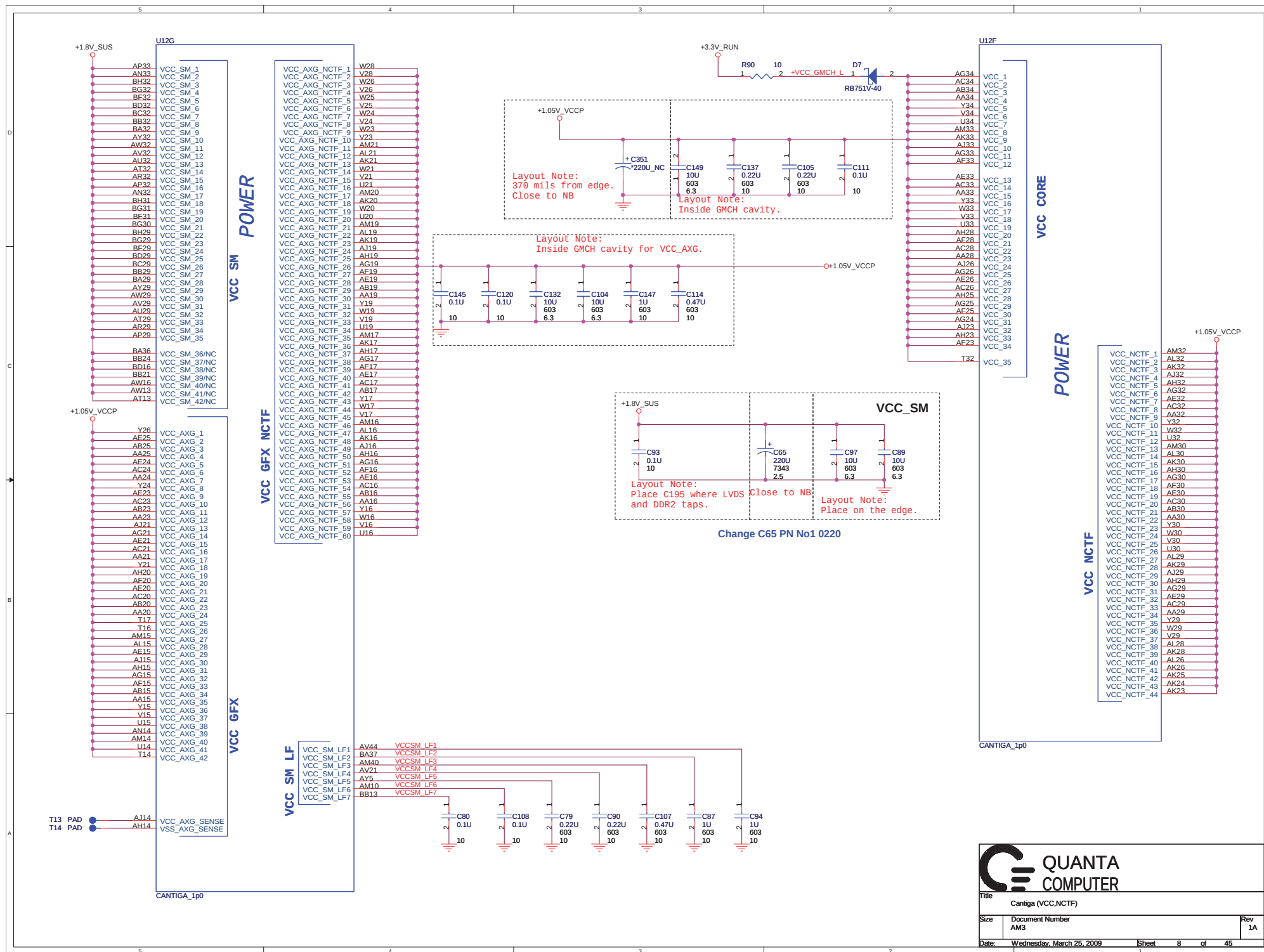
DDR SYSTEM MEMORY B

U12D

U12E

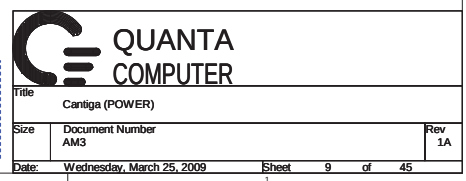
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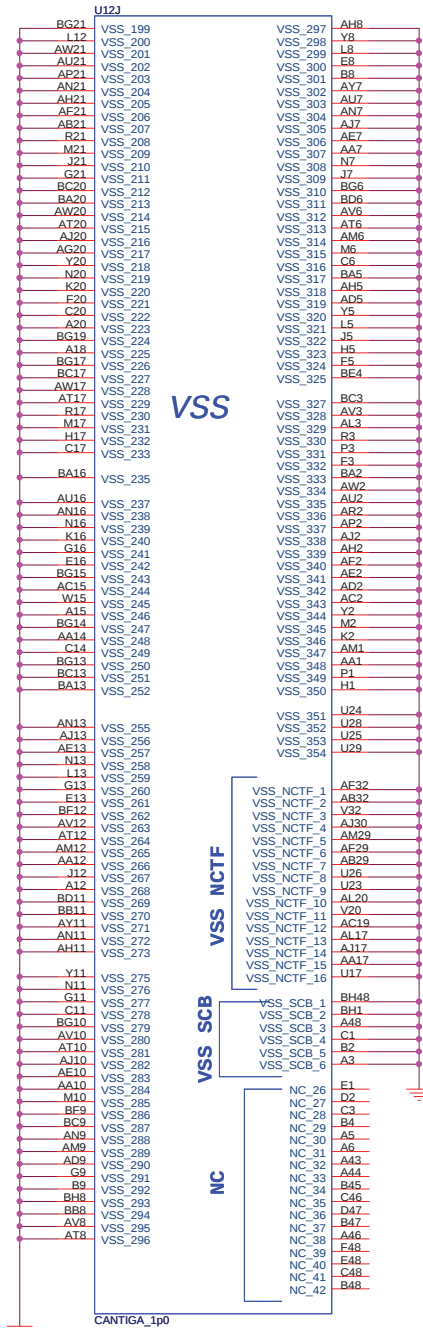
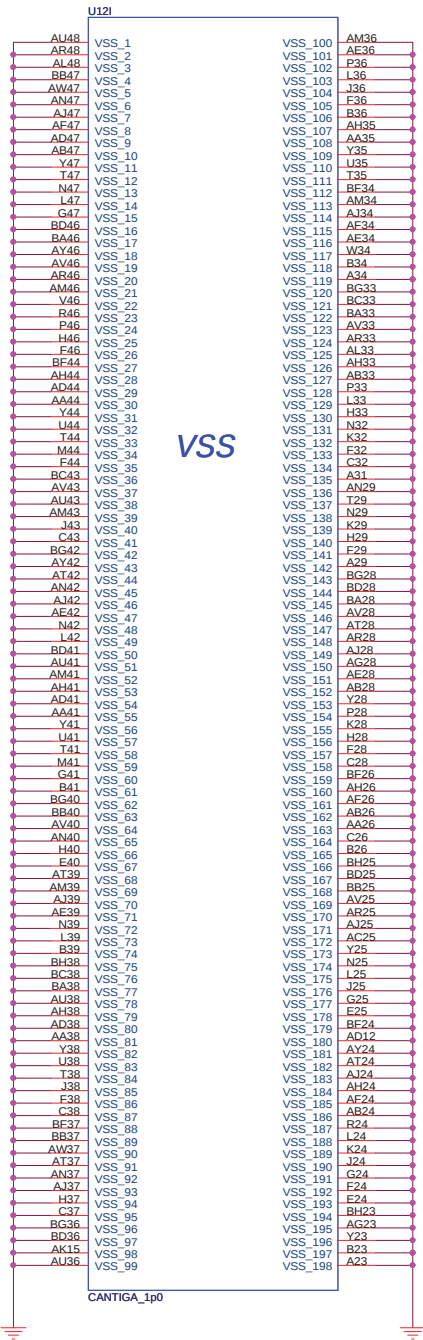
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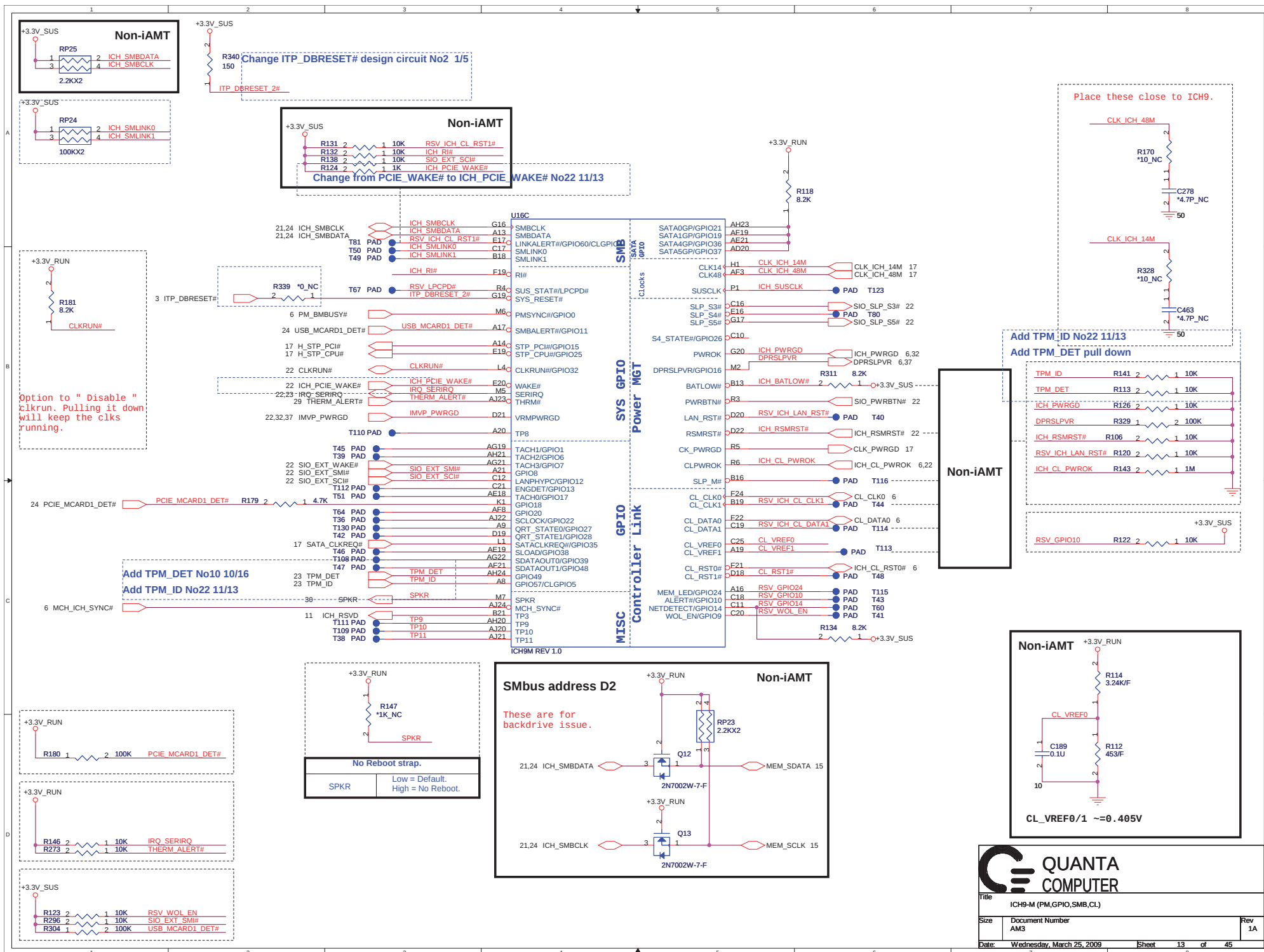


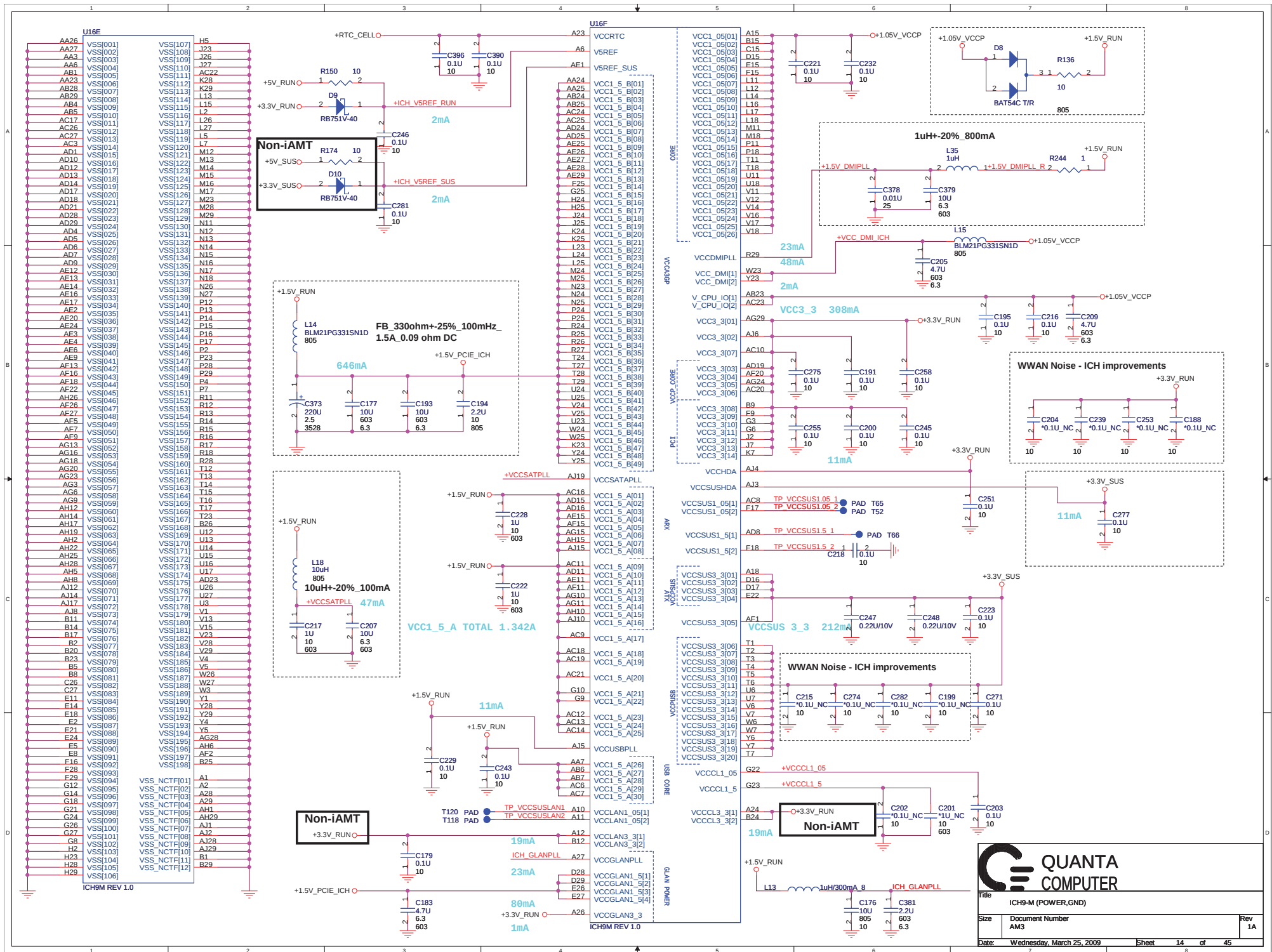
QUANTA
COMPUTER

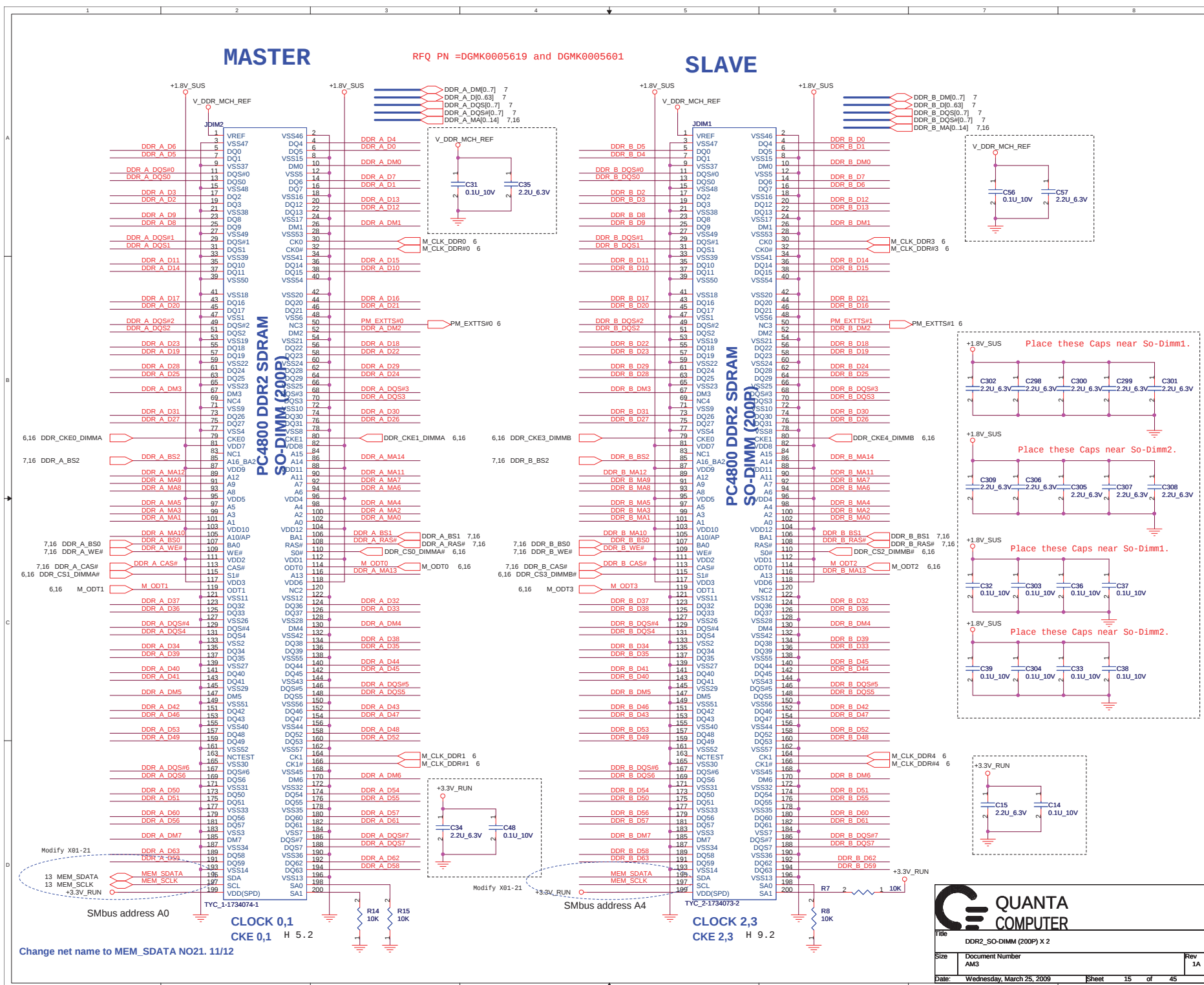
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Cantiga (VCC,NCTF)				
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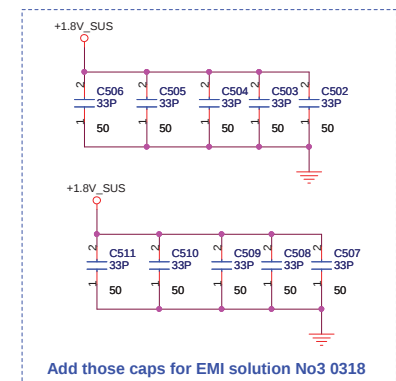
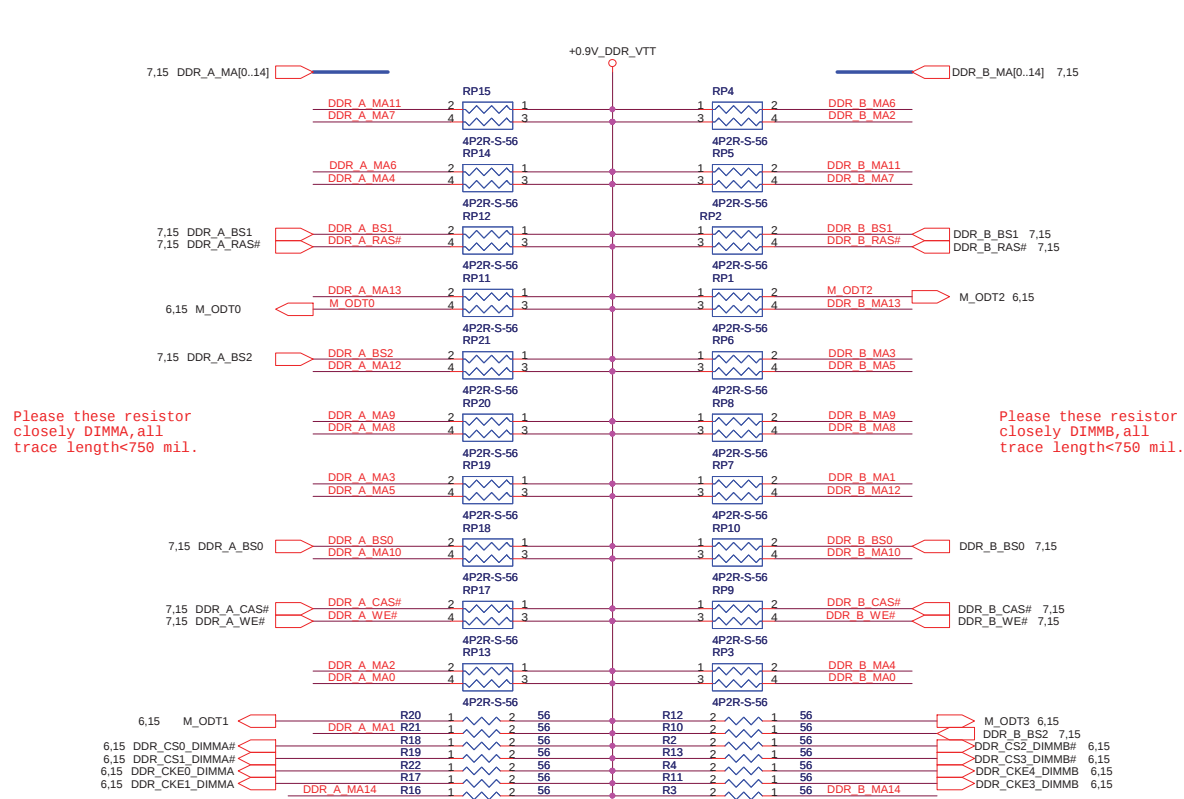
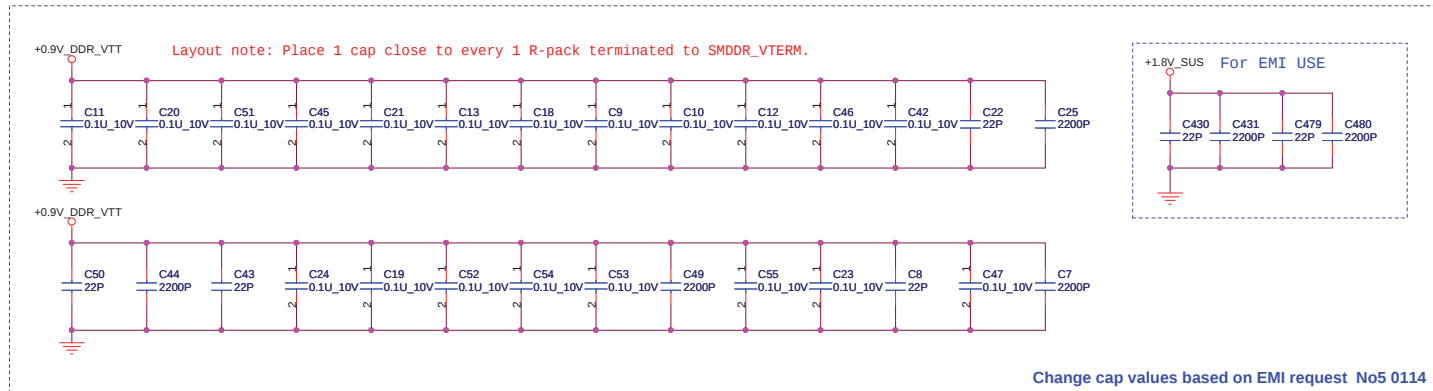




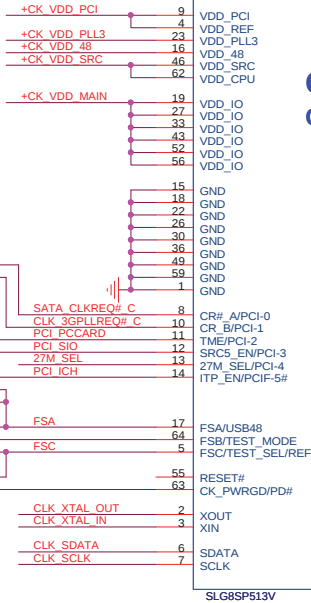
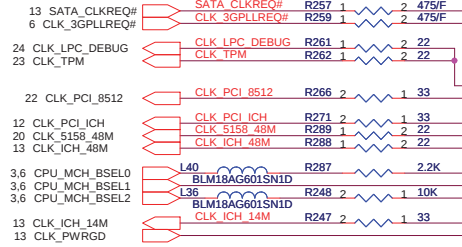
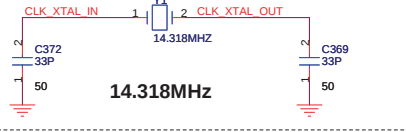
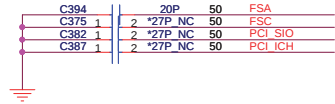




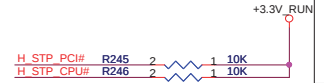
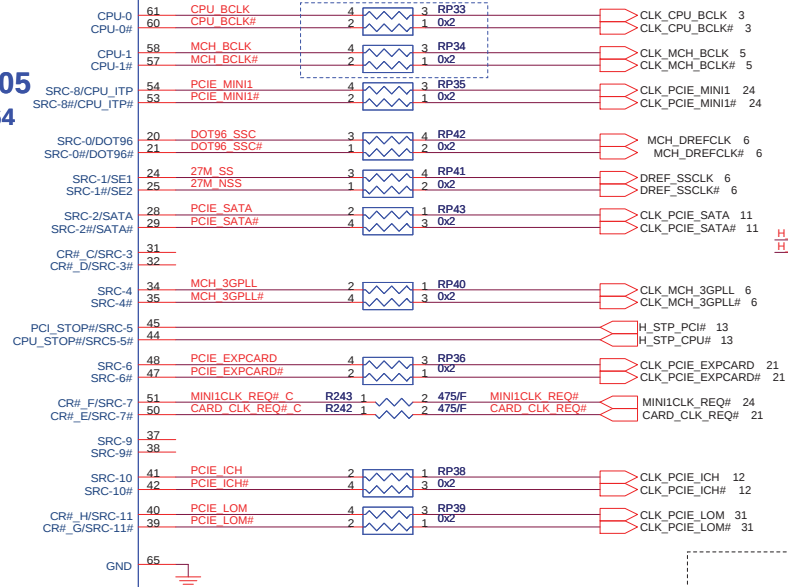




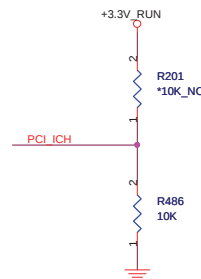
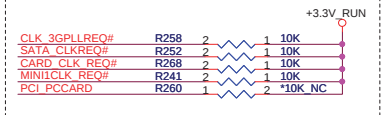
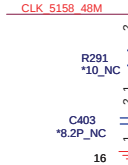
Add capacitor pads for improving WWAN.



Change resistor values based on EMI request No5 0114
Change resistor values based on EMI request No6 0119



Reserved for EMI



Add R201 ND R486 No9 0202

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL

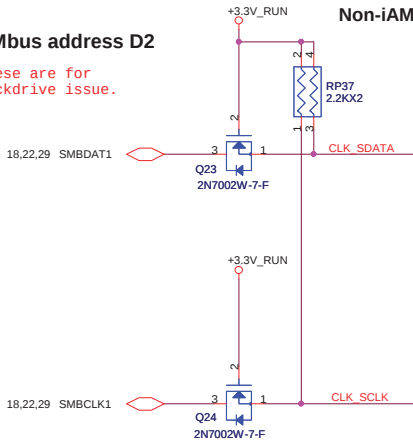
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GFRX down	SRCT0	SRCC0	27Mout	27MSSout



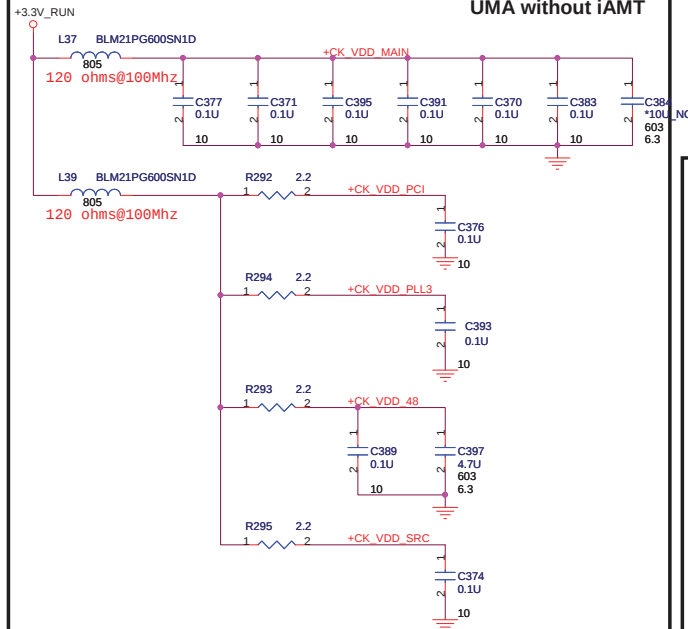
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SMbus address D2

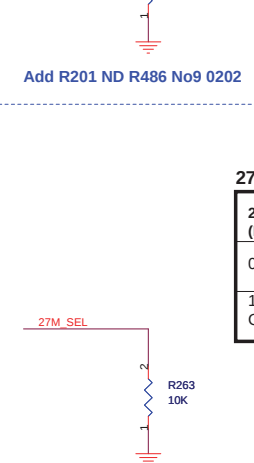
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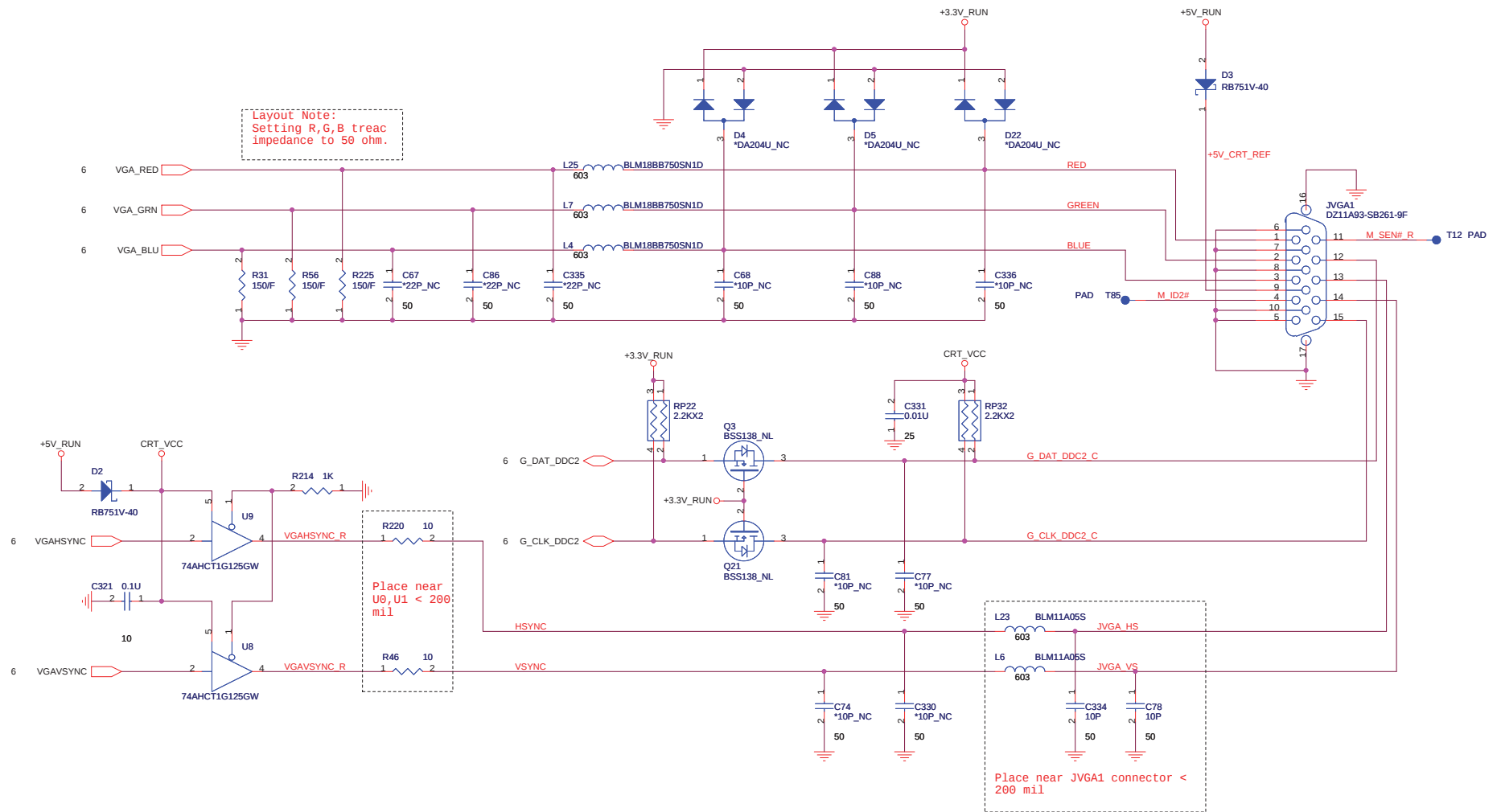


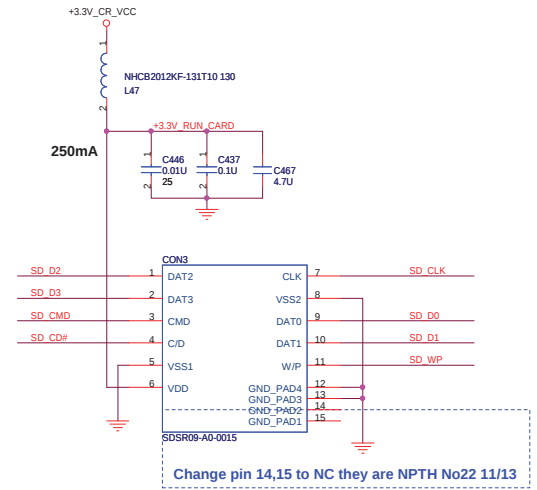
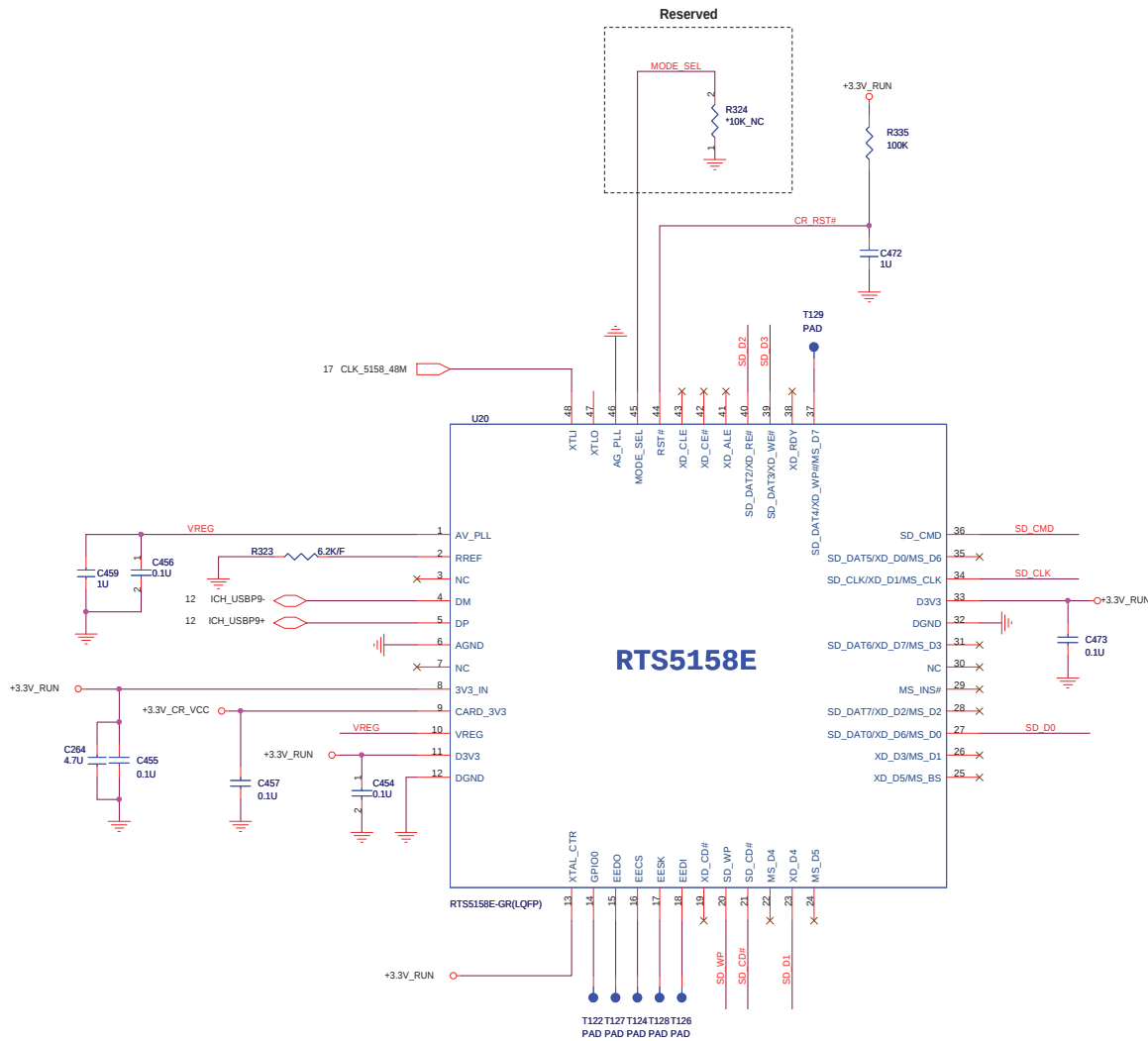
UMA without iAMT



Non-iAMT



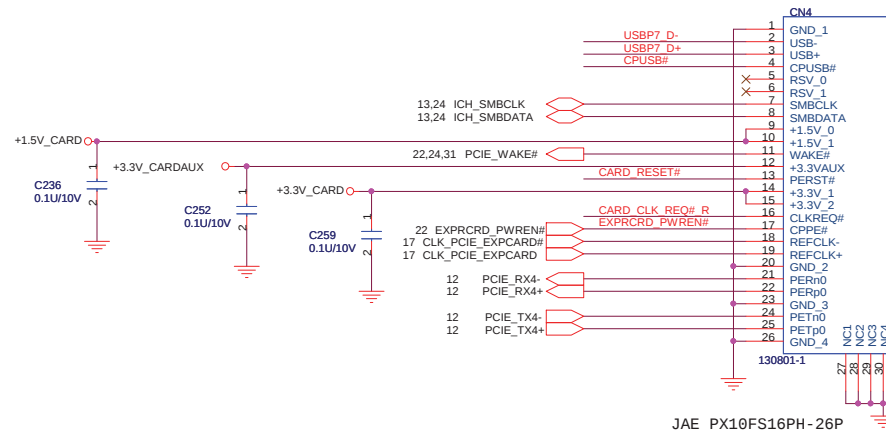
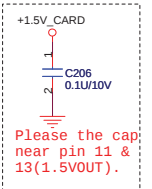
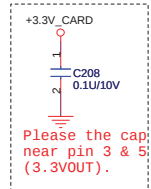
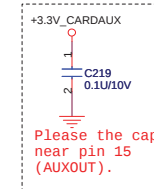
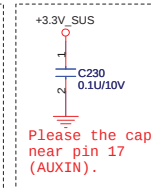
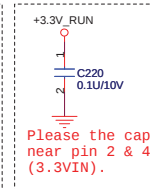
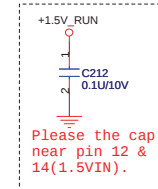
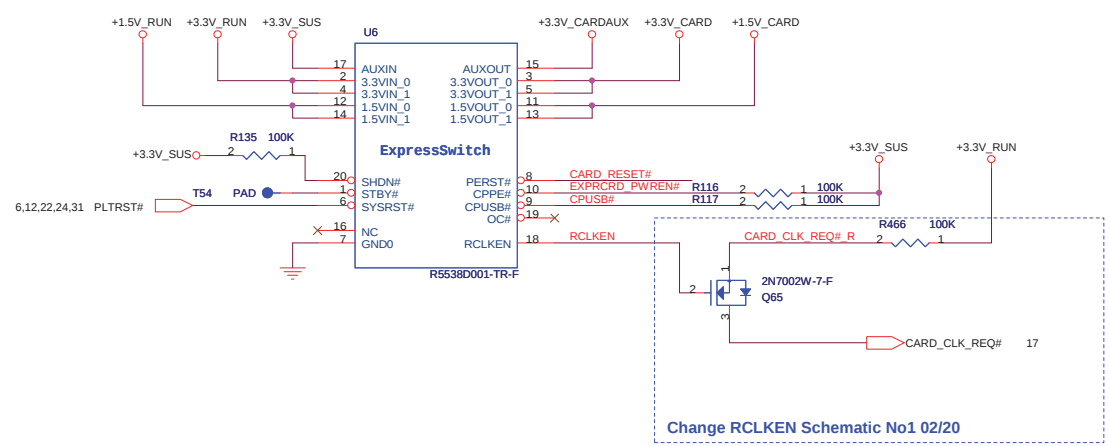
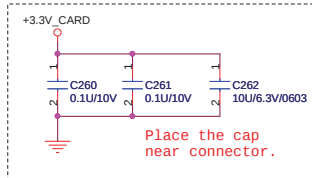
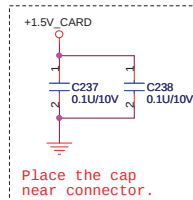




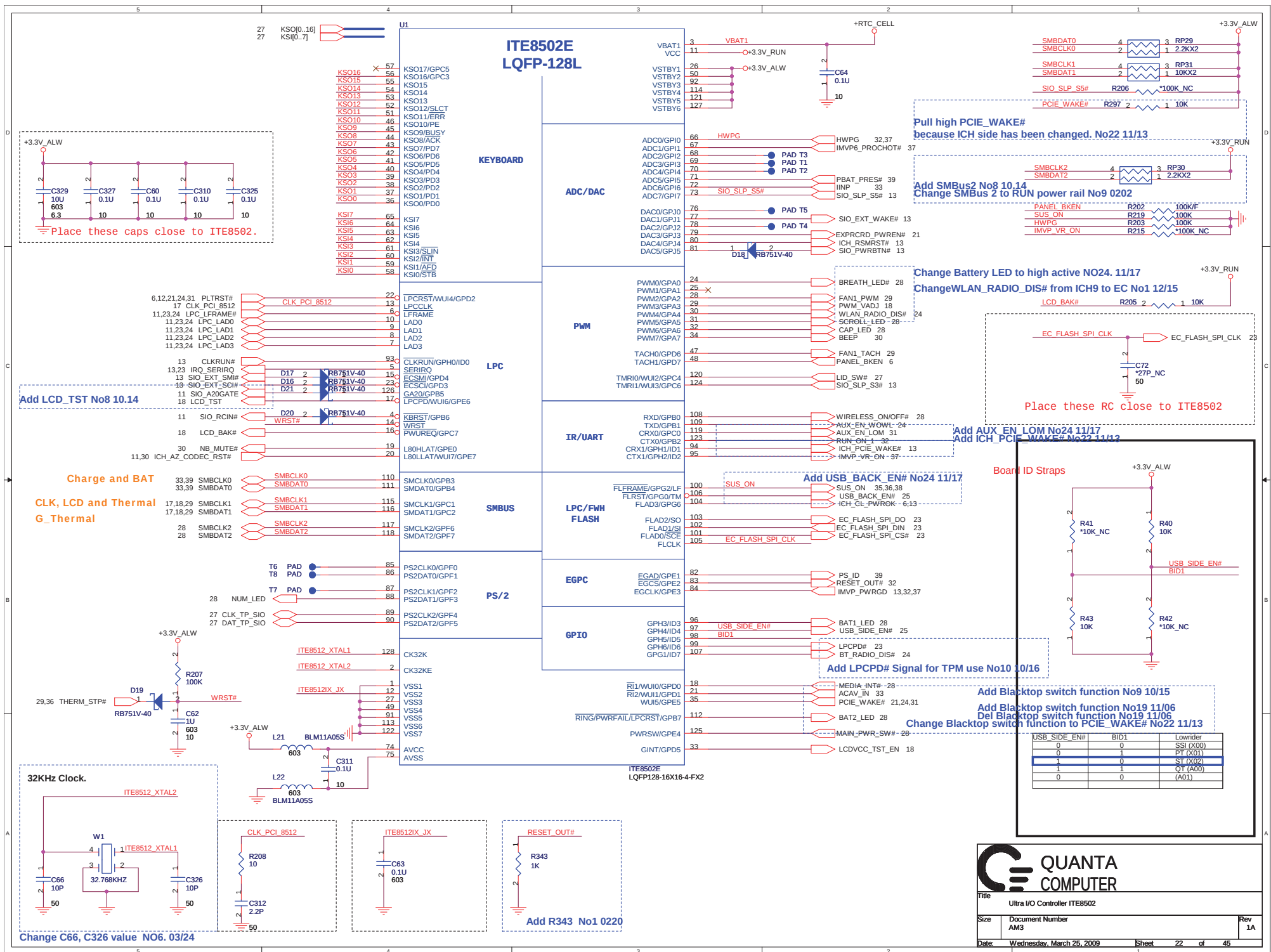
3 IN 1 CARD READER (SD/MMC/HCS memory Card)



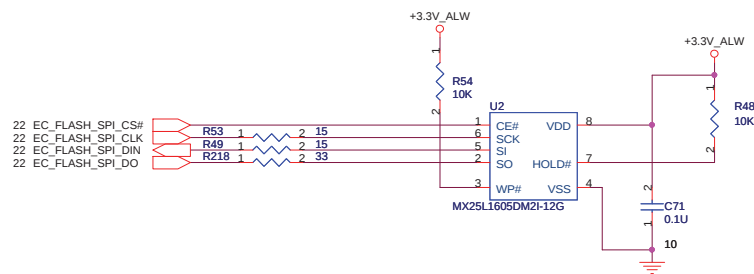
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5 IN 1 CONTROLLER		
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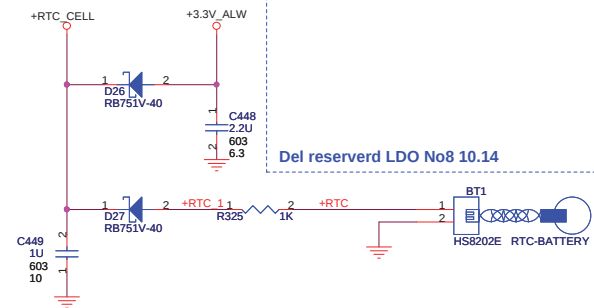
Express Card



16Mbit (2M Byte), SPI

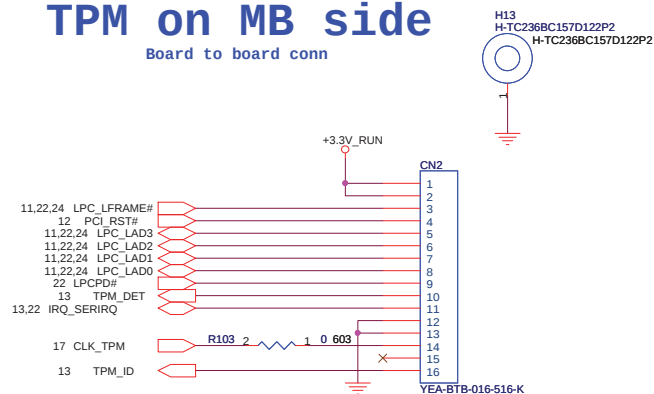


RTC BATTERY



TPM on MB side

Board to board conn

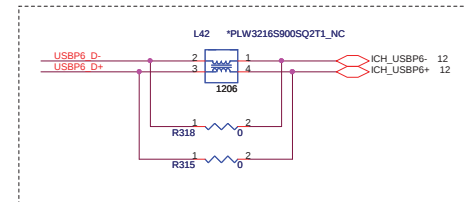
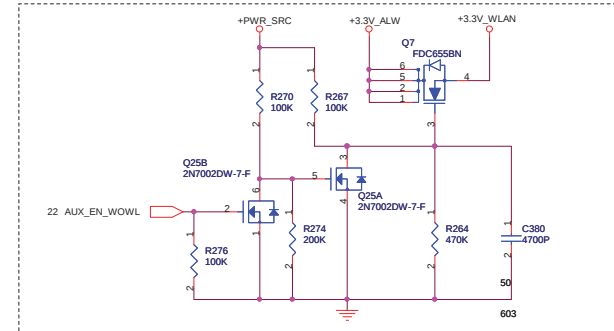
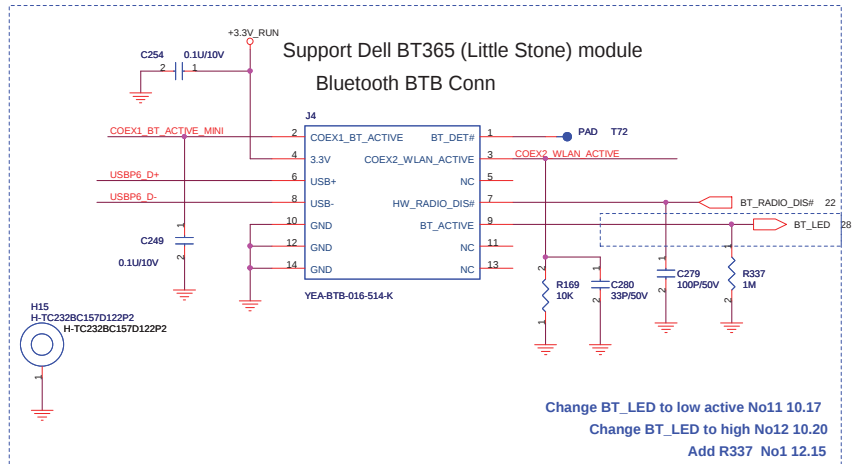
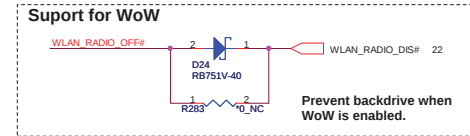
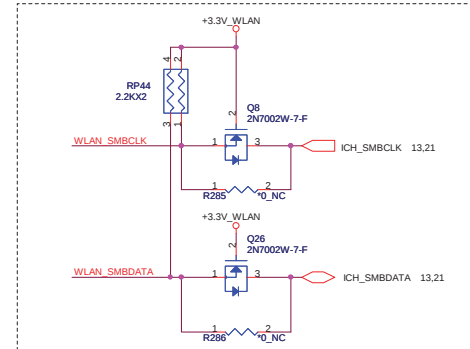
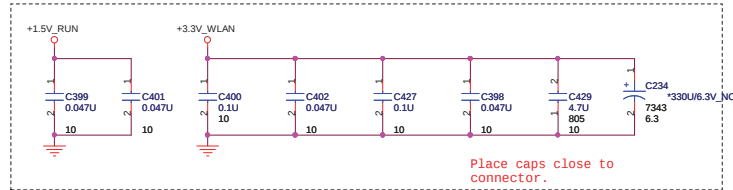
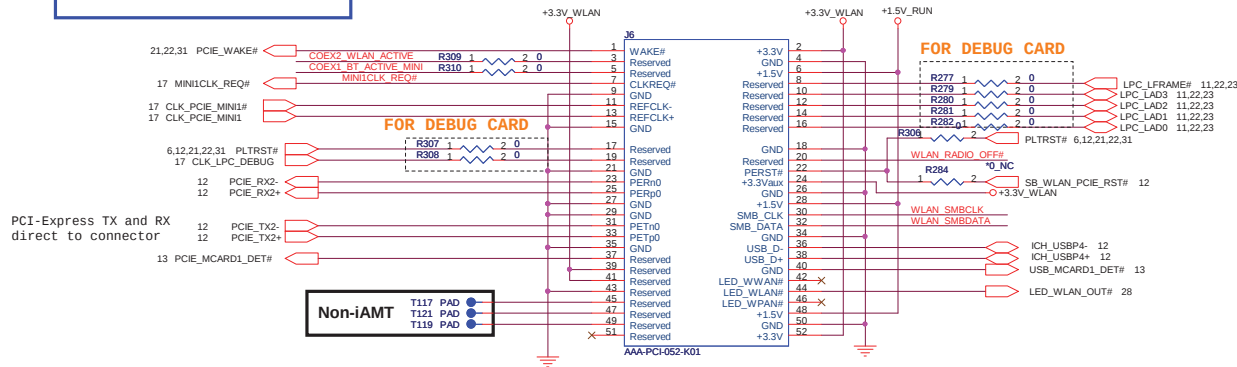


Change pin define and add TPM_DET and LPCPD# No10 10/16

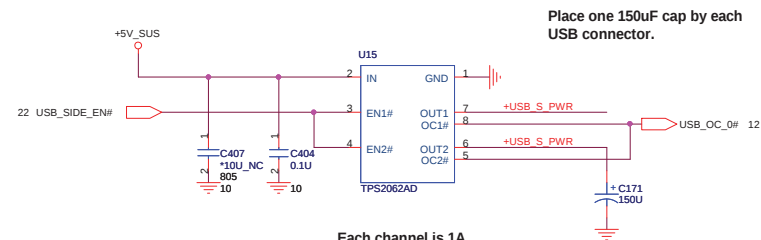
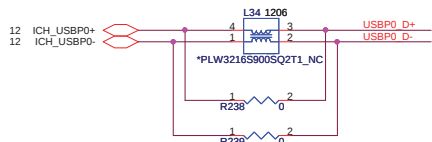
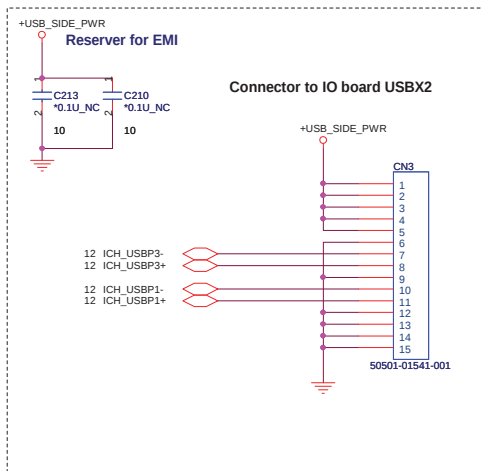
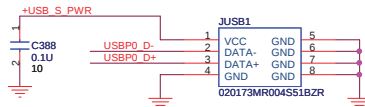
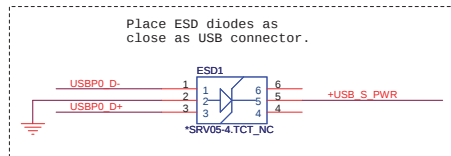
Add 0-ohm resister for EMI request No16 10/29

Add TPM_ID No22 11/13

MiniCard WLAN connector

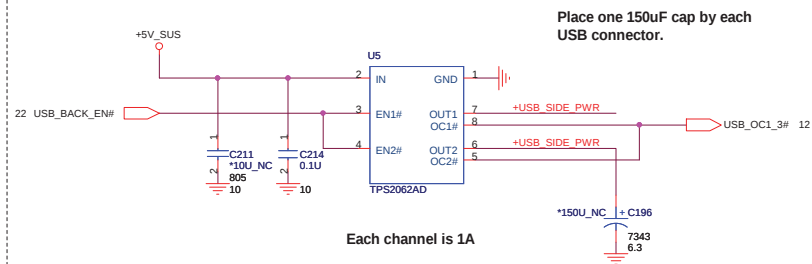


Title			
MDC CONN.			
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AM3		1A	
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Update USB OC circuit No24 11/17
Change C171 PN No1 0220

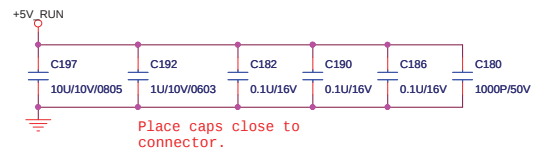
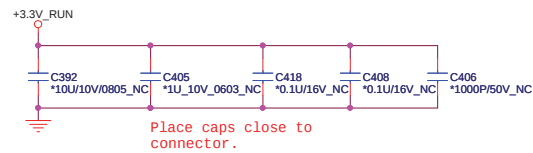
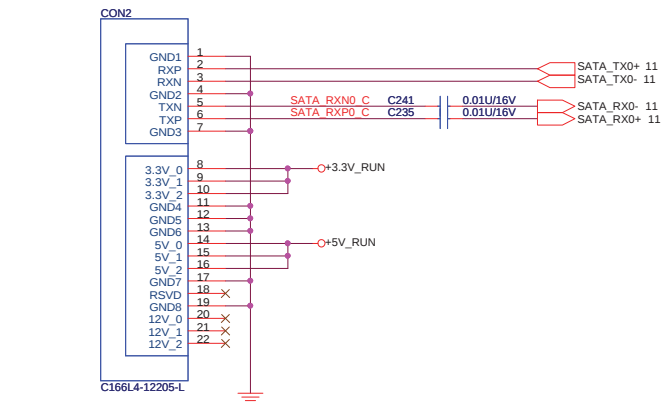
Each channel is 1A



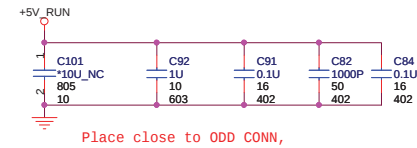
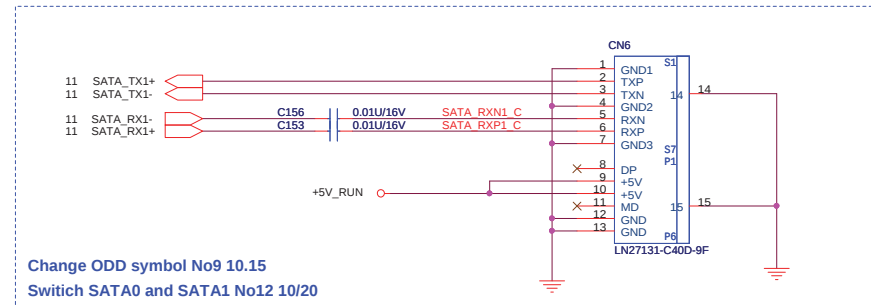
Move 2062 from IO to MB No13 10.21

Each channel is 1A

SATA HDD Connector.

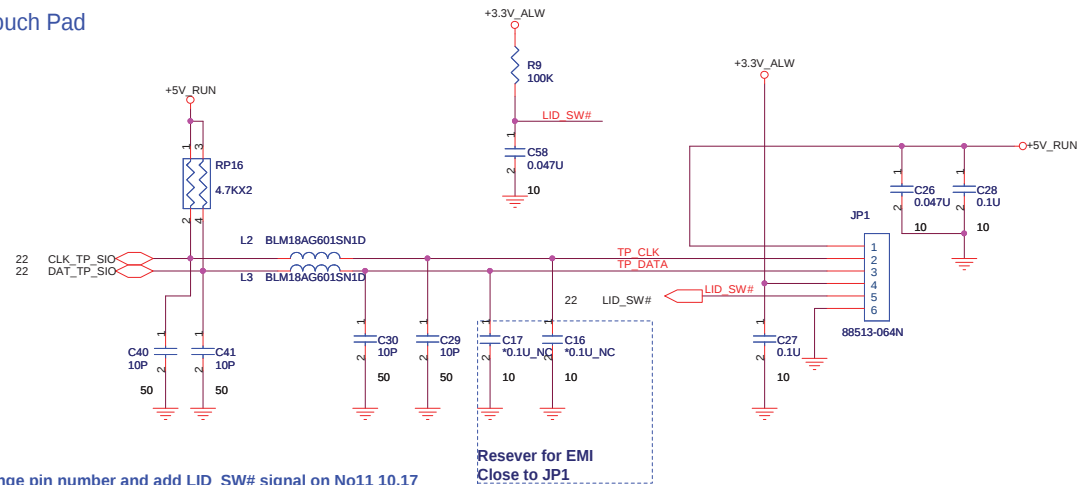


SATA ODD Connector.



Title		
SATA (HDD&CD_ROM)		
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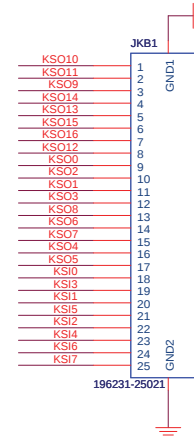
Touch Pad



Change pin number and add LID_SW# signal on No11 10.17
 Change pin define No14 10/22
 Change touch pad pn and footprint No14 10/22
 Change Touch pad pin define, avoiding power and ground pin close to each other

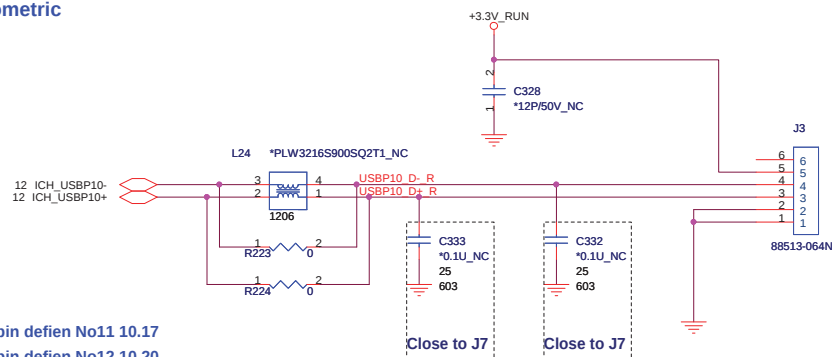
KEYBOARD CONNECTOR

22 KSO[0..16]
 22 KSI[0..7]



Change pin define No14 10/22
 Change pin define No22 11/13

Biometric

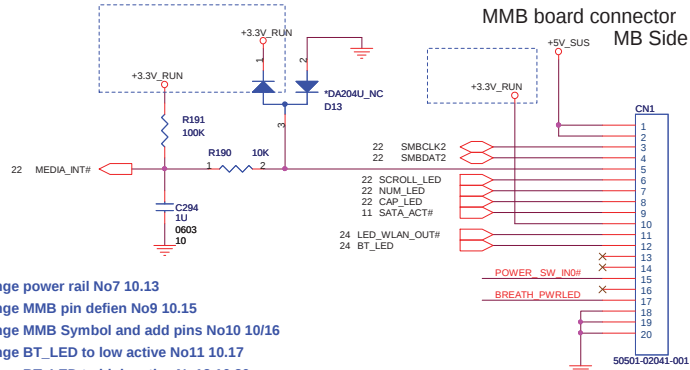


Change pin defien No11 10.17
 Change pin defien No12 10.20
 Change touch pad pn and footprint No14 10/22
 Change FP pin define No15 10/24
 Change FP pin define No23 11/14



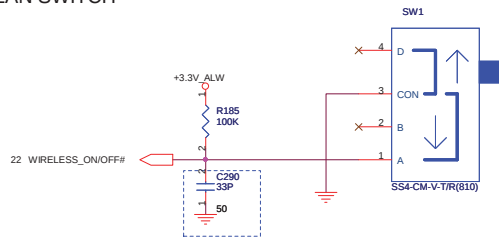
QUANTA
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Title	TOUCH PAD, BULE TOOTH & FIR		
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Change power rail No7 10.13
 Change MMB pin defien No9 10.15
 Change MMB Symbol and add pins No10 10/16
 Change BT_LED to low active No11 10.17
 Change BT_LED to high active No12 10.20
 Change 3.3V_ALW to 3.3V_SUS No24 11/17
 Change MMB IC power rail from SUS to RUN No26 11/19

WLAN SWITCH



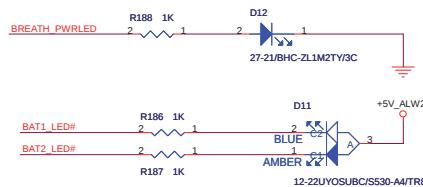
Change C290 PN and size No3 0318

Battery status.



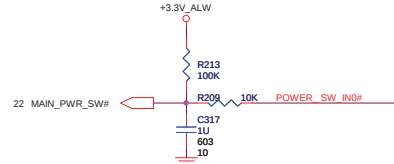
Change Battery setting NO20. 11/11
 Change Battery setting NO24. 11/17

Right angle LED



Change Battery setting NO20. 11/11
 Change Battery setting NO24. 11/17
 Change R186., R187 and R188 value NO6. 03/24

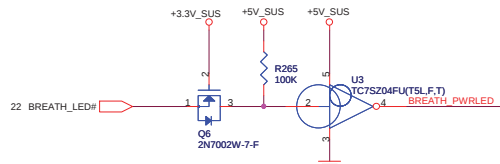
Power Switch



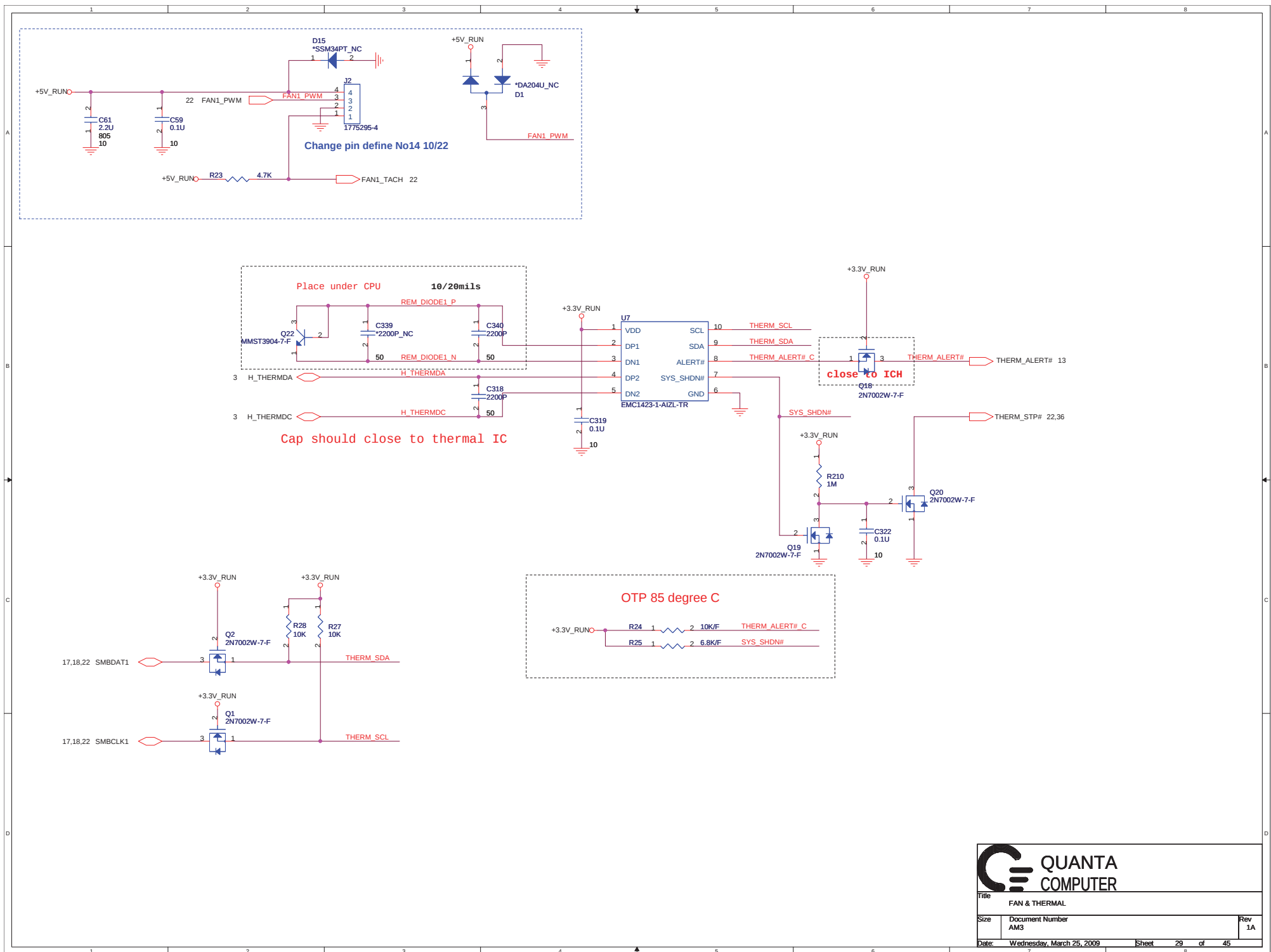
Blacktop Switch

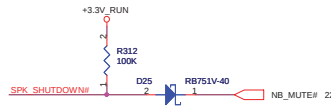
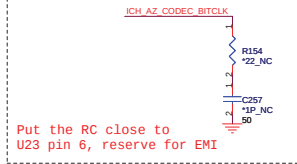
Add Blacktop switch function No9 10/15
 Del Blacktop switch function No19 11/06
 Add Blacktop switch function No19 11/06
 Del Blacktop switch function No23 11/14

Power & Suspend.



Add WLAN LED on MB NO7. 10/13
 Del WLAN LED on MB No9 10/15

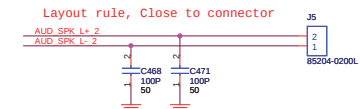




Add PC beep for system error circuit No9 10.14

Del PC beep No9 10.15

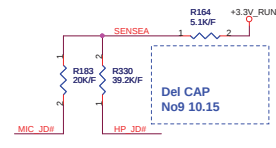
Speakers conn



Add ESD2 for ESD concern No6 1/19

Remove ESD2 for ESD concern No8 1/21

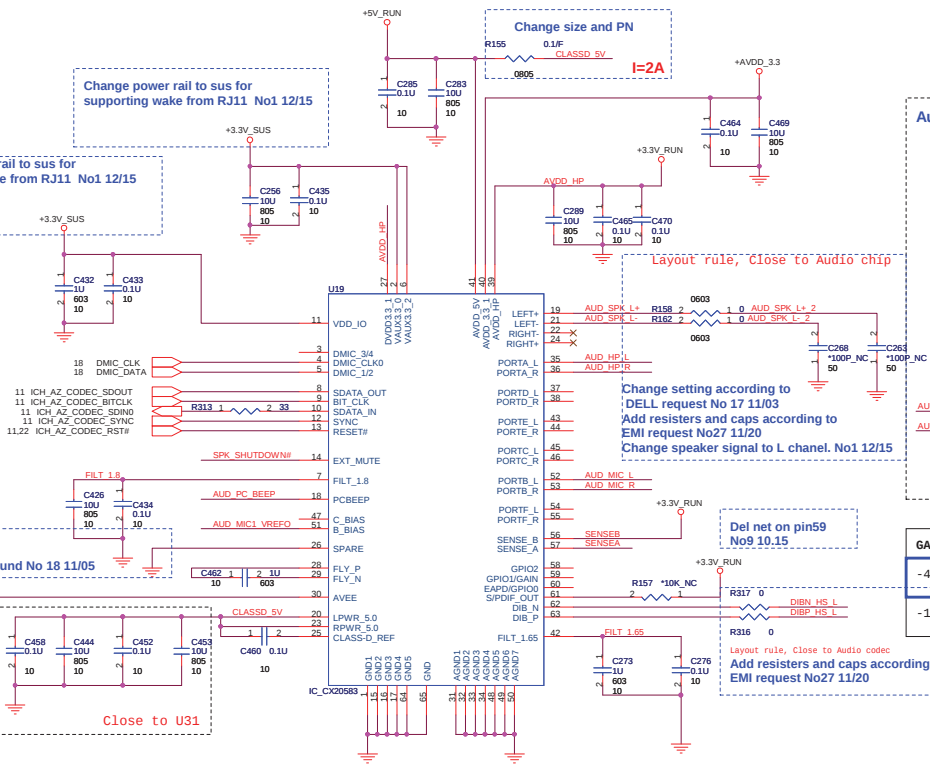
Jack Sense

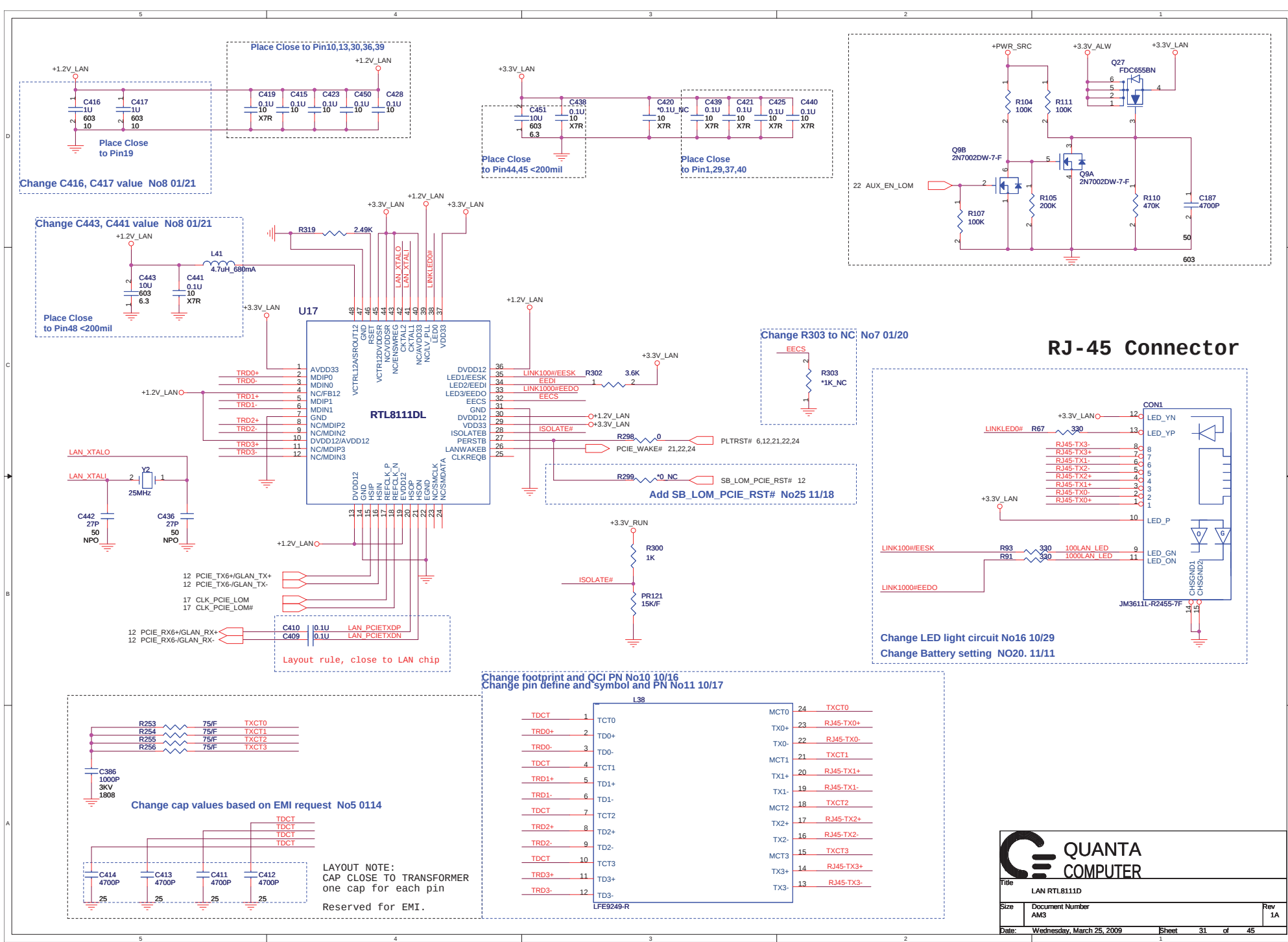


AUDIO CODEC

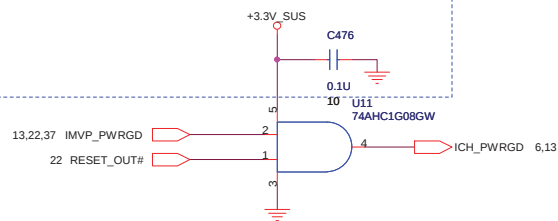
Change power rail to sus for supporting wake from RJ11 No1 12/15

Change power rail to sus for supporting wake from RJ11 No1 12/15

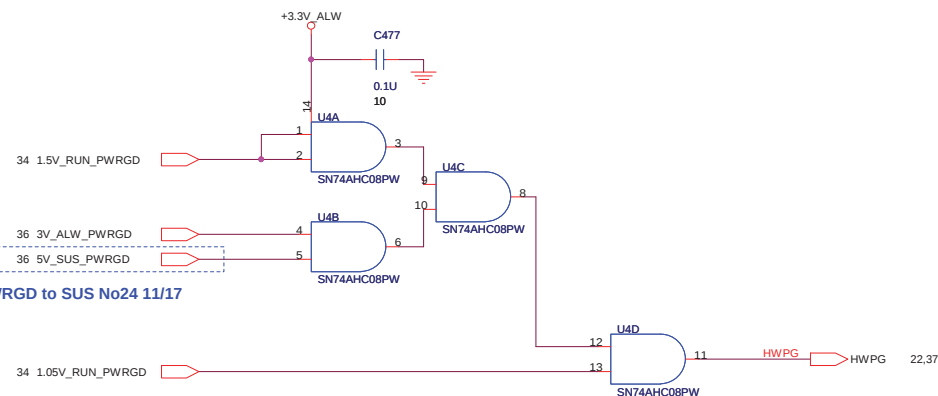




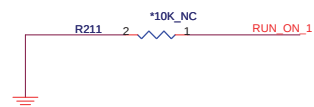
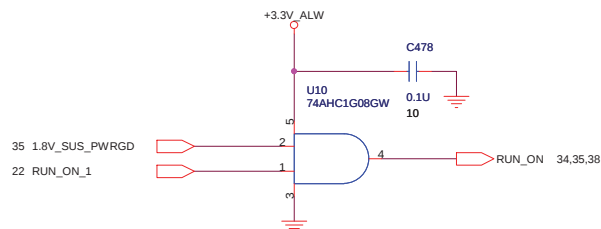
Change power source No22 11/13
Remove 0-ohm resistor and 3.3V_ALW power rail No3 01/06



Keep Away from high speed buses



Change from 5V_ALW_PWRGD to SUS No24 11/17



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Title	System Reset Circuit	
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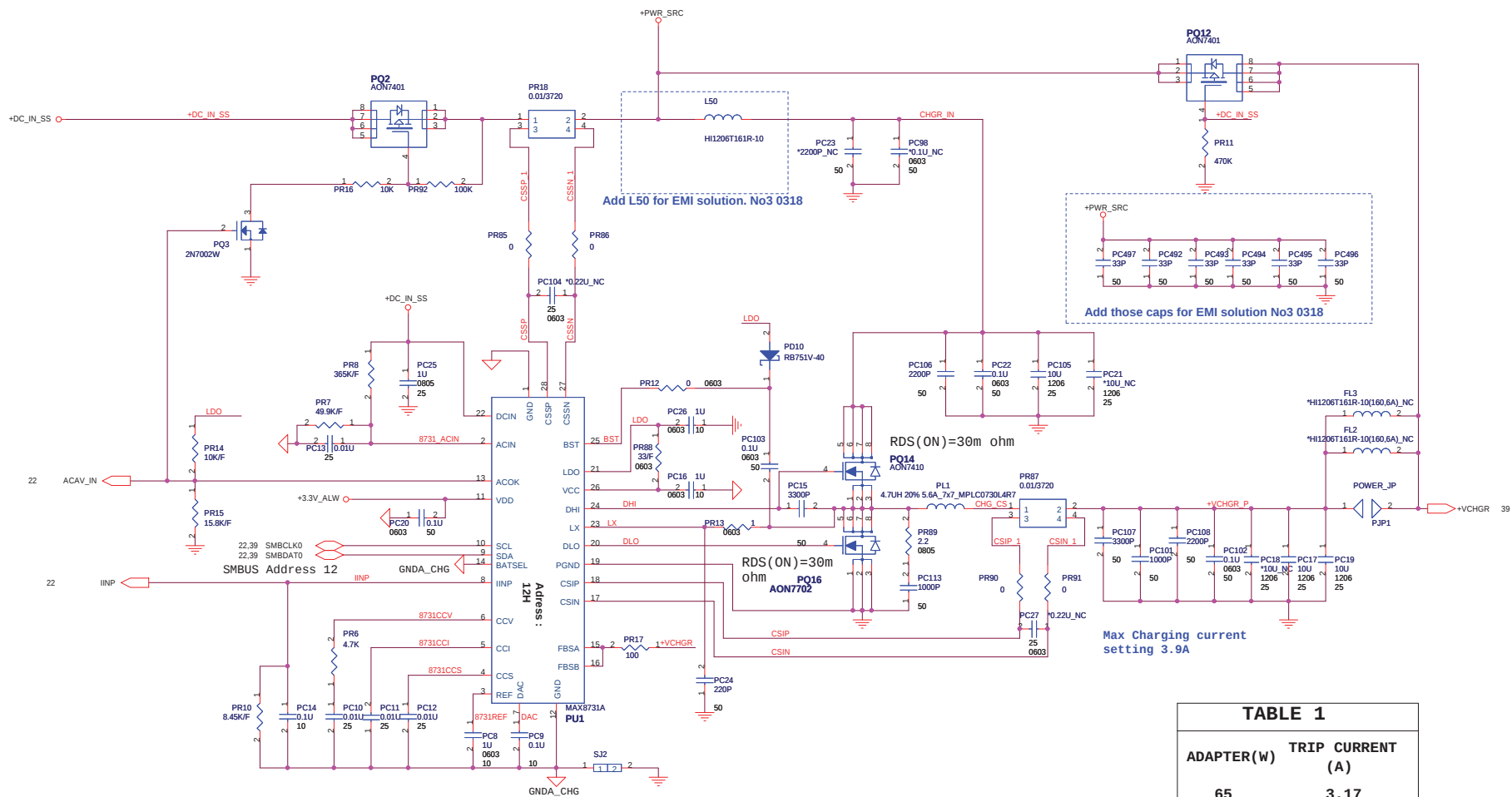
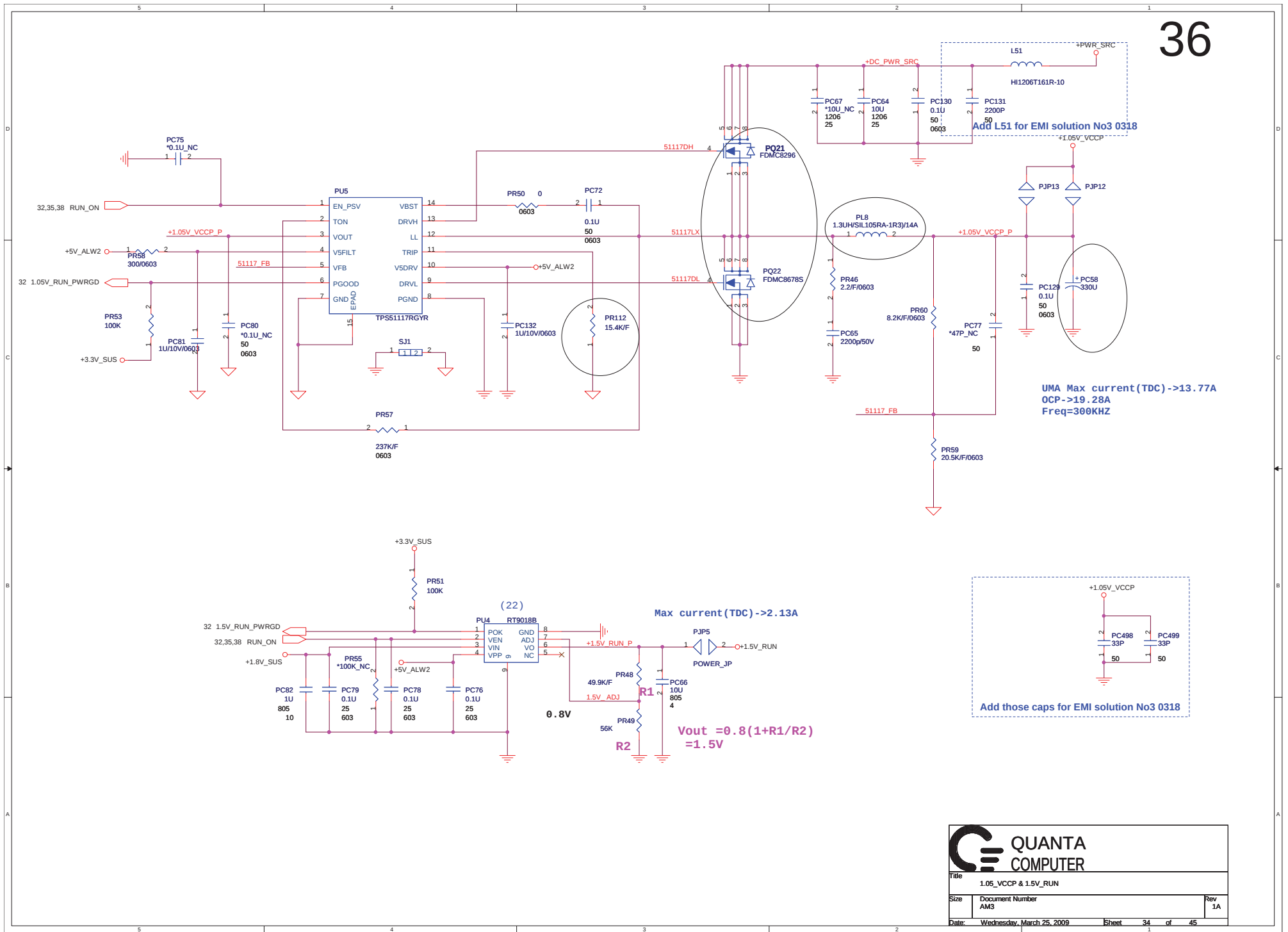
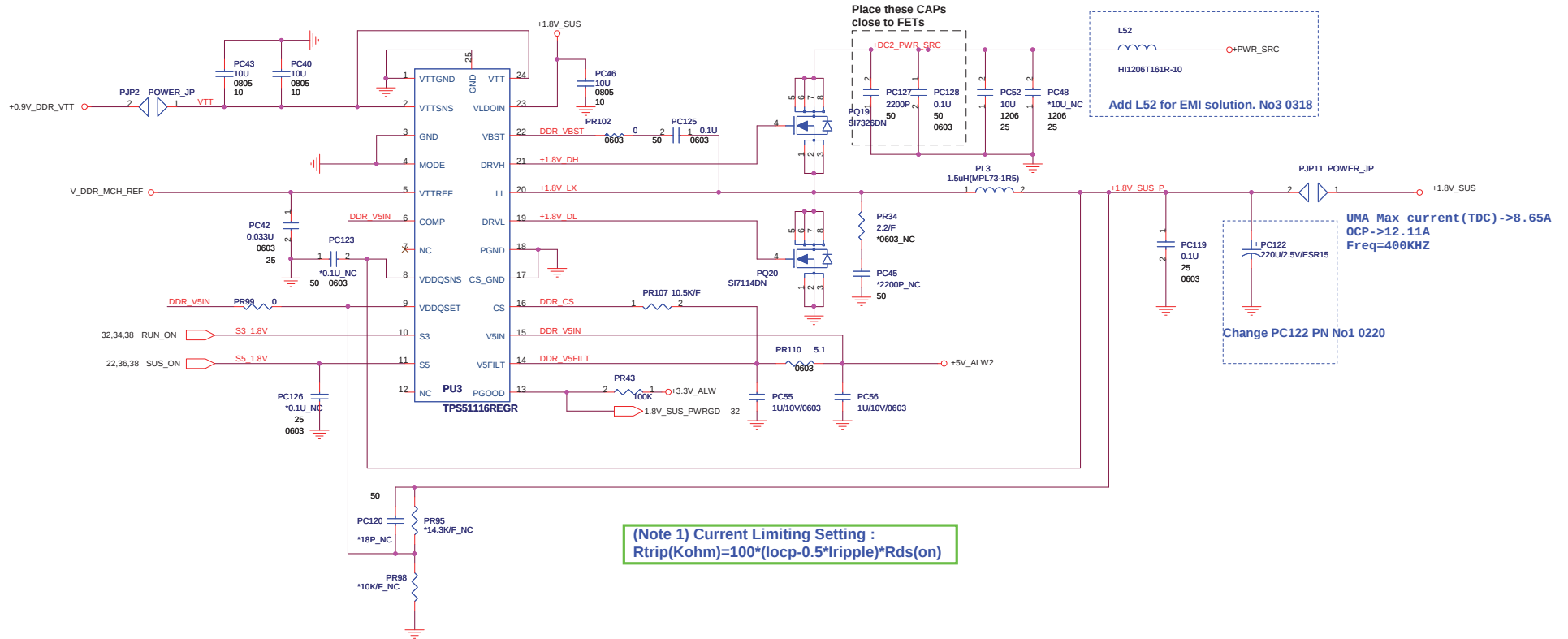
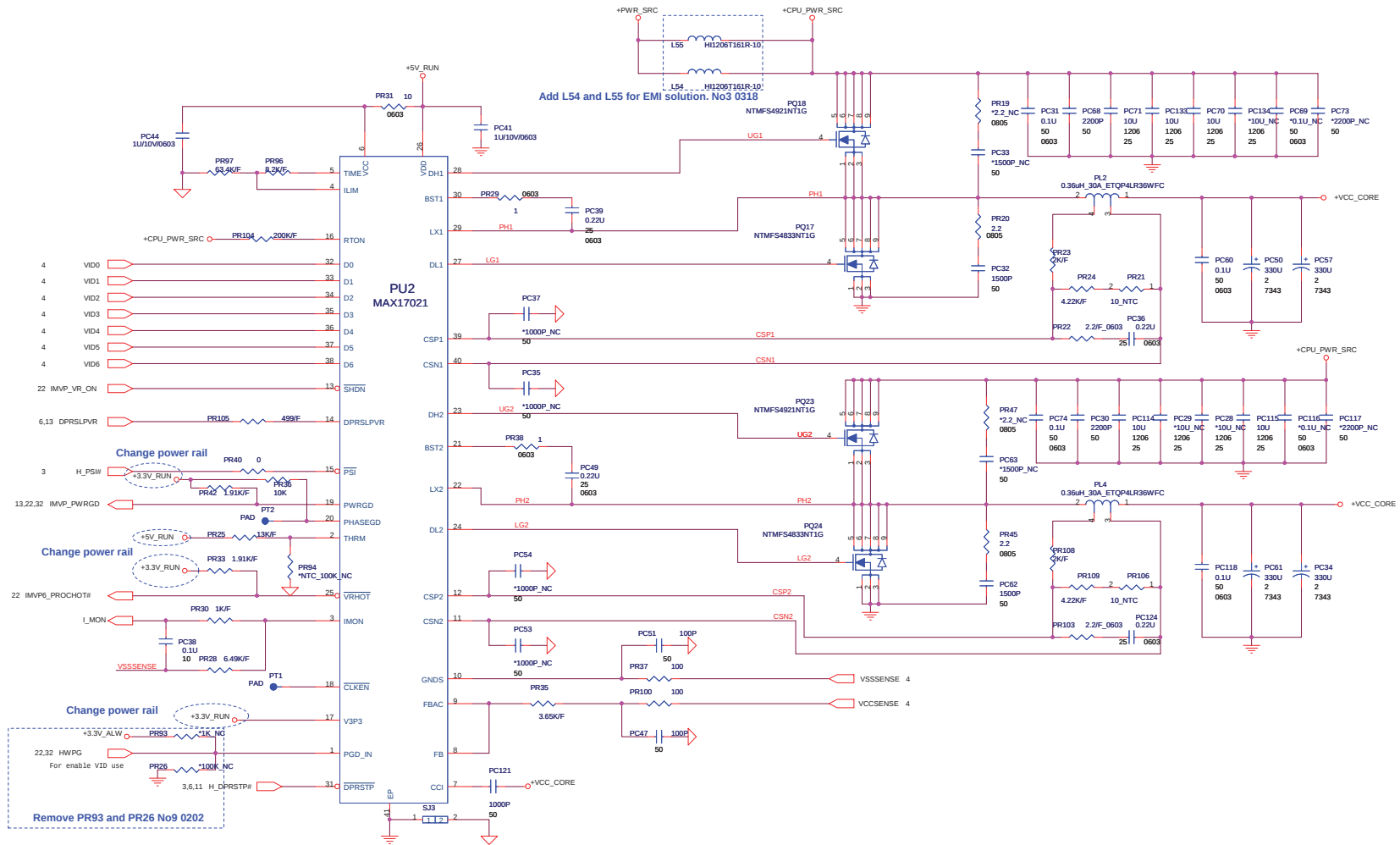


TABLE 1	
ADAPTER(W)	TRIP CURRENT (A)
65	3.17
90	4.43
130	6.43
150	7.43
200	9.75
230	11.28 (see note3)







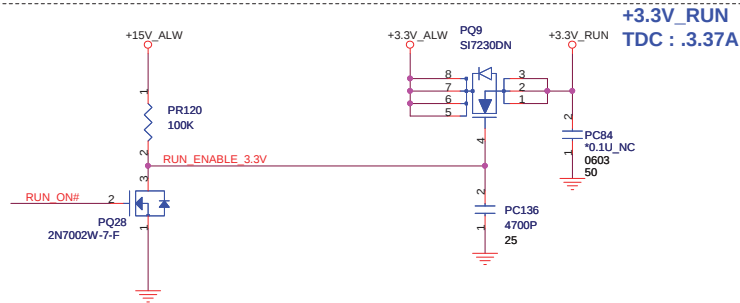
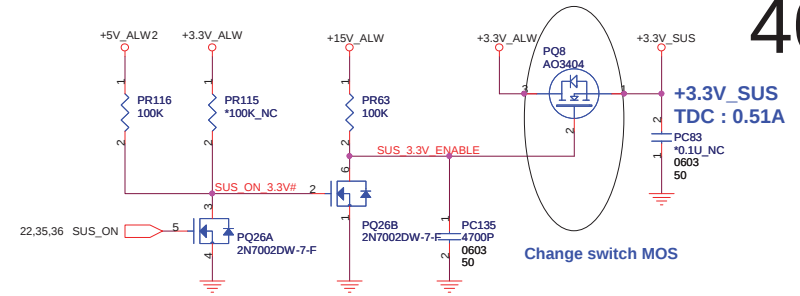
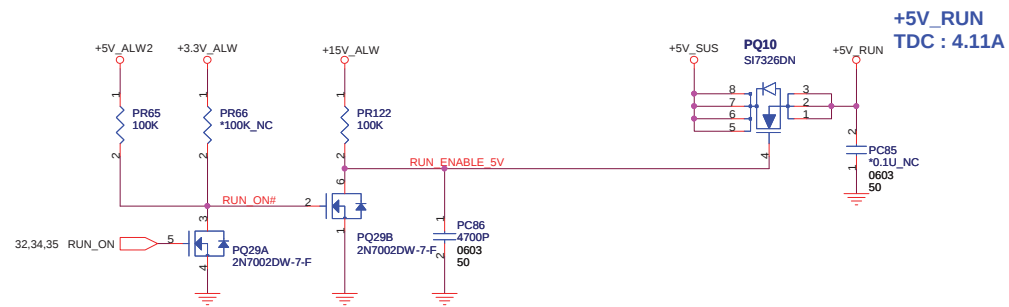
File: Vcore-MAX17021

Size: Document Number AM5

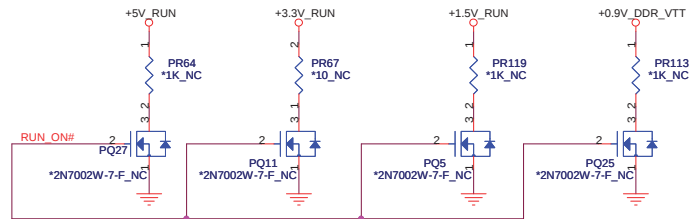
Date: Wednesday, March 29, 2009

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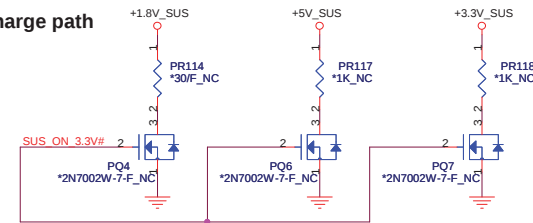
Rev 1A



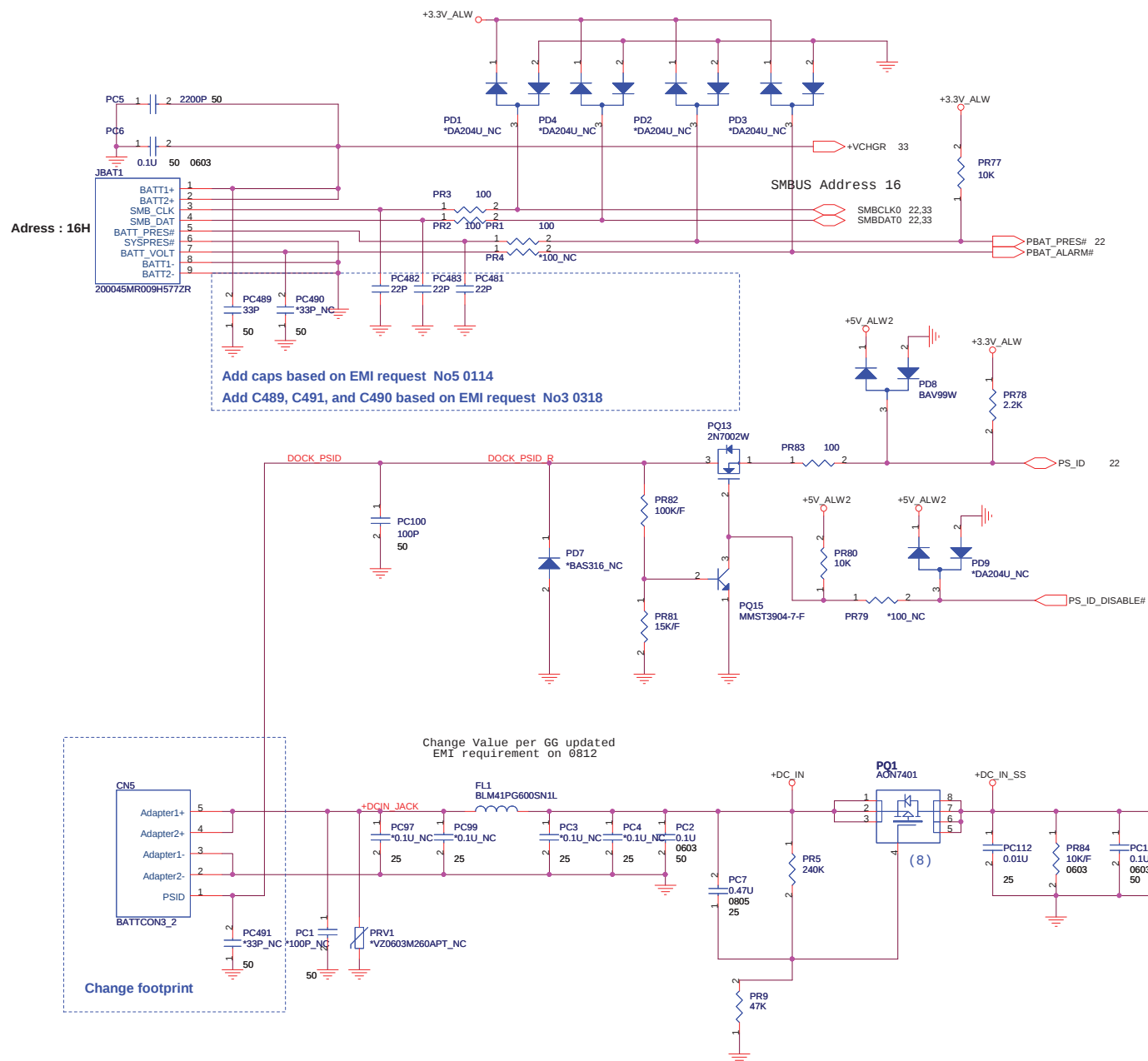
Reserve discharge path



Reserve discharge path

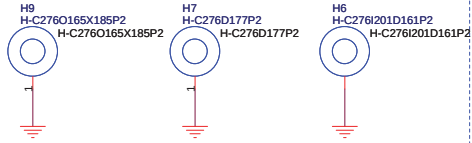


Title	RUN POWER SW		
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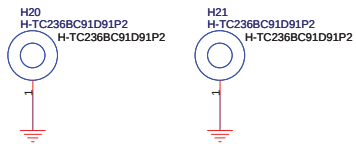


Create hole footprints No9 10.15

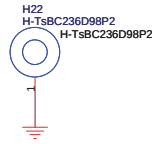
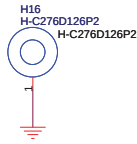
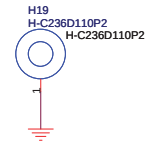
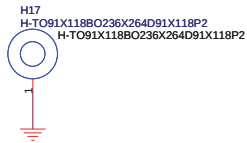
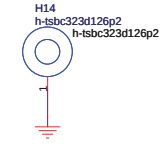
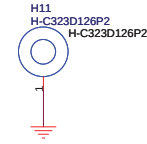
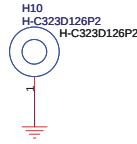
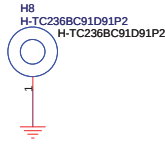
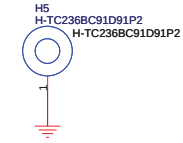
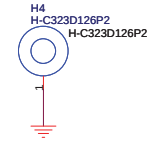
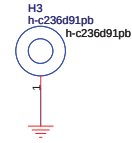
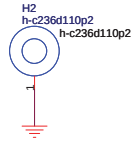
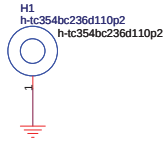
For CPU use



For ODD use

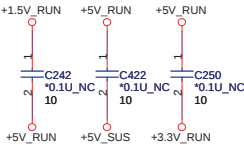


Add Screw hole No6 0119

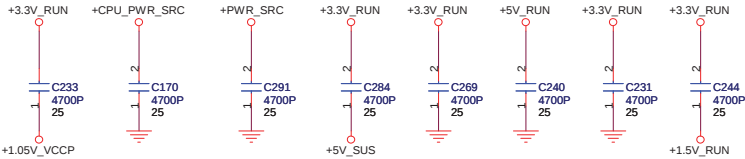


Reserved for EMI.

Stitching caps for PCI bus.



Stitching caps for PCI EMC.



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