

Model Name: KAL80

PCB NO: LA-4232P

BOM P/N:

Half Penny Bridge 13.3

Compal Confidential

Schematic Document

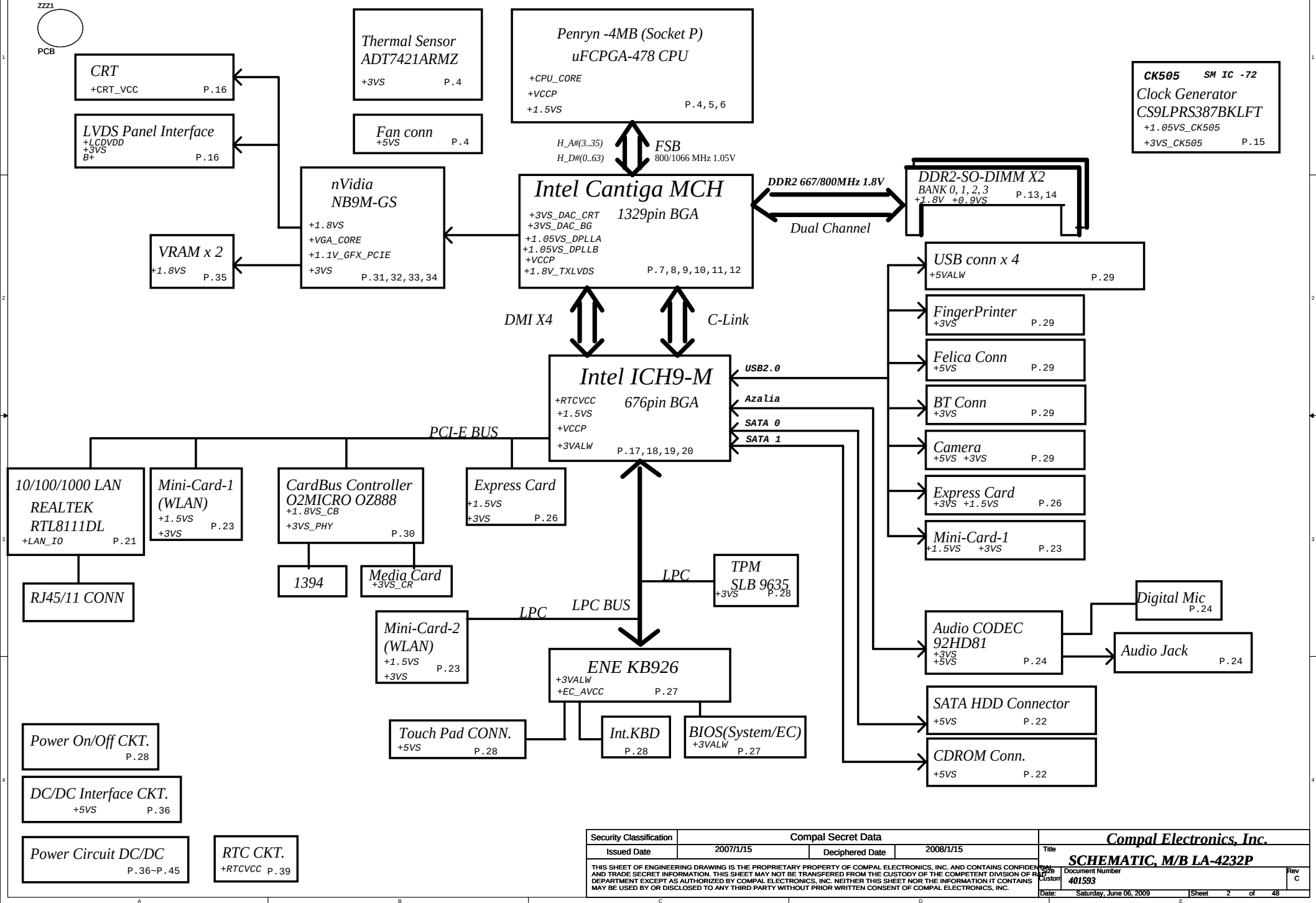
Cantiga + ICH9

2009 / 06 / 01 Rev:1.0(A00)

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ZZZ1
PCB



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Voltage Rails 0 MEANS ON X MEANS OFF

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE
				+VGA_CORE +1.8VS +1.1VS +0.9VGA
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

ICH9-M	USB PORT#	DESTINATION
	0	JUSBP1
	1	CAMERA
	2	JUSBP3(SINGLE)
	3	Felica
	4	Blue Tooth
	5	Finger Printer
	6	JMINI2-WLAN
	7	Express card
	8	JUSBP3(DUEL TOP)
	9	JUSBP3(DUEL BOTTOM)
	10	NA
	11	NA

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build
CONN@: connect
VGA@: discrete component
UMA@: uma component
TPM@: TPM compoent

PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD-2 WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ888
Lane 6	NA

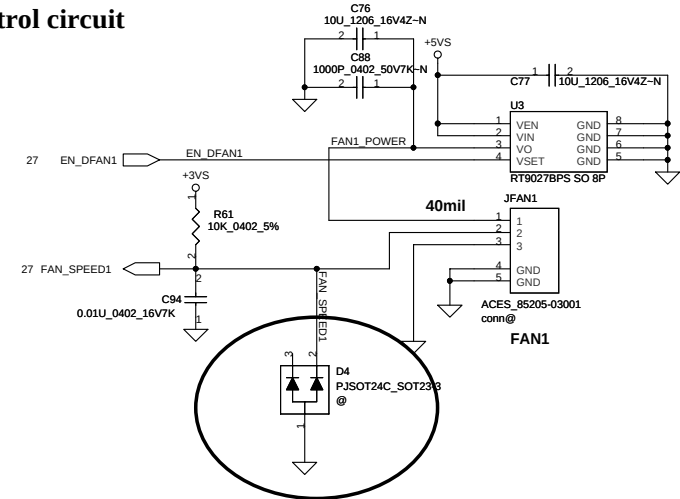
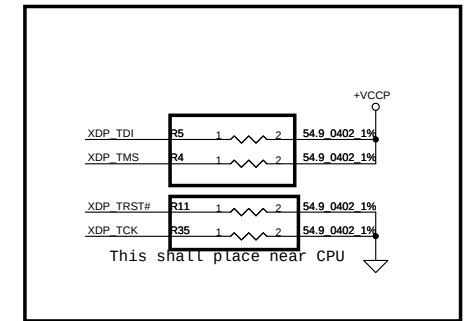
SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	X	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

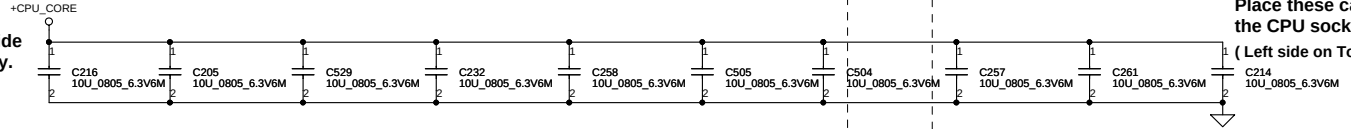


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High Frequency Decoupling

10uF 0805 X5R -> 85 degree.

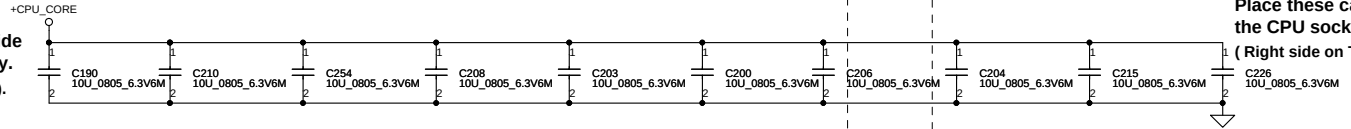
Place these caps inside the CPU socket cavity. (Left side on Top).



Place these caps inside the CPU socket.

(Left side on Top).

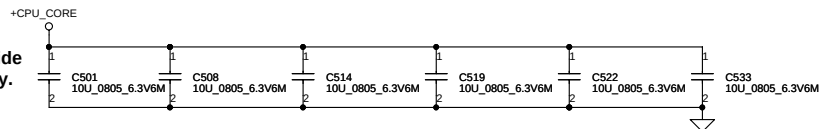
Place these caps inside the CPU socket cavity. (Right side on Top side).



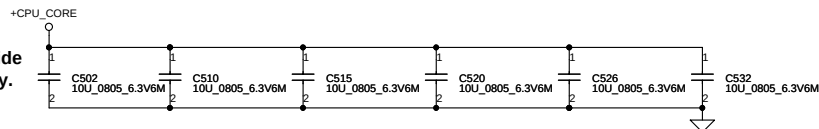
Place these caps inside the CPU socket.

(Right side on Top).

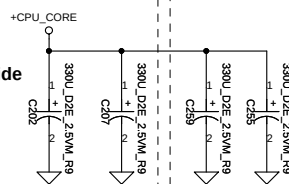
Place these caps inside the CPU socket cavity. (Left side on Bottom).



Place these caps inside the CPU socket cavity. (Right side on Bottom).

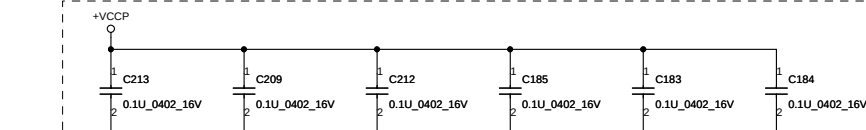


Place these caps inside the CPU socket. (Left side on Top).

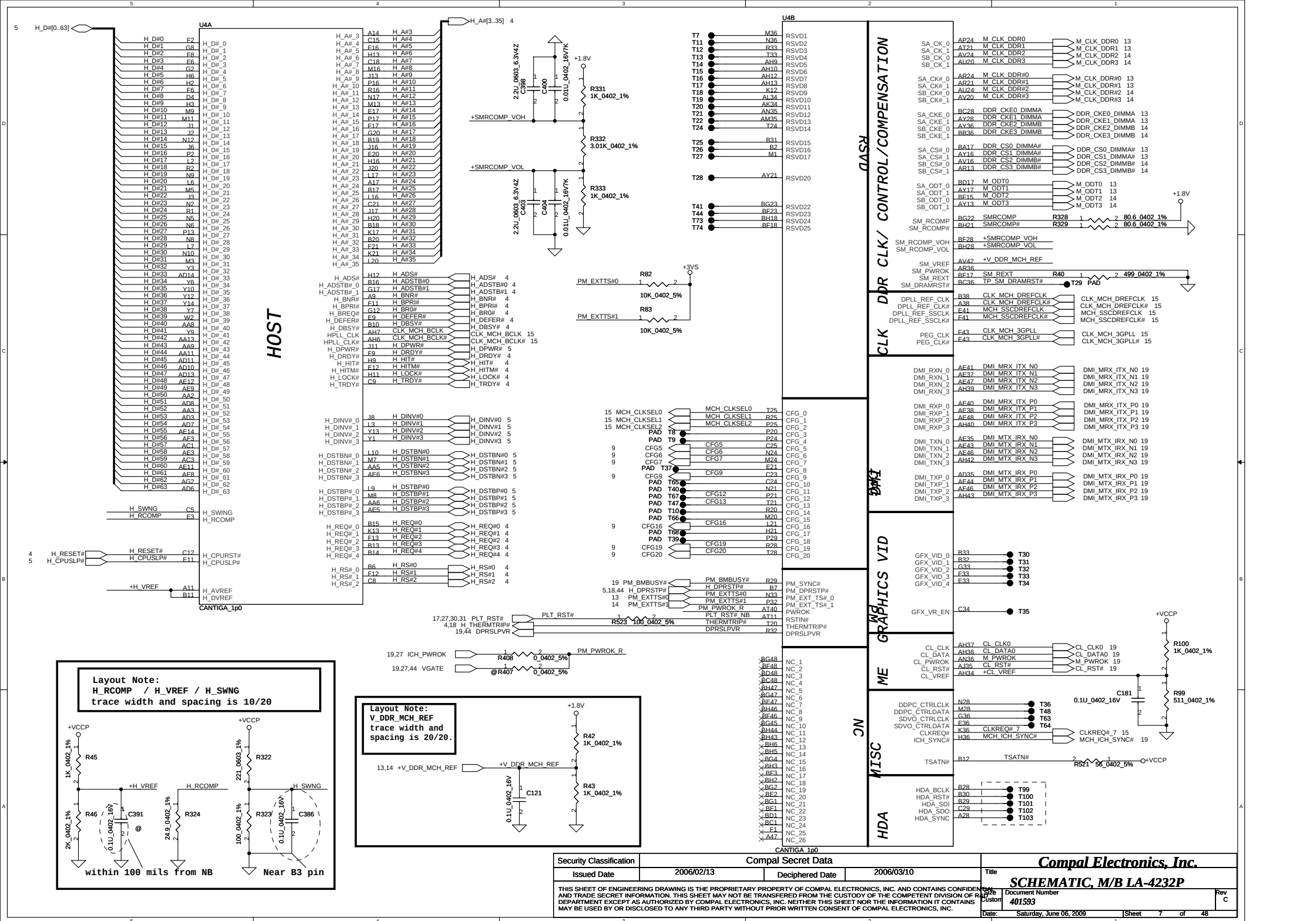


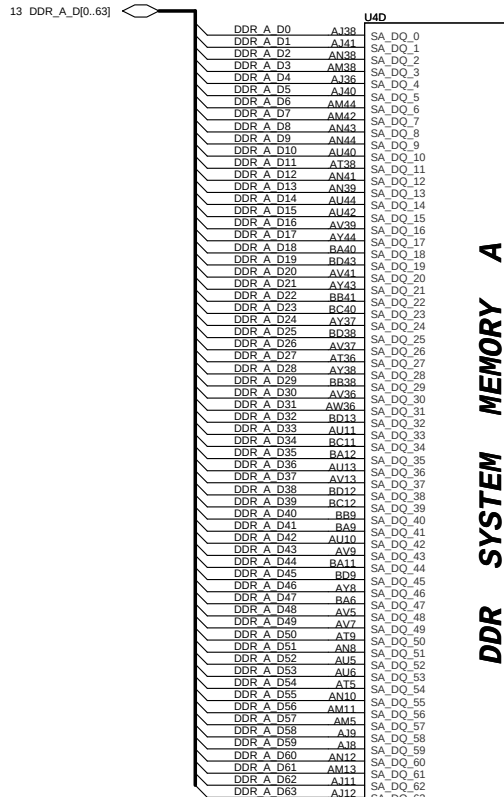
Place these caps inside the CPU socket. (Right side on Top side).

ESR <= 1.5m ohm
Capacitor > 880 uF



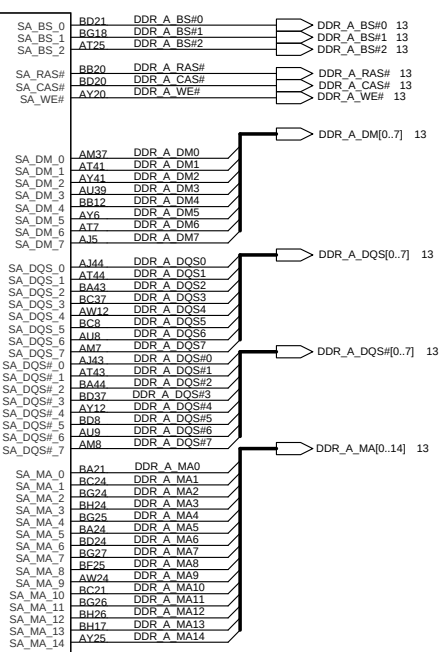
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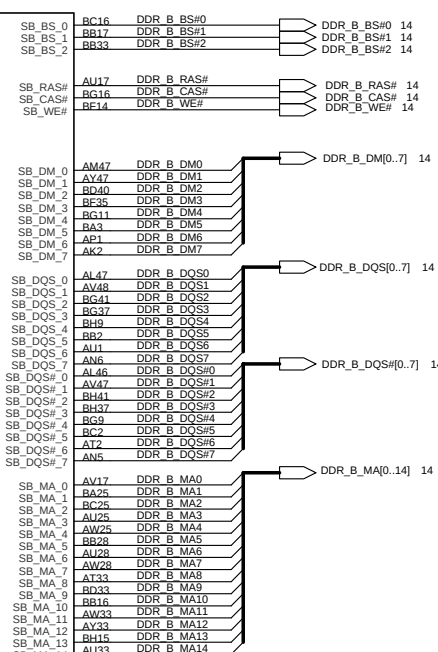
CANTIGA_1p0

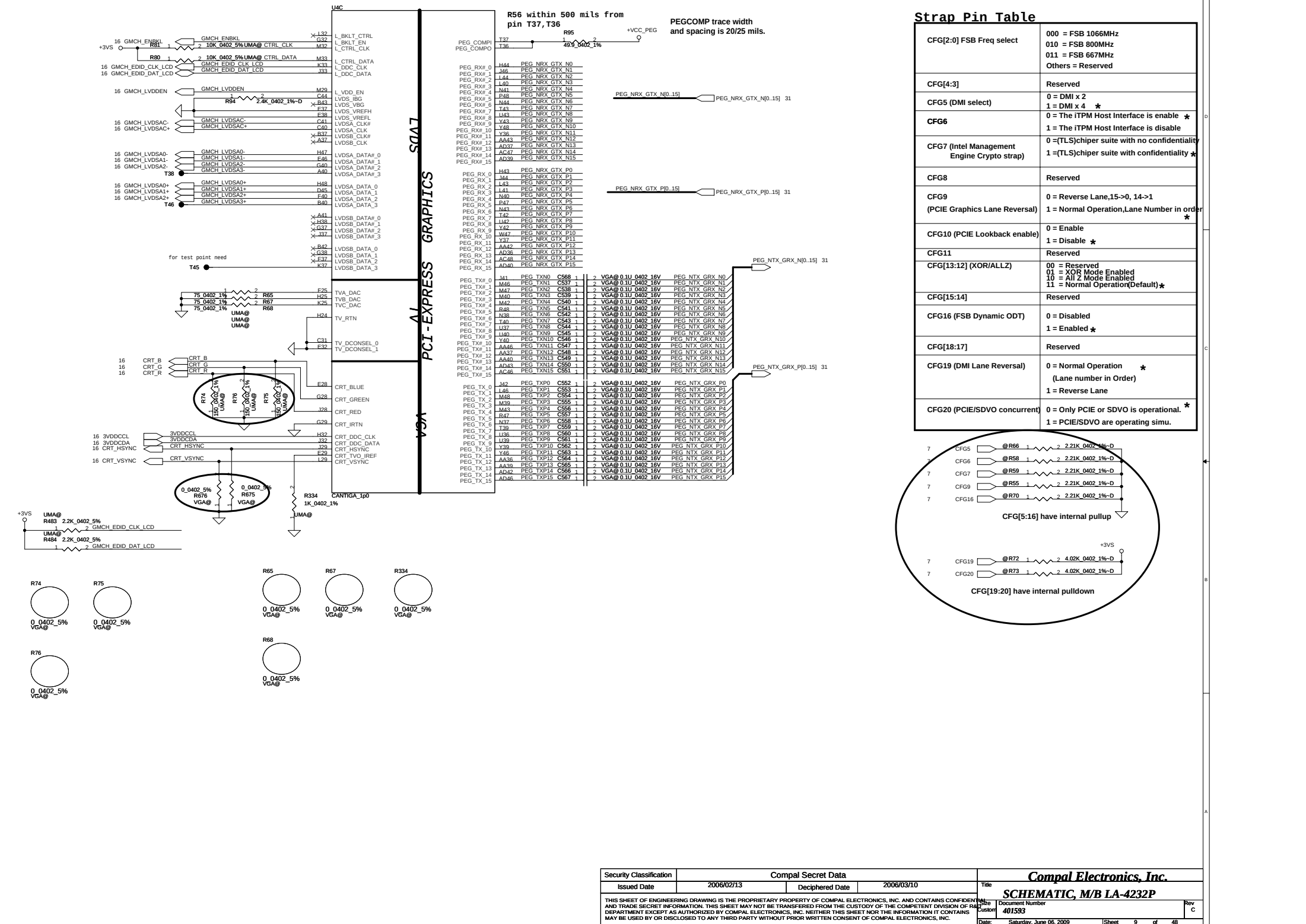
DDR SYSTEM MEMORY A



CANTIGA_1p0

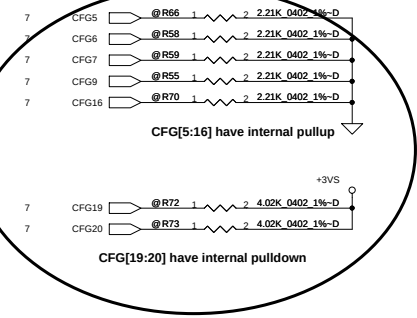
DDR SYSTEM MEMORY B

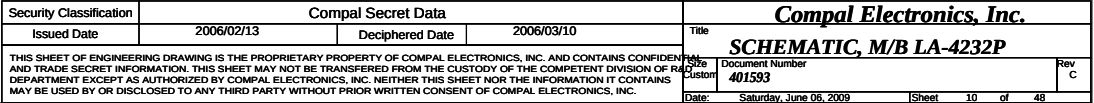


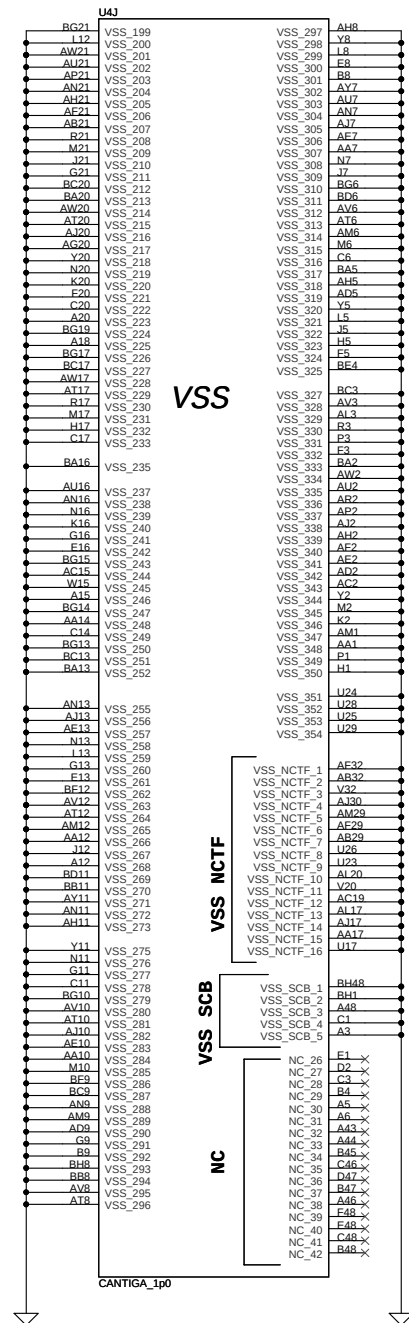
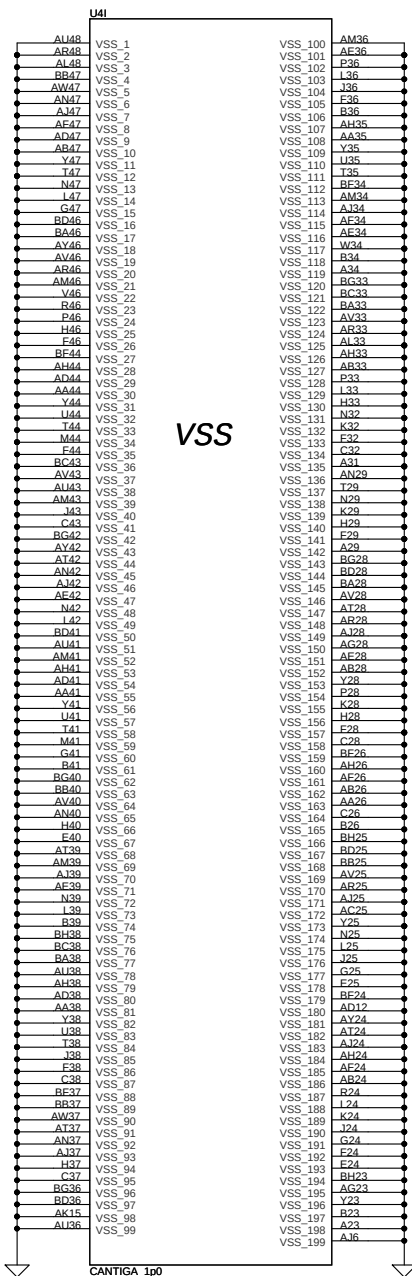


Strap Pin Table

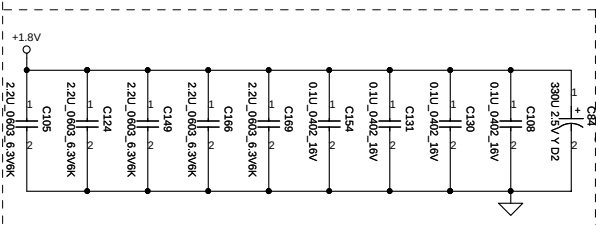
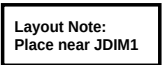
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chipr suite with no confidentiality 1 = (TLS)chipr suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation 1 = Reverse Lane *
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. 1 = PCIe/SDVO are operating simul. *



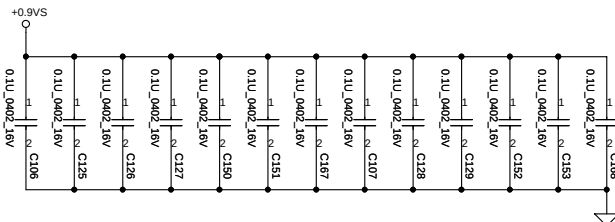




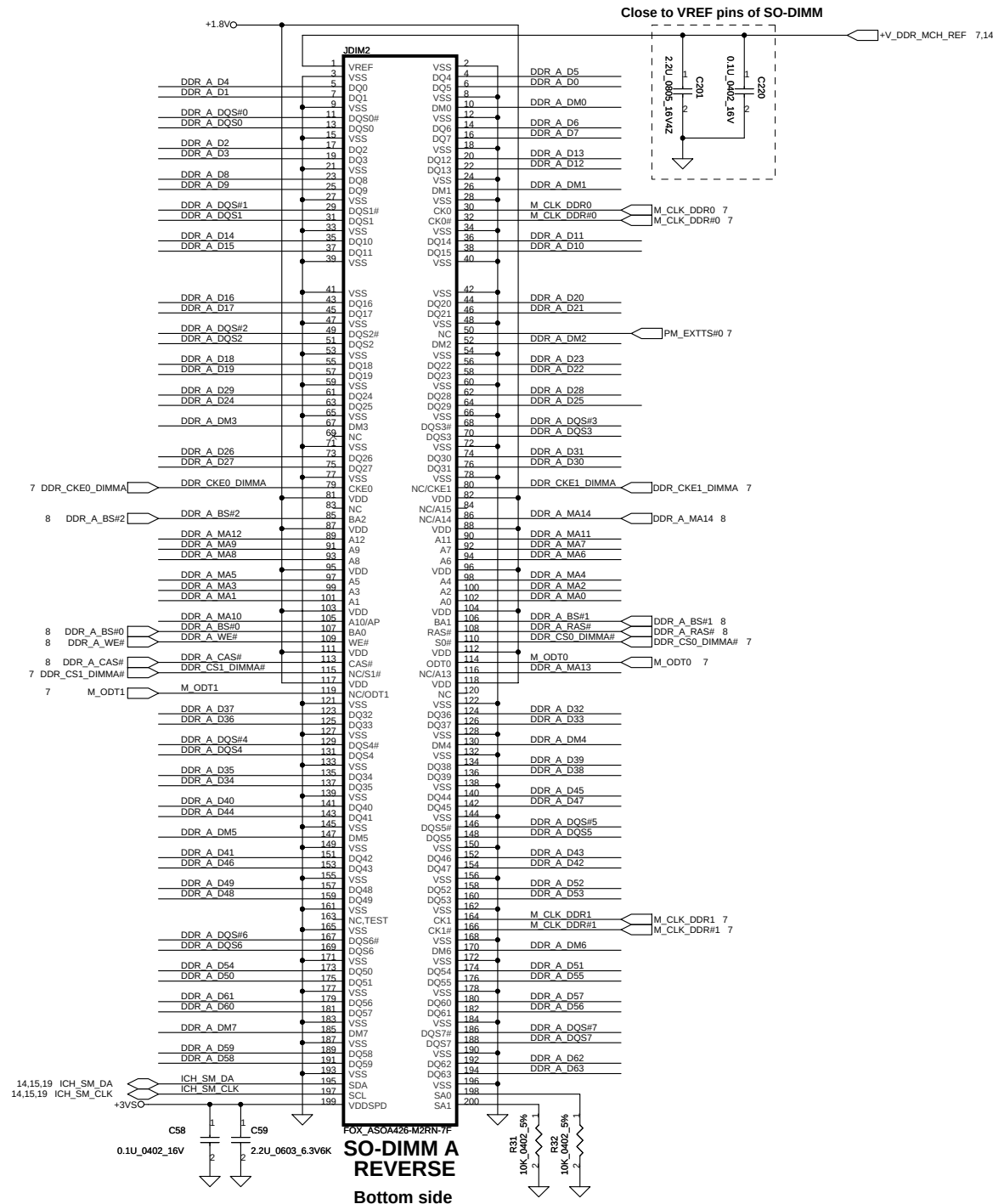
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Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

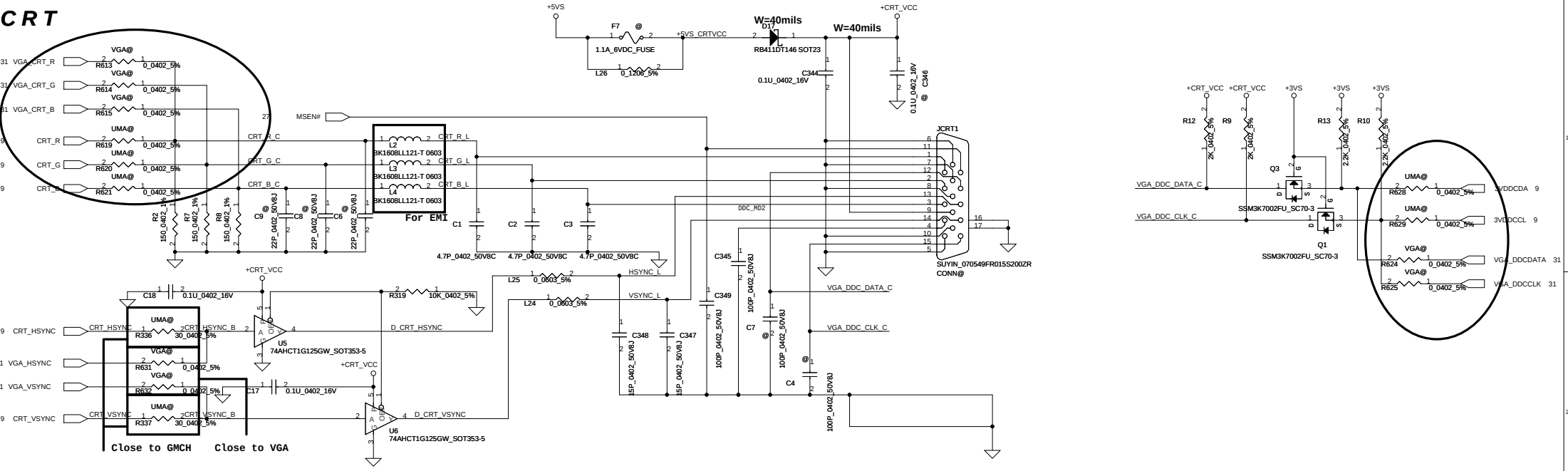


Layout Note:
Place these resistor
closely JP41,all
trace length Max=1.5"

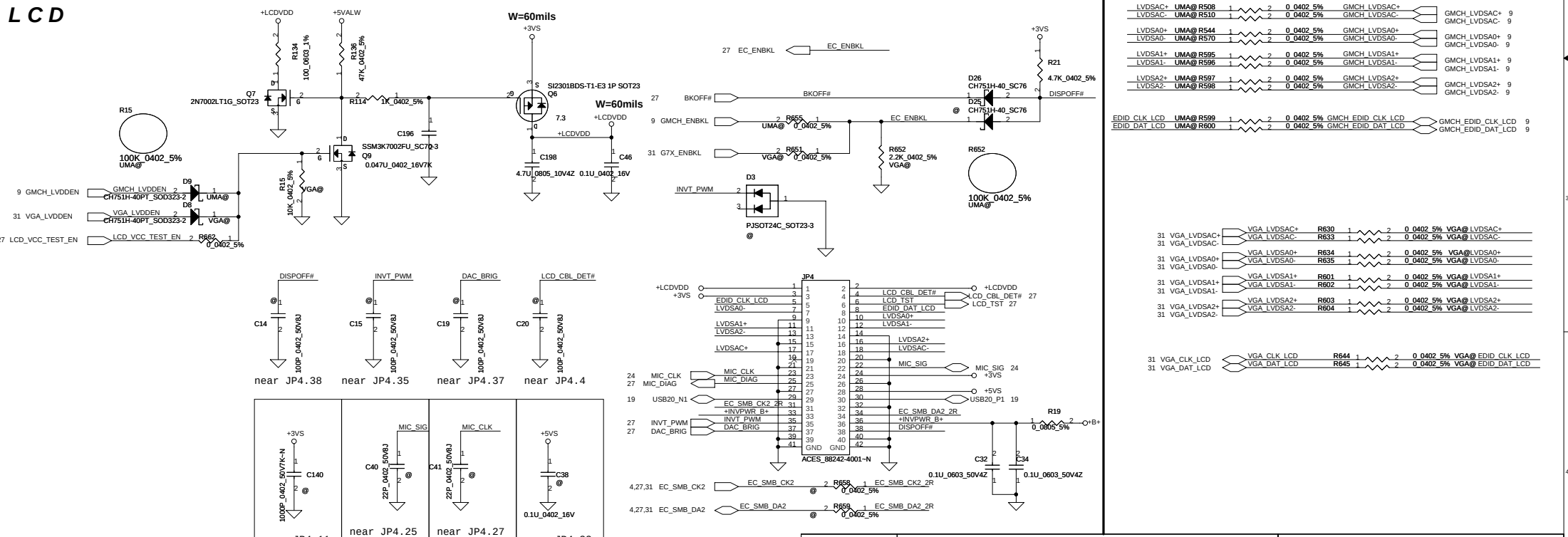


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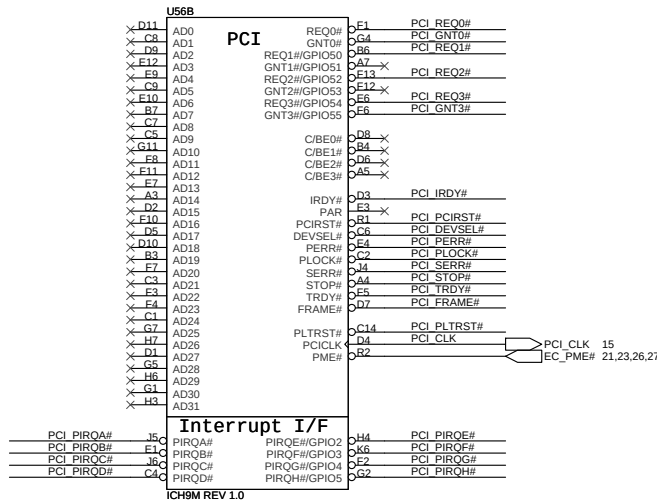
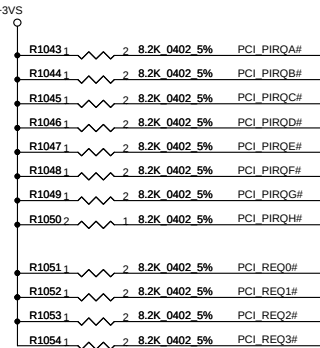
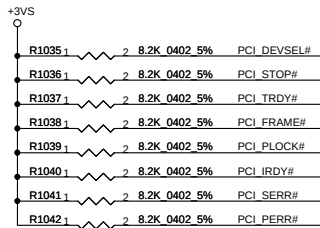
CRT



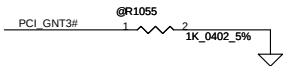
LCD



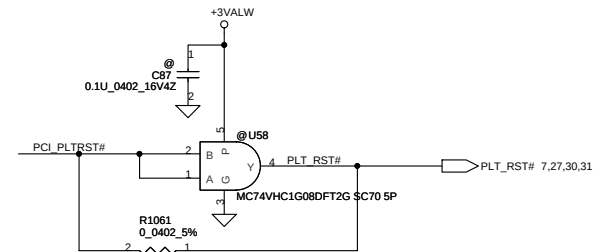
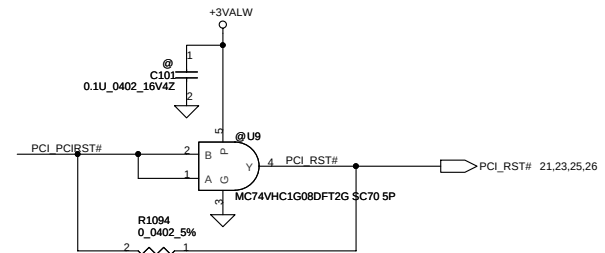
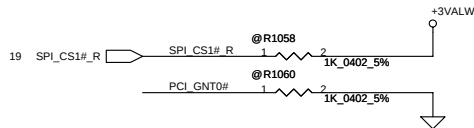
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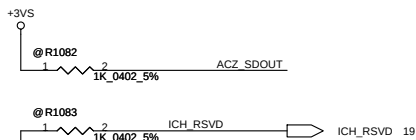
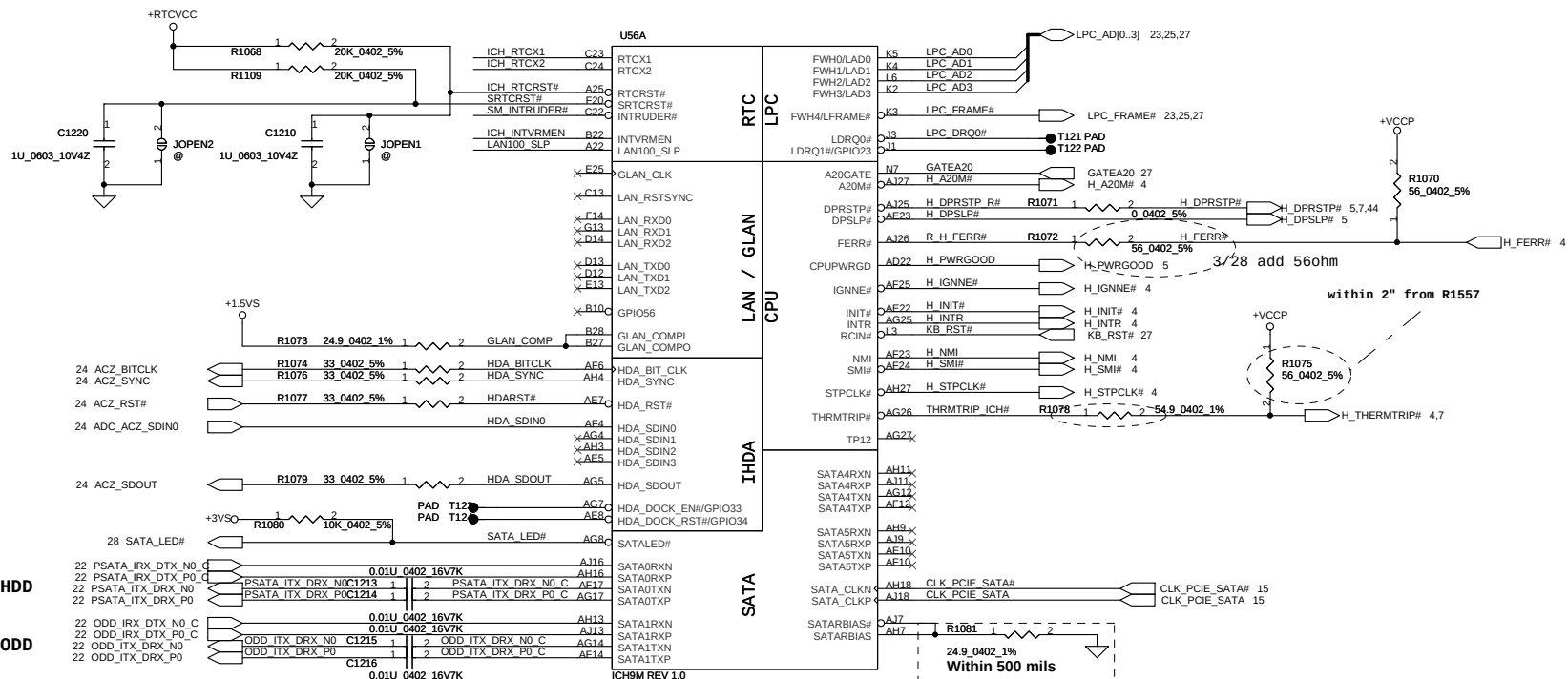
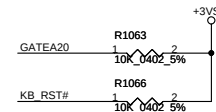
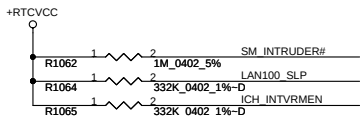


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *



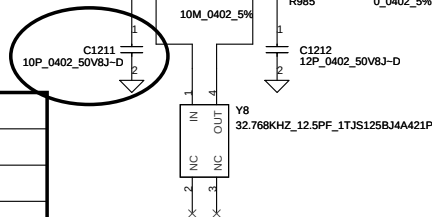
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





XOR CHAIN ENTRANCE STRAP:RSVD

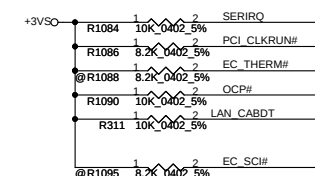
XOR Chain Entrance Strap		
ICH_RSVD_TP3	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



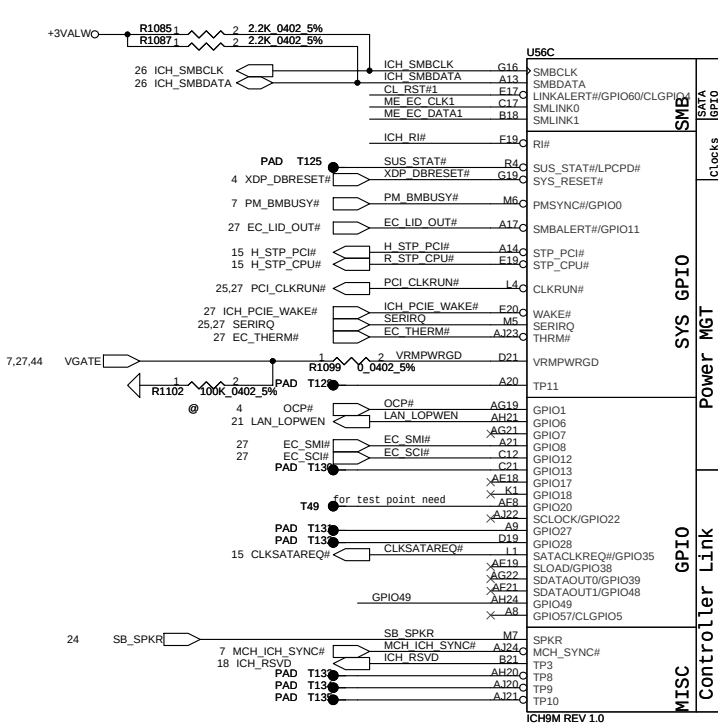
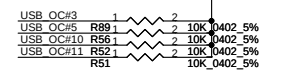
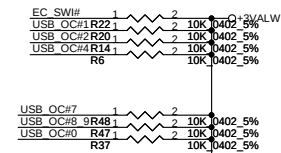
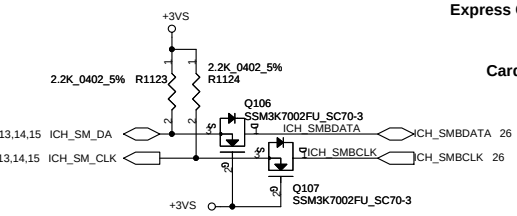
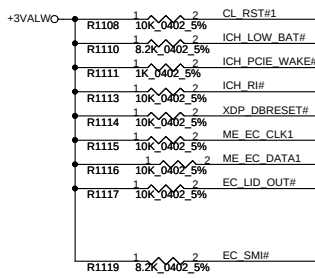
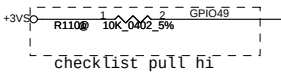
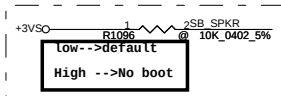
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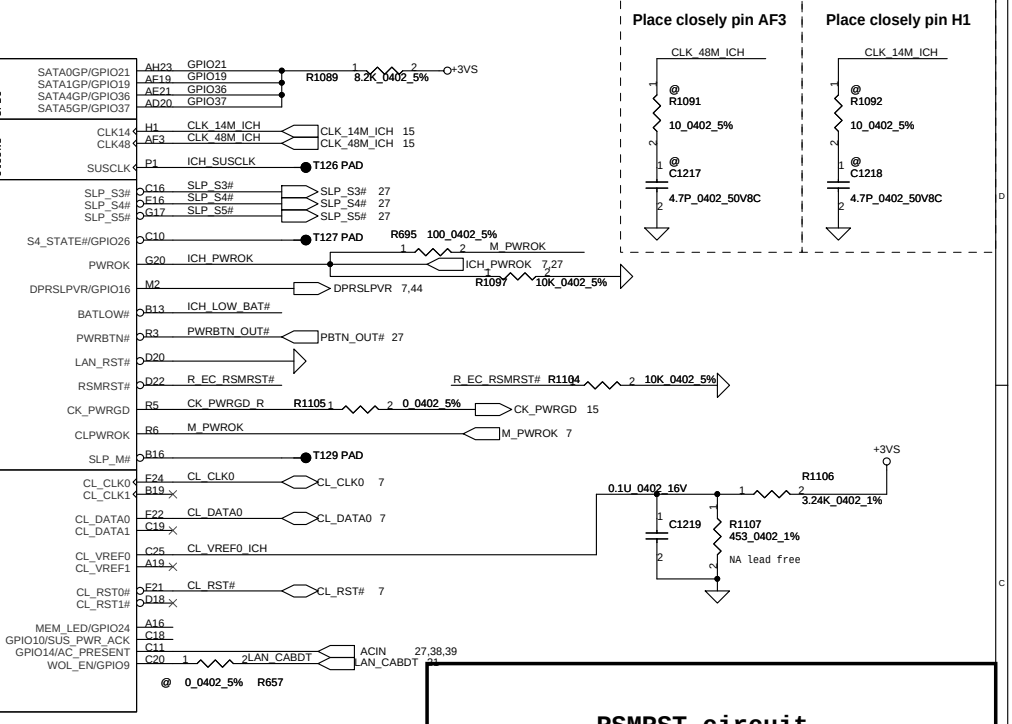
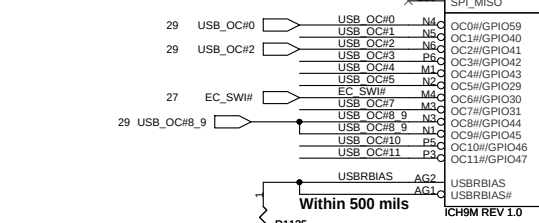
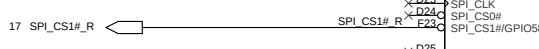
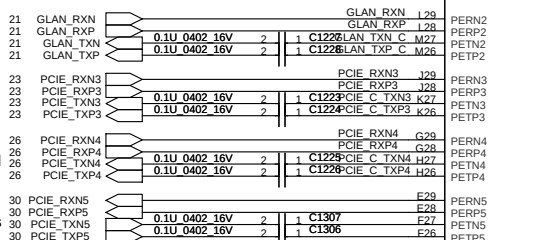
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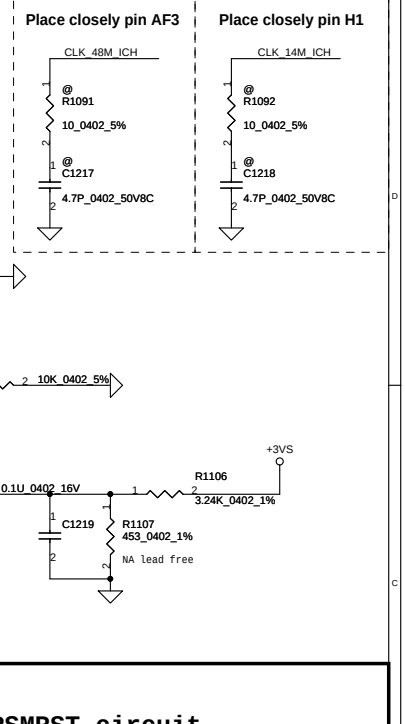
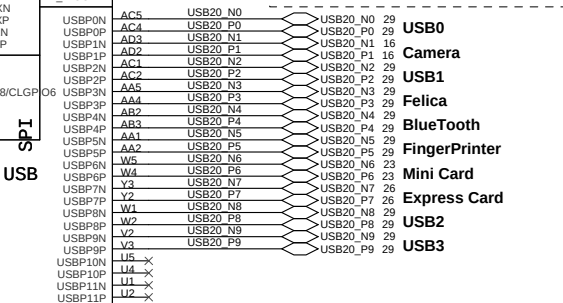
ICH8 don't have



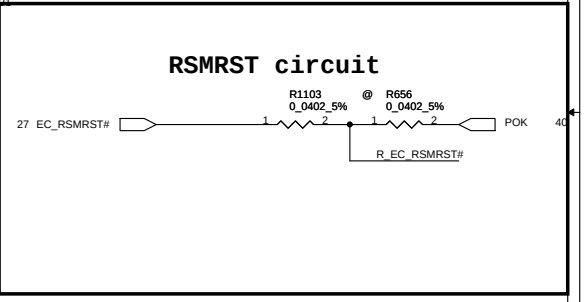
GLAN
WLAN
Express Card
CardBus



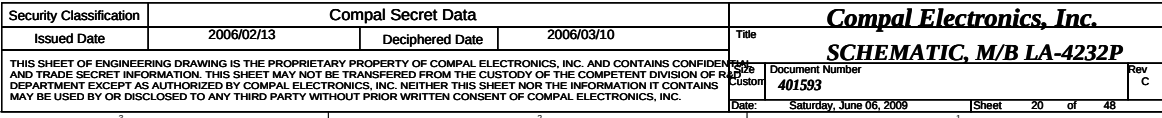
Direct Media Interface
PCI-Express
SPI

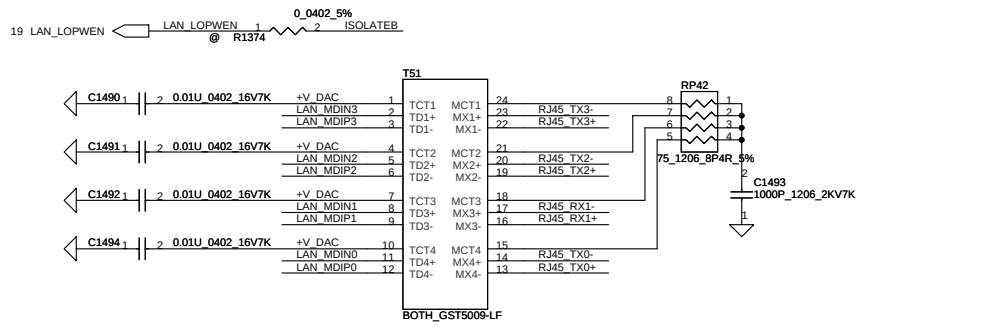
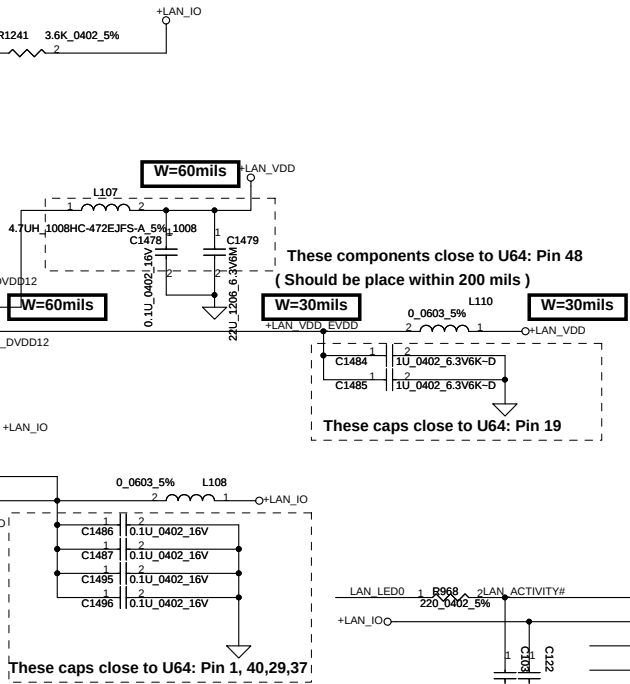
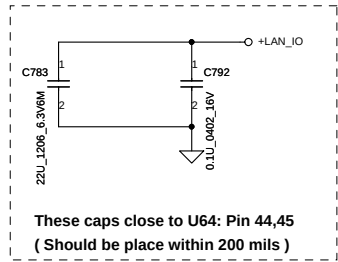
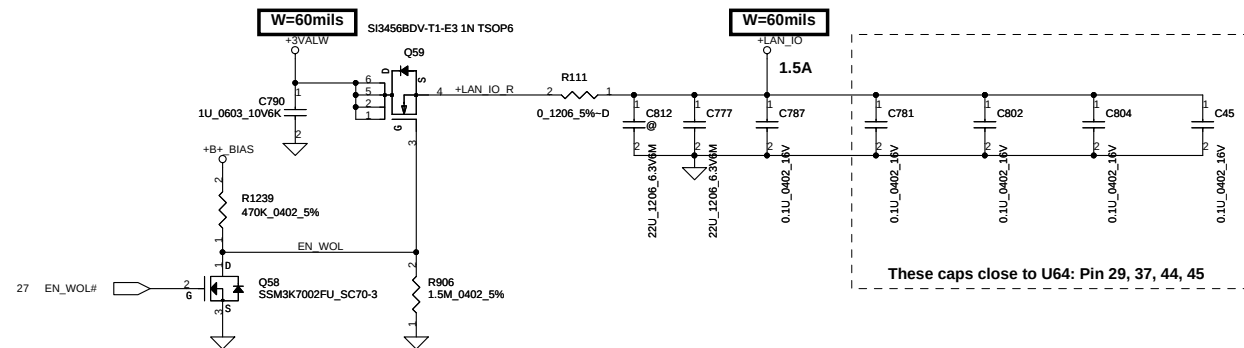


RSMRST circuit



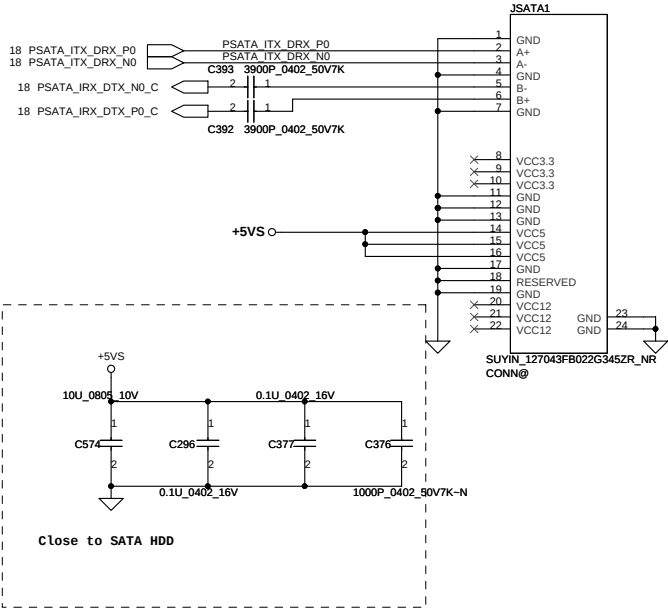
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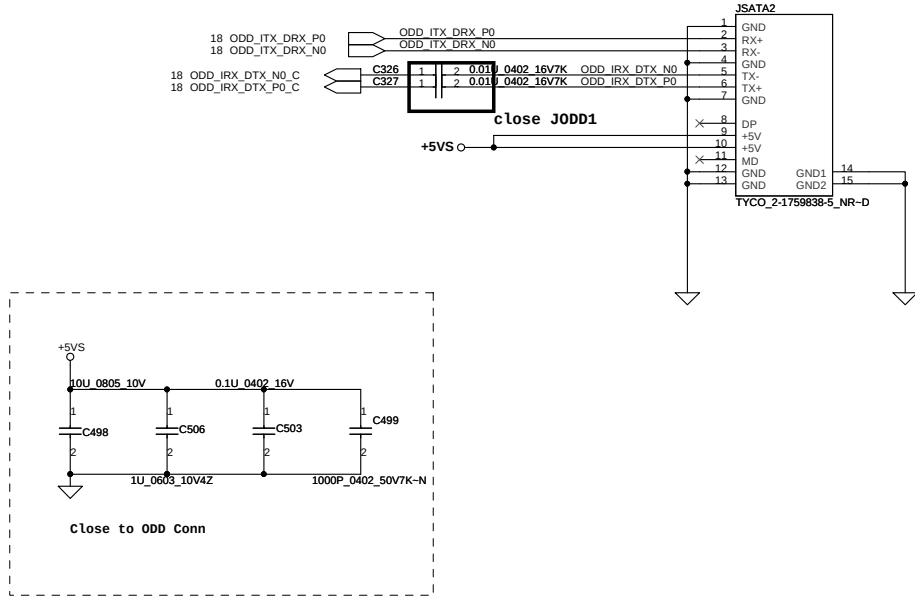


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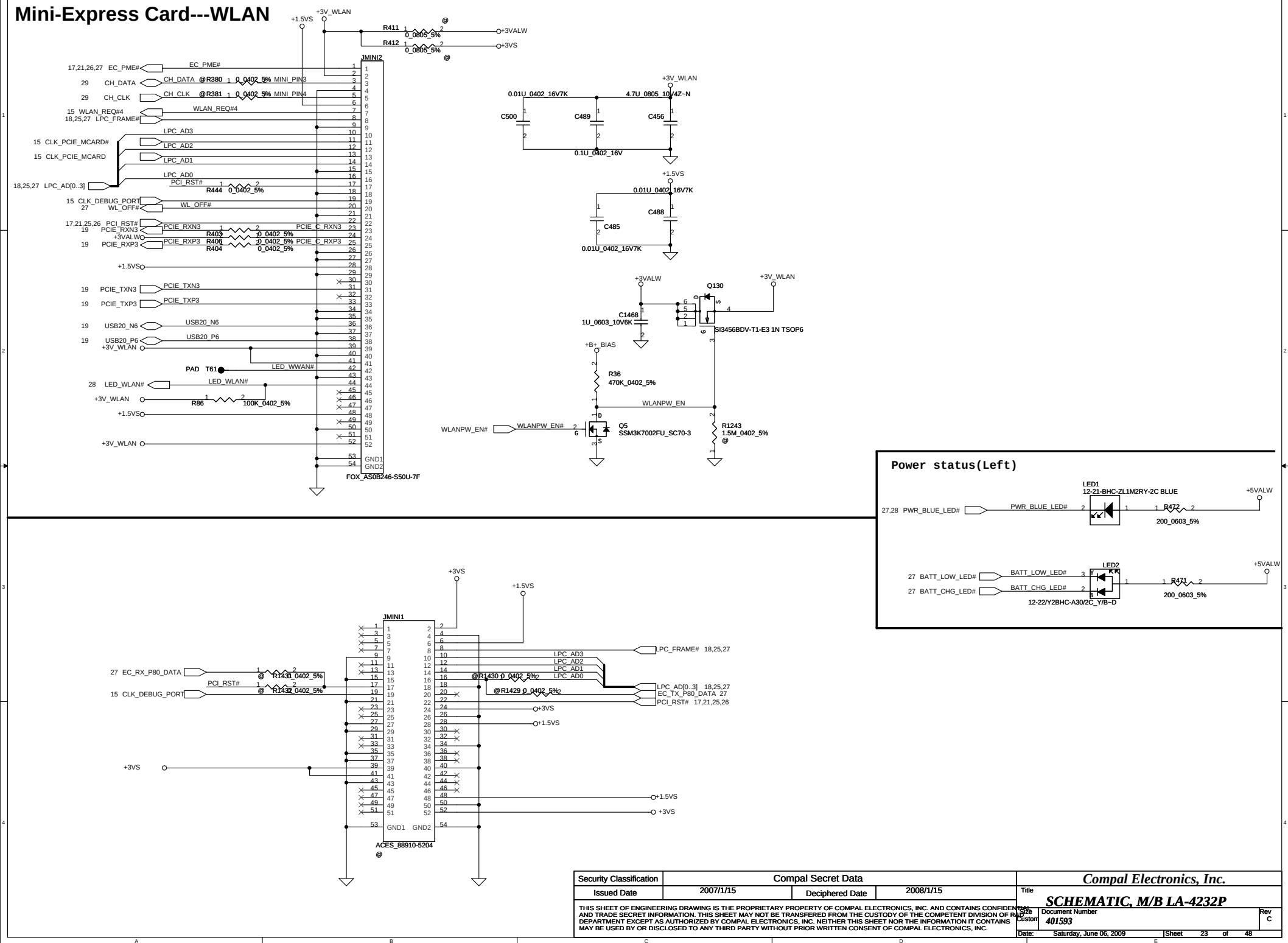
SATA HDD CONN



SATA ODD CONN



Mini-Express Card---WLAN

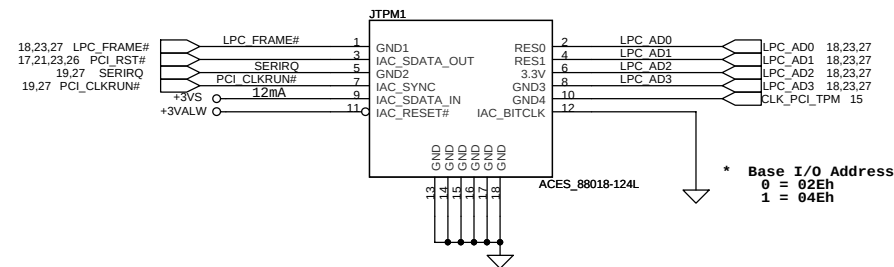


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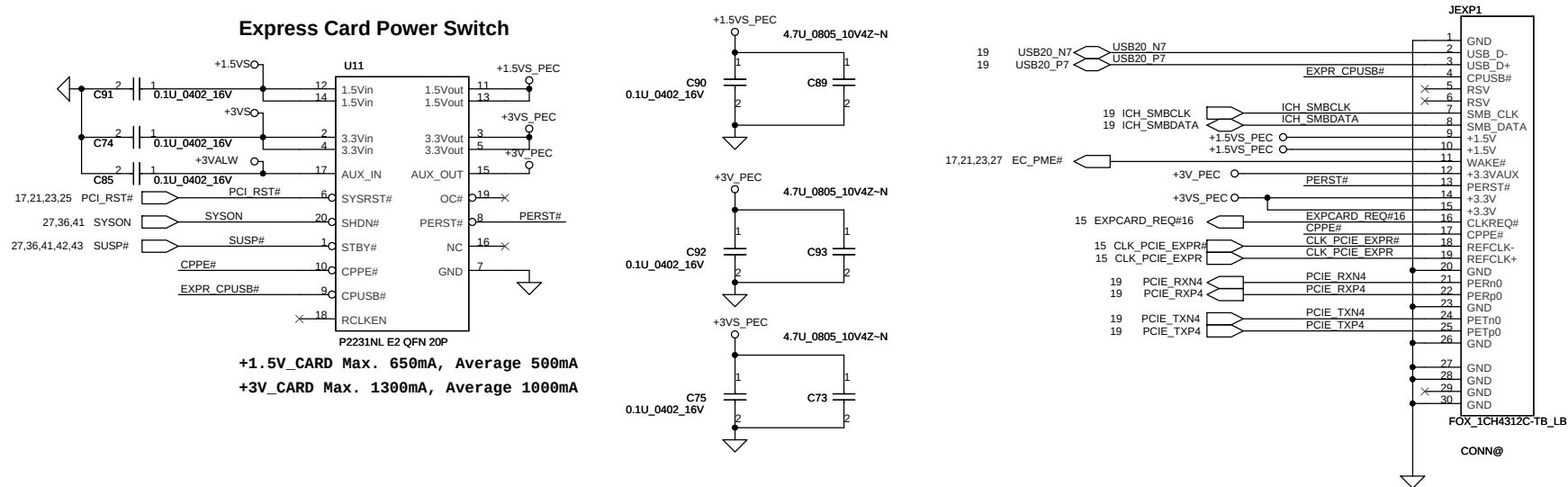
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TPM 1.2



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Express card



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Power Button

The schematic diagram illustrates the Power Button circuit. It features a CHN202UPT SC-70 switch (D15) and a MOSFET (Q26, SSM3K7002FU_SC70-3). The PWR_ON-OFF_BTN# input (pin 1) is connected to the switch. The switch's other terminal (pin 2) is connected to a +3VALW supply through a 100K_0402_5% resistor (R297). The switch's third terminal (pin 3) is connected to a 51ON# input (pin 38) and also to the base of the MOSFET. The MOSFET's source (pin 6) is connected to ground, and its drain (pin 2) is connected to a +3VALW supply through a 4.7K_0402_5% resistor (R296). The MOSFET's drain is also connected to the anode of a diode (D13, RLZ20A_LL34). The diode's cathode (pin 1) is connected to a 51ON# input (pin 38) through a 1000P_0402_50V7K-N capacitor (C313). The diode's anode (pin 2) is connected to the MOSFET's drain. The MOSFET's gate (pin 1) is connected to the +3VALW supply through a 4.7K_0402_5% resistor (R291). The MOSFET's gate is also connected to the EC_ON input (pin 2) through a 0_0402_5% resistor (R291).

The diagram shows an adjustable output circuit. A +5VS input is connected to the VIN pin (pin 1) of the RT9198-33PBR SOT-23 5P regulator (U54). A 10k_0603_1% resistor (R901) is connected between the SHDN# pin (pin 3) and the BP pin (pin 4). The BP pin (pin 4) is also connected to the +3VS_FUN output. The GND pin (pin 2) and the VOUT pin (pin 5) are connected to a common ground point. A 1u0400.63uVZ capacitor (C280) is connected between the VIN pin (pin 1) and ground. The output of the regulator is labeled +3VS_FUN.

INT _KBD CONN.

27 KSI[0..7] KSI[0..7]

27 KSO[0..15] KSO[0..15]

JKB1

KSI0	1
KSI1	2
KSI2	3
KSI3	4
KSI4	5
KSI5	6
KSI6	7
KSI7	8
KSO0	9
KSO1	10
KSO2	11
KSO3	12
KSO4	13
KSO5	14
KSO6	15
KSO7	16
KSO8	17
KSO9	18
KSO10	19
KSO11	20
KSO12	21
KSO13	22
KSO14	23
KSO15	24
×	25
×	26

27
28

GND1
GND2

ACES_88514-2601

KSO8 @C449	100P 0402 25V8K	KS17 @C235	100P 0402 25V8K
KS13 @C239	100P 0402 25V8K	KS16 @C236	100P 0402 25V8K
KSO9 @C249	100P 0402 25V8K	KS15 @C237	100P 0402 25V8K
KS12 @C240	100P 0402 25V8K	KSO0 @C441	100P 0402 25V8K
KS11 @C241	100P 0402 25V8K	KSO1 @C442	100P 0402 25V8K
KSO10 @C248	100P 0402 25V8K	KSO2 @C443	100P 0402 25V8K
KSO11 @C247	100P 0402 25V8K	KS14 @C238	100P 0402 25V8K
KS10 @C242	100P 0402 25V8K	KSO3 @C444	100P 0402 25V8K
KSO12 @C246	100P 0402 25V8K	KSO4 @C445	100P 0402 25V8K
KSO13 @C245	100P 0402 25V8K	KSO5 @C446	100P 0402 25V8K
KSO14 @C244	100P 0402 25V8K	KSO6 @C447	100P 0402 25V8K
KSO15 @C243	100P 0402 25V8K	KSO7 @C448	100P 0402 25V8K

For EMI

For ENE

FB_SDATA

FB_SCLK

R611

SUPPRE_KC FBMA-11-100505-801T 0402

R612

SUPPRE_KC FBMA-11-100505-801T 0402

R800

0.0603, 5%

R622

0.0402, 5%

R606

0.0402, 5%

C324

4.7uF

3V3

3V3_FUN

18 SATA_LED#

23 LED_WLAN#

29 BLUETOOTH_LED#

36.37 PWR_BLUE_LED#

37 TOUCHKEY_TINT

38 NUMLED#

39 CAPSLED#

40 SCRLED#

41 BTOP_BTN#

42 PWR_ON-OFF_BTN#

D58

PJ50T24C_SOT23-3

JFN1

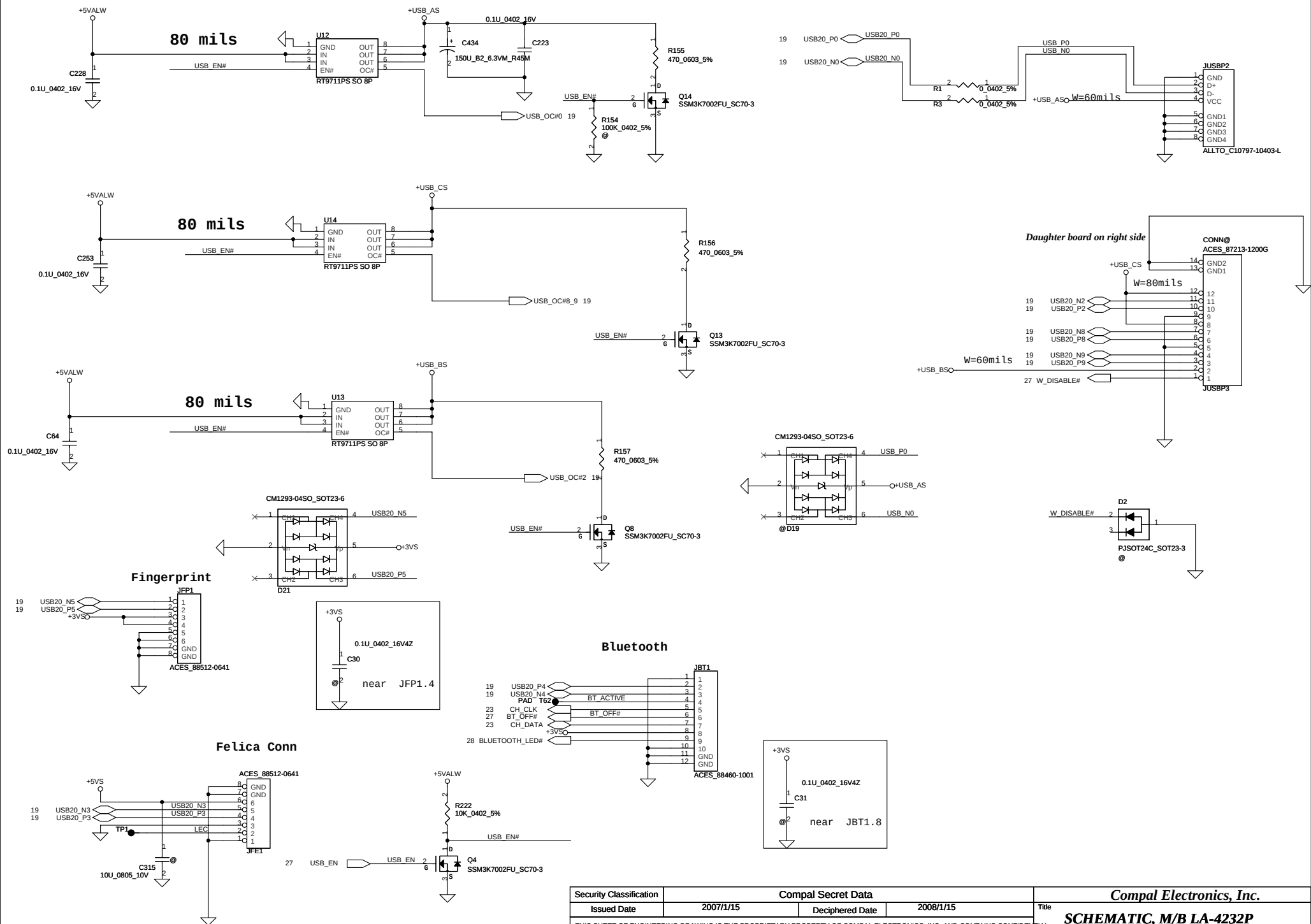
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near 1EN1.7

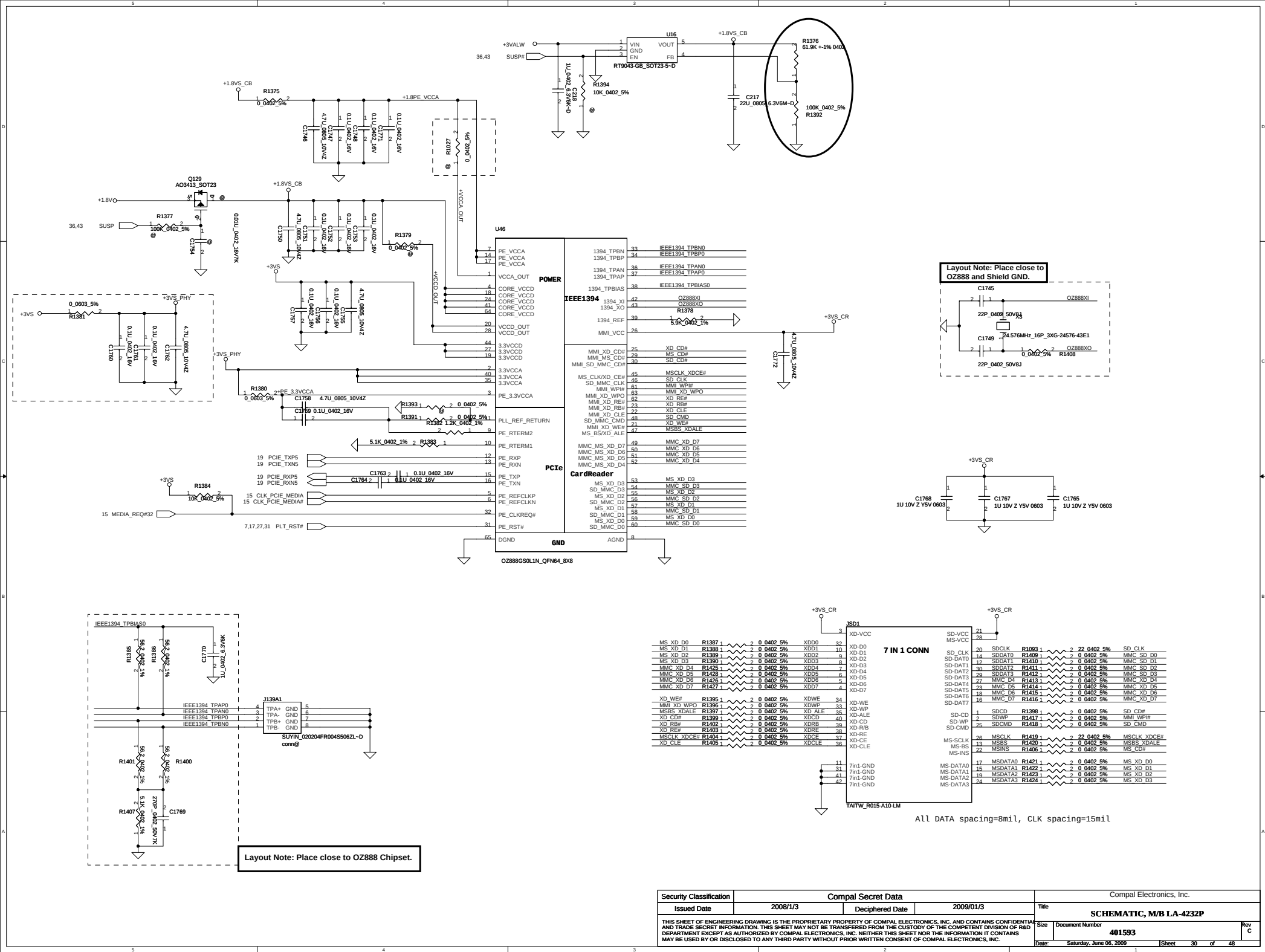
TP/B TO M/B

The schematic shows the connection between the TP/B and M/B connectors. A +5VS supply is connected to a C300 capacitor (0.01uF, 0402, 16V7K) and the TP_CLK/TP_DATA bus. The bus is connected to a TP/B connector and an M/B connector. The M/B connector is connected to an ACES 88514-0041 component. The bus also passes through two 100pF capacitors (C309, C310) and a diode (D24, SM05T1G_SOT23-3-D) to ground.

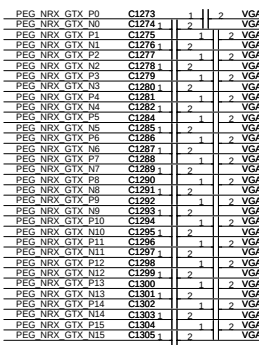
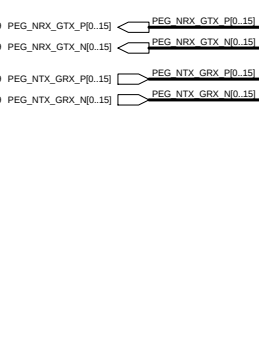
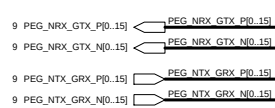
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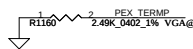
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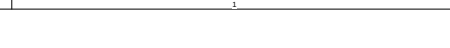
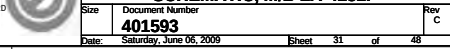
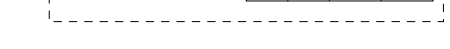
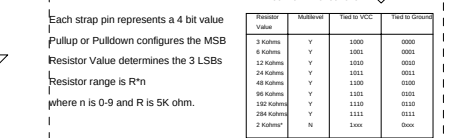
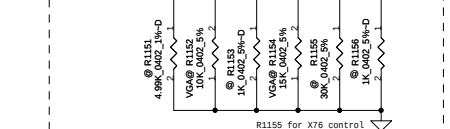
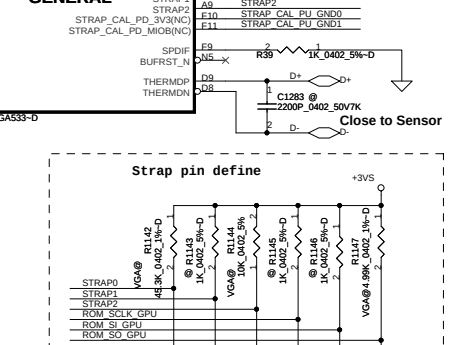
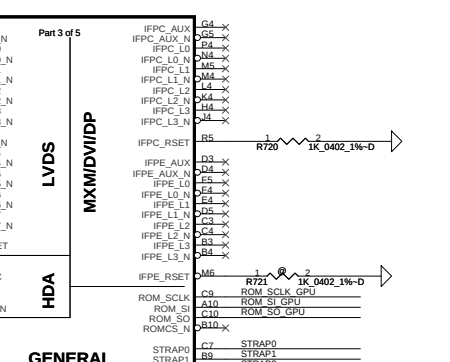
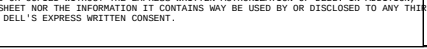
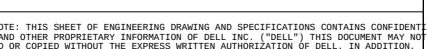
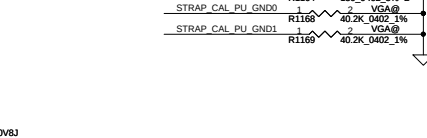
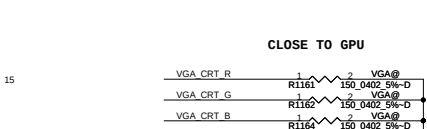
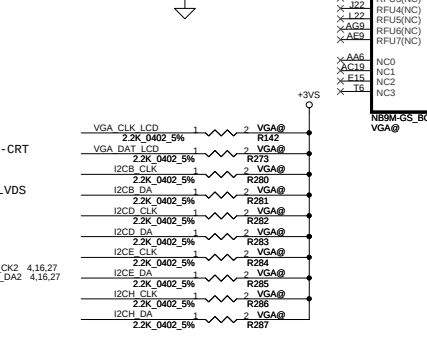
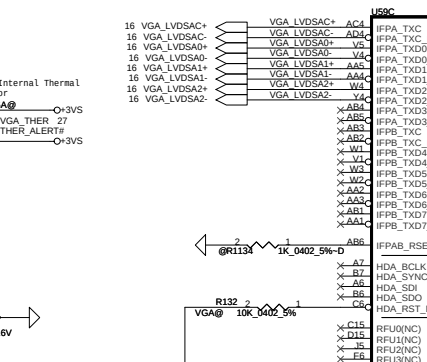
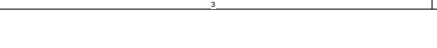
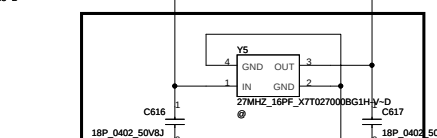
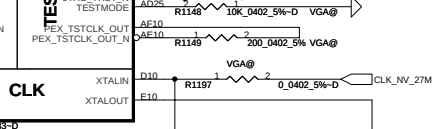
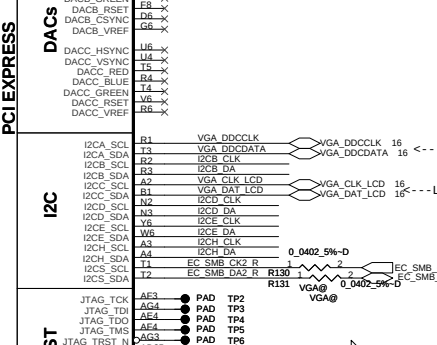
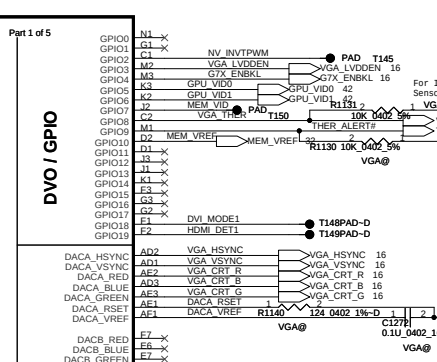
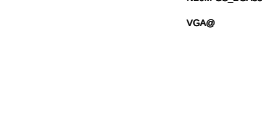
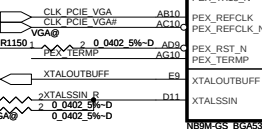
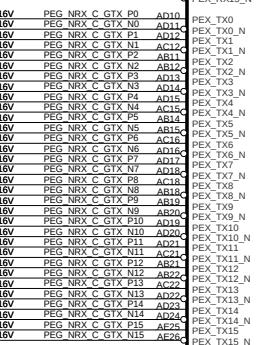
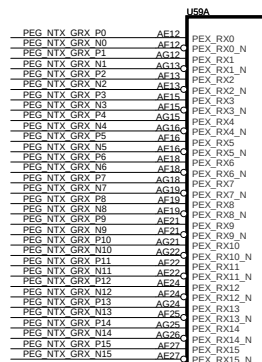
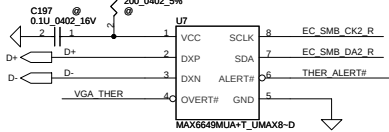
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Check reset timing



External Thermal sensor



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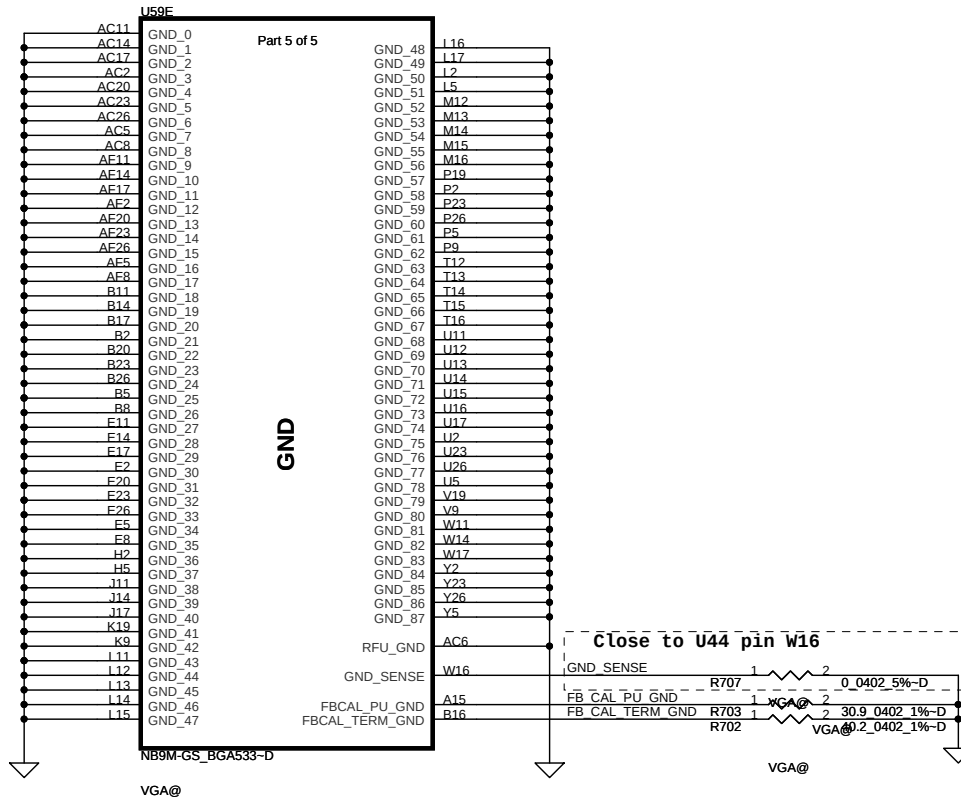
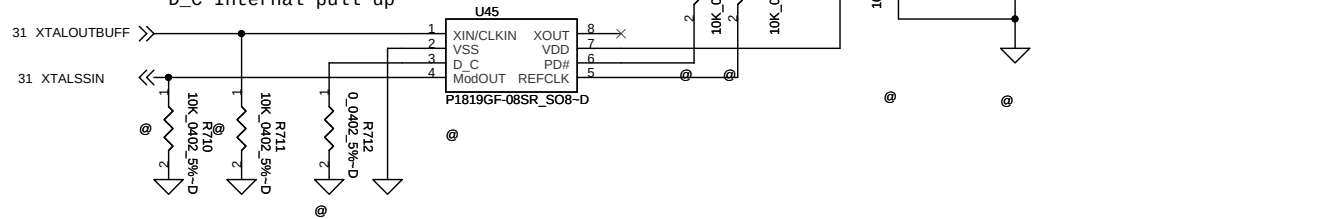
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Resistor Value	Multiplier	Tied to VCC	Tied to GND
3 KOhms	Y	1000	0000
4 KOhms	Y	1001	0001
12 KOhms	Y	1010	0010
24 KOhms	Y	1011	0011
48 KOhms	Y	1100	0100
96 KOhms	Y	1101	0101
192 KOhms	Y	1110	0110
384 KOhms	Y	1111	0111
2 KOhms*	N	1000	0000

	D_C
-1.75% (DOWN)	0
±0.875% (CENTER)	1

D_C Internal pull up



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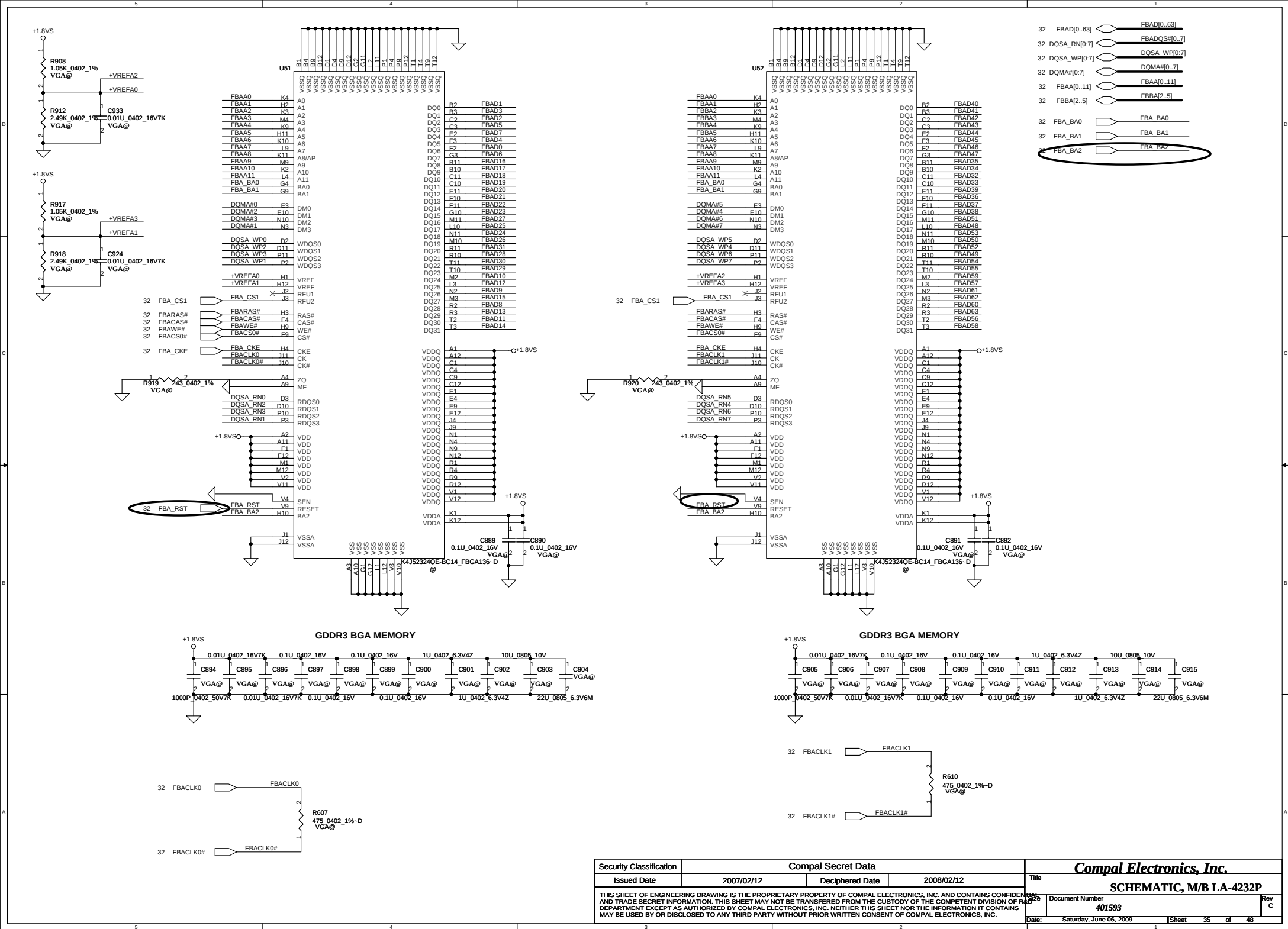
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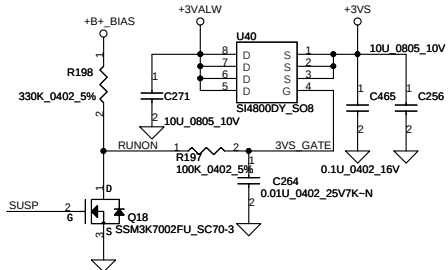
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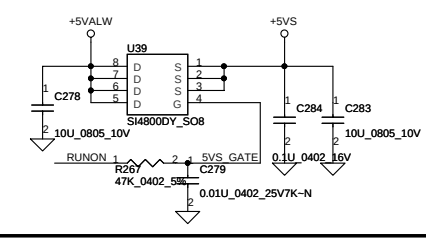
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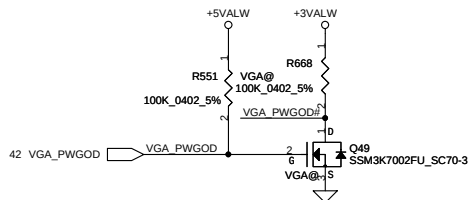
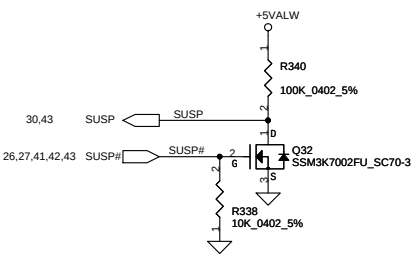
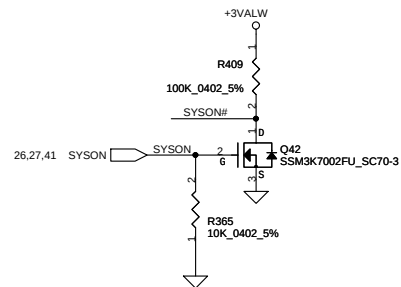
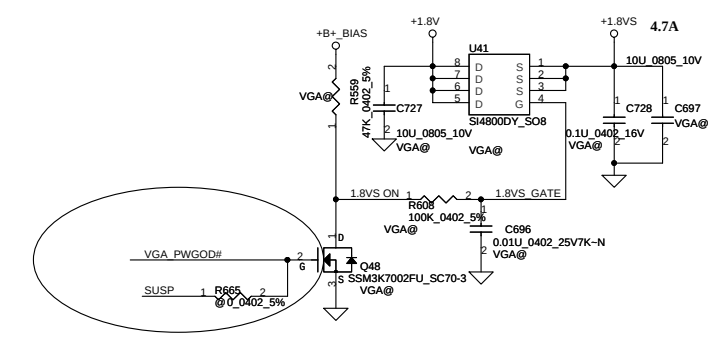
+3VALW to +3VS Transfer



+5VALW to +5VS Transfer

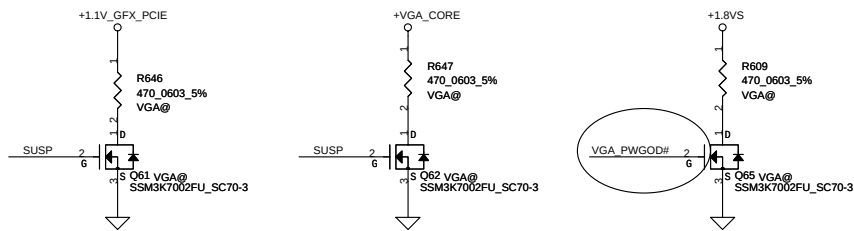


+1.8V to +1.8VS Transfer

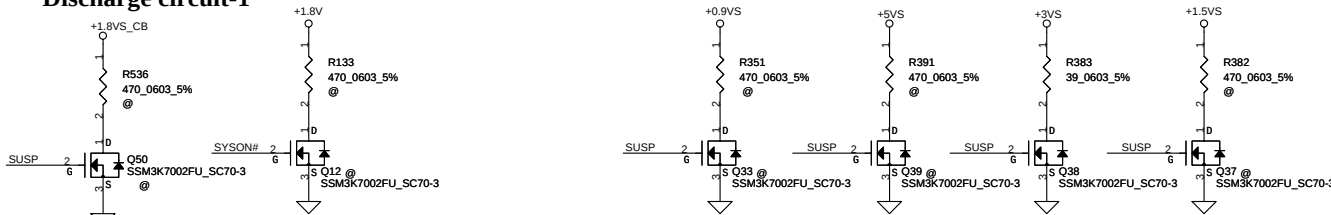


SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

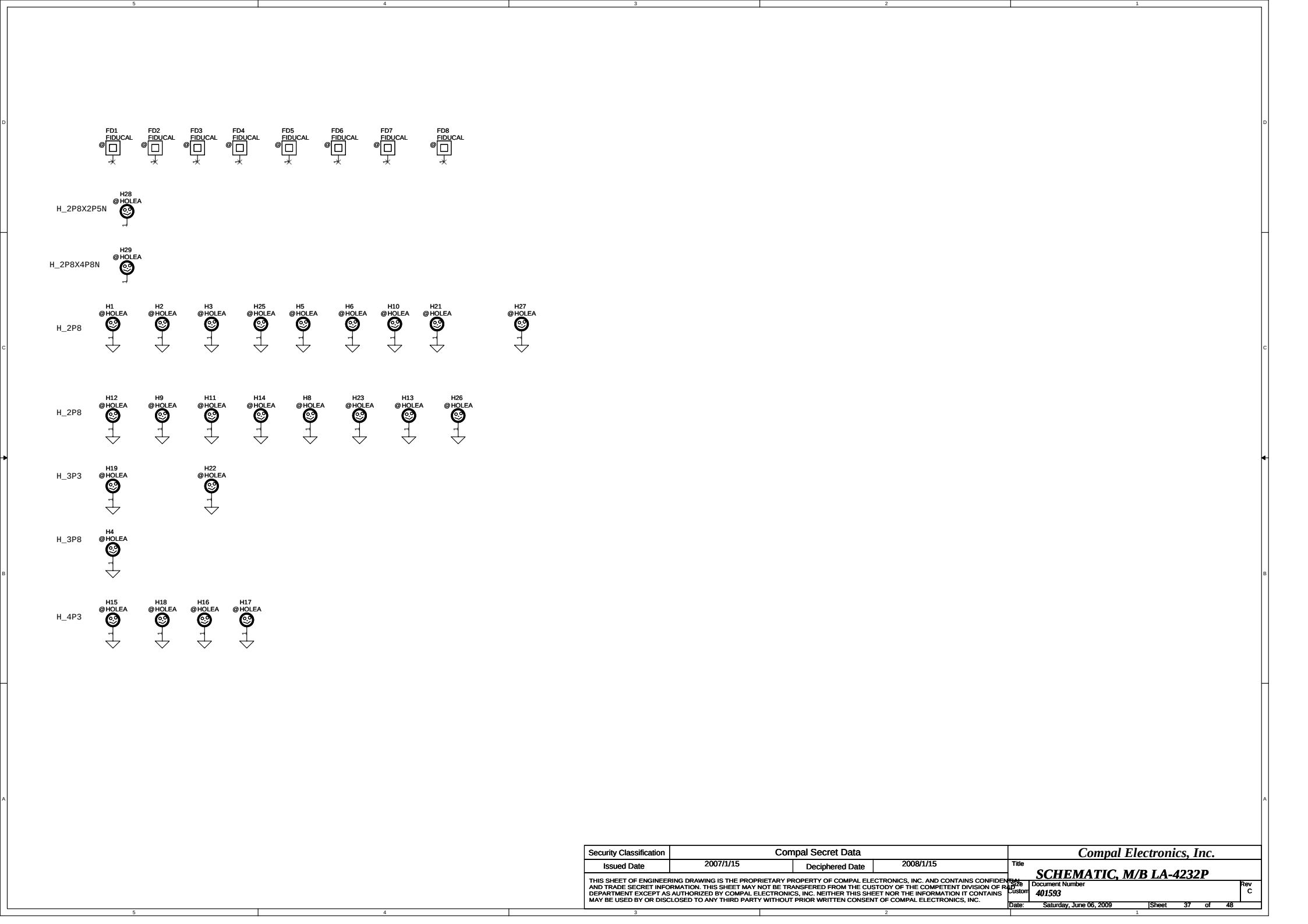
VGA Discharge circuit



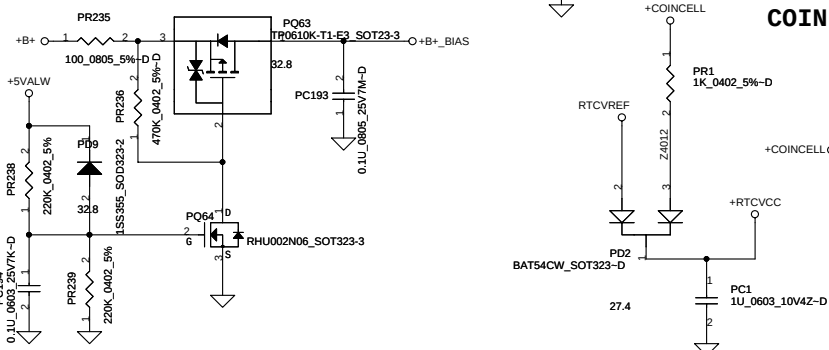
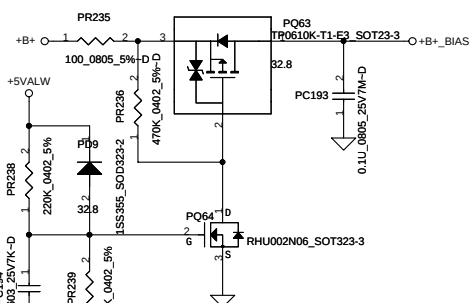
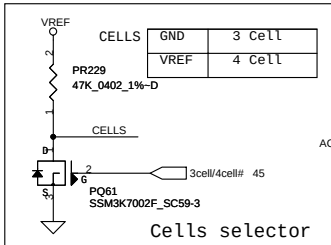
Discharge circuit-1



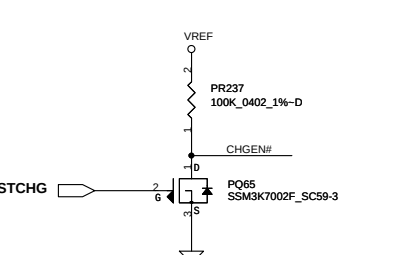
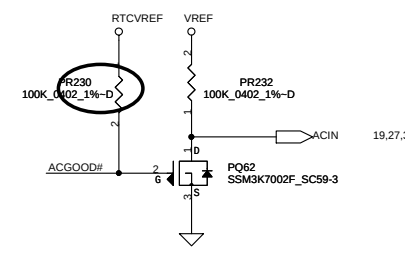
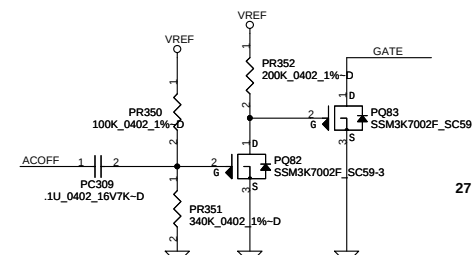
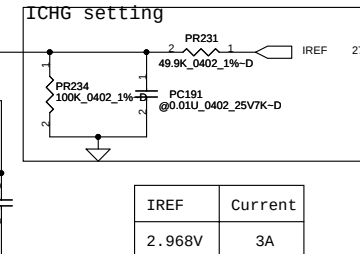
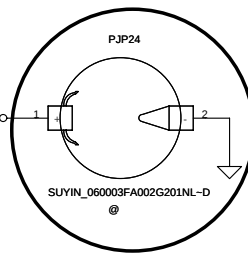
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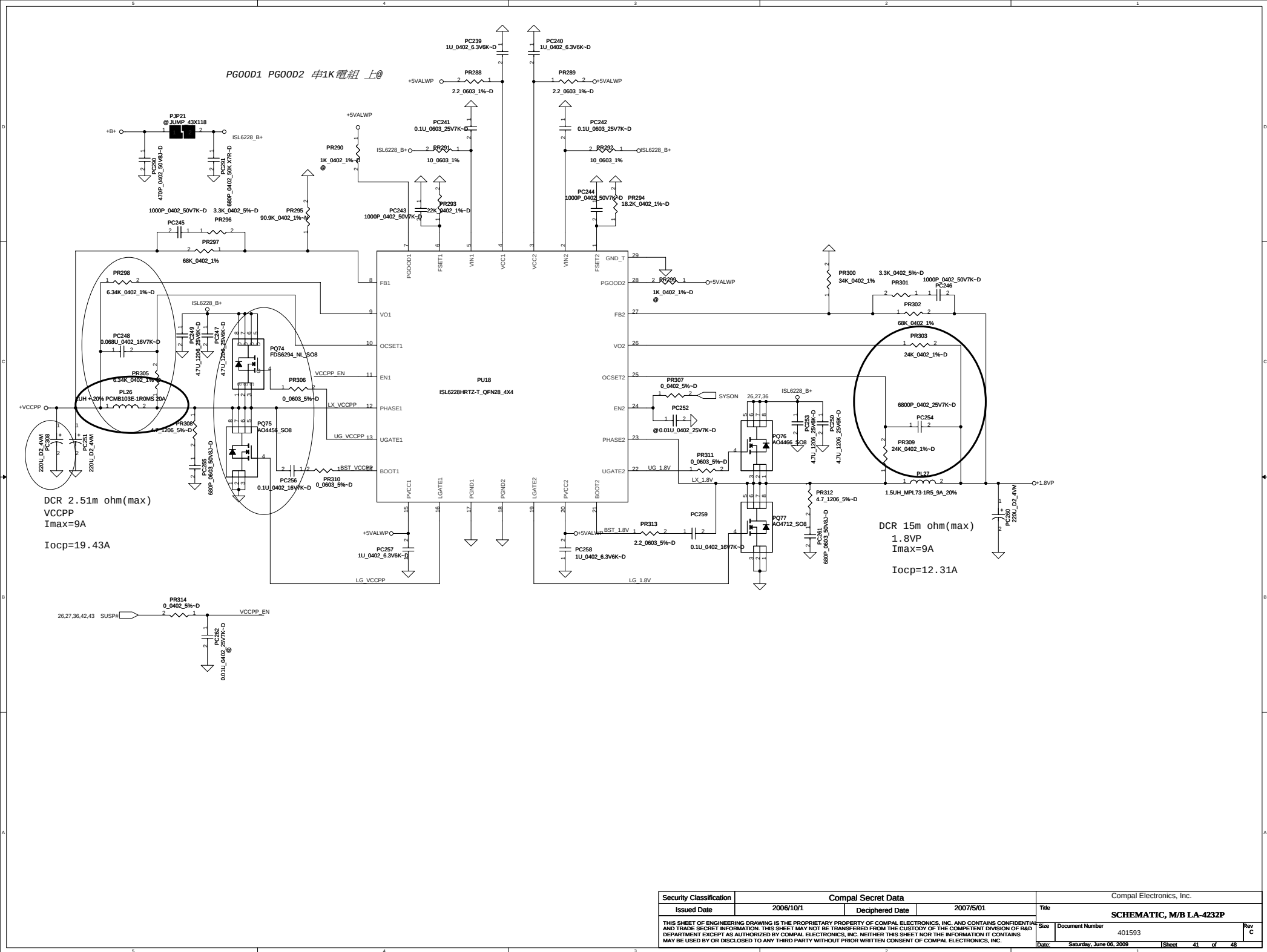


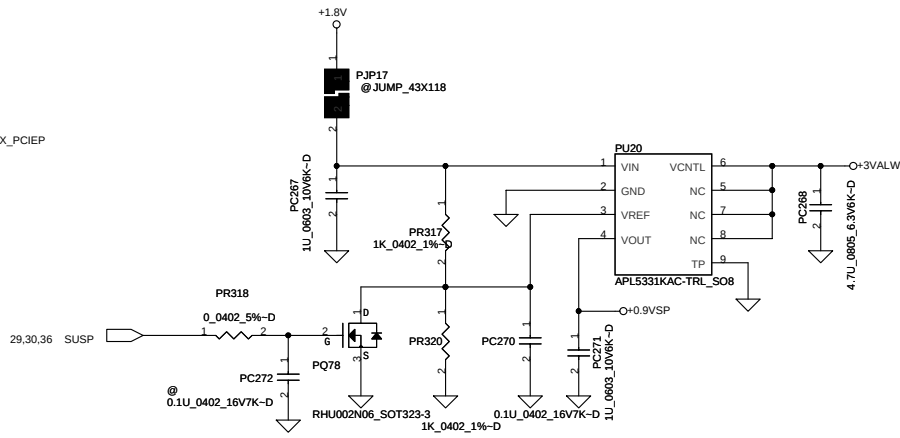
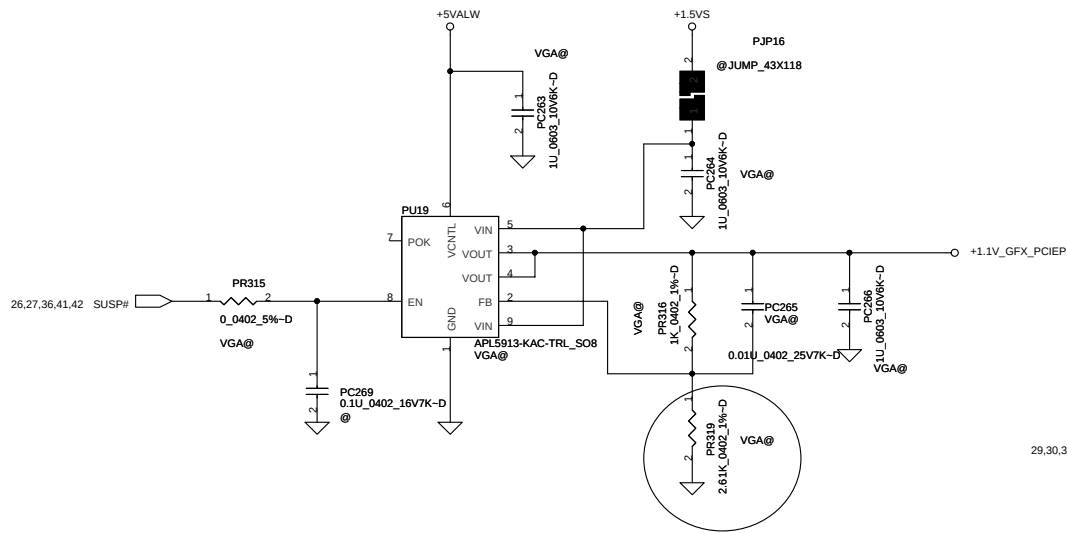
90W adapter
 $I_{charge} = (V_{rsrvt} / V_{vdac}) * (0.1 / PR222) = 3.3A$
 $I_{adapter} = (V_{acset} / V_{vdac}) * (0.1 / PR217) = 3.1A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz

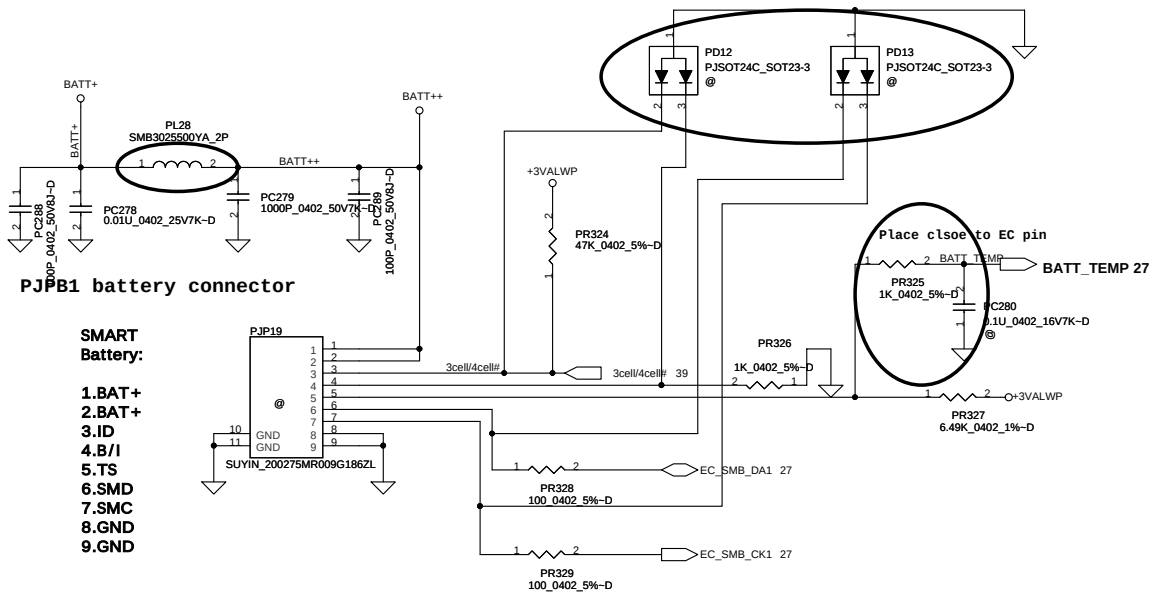


COIN RTC Battery



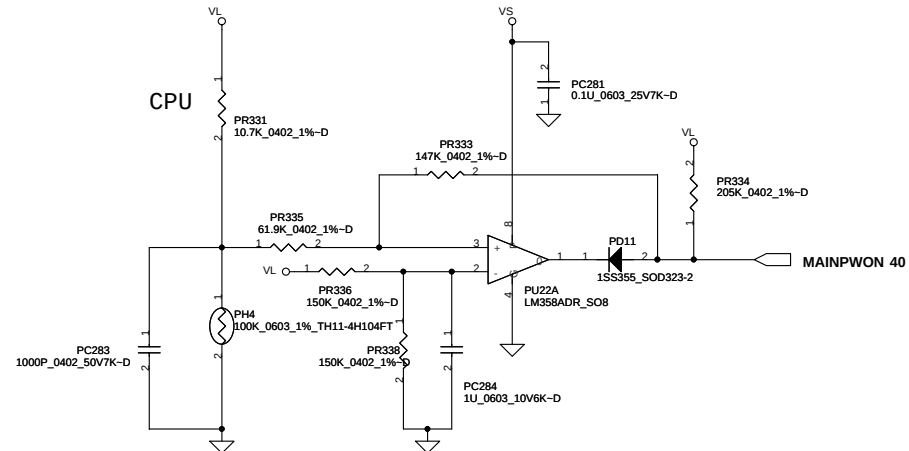
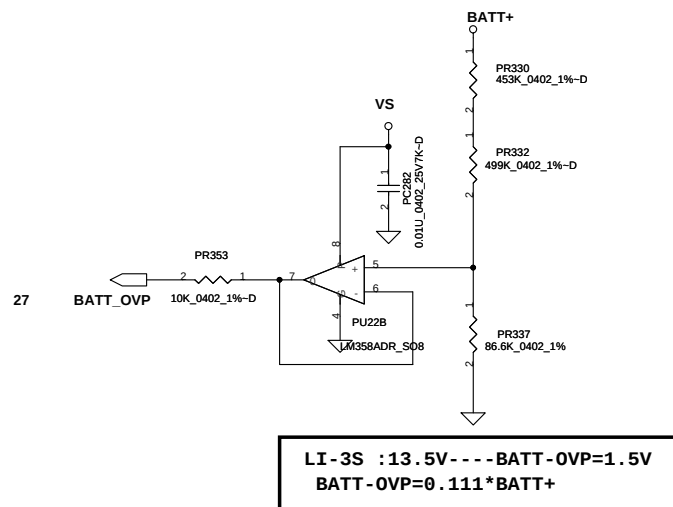






CPU

PH1 under CPU bottom side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 50 +-3 degree C



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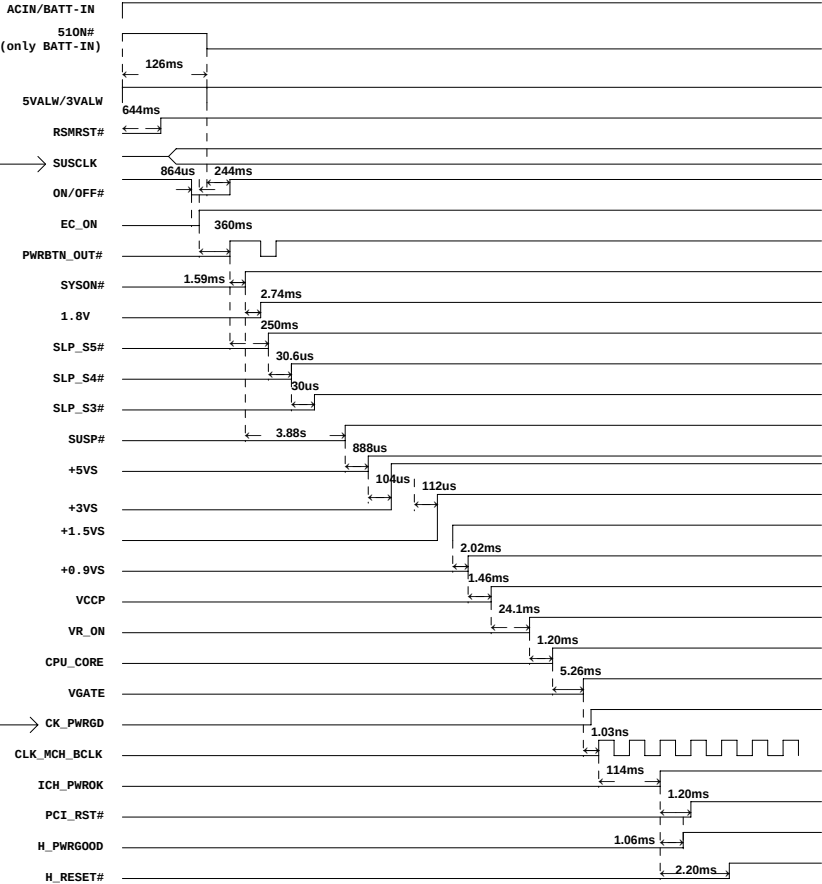
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	board rev update to 0.2	R231 change to 15K & R232 pop	0.2
2	40	P40-0Z129_Card Reader/1394	07/10/30	compal	CardBus vendor change	CardBus R5C833 change to 0Z129	0.2
3	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Change pull up resistance	Change EC pin17,18 pull up to 4.7Kohm	0.2
4	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Need pull up	NET MIC_DIAG pull up R to 10Kohm 3VS	0.2
5	13,14	DDR2 SODIMM-I,II Socket	07/10/30	compal	Change Capacitance	Change C84,C189 to SGA00002680 330U	0.2
6	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	EC update rev	EC change to 926C	0.2
7	28	P28-Express card	07/10/30	compal	Express card can't detect	POWER IC(U11) ADD PIN10 CPUSB# PIN9 EXPR_CPUSB#S	0.2
8	32	P32-USB/ BlueTooth/ FP/ Felica	07/10/30	compal	Bluetooth can't detect	BLUETOOTH CONN USB+- change	0.2
9	42	P42-Screws	07/10/30	compal	FIDUCAL no enough	ADD FIDUCAL*4	0.2
10	41	P41-DC/DC Interface	07/10/30	compal	Need pull down	SYS0N pull down 10K ohm	0.2
11	41	P41-DC/DC Interface	07/11/12	compal	USB can't detect	SUSP change to 5VALW(Q32)	0.2
12	06	P06-Merom(3/3)-GND/Bypass	07/11/12	compal	Change CPU High Freqeunce Decoupling Capacitance	C195 change to C1150-C1181	0.2
13	41	P41-DC/DC Interface	07/11/13	compal	+1.8VS Discharge error	+1.8VS Discharge circuit Q65 net change to VGA_PWG0D#	0.2
14	41	P41-DC/DC Interface	07/11/16	compal	Delete	Remove SIM card connector	0.2
15	42	P42-Screws	07/11/16	compal	Change Holea size	Change Holea size 2.5 to 2.8, change 3.5 to 3.8	0.2
16	31	P31-PWR_OK/ BTN/ KB / TouchPad	07/11/21	compal	Change Touch PAD/B connector	Touch PAD/B connector change net	0.2
17	15	P15-CRT Conn.& LCD Conn.	07/11/21	compal	Add LCD control pin	Add LCD control pin LCD_CBL_DET# & LCD_TST & LCD_VCC_TEST_EN	0.2
18	20	P20-ICH9(4/4)_POWER&GND	08/04/22	compal	+5VS & +3VS have leakage	Change VCCCL3[1] [2] & VCCLAN3_3[1] [2] power source to +LAN_IO	
19	20	P09-Cantiga(3/6)-VGA/LVDS/TV	08/04/22	compal	Can't boot to OS	Add BOM Structure @	
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	1.8VP/+VCCPP	08/10/22	COMPAL	adjust +VCCP OCP set	Change PC248 from 0.033u to 0.068u	0.2
2	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	ripple voltage fail	Change PC227 from SF22001M300 to SGA20221150	0.2
3	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	convenient test	Add PR304	0.2
4	44	CPU_CORE	08/10/22	COMPAL	load line fail	Change PR187 from 2.21K to 3.24K	0.2
5	38	DCIN / Precharge	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
6	39	Charger	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
7	40	+3VALWP/+5VALWP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
8	41	1.8VP/+VCCPP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
9	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
10	43	+0.9VSP/+1.1V_GFX_PCIEP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
11	44	CPU_CORE	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
12	45	BATTERY CONN	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
13	40	+3VALWP/+5VALWP	08/10/24	COMPAL	boost choke current rating	change PL20 PL21 from SH000006380 to SH00000AY00	0.2
14	45	BATTERY CONN	08/10/30	COMPAL	delete diode for EMD request	del PD14 PD15	0.2
15	45	BATTERY CONN	08/10/30	COMPAL	change diode for EMD request	change PD12 PD13 from SC1A204U00L to SCA00000E00	0.2
16	39	Charger	08/10/31	COMPAL	design modify	add PR372 PR373	0.2
17	41	1.8VP/+VCCPP	08/11/03	COMPAL	dynamic fail	change PC233 from SGA20221150 to SGA00001U80	0.2
18	44	CPU_CORE	08/12/08	COMPAL	cost down	change PU11 from SA00001HU80 to SA000031W00 and interrelated components	0.3
19	38	DCIN / Precharge	08/12/08	COMPAL	common circuit design modify	change PR203 from 33 to 68 and add PR204 to 68	0.3
20	39	Charger	08/12/08	COMPAL	vendor FAE suggest	change PR272 PR339 from 1 to 3.3	0.3
21	38	DCIN / Precharge	08/12/08	COMPAL	design modify	change PL17 from SM010018880 to SM010008E10	0.3
22	45	BATTERY CONN	08/12/08	COMPAL	design modify	change PL28 from SM010018210 to SM010008E10	0.3
23	39	Charger	08/12/15	COMPAL	change component for EMD request	change PJP15 to PL19 SM010016410	0.3
24	39	Charger	08/12/15	COMPAL	add capacitor for EMD request	add PC274 0.1u	0.3
25	42	1.5VSP/+VGA_CORE	09/01/19	COMPAL	adjust VGA_CORE OCP set	change PQ72 from SB00000CG00 to SB562940080	0.4
26						change PQ73 from SB00000AJ00 to SB000003W00	0.4
27						change PL24 from SH000008700 to SH000005400	0.4
28						change PR276 PR282 from 24K to 19.6K	0.4
29						change PC230 from 0.022u to 6800p	0.4
30					consumption adjust	change PR269 from 3.3K to 2.2K	0.4
31	44	CPU_CORE	09/01/19	COMPAL	vendor FAE suggest	add PC141 330p	0.4
32	45	BATTERY CONN	09/02/18	COMPAL	delete diode for ESD request	del PD12 PD13	0.4

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KAL80 POWER UP SEQUENCE



Suspend Clock (32KHz)
ICH9 Internal clock

This signal is
asserted high when
both SLP_S5# and
VHWPWRGD are high