

COMPAL CONFIDENTIAL

MODEL NAME : *BDW00*
COMPAL P/N : *DA8DW00L100*
PCB NO : *LA-1452*
Revision : *0.2*
DATE :

Abacus/TangII Schematics Document
uFCBGA/uFCPGA Northwood

2002-08-22
REV: 0.2 (PT)

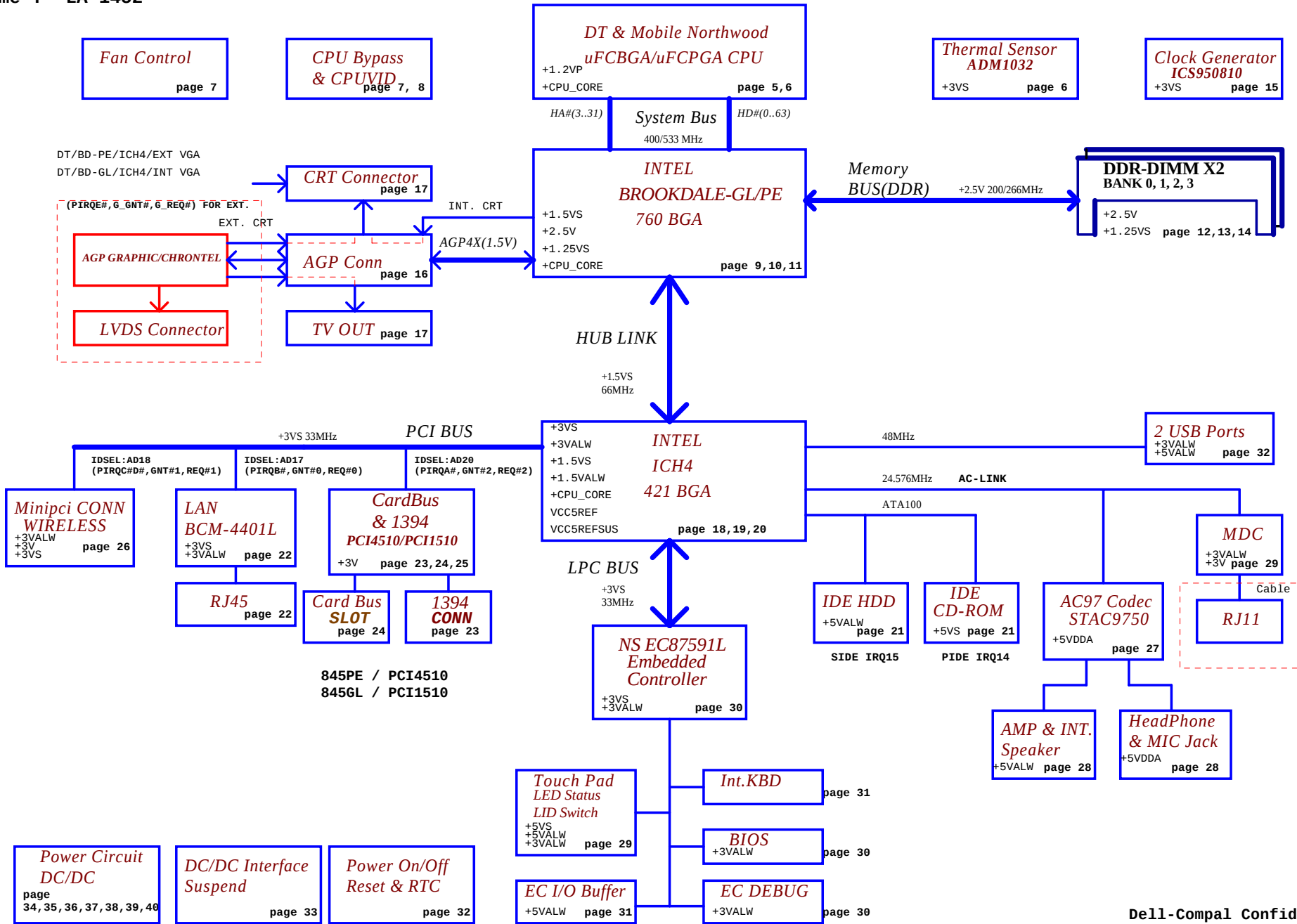
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Title		
Cover Sheet		
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	Abacus/TangII LA-1452	0.2
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Model Name : ABACUS/TangII

File Name : LA-1452



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Block Diagram			
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Revision List

	Schematics Rev	PCB Rev	CHIPS Rev
SST-Build	0.1	0.1	
PT-Build	0.2	0.2	845PE Rev B0 845GL Rev B1 ICH4 Rev B0
ST-Build			
QT-Build			

Ceramic Capacitor Spec Guide:

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NP0	C0G		BJ	CH	CJ	CK	SH	SJ

H	I	J	
UJ	UK	SL	

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	+-.05PF	+-.0.1PF	+-.0.25PF	+-.0.5PF	+-.1PF	+-.2%	+-.3%	+-.5%

K	M	N	P	Q	V	X	Z	
+-.10%	+-.20%	+-.30%	+100, -0%	+30, -10%	+20, -10%	+40, -20%	+80, -20%	

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) (U57)	THERMAL SENSOR (U25/U23)	SODIMM	CLK CHIP	MINI PCI
SMB_EC_CK1 SMB_EC_DA1	NS 87591	✓	✓	✓ (1010)	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	NS 87591	✗	✗	✗	✓	✓	✗	✗	✗
SMB_CLK SMB_DATA	ICH4	✗	✗	✗	✗	✗	✓	✓	✓

Power Managment table

Signal State	+3VALW +5VALW +12VALW	+3V +5V +2.5V	+3VS +5VS +1.5VS +1.2VP +CPU_CORE +1.25VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

NOTE1:

@XX : Depop component

1@XX : Pop for INT, Depop for EXT

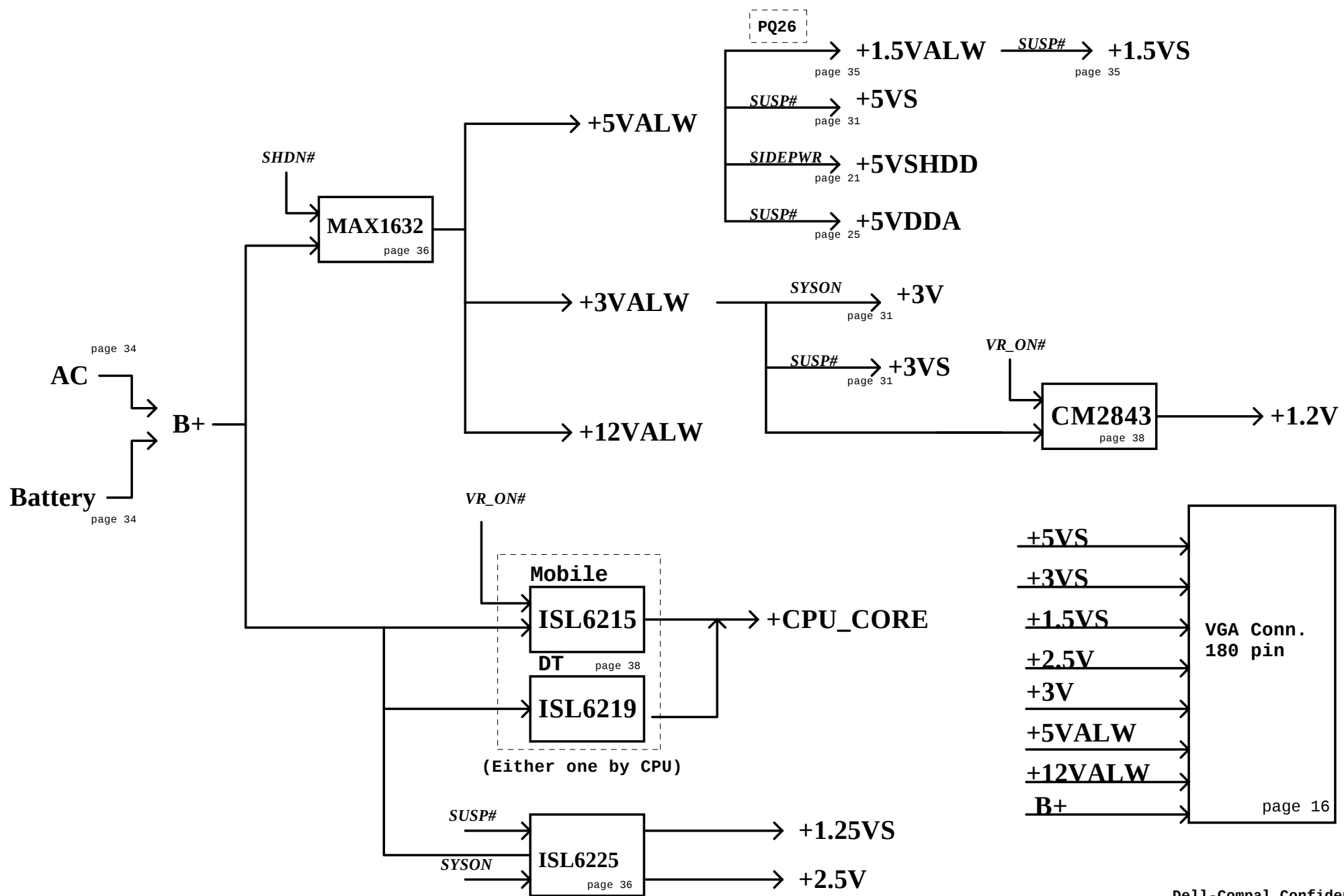
2@XX : Pop for EXT, Depop for INT

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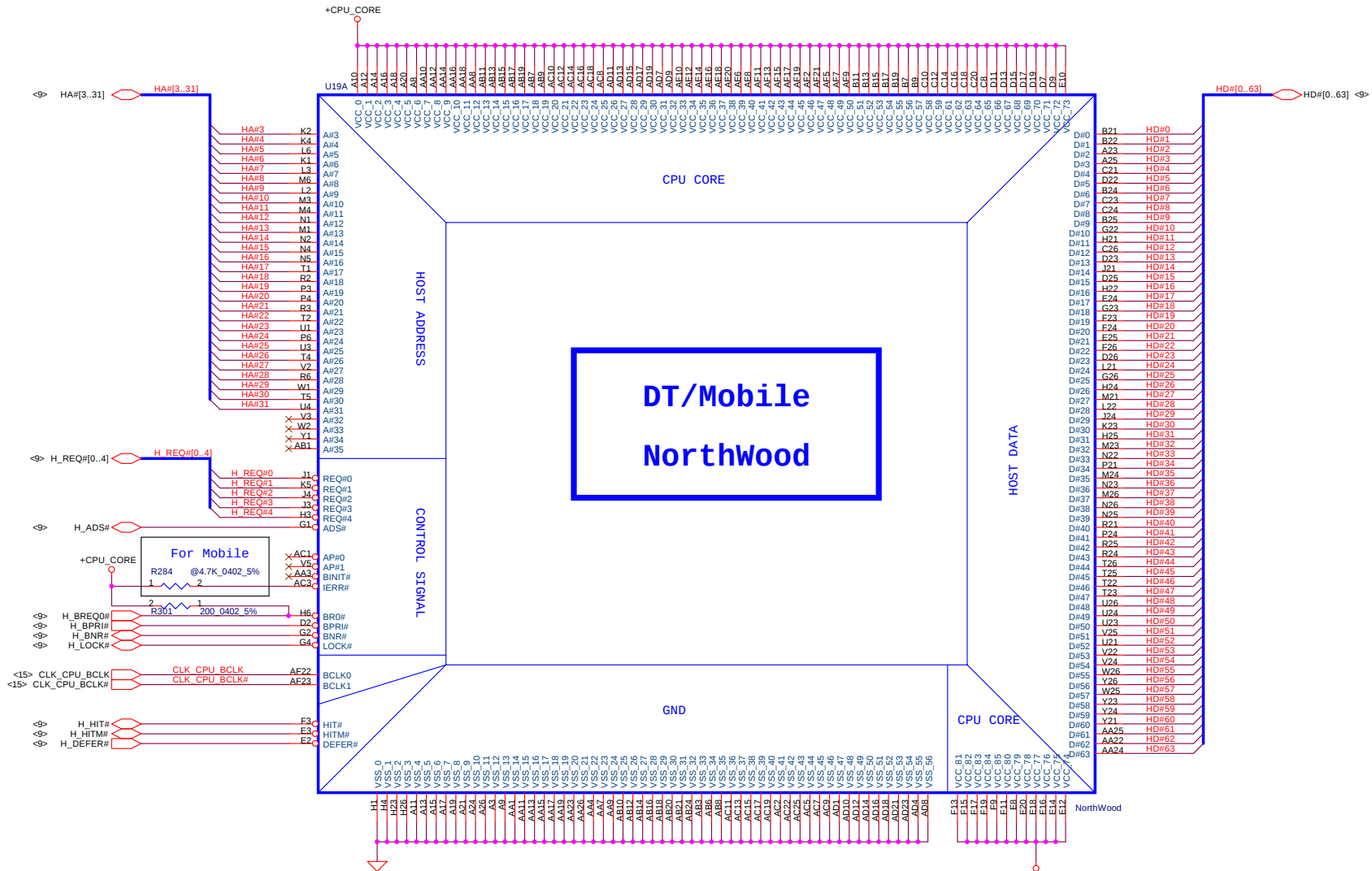
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Title			
POWER DIAGRAM			
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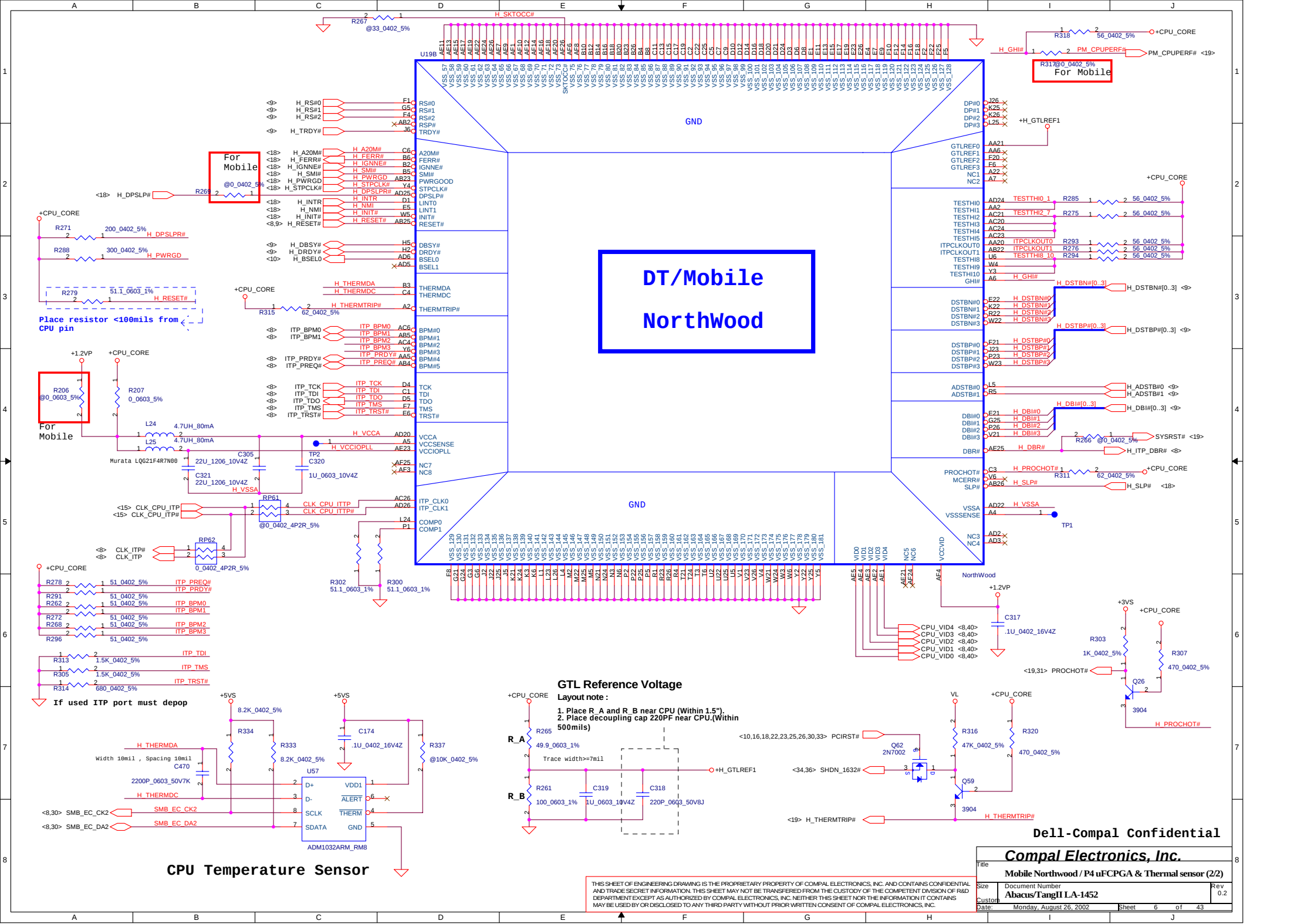


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Title			Northwood / P4 uFCPGA (1/2)
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Place close to CPU, Use 2-3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2-3 vias per PAD.

The diagram illustrates the CPU core power distribution network (PDN) for the i7-10700K. It shows two parallel paths for the +CPU_CORE and -CPU_CORE rails. Each rail consists of a series of five capacitors: C407, C391, C63, C65, and C294 for the positive rail, and C412, C376, C290, C282, and C406 for the negative rail. All capacitors are 10µF, 1206, 6.3V7K. The diagram includes connection points to the CPU core and ground.

Three circuit diagrams are shown, each representing a different power rail connection for capacitors. Each diagram shows a horizontal line representing the power rail, with a ground symbol (a triangle with a horizontal line) at the right end. Capacitors are connected in parallel between the power rail and ground. The capacitors are labeled with their part number, value, and tolerance.

- Top Diagram (+CPU_CORE):** Shows capacitors C388, C408, C400, C258, and C293 connected in parallel between the +CPU_CORE rail and ground.
- Middle Diagram (+CPU_CORE):** Shows capacitors C411, C410, C257, C402, and C401 connected in parallel between the +CPU_CORE rail and ground.
- Bottom Diagram (+CPU_CORE):** Shows capacitors C403, C405, C291, and C99 connected in parallel between the +CPU_CORE rail and ground.

Three circuit diagrams showing the connection of capacitors to the +CPU_CORE supply rail. Each capacitor is connected in parallel to the supply rail and ground. The capacitors are labeled with their values: 10U_1206_6.3V7K.

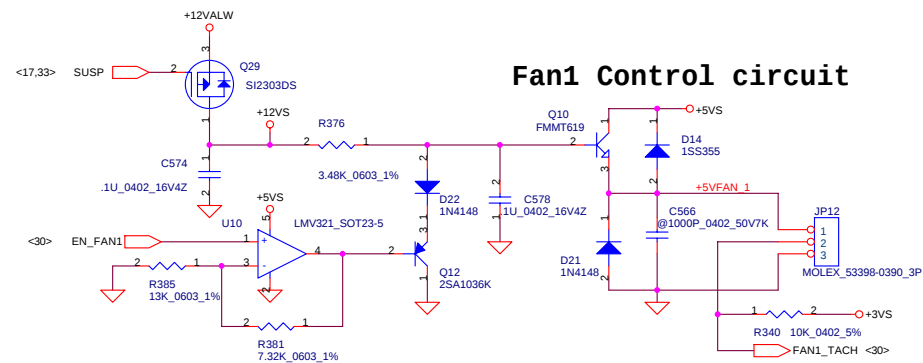
- Diagram 1:** Shows capacitors C122, C121, C356, C62, and C404 connected to the +CPU_CORE supply rail.
- Diagram 2:** Shows capacitors C351, C292, C368, C100, and C296 connected to the +CPU_CORE supply rail.
- Diagram 3:** Shows capacitors C409, C64, C68, and C66 connected to the +CPU_CORE supply rail.

Place close to CPU power and ground pin as possible (<1inch)

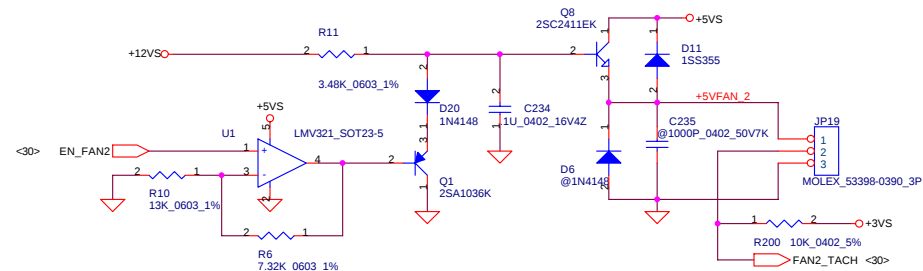
For Mobile's CPU:
ESR total=1.875m ohm
C total=2590uF

PLACE ON CPU SIDE

The diagram shows the CPU side of the power supply circuit. It features a series of capacitors (C104, C111, C113, C117, C119, C120, C110, C112, C116, C118) connected in a chain between the +CPU_CORE and 22U_0603_10V7K rails. Each capacitor is connected to the top rail through a 22U_0603_10V7K component. The bottom rail is also connected to the 22U_0603_10V7K components.



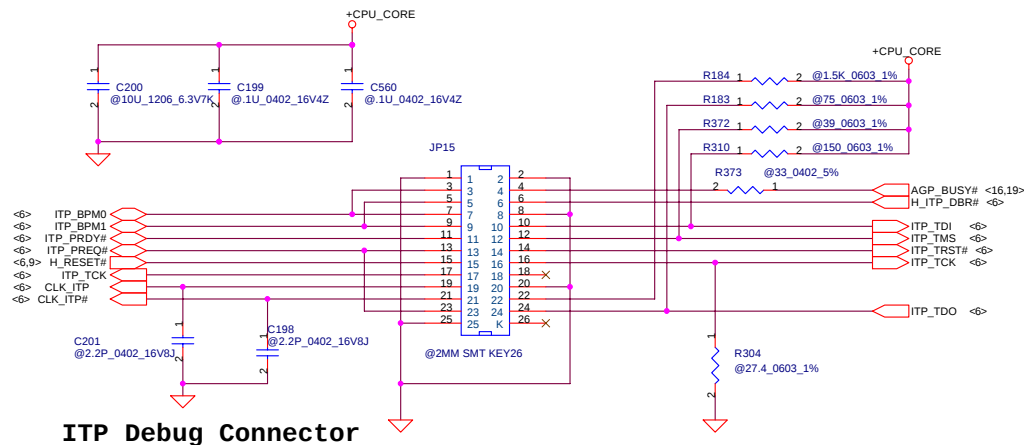
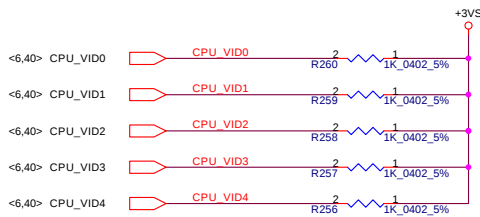
Fan2 Control circuit



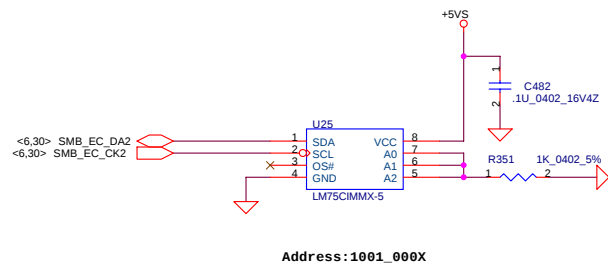
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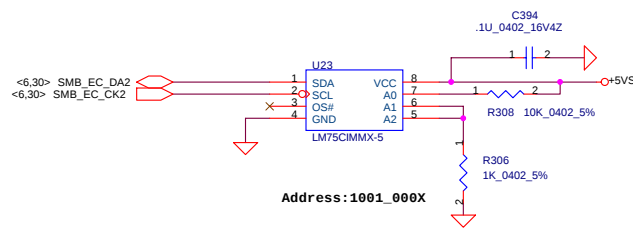
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ITP Debug Connector



Address:1001_000X



Address:1001_000X

MO/DT_CPU	Mobile CPU					Desktop CPU				
	1					0				
VID	4	3	2	1	0	4	3	2	1	0
VCC										
1.750V	0	0	0	0	0	0	0	1	0	0
1.700V	0	0	0	0	1	0	0	1	1	0
1.650V	0	0	0	1	0	0	1	0	0	0
1.600V	0	0	0	1	1	0	1	0	1	0
1.550V	0	0	1	0	0	0	1	1	0	0
1.500V	0	0	1	0	1	0	1	1	1	0
1.450V	0	0	1	1	0	1	0	0	0	0
1.400V	0	0	1	1	1	1	0	0	1	0
1.350V	0	1	0	0	0	1	0	1	0	0
1.300V	0	1	0	0	1	1	0	1	1	0
1.250V	0	1	0	1	0	1	1	0	0	0
1.200V	0	1	0	1	1	1	1	0	1	0
1.150V	0	1	1	0	0	1	1	1	0	0
1.100V	0	1	1	0	1	1	1	1	1	0
1.050V	0	1	1	1	0	X	X	X	X	X
1.000V	0	1	1	1	1	X	X	X	X	X
0.975V	1	0	0	0	0	X	X	X	X	X
0.950V	1	0	0	0	1	X	X	X	X	X
0.925V	1	0	0	1	0	X	X	X	X	X
0.900V	1	0	0	1	1	X	X	X	X	X
0.875V	1	0	1	0	0	X	X	X	X	X
0.850V	1	0	1	0	1	X	X	X	X	X
0.825V	1	0	1	1	0	X	X	X	X	X
0.800V	1	0	1	1	1	X	X	X	X	X
0.775V	1	1	0	0	0	X	X	X	X	X
0.750V	1	1	0	0	1	X	X	X	X	X
0.725V	1	1	0	1	0	X	X	X	X	X
0.700V	1	1	0	1	1	X	X	X	X	X
0.675V	1	1	1	0	0	X	X	X	X	X
0.650V	1	1	1	0	1	X	X	X	X	X
0.625V	1	1	1	1	0	X	X	X	X	X
0.600V	1	1	1	1	1	X	X	X	X	X
VRM output off						1	1	1	1	1

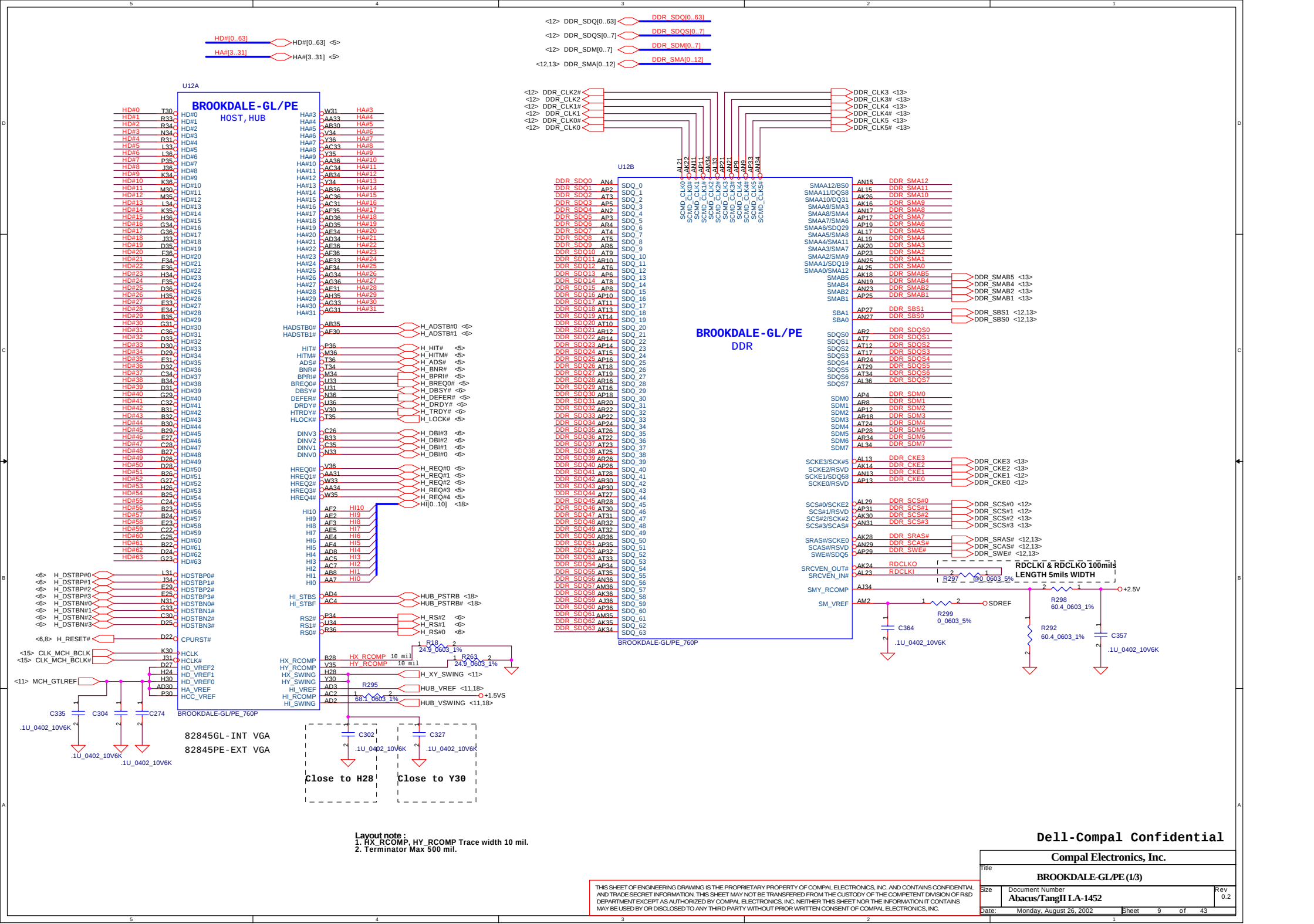
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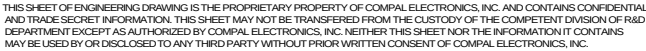
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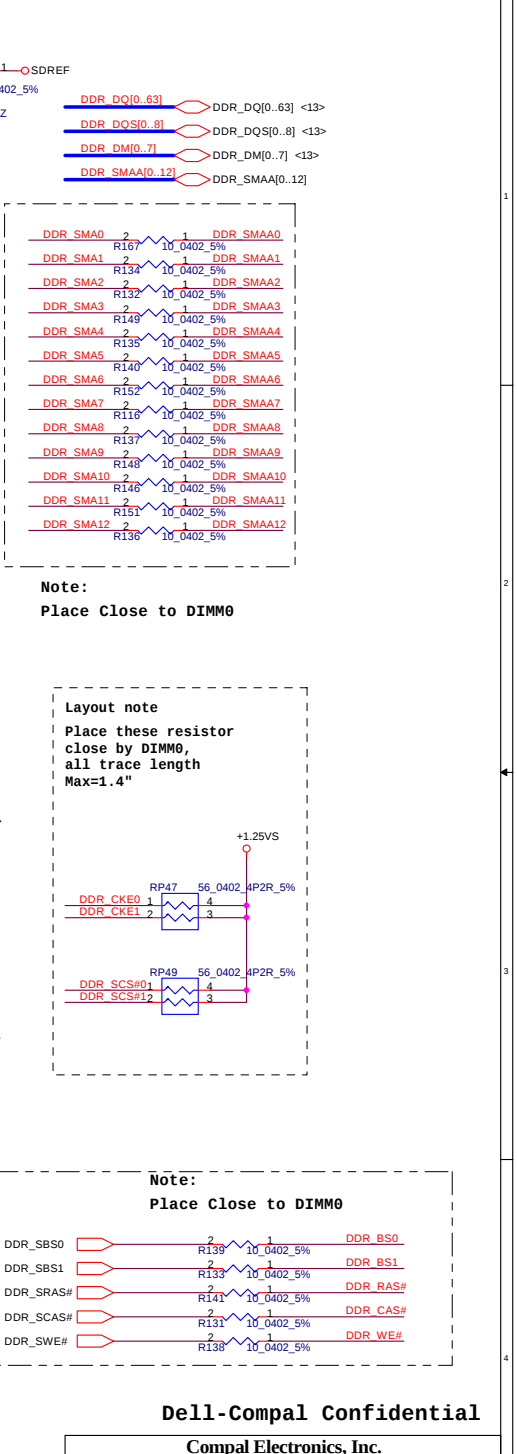
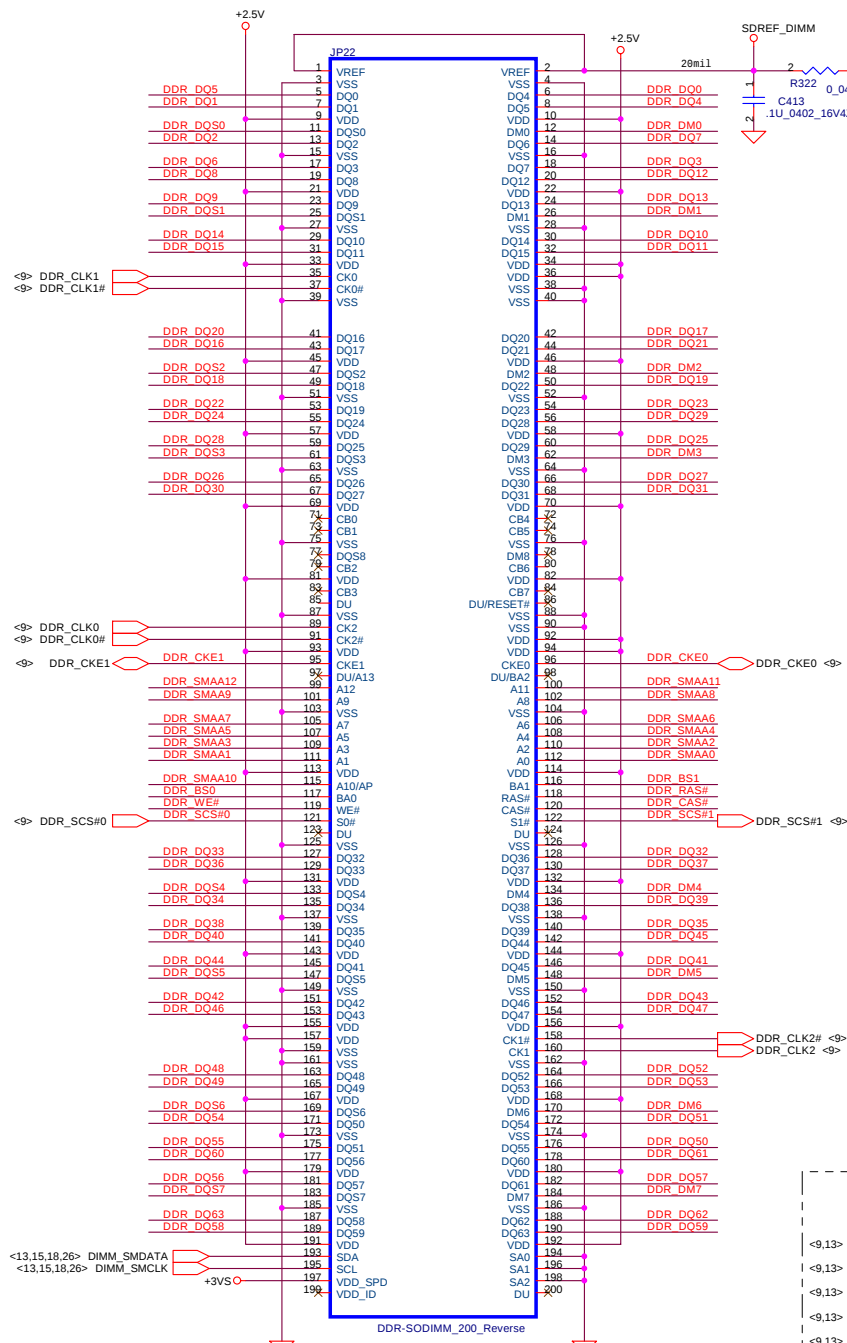
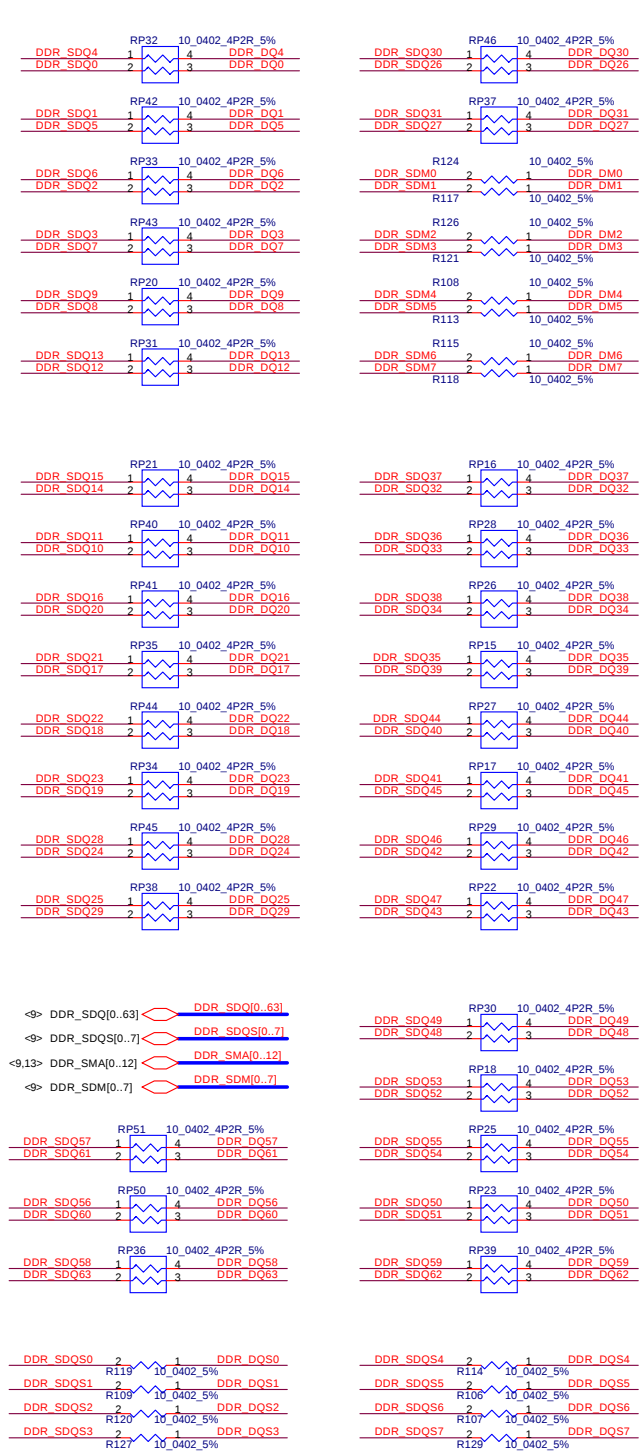
CPU VID & ITP PORT

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Layout note
Place these resistors
close to DIMM0,
all trace length<500 mil

Note:
Place Close to DIMM0

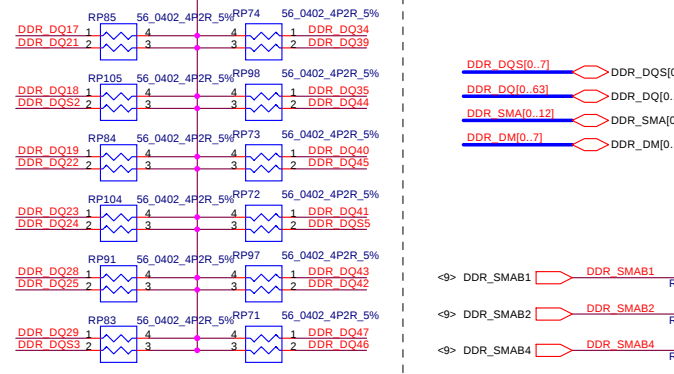
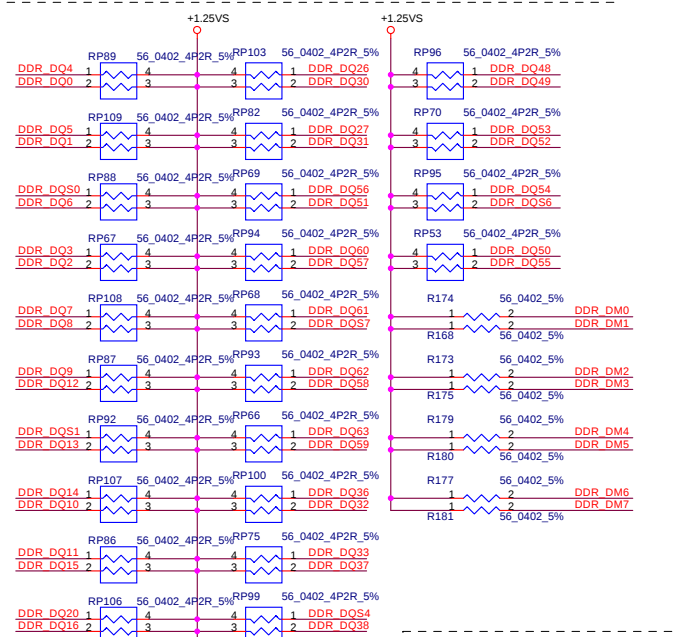
Layout note
Place these resistor
close by DIMM0,
all trace length
Max=1.4"

Note:
Place Close to DIMM0

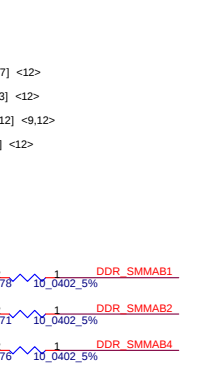
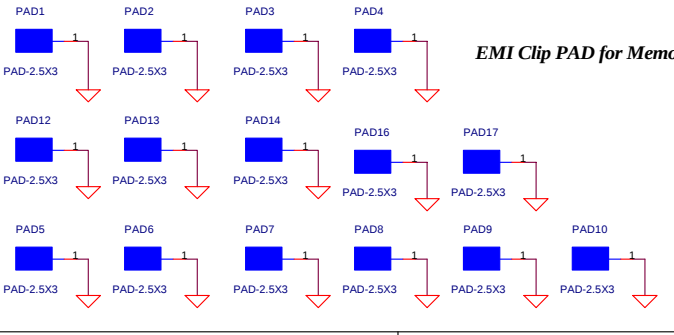
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DDR-SODIMM SLOT0			
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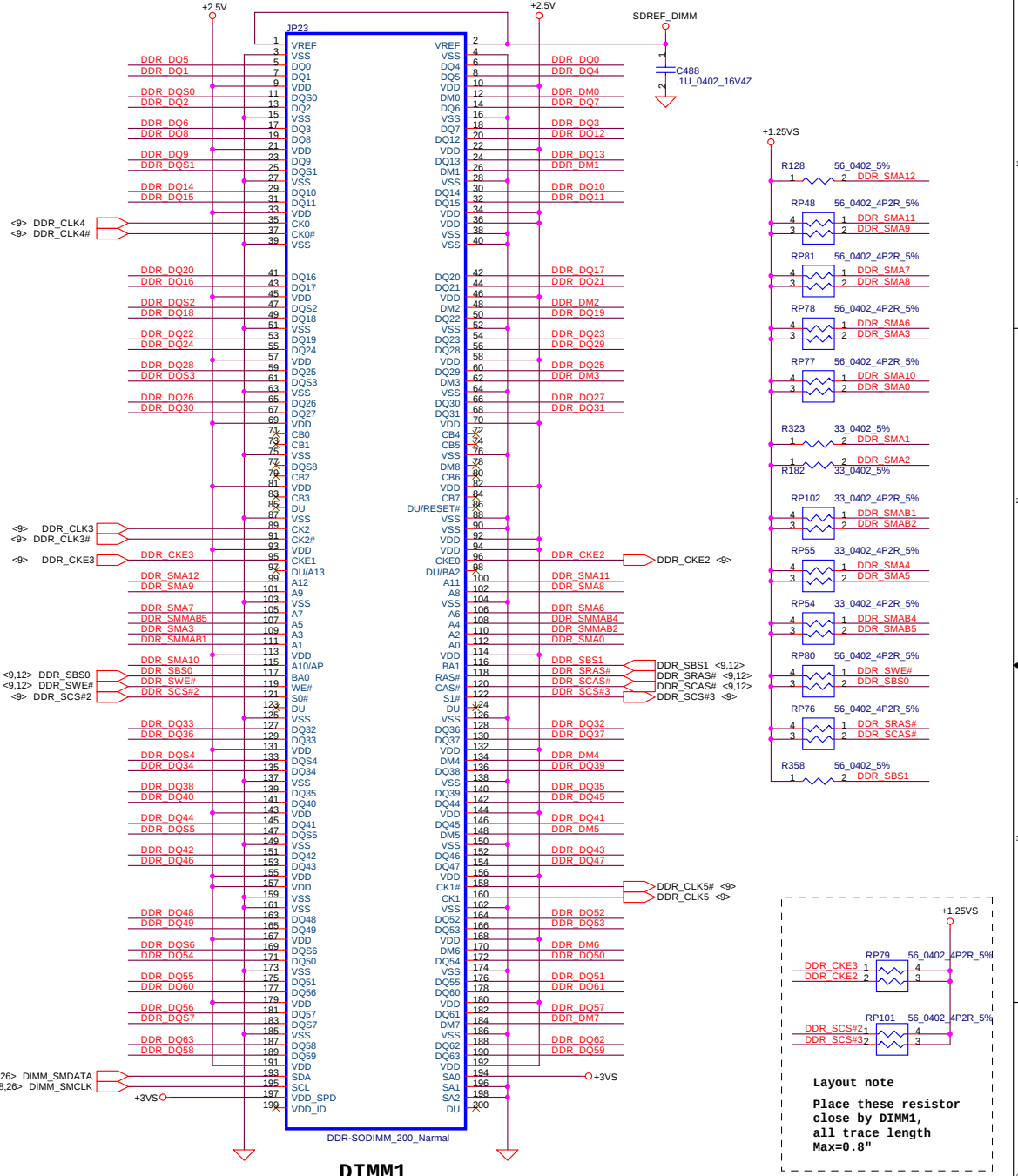
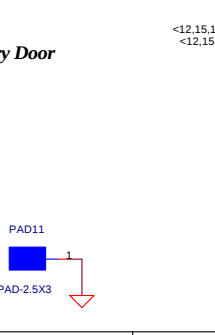
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Layout note
Place these resistor
closely DIMM1,
all trace
length<=800m11



Layout note
Place these resistor
closely DIMM1,
all trace
length<=800m11

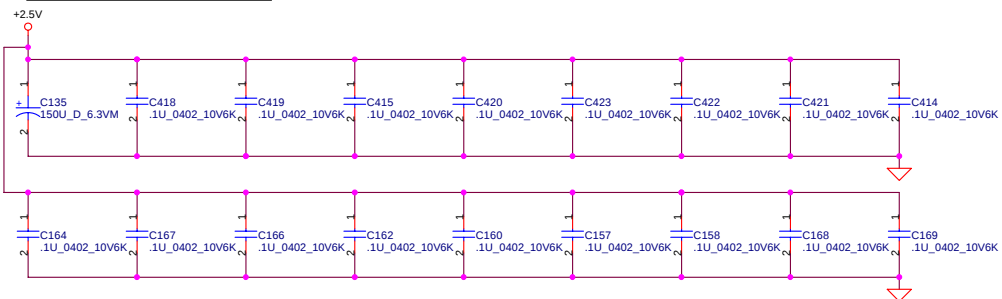


Layout note
Place these resistor
close by DIMM1,
all trace length
Max=0.8"

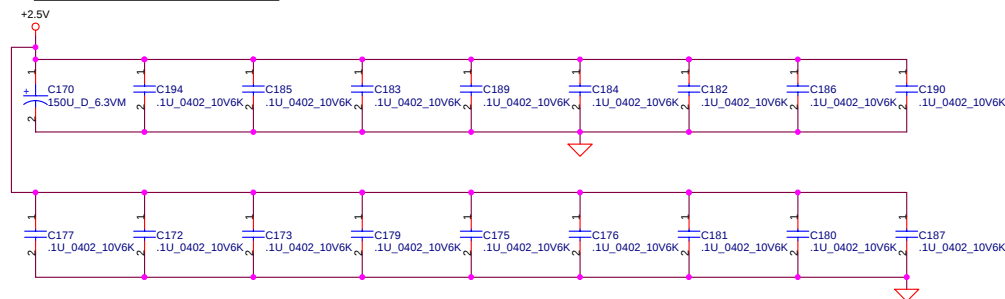
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Title			
DDR-SODIMM SLOT1			
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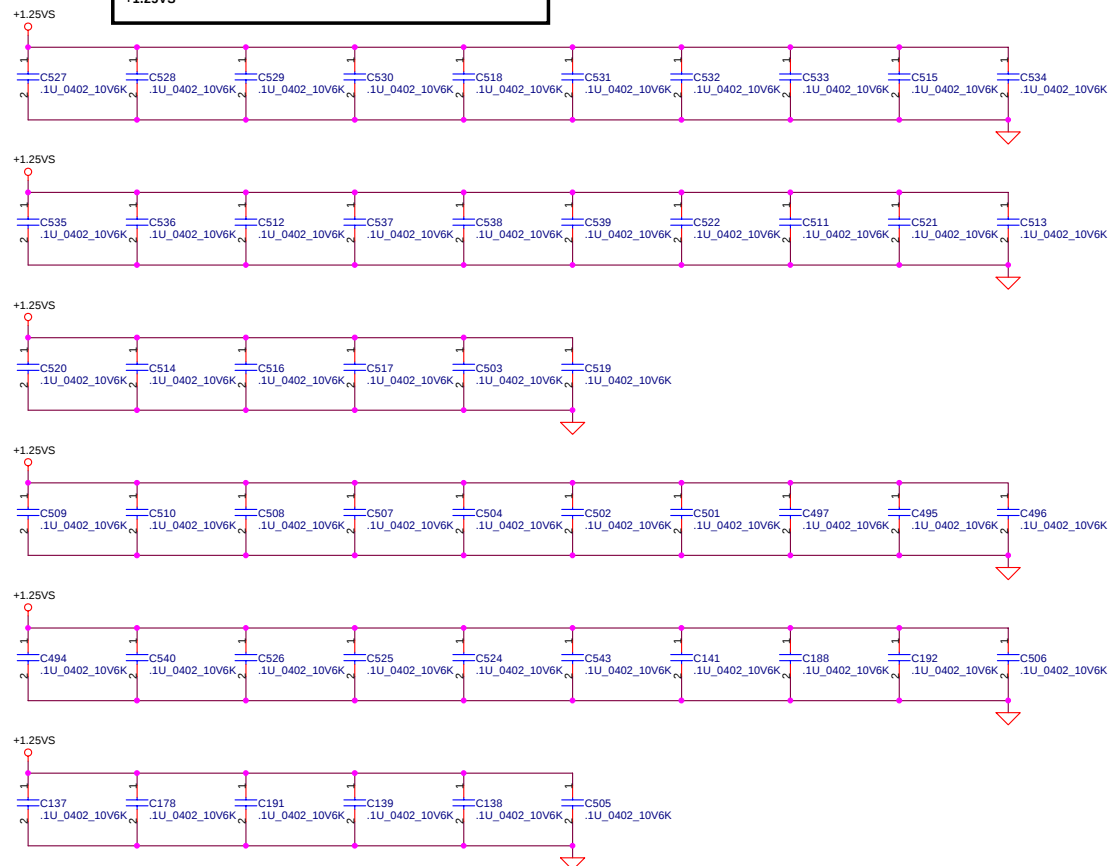
Layout note :
Distribute as close as possible
to DDR-SODIMM0.



Layout note :
Distribute as close as possible
to DDR-SODIMM1.



Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25VS

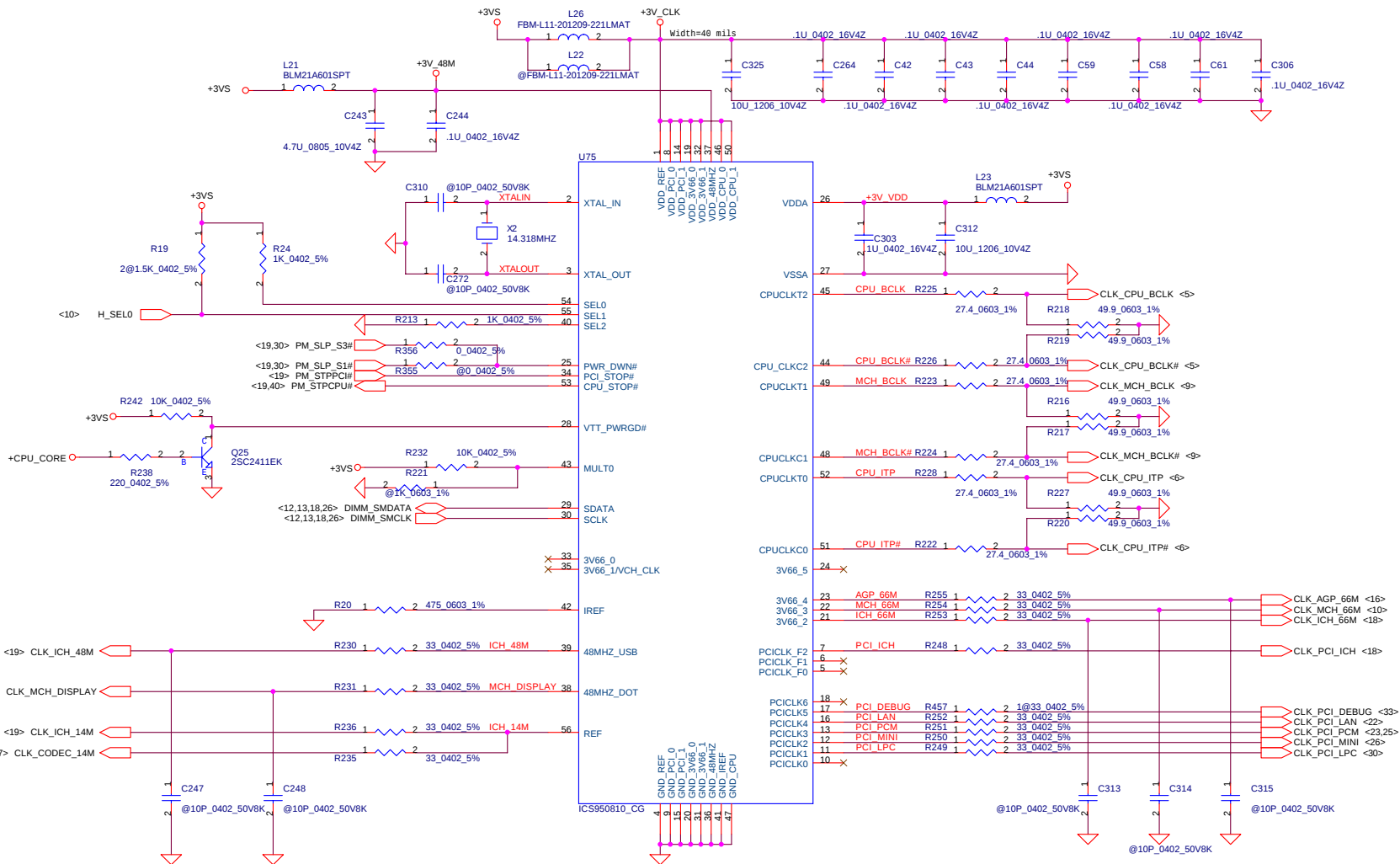


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Title		
DDR SODIMM Decoupling		
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CPU Frequency Select Table

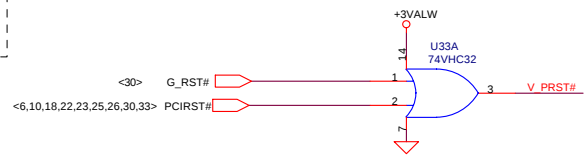
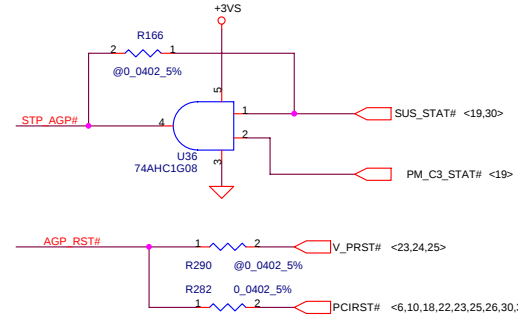
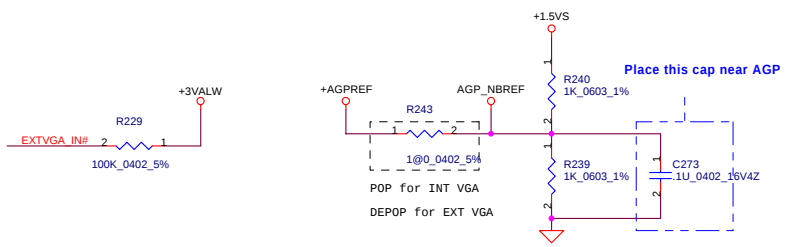
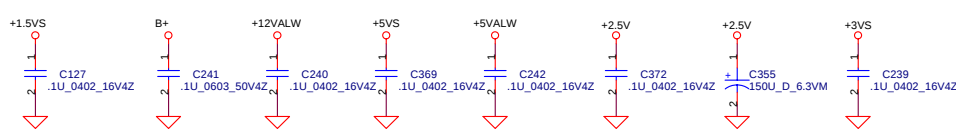
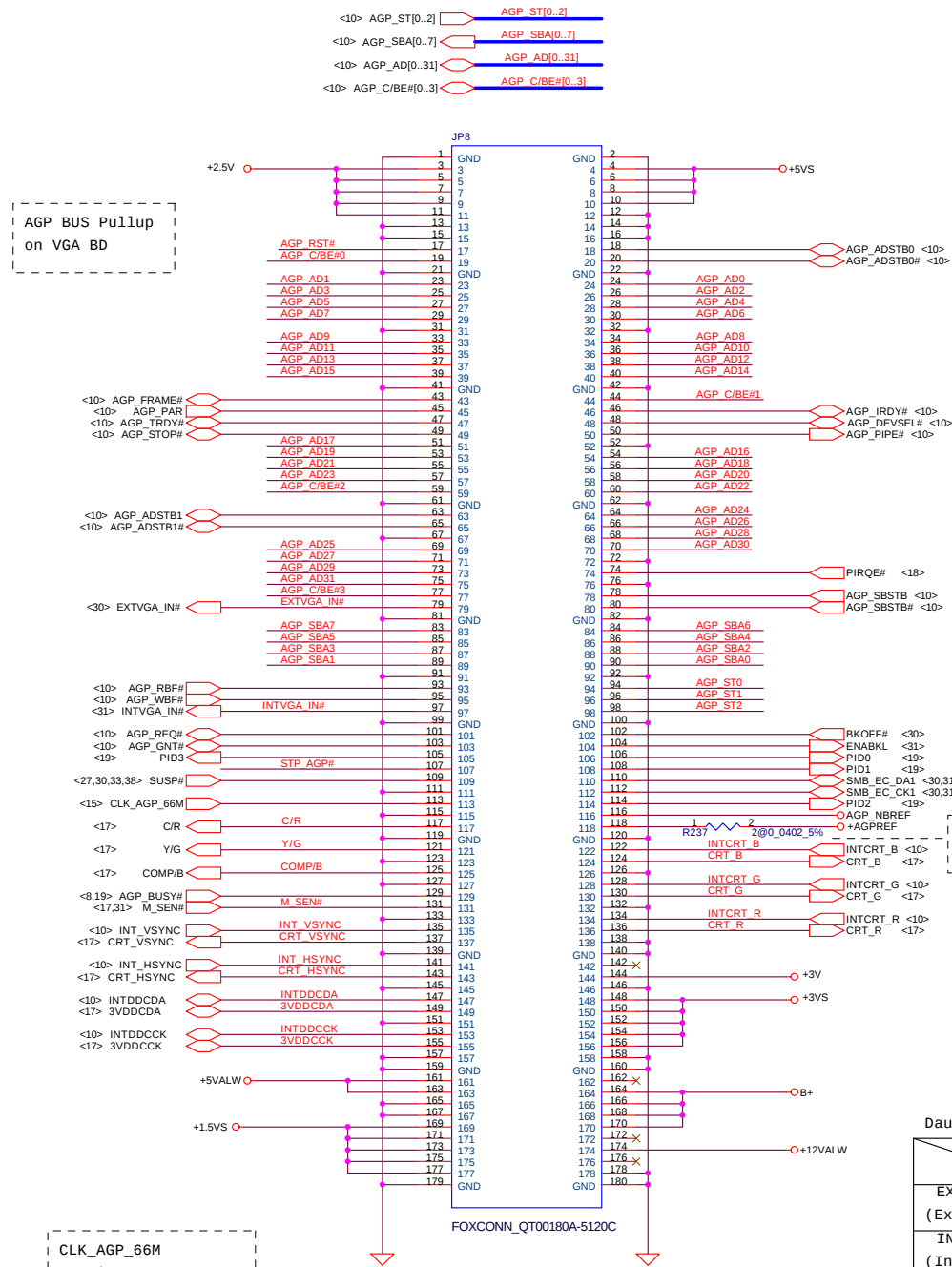
SEL[2:0]	CK-408 Speed
001	100 MHZ
011	133 MHZ

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Title			
Clock Generator			
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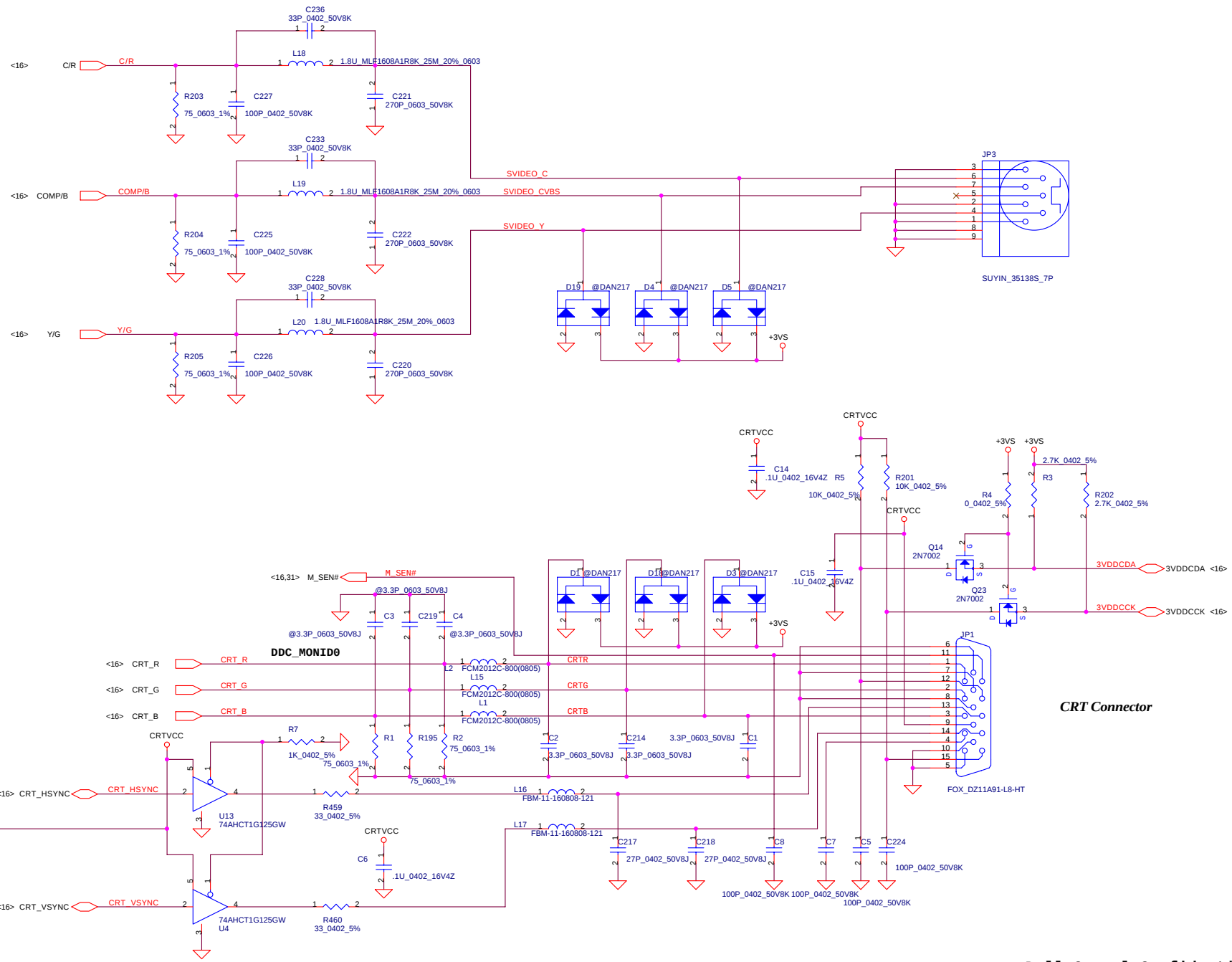
Daughter Card Present Table

	DOCKED	NON DOCKED
EXTVGA_IN# (Ext. Graphy)	LOW	HIGH
INTVGA_IN# (Int. Graphy)	LOW	HIGH

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AGP Conn.			
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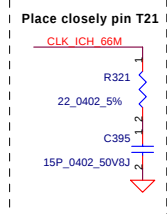
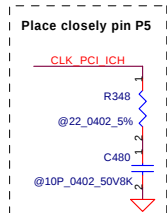
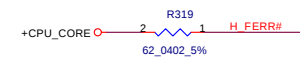


CRT Connector

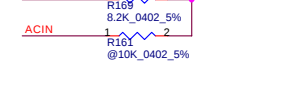
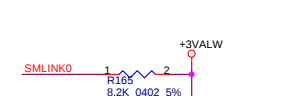
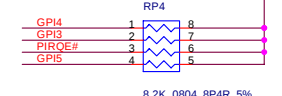
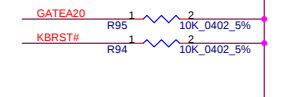
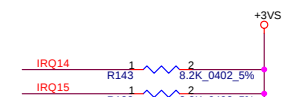
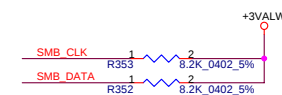
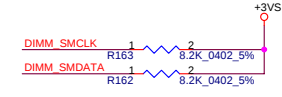
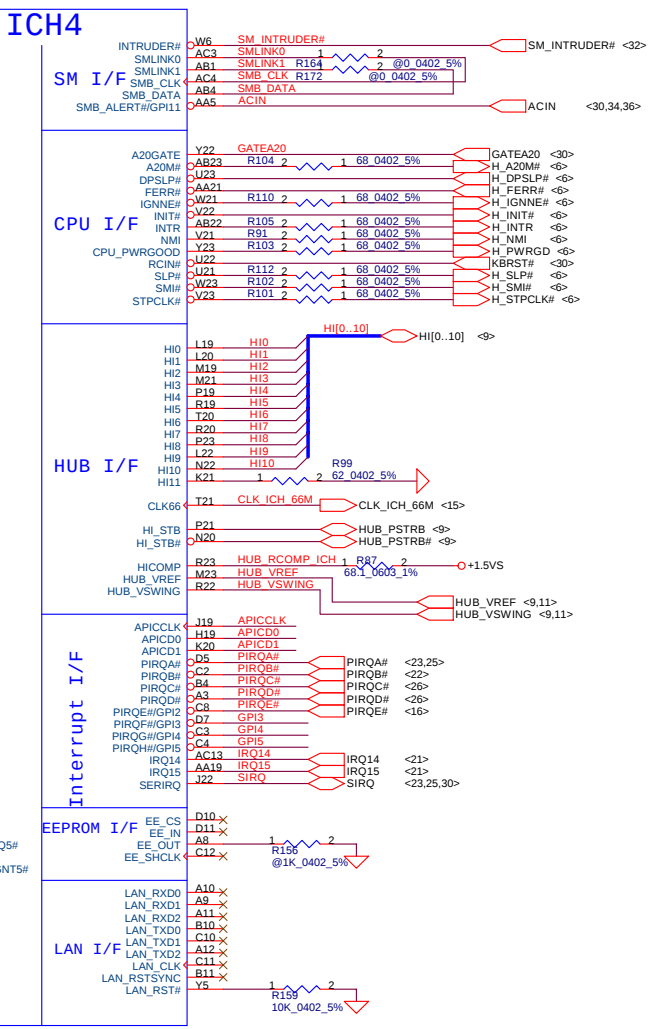
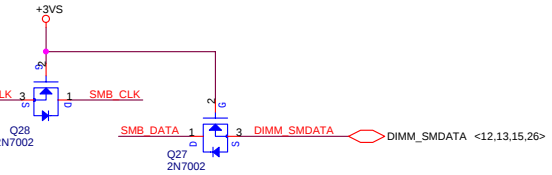
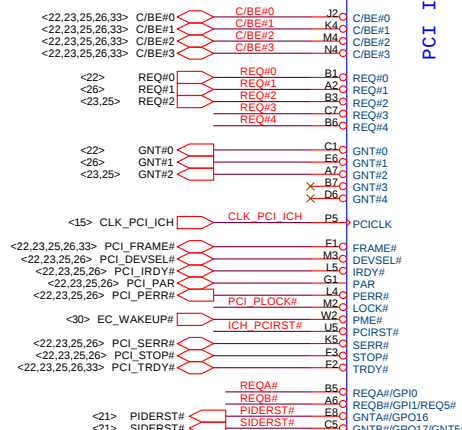
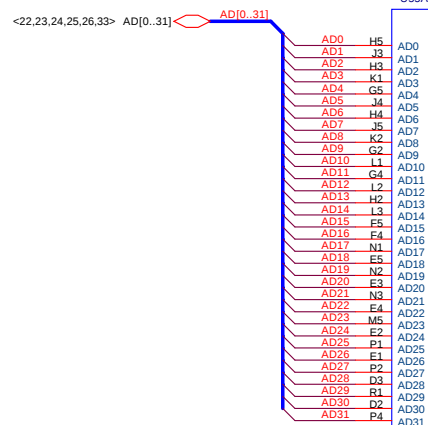
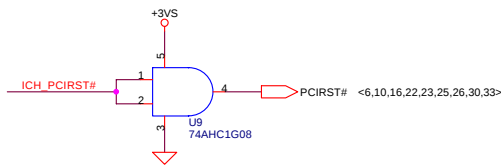
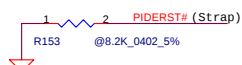
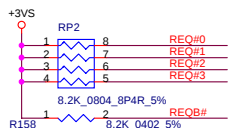
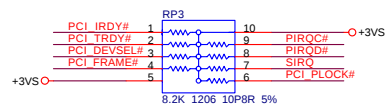
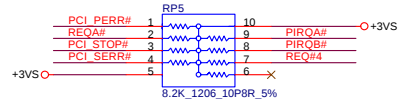
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Compal Electronics, Inc.			
Title			
TV OUT & CRT			
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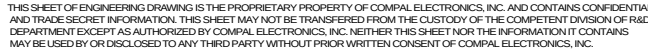
PCI Pullups



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Compal Electronics, Inc.			
INTEL ICH4 (I/3)			
Size	Document Number	Sheet	Rev
	Abacus/TangII LA-1452	18	0.2
Date:	Tuesday, August 27, 2002	Sheet	18 of 43

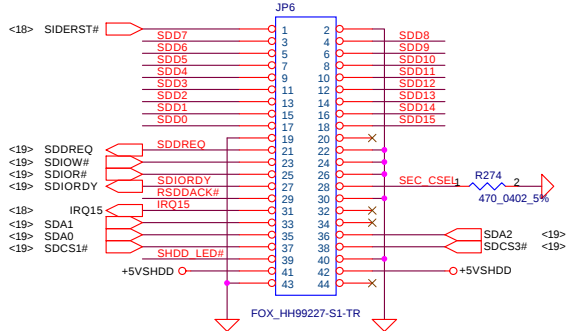
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HDD Connector

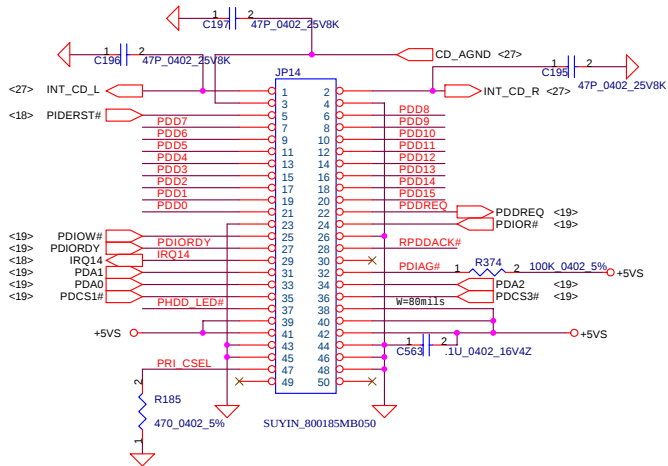
<19> SDD[0..15] SDD[0..15]

Correct HDD pin define ,pls update layout



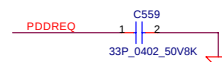
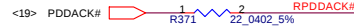
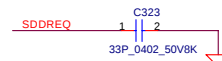
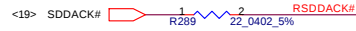
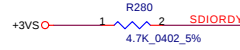
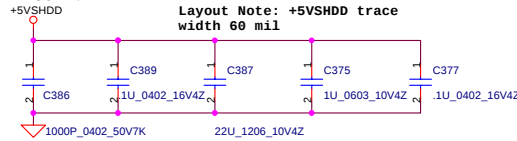
CD-ROM Connector

<19> PDD[0..15] PDD[0..15]

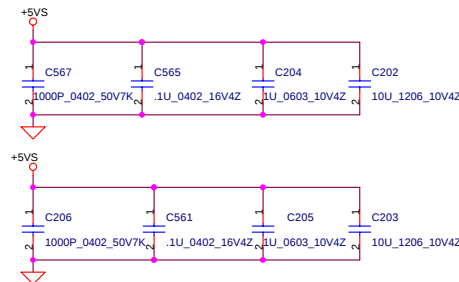


Place caps. near HDD CONN.

Layout Note: +5VSHDD trace width 60 mil

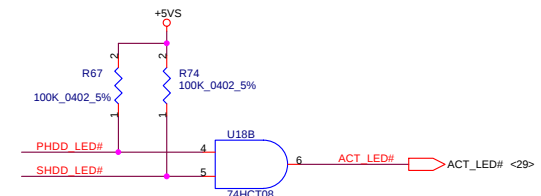
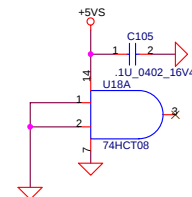
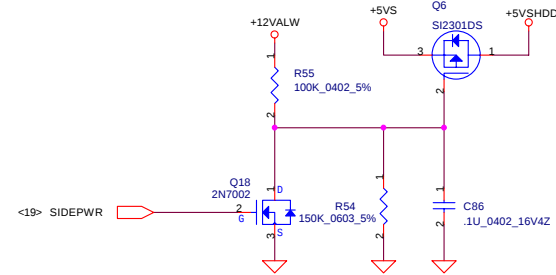


Place caps. near CDROM CONN.



SI2301DS: P CHANNEL
VGS: -4.5V, RDS: 130 mOHM
VGS: -2.5V, RDS: 190mOHM
Id(MAX): 2.3A
VGS(MAX): +-8V

1 D



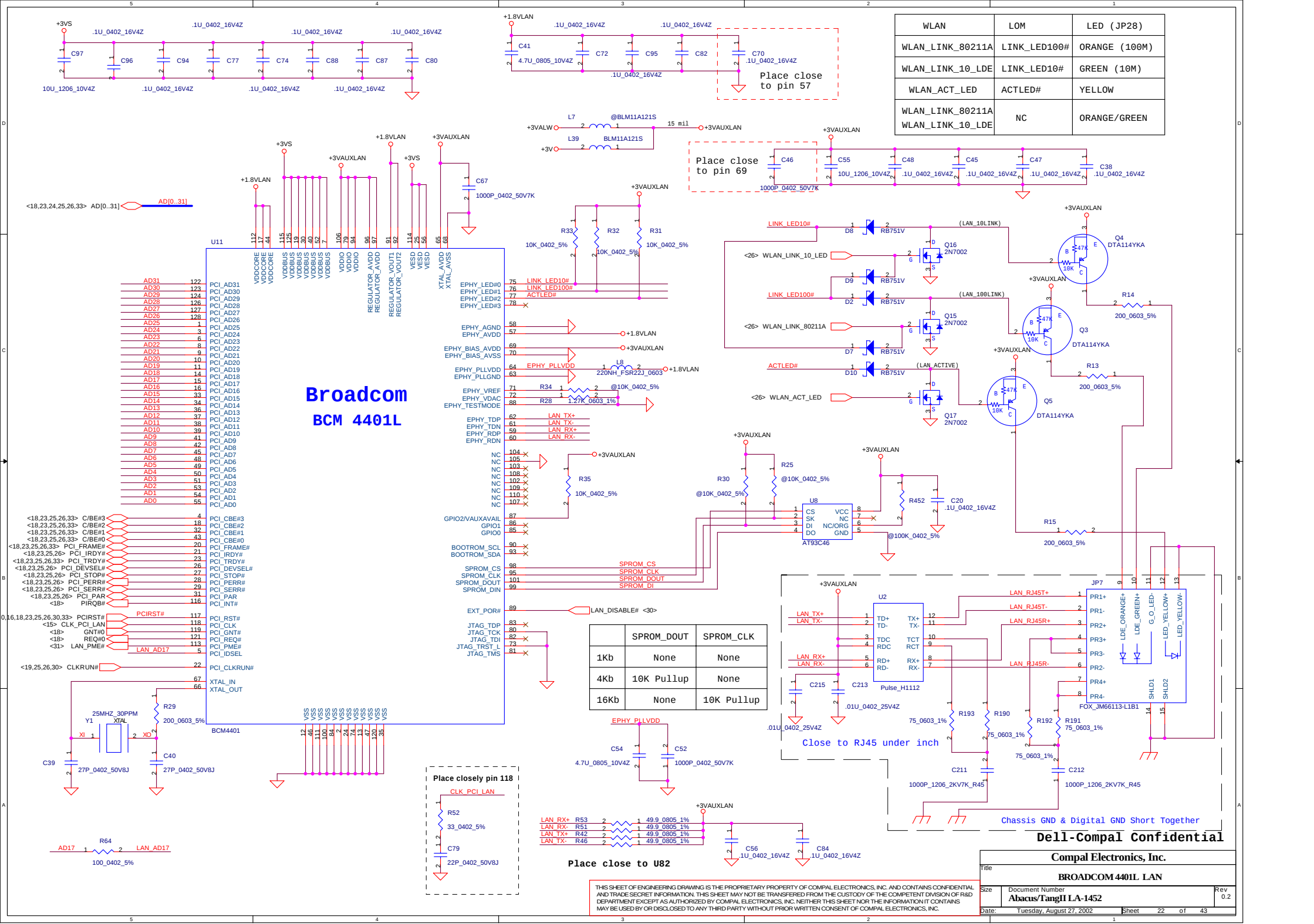
Dell-Compal Confidential

Compal Electronics, Inc.

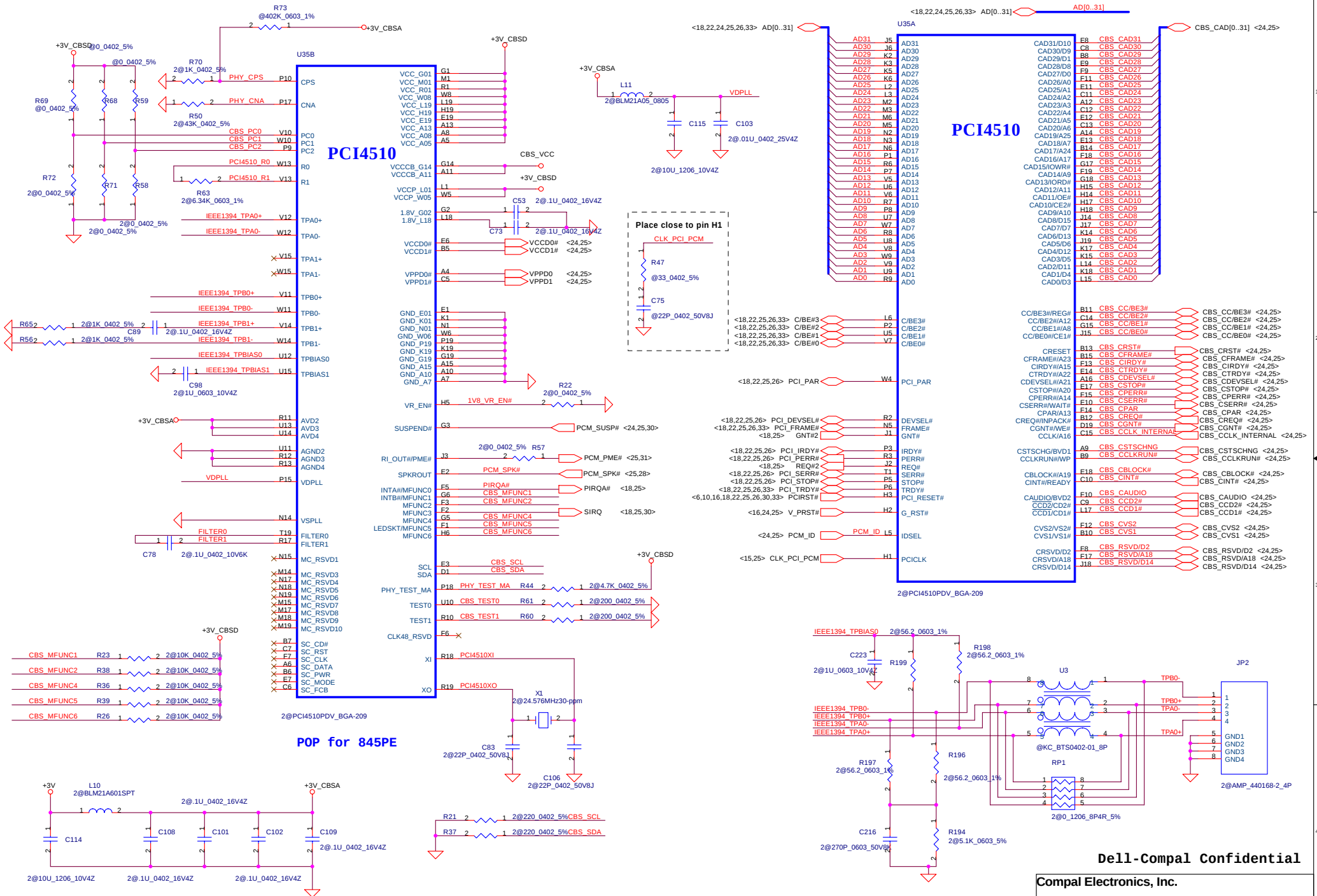
IDE/FDD/CD-ROM Module

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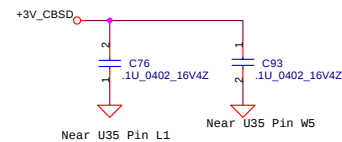
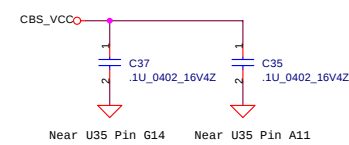
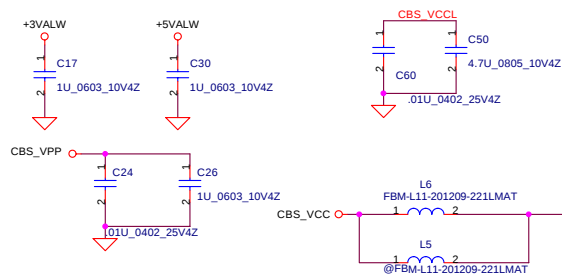
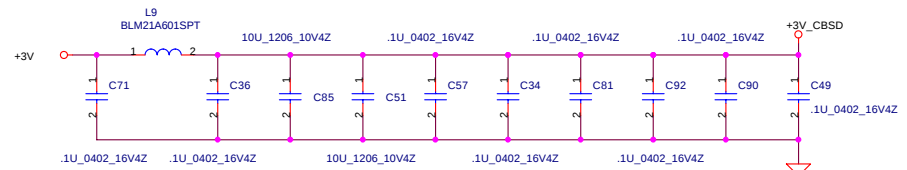
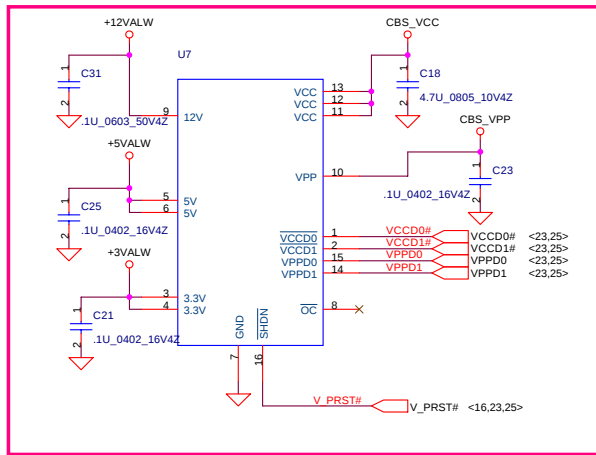
Dell-Compal Confidential

Compal Electronics, Inc.

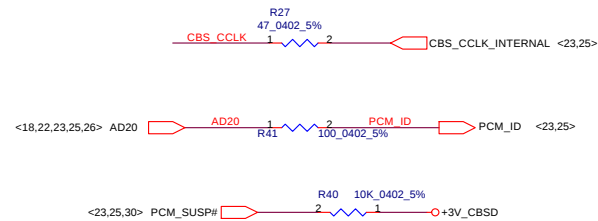
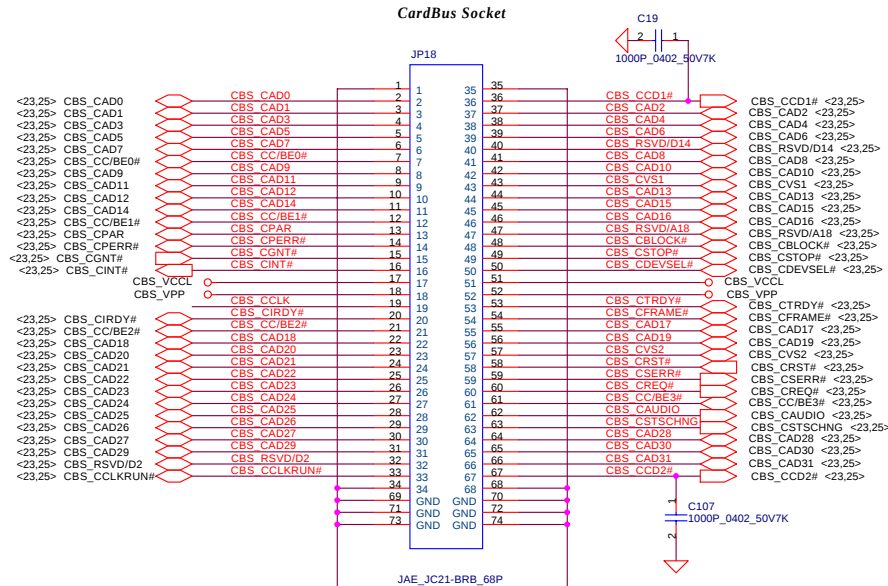
Title			
PCMCIA Ctrl OZ6912 & Socket			
Size	Document Number	Rev	
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PCMCIA Power Controller



CardBus Socket



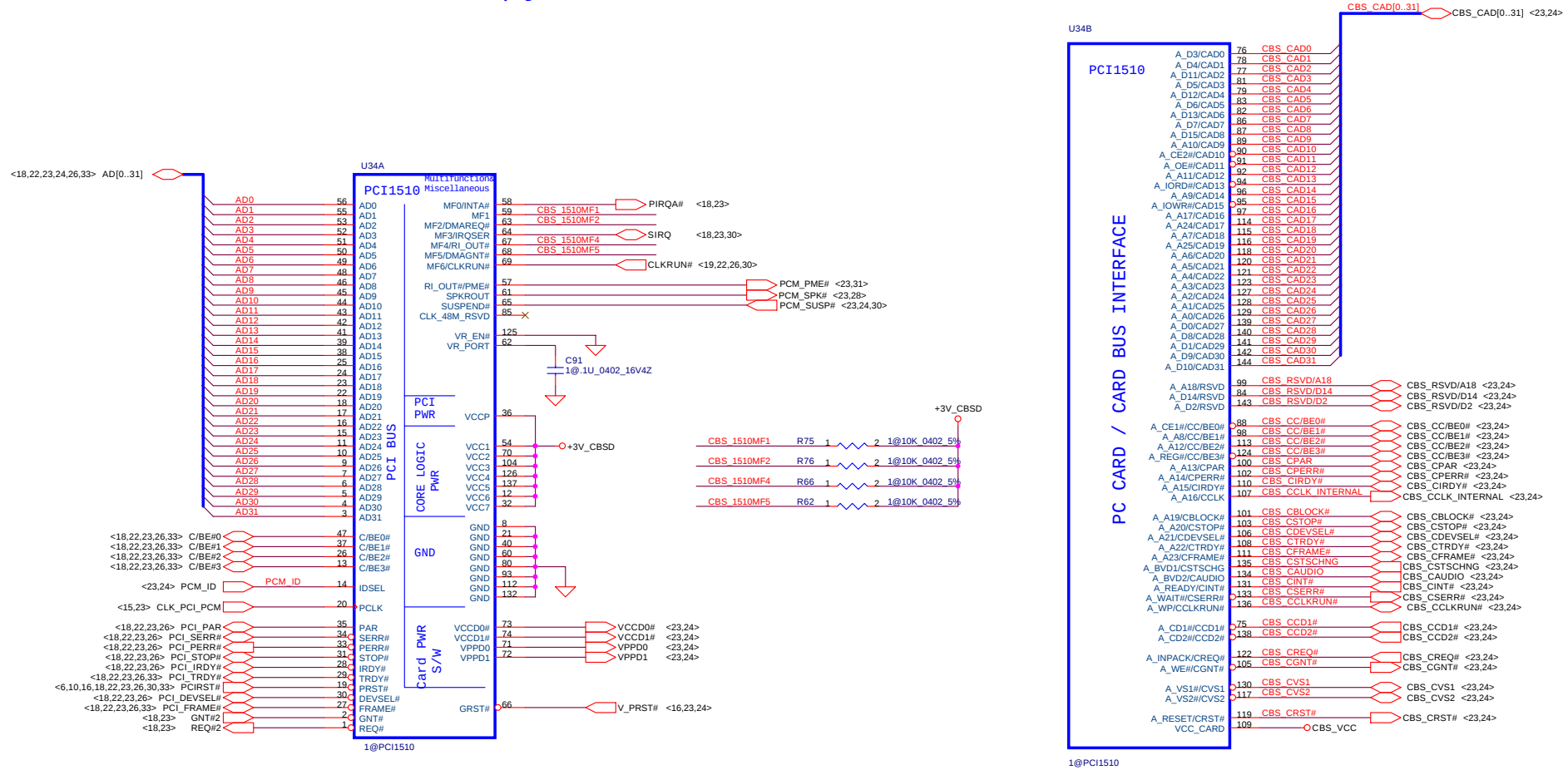
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Compal Electronics, Inc.

Title			PCMCIA Ctrl OZ6912 & Socket
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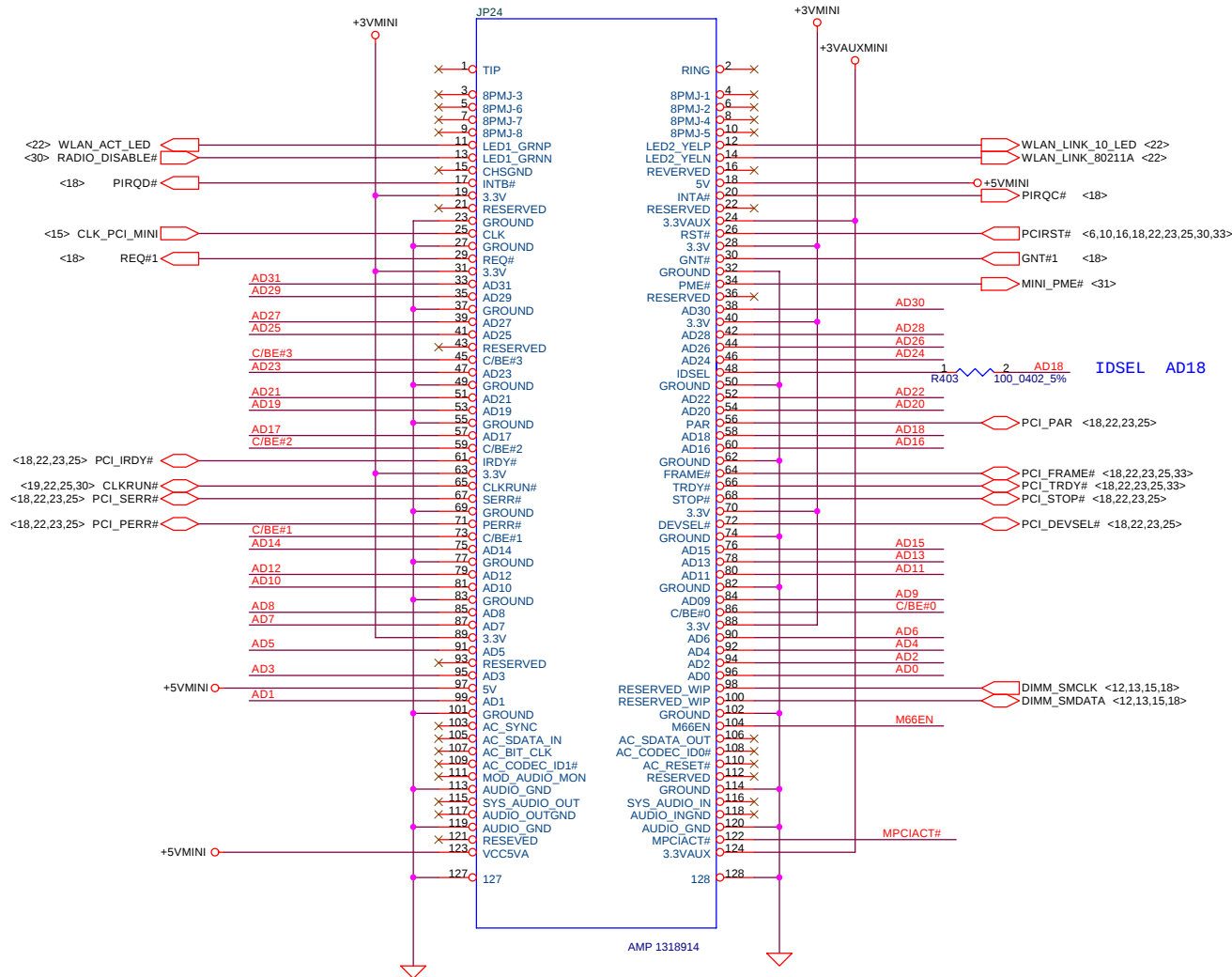
Dell-Compal Confidential

Compal Electronics, Inc.

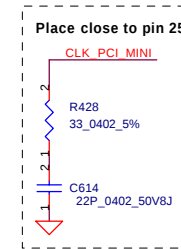
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PCMCIA Ctrl OZ6912 & Socket			
Size	Document Number	Rev	
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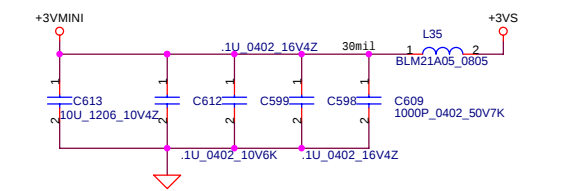
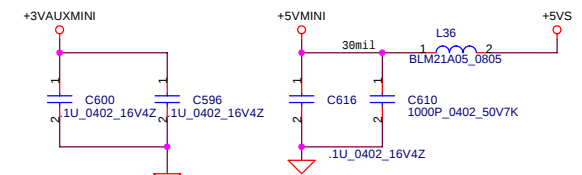
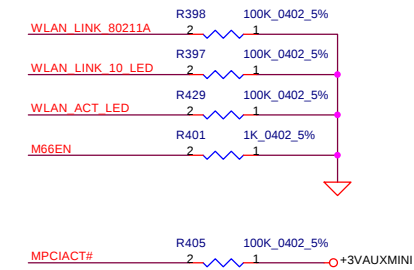
MINI PCI TYPE III



WIRELESS SUPPORT ONLY



<18,22,23,24,25,33> AD[0..31]
<18,22,23,25,33> C/BE#[0..3]

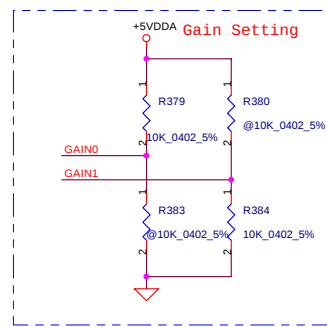
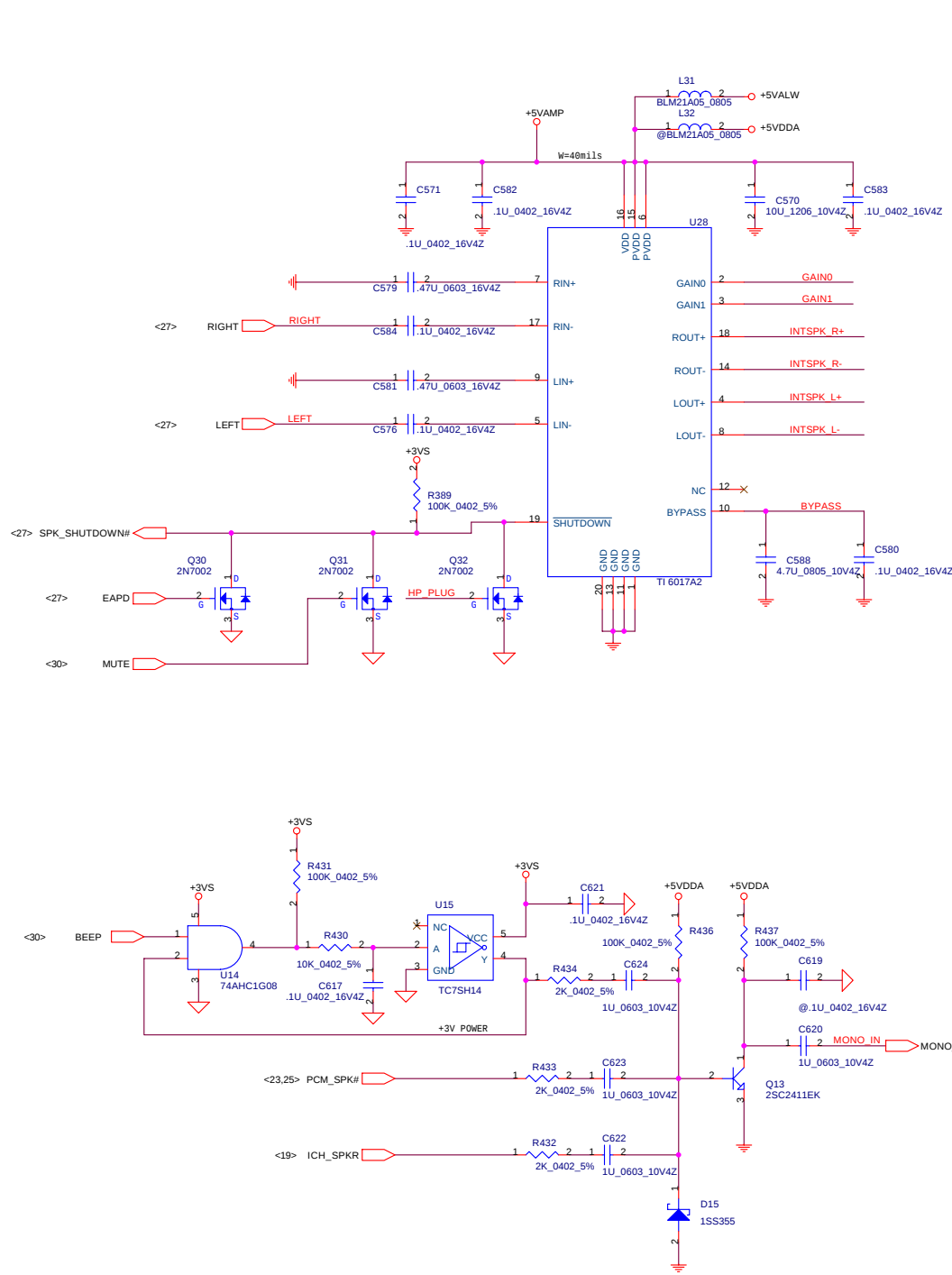


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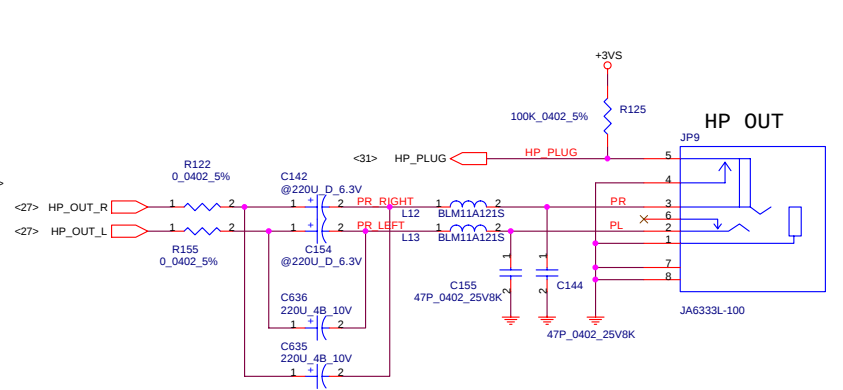
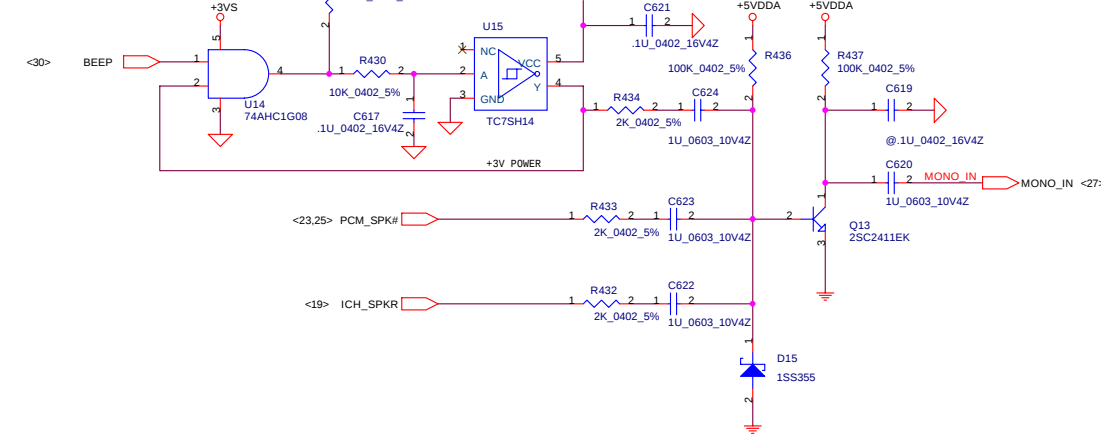
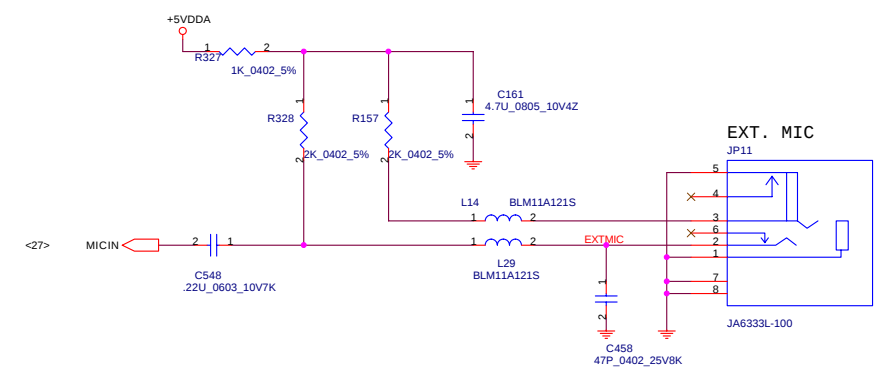
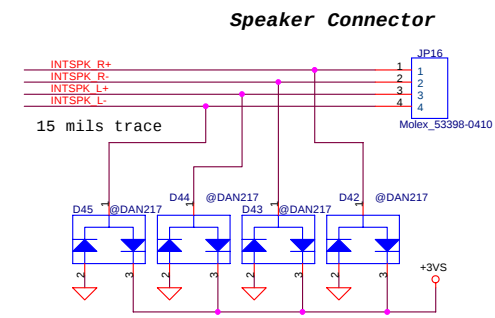
Compal Electronics, Inc.

Title		
MiniPci Port		
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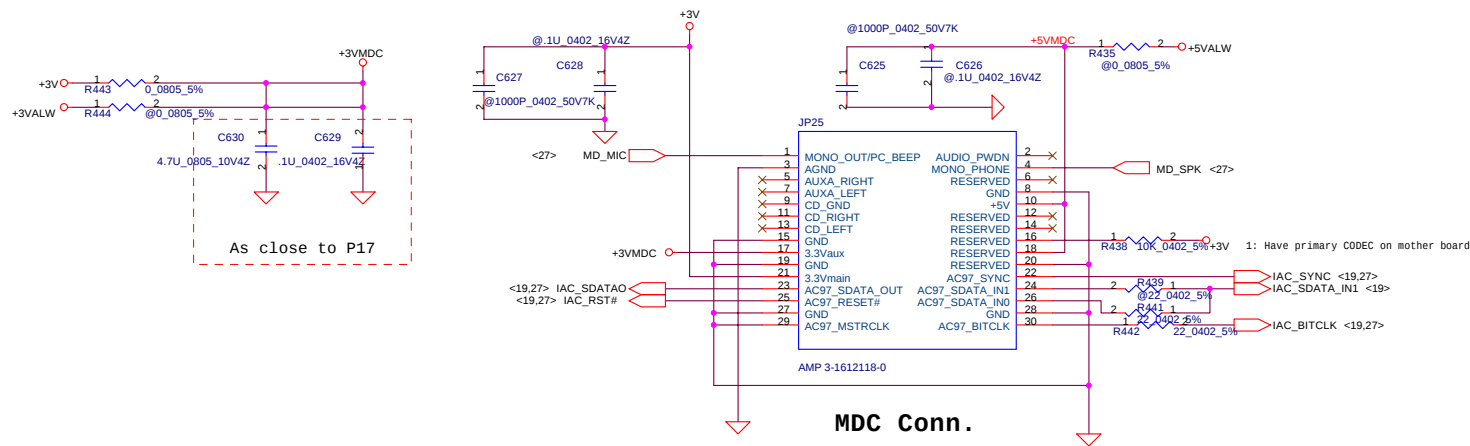
GAIN0	GAIN1	AV(inv)	INPUT IMPEDANCE
0	0	6dB	90K ohm
0	1	10dB	70K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	25K ohm



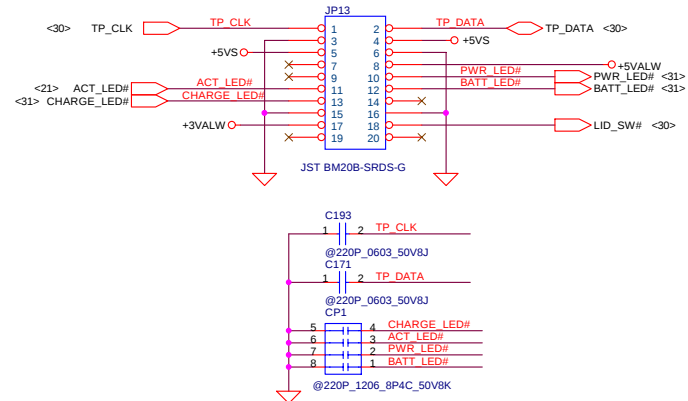
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Compal Electronics, Inc.		
Title		
AMP & Audio Jack		
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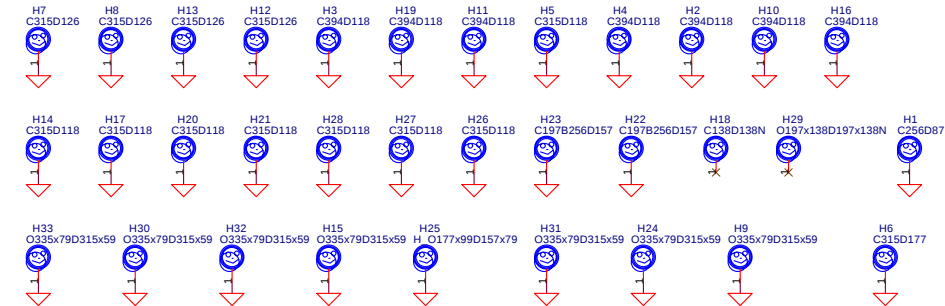
Touch Pad & Status LED Conn.



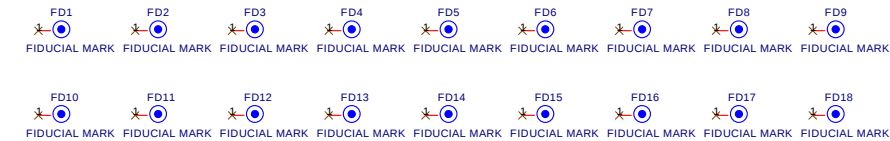
MDC Note

Pin 1 is NC for Pctel and connexant MDC modem
Pin 2 is NC for Pctel and connexant MDC modem

Screw Hole



Fiducial Mark

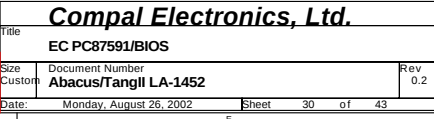


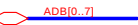
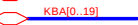
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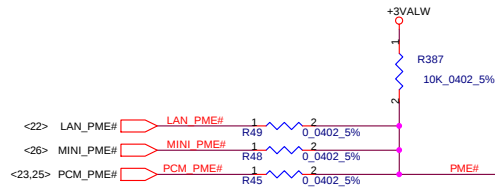
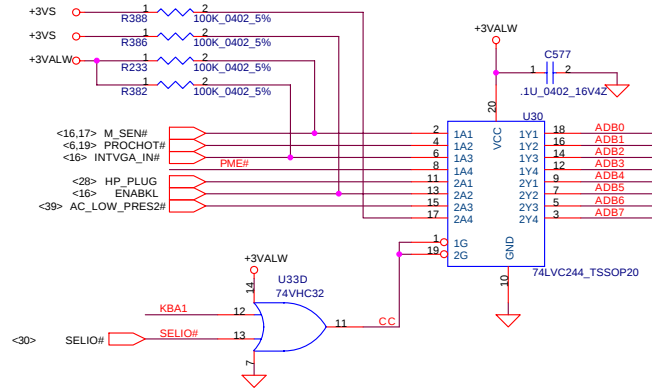
Title			
MDC connector / SWITCH / ACPI/DEBUG			
Size	Document Number	Rev	
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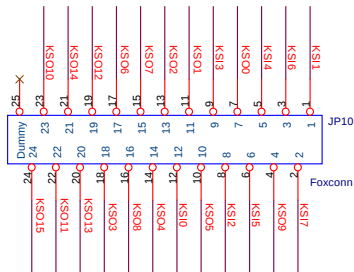


<30> ADB[0..7]  ADB[0..7]
<30> KBA[0..19]  KBA[0..19]

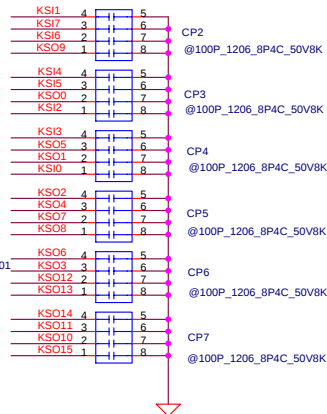
Input Port



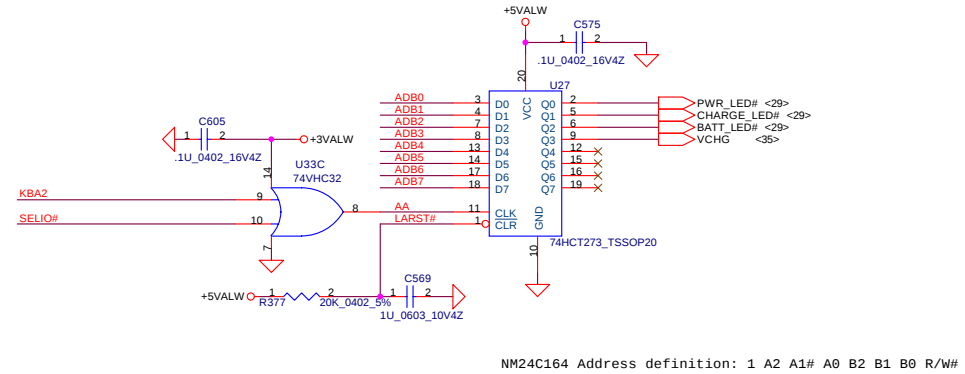
INT_KBD CONN.



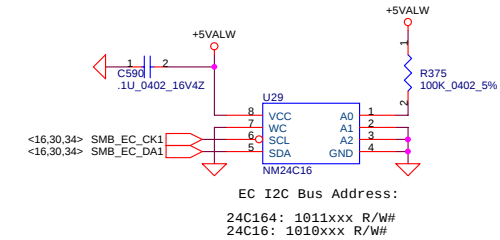
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<30,32> KSI[0..7]  KSI[0..7]



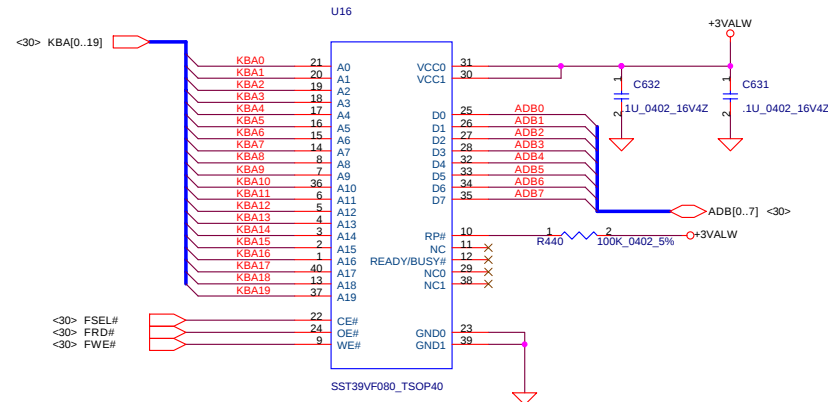
Output Port



NM24C164 Address definition: 1 A2 A1# A0 B2 B1 B0 R/W#



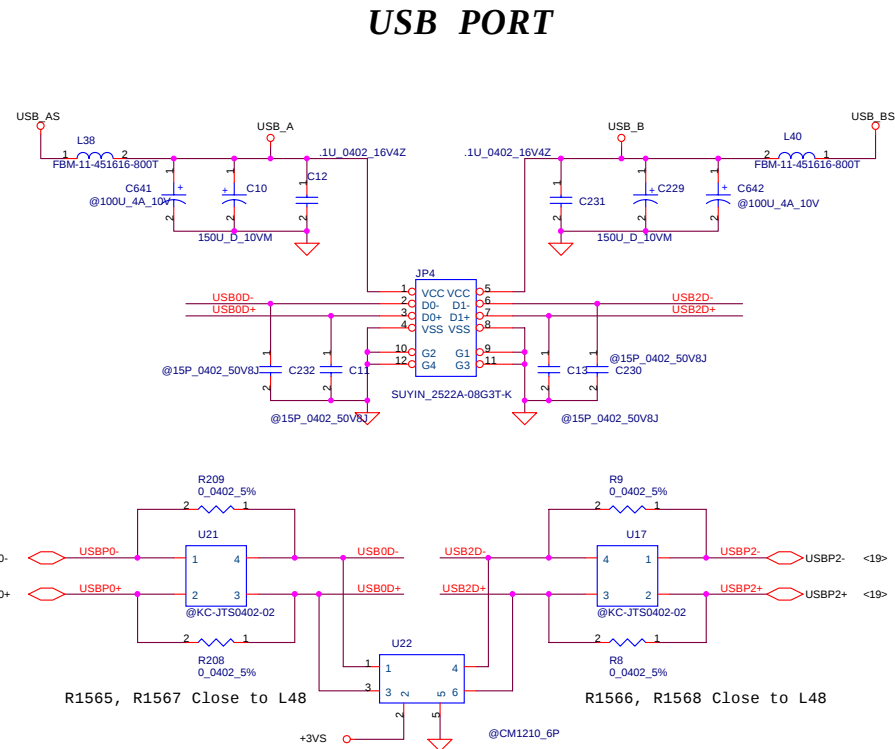
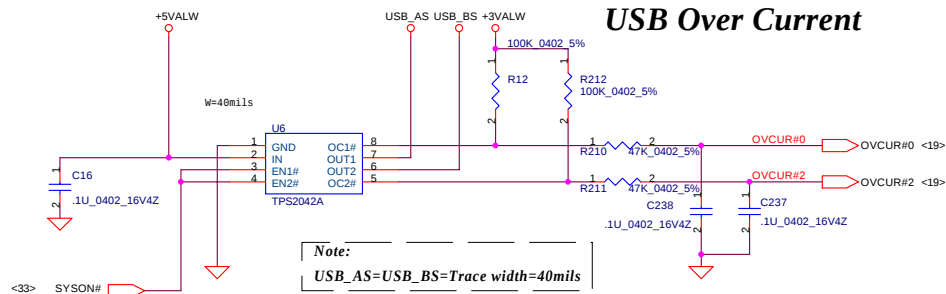
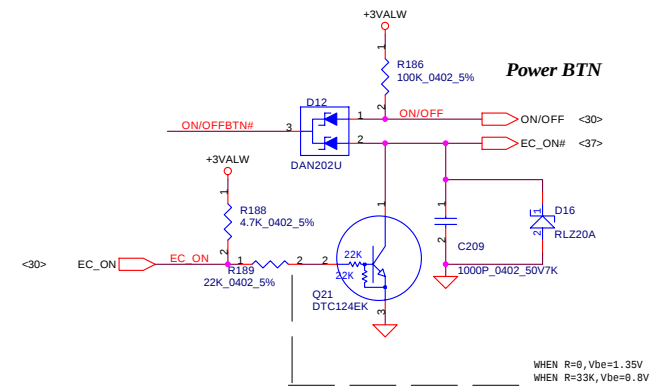
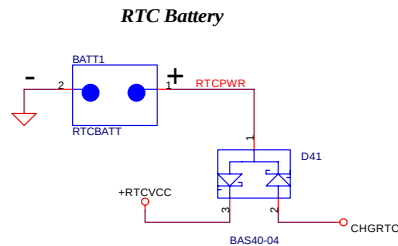
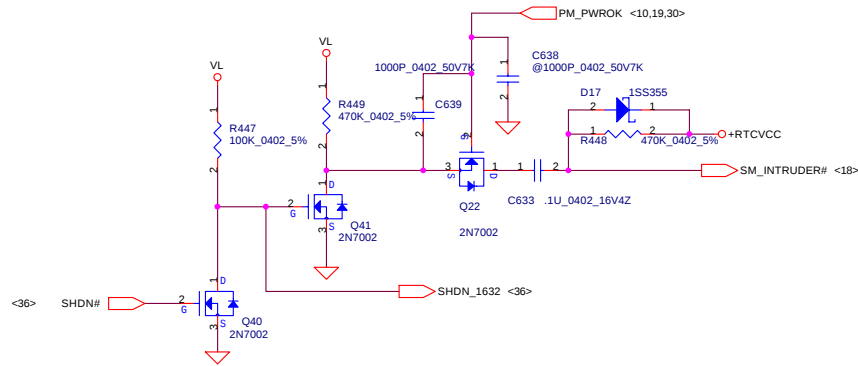
EC I2C Bus Address:
24C164: 1011xxx R/W#
24C16: 1010xxx R/W#



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EC Extend I/O KB Conn. & BIOS			
Title	Abacus/TangII LA-1452		
Size	Document Number	Sheet	Rev
	Monday, August 26, 2002	31 of 43	0.2

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LID Switch & Function Button

USB Over Current

USB PORT

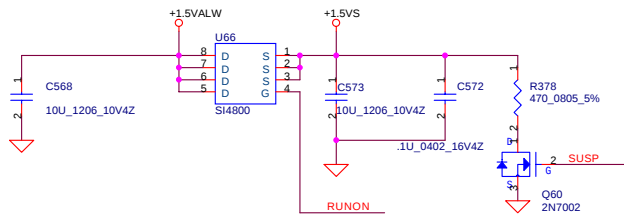
Note:
USB_AS=USB_BS=Trace width=40mils

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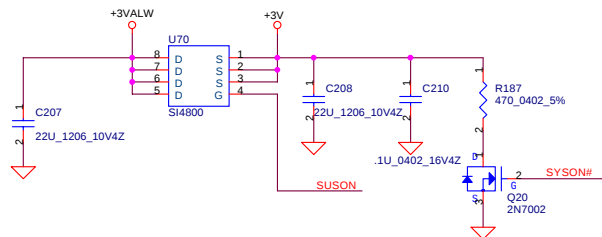
Compal Electronics, Inc.		
Title		
Power OK/Reset/RTC battery/USB Conn.& Lid Switch		
Size	Document Number	Rev
	Abacus/TangH LA-1452	0.2
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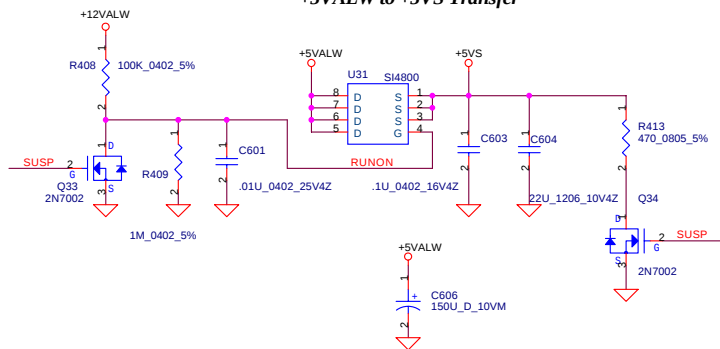
+1.5VALW to +1.5VS Transfer



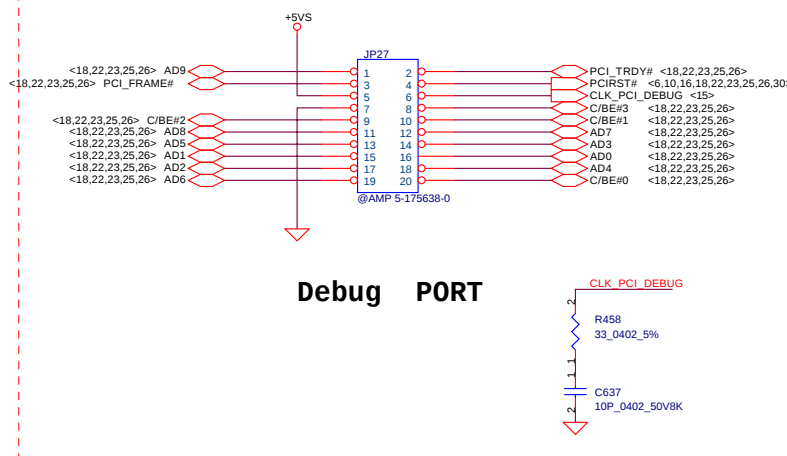
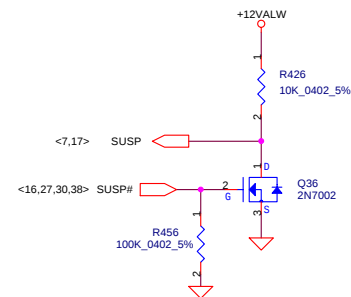
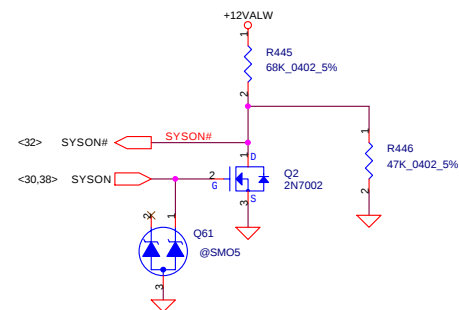
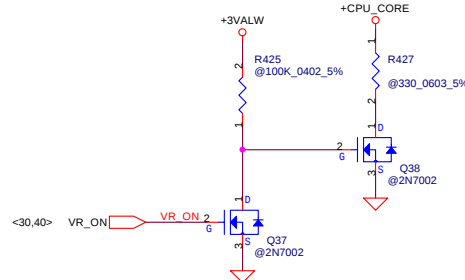
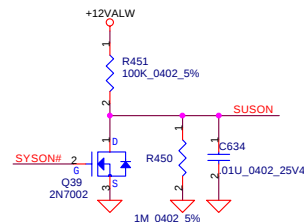
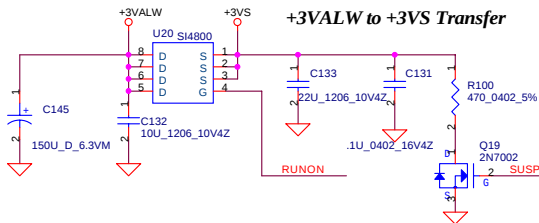
+3VALW to +3V Transfer



+5VALW to +5VS Transfer



+3VALW to +3VS Transfer

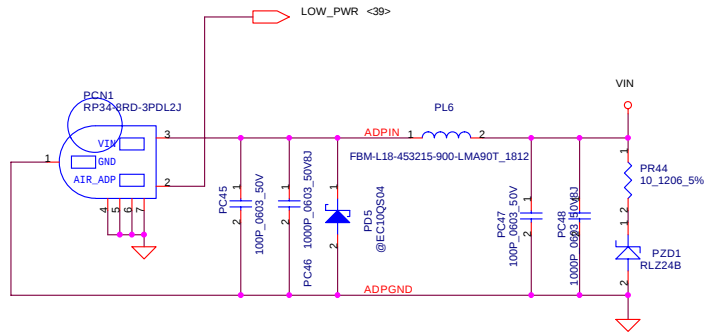


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DC/DC Circuit			
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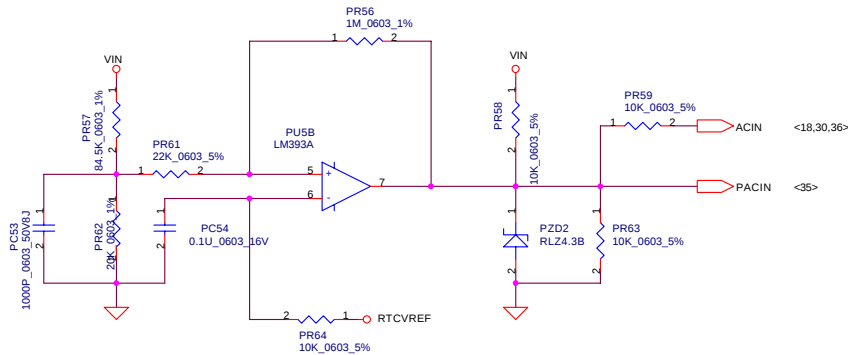
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PCN2 battery connector pin assignment

- SMART Battery:**
 1.BATT+
 2.BATT+
 3.9C/12C#/8C#
 4.B/I
 5.TS
 6.SMB_EC_DA1
 7.SMB_EC_CK1
 8.GND
 9.GND

Vin Detector
 17.90V/17.24V



Precharge detector
 15.9V/13.2V FOR
 ADAPTOR

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Detector			
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I_{adp}=0~4.10A(90W)
I_{adp}=0~3.20A(70W)
I_{air}=0~2.25A(Air)

IREF=0.82*I_{charge}
IREF=0~3.3V

Charge voltage
4S CC-CV MODE : 16.8V
VCHG is H
4S PULSE MODE : 17.4V
VCHG is L

OVP voltage :

LI-4S :18.0V----BATT-OVP=2.00V

LI-3S :13.5V----BATT-OVP=1.50V

BATT-OVP=0.2206*BATT++

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Charger

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+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

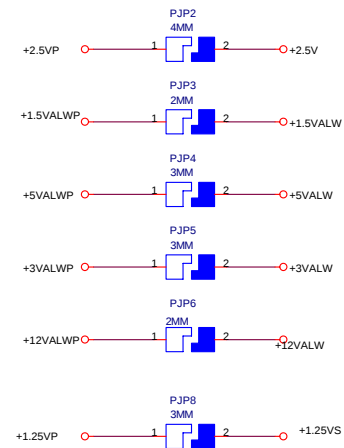
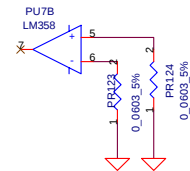
CPU thermal protection at 95 degree C
Recovery at 45 degree C

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Title			+3.3V/+5V/+12V	
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AL D	Title			
	+1.5VS			
	Size	Document Number		Rev
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+2.5V Ipeak =8.49A ~ 14.78A

+2.5V/+1.25V

DDR Termination Voltage

ISL6225

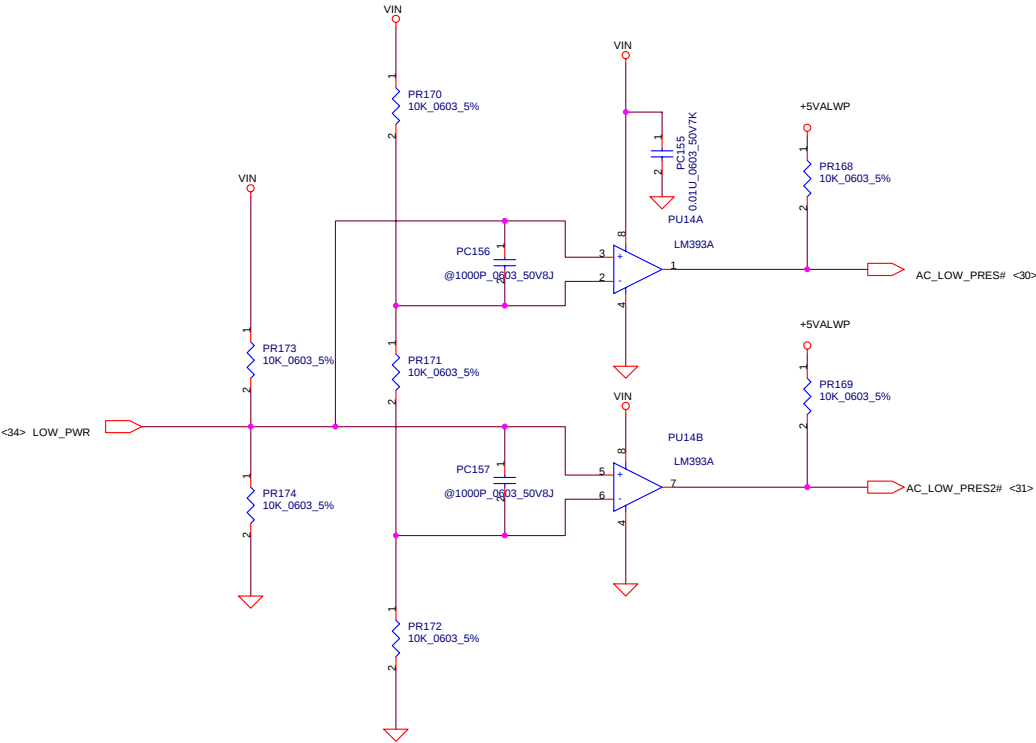
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Title		
DDR POWER 2.5V & 1.25V		
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AC Adapter Detector



AC Adapter	LOW_PWR	AC_LOW_PRES#	AC_LOW_PRES2#	IREF2
90W	0V	0	0	2.96V
70W	Float	0	1	2.31V
AIRLINE	20V	1	1	1.62V

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Title Adapter Detector			
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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	Fireware issue	The ICH4 GNTA# strap pull up for EC BIOS	0.1A	18	Depop R153, GNTA# have internal pull up	0.1	SST
2	Leakage current issue	Reduce Broadcom 4401L leakage current	0.1A	22	Depop L39 and pop L7, connector power source from +3VALW to +3V, R31, R32, R33 pull up to +3VAUXLAN	0.1	SST
3	Fix schematics part value	L21, L22, L23, L26 part value different with BOM	0.1B	15	Change L21, L22, L23, L26 part value from CH82012U121 to BLM21A601SPT on schematics	0.1	SST
4	BOM issue	R445 include wrong part number	0.1B	33	Change R445 part number from SD028470200 to SD028680200. PN indicate value from 47K_0402_5% to 68K_0402_5%	0.1	SST
5	HDD leakage current issue	When AC in +5VSHDD will go up to 5V	0.1C	21	Q6 change to S12302DS as schematics, S10EPWR active low when HDD power on	0.1	SST
6	Capture library package issue	2N7002 Drain is pin1, Source is pin3	0.1C	28	Fixed Q30, Q31, Q32 Capture libaray, pin1 fixed to pin3, pin3 fixed to pin1	0.1	SST
7	BOM issue	Fixed R196-R199 from 56.2K ohm to 56.2 ohm	0.1C	23	Change R196-R199 PN from SD014562207 to SD014562A00 on schematics	0.1	SST
8	Fix LOM EEPROM issue	U8 (AT93C46) is used X16 organization	0.1C	22	NC U8 pin6 for X16 organization select	0.1	SST
9	Fix CLKRUN# leakage issue	ICH4 not implement CLKRUN#, GPIO24 is resume power well.	0.1D	19	Add a diode D46 to isolate GPIO24 from ICH4 to PCI devices, and depop D46.	0.2	PT
10	LOM EEPROM issue	U8 (AT93C46) is used X16 organization. U8 pin6 pull up or NC for X16 organization select, pull down for X8 organization selcet.	0.1D	22	U8 pin6 pull up +3VAUXLAN via R452, and depop R452.	0.2	PT
11	SW BD LED keep turn on	SW BD LED control transistor emitter connect to +5VALW be keep LED always turn on	0.1D	32	Change JP5 pin9 from +5VALW to +3VS	0.2	PT
12	Fix VCCA_SM voltage drop issue	Add current rating for VCCA_SM, VCCA_DPLL, VCCA_FSB (1.5VS)	0.1E	10	Change L3, L4, L27, L28 from MLF2012DR68XT to FBM-L11-201209-121LMA05	0.2	PT
13	Change address and control signals layout topology	Change ddr address and control signal layout topology	0.1E	12,13	DDR address and control signals layout topology same the ddr data layout topology	0.2	PT
14	Fix EE issue item 89	Signal COMP/B and Y/G connect error	0.1E	17	Swap COMP/B and Y/G to correct connection	0.2	PT
15	Fix EE issue item 91	BEEP# from EC should be high active	0.1E	28	Change net name BEEP# to BEEP	0.2	PT
16	Fix EE issue item 92	Fix FSB 400MHz when 8456L pop	0.1E	15	Add R455 (8.2K_5%) pull down for H_BSEL0	0.2	PT
17	Fix EE issue item 95	When AC insertion SUSP# may be floating before the KBC can programit.	0.1E	33	Add R456 (100K_5%) pull down SUSP#	0.2	PT
18	Fix EE issue item 47	Provide enough current rating	0.1F	15	L22 and L26 change frome BLM21A601SPT (300mA) to FBM-L11-201209-121LMA05 (500mA) and depop L22	0.2	PT
19	Card Bus power bead current rating not enough	Provide enough current rating	0.1F	24	L5 and L6 change frome FBM-L11-160808-000LMT_0603 (300mA) to FBM-L11-201209-121LMA05 (500mA)	0.2	PT
20	Fix EE issue item 102	Fix Intel CPU FSB frequency issue	0.1F	10,15	H_SEL0 connect to R270 pin1 from CLK generator, H_BSEL0 connector to R270 pin2 from CPU. Depop R270 on GL board.	0.2	PT
21	Battery charge issue	ACIN pull up +3VALW can't change power supplier to battery when AC exit	0.1F	18	Depop R161	0.2	PT
22	NO	Change PCMCIA connector	0.1F	24	Change PCMCIA connector from AMP_0-1376275-1 to JAE_JC21-BRB	0.2	PT
23	Fix INTRUDER issue	ESD protect for Q22	0.1F	32	Add C638, C639 for Q22 protection	0.2	PT
24	Remove PS2 connector	No necessary	0.1G	29	Remove RP7, JP26	0.2	PT
25	Add debug port	PE board have not pop minipci connector, we need a port 80 debug tool	0.1G	33	Add R458, C637 and JP27	0.2	PT
27	For cost save	For cost save	0.1G	32	Depop C10, C229 (150U Poly Cap), add C641, C642 (100U Petit Cap)	0.2	PT
28	It no need	Use R19 pop and depop to control H_SEL0 high or low	0.1G	15	Remove R455	0.2	PT
29	Fix EE issue item 134	Change ddr address and control signal layout topology	0.1H	12,13	Change DDR address and control signal to go back SST topology	0.2	PT
30	Fix EE issue item 149	Pop Petit Cap after EA test	0.1H	32	Depop C641, C642 and pop C10, C229	0.2	PT
31	Fix EMI issue	EMI team's recommendation	0.1I	10	Pop R52, C79 for CLK_CLK_PCI_LAN; R428, C614 for CLK_PCI_MINI; R406, C597 for CLK_PCI_LPC; R321, C395 for CLK_ICH_66M	0.2	PT

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Title			P.I.R History
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	ADY13 LA-1271		0.2
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
32	Fix EE issue item 171	For CRT Hsync and Vsync to allow tuning	0.11	17	Add series resistors R459, R460 for Hsync and Vsync	0.2	PT
33	No	Schematic version change for PT build	0.2	ALL	Change revision from 0.11 to 0.2	0.2	PT

Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	CPU_CORE can't power up	Pin7 of PU16 can't be used as on/off control pin	0.1B	40	1. Change VCC power source of PU16 from +5VALWP to +5VS	0.1	SST
2	current limited is not up to 60A	Current limited is about 37A while PH6,PH7,PH8 is 1.5K that is not enough for design target.Because we don't use PTC resistor on PCB now, the value must be tuned later.	0.1B	40	1. Change PH6,PH7,PH8 from 1.5K_0603_5% to 3K_0603_1%	0.1	SST
3	Turn on voltage of PQ19 is not enough	Vgs of PQ19 is 2V while PR72 is 47K. That is not enough. While PR72 is 22K, the Vgs can be improved to 2.5V.	0.1B	35	1. Change PR72 from 47K_0402_5% to 22K_0402_5%	0.1	SST
4	current rating is not enough.	FBM-L11-322513-151LMAT is 5A that is not enough.So FBM-L18-453215-900LMA90T1812 is 9A that is better.	0.1B	35	1. Change PL8 from FBM-L11-322513-151LMAT to FBM-L18-453215-900LMA90T1812.	0.2	PT
5	Fix noise issue	On SST PCB, we can sound some noise due to PC77, the cernamic capacitor has sounded noise with thinner type.	0.1C	36	1. Change PC77 from 2.2U_1206_25V to 4.7U_1210_25V	0.2	PT
6	Fix CPU_CORE Transient Response fail	The transient response is too slow. We must to tune feedback resistor and capacitor to fix it.	0.1E	40	1. Change PR249 from 3.48K_0603_1% to 5.76K_0603_1%. 2. Change PR257 from 49.9_0603_1% to 1.1K_0603_1% 3. Populate PC172 68PF_0603_50V.	0.2	PT
7	SDREF output voltage is over spec.	Add bypass capacitor pallel pin18 of ISL6225	0.1E	38	Populate PC218 470P_0603_50V7K	0.2	PT
8	PG of CM28423 has a glitch while VCC is ready and VR_ON is float	Add pulldown resistor tie to GND while VR_ON is float that can be made sure the logic is low.	0.1E	40	Add PR301 100K_0603_1%	0.2	PT
9	Change VCC power source of PU15, PU17, PU19 from +5VALWP to +5VS	Negative voltage was observed on +5VALWP when system powered off	0.1E	40	1. Change VCC power source of PU15, PU17, PU19 from +5VALWP to +5VS	0.2	PT
10	Prevent abnormal function OVP caused by ISL6219 while system powerwd off ; bouble pulses was observed at output PW1, PW2, PWM3 of ISL6219	ISL6219 caused OVP when on/off pin changed from high to low level	0.1E	40	1. Add PQ82 2N7002 2. Change PR232 from 5.1_0603_5% to 10K_0603_5% 3. Change PC168 from 1U_0805_25V to 0.01U_0603_50V. 4. Depop PR251, PR270, PC183, PC194 5. Tie the EN pin of PU15, PU17, PU19 to Pin1 of PQ82	0.2	PT
11	Fine-tune current sharing of CPU VR phase1,2,3 to have thermal balance	uneven current sharing found	0.1E	40	1. Change PH6, PH7, PH8 form 3K_0603_1% to 0_0603_5% 2. Change PR245 from 0_0603_5% to 1.96K_0603_1% 3. Change PR263 from 0_0603_5% to 1.43K_0603_1%. 4. Change PR276 from 0_0603_5% to 1.5K_0603_1%	0.2	PT
12	Fine-tune CPU load-line with NTC	Fine-tune CPU load-line with NTC	0.1E	40	1. Keep PR268 nonpop 2. Change PR256 from 2K_0603_1% to 1.74K_0603_1% 3. Change PR297 from 0_0603_5% to 1.15K_0603_1%. 4. Change PH5from depop to 4.7K_0603_1% 5. Change PR298 from depop to 681_0603_1% 6. Change PR257 from 49.9_0603_1% to 909_0603_1% 7. Change PC179 from 3900P_0603_50V to 5.6N_0603_50V 8. Change PR249 from 3.48K_0603_5% to 7.5K_0603_1% 7. Change PC171 from 6800P_0603_50V to 5.6N_0603_50V 8. Change PC172 from depop to 47P_0603_50V	0.2	PT
13	Audio noise found	Still find root cause	0.1E	35, 36, 40	1. reserve 15U_D_25V capacitors on PC226-PC235,	0.2	PT
14	PC212 location space change	requested by ME to put a connector around	0.1E	38	1. change the size of PC212 from D size to 0805 and pop 4.7U_0805_10V	0.2	PT

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