Compal Confidential

Schematic Document

Crestline_GM/PM+NB8M-GS & ICH8M

2007 / 1 / 2 Rev:0.4

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: *Cover Sheet*

Size: Custom | Document Number: *LA-4121P* | Rev: 0.4

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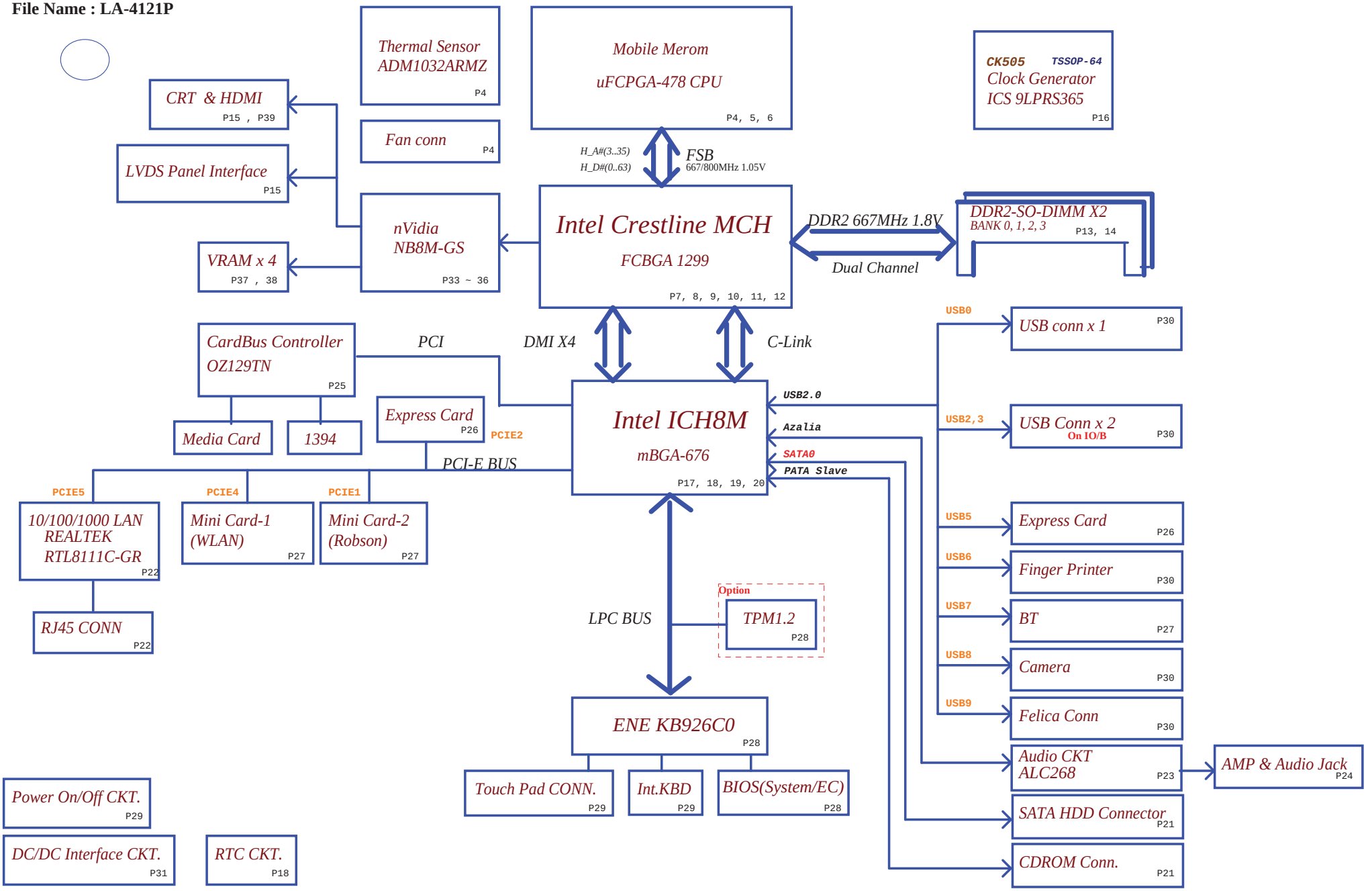
Project Code: ANRJAL3000 (JAL30)

File Name : LA-4121P

JAL30 UMA/Discrete



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Title: **Block Diagram**

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Voltage Rails

O MEANS ON X MEANS OFF

State \ Power plane	+B	+3VALW		+5VS +3VS +1.8VS +1.25VS +CPU_CORE +VCCP	CLOCK
	O	O	O	O	O
S3	O	O		X	O
	O		X	X	O
S5 S4/ Battery only	O	X	X	X	X
	X	X	X	X	X

O MEANS ON
X MEANS OFF

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra / Rc	100K +/- 5%

Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD21	0	PIRQE/PIRQF/PIRQG

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b?
EEPROM(24C16/02)	1010 000X b?
(24C04)	1011 000Xb?

EC SM Bus2 address

Device	Address
ADM1032	4D

ICH7 SM Bus address

Device	Address
Clock Generator (ICS ICS9LPR310)	1101 001Xb?
DDRII DIMM0	1001 000Xb?
DDRII DIMM2	1001 010Xb?

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure

Title	Notes		
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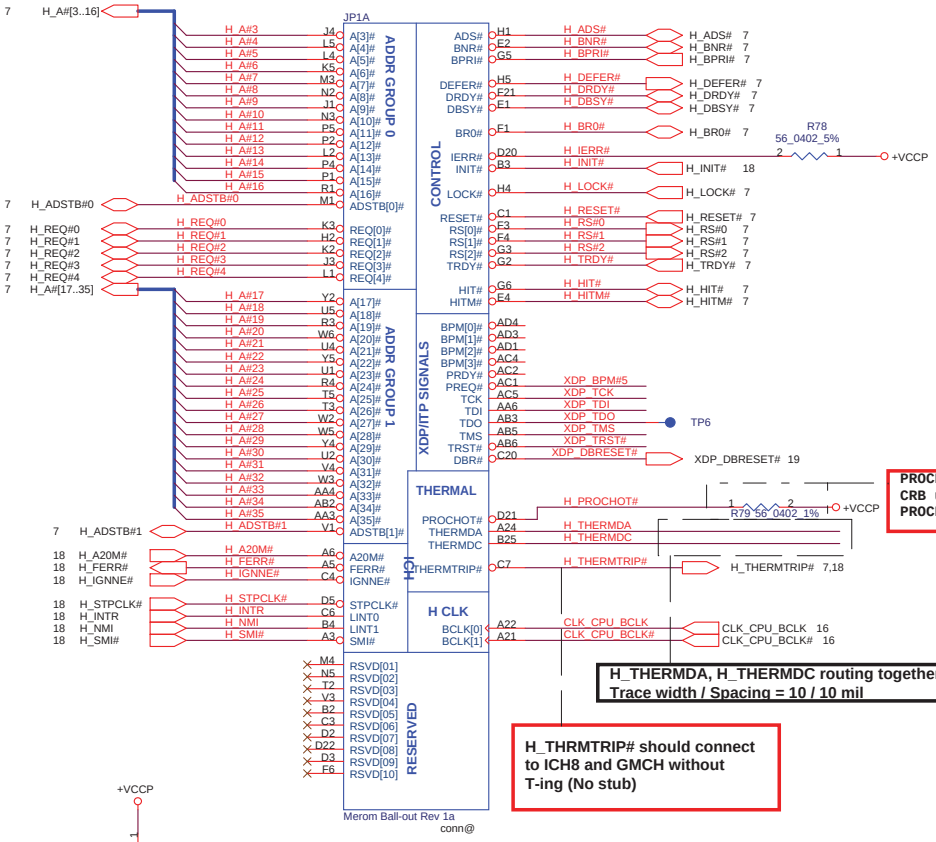
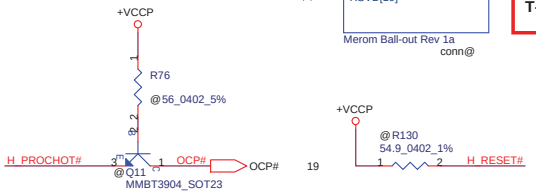


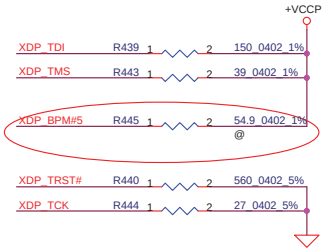
PROCHOT# is not used ---> 56 ohms pull-up
CRB uses 1K ohms pull-up resistor to fix
PROCHOT# failure when driven by a thermal sensor.

H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

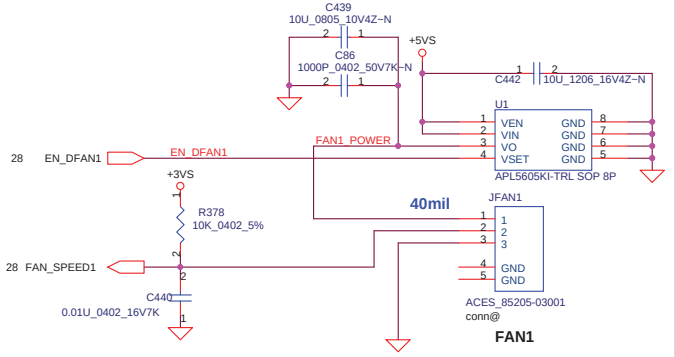
H_THRMTRIP# should connect
to ICH8 and GMCH without
T-ing (No stub)



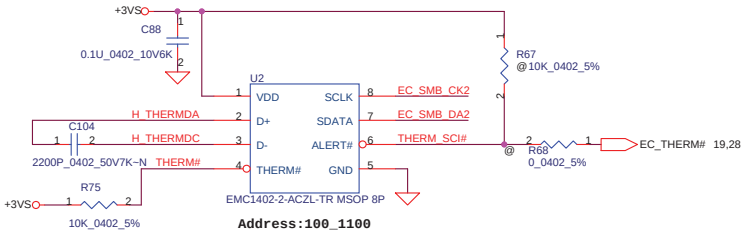
XDP Reserve



FAN1 Control and Tachometer



Thermal Sensor EMC1402-2-ACZL-TR



Address:100_1100

28,29,34 EC_SMB_CK2 EC_SMB_CK2
28,29,34 EC_SMB_DA2 EC_SMB_DA2

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Title: Merom(1/3)-AGTL+/XDP

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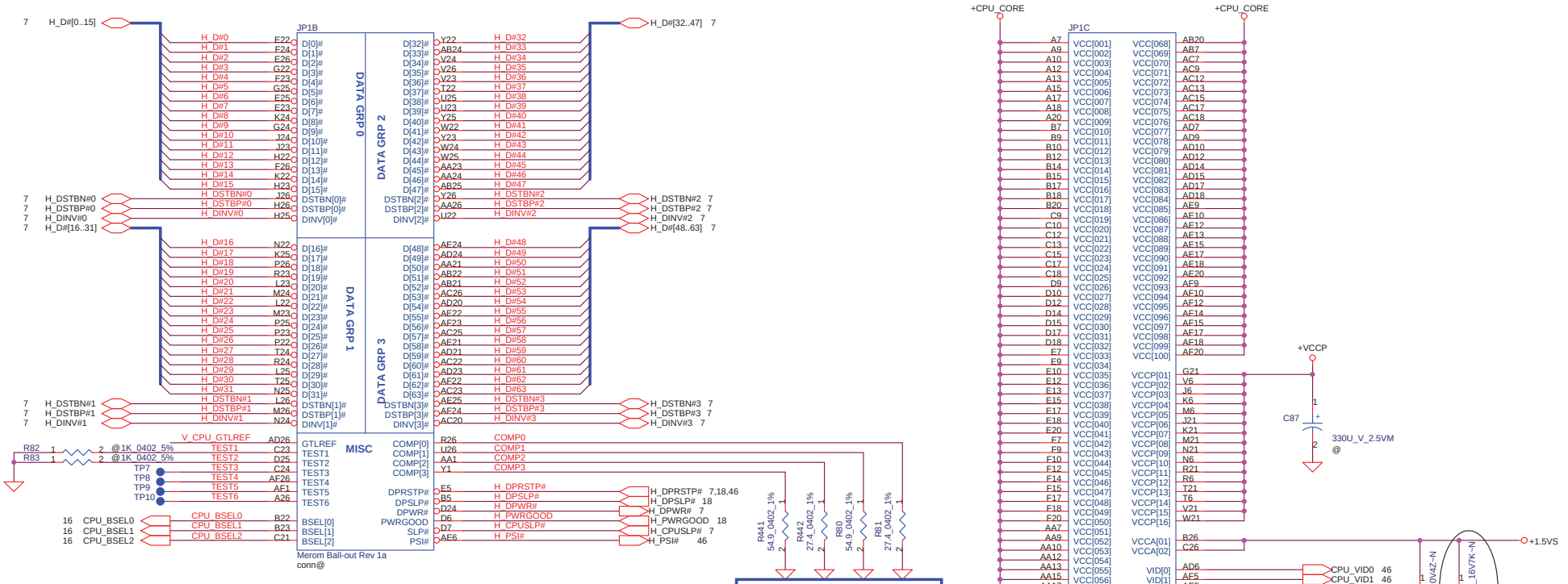
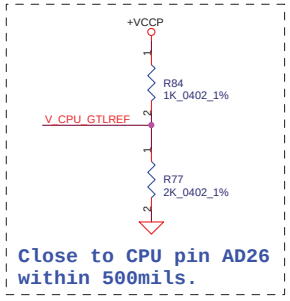


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

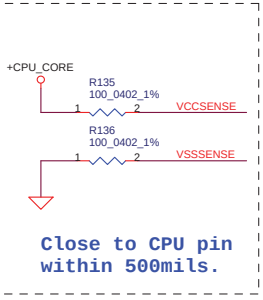
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal.
COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Close to CPU pin AD26 within 500mils.

Near pin B26

Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

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Compal Electronics, Inc.

Title: Merom(2/3)-AGTL+/PWR

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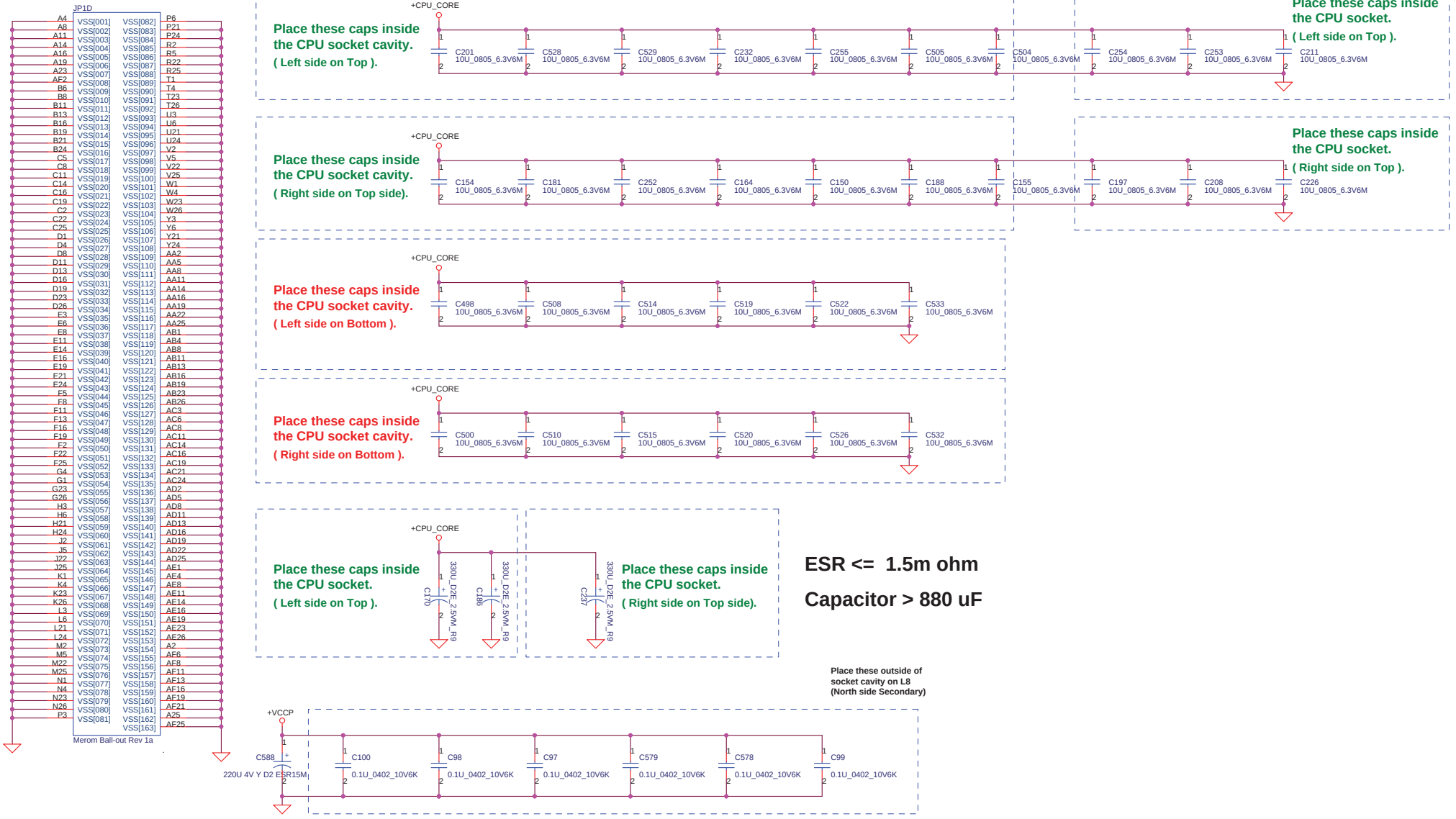
High Frequence Decoupling

10uF 0805 X5R -> 85 degree.



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Compal Electronics, Inc.

Title: **Merom(3/3)-GND&Bypass**

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layout note:

Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

within 100 mils from NB

Near B3 pin

Layout Note:
+DDR_MCH_REF
trace width and spacing is 20/20.

close to NB

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Compal Electronics, Inc.

Title: **CRESTLINE(1/6)-AGTL+/DMI/DDR2**

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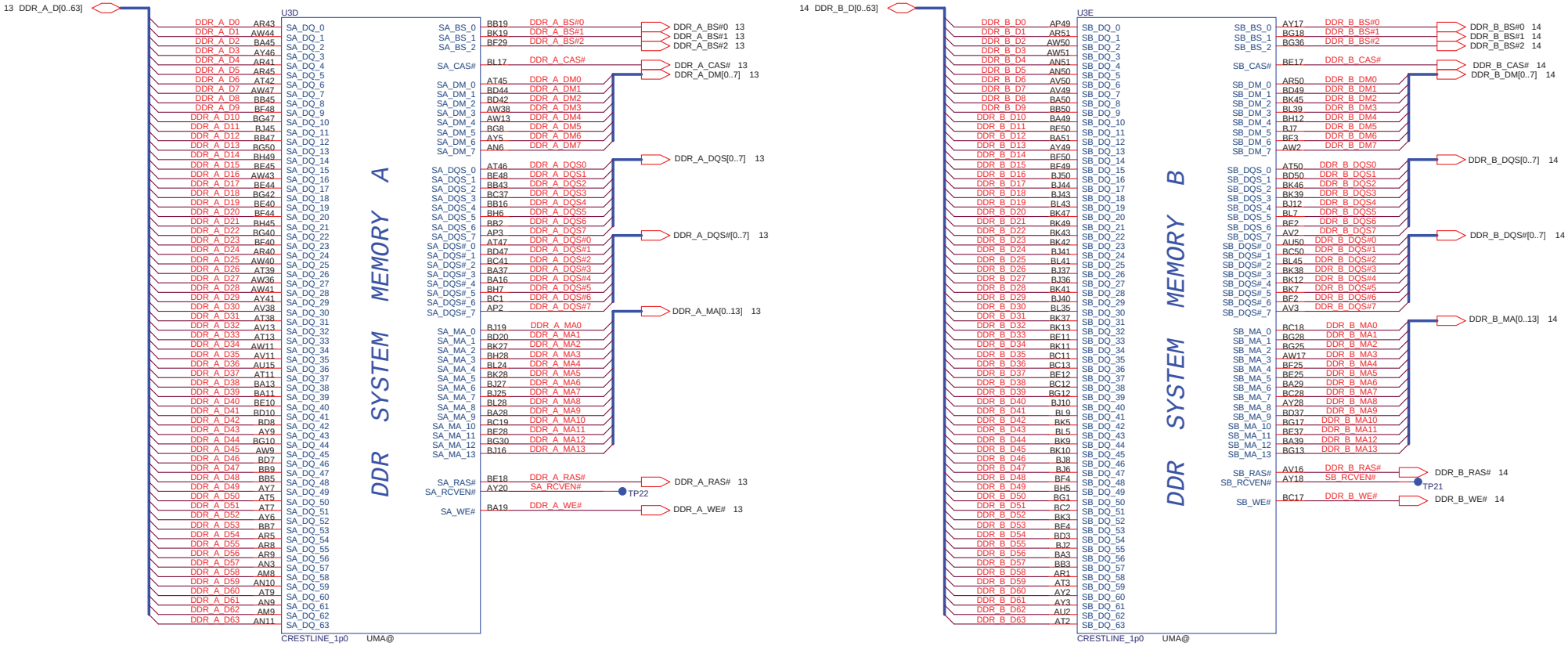

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Compal Electronics, Inc.

Title: **CRESTLINE(2/6)-DDR2 A/B CH**

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For Crestline:2.4kohm
For Calero: 1.5Kohm

PEGCOMP trace width
and spacing is 20/25 mils.

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

For Crestline:1.3kohm
For Calero: 255ohm

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

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Title: CRESTLINE(3/6)-VGA/LVDS/TV

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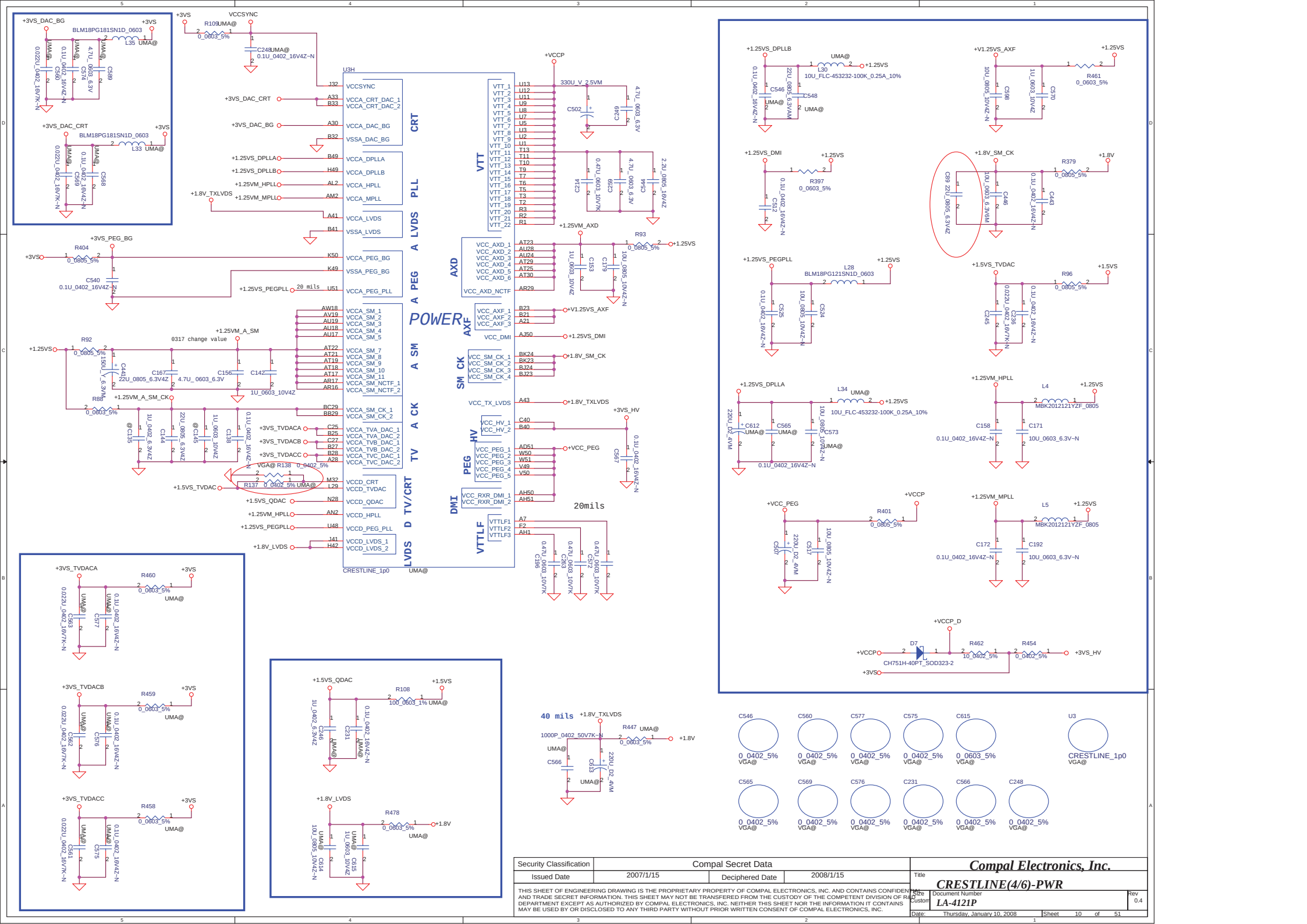

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Title: **CRESTLINE(4/6)-PWR**

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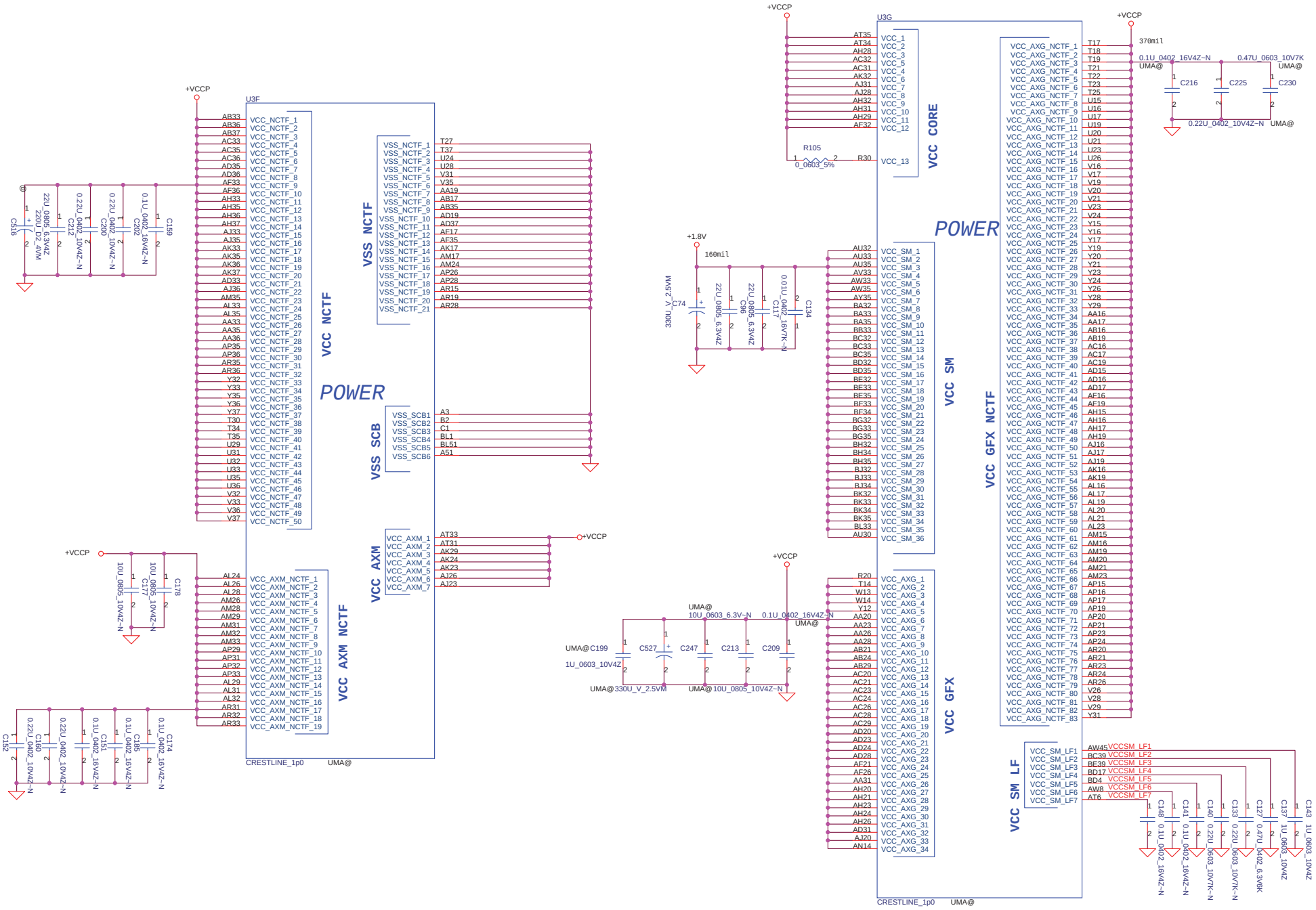

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **CRESTLINE(5/6)-PWR/GND**

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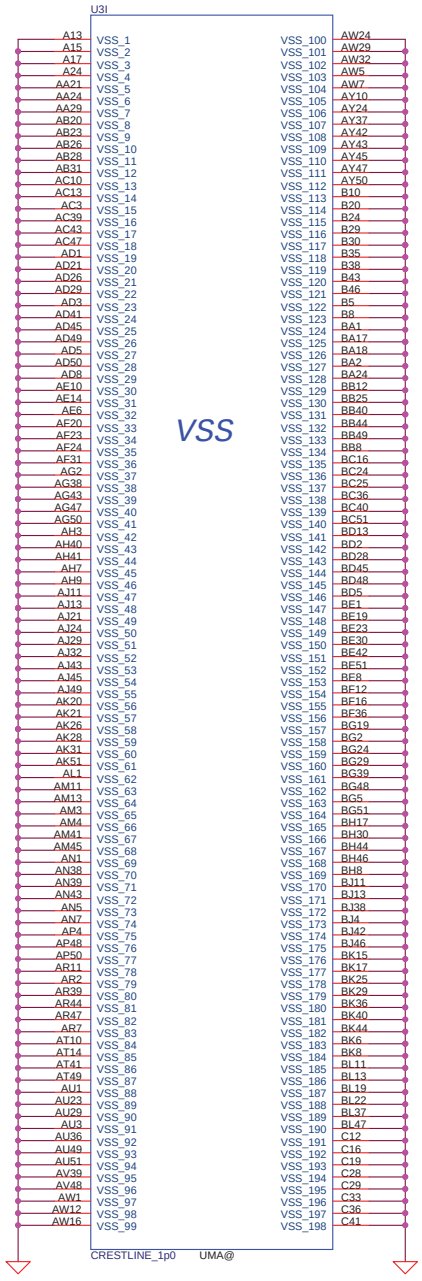

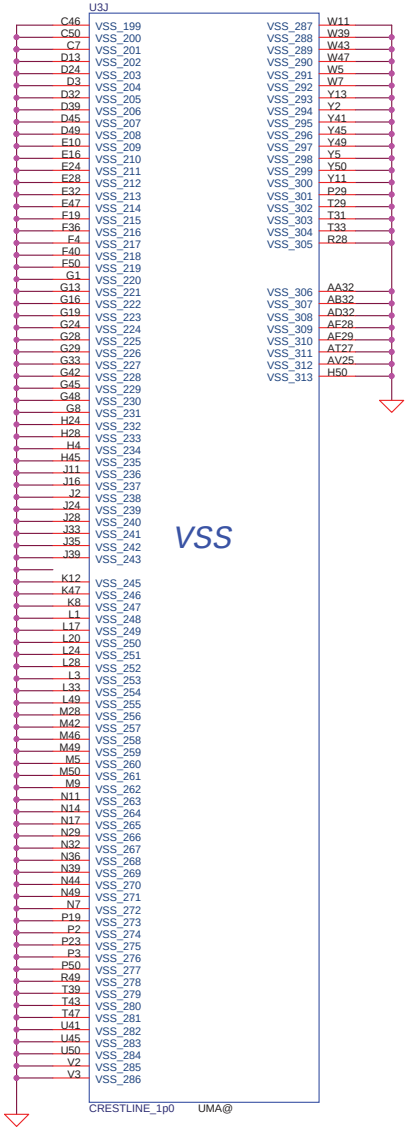

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Title: **CRESTLINE(6/6)-PWR/GND**

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Close to VREF pins of SO-DIMM

Layout Note:
+DDR_MCH_REF trace width and spacing is 20/20.

Layout Note:
Place near JDIM1

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

Layout Note:
Place these resistor closely JP41,all trace length Max=1.5"

close to connector

JDIM1

FOX_ASOA426-M2RN-7F

SO-DIMM A
REVERSE
Bottom side

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Compal Electronics, Inc.

Title: DDR2 SO-DIMM I

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8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]

Layout Note:
Place near JDIM2

+1.8V
2.2U_0603_6.3V6K C25, C28, C29, C27, C24
0.1U_0402_16V4Z C57, C42, C26, C56
330U_D2E_2.5VM_R7 C79 @

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS
DDR_B_V
0.1U_0402_16V4Z C33, C32, C30, C44, C36, C46, C31, C37, C45, C41, C40, C34, C35

Layout Note:
Place these resistor closely JP42,all trace length Max=1.5"

DDR_B_V
RP14: DDR_B_MA14, DDR_B_MA11 / RP6: DDR_B_MA7, DDR_B_MA9
RP12: DDR_B_MA8, DDR_B_MA5 / RP5: DDR_B_MA3, DDR_B_MA1
RP3: DDR_B_RAS#, DDR_B_BS#1 / RP13: DDR_B_MA12, DDR_B_MA6
RP9: DDR_B_CAS#, DDR_CS2_DIMMB# / RP4: DDR_B_MA0, DDR_B_MA4
RP10: DDR_B_WE#, DDR_B_BS#0 / RP11: DDR_B_MA2, DDR_B_MA10
RP8: DDR_CS3_DIMMB#, M_ODT3 / RP2: M_ODT2, DDR_B_MA13
RP7: DDR_CKE2_DIMMB, DDR_B_BS#2
DDR_CKE3_DIMMB 1 — R49 56_0402_5% — 2
56_0404_4P2R_5%

Close to VREF pins of SO-DIMM

+1.8V
+DDR_MCH_REF1 — +DDR_MCH_REF1 13
2.2U_0805_16V4Z C39, 0.1U_0402_16V4Z C49

JDIM2

	VREF	1	2	VSS	
	VSS	3	4	DQ4	DDR_B_D5
DDR_B_D0	DQ0	5	6	DQ5	DDR_B_D4
DDR_B_D1	DQ1	7	8	VSS	
	VSS	9	10	DM0	DDR_B_DM0
DDR_B_DQS#0	DQS0#	11	12	VSS	
DDR_B_DQS0	DQS0	13	14	DQ6	DDR_B_D6
	VSS	15	16	DQ7	DDR_B_D7
DDR_B_D2	DQ2	17	18	VSS	
DDR_B_D3	DQ3	19	20	DQ12	DDR_B_D12
	VSS	21	22	DQ13	DDR_B_D13
DDR_B_D8	DQ8	23	24	VSS	
DDR_B_D9	DQ9	25	26	DM1	DDR_B_DM1
	VSS	27	28	VSS	
DDR_B_DQS#1	DQS1#	29	30	CK0	M_CLK_DDR2 7
DDR_B_DQS1	DQS1	31	32	CK0#	M_CLK_DDR#2 7
	VSS	33	34	VSS	
DDR_B_D10	DQ10	35	36	DQ14	DDR_B_D14
DDR_B_D11	DQ11	37	38	DQ15	DDR_B_D15
	VSS	39	40	VSS	
	VSS	41	42	VSS	
DDR_B_D17	DQ16	43	44	DQ20	DDR_B_D21
DDR_B_D20	DQ17	45	46	DQ21	DDR_B_D16
	VSS	47	48	VSS	
DDR_B_DQS#2	DQS2#	49	50	NC	PM_EXTTS#1 7
DDR_B_DQS2	DQS2	51	52	DM2	DDR_B_DM2
	VSS	53	54	VSS	
DDR_B_D18	DQ18	55	56	DQ22	DDR_B_D22
DDR_B_D19	DQ19	57	58	DQ23	DDR_B_D23
	VSS	59	60	VSS	
DDR_B_D28	DQ24	61	62	DQ28	DDR_B_D26
DDR_B_D25	DQ25	63	64	DQ29	DDR_B_D24
	VSS	65	66	VSS	
DDR_B_DM3	DM3	67	68	DQS3#	DDR_B_DQS#3
	NC	69	70	DQS3	DDR_B_DQS3
	VSS	71	72	VSS	
DDR_B_D30	DQ26	73	74	DQ30	DDR_B_D29
DDR_B_D31	DQ27	75	76	DQ31	DDR_B_D27
	VSS	77	78	VSS	
7 DDR_CKE2_DIMMB	DDR_CKE2_DIMMB	CKE0	79	80	NC/CKE1	DDR_CKE3_DIMMB	DDR_CKE3_DIMMB 7
	VDD	81	82	VDD	
	NC	83	84	NC/A15	
8 DDR_B_BS#2	DDR_B_BS#2	BA2	85	86	NC/A14	DDR_B_MA14	DDR_B_MA14 7
	VDD	87	88	VDD	
DDR_B_MA12	A12	89	90	A11	DDR_B_MA11
DDR_B_MA9	A9	91	92	A7	DDR_B_MA7
DDR_B_MA8	A8	93	94	A6	DDR_B_MA6
	VDD	95	96	VDD	
DDR_B_MA5	A5	97	98	A4	DDR_B_MA4
DDR_B_MA3	A3	99	100	A2	DDR_B_MA2
DDR_B_MA1	A1	101	102	A0	DDR_B_MA0
	VDD	103	104	VDD	
DDR_B_MA10	A10/AP	105	106	BA1	DDR_B_BS#1	DDR_B_BS#1 8
8 DDR_B_BS#0 DDR_B_BS#0	BA0	107	108	RAS#	DDR_B_RAS#	DDR_B_RAS# 8
8 DDR_B_WE#	WE#	109	110	S0#	DDR_CS2_DIMMB#	DDR_CS2_DIMMB# 7
	VDD	111	112	VDD	
8 DDR_B_CAS# DDR_B_CAS#	CAS#	113	114	ODT0	M_ODT2	M_ODT2 7
7 DDR_CS3_DIMMB# DDR_CS3_DIMMB#	NC/S1#	115	116	NC/A13	DDR_B_MA13	DDR_B_MA13
	VDD	117	118	VDD	
7 M_ODT3 M_ODT3	NC/ODT1	119	120	NC	
	VSS	121	122	VSS	
DDR_B_D32	DQ32	123	124	DQ36	DDR_B_D36
DDR_B_D33	DQ33	125	126	DQ37	DDR_B_D37
	VSS	127	128	VSS	
DDR_B_DQS#4	DQS4#	129	130	DM4	DDR_B_DM4
DDR_B_DQS4	DQS4	131	132	VSS	
	VSS	133	134	DQ38	DDR_B_D39
DDR_B_D34	DQ34	135	136	DQ39	DDR_B_D38
DDR_B_D35	DQ35	137	138	VSS	
	VSS	139	140	DQ44	DDR_B_D44
DDR_B_D40	DQ40	141	142	DQ45	DDR_B_D45
DDR_B_D41	DQ41	143	144	VSS	
	VSS	145	146	DQS5#	DDR_B_DQS#5
DDR_B_DM5	DM5	147	148	DQS5	DDR_B_DQS5
	VSS	149	150	VSS	
DDR_B_D42	DQ42	151	152	DQ46	DDR_B_D46
DDR_B_D43	DQ43	153	154	DQ47	DDR_B_D47
	VSS	155	156	VSS	
DDR_B_D48	DQ48	157	158	DQ52	DDR_B_D52
DDR_B_D49	DQ49	159	160	DQ53	DDR_B_D53
	VSS	161	162	VSS	
	NC,TEST	163	164	CK1	M_CLK_DDR3	M_CLK_DDR3 7
	VSS	165	166	CK1#	M_CLK_DDR#3	M_CLK_DDR#3 7
DDR_B_DQS#6	DQS6#	167	168	VSS	
DDR_B_DQS6	DQS6	169	170	DM6	DDR_B_DM6
	VSS	171	172	VSS	
DDR_B_D51	DQ50	173	174	DQ54	DDR_B_D54
DDR_B_D50	DQ51	175	176	DQ55	DDR_B_D55
	VSS	177	178	VSS	
DDR_B_D56	DQ56	179	180	DQ60	DDR_B_D60
DDR_B_D61	DQ57	181	182	DQ61	DDR_B_D57
	VSS	183	184	VSS	
DDR_B_DM7	DM7	185	186	DQS7#	DDR_B_DQS#7
	VSS	187	188	DQS7	DDR_B_DQS7
DDR_B_D59	DQ58	189	190	VSS	
DDR_B_D58	DQ59	191	192	DQ62	DDR_B_D62
	VSS	193	194	DQ63	DDR_B_D63
13,16,19 ICH_SM_DA	SDA	195	196	VSS	
13,16,19 ICH_SM_CLK	SCL	197	198	SAO	
+3VS	VDDSPD	199	200	SA1	R44 1 — 2 — +3VS 10K_0402_5%

FOX_AS0A426-NARN-7F-N

C43 0.1U_0402_16V4Z, C38 2.2U_0603_6.3V6K
R45 10K_0402_5%

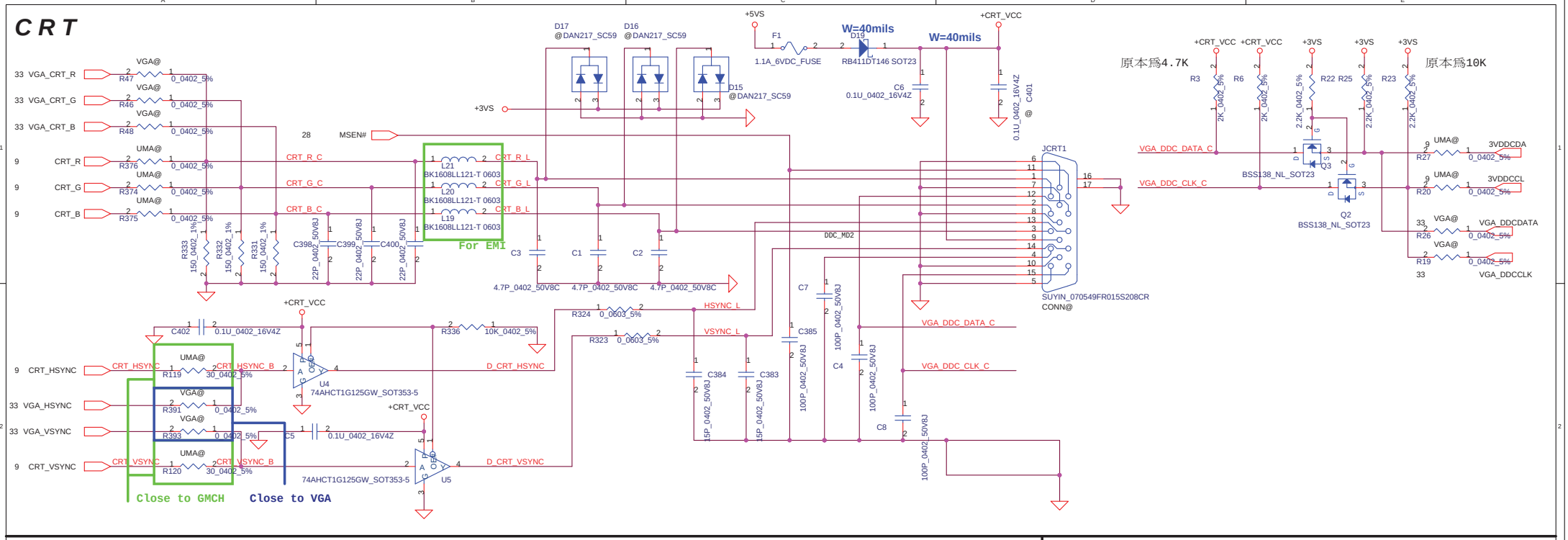
SO-DIMM B
REVERSE
Bottom side

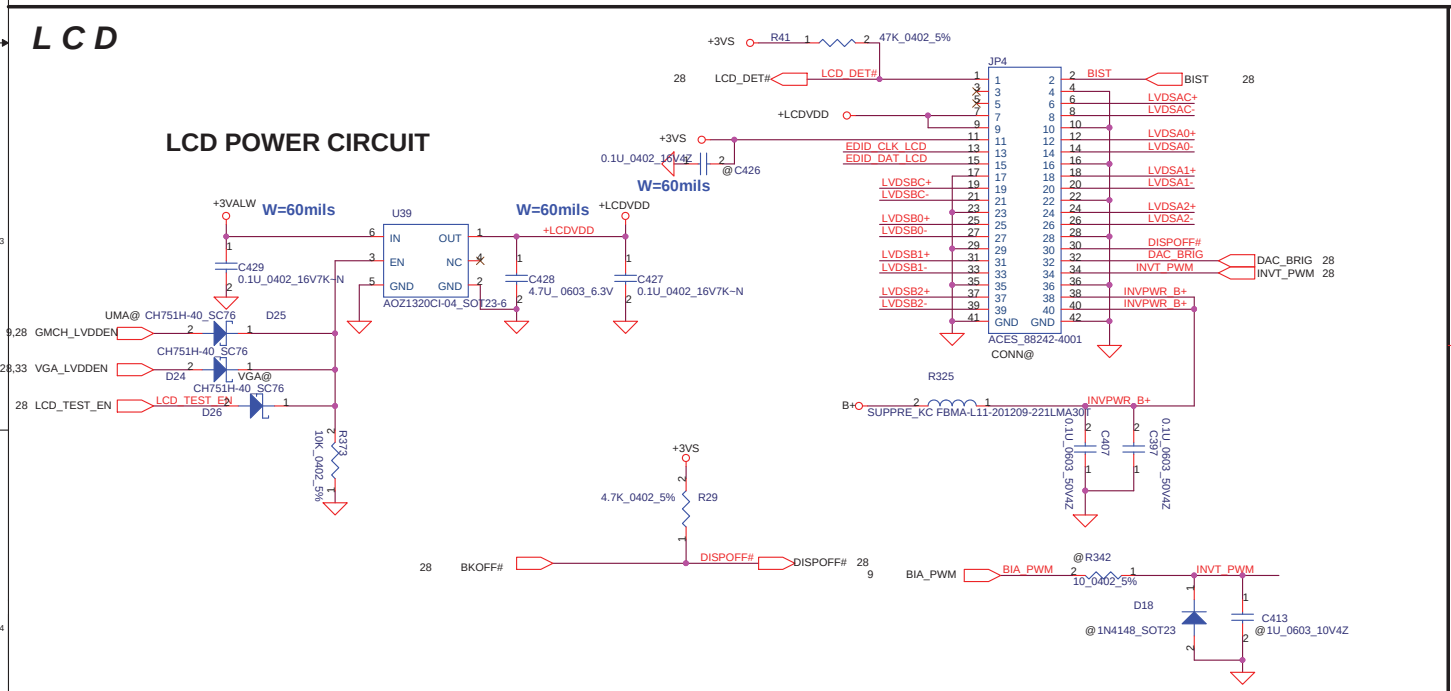
Compal Electronics, Inc.

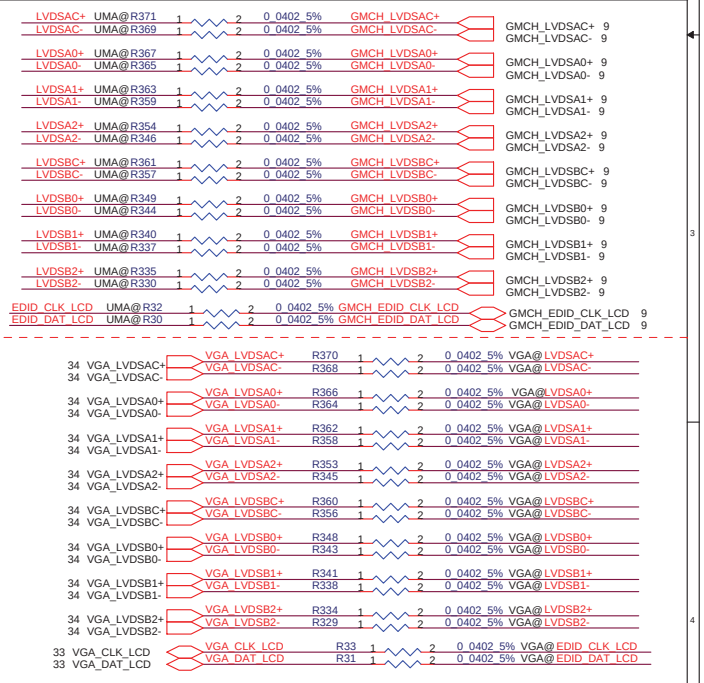
Title: **DDR2 SO-DIMM II**

Size	Document Number	Rev
Custom	LA-4121P	0.4

Date: Thursday, January 10, 2008 | Sheet 14 of 51







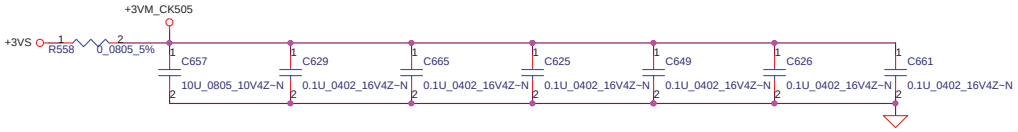
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

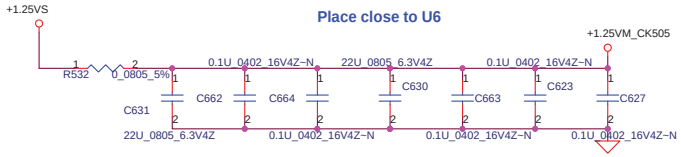
Compal Electronics, Inc.	
Title	CRT CONN/LCD CONN
Size: Custom	Document Number: LA-4121P
Rev	0.4
Date: Thursday, January 10, 2008	Sheet 15 of 51

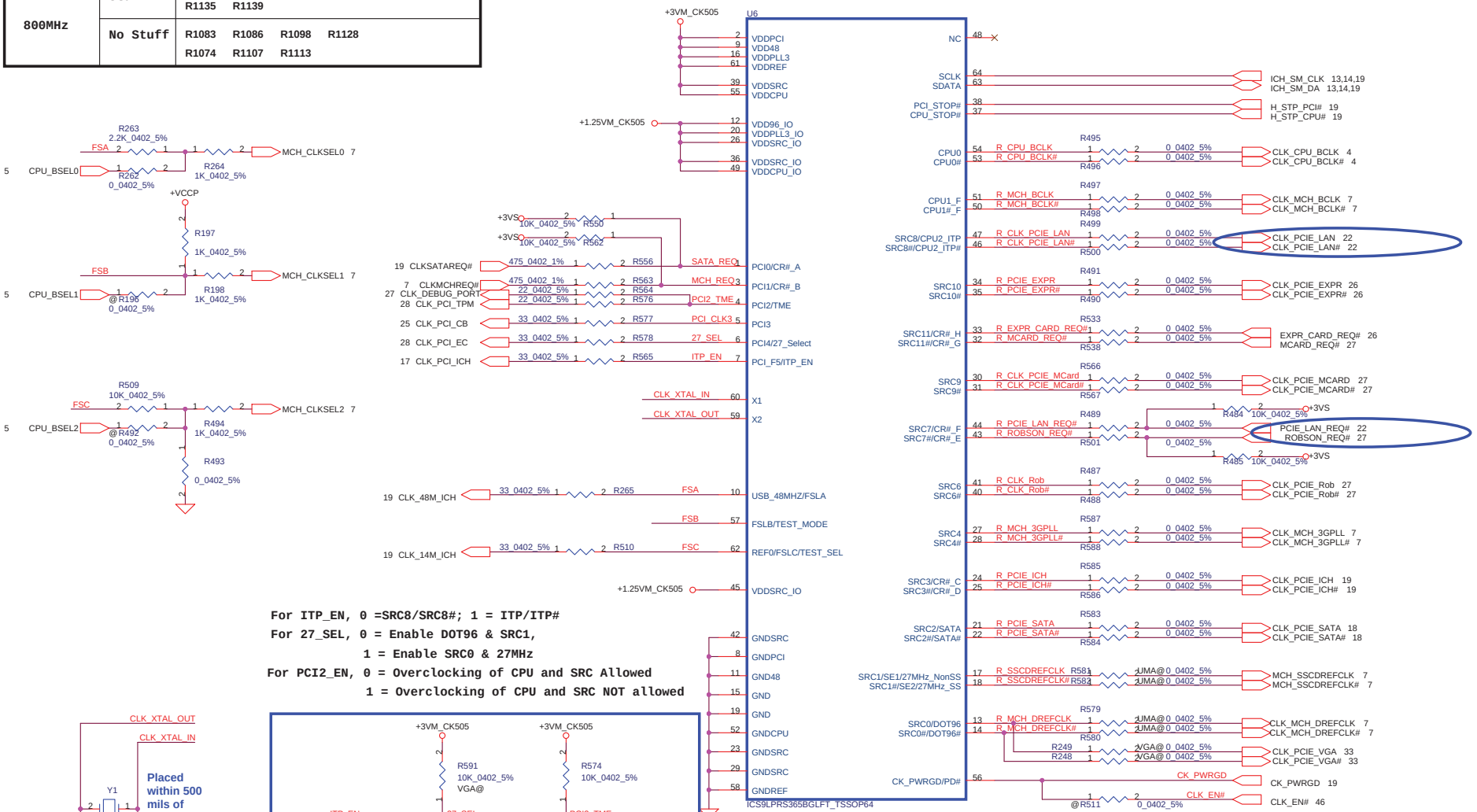
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

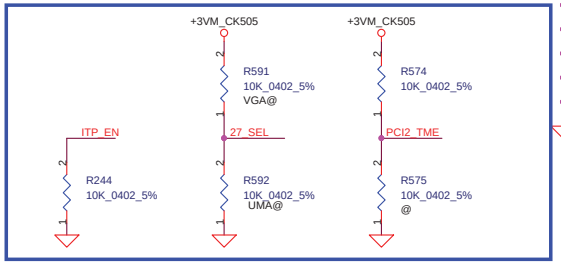
FSB Frequency Selet:

CPU Driven	Stuff	R1107	R1135	R1083			
*(Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139
667MHz	Stuff	R1086	R1139	R1135	R1074	R1139	R1135
	No Stuff	R1083	R1107	R1128			
		R1113	R1098				
800MHz	Stuff	R1135	R1139				
	No Stuff	R1083	R1086	R1098	R1128		
		R1074	R1107	R1113			









For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1 = Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

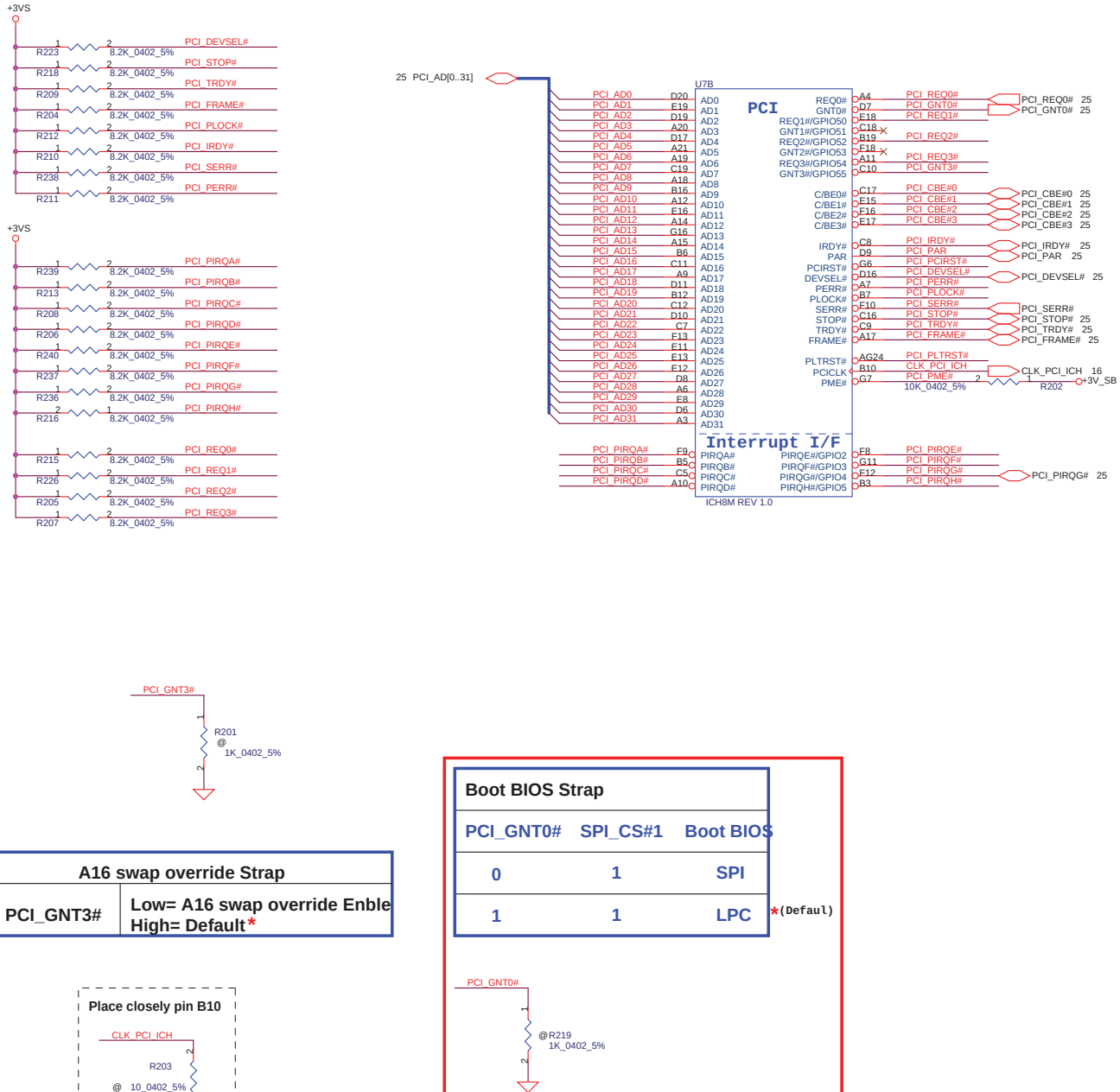
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: Clock Generator

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 16 of 51



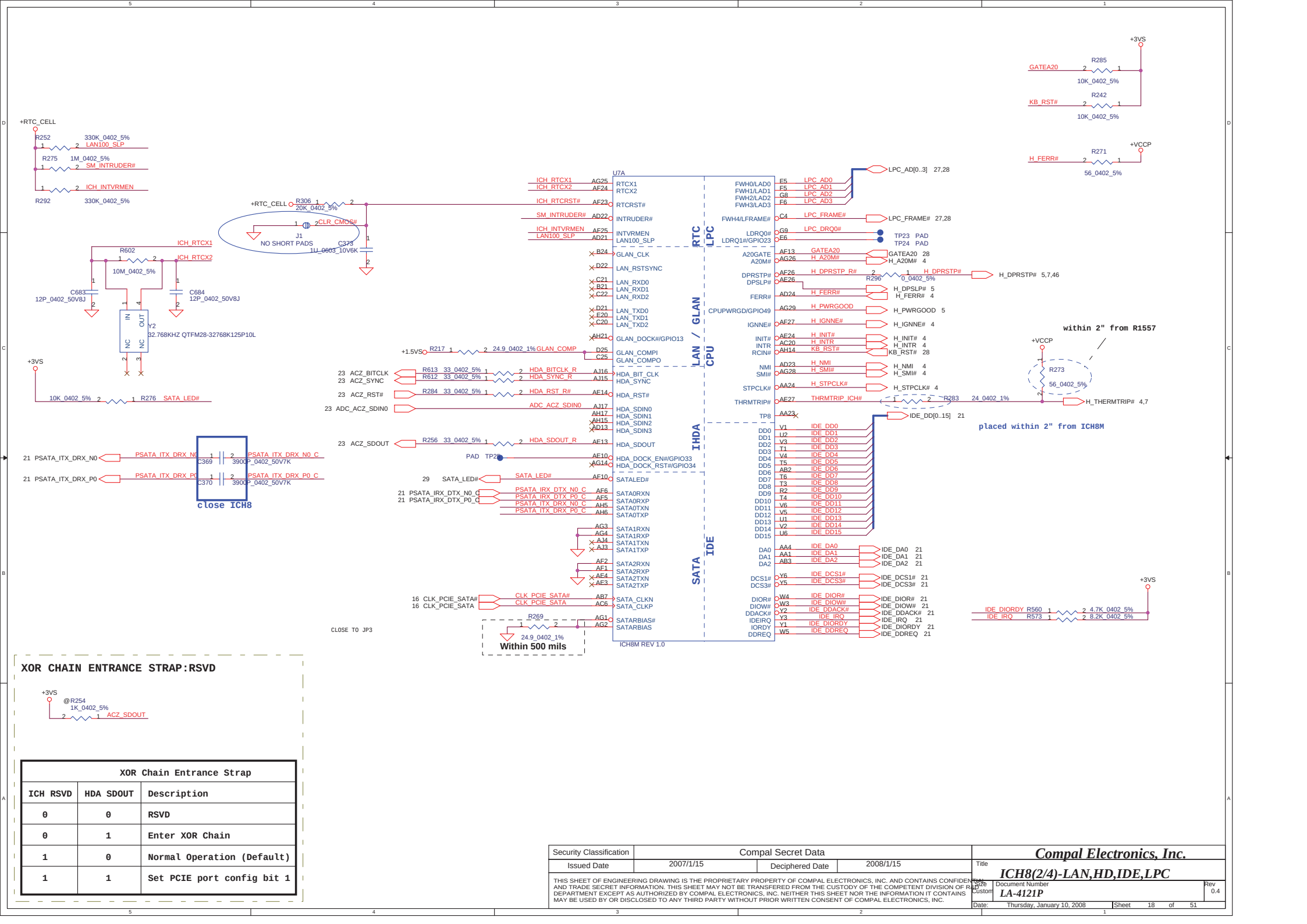
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: ICH8(1/4)-PCI/INT

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 17 of 51


+RTC_CELL
R252 330K_0402_5%
LAN100_SLP
R275 1M_0402_5%
SM_INTRUDER#
ICH_INTVRMEN
R292 330K_0402_5%
R306 20K_0402_5%
CLR_CMOS#
J1
NO SHORT PADS
C373 1U_0603_10V6K
ICH_RTCX1
ICH_RTCX2
R602 10M_0402_5%
C683 12P_0402_50V8J
C684 12P_0402_50V8J
Y2 32.768KHZ QTFM28-32768K125P10L
+3VS
R276 SATA_LED#
close ICH8
PSATA_ITX_DRX_N0
PSATA_ITX_DRX_P0
C369 3900P_0402_50V7K
C370 3900P_0402_50V7K
U7A
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
R269 24.9_0402_1%
Within 500 mils
CLOSE TO JP3
ICH8M REV 1.0
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
IDE
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LPC_AD[0..3] 27,28
LPC_FRAME# 27,28
TP23 PAD
TP24 PAD
GATEA20 28
H_A20M# 4
H_DPRSTP# 5,7,46
H_FERR# 4
H_PWRGOOD 5
H_IGNNE# 4
H_INIT# 4
H_INTR 4
KB_RST# 28
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THERMTRIP# 4,7
IDE_DD[0..15] 21
IDE_DA0 21
IDE_DA1 21
IDE_DA2 21
IDE_DCS1# 21
IDE_DCS3# 21
IDE_DIOR# 21
IDE_DIOW# 21
IDE_DDACK# 21
IDE_IRQ 21
IDE_DIORDY 21
IDE_DDREQ 21
+VCCP
+3VS
GATEA20 R285 10K_0402_5%
KB_RST# R242 10K_0402_5%
H_FERR# R271 56_0402_5%
R273 56_0402_5%
within 2" from R1557
R283 24_0402_1%
placed within 2" from ICH8M
IDE_DIORDY R560 4.7K_0402_5%
IDE_IRQ R573 8.2K_0402_5%
R296 0_0402_5%
R217 24.9_0402_1%
GLAN_COMP
R613 33_0402_5%
R612 33_0402_5%
HDA_BITCLK_R
HDA_SYNC_R
R284 33_0402_5%
HDA_RST_R#
R256 33_0402_5%
HDA_SDOUT_R
ADC_ACZ_SDIN0
PAD TP28
SATA_LED#
PSATA_IRX_DTX_N0_C
PSATA_IRX_DTX_P0_C
PSATA_ITX_DRX_N0_C
PSATA_ITX_DRX_P0_C
CLK_PCIE_SATA#
CLK_PCIE_SATA
XOR CHAIN ENTRANCE STRAP:RSVD
@R254 1K_0402_5%
ACZ_SDOUT
XOR Chain Entrance Strap
ICH RSVD | HDA SDOUT | Description
0 | 0 | RSVD
0 | 1 | Enter XOR Chain
1 | 0 | Normal Operation (Default)
1 | 1 | Set PCIE port config bit 1
Security Classification
Compal Secret Data
Issued Date
2007/1/15
Deciphered Date
2008/1/15
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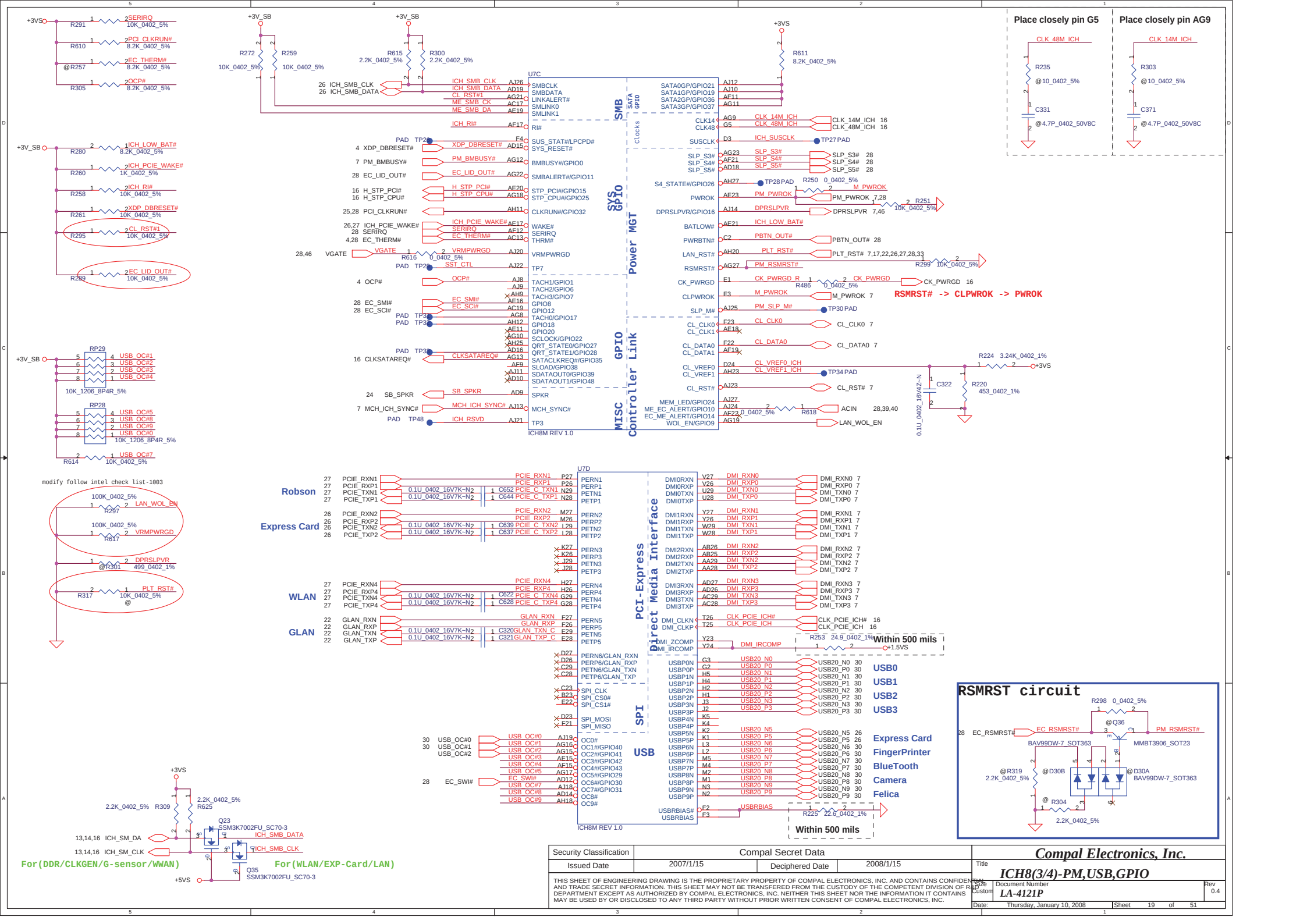
Compal Electronics, Inc.
Title
ICH8(2/4)-LAN,HD,IDE,LPC
Size Custom
Document Number LA-4121P
Rev 0.4
Date: Thursday, January 10, 2008
Sheet 18 of 51



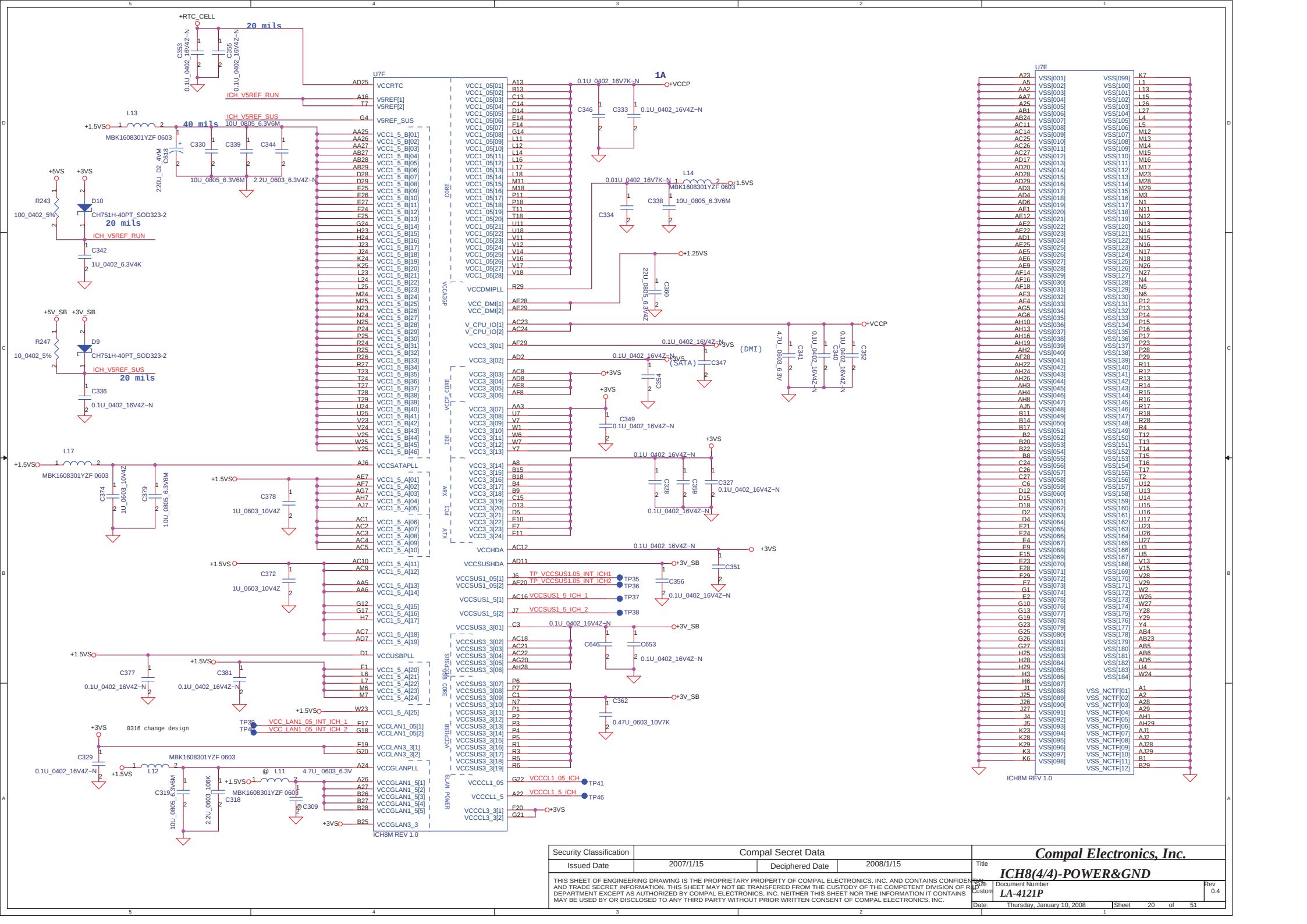
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: ICH8(3/4)-PM,USB,GPIO

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 19 of 51


+RTC_CELL
20 mils
C353 0.1U_0402_16V4Z-N
C355 0.1U_0402_16V4Z-N
U7F
AD25 VCCRTC
ICH_V5REF_RUN
A16 V5REF[1]
T7 V5REF[2]
L13
+1.5VS
40 mils
MBK1608301YZF 0603
ICH_V5REF_SUS
G4 V5REF_SUS
10U_0805_6.3V6M
C330
C339
C344
C618 220U_D2_4VM
10U_0805_6.3V6M
2.2U_0603_6.3V4Z-N
+5VS
+3VS
R243 100_0402_5%
D10 CH751H-40PT_SOD323-2
20 mils
ICH_V5REF_RUN
C342 1U_0402_6.3V4K
+5V_SB
+3V_SB
R247 10_0402_5%
D9 CH751H-40PT_SOD323-2
ICH_V5REF_SUS
20 mils
C336 0.1U_0402_16V4Z-N
L17
+1.5VS
MBK1608301YZF 0603
C374 1U_0603_10V4Z
C379 10U_0805_6.3V6M
C378 1U_0603_10V4Z
C372 1U_0603_10V4Z
C377 0.1U_0402_16V4Z-N
C381 0.1U_0402_16V4Z-N
0316 change design
C329 0.1U_0402_16V4Z-N
L12 MBK1608301YZF 0603
C319 10U_0805_6.3V6M
C318 2.2U_0603_106K
@ L11 4.7U_0603_6.3V
@C309
VCC1_5_B[01] VCC1_5_B[02] VCC1_5_B[03] VCC1_5_B[04] VCC1_5_B[05] VCC1_5_B[06] VCC1_5_B[07] VCC1_5_B[08] VCC1_5_B[09] VCC1_5_B[10] VCC1_5_B[11] VCC1_5_B[12] VCC1_5_B[13] VCC1_5_B[14] VCC1_5_B[15] VCC1_5_B[16] VCC1_5_B[17] VCC1_5_B[18] VCC1_5_B[19] VCC1_5_B[20] VCC1_5_B[21] VCC1_5_B[22] VCC1_5_B[23] VCC1_5_B[24] VCC1_5_B[25] VCC1_5_B[26] VCC1_5_B[27] VCC1_5_B[28] VCC1_5_B[29] VCC1_5_B[30] VCC1_5_B[31] VCC1_5_B[32] VCC1_5_B[33] VCC1_5_B[34] VCC1_5_B[35] VCC1_5_B[36] VCC1_5_B[37] VCC1_5_B[38] VCC1_5_B[39] VCC1_5_B[40] VCC1_5_B[41] VCC1_5_B[42] VCC1_5_B[43] VCC1_5_B[44] VCC1_5_B[45] VCC1_5_B[46]
VCCA3GP
VCCDMIPLL
R29
VCC_DMI[1] AE28
VCC_DMI[2] AE29
V_CPU_IO[1] AC23
V_CPU_IO[2] AC24
VCCSATAPLL AJ6
VCC1_5_A[01] AE7
VCC1_5_A[02] AF7
VCC1_5_A[03] AG7
VCC1_5_A[04] AH7
VCC1_5_A[05] AJ7
VCC1_5_A[06] AC1
VCC1_5_A[07] AC2
VCC1_5_A[08] AC3
VCC1_5_A[09] AC4
VCC1_5_A[10] AC5
VCC1_5_A[11] AC10
VCC1_5_A[12] AC9
VCC1_5_A[13] AA5
VCC1_5_A[14] AA6
VCC1_5_A[15] G12
VCC1_5_A[16] G17
VCC1_5_A[17] H7
VCC1_5_A[18] AC7
VCC1_5_A[19] AD7
VCCUSBPLL D1
VCC1_5_A[20] F1
VCC1_5_A[21] L6
VCC1_5_A[22] L7
VCC1_5_A[23] M6
VCC1_5_A[24] M7
VCC1_5_A[25] W23
VCCLAN1_05[1] F17
VCCLAN1_05[2] G18
VCCLAN3_3[1] F19
VCCLAN3_3[2] G20
VCCGLANPLL A24
VCCGLAN1_5[1] A26
VCCGLAN1_5[2] A27
VCCGLAN1_5[3] B26
VCCGLAN1_5[4] B27
VCCGLAN1_5[5] B28
VCCGLAN3_3 B25
ICH8M REV 1.0
VCC1_05[01] VCC1_05[02] VCC1_05[03] VCC1_05[04] VCC1_05[05] VCC1_05[06] VCC1_05[07] VCC1_05[08] VCC1_05[09] VCC1_05[10] VCC1_05[11] VCC1_05[12] VCC1_05[13] VCC1_05[14] VCC1_05[15] VCC1_05[16] VCC1_05[17] VCC1_05[18] VCC1_05[19] VCC1_05[20] VCC1_05[21] VCC1_05[22] VCC1_05[23] VCC1_05[24] VCC1_05[25] VCC1_05[26] VCC1_05[27] VCC1_05[28]
VCC3_3[01] VCC3_3[02] VCC3_3[03] VCC3_3[04] VCC3_3[05] VCC3_3[06] VCC3_3[07] VCC3_3[08] VCC3_3[09] VCC3_3[10] VCC3_3[11] VCC3_3[12] VCC3_3[13] VCC3_3[14] VCC3_3[15] VCC3_3[16] VCC3_3[17] VCC3_3[18] VCC3_3[19] VCC3_3[20] VCC3_3[21] VCC3_3[22] VCC3_3[23] VCC3_3[24]
VCCHDA AC12
VCCSUSHDA AD11
VCCSUS1_05[1] J6
VCCSUS1_05[2] AF20
VCCSUS1_5[1] AC16
VCCSUS1_5[2] J7
VCCSUS3_3[01] C3
VCCSUS3_3[02] AC18
VCCSUS3_3[03] AC21
VCCSUS3_3[04] AC22
VCCSUS3_3[05] AG20
VCCSUS3_3[06] AH28
VCCSUS3_3[07] P6
VCCSUS3_3[08] P7
VCCSUS3_3[09] C1
VCCSUS3_3[10] N7
VCCSUS3_3[11] P1
VCCSUS3_3[12] P2
VCCSUS3_3[13] P3
VCCSUS3_3[14] P4
VCCSUS3_3[15] P5
VCCSUS3_3[16] R1
VCCSUS3_3[17] R3
VCCSUS3_3[18] R5
VCCSUS3_3[19] R6
VCCCL1_05 G22
VCCCL1_5 A22
VCCCL3_3[1] F20
VCCCL3_3[2] G21
TP35 TP36 TP37 TP38 TP39 TP40 TP41 TP46
VCC_LAN1_05_INT_ICH_1
VCC_LAN1_05_INT_ICH_2
VCCSUS1_05_INT_ICH1
VCCSUS1_05_INT_ICH2
VCCSUS1_5_ICH_1
VCCSUS1_5_ICH_2
VCCCL1_05_ICH
VCCCL1_5_ICH
1A
0.1U_0402_16V7K-N
C346 C333 0.1U_0402_16V4Z-N
+VCCP
0.01U_0402_16V7K-N
L14 MBK1608301YZF 0603
+1.5VS
C334
C338 10U_0805_6.3V6M
+1.25VS
220U_0805_6.3V4Z
C360
0.1U_0402_16V4Z-N
+3VS
(DMI)
(SATA)
C341 4.7U_0603_6.3V
C340 0.1U_0402_16V4Z-N
C352 0.1U_0402_16V4Z-N
C347
C354
C349
C328 C359 C327
C351
C356
C646 C653
C362 0.47U_0603_10V7K
+3V_SB
U7E
VSS[001] VSS[002] VSS[003] VSS[004] VSS[005] VSS[006] VSS[007] VSS[008] VSS[009] VSS[010] VSS[011] VSS[012] VSS[013] VSS[014] VSS[015] VSS[016] VSS[017] VSS[018] VSS[019] VSS[020] VSS[021] VSS[022] VSS[023] VSS[024] VSS[025] VSS[026] VSS[027] VSS[028] VSS[029] VSS[030] VSS[031] VSS[032] VSS[033] VSS[034] VSS[035] VSS[036] VSS[037] VSS[038] VSS[039] VSS[040] VSS[041] VSS[042] VSS[043] VSS[044] VSS[045] VSS[046] VSS[047] VSS[048] VSS[049] VSS[050] VSS[051] VSS[052] VSS[053] VSS[054] VSS[055] VSS[056] VSS[057] VSS[058] VSS[059] VSS[060] VSS[061] VSS[062] VSS[063] VSS[064] VSS[065] VSS[066] VSS[067] VSS[068] VSS[069] VSS[070] VSS[071] VSS[072] VSS[073] VSS[074] VSS[075] VSS[076] VSS[077] VSS[078] VSS[079] VSS[080] VSS[081] VSS[082] VSS[083] VSS[084] VSS[085] VSS[086] VSS[087] VSS[088] VSS[089] VSS[090] VSS[091] VSS[092] VSS[093] VSS[094] VSS[095] VSS[096] VSS[097] VSS[098]
VSS[099] VSS[100] VSS[101] VSS[102] VSS[103] VSS[104] VSS[105] VSS[106] VSS[107] VSS[108] VSS[109] VSS[110] VSS[111] VSS[112] VSS[113] VSS[114] VSS[115] VSS[116] VSS[117] VSS[118] VSS[119] VSS[120] VSS[121] VSS[122] VSS[123] VSS[124] VSS[125] VSS[126] VSS[127] VSS[128] VSS[129] VSS[130] VSS[131] VSS[132] VSS[133] VSS[134] VSS[135] VSS[136] VSS[137] VSS[138] VSS[139] VSS[140] VSS[141] VSS[142] VSS[143] VSS[144] VSS[145] VSS[146] VSS[147] VSS[148] VSS[149] VSS[150] VSS[151] VSS[152] VSS[153] VSS[154] VSS[155] VSS[156] VSS[157] VSS[158] VSS[159] VSS[160] VSS[161] VSS[162] VSS[163] VSS[164] VSS[165] VSS[166] VSS[167] VSS[168] VSS[169] VSS[170] VSS[171] VSS[172] VSS[173] VSS[174] VSS[175] VSS[176] VSS[177] VSS[178] VSS[179] VSS[180] VSS[181] VSS[182] VSS[183] VSS[184]
VSS_NCTF[01] VSS_NCTF[02] VSS_NCTF[03] VSS_NCTF[04] VSS_NCTF[05] VSS_NCTF[06] VSS_NCTF[07] VSS_NCTF[08] VSS_NCTF[09] VSS_NCTF[10] VSS_NCTF[11] VSS_NCTF[12]
ICH8M REV 1.0
Security Classification
Compal Secret Data
Issued Date
2007/1/15
Deciphered Date
2008/1/15
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Compal Electronics, Inc.
Title
ICH8(4/4)-POWER&GND
Size Custom
Document Number
LA-4121P
Rev 0.4
Date: Thursday, January 10, 2008
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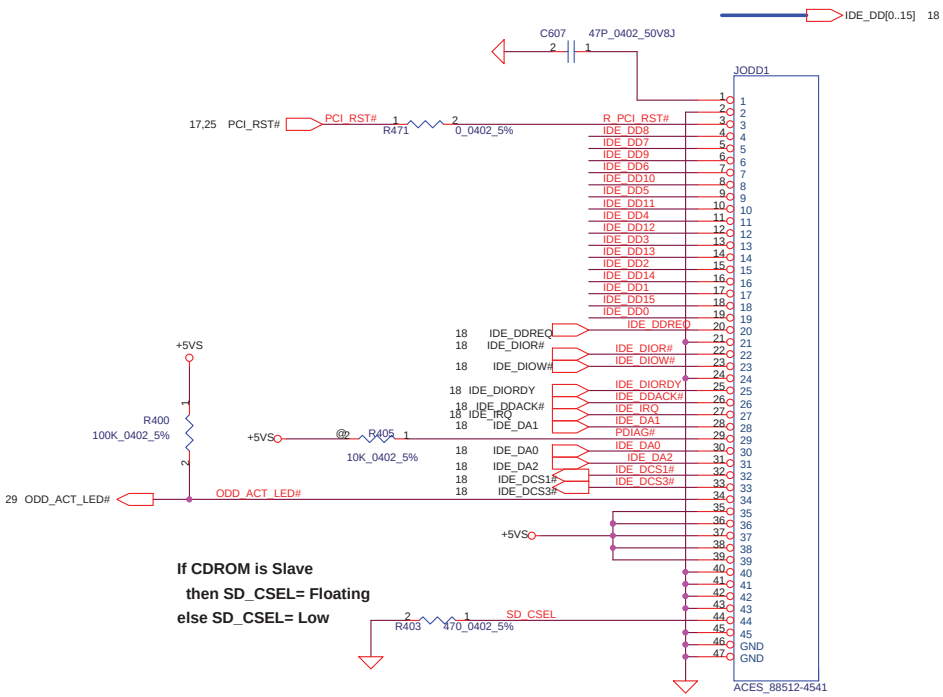
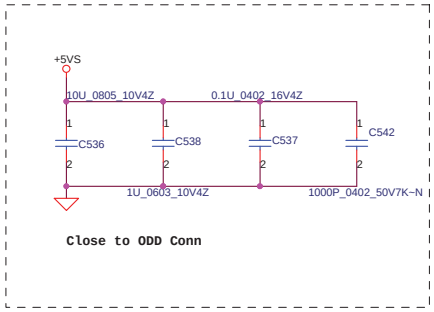
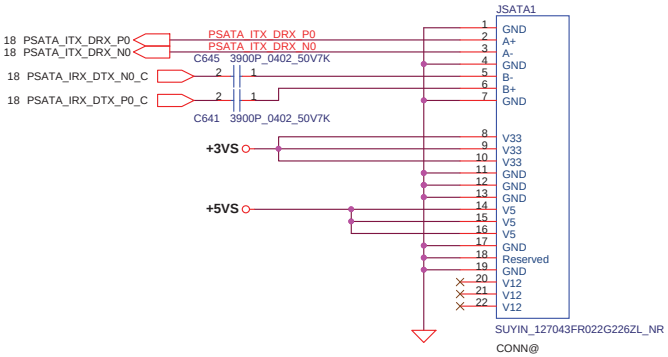
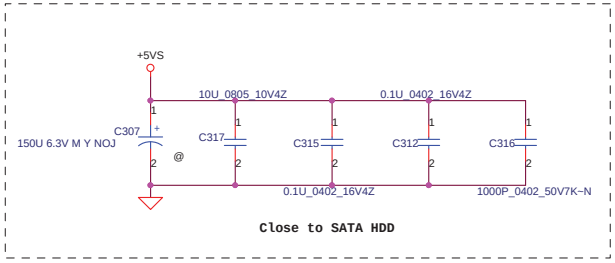
CDROM CONN





SATA HDD CONN





then SD_CSEL= Floating
else SD_CSEL= Low

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **HDD/CDROM**

Size	Document Number	Rev
Custom	LA-4121P	0.4

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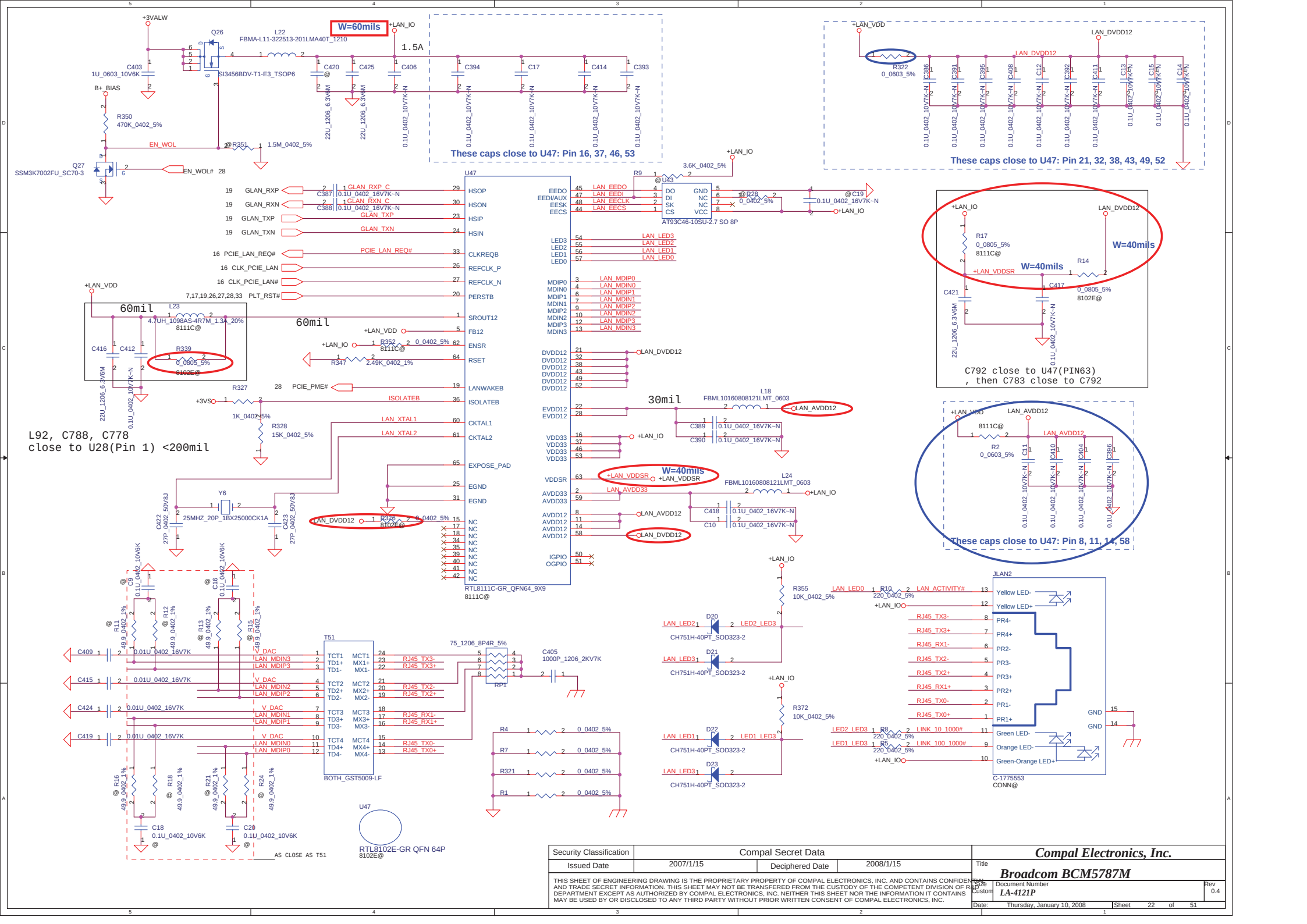
W=60mils
1.5A
These caps close to U47: Pin 16, 37, 46, 53
These caps close to U47: Pin 21, 32, 38, 43, 49, 52
W=40mils
C792 close to U47(PIN63)
, then C783 close to C792
30mil
These caps close to U47: Pin 8, 11, 14, 58
60mil
L92, C788, C778
close to U28(Pin 1) <200mil
RTL8111C-GR_QFN64_9X9
8111C@
RTL8102E-GR QFN 64P
8102E@
BOTH_GST5009-LF
AS CLOSE AS T51
AT93C46-10SU-2.7 SO 8P
CH751H-40PT_SOD323-2
C-1775553
CONN@
Compal Secret Data
Issued Date 2007/1/15
Deciphered Date 2008/1/15
Compal Electronics, Inc.
Broadcom BCM5787M
Document Number LA-4121P
Rev 0.4
Thursday, January 10, 2008
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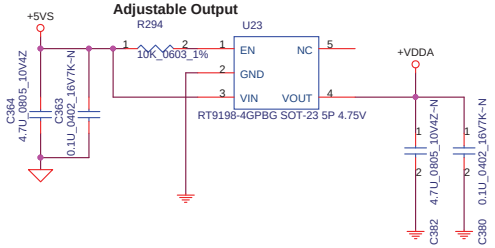
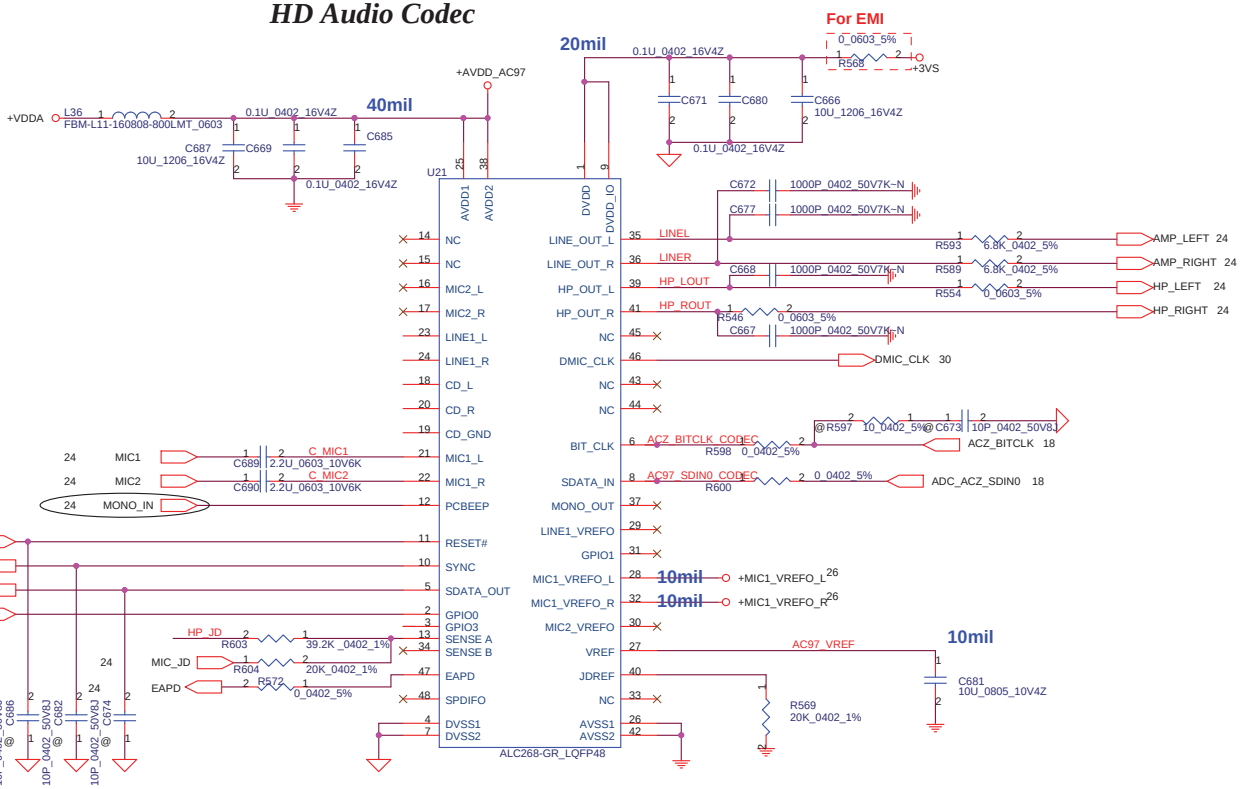
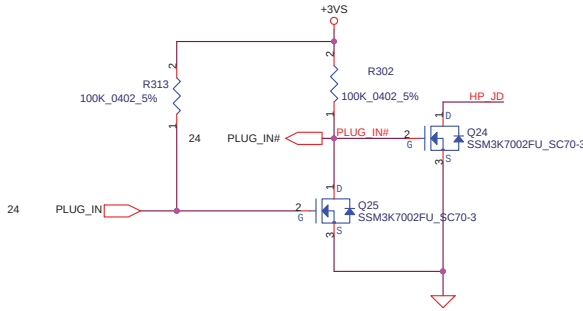
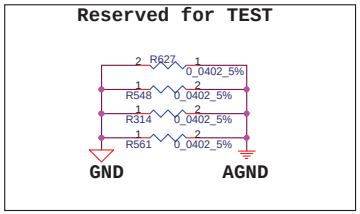


HD Audio Codec







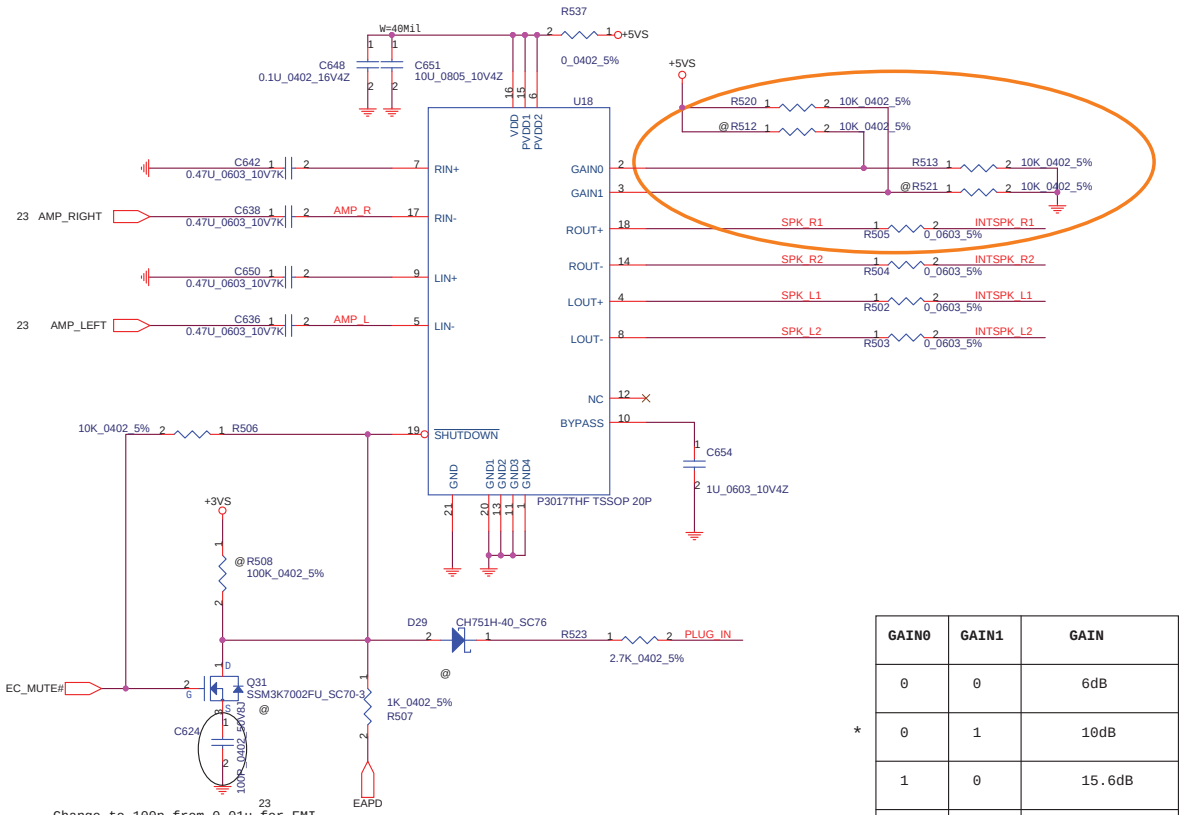
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **Codec ALC268**

Size	Document Number	Rev
Custom	LA-4121P	0.4

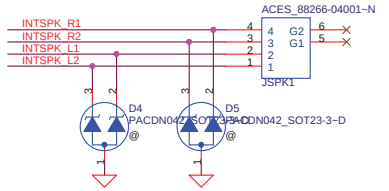
Date: Thursday, January 10, 2008 | Sheet 23 of 51



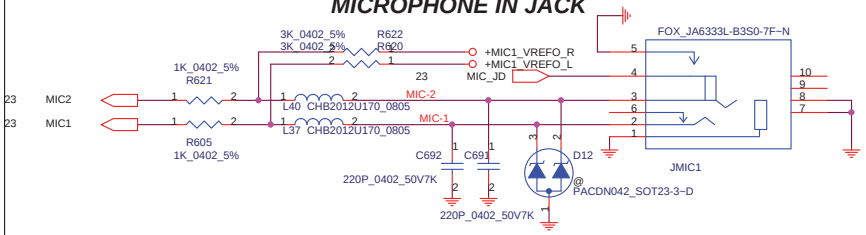
GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

*

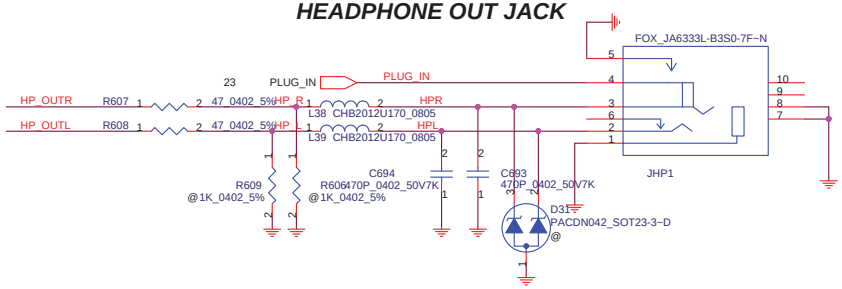
Speaker Connector

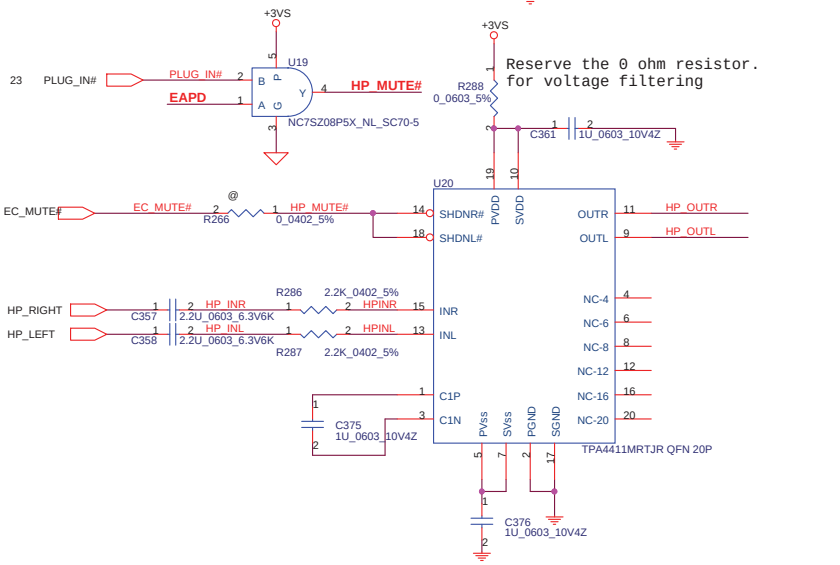


MICROPHONE IN JACK



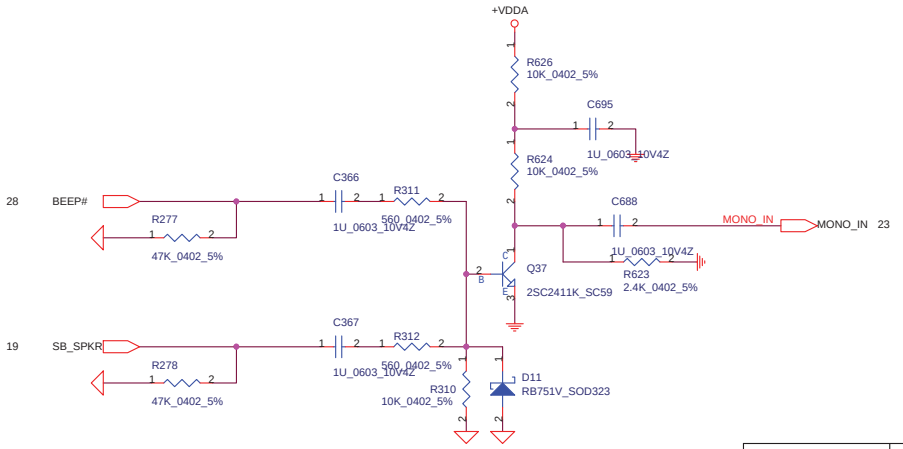
HEADPHONE OUT JACK





EC Beep

ICH Beep



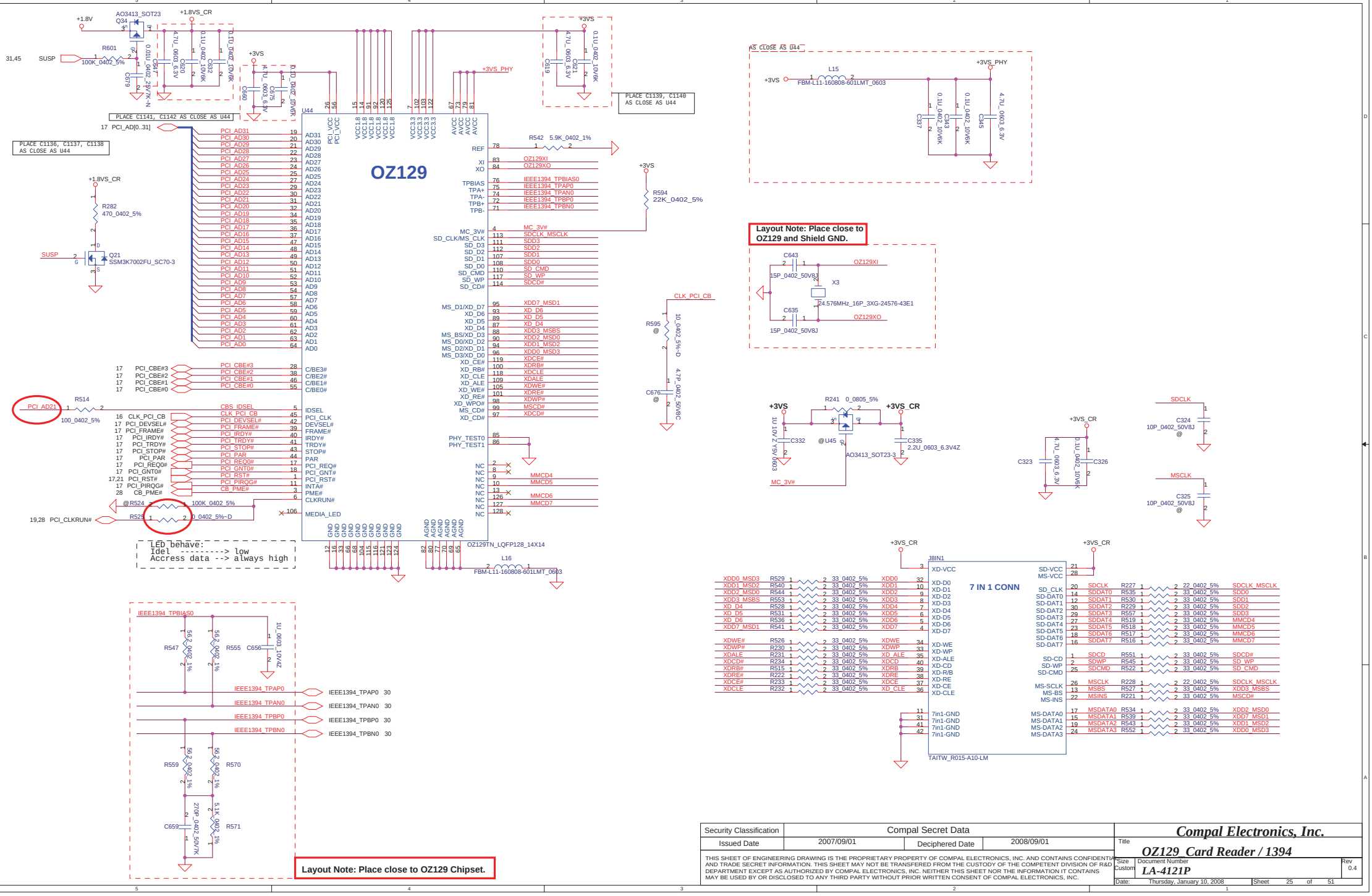
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: AMP/Audio Jack

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 24 of 51



Security Classification	Compal Secret Data		
Issued Date	2007/09/01	Deciphered Date	2008/09/01

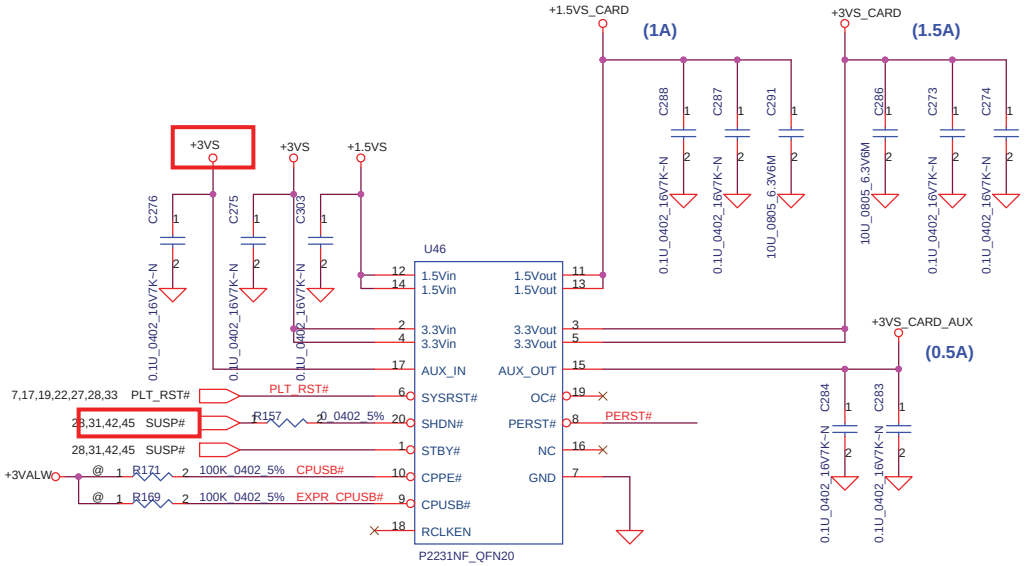
Compal Electronics, Inc.

Title: *OZ129 Card Reader / 1394*

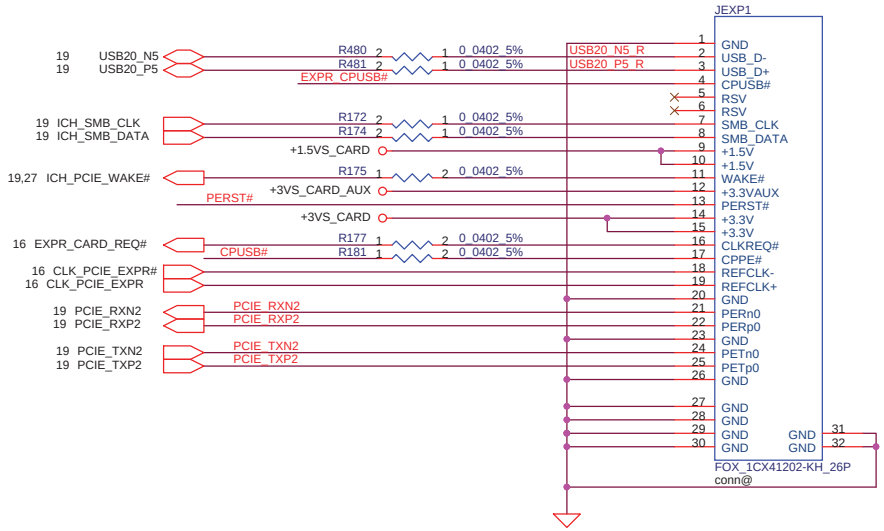
Size	Document Number	Rev
Custom	LA-4121P	0.4

Date: Thursday, January 10, 2008 Sheet 25 of 51

Express Card Power Switch



Express Card



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **Express Card**

Size	Document Number	Rev
Custom	LA-4121P	0.4

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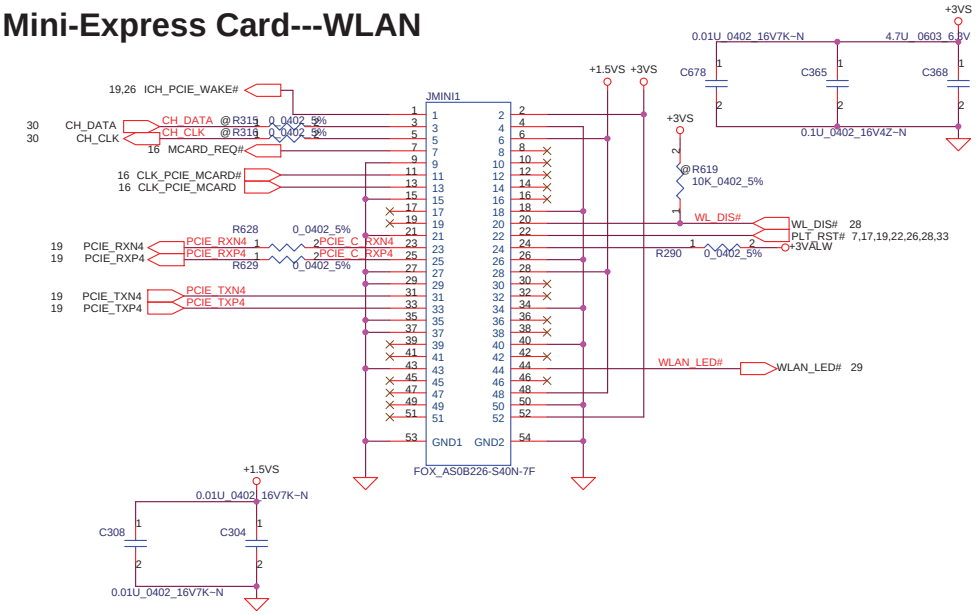
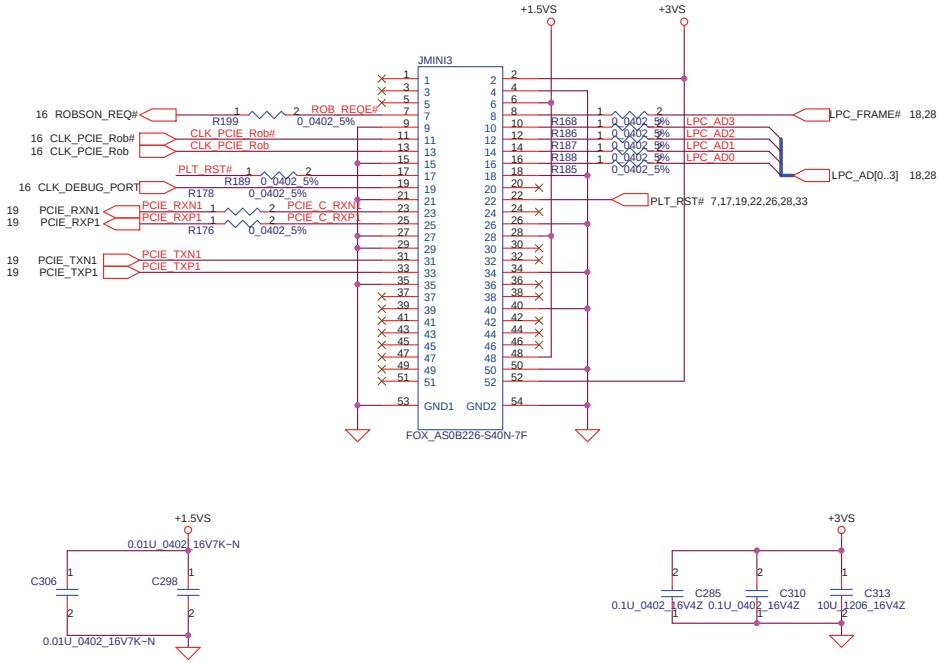
Mini-Express Card---WLAN



Robson



Mini-Express Card---WWAN

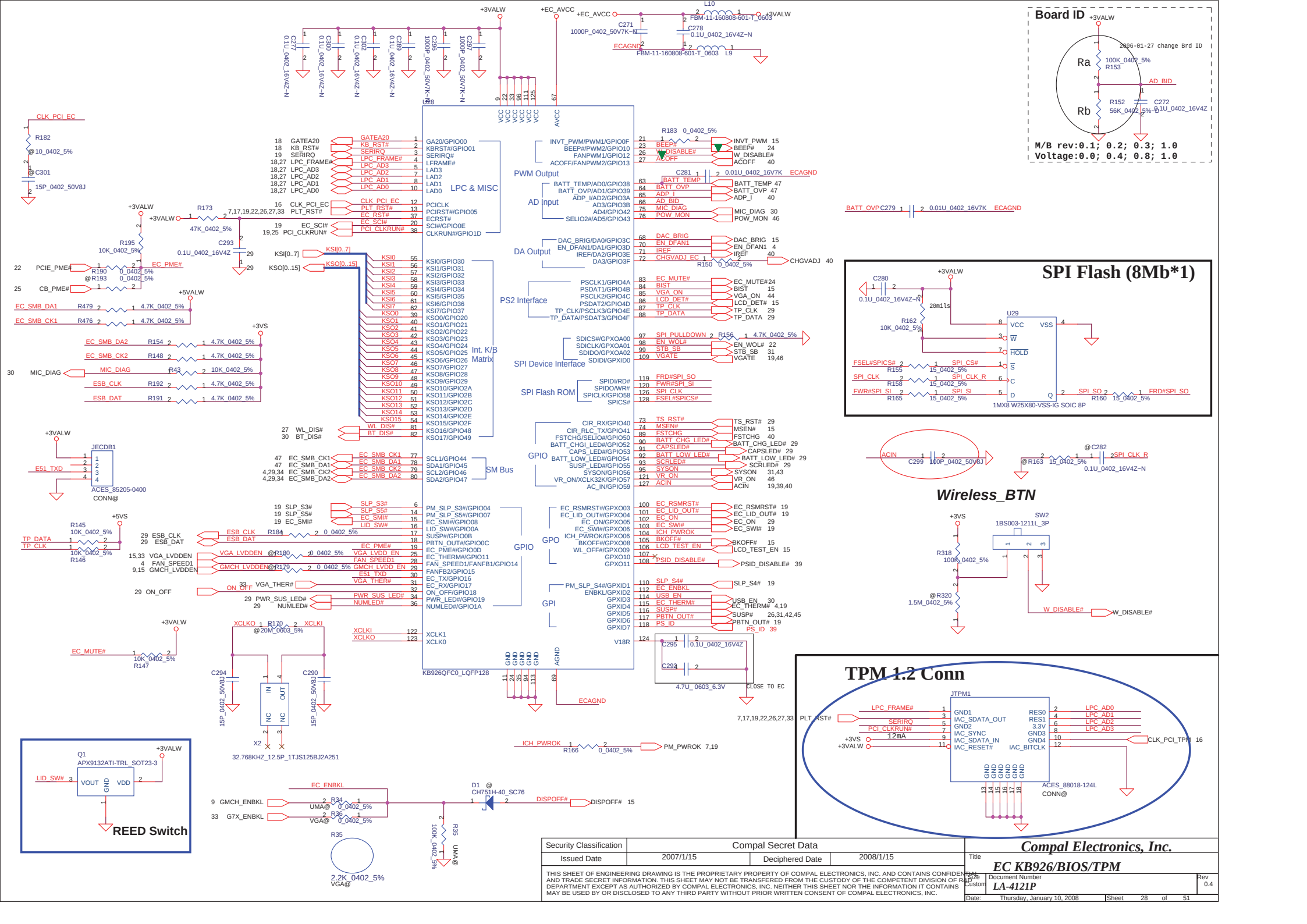
Mini-Express Card---Bluetooth

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **Mini Card**

Size: Custom	Document Number: LA-4121P	Rev: 0.4
Date: Thursday, January 10, 2008	Sheet 27 of 51	


Board ID
+3VALW
2006-01-27 change Brd ID
Ra
100K_0402_5%
R153
AD_BID
Rb
R152
56K_0402_5%
C272
0.01U_0402_16V4Z
M/B rev:0.1; 0.2; 0.3; 1.0
Voltage:0.0; 0.4; 0.8; 1.0
SPI Flash (8Mb*1)
U29
VCC
VSS
W
HOLD
S
C
D
Q
SPI_CS#
SPI_CLK_R
SPI_SI
SPI_SO
FRD#SPI_SO
1MX8 W25X80-VSS-IG SOIC 8P
Wireless_BTN
SW2
1BS003-1211L_3P
W_DISABLE#
TPM 1.2 Conn
JTPM1
LPC_FRAME#
SERIRQ
PCI_CLKRUN#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
CLK_PCI_TPM
ACES_88018-124L
CONN@
REED Switch
Q1
APX9132ATI-TRL_SOT23-3
LID_SW#
VOUT
GND
VDD
X2
32.768KHZ_12.5P_1TJS125BJ2A251
KB926QFC0_LQFP128
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
Security Classification
Compal Secret Data
Issued Date
2007/1/15
Deciphered Date
2008/1/15
Compal Electronics, Inc.
EC KB926/BIOS/TPM
Document Number
LA-4121P
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Date: Thursday, January 10, 2008
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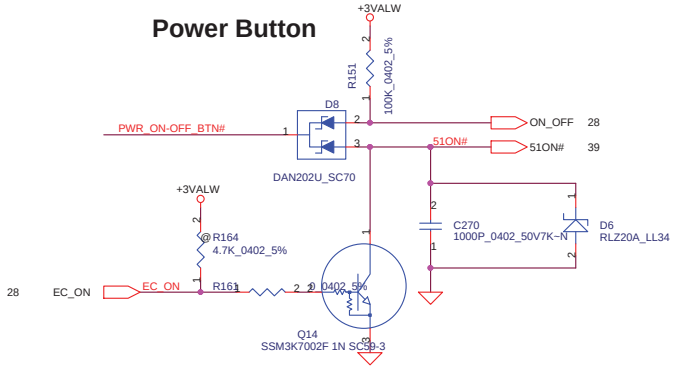
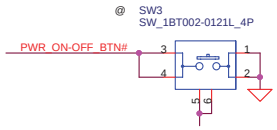
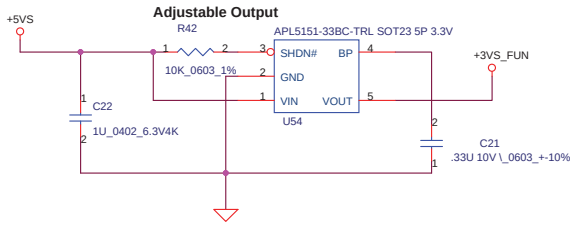
Power Button

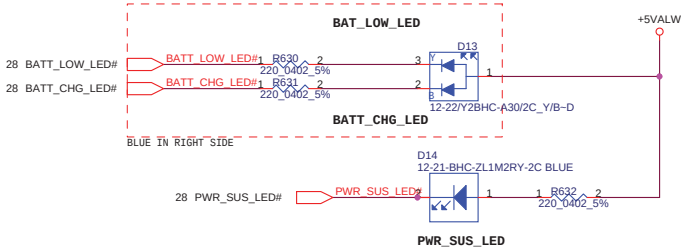




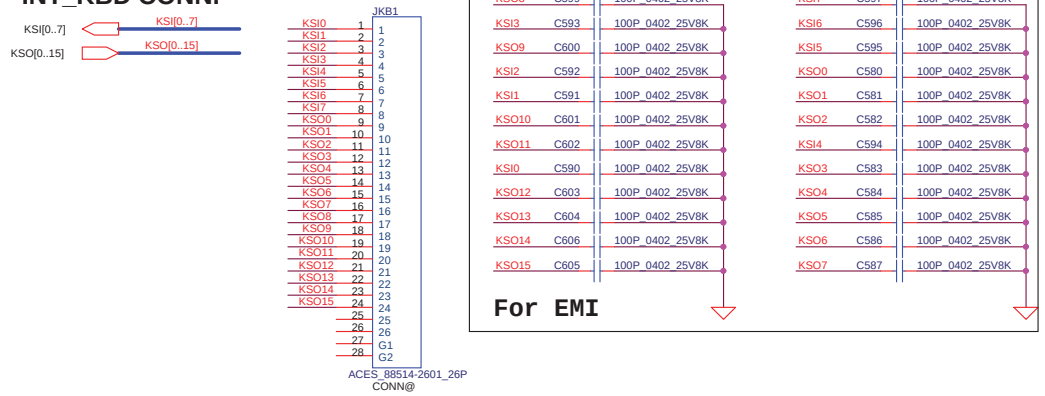
POWER SWITCH

Regulator for ENE sensor

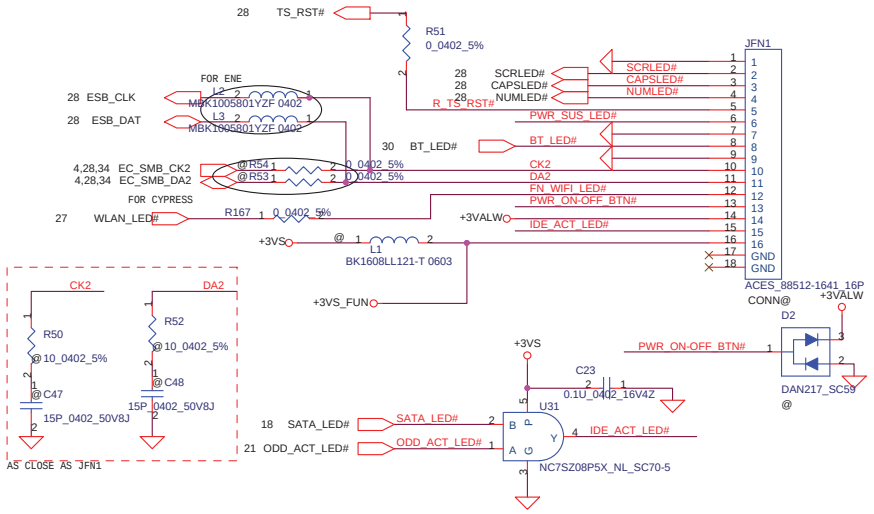




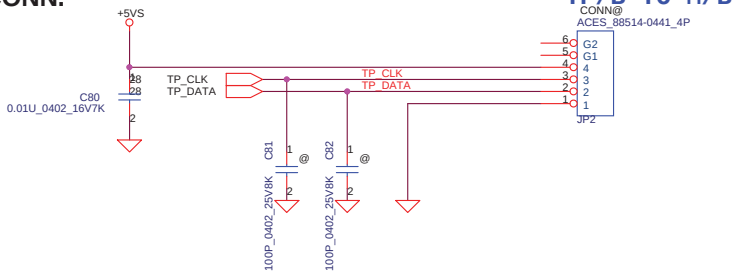
INT_KBD CONN.



Function/B CONN.



Touch PAD/B CONN.



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.			
Title: PWR_OK/BTN/KB/TP			
Size: Custom	Document Number: LA-4121P		Rev: 0.4
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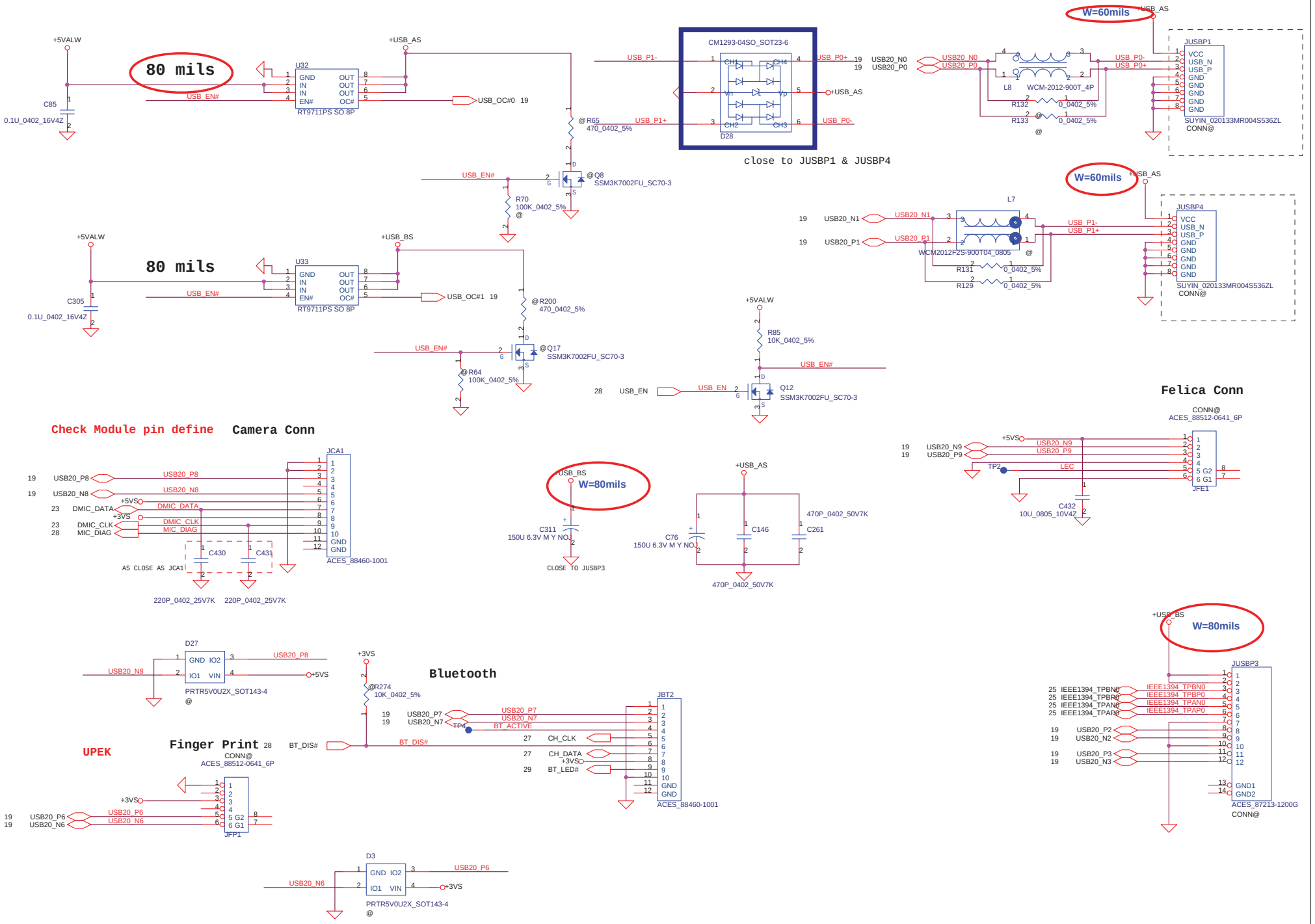


Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

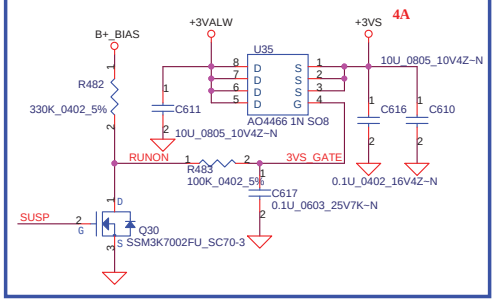
Compal Electronics, Inc.

Title: **USB/BlueTooth/FP/Felcia/Camera**

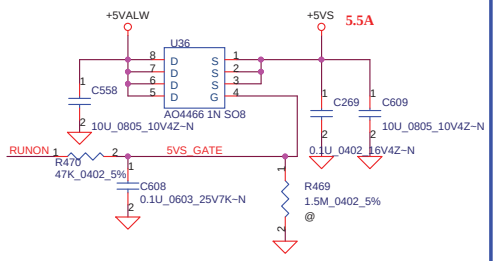
Size	Document Number	Rev
Custom	LA-4121P	0.4

Date: Thursday, January 10, 2008 | Sheet 30 of 51

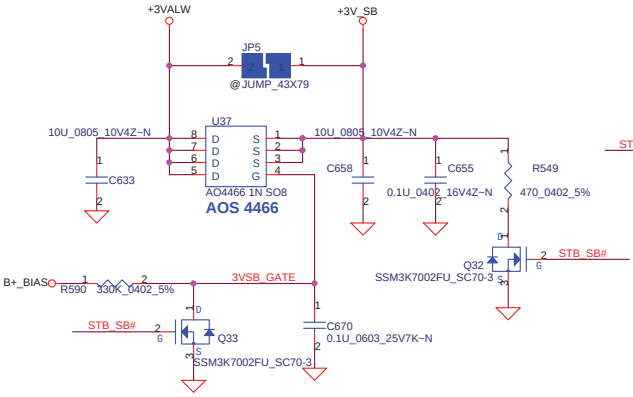
+3VALW to +3VS Transfer



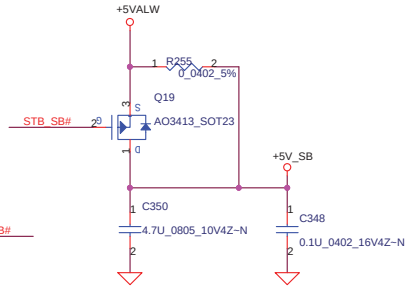
+5VALW to +5VS Transfer

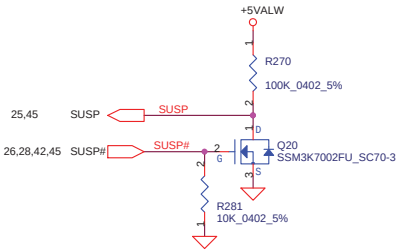


+3VALW TO +3V_SB

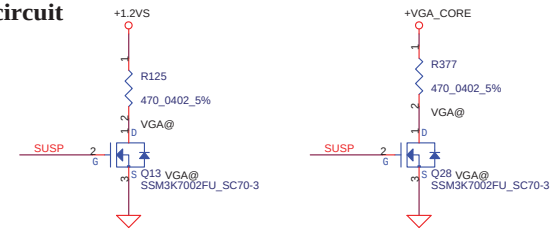


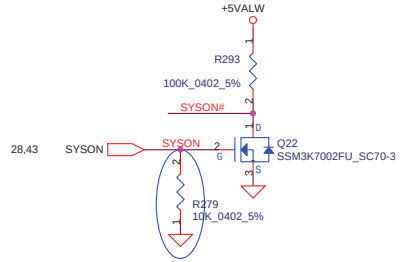
+5VALW TO +5V_SB



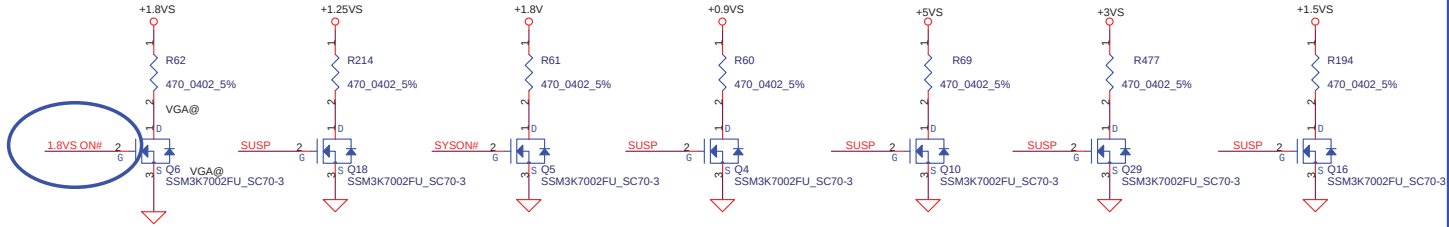


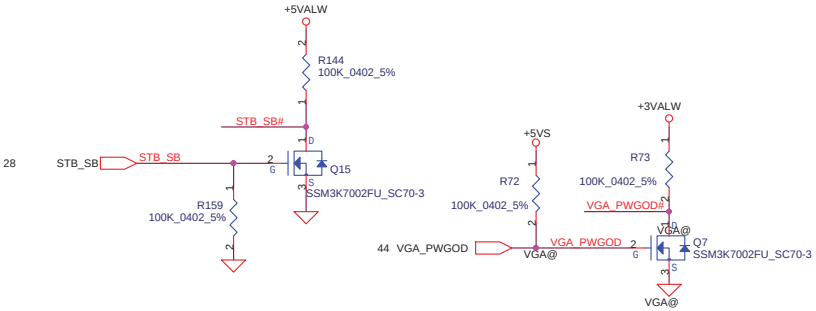
VGA Discharge circuit



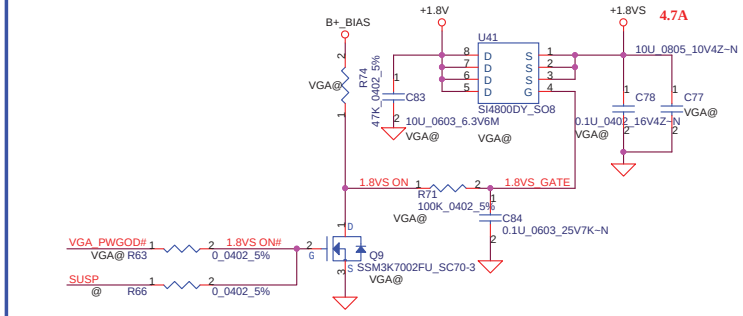


Discharge circuit -1





+1.8V to +1.8VS Transfer



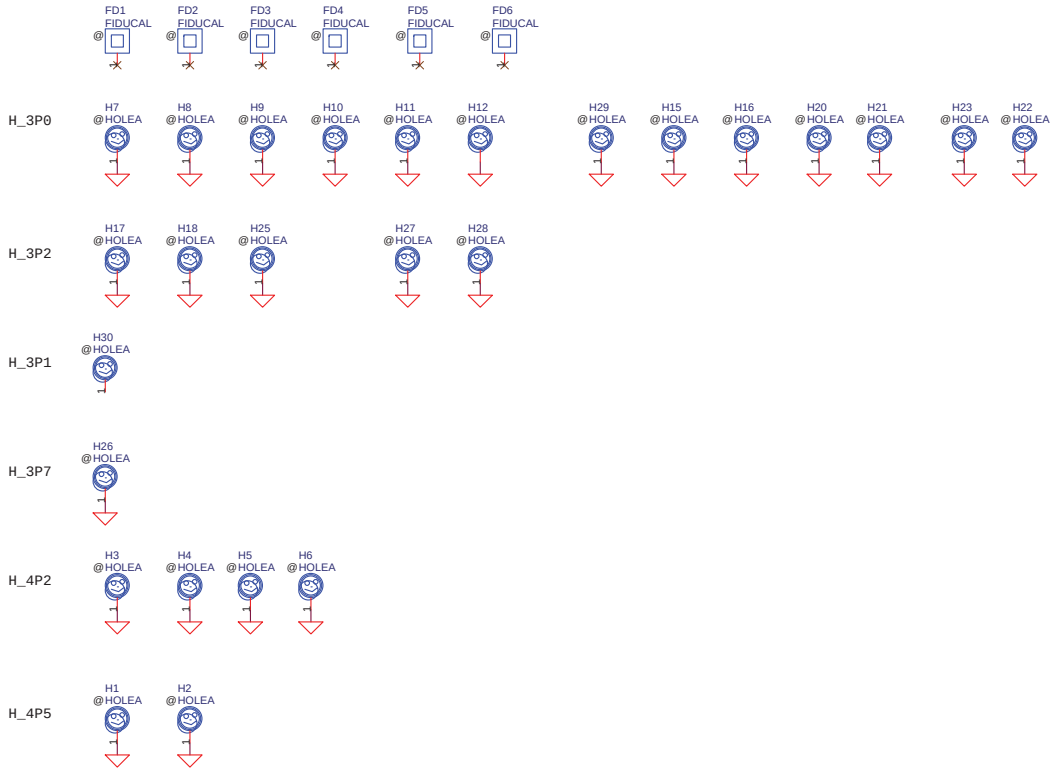
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: DC/DC Circuits

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 31 of 51

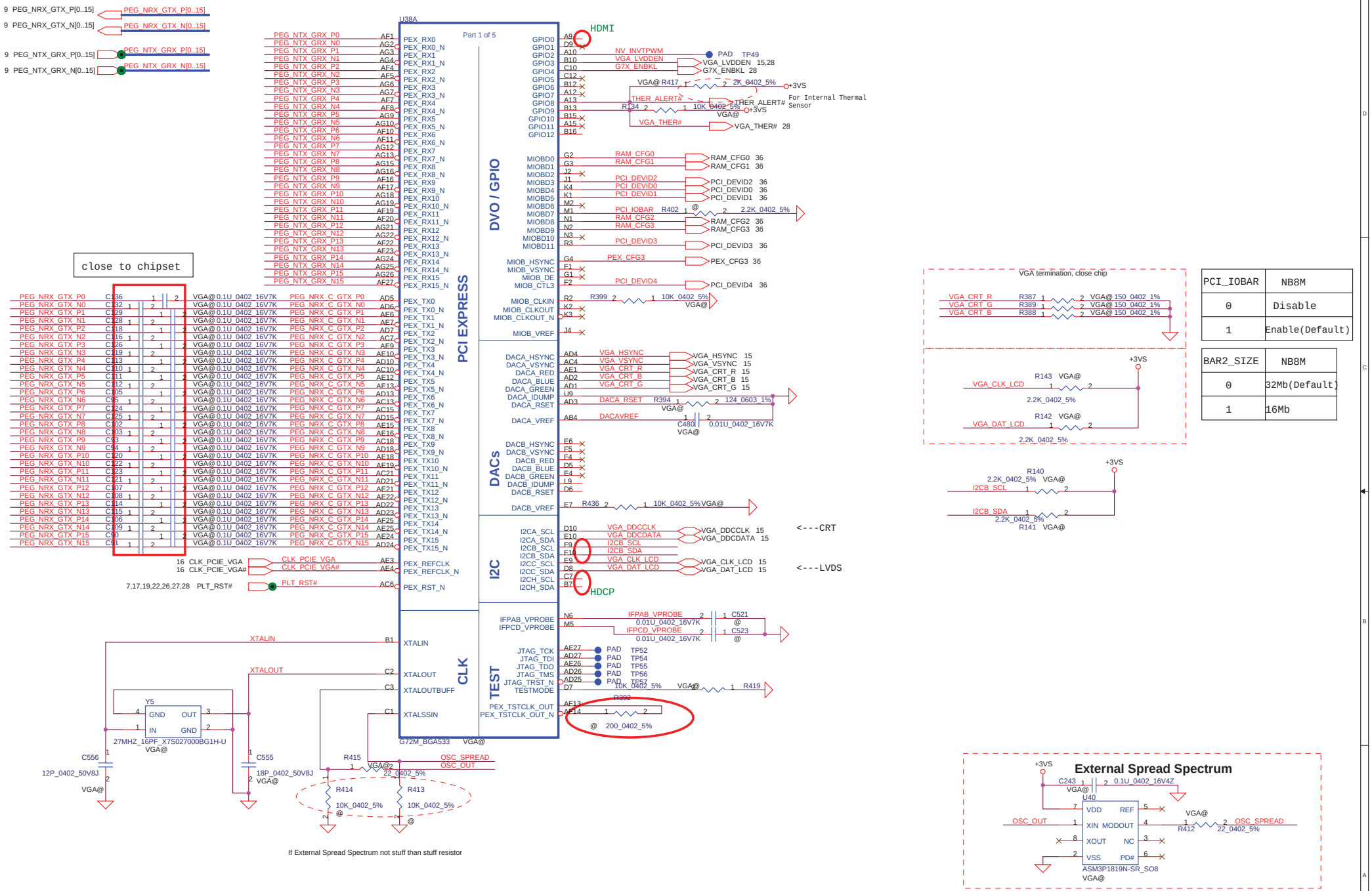


Compal Electronics, Inc.

Title: ***Screws***

Size	Document Number	Rev
Custom	*LA-4121P*	0.4

Date: Thursday, January 10, 2008 | Sheet 32 of 51



PCI_IOBAR	NB8M
0	Disable
1	Enable(Default)

BAR2_SIZE	NB8M
0	32Mb(Default)
1	16Mb

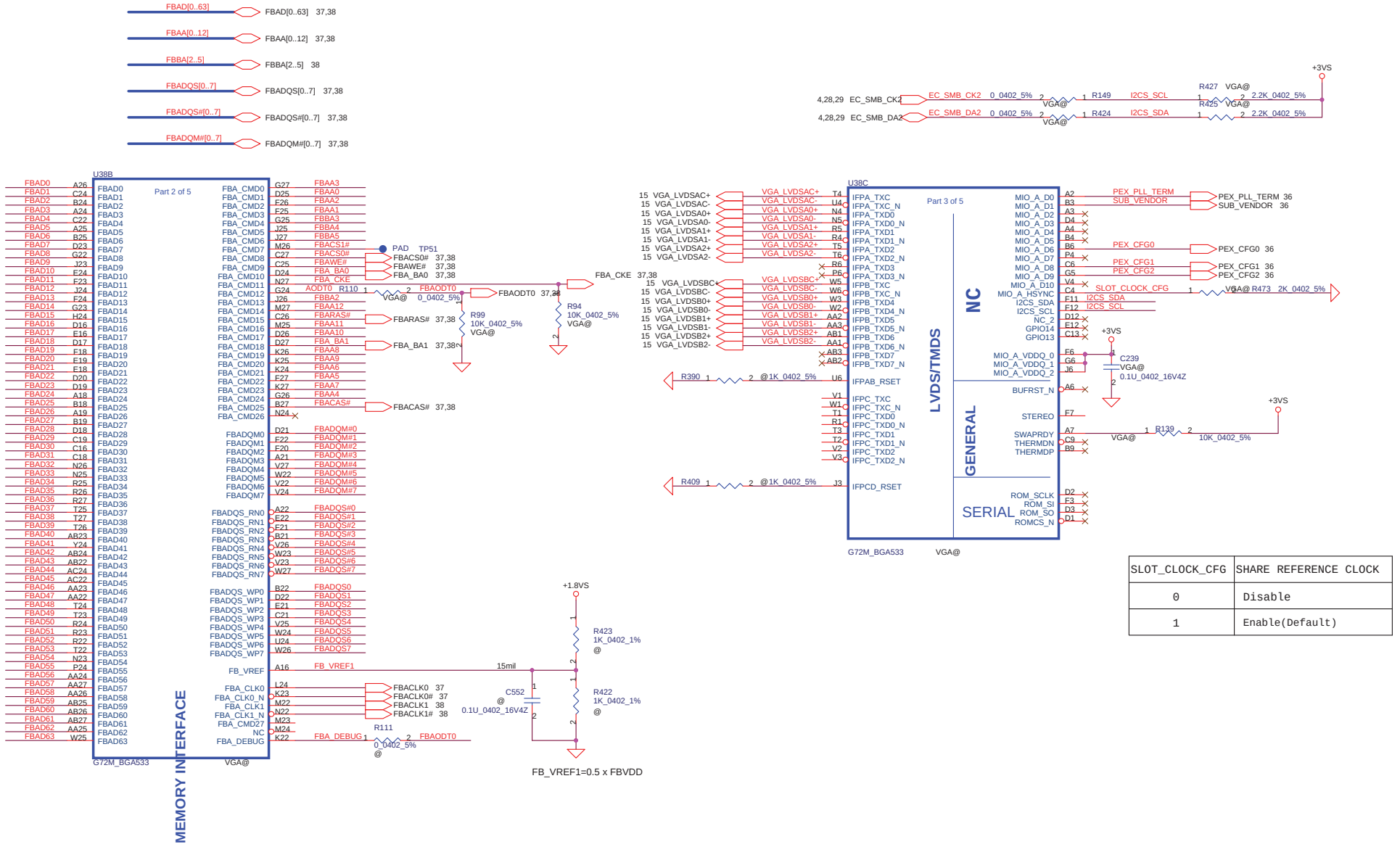
Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

Compal Electronics, Inc.

Title: NB8M-GS Main

Size	Document Number	Rev
Custom		0.4

Date: Thursday, January 10, 2008 | Sheet 33 of 51



SLOT_CLOCK_CFG	SHARE REFERENCE CLOCK
0	Disable
1	Enable(Default)

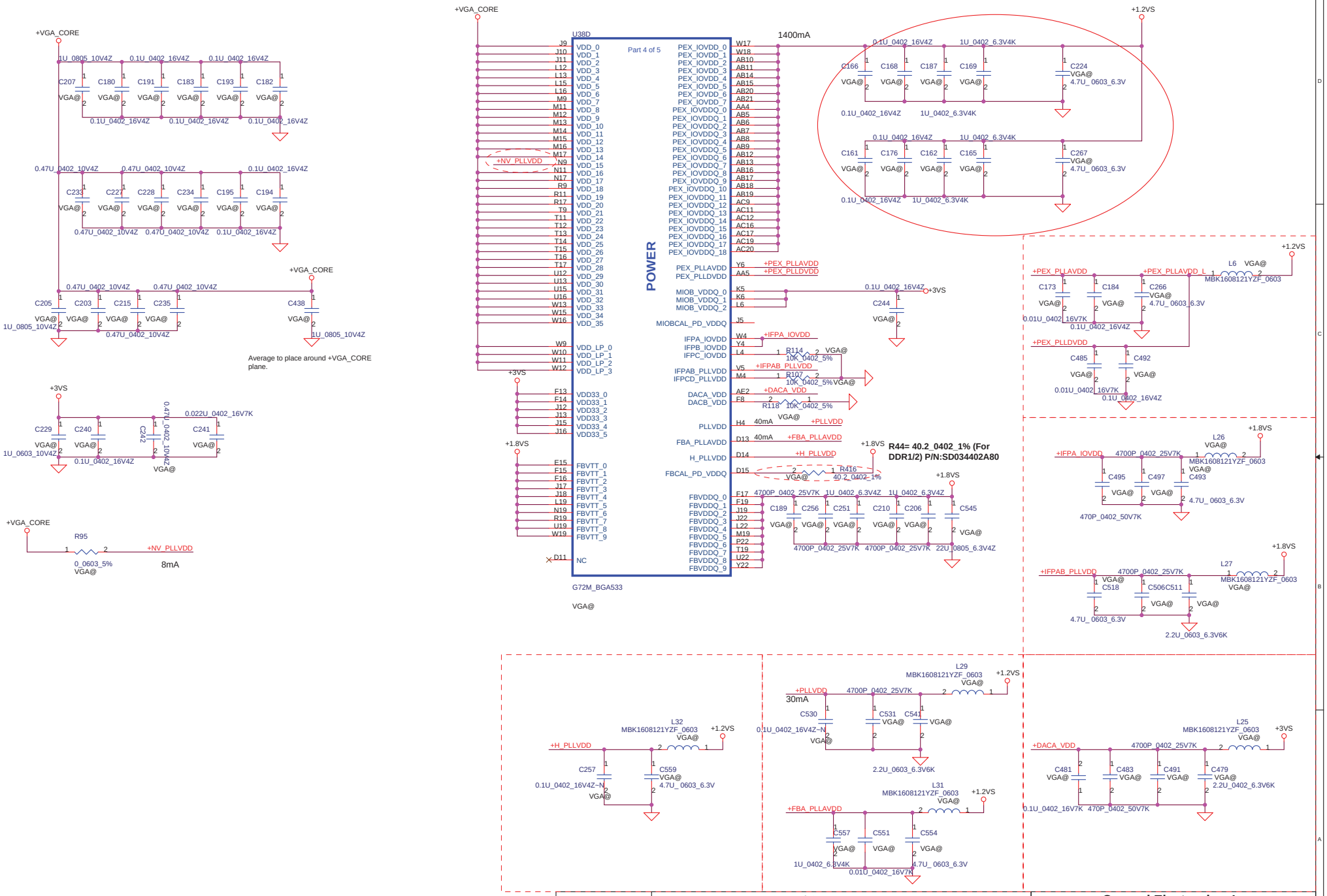
Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

Compal Electronics, Inc.

Title: NB8M-GS Memory

Size: Custom | Document Number | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 34 of 51



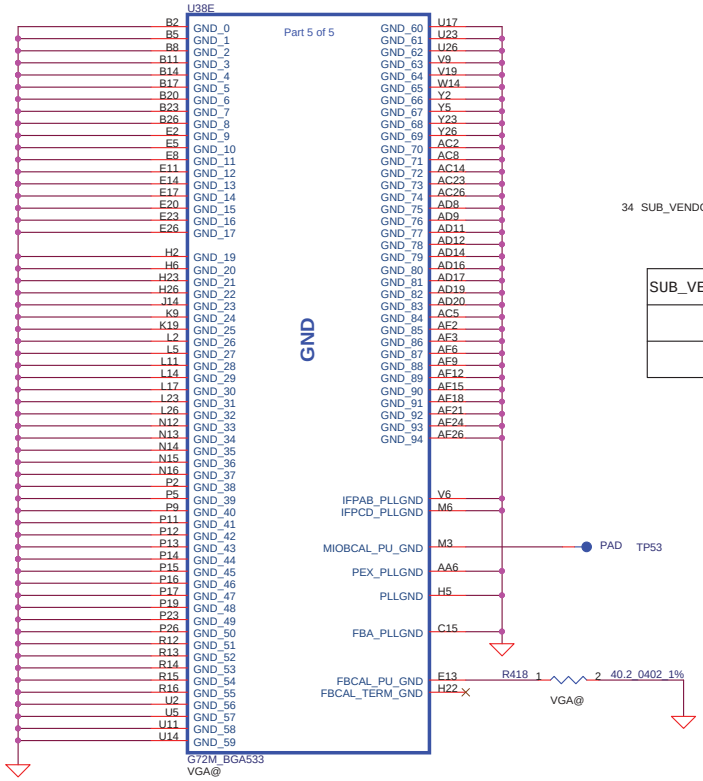
Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

Compal Electronics, Inc.

Title: NB8M-GS Power

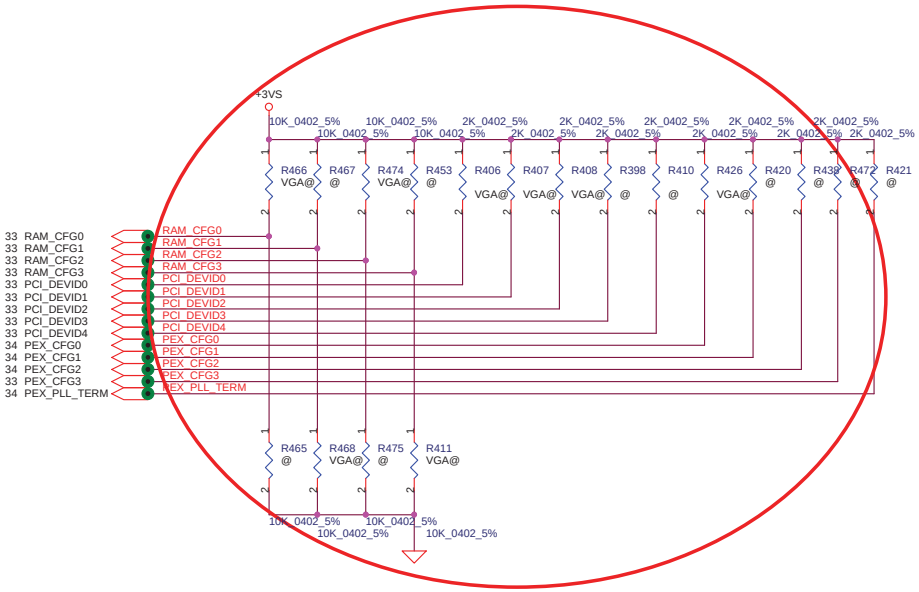
Size	Document Number	Rev
Custom		0.4

Date: Thursday, January 10, 2008 | Sheet 35 of 51



SUB_VENDOR	
0	N0 VIDEO BIOS ROM
1	BIOS ROM is present(Default)

STRAPS	PIN	DESCRIPTION	Value	Value
SUB_VENDOR	MIOAD1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOAD0		0	
PEX_CFG[2:0]	MIOAD [9,8,6]	Recommended for G7x	001	
RAM_CFG[3:0]	MIOAD[5:2]	**RAM_CFG[3] (Bandwidth 0=Full, 1=Half)**		
		RAM_CFG[2] (0=16M or 1=32M)		
		RAM_CFG[1:0] **(Manufacture)** **(01=Sam, 10=Inf, 11=Hyn)**		
PCI_DEVID[3:0]	VIPD[5:3] MIOA_HSYNC	G73M-xxxx8 G72M-0x01D8 NB8M-GS : 0X0427 NB8M-SE : 0X0428	0111 1000	
		G72MV-0x01D7 TBD/TBD	0111	



Bandwidth	RAM Type	Vendor	
FULL R17	32M R11	Samsung	**R20, R19**
HALF R12	16M R16	Hynix	**R18, R19**
		Infineon	**R18, R21**

Package		
(10*12.5)	**Infineon GDDR2(400): SA00000S800 (HYB18T256161AFL-25)**	**Infineon GDDR2(350): SA00000T700 (HYB18T256161AF-28)**
(11*13)	**Samsung GDDR2 (400): SA00000FG10 (K4N56163QF-ZC25)**	**Samsung GDDR2 (350): SA00000TB00 (K4N56163QF-ZC2A)**
(8*13)	**Hynix GDDR2 (400): SA00000FF10 (HY5PS561621AFP-25)**	**Hynix GDDR2 (350): SA00000TJ00 (HY5PS561621AFP-28)**

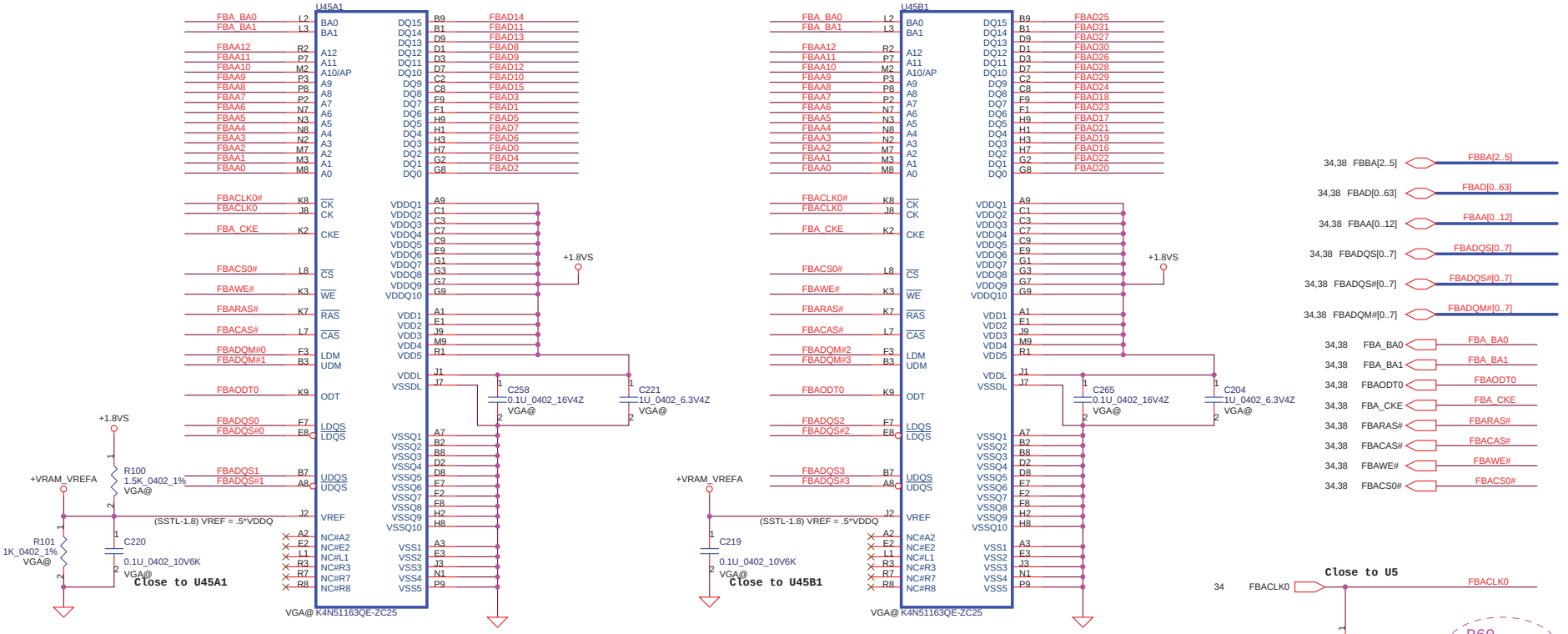
Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

Compal Electronics, Inc.

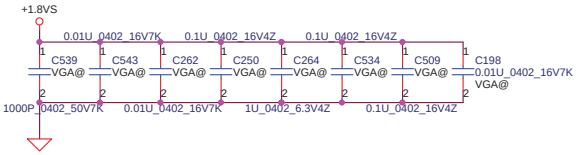
Title: NB8M-GS GND & STRAP

Size: Custom | Document Number | Rev 0.4

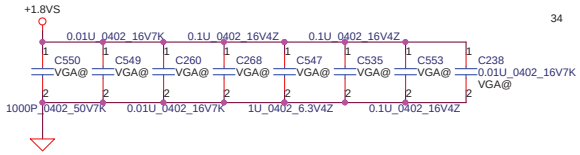
Date: Thursday, January 10, 2008 | Sheet 36 of 51



DDR2 BGA MEMORY



DDR2 BGA MEMORY



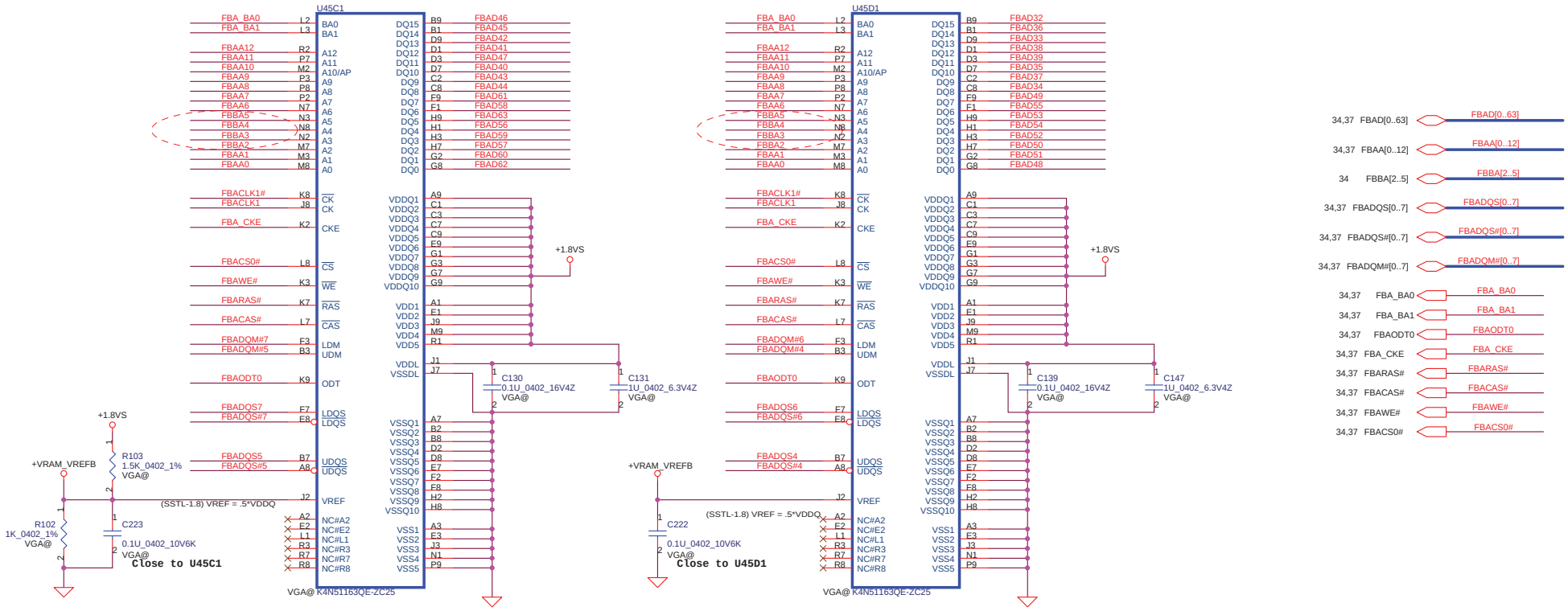
Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

Compal Electronics, Inc.

Title: VRAM DDRA

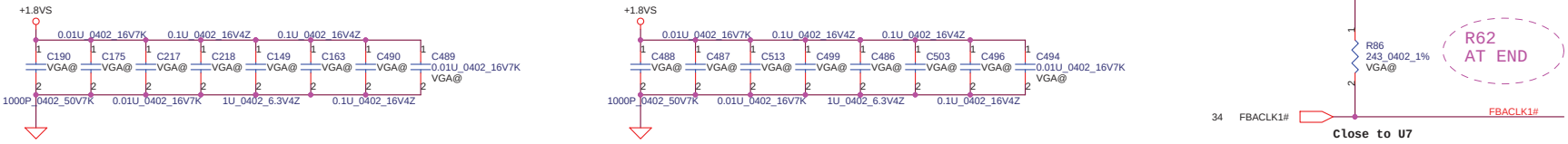
Size	Document Number	Rev
Custom		0.4

Date: Thursday, January 10, 2008 Sheet 37 of 51



DDR2 BGA MEMORY

DDR2 BGA MEMORY



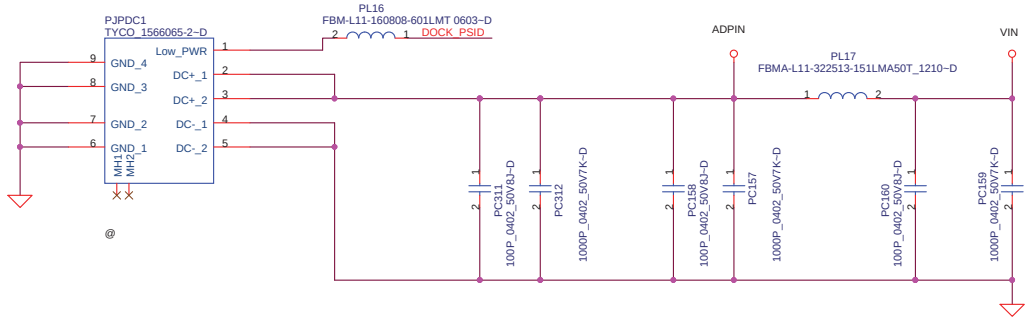
Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

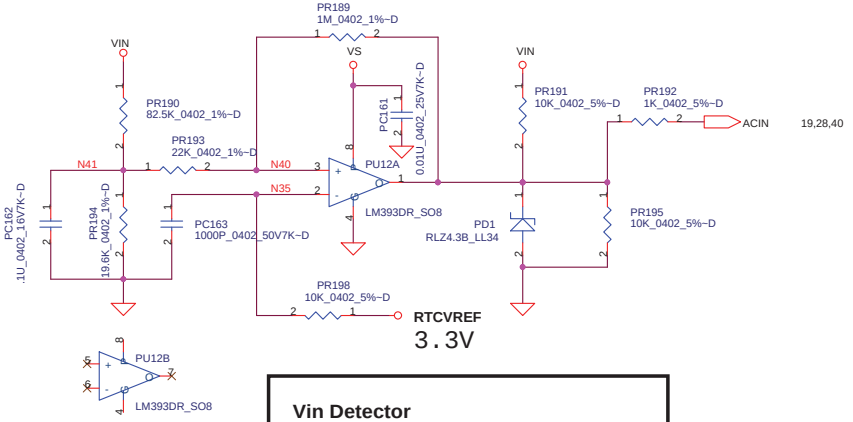
Compal Electronics, Inc.

Title: VRAM DDRB

Size	Document Number	Rev
Custom		0.4

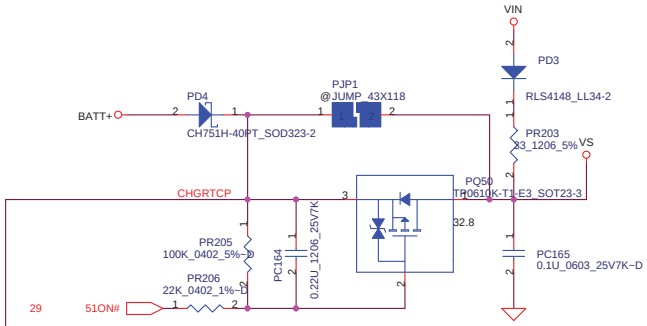
Date: Thursday, January 10, 2008 | Sheet 38 of 51

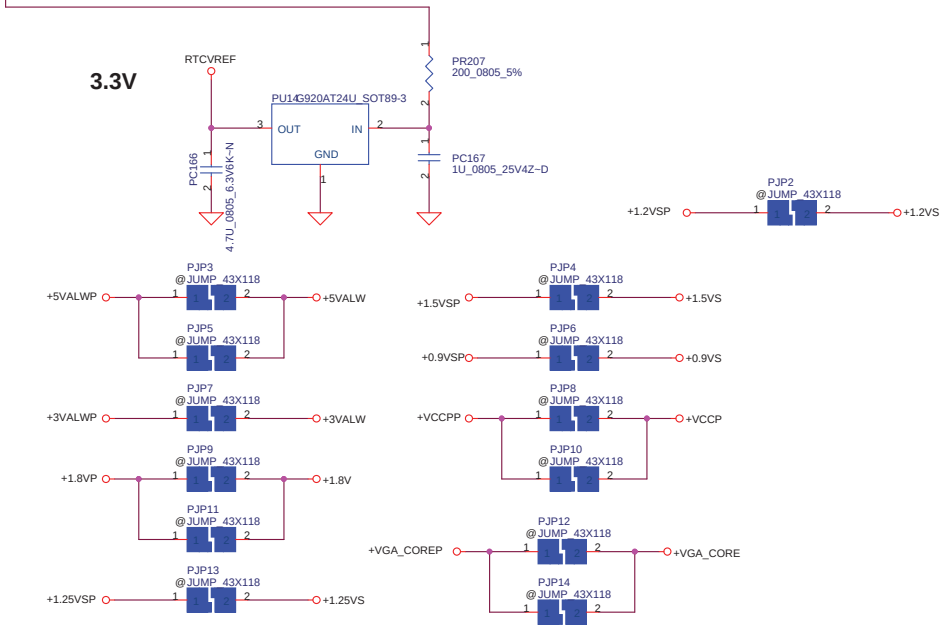


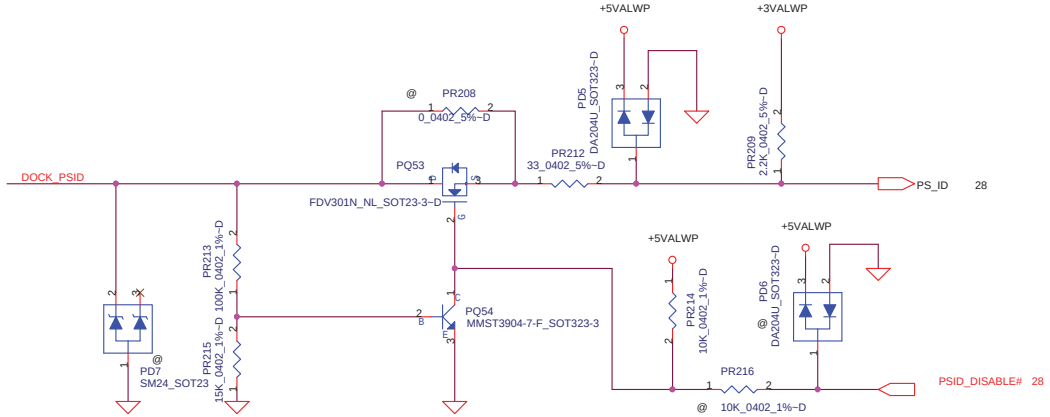


Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813





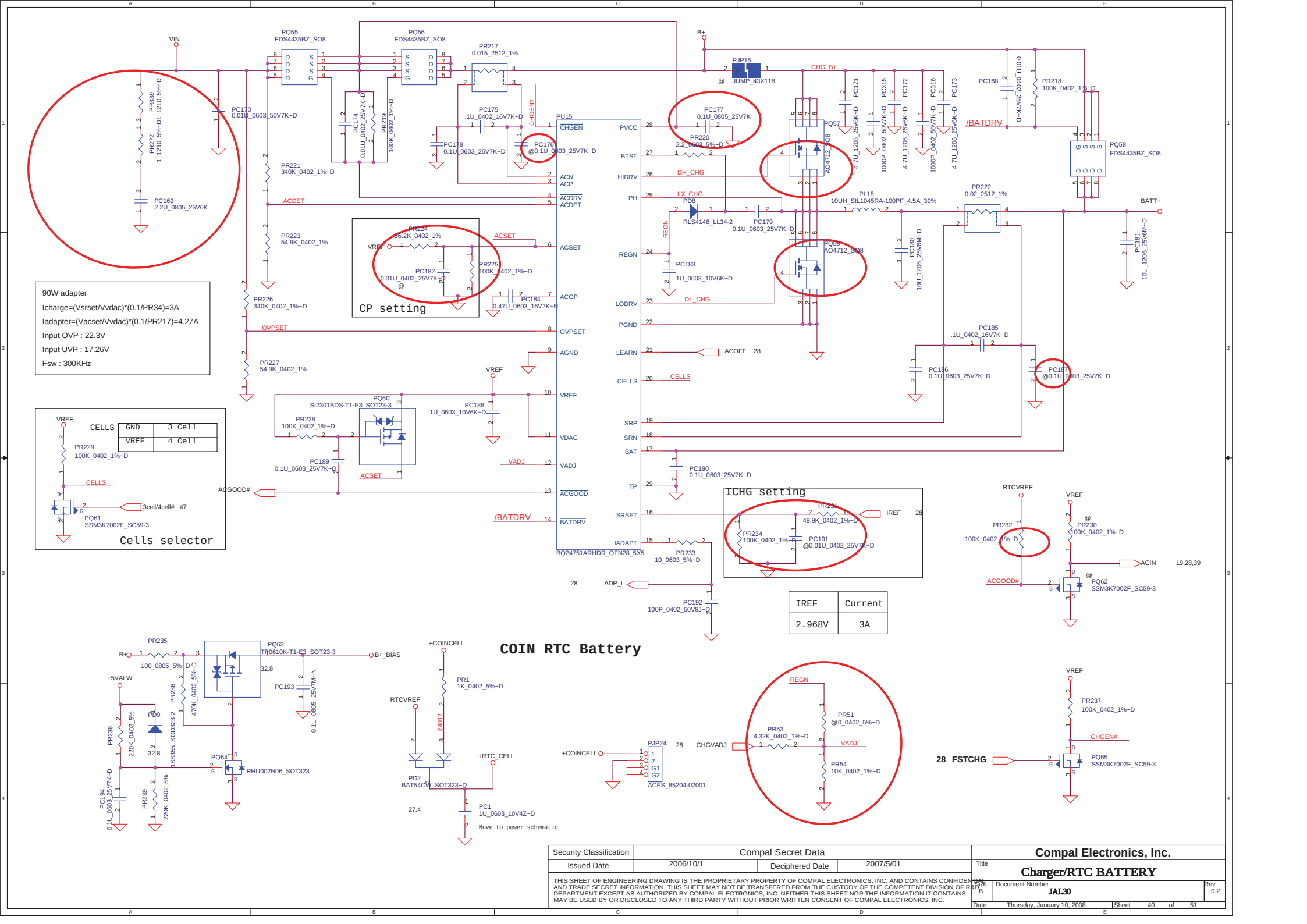


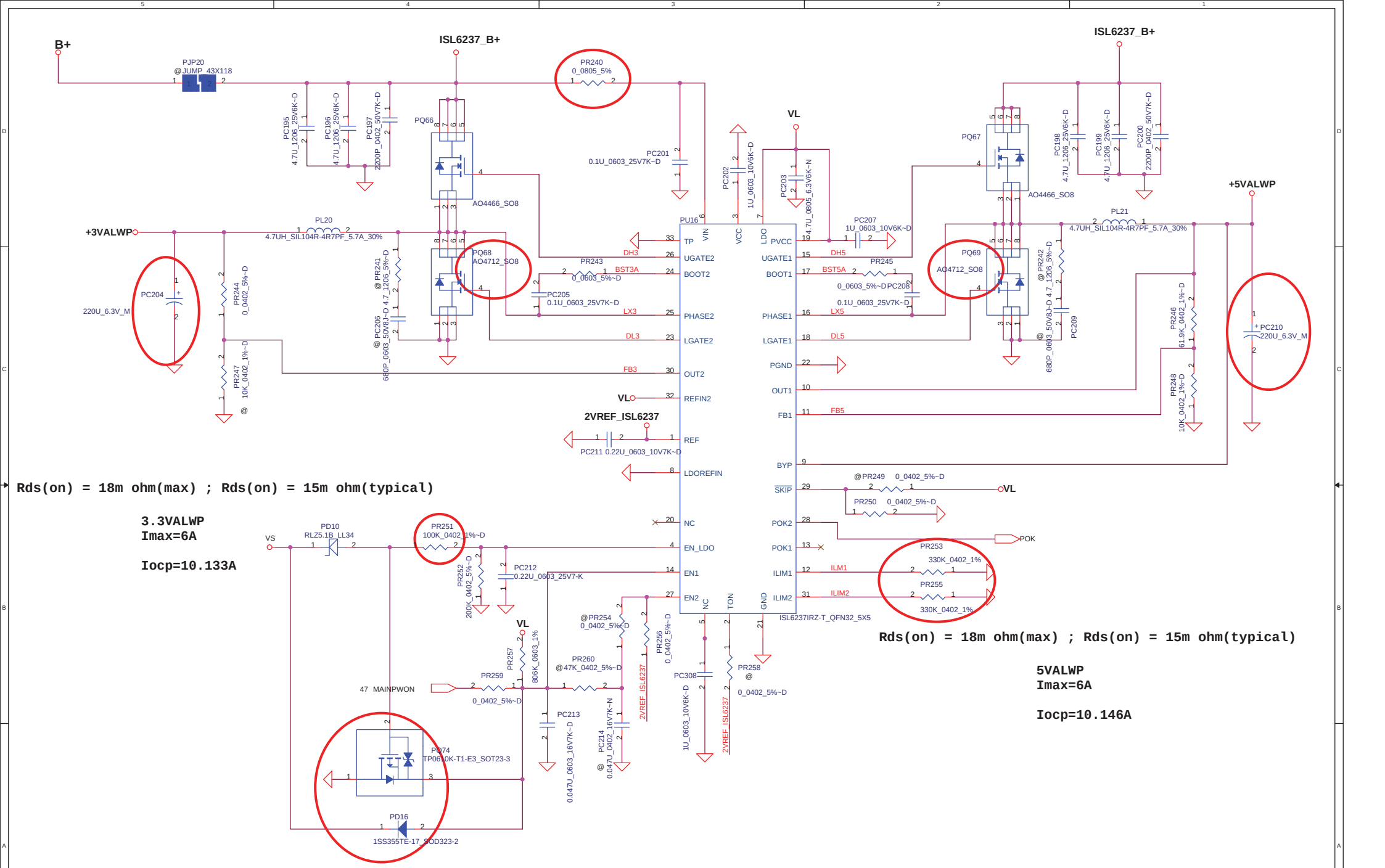
Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Title: **DCIN / Precharge**

Size	Document Number	Rev
Custom	JAL30	0.2

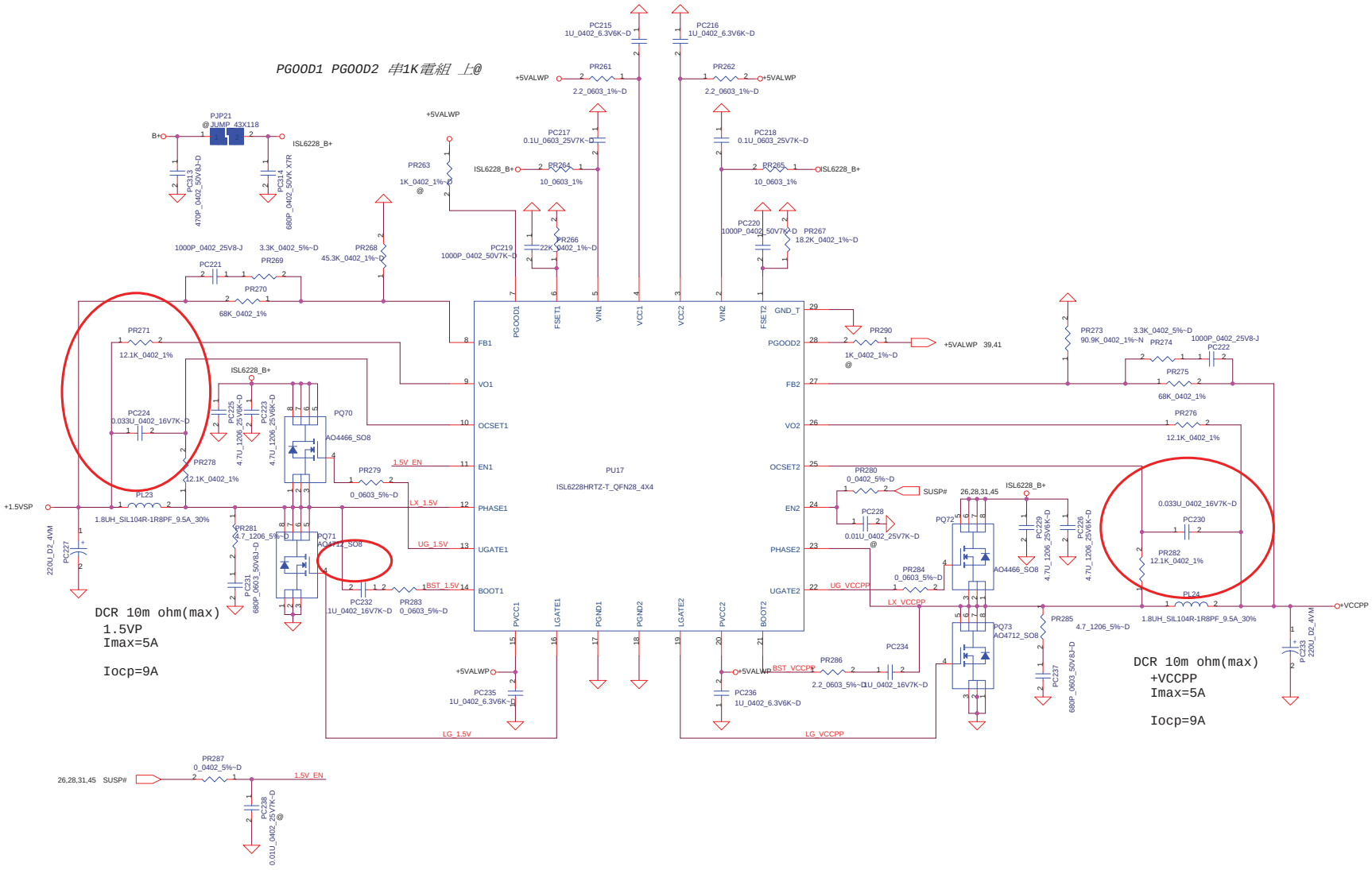
Date: Thursday, January 10, 2008 Sheet 39 of 51


90W adapter
Icharge=(Vsrset/Vvdac)*(0.1/PR34)=3A
Iadapter=(Vacset/Vvdac)*(0.1/PR217)=4.27A
Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz
CP setting
ICHG setting
Cells selector
CELLS GND 3 Cell
VREF 4 Cell
IREF Current
2.968V 3A
COIN RTC Battery
Move to power schematic
BQ24751ARHDR_QFN28_5X5
Security Classification
Compal Secret Data
Issued Date
2006/10/1
Deciphered Date
2007/5/01
Compal Electronics, Inc.
Charger/RTC BATTERY
Document Number
JAL30
Rev
0.2
Date: Thursday, January 10, 2008
Sheet 40 of 51



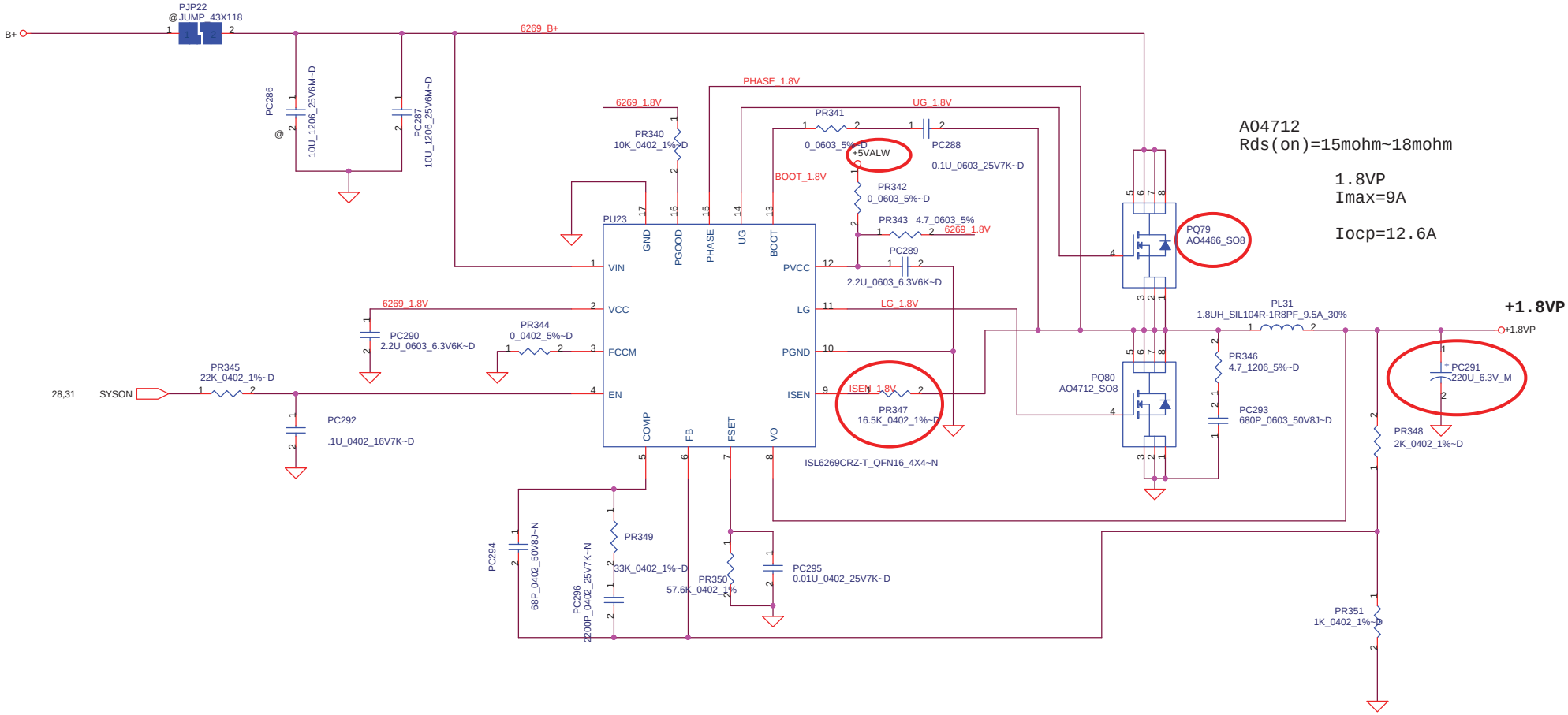
Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.			
Title: +3VALWP, +5VALWP			
Size: Custom	Document Number: JAL30		Rev: 0.2
Date: Thursday, January 10, 2008	Sheet 41 of 51		



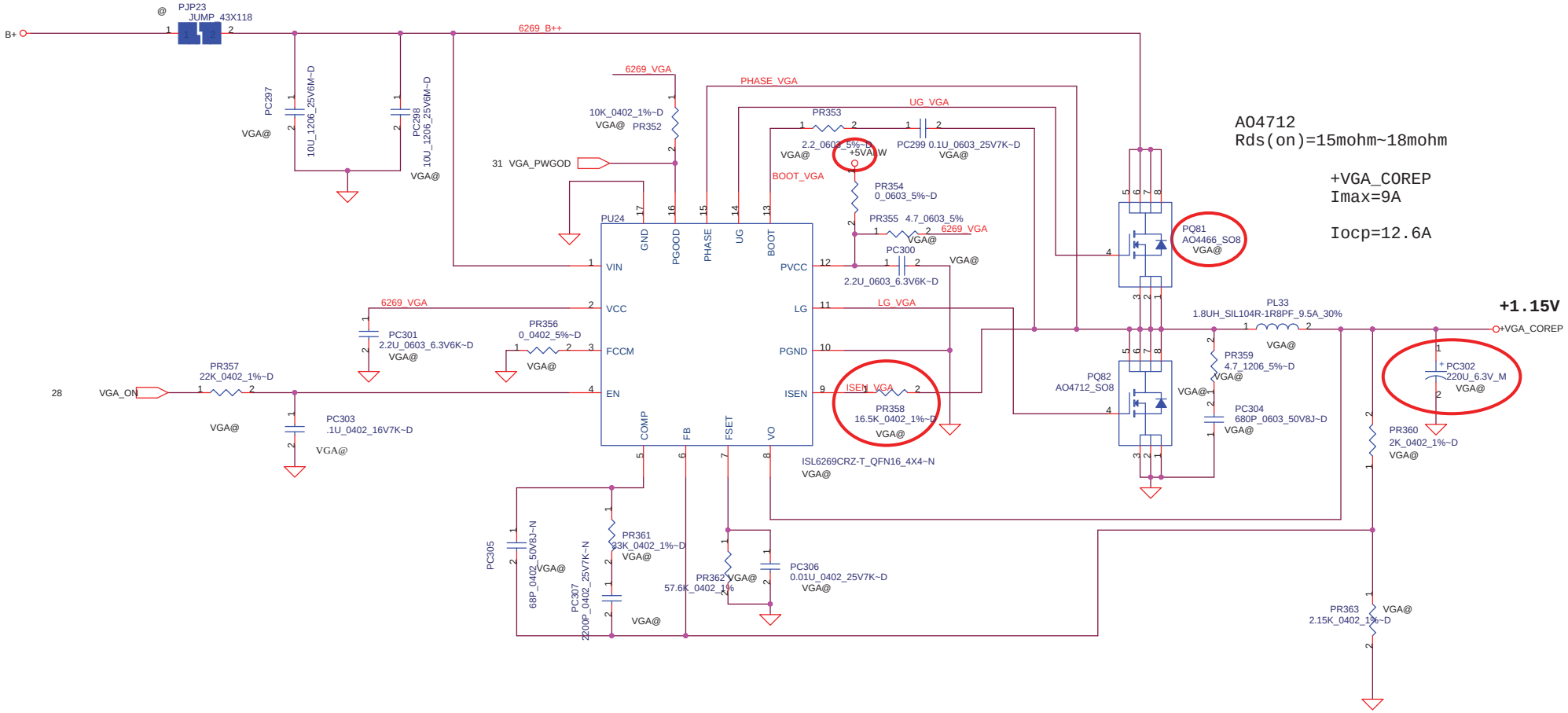
Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Title	+1.5VP/VCCPP		
Size	Document Number	JAL30	Rev 0.2
Date:	Thursday, January 10, 2008	Sheet 42 of 51	

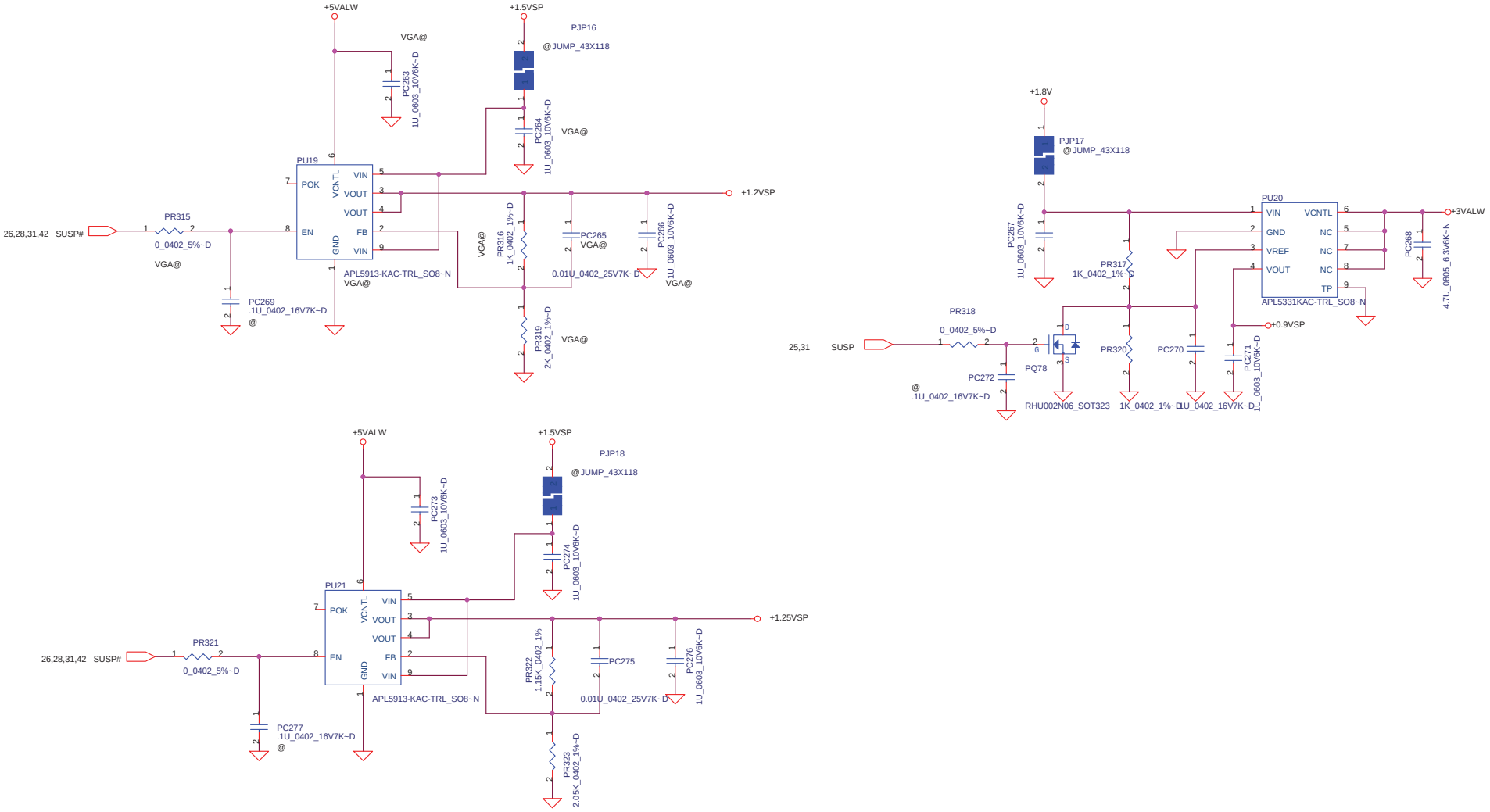


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2006/10/1	Deciphered Date	2007/05/30

Title	NB_CORE		
Size	Document Number		Rev
	JAL30		0.11
Date:	Thursday, January 10, 2008	Sheet	43 of 51



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2006/10/1	Deciphered Date	2007/05/30
Title	+VGA_COREP		
Size	Document Number	JAL60	Rev 0.11
Date:	Thursday, January 10, 2008	Sheet 44 of 51	



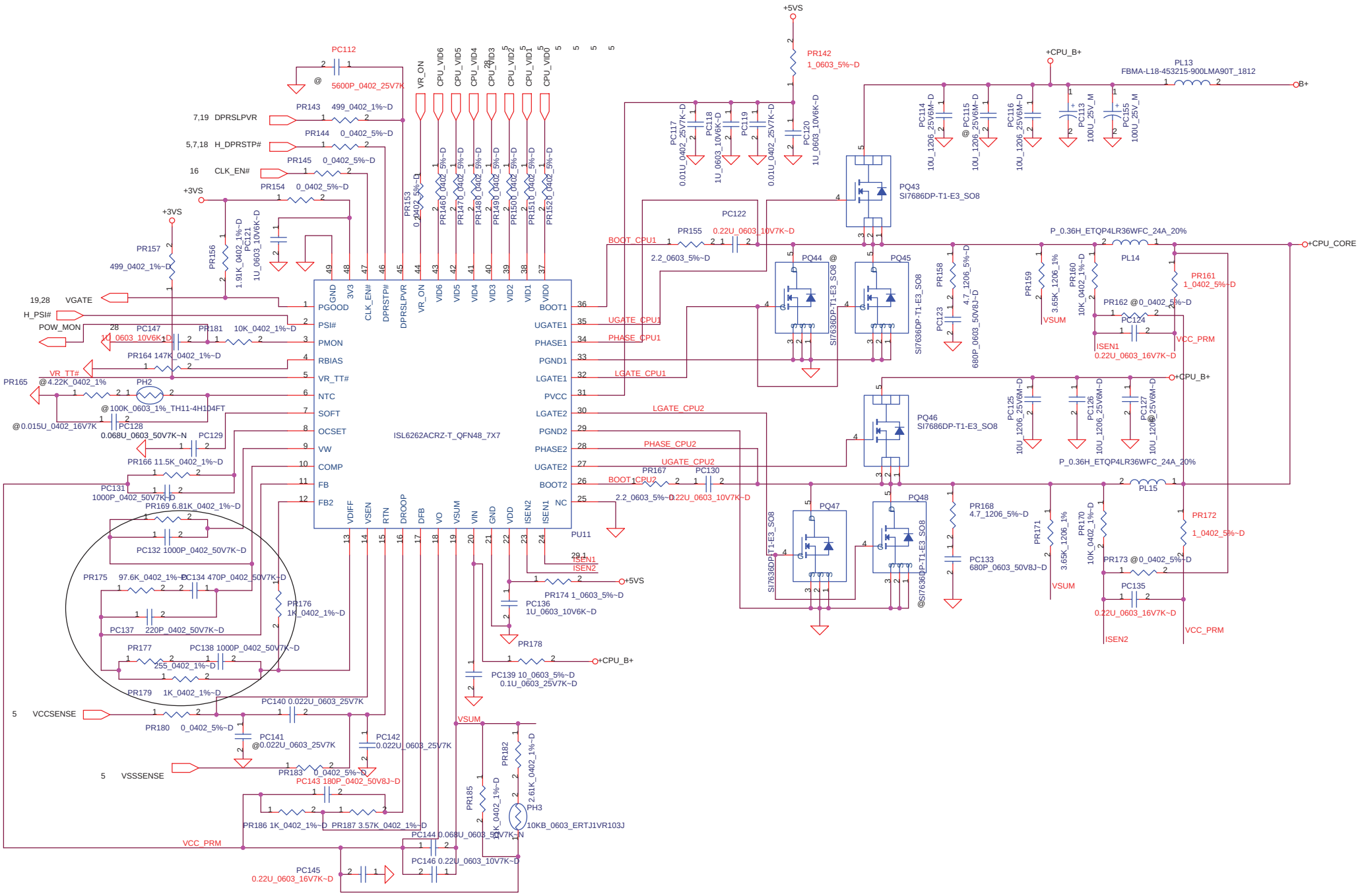
Security Classification	Compal Secret Data		
Issued Date	2005/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.

Title: **+1.25VSP / +0.9VSP/ +1.2VSP**

Size	Document Number	Rev
Custom	JAL30	0.2

Date: Thursday, January 10, 2008 Sheet 45 of 51



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

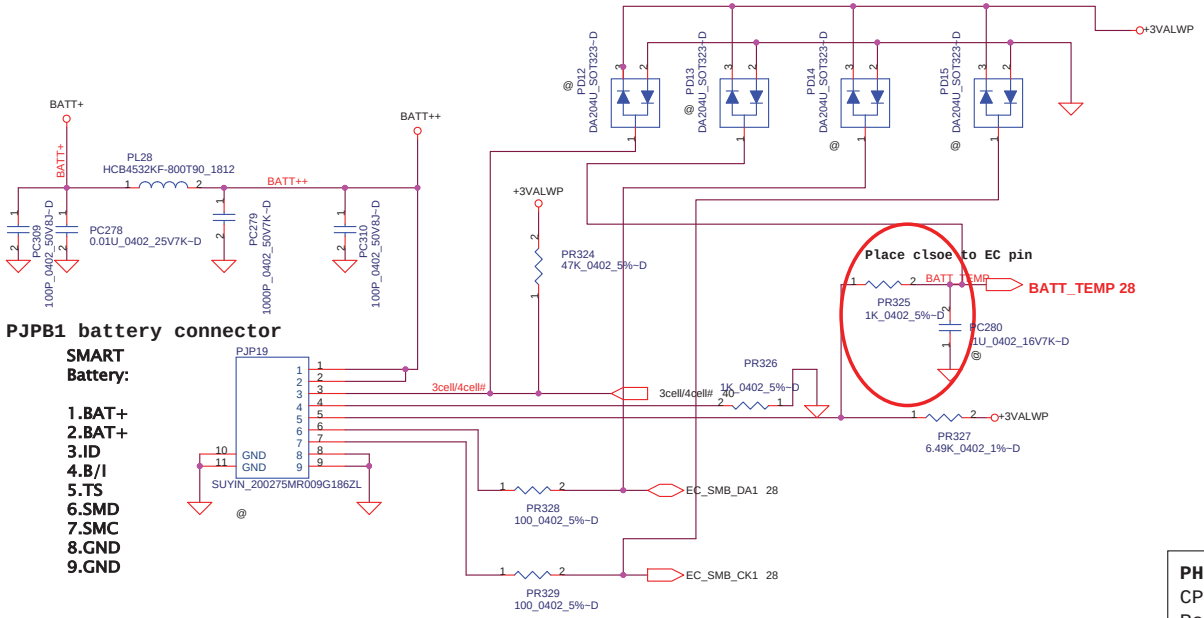
Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom	JAL30	0.1

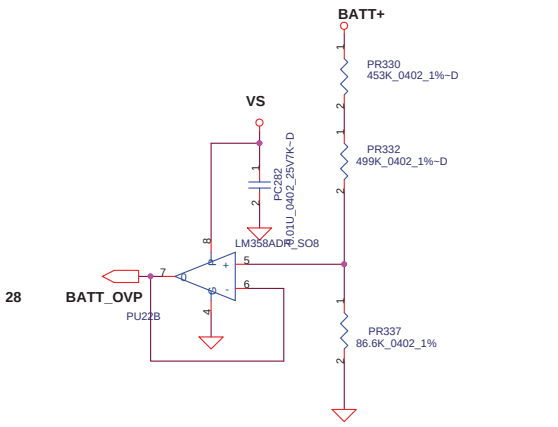
Date: Thursday, January 10, 2008 | Sheet 46 of 51

Battery Connect/OTP

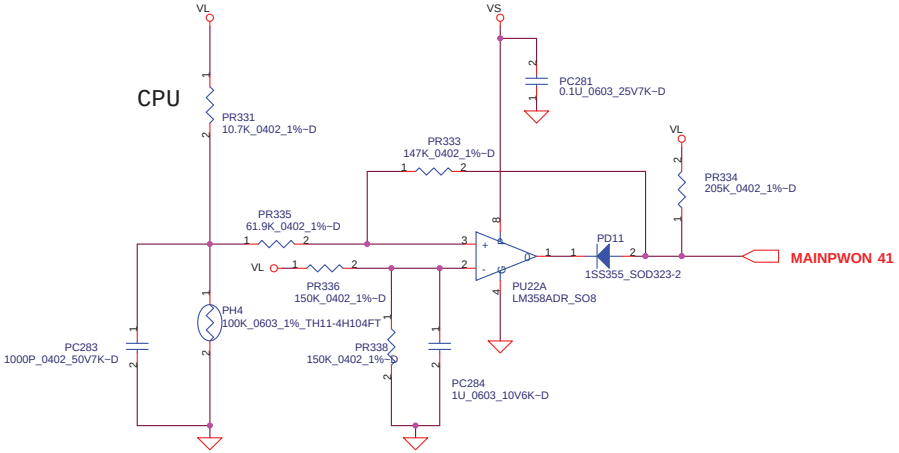


CPU

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C



LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.111*BATT+



Security Classification	Compal Secret Data		
Issued Date	2005/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.

Title	BATTERY CONN		
Size: Custom	Document Number: JAL30		Rev: 0.2
Date: Thursday, January 10, 2008	Sheet 47 of 51		

Version Change List (P. I. R. List) Page 1/1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	+3VALWP/+5VALWP	07/11/19	COMPAL	When in the DC-mode , shut down the system ,5valwp output not turn off	ADD PQ76 to turn off 5VALWP wehn shut down the system in the DC-mode	
2	40	Charge	07/11/25	COMPAL	Change RTC circuitry part	del PD16 PC285 PL29 JRTC1	
3	40	Charge	07/11/25	COMPAL	change charge voltage can to adjust	ADD PR53 PR54	
4	40	Charge	07/11/25	COMPAL	increase Coin RTC battery circuitry	ADD PD2 PR1 PC1	
5	40	Charge	07/11/25	COMPAL	increase BQ24751 Vin Detector function	increase PR232	
6	40	Charge	07/12/26	COMPAL	change charge voltage can to adjust	Change PR53 from 15K to 4.3K	
7	42	1.5VSP/+VCCPP	07/12/26	COMPAL	adjust 1.5VSP/+VCCPP OCP set	Change PR271 PR276 PR278 PR282 from 9.09K to 12.1K	
8	43	1.8VP	07/12/26	COMPAL	adjust 1.8VP OCP set	Change PR347 from 12.1K to 16.5K	
9	44	VGA_CORE	07/12/26	COMPAL	adjust VGA_CORE OCP set	Change PR358 from 12.1K to 16.5K	
10	41	+3VALWP/+5VALWP	07/12/26	COMPAL	The schematic location doesn't correspond to PCBA	Change location from PQ76 to PQ74	
11	43	1.8VP	07/12/26	COMPAL	delete resistor 0ohm for HW request	DEL PR342	
12	44	VGA_CORE	07/12/26	COMPAL	delete resistor 0ohm for HW request	DEL PR354	
13	46	CPU_CORE	07/12/26	COMPAL	modify MOS type SO8 to Power Pack for height limit	DEL PQ44 PQ48	
14	43	1.8VP	08/01/04	COMPAL	In order to replace IC for system request	ADD PU23 PR342	
15	44	VGA_CORE	08/01/04	COMPAL	In order to replace IC for system request	ADD PU24 PR354	
16	41	+3VALWP/+5VALWP	08/01/04	COMPAL	When in the DC-mode , shut down the system ,5valwp output not turn off	ADD PD16 to turn off 5VALWP wehn shut down the system in the DC-mode	
17	40	Charge	08/01/04	COMPAL	adjust battery charge voltage set	CHANGE PR53 from 15K to 4.3K	
18	40	Charge	08/01/04	COMPAL	VIN Detector has the same function	DEL PR230 PQ62	
19							
20			08/01/04	COMPAL	Increase Resistor on charge boot for EMI request	CHANGE PR220 PR286from 0 to 2.2 ohm	
21			08/01/04	COMPAL	Increase Capacitor on charge boot for EMI request	ADD PC123 PC133 PC231 PC237 PC309 PC310 PC311 PC313 PC312 PC314 PC293	
22			08/01/04	COMPAL	Increase Resistor on charge boot for EMI request	ADD PR158 PR168 PR285 PR281 PR346	
23			08/01/04	COMPAL	Increase Bead on charge boot for EMI request	ADD PL17 PL28	
24							
25							
26							
27							
28							
29							
30							
31							
32							

Compal Electronics, Inc.

Title: PW PIR-1

Size: Custom | Document Number: LA-3682P | Rev: 0.1

Date: Thursday, January 10, 2008 | Sheet 48 of 51

Version Change List (P. I. R. List) Page 1/1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	24	P24-Mini-Card/WWAN/Roboson	2007/2/3	Compal HW	LED1 Pin3 and Pin4 swap cause BATT_LOW_LED# no function.	Correct LED1 footprint to LED_HT-297UD-CB_4P	0.2 (SW1-13.3")
2	22	P22-Gigabit LAN(BCM5787M)	2007/2/3	Compal HW	+3VLAN voltage abnormally	Add Q46 for B+_BIAS turn on	0.2 (SW1-13.3")
3	19	P19-ICH8(3/4)_DMI,USB,GPIO,PCIE	2007/2/3	Compal HW	R121 no need for INTEL no reserve	Un mount R121	0.2 (SW1-13.3")
4	19	P22-Gigabit LAN(BCM5787M)	2007/2/13	Compal HW	Can't install MAC to EEPROM due to VCC 2.04V only	Change R4 to 0ohm or short R4.	0.2 (SW1-13.3")
5	29	P29-EC KB926/REED SW/TPM1.2	2007/3/1	Compal HW	KB matrix error by use AK1 KB circuit	Modify to SW1 KB pin define	0.2 (SW1-13.3")
6	27	P27-CardBus/R5C803	2007/3/1	Compal HW	CB_PME# pull high of two kind power plan (+3V & +3V_SB)	Un-mount R419	0.2 (SW1-13.3")
7	32	P32-DC/DC Interface	2007/5/11	Compal HW	No VGAPOWERGOOD for turn on +1.8VS	Add pull hish +3VS for VGA_PWGOD	0.2
8	11	P11-CRESTLINE(5/6)-PWR/GND	2007/5/11	Compal HW	VCCP no power	Remove C140(0 ohm in VGA BOM)	
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							
24	4						
25							
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28							
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30							
31							
32							

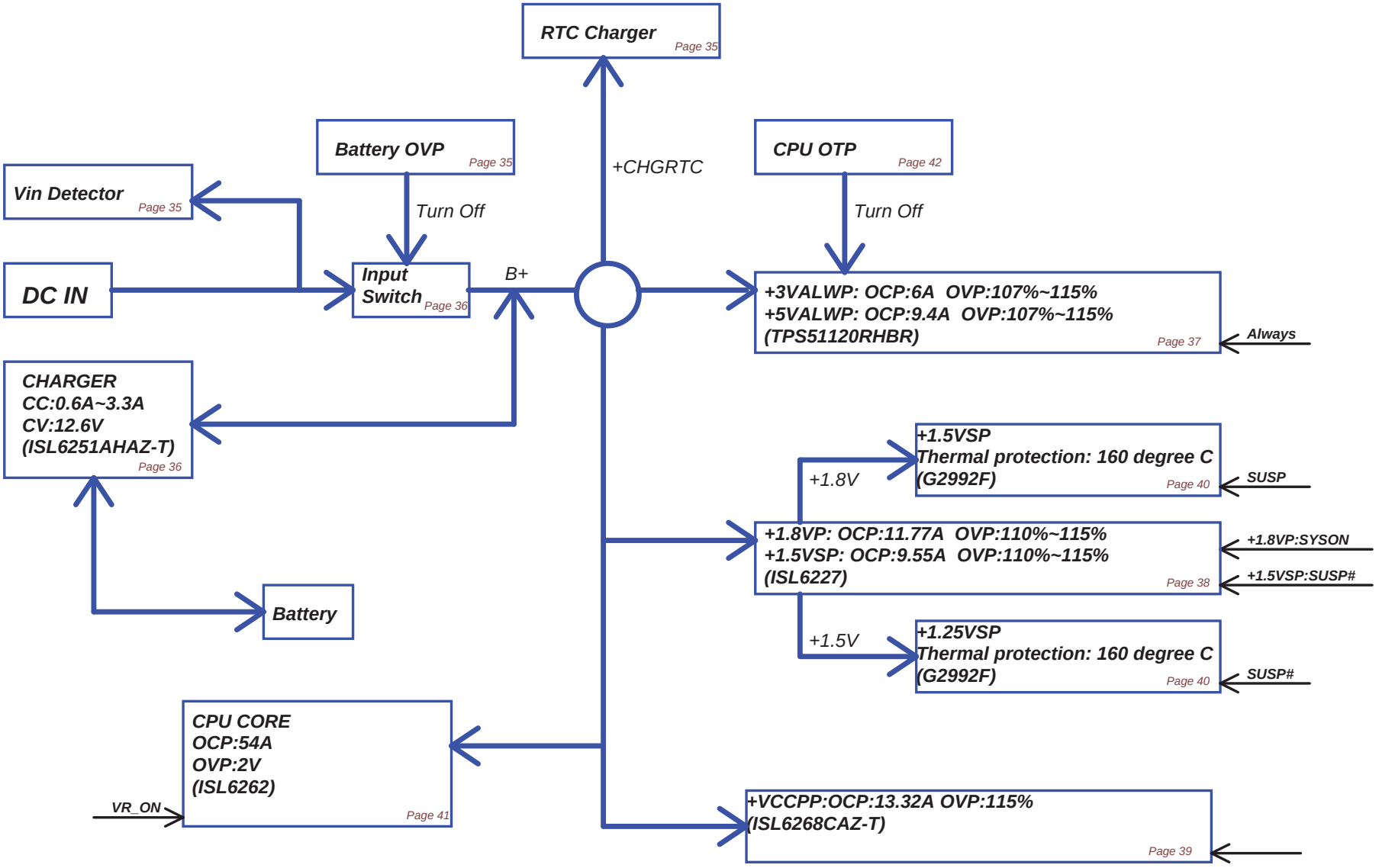
Compal Electronics, Inc.

Title: EE PIR-1

Size: Custom | Document Number: LA-4121P | Rev: 0.4

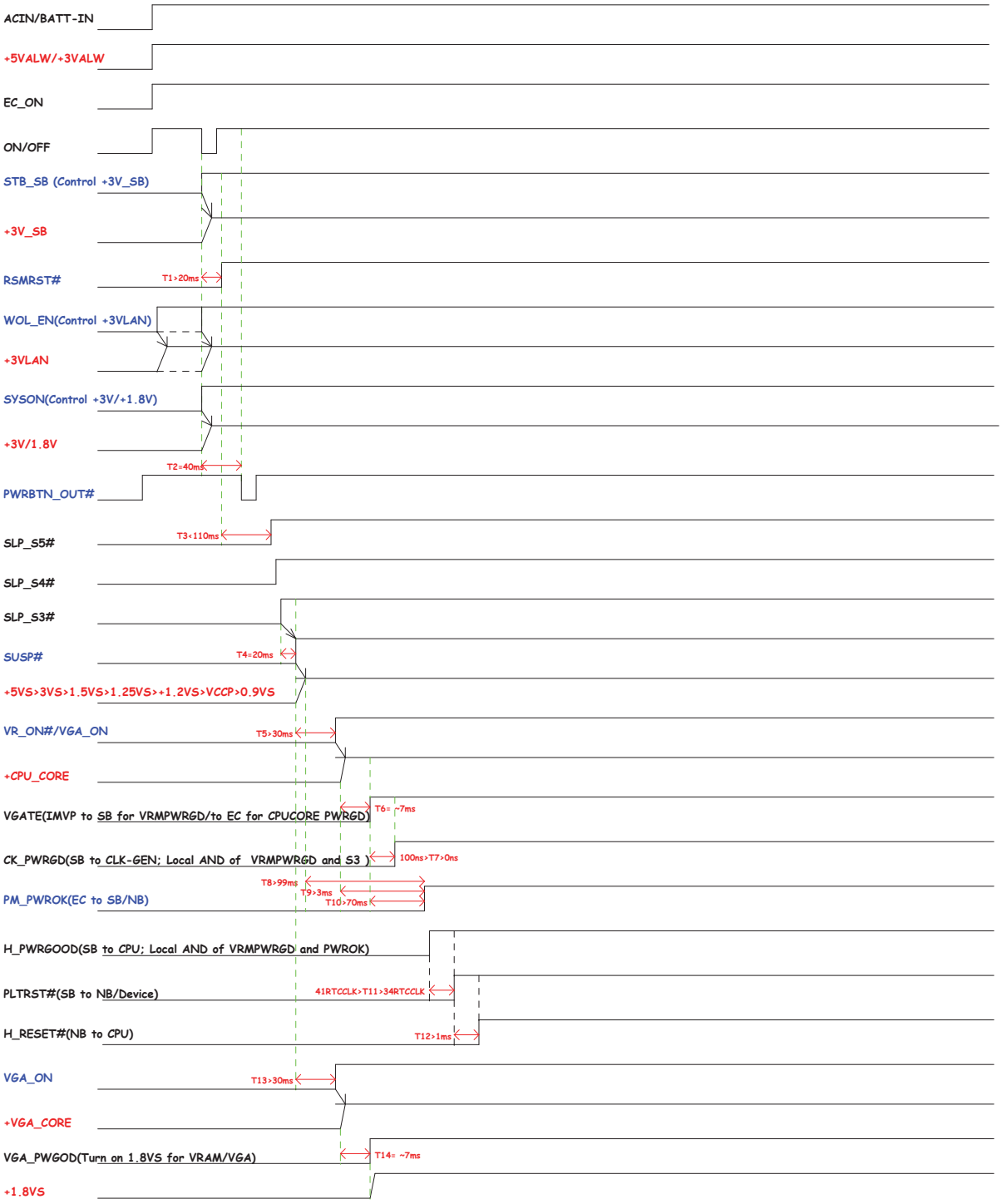
Date: Thursday, January 10, 2008 | Sheet 49 of 51

JAL30 Power Bock



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Title	Power Block		
Size: Custom	Document Number: LA-4121P		Rev: 0.4
Date: Thursday, January 10, 2008	Sheet 50 of 51		



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Title: *Power On Sequence*

Size	Document Number	Rev
Custom	*LA-4121P*	0.4
Date: Thursday, January 10, 2008	Sheet 51 of 51	