

Compal Model Name: KML60
PCB NO: LA-4671P R03(X02)
BOM P/N: 46161631L01 (DIS)
46161631L02 (UMA)
Function Field: @ unpop
UMA@ UMA component
VGA@ discrete component
CONN@ ME connector
TPM@ TPM component

Half Penny Bridge 17"

Compal Confidential

Schematic Document

Cantiga + ICH9

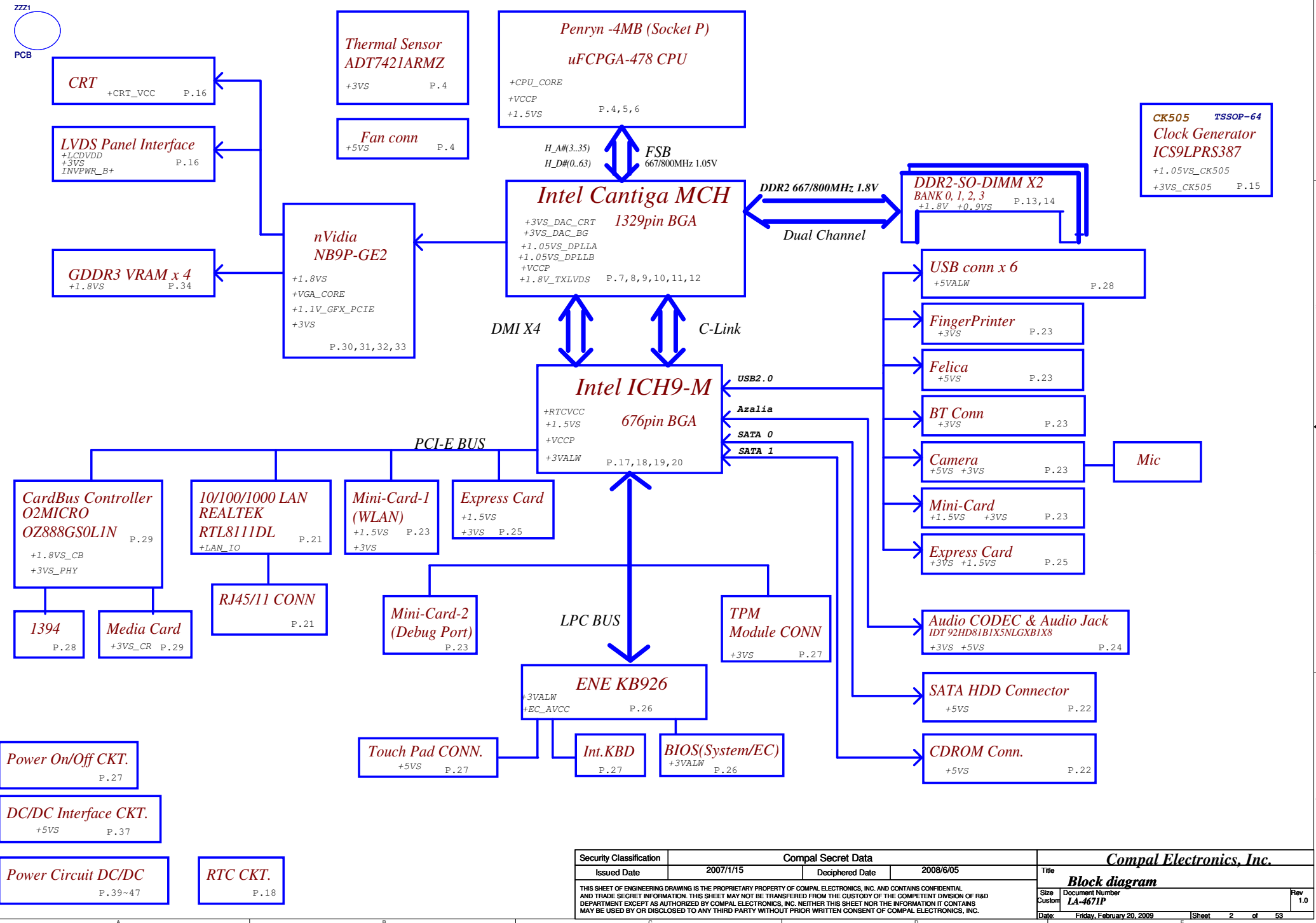
2009 / 2 / 19 Rev:1.0 (A00)

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Compal confidential

File Name : LA-4671P

Half Penny Bridge17



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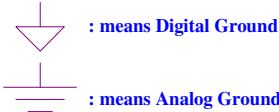
Voltage Rails

O MEANS ON X MEANS OFF

power plane	+B	+5VALW	+1.8V	+5VS
				+3VS
State		+3VALW		+1.5VS
				+0.9V
				+VCCP
				+CPU_CORE
				+VGA_CORE
				+2.5VS
				+1.8VS
				+1.2VS
				+0.9VGA
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

ICH9-M	USB PORT#	DESTINATION
	0	JUSBP1
	1	CAMERA
	2	JUSBP3
	3	Felica
	4	Blue Tooth
	5	Finger Printer
	6	JMINI2-WLAN
	7	Express card
	8	JUSBP3
	9	JMINI1-WWAN
	10	JUSBP4
	11	NA

Symbol Note :



@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	115K +/-1%	1.6613 V	1.7651 V	1.8706 V
1	154K +/-1%	1.8857 V	2.0008 V	2.1173 V
2	215K +/-1%	2.1261 V	2.2524 V	2.38 V
3	316K +/-1%	2.3948 V	2.5067 V	2.6447 V
4	560K +/-1%	2.6519 V	2.8 V	2.9488 V
5	NC			
6	NC			
7	NC			

PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ886
Lane 6	NA

SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

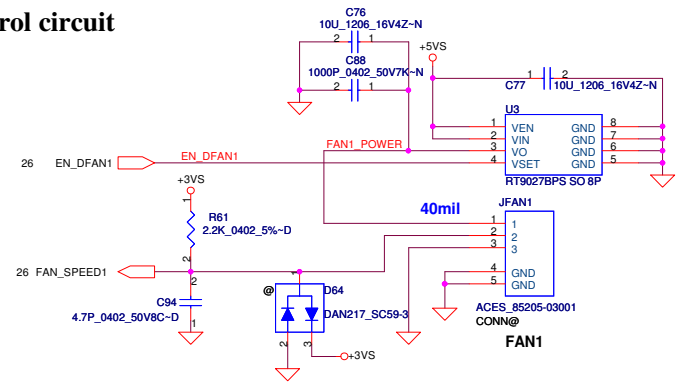
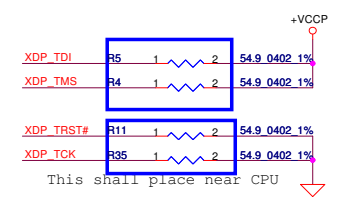
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

SMBUS Control Table

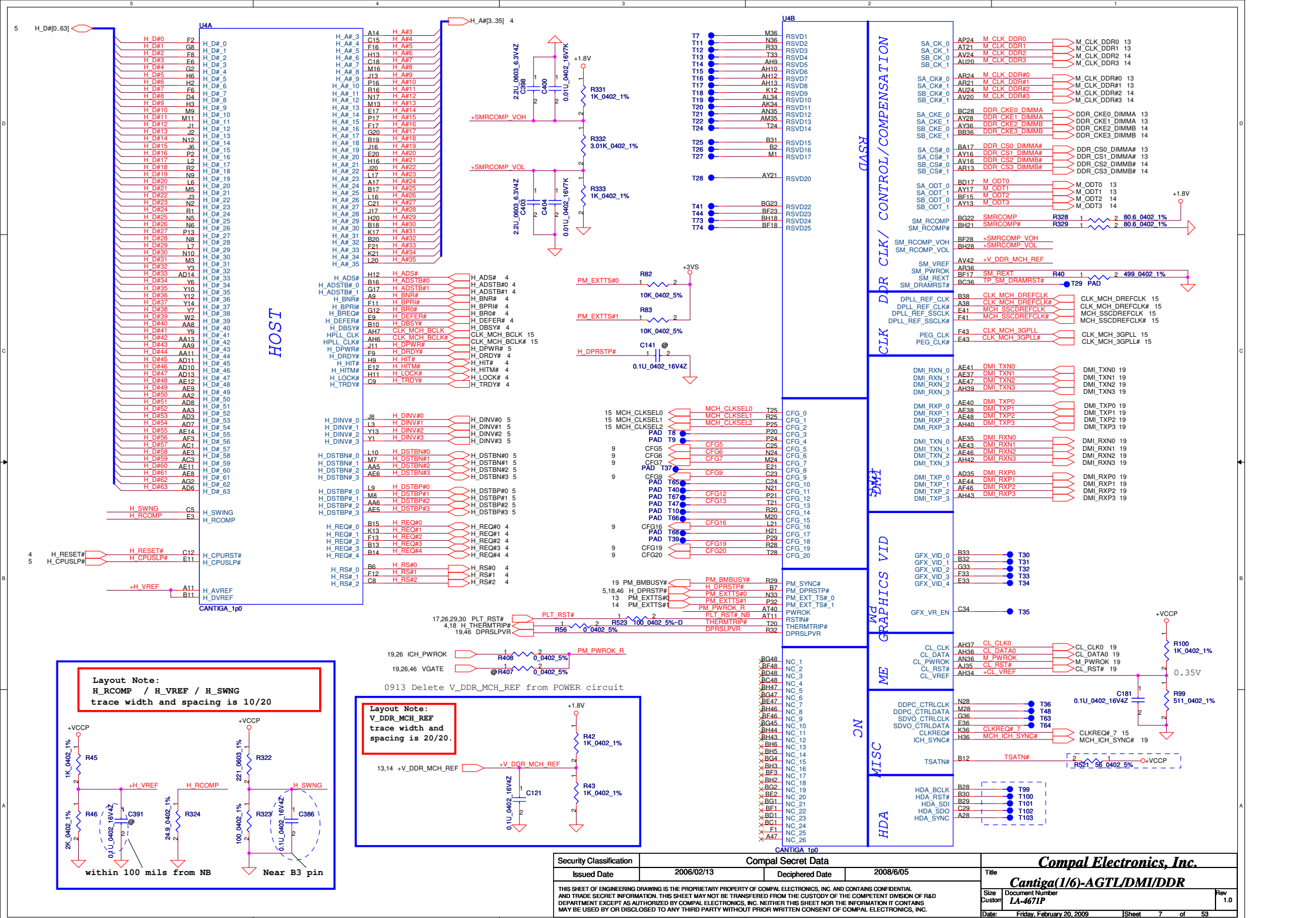
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

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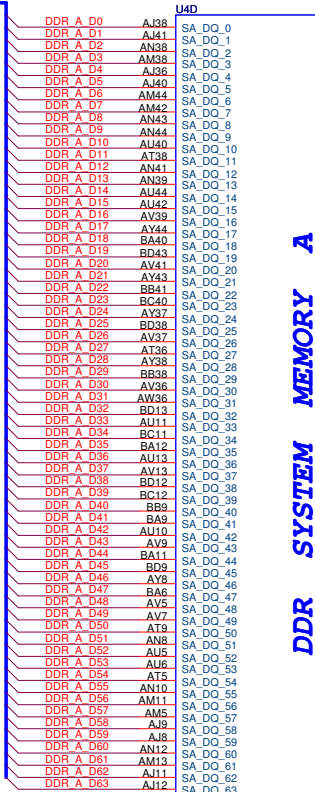


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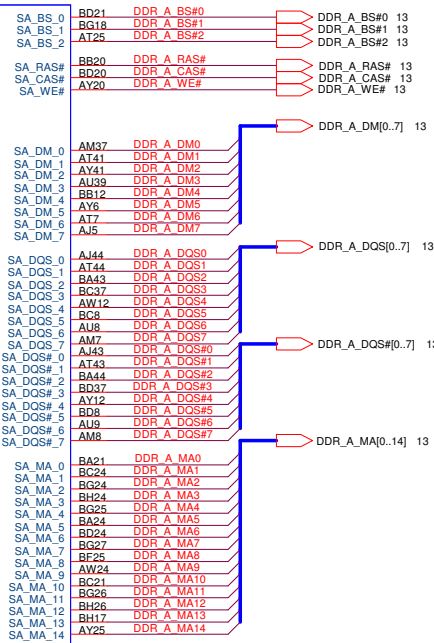
layout note: Rout H_DPRSTP# from ICH9 to IMVP6 then to GMCH & CPU
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPS



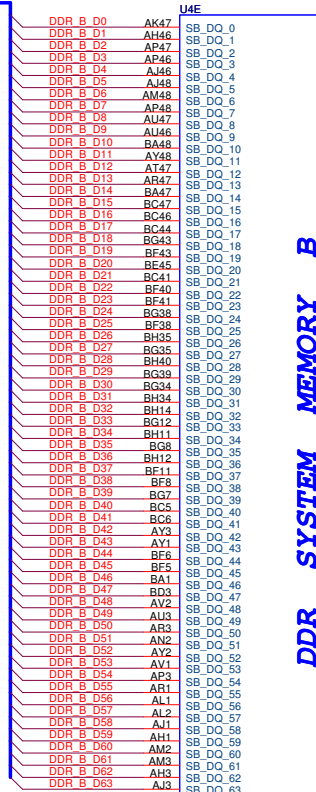
13 DDR_A_D[0..63]



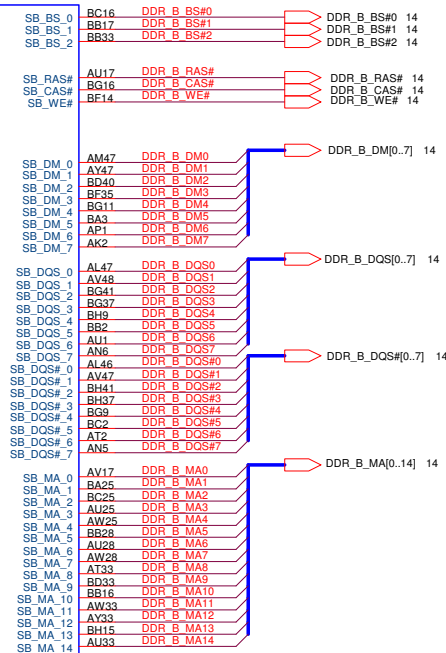
CANTIGA_1p0



14 DDR_B_D[0..63]



CANTIGA_1p0



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CFG[5:16] have internal pullup

CFG5 @ P66 1 2 2.21K 0402 1%-D

CFG6 @ P58 1 2 2.21K 0402 1%-D

CFG7 @ P59 1 2 2.21K 0402 1%-D

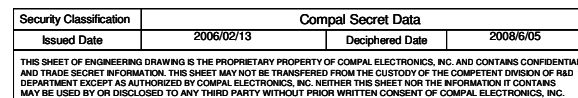
CFG9 @ P55 1 2 2.21K 0402 1%-D

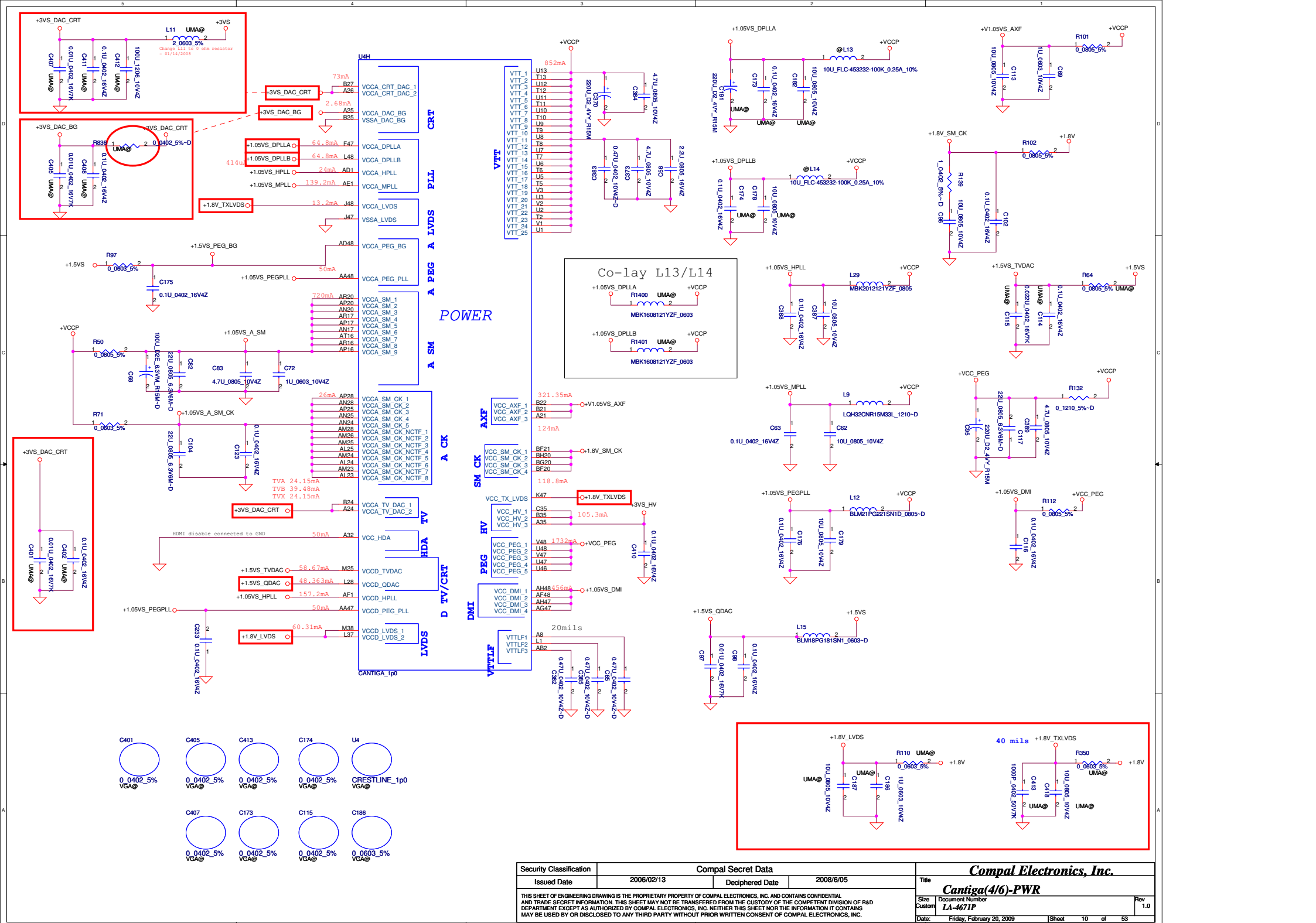
CFG16 @ R70 1 2 2.21K 0402 1%-D

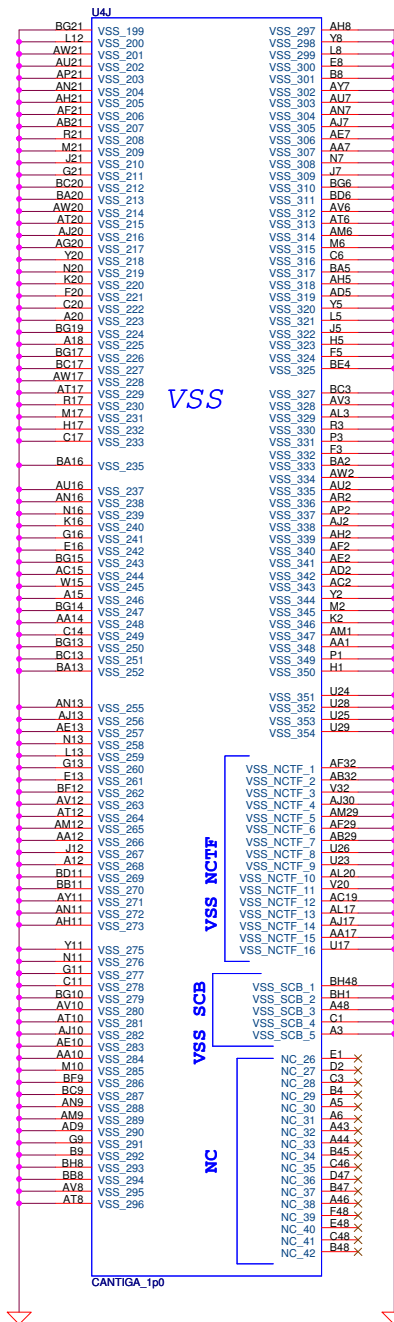
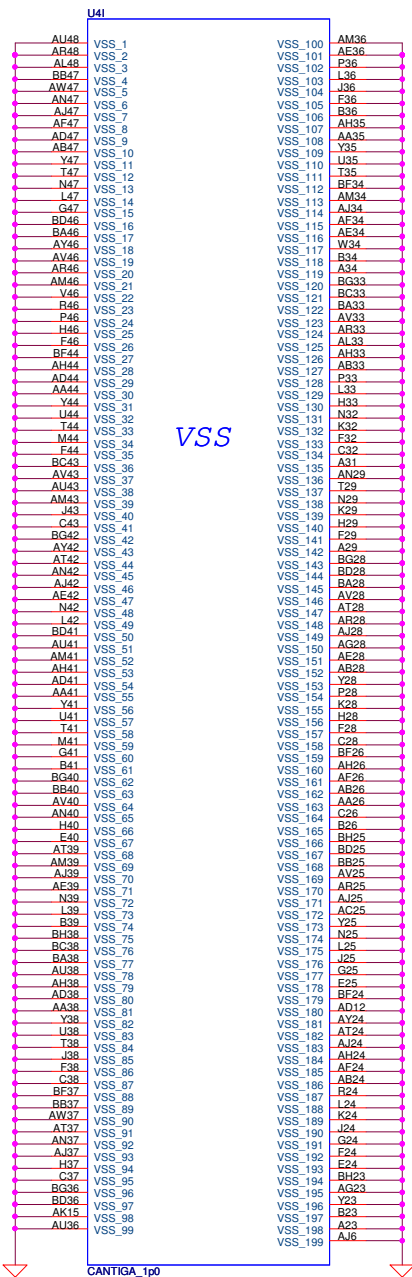
CFG19 @ R72 1 2 4.02K 0402 1%-D

CFG20 @ R73 1 2 4.02K 0402 1%-D

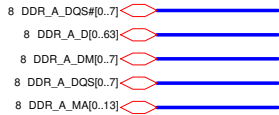
CFG[19:20] have internal pulldown



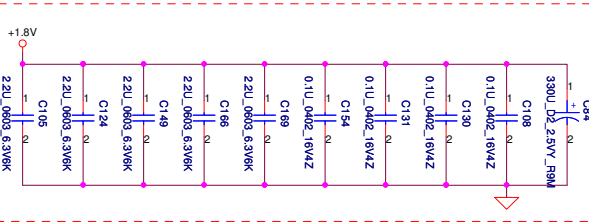




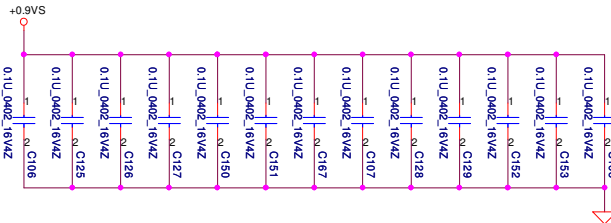
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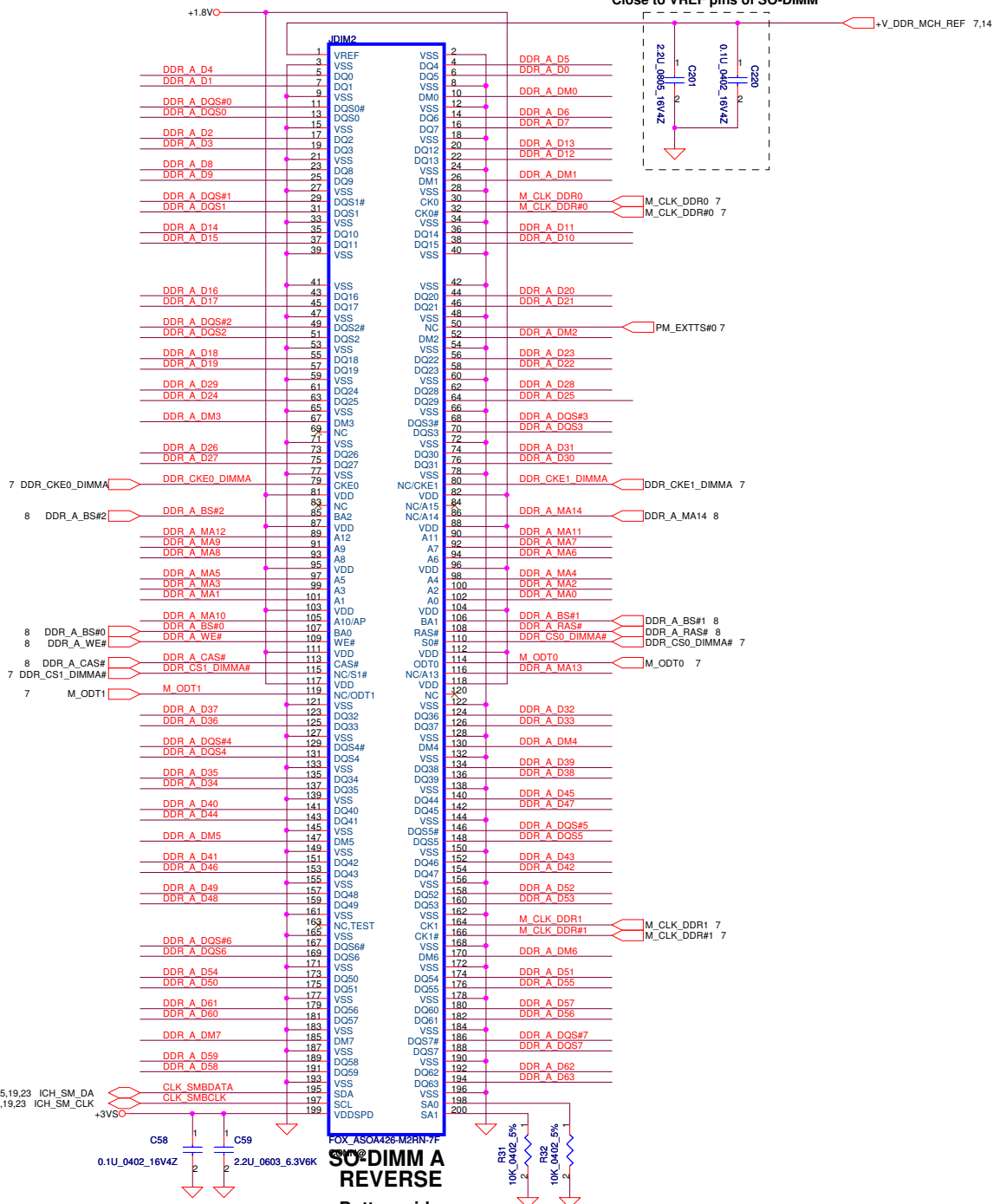
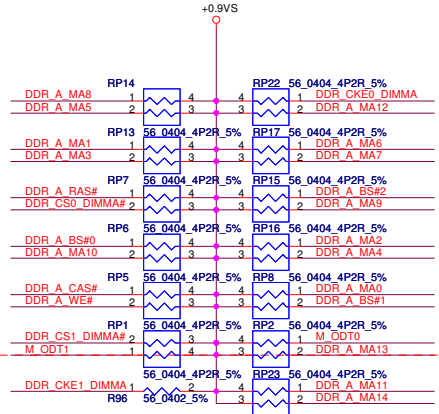
Layout Note:
Place near JDIM2



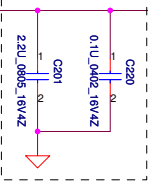
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place these resistor closely JDIM2, all trace length Max=1.5"

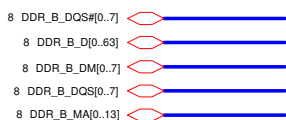


Close to VREF pins of SO-DIMM

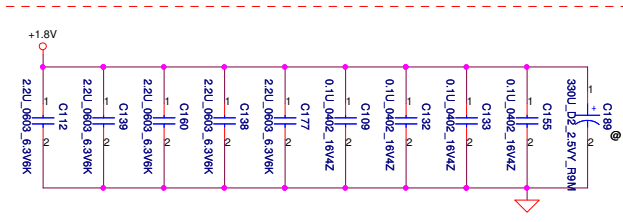


SO-DIMM A
REVERSE
Bottom side

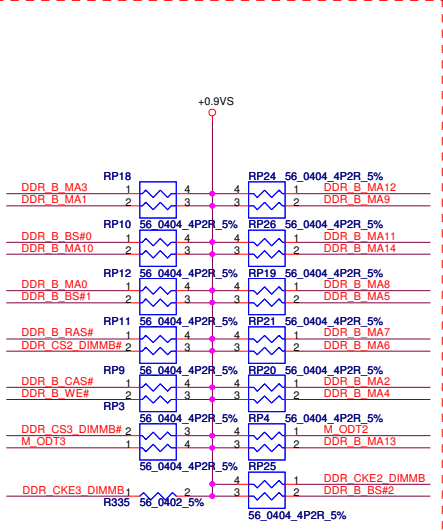
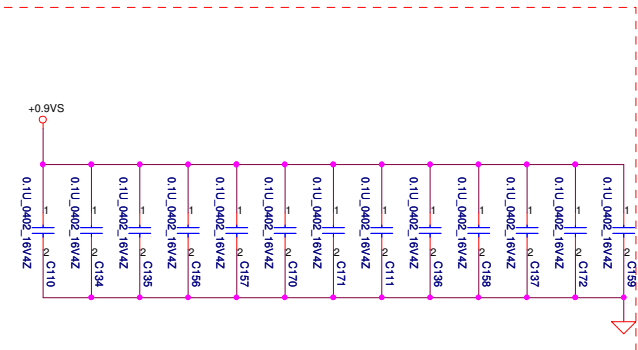
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2007/1/15				2008/6/05				DDR2 SO-DIMM I			
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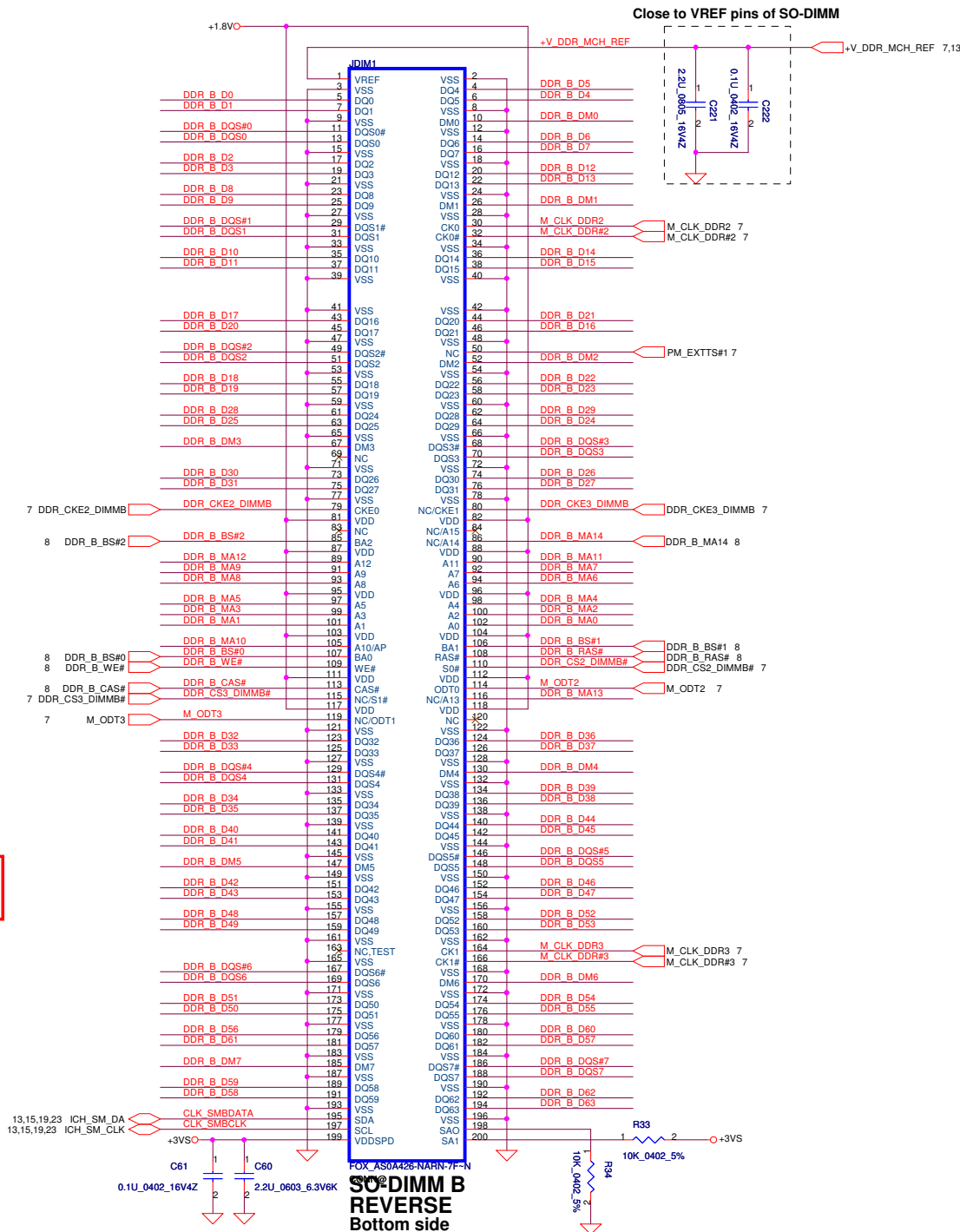
Layout Note:
Place near JDIM1



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS

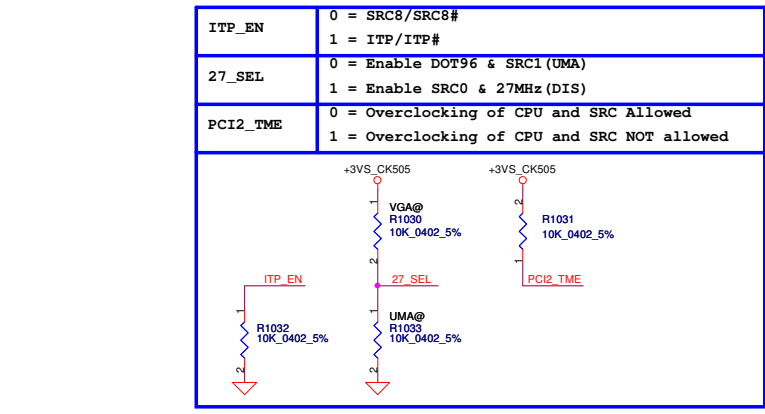
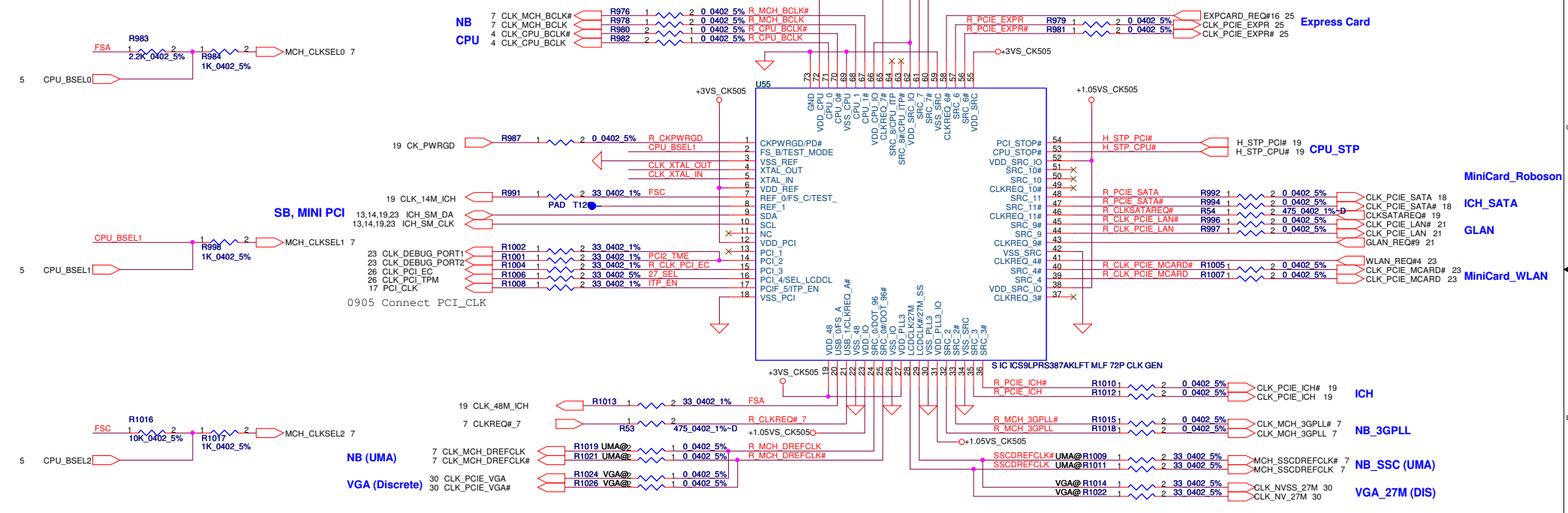


Layout Note:
Place these resistor
closely JDIM1, all
trace length Max=1.5"

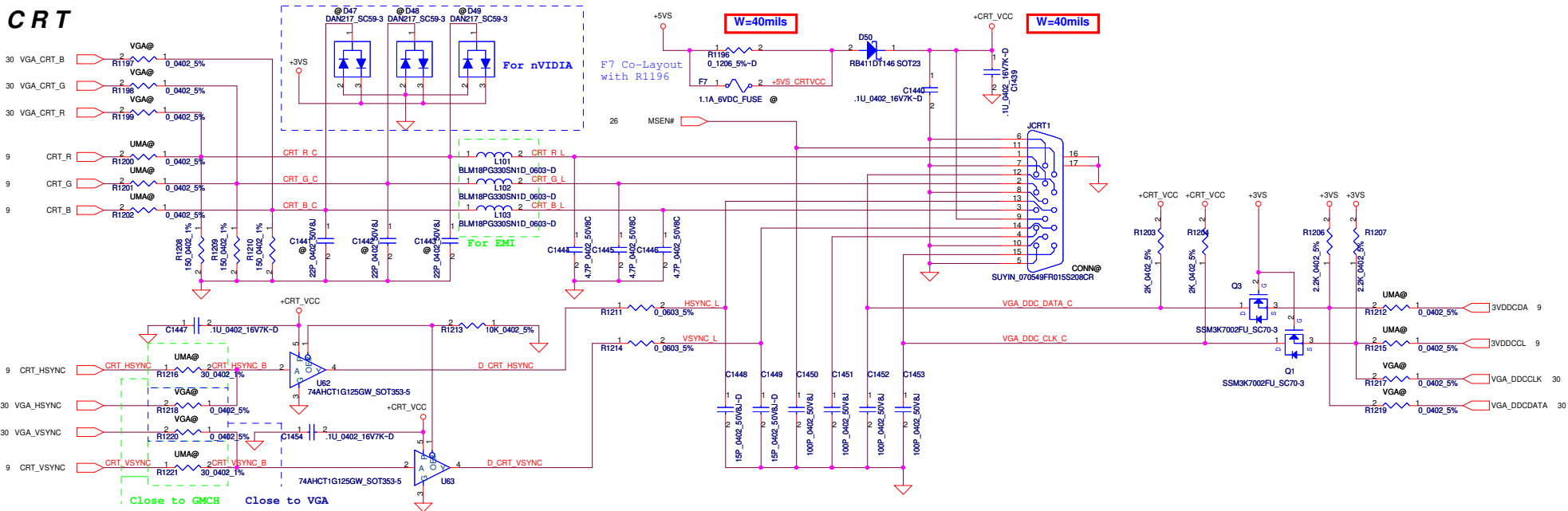


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				DDR2 SO-DIMM II		
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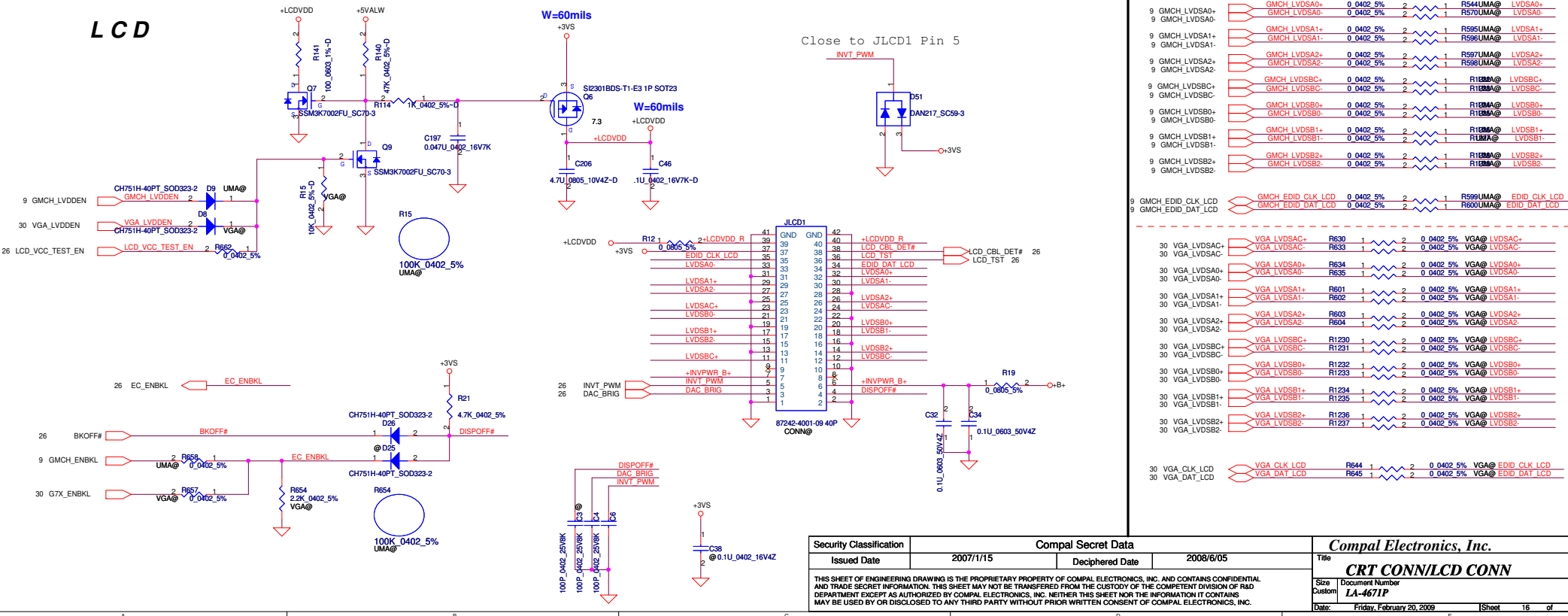
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



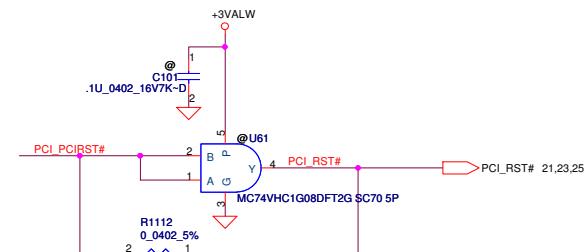
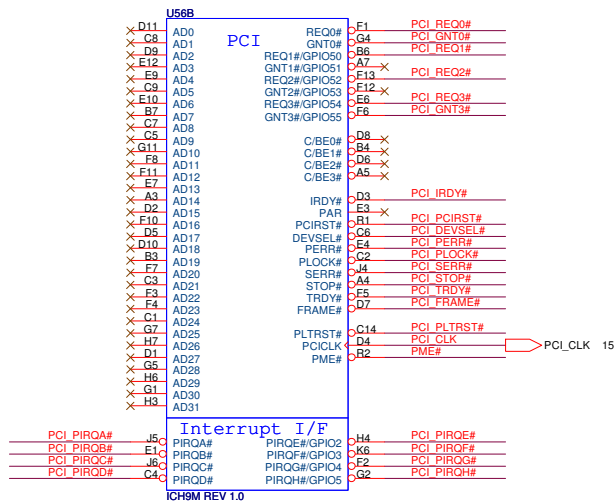
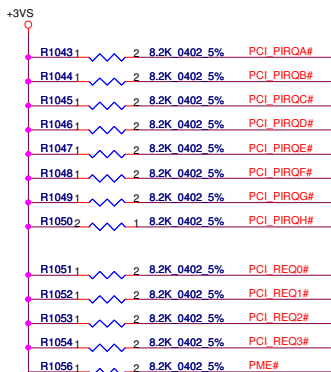
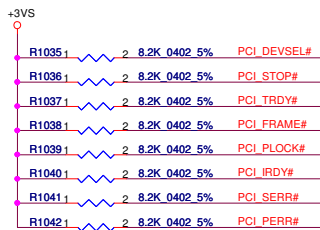
CRT



LCD



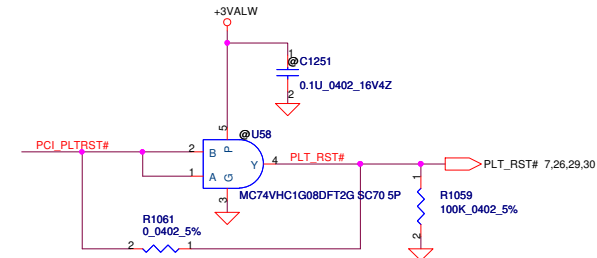
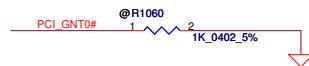
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A16 swap override Strap	
Low= A16 swap override Enble	High= Default*
PCI_GNT3#	

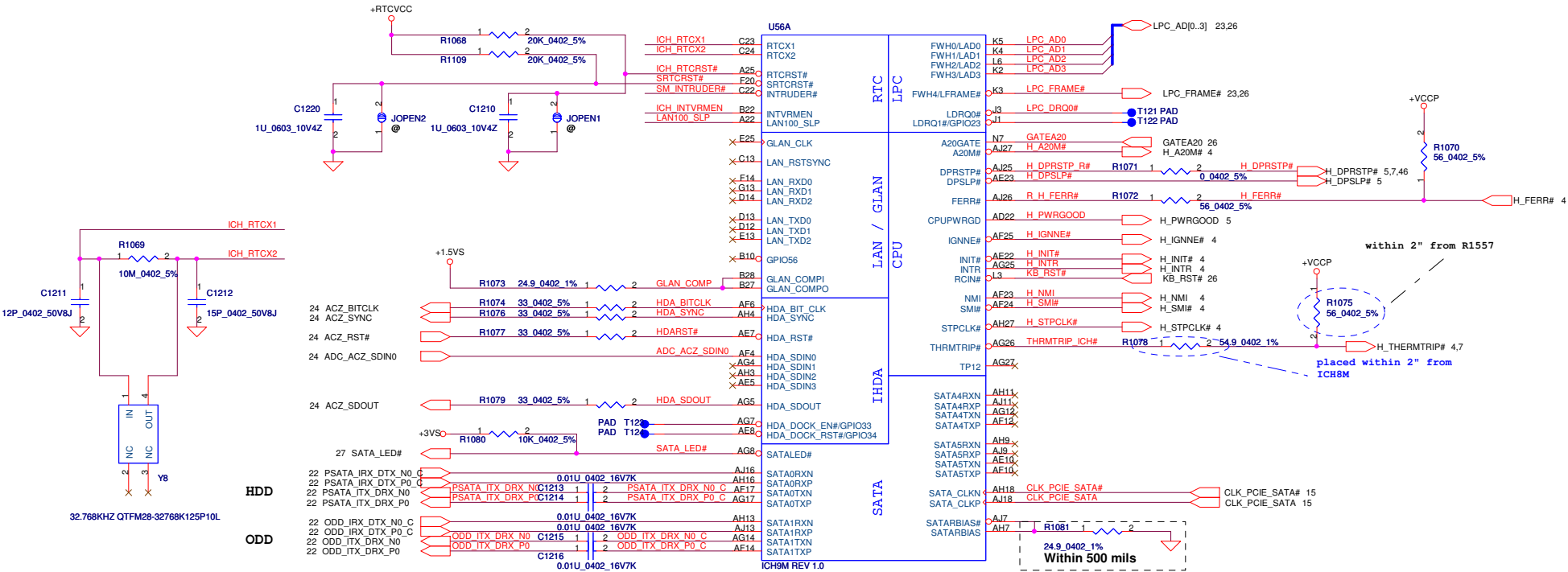
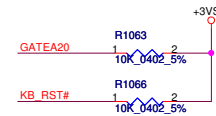
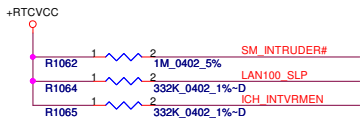


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

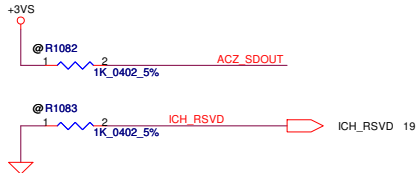


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ICH9(1/4)-PCI/INT

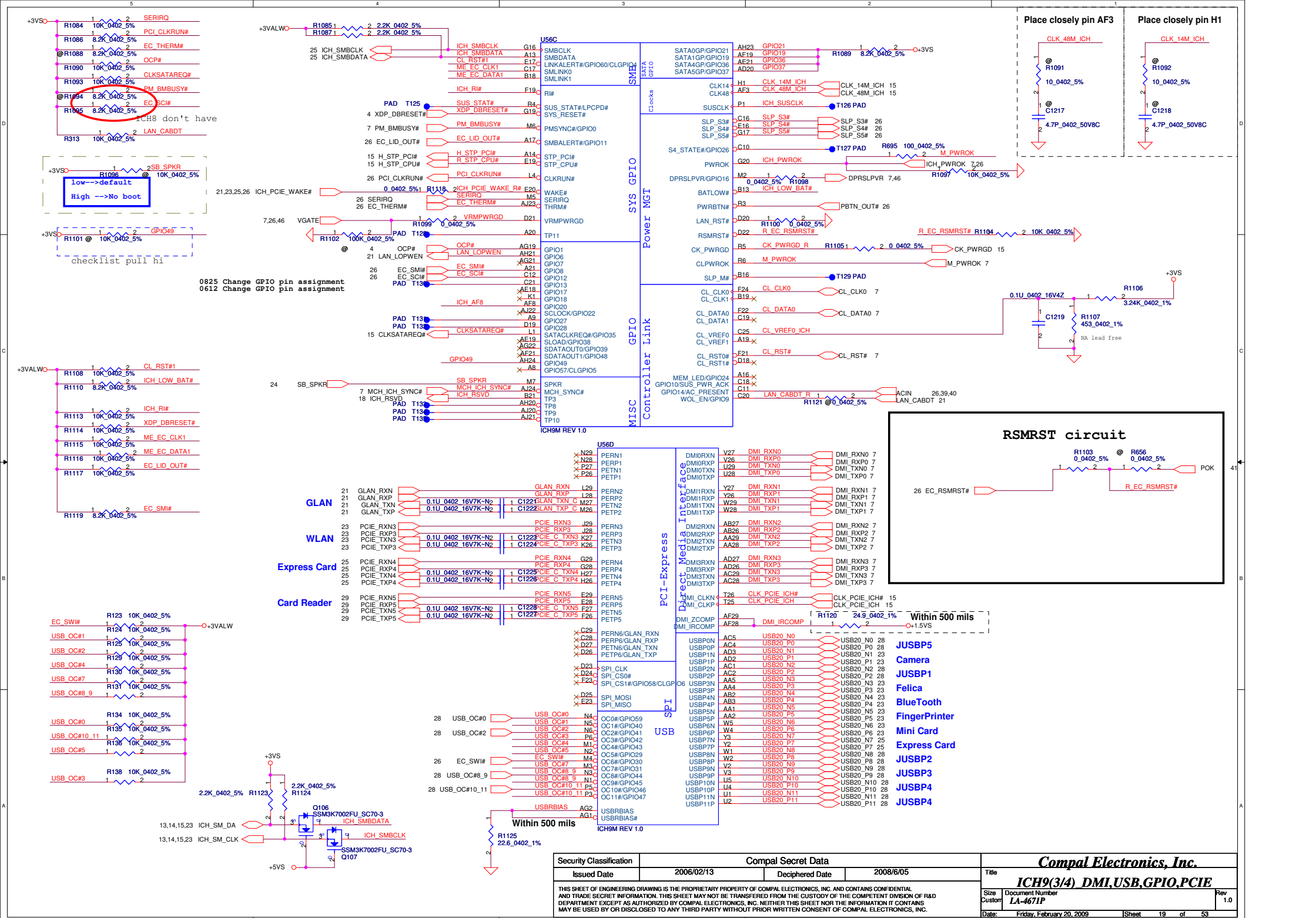


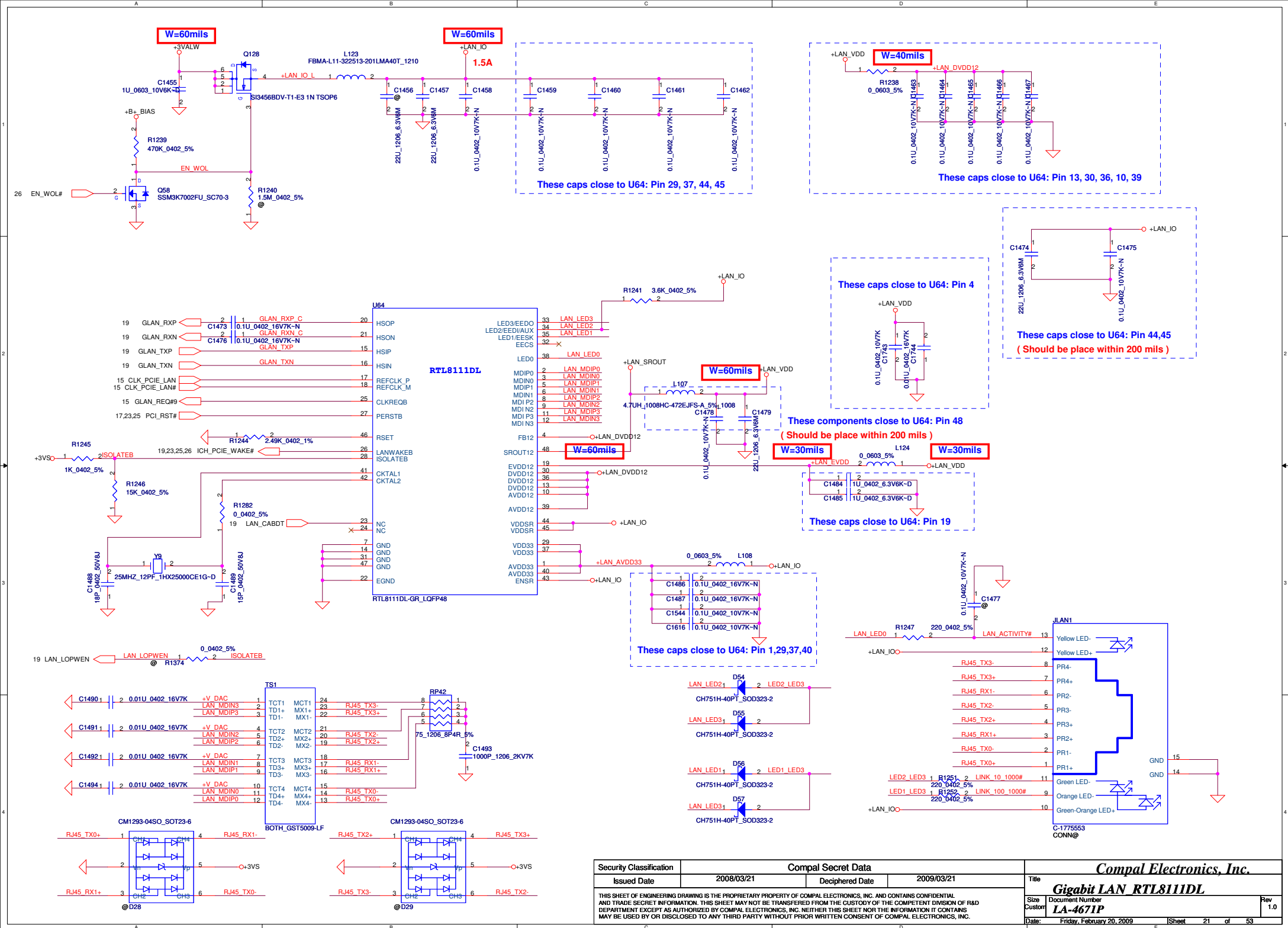
XOR CHAIN ENTRANCE STRAP:RSVD



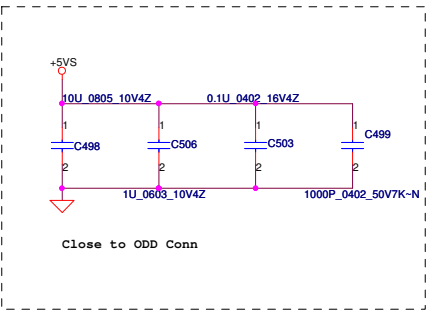
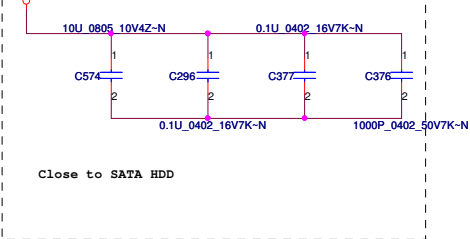
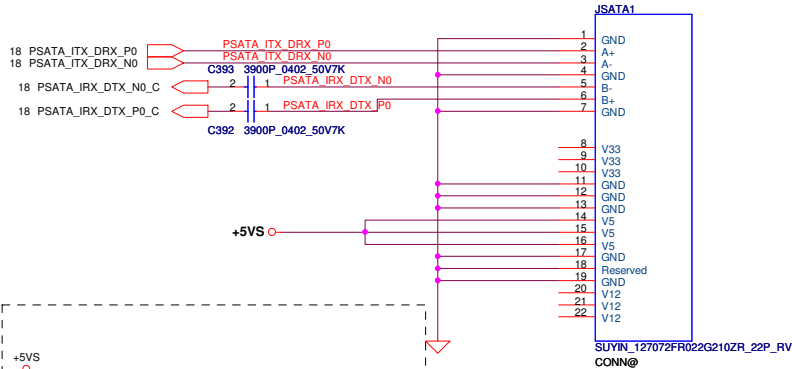
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ICH9(2/4) LAN,HD,IDE,LPC

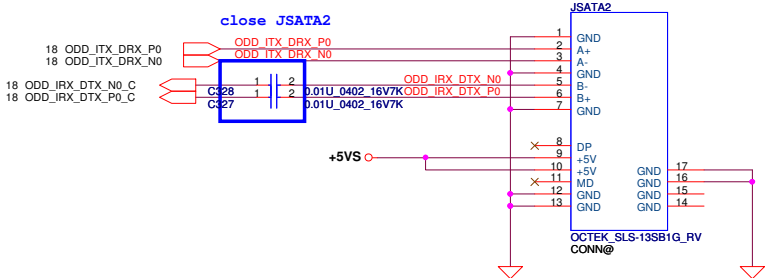




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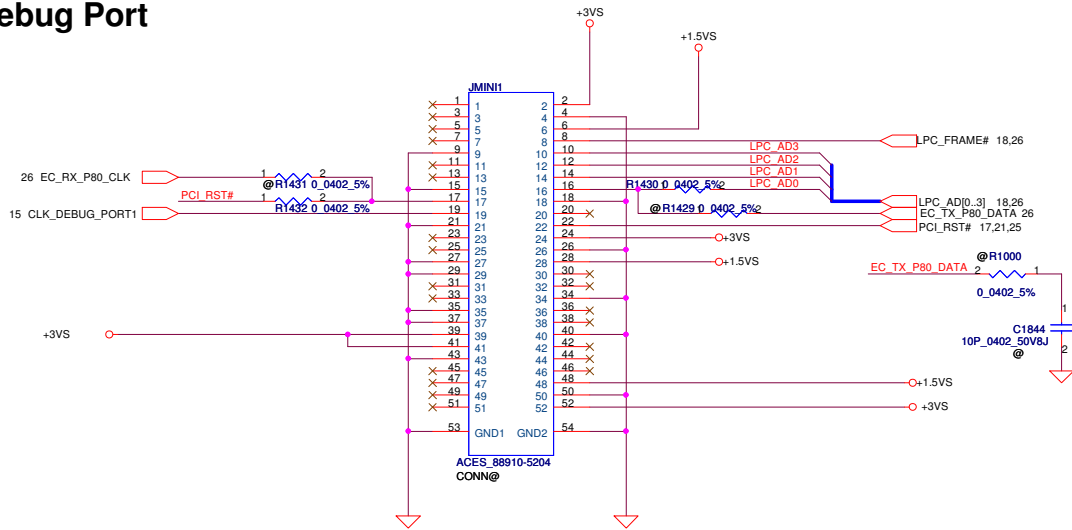


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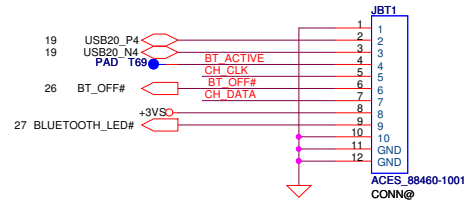


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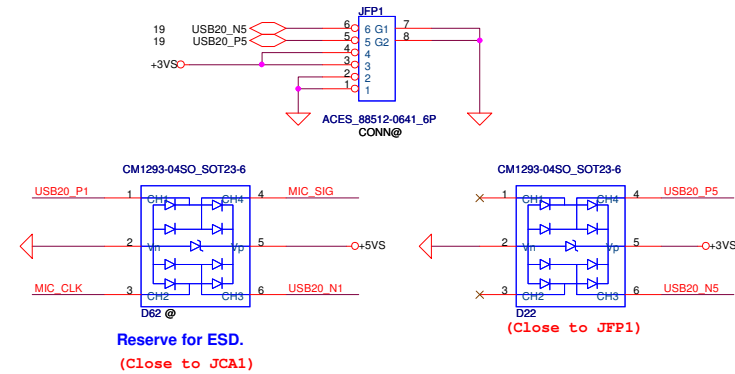
Debug Port



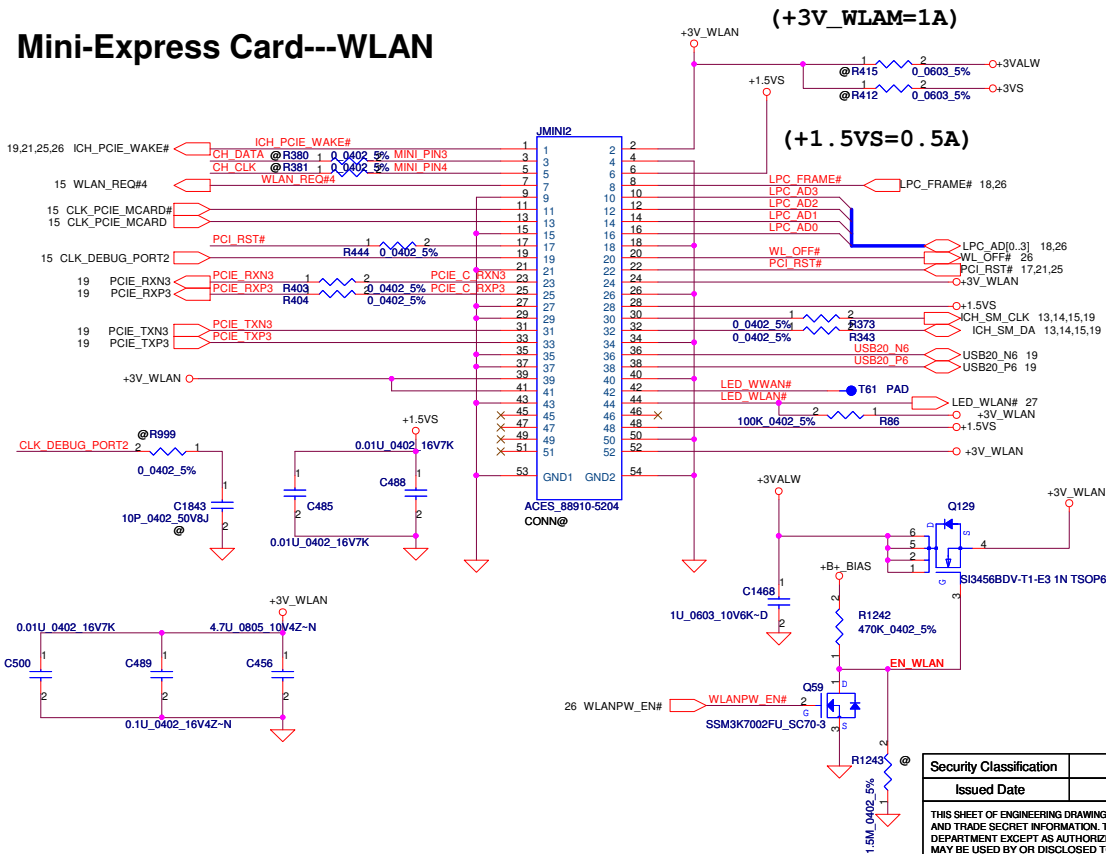
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Fingerprint

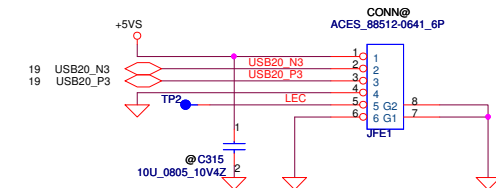


Mini-Express Card---WLAN

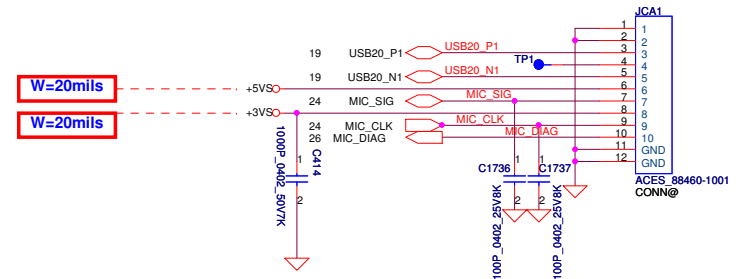


Felica

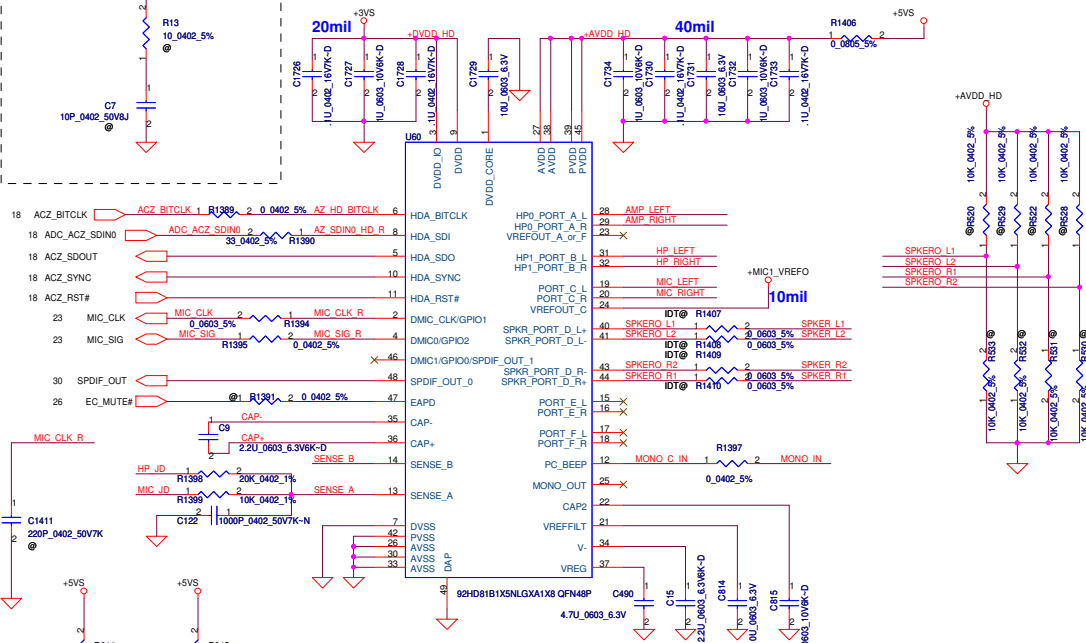
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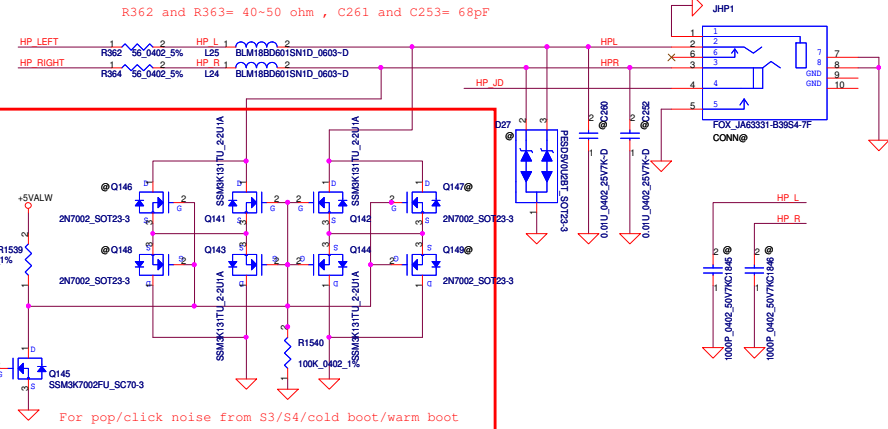
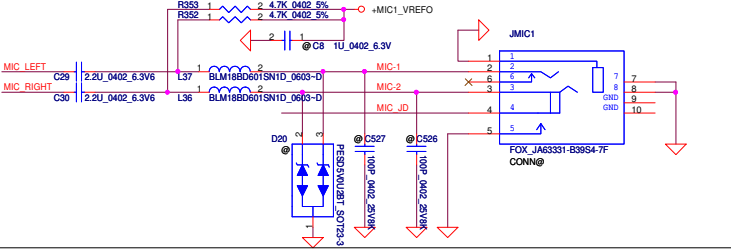
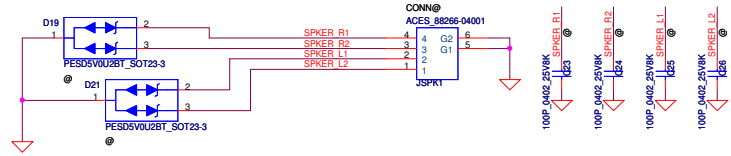
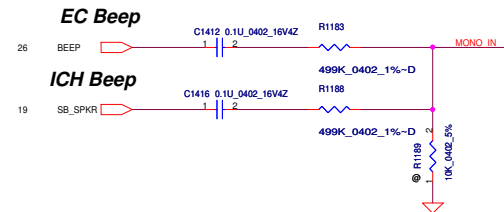
Camera Conn



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Deciphered Date		2008/6/05		Size	
2008/6/05		Document Number		LA-4671P	
Date		Friday, February 20, 2009		Rev	
Sheet		23		1.0	

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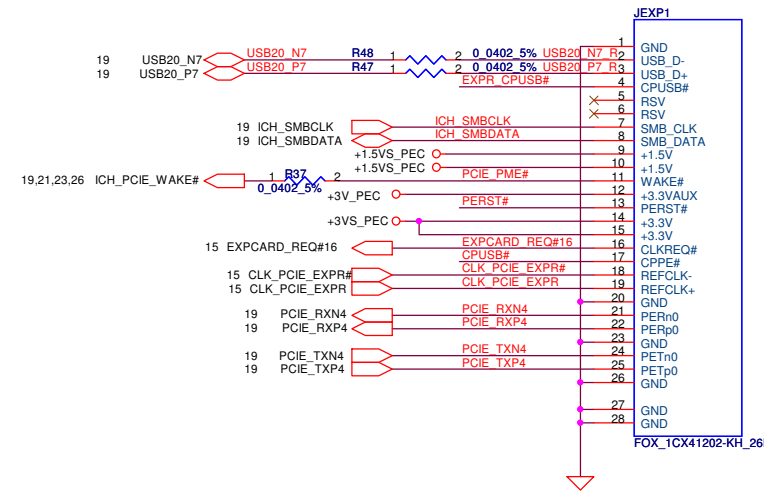
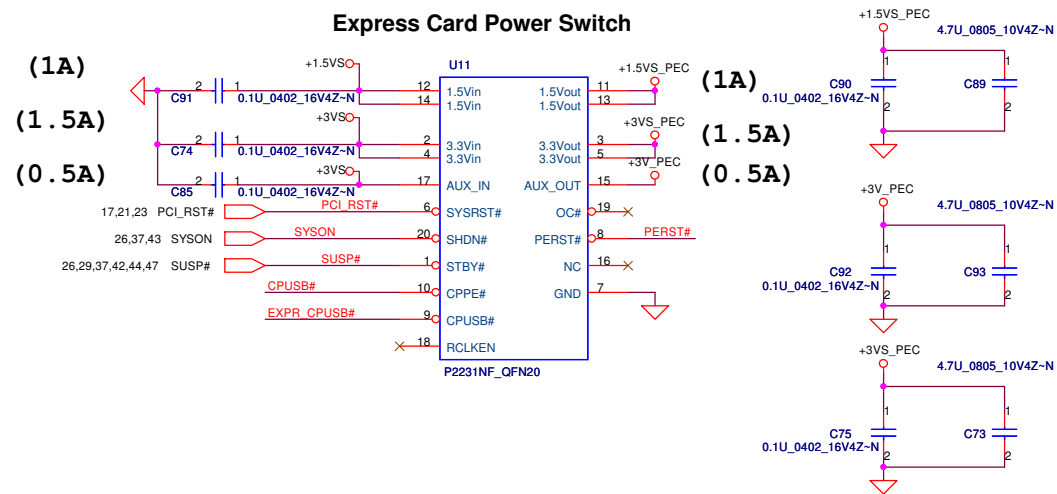
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0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



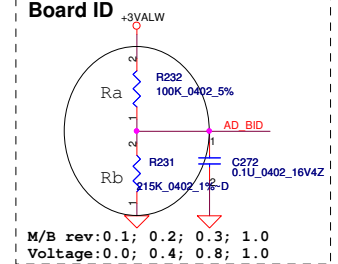
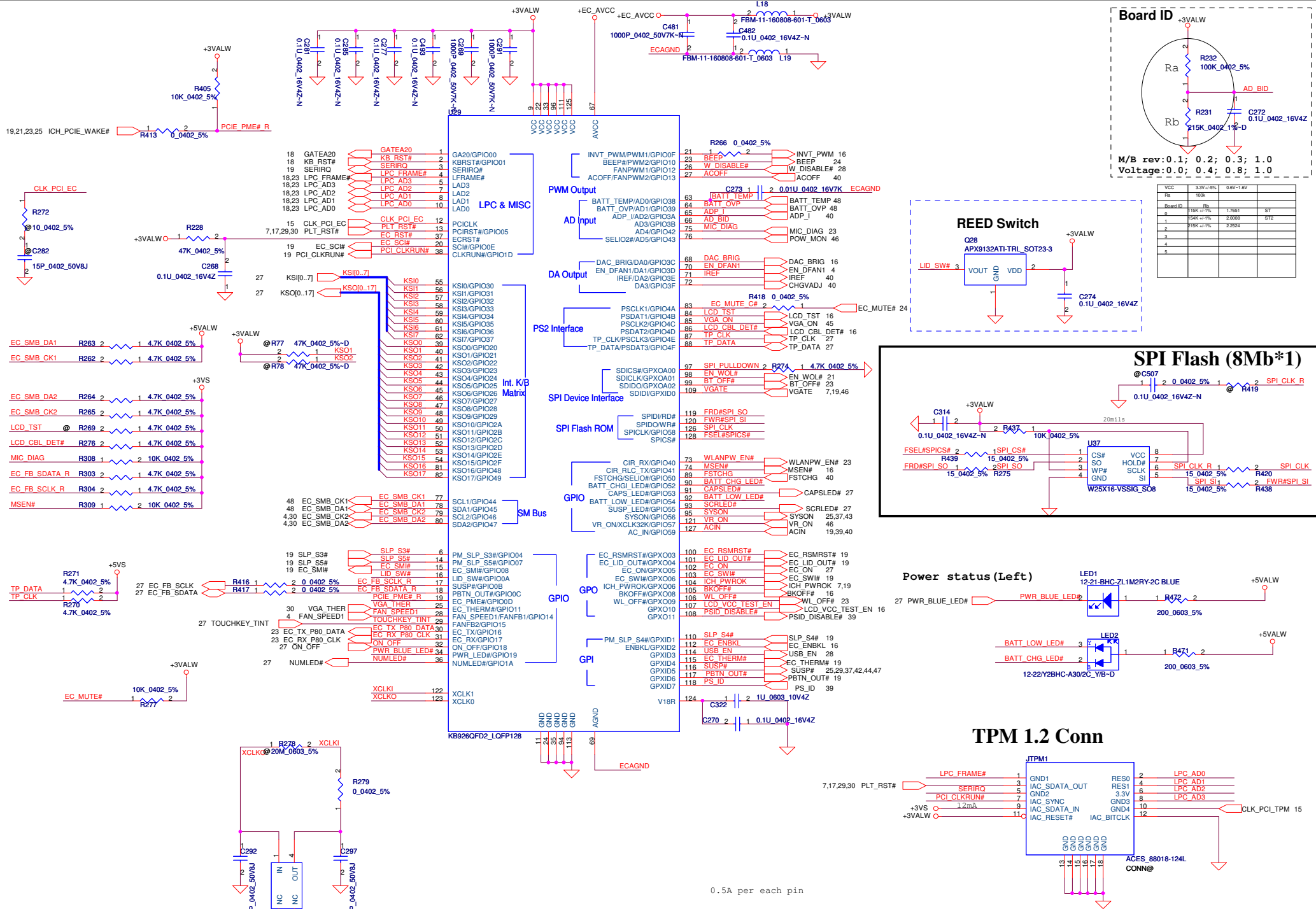
Q141~Q144 Co-Layout with Q146~Q149

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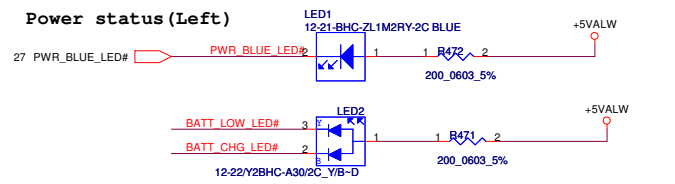
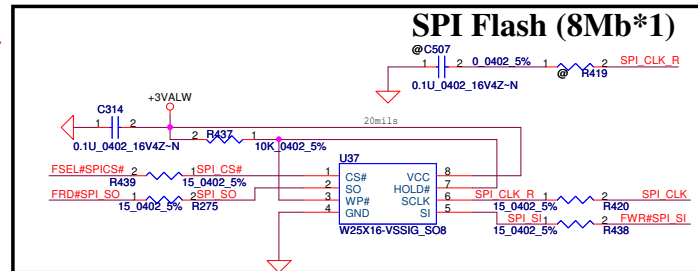
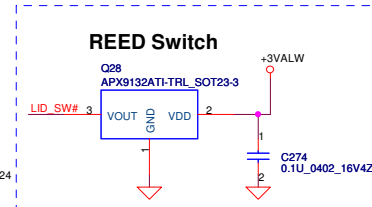
Express card



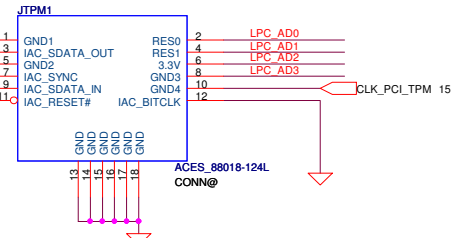
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Issued Date	2007/1/15	Deciphered Date	2008/6/05	Title	
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Size	Custom	Document Number	LA-4671P	Date	Friday, February 20, 2009
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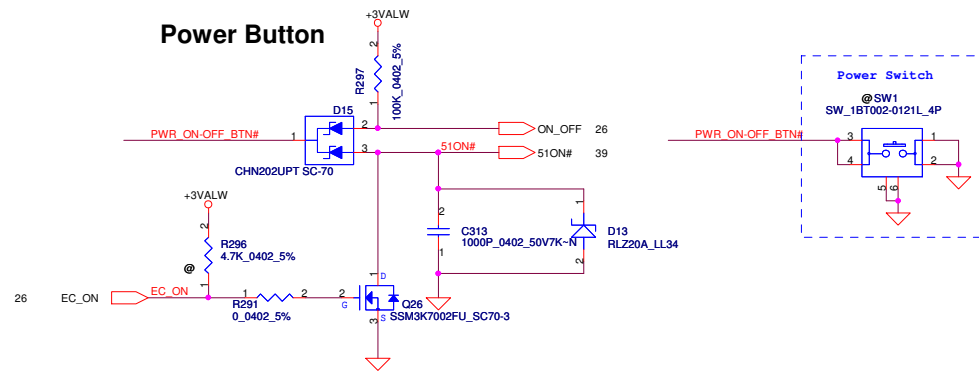
VCC	3.3V±16%	0.6V-1.8V
Ra	100K	
Rb	15K	1.3651
1	15K	2.0008
2	15K	2.2624
3		
4		
5		



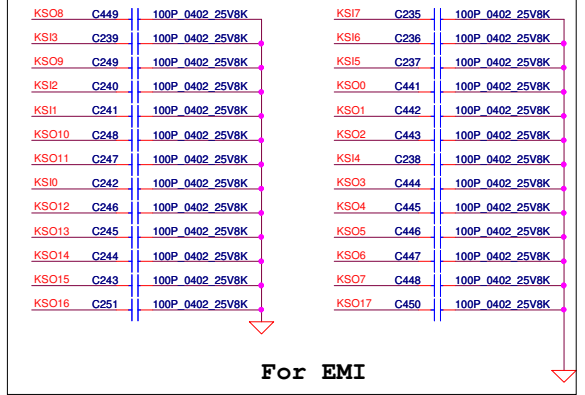
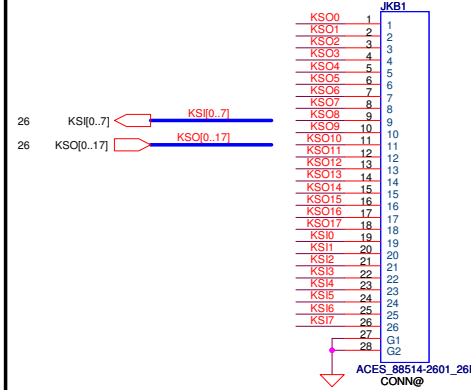
TPM 1.2 Conn



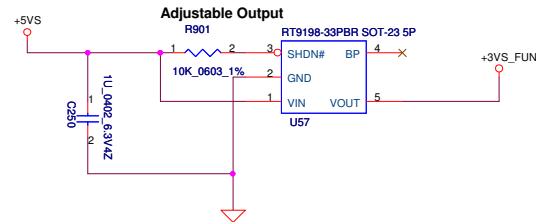
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Issued Date	2007/1/15	Deciphered Date	2008/6/05	Title
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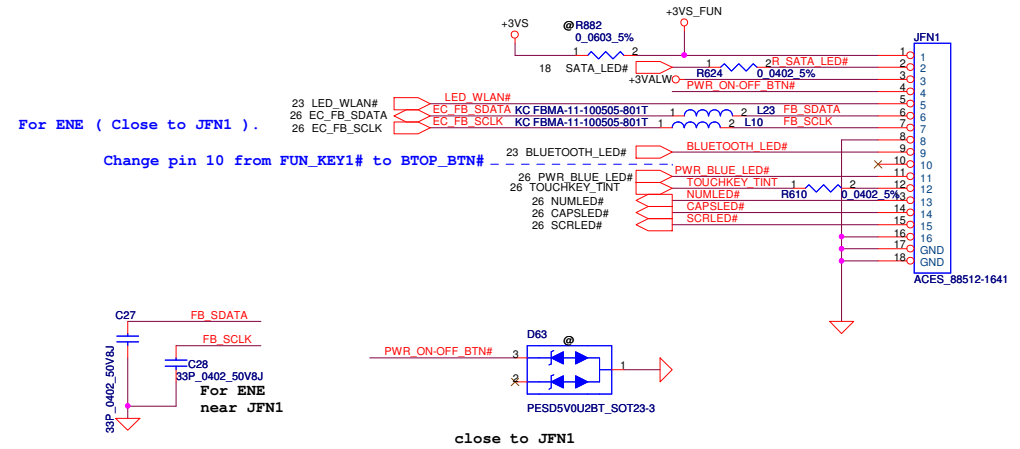
INT_KBD CONN.



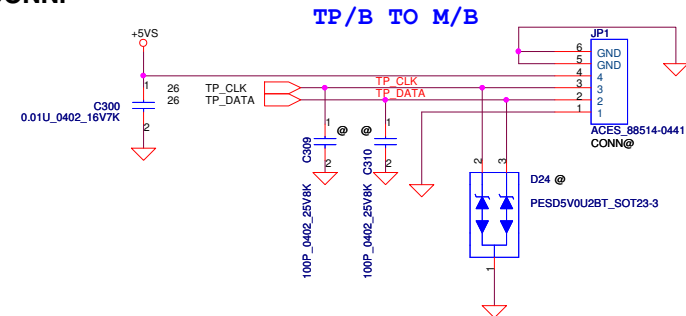
Regulator for ENE sensor



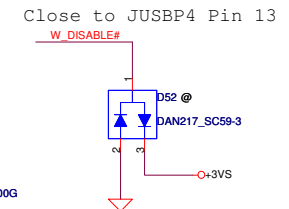
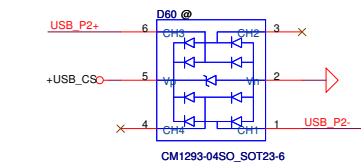
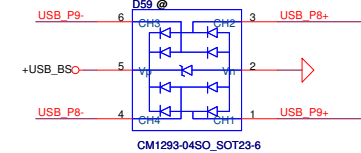
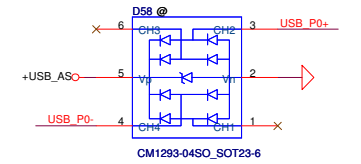
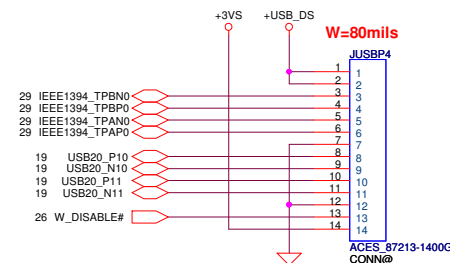
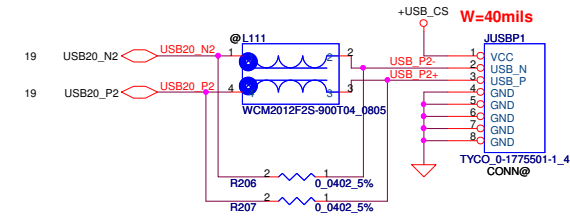
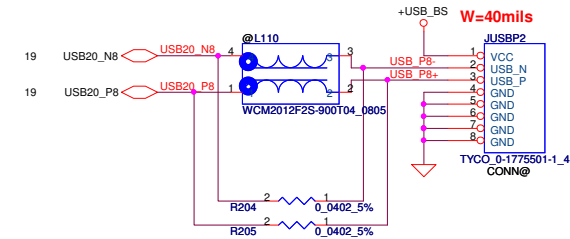
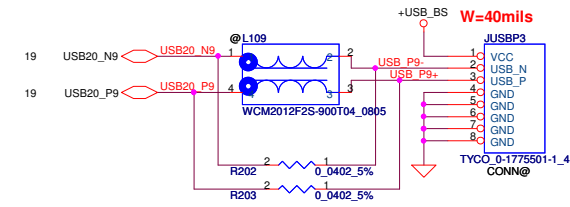
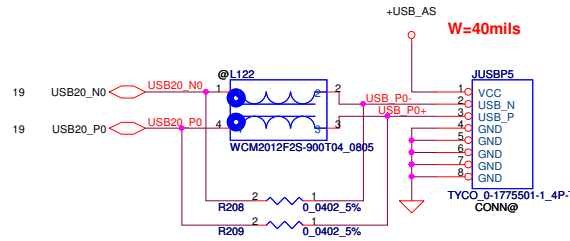
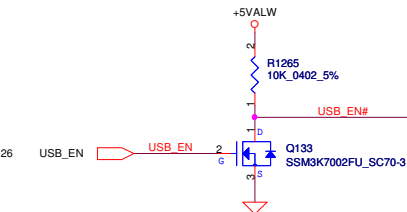
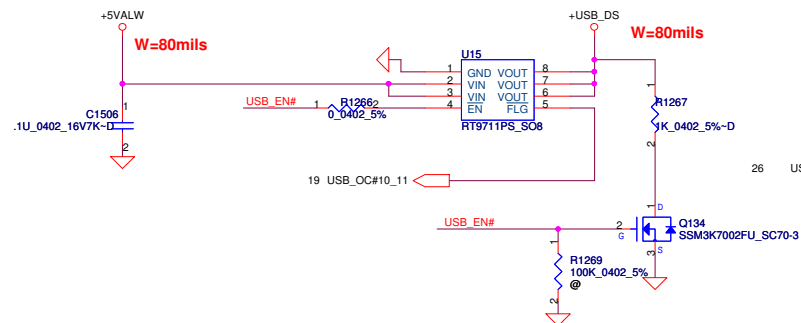
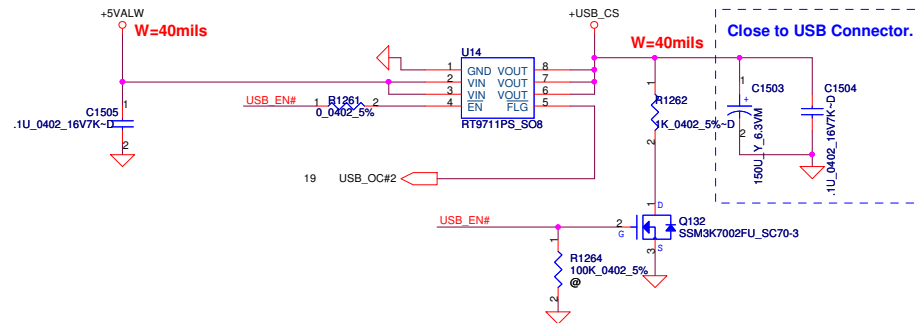
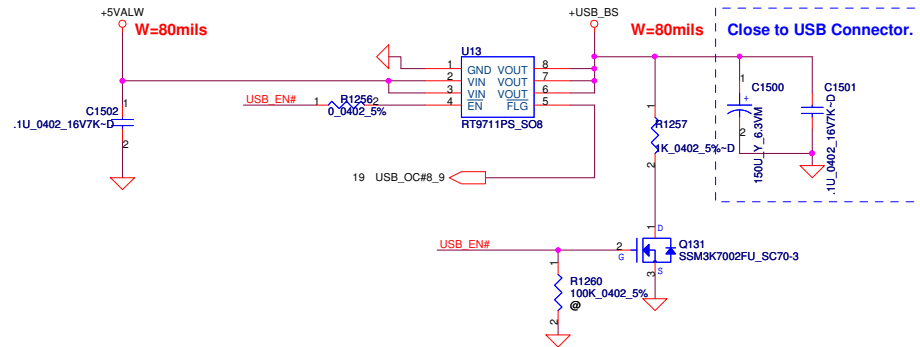
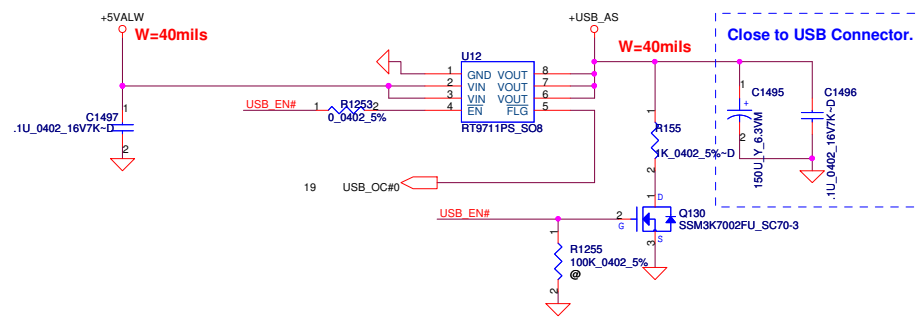
Function/B CONN.



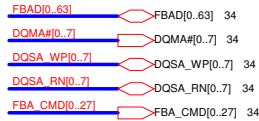
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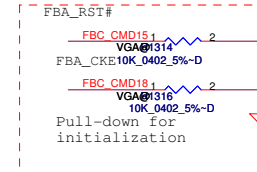
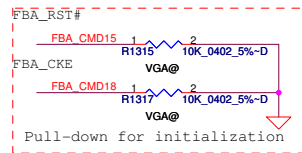
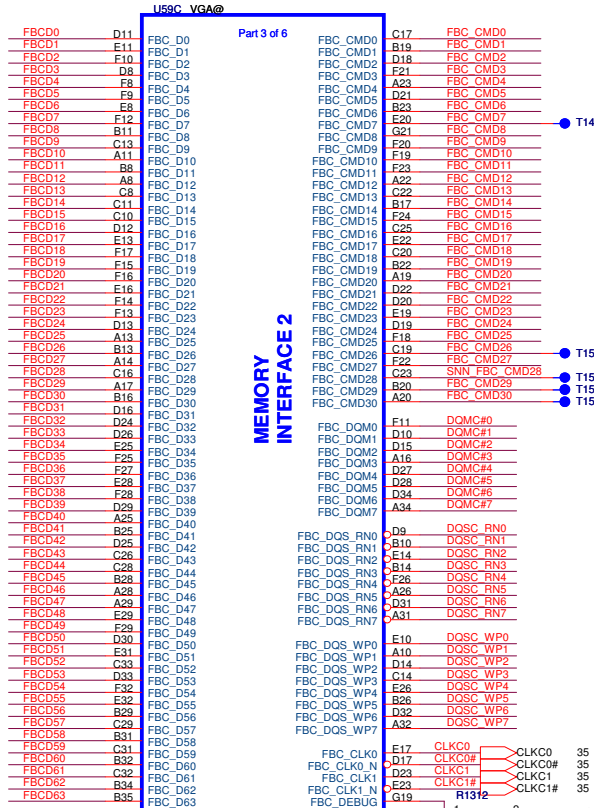
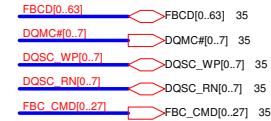
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	0..31	32..63
FBA_CMD0	A4	
FBA_CMD1	RAS#	RAS#
FBA_CMD2	A5	
FBA_CMD3	BA1	BA1
FBA_CMD4		A2
FBA_CMD5		A4
FBA_CMD6		A3
FBA_CMD7	CS1#	CS1#
FBA_CMD8	CS0#	CS0#
FBA_CMD9	A11	A11
FBA_CMD10	CAS#	CAS#
FBA_CMD11	WE#	WE#
FBA_CMD12	BA0	BA0
FBA_CMD13		A5
FBA_CMD14	A12	A12
FBA_CMD15	RST/ODT	RST/ODT
FBA_CMD16	A7	A7
FBA_CMD17	A10	A10
FBA_CMD18	CKE	CKE
FBA_CMD19	A0	A0
FBA_CMD20	A9	A9
FBA_CMD21	A6	A6
FBA_CMD22	A2	A2
FBA_CMD23	A8	A8
FBA_CMD24	A3	A3
FBA_CMD25	A1	A1
FBA_CMD26	A13	A13
FBA_CMD27	BA2	BA2
FBA_CMD28	RFU0	RFU0
FBA_CMD29	RFU1	RFU1
FBA_CMD30	RFU2	RFU2

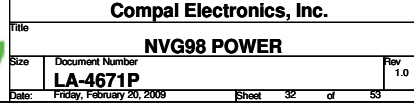


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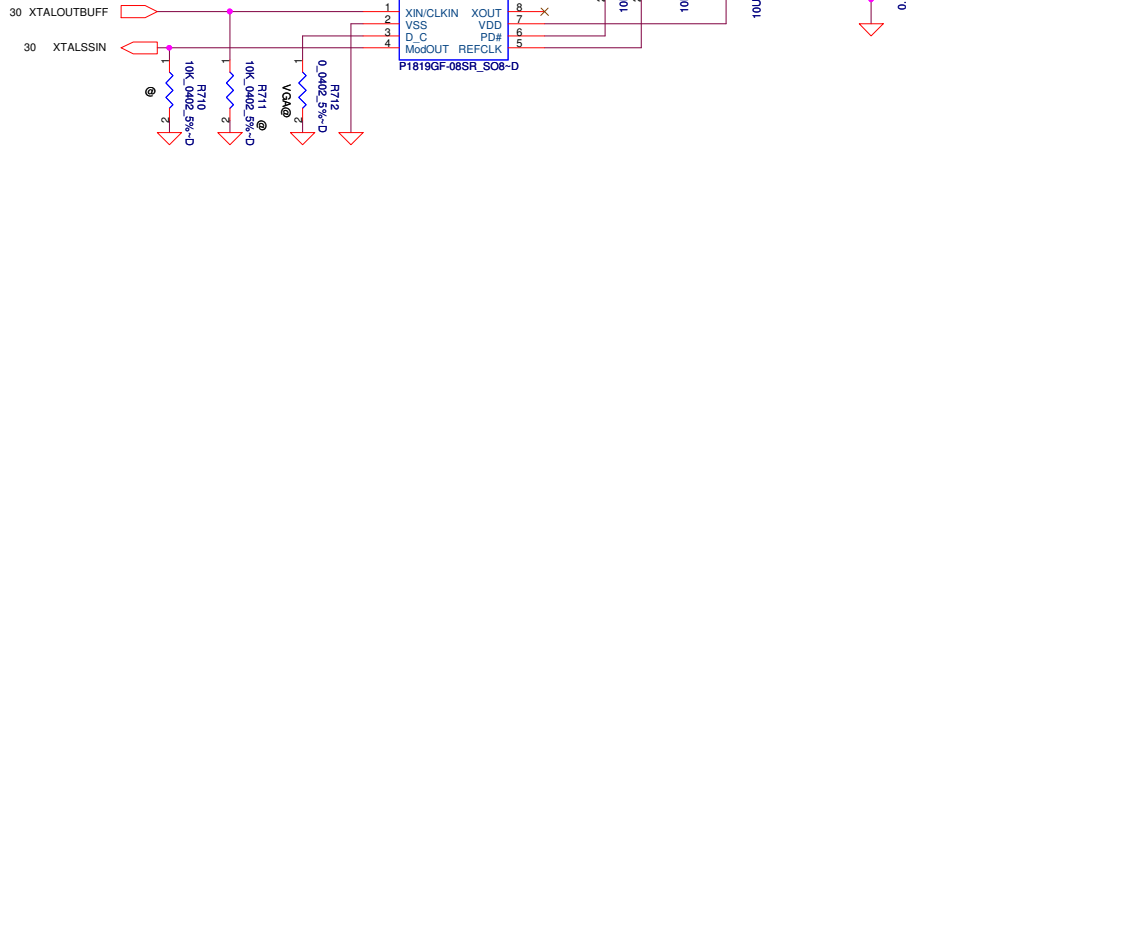
Compal Electronics, Inc.			
Title NVG98 Memory Interface			
Size	Document Number	Rev	
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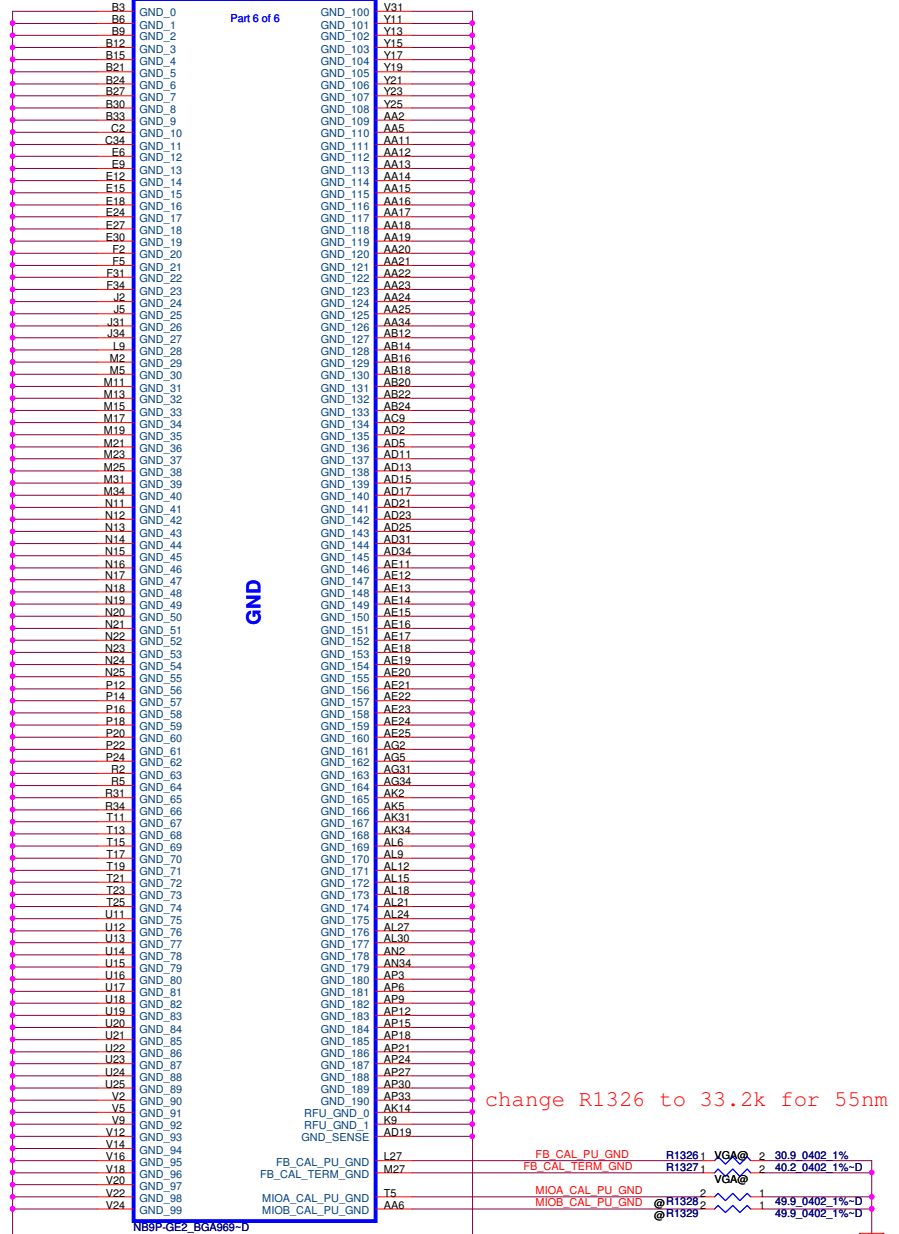


	D_C
-1.75% (DOWN)	0
±0.875% (CENTER)	1

D_C Internal pull up



VGA@ U59F



change R1326 to 33.2k for 55nm

R860/R861 ; depop for G84

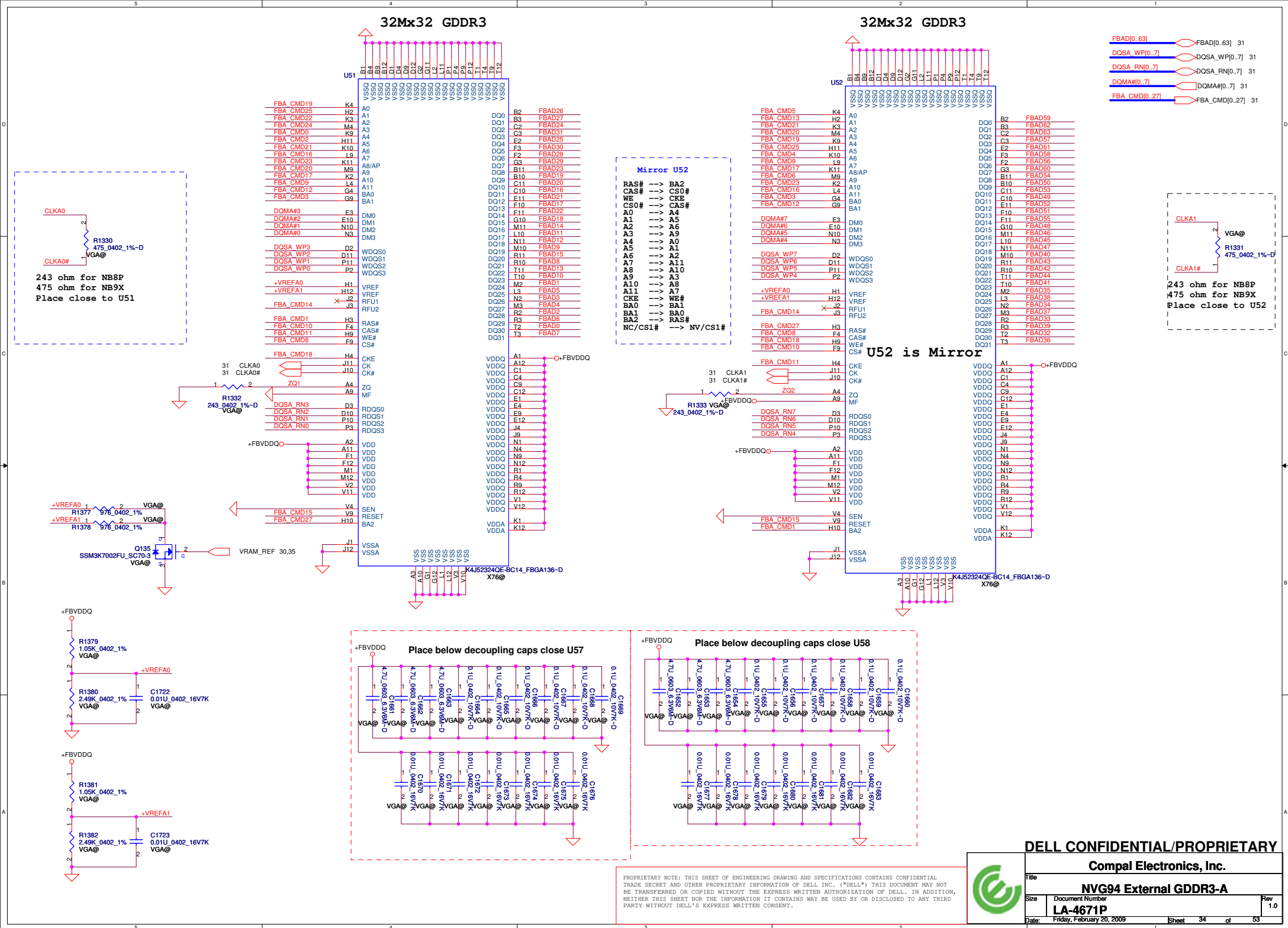
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

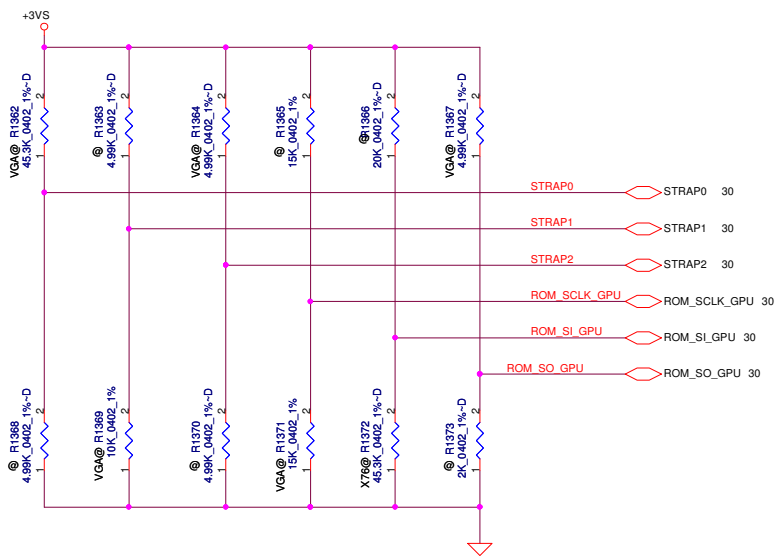


Title				NVG98 GND	
Size	Document Number	LA-4671P		Rev	1.0
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ZZZ
VRAM



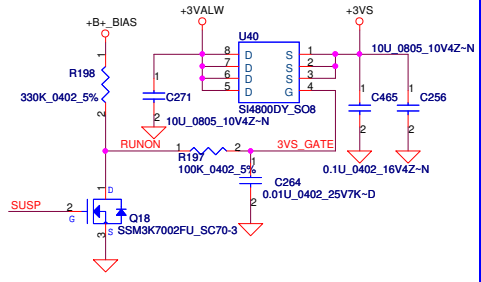
STRAP0	Pull up 45K
STRAP1	Pull down 10K
STRAP2	Pull up 5K
ROM_SCLK_GPU	Pull down 15K
ROM_SI_GPU	
ROM_SO_GPU	Pull up 5K

All GDDR3

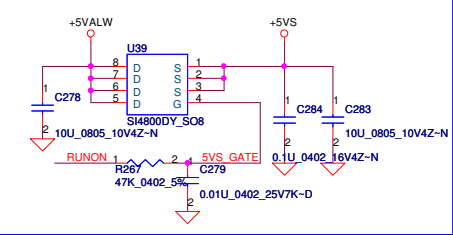
ROM_SI_GPU	Pull down
Q:16x32	10K_1%
H:16x32	15K_1%
S:16x32	20K_1%
Q:32x32	30K_1%
H:32x32	35K_1%
S:32x32	45.3K_1%

	R1364	R1365	
17"	24.9K	15K	NB9P-???

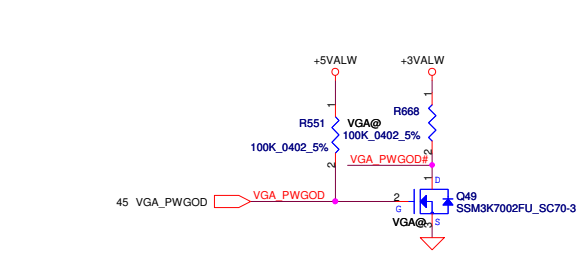
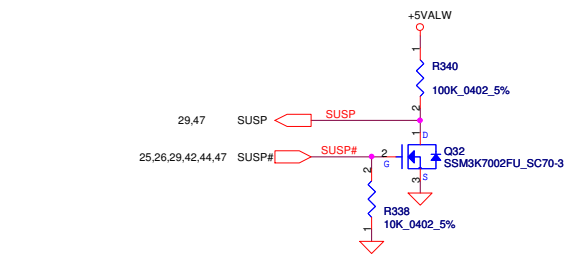
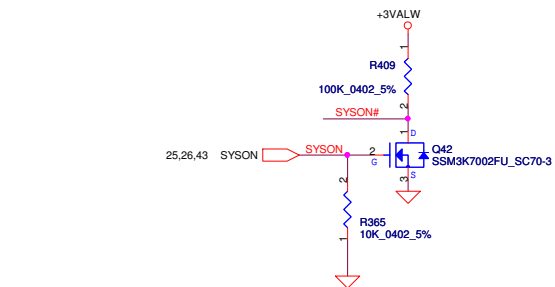
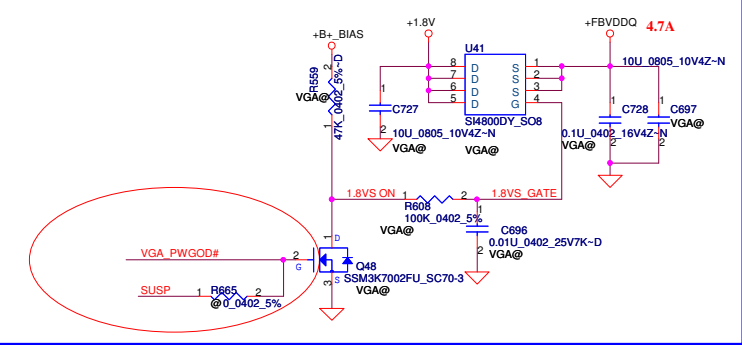
+3VALW to +3VS Transfer



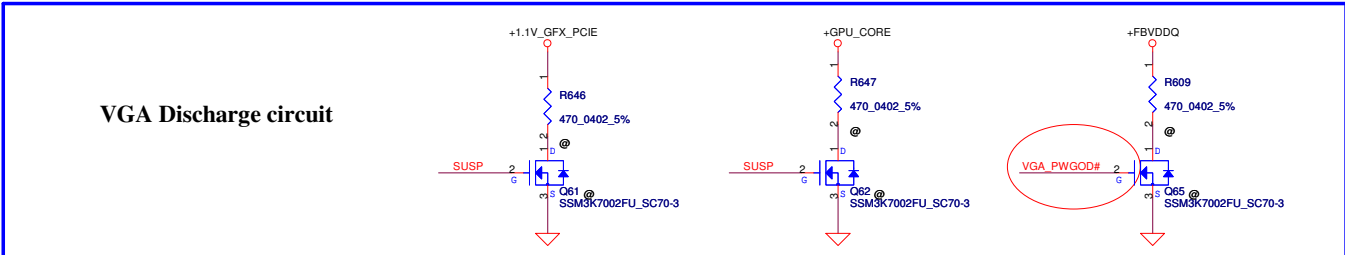
+5VALW to +5VS Transfer



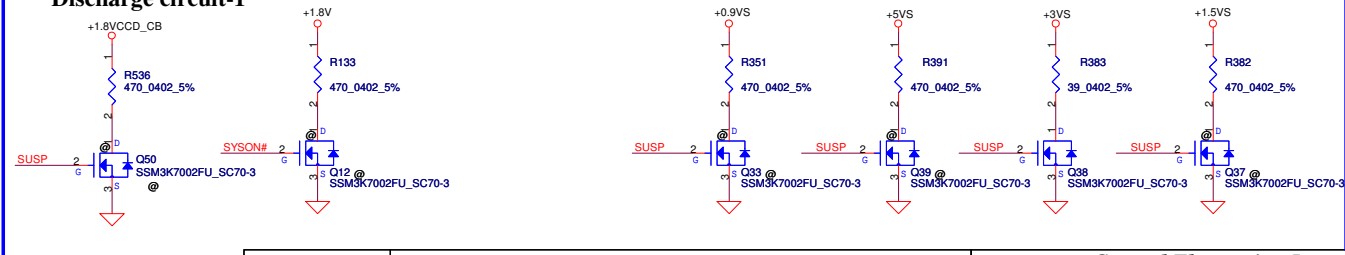
+1.8V to +1.8VS Transfer



VGA Discharge circuit



Discharge circuit-1



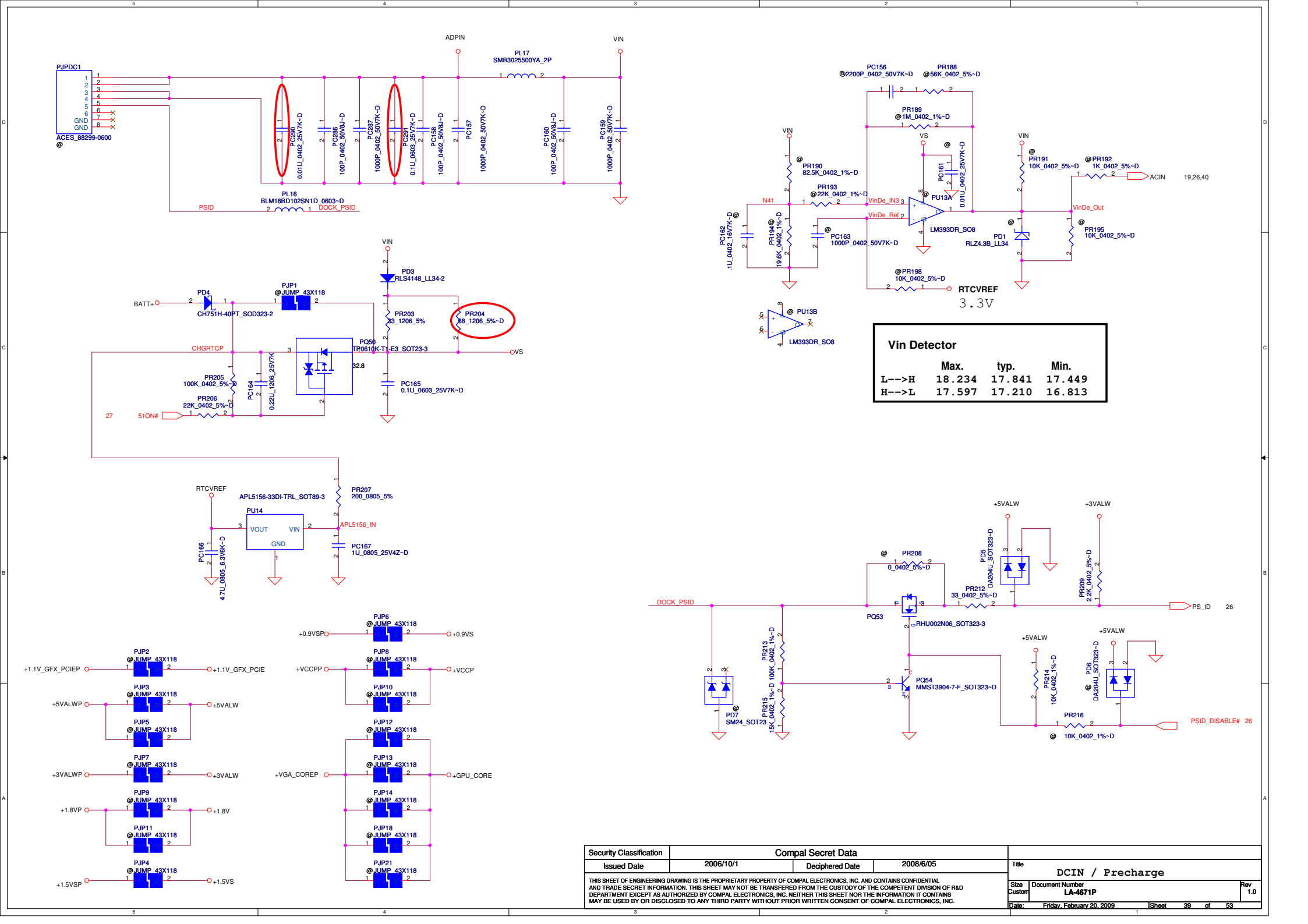
SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

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				2008/6/05				Title			
								DC/DC Circuits			
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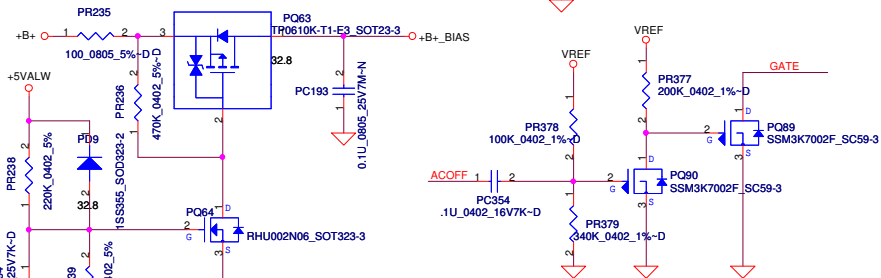
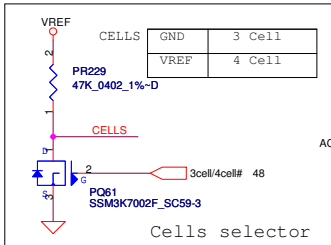


Change Location H5 (3P2), H17 (3P7)
Add H27 (3P2)
(2008-10-31 update)

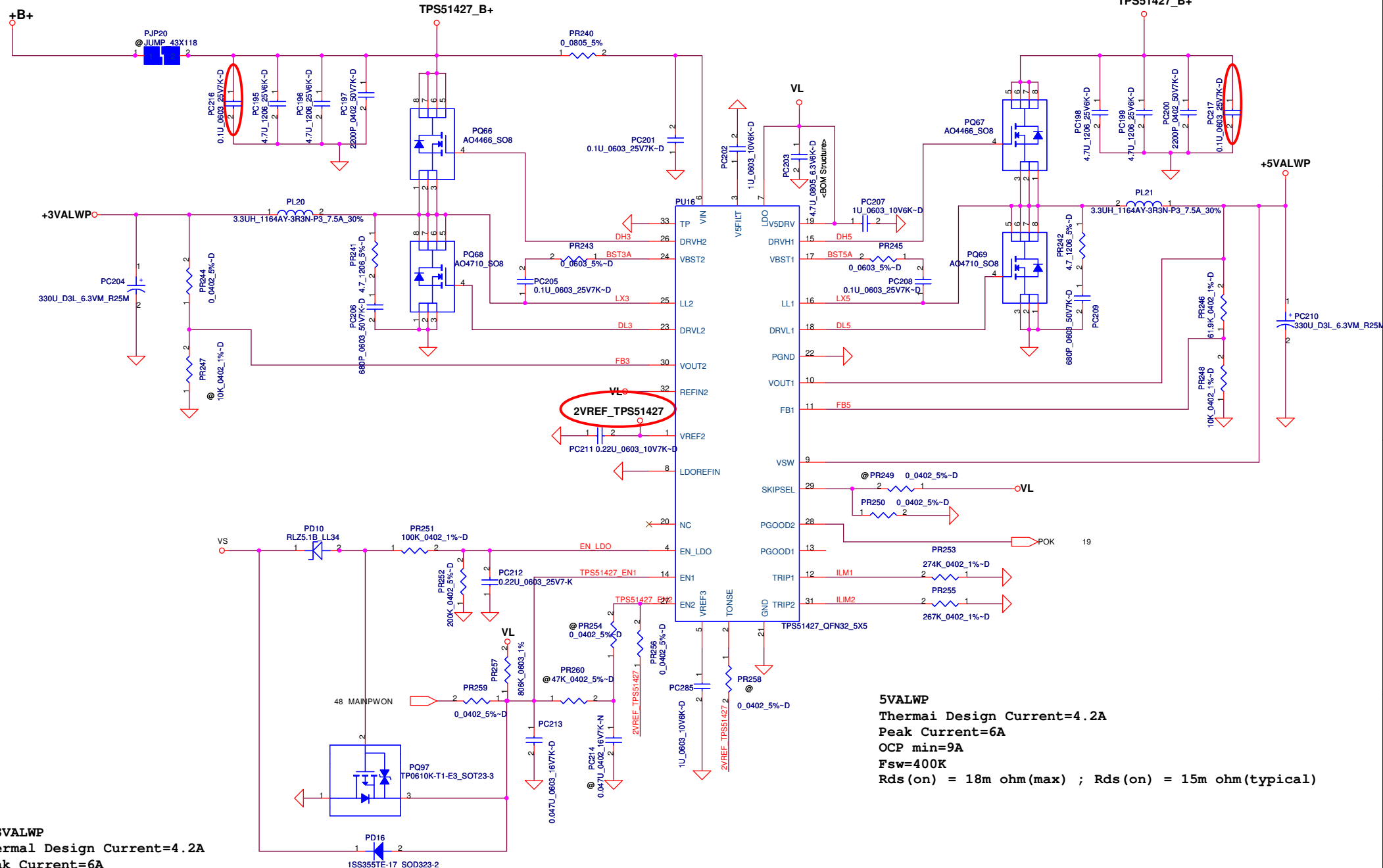
Add H34 (3P2)
(2008-11-11 update)



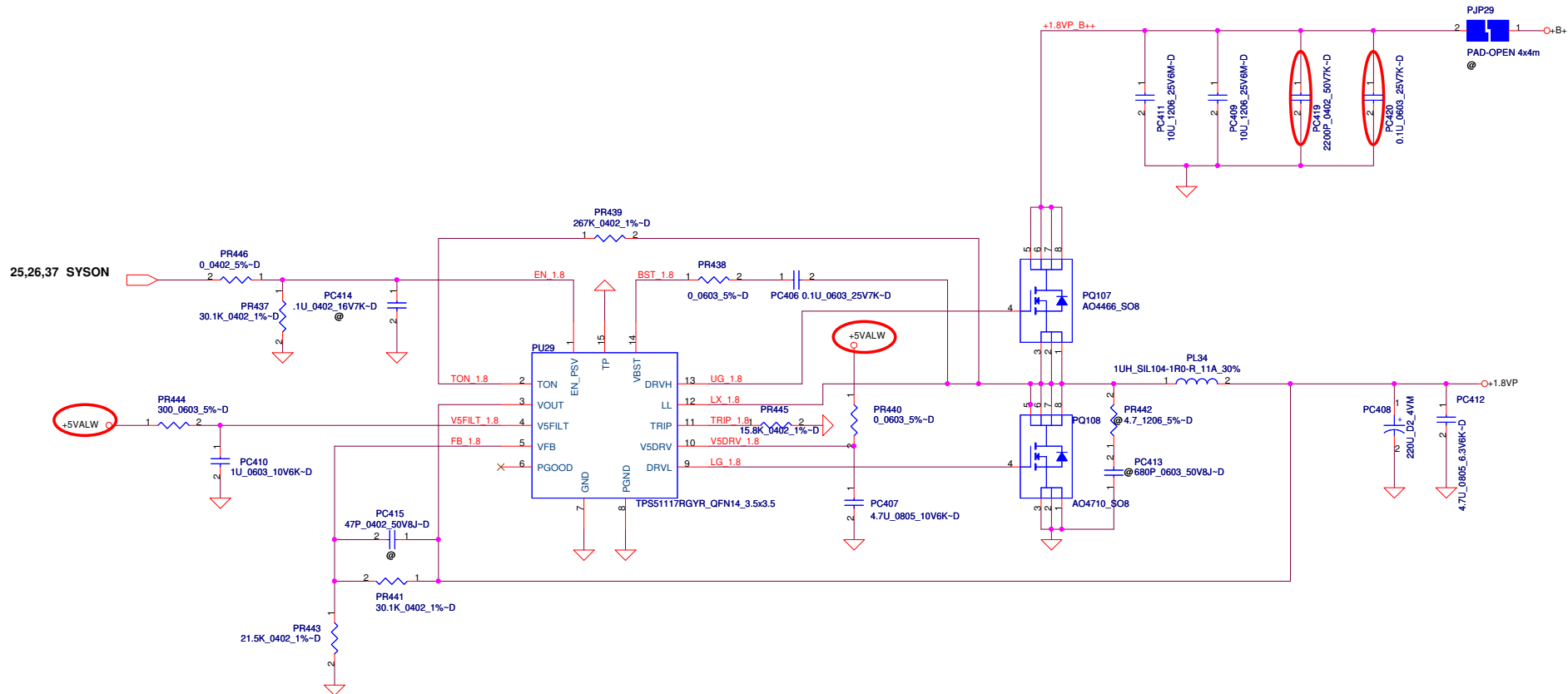
90W adapter
 $I_{charge} = (V_{srset}/V_{vdac}) * (0.1/PR222) = 3.3A$
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR217) = 4.4A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz



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				Size B	Document Number KML60	Rev 1.0
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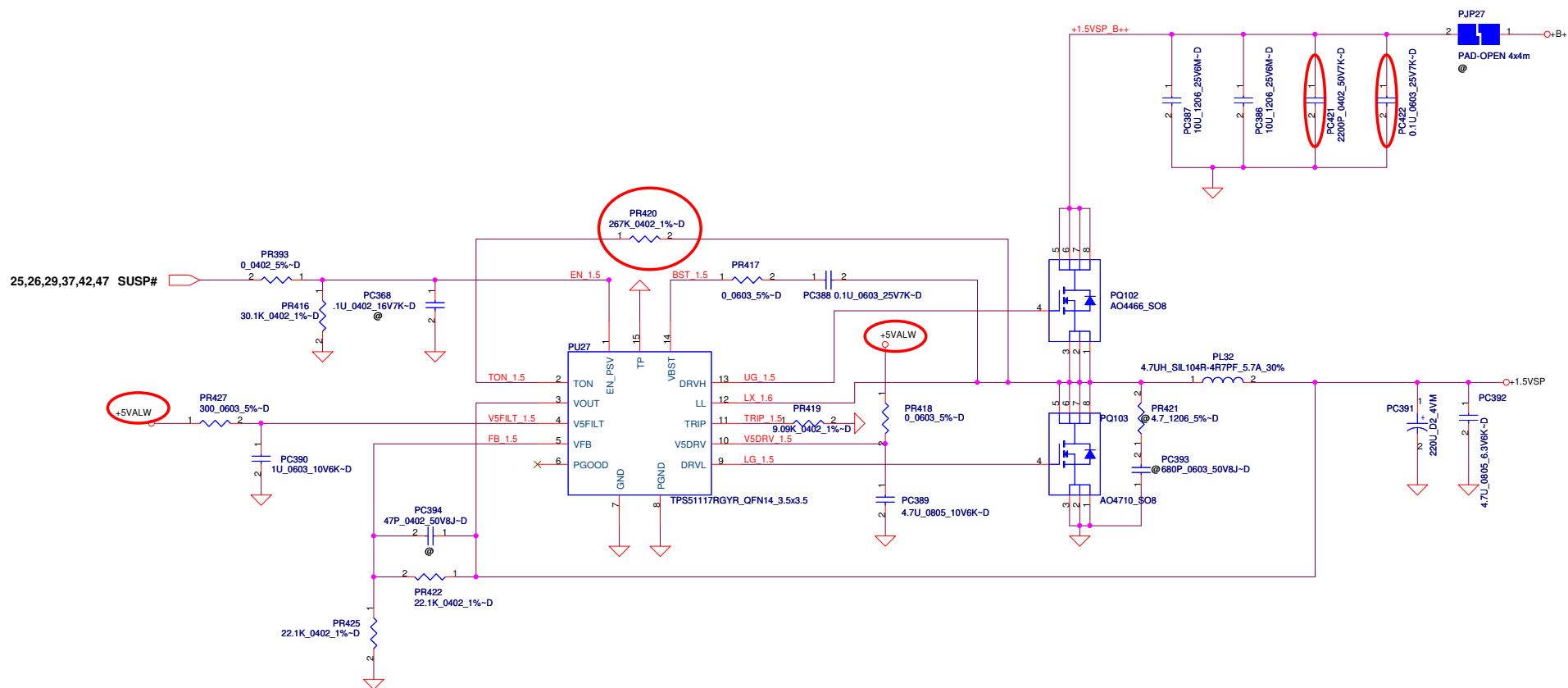
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Issued Date	2006/10/1	Deciphered Date	2008/6/05	Title	
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1.8V
Thermal Design Current=6.3A
Peak Currnet=9A
OCF min=12A
Fsw=297KHz

<Vo=1.8V> VFB=0.75V
Vo=VFB*(1+PR441/PR443)=0.75*(1+30.1K/21.5K)=1.8V
Fsw=297KHz

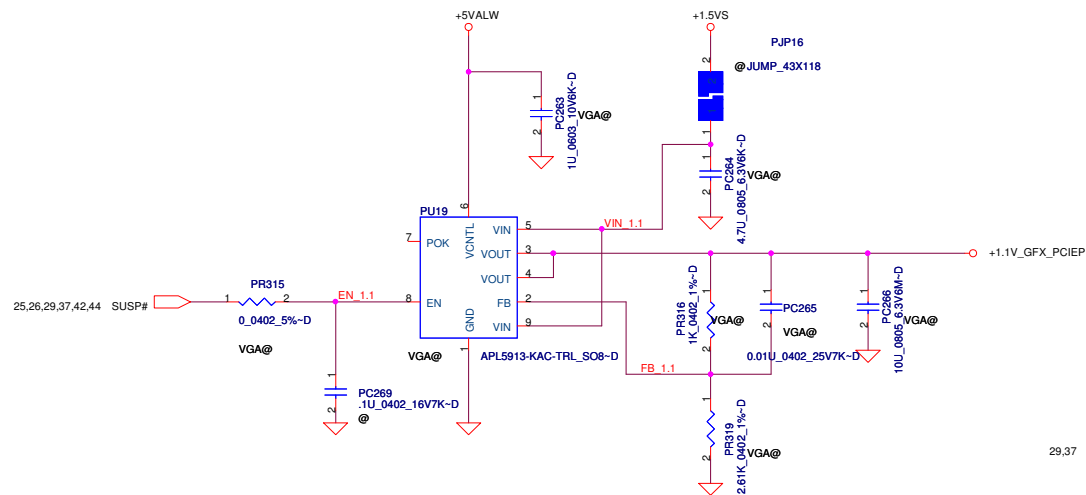
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/2/5	Deciphered Date	2008/6/05	Title	+1.8VP
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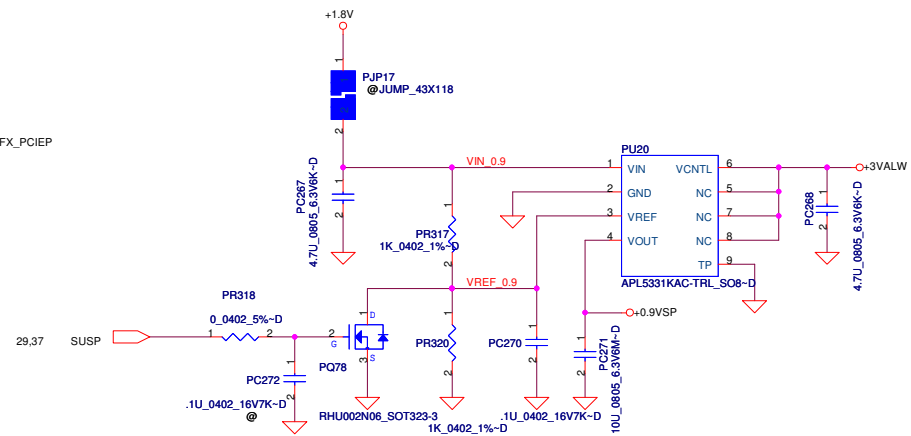
1.5V
 Thermal Design Current=2.45A
 Peak Current=3.5A
 OCP min=5.25A
 Fsw=298KHz

 $V_o = 1.5V$ $V_{FB} = 0.75V$
 $V_o = V_{FB} * (1 + PR422 / PR425) = 0.75 * (1 + 22.1K / 22.1K) = 1.5V$

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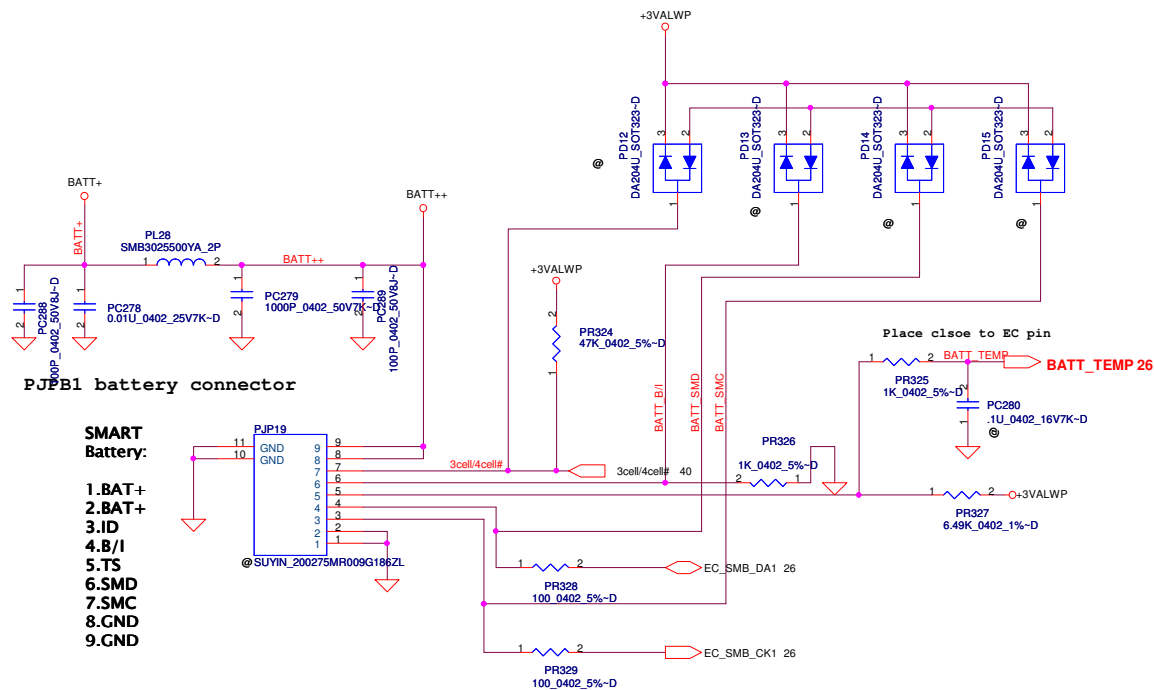


1.1V GFX_PCIEP
Thermal Design Current=1.61A
Peak Currnet=2.3A
OCP min=2.76A

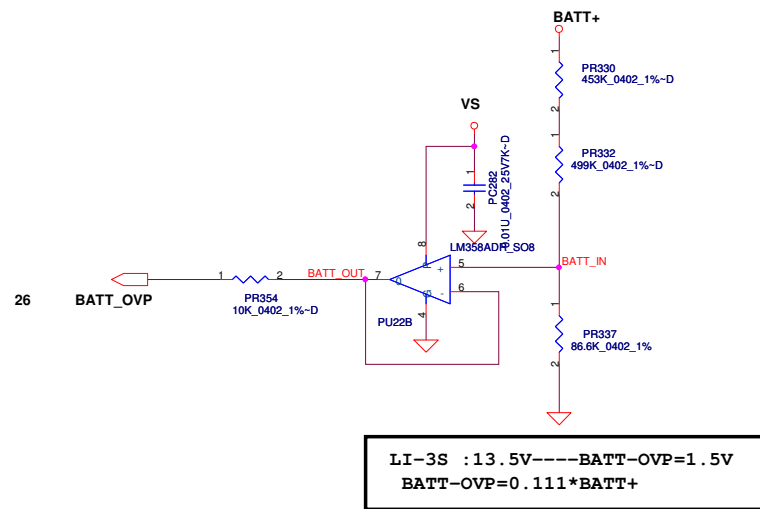


0.9VSP
Thermal Design Current=0.7A
Peak Currnet=1A
OCP min=1.2A

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Deciphered Date				2008/6/05				+0.9VSP/ +1.1V GFX_PCIEP			
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Battery Connect/OTP



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Deciphered Date				2008/6/05				BATTERY CONN			
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Date: Friday, February 20, 2009				Document Number				1.0			
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Version Change List (P. I. R. List)

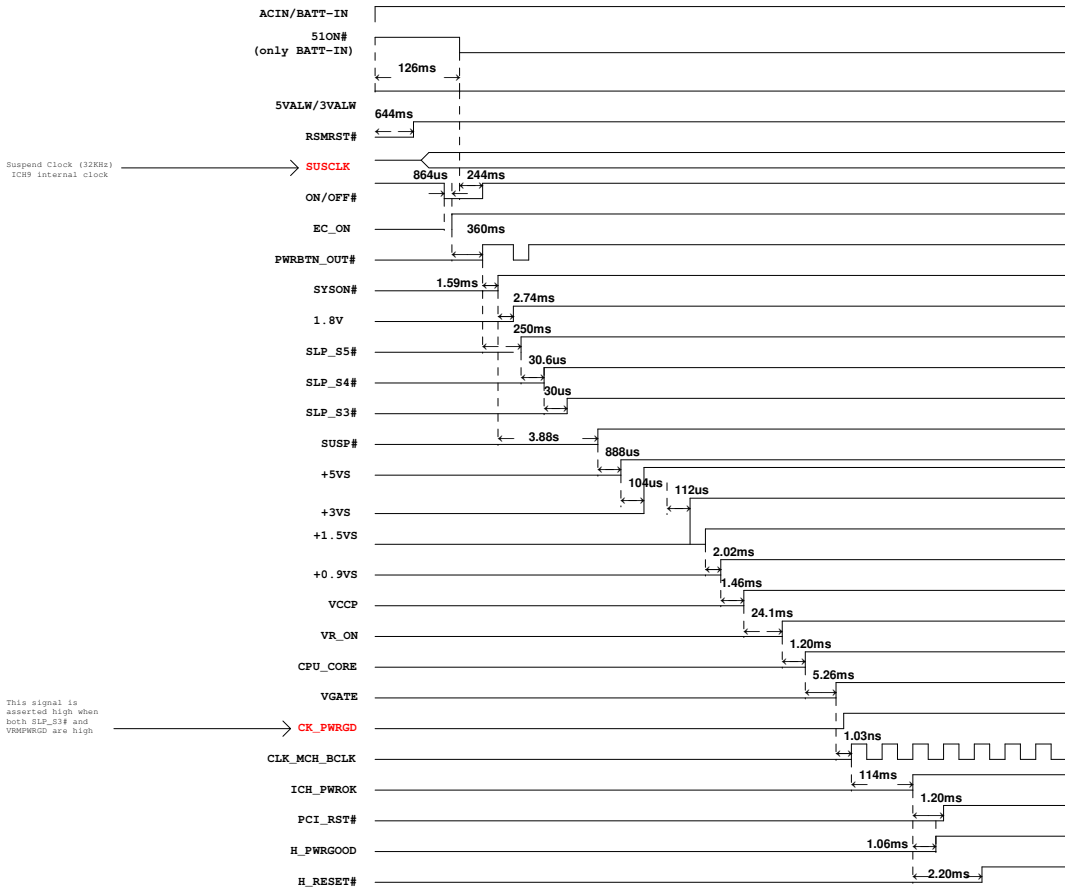
Page 1

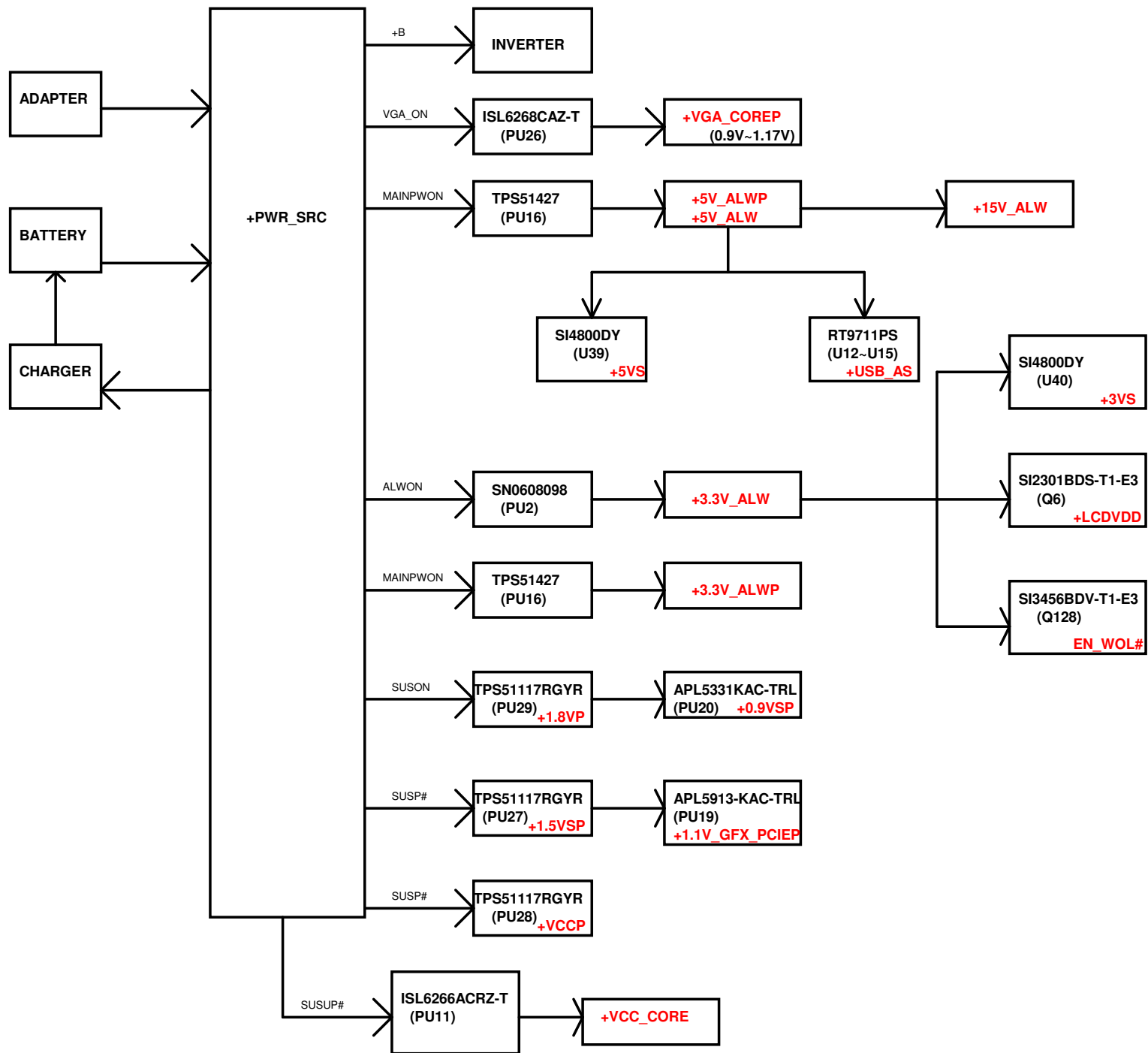
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	40	DCIN/Precharge	08/12/17	COMPAL	Common circuit design modify	add PC290,PC291 between ADPIN and GND	
2			08/12/17	COMPAL	Common circuit design modify	add PR204 between VS and PD3.1	
3	41	Charger	08/12/17	COMPAL	Common circuit design modify	add PR262 between +3VALW and PU15.11	
4			08/12/17	COMPAL	Common circuit design modify	reserve PR261 between PU15.10 and PU15.11	
5			08/12/17	COMPAL	Common circuit design modify	change PR224.1 POWER source from VREF into +3VALW	
6	42	+3VALWP,+5VALWP	08/12/17	COMPAL	Common circuit design modify	add PC216,PC217 between TP551427+B+ and GND	
7			08/12/17	COMPAL	Wrong net name issue	change PU16.1 net name from 2VREF_1SL6237 to 2VREF_TP551427	
8	44	+1.8VP	08/12/17	COMPAL	+1.8V no power issue in S3 mode	change PR440.1,PR444.1 POWER source from +5VS to +5VALW	
9			08/12/17	COMPAL	Common circuit design modify	add PC419,PC420 between +1.8VP_B++ and GND	
10	46	+VGA_COREP	08/12/17	COMPAL	Common circuit design modify	add PC423,PC424 between VGA_B++ and GND	
11			08/12/17	COMPAL	Change VID require	change PR410 to 5.62K ohm	
12			08/12/17	COMPAL	Change VID require	reserve PQ100,PR406,PC382,PR408,PC384,PR413,PR411,PR409	
13			08/12/17	COMPAL	Common circuit design modify	change PR409.2,PR412.2 POWER source from +5VS to +3VS	
14			08/12/17	COMPAL	Common circuit design modify	change 396.1 POWER source from +5VS to +5ALW	
15	43	+VCCP	08/12/17	COMPAL	Common circuit design modify	add PC417,PC418 between VCCP_B++ and GND	
16			08/12/17	COMPAL	Common circuit design modify	change PR434.1,PR431.1 POWER source from +5VS to +5ALW	
17	45	+1.5VSP	08/12/17	COMPAL	Common circuit design modify	add PC421,PC422 between +1.5VSP_B++ and GND	
18			08/12/17	COMPAL	Common circuit design modify	change PR427.1,PR418.1 POWER source from +5VS to +5ALW	
19	47	+CPU_CORE	08/12/17	COMPAL	Common circuit design modify	add PC148,PC149,PC150,PC151 between +CPU_B+ and GND	
20			08/12/17	COMPAL	Common circuit design modify	add PR176 between PU11.12 and PU11.13	
21			08/12/17	COMPAL	Common circuit design modify	reserve PR184 between PU11.11 and GND	
22	48	+VGA_COREP	08/12/22	COMPAL	Change VID require	change PR410 to 8.45K ohm	
23			08/12/22	COMPAL	Relink data base	Relink data base for PQ98	
24							
25							

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P10	Cantiga(4/6)-PWR	12/15/2008	EE	DIS can not boot issue	a. change L13 L14 BOM structure from "UMA@" to "g" b. change R1400 R1401 BOM structure to "UMA@"	X02
2	P17	ICH9(1/4)-PCI/INT	12/15/2008	EE	PCI reset and PLT reset connect error	change R1112 pin 1 net name from PLT_RST# to PCI_RST#	X02
3	P24	Codec 92HD81B	12/15/2008	EE	Internal MIC no function issue	add a 2.49K ohm pull high resistor (R315) to +5VS at SENSE_A	X02
4	P27	PWR_OK/BTN/TP	12/15/2008	EE	CAP sensor no function issue	SWAP JFN1 pin 6 and pin 7 signals	X02
5	P27	PWR_OK/BTN/TP	12/15/2008	EE	Battery only can not boot issue	The breakdown voltage of D63 is too low now. Change D63 back to old part.	X02
6	P19	ICH9(3/4)_DMI,USB,GPIO,PCIE	12/15/2008	EE	part change to consistent with 13" and 15"	Change Q106 to SSM3K7002FU_SC70-3 and add Q107	X02
7	P26	BIOS & EC I/O Port	12/15/2008	EE	Add wake on LAN feature	change PCIE wake up signal connection to support wake up on LAN/WLAN feature.	X02
8	P23	WLAN/BT/FP	12/16/2008	EE	WLAN card S3/S4 resume fail issue and add wake on LAN function	Add Q129 and net WLANPW_DIS# to switch +3V_WLAN power from +3VALW unpop R412, R415	X02
9	P10	Cantiga(4/6)-PWR	12/16/2008	EE	follow 13"/15" design	change R101 from 0603 to 0805 size	X02
10	P26	BIOS & EC I/O Port	12/16/2008	EE	follow 13"/15" design	unpop R77 R78	X02
11	P21	Gigabit LAN_RTL8111DL	12/16/2008	EE	follow 13"/15" design	Change C1484, C1485 from 0.1uF to 1uF	X02
12	P10	Cantiga(4/6)-PWR	12/16/2008	EE		change R69 to L15	X02
13	P24	Codec 92HD81B	12/16/2008	EE	vendor (IDT) request	unpop C260 C262	X02
14	P22	HDD/CDROM	12/17/2008	ME	For ODD CONN SMT issue	Change part of JSATA2	X02
15	P34 P35	NVG94 External GDDR3	12/17/2008	EE		Change Q135 Q136 to SSM3K7002FU_SC70-3	X02
16	P29	OZ129_Card Reader / 1394	12/19/2008	EE	For Card Reader / 1394 issue	add a LDO (U65) for +1.8VS_CB	X02
17	P16	CRT CONN/LCD CONN	12/19/2008	EE	U29 pin 21 (INVT_PWM) broken issue	add a ESD diode(D51) to INVT_PWM close to JLCD1	X02
18	P29	OZ129_Card Reader / 1394	12/19/2008	EE	crystal vendor suggestion	change X3 bypass CAP. C1781 C1785 from 15pF to 18pF	X02
19	P21	Gigabit LAN_RTL8111DL	12/19/2008	EE	crystal vendor suggestion	change Y9 from CL=20pF to CL=12pF change C1488=18pF, C1489=15pF	X02
20	P7	Cantiga(1/6)-AGTL/DMI/DDR	12/22/2008	EE	13"/15" system hang with some special CPUs issue	Reserve 0.1uF Cap. C141 at H_DPRSTP# close to MCH	X02
21	P38	Screws	12/22/2008	ME	ME change ODD connector and change screw holes	remove H14	X02
22	P07~P12	GMCH	12/22/2008	EE	GMCH revision change	change GMCH from A1 version to B3	X02
23	P18	ICH9(2/4)_LAN,HD,IDE,LPC	12/23/2008	EE	crystal vendor suggestion	change C1211 from 15pF to 12pF	X02
24	P23	WLAN/BT/FP	12/23/2008	EE	ESD team request	change D22, D62 to SC300000000	X02
25	P24	Codec 92HD81B	12/23/2008	EE	ESD team request	change D19, D20, D21, D27 to SCA00000T00	X02
26	P27	PWR_OK/BTN/TP	12/23/2008	EE	ESD team request	change D63 D24 to SC300000000	X02
27	P28	USB/ESATA/1394 CONN	12/23/2008	EE	ESD team request	change D58 D59 D60 to SC300000000	X02
28	P27	PWR_OK/BTN/TP	12/23/2008	EE	ESD team request	change L10, L23 from 301T to 801T pop C27, C28	X02
29	P23	WLAN/BT/FP	12/23/2008	EE	ESD team request	add a 1000pF cap C414 at +3VS close to JCA1	X02
30	P28	USB/ESATA/1394 CONN	12/24/2008	EE	follow 13"/15" schematic	change R155 R1257 R1262 R1267 from 30K to 470 ohm un-pop R1255 R1260 R1264 R1269	X02
31	P29	OZ129_Card Reader / 1394	01/05/2009	EE	customer suggestion	change LDO output to 1.95V	X02
32							

KAL60 POWER UP SEQUENCE





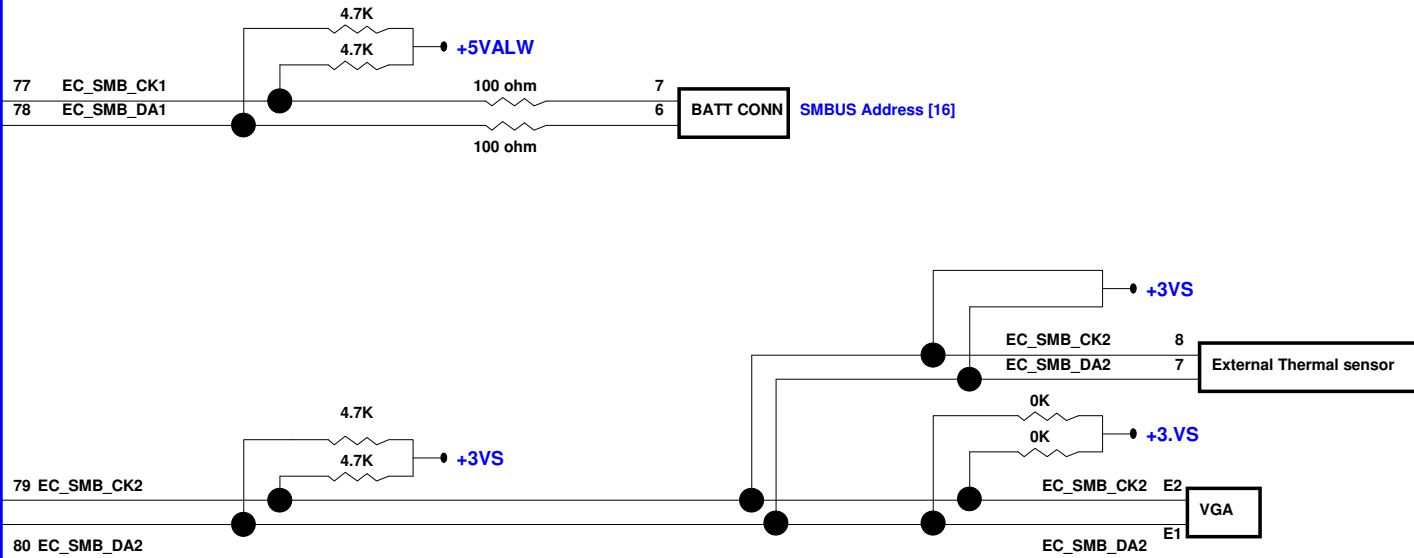
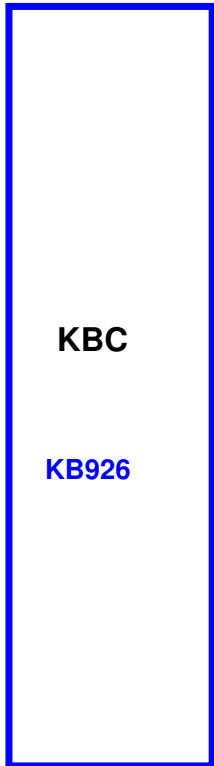
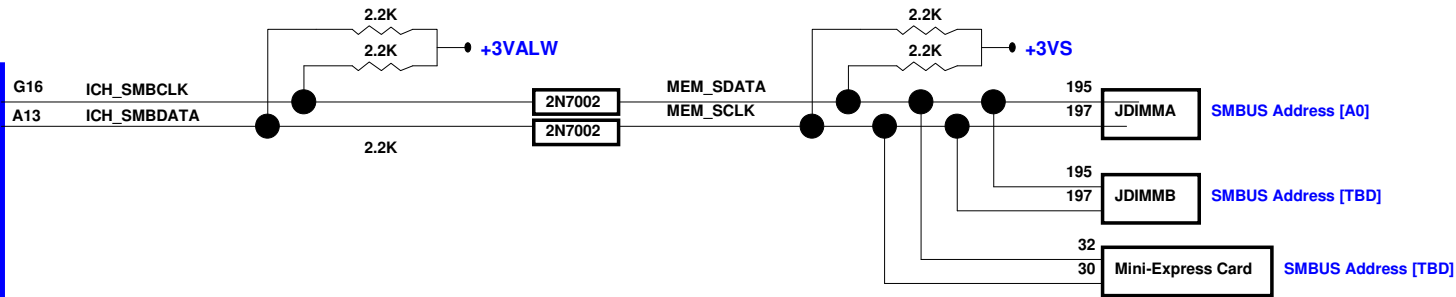
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