Winery13 CALPELLA DIS N11M-GE1 Schematics

uFCPGA Mobile Arrandale

Intel Ibex Peak-M

2010-01-13

REV : A00

DY : Nopop Component

UMA : Pop when schematic is UMA

DIS : Pop when schematic is DIS

<Core Design>

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Winery CALPELLA Block Diagram

PCB LAYER

L1: Top
L2: GND
L3: Signal
L4: Signal
L5: VCC
L6: Signal
L7: GND
L8: Bottom

Project code : 91.4EX01.001
Part Number : 48.4EX01.001
PCB P/N : 09288
Revision : A00

Clock Generator SLG8SP585 7

VRAM(gDDR3) 64Mbx16x4 (512MB) 84,85
VRAM
Nvidia N11M-GE1(40nm) 80,81,82,83
100MHz/ 2.5Gbps
PCIe x 16
Bandwidth :8GB
LVDS
RGB CRT

Intel CPU Arrandale 8,9,10,11,12,13,14
DDRIII 1066 Channel A 800/1066MHz
DDR III 1066 Channel B 800/1066MHz
DDRIII 1066 Slot 0 18
DDRIII 1066 Slot 1 19

Power SW TPS2231R 34
New Card (FPC Cable to Connect) 34
PCIE x 1 & USB 2.0 x 1

CRT 55
LCD (Single Chanel) 54
RGB CRT
LVDS
Switchable 74

DMIx4 2.5 GT/s
FDI (UMA) 2.7 GT/s
100MHz 2.5Gbps
PCIE

Intel PCH
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
20,21,22,23,24,25,26,27,28

10/100/1000LOM RTL8111DL 35
RJ45 CONN
Mini-Card WWAN/ WiMAX? 64
Left Side: USB x 1
(On daughter board)
USB 2.0 x 2
PCIE x 1
USB 2.0 x 1

Mini-Card WLAN 802.11a/b/g/n 64
Right Side: USB x 1 63
Bluetooth 73
Biometric 78

CardReader REALTEK RTS5138 32
(3 in 1) SD/MMC/MMC+ 33
USB 2.0 480Mbps

CAMERA 73
Digital Mic Array
USB2.0 x 1
Azalia CODEC OP AMP IDT 92HD81UA 30
AZALIA 24MHz
MIC IN
HP OUT
1CH SPEAKER 60

SM Bus 400KHz
Free fall sensor 40
LPC Bus 33MHz

KBC NUVOTON NPCE781BA0DX 37
SPI
SM Bus
Thermal & Fan EMC2102 39,58
Capacity Board 78

SATA, USB
SATA 3Gbps
SPI
USB,ESATA Multi-Port x1 63
ODD HDD 59
Flash ROM 4MB 62
Flash ROM 256kB 62
Touch PAD 68
Int. KB 68

CPU DC/DC ISL62883 47,48

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC RT8205B 46

INPUTS	OUTPUTS
+PWR_SRC	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC TPS51116 50

INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC ADP3211 53

INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

SYSTEM DC/DC TPS51218 86

INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

CHARGER BQ24745 45

INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC TPS51218 49

INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

LDO APL5930 51

INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

LDO RT9025 51

INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN_GPU

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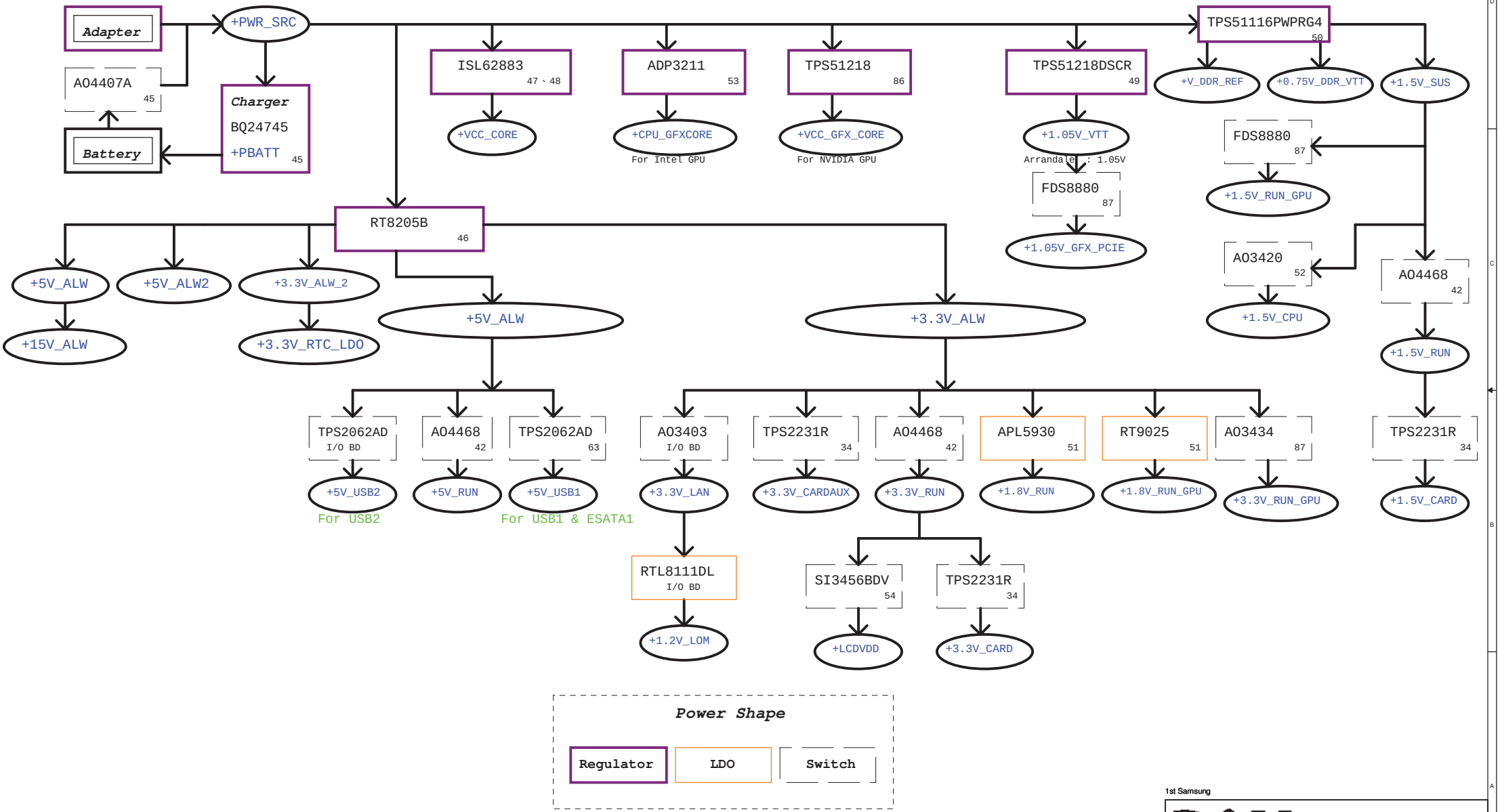

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Title: Power Block Diagram

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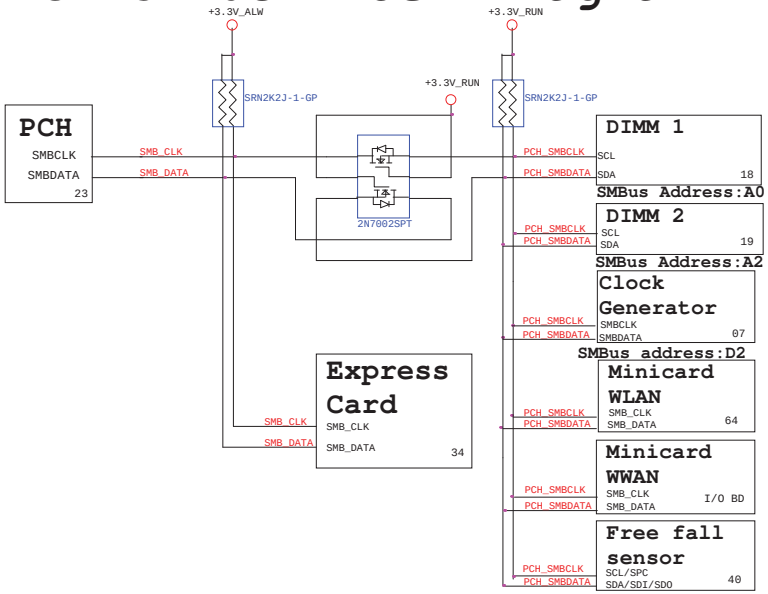
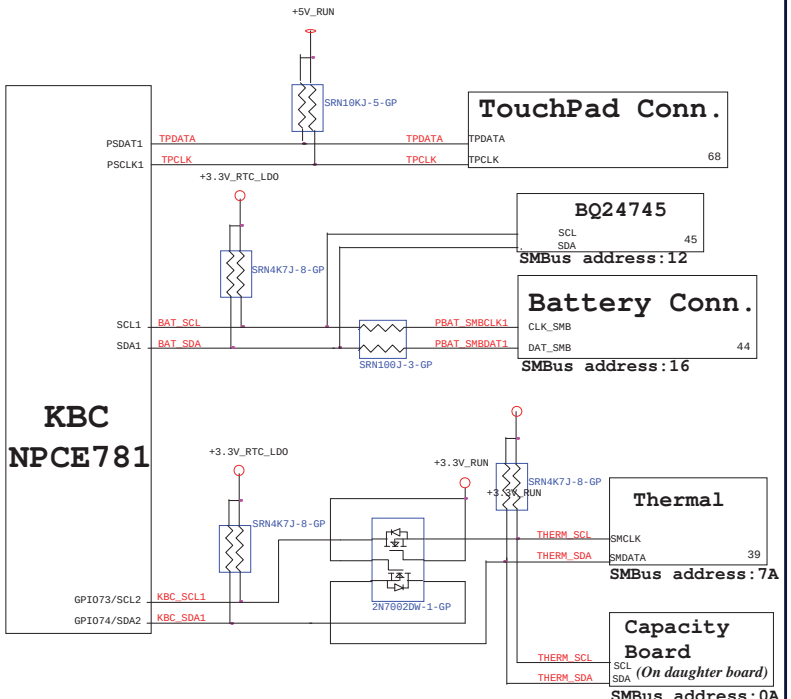
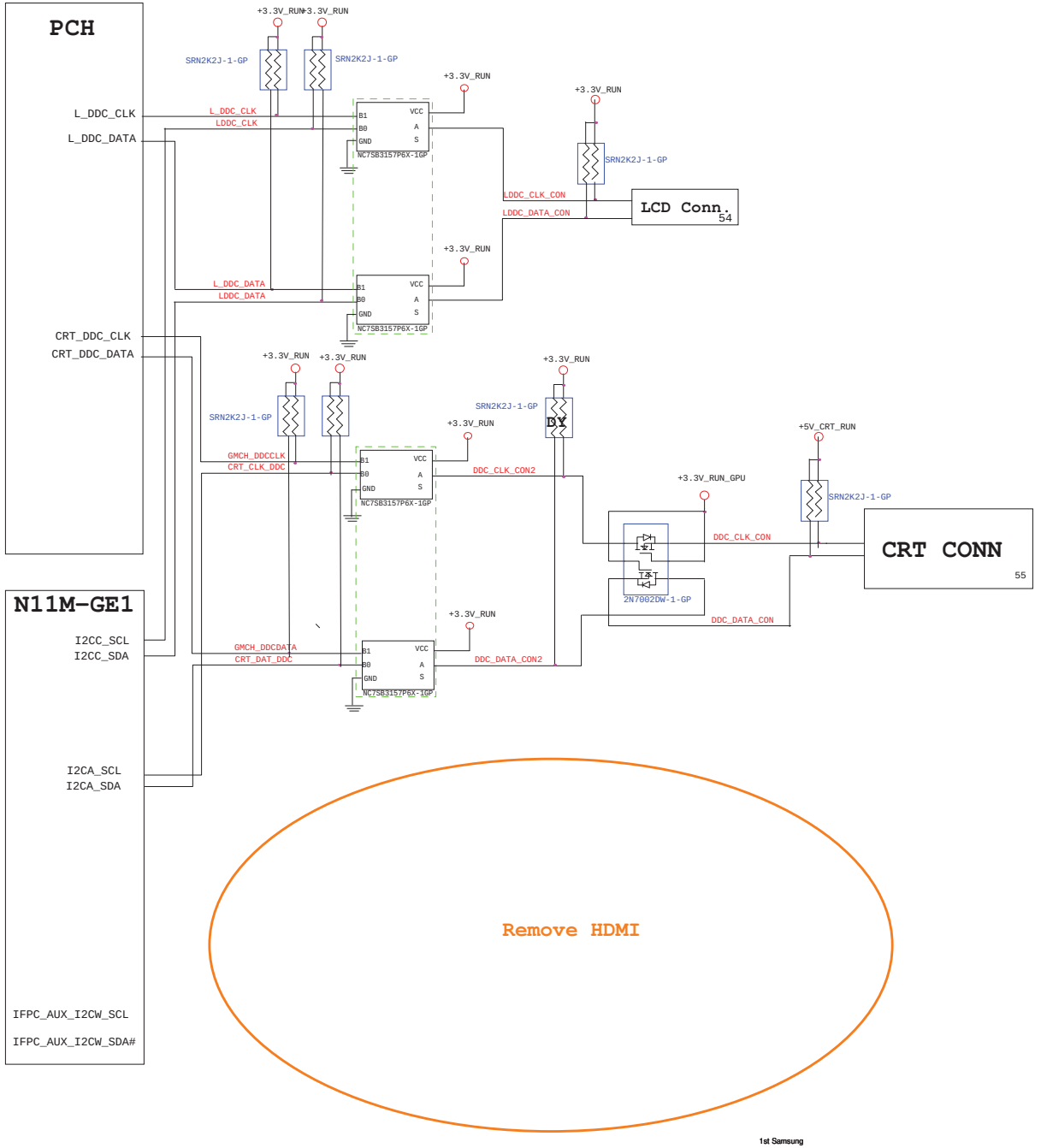
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Switchable Graphic SMBus Block Diagram



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Title: SMBUS Block Diagram

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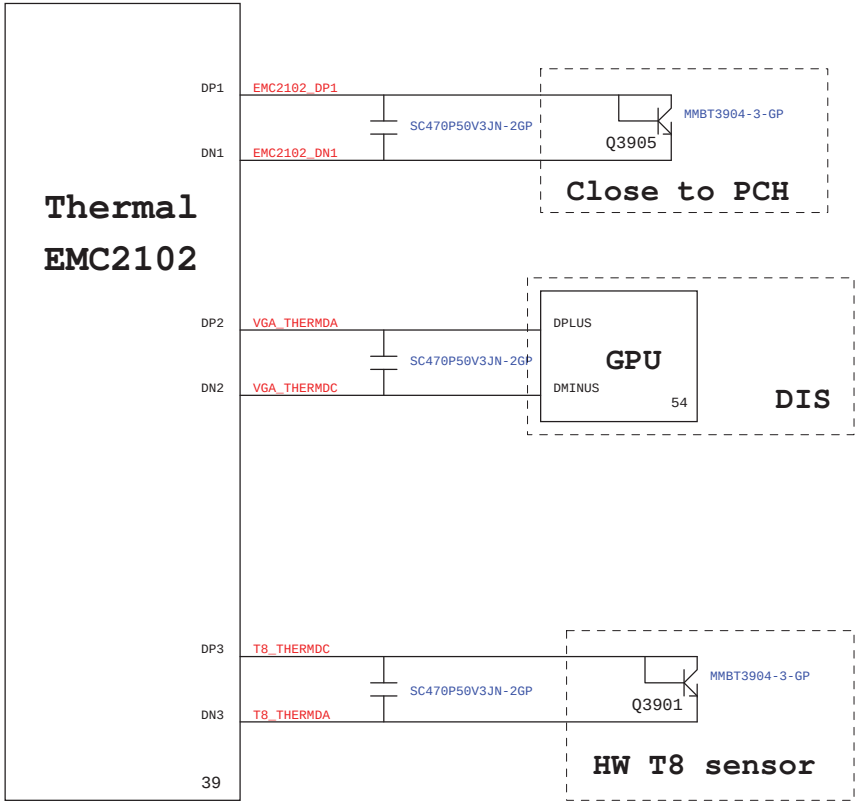
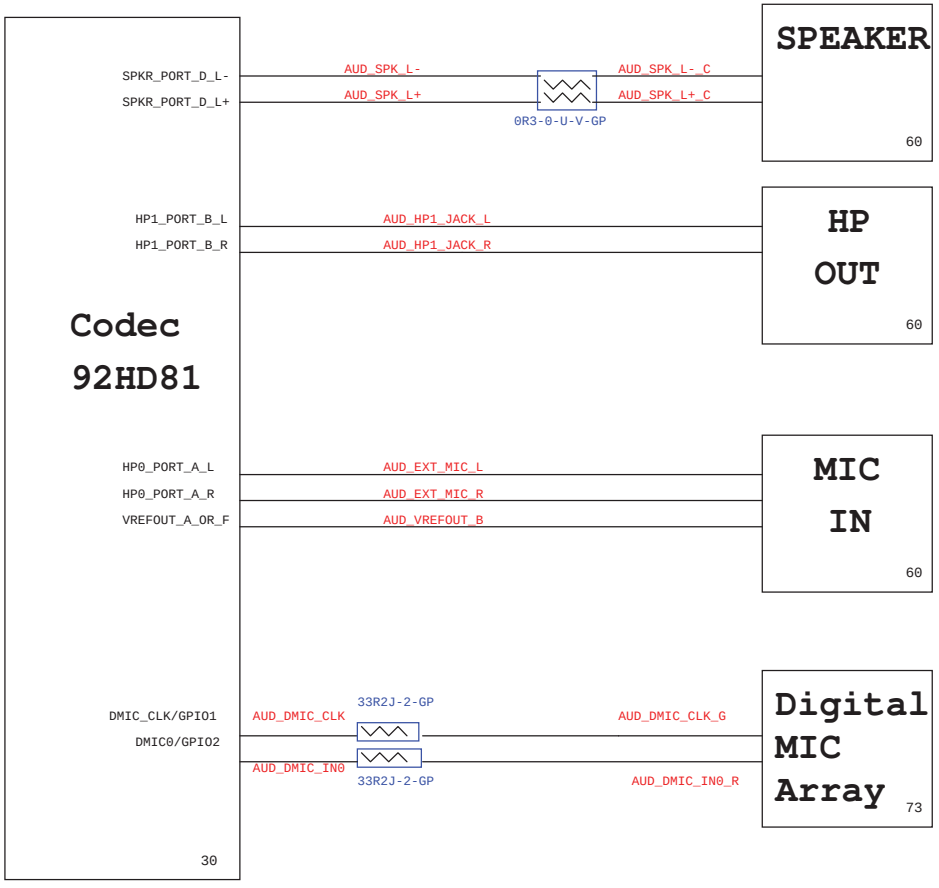
Thermal Block Diagram



Audio Block Diagram



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Title	Thermal/Audio Block Diagram	
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PCH Strapping Calpella Schematic Checklist Rev1.6

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor. Intel suggest 1K resistor (Fonseca)
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** Note: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ; do not stuff resistor.
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled** **Note:** CRB uses a 330-kΩ resistor.
GNT0#, GNT1#	**Default (SPI):** Leave both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	**Enable Intel Anti-Theft Technology:**Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Intel Anti-Theft Technology:**Left floating, no pull-down required.
NV_ALE	**Enable Intel Anti-Theft Technology:**Connect to +NVRAM_Vccq with 8.2-kΩ weak pull-up resistor.[CRB has it pulled up with 1-kΩ no-stuff resistor] **Disable Intel Anti-Theft Technology:**Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0)–** Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. **High (1)–:**Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. **Note:**CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	**Low (0)–**Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality **High (1)–:**Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality **Note:** This is an unmuxed signal. This signal has a weak internal pull-down of 20 KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kΩ pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	**Default = Do not connect (floating). Internal pull-up.** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping Calpella Schematic Checklist Rev1.6

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1

PCIE Routing

LANE1	Card reader
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	New Card

USB Table

USB	
Pair	Device
0	USB1
1	USB for ESATA
2	USB2
3	RESERVE
4	WLAN
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BlUETOOTH
9	Card Reader
10	Biometric
11	CAMERA
12	New Card
13	RESERVED

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Title: Table of Content

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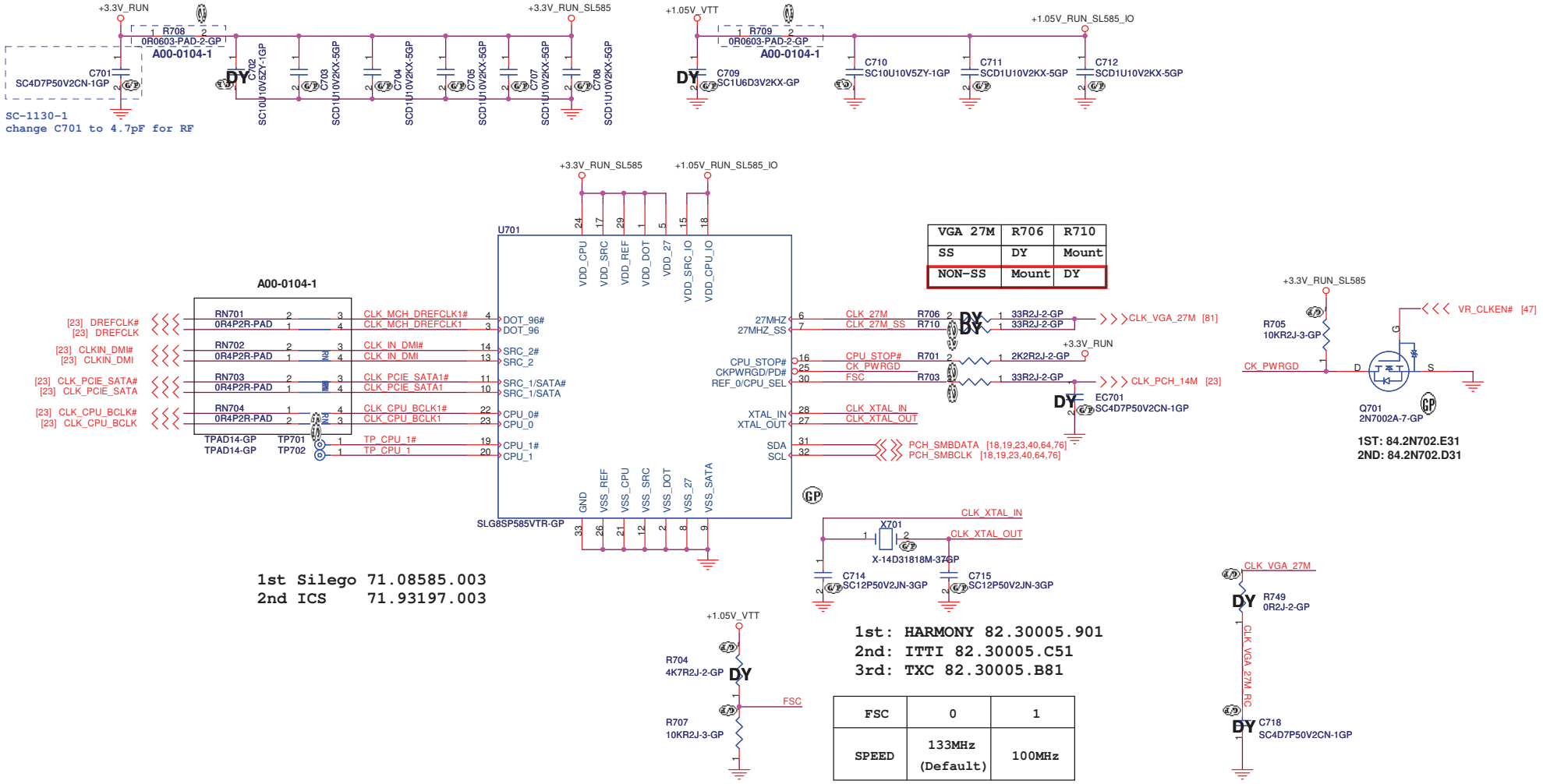
SSID = Clock GEN



VGA 27M	R706	R710
SS	DY	Mount
NON-SS	Mount	DY

1ST: 84.2N702.E31
2ND: 84.2N702.D31

1st Silego 71.08585.003
2nd ICS 71.93197.003

1st: HARMONY 82.30005.901
2nd: ITTI 82.30005.C51
3rd: TXC 82.30005.B81

FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: Clock Generator SLG8SP585

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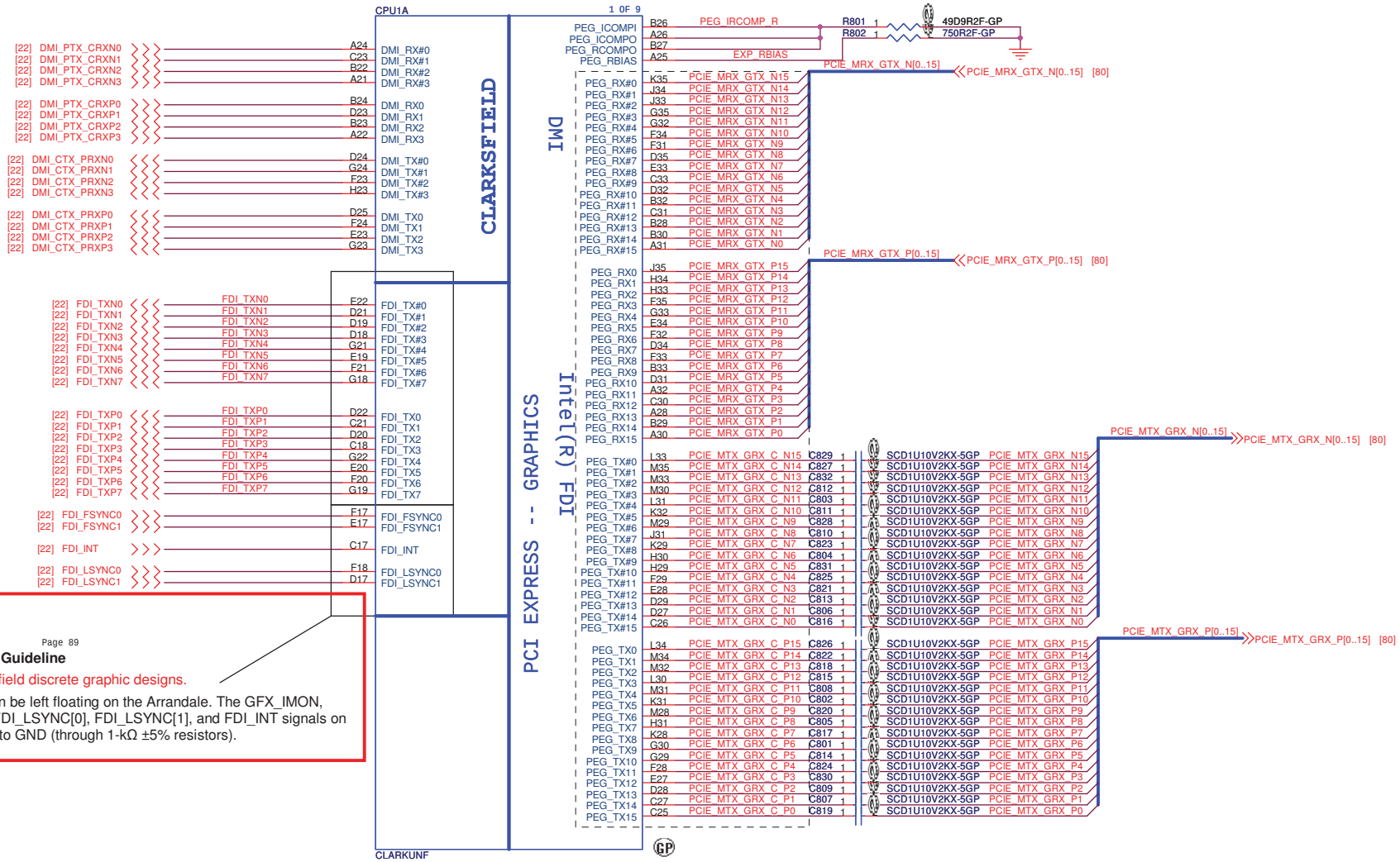
SSID = CPU



Calpella Platform Design Guide
Revision 1.6

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2.4 Arrandale Graphics Disable Guideline

It applies to Arrandale and Clarksfield discrete graphic designs.

FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

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Title: **CPU (PCIE/DMI/FDI)**

Size | Document Number: **Winery13 MB DIS** | Rev: **A00**

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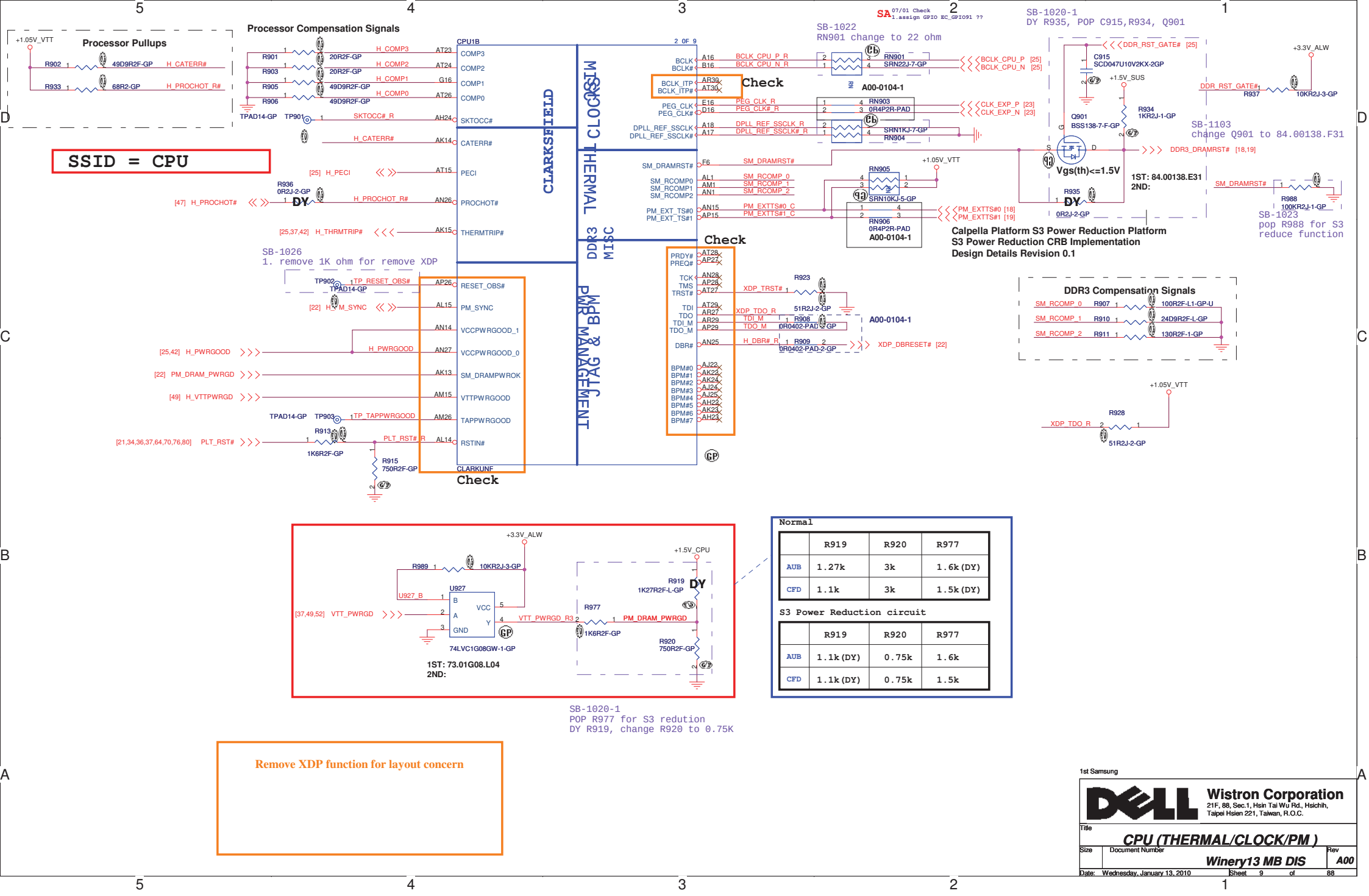

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Title: CPU (THERMAL/CLOCK/PM)

Size | Document Number: Winery13 MB DIS | Rev: A00

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SSID = CPU

CPU1C

3 OF 9

CLARKSFIELD

DDR SYSTEM MEMORY A

CLARKUNF

CPU1D

4 OF 9

CLARKSFIELD

DDR SYSTEM MEMORY - B

CLARKUNF

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Title	CPU (DDR)
Size	Document Number: Winery13 MB DIS
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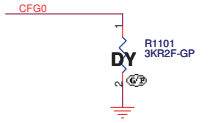
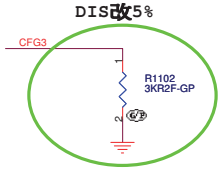
SSID = CPU



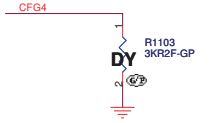
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



DW

07/10 Reversal
1.PCI-Express Static Lane Reversal

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

Calpella Platform Design Guide
Revision 1.6

4.8.3.1 LVDS Switching

Switchable GFX, just like integrated GFX only, to enable LVDS it is required that the OEM set the LDVS (L_DDC_DATA) strap to present (pulled up) and the eDP strap (CFG[4]) to disabled (not pulled down).

4.8.3.2 eDP Switching

eDP for Switchable GFX can only be driven out of Port D of PCH. To configure Port D for embedded DP it is required to set the DDPD_CTRLDATA strap high to 3.3V Core rail through 2.2 kΩ ±5% resistor, LVDS (L_DDC_DATA) strap as no connect and the eDP strap CFG[4] as no connect.

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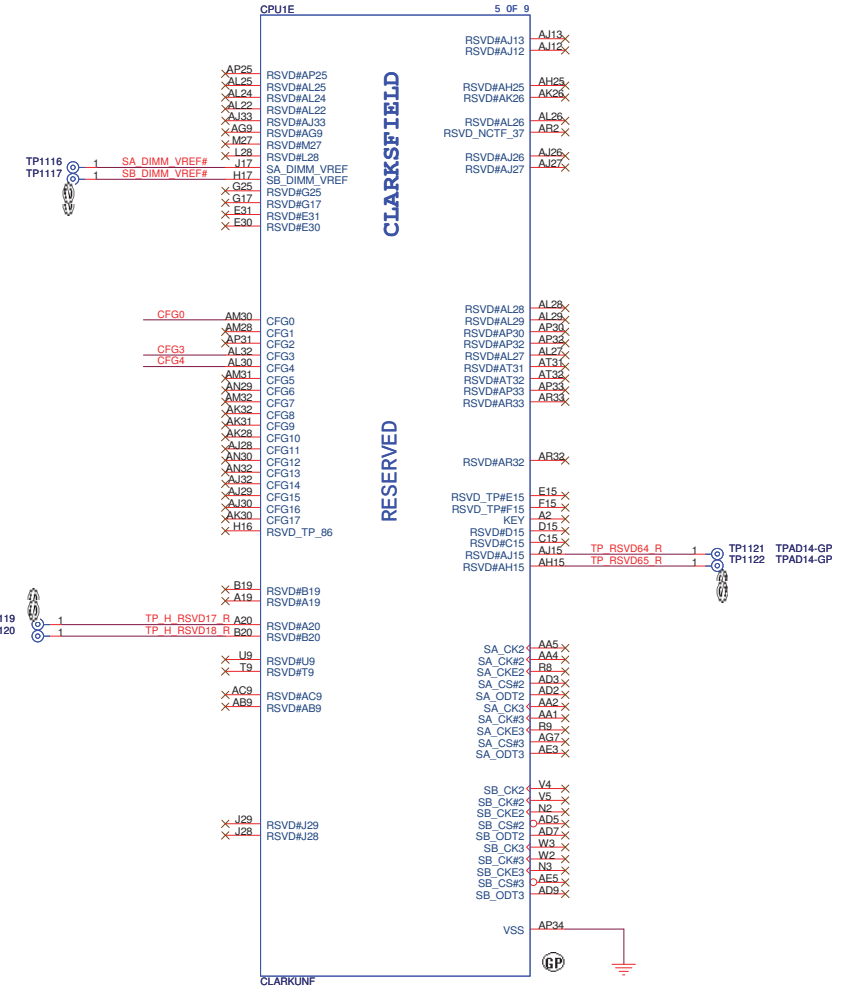
DW

07/02 Added
1.Added display Switchable strap commentariat

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

DW30 Only support Arrandale, CFG7 no need pull down



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Title		
CPU (RESERVED)		
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SSID = CPU

PROCESSOR CORE POWER

48A (Arburdale)

18A

CLARKSFIELD

CPU1F

6 OF 9

1.1V RAIL POWER

CPU CORE SUPPLY

CPU VIDS

SENSE LINES

POWER

CLARKUNF

+VCC_CORE

+1.05V_VTT

C1206 C1207 C1208 C1209 C1220 C1210 — SC10U6D3V5KX-1GP / SC22U6D3V6MX-2GP

C1212 C1213 C1214 C1215 C1223 C1224 — SC10U6D3V5KX-1GP / SC22U6D3V6MX-2GP

C1225 C1226 C1227 C1228 C1229 C1230 C1231 C1232 — SC22U6D3V5MX-2GP / SC10U6D3V5KX-1GP

C1235 C1236 C1237 C1238 C1239 C1240 C1241 C1242 — SC10U6D3V5KX-1GP / SC22U6D3V6MX-2GP / SC10U6D3V6MX-3GP

C1243 SCD1U50V3KX-GP

SC-1207-1
pop C1243 and change size to 0603 for EMI

C1201 C1202 C1203 C1216 C1217 C1218 C1219 C1204 C1205 — SC10U6D3V5KX-1GP / SC22U6D3V6MX-2GP / SC1U6D3V2KX-GP

C1211 C1221 C1222 — SC10U6D3V5KX-1GP / SC22U6D3V6MX-2GP / SC10U6D3V6MX-3GP

C1233 C1234 — SC10U6D3V5KX-1GP / SC10U6D3V6MX-3GP

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are
Arrandale VTT=1.05V;
Clarksfield VTT=1.1V

H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

SA
07/01 Check
1.DPRSLPVR ??

PSI# AN33 → PSI# [47]

VID AK35 CPU_VID0, AK33 CPU_VID1, AK34 CPU_VID2, AL35 CPU_VID3, AL33 CPU_VID4, AM33 CPU_VID5, AM35 CPU_VID6 → CPU_VID[6..0] [47]

PROC_DPRSLPVR AM34 → PM_DPRSLPVR [47]

VTT_SELECT G15 TP_H_VTTVID1 → TP1203 TPAD14-GP

ISENSE AN35 → IMVP_IMON [47]

VCC_SENSE AJ34 VCC_SENSE, VSS_SENSE AJ35 VSS_SENSE → VCC_SENSE [47], VSS_SENSE [47]

VTT_SENSE B15, VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT → VTT_SENSE [49] → TP1202 TPAD14-GP

R1201 100R2F-L1-GP-U

R1204 100R2F-L1-GP-U

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Title: CPU (VCC_CORE)

Size | Document Number: Winery13 MB DIS | Rev: A00

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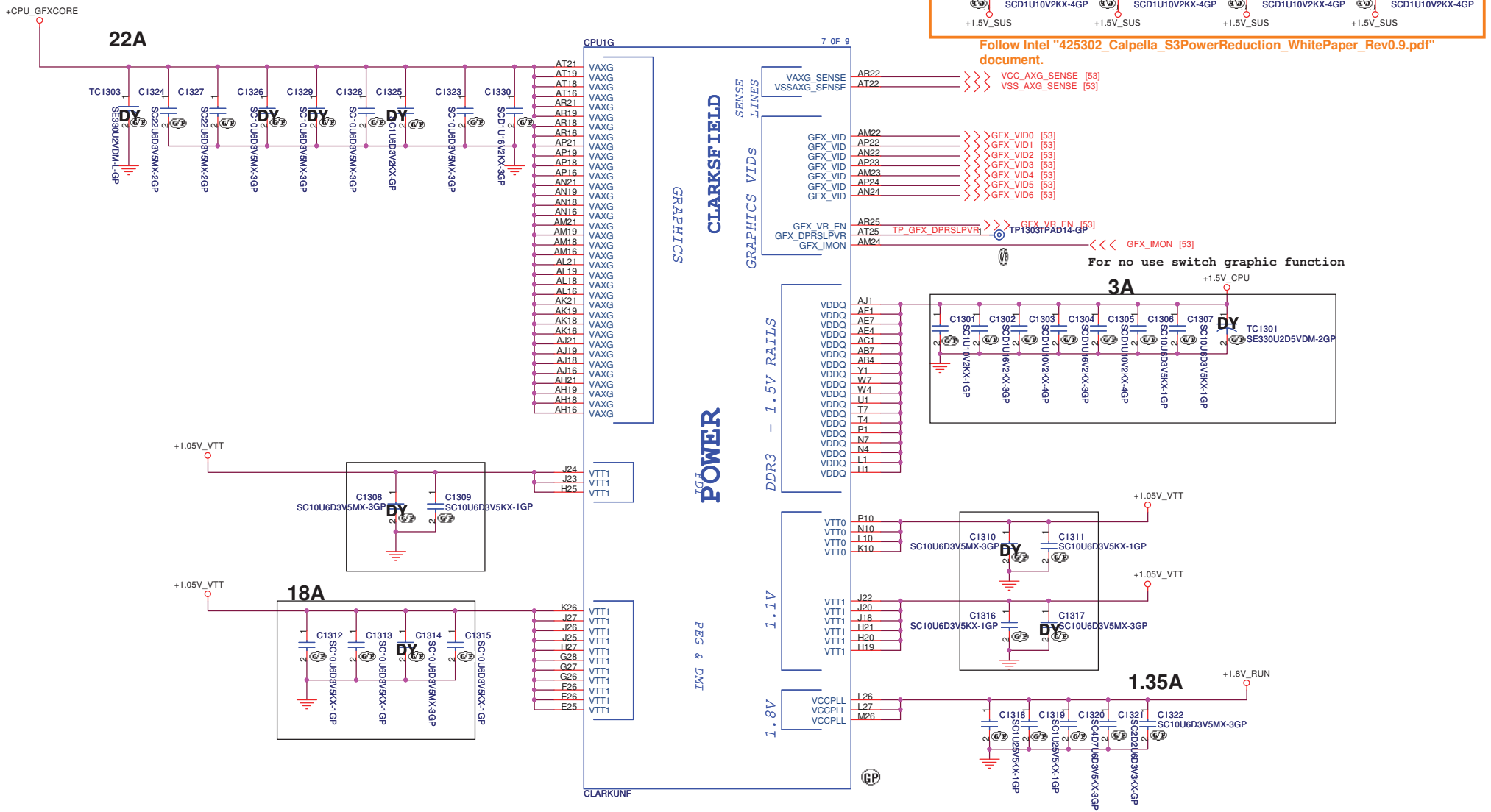
SSID = CPU



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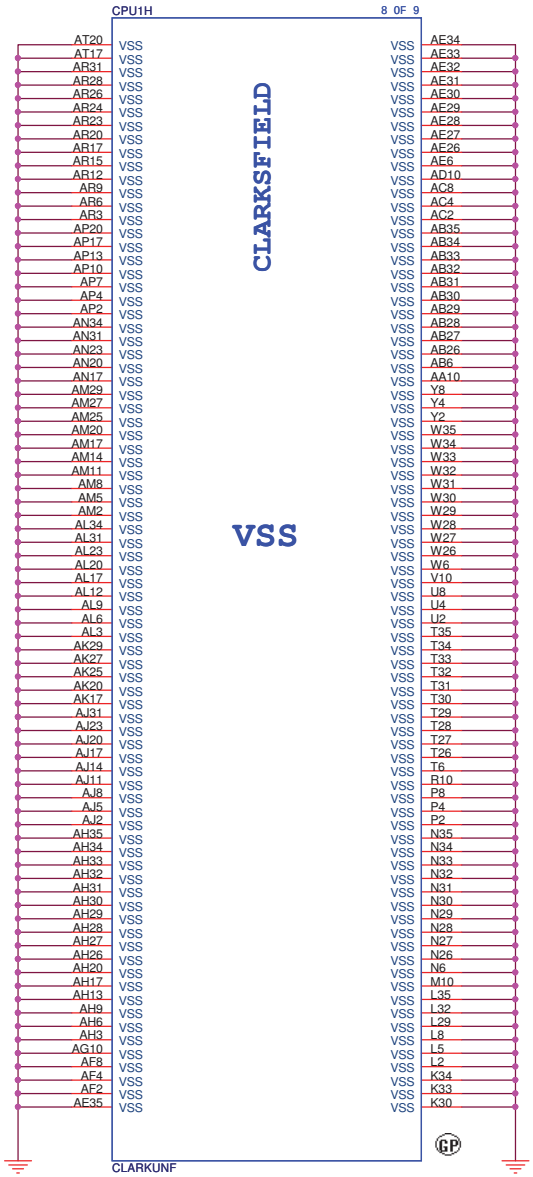
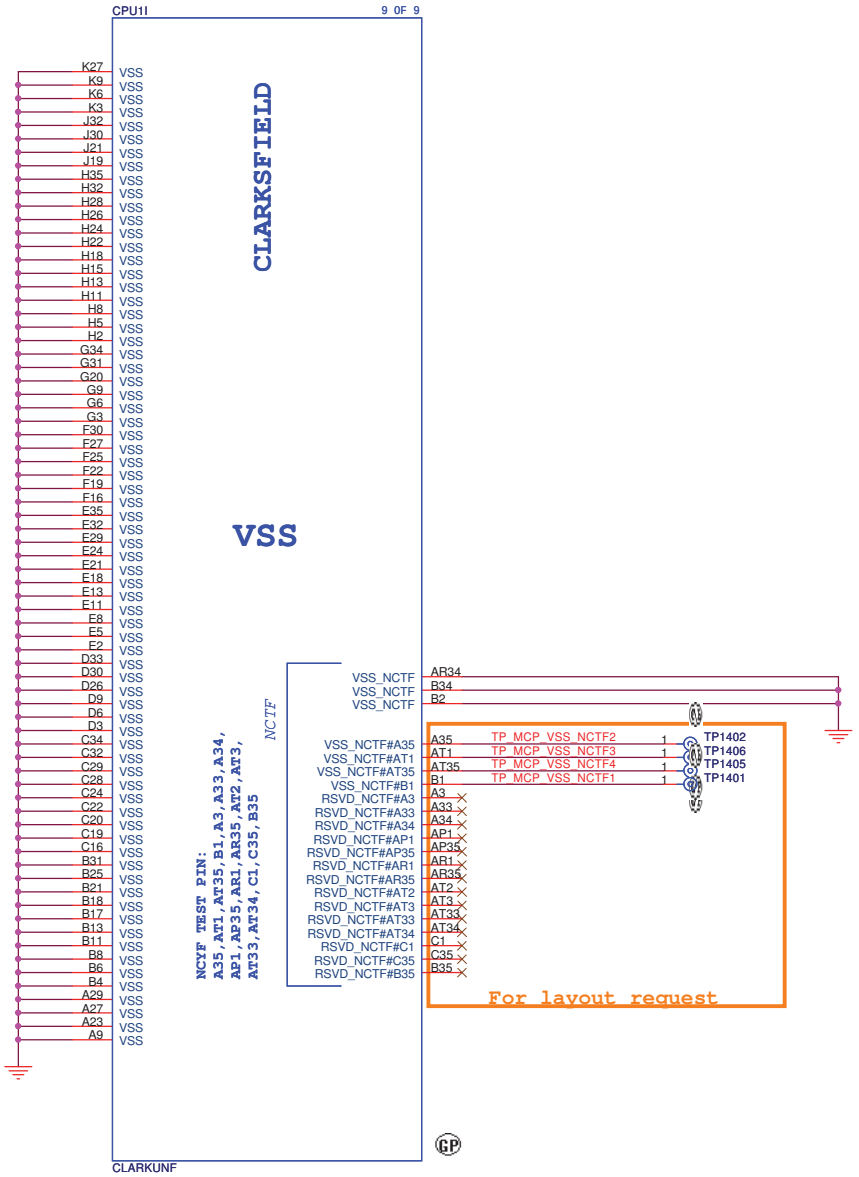
Title	CPU (VCC_GFXCORE)
Size	Document Number: Winery13 MB DIS
Rev	A00
Date: Wednesday, January 13, 2010	Sheet 13 of 88

SSID = CPU





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Title	CPU (VSS)	
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Title: *Reserved*

Size: A3 | Document Number: *Winery13 MB DIS* | Rev: *A00*

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Title: *(Reserve)*

Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

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SSID = MEMORY

[10] M_A_DQS#[7..0]
[10] M_A_DQ[63..0]
[10] M_A_DM[7..0]
[10] M_A_DQS[7..0]
[10] M_A_A[15..0]

DM1

M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15
[10] M_A_BS2 M_A_BS2 79 A16/BA2
[10] M_A_BS0 M_A_BS0 109 BA0
[10] M_A_BS1 M_A_BS1 108 BA1

M_A_DQ0 5 DQ0
M_A_DQ1 7 DQ1
M_A_DQ2 15 DQ2
M_A_DQ3 17 DQ3
M_A_DQ4 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ6 16 DQ6
M_A_DQ7 18 DQ7
M_A_DQ8 21 DQ8
M_A_DQ9 23 DQ9
M_A_DQ10 33 DQ10
M_A_DQ11 35 DQ11
M_A_DQ12 22 DQ12
M_A_DQ13 24 DQ13
M_A_DQ14 34 DQ14
M_A_DQ15 36 DQ15
M_A_DQ16 39 DQ16
M_A_DQ17 41 DQ17
M_A_DQ18 51 DQ18
M_A_DQ19 53 DQ19
M_A_DQ20 40 DQ20
M_A_DQ21 42 DQ21
M_A_DQ22 50 DQ22
M_A_DQ23 52 DQ23
M_A_DQ24 57 DQ24
M_A_DQ25 59 DQ25
M_A_DQ26 67 DQ26
M_A_DQ27 69 DQ27
M_A_DQ28 56 DQ28
M_A_DQ29 58 DQ29
M_A_DQ30 68 DQ30
M_A_DQ31 70 DQ31
M_A_DQ32 129 DQ32
M_A_DQ33 131 DQ33
M_A_DQ34 141 DQ34
M_A_DQ35 143 DQ35
M_A_DQ36 130 DQ36
M_A_DQ37 132 DQ37
M_A_DQ38 140 DQ38
M_A_DQ39 142 DQ39
M_A_DQ40 147 DQ40
M_A_DQ41 149 DQ41
M_A_DQ42 157 DQ42
M_A_DQ43 159 DQ43
M_A_DQ44 146 DQ44
M_A_DQ45 148 DQ45
M_A_DQ46 158 DQ46
M_A_DQ47 160 DQ47
M_A_DQ48 163 DQ48
M_A_DQ49 165 DQ49
M_A_DQ50 175 DQ50
M_A_DQ51 177 DQ51
M_A_DQ52 164 DQ52
M_A_DQ53 166 DQ53
M_A_DQ54 174 DQ54
M_A_DQ55 176 DQ55
M_A_DQ56 181 DQ56
M_A_DQ57 183 DQ57
M_A_DQ58 191 DQ58
M_A_DQ59 193 DQ59
M_A_DQ60 180 DQ60
M_A_DQ61 182 DQ61
M_A_DQ62 192 DQ62
M_A_DQ63 194 DQ63

M_A_DQS#0 10 DQS0#
M_A_DQS#1 27 DQS1#
M_A_DQS#2 45 DQS2#
M_A_DQS#3 62 DQS3#
M_A_DQS#4 135 DQS4#
M_A_DQS#5 152 DQS5#
M_A_DQS#6 169 DQS6#
M_A_DQS#7 186 DQS7#

M_A_DQS0 12 DQS0
M_A_DQS1 29 DQS1
M_A_DQS2 47 DQS2
M_A_DQS3 64 DQS3
M_A_DQS4 137 DQS4
M_A_DQS5 154 DQS5
M_A_DQS6 171 DQS6
M_A_DQS7 188 DQS7

[10] M_ODT0 M_ODT0 116 ODT0
[10] M_ODT1 M_ODT1 120 ODT1

126 VREF_CA
1 VREF_DQ

[9,19] DDR3_DRAMRST# 30 RESET#

203 VTT1
204 VTT2

NP1 NP1
NP2 NP2

RAS# 110 M_A_RAS# [10]
WE# 113 M_A_WE# [10]
CAS# 115 M_A_CAS# [10]

CS0# 114 M_CS0# [10]
CS1# 121 M_CS1# [10]

CKE0 73 M_CKE0 [10]
CKE1 74 M_CKE1 [10]

CK0 101 M_CLK_DDR0 [10]
CK0# 103 M_CLK_DDR#0 [10]
CK1 102 M_CLK_DDR1 [10]
CK1# 104 M_CLK_DDR#1 [10]

DM0 11 M_A_DM0
DM1 28 M_A_DM1
DM2 46 M_A_DM2
DM3 63 M_A_DM3
DM4 136 M_A_DM4
DM5 153 M_A_DM5
DM6 170 M_A_DM6
DM7 187 M_A_DM7

SDA 200 PCH_SMBDATA
SCL 202 PCH_SMBCLK

PCH_SMBDATA [7,19,23,40,64,76]
PCH_SMBCLK [7,19,23,40,64,76]

EVENT# 198 PM_EXTTS#0 [9]

VDDSPD 199

SA0 197 SA0_DM1
SA1 201 SA1_DM1

NC#1 77
NC#2 122
NC#/TEST 125

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

VSS 2, 3, 8, 9, 13, 14, 19, 20, 25, 26, 31, 32, 37, 38, 43, 44, 48, 49, 54, 55, 60, 61, 65, 66, 71, 72, 127, 128, 133, 134, 138, 139, 144, 145, 150, 151, 155, 156, 161, 162, 167, 168, 172, 173, 178, 179, 184, 185, 189, 190, 195, 196, 205, 206

Height 5.2mm

DDR3-204P-25-GP

+3.3V_RUN
+1.5V_SUS
+0.75V_DDR_VTT
+V_DDR_REF

C1806 SCD1U10V2KX-5GP
C1807 SC2D2U6D3V3KX-GP DY
C1810 SCD1U10V2KX-5GP
C1817 SCD1U10V2KX-5GP
C1809 SC2D2U6D3V3KX-GP DY

SA0_DM1
SA1_DM1
R1802 10KR2J-3-GP
R1801 10KR2J-3-GP
SMBUS address:A0

DW
07/02 Reserve
1.Added SA0_DM1 pull-up resistor
07/07
2.Reserve pull-hi,lo resistor

Layout Note:
Place near DM1

+1.5V_SUS
C1802 SC10U6D3V5KX-1GP
C1803 SC10U6D3V5KX-1GP
C1804 SC10U6D3V5KX-1GP
C1811 SC10U6D3V5KX-1GP
C1812 SC10U6D3V5KX-1GP
C1816 SC10U6D3V5KX-1GP
TC1803 ST330U2D5VBM-1-GP DY

Layout Note:
Put close to VTT1,VTT2.

Layout Note:
Put between two SO-DIMM

+0.75V_DDR_VTT
C1801 SC1U6D3V2KX-GP
C1813 SC1U6D3V2KX-GP DY
C1814 SC1U6D3V2KX-GP
C1815 SC1U6D3V2KX-GP DY
C1823 SC10U6D3V5MX-3GP DY

DG:
1uF*4 (per SO-DIMM)
10uF*3 (two close to VR and one between the two SO-DIMM)

+1.5V_SUS
C1872 SCD1U10V2KX-4GP
C1873 SCD1U10V2KX-4GP
C1874 SCD1U10V2KX-4GP
C1875 SCD1U10V3KX-4GP

Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9. pdf" document.

put near connector

M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
C1821 DUMMY-C2
C1819 DUMMY-C2
C1820 DUMMY-C2
C1818 DUMMY-C2

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII-SODIMM SLOT1
Size: Custom
Document Number: Winery13 MB DIS
Rev: A00
Date: Wednesday, January 13, 2010
Sheet 18 of 88

SSID = MEMORY

Change CONN
2009/06/01

[10] M_B_DQS#[7..0]
[10] M_B_DQ[63..0]
[10] M_B_DM[7..0]
[10] M_B_DQS[7..0]
[10] M_B_A[15..0]

DM2

M_B_A0 98 A0
M_B_A1 97 A1
M_B_A2 96 A2
M_B_A3 95 A3
M_B_A4 92 A4
M_B_A5 91 A5
M_B_A6 90 A6
M_B_A7 86 A7
M_B_A8 89 A8
M_B_A9 85 A9
M_B_A10 107 A10/AP
M_B_A11 84 A11
M_B_A12 83 A12
M_B_A13 119 A13
M_B_A14 80 A14
M_B_A15 78 A15
[10] M_B_BS2 M_B_BS2 79 A16/BA2
[10] M_B_BS0 M_B_BS0 109 BA0
[10] M_B_BS1 M_B_BS1 108 BA1

M_B_DQ0 5 DQ0
M_B_DQ1 7 DQ1
M_B_DQ2 15 DQ2
M_B_DQ3 17 DQ3
M_B_DQ4 4 DQ4
M_B_DQ5 6 DQ5
M_B_DQ6 16 DQ6
M_B_DQ7 18 DQ7
M_B_DQ8 21 DQ8
M_B_DQ9 23 DQ9
M_B_DQ10 33 DQ10
M_B_DQ11 35 DQ11
M_B_DQ12 22 DQ12
M_B_DQ13 24 DQ13
M_B_DQ14 34 DQ14
M_B_DQ15 36 DQ15
M_B_DQ16 39 DQ16
M_B_DQ17 41 DQ17
M_B_DQ18 51 DQ18
M_B_DQ19 53 DQ19
M_B_DQ20 40 DQ20
M_B_DQ21 42 DQ21
M_B_DQ22 50 DQ22
M_B_DQ23 52 DQ23
M_B_DQ24 57 DQ24
M_B_DQ25 59 DQ25
M_B_DQ26 67 DQ26
M_B_DQ27 69 DQ27
M_B_DQ28 56 DQ28
M_B_DQ29 58 DQ29
M_B_DQ30 68 DQ30
M_B_DQ31 70 DQ31
M_B_DQ32 129 DQ32
M_B_DQ33 131 DQ33
M_B_DQ34 141 DQ34
M_B_DQ35 143 DQ35
M_B_DQ36 130 DQ36
M_B_DQ37 132 DQ37
M_B_DQ38 140 DQ38
M_B_DQ39 142 DQ39
M_B_DQ40 147 DQ40
M_B_DQ41 149 DQ41
M_B_DQ42 157 DQ42
M_B_DQ43 159 DQ43
M_B_DQ44 146 DQ44
M_B_DQ45 148 DQ45
M_B_DQ46 158 DQ46
M_B_DQ47 160 DQ47
M_B_DQ48 163 DQ48
M_B_DQ49 165 DQ49
M_B_DQ50 175 DQ50
M_B_DQ51 177 DQ51
M_B_DQ52 164 DQ52
M_B_DQ53 166 DQ53
M_B_DQ54 174 DQ54
M_B_DQ55 176 DQ55
M_B_DQ56 181 DQ56
M_B_DQ57 183 DQ57
M_B_DQ58 191 DQ58
M_B_DQ59 193 DQ59
M_B_DQ60 180 DQ60
M_B_DQ61 182 DQ61
M_B_DQ62 192 DQ62
M_B_DQ63 194 DQ63

M_B_DQS#0 10 DQS0#
M_B_DQS#1 27 DQS1#
M_B_DQS#2 45 DQS2#
M_B_DQS#3 62 DQS3#
M_B_DQS#4 135 DQS4#
M_B_DQS#5 152 DQS5#
M_B_DQS#6 169 DQS6#
M_B_DQS#7 186 DQS7#

M_B_DQS0 12 DQS0
M_B_DQS1 29 DQS1
M_B_DQS2 47 DQS2
M_B_DQS3 64 DQS3
M_B_DQS4 137 DQS4
M_B_DQS5 154 DQS5
M_B_DQS6 171 DQS6
M_B_DQS7 188 DQS7

[10] M_ODT2 M_ODT2 116 ODT0
[10] M_ODT3 M_ODT3 120 ODT1

126 VREF_CA
1 VREF_DQ

[9,18] DDR3_DRAMRST# 30 RESET#

203 VTT1
204 VTT2

NP1 NP1
NP2 NP2

RAS# M_B_RAS# [10]
WE# M_B_WE# [10]
CAS# M_B_CAS# [10]

CS0# M_CS2# [10]
CS1# M_CS3# [10]

CKE0 M_CKE2 [10]
CKE1 M_CKE3 [10]

CK0 M_CLK_DDR2 M_CLK_DDR2 [10]
CK0# M_CLK_DDR#2 M_CLK_DDR#2 [10]

CK1 M_CLK_DDR3 M_CLK_DDR3 [10]
CK1# M_CLK_DDR#3 M_CLK_DDR#3 [10]

DM0 M_B_DM0
DM1 M_B_DM1
DM2 M_B_DM2
DM3 M_B_DM3
DM4 M_B_DM4
DM5 M_B_DM5
DM6 M_B_DM6
DM7 M_B_DM7

SDA PCH_SMBDATA PCH_SMBDATA [7,18,23,40,64,76]
SCL PCH_SMBCLK PCH_SMBCLK [7,18,23,40,64,76]

EVENT# PM_EXTTS#1 [9]

VDDSPD

SA0 SA0_DM2
SA1 SA1_DM2

NC#1
NC#2
NC#/TEST

VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18

VSS

Height 9.2mm

DDR3-204P-24-GP

+1.5V_SUS

+3.3V_RUN

+0.75V_DDR_VTT

+V_DDR_REF

Layout Note:
Place near DM2

C1905 SC10U6D3V5KX-1GP
C1911 SC10U6D3V5KX-1GP
C1913 SC10U6D3V5KX-1GP
C1916 SC1U6D3V5MX-3GP
C1919 SC10U6D3V5KX-1GP
C1920 SC10U6D3V5KX-1GP
TC1903 ST330U2D5VBM-1-GP

Layout Note:
Put close to VTT1,VTT2.

C1908 SC1U6D3V2KX-GP
C1917 SC1U6D3V2KX-GP
C1918 SC1U6D3V2KX-GP
C1909 SC1U6D3V2KX-GP

DG:
1uF*4 (per SO-DIMM)
10uF*3 (two close to VR and one between the two SO-DIMM)

C1976 SCD1U10V2KX-4GP
C1977 SCD1U10V2KX-4GP
C1978 SCD1U10V2KX-4GP
C1979 SCD1U10V2KX-4GP

Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9.pdf" document.

C1907 SCD1U10V2KX-5GP
C1910 SCD1U10V2KX-5GP
C1914 SC2D2U6D3V3KX-GP

C1906 SCD1U10V2KX-5GP
C1921 SC2D2U6D3V3KX-GP

R1903 10KR2J-3-GP
R1904 10KR2J-3-GP
EC1901 SCD1U25V3KX-GP
R1901 10KR2J-3-GP
R1902 10KR2J-3-GP
SA1_DM2
SA0_DM2

SMBUS address:A4

Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4

put near connector

M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3

C1901 DUMMY-C2
C1904 DUMMY-C2
C1902 DUMMY-C2
C1903 DUMMY-C2

1st Samsung

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII-SODIMM SLOT2

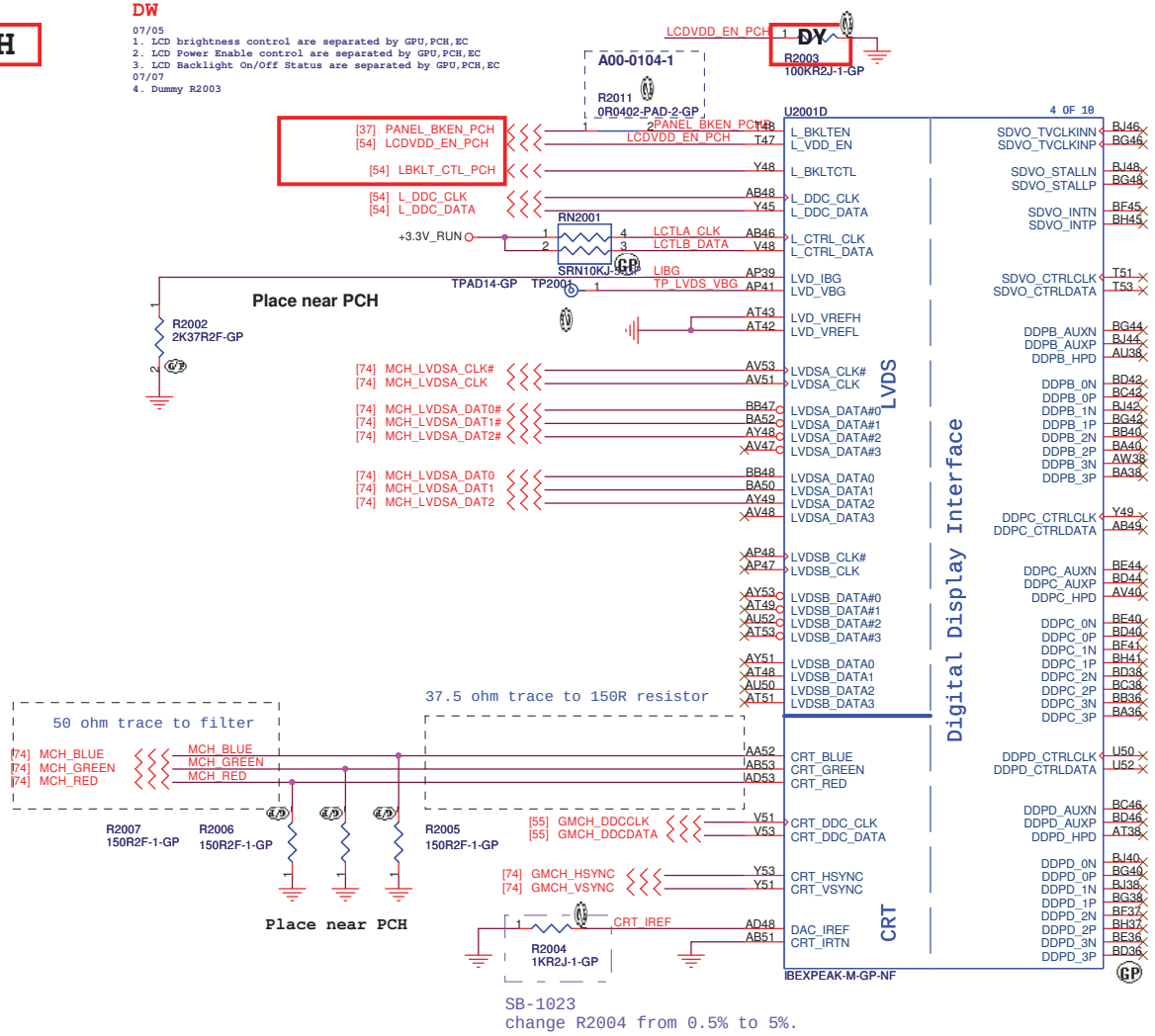
Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 19 of 88

SSID = PCH

DW

07/05
1. LCD brightness control are separated by GPU,PCH,EC
2. LCD Power Enable control are separated by GPU,PCH,EC
3. LCD Backlight On/Off Status are separated by GPU,PCH,EC
07/07
4. Dummy R2003



SB-1023
change R2004 from 0.5% to 5%.

1st Samsung

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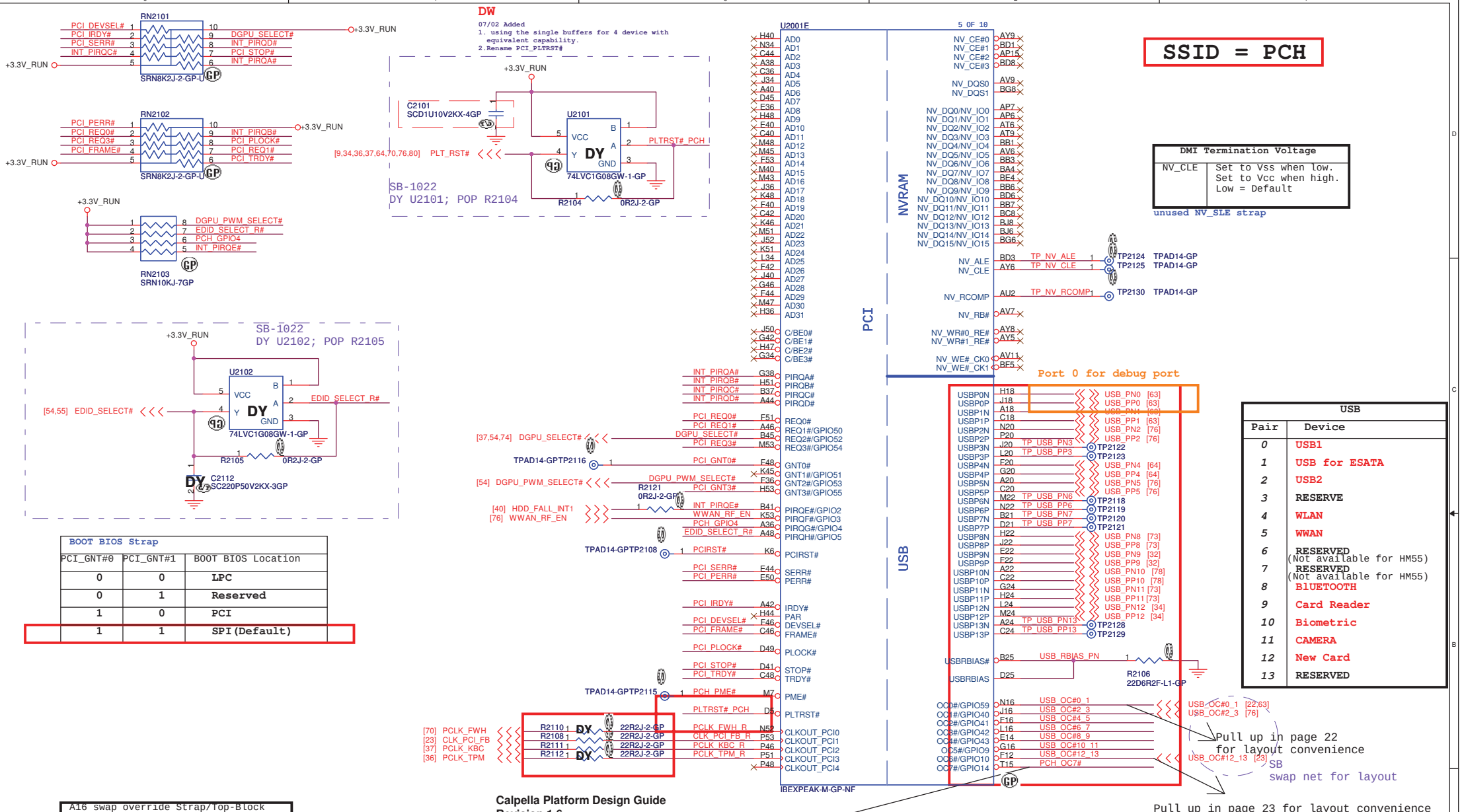
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

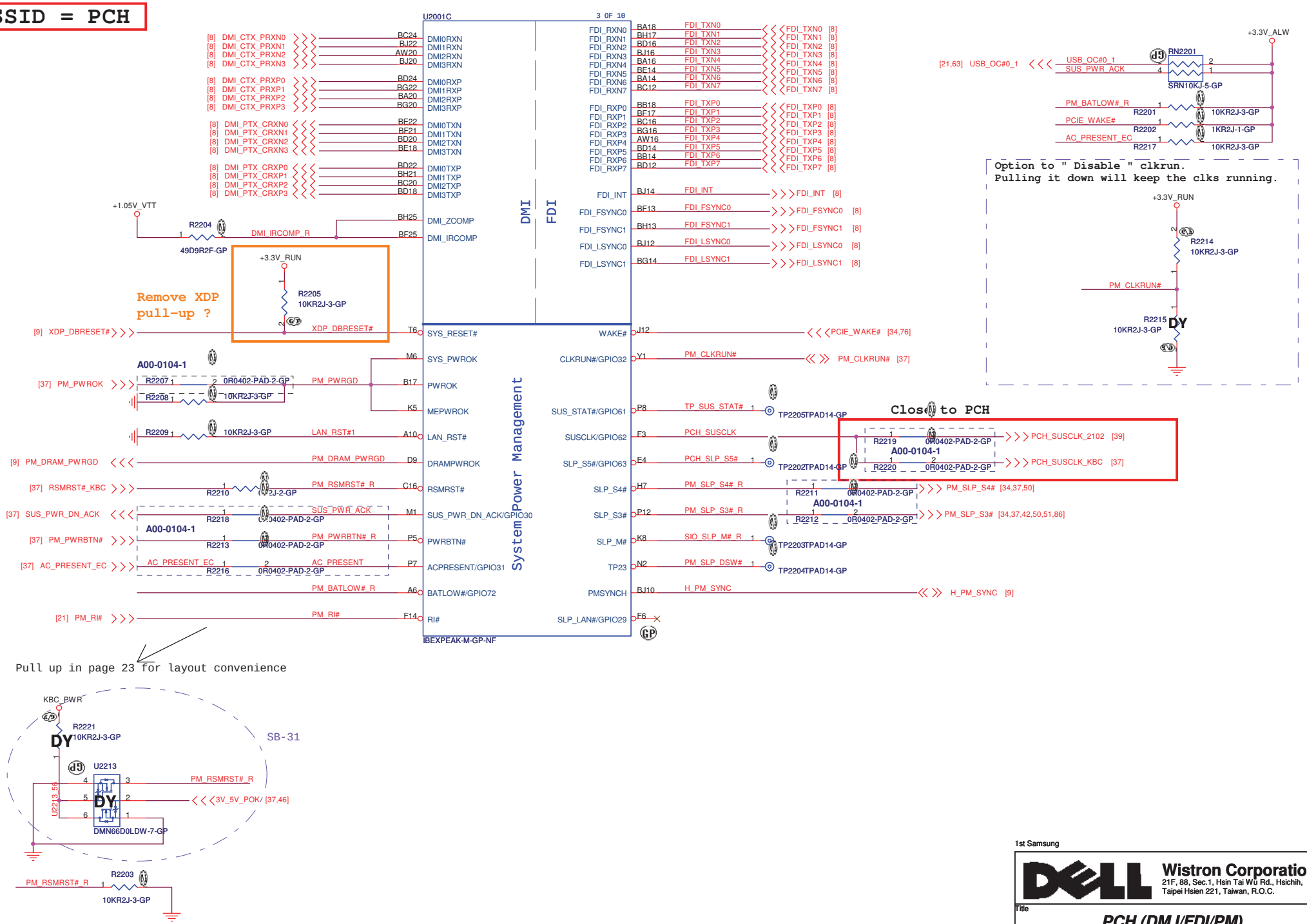
Title: **PCH (LVDS/CRT/DDI)**

Size | Document Number: **Winery13 MB DIS** | Rev: **A00**

Date: Wednesday, January 13, 2010 | Sheet 20 of 88


SSID = PCH
DW
07/02 Added
1. using the single buffers for 4 device with equivalent capability.
2.Rename PCI_PLTRST#
SB-1022
DY U2101; POP R2104
SB-1022
DY U2102; POP R2105
DMI Termination Voltage
NV_CLE
Set to Vss when low.
Set to Vcc when high.
Low = Default
unused NV_SLE strap
BOOT BIOS Strap
PCI_GNT#0
PCI_GNT#1
BOOT BIOS Location
0 0 LPC
0 1 Reserved
1 0 PCI
1 1 SPI(Default)
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT#3
Low = A16 swap override/Top-Block Swap Override enabled
High = Default
Port 0 for debug port
USB
Pair
Device
0 USB1
1 USB for ESATA
2 USB2
3 RESERVE
4 WLAN
5 WWAN
6 RESERVED (Not available for HM55)
7 RESERVED (Not available for HM55)
8 BlUETOOTH
9 Card Reader
10 Biometric
11 CAMERA
12 New Card
13 RESERVED
Pull up in page 22 for layout convenience
SB
swap net for layout
Pull up in page 23 for layout convenience
SB
swap net for layout
Calpella Platform Design Guide
Revision 1.6
Page 233
Table 111. Overcurrent Pin Example Configuration
These OC7# pins are not used for USB overcurrent protection and should be configured as GPIOs.
The unused USB ports can be left as no connect.
1st Samsung
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (PCI/USB/NVRAM)
Size
Document Number
Winery13 MB DIS
Rev
A00
Date: Wednesday, January 13, 2010
Sheet 21 of 88

SSID = PCH



1st Samsung

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Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (DM I/FDI/PM)	
Size	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 22 of 88	

SSID = PCH

U2001B — 2 OF 10 — IBEXPEAK-M-GP-NF

PCI-E* Controller Link

SMBus

PEG

From CLK BUFFER

Clock Flex

WLAN

LAN

WWAN

New Card

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN

Remove XDP pull-up

SB-1020

A00-0104-1

un-stuff 25M X'tal without HDMI/eDP/DP

Pull up in page 21 for layout convenience

SB-1020
move EDID_SELECT# from GPIO66 to GPIO5

SB
swap net for layout

SB-1026
swap net for layout

SB-1023
RN2308 change to 2*1 size

1ST: 84.03904.H11
2ND: 84.03904.L06

1ST: 84.DMN66.03F
2ND: 84.27002.F3F

1ST: 84.2N702.E31
2ND: 84.2N702.D31

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 23 of 88

SSID = PCH

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

1st: EPSON 82.30001.861
2nd: QUARTECH 82.30001.A81
3rd: KDS 82.30001.691

SB-18

DW
07/23 Added
1.Added "ME in Manufacturing Mode" strap
2.Added CardReader_Wake# to sent Card detect signal for PCH . (Only For JMB380)

Flash Descriptor Security Override/ ME Debug Mode	
ME_UNLOCK#	This strap should only be asserted low via external pull down in manufacturing/debug environments ONLY.

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

SB-1026
1. remove R2411 pull high INT_SERIRQ to RN2501.1

DW
07/02 Change
1.Change R2410 to dummy

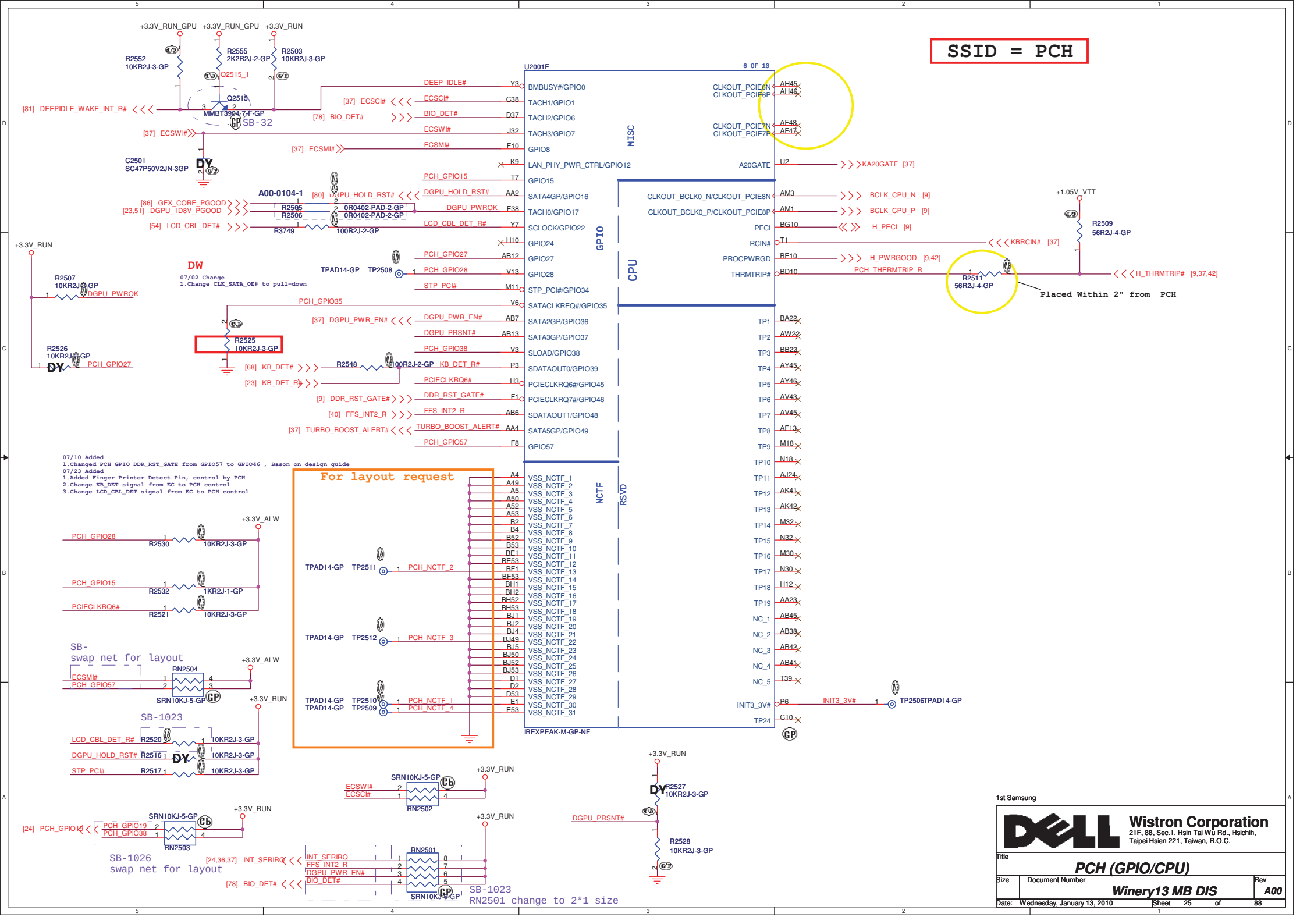
SC-1208-1
change R2413,R2414,R2415 from 15ohm to 0 ohm

DW
07/10 assign GPIO
1.assign GPIO GPIO_DSM,Felic_DETECT#

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: Document Number: Winery13 MB DIS Rev: A00
Date: Wednesday, January 13, 2010 Sheet 24 of 88


SSID = PCH
U2001F
6 OF 10
BMBUSY#/GPIO0
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
SATA4GP/GPIO16
TACH0/GPIO17
SCLOCK/GPIO22
GPIO24
GPIO27
GPIO28
STP_PCI#/GPIO34
SATACLKREQ#/GPIO35
SATA2GP/GPIO36
SATA3GP/GPIO37
SLOAD/GPIO38
SDATAOUT0/GPIO39
PCIECLKRQ6#/GPIO45
PCIECLKRQ7#/GPIO46
SDATAOUT1/GPIO48
SATA5GP/GPIO49
GPIO57
MISC
GPIO
CPU
NCTF
RSVD
CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
A20GATE
CLKOUT_BCLK0_N/CLKOUT_PCIE8N
CLKOUT_BCLK0_P/CLKOUT_PCIE8P
PECI
RCIN#
PROCPWRGD
THRMTRIP#
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TP17
TP18
TP19
NC_1
NC_2
NC_3
NC_4
NC_5
INIT3_3V#
TP24
IBEXPEAK-M-GP-NF
DEEP_IDLE#
ECSCI#
BIO_DET#
ECSWI#
ECSMI#
PCH_GPIO15
DGPU_HOLD_RST#
DGPU_PWROK
LCD_CBL_DET_R#
PCH_GPIO27
PCH_GPIO28
STP_PCI#
PCH_GPIO35
DGPU_PWR_EN#
DGPU_PRSNT#
PCH_GPIO38
KB_DET_R#
PCIECLKRQ6#
DDR_RST_GATE#
FFS_INT2_R
TURBO_BOOST_ALERT#
PCH_GPIO57
BCLK_CPU_N [9]
BCLK_CPU_P [9]
H_PECI [9]
KBRCIN# [37]
H_PWRGOOD [9,42]
PCH_THERMTRIP_R
H_THRMTRIP# [9,37,42]
KA20GATE [37]
Placed Within 2" from PCH
+1.05V_VTT
+3.3V_RUN
+3.3V_RUN_GPU
+3.3V_ALW
R2552 10KR2J-3-GP
R2555 2K2R2J-2-GP
R2503 10KR2J-3-GP
Q2515_1
Q2515
MMBT3904-7-F-GP
SB-32
C2501 SC47P50V2JN-3GP
A00-0104-1
R2505 0R0402-PAD-2-GP
R2506 0R0402-PAD-2-GP
R3749 100R2J-2-GP
R2507 10KR2J-GP
R2526 10KR2J-GP
R2525 10KR2J-3-GP
R2548 100R2J-2-GP
R2509 56R2J-4-GP
R2511 56R2J-4-GP
TPAD14-GP TP2508
DW
07/02 Change
1.Change CLK_SATA_OE# to pull-down
07/10 Added
1.Changed PCH GPIO DDR_RST_GATE from GPIO57 to GPIO46 , Bason on design guide
07/23 Added
1.Added Finger Printer Detect Pin, control by PCH
2.Change KB_DET signal from EC to PCH control
3.Change LCD_CBL_DET signal from EC to PCH control
For layout request
TPAD14-GP TP2511 PCH_NCTF_2
TPAD14-GP TP2512 PCH_NCTF_3
TPAD14-GP TP2510 PCH_NCTF_1
TPAD14-GP TP2509 PCH_NCTF_4
R2530 10KR2J-3-GP
R2532 1KR2J-1-GP
R2521 10KR2J-3-GP
SB-swap net for layout
RN2504 SRN10KJ-5-GP
SB-1023
R2520 10KR2J-3-GP
R2516 10KR2J-3-GP
R2517 10KR2J-3-GP
RN2502 SRN10KJ-5-GP
R2527 10KR2J-3-GP
R2528 10KR2J-3-GP
RN2503 SRN10KJ-5-GP
SB-1026 swap net for layout
RN2501 SRN10KJ-5-GP
SB-1023 RN2501 change to 2*1 size
INT_SERIRQ
FFS_INT2_R
DGPU_PWR_EN#
BIO_DET#
1st Samsung
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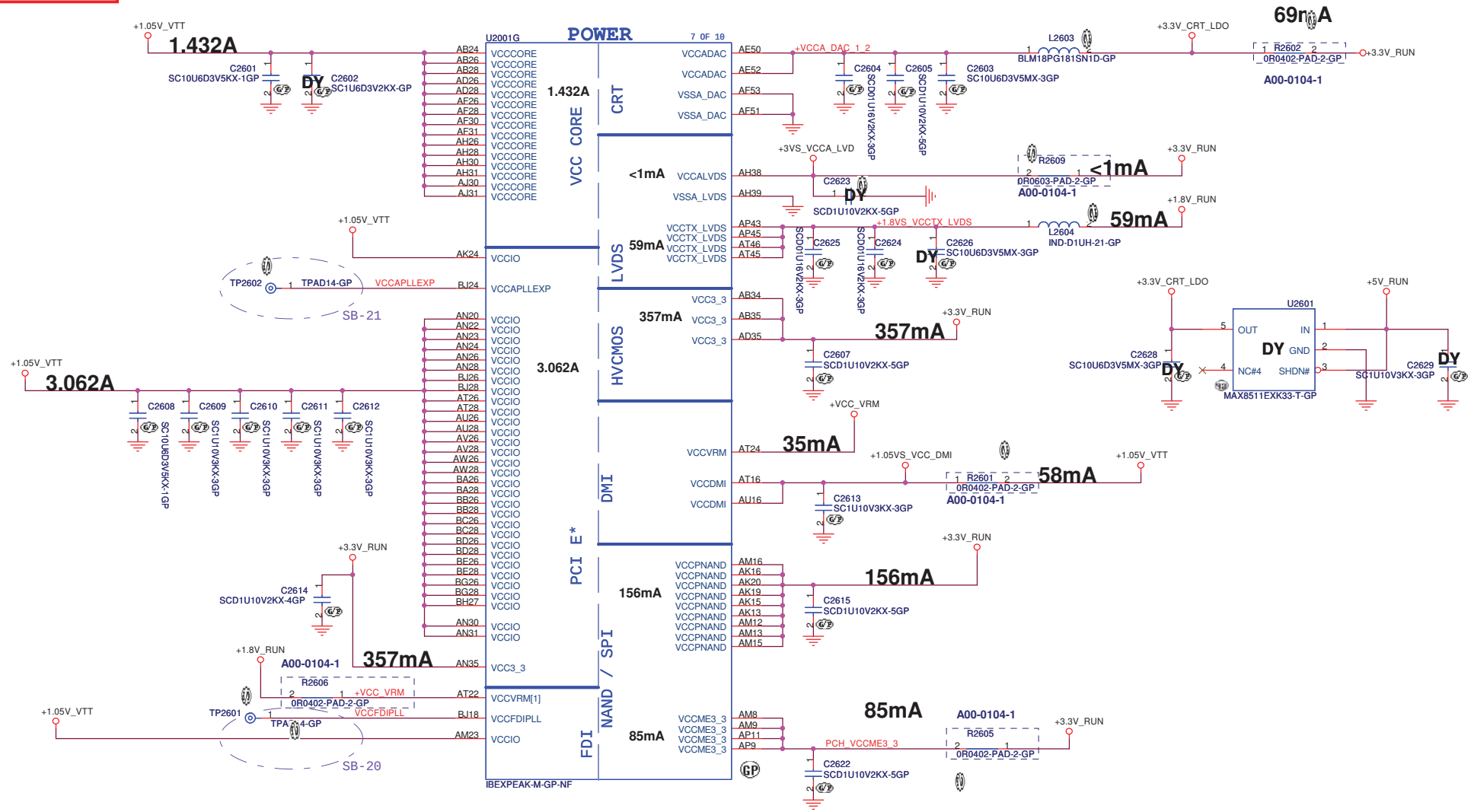
Title
PCH (GPIO/CPU)
Size
Document Number
Winery13 MB DIS
Rev
A00
Date: Wednesday, January 13, 2010
Sheet 25 of 88

SSID = PCH



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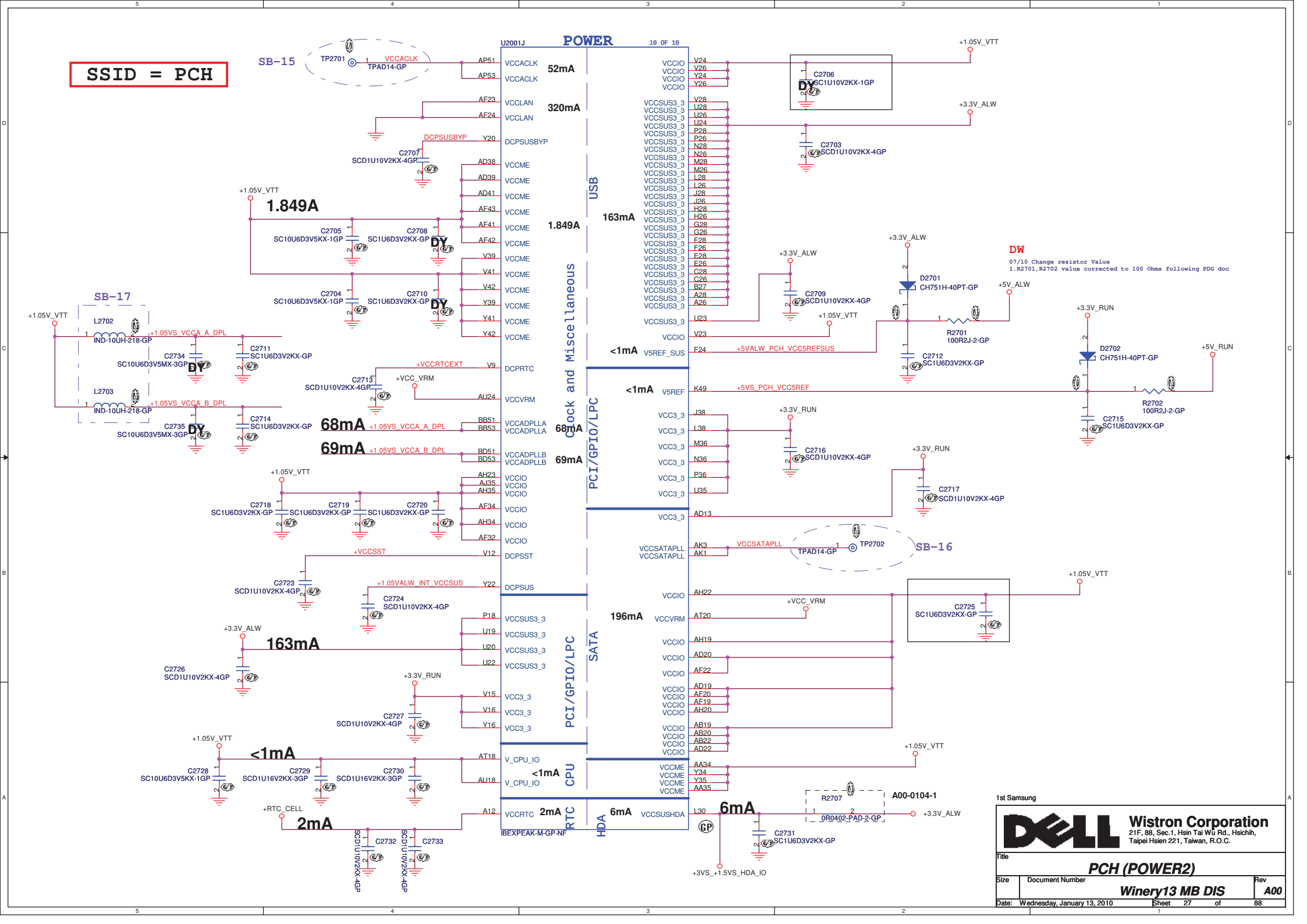
Title		
PCH (POWER1)		
Size	Document Number	Rev
	Winery13 MB DIS	A00
Date: Wednesday, January 13, 2010	Sheet 26 of 88	


SSID = PCH
POWER
U2001J
10 OF 10
SB-15
TP2701
VCCACLK
TPAD14-GP
SB-17
SB-16
TP2702
VCCSATAPLL
DW
07/10 Change resistor Value
1.R2701,R2702 value corrected to 100 Ohms following PDG doc
1.849A
68mA
69mA
163mA
196mA
<1mA
2mA
6mA
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IBEXPEAK-M-GP-NF
+1.05V_VTT
+3.3V_ALW
+3.3V_RUN
+5V_ALW
+5V_RUN
+VCC_VRM
+VCCSST
+VCCRTCEXT
+RTC_CELL
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+1.05VALW_INT_VCCSUS
+5VALW_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
+3VS_+1.5VS_HDA_IO
DCPSUSBYP
DCPRTC
DCPSST
DCPSUS
V_CPU_IO
VCCRTC
VCCSUSHDA
VCCACLK
VCCLAN
VCCME
VCCVRM
VCCIO
VCCSUS3_3
VCC3_3
V5REF_SUS
V5REF
VCCADPLLA
VCCADPLLB
VCCSATAPLL
R2707
0R0402-PAD-2-GP
A00-0104-1
1st Samsung
Wistron Corporation
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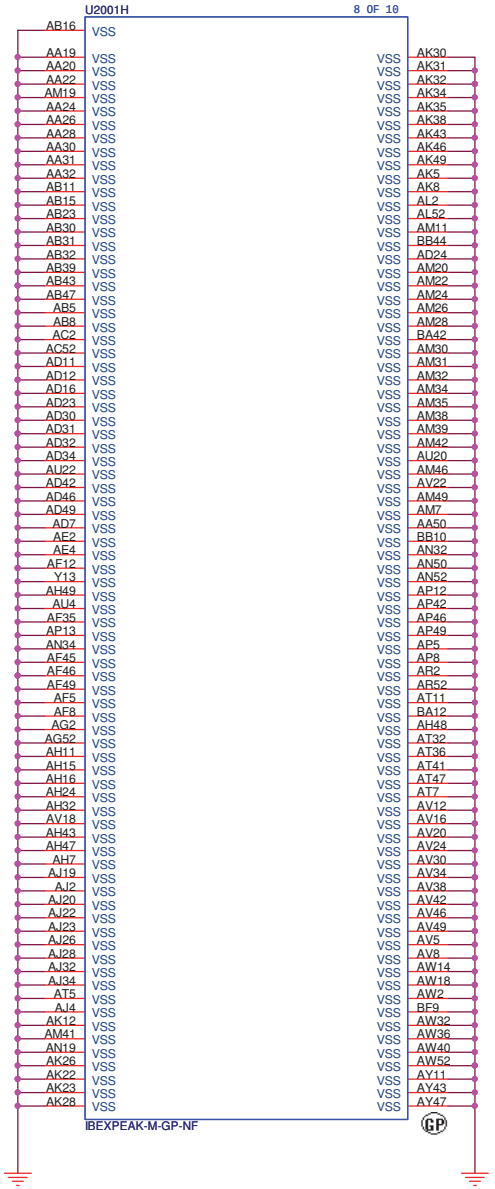
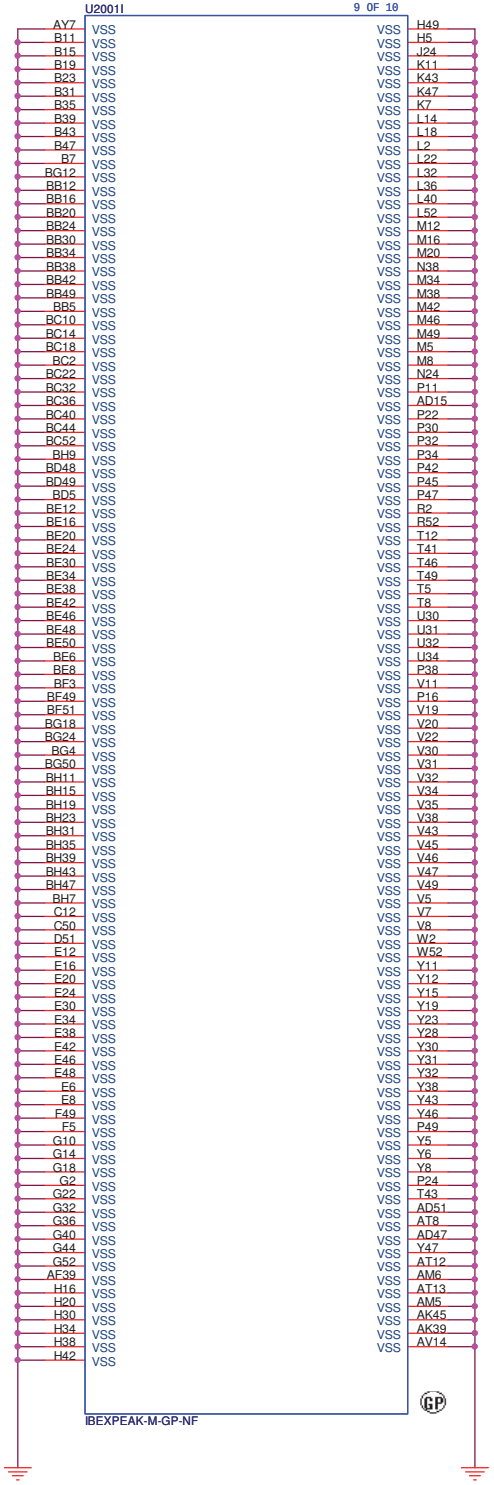
Title
PCH (POWER2)
Size
Document Number
Winery13 MB DIS
Rev
A00
Date: Wednesday, January 13, 2010
Sheet 27 of 88

SSID = PCH





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Title	PCH (VSS)	
Size	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 28 of 88	

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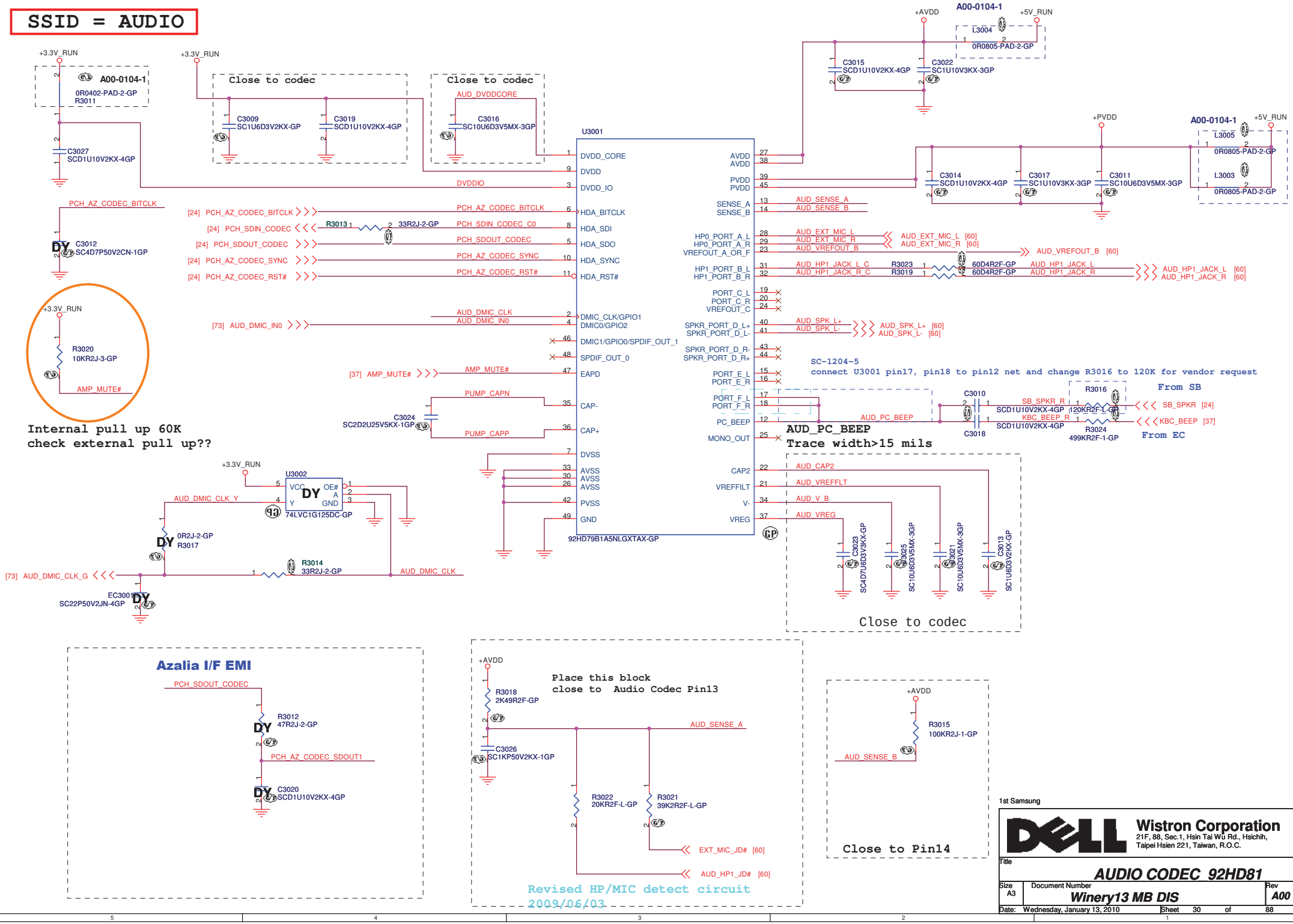
Title

(Reserve)

Size	Document Number	Rev
Custom	*Winery13 MB DIS*	*A00*

Date:	Wednesday, January 13, 2010	Sheet	29	of	88

SSID = AUDIO


+3.3V_RUN
A00-0104-1
0R0402-PAD-2-GP
R3011
C3027
SCD1U10V2KX-4GP
Close to codec
C3009
SC1U6D3V2KX-GP
C3019
SCD1U10V2KX-4GP
Close to codec
AUD_DVDDCORE
C3016
SC10U6D3V5MX-3GP
U3001
DVDD_CORE
DVDD
DVDD_IO
DVDDIO
PCH_AZ_CODEC_BITCLK
C3012
SC4D7P50V2CN-1GP
[24] PCH_AZ_CODEC_BITCLK
[24] PCH_SDIN_CODEC
[24] PCH_SDOUT_CODEC
[24] PCH_AZ_CODEC_SYNC
[24] PCH_AZ_CODEC_RST#
R3013
33R2J-2-GP
PCH_AZ_CODEC_BITCLK
PCH_SDIN_CODEC_C0
PCH_SDOUT_CODEC
PCH_AZ_CODEC_SYNC
PCH_AZ_CODEC_RST#
HDA_BITCLK
HDA_SDI
HDA_SDO
HDA_SYNC
HDA_RST#
R3020
10KR2J-3-GP
AMP_MUTE#
Internal pull up 60K
check external pull up??
[73] AUD_DMIC_IN0
AUD_DMIC_CLK
AUD_DMIC_IN0
DMIC_CLK/GPIO1
DMIC0/GPIO2
DMIC1/GPIO0/SPDIF_OUT_1
SPDIF_OUT_0
[37] AMP_MUTE#
AMP_MUTE#
EAPD
PUMP_CAPN
PUMP_CAPP
C3024
SC2D2U25V5KX-1GP
CAP-
CAP+
DVSS
AVSS
AVSS
AVSS
PVSS
GND
92HD79B1A5NLGXTAX-GP
+3.3V_RUN
U3002
74LVC1G125DC-GP
AUD_DMIC_CLK_Y
R3017
0R2J-2-GP
[73] AUD_DMIC_CLK_G
R3014
33R2J-2-GP
AUD_DMIC_CLK
EC3001
SC22P50V2JN-4GP
+AVDD
A00-0104-1
L3004
0R0805-PAD-2-GP
C3015
SCD1U10V2KX-4GP
C3022
SC1U10V3KX-3GP
+PVDD
+5V_RUN
L3005
0R0805-PAD-2-GP
L3003
0R0805-PAD-2-GP
C3014
SCD1U10V2KX-4GP
C3017
SC1U10V3KX-3GP
C3011
SC10U6D3V5MX-3GP
AVDD
AVDD
PVDD
PVDD
SENSE_A
SENSE_B
AUD_SENSE_A
AUD_SENSE_B
HP0_PORT_A_L
HP0_PORT_A_R
VREFOUT_A_OR_F
AUD_EXT_MIC_L
AUD_EXT_MIC_R
AUD_VREFOUT_B
AUD_EXT_MIC_L [60]
AUD_EXT_MIC_R [60]
AUD_VREFOUT_B [60]
HP1_PORT_B_L
HP1_PORT_B_R
AUD_HP1_JACK_L_C
AUD_HP1_JACK_R_C
R3023
R3019
60D4R2F-GP
AUD_HP1_JACK_L
AUD_HP1_JACK_R
AUD_HP1_JACK_L [60]
AUD_HP1_JACK_R [60]
PORT_C_L
PORT_C_R
VREFOUT_C
SPKR_PORT_D_L+
SPKR_PORT_D_L-
AUD_SPK_L+
AUD_SPK_L-
AUD_SPK_L+ [60]
AUD_SPK_L- [60]
SPKR_PORT_D_R-
SPKR_PORT_D_R+
PORT_E_L
PORT_E_R
PORT_F_L
PORT_F_R
PC_BEEP
MONO_OUT
AUD_PC_BEEP
SC-1204-5
connect U3001 pin17, pin18 to pin12 net and change R3016 to 120K for vendor request
C3010
C3018
SCD1U10V2KX-4GP
SB_SPKR_R
KBC_BEEP_R
R3016
120KR2F-L-GP
R3024
499KR2F-1-GP
From SB
From EC
SB_SPKR [24]
KBC_BEEP [37]
AUD_PC_BEEP
Trace width>15 mils
CAP2
VREFFILT
V-
VREG
AUD_CAP2
AUD_VREFFLT
AUD_V_B
AUD_VREG
C3023
SC4D7U6D3V9KX-GP
C3025
SC10U6D3V5MX-3GP
C3021
SC10U6D3V5MX-3GP
C3013
SC1U6D3V2KX-GP
Close to codec
Azalia I/F EMI
PCH_SDOUT_CODEC
R3012
47R2J-2-GP
PCH_AZ_CODEC_SDOUT1
C3020
SCD1U10V2KX-4GP
+AVDD
Place this block
close to Audio Codec Pin13
R3018
2K49R2F-GP
AUD_SENSE_A
C3026
SC1KP50V2KX-1GP
R3022
20KR2F-L-GP
R3021
39K2R2F-L-GP
EXT_MIC_JD# [60]
AUD_HP1_JD# [60]
Revised HP/MIC detect circuit
2009/06/03
+AVDD
R3015
100KR2J-1-GP
AUD_SENSE_B
Close to Pin14
1st Samsung
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC 92HD81
Size A3
Document Number
Winery13 MB DIS
Rev A00
Date: Wednesday, January 13, 2010
Sheet 30 of 88

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1st Samsung

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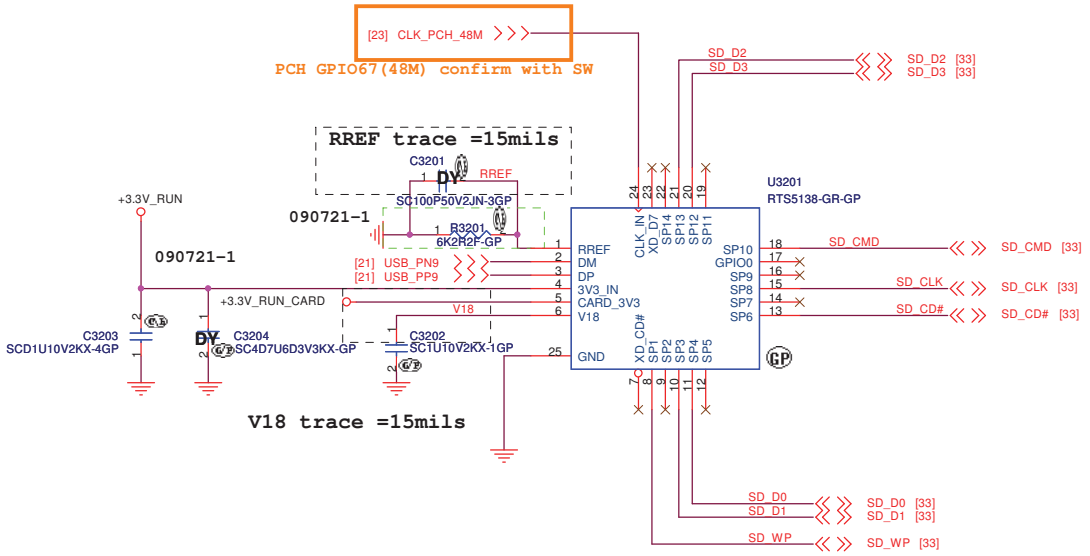
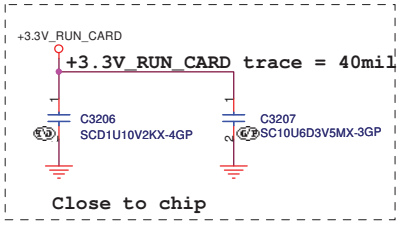
Title: *(Reserve)*

Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

Date: Wednesday, January 13, 2010 | Sheet 31 of 88

SSID = SDIO





1st Samsung

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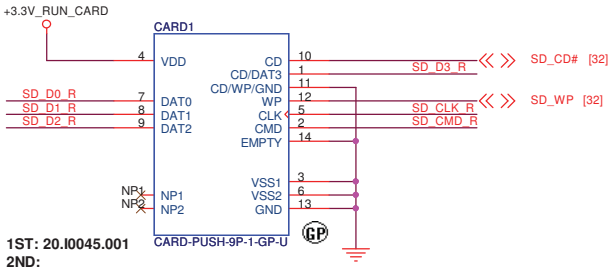
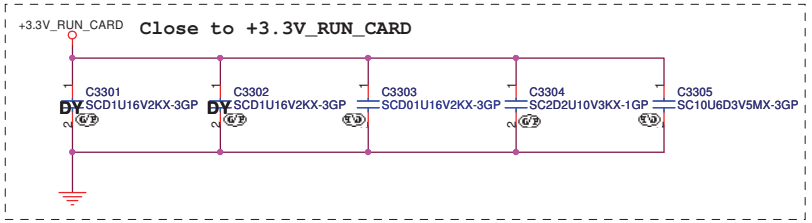
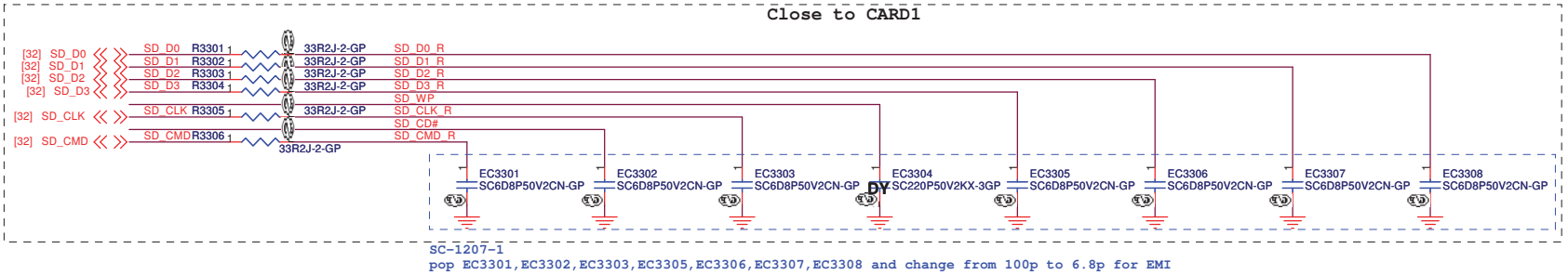
Title	CardReader/RTS5138	
Size: Custom	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 32 of 88	

SSID = SDIO

SD/MMC/MMC+ Card Reader







SSID = 1394

Remove 1394

1st Samsung

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Taipei Hsien 221, Taiwan, R.O.C.

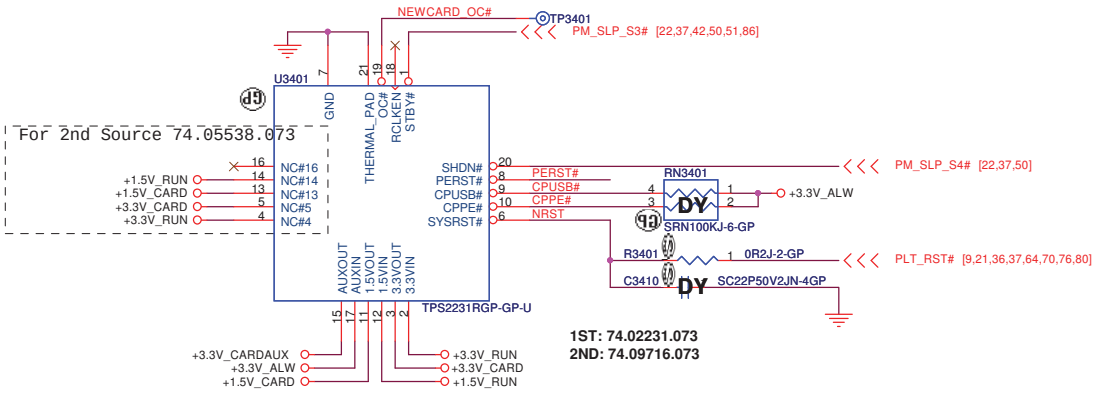
Title: CARD READER CONN

Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 33 of 88

SSID = ExpressCard

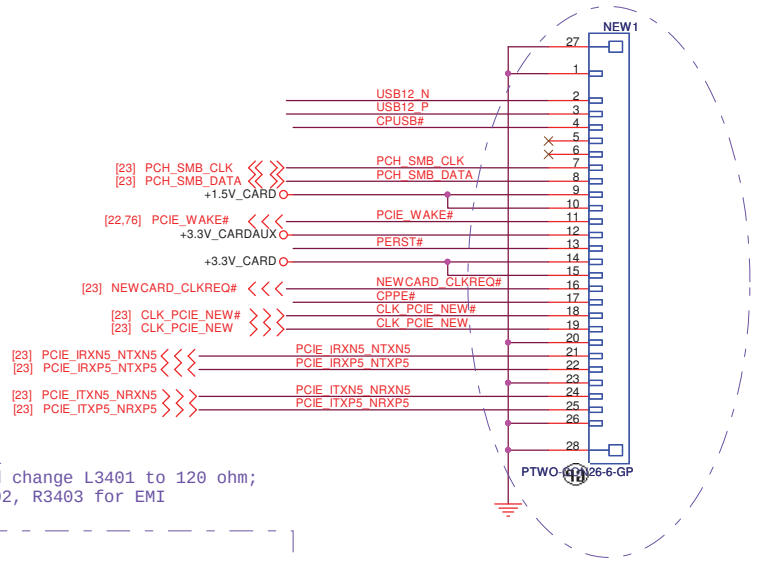
+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA



1ST: 74.02231.073
2ND: 74.09716.073

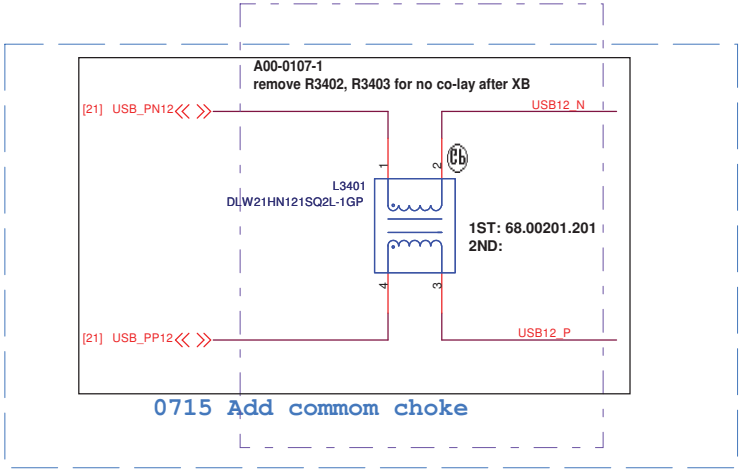
+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

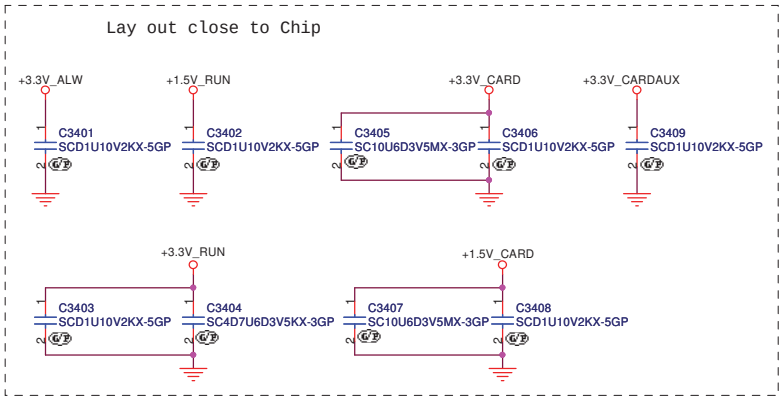
SB-26



1ST: 20.K0370.026
2ND: 20.K0315.026

SB-1021
pop and change L3401 to 120 ohm;
DY R3402, R3403 for EMI





1st Samsung

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Title: ExpressCard
Size: A3
Document Number: Winery13 MB DIS
Rev: A00
Date: Wednesday, January 13, 2010
Sheet 34 of 88

(Blank)

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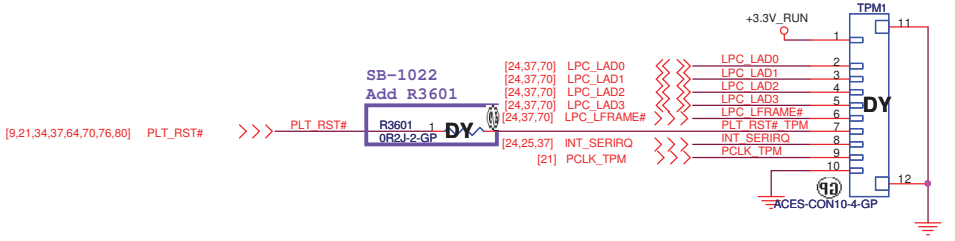
Title: *(Reserve)*

Size: A3 | Document Number: *Winery13 MB DIS* | Rev: *A00*

Date: Wednesday, January 13, 2010 | Sheet 35 of 88

SSID = User.Interface

TPM board CONN



SC-1125-1
remove TPM AFTP

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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPM		
Size: Custom	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 36 of 88	

SSID = KBC

Put 0.1uf close to VCC-GND pin pair.

Pull High : Discrete
internal Pull Low for UMA

Remove
HDD_FALL_INT1

Pull High : Switch Board
Pull Low : UnSwitch Board

C3710 need place near pin 44.

SC-1118-1
change power rail to KBC_PWR

SC-1125-2
add U3703 mux for panel backlight enable signal select

SB-1020

SB-22

SB-34

MB VERSION

ID	VER1	VER0
SA	0	0
SB	0	1
SC	1	0
-1	1	1

KBC CLK EMI

WD
07/23
1. Added R3712 100 Ohm damping resistor
2. Added R3713 100 Ohm damping resistor
3. Added R3751 100 Ohm damping resistor

DW
07/10 Added
1.Added circuit ,
For prevent electric leakage

DW
07/10 assign GPIO
1.assign GPIO TUCPANEL_STP#

DW
07/07 Dummy
1.Dummy R3736

DW
07/07 Change
1.Change Power rail

1ST: 68.00084.881
2ND:

1ST: 84.03904.H11
2ND: 84.03904.L06

1ST: 84.03904.P11
2ND: 84.03904.T11

1ST: 84.03906.H11
2ND: 84.03906.R11

1ST: 73.03157.C0H
2ND: 73.03157.E0J

1ST: 83.01621.01F
2ND:

A00-0105-1
Add reset IC U3704 to prevent SPI ROM data lost

1st Samsung

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC Nuvoton NPCE781BA0DX**

Size: Custom | Document Number: **Winery13 MB DIS** | Rev: **A00**

Date: Wednesday, January 13, 2010 | Sheet 37 of 88

(Blank)

1st Samsung

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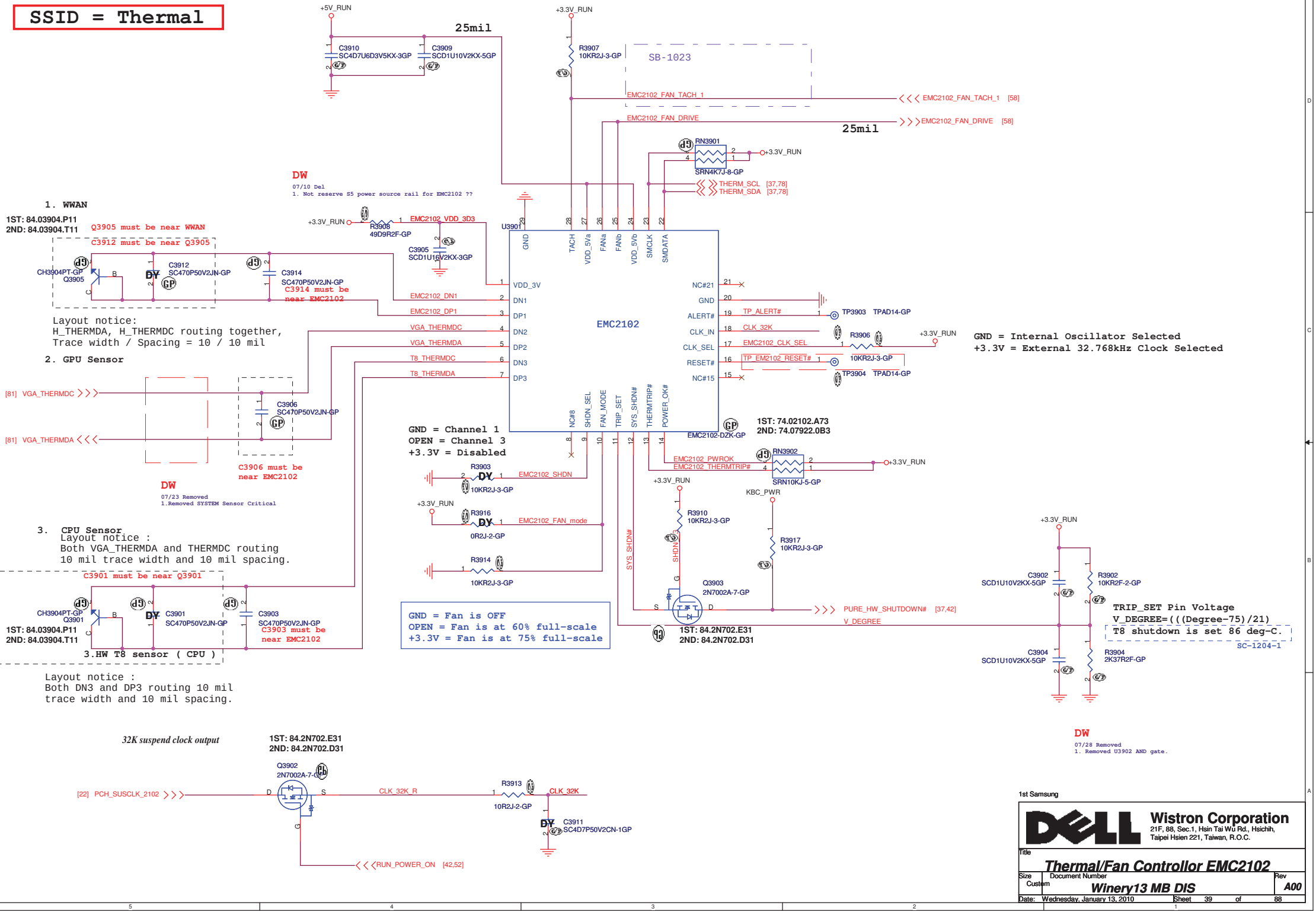
Title: *(Reserve)*

Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

Date: Wednesday, January 13, 2010 | Sheet 38 of 88

SSID = Thermal



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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

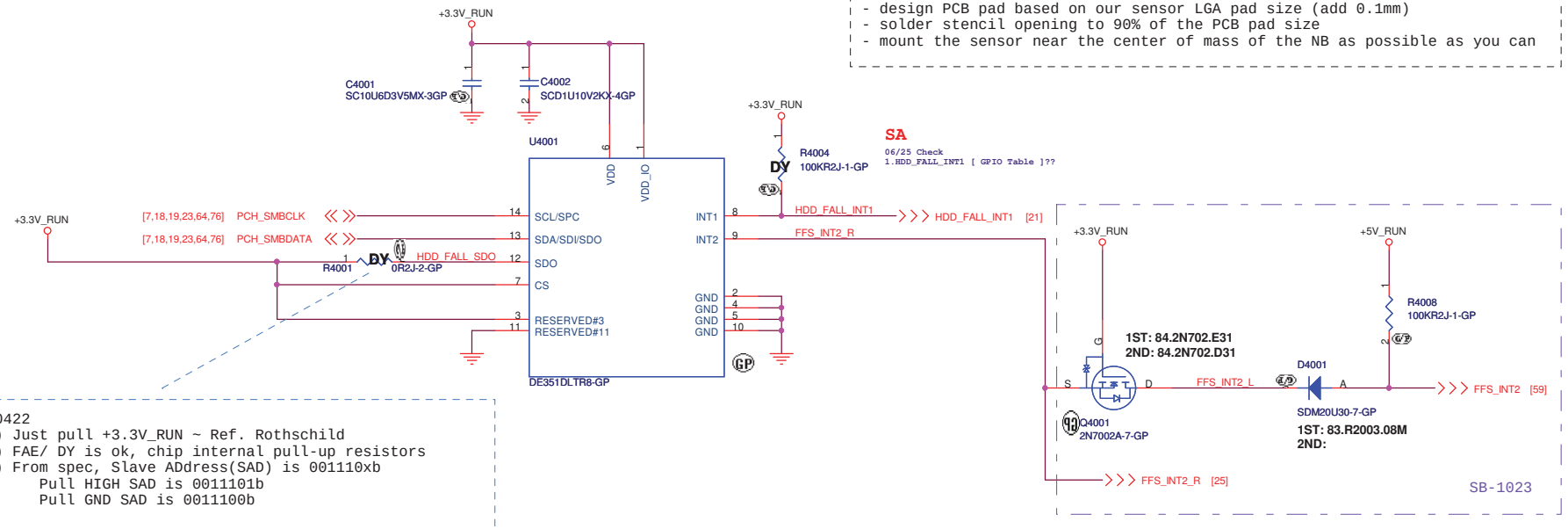
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 39 of 88

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave ADdress(SAD) is 001110xb
Pull HIGH SAD is 0011101b
Pull GND SAD is 0011100b

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

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Title	Free Fall Sensor	
Size: Custom	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 40 of 88	

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Taipei Hsien 221, Taiwan, R.O.C.

Title

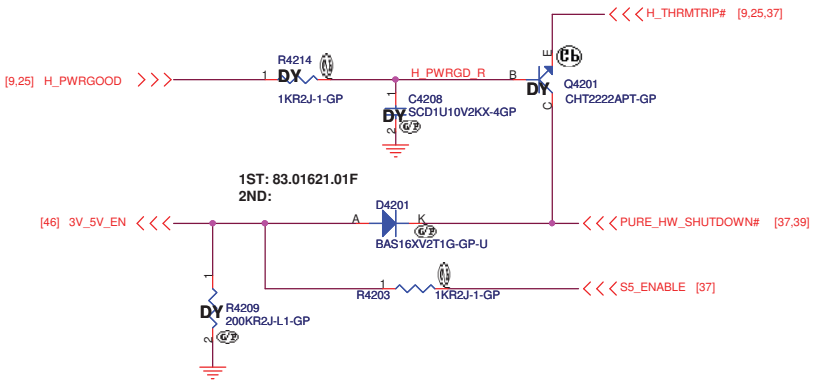
(Reserve)

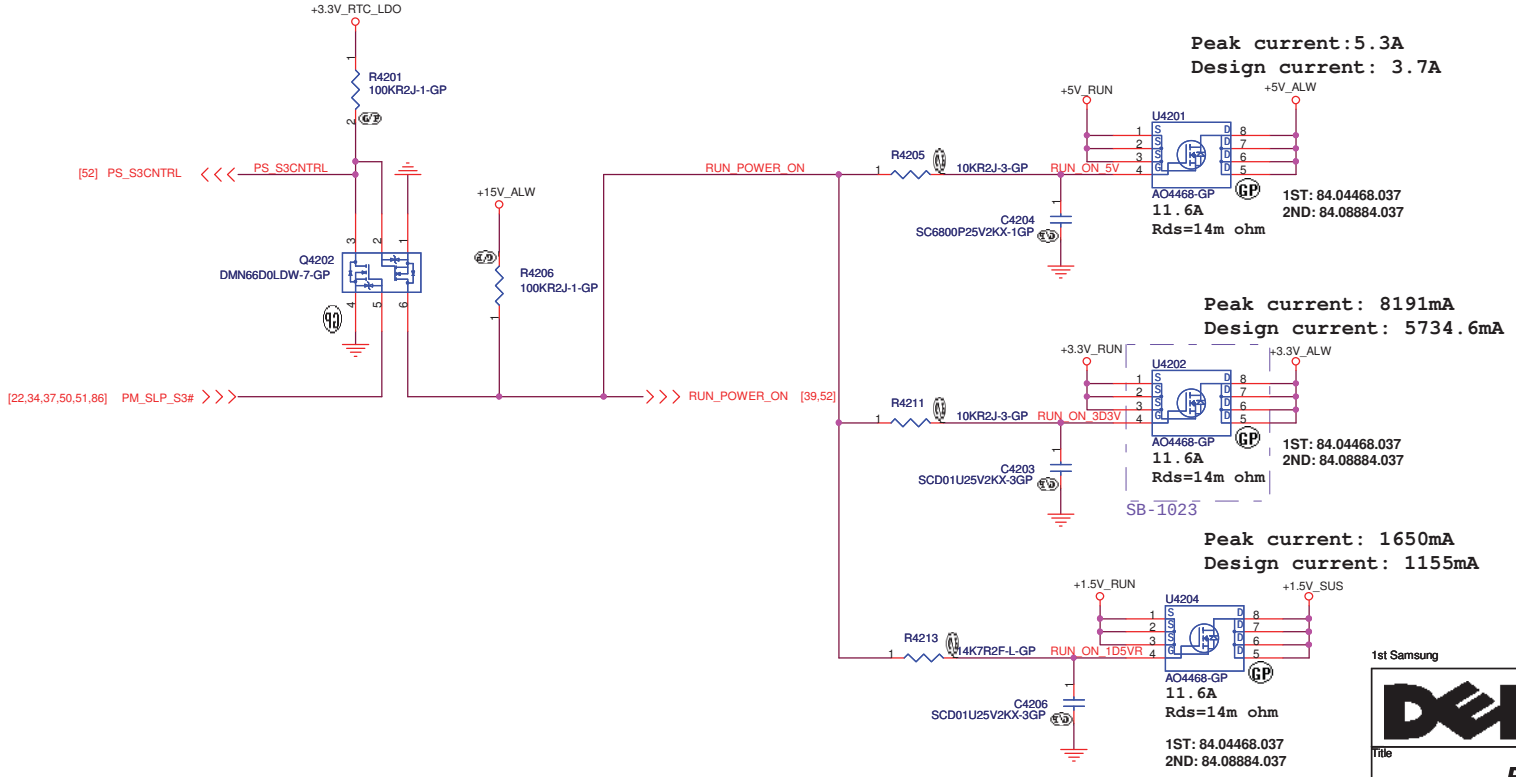
Size	Document Number	Rev
Custom	*Winery13 MB DIS*	*A00*

Date:	Wednesday, January 13, 2010	Sheet	41	of	88

SSID = Reset.Suspend

Remove +3.3V_DELAY power rail 2009/05/25





1st Samsung

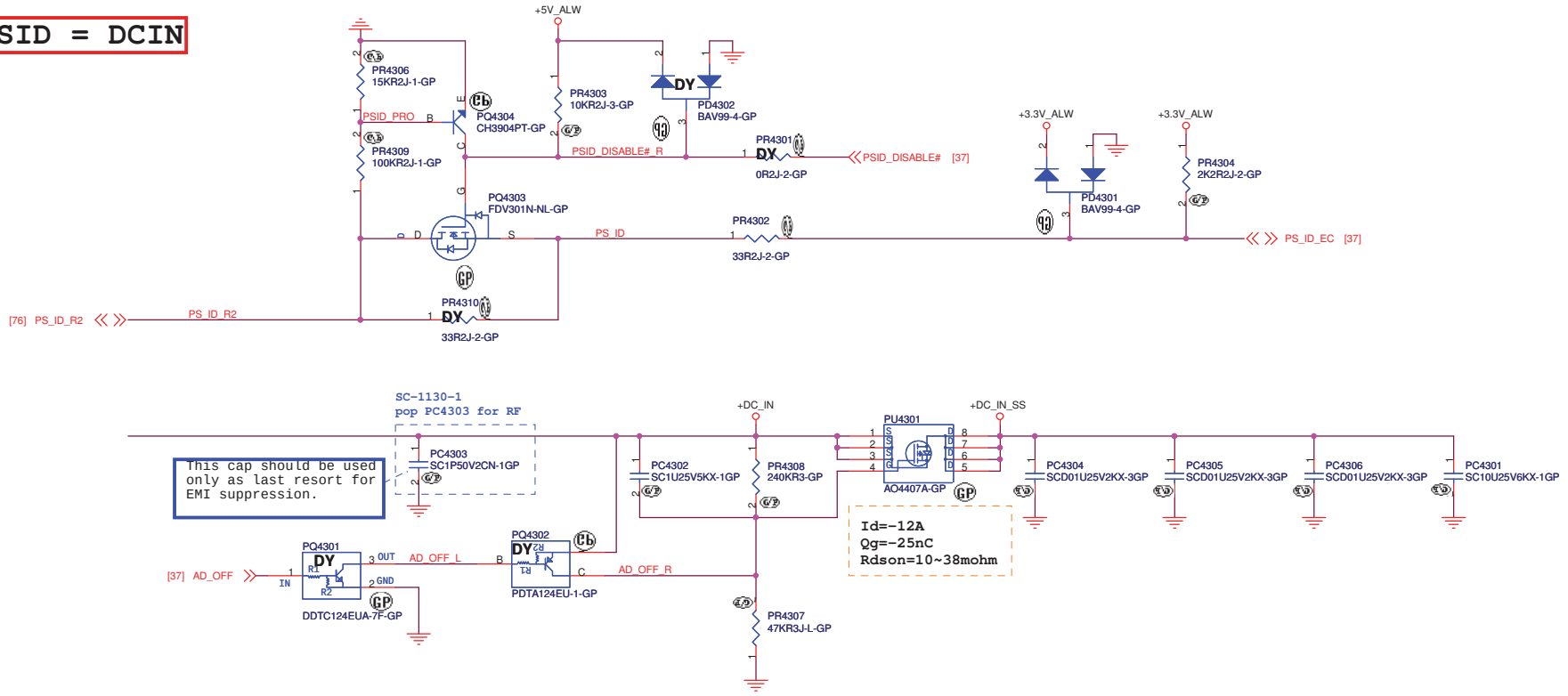
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 42 of 88

SSID = DCIN



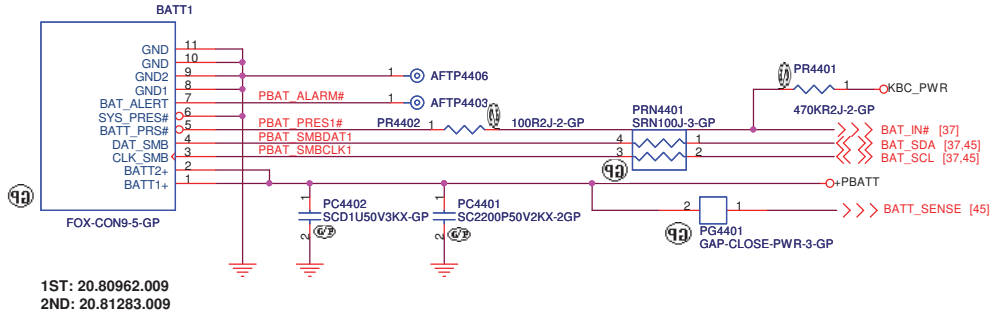
1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

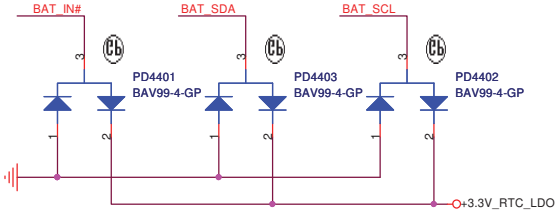
Title	DCIN	
Size: Custom	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 43 of 88	

SSID = BATT

Batt Connecter



1ST: 20.80962.009
2ND: 20.81283.009

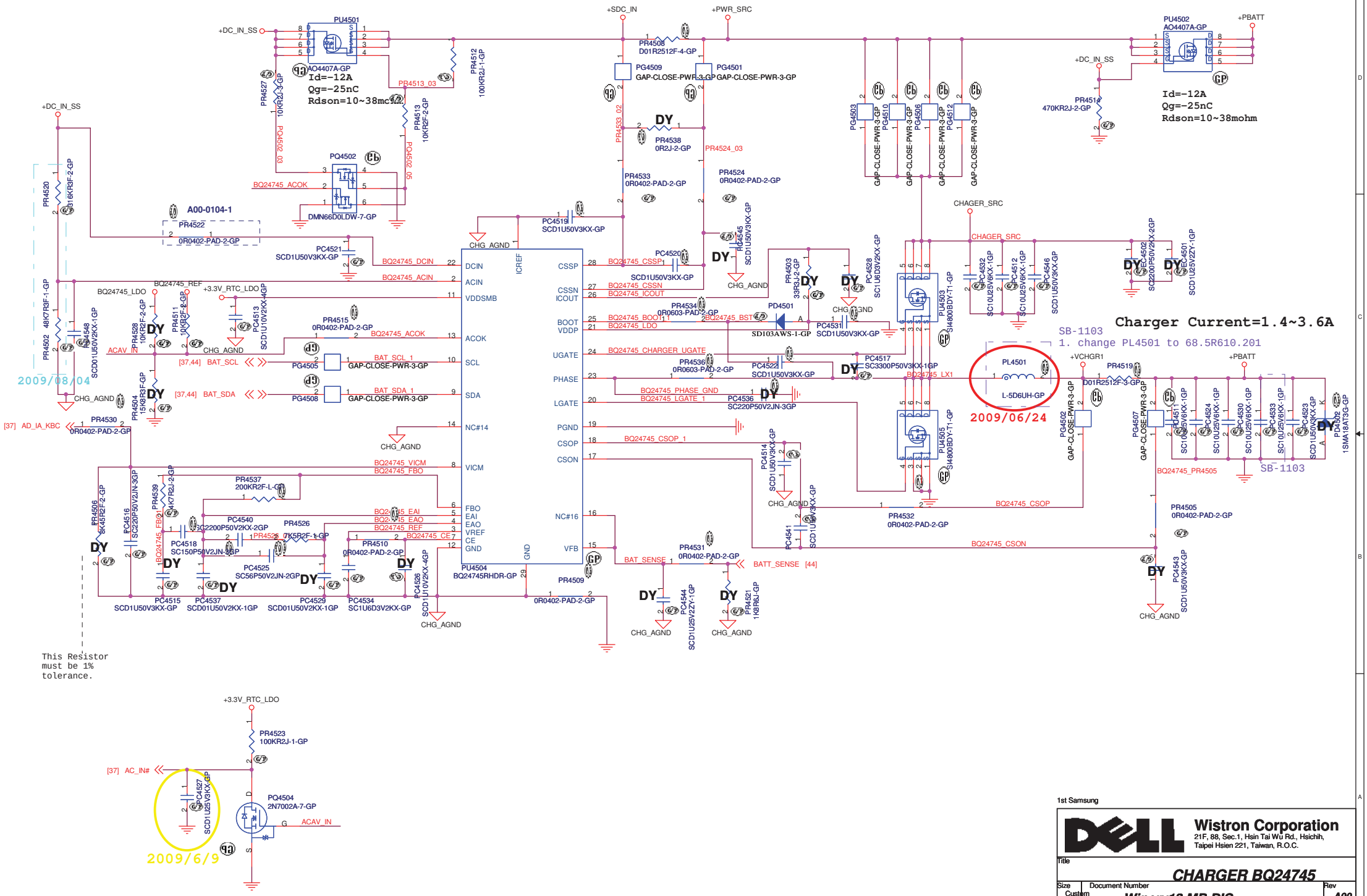


1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Batt Connecter	
Size A3	Document Number Winery13 MB DIS	Rev A00
Date: Wednesday, January 13, 2010	Sheet 44 of 88	

SSID = Charger



1st Samsung

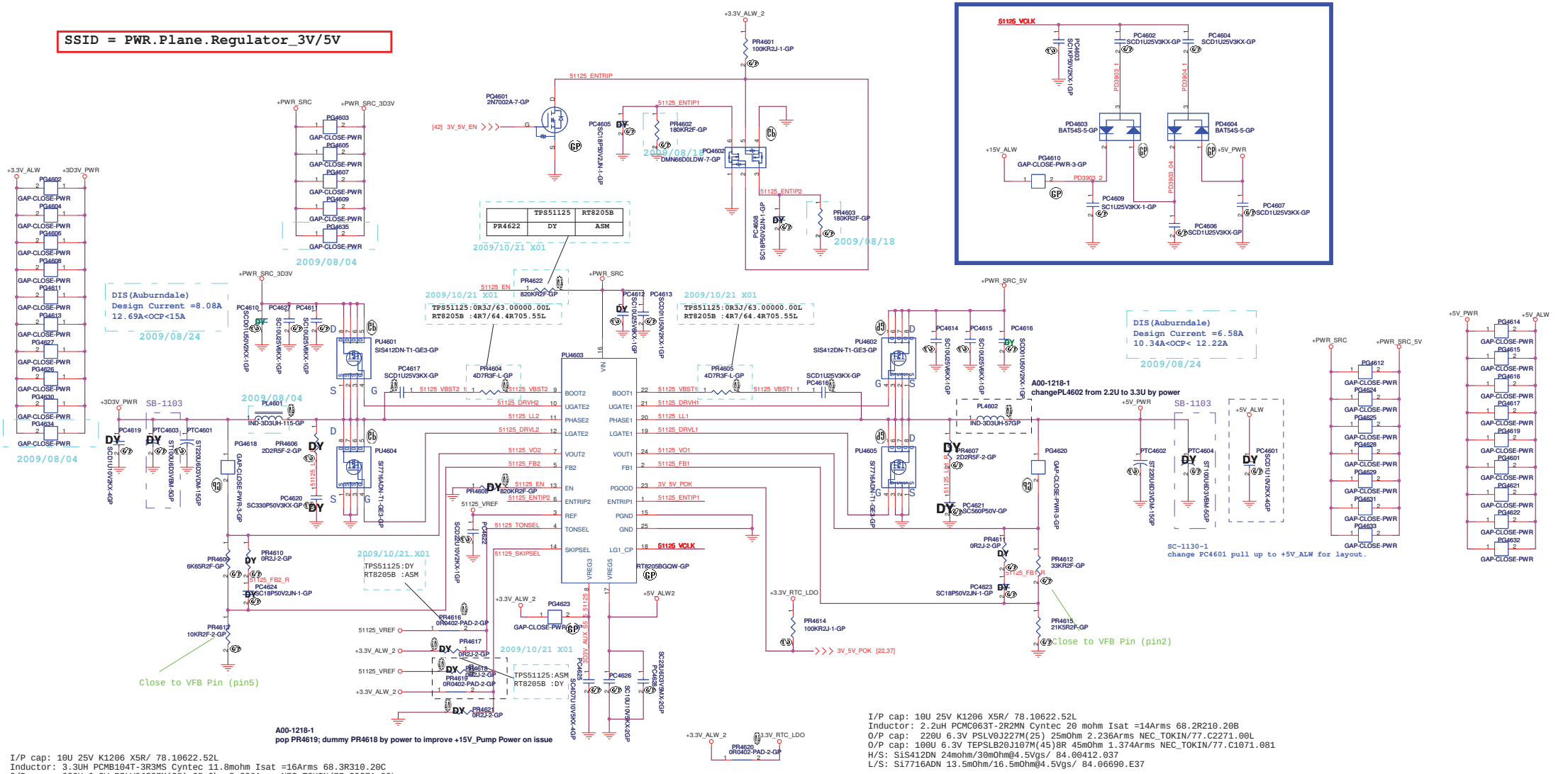
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER BQ24745**

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 45 of 88

SSID = PWR.Plane.Regulator_3V/5V



A00-1218-1
pop PR4619; dummy PR4618 by power to improve +15V_Pump Power on issue

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cyntec 11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: SiS412DN 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: Si7716ADN 13.5mOhm/16.5mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 20 mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: SiS412DN 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: Si7716ADN 13.5mOhm/16.5mOhm@4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

1st Samsung

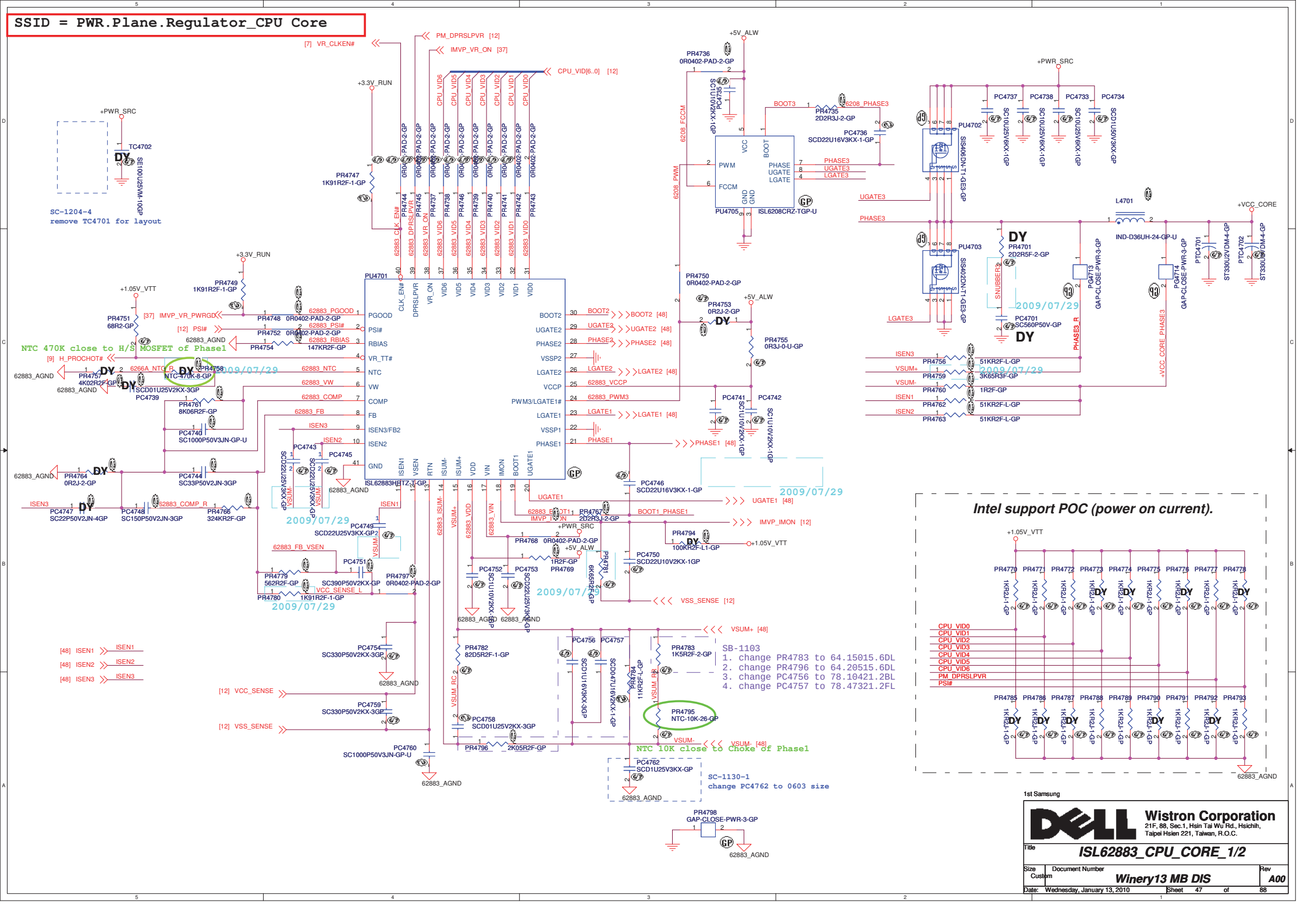
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8205B_5V/3D3V

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 46 of 88

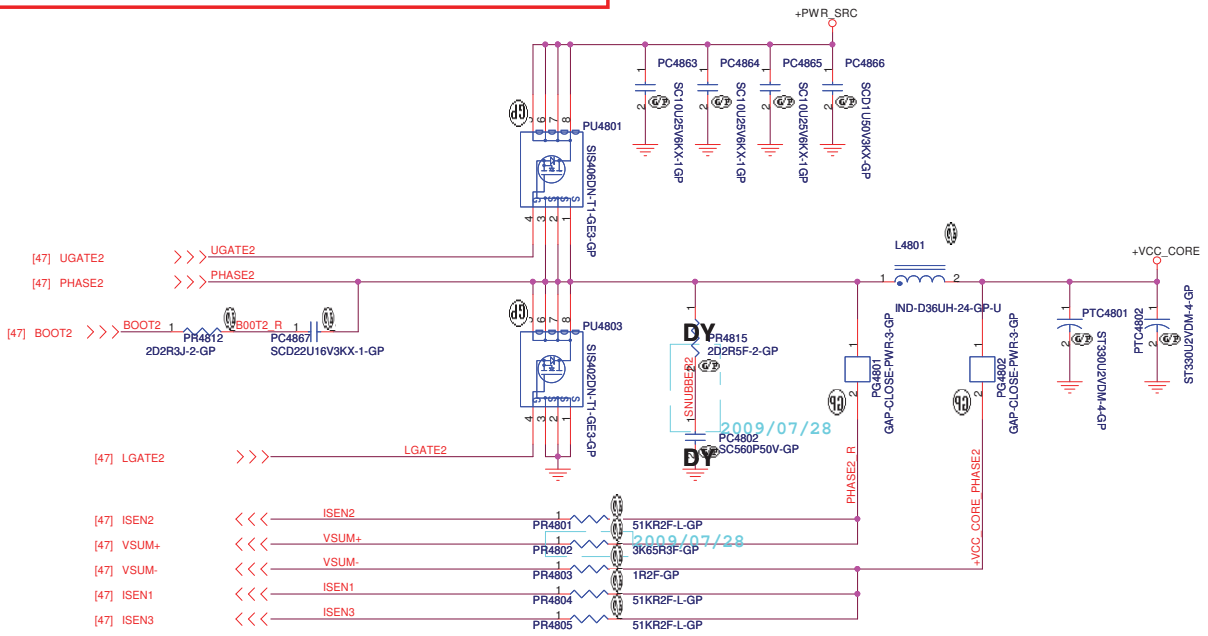
SSID = PWR.Plane.Regulator_CPU Core



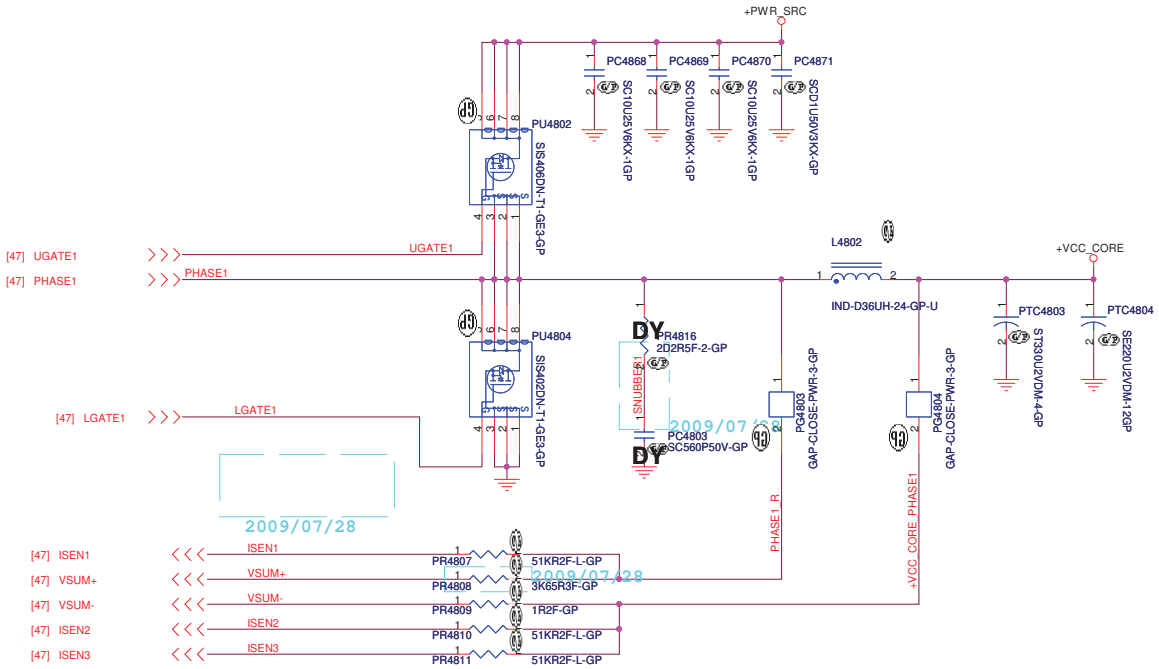
1st Samsung

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ISL62883_CPU_CORE_1/2
Size: Custom	Document Number: Winery13 MB DIS
Rev: A00	
Date: Wednesday, January 13, 2010	Sheet 47 of 88

SSID = PWR.Plane.Regulator_CPU Core



DIS(Auburndale)
Design Current = 34A
Peak Current=48A
57.6A<OCP< 67.2A



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
O/P cap: 220U 2V EEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
H/S: SiR474DP/ POWERPAK-8/ 10mOhm/12mOhm @4.5Vgs/ 84.00474.037
L/S: Si7170DP/ POWERPAK-8/ 3.6mOhm/4.3mohm@4.5Vgs/ 84.07170.037
Freq=300KHz@PER PHASE

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

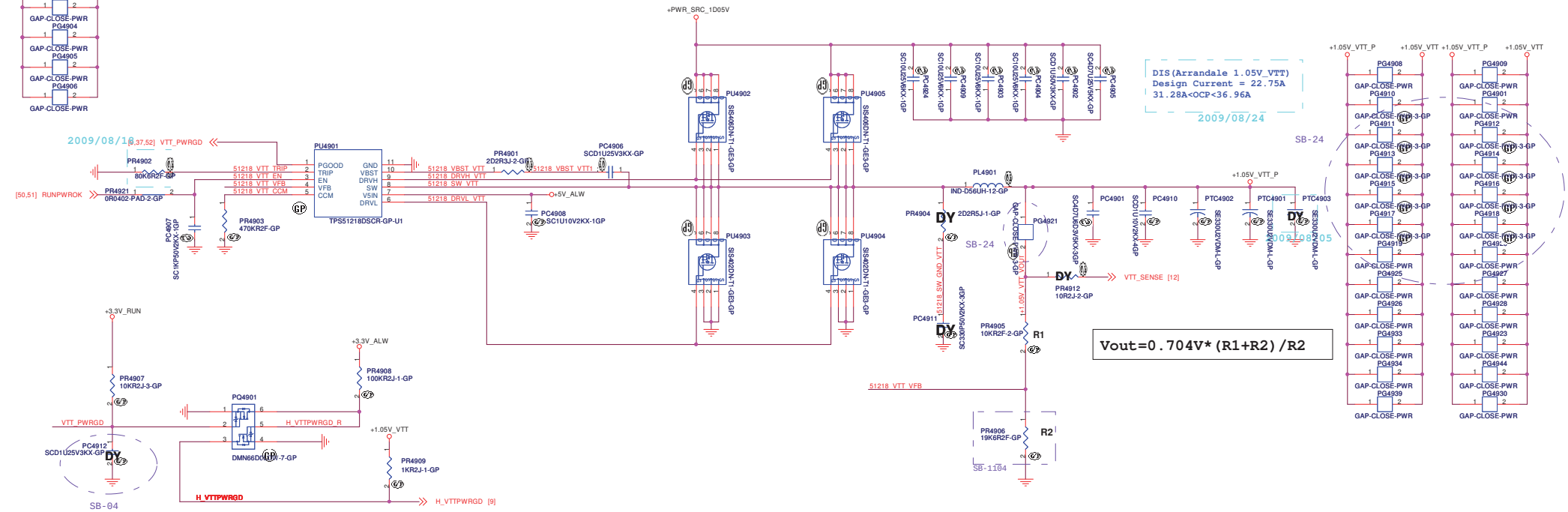
Title: ISL62883_CPU_CORE_2/2

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 48 of 88

SSID = PWR.Plane.Regulator_1D05V_VTT

TPS51218 for +1.05V_VTT



Vout=0.704V*(R1+R2)/R2

Frequency setting	
470K	-->290KHz
200K	-->340KHz
100K	-->380KHz
39K	-->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

1st Samsung

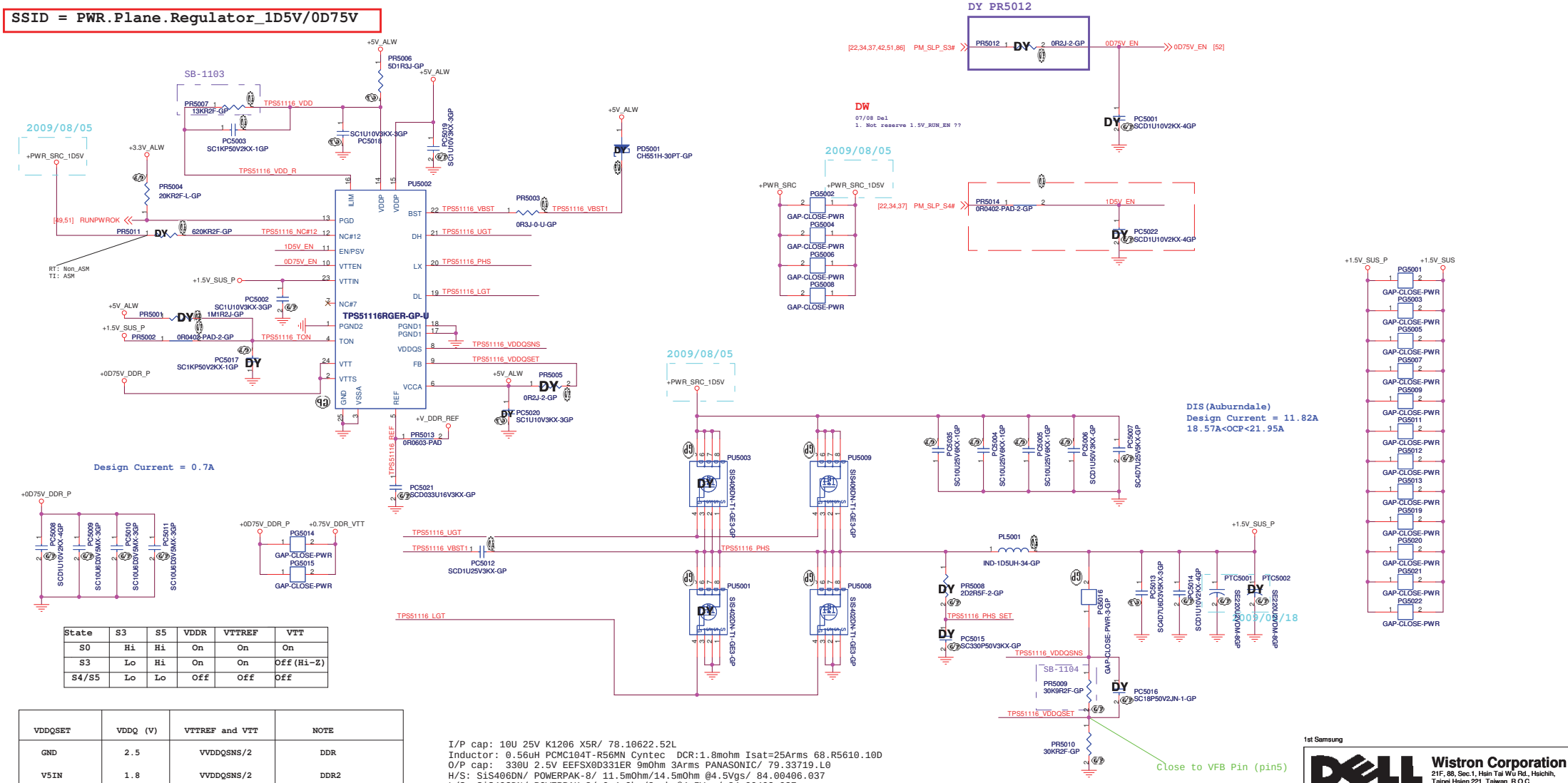
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218_+1.05V_VTT

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 49 of 88

SSID = PWR.Plane.Regulator_1D5V/0D75V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L0
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037
Switching freq-->400KHz

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

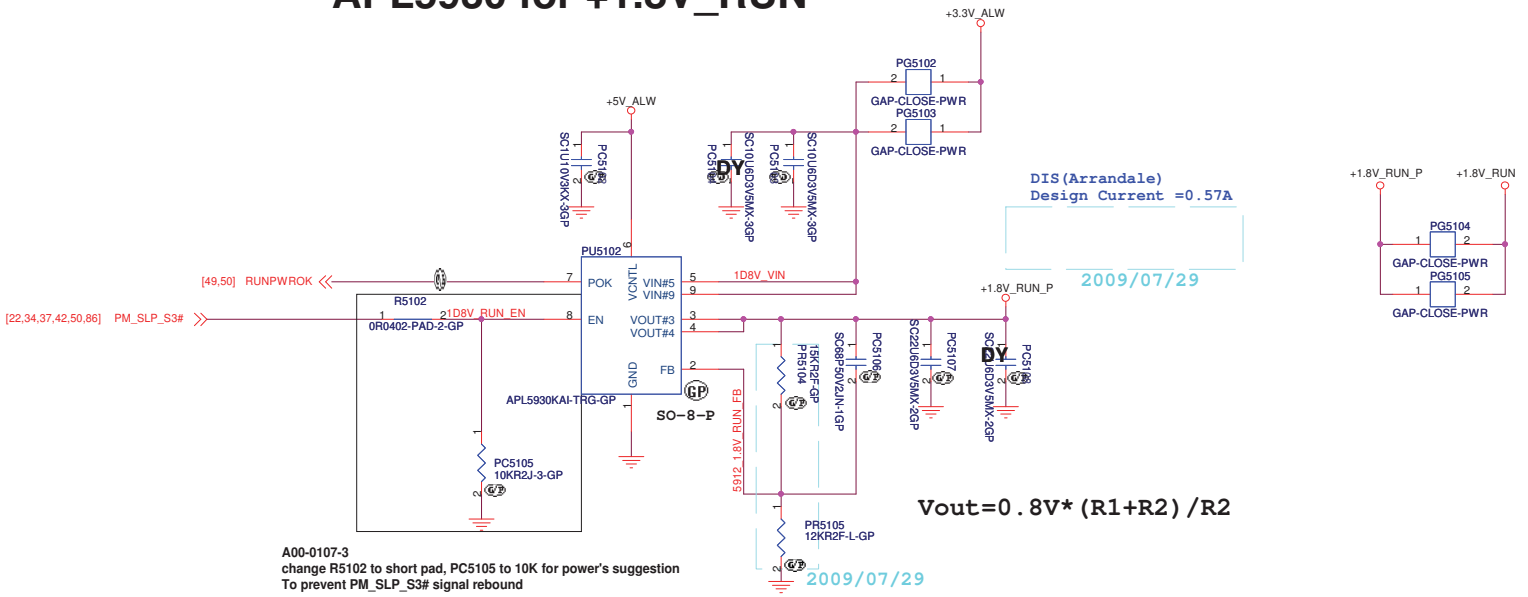
Title: TPS51116_+1.5V_SUS

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

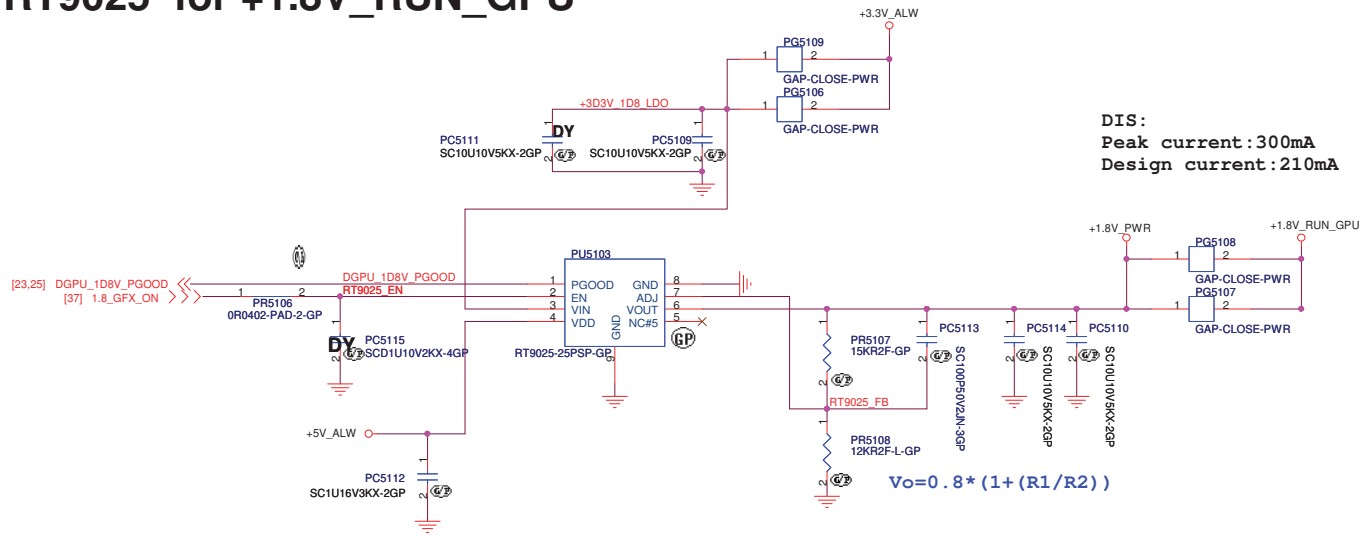
Date: Wednesday, January 13, 2010 Sheet 50 of 88

SSID = PWR.Plane.Regulator_1D8V

APL5930 for +1.8V_RUN



RT9025 for +1.8V_RUN_GPU



1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

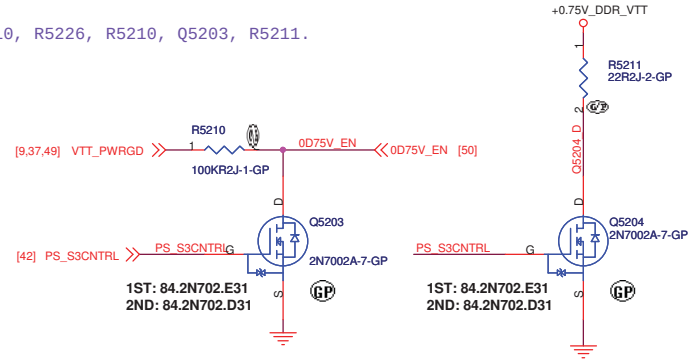
Title: APL5930/RT9205

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 51 of 88

SSID = PWR.Plane.Switch_1D5V CPU

SB-1020-1
DY R5215, R5222, R5223; POP R5221, C5210, R5226, R5210, Q5203, R5211.

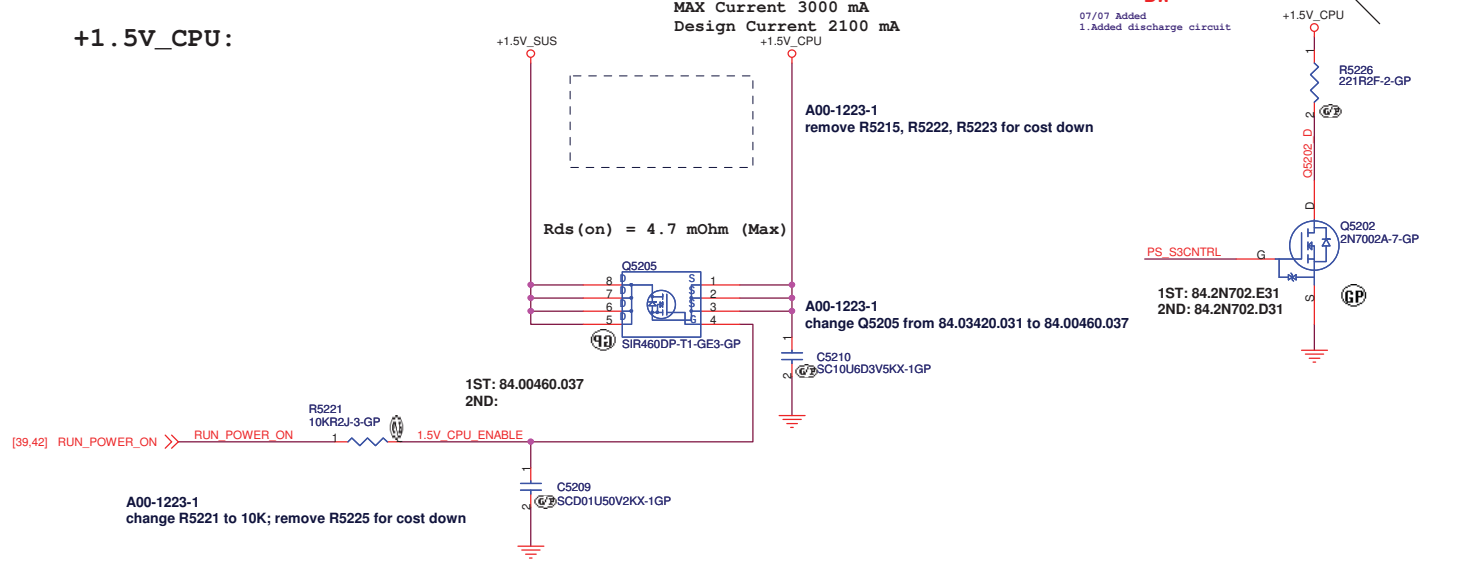


Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details
Revision 0.1

DW
07/07 Added
1.Added discharge circuit

+1.5V_CPU:

MAX Current 3000 mA
Design Current 2100 mA



DW
07/20 corrected
1. Removed C5288
2. RemovedQ5207,R5225,R5220 to save more part counts

1st Samsung

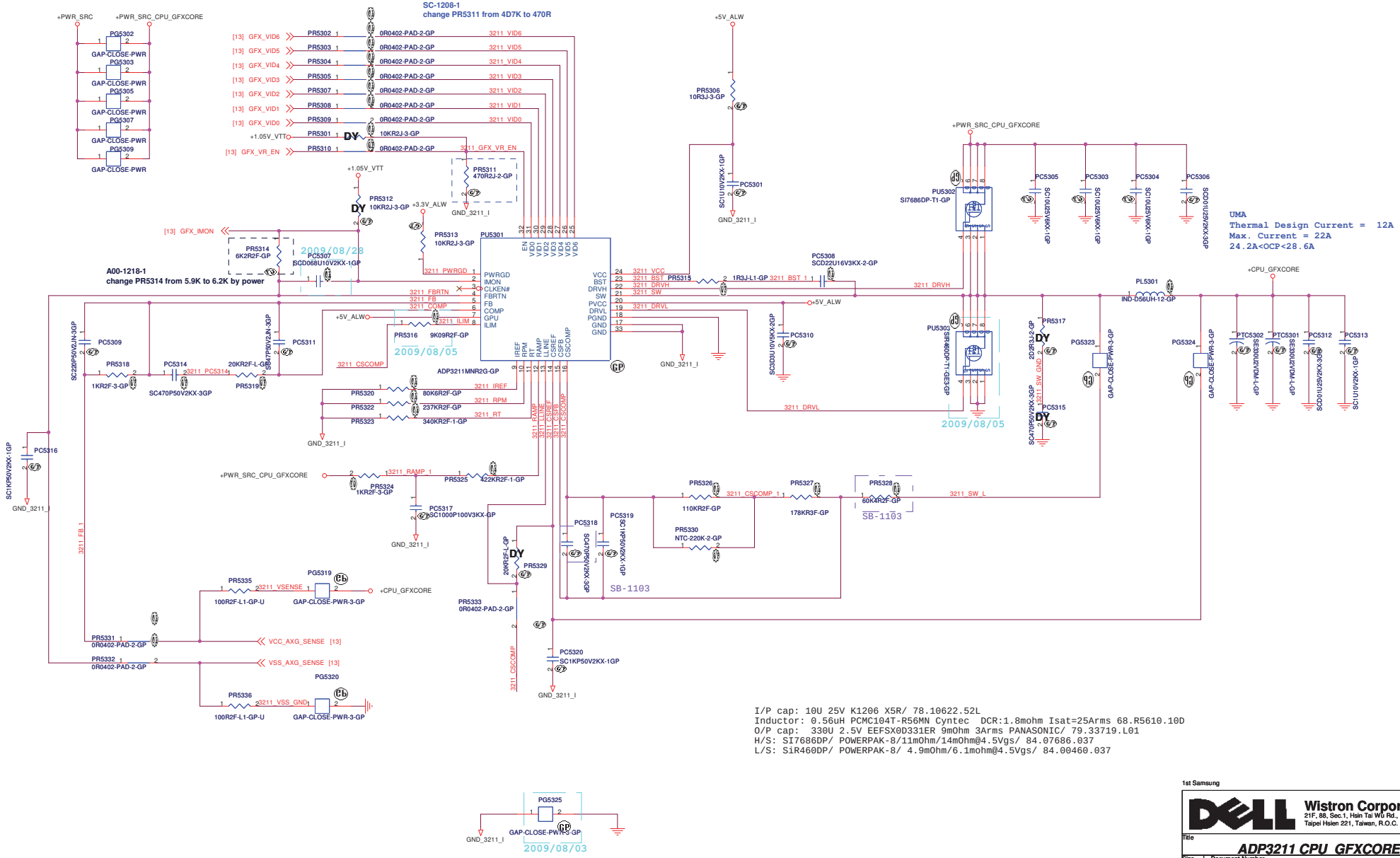
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1D5V

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 52 of 88

SSID = CPU.GFX.Regulator



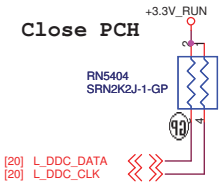
1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

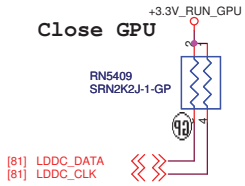
Title	ADP3211 CPU_GFXCORE		
Size: Custom	Document Number: Winery13 MB DIS		Rev: A00
Date: Wednesday, January 13, 2010	Sheet 53 of 88		

SSID = VIDEO

Close PCH



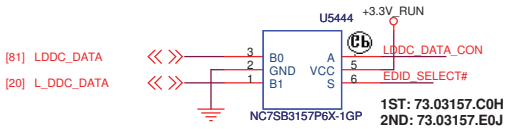
Close GPU



DW

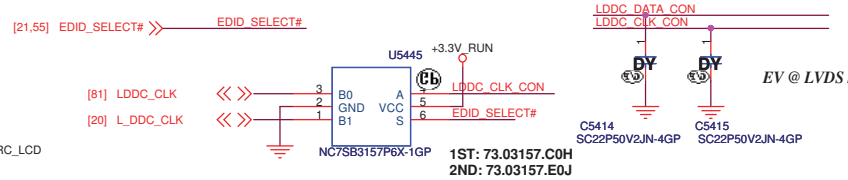
07/07 Added
1.Added LVDS DDC CLK/DAT Pull Hi

UMA/DIS LVDS DDC CLK/DAT select circuit



H=>B1 –iGPU PCH (UMA)
L=>B0 –dGPU GPU (DIS)

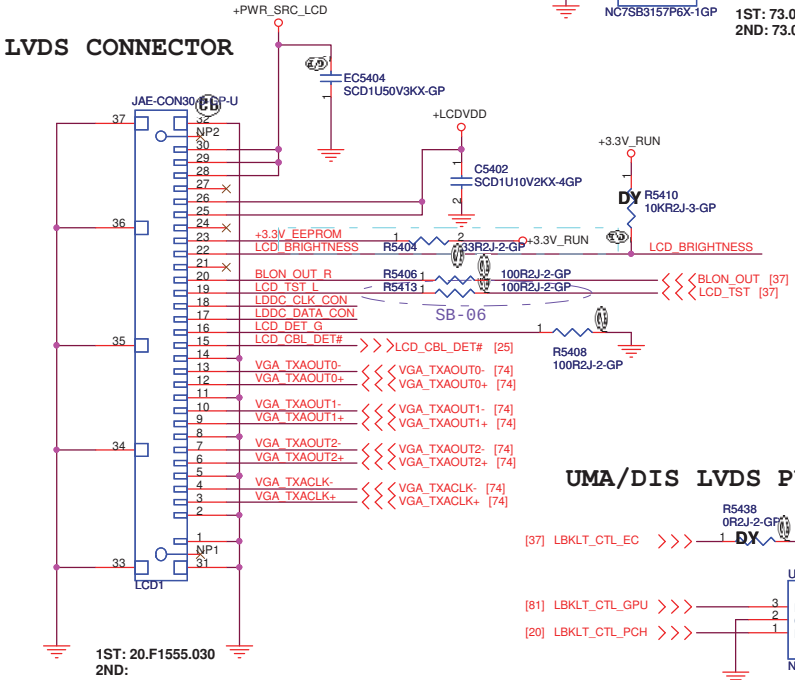
1ST: 73.03157.C0H
2ND: 73.03157.E0J



EV @ LVDS side

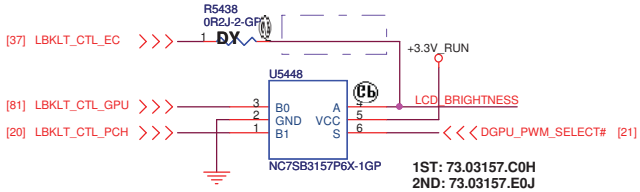
1ST: 73.03157.C0H
2ND: 73.03157.E0J

LVDS CONNECTOR



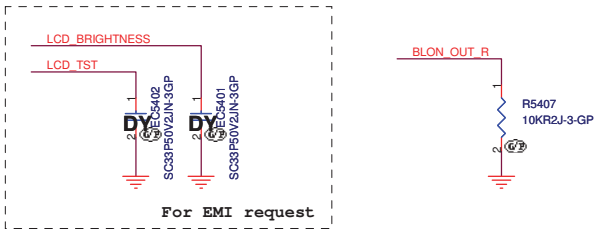
1ST: 20.F1555.030
2ND:

UMA/DIS LVDS PWM select circuit



1ST: 73.03157.C0H
2ND: 73.03157.E0J

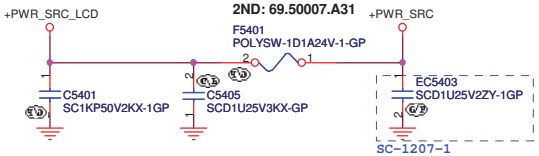
H=>B1 –iGPU PCH (UMA)
L=>B0 –dGPU GPU (DIS)



SSID = Inverter

INVERTER POWER

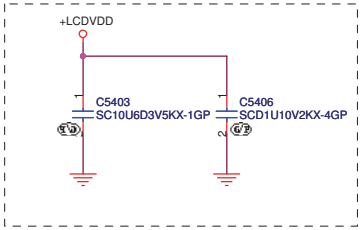
1ST: 69.50007.A41
2ND: 69.50007.A31



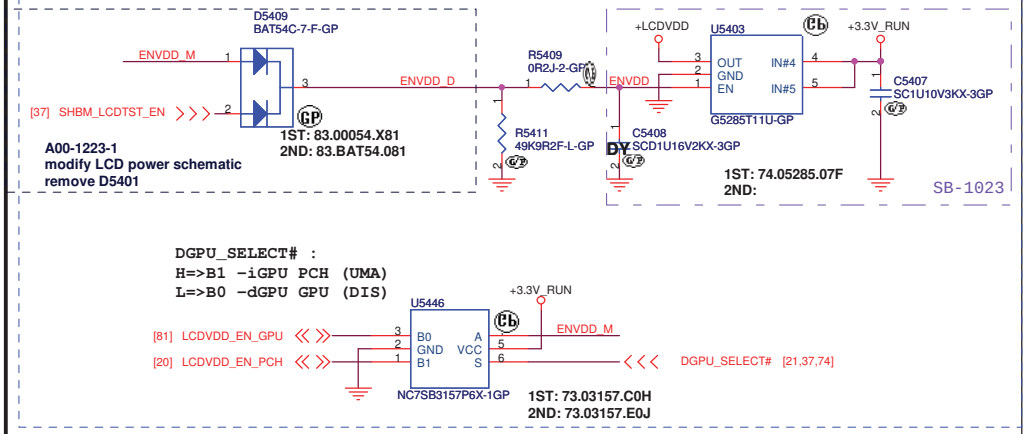
SC-1207-1
pop EC5403 for EMI

SSID = VIDEO

LCD POWER



SC-1125-2
add mux U5446 to select LCDVDD enable signal



A00-1223-1
modify LCD power schematic
remove D5401

1ST: 83.00054.X81
2ND: 83.BAT54.081

1ST: 74.05285.07F
2ND:

DGPU_SELECT# :
H=>B1 –iGPU PCH (UMA)
L=>B0 –dGPU GPU (DIS)

1ST: 73.03157.C0H
2ND: 73.03157.E0J

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LCD/Inverter Connector*

Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

Date: Wednesday, January 13, 2010 | Sheet 54 of 88

SSID = VIDEO

A00-1218-1
change R5504, R5505, R5506 from 0R to 33R by EMI

A00-1218-1
change L5501, L5502, L5503 to 0R

[74] M_RED
[74] M_GREEN
[74] M_BLUE

R5504 M_RED_C 33R2J-2-GP
R5505 M_GREEN_C 33R2J-2-GP
R5506 M_BLUE_C 33R2J-2-GP

L5502 0R3J-0-U-GP CRT_R
L5501 0R3J-0-U-GP CRT_G
L5503 0R3J-0-U-GP CRT_B

R5502 150R2F-1-GP
R5501 150R2F-1-GP
R5503 150R2F-1-GP

C5508 SC8P250V2CC-GP
C5501 SC8P250V2CC-GP
C5506 SC8P250V2CC-GP

C5509 SC8P250V2CC-GP
C5507 SC8P250V2CC-GP
C5512 SC8P250V2CC-GP

D5501 BAV99-4-GP
D5502 BAV99-4-GP
D5503 BAV99-4-GP
+3.3V_RUN_GPU

+5V_CRT_RUN
+5V_RUN
D5504 B0530WS-7-F-GP
C5510 SCD01U16V2KX-3GP

A00-0104-1
change CRT1 from 20.20431.015 to 20.20401.015

CRT1 VIDEO-15-127-GP-U
AFTP5502
CRT_R
CRT_G
CRT_B
DDC_DATA_CON
JVGA_HS [74]
JVGA_VS [74]
DDC_CLK_CON

1ST: 20.20401.015
2ND: 20.20479.015

C5502 SC33P50V2JN-3GP
C5504 SC33P50V2JN-3GP

Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

AFTP5503 +5V_CRT_RUN
AFTP5501 DDC_DATA_CON
AFTP5509 DDC_CLK_CON
AFTP5507 CRT_R
AFTP5506 CRT_G
AFTP5508 CRT_B
AFTP5504 JVGA_HS
AFTP5505 JVGA_VS

DW
07/14 Change
1.Change CRT1 CONN PN from 20.20431.015 to 20.20401.015 base on ME emm files.

DW
07/07 Change
1.Change CRT DDC CLK/DAT Circuit

UMA/DIS CRT DDC CLK/DAT select circuit

Close PCH
Close GPU
+3.3V_RUN
+3.3V_RUN_GPU
RN5510 SRN2K2J-1-GP
RN5511 SRN2K2J-1-GP
[20] GMCH_DDCDATA
[20] GMCH_DDCCLK
[81] CRT_DAT_DDC
[81] CRT_CLK_DDC

U5542 NC7SB3157P6X-1GP
U5543 NC7SB3157P6X-1GP
B0 GND B1 VCC A S
[81] CRT_DAT_DDC
[20] GMCH_DDCDATA
DDC_DATA_CON2
EDID_SELECT#
[21,54] EDID_SELECT#
[81] CRT_CLK_DDC
[20] GMCH_DDCCLK
DDC_CLK_CON2

Q5517 DMN66D0LDW-7-GP
DDC_DATA_CON2
DDC_DATA_CON
DDC_CLK_CON2
DDC_CLK_CON

H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

+5V_CRT_RUN
RN5513 SRN2K2J-1-GP
DDC_DATA_CON
DDC_CLK_CON
C5519 SC22P50V2JN-4GP
C5520 SC10P50V2JN-4GP

A00-1218-1
change C5520 from 22p to 10p by EMI

5V @ CRT side

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector
Size: A3
Document Number: Winery13 MB DIS
Rev: A00
Date: Wednesday, January 13, 2010
Sheet 55 of 88

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1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Winery13 MB DIS*	*A00*

Date:	Wednesday, January 13, 2010	Sheet	56	of	88

(Blank)

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

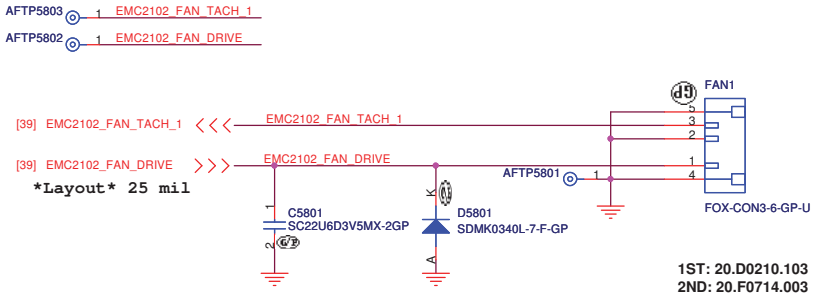
Title: HDMI Connector

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 57 of 88

SSID = Thermal

Fan Connector



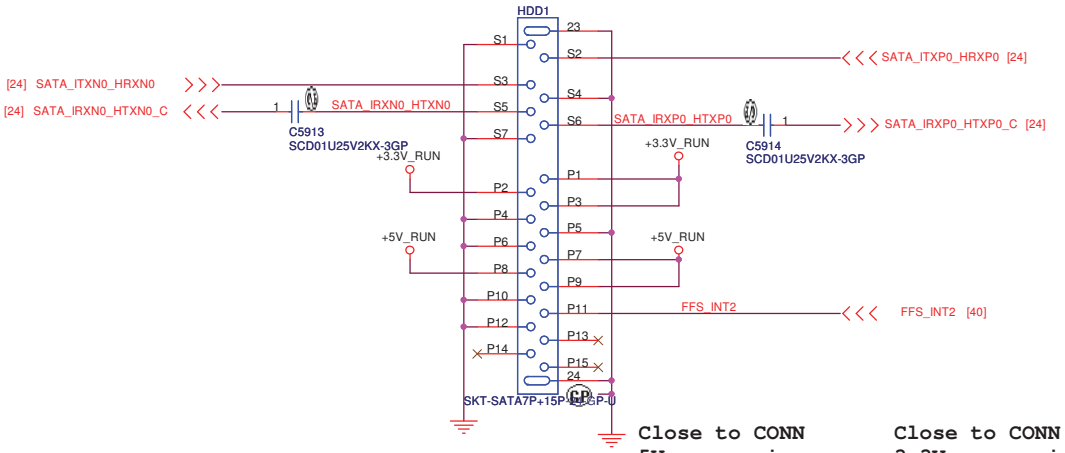
1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FAN		
Size: A3	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 58 of 88	

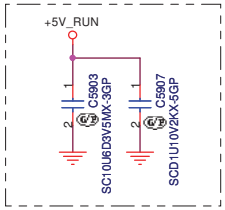
SSID = SATA

SATA HDD Connector

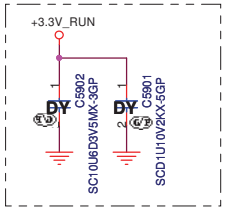


1ST: 22.10300.451
2ND:

Close to CONN
5V power pin



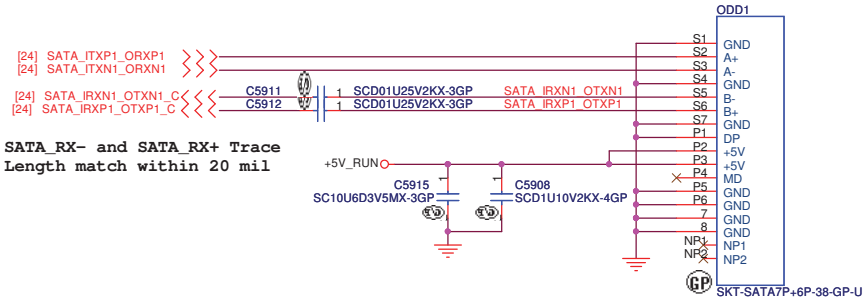
Close to CONN
3.3V power pin




```
SATA HDD Interface comment
*****************************
S1:GND
S2:RX+
S3:RX-
S4:GND
S5:TX-
S6:TX+
S7:GND
*****************************
P1------------ 3.3V
P2------------ 3.3V
P3------------ 3.3V
P4:GND
P5:GND / Dell Detected Pin
P6:GND
P7------------ 5V
P8------------ 5V
P9------------ 5V
P10--- GND
P11:Dell: FFS_INT for supported HDD
P12:GND
P13------------ 12V
P14------------ 12V
P15------------ 12V
*****************************
```

SSID = SATA

ODD Connector



SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

1ST: 62.10065.531
2ND: 62.10065.D21

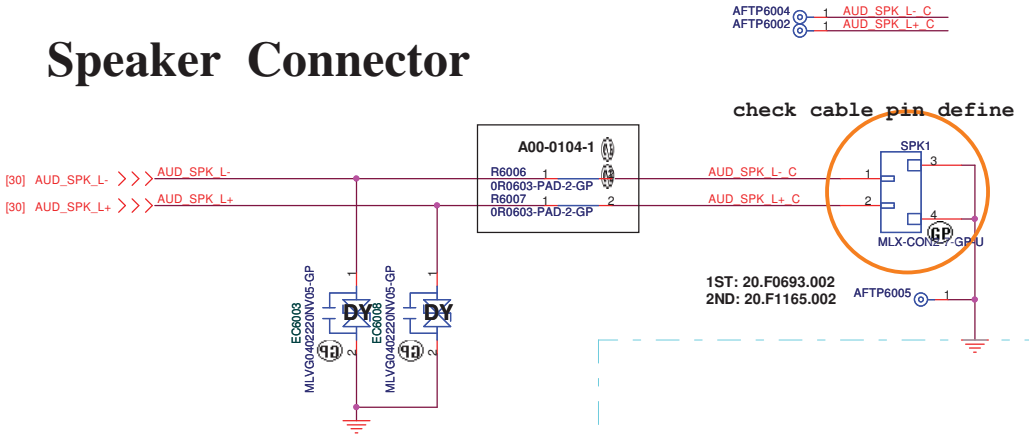
1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD/ODD Connector		
Size: A3	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 59 of 88	

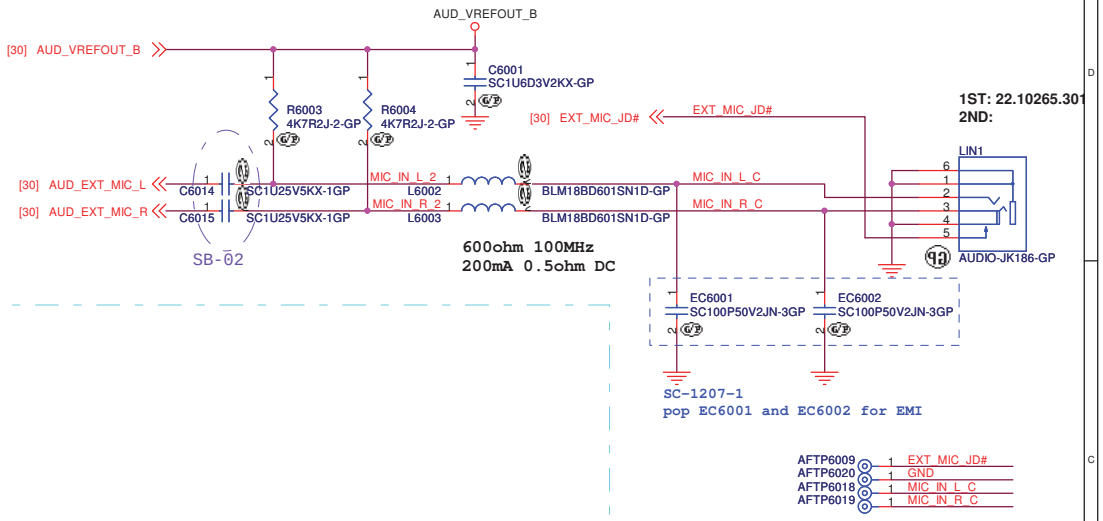
SSID = AUDIO

Speaker Connector



SSID = AUDIO

MIC IN

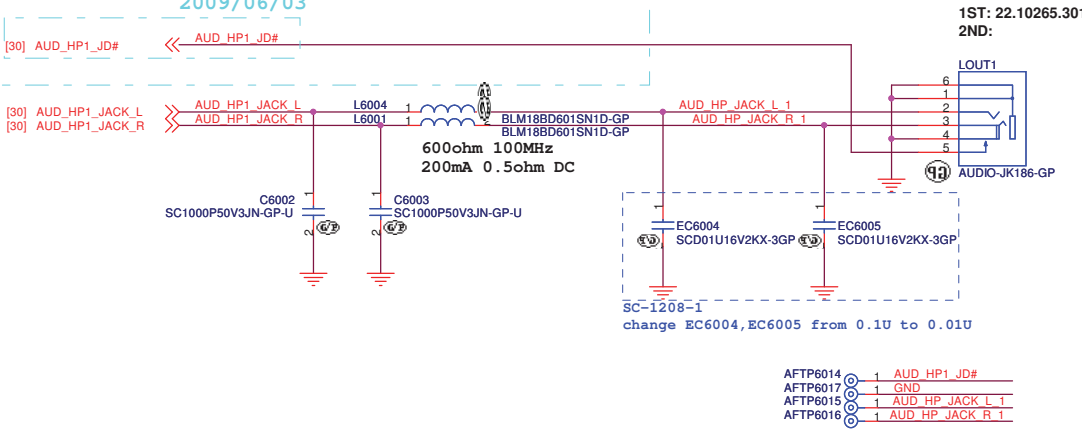


Delete Audio De-pop Circuit
2009/07/24

SSID = AUDIO

Head Phone

2009/06/03



Added HP circuit 2009/05/26

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SPEAKER/MIC/AUDIO JACK

Size	Document Number	Rev
A3	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 60 of 88

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1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

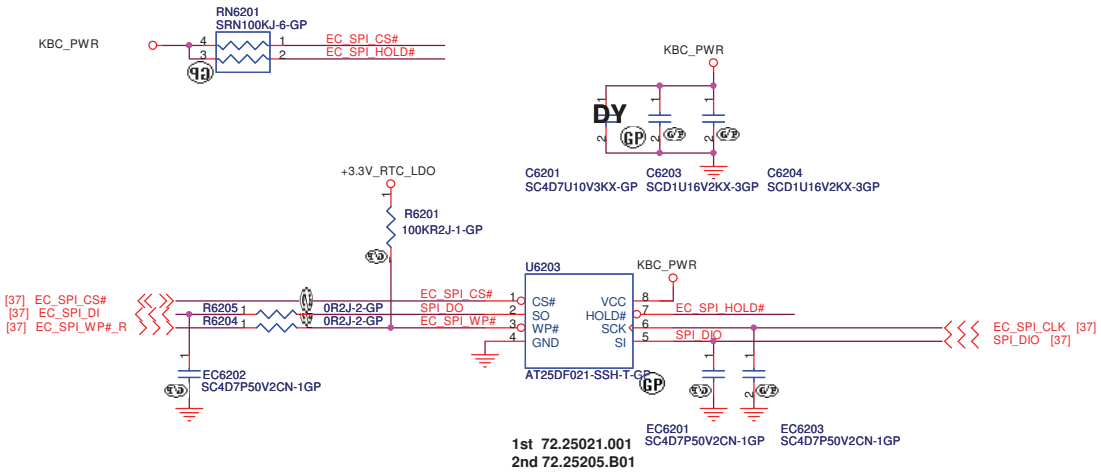
(Reserve)

Size	Document Number	Rev
Custom	*Winery13 MB DIS*	*A00*

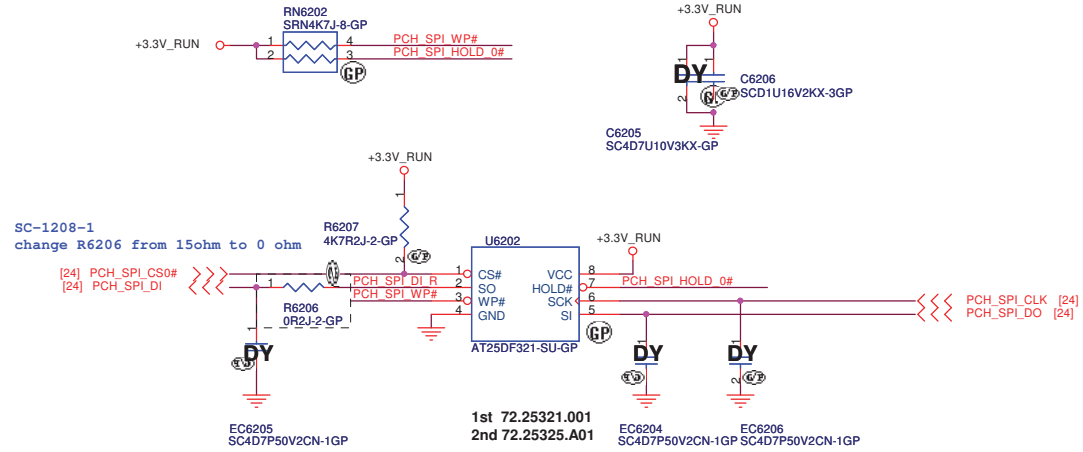
Date:	Wednesday, January 13, 2010	Sheet	61	of	88

SSID = Flash.ROM

SPI FLASH ROM (2M bits) for KBC

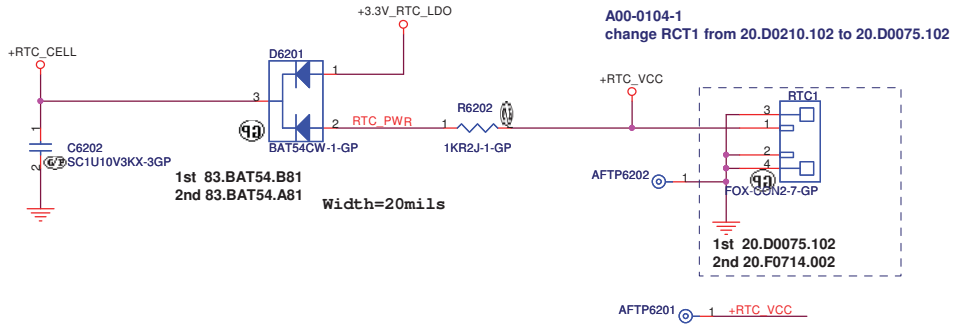


SPI FLASH ROM (32M bits) for PCH



SSID = RBATT

RTC Connector



1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

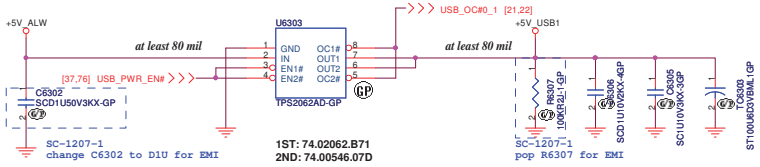
Title: EEPROM/RTC Connector

Size	Document Number	Rev
A3	Winery13 MB DIS	A00

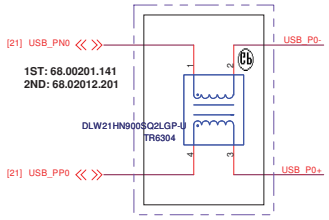
Date: Wednesday, January 13, 2010 Sheet 62 of 88

SSID = USB

USB & ESATA Power SW

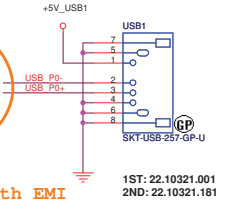


SB-1021
1. pop and change TR6304 to 90 ohm for EMI;
DY R6302, R6308



A00-0106-1
remove R6302, R6308 for no co-lay after XB

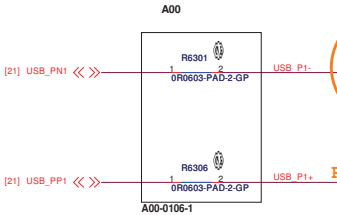
Remove ESD diode, confirmed with EMI



SSID = ESATA

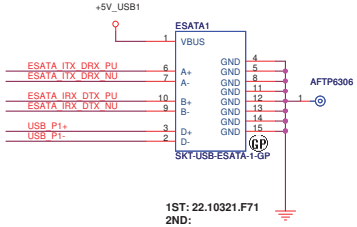
ESATA Power

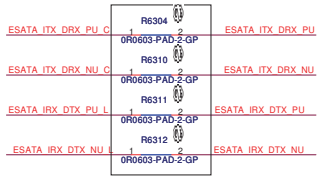
Share one power SW with USB port 1



A00-0106-1
remove TR6301 for no co-lay after XB

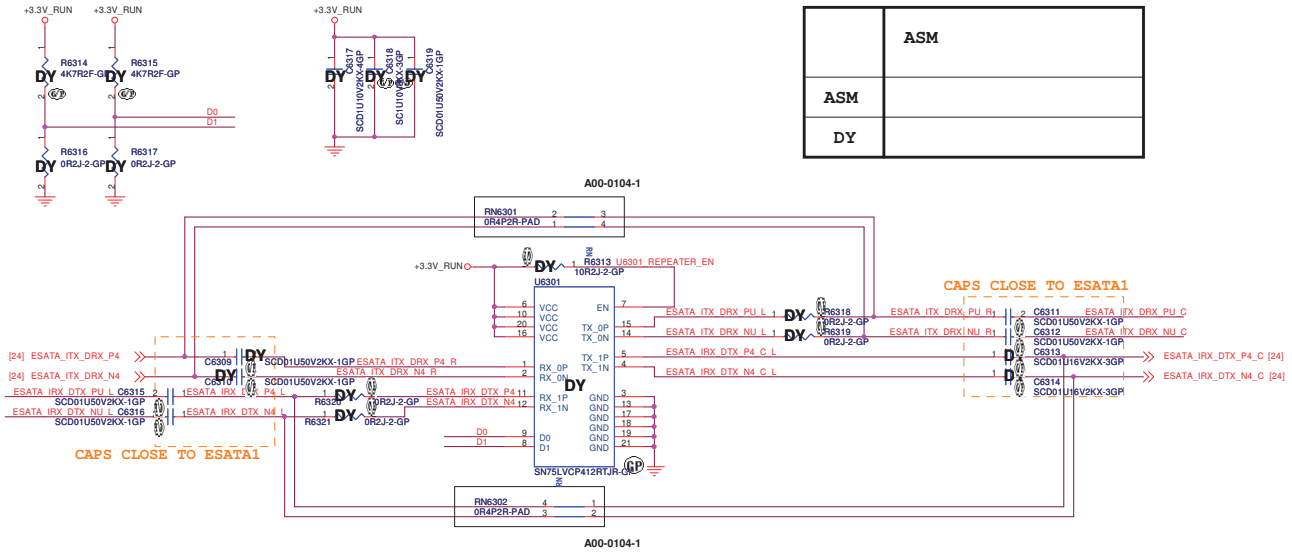
Remove ESD diode, confirmed with EMI





A00-0106-1
remove TR6302, TR6303 for no co-lay after XB

	ASM
ASM	
DY	



1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

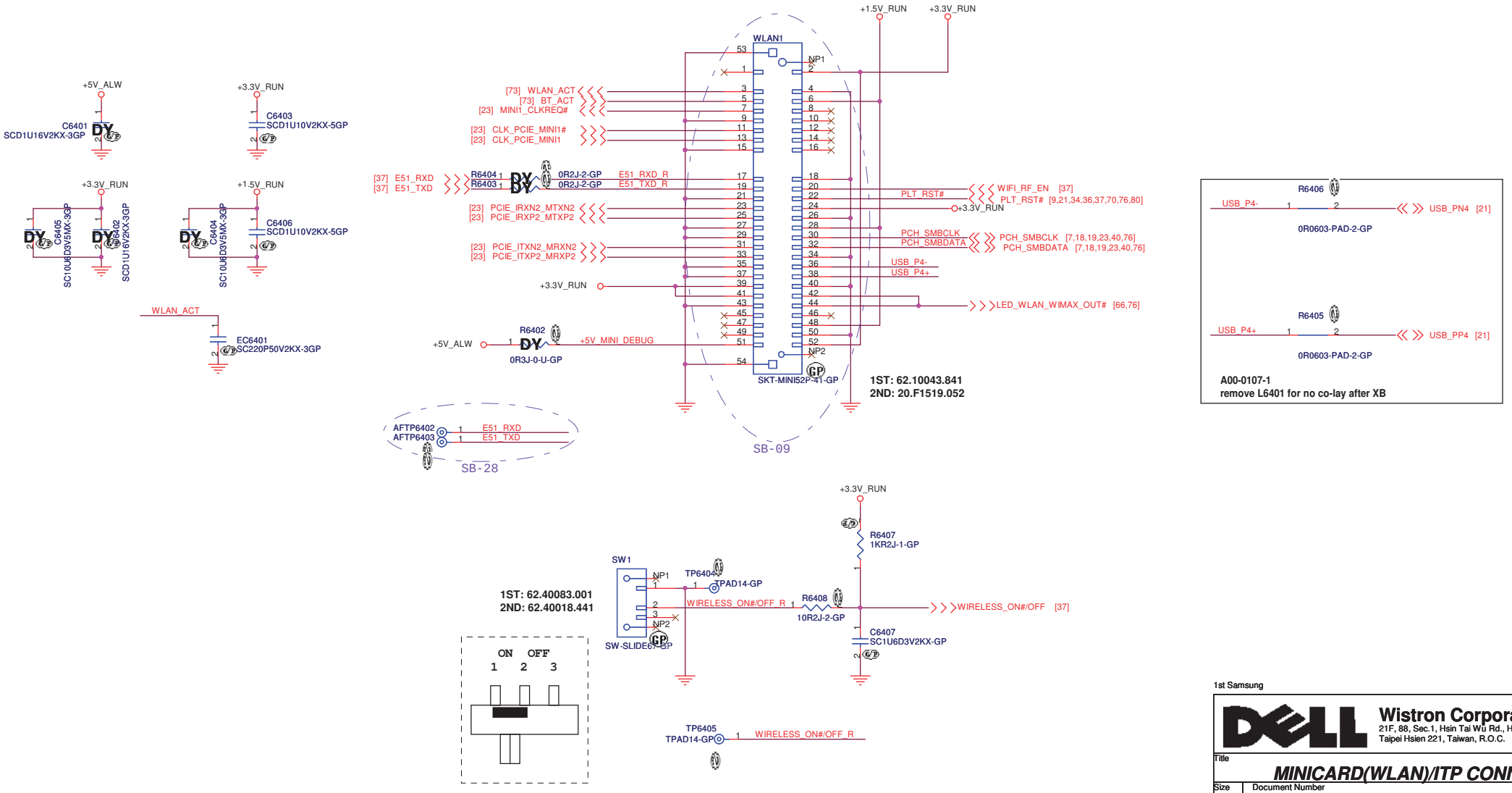
Title: USB/ESATA Port

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 63 of 88

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

Size	Document Number	Rev
A3	Winery13 MB DIS	A00

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1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

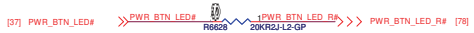
Date: Wednesday, January 13, 2010 | Sheet 65 of 88

SSID = LED

For LED & Capacity board:

LED Type	Color	Power rail
BATTERY LED1	Amber(Multi-color)	ALW
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN/WWAN ACT LED	White	RUN

PWR BTN LED

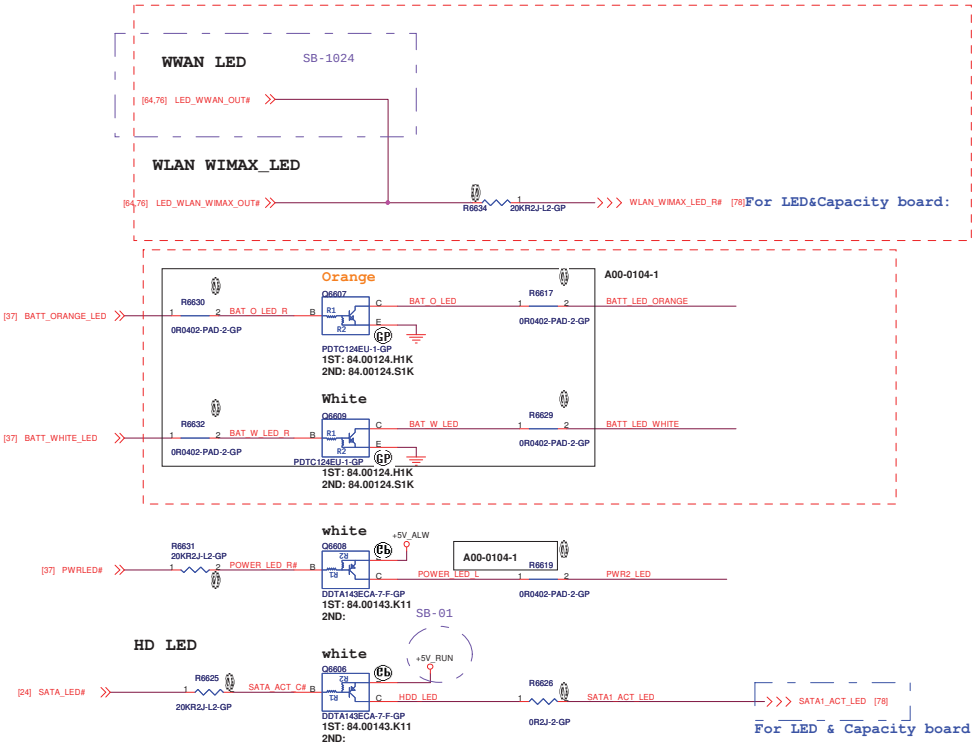


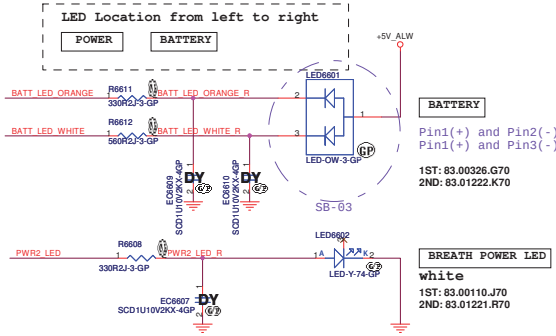
SCRLK LED

CAPS LED

NUM LED

Bluetooth LED





Remove HDD LED

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED

Size: A2 | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 66 of 88

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1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

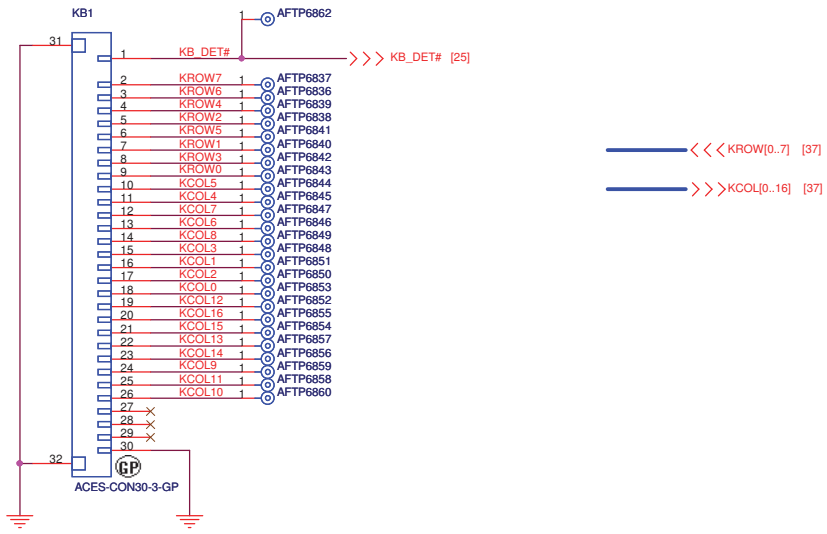
Title: *(Reserve)*

Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

Date: Wednesday, January 13, 2010 | Sheet 67 of 88

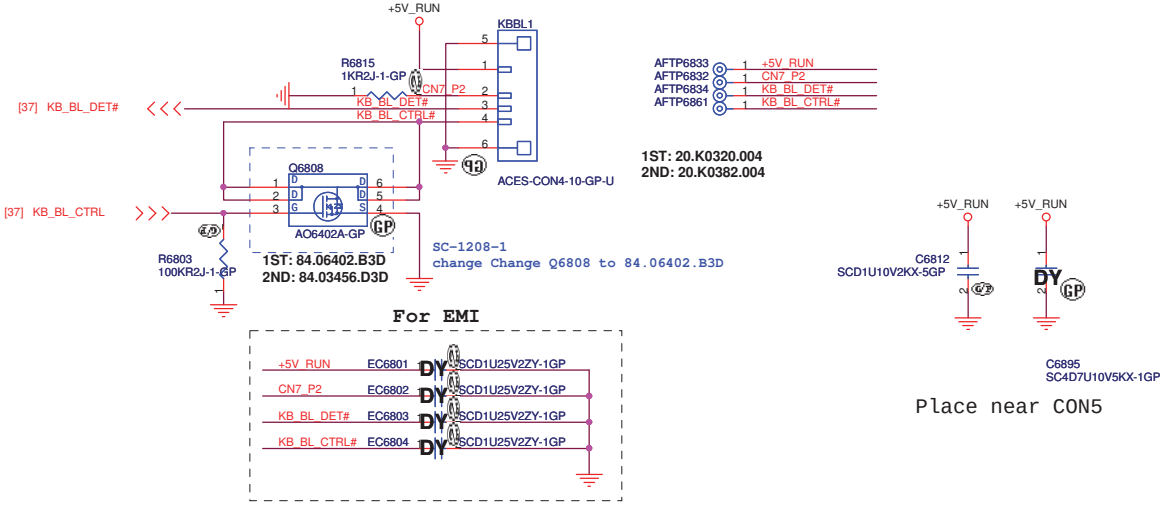
SSID = KBC

Internal KeyBoard Connector



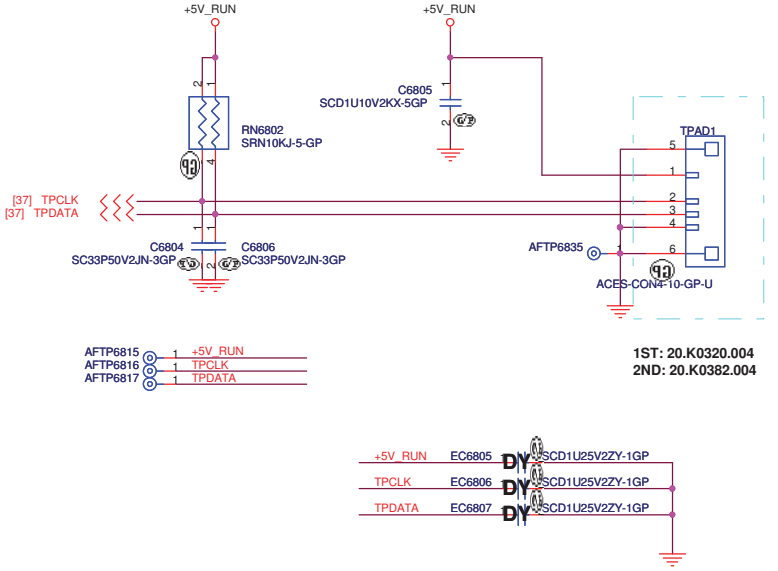
1ST: 20.K0421.030
2ND: 20.K0259.030

KB Backlight CONN



SSID = Touch.Pad

TouchPad Connector



1st Samsung

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

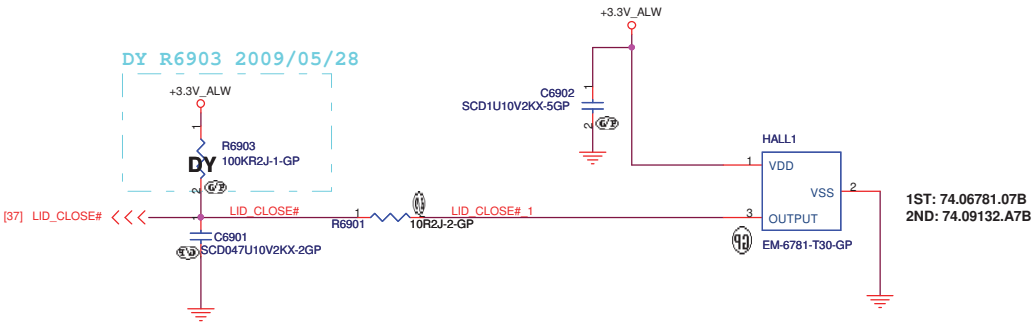
Title: Keyboard/Touch Pad

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 68 of 88

SSID = User.Interface

Hall Sensor Connector



1ST: 74.06781.07B
2ND: 74.09132.A7B

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

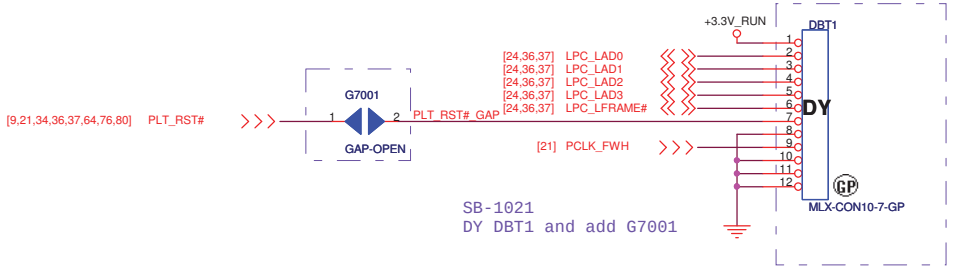
Title: Hall sensor

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 69 of 88

SSID = DEBUG PORT

GOLDEN FINGER FOR DEBUG BOARD



1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Debug port*		
Size: Custom	Document Number: *Winery13 MB DIS*	Rev: *A00*
Date: Wednesday, January 13, 2010	Sheet 70 of 88	

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1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Winery13 MB DIS*	*A00*

Date:	Wednesday, January 13, 2010	Sheet	71	of	88

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1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

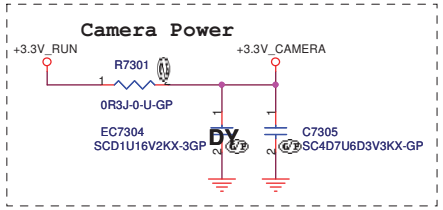
Title: Braidwood

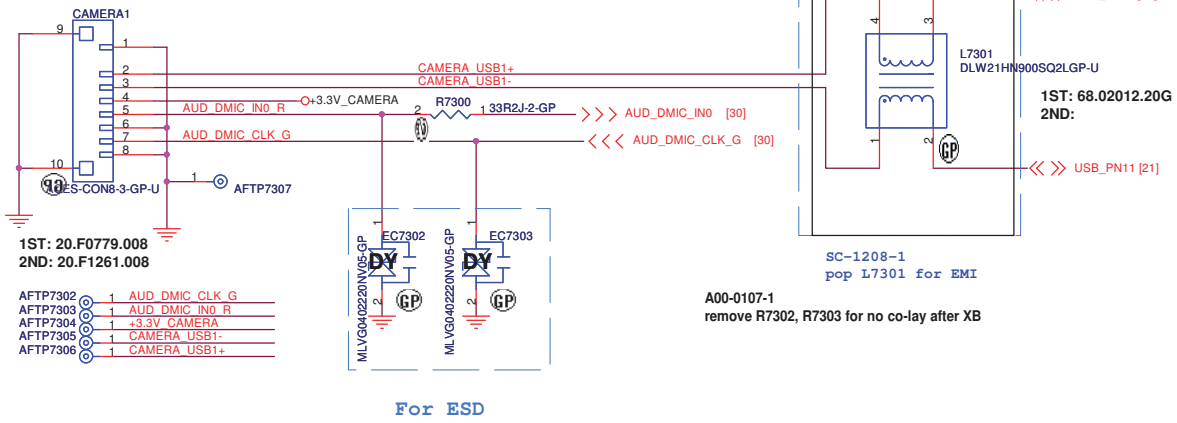
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 72 of 88

SSID = User.Interface

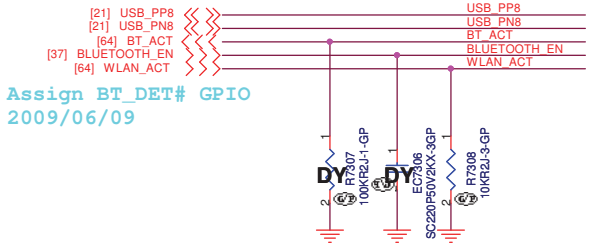
Camera Connector

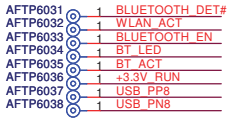


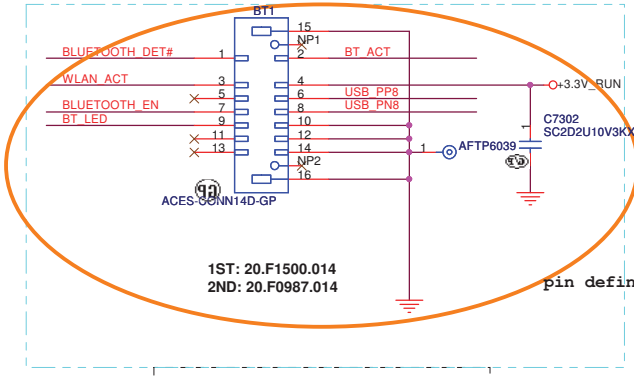


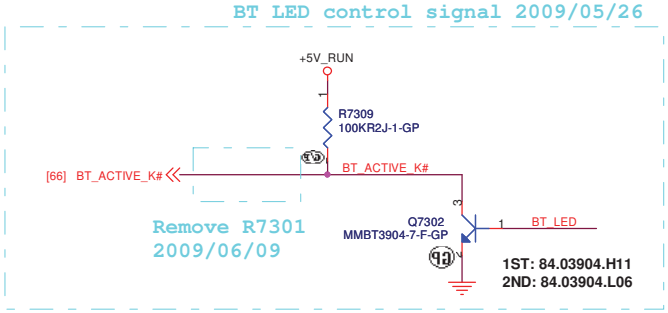
SSID = User.Interface

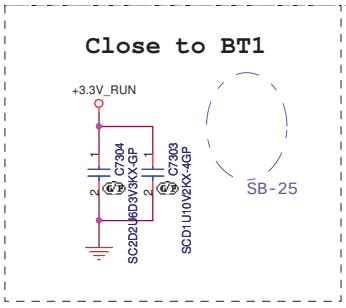
Bluetooth cable conn.











1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

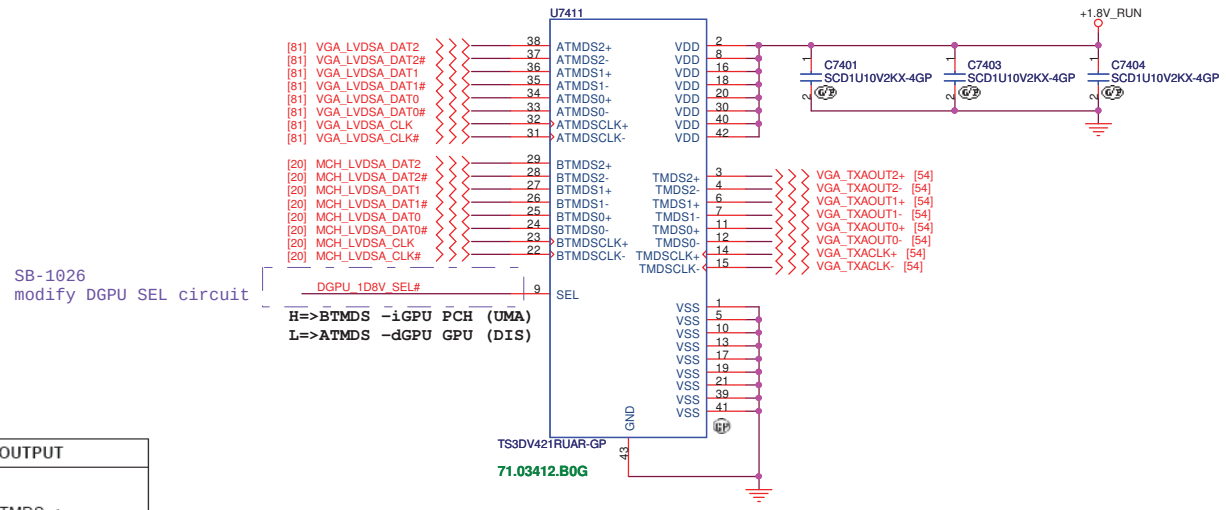
Title: Camera CONN

Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 73 of 88

SSID = VIDEO

UMA/DIS LVDS signal select circuit

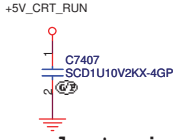


SB-1026
modify DGPU SEL circuit

H=>BTMDS -iGPU PCH (UMA)
L=>ATMDS -dGPU GPU (DIS)

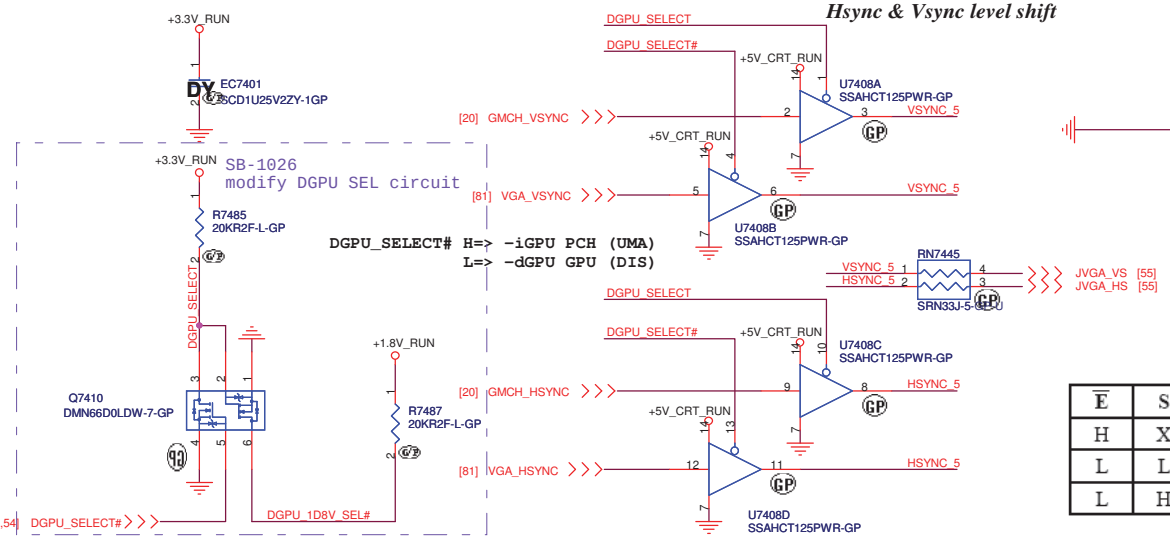
FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-



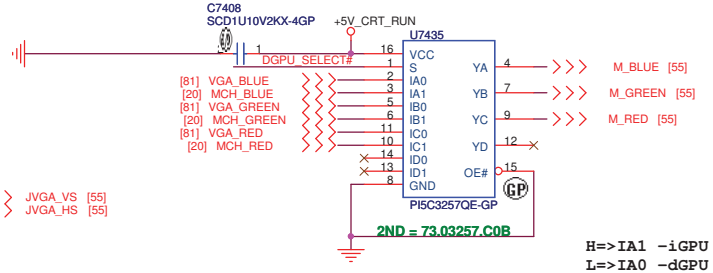
UMA/DIS CRT Hsync/Vsync select circuit

Hsync & Vsync level shift



DGPU_SELECT# H=> -iGPU PCH (UMA)
L=> -dGPU GPU (DIS)

UMA/DIS CRT signal select circuit



H=>IA1 -iGPU PCH (UMA)
L=>IA0 -dGPU GPU (DIS)

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

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Title: **PX Swith-1**

Size: Custom | Document Number: **Winery13 MB DIS** | Rev: **A00**

Date: Wednesday, January 13, 2010 | Sheet 74 of 88

(Blank)

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Title: *(Reserve)*

Size: A3 | Document Number: *Winery13 MB DIS* | Rev: *A00*

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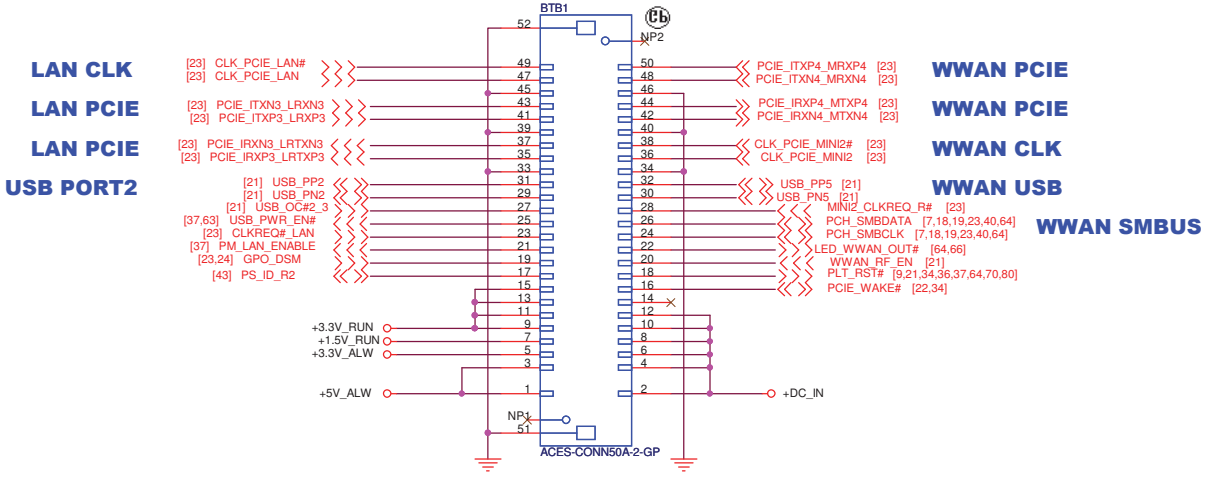
DC_IN baord CON

+DC_IN	:	19.5V/85W
+3.3V_RUN	:	3300mA
+5V_ALW	:	1000mA
+1.5V_RUN	:	500mA
+3.3V_ALW	:	58mA

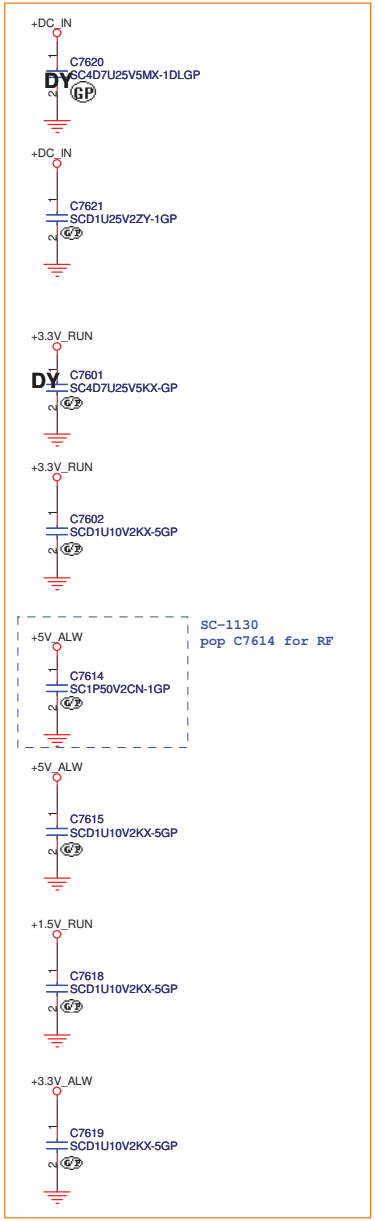
Please reoute 300 mil at least.



Remove AFTP test point
Confirmed with AFTE.

1ST: 20.F1631.050
2ND:

Place near BTB1



<Core Design>

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Title	DC_IN Board BTB Connector	
Size: Custom	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 76 of 88	

(Blank)

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Title

Audio BD/IO BD CONN

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

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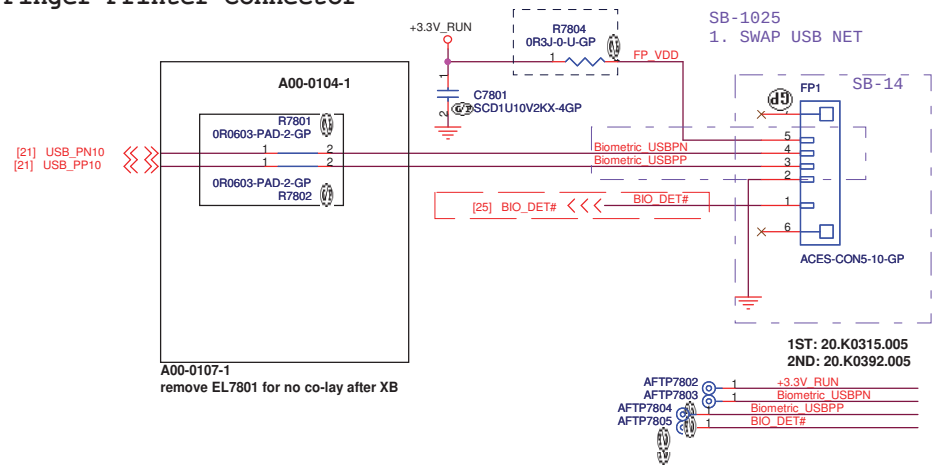
SSID = User.Interface

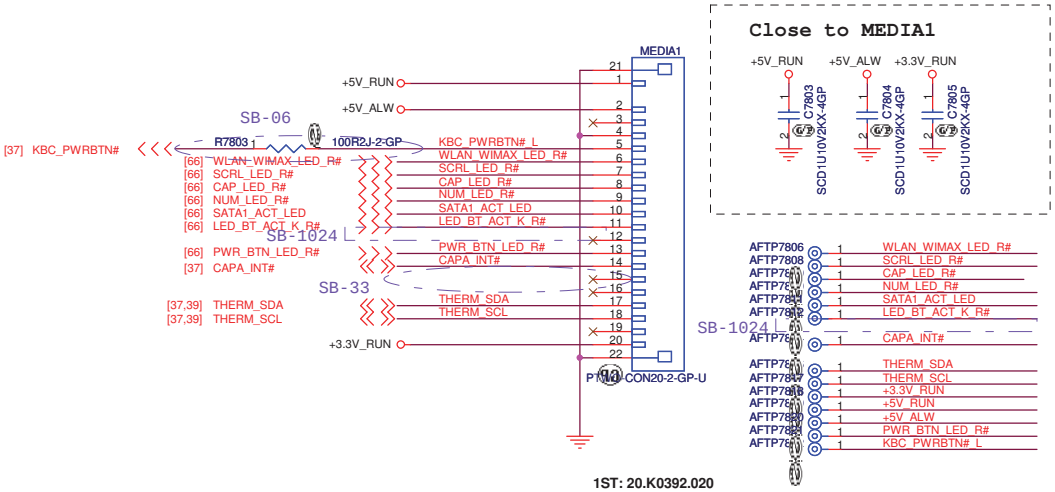
Finger Printer Connector

A00-1223-1
1. dummy FP1 pin6, pin7 for power pin short to GND when plug in cable issue
2. add damping resister R7804



1ST: 20.K0315.005
2ND: 20.K0392.005

LED&Capacity board CONN



1ST: 20.K0392.020
2ND: 20.K0481.020

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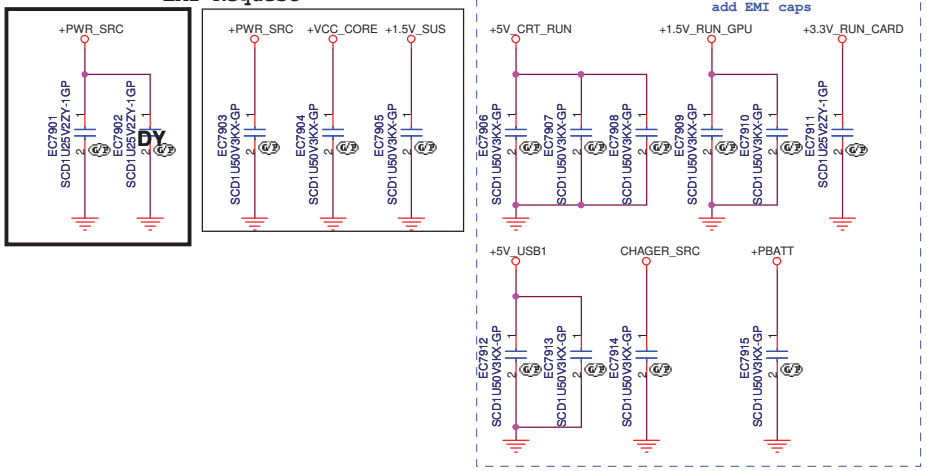
Title: *Finger Printer/Felica/Capacity*

Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

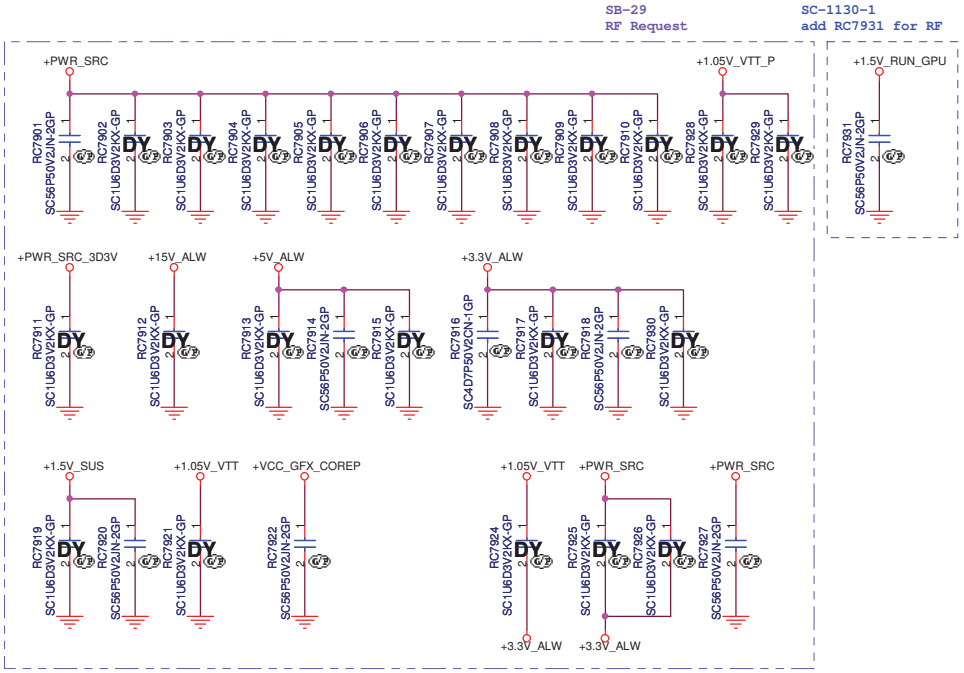
Date: Wednesday, January 13, 2010 | Sheet 78 of 88

SSID = EMI

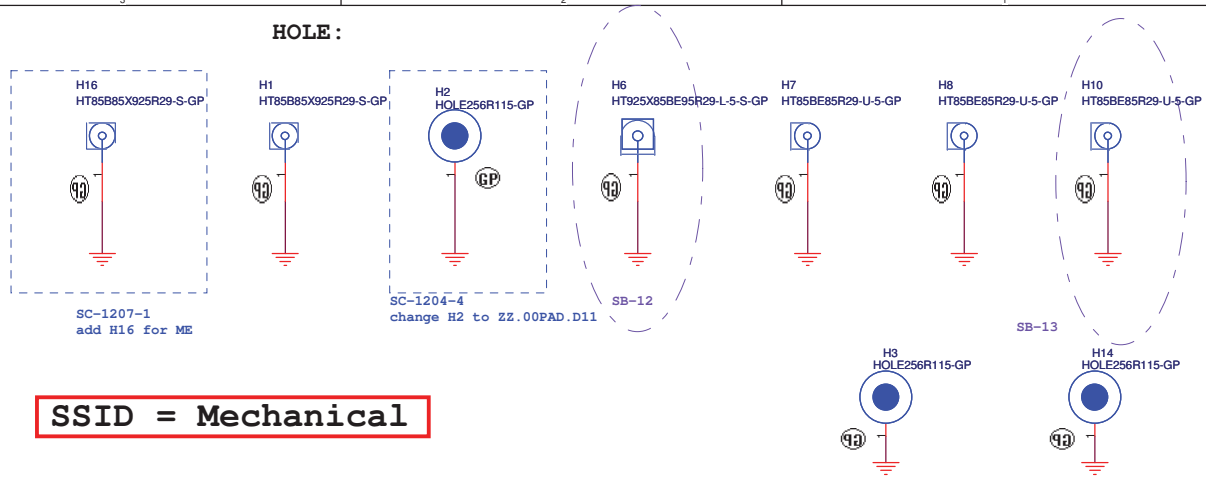
EMI Request



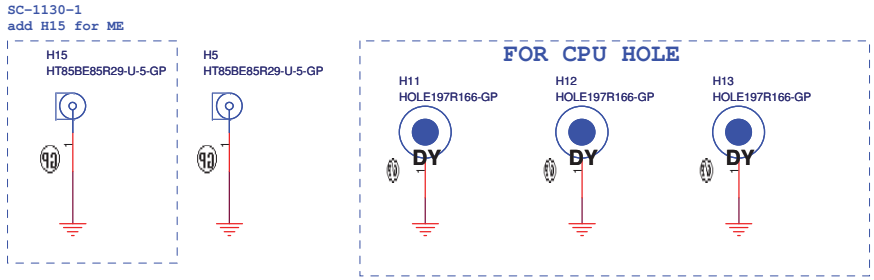
SSID = RF

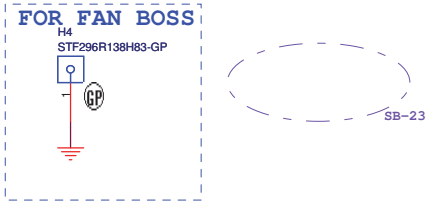


HOLE:

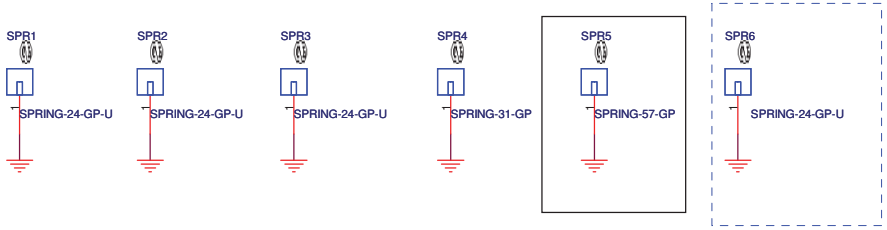


SSID = Mechanical





A00-0105-1
change SPR5 from 34.4F822.002 to 34.42T14.002 by ME



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Title: Miscellaneous Components

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 79 of 88

SSID = VIDEO

PCIE_MTX_GRX_P[0..15] PCIE_MTX_GRX_P[0..15] [8]
PCIE_MTX_GRX_N[0..15] PCIE_MTX_GRX_N[0..15] [8]
PCIE_MRX_GTX_P[0..15] PCIE_MRX_GTX_P[0..15] [8]
PCIE_MRX_GTX_N[0..15] PCIE_MRX_GTX_N[0..15] [8]

U8001B 2 OF 7

PCIE_MTX_GRX_P0	AE12	PEX_RX0	PEX_TX0	AD10	PCIE_MRX_GTX_C_P0	C8033
PCIE_MTX_GRX_N0	AF12	PEX_RX0#	PEX_TX0#	AD11	PCIE_MRX_GTX_C_N0	C8034
PCIE_MTX_GRX_P1	AG12	PEX_RX1	PEX_TX1	AD12	PCIE_MRX_GTX_C_P1	C8035
PCIE_MTX_GRX_N1	AG13	PEX_RX1#	PEX_TX1#	AC12	PCIE_MRX_GTX_C_N1	C8036
PCIE_MTX_GRX_P2	AF13	PEX_RX2	PEX_TX2	AB11	PCIE_MRX_GTX_C_P2	C8037
PCIE_MTX_GRX_N2	AE13	PEX_RX2#	PEX_TX2#	AB12	PCIE_MRX_GTX_C_N2	C8038
PCIE_MTX_GRX_P3	AE15	PEX_RX3	PEX_TX3	AD13	PCIE_MRX_GTX_C_P3	C8039
PCIE_MTX_GRX_N3	AF15	PEX_RX3#	PEX_TX3#	AD14	PCIE_MRX_GTX_C_N3	C8040
PCIE_MTX_GRX_P4	AG15	PEX_RX4	PEX_TX4	AD15	PCIE_MRX_GTX_C_P4	C8042
PCIE_MTX_GRX_N4	AG16	PEX_RX4#	PEX_TX4#	AC15	PCIE_MRX_GTX_C_N4	C8043
PCIE_MTX_GRX_P5	AF16	PEX_RX5	PEX_TX5	AB14	PCIE_MRX_GTX_C_P5	C8044
PCIE_MTX_GRX_N5	AE16	PEX_RX5#	PEX_TX5#	AB15	PCIE_MRX_GTX_C_N5	C8045
PCIE_MTX_GRX_P6	AE18	PEX_RX6	PEX_TX6	AC16	PCIE_MRX_GTX_C_P6	C8047
PCIE_MTX_GRX_N6	AF18	PEX_RX6#	PEX_TX6#	AD16	PCIE_MRX_GTX_C_N6	C8048
PCIE_MTX_GRX_P7	AG18	PEX_RX7	PEX_TX7	AD17	PCIE_MRX_GTX_C_P7	C8050
PCIE_MTX_GRX_N7	AG19	PEX_RX7#	PEX_TX7#	AD18	PCIE_MRX_GTX_C_N7	C8051
PCIE_MTX_GRX_P8	AF19	PEX_RX8	PEX_TX8	AC18	PCIE_MRX_GTX_C_P8	C8052
PCIE_MTX_GRX_N8	AE19	PEX_RX8#	PEX_TX8#	AB18	PCIE_MRX_GTX_C_N8	C8053
PCIE_MTX_GRX_P9	AE21	PEX_RX9	PEX_TX9	AB19	PCIE_MRX_GTX_C_P9	C8054
PCIE_MTX_GRX_N9	AF21	PEX_RX9#	PEX_TX9#	AB20	PCIE_MRX_GTX_C_N9	C8055
PCIE_MTX_GRX_P10	AG21	PEX_RX10	PEX_TX10	AD19	PCIE_MRX_GTX_C_P10	C8056
PCIE_MTX_GRX_N10	AG22	PEX_RX10#	PEX_TX10#	AD20	PCIE_MRX_GTX_C_N10	C8057
PCIE_MTX_GRX_P11	AF22	PEX_RX11	PEX_TX11	AD21	PCIE_MRX_GTX_C_P11	C8058
PCIE_MTX_GRX_N11	AE22	PEX_RX11#	PEX_TX11#	AC21	PCIE_MRX_GTX_C_N11	C8077
PCIE_MTX_GRX_P12	AE24	PEX_RX12	PEX_TX12	AB21	PCIE_MRX_GTX_C_P12	C8078
PCIE_MTX_GRX_N12	AF24	PEX_RX12#	PEX_TX12#	AB22	PCIE_MRX_GTX_C_N12	C8079
PCIE_MTX_GRX_P13	AG24	PEX_RX13	PEX_TX13	AC22	PCIE_MRX_GTX_C_P13	C8080
PCIE_MTX_GRX_N13	AF25	PEX_RX13#	PEX_TX13#	AD22	PCIE_MRX_GTX_C_N13	C8081
PCIE_MTX_GRX_P14	AG25	PEX_RX14	PEX_TX14	AD23	PCIE_MRX_GTX_C_P14	C8082
PCIE_MTX_GRX_N14	AG26	PEX_RX14#	PEX_TX14#	AD24	PCIE_MRX_GTX_C_N14	C8083
PCIE_MTX_GRX_P15	AE27	PEX_RX15	PEX_TX15	AE25	PCIE_MRX_GTX_C_P15	C8084
PCIE_MTX_GRX_N15	AF27	PEX_RX15#	PEX_TX15#	AE26	PCIE_MRX_GTX_C_N15	C8085

SCD1U10V2KX-5GP PCIE_MRX_GTX_P0 … PCIE_MRX_GTX_P15
SCD1U10V2KX-5GP PCIE_MRX_GTX_N0 … PCIE_MRX_GTX_N15

+1.05V_GFX_PCIE

SC22U6D3V5MX-2GP C8069, SC1U6D3V5KX-1GP C8074, SC4D7U6D3V3KX-GP C8064, SC1U10V2KX-1GP C8067, SC1U6D3V2KX-GP C8068 — Place near GPU

SCD1U16V2KX-3GP C8066, SCD1U16V2KX-3GP C8065 — Place under GPU

Revised decoupling C 2009/05/28

AB13	PEX_IOVDDQ	PEX_IOVDD	AC9
AB16	PEX_IOVDDQ	PEX_IOVDD	AD7
AB17	PEX_IOVDDQ	PEX_IOVDD	AD8
AB7	PEX_IOVDDQ	PEX_IOVDD	AE7
AB8	PEX_IOVDDQ	PEX_IOVDD	AF7
AB9	PEX_IOVDDQ	PEX_IOVDD	AG7
AC13	PEX_IOVDDQ		
AC7	PEX_IOVDDQ		
AD6	PEX_IOVDDQ		
AE6	PEX_IOVDDQ		
AF6	PEX_IOVDDQ		
AG6	PEX_IOVDDQ		

PEX_REFCLK AB10 CLK_PCIE_VGA → CLK_PCIE_VGA [23]
PEX_REFCLK# AC10 CLK_PCIE_VGA# → CLK_PCIE_VGA# [23]

PEX_TSTCLK_OUT AF10 PEX_TEST_PLL_CLK_OUT
PEX_TSTCLK_OUT# AE10 PEX_TEST_PLL_CLK_OUT# — 200R2F-L-GP — DY — R8002

PEX_CLKREQ# AE9 PEX_CLKREQ#
PEX_RST# AD9 PEX_RST#

PEX_SVDD_3V3 AG9 — +3.3V_RUN_GPU
PEX_TERMP AG10 PEX_TERMP — R8001 2K49R2F-GP
PEX_PLLVDD AF9 — +PEX_PLLVDD
PLLVDD K5 — +GPU_PLLVDD

GT218-ES-S-A1-GP

Revised decoupling C 2009/05/28

SCD1U16V2KX-3GP C8059, SCD1U16V2KX-3GP C8060 — Place under GPU
SC1U6D3V2KX-GP C8063, SC1U6D3V2KX-GP C8062, SC1U10V3KX-3GP C8061, SC1U10V3KX-3GP C8073, SC10U6D3V5KX-1GP C8041, SC10U6D3V5KX-1GP C8040 — Place near GPU, +1.05V_GFX_PCIE

Revised decoupling C 2009/05/28

+3.3V_RUN_GPU
R8004 10KR2J-3-GP

Change R8004 resistor value 2009/06/05

DW
07/10 NO STUFF
1. R8002 made NO STUFF

SCD1U10V2KX-4GP C8049 — Place under GPU

Remove 0.01u capacity C8039 2009/05/28

Change power rail 2009/05/26

[25] DGPU_HOLD_RST#
[9,21,34,36,37,64,70,76] PLT_RST#
R8039 0R2J-2-GP
PLT_RST# RC
U8028 74LVC1G08GW-1-GP (B, A, GND, VCC, Y)
+3.3V_RUN
PEX_RST#
R8017 100KR2J-1-GP
DY C8086 SC1U6D3V2KX-GP
R8016 100KR2J-1-GP

DW
07/10 Change
1. Change U8028 from Operating voltage Range 5 to 3 V . Add
2.Added Pull-down resistors on GPU Reset [PEX_REST#] Pin

+PEX_PLLVDD — PEX_PLLVDD = 120mA — +1.05V_GFX_PCIE
L8011 IND-D1UH-20-GP 100NH 0603 DCR= 0.13 ohm
C8087 SCD1U16V2KX-3GP, C8070 SC1U10V2KX-1GP, C8046 SC4D7U6D3V3KX-GP
NV suggestion. Place near GPU

Revised decoupling C 2009/05/28

Place under GPU (Pre pin)
+GPU_PLLVDD
C8071 SCD1U16V2KX-3GP, C8072 SCD1U16V2KX-3GP

Place near GPU SB-30
+1.05V_GFX_PCIE
L8005 BLM18SG121TN1D-GP
I SP_PLLVDD=45mA
C8076 SC1U10V2KX-1GP, C8075 SC4D7U6D3V3KX-GP

Revised decoupling C 2009/05/28

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Title: VGA-PCIE/LVDS(1/4)
Size: A3 | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 80 of 88

SSID = VIDEO

DW

07/05
1. LCD brightness control are separated by GPU,PCH,EC
2. LCD Power Enable control are separated by GPU,PCH,EC
3. LCD Backlight On/Off Status are separated by GPU,PCH,EC
07/10 Not Reserve
1. Shorted LBKLT_CTL_GPU,LCDVDD_EN_GPU,PANEL_BKEN_GPU Not Reserve R8134,R8135,R8136.

U8001D

SC-1204-1
add EC8101,EC8102,EC8103 for EMI

+DACA_VDD = 120mA

Place near GPU
Place under GPU
16mil
Spec 300 ohm,
ESR<0.25 ohm
Revised decoupling C 2009/05/28

U8001C

DW30 LVDS only 1 chanel
Vendor confirm tie to +1.8V powe rail

DW30 not support HDMI
NV DG: pull-down 10K

Unused IFP
Interfaces setting
2009/06/03

+IFPAB_IOVDD

IFPAB_IOVDD = 300mA
Place near GPU
Revised decoupling C 2009/05/28
Place under GPU
near IFPA_IOVDD
Place under GPU
near IFPB_IOVDD

+IFPAB_PLLVDD

Revised decoupling C 2009/05/28
Change power
rail
2009/05/28
IFPAB_PLLVDD = 220mA
Place near GPU

CLK GEN 27M select:

VGA 27M	R8123	R8131	R8125	R8132
SS	DY	POP	DY	POP
NON-SS	POP	DY	POP	DY

Remove R8112,
R8114 2009/06/09
Added CLK GEN 27M select circuit 2009/06/15
Added R8132 (DY) 2009/06/17

Default X'tal

Main 82.30034.651
Second ?
SB-19

1st: HARMONY 82.30034.651
2nd: ITTI 82.30034.801
3rd: TXC 82.30034.681

SB-30
Place near GPU
I SP_PLLVDD=45mA
Revised decoupling C 2009/05/28

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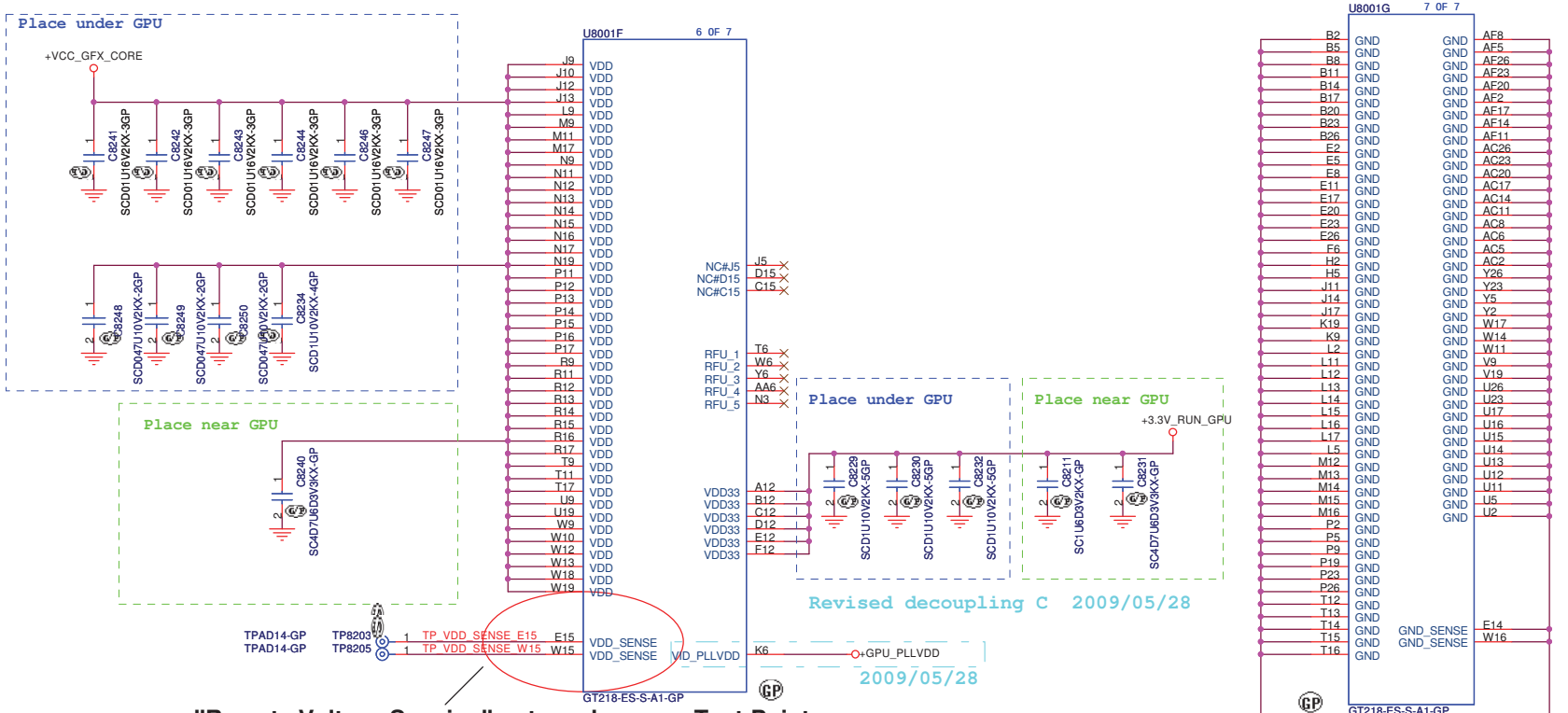
Title: VGA-LVDS/CRT/DP PORT
Size: A2
Document Number: Winery13 MB DIS
Rev: A00
Date: Wednesday, January 13, 2010
Sheet 81 of 88

SSID = VIDEO

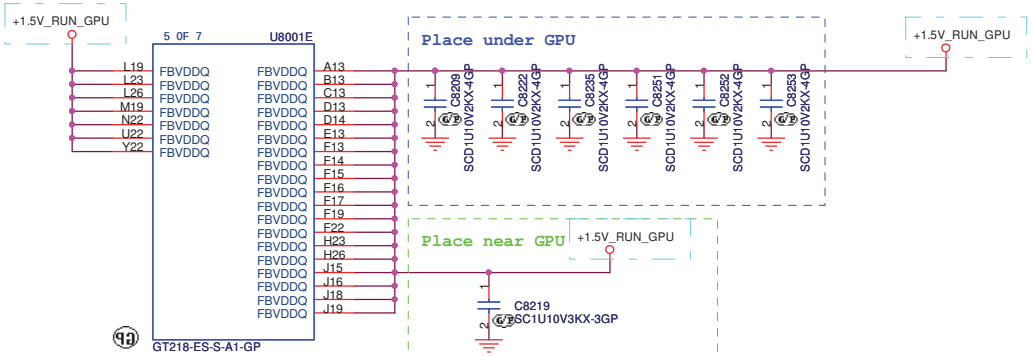
Revised decoupling C 2009/05/28



"Remote Voltage Sensing" not used,reserve Test-Point.

Change FBVDDQ power rail
2009/05/28

FBVDD/Q = 2.24A



Revised decoupling C 2009/05/28

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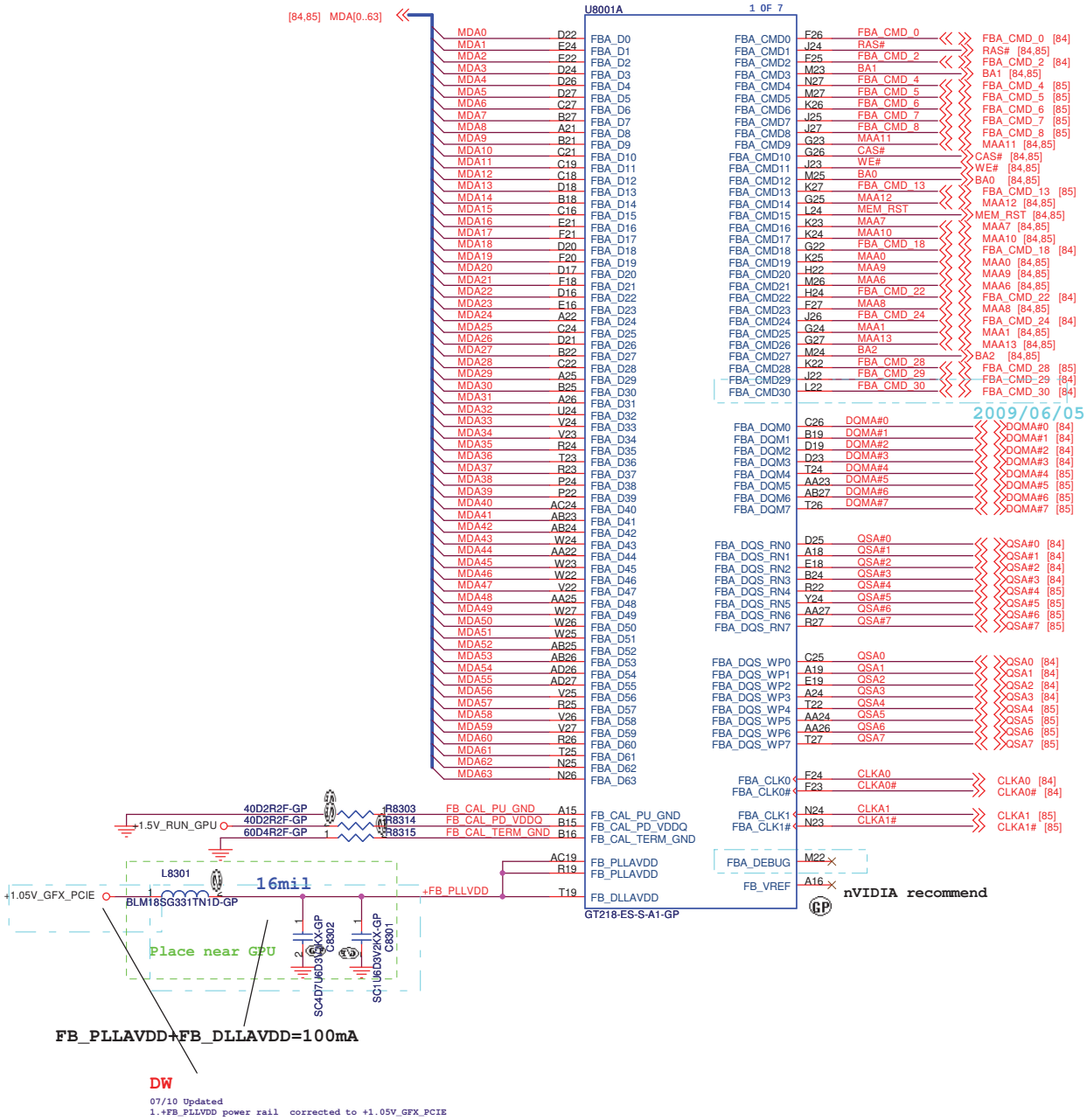
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-POWER/GND(3/4)

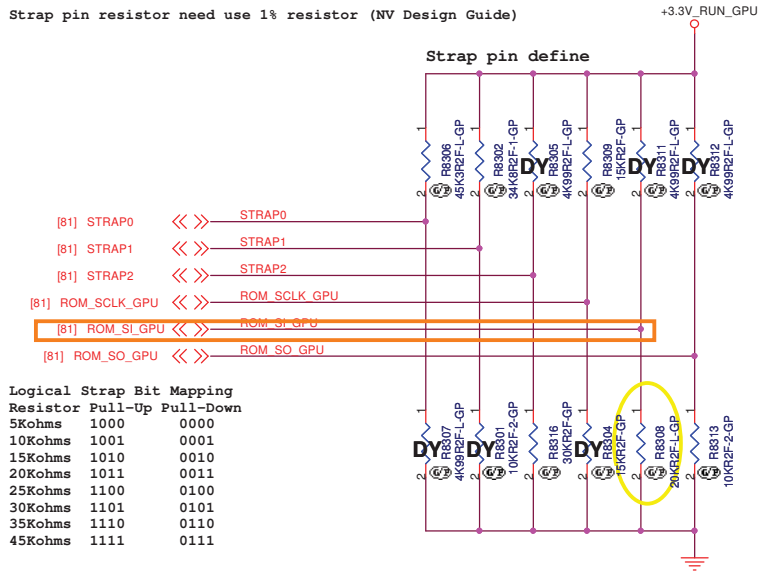
Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 82 of 88

SSID = VIDEO



Strap pin resistor need use 1% resistor (NV Design Guide)



Logical Strap Bit Mapping

Resistor	Pull-Up	Pull-Down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

Strap0		Strap1		Strap2	
USER_BIT0	1	3GIO_PADCFG_LUT_ADR0	0	PCI_DEVID_0	1
USER_BIT1	1	3GIO_PADCFG_LUT_ADR1	1	PCI_DEVID_1	0
USER_BIT2	1	3GIO_PADCFG_LUT_ADR2	1	PCI_DEVID_2	1
USER_BIT3	1	3GIO_PADCFG_LUT_ADR3	1	PCI_DEVID_3	0
EDID is used		Reserved		N11M-GE1 GPU Device ID=0x0A75	

ROM_SI_GPU		ROM_SO_GPU		ROM_SCLK_GPU	
RAM_CFG0		VGA_DEVICE	1	PEX_PLL_EN_TERM	0
RAM_CFG1		SMB_ALT_ADDR	0	SLOT_CLK_CONFIG	1
RAM_CFG2		FB_0_BAR_SIZE	0	SUB_VENDOR	0
RAM_CFG3		XCLK_417	0	PCI_DEVID_4	1

Default setting: SAMSUNG sDDR3 64Mx16BIT-->20K pull down (0x0011)
If use Hynix sDDR3 64Mx16BIT(0x0010), R8308 change to 15K.

RAM_CFG[3:0]	Config	FB_BUS Width	Definitions
0000			
0001			
0010	64MX16	DDR3 64Bit	Hynix
0011	64MX16	DDR3 64Bit	Samsung
0100			Default
0101			
0110			
0111			

SUB_VENDOR		XCLK_417		PEX_PLL_EN_TERM	
0	No VBIOS ROM	0	277MHz(POR)	0	Disable (POR)
1	BIOS ROM present	1	Reserved	1	Enable

3GIO_PADCFG	USER[3:0]
0000	Desktop
1110	Notebook (POR)

1111 Use EDID to detect panel settings

SLOT_CLOCK_CFG
0 GPU and MCH do not share a common reference clock
1 GPU and MCH share a common reference clock (POR)

1st Samsung

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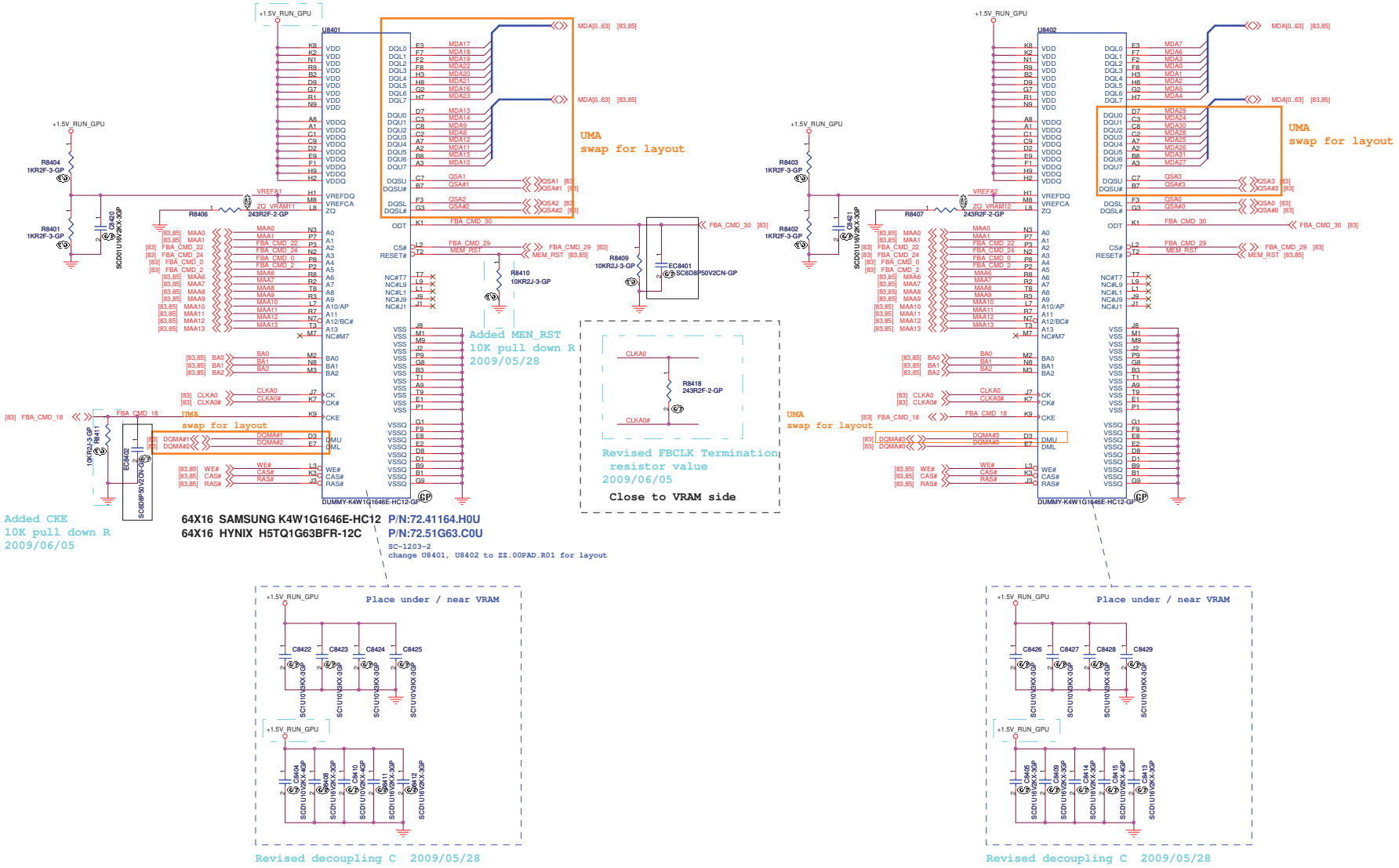
Title: VGA-MEMORY/STRAPS(4/4)
Size: A3 | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 83 of 88

SSID = VIDEO



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Title: **VRAM(1/2)**

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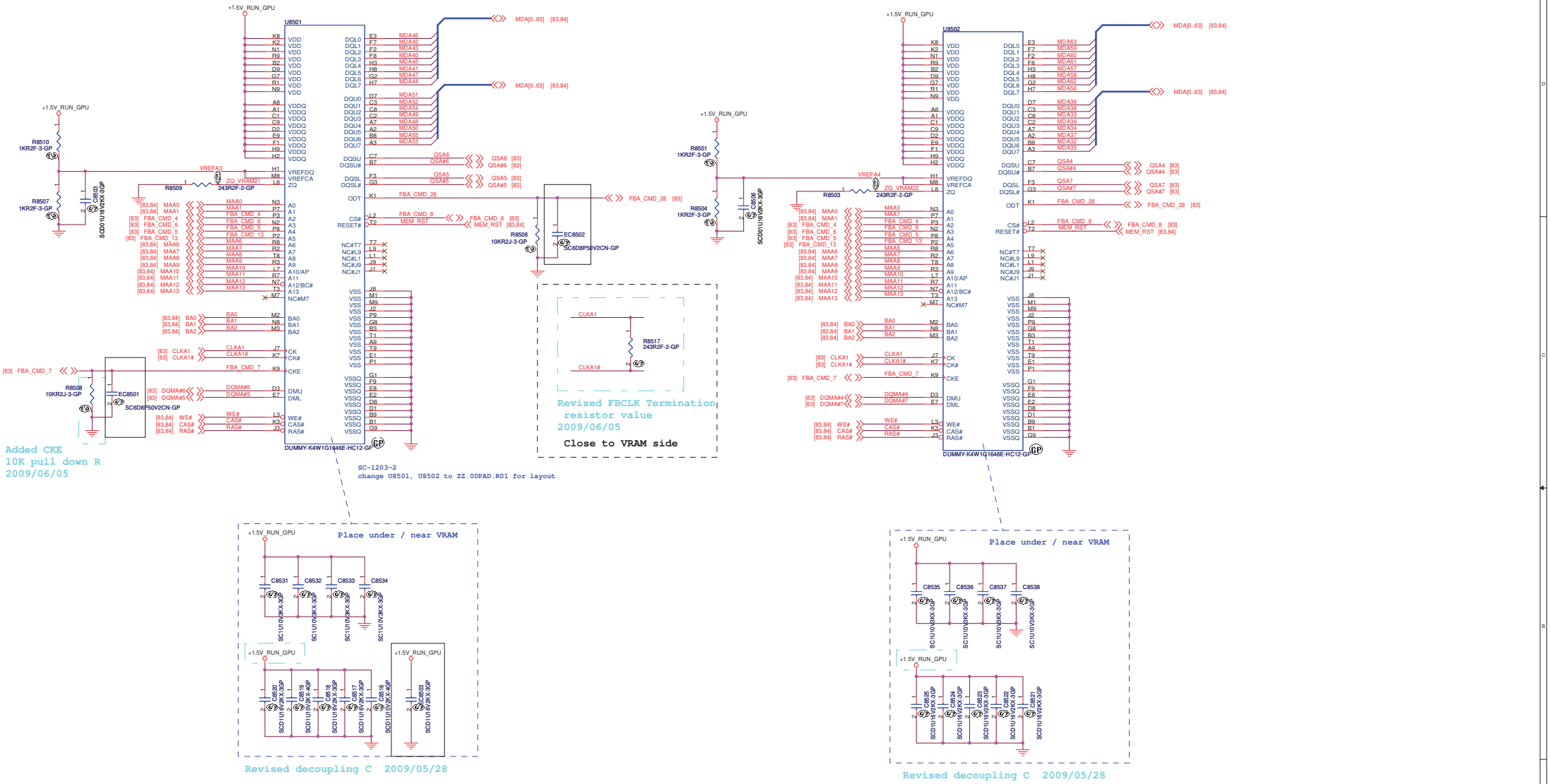
SSID = VIDEO



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Title	VRAM	
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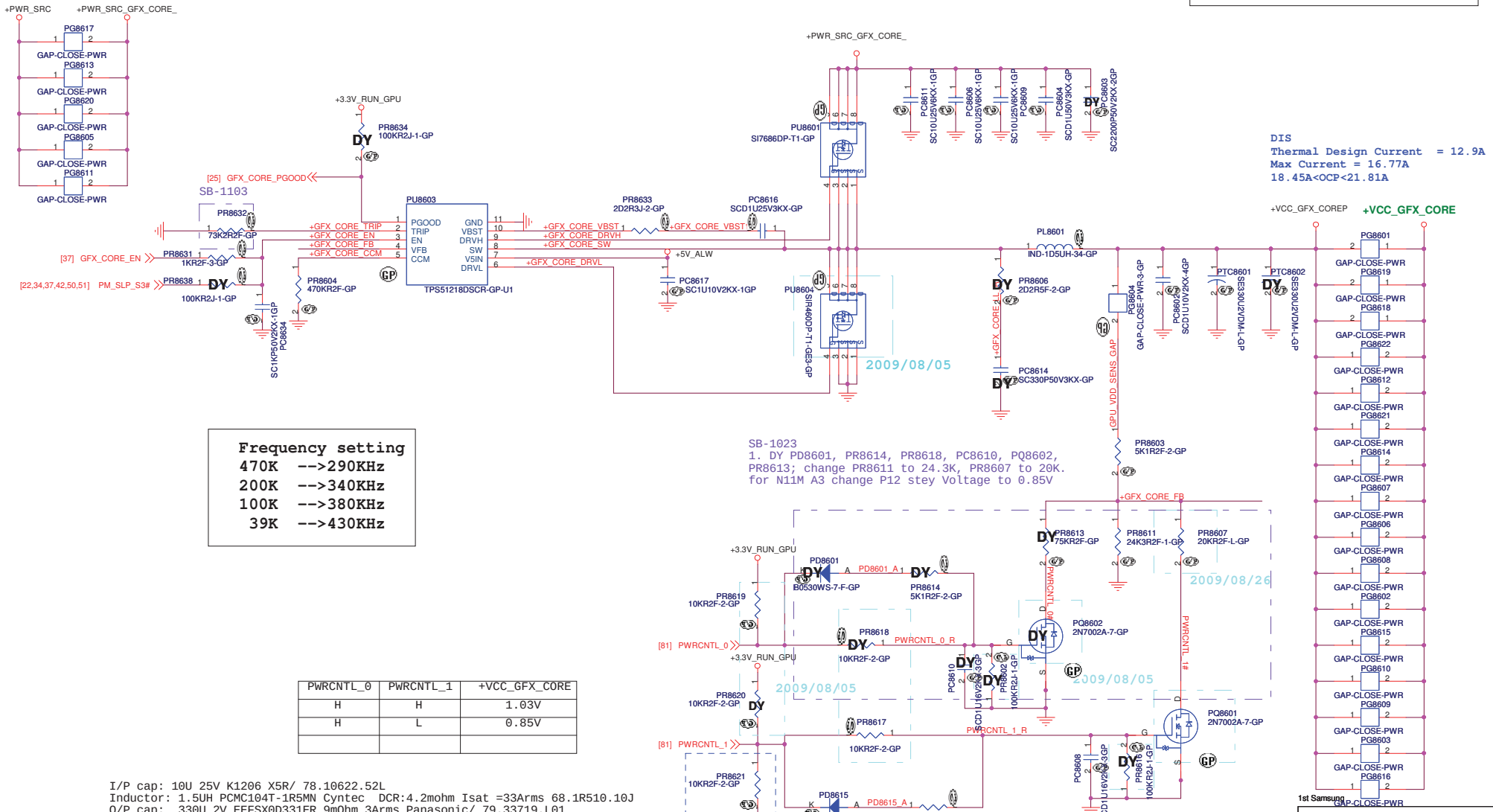
SSID = PWR.Plane.Regulator_GFX

Vout=0.704V*(R1+R2)/R2



DIS
Thermal Design Current = 12.9A
Max Current = 16.77A
18.45A<OCP<21.81A

2009/08/05

2009/08/26

2009/08/05

2009/08/05

SB-1023
1. DY PD8601, PR8614, PR8618, PC8610, PQ8602, PR8613; change PR8611 to 24.3K, PR8607 to 20K. for N11M A3 change P12 stey Voltage to 0.85V

Frequency setting

470K	-->290KHz
200K	-->340KHz
100K	-->380KHz
39K	-->430KHz

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	1.03V
H	L	0.85V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->350KHz

SC-1204-5
add PR8621 pull low 10K R

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Title: TPS51218 +VCC_GFX_CORE

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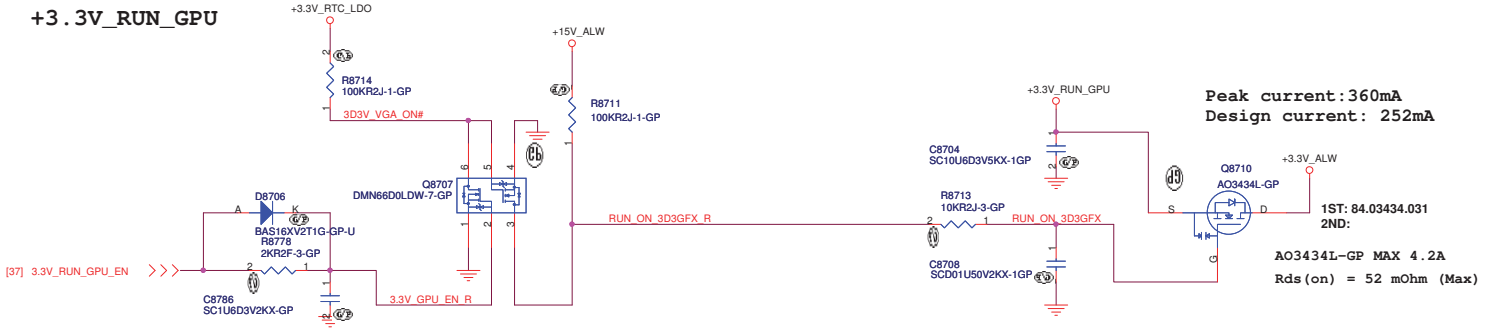
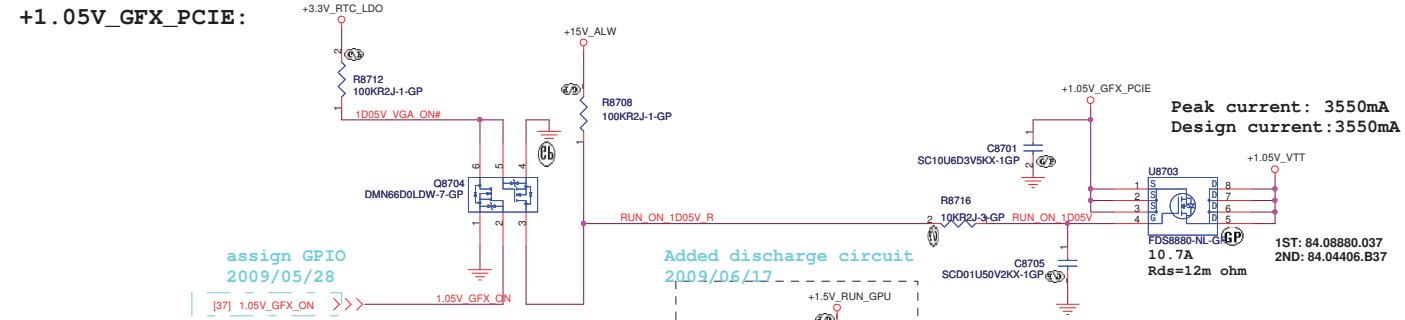
SSID = VIDEO

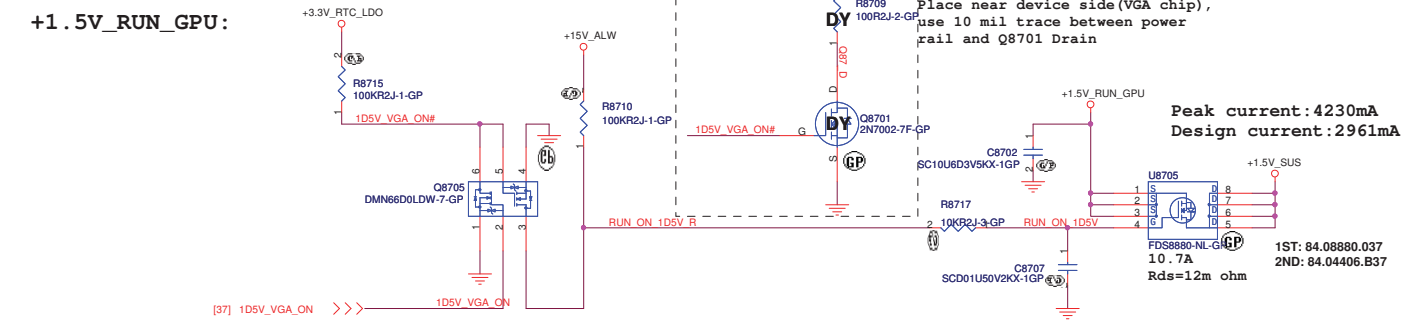
+3.3V_RUN_GPU



+1.05V_GFX_PCIE:



+1.5V_RUN_GPU:



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Title	LDO 1.8V	
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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
01	66	2009/10/08	EE	HDD LED light in S5.	Change HDD LED power rail from +5V_ALW to +5V_RUN.	SB
02	60	2009/10/08	EE	External MIC NG.	Add caps C6014 C6015.	SB
03	66	2009/10/08	EE	Correct battery LED color.	Swap LED6601 pin2 & pin3.	SB
04	49	2009/10/08	EE	Improve VTT_PWRGD ramp up signal.	Dummy C4912.	SB
05	51	2009/10/08	EE	Fine tune +1.8V_RUN power on sequence behind +3.3V_RUN.	Change PR5102 from 2.2K to 3K and PC5105 from 4700pF to 1uF.	SB
06	54,78	2009/10/08	EE	For KBC ESD protect.	Add 100 ohm resistances R5413, R7803.	SB
07						
08	30	2009/10/08	EE		Change CODEC to 92HD79.	SB
09	64	2009/10/08	EE	By ME request	Change WLAN1 to 62.10043.841.	SB
10						
11	37	2009/10/09	EE	Change board ID.	Dummy R3708 and pop R3701.	SB
12	79	2009/10/12	ME	By ME request	Change H6 to ZZ.00PAD.F91	SB
13	79	2009/10/12	ME	By ME request	Change H10 to ZZ.00PAD.D41	SB
14	78	2009/10/12	ME	By ME request	Change FP1 to 20.K0315.005	SB
15	27	2009/10/12	EE	Follow Intel spec	Remove L2701, C2701, C2702; Add TP2701	SB
16	27	2009/10/12	EE	Follow Intel spec	Remove L2704, C2721, C2722; Add TP2702	SB
17	27	2009/10/12	EE	Cost down	Change L2702, L2703 to 68.10050.10Y	SB
18	24	2009/10/12	EE	XTAL Load Capacitance as Vendor suggestion	Change C2402, C2403 to 12pF	SB
19	81	2009/10/12	EE	XTAL Load Capacitance as Vendor suggestion	Change C8135, C8138 to 15pF	SB
20	26	2009/10/13	EE	Follow Intel spec	Remove L2602, C2616; Add TP2601	SB
21	26	2009/10/13	EE	Follow Intel spec	Remove L2601, C2606; Add TP2602	SB
22	37	2009/10/13	EE	Modify 10mW schematic		SB
23	79	2009/10/13	ME	By ME request	Remove H9 (BT BOSS)	SB
24	49	2009/10/13	EE	By PSE request	Change pg4910~pg4918 and pg4921 close gap to mask type	SB
25	73	2009/10/13	EE	Two AFTP for +3.3V_RUN	Remove AFTP6030	SB
26	34	2009/10/14	ME	By ME request	change NEW1 connector to 20.K0370.026	SB
27	79	2009/10/14	ME	By ME request	change SPR5 to 34.4F822.002	SB
28	64	2009/10/14	EE	By AFTE request	Add AFTP6402, AFTP6403	SB
29	79	2009/10/16	EE	By RF request	Add Cross Moat Caps	SB
30	80,81	2009/10/16	EE	Voltage Drop over 3%	change bead value to 120 ohm DCR 0.55 ohm	SB
31	22	2009/10/16	EE	RTC data loss	Added 3v/5v S5 power good to control resume reset sequence prevent RTC data loss	SB
32	25	2009/10/16	EE		Swapped Q2515 C,E Pin	SB
33	78	2009/10/16	EE		remove CAPA_RST# from capacity board	SB
34	37	2009/10/16	EE	By SW request	Added Switch Baord Detection circuit	SB

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Title: Change List(1/3)

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
01	37	2009/11/18	EE	Correct R3745 power rail to KBC_PWR	Change R3745 power rail to KBC_PWR	SC
02	36	2009/11/25	EE	TPM connector needn't AFTE test point	Remove TPM1 AFTP	SC
03	23	2009/11/25	EE	No support HDMI and eDP so needn't pop 25MHz Xtal of PCH.	C2313 pop 0 ohm if no use 25MHz XTAL	SC
04	37	2009/11/25	EE	Toggle VGA mode will flicker white screen in hybrid mode.	Add U3703 mux for panel backlight enable signal select	SC
05	54	2009/11/25	EE	Toggle VGA mode will flicker white screen in hybrid mode.	Add mux U5446 to select LCDVDD enable signal	SC
06	7	2009/11/30	RF	For solve WiMAX noise	Change C701 to 4.7pF for RF	SC
07	43	2009/11/30	RF	For solve WiMAX noise	Pop PC4303 for RF	SC
08	46	2009/11/30	RF	For solve WiMAX noise	Change PC4601 pull up to +5V_ALW for layout.	SC
09	47	2009/11/30	EE	For combine material item	Change PC4762 to 0603 size	SC
10	79	2009/11/30	ME	For one hand hold issue, ODD have noise	Add H15 for ME	SC
11	79	2009/11/30	RF	For solve WWAN noise	Add RC7931 for RF	SC
12	79	2009/11/30	RF	For solve WiMAX noise	Add SPR6 for RF	SC
13	55	2009/12/04	EMI	By EMI requirement	Change L5501,L5502,L5503 for EMI	SC
14	79	2009/12/04	EMI	By EMI requirement	Add EMI caps	SC
15	81	2009/12/04	EMI	By EMI requirement	Add EC8101,EC8102,EC8103 for EMI	SC
16	47	2009/12/04	ME	For cosmatic issue when insert 8 cell battery	Remove TC4701 for layout	SC
17	79	2009/12/04	ME	For cosmatic issue when insert 8 cell battery	Change H2 to ZZ.00PAD.D11	SC
18	30	2009/12/04	EE	Base on Application Note: IDT 92H81/79 AUX Mode as input of Diagnostic sound.	Connect U3001 pin17, pin18 to pin12 net and change R3016 to 120K for vendor request	SC
19	86	2009/12/04	EE	Set PWRCNTL_1 for default low.	Add PR8621 pull low 10K ohm	SC
20	12	2009/12/07	EMI	By EMI requirement	Pop C1243 and change size to 0603 for EMI	SC
21	33	2009/12/07	EMI	By EMI requirement	Pop C3301, EC3302, EC3303, EC3305, EC3306, EC3307, EC3308 and change from 100p to 6.8p for EMI	SC
22	54	2009/12/07	EMI	By EMI requirement	Pop EC5403 for EMI	SC
23	60	2009/12/07	EMI	By EMI requirement	Pop EC6001 and EC6002 for EMI	SC
24	63	2009/12/07	EMI	By EMI requirement	Pop R6307 for EMI	SC
25	79	2009/12/07	ME	For cosmatic issue when insert 8 cell battery	Add H16 for ME	SC
26	24	2009/12/08	EE	Base on EA teset result, change to 0 ohm.	Change R2413,R2414,R2415 from 15ohm to 0 ohm	SC
27	53	2009/12/08	EE	Base on ARD_Sightings_Report_18 #3622146	Change PR5311 from 4.7K to 470 ohm	SC
28	60	2009/12/08	EE	Audio AP LO THD+N fail	Change EC6004,EC6005 from 0.1U to 0.01U	SC
29	62	2009/12/08	EE	Base on EA teset result, change to 0 ohm.	Change R6206 from 15ohm to 0 ohm	SC
30	68	2009/12/08	EE	Change PCB Footprint	Change Q6808 to 84.06402.B3D	SC
31	73	2009/12/08	EMI	By EMI requirement	Pop L7301 for EMI	SC

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Title: Change List(2/3)

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
01	34	2010/01/07	EE	For no co-lay after XB	remove R3402, R3403	A00
02	37	2010/01/05	EE	Prevent SPI ROM data lost	Add reset IC U3704	A00
03	46	2009/12/18	EE	By POWER requirement	changePL4602 from 2.2U to 3.3U	A00
04	46	2009/12/18	EE	TO improve +15V_Pump Power on issue	pop PR4619; dummy PR4618	A00
05	51	2010/01/07	EE	To prevent PM_SLP_S3# signal rebound	change R5102 to short pad, PC5105 to 10K	A00
06	52	2009/12/23	EE	PREVNET MOS DEMAGE	Change C701 to 4.7pF for RF	A00
07	53	2009/12/18	EE	By POWER requirement	change PR5314 from 5.9K to 6.2K	A00
08	55	2009/12/18	EMI	By EMI requirement	change L5501, L5502, L5503 to 0R	A00
09	55	2009/12/18	EMI	By EMI requirement	change R5504, R5505, R5506 from 0R to 33R	A00
10	55	2009/12/18	EMI	By EMI requirement	change C5520 from 22p to 10p	A00
11	55	2010/01/04	ME	By ME requirement	change CRT1 from 20.20431.015 to 20.20401.015	A00
12	62	2010/01/04	ME	By ME requirement	change RCT1 from 20.D0210.102 to 20.D0075.102	A00
13	63	2010/01/06	EE	For no co-lay after XB	remove R6302, R6308,TR6301,TR6302, TR6303	A00
14	64	2010/01/07	EE	For no co-lay after XB	remove L6401	A00
15	73	2010/01/07	EE	For no co-lay after XB	remove R7302, R7303	A00
16	78	2009/12/23	EE	TO PREVENT power pin short to GND when plug in cable	dummy FP1 pin6, pin7	A00
17	78	2009/12/23	EE	add damping resister R7804	add R7804	A00
18	79	2010/01/05	ME	By ME requirement	change SPR5 from 34.4F822.002 to 34.42T14.002	A00

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Title: *Change List(3/3)*

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