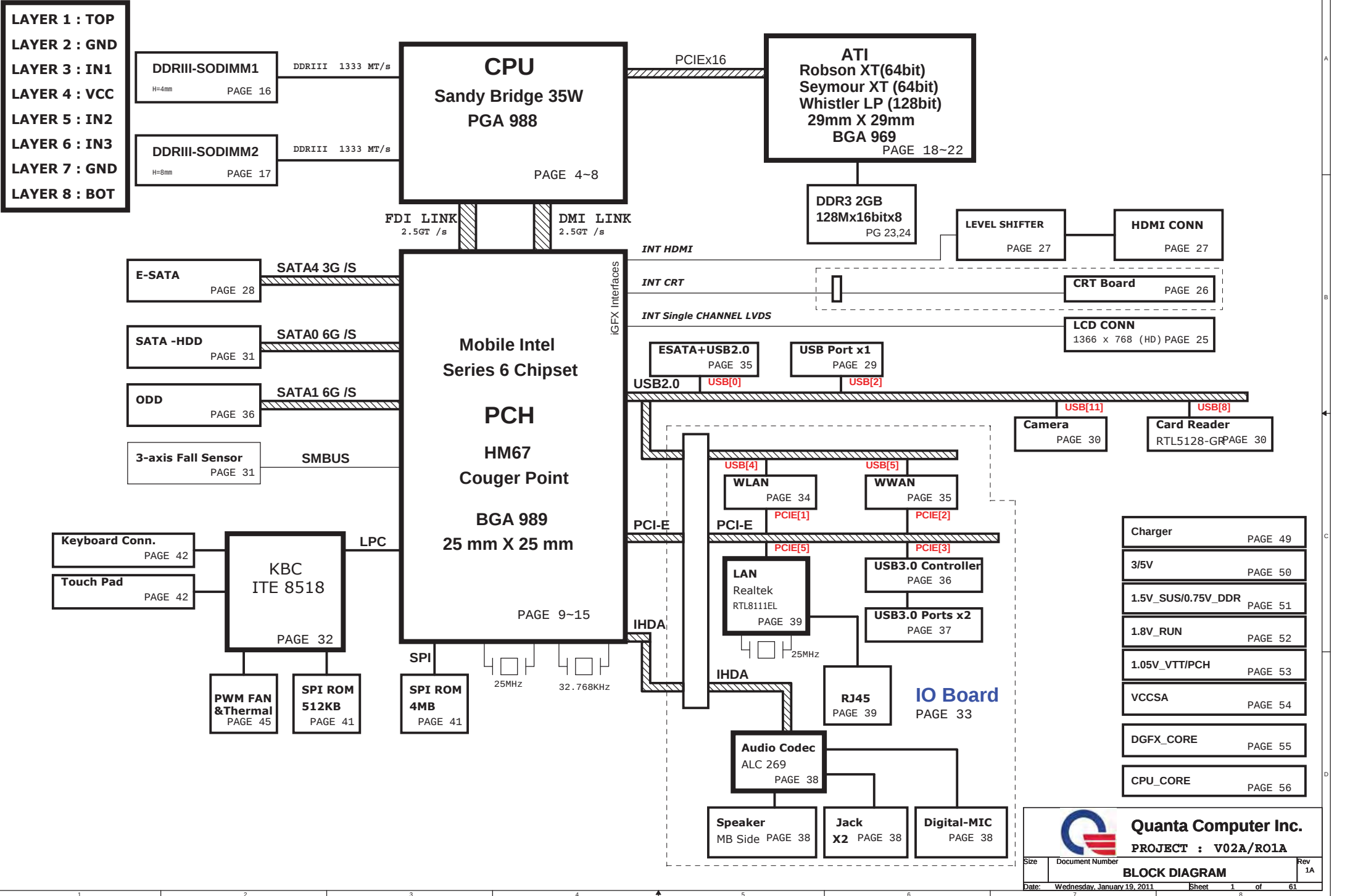


V02A/R01A DIS BLOCK DIAGRAM



power State					
S0					
S1					
S3					
S4/S5 AC					
S4/S5 DC Only					
AC/DC No Exist					

SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								

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Size

Document Number

Rev

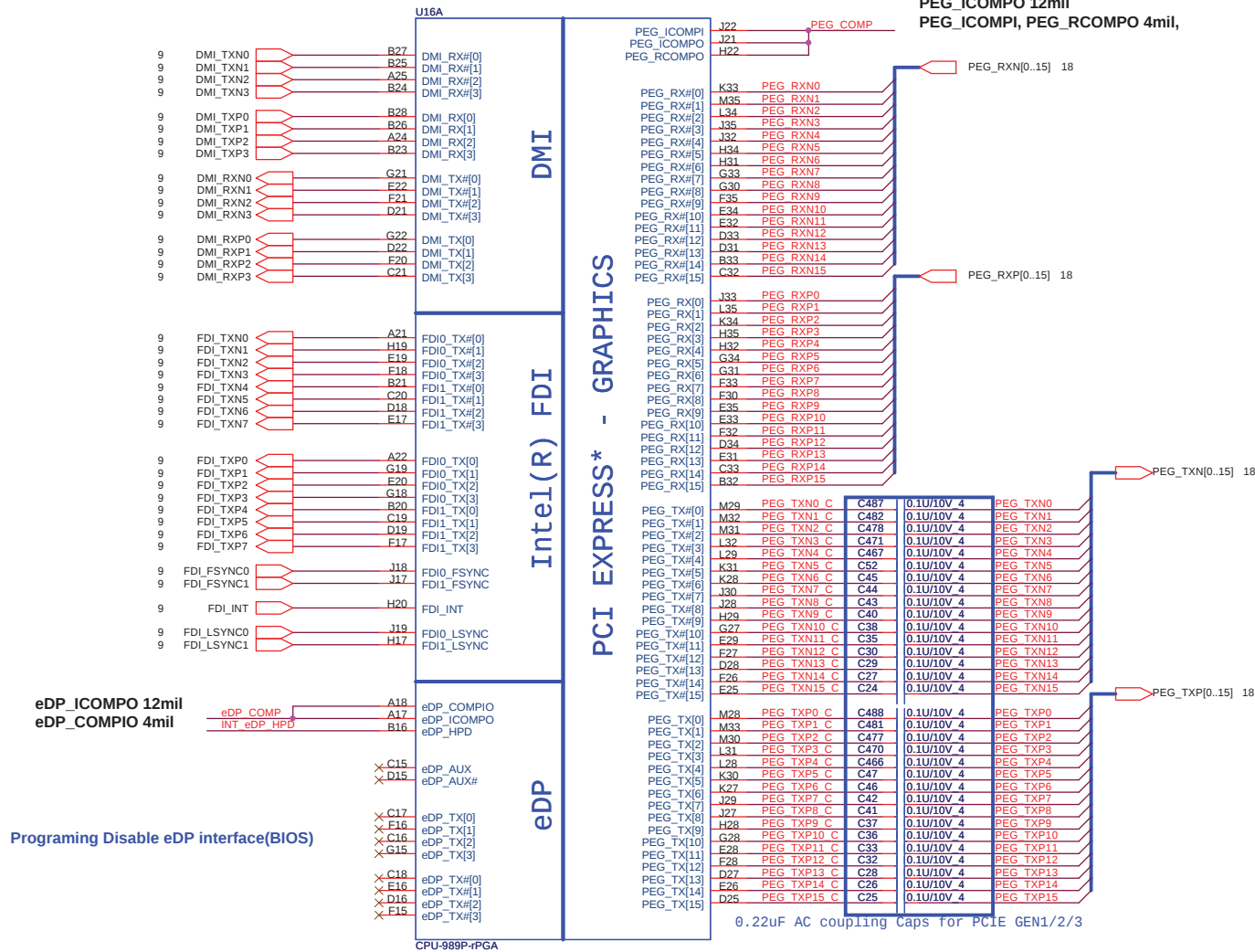
1A

BLANK

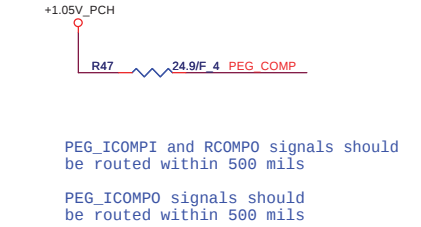
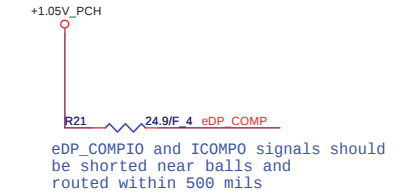
Date: Wednesday, January 19, 2011

Sheet 3 of 61

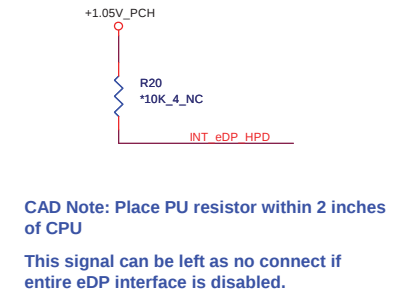
Sandy Bridge Processor (DMI, PEG, FDI)



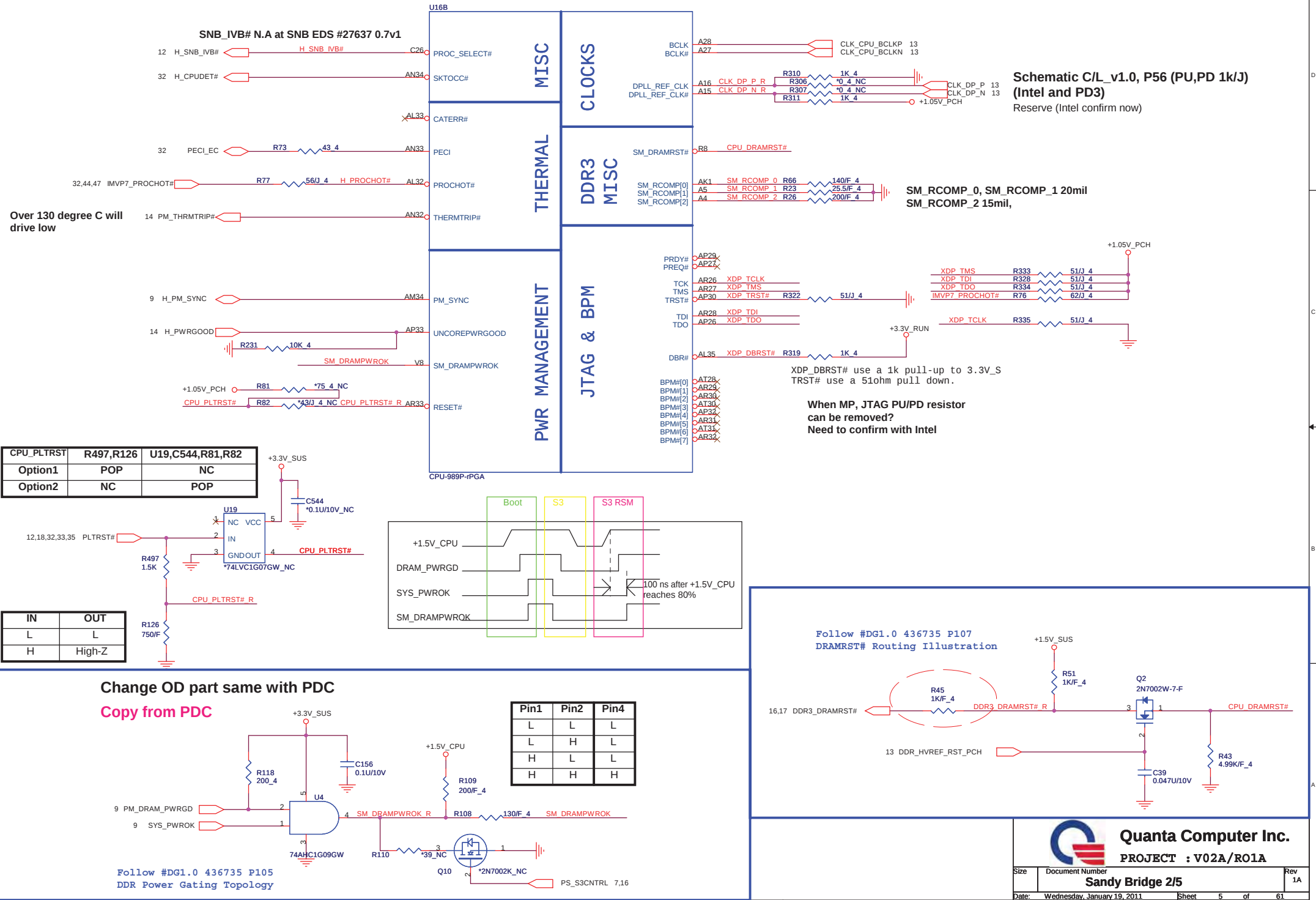
DP & PEG Compensation



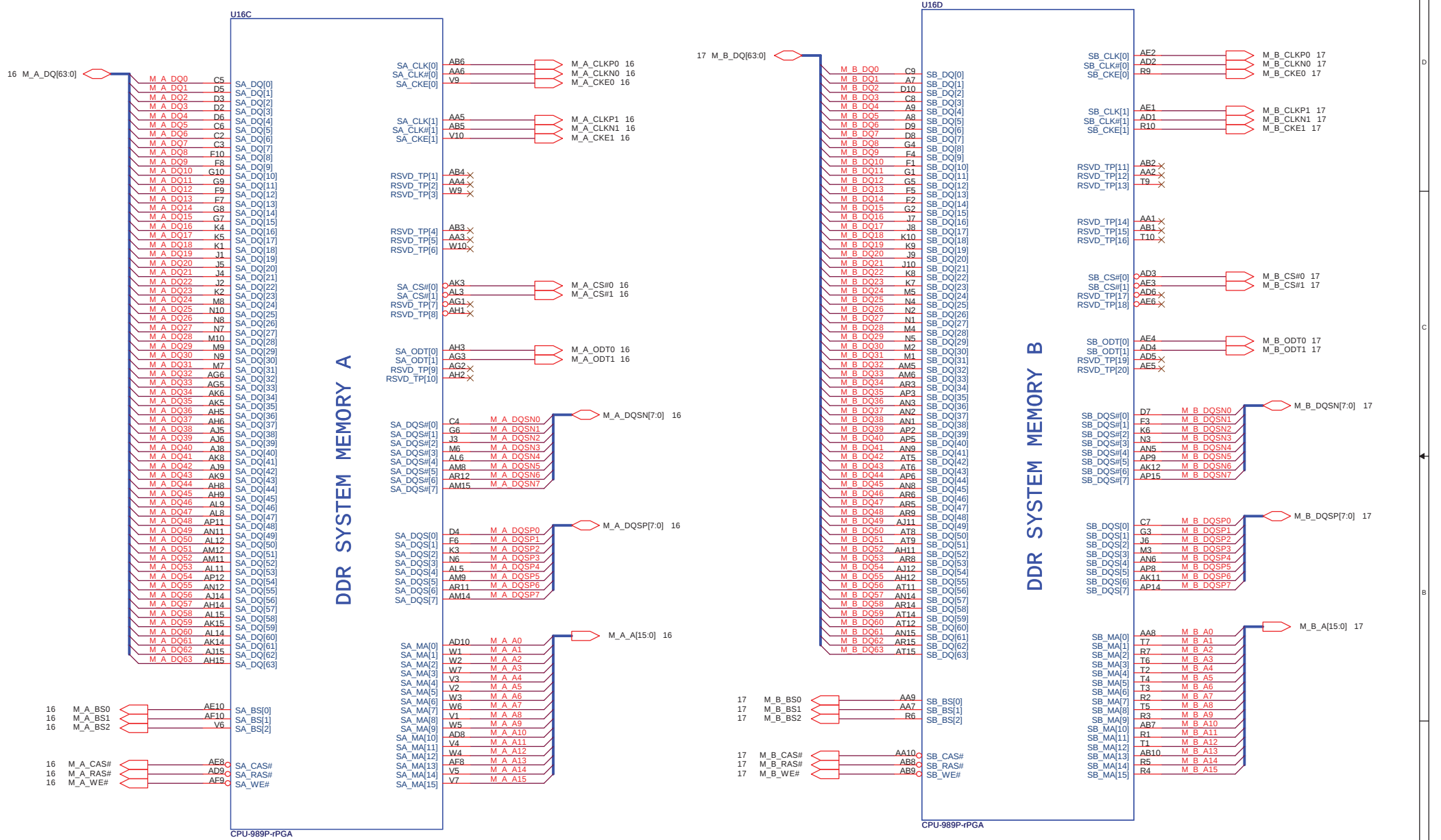
eDP Hot-plug (Disable)



Sandy Bridge Processor (CLK,MISC,JTAG)



Sandy Bridge Processor (DDR3)



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PROJECT : V02A/R01A

Sandy Bridge Processor (POWER)

POWER

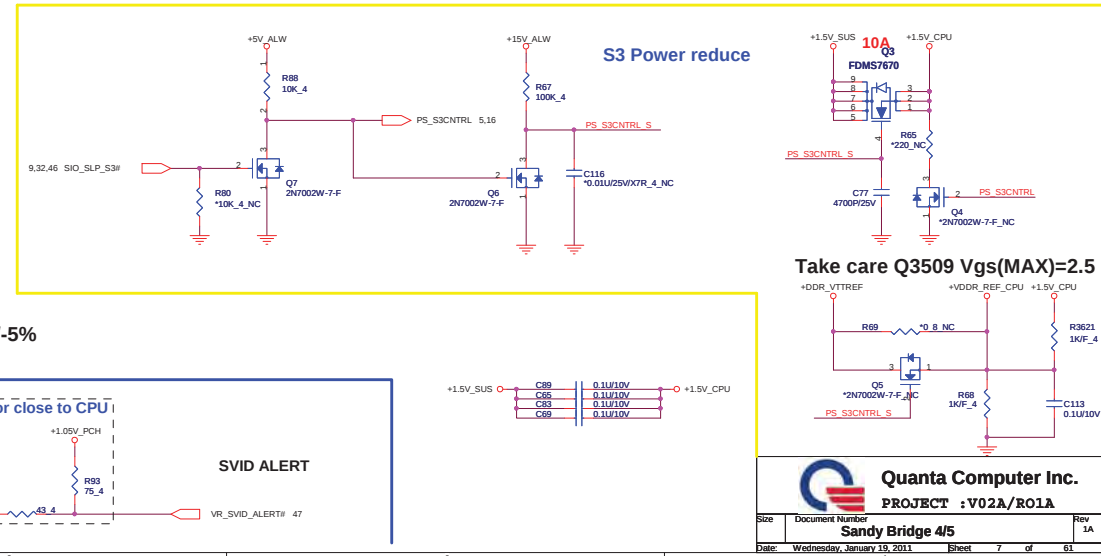
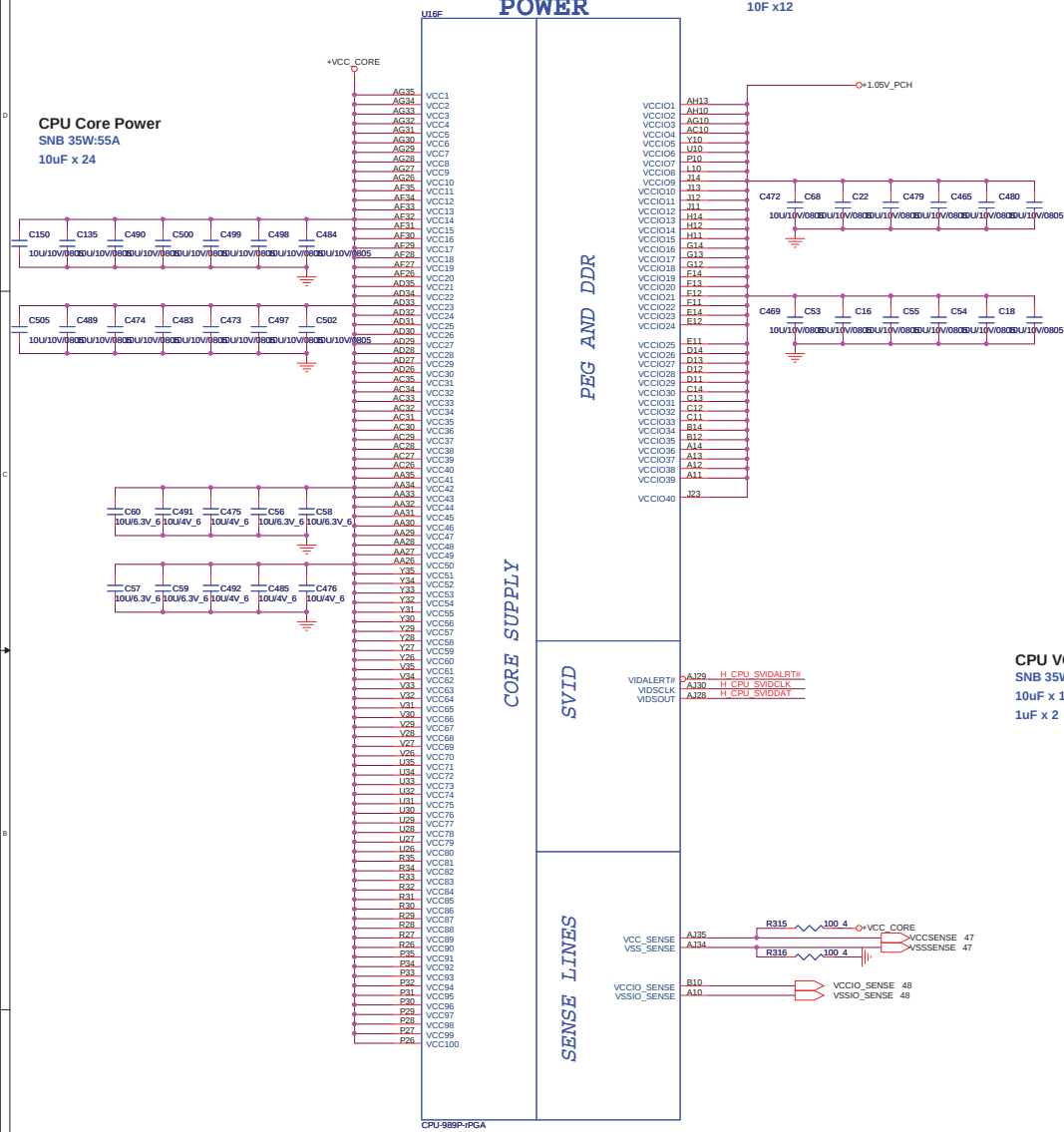
CPU Core Power
SNB 35W:55A
10uF x 24

CPU VTT
SNB 35W:8.5A
10F x12

CPU VGT
SNB 35W:22A
10uF x 12

Sandy Bridge Processor (GRAPHIC POWER)

POWER



Layout note: need routing
together and ALERT need
between CLK and DATA

SVID CLK

Place PU resistor close to CPU

SVID DATA

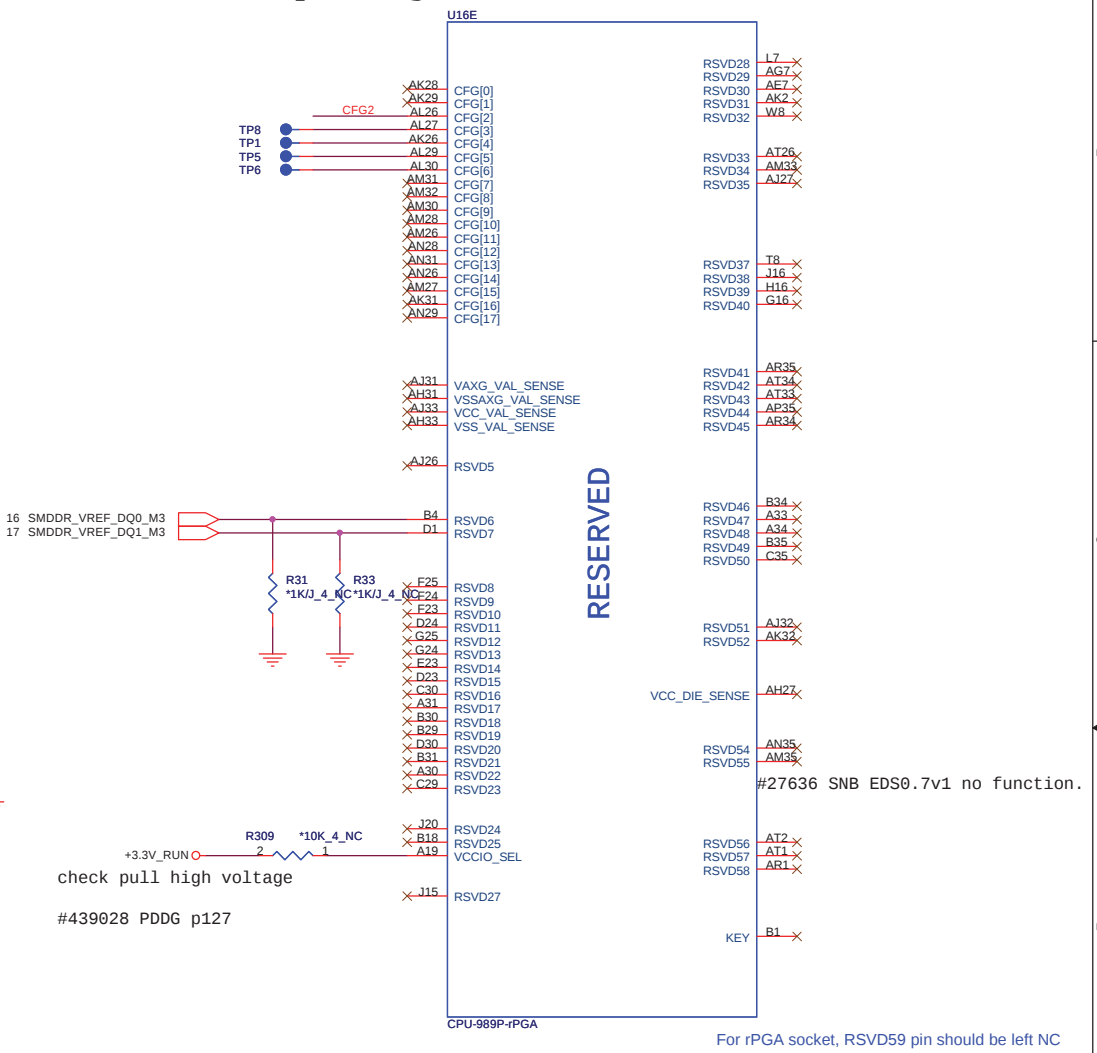
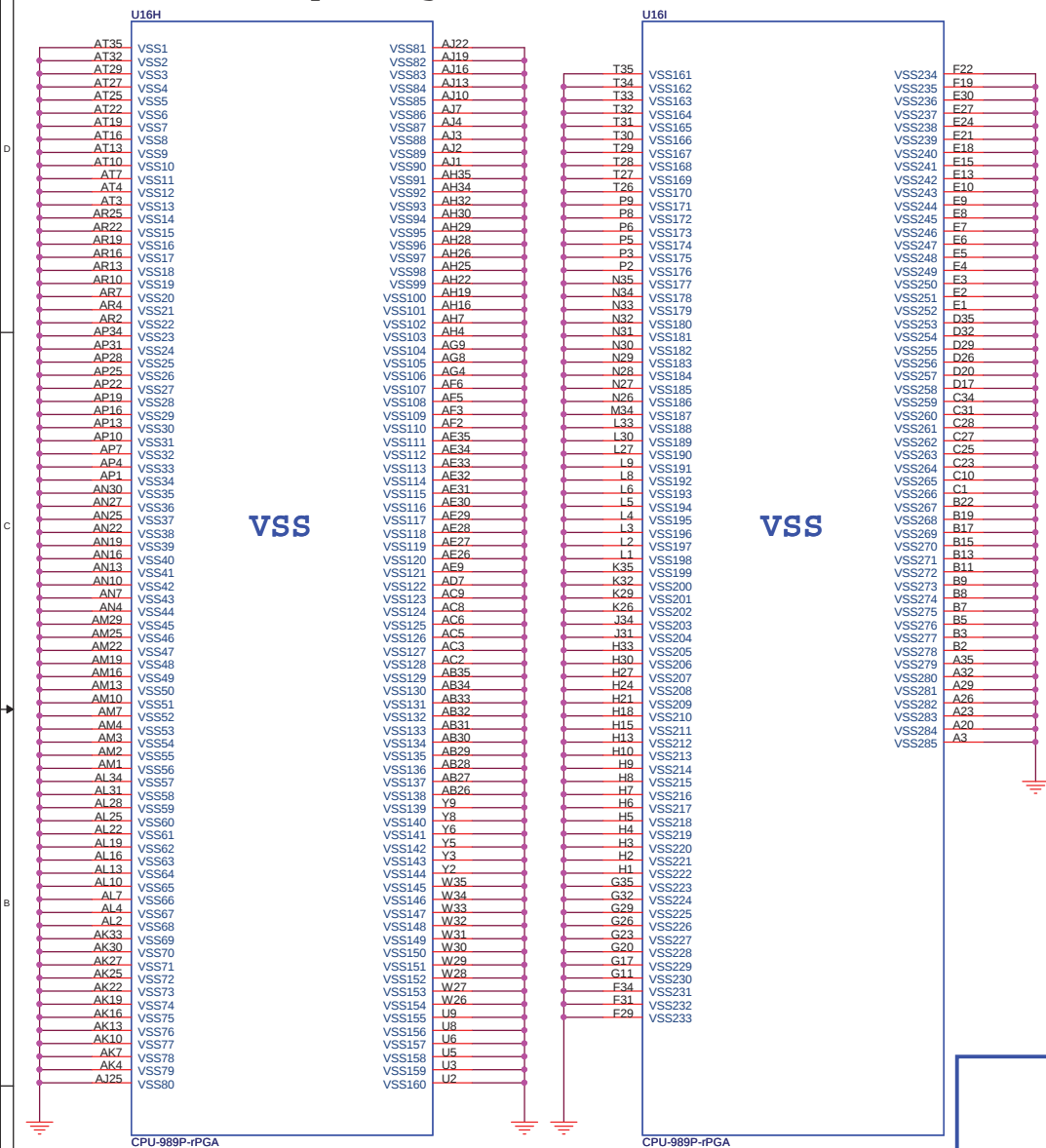
Place PU resistor close to CPU

SVID ALERT

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PROJECT : V02A/RO1A
Size Document Number
Sandy Bridge 4/5
Date: Wednesday, January 19, 2011 Sheet 7 of 61

Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

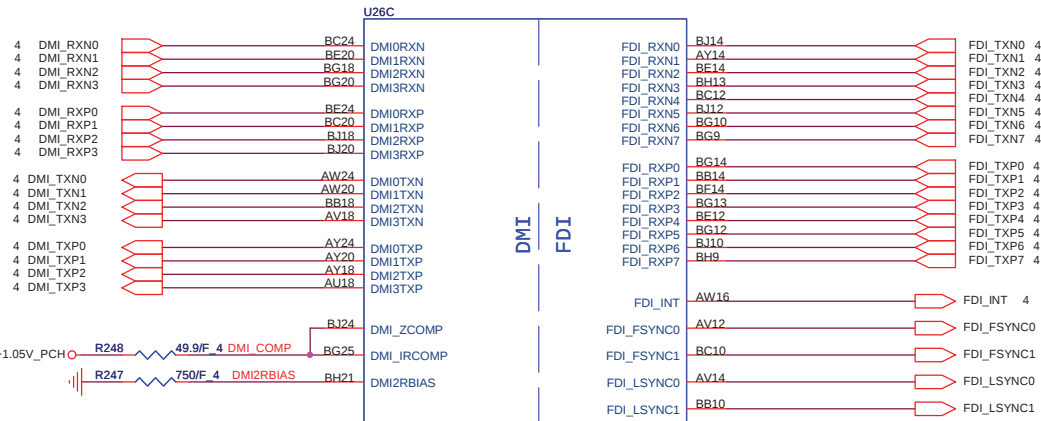
CFG2 R106 1K/F 4



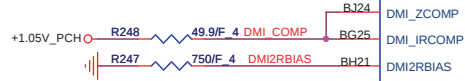
Quanta Computer Inc.
PROJECT : V02A/R01A

Cougar Point (DMI, FDI, PM)

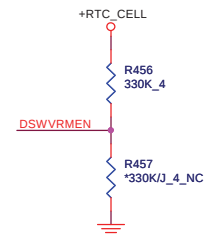
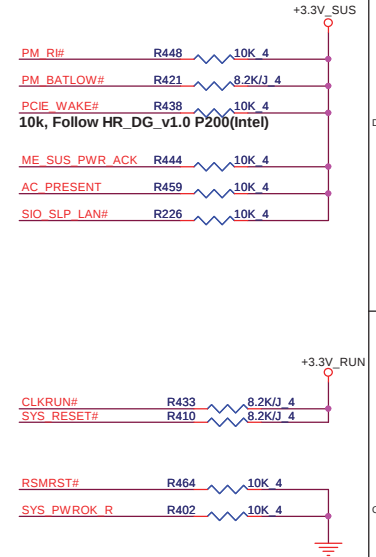
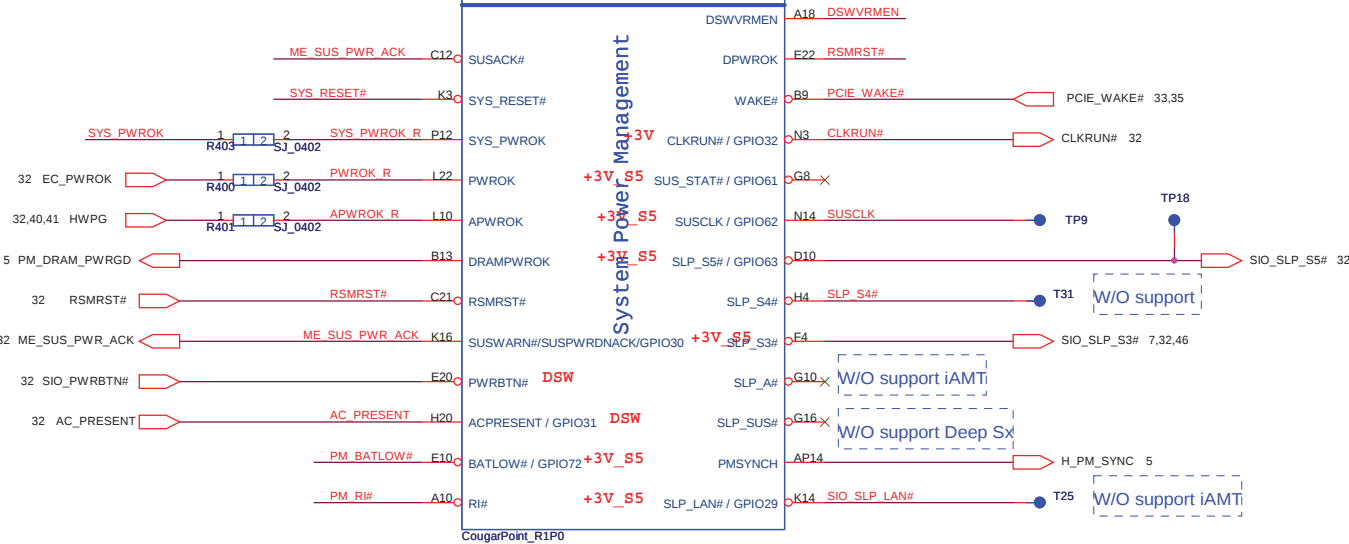
PCH Pull-high/low(CLG)



DMI_ZCOMP, DMI_IRCOMP 4mil

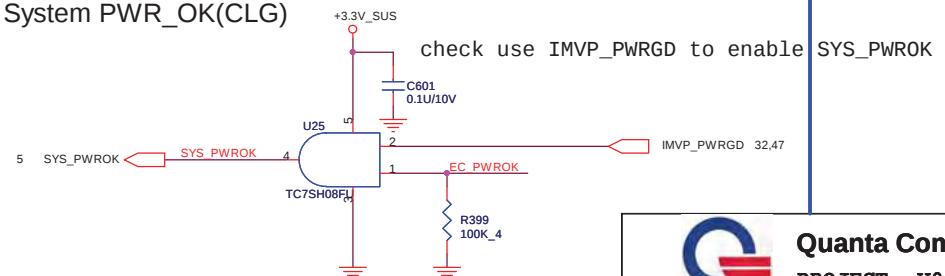


Take care of timing



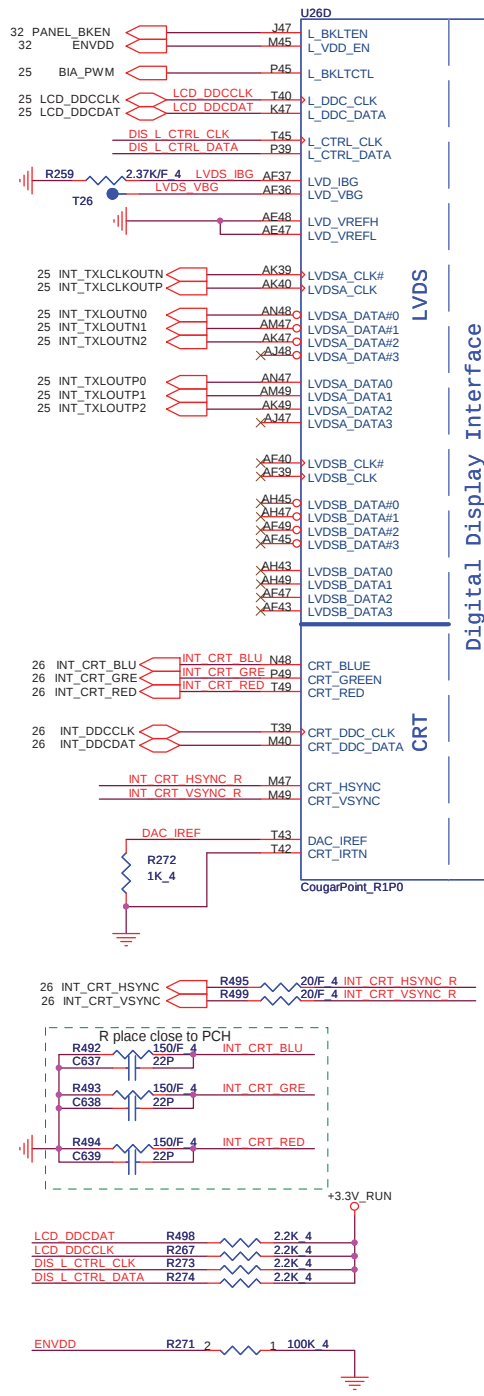
On Die DSW VR Enable
High = Enable (Default)
Low = Disable

System PWR_OK(CLG)

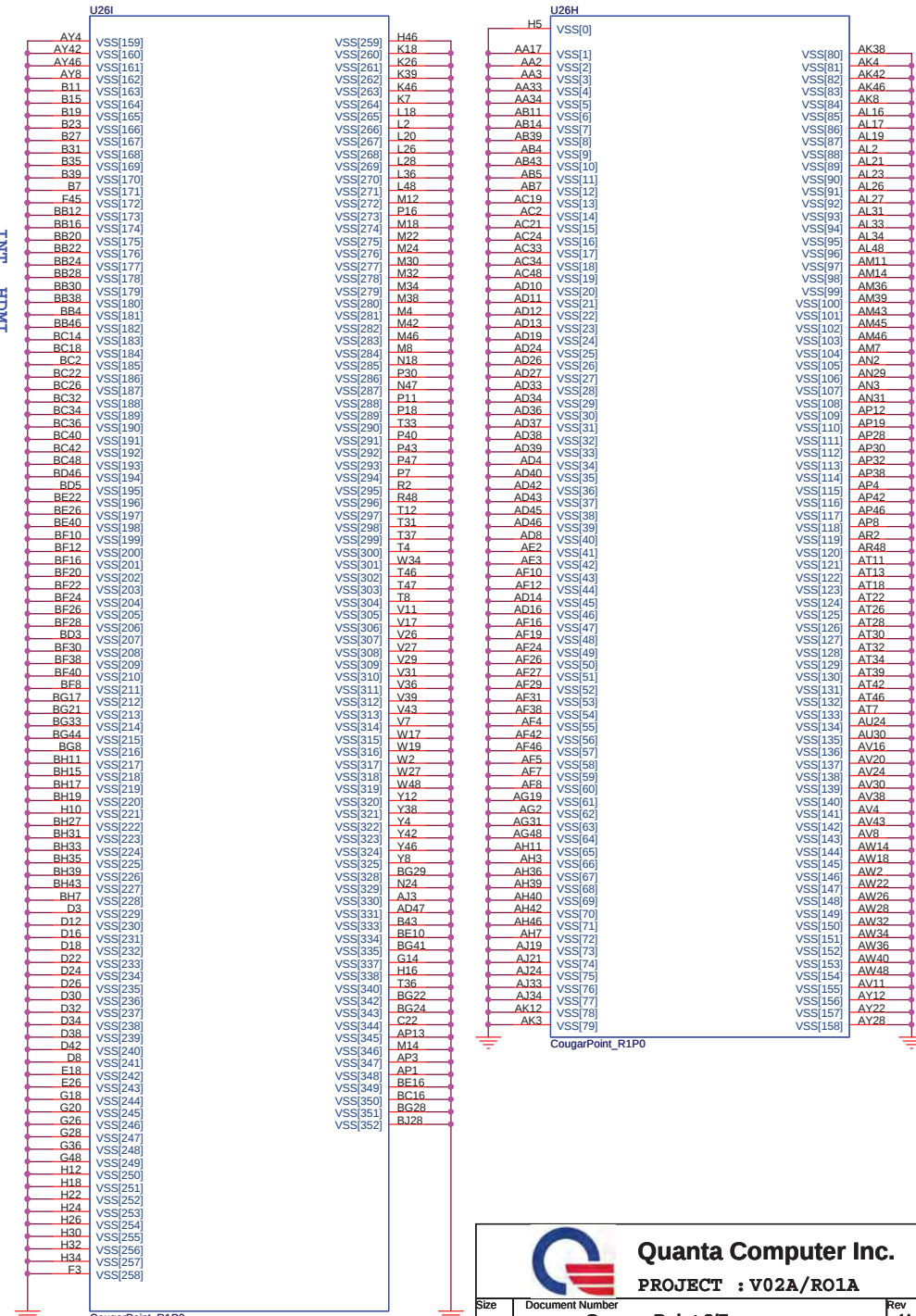


Quanta Computer Inc.
PROJECT : V02A/R01A

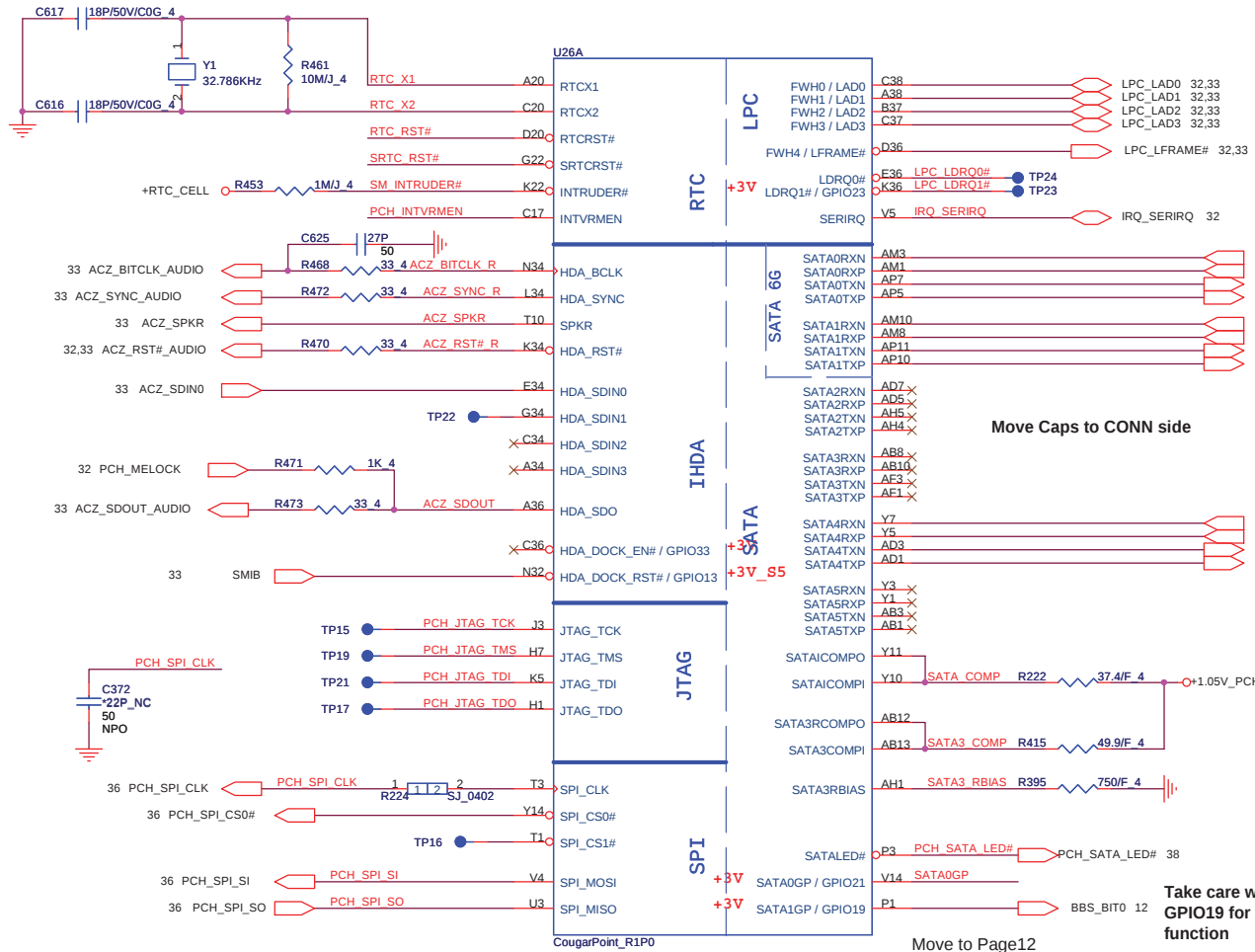
Cougar Point (LVDS, DDI)



Cougar Point (GND)

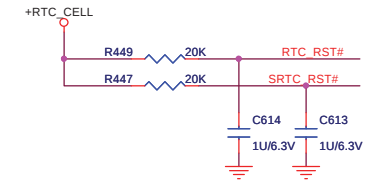
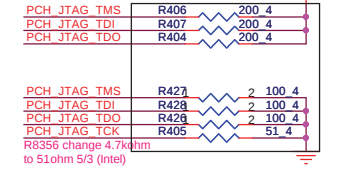


Cougar Point (HDA, JTAG, SATA)



PCH JTAG Debug (CLG)

5% fine (Intel), 210->200 (PDDG, Intel) MP remove(Intel)



SATA HDD/SSD

SATA ODD

ESATA

Move Caps to CONN side

Take care while using GPIO19 for Hot Plug function

Move to Page12

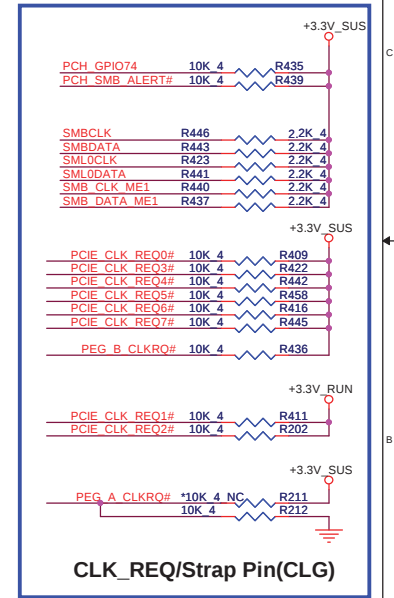
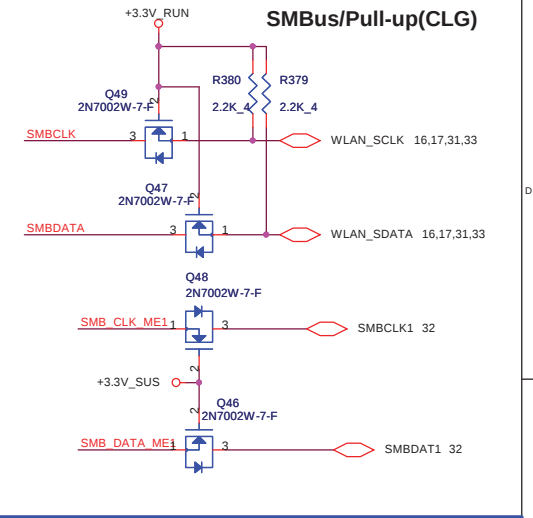
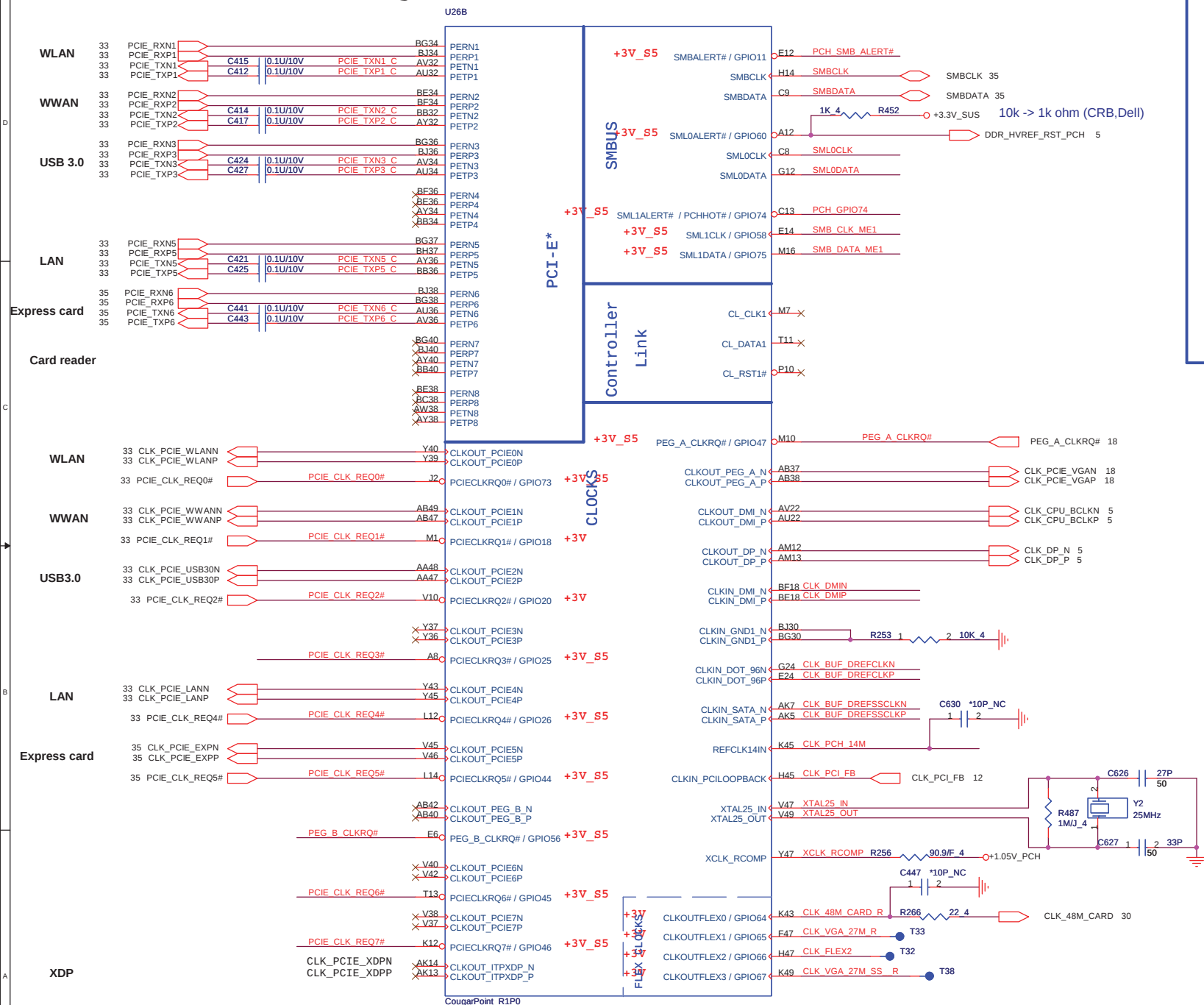
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_SUS R413 *1K 4 NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R474 *1K 4 NC ACZ_SDOUT
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R455 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R469 1K 4 ACZ_SYNC_R

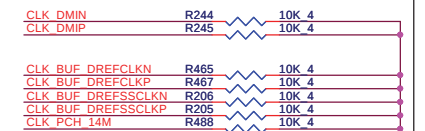


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Cougar Point-M (PCI-E, SMBUS, CLK)



Stuff for Integrated CLK Gen Mode



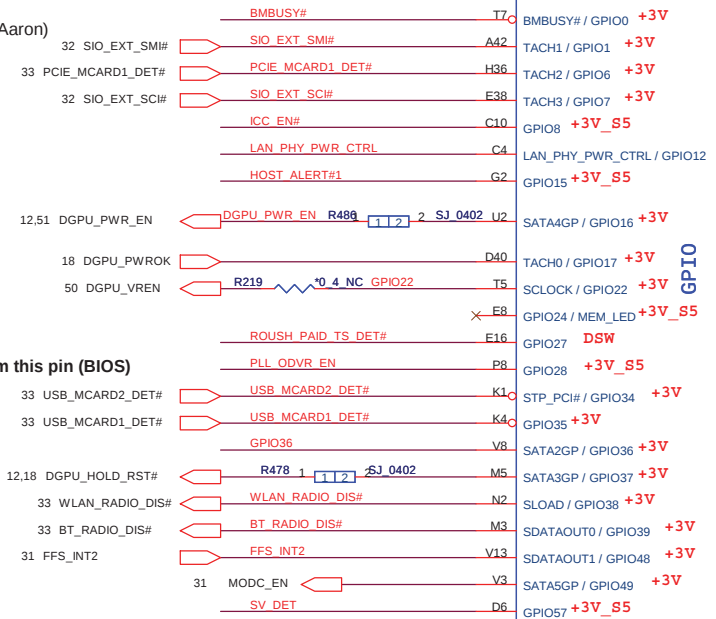
CougarPoint_R1P0	
CLKOUTFLEX0 / GPIO64	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following: • 33 / 27 / 48 / 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 / GPIO65	unsupported clock output value (Default) / 27 / 14.318 MHz output to SIO/EC / 48/24 MHz
CLKOUTFLEX2 / GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 / GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)



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Cougar Point (GPIO,VSS_NCTF,RSVD)

change to GPIO14 (Aaron)



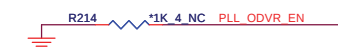
DO NOT program this pin (BIOS)

CPU/MISC

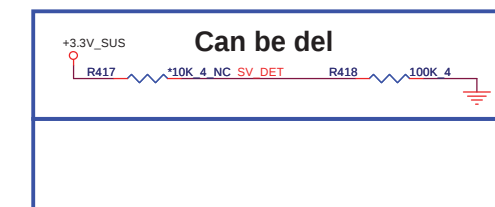
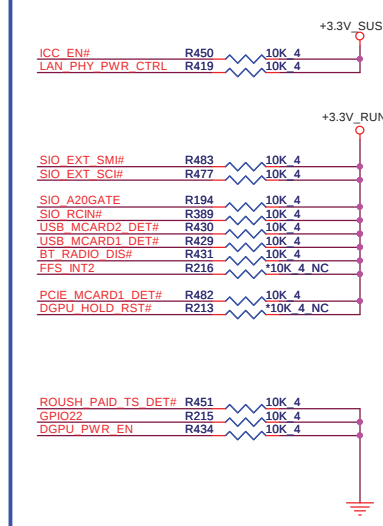
NCTF

Check When Symbol Update (OK)

Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)



GPIO Pull-up/Pull-down(CLG)



DMI TERMINATION VOLTAGE OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

GPIO36

R221 200K

+3.3V_RUN

SGPIO Confirm with Intel

BMBUSY# (Intel feedback) Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY# R220 10K 4

+3.3V_RUN

BMBUSY# (Intel feedback) Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY# If not used, require a weak pull-up (8.2- KΩ to 10 KΩ) to Vcc3_3. CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

Have to Reserve

HOST_ALERT#1 R425 1K 4

+3.3V_SUS

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (default)

High = Enable

MFG-TEST

WLAN_RADIO_DIS# R412 10K 4

+3.3V_RUN

WLAN_RADIO_DIS# R412 10K 4

Quanta Computer Inc.

PROJECT : V02A/R01A

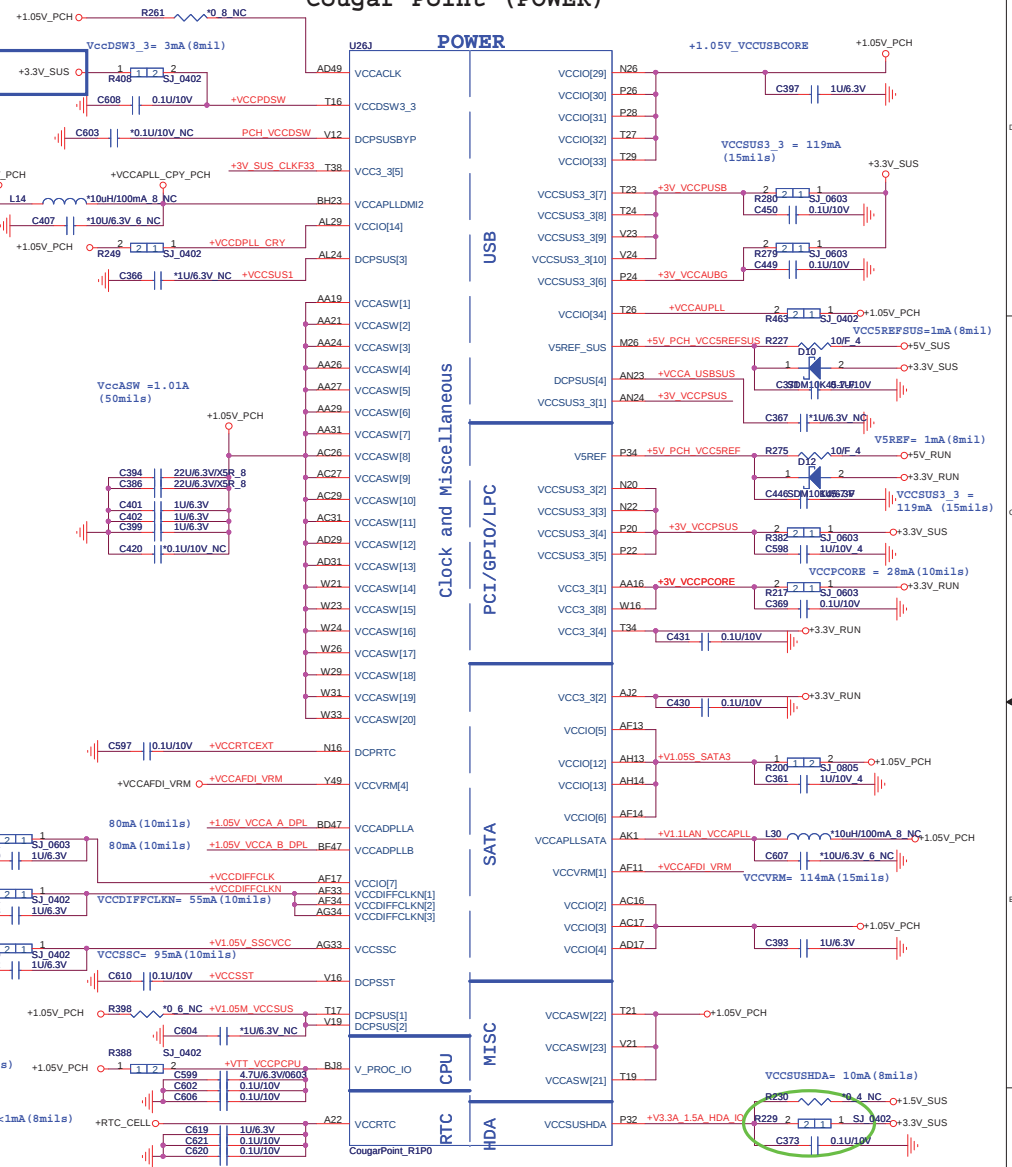
Size Document Number

Cougar Point 6/7

Date: Wednesday, January 19, 2011 Sheet 14 of 61

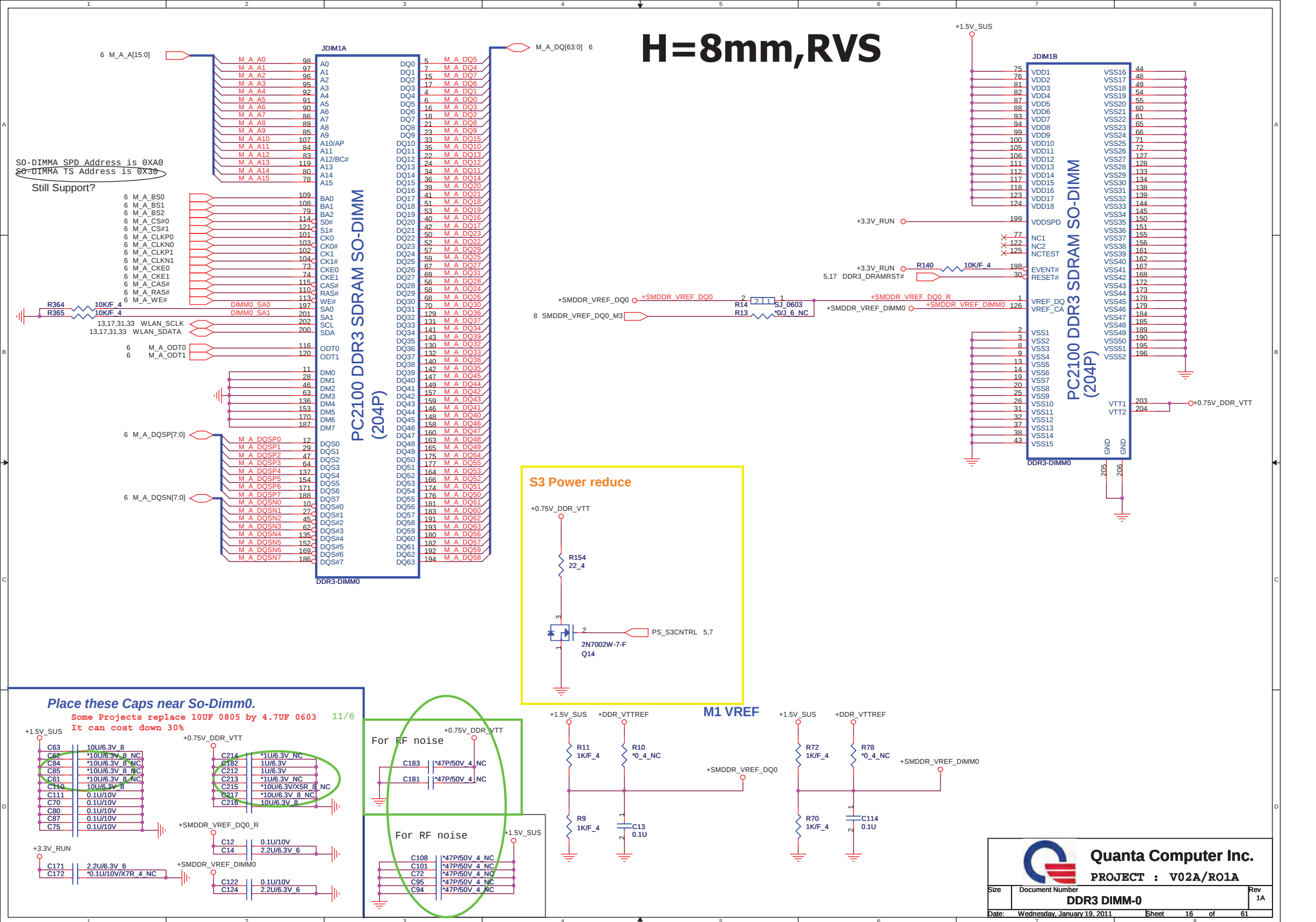
Rev 1A

Cougar Point (POWER)

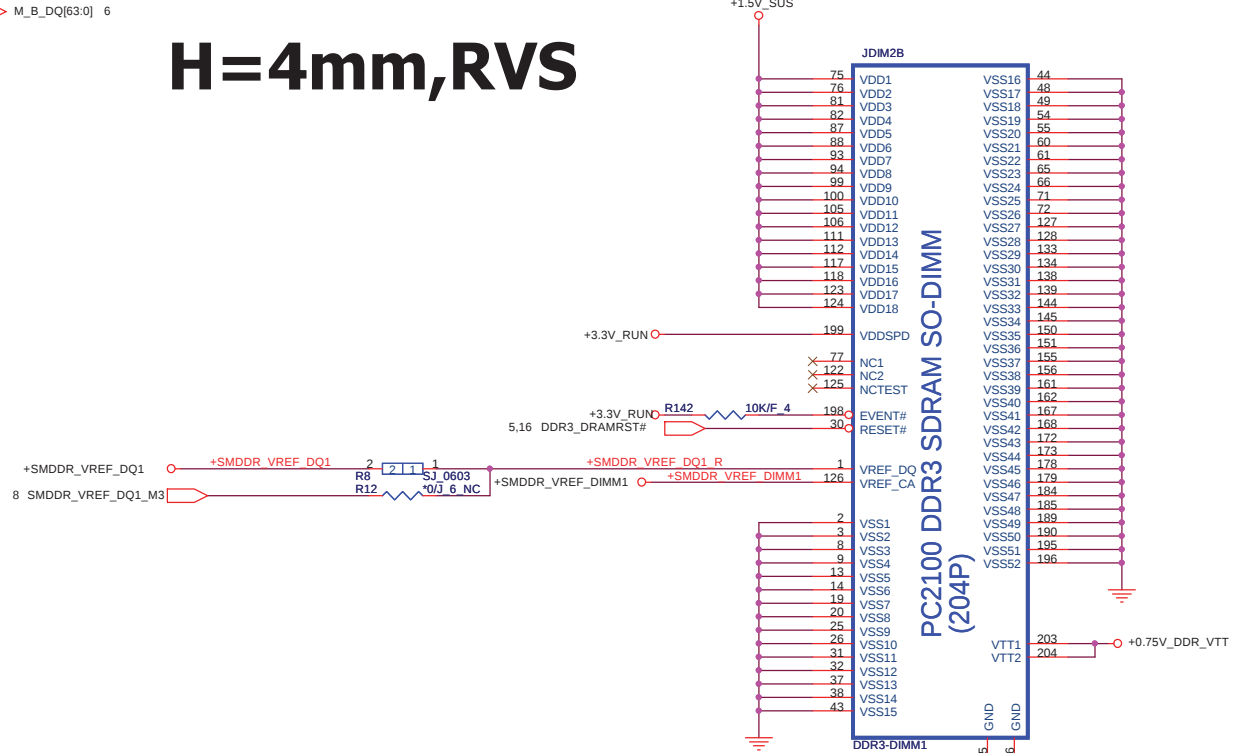
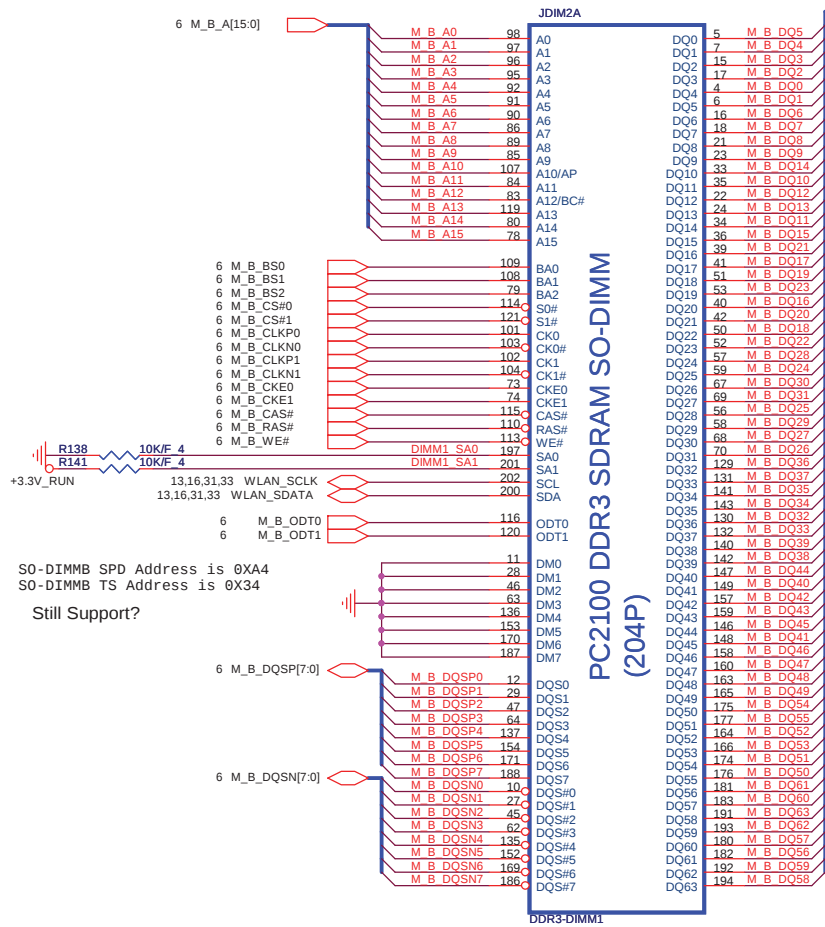


Ask PD3 or Intel, why
need 1ohm
change to +/-5%

H=8mm,RVS

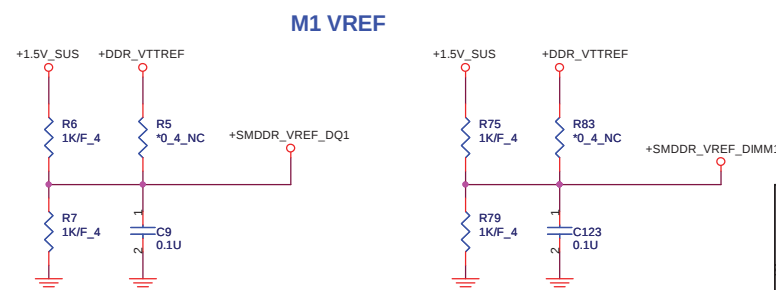
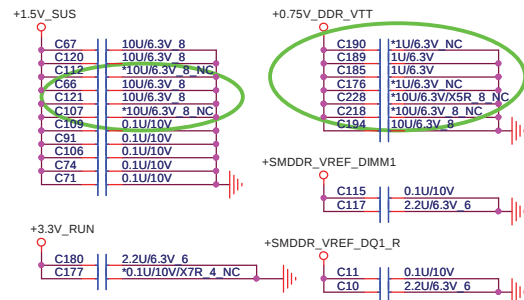


H=4mm,RVS



Place these Caps near So-Dimm1.

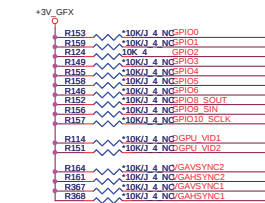
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



Quanta Computer Inc.
PROJECT : V02A/R01A

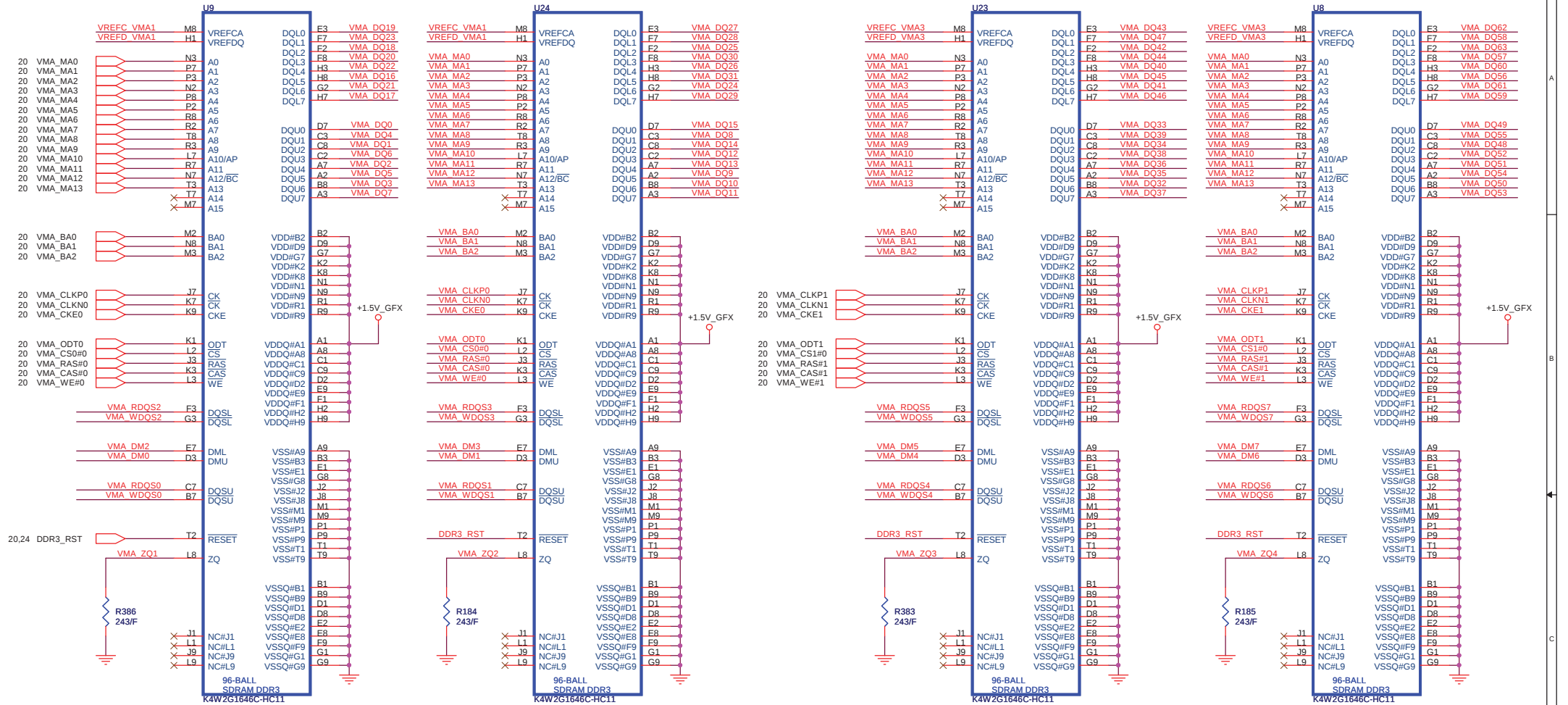
CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	0
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	1
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGA_VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	00
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0

APERTURE SIZE			
MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0



20 VMA_DQ[63..0]
20 VMA_DM[7..0]
20 VMA_WDQS[7..0]
20 VMA_RDQS[7..0]

CHANNEL A: 1024MB DDR3

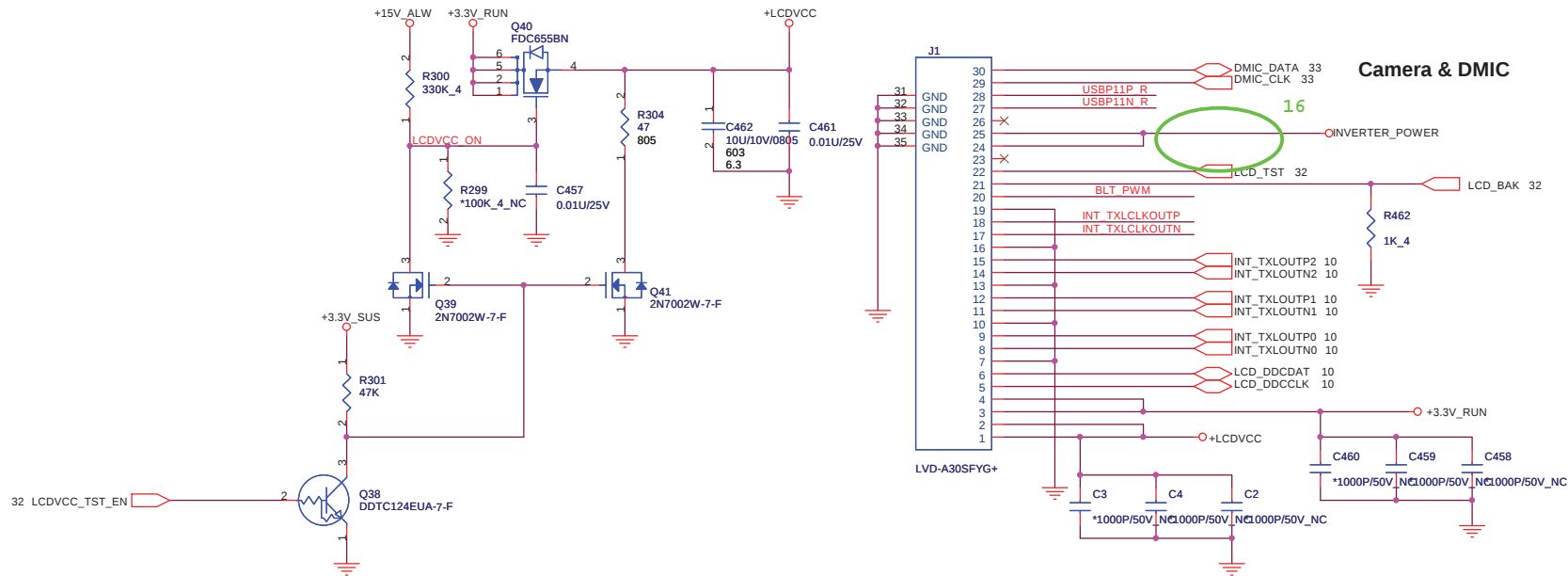


```

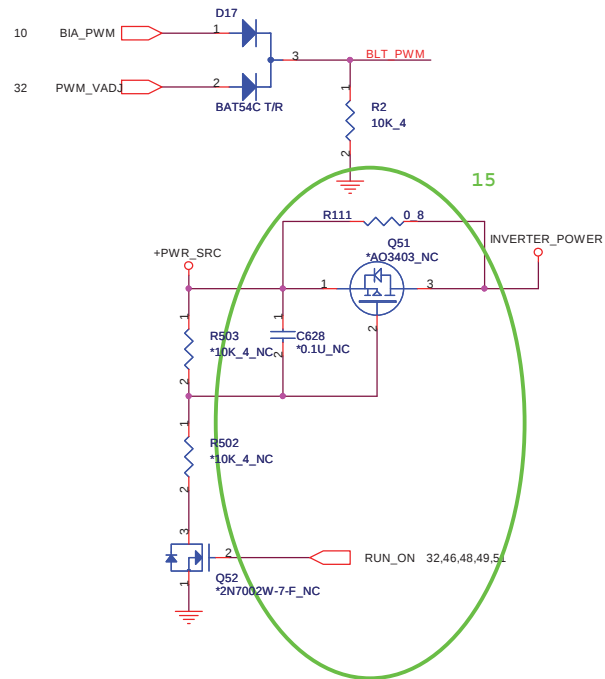
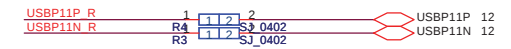
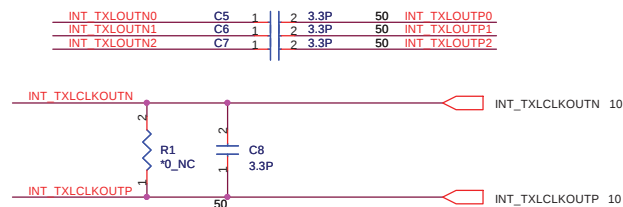
20 VMC_DQ[63..0]
20 VMC_DM[7..0]
20 VMC_WDQS[7..0]
20 VMC_RDQS[7..0]

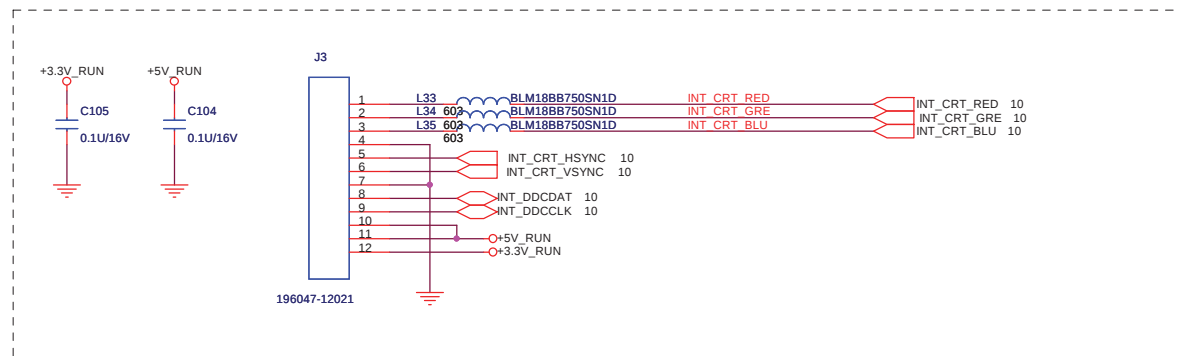
```

The schematic diagram illustrates the clock input circuit for the VMC. It features two clock inputs: VMC CLKP0 (R372) and VMC CLKN0 (R371) connected to a common node C561, and VMC CLKP1 (R357) and VMC CLKN1 (R359) connected to a common node C530. Both nodes are connected to a 0.01uF/25V capacitor and a 4-pin connector.



Shunt capacitors on LVDS for improving WWAN.

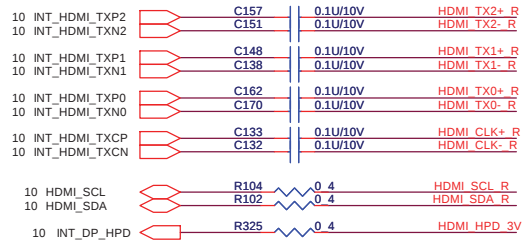




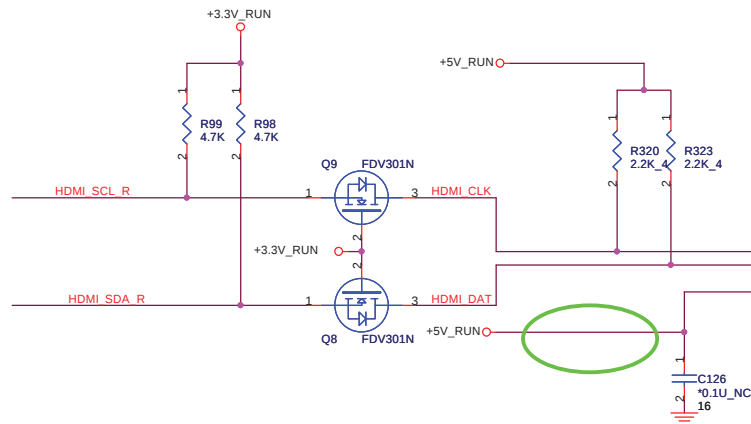
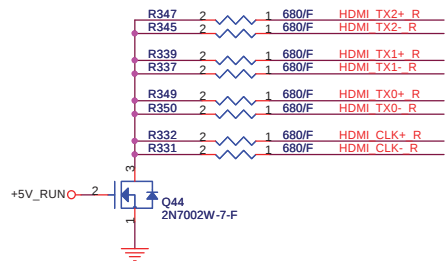
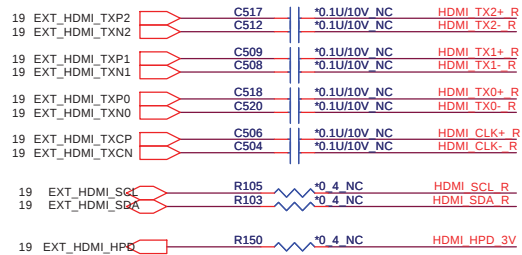
Quanta Computer Inc.
PROJECT : V02A/RO1A

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	BLANK	1A
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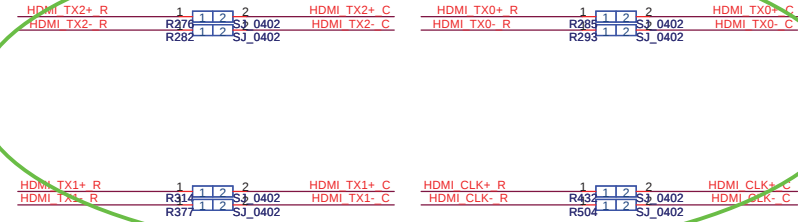
UMA HDMI



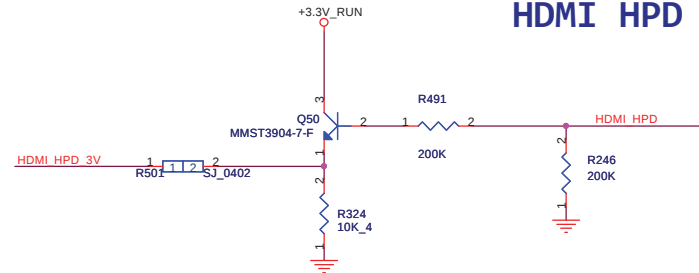
DIS HDMI



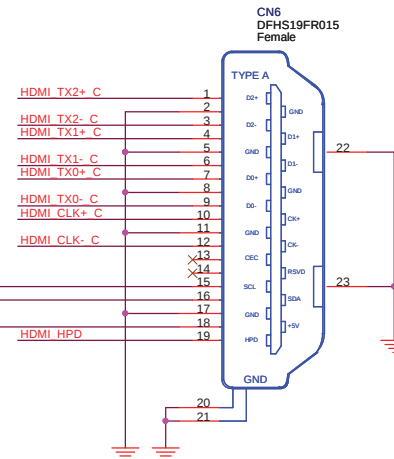
Reserve for EMI and close to HDMI CONN



HDMI HPD



HDMI Conn.

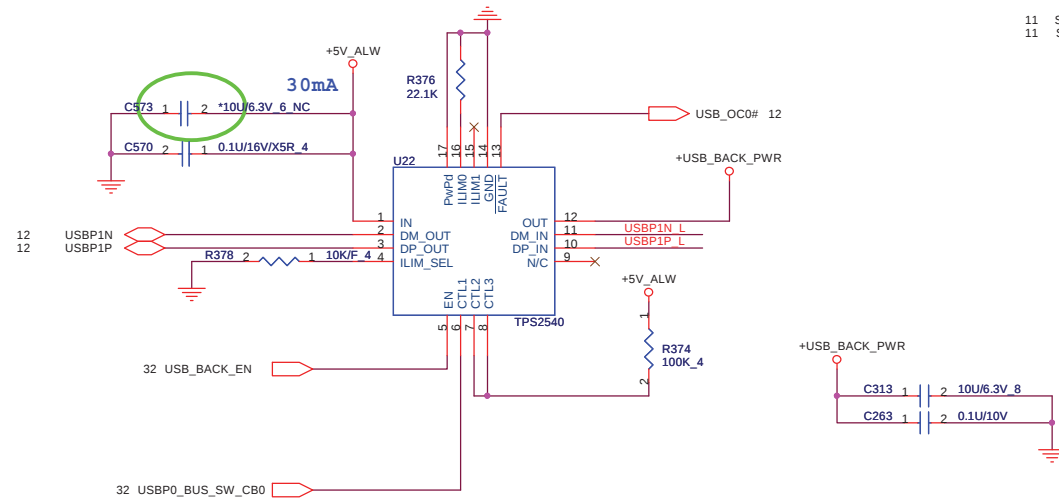


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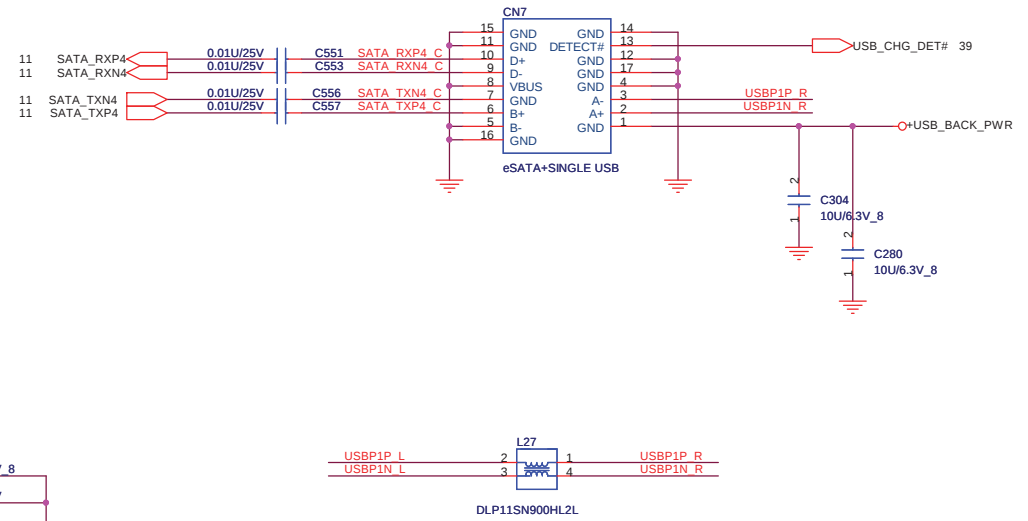
ESATA + USB Conn + Power share

S3/S5 USB charging circuit

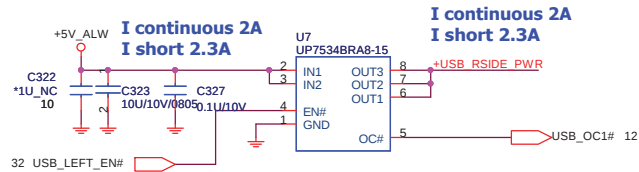


USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

	R8224	mA	
OC	100k ohm	480	
limitation	22.1k ohm	2171	Applied Now

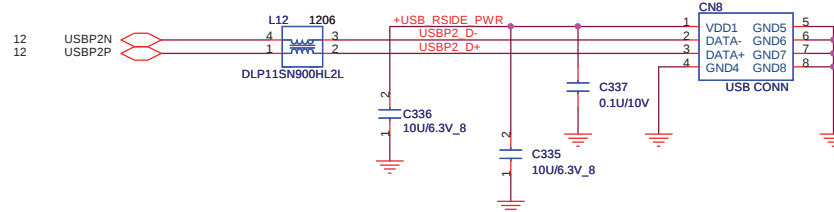
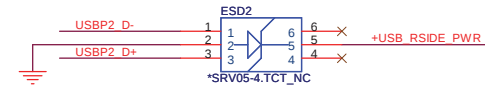


UPI power switch



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



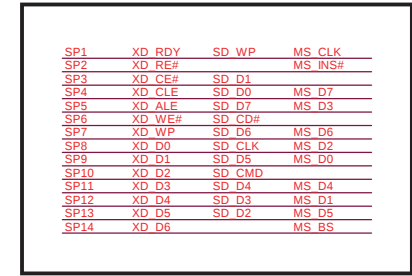
Quanta Computer Inc.
PROJECT : V02A/R01A

The diagram illustrates the pin connections for the Inspiron SD card connector (CON1). The connector has 25 pins, numbered 1 to 25. The connections are as follows:

- Pin 1:** SD D2
- Pin 2:** SD D3
- Pin 3:** SD D4
- Pin 4:** SD CMD
- Pin 5:** SD D5
- Pin 6:** MMC-11(D5)
- Pin 7:** SD-3(VSS)
- Pin 8:** SD-4(VDD)
- Pin 9:** MS-10(VSS)
- Pin 10:** MS-9(VCC)
- Pin 11:** MS-8(SCLK)
- Pin 12:** MS-7(D3)
- Pin 13:** MS-6(INS)
- Pin 14:** MS-5(D2)
- Pin 15:** MS-4(D0)
- Pin 16:** MS-3(D1)
- Pin 17:** MS-2(BS)
- Pin 18:** MS-1(VSS)
- Pin 19:** SD-5(CLK)
- Pin 20:** MMC-12(D6)
- Pin 21:** SD-6(GND)
- Pin 22:** MMC-13(D7)
- Pin 23:** SD-7(D0)
- Pin 24:** SD-8(D1)
- Pin 25:** SD(SW,COM)
- Pin 26:** SD(SW,CD)
- Pin 27:** XD-1(CDSW)
- Pin 28:** XD-9(GND)
- Pin 29:** XD-2(R/B-)
- Pin 30:** XD-3(RE)
- Pin 31:** XD-4(CE)
- Pin 32:** XD-5(CLE)
- Pin 33:** XD-6(ALE)
- Pin 34:** XD-7(WE)
- Pin 35:** XD-8(-WP)
- Pin 36:** XD-9(GND)
- Pin 37:** XD-10(D0)
- Pin 38:** XD-11(D1)
- Pin 39:** XD-12(D2)
- Pin 40:** XD-13(D3)
- Pin 41:** XD-14(D4)
- Pin 42:** XD-15(D5)
- Pin 43:** XD-16(D6)
- Pin 44:** XD-17(D7)
- Pin 45:** XD-18(VCC)
- Pin 46:** SD(SW,WP)

The diagram also shows the following components and connections:

- Capacitors:** C624 (1u/6.3V) connected to pin 1; C615 and C622 connected to pins 10 and 11 respectively; C370 (*0.1u/16V_NC) connected to pin 45.
- Power and Ground:** +CARD_3V3 connected to pin 25; *27P_NC connected to pins 10 and 11; GND connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46.
- Signal Lines:** SD D2, SD D3, SD D4, SD CMD, SD D5, MS CLK, MS D3, MS INS#, MS D2, MS D0, MS D1, MS BS, SD CLK, SD D6, SD D7, SD D0, SD D1, SD CD#, XD CD#, XD RDY, XD RE#, XD CE#, XD CLE, XD ALE, XD WE#, XD WP, XD D0, XD D1, XD D2, XD D3, XD D4, XD D5, XD D6, XD D7, SD WP.



DLP11SN900HL2L

12 USBP8N 3 4 USBP8 D-
 12 USBP8P 2 1 USBP8 D+

L32

Cardreader	POP	NC
Inspiron	CON1	CON3
VOSTOR	CON3	CON1

The image shows the PCB layout of the VOSTOR module. The module is a blue rectangular component with pins labeled 1 through 45. It is connected to a red PCB. The connections include:

- SD D2, SD D3, SD D4, SD CMD, SD D5
- MS CLK, MS D3, MS INS#, MS D2, MS D0, MS D1, MS BS
- SD CLK, SD D6, SD D7, SD D0, SD D1
- C623 (1uF/6.3V)
- C642 (22pF)
- C618 (*27P_NC)
- C448 (*27P_NC)
- C605 (*0.1uF/16V_NC)
- +CARD_3V3

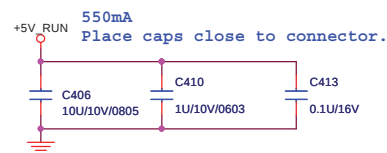
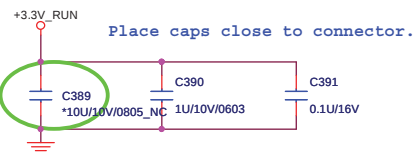
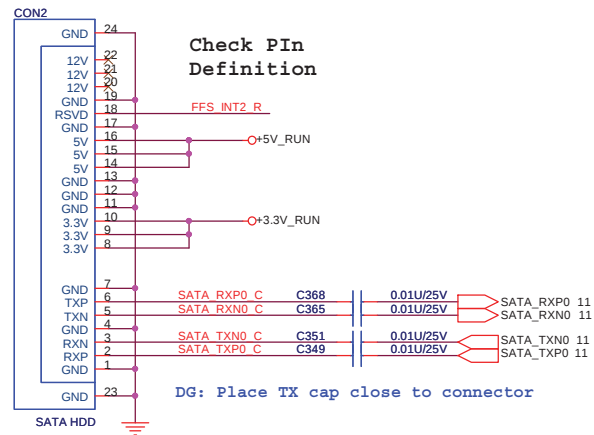
The module is labeled "TAS_5-250907001000-9" and "5in1-scdg2c0101-45p".



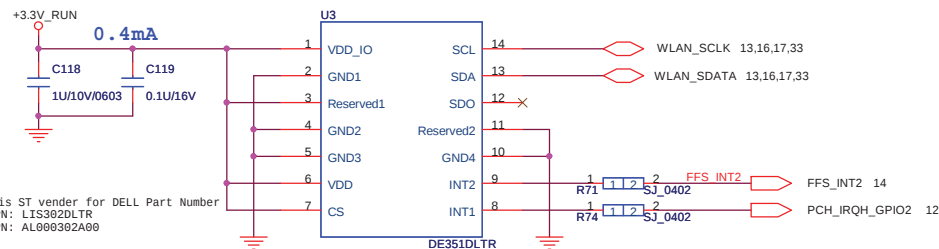
PROJECT : V02A/RO1A

Size	Document Number	Rev
	Cardreader (RTS5128)	1A
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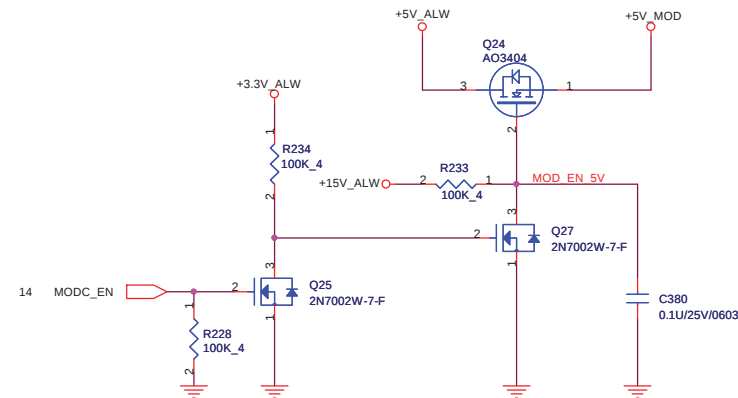
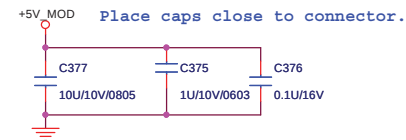
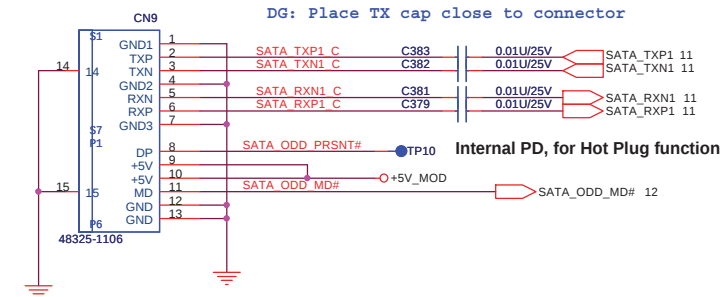
SATA Connector UM8



3-axis Fall Sensor (HDD data protector)



ODD Connector

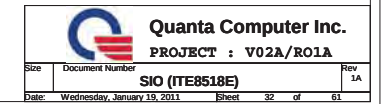


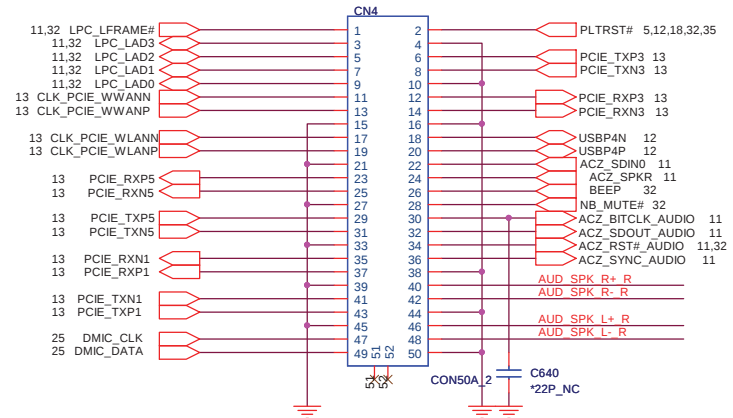
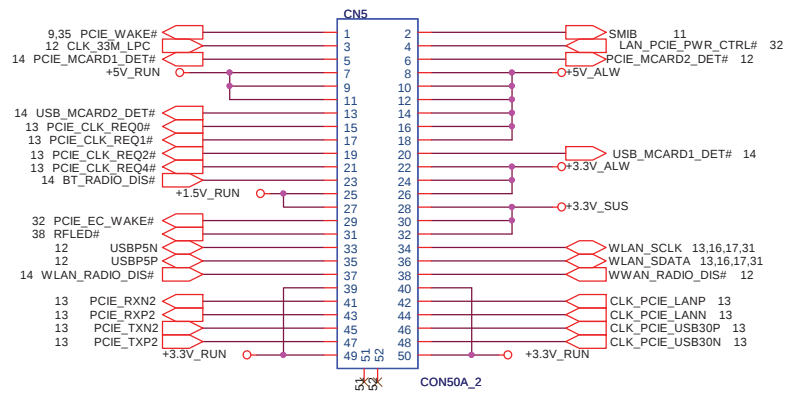
3-axis Fall Sensor	VOSTOR	Inspiron
U3, Q29, D11 R71, R74, R252 C118, C119	POP	NC



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	SATA HDD/ODD	1A
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Int. Stereo Speakers
5V / 4 Ohm / 2W

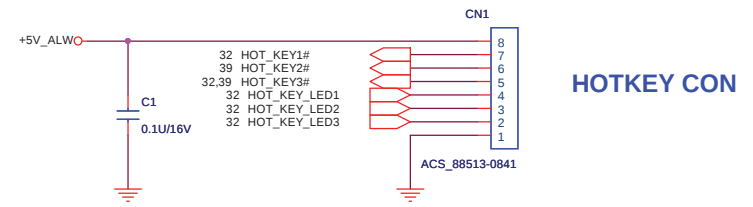


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SIO (ITE8518E)

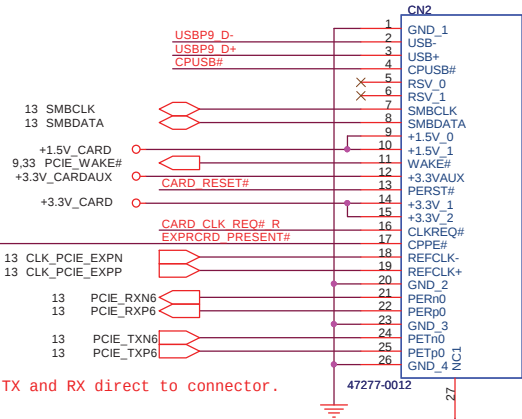
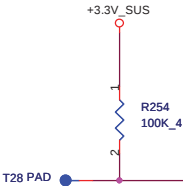
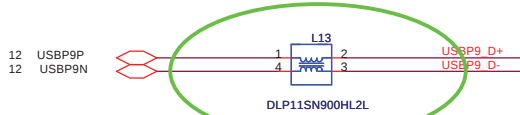
Size	Document Number	Rev
		1A
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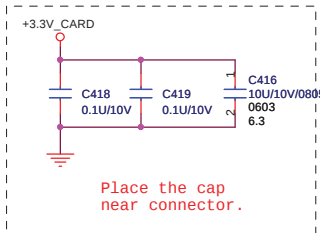
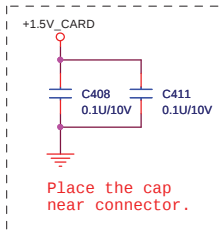
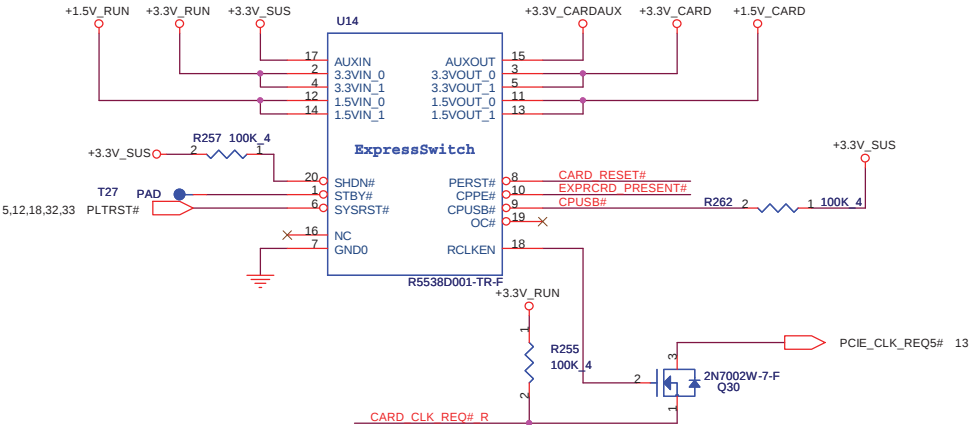
Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	MINI-PCI (WLAN/WPAN)	1A
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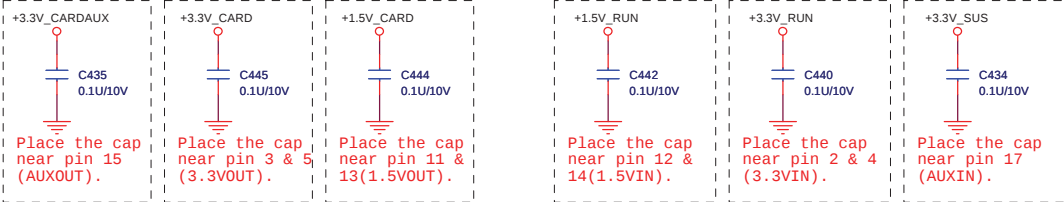
Express Card



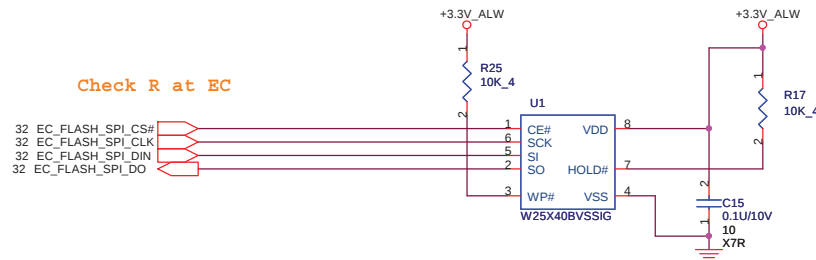
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



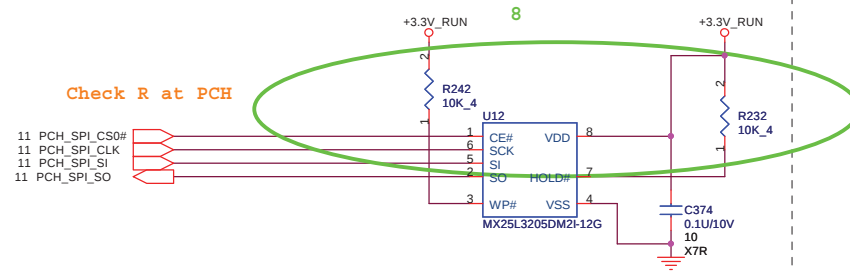
If close enough, could combine



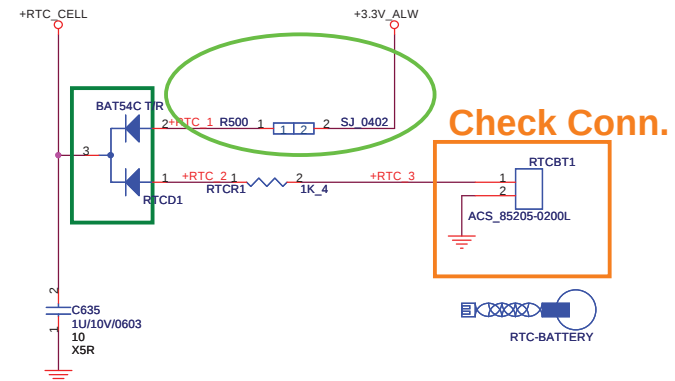
For EC 4Mbit (512K Byte)



For PCH 32Mbit (4M Byte)



RTC



Double, 25°C, Vf=0.4V, If=25mA
one, 25°C, Vf=0.35V, If=15.8mA

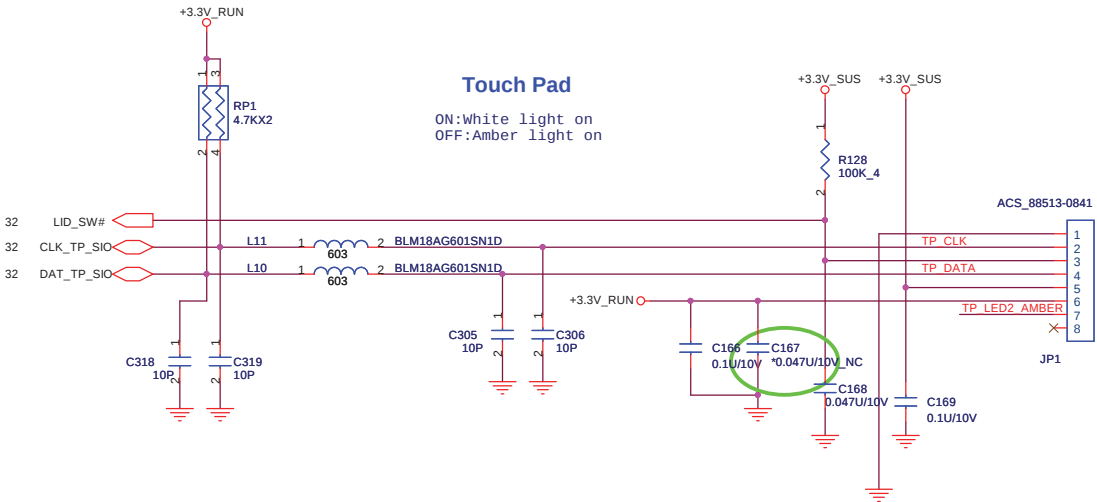


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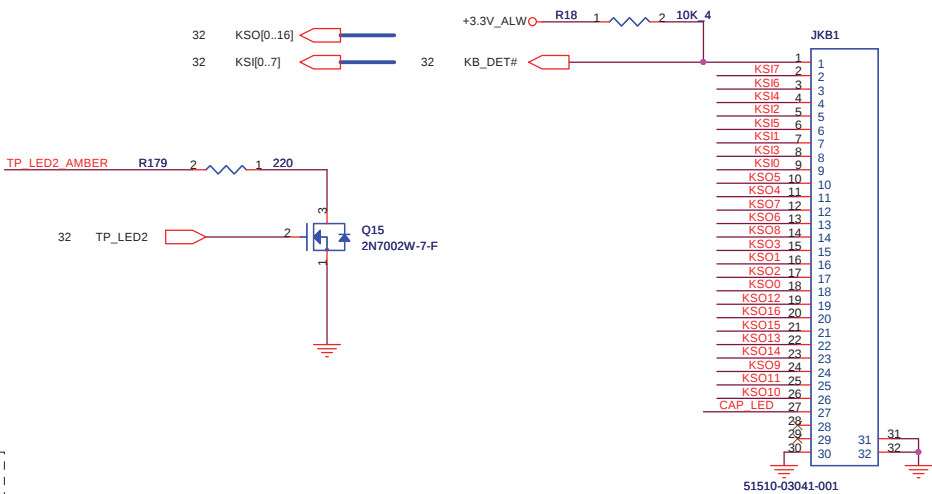
PROJECT : V02A/R01A

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FLASH / RTC

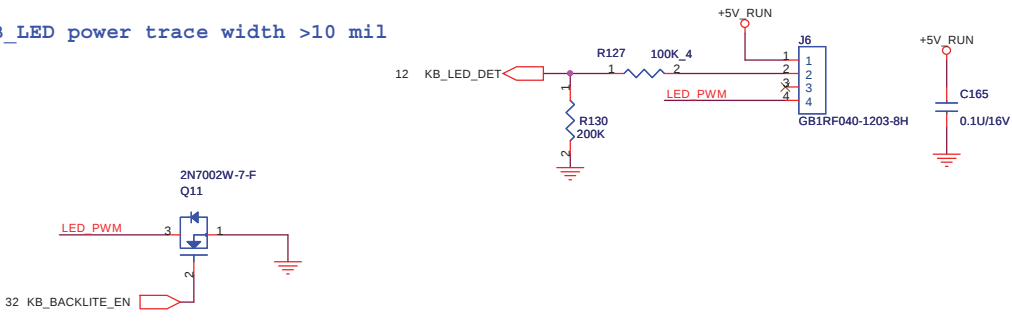


KEYBOARD CONNECTOR

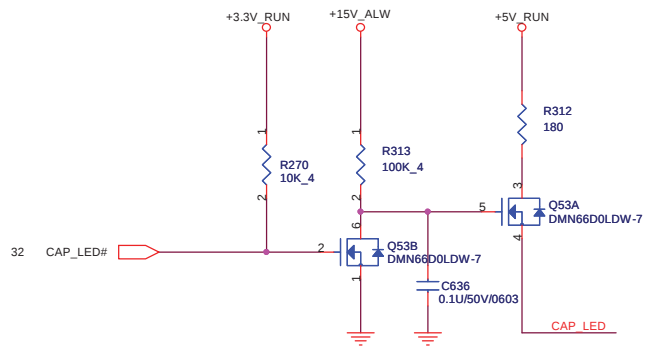
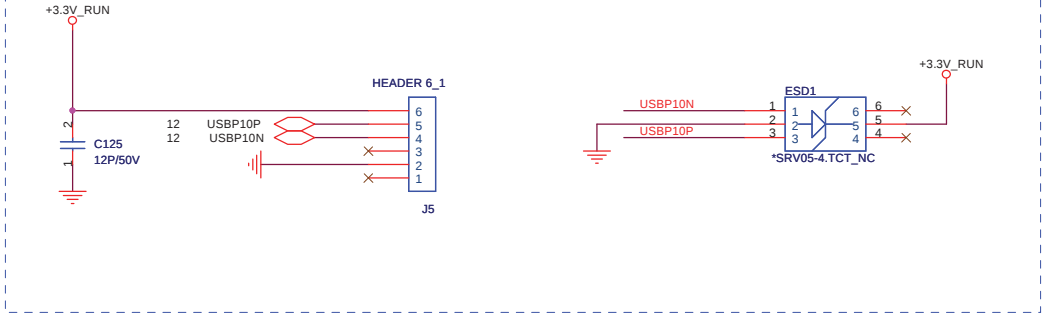


Key board illumination

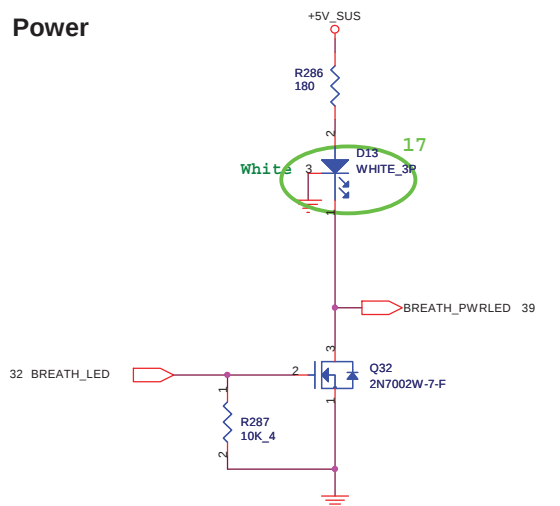
+KB_LED power trace width >10 mil



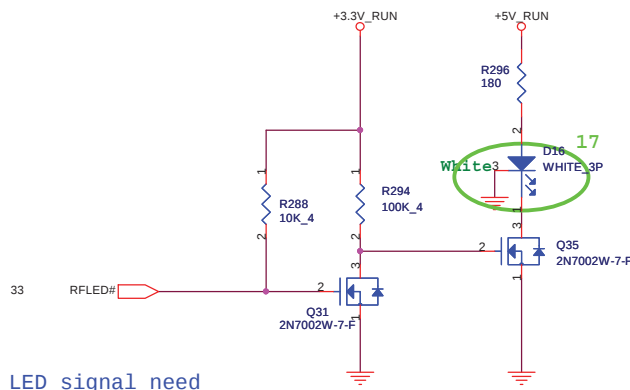
Biometric



Power

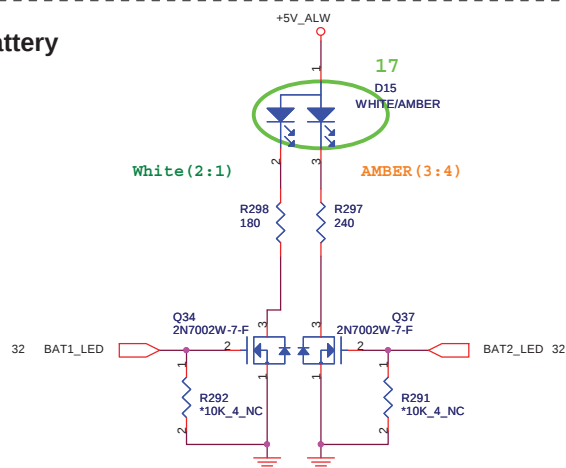


Bluetooth / WLAN on/off LED

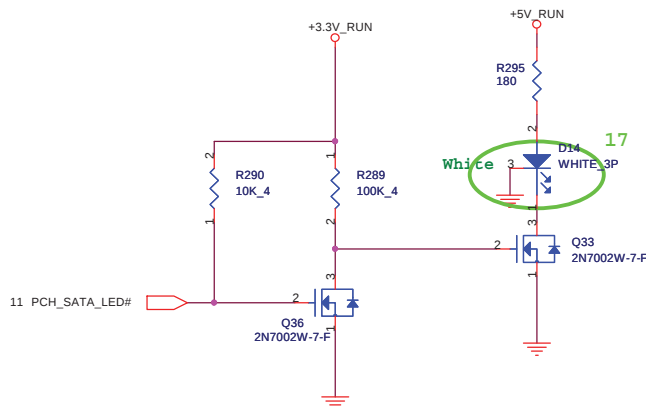


BT LED signal need

Battery



HDD activity LED.

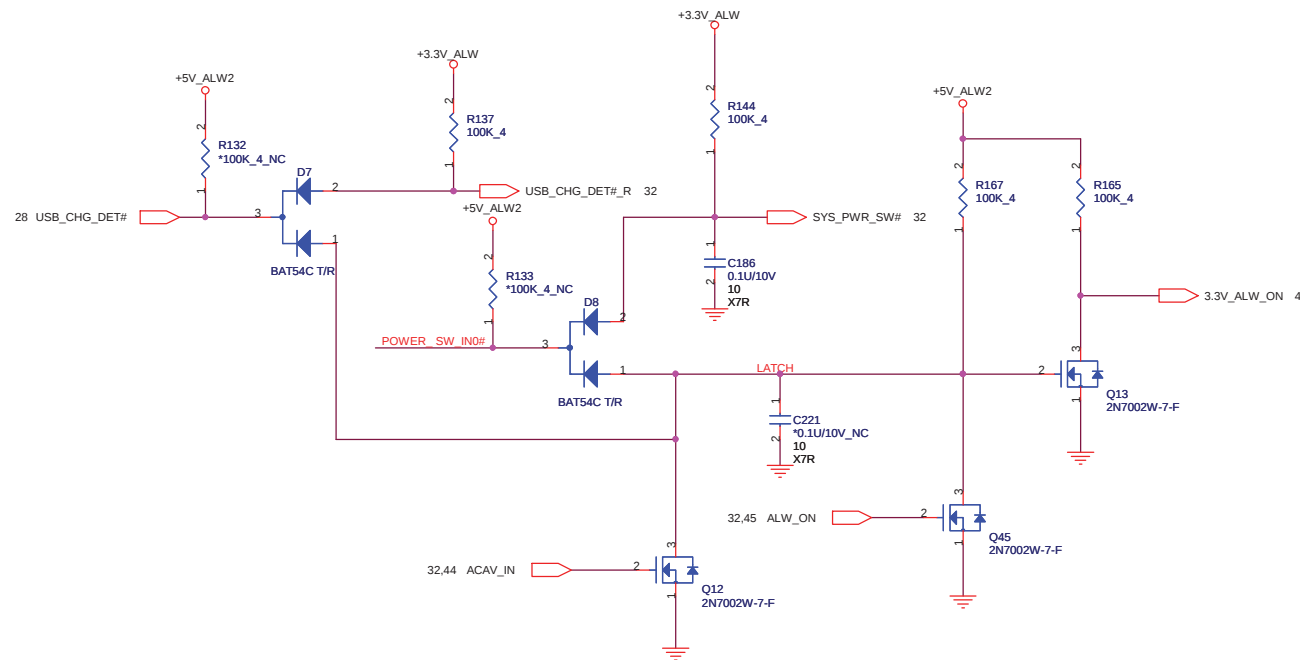


VOSTOR	R286, R295, R296, R298	R297
	180 ohm PN:CS11802JB15	240 ohm PN:CS12402JB13
Inspiron	R286, R295, R296, R298	R297
	390 ohm PN:CS13902JB14	330 ohm PN:CS13302JB21



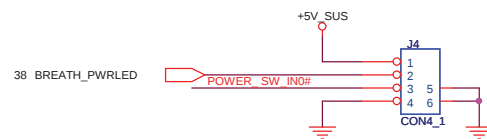
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PROJECT : V02A/RO1A

3VALW ON POWER LOGIC

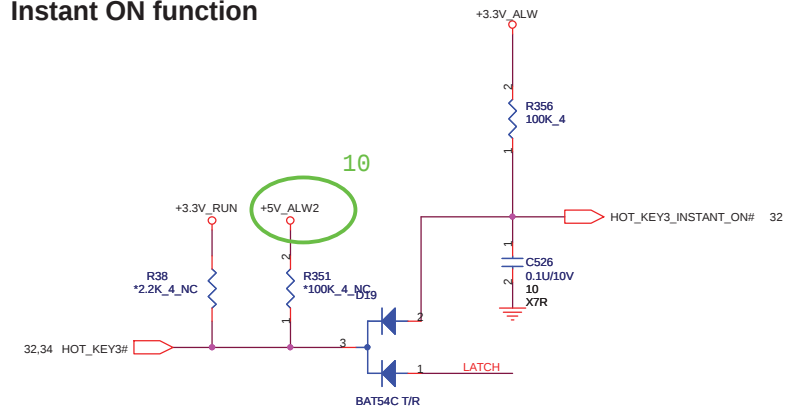


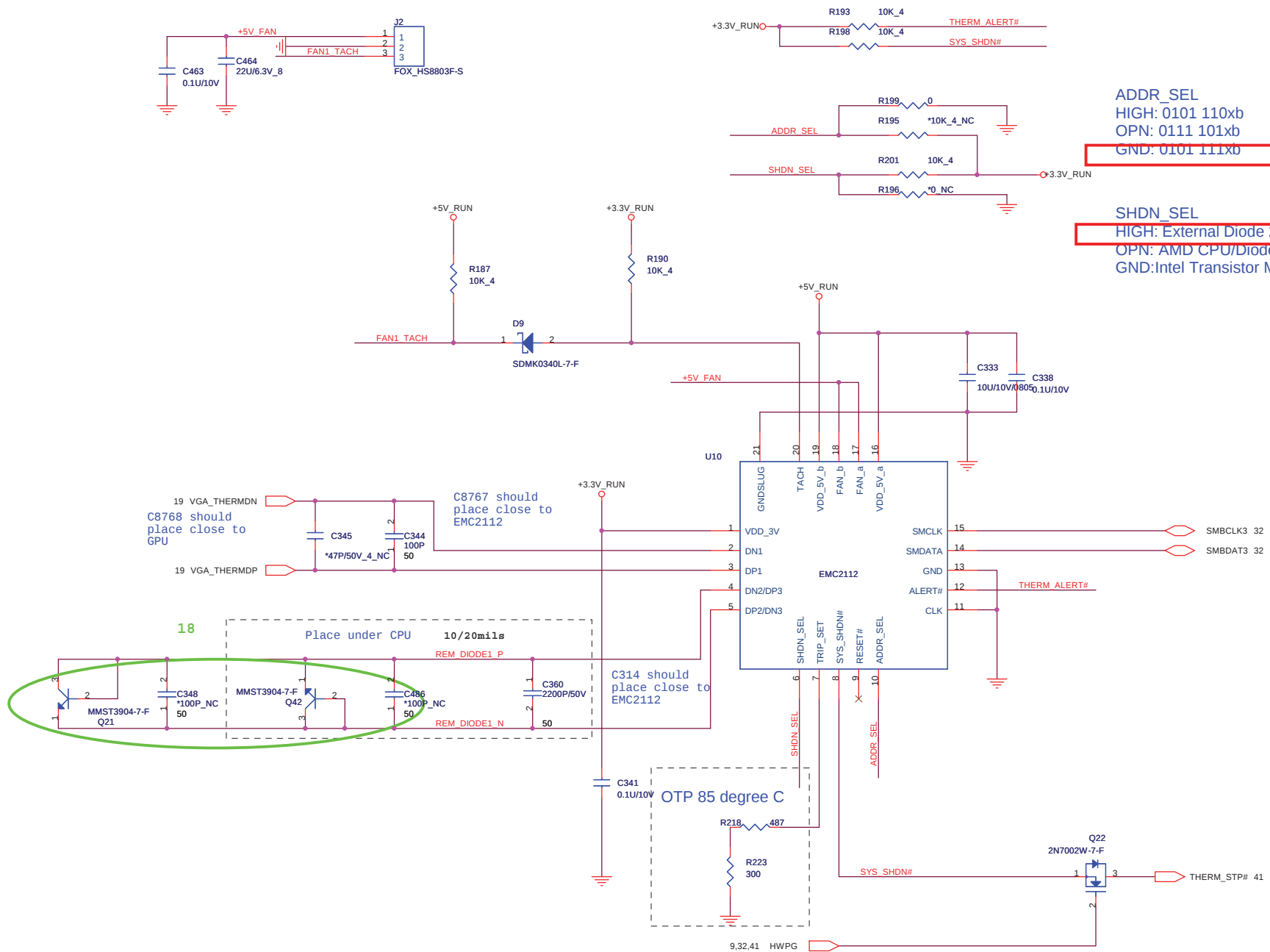
Vostro pop D19,C526,R356 depop R38,R39
Inspiron depop D19,C526,R356 pop R38,R39

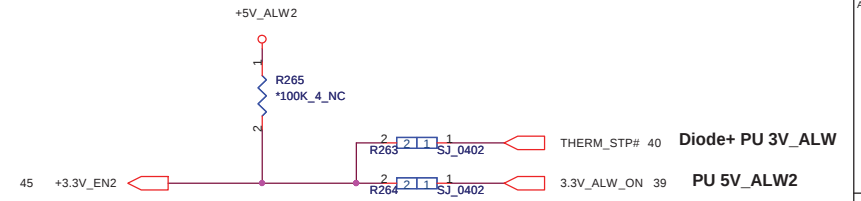
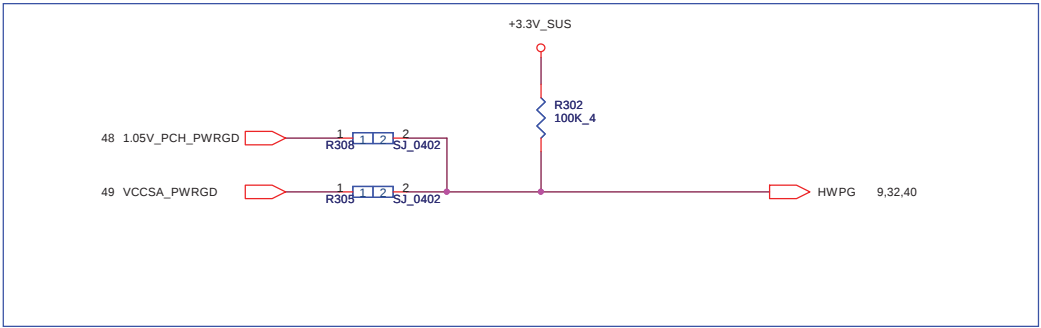
PWR button board

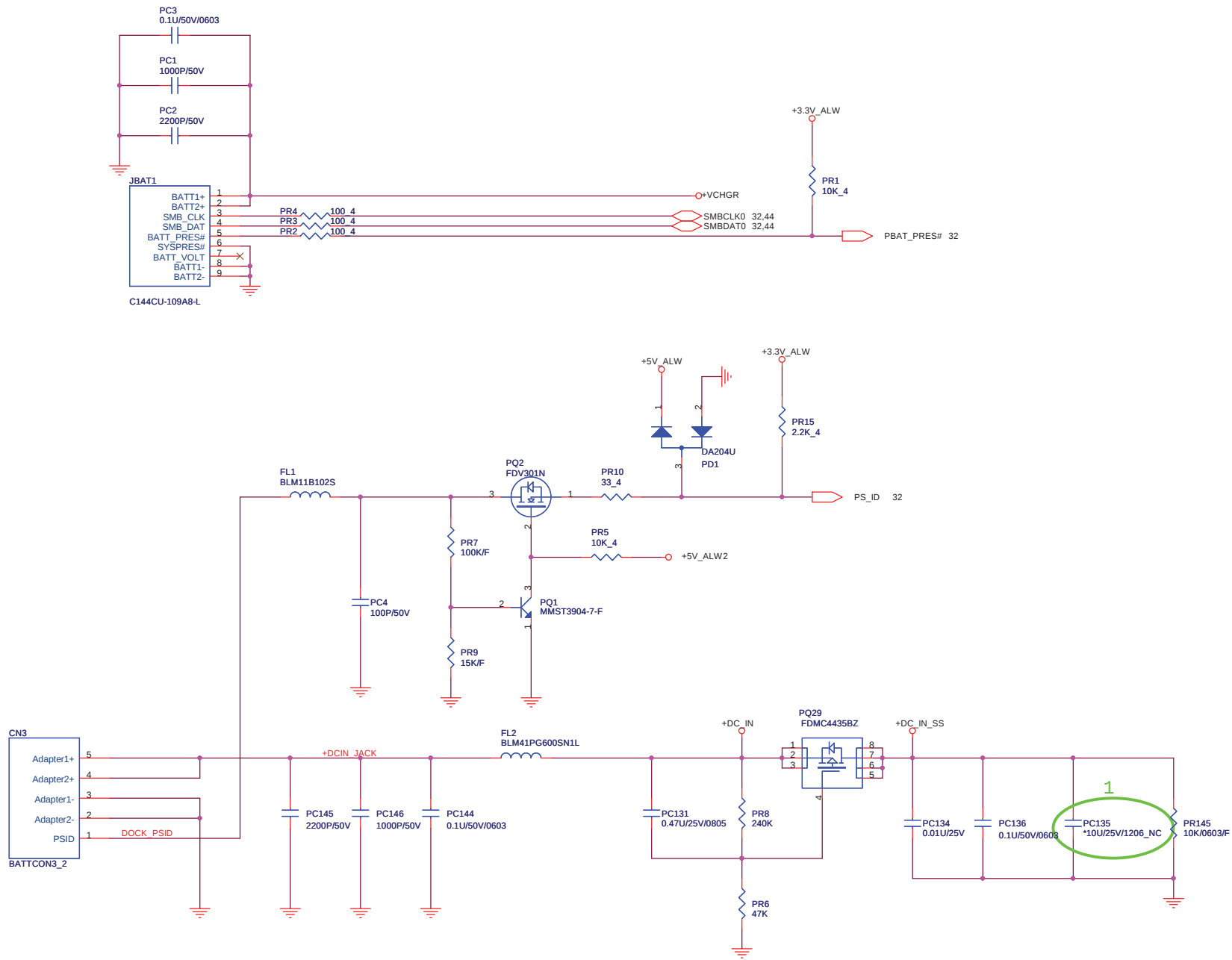


Instant ON function



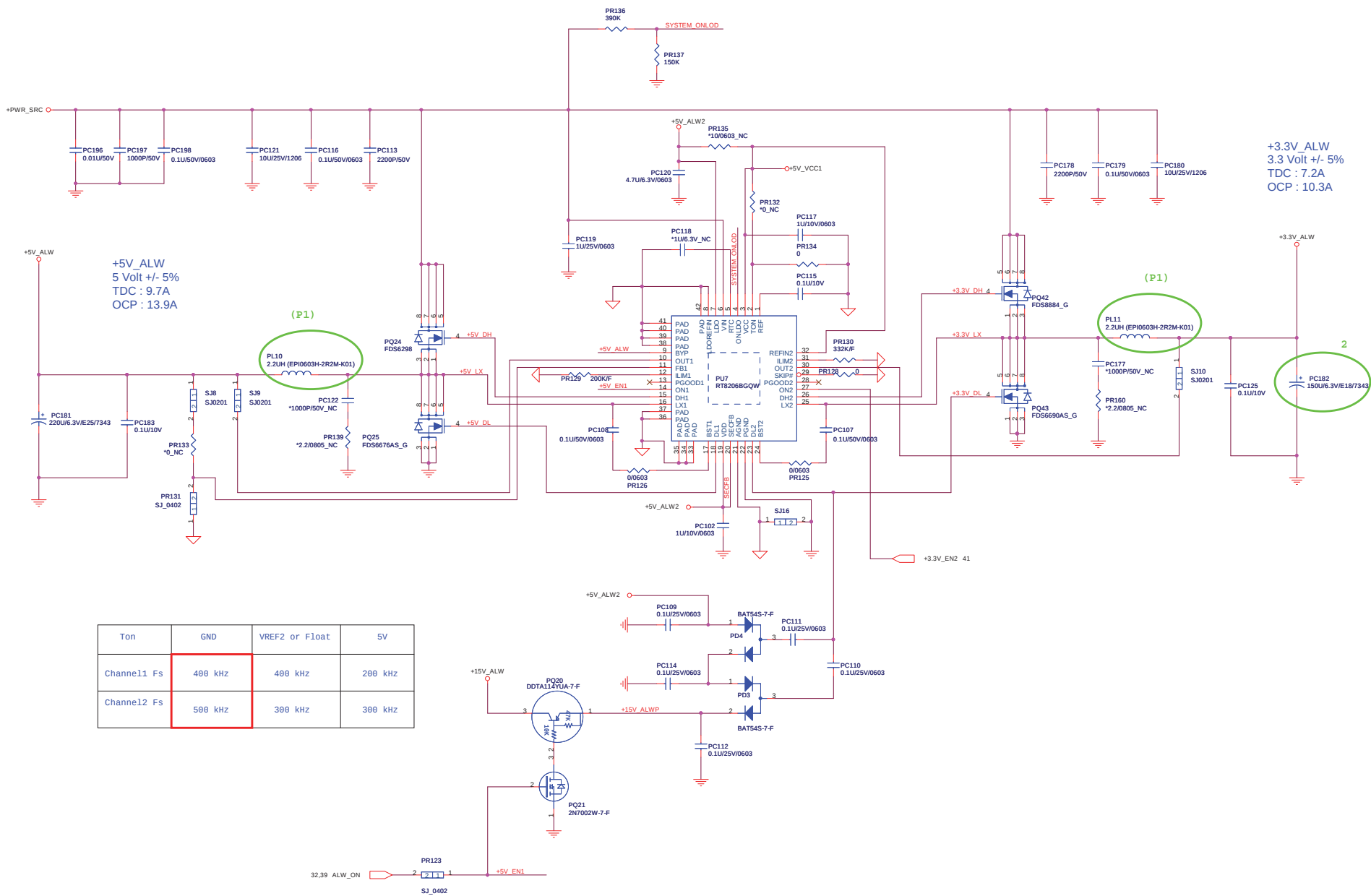


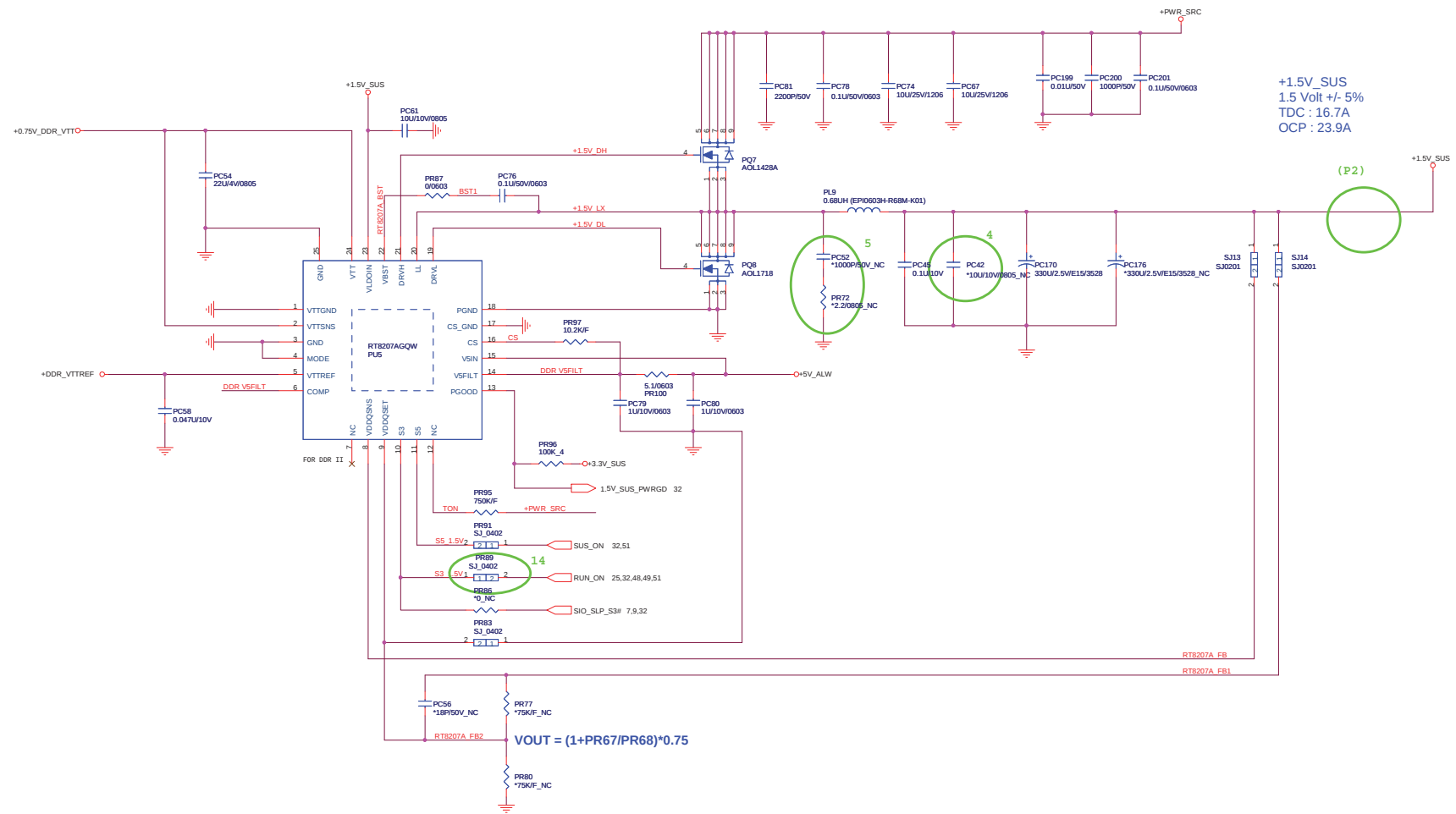




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	DC IN / BATT	1A
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+1.5V_SUS
1.5 Volt +/- 5%
TDC : 16.7A
OCP : 23.9A

VDDQ and VIT discharge control

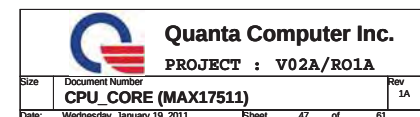
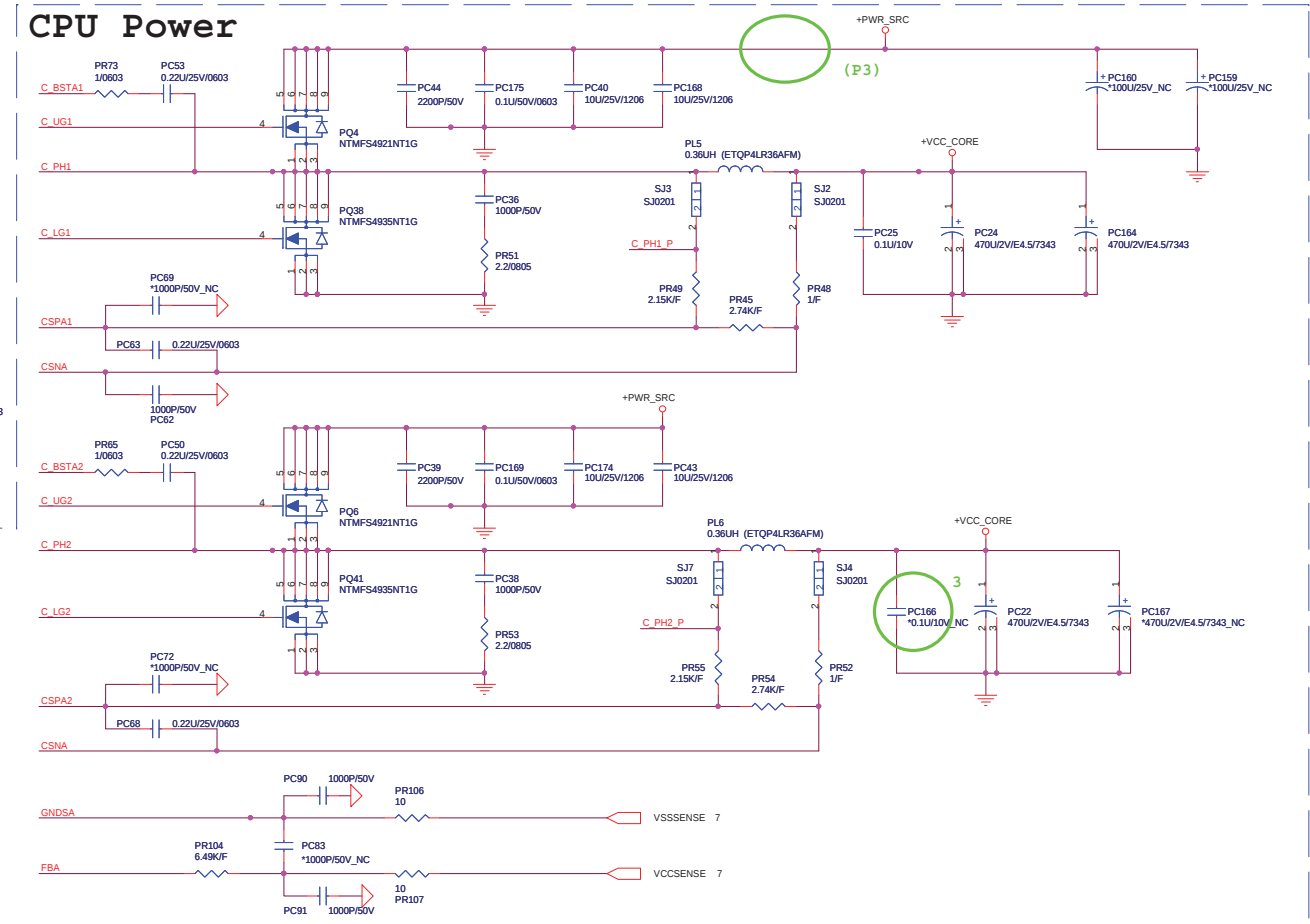
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

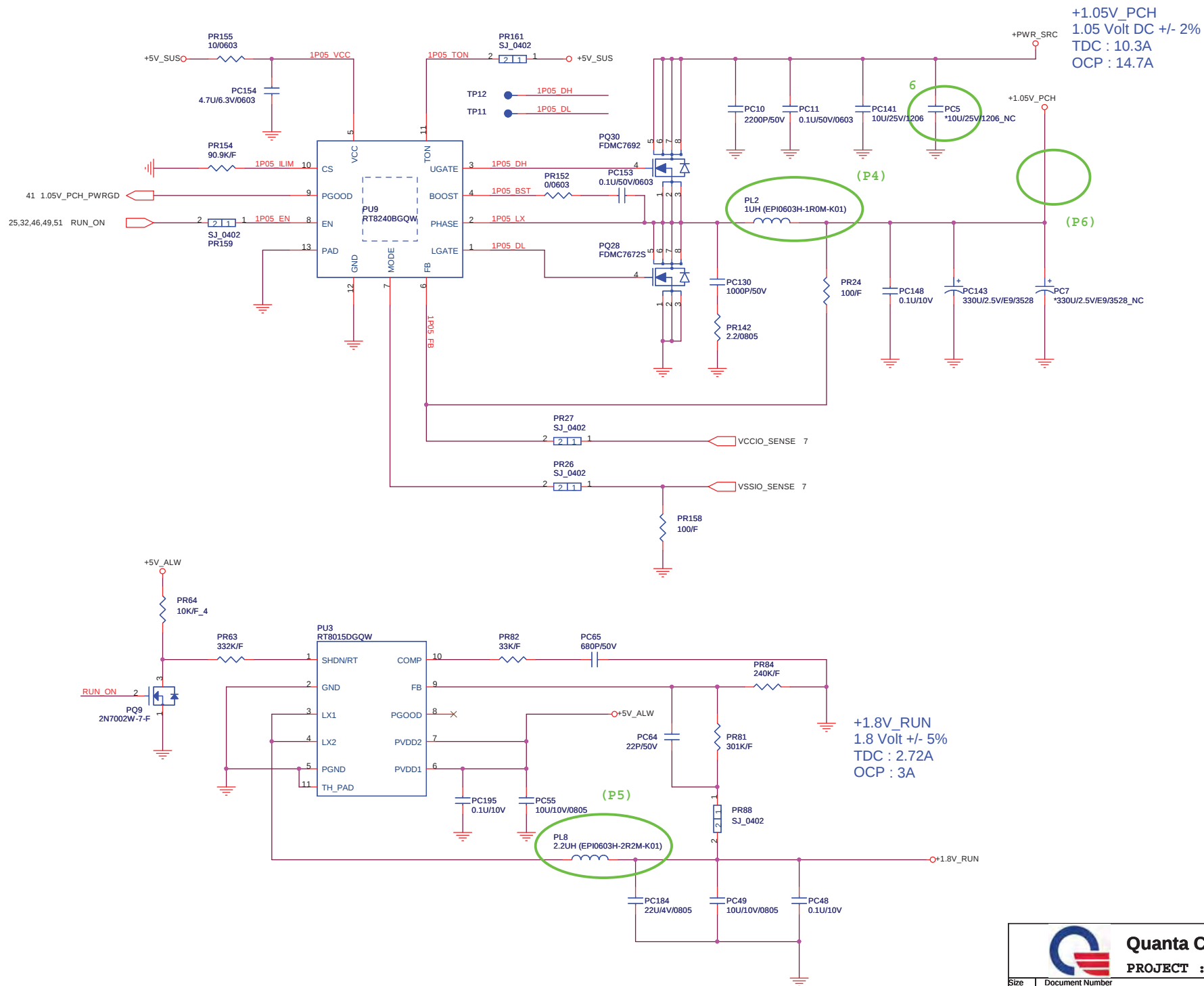
VDDQ output voltage selection

VDDQSET	VDDQ (V)	VITREF and VIT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VITREF	VIT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

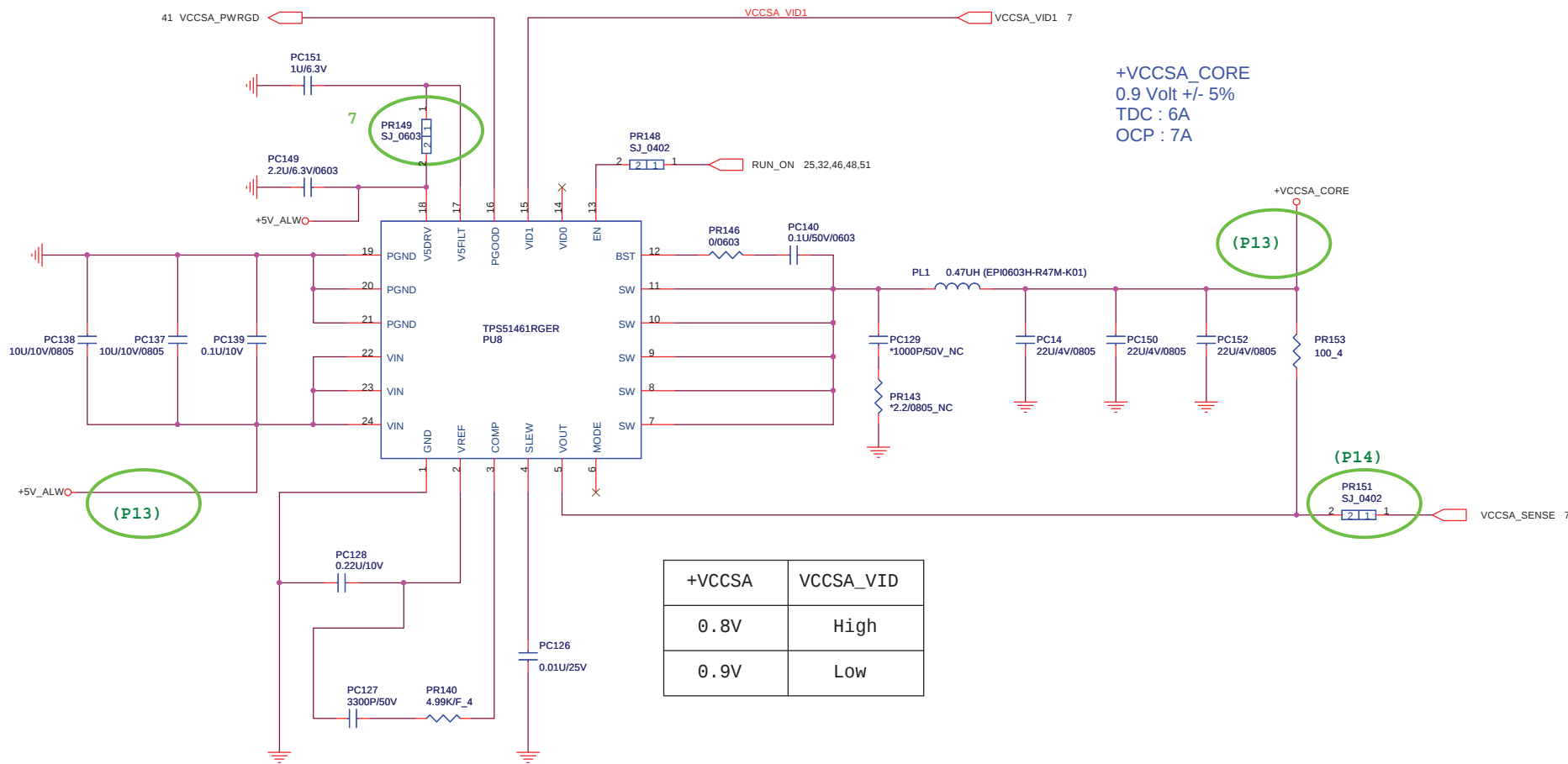




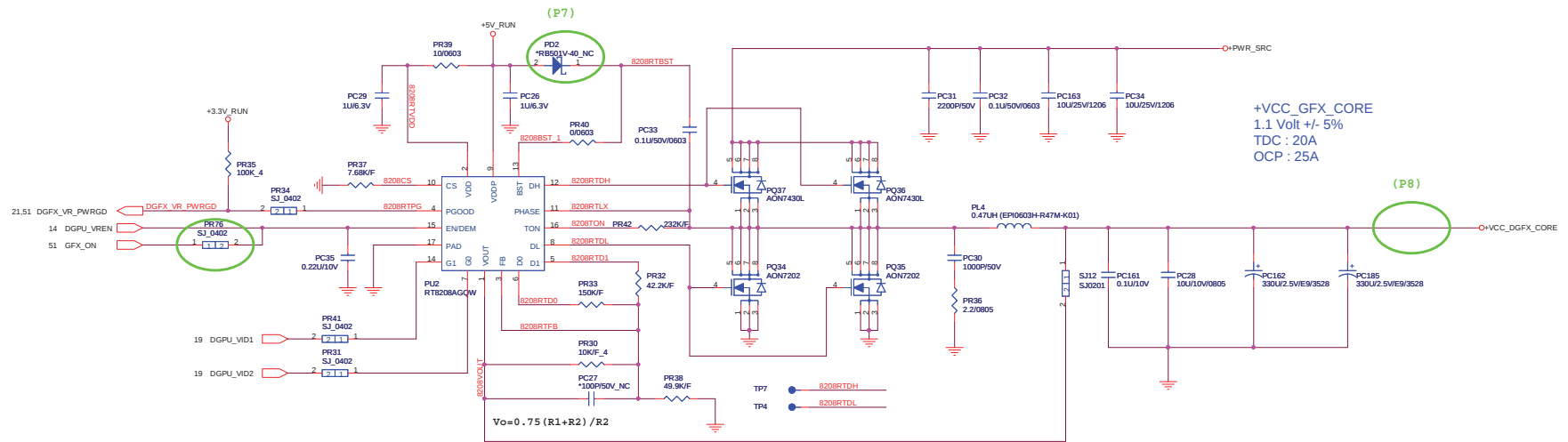
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Size	Document Number	Rev
	+1.05V_PCH / VTT (TPS51218DSCR)	1A
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Robson_XT

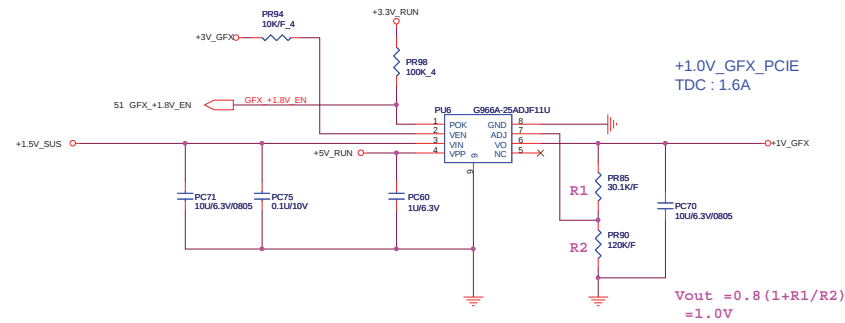
DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
HIGH	HIGH	1.12V
Setting		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS34992FB10	49.9K
PR33	CS41502FB18	150K
PR32	CS34222FB00	44.2K

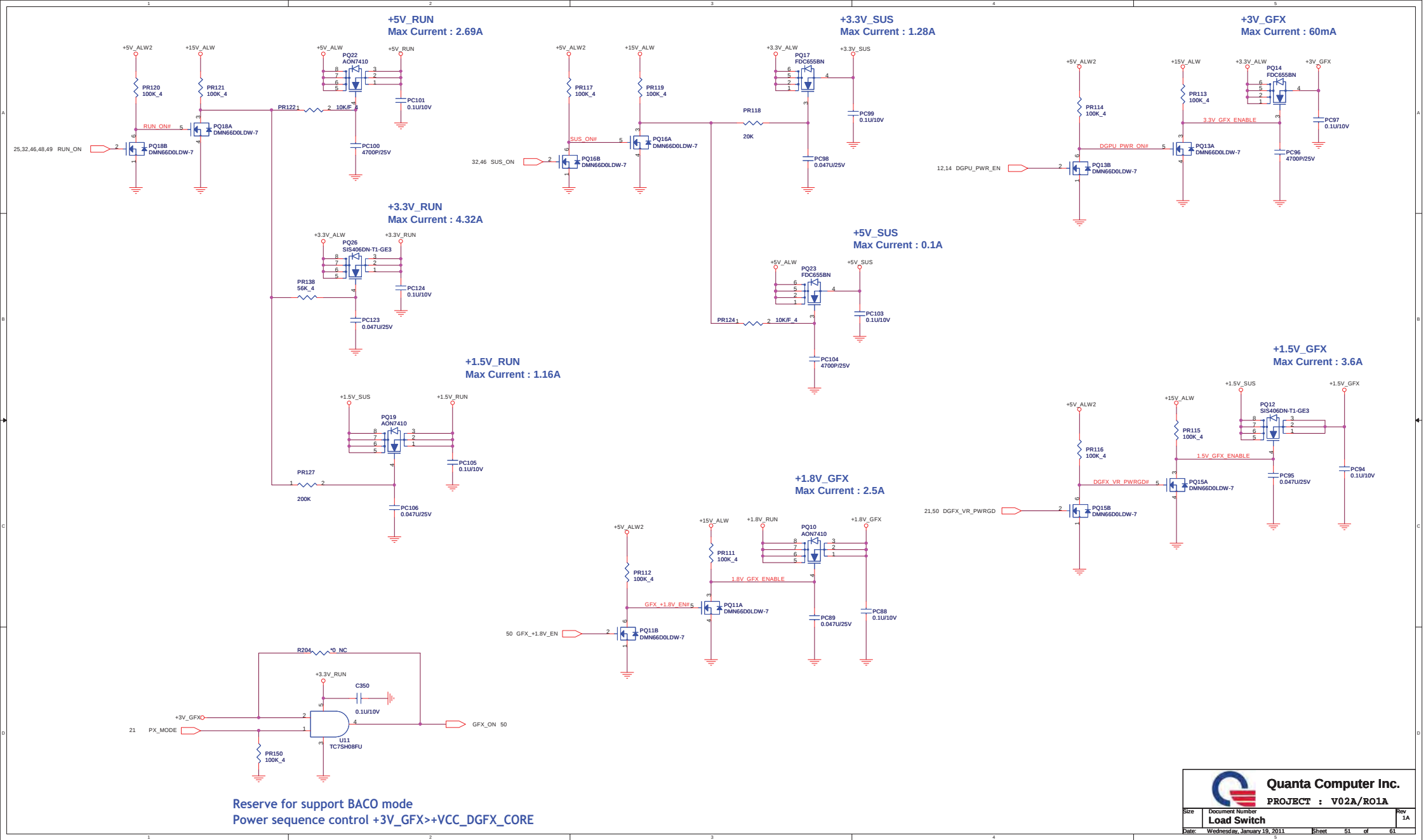
Whistler_LP

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	0.9V
HIGH	HIGH	1.0V
Setting		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS37502FB12	75K
PR33	CS41502FB18	150K
PR32	CS37502FB12	75K

Seymour_XT

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	0.9V
LOW	HIGH	1.0V
HIGH	HIGH	1.1V
Setting		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS37502FB12	75K
PR33	CS41072FB11	107K
PR32	CS34122FB19	41.2K





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Load Switch		1A
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