

MODEL NAME : VAUB0

PCB NO : LA-9941P  
DAA0006W000

BOM P/N : TBD

# Dell/Compal Confidential

## Schematic Document

### Phantom (Shark Bay)

### Haswell (BGA) + Lynx Point

DISCRETE VGA N14P (optimus) --- Testarossa  
DISCRETE VGA N15P (optimus) --- Testarossa-P

2013-01-02

Rev: 0.1 (X00)

@ : Nopop Component

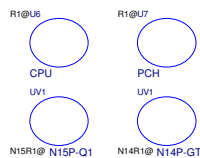
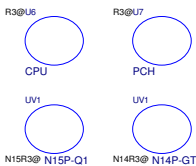
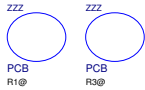
CONN@ : Connector Component

TPM@ : TPM function

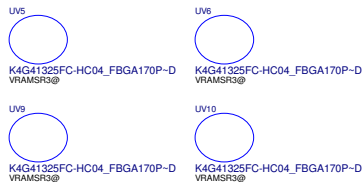
DSP@ : DSP function

N14@ : DGPU N14P-GT

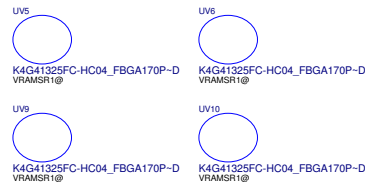
N15@ : DGPU N15P-Q1



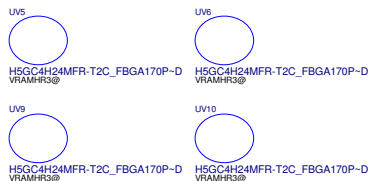
#### Samsung 2G



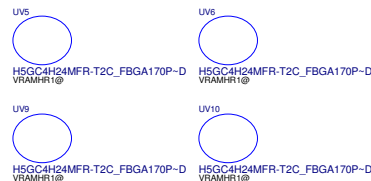
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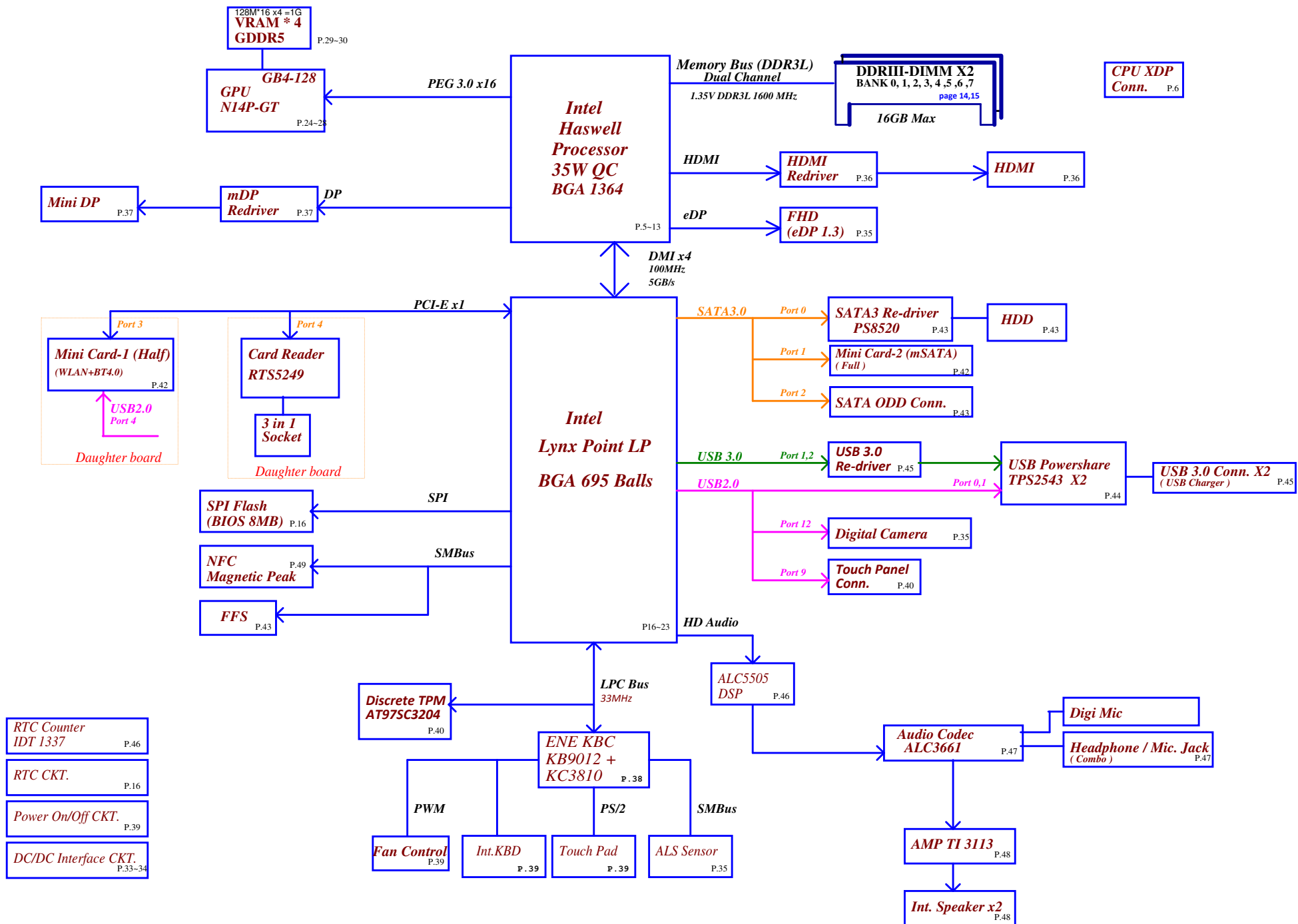
#### Hynix 2G



#### Hynix 2G



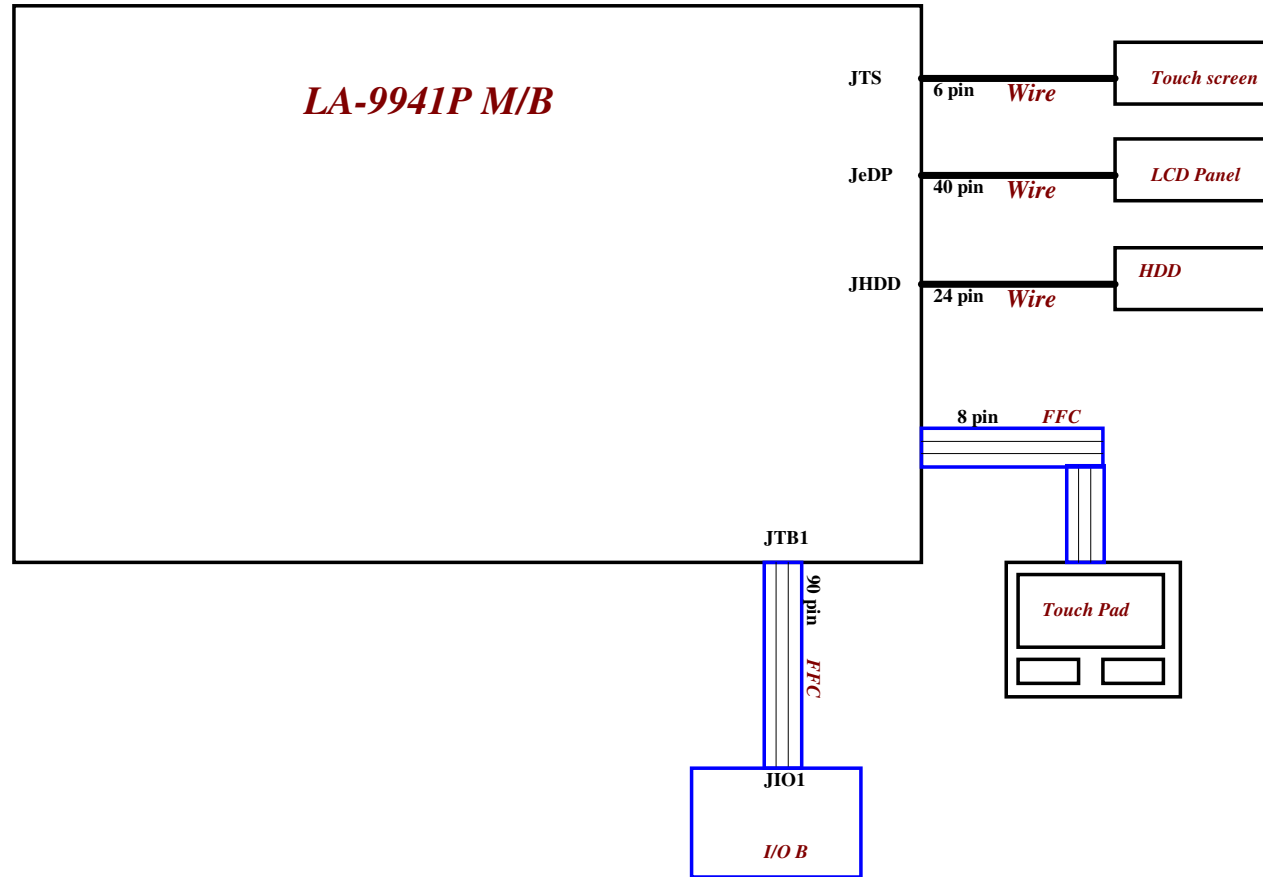
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Project Code : VAUB0

File Name : LA-9941P



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Vcc	3.3V			
Ra	100K +/- 1%			
Board ID	Rb		Board ID	PCB Revision
0	0		0	DIS 0.1
1	12K +/- 1%		1	DIS 0.2
2	15K +/- 1%		2	DIS 0.3
3	20K +/- 1%		3	DIS 0.4
4	27K +/- 1%		4	DIS 0.5
5	33K +/- 1%		5	DIS 1.0
6	43K +/- 1%		6	DIS-P 0.2
7	56K +/- 1%		7	DIS-P 0.3
8	75K +/- 1%		8	DIS-P 0.4
9	100K +/- 1%		9	DIS-P 1.0
10	130K +/- 1%		10	UMA 0.2
11	160K +/- 1%		11	UMA 0.3
12	200K +/- 1%		12	UMA 0.4
13	240K +/- 1%		13	UMA 1.0
14	270K +/- 1%		14	
15	330K +/- 1%		15	
16	430K +/- 1%		16	
17	560K +/- 1%		17	
18	750K +/- 1%		18	
19	NC		19	

<b>PCH</b>	USB PORT#	DESTINATION
	0	USB Conn 1 (Power share)
	1	USB Conn 3 (Power share)
	2	USB Conn 2 (Power share)
	3	USB Conn 4 (Power share)
	4	JMINI1 (WLAN)
	5	None
	6	None
	7	None
	8	None
	9	Touch screen
	10	None
	11	None
	12	CAMERA
13	None	

PCI EXPRESS	DESTINATION
Lane 1	None
Lane 2	None
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

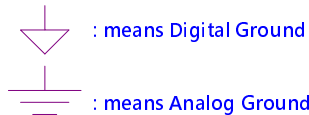
SATA	DESTINATION
SATA0	HDD
SATA1	SSD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

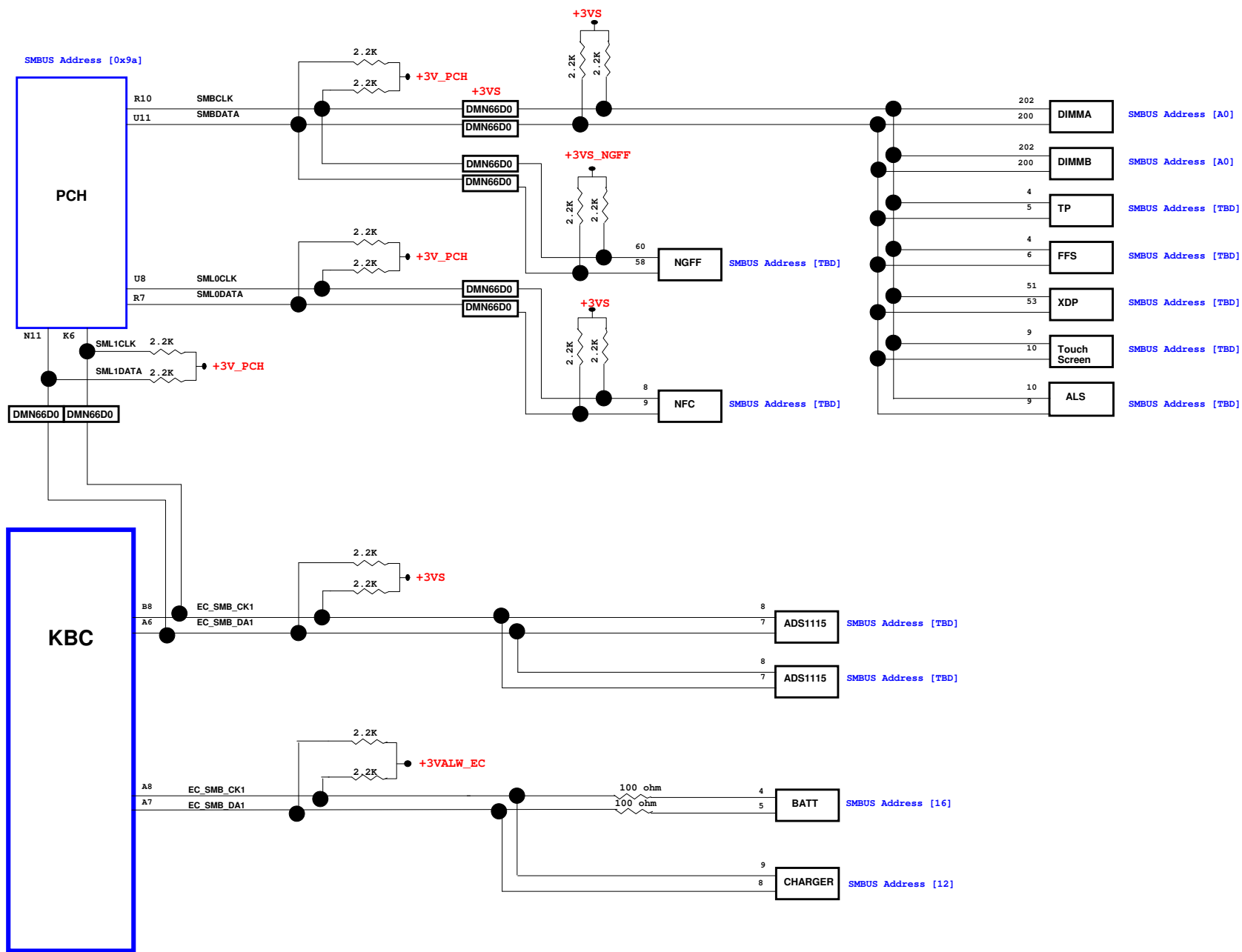
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

USB3	DESTINATION
1	USB Conn 1 (Power share)
2	USB Conn 3 (Power share)
3	USB Conn 2 (Power share)
4	USB Conn 4 (Power share)

<b>CLK</b>	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	CLK_PCI_TPM
	CLKOUT_PCIE1	None	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
CLKOUT_PEG_B	None			

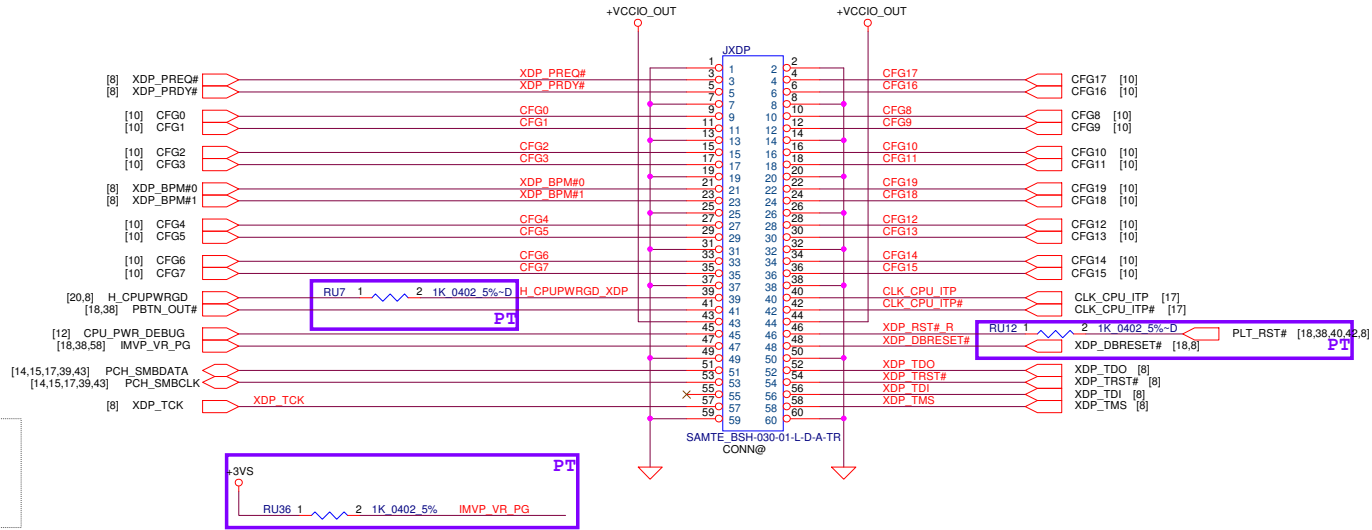
Symbol Note :





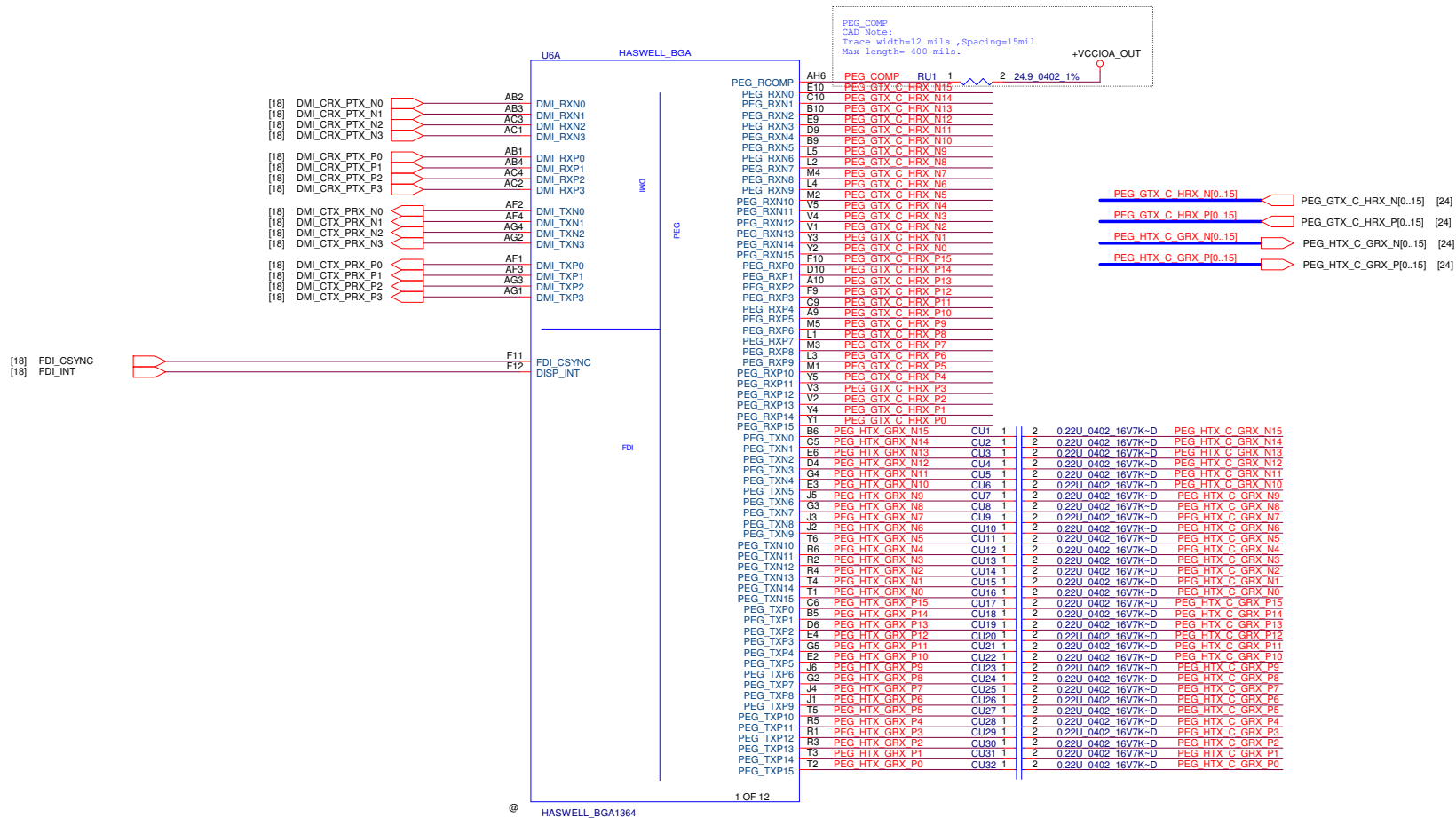
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Issued Date	2011/08/25	Deciphered Date	2012/07/15	<i>Compal Electronics, Inc.</i>
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				<b>SMBus Block Diagram</b>
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# XDP CONN

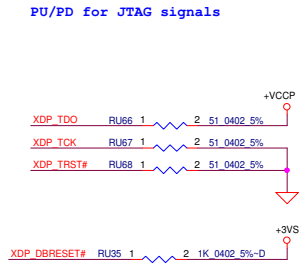
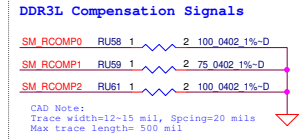
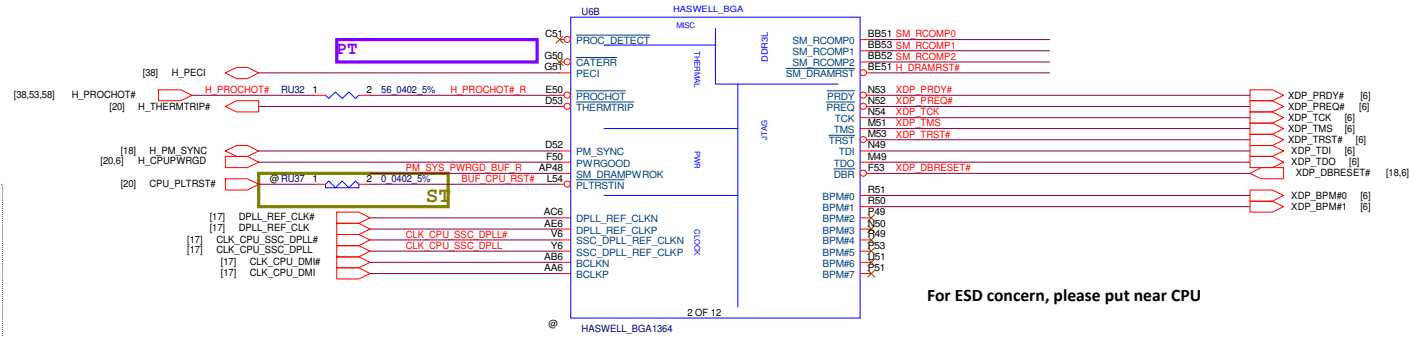
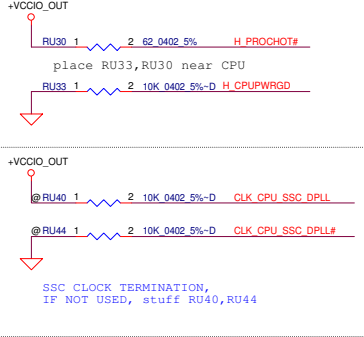


The resistor for HOOK2 should be placed such that the stub is very small on CFG0 net

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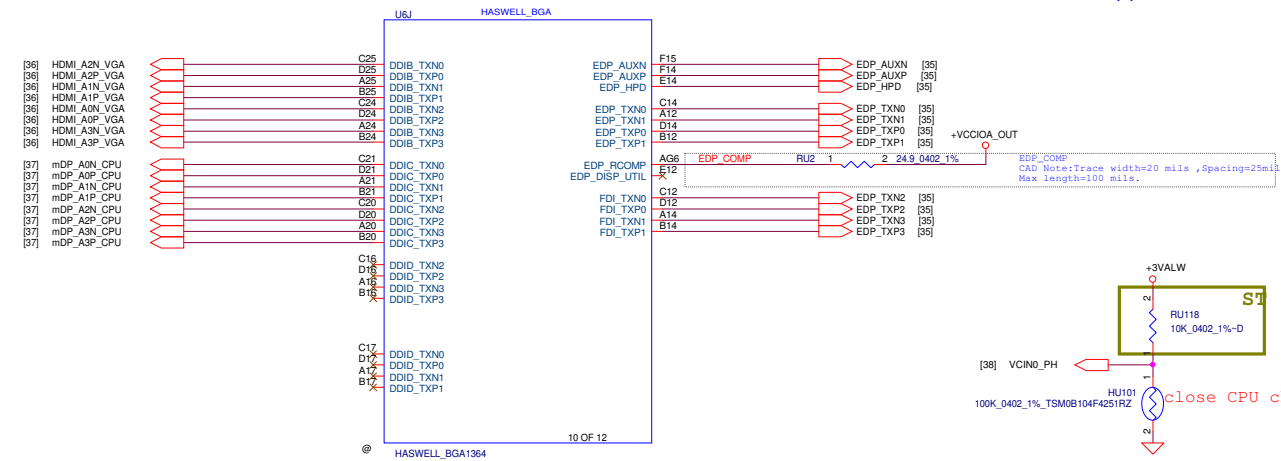
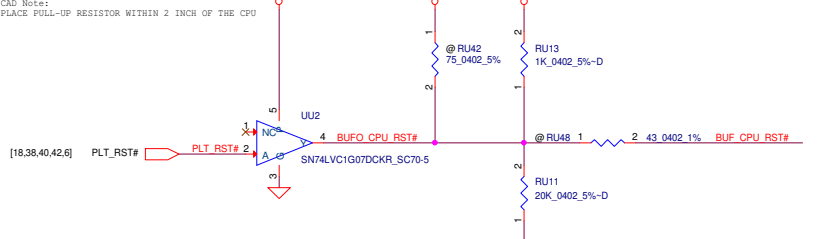


### Processor Pullups

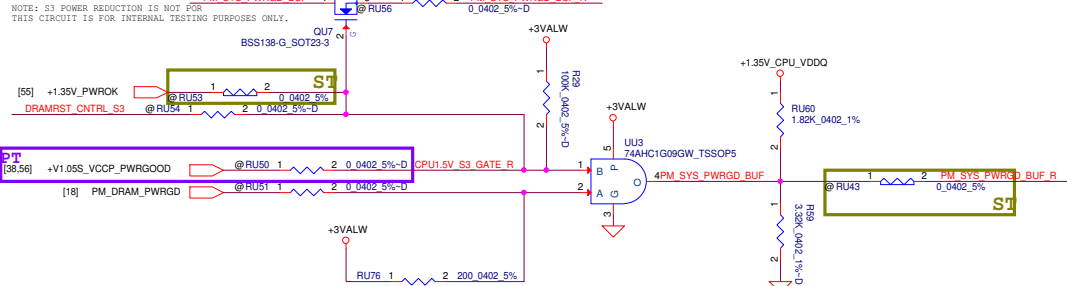


For ESD concern, please put near CPU

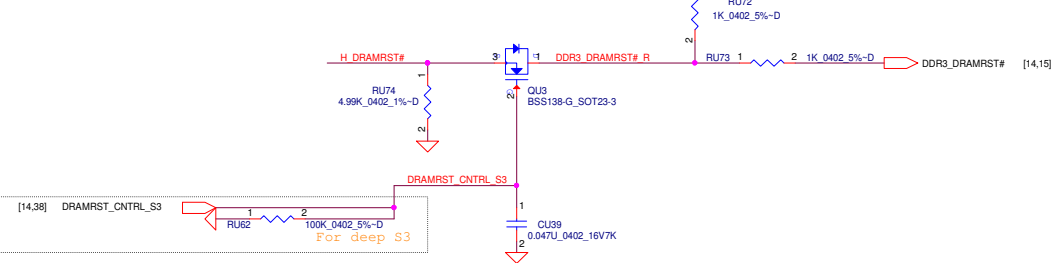
### Buffered reset to CPU



### SM\_DRAMPWROK



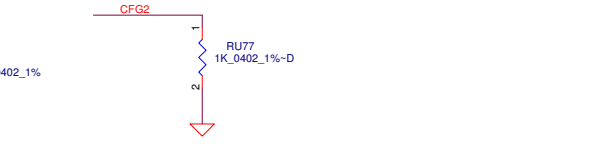
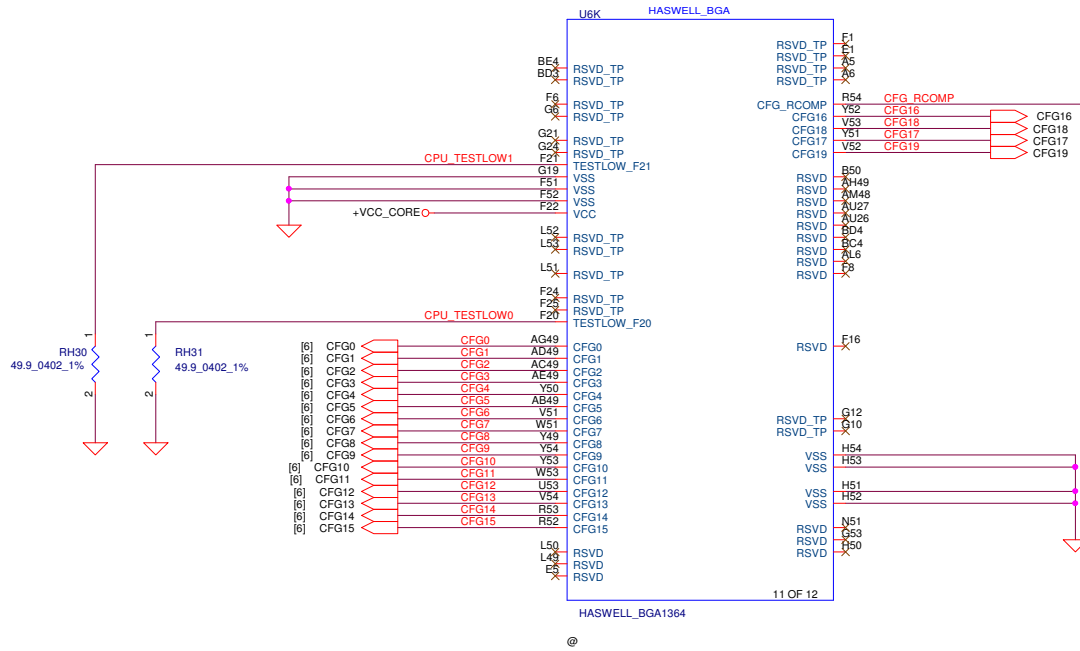
### S3 circuit: DRAM\_RST# to memory



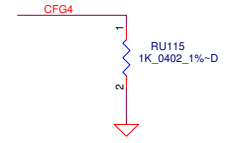
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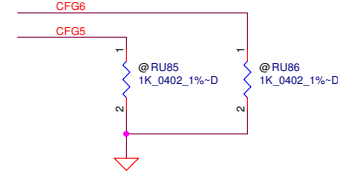
# CFG Straps for Processor



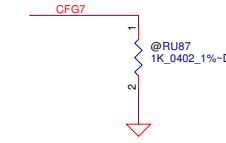
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



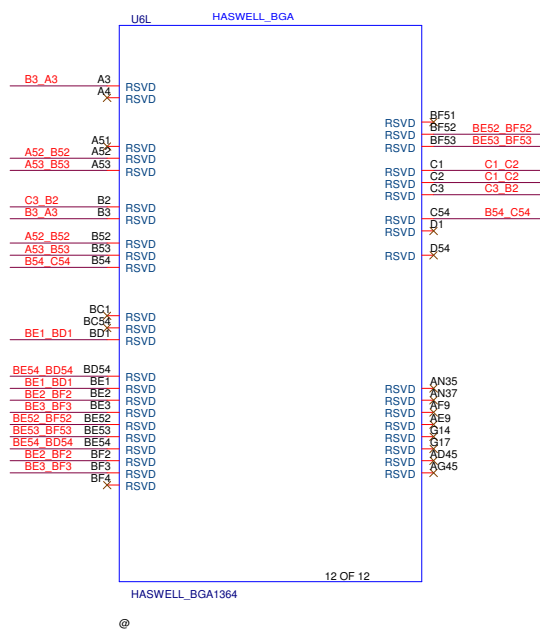
Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port * 0: Enabled; An external Display Port device is connected to the Embedded Display Port



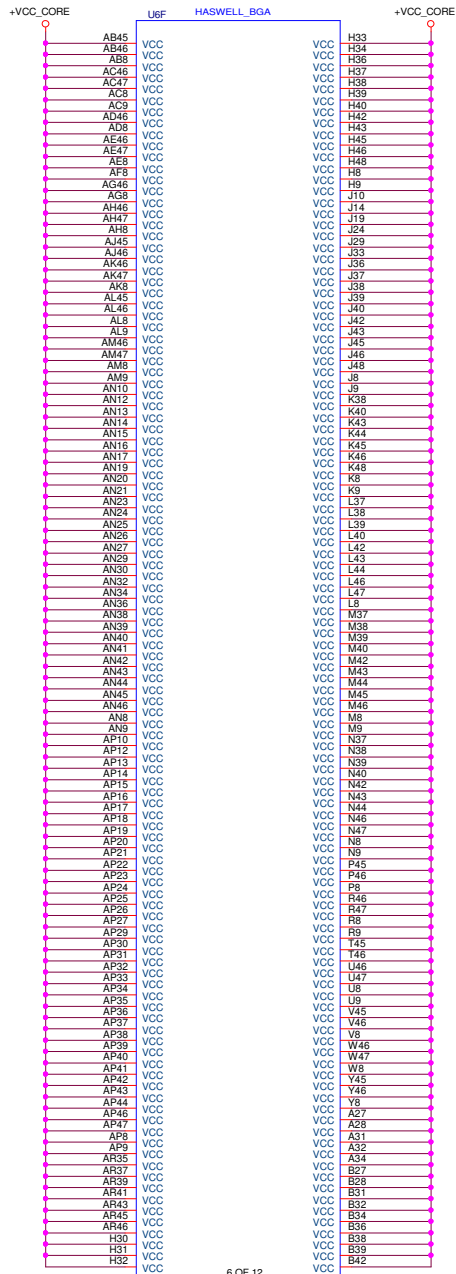
PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

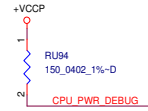
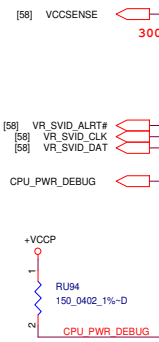
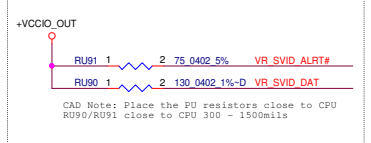
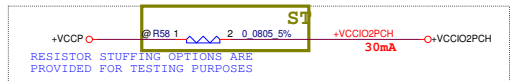
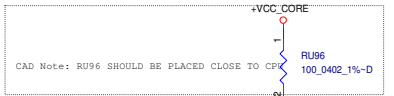
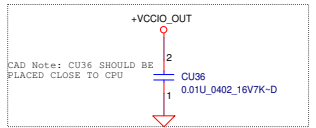
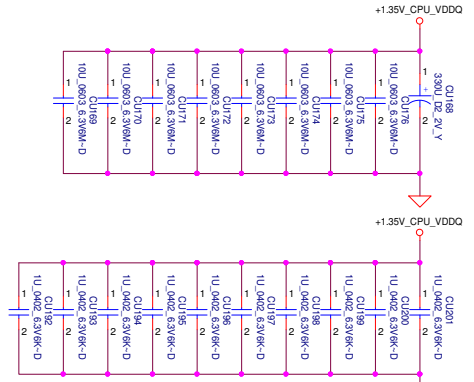
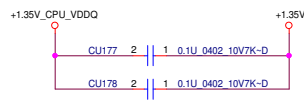


55A

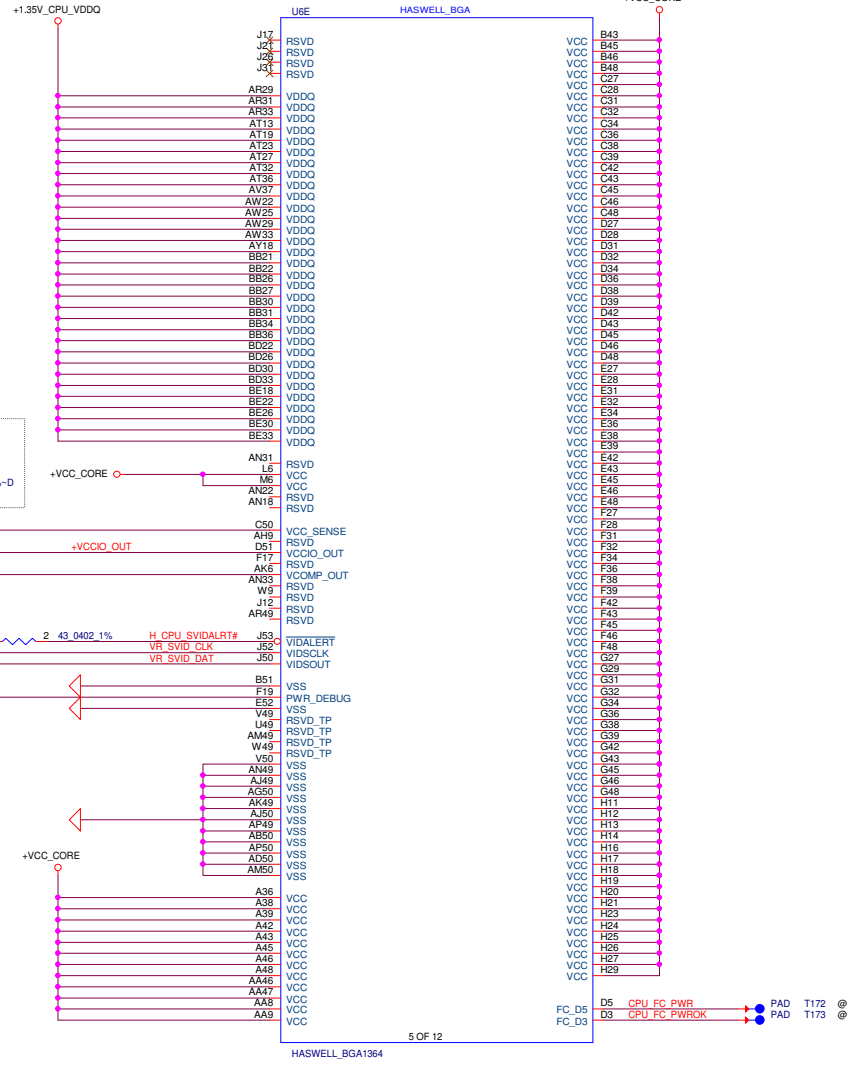
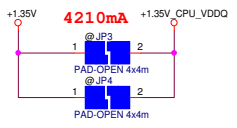


HASWELL\_BGA1364

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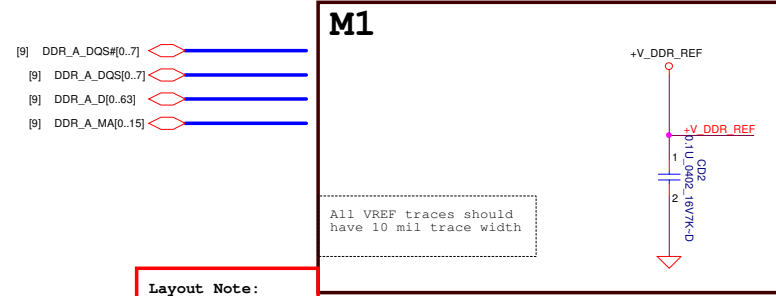


**+1.35V\_CPU\_VDDQ Source**

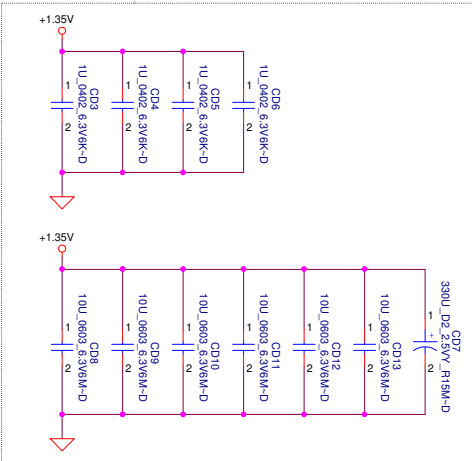


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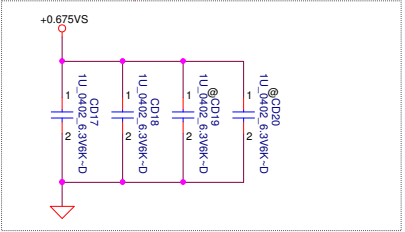




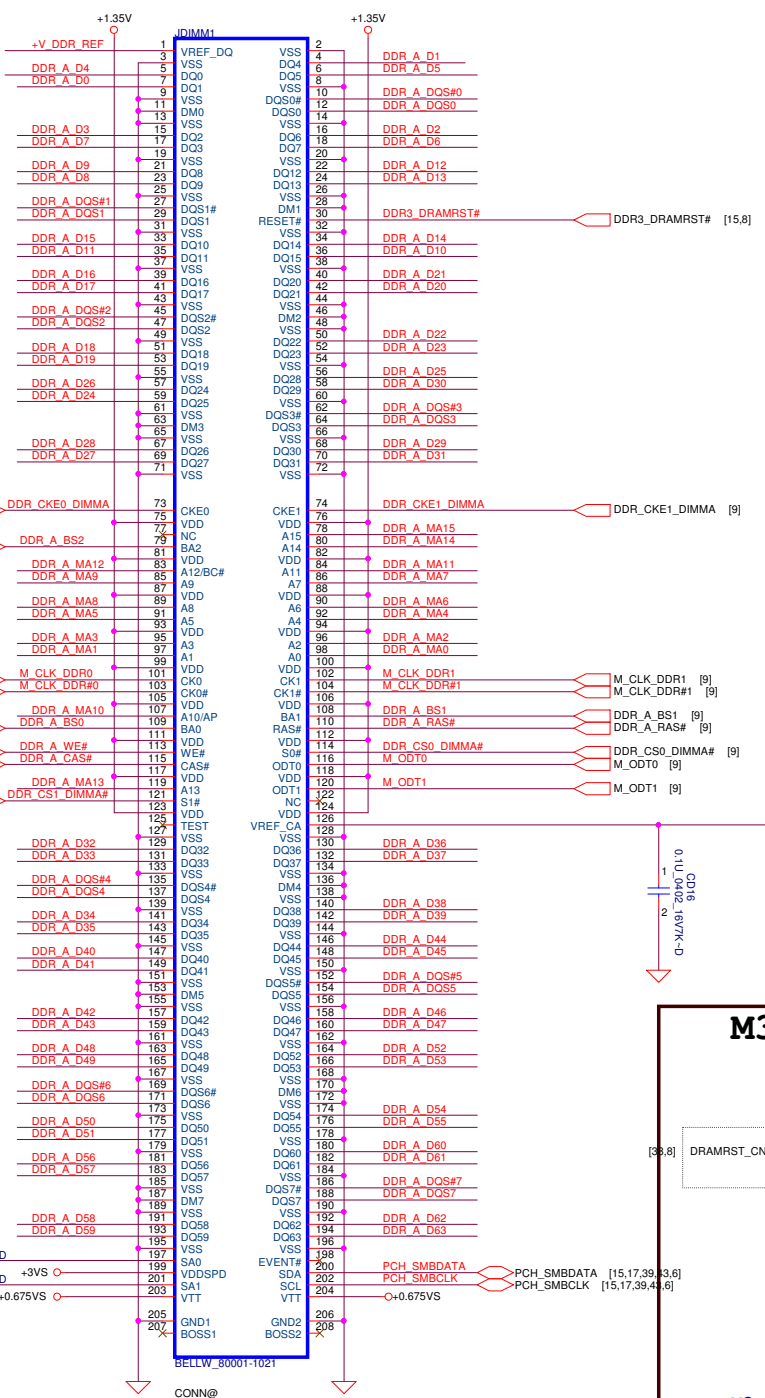
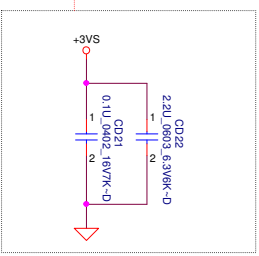
**Layout Note:**  
Place near JDIMM1



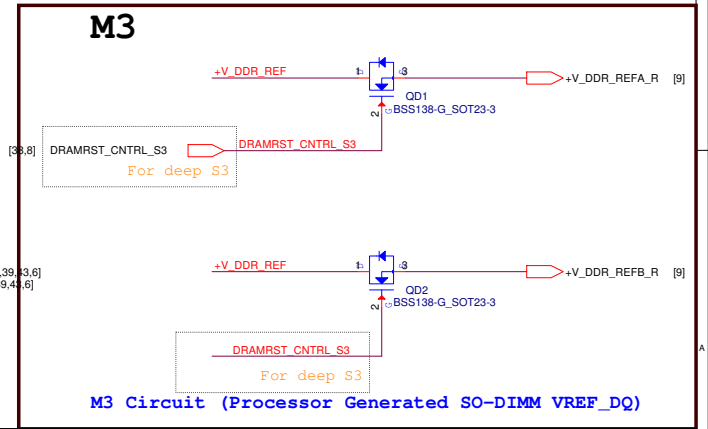
**Layout Note:**  
Place near JDIMM1.203, 204



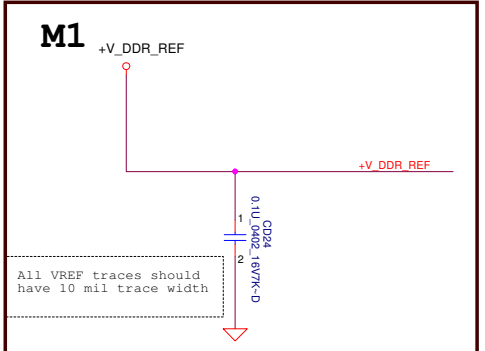
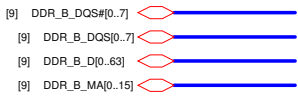
**Layout Note:**  
Place near JDIMM1.199



All VREF traces should have 10 mil trace width

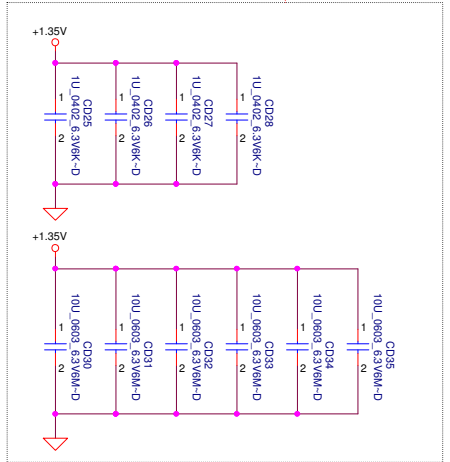


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				<b>DDRIII DIMMA</b>
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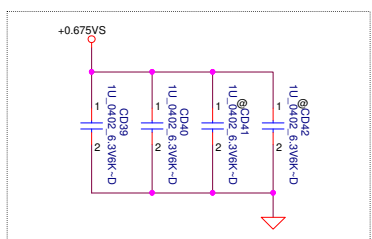


All VREF traces should have 10 mil trace width

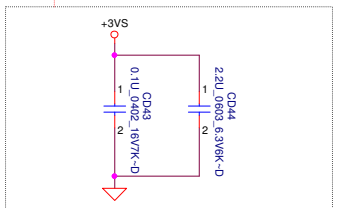
Layout Note:  
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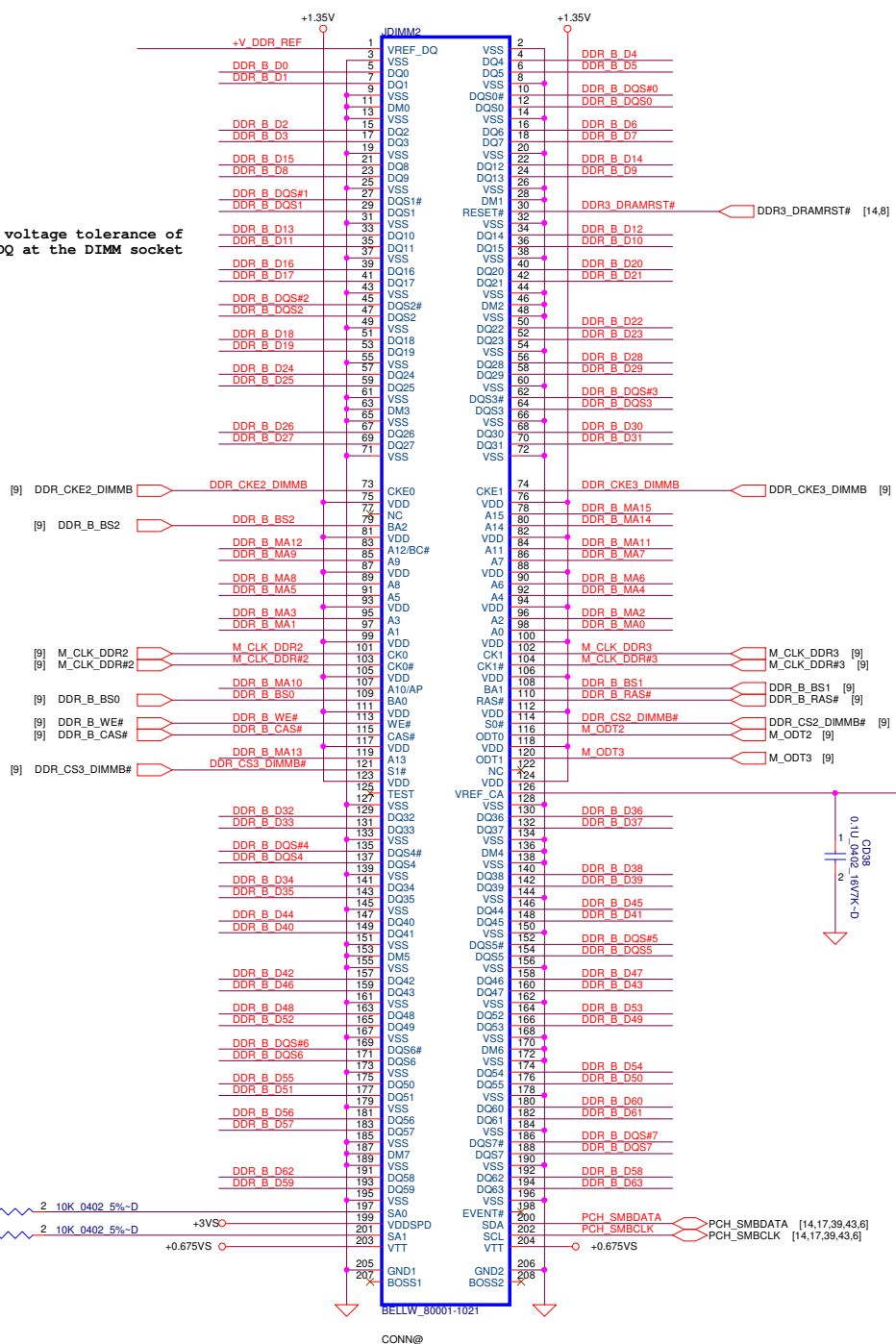
Layout Note:  
Place near JDIMMB.203,204



Layout Note:  
Place near JDIMMB.199



Note:  
Check voltage tolerance of VREF\_DQ at the DIMM socket

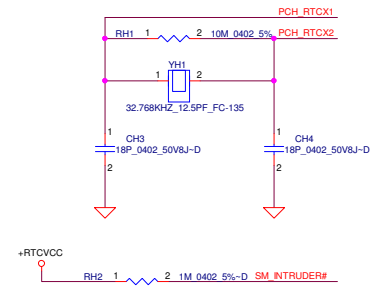


All VREF traces should have 10 mil trace width

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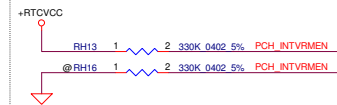
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Title	DDRIII DIMMB
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# RTC CRYSTAL

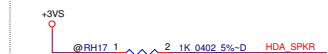


# PCH Strap PIN

## INTVRMEN Integrated 1.05V VRM Enable/Disable

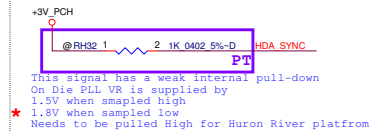


## SPKR No Reboot

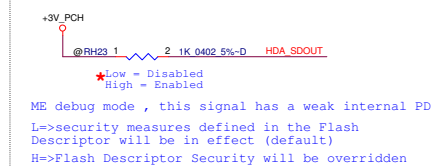


If the signal is sampled high, this indicate that the system is strapped to the "No Reboot" mode

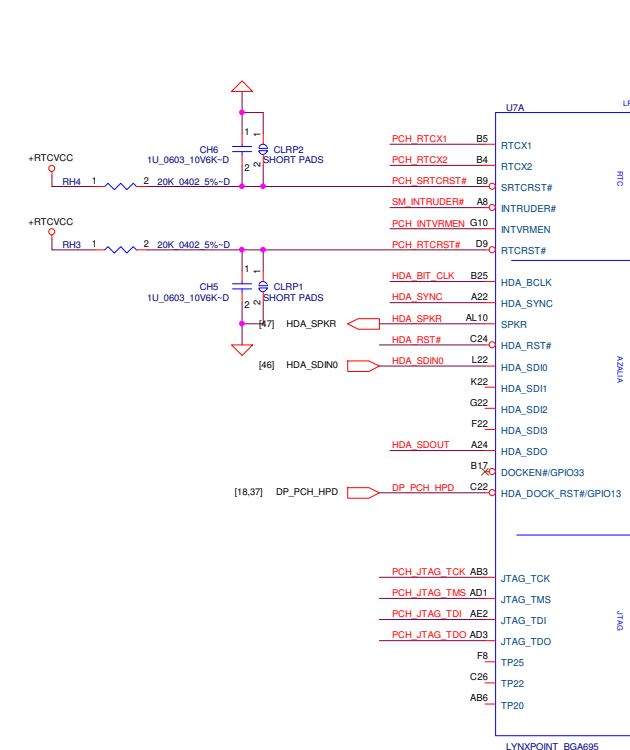
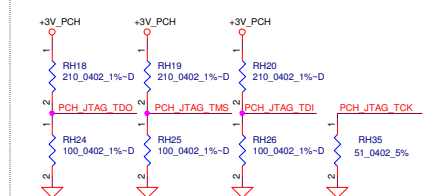
## HDA\_SYNC On-Die PLL Voltage Regulator Voltage Select



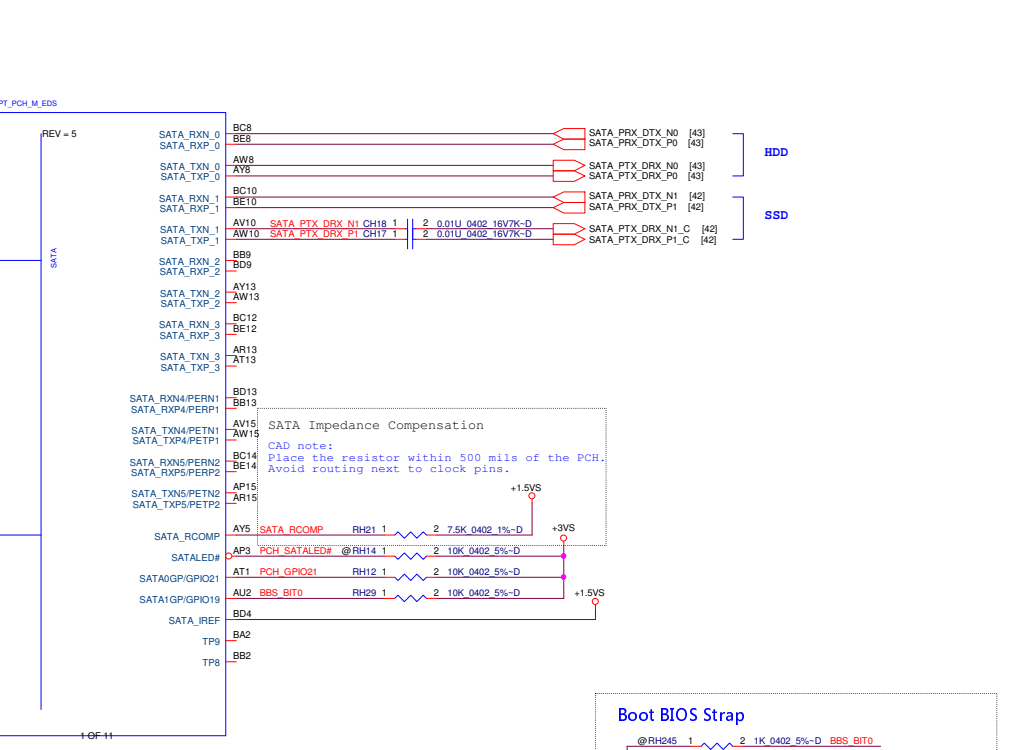
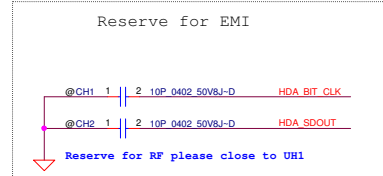
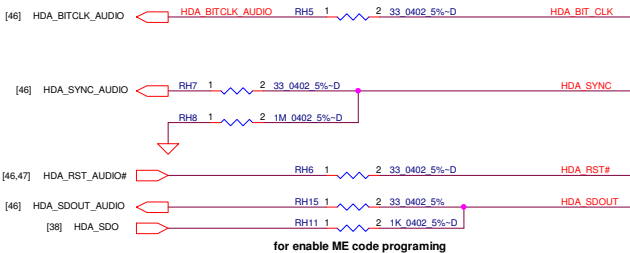
## HDA\_SDO Flash Descriptor Security Override/Intel ME Debug Mode



## JTAG



## HD Audio



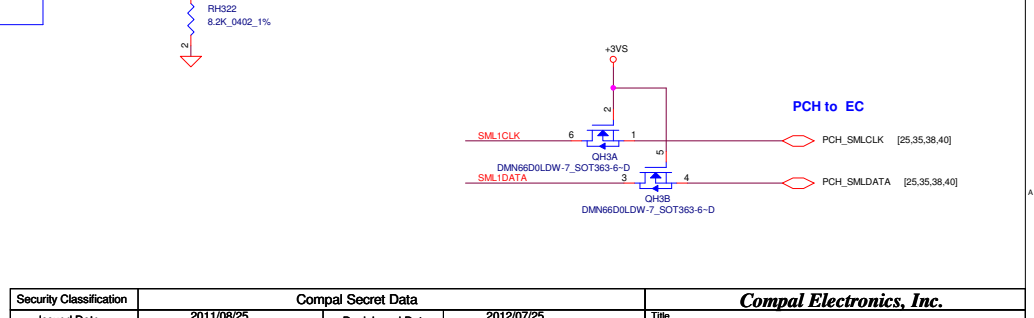
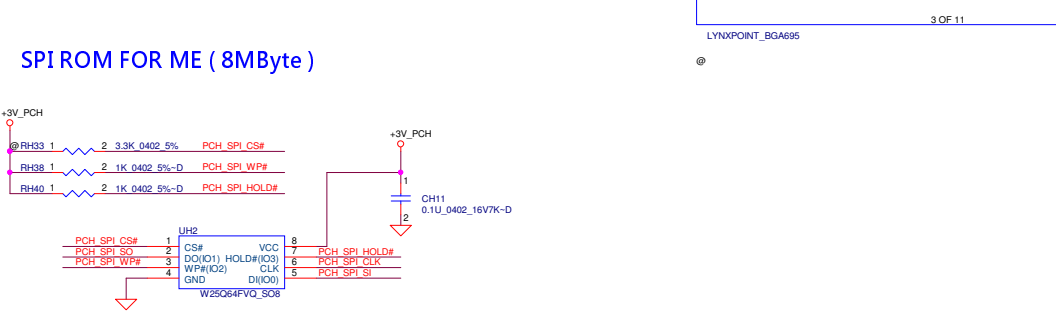
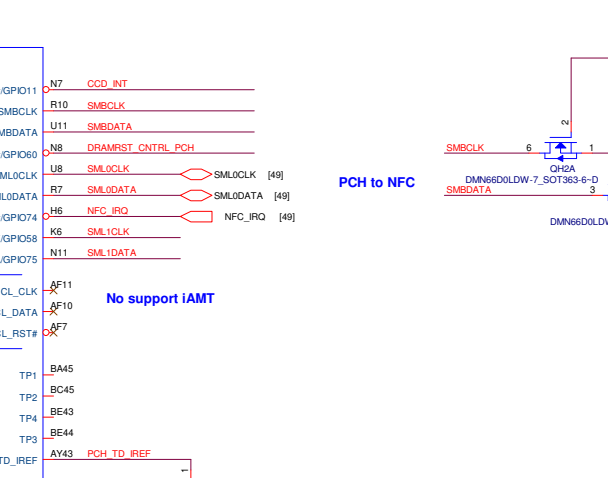
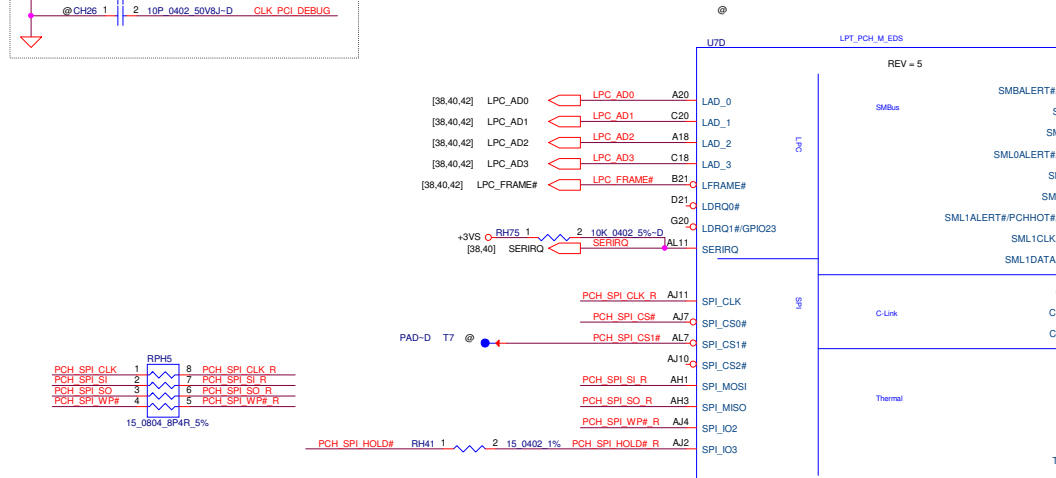
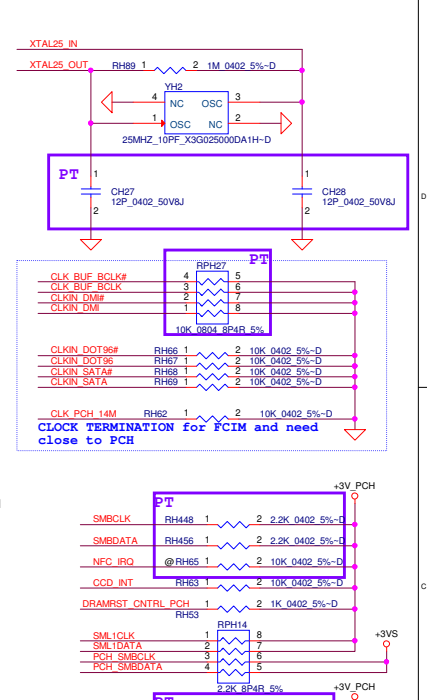
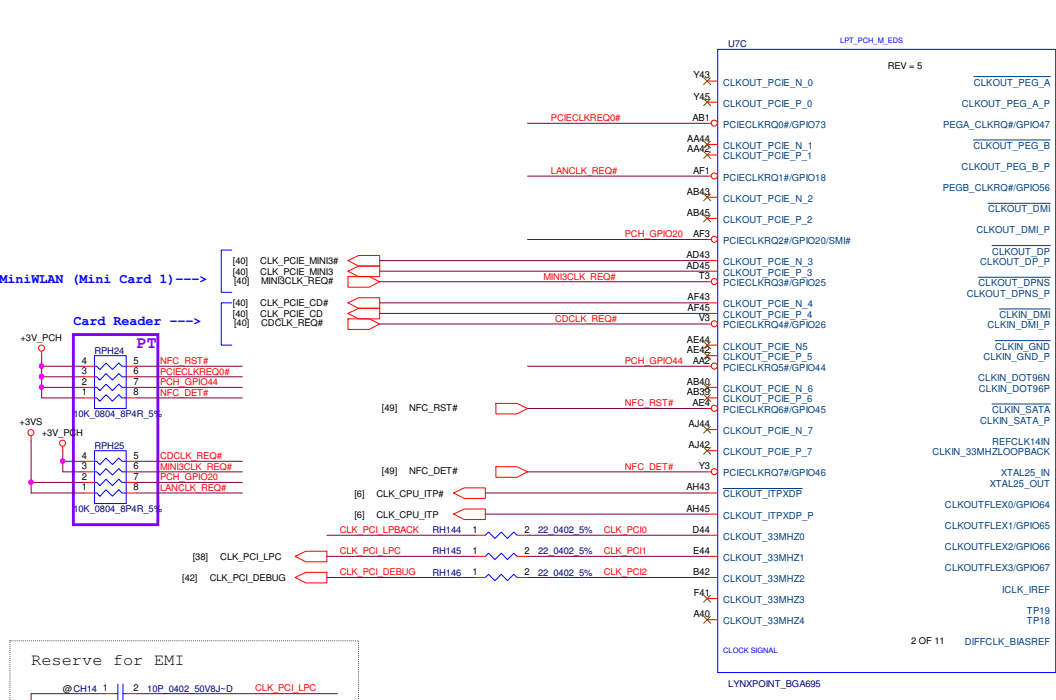
### Boot BIOS Strap

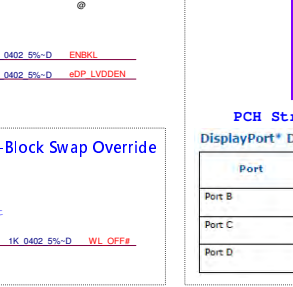
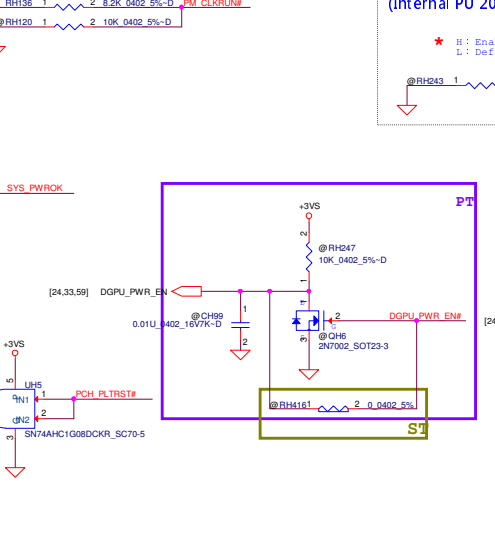
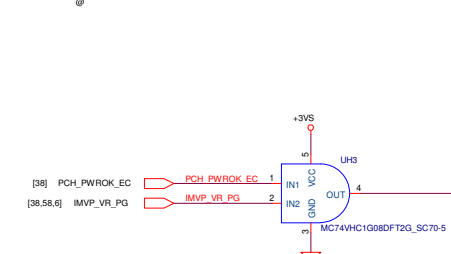
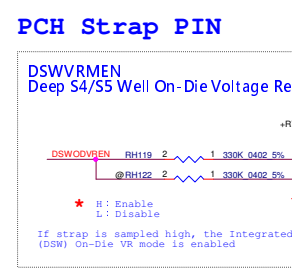
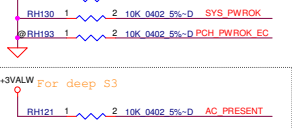
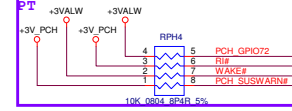
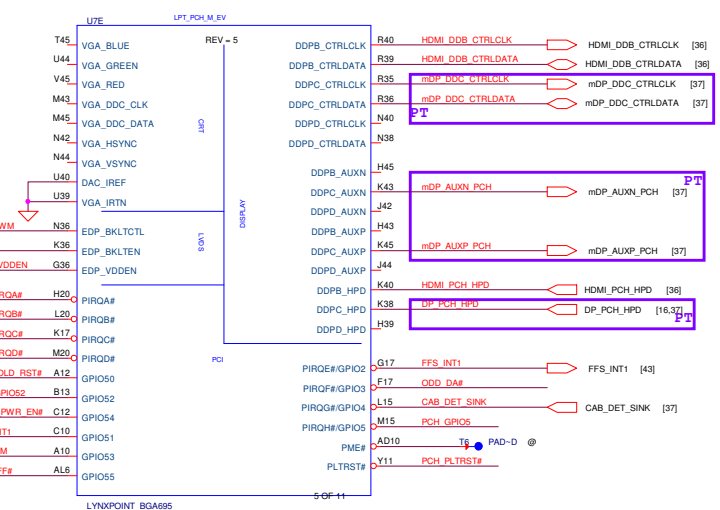
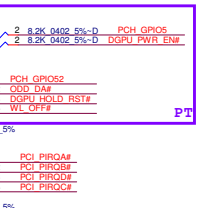
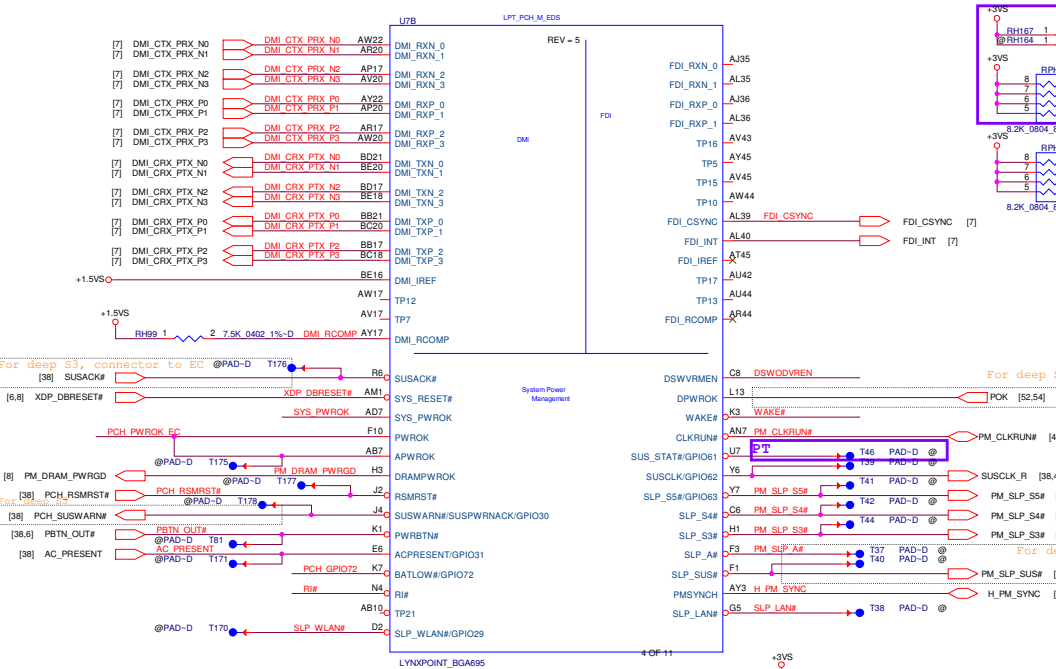
GPIO19 => BBS\_BIT0  
GPIO51 => BBS\_BIT1

Boot BIOS Strap		
BBS_BIT[1]	BBS_BIT[0]	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

## RTC Battery



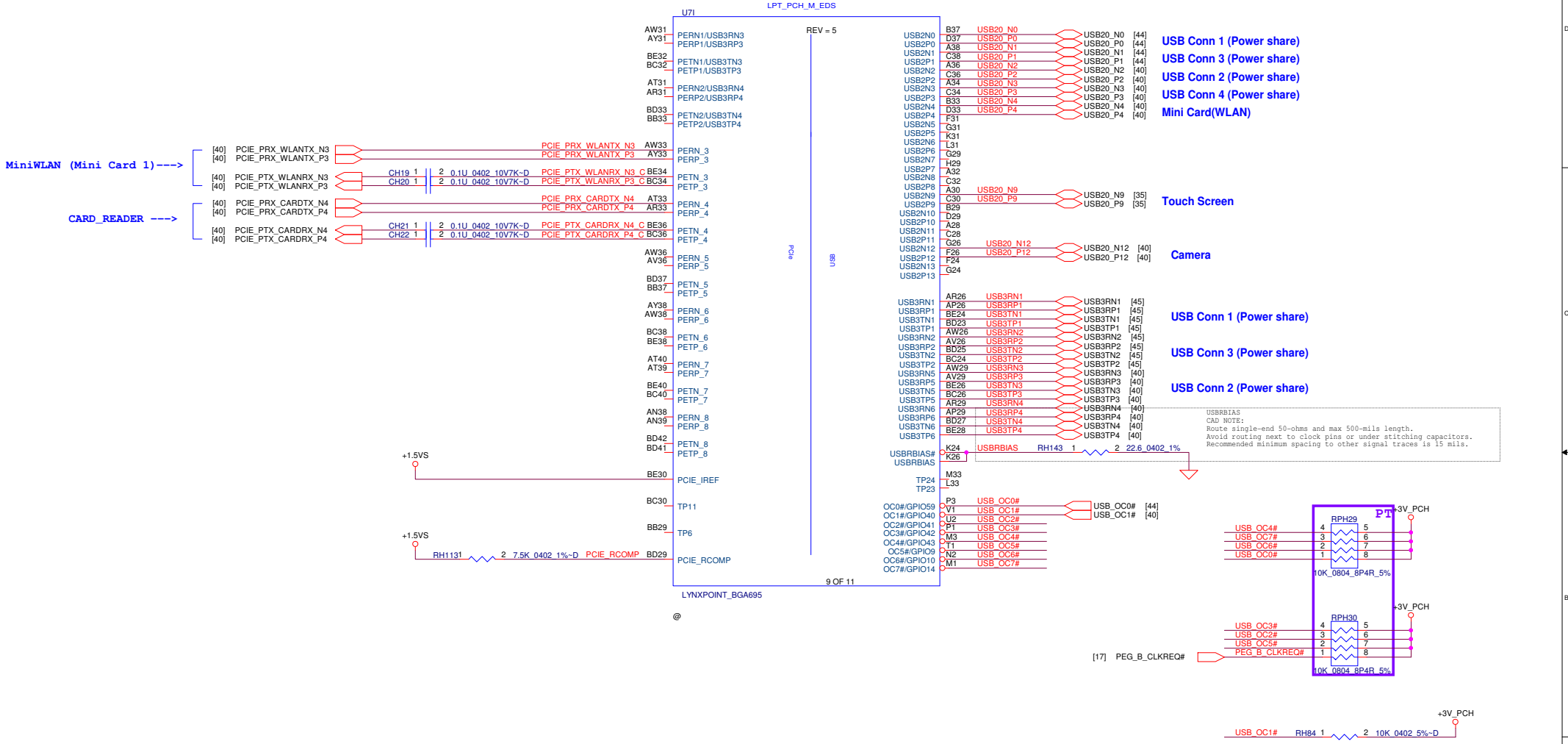




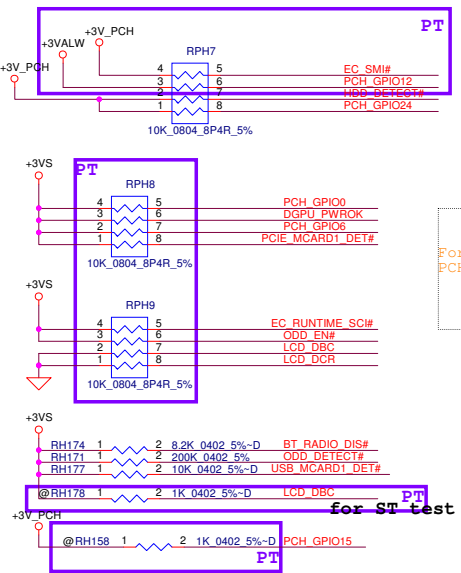
### PCH Strap PIN

#### DisplayPort\* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect



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### PCH Strap PIN

**GPIO37 TLS Confidentiality**  
 Low - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality  
 High - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

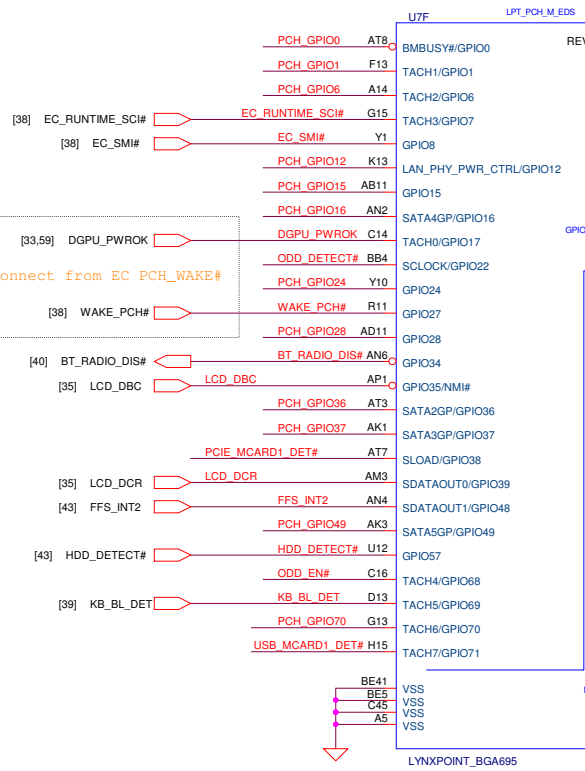
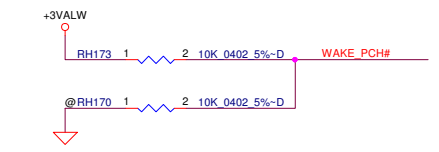
★

**GPIO28 On-Die PLL Voltage Regulator**  
 This signal has a weak internal pull up

★ H : On-Die voltage regulator enable  
 L : On-Die PLL Voltage Regulator disable

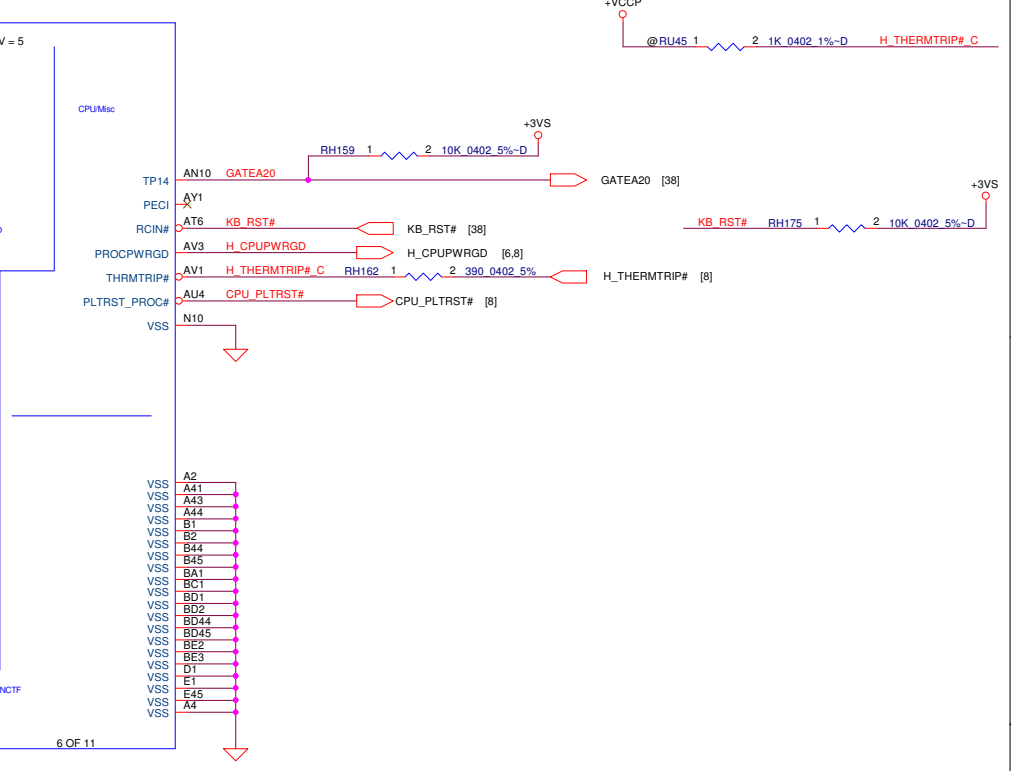
**SATA2GP/GPIO36 Reserved**

When Unused as GPIO or SATA\*GP -  
 Use 8.2K-10K pull-down to ground



For deep S3,  
 PCH\_GPIO27 connect from EC PCH\_WAKE#

config	GPIO16, GPIO49
★ USB X4, PCIEX8, SATAX6	11
USB X6, PCIEX8, SATAX4	01



**DGPU Board ID Optional**

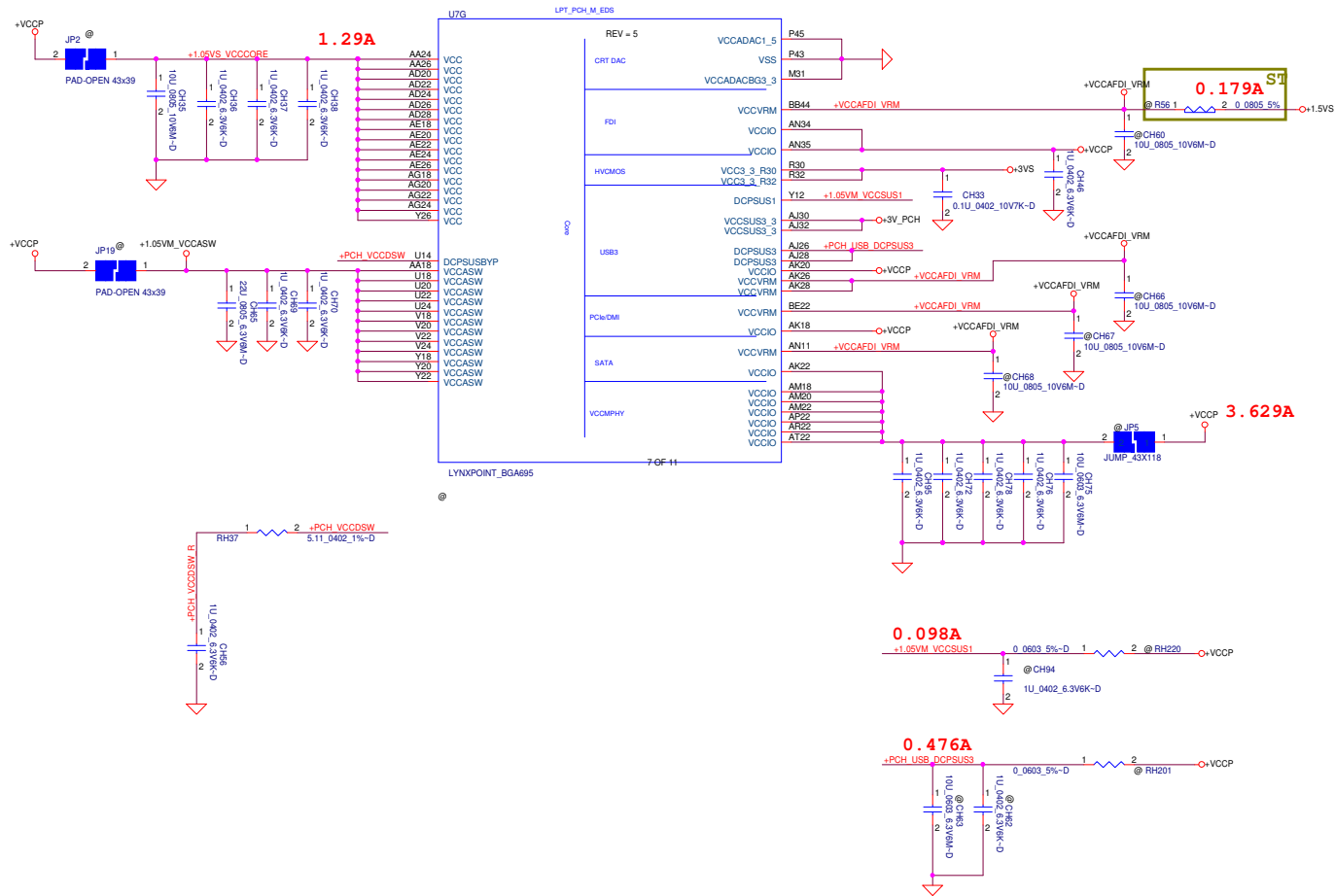
N14@ RH168  
 10K\_0402\_5%-D

N15@ RH172  
 10K\_0402\_5%-D

PCH_GPIO1	
N14P	1 = N14P-GT 0 = N15P

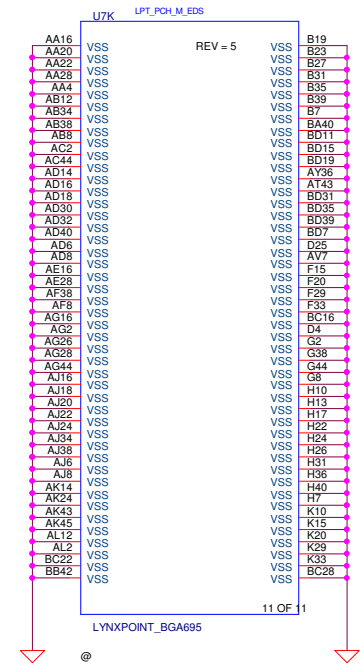
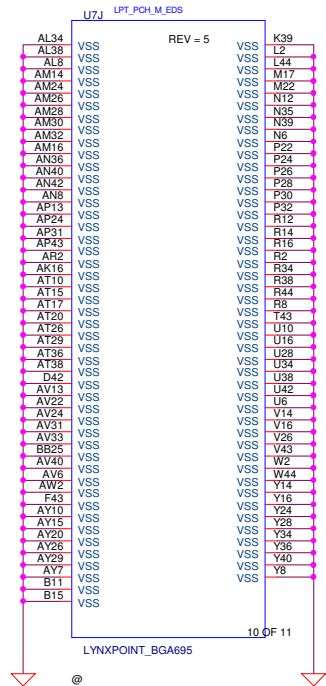
N163  
 10K\_0402\_5%-D

PCH_GPIO70	
DIS	1
UMA	0



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				Size
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				Sheet 21 of 62





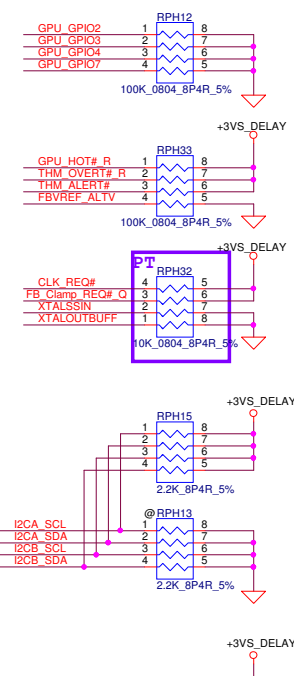
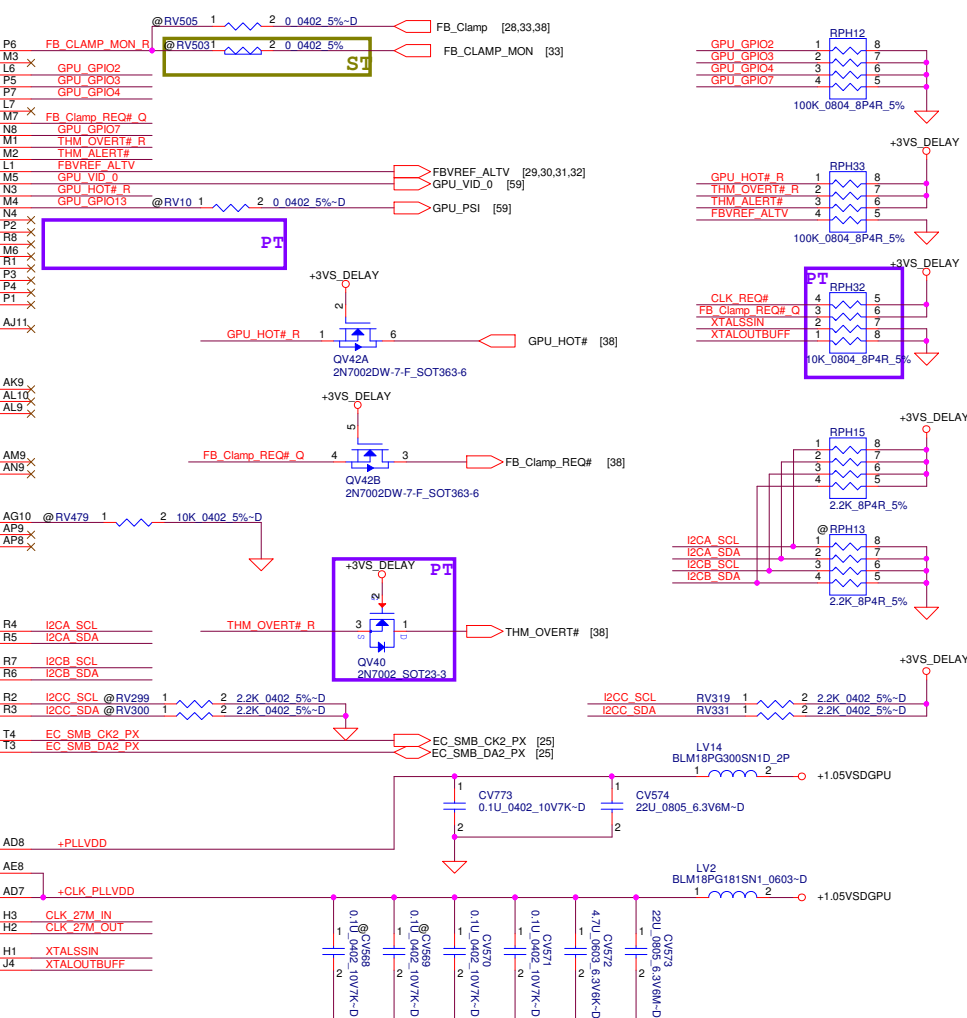
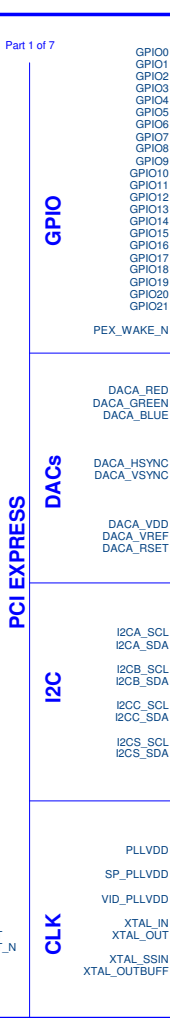
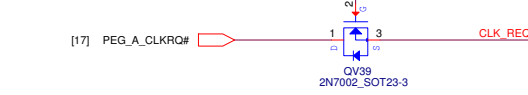
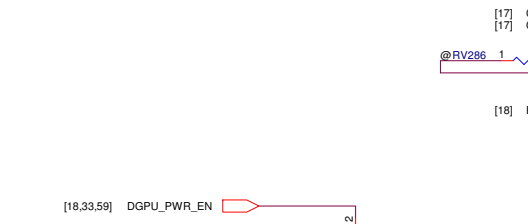
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- [7] PEG\_HTX\_C\_GRX\_P[0..15] → PEG\_HTX\_C\_GRX\_P[0..15]
- [7] PEG\_HTX\_C\_GRX\_N[0..15] → PEG\_HTX\_C\_GRX\_N[0..15]
- [7] PEG\_GTX\_C\_HRX\_P[0..15] → PEG\_GTX\_C\_HRX\_P[0..15]
- [7] PEG\_GTX\_C\_HRX\_N[0..15] → PEG\_GTX\_C\_HRX\_N[0..15]

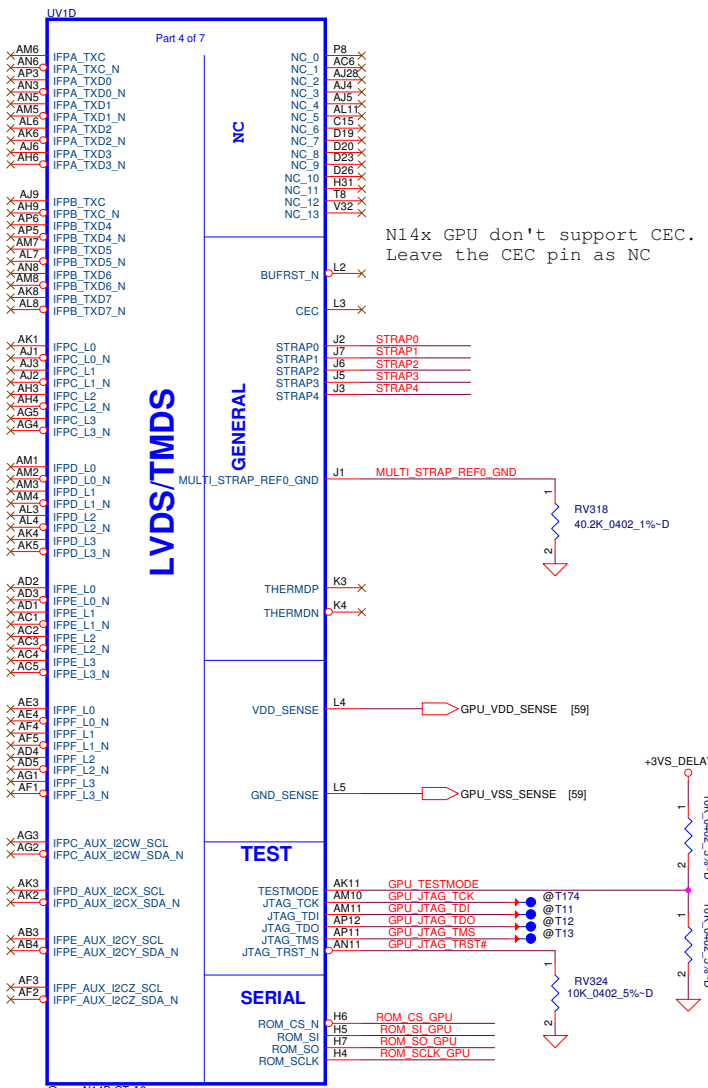
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PEG GTX C HRX P1	CV533	2	1	0.22U	0402	16V7K-D	PEG GTX HRX P1
PEG GTX C HRX N1	CV534	2	1	0.22U	0402	16V7K-D	PEG GTX HRX N1
PEG GTX C HRX P2	CV535	2	1	0.22U	0402	16V7K-D	PEG GTX HRX P2
PEG GTX C HRX N2	CV536	2	1	0.22U	0402	16V7K-D	PEG GTX HRX N2
PEG GTX C HRX P3	CV537	2	1	0.22U	0402	16V7K-D	PEG GTX HRX P3
PEG GTX C HRX N3	CV538	2	1	0.22U	0402	16V7K-D	PEG GTX HRX N3
PEG GTX C HRX P4	CV539	2	1	0.22U	0402	16V7K-D	PEG GTX HRX P4
PEG GTX C HRX N4	CV540	2	1	0.22U	0402	16V7K-D	PEG GTX HRX N4
PEG GTX C HRX P5	CV541	2	1	0.22U	0402	16V7K-D	PEG GTX HRX P5
PEG GTX C HRX N5	CV542	2	1	0.22U	0402	16V7K-D	PEG GTX HRX N5
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PEG GTX C HRX P7	CV545	2	1	0.22U	0402	16V7K-D	PEG GTX HRX P7
PEG GTX C HRX N7	CV546	2	1	0.22U	0402	16V7K-D	PEG GTX HRX N7
PEG GTX C HRX P8	CV547	2	1	0.22U	0402	16V7K-D	PEG GTX HRX P8
PEG GTX C HRX N8	CV548	2	1	0.22U	0402	16V7K-D	PEG GTX HRX N8
PEG GTX C HRX P9	CV550	2	1	0.22U	0402	16V7K-D	PEG GTX HRX P9
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PEG GTX C HRX P11	CV558	2	1	0.22U	0402	16V7K-D	PEG GTX HRX P11
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PEG GTX C HRX P14	CV564	2	1	0.22U	0402	16V7K-D	PEG GTX HRX P14
PEG GTX C HRX N14	CV565	2	1	0.22U	0402	16V7K-D	PEG GTX HRX N14
PEG GTX C HRX P15	CV566	2	1	0.22U	0402	16V7K-D	PEG GTX HRX P15
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PEG_HTX_C_GRX_N0	AM12	PEX_RX0_N
PEG_HTX_C_GRX_P1	AN14	PEX_RX1
PEG_HTX_C_GRX_N1	AM14	PEX_RX1_N
PEG_HTX_C_GRX_P2	AP14	PEX_RX2
PEG_HTX_C_GRX_N2	AM15	PEX_RX2_N
PEG_HTX_C_GRX_P3	AN15	PEX_RX3
PEG_HTX_C_GRX_N3	AM15	PEX_RX3_N
PEG_HTX_C_GRX_P4	AN17	PEX_RX4
PEG_HTX_C_GRX_N4	AM17	PEX_RX4_N
PEG_HTX_C_GRX_P5	AP17	PEX_RX5
PEG_HTX_C_GRX_N5	AM18	PEX_RX5_N
PEG_HTX_C_GRX_P6	AN18	PEX_RX6
PEG_HTX_C_GRX_N6	AM18	PEX_RX6_N
PEG_HTX_C_GRX_P7	AN20	PEX_RX7
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PEG_HTX_C_GRX_N9	AM21	PEX_RX9_N
PEG_HTX_C_GRX_P10	AN23	PEX_RX10
PEG_HTX_C_GRX_N10	AM23	PEX_RX10_N
PEG_HTX_C_GRX_P11	AP23	PEX_RX11
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PEG_HTX_C_GRX_P12	AN24	PEX_RX12
PEG_HTX_C_GRX_N12	AM24	PEX_RX12_N
PEG_HTX_C_GRX_P13	AN26	PEX_RX13
PEG_HTX_C_GRX_N13	AM26	PEX_RX13_N
PEG_HTX_C_GRX_P14	AP26	PEX_RX14
PEG_HTX_C_GRX_N14	AM27	PEX_RX14_N
PEG_HTX_C_GRX_P15	AN27	PEX_RX15
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PEG GTX HRX P0	AK14	PEX_TX0
PEG GTX HRX N0	AJ14	PEX_TX0_N
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PEG GTX HRX N1	AG14	PEX_TX1_N
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PEG GTX HRX N3	AK16	PEX_TX3_N
PEG GTX HRX P4	AK17	PEX_TX4
PEG GTX HRX N4	AJ17	PEX_TX4_N
PEG GTX HRX P5	AH17	PEX_TX5
PEG GTX HRX N5	AG17	PEX_TX5_N
PEG GTX HRX P6	AK18	PEX_TX6
PEG GTX HRX N6	AJ18	PEX_TX6_N
PEG GTX HRX P7	AL19	PEX_TX7
PEG GTX HRX N7	AK19	PEX_TX7_N
PEG GTX HRX P8	AK20	PEX_TX8
PEG GTX HRX N8	AJ20	PEX_TX8_N
PEG GTX HRX P9	AH20	PEX_TX9
PEG GTX HRX N9	AG20	PEX_TX9_N
PEG GTX HRX P10	AK21	PEX_TX10
PEG GTX HRX N10	AJ21	PEX_TX10_N
PEG GTX HRX P11	AL22	PEX_TX11
PEG GTX HRX N11	AK22	PEX_TX11_N
PEG GTX HRX P12	AK23	PEX_TX12
PEG GTX HRX N12	AJ23	PEX_TX12_N
PEG GTX HRX P13	AH23	PEX_TX13
PEG GTX HRX N13	AG23	PEX_TX13_N
PEG GTX HRX P14	AK24	PEX_TX14
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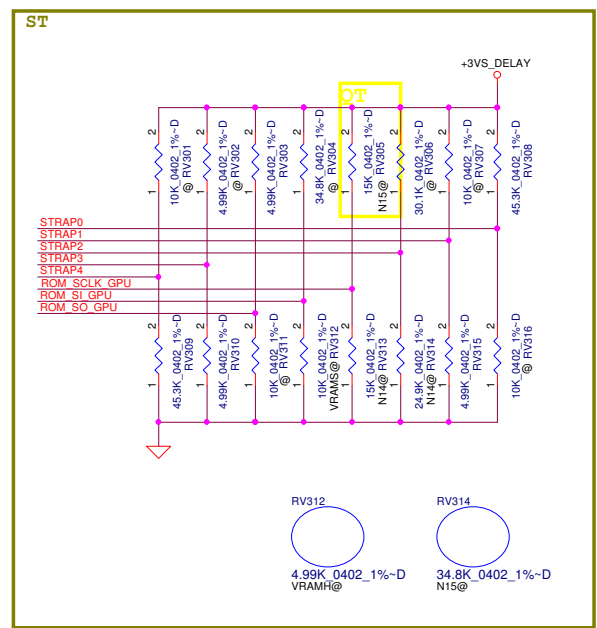


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Date:	Tuesday, September 03, 2013	Sheet	24	of 62



N14x GPU don't support CEC.  
Leave the CEC pin as NC

### Straps

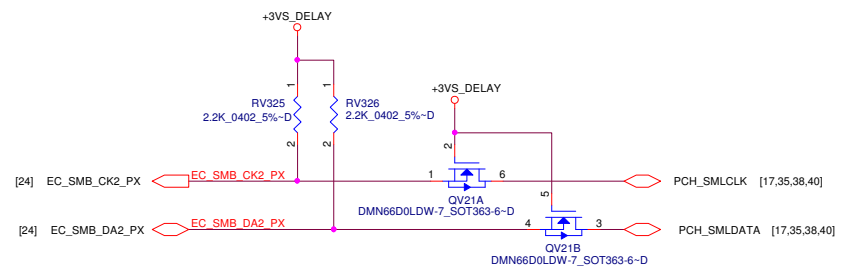
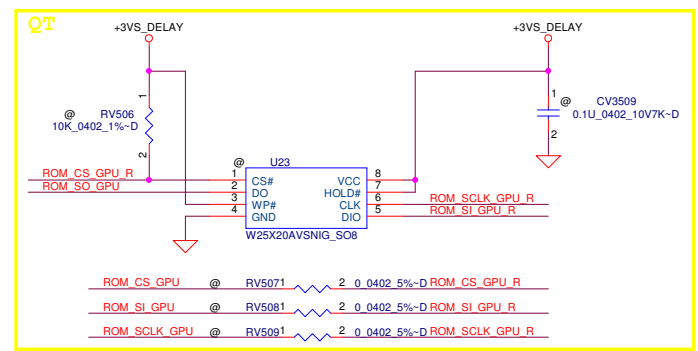


	N14P-GT	N15P-Q1
ROM_SCL	PD 15K	PU 15K
ROM_SI		PD 10K
ROM_SO		PU 5K
STRAP[0]		PU 45K
STRAP[1]		PD 5K
STRAP[2]	PD 24.9K	PD 35K
STRAP[3]		PD 5K
STRAP[4]		PD 45K

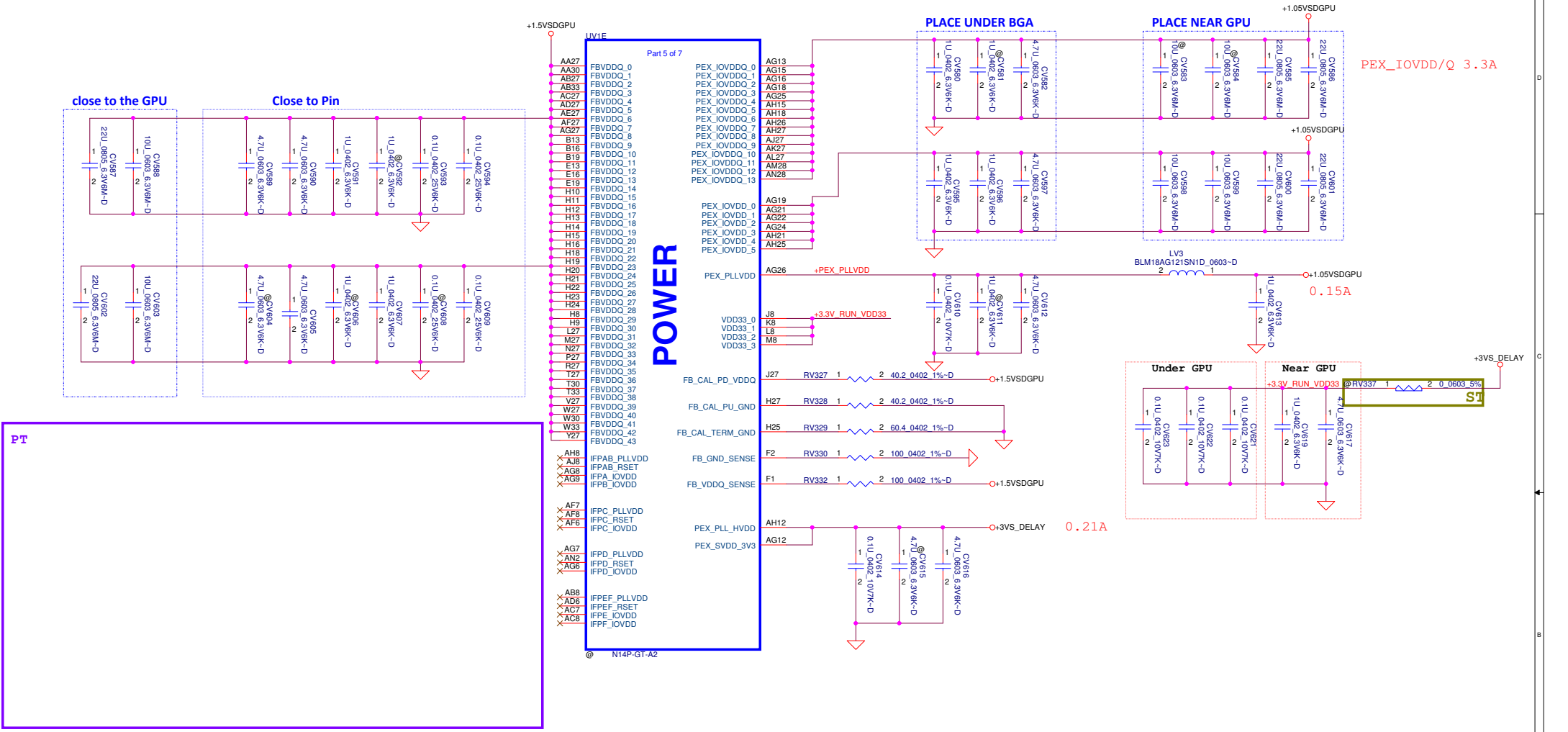
Change to PU35K in N15 for use ext ROM

Hynix "0". ROM\_Si=PD 5K ohm Samsung"1". ROM\_Si=PD 10K ohm

### SPI ROM for N14E-GL ( 2M bit/256K byte )



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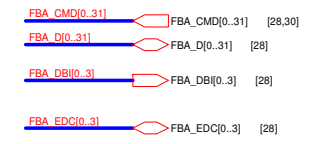
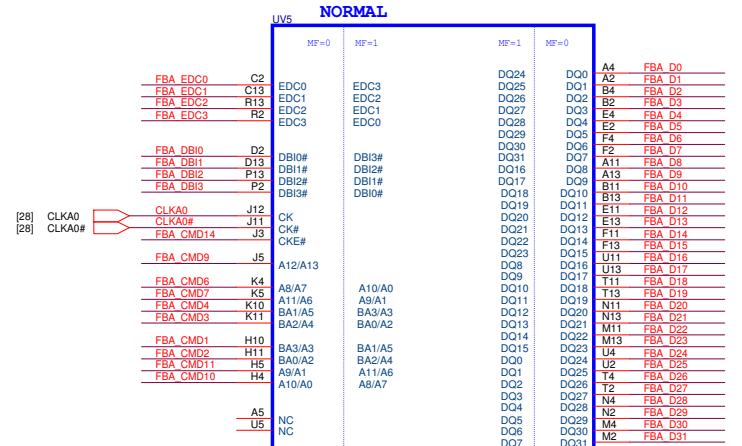
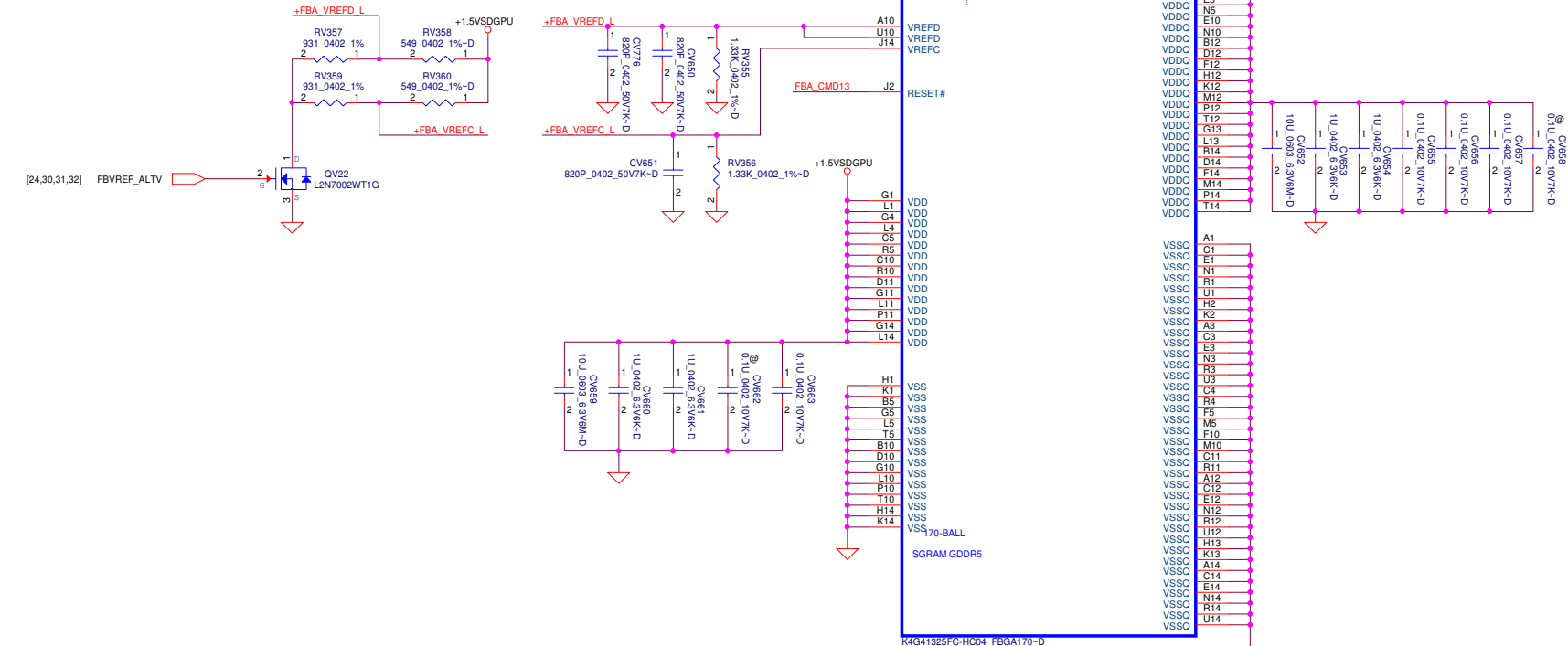


# Memory Partition A - Lower 32 bits

64X32 GDDR5

Table 46. GDDR5 Mode H Mapping

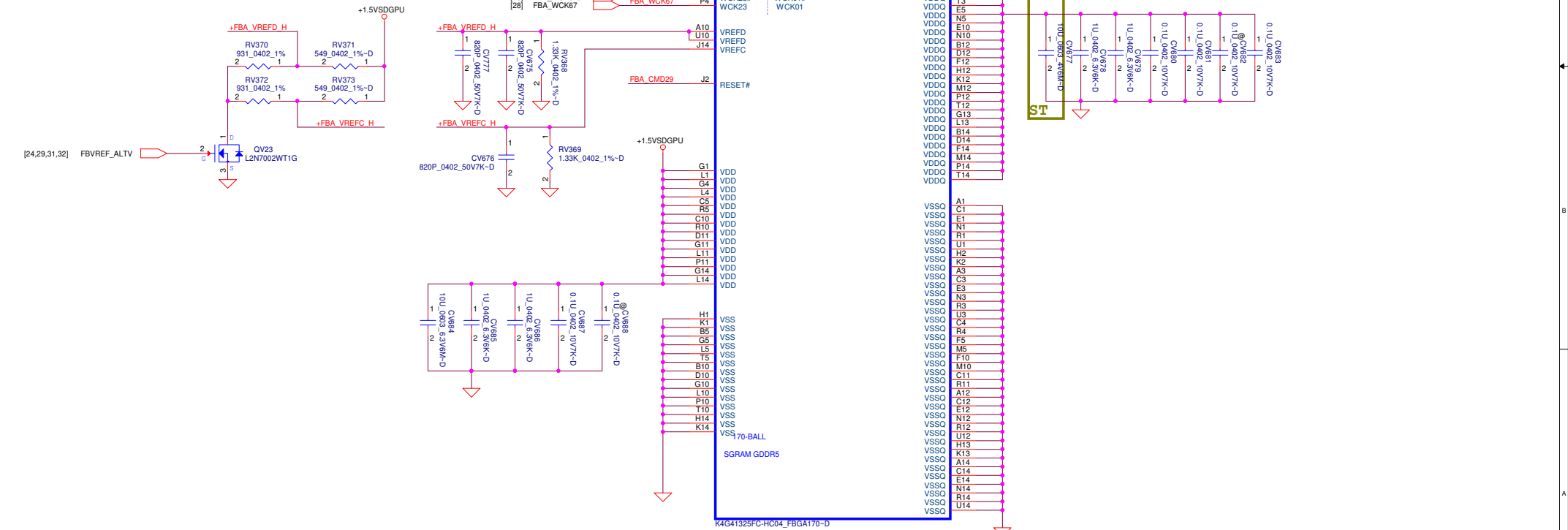
GB2-64, GB4-128	Channel 0 B, .31	GB2-64, GB4-128	Channel 1 32, .63
CM00	LS*	CM016	CS*
CM01	A2_BA3	CM017	A2_BA3
CM02	A3_BA0	CM018	A2_BA0
CM03	A4_BA2	CM019	A4_BA2
CM04	A8_BA1	CM020	A8_BA1
EM05	WE*	EM021	WE*
CM06	A7_A8	CM022	A7_A8
CM07	A8_A11	CM023	A8_A11
CM08	AB*	CM024	AB*
CM09	A12_PP0	CM025	A12_PP0
CM010	A6_A10	CM026	A6_A10
CM011	A1_A8	CM027	A1_A8
CM012	RA*	CM028	RA*
CM013	RS*	CM029	RS*
CM014	CK*	CM030	CK*
CM015	CA*	CM031	CA*



# Memory Partition A - Upper 32 bits

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 D..31	GB2-64, GB4-128	Channel 1 32..63
CM00	CS1	CM016	CS1
CM01	A3_BA3	CM017	A3_BA3
CM02	A1_BA0	CM018	A1_BA0
CM03	A4_BA2	CM019	A4_BA2
CM04	A8_BA1	CM020	A8_BA1
CM05	WE*	CM021	WE*
CM06	A7_A8	CM022	A7_A8
CM07	A8_A11	CM023	A8_A11
CM08	AB*	CM024	AB*
CM09	A12_PP0	CM025	A12_PP0
CM010	A0_A10	CM026	A0_A10
CM011	A1_A9	CM027	A1_A9
CM012	RAA*	CM028	RAA*
CM013	RS*	CM029	RS*
CM014	CKE*	CM030	CKE*
CM015	CA*	CM031	CA*

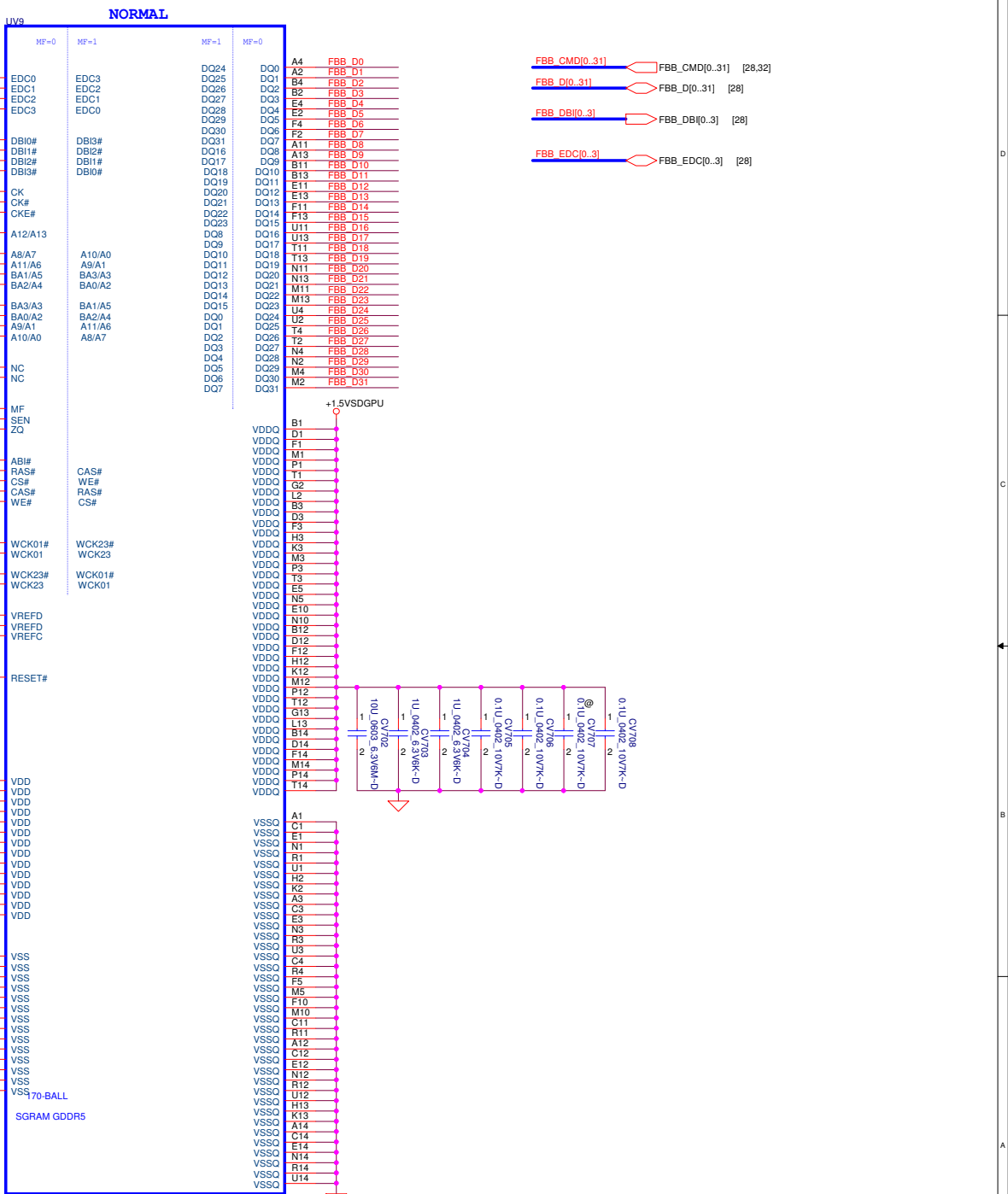
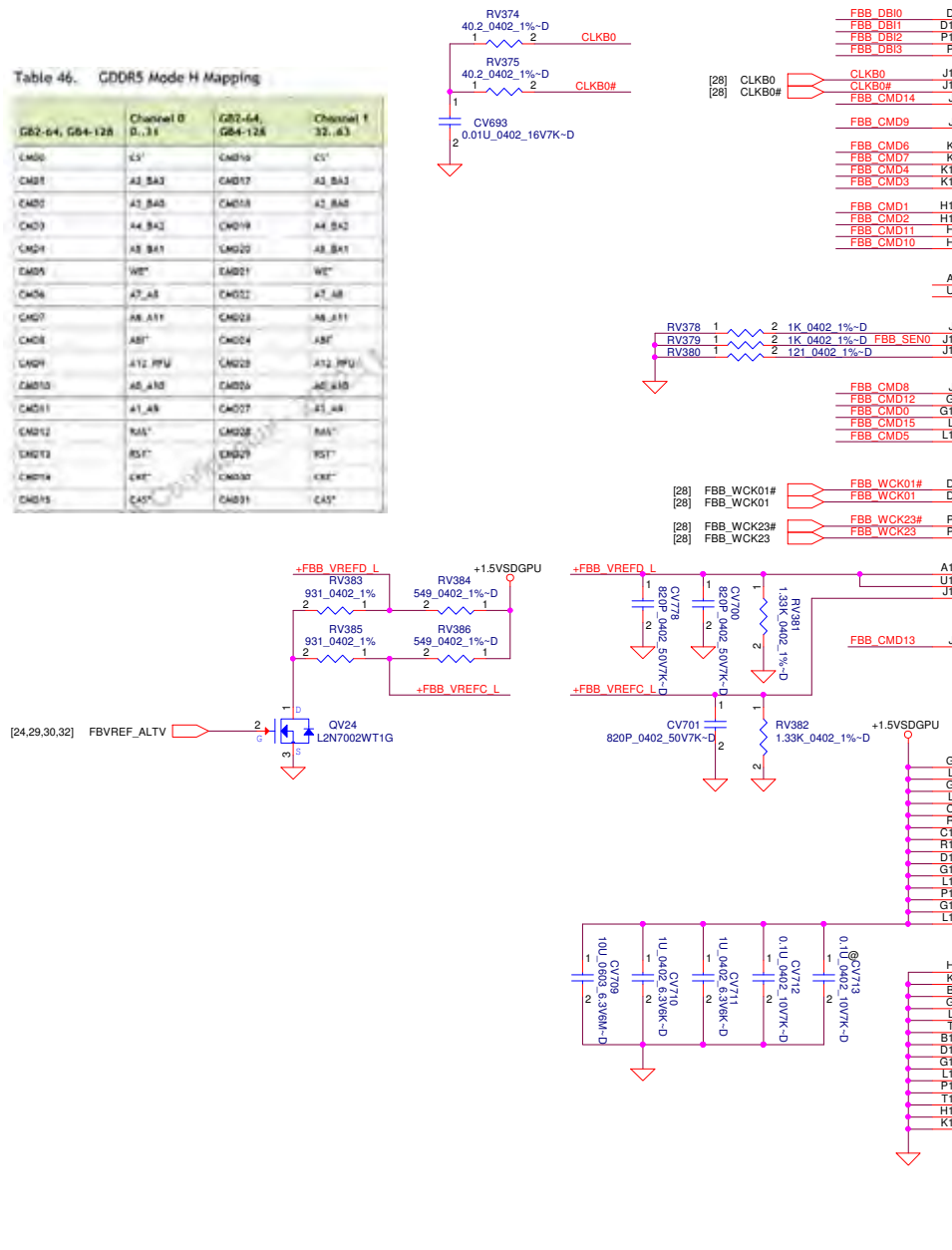


# Memory Partition B - Lower 32 bits

64X32 GDDR5

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 D <sub>0..31</sub>	GB2-64, GB4-128	Channel 1 D <sub>32..63</sub>
CM00	C5*	CM010	C5*
CM01	A3_BA3	CM017	A3_BA3
CM02	A3_BA3	CM018	A3_BA3
CM03	A4_BA2	CM019	A4_BA2
CM04	A5_BA1	CM020	A5_BA1
CM05	WE*	CM021	WE*
CM06	A7_A8	CM022	A7_A8
CM07	A8_A11	CM023	A8_A11
CM08	AB*	CM024	AB*
CM09	A12_BF0	CM025	A12_BF0
CM10	A5_A10	CM026	A5_A10
CM11	A1_A8	CM027	A1_A8
CM12	RAA*	CM028	RAA*
CM13	RS1*	CM029	RS1*
CM14	KKE*	CM030	KKE*
CM15	CA5*	CM031	CA5*

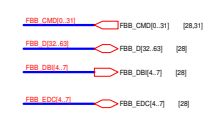
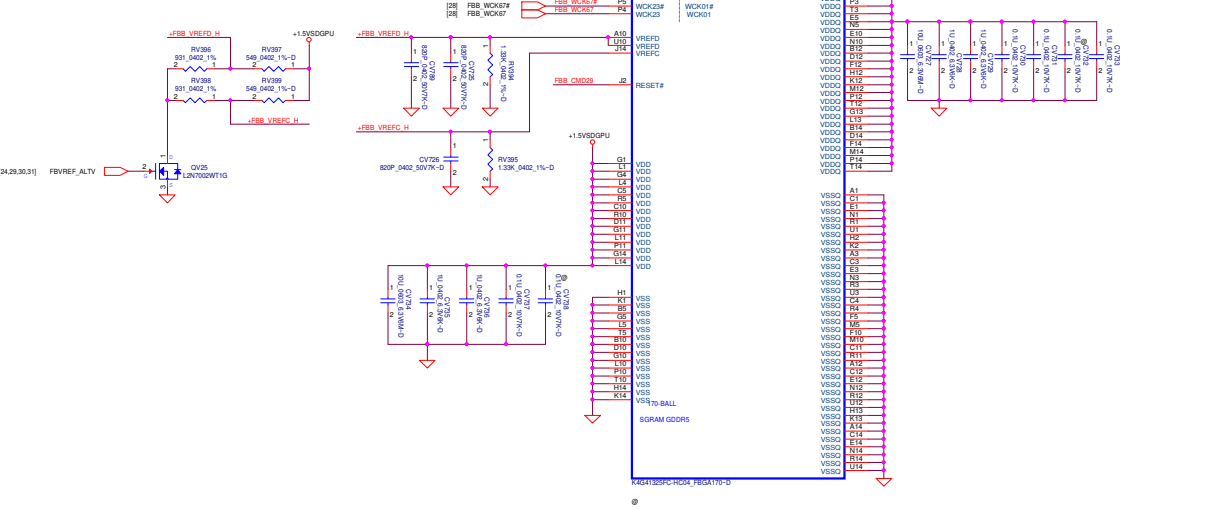


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# Memory Partition B - Upper 32 bits

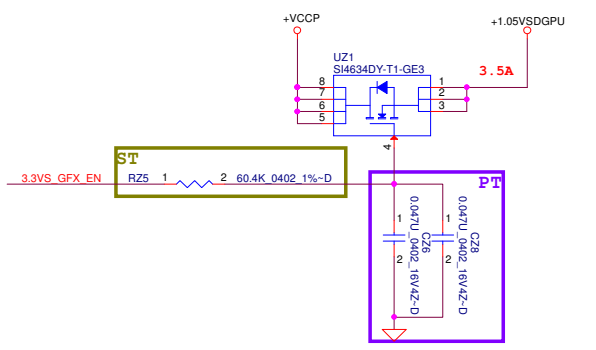
Table 46. CDRS Mode H Mapping

GR2-64, GR4-128	Channel B D, J1	GR2-64, GR4-128	Channel F 32, A3
CM00	A1	CM00	A1
CM01	A2, B43	CM01	A2, B43
CM02	A3, B48	CM03	A2, B48
CM03	A4, B42	CM04	A4, B42
CM04	A8, B41	CM05	A8, B41
CM05	W6*	CM06	W6*
CM06	A7, A8	CM07	A7, A8
CM07	A8, A11	CM08	A8, A11
CM08	A8*	CM09	A8*
CM09	A12, P10	CM10	A12, P10
CM10	A8, A18	CM11	A8, A18
CM11	A1, A8	CM12	A3, A8
CM12	N4*	CM13	N4*
CM13	B3*	CM14	B3*
CM14	K4*	CM15	K4*
CM15	C4*	CM16	C4*

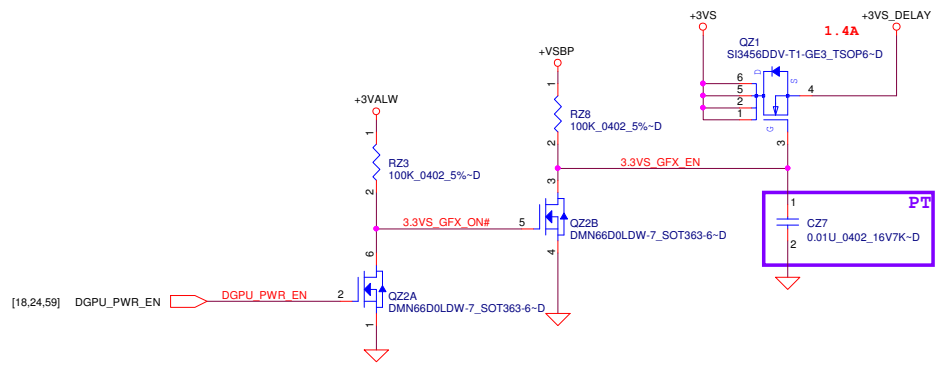


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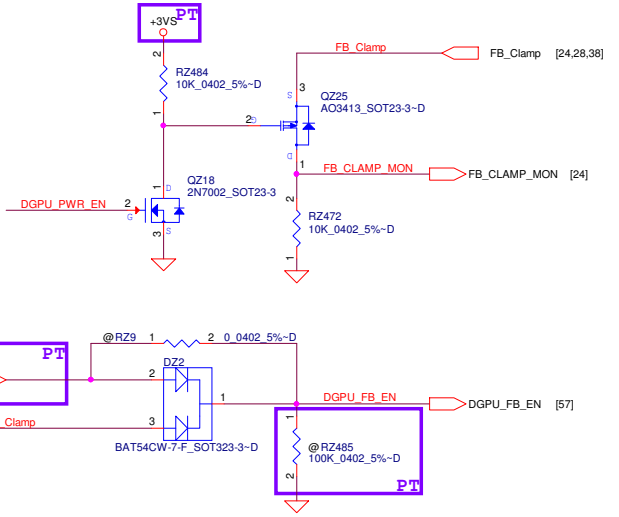
**+1.05VS to +1.05VSDGPU**



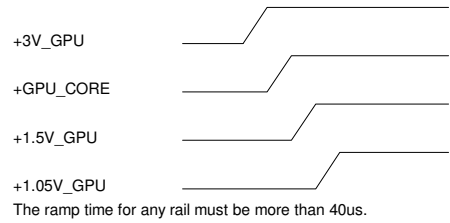
**+3VS to +3VS\_DELAY**



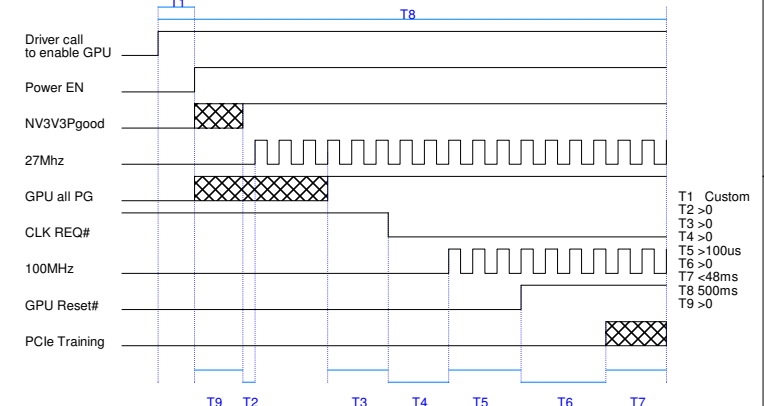
**GC6**



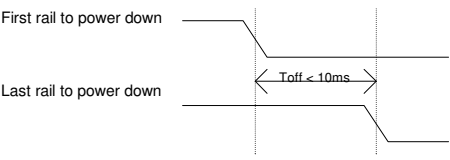
**GPU Power Up Power Rail Sequence**



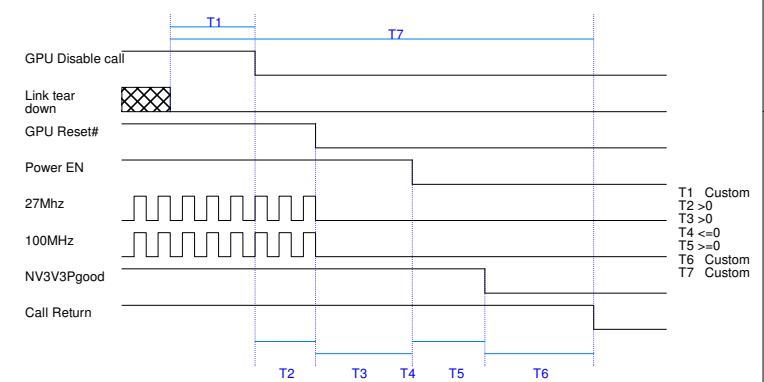
**GPU Power Up Sub-system Sequence**



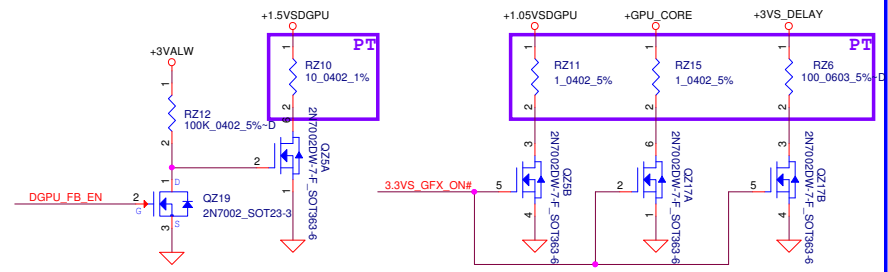
**GPU Power Down Sequence**



**GPU Power Down Sub-system Sequence**

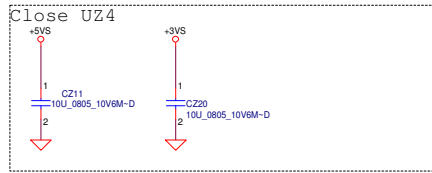
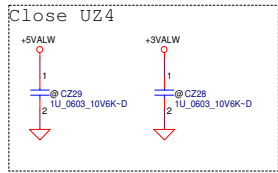
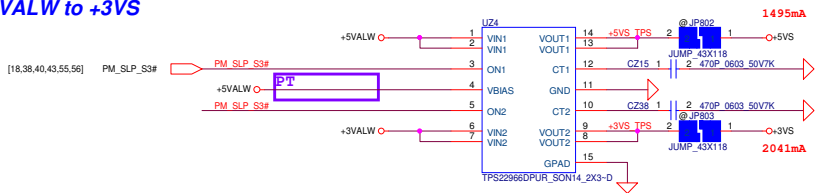


**Discharge**

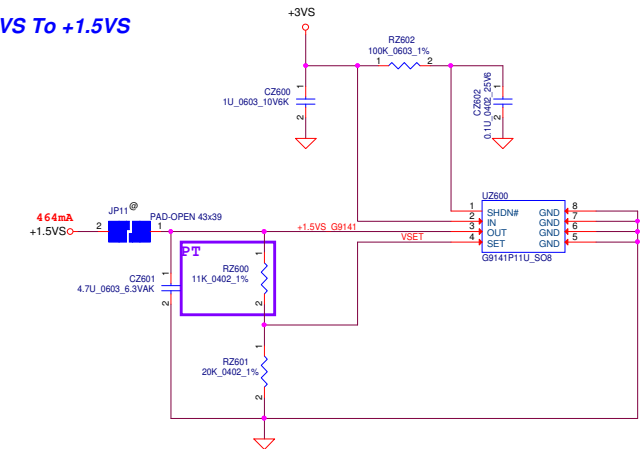


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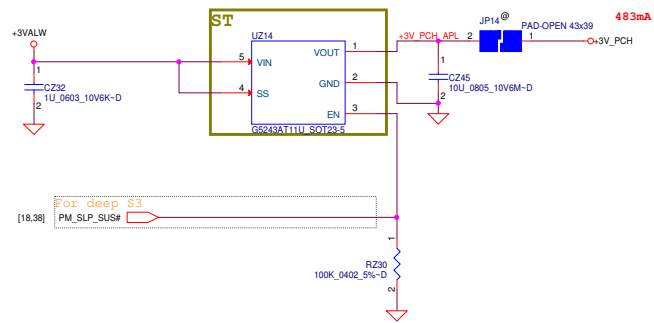
**+5VALW to +5VS**  
**+3VALW to +3VS**



**+3VS To +1.5VS**



**+3VALW to +3V\_PCH**

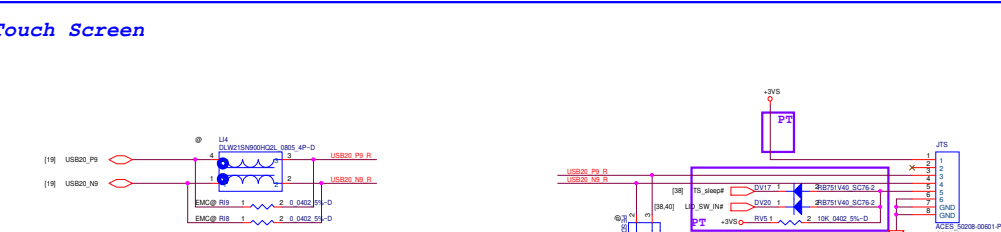
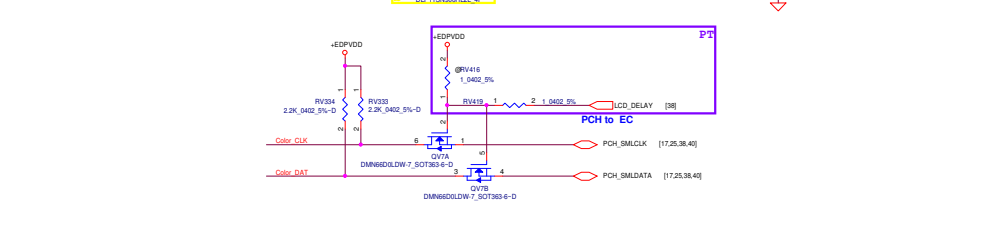
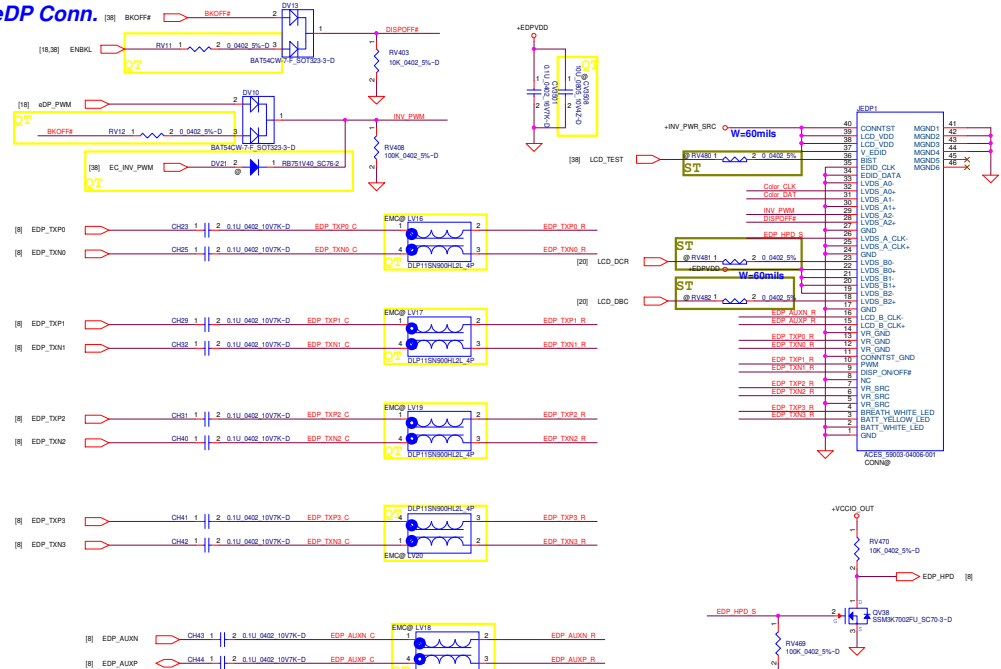


**Discharge**

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# eDP Redriver

# eDP Conn.



# LCD PWR CTRL

# LCD backlight PWR CTRL

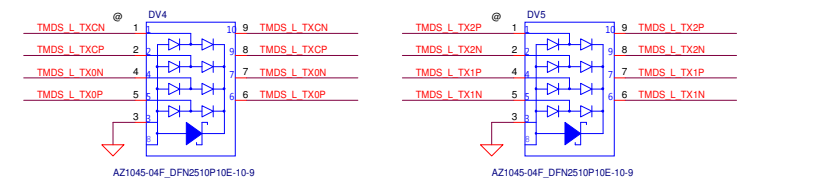
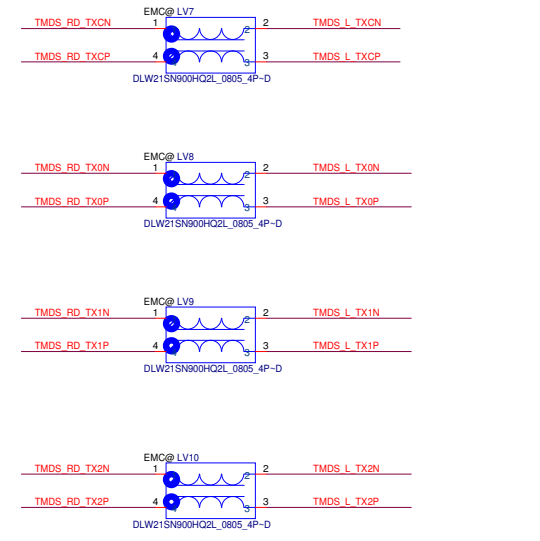
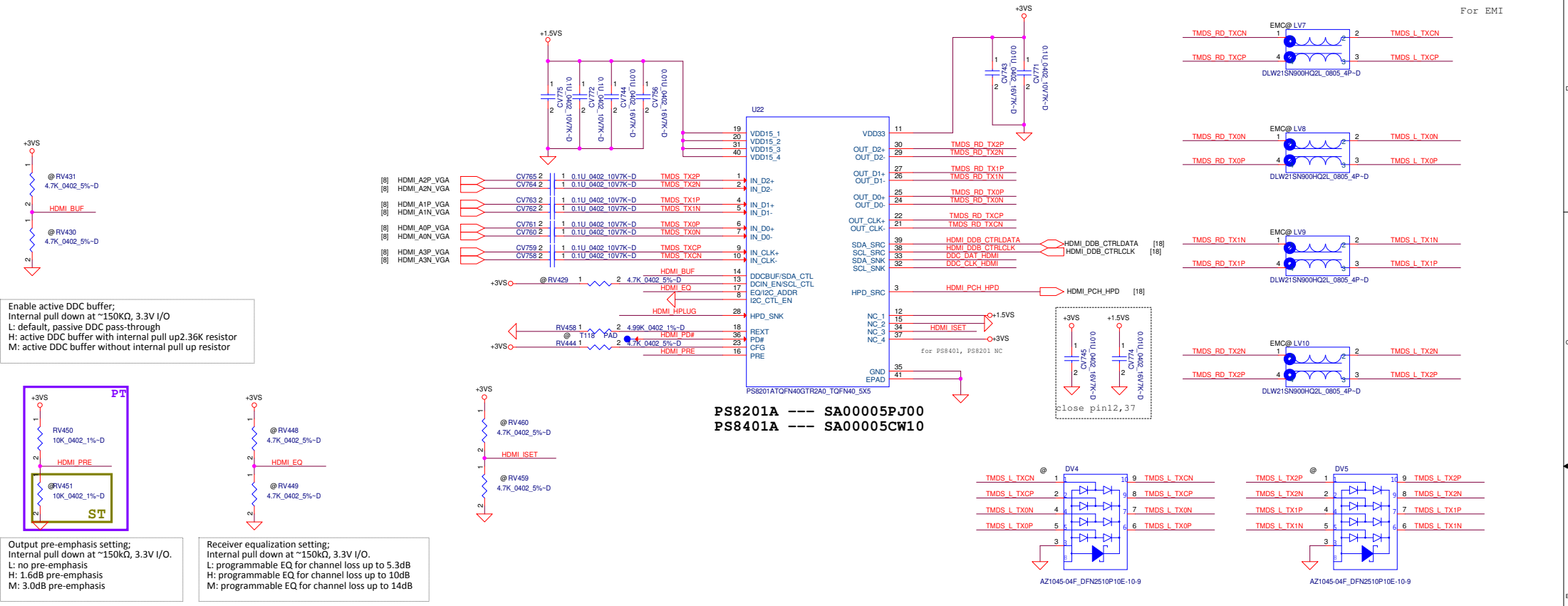
# Touch Screen

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Doc No.	LA-9941P		Rev	01	
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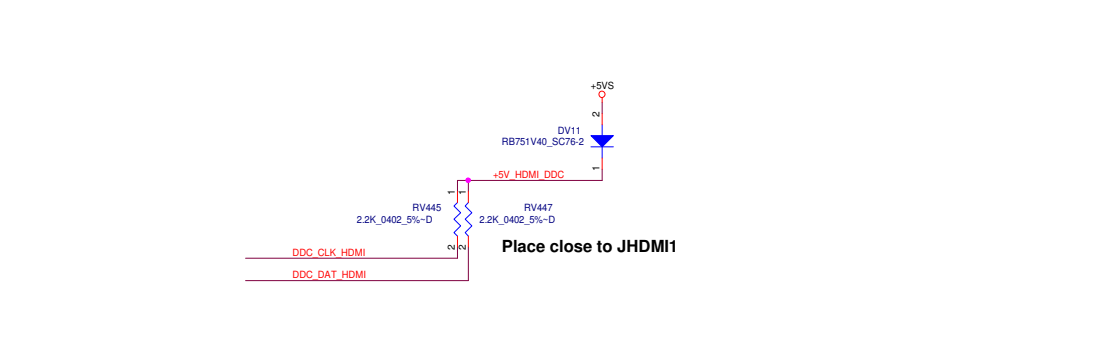
# HDMI Active Level Shift (ALS type)

Place close to JHDMI1

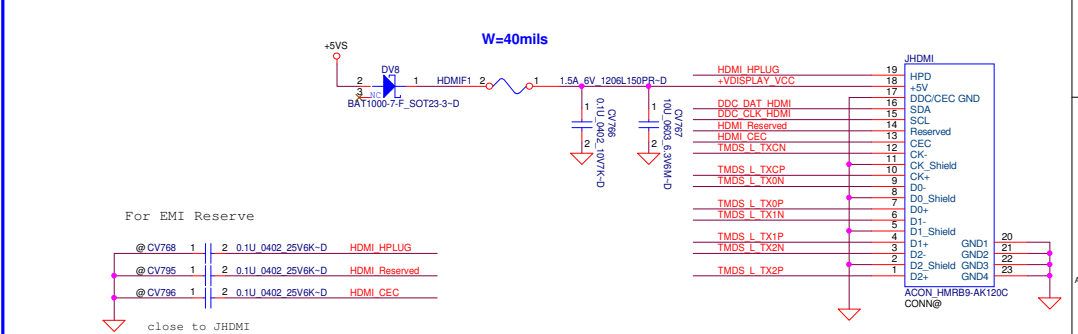
For EMI



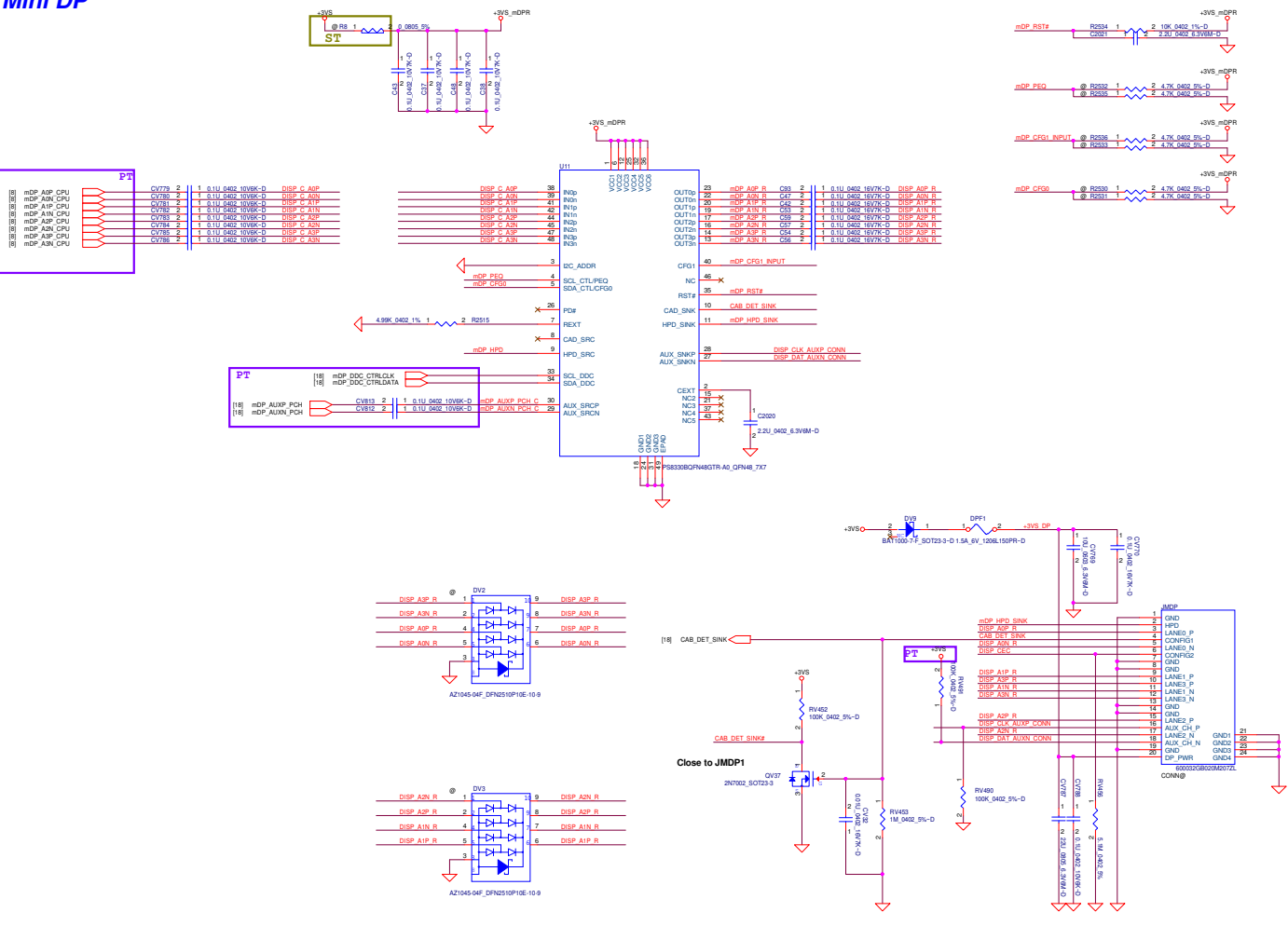
## HDMI DDC



## HDMI conn



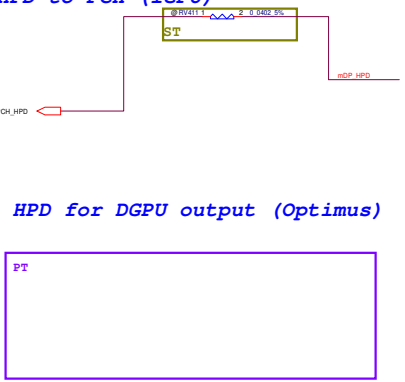
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			Date:	Tuesday, September 03, 2013	Sheet 36 of 62

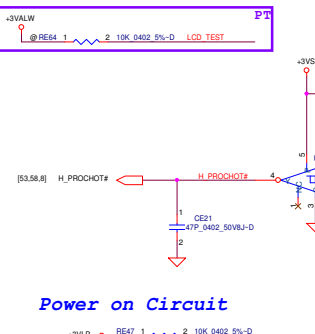
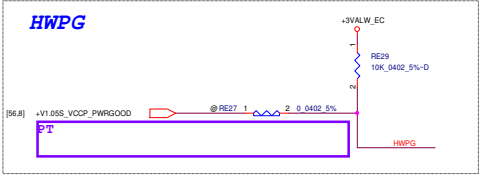
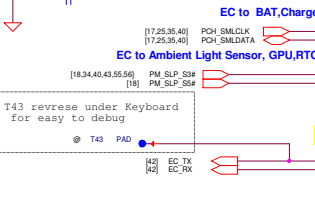
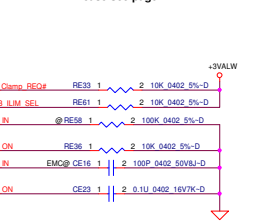
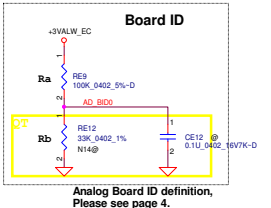
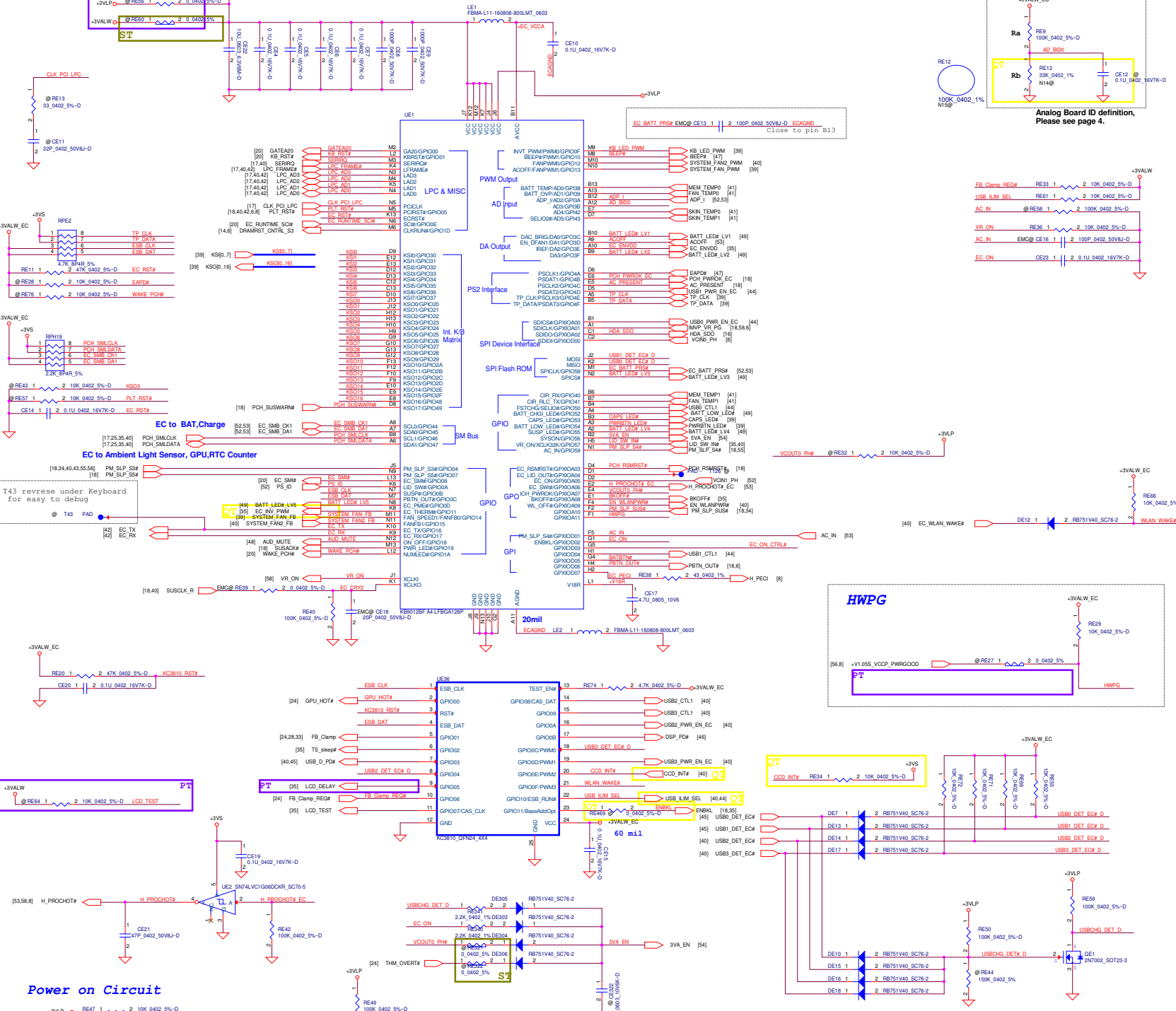


DDC Dongle SW for DP

DP HPD to PCH (iGPU)

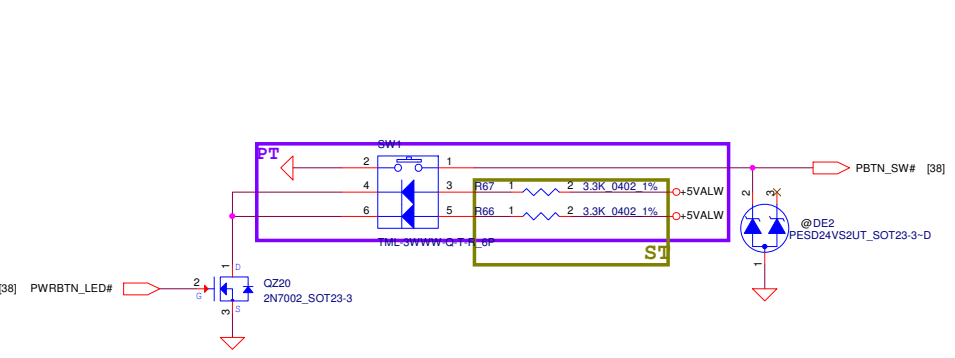
DP HPD for DGPU output (Optimus)



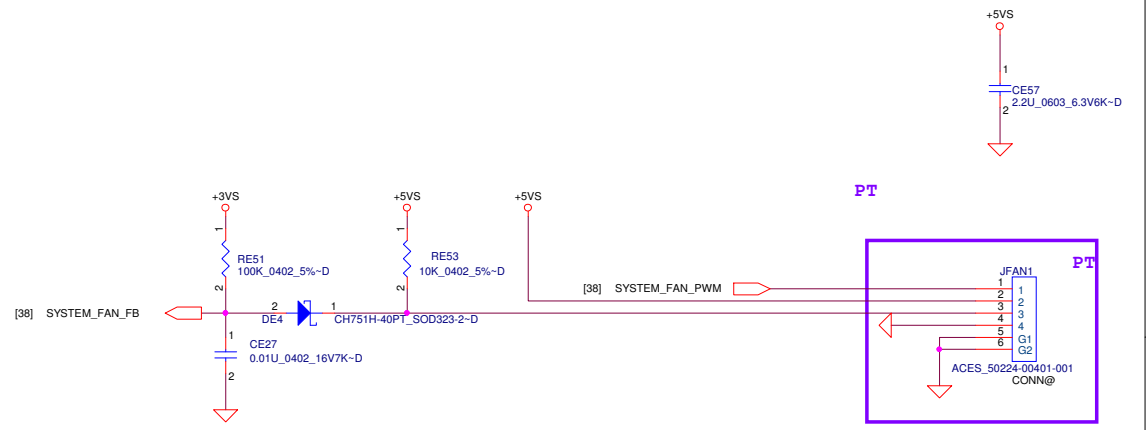


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<p>Compal Electronics, Inc.</p> <p>EC ENE-KB930/ ENE3810</p>		<p>LA-99A1P</p>	
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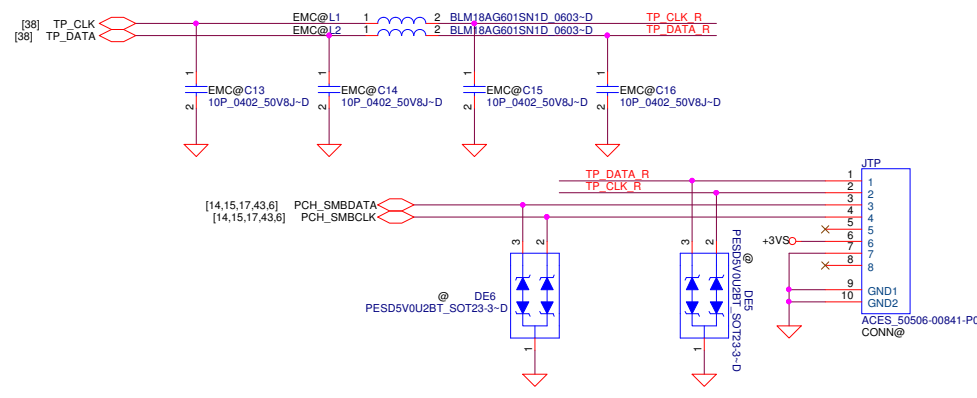
# Power on Button



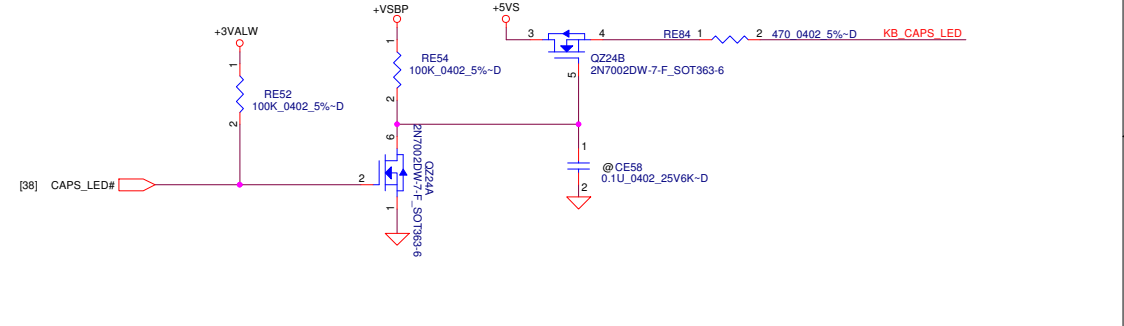
# PWM FAN



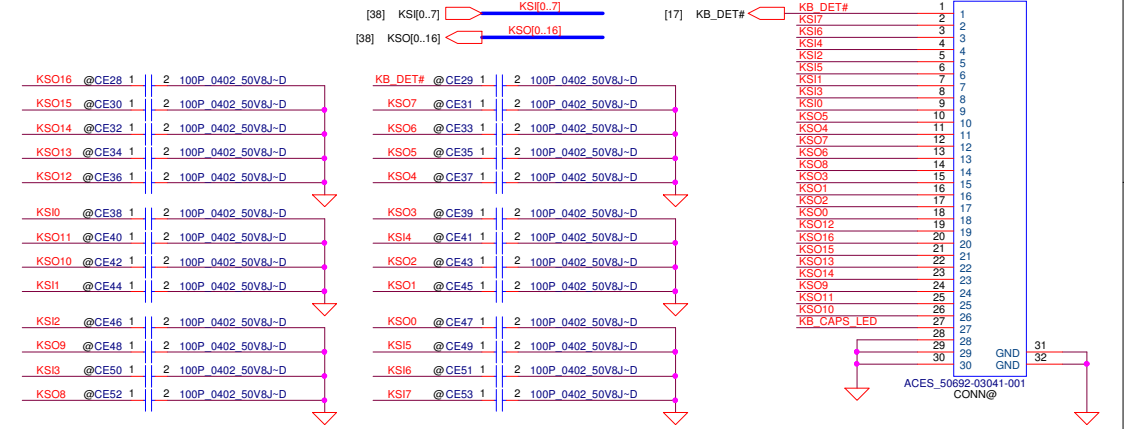
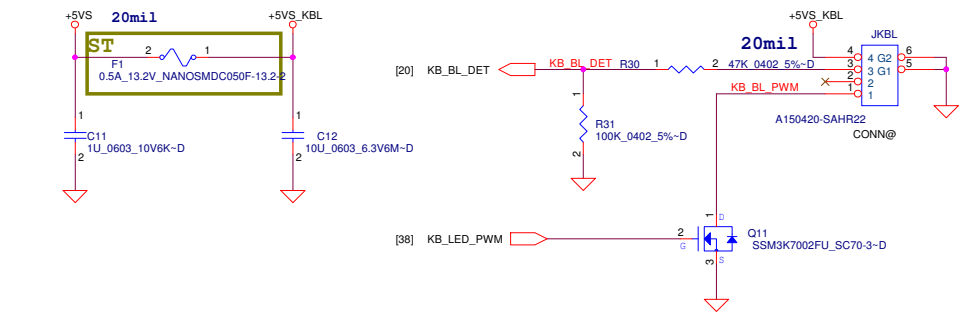
# Touch pad



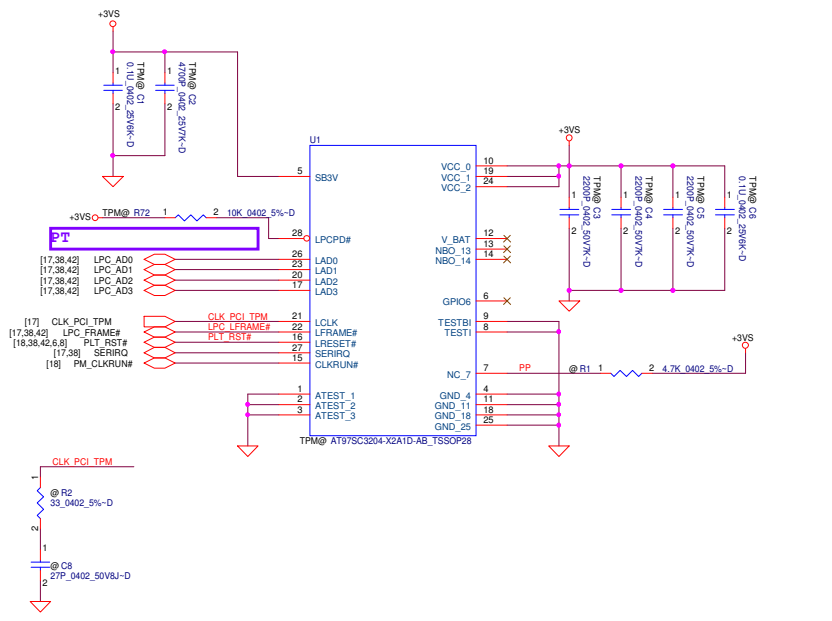
# INT\_KBD CONN



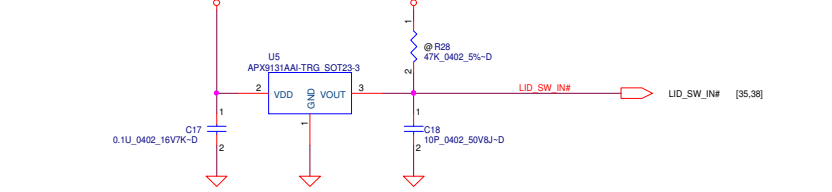
# Keyboard back light



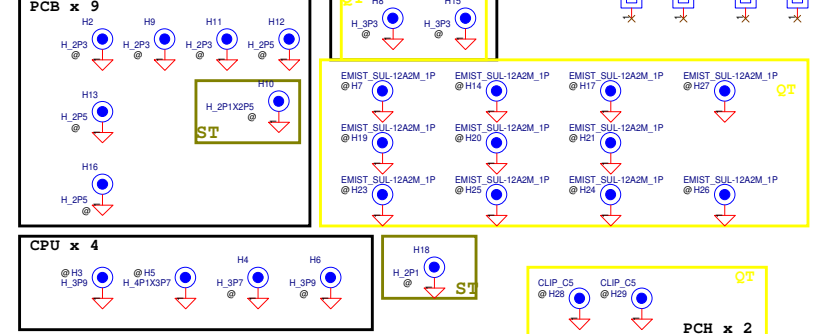
# ATMEL TPM



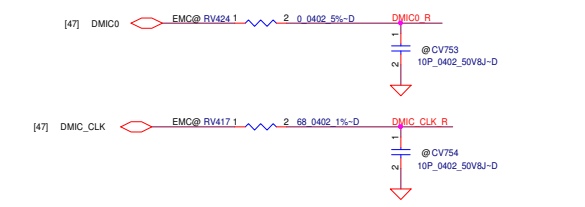
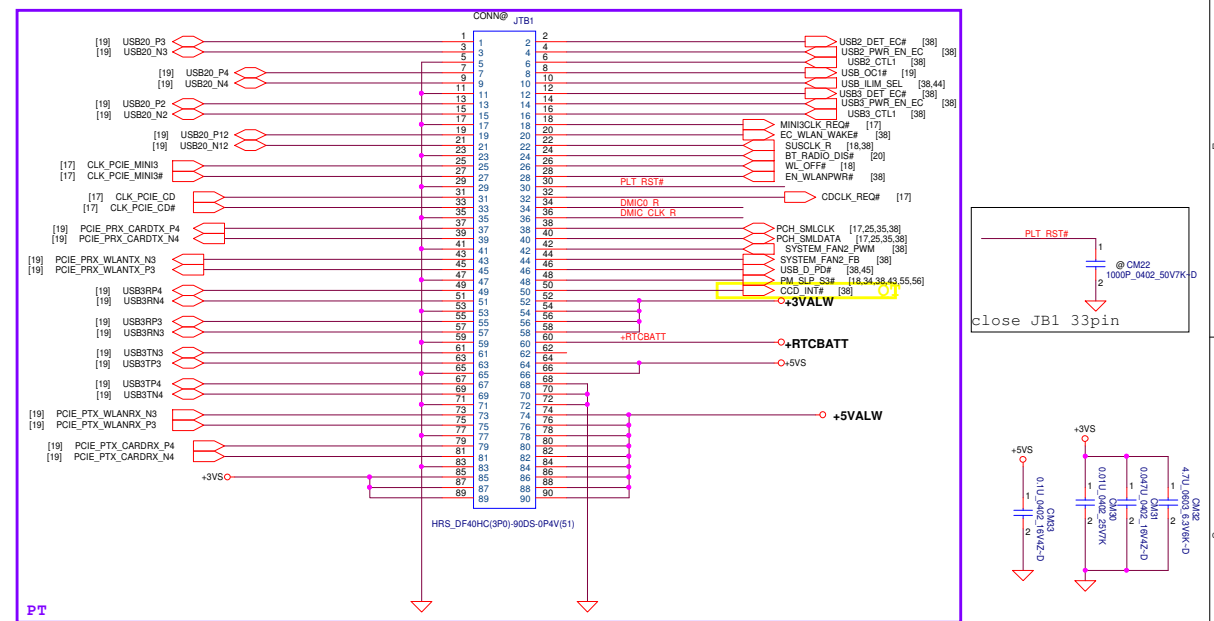
# Lid Switch



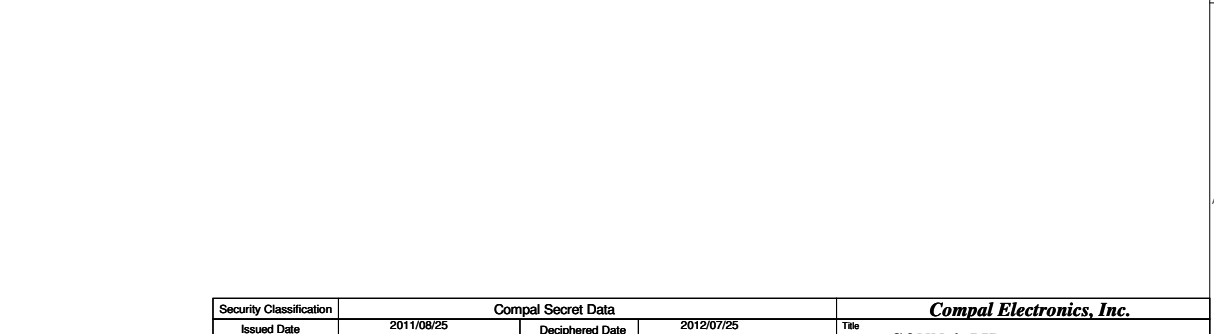
# Screw Hole



# M/B to D/B conn.

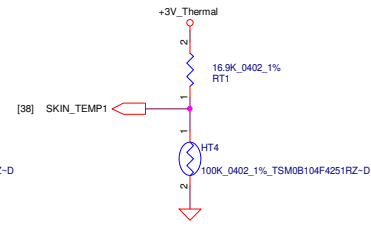
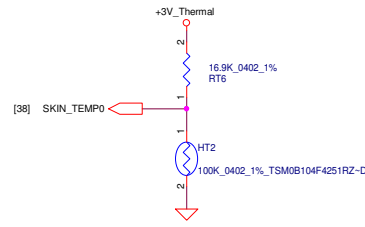
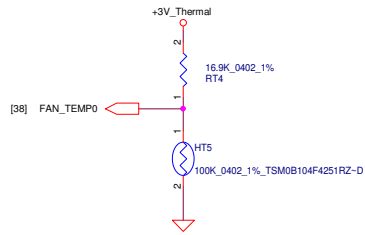
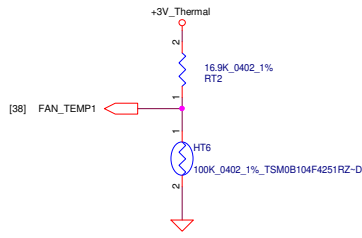
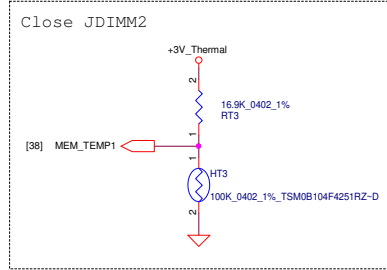
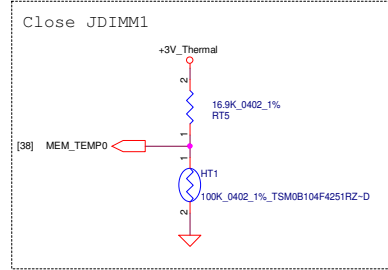
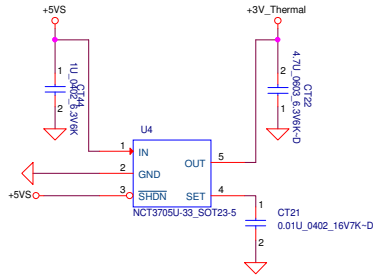


# Wedcam PWR CTRL



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# Thermal sensor

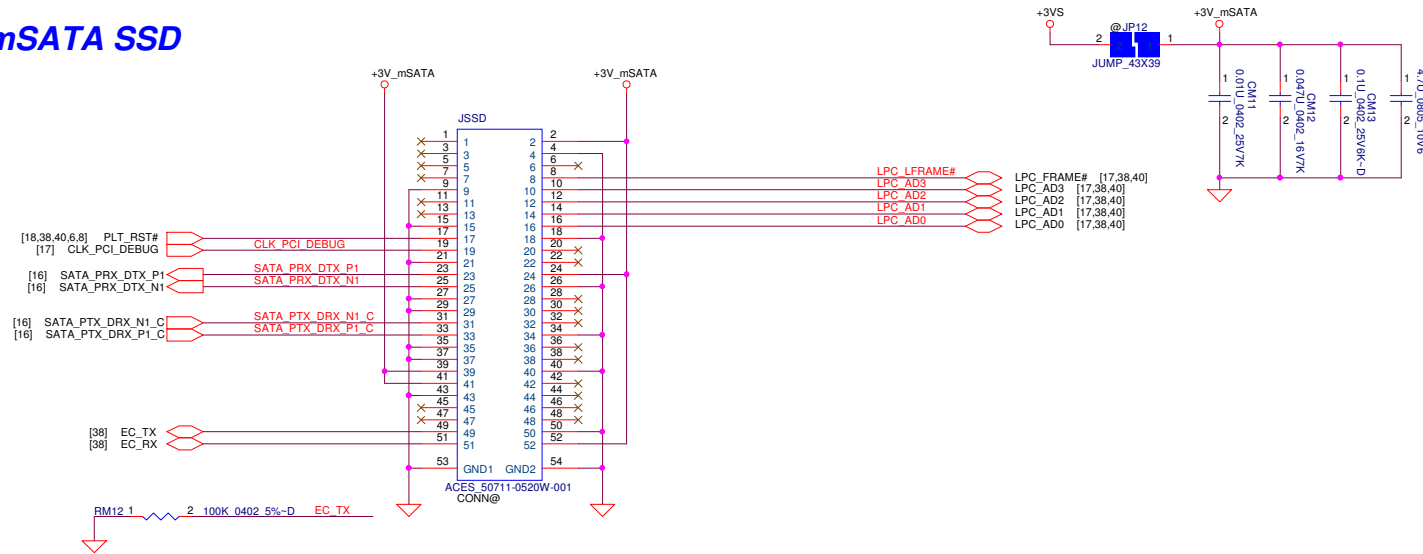


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Size	Document Number	Date	Sheet	Rev
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# WLAN / BT4.0 PCIE Mini Card

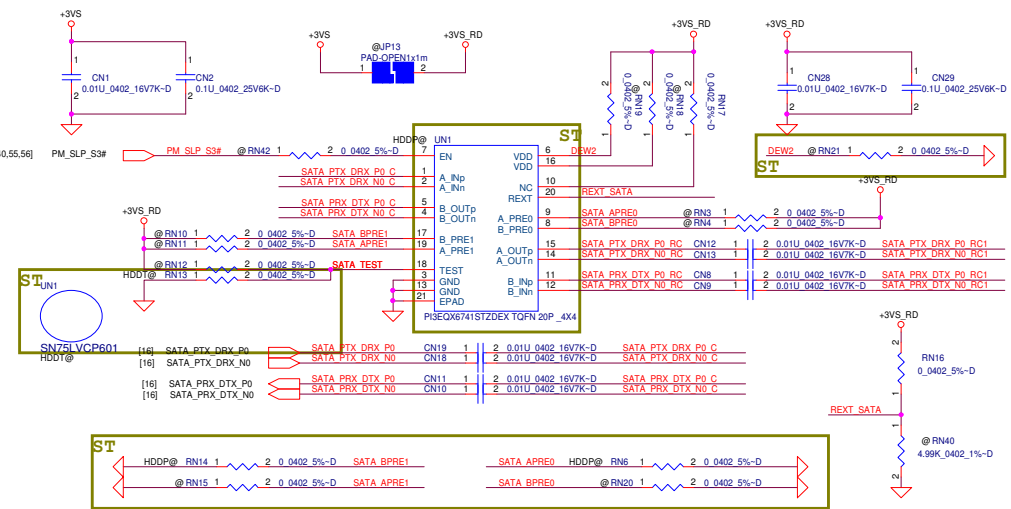
Pin#	Assignment	Description	Pin#	Assignment	Description
1	N/A	N/A	27	GND	Return Current Path
2	+3.3V	3.3V source	28	N/A	N/A
3	N/A	N/A	29	GND	Return Current Path
4	GND	Return Current Path	30	N/A	N/A
5	N/A	N/A	31	-A (port 1)	SATA Differential Rx- based on SSD
6	N/A	N/A	32	N/A	N/A
7	N/A	N/A	33	+A (port 1)	SATA Differential Rx+ based on SSD
8	N/A	N/A	34	GND	Return Current Path
9	GND	Return Current Path	35	GND	Return Current Path
10	N/A	N/A	36	Reserved	No Connect
11	N/A	N/A	37	GND	Return Current Path
12	N/A	N/A	38	Reserved	No Connect
13	N/A	N/A	39	+3.3V	3.3V Source
14	N/A	N/A	40	GND	Return Current Path
15	GND	Return Current Path	41	+3.3V	3.3V Source
16	N/A	N/A	42	N/A	N/A
17	N/A	N/A	43	N/A	N/A
18	GND	Return Current Path	44	N/A	N/A
19	N/A	N/A	45	Reserved	N/A
20	N/A	N/A	46	N/A	N/A
21	GND	Return Current Path	47	Reserved	N/A
22	N/A	N/A	48	N/A	N/A
23	+B(port 1)	SATA Differential	49	DAVSS0	Device Activity / Disable Staggered Spin-up
24	+3.3V	3.3V Source	50	GND	Return Current Path
25	-B(port 1)	SATA Differential	51	Presence Detection	shall be pulled to GND by device
26	GND	Return Current Path	52	+3.3V	3.3V Source

## mSATA SSD

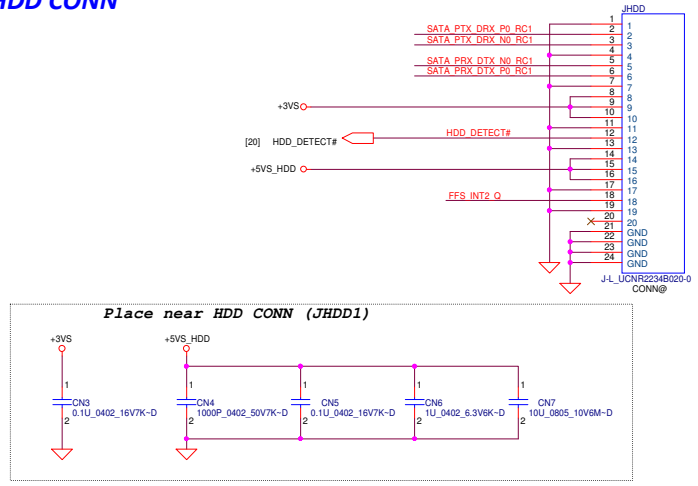


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<b>Issued Date</b>	2011/08/25	<b>Deciphered Date</b>	2012/07/25	<b>WLAN/WWAN/SIM/BT</b>	
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			L.A.9941P		0.1
			Date: Tuesday, September 03, 2013	Sheet	42 of 62

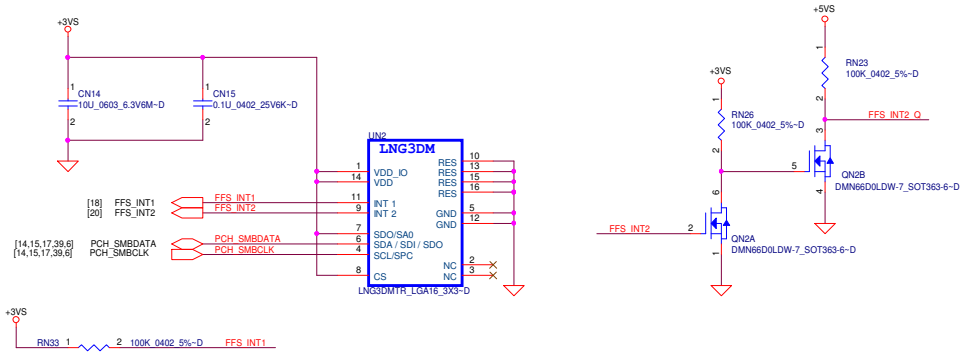
### SATA III Re-driver for HDD



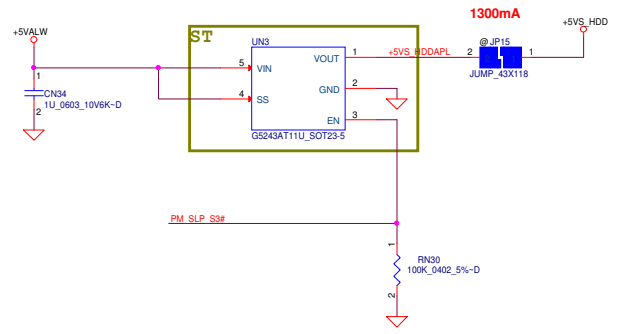
### HDD CONN



### Free Fall Sensor

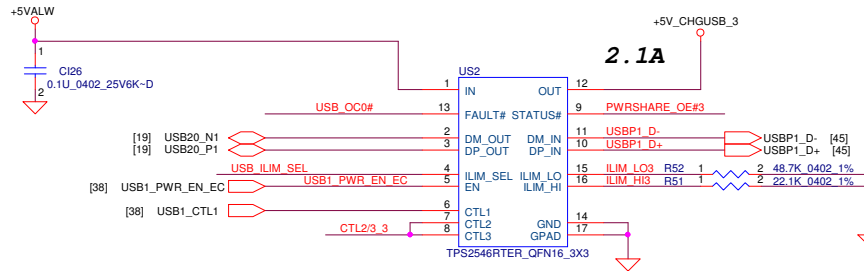
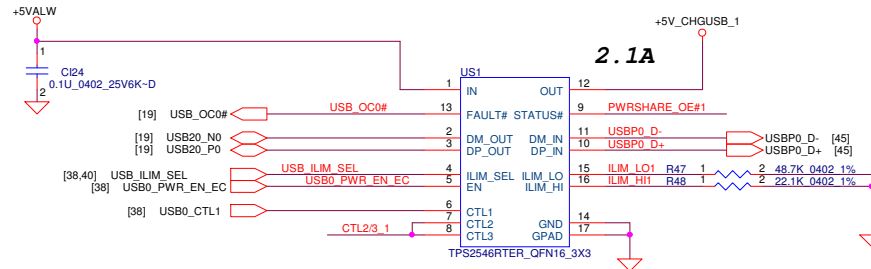
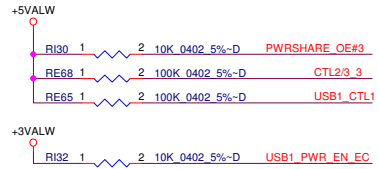
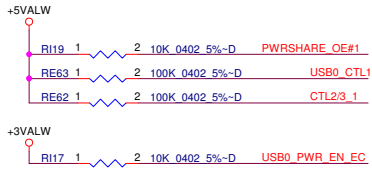


### HDD power control for AOAC



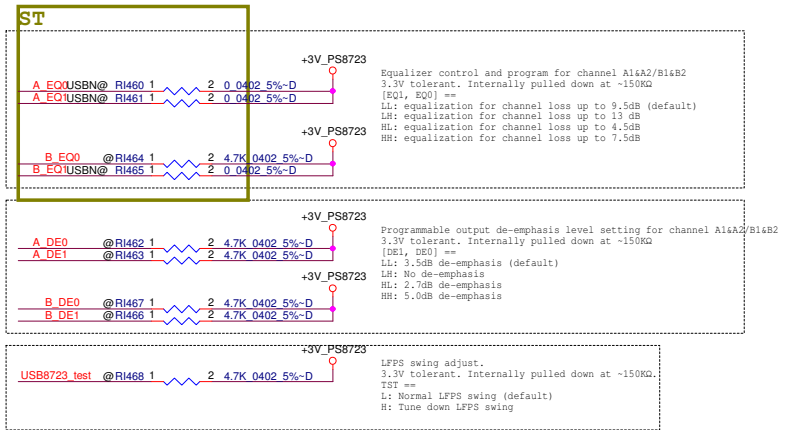
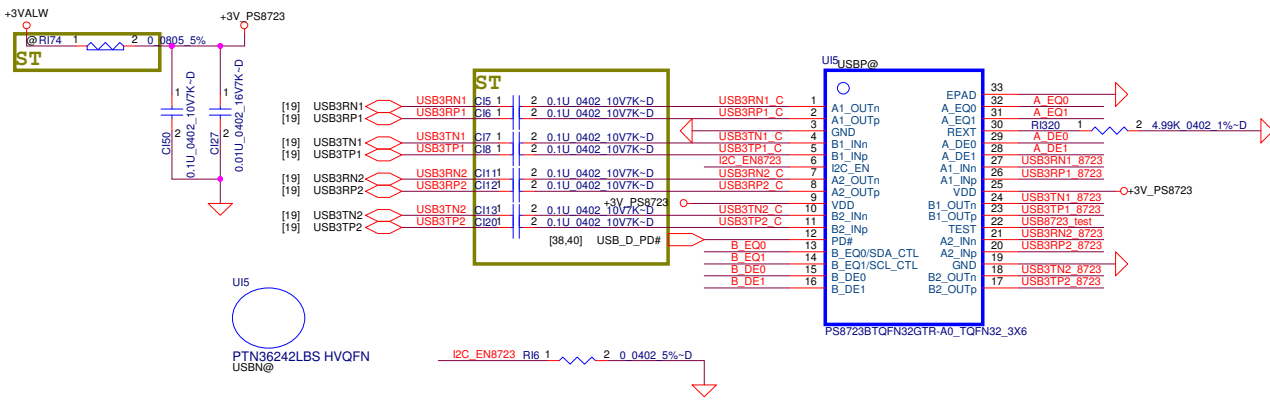
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title
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				LA-9941P
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				B.1
				Date: Tuesday, September 03, 2013
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# USB Powershare

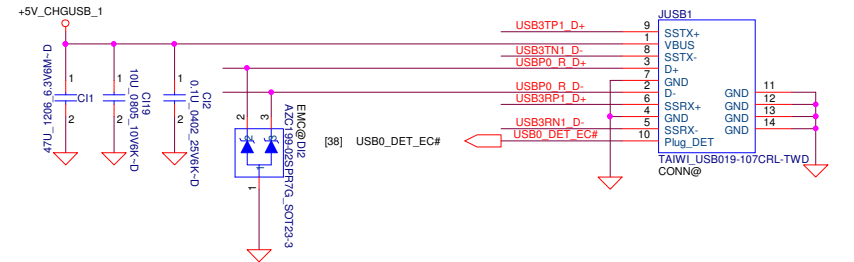
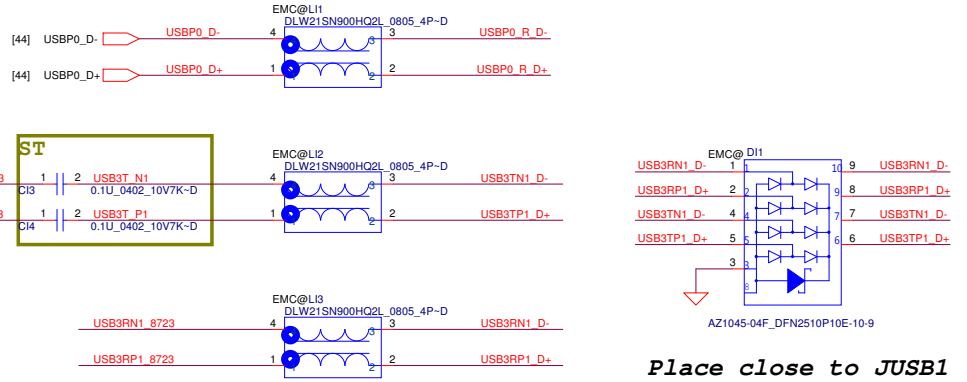


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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	USB Powershare
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				LA-9941P	0.1
				Date: Tuesday, September 03, 2013	Sheet 44 of 62

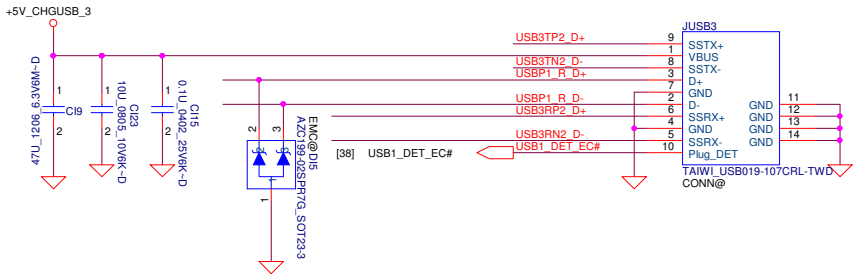
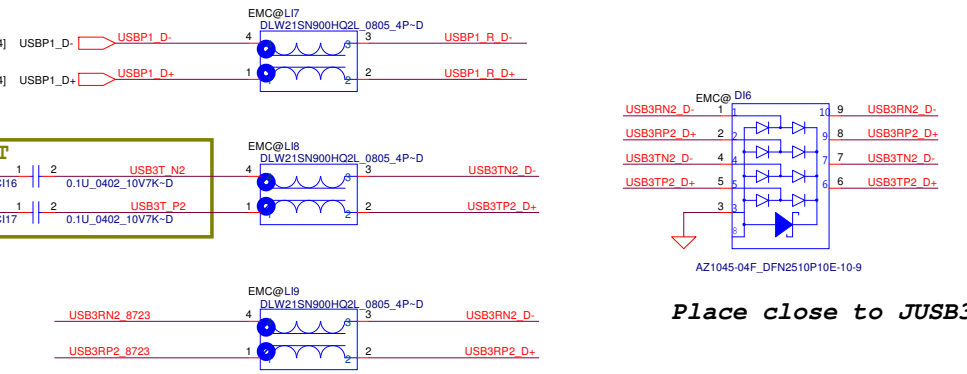
# USB3.0 Re-driver



## USB3.0 / USB2.0 Port1

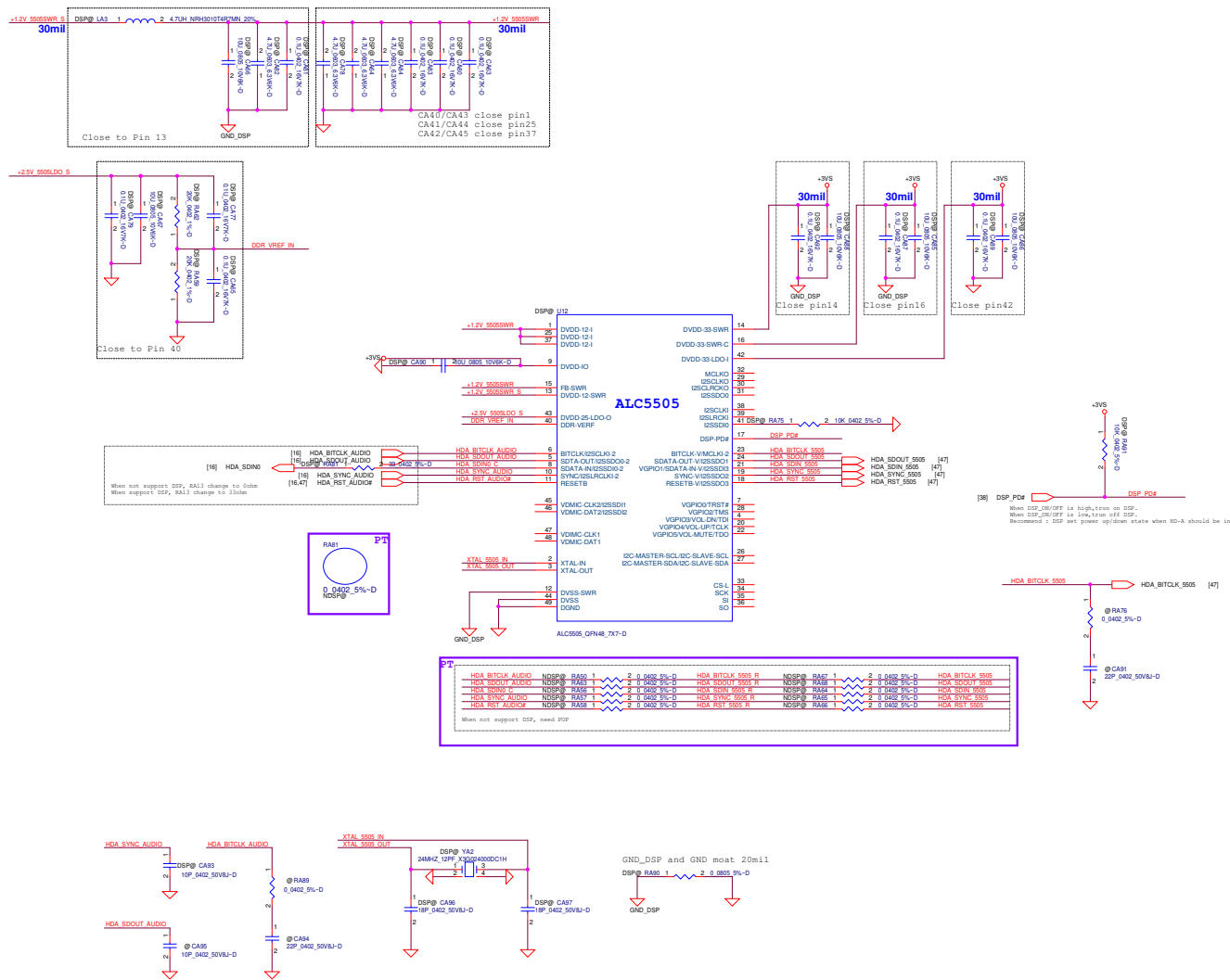


## USB3.0 / USB2.0 Port3



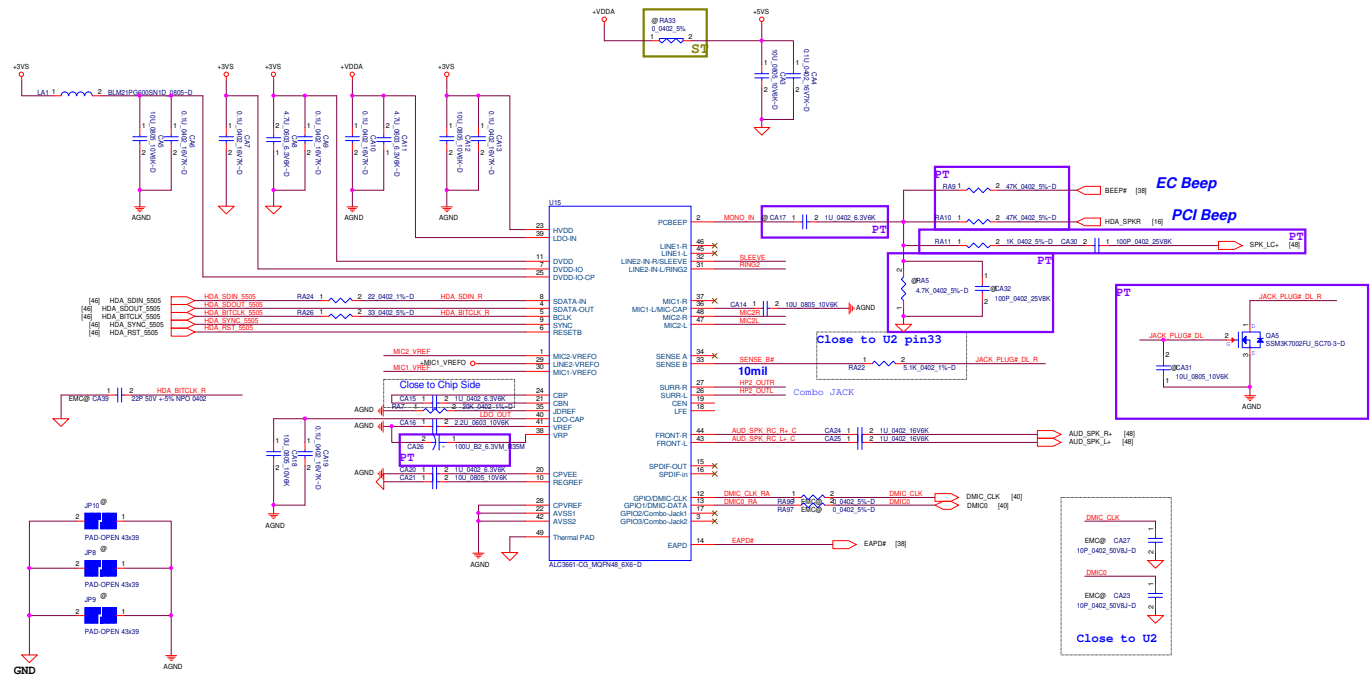
Security Classification	Compal Secret Data			Title <b>USB conn.</b>
Issued Date	2011/08/25	Deciphered Date	2012/07/25	
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# HD Audio DSP

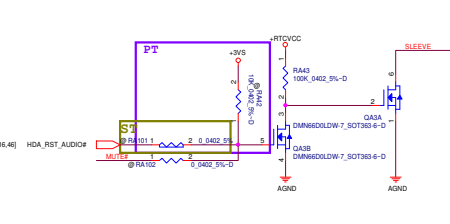


# Green Clock

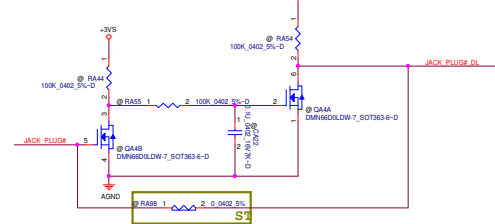
Security Classification	Compal Secret Data		Title	<b>Compal Electronics, Inc.</b>
Issued Date	2011/08/25	Deciphered Date	2012/07/25	<b>RTC Counter/Green Clock</b>
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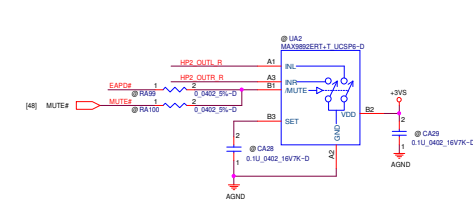
Prevent S3/S4/S5 Noise



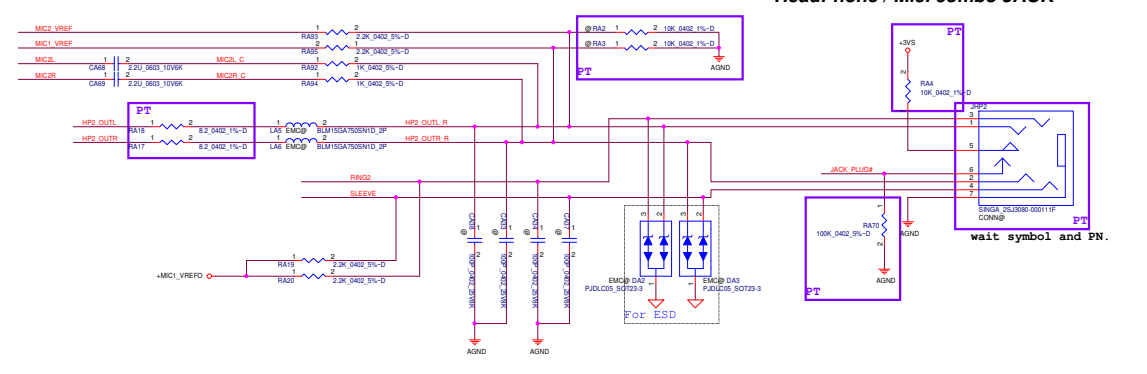
Reserved Delay Circuit



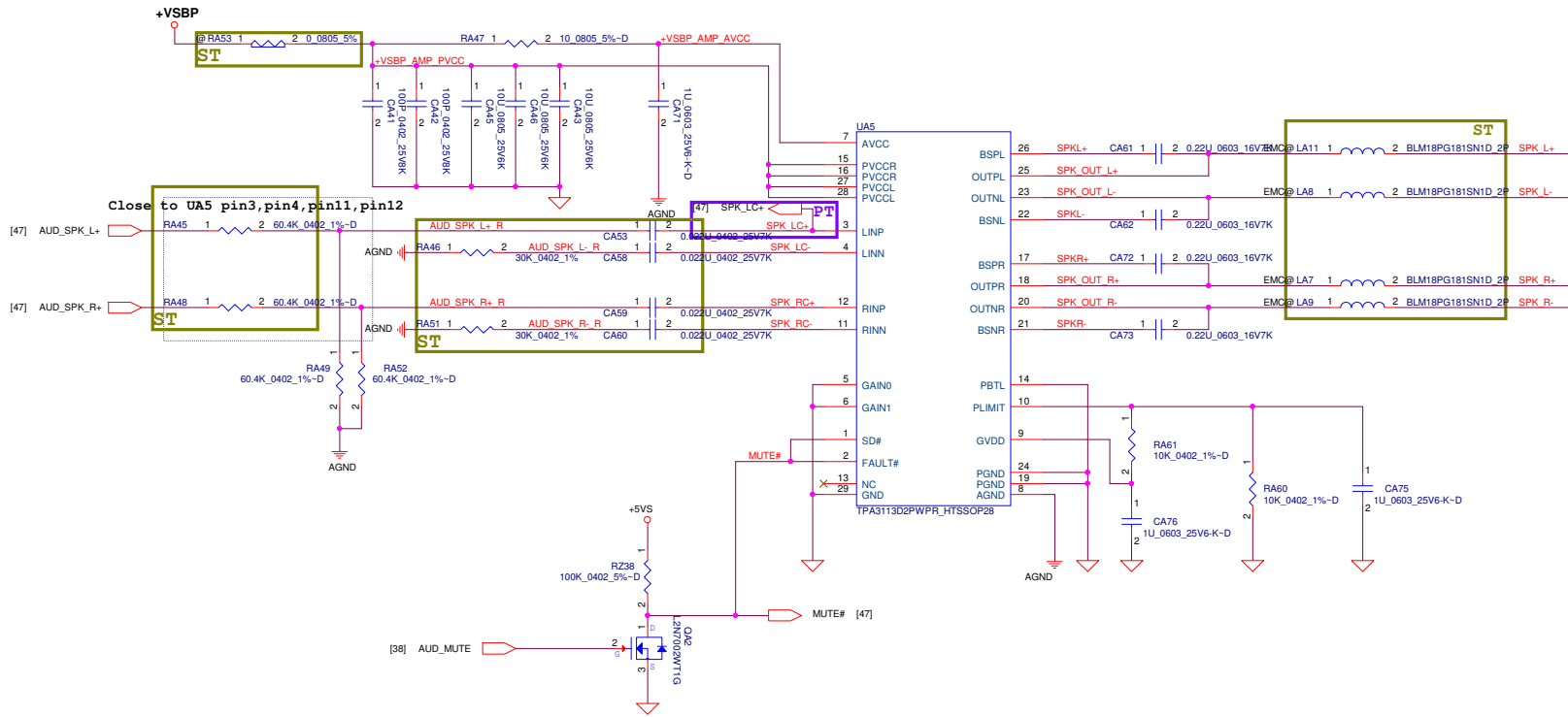
For De-pop noise



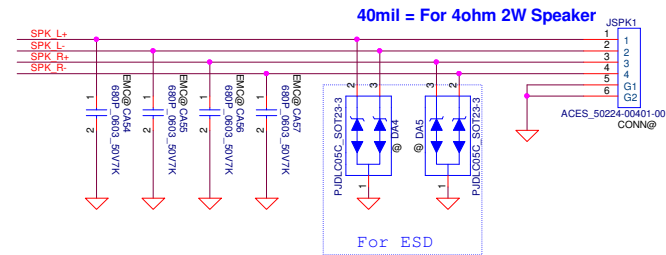
HeadPhone / Mic. combo JACK



# Audio AMP

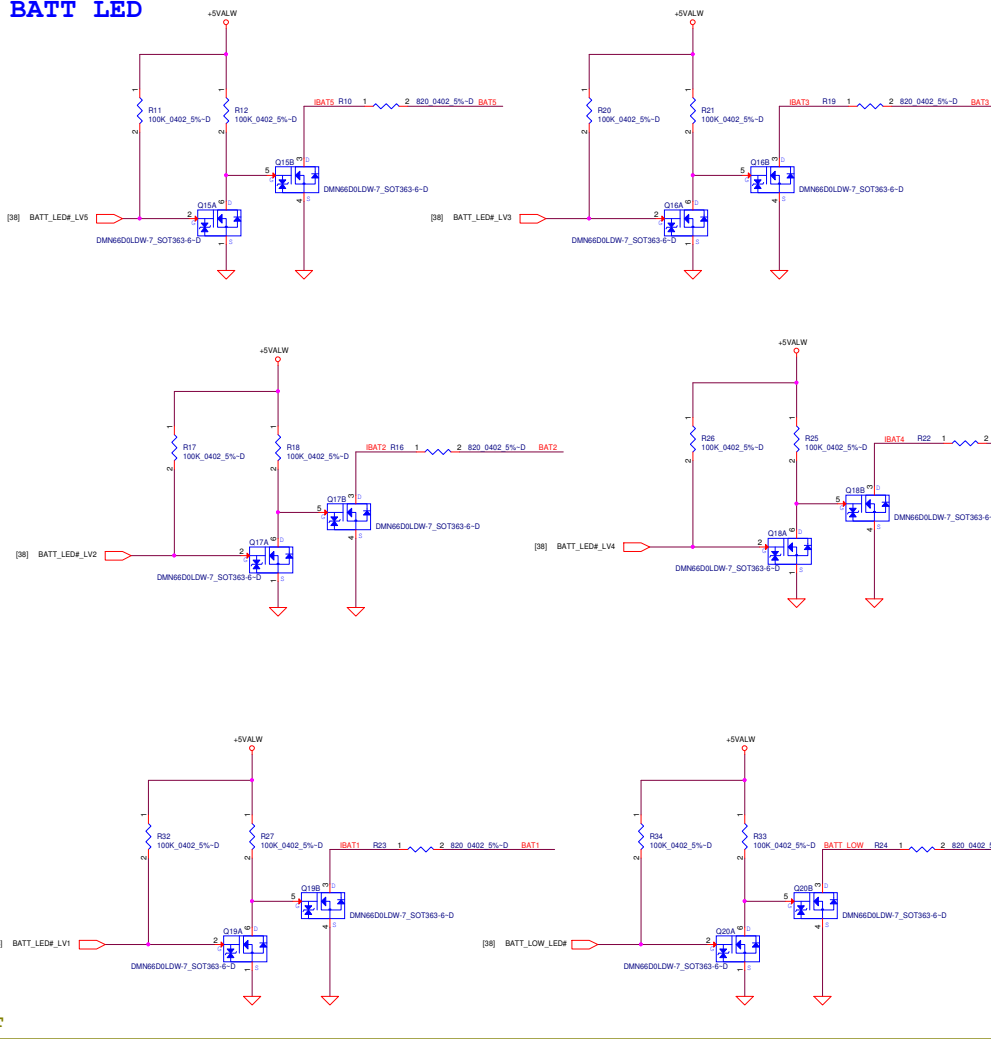


## Int. Speaker Conn.

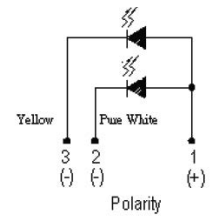
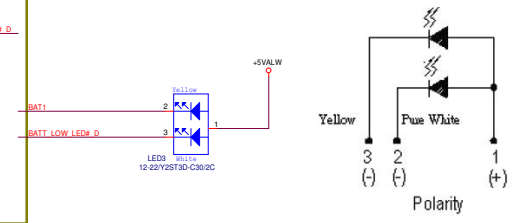
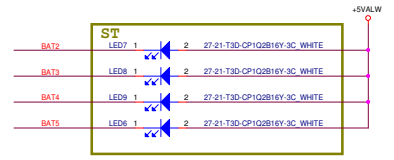
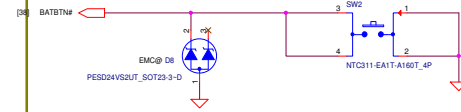


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			Speaker/Audio Jack	
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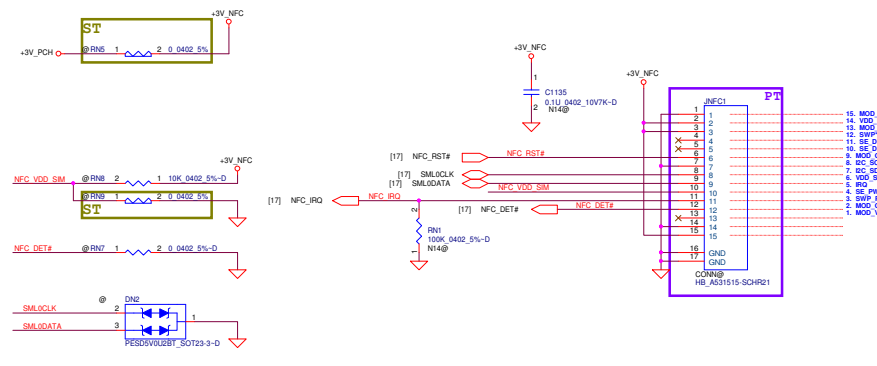
### BATT LED



### BATT LED Power Button



### NFC Connector

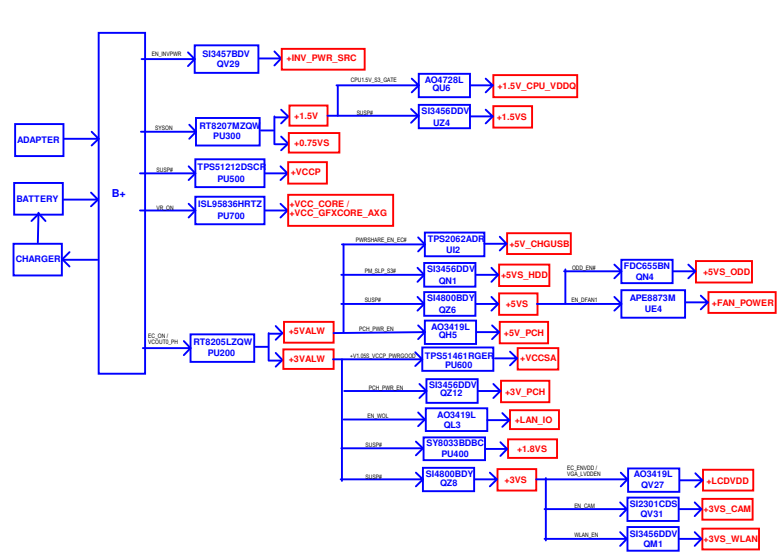


### RTC counter

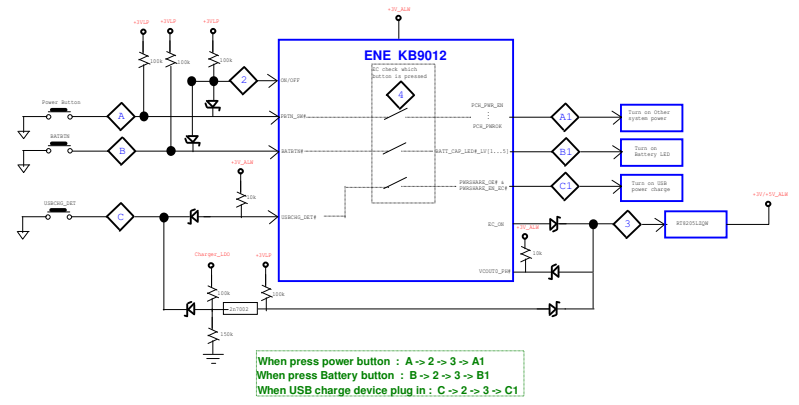
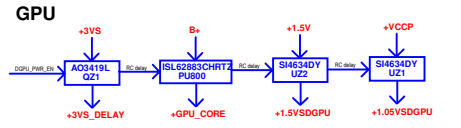
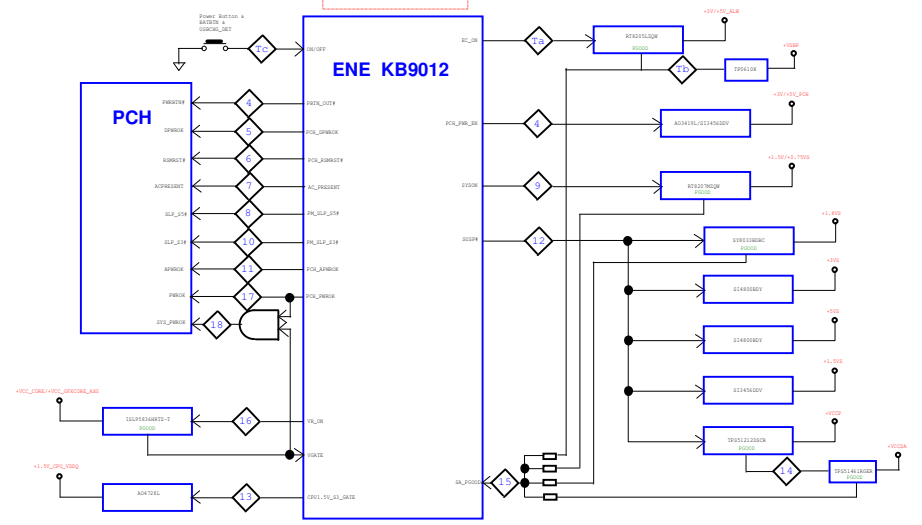


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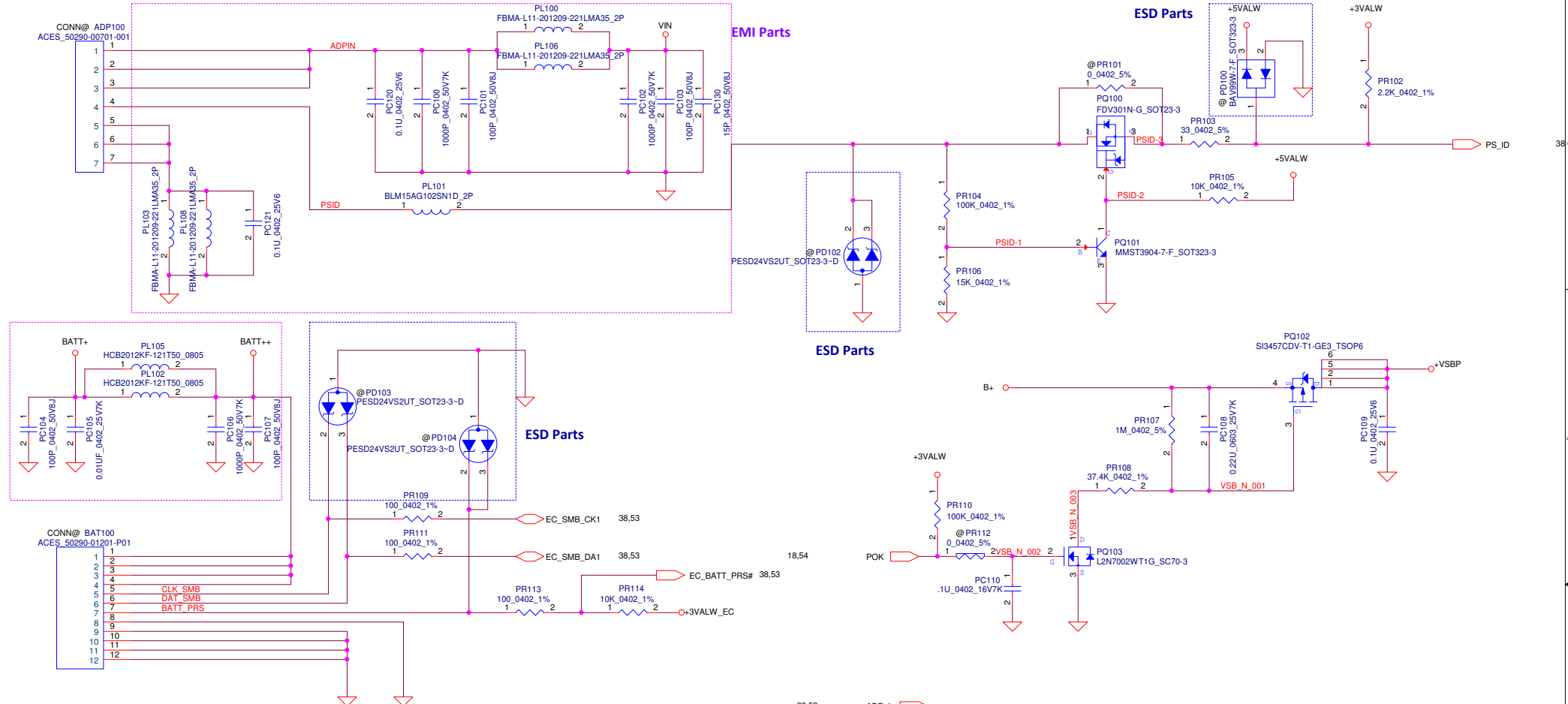




AC mode Ta -> Tb -> Tc  
DC mode Tc -> Ta -> Tb

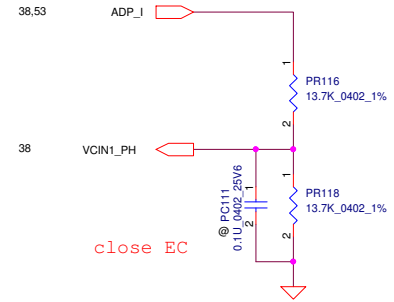


When press power button : A -> 2 -> 3 -> A1  
When press Battery button : B -> 2 -> 3 -> B1  
When USB charge device plug In : C -> 2 -> 3 -> C1



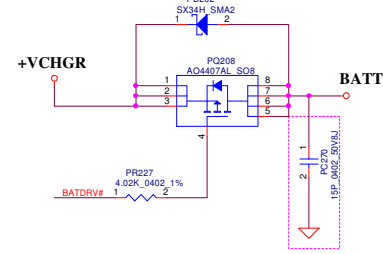
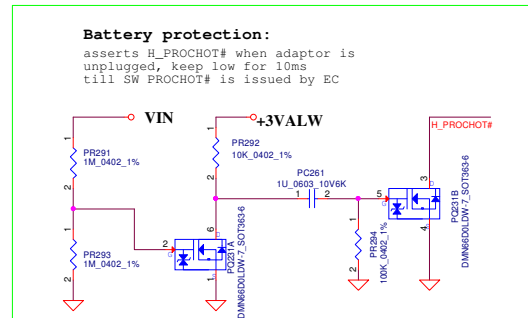
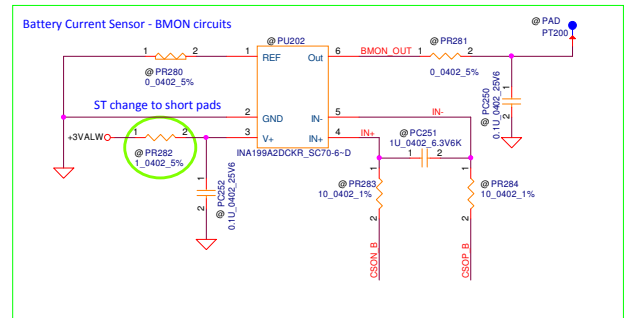
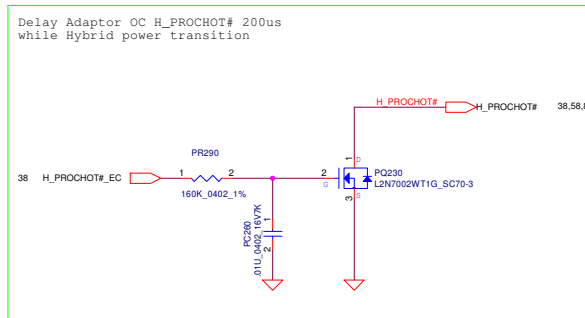
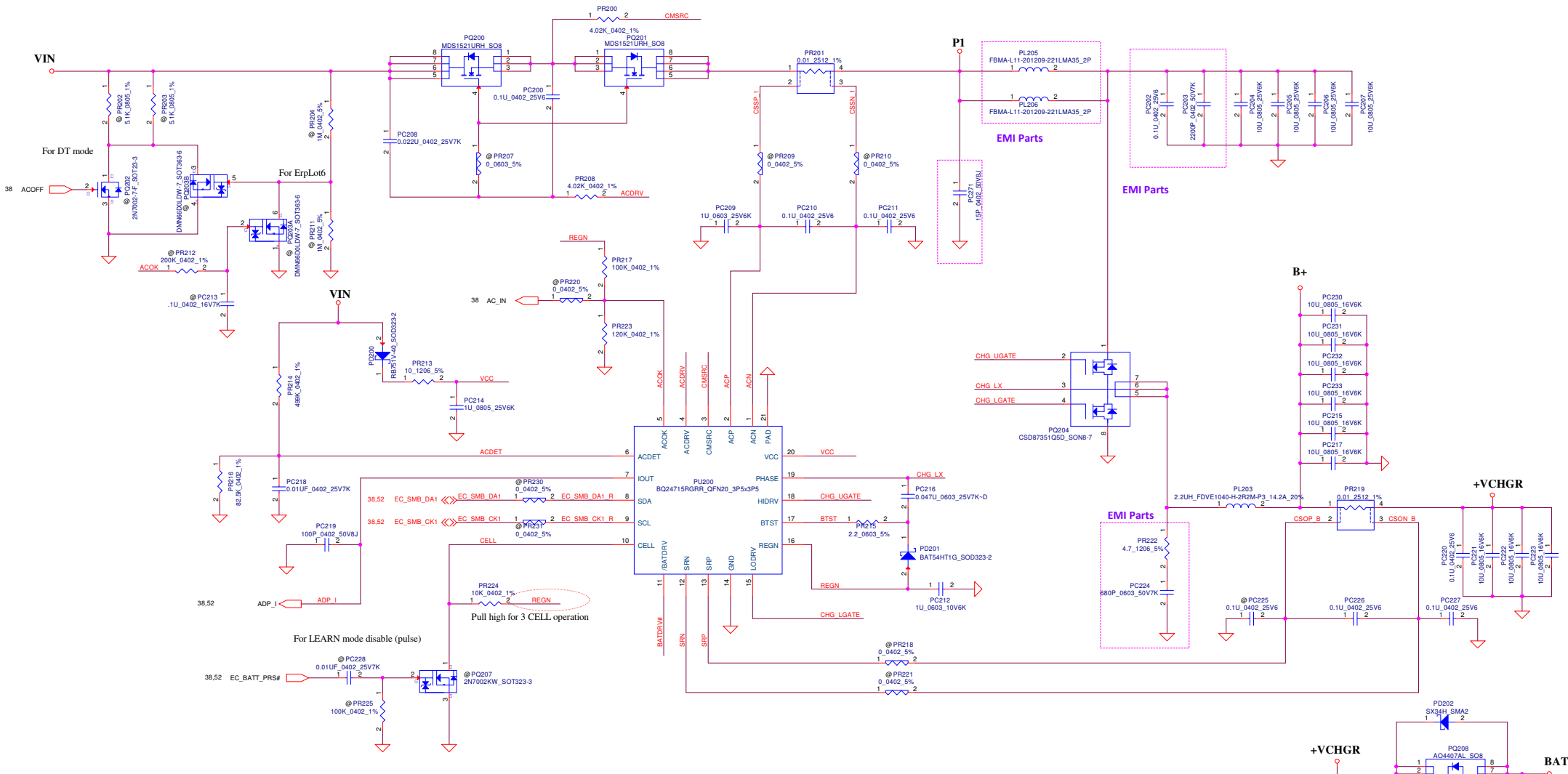
**JIMBTY battery connector**

- SMART Battery:**  
 01.BAT+  
 02.BAT+  
 03.BAT+  
 04.BAT+  
 05.CLK\_SMB  
 06.DAT\_SMB  
 07.BATT\_PRS  
 08.SYS\_PRS  
 09.GND  
 10.GND  
 11.GND  
 12.GND



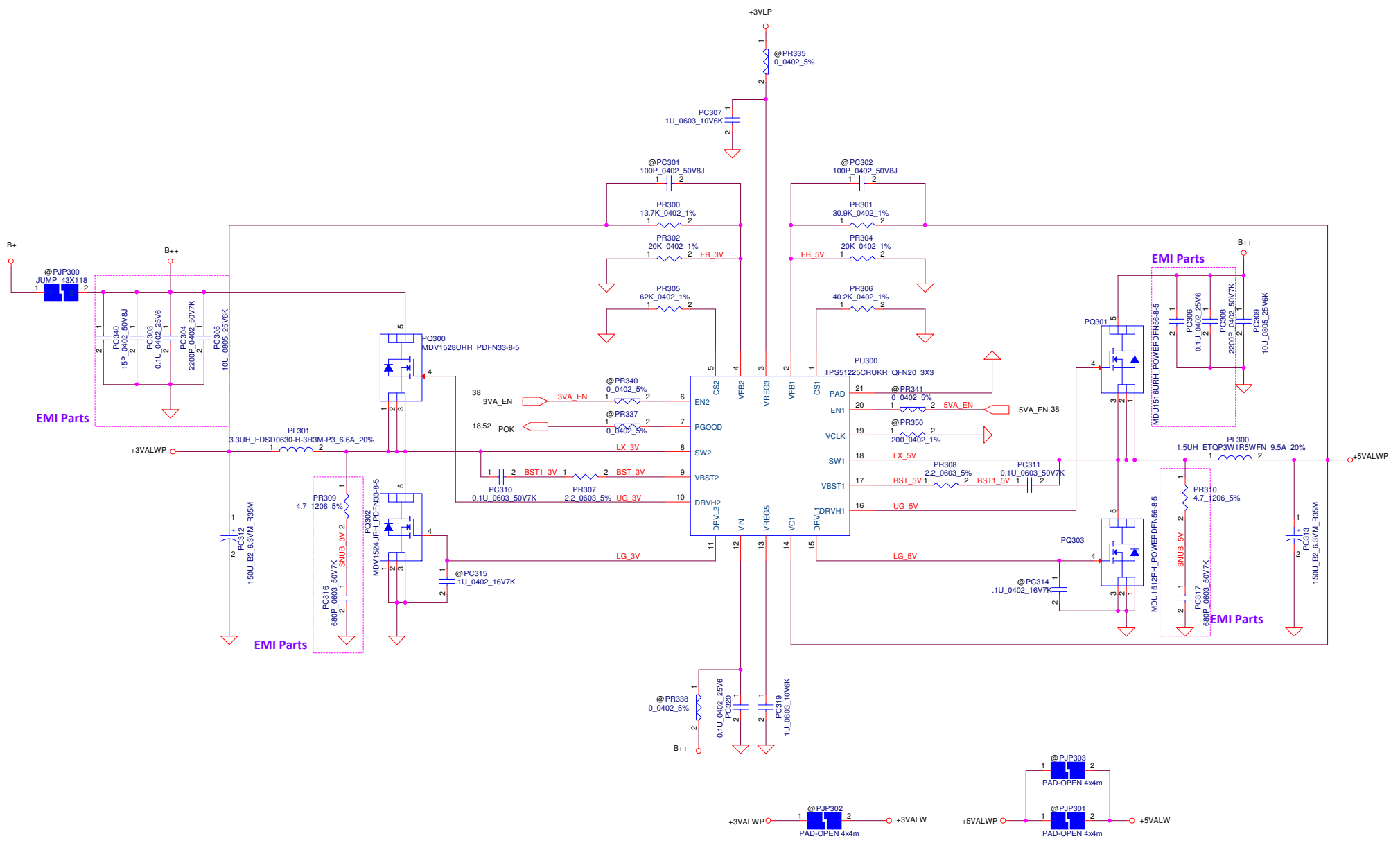
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<b>PWR-DCIN / BATT CONN / OTP</b>			
File	Document Number		Rev
	<b>LA-9941P</b>		<b>0.1</b>
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**3S3P**  
**CC = 5.28A**  
**CV = 3S (12.6V)**

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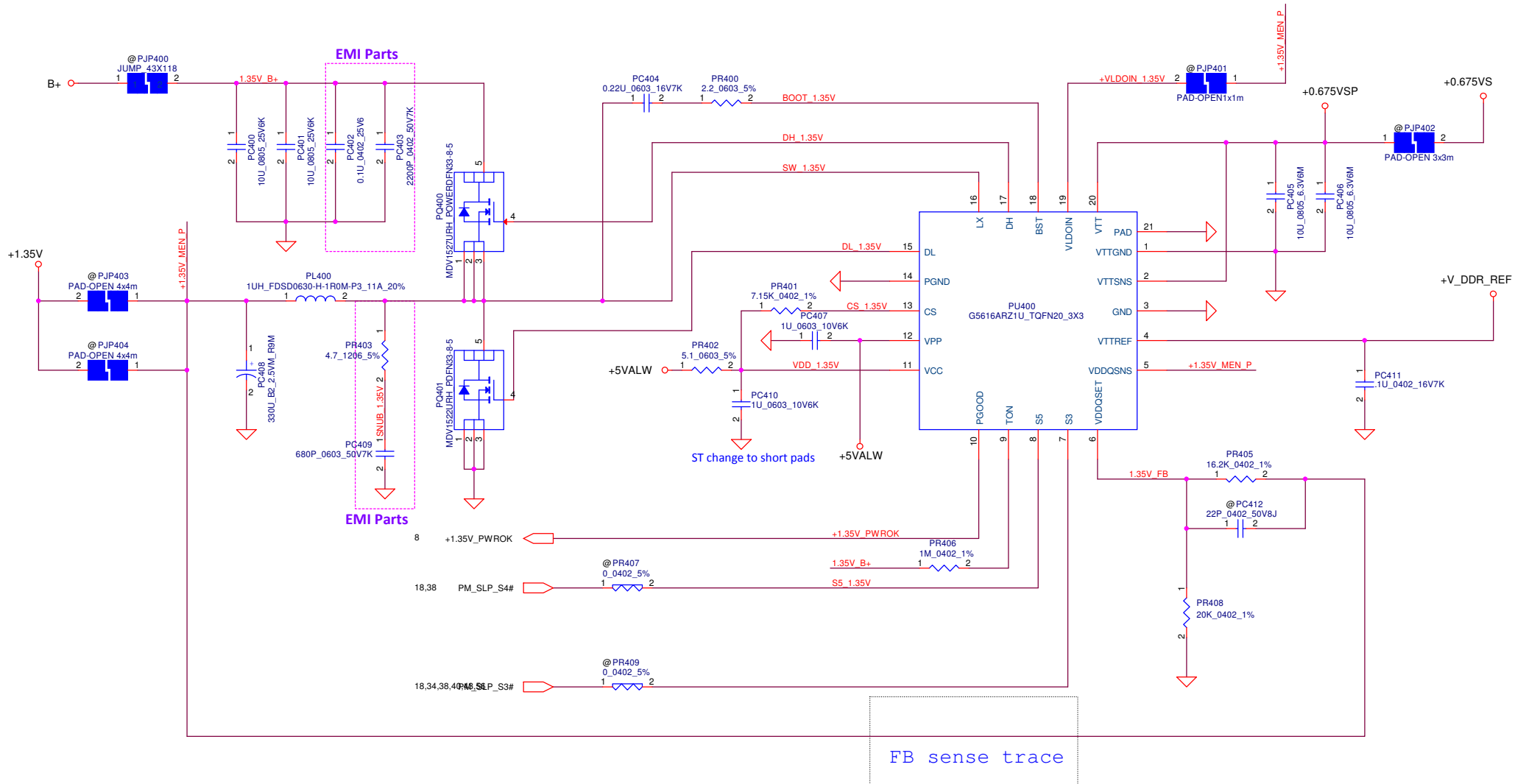
**3. 3VALWP**  
**TDC 4.6A**  
**Peak Current 6.5A**  
**OCP current 7.8A**

**5VALWP**  
**TDC 7.9A**  
**Peak Current 11.3A**  
**OCP current 13.4A**

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<b>Title</b>		
<b>PWR-3VALWP/5VALWP</b>		
<b>Size</b>	<b>Document Number</b>	<b>Rev</b>
<b>LA-9941P</b>		<b>0.1</b>
<b>Date:</b> Wednesday, September 04, 2013 <b>Sheet</b> 54 <b>of</b> 62		



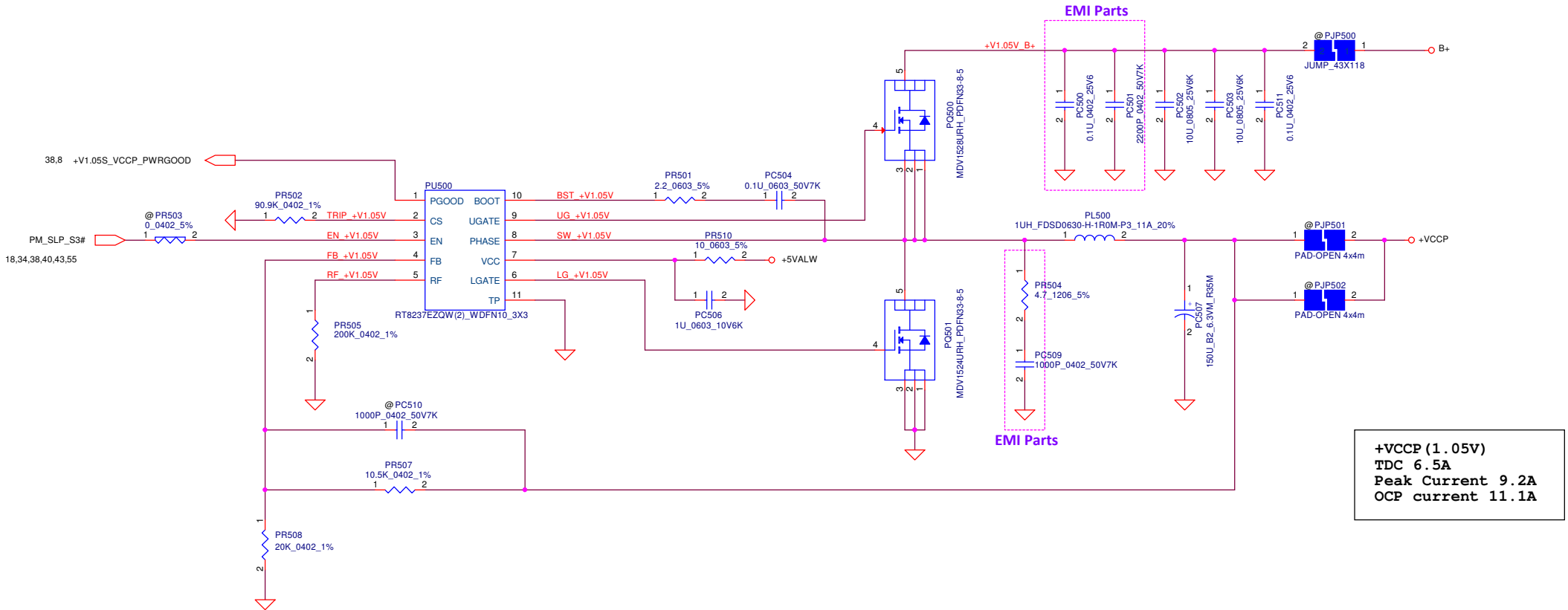
1.35Volt +/- 5%  
 TDC 7.2A  
 Peak Current 10.2A  
 OCP current 12.2A

0.675Volt +/- 5%  
 TDC 0.7A  
 Peak Current 1A  
 OCP Current 1.1A


FB sense trace

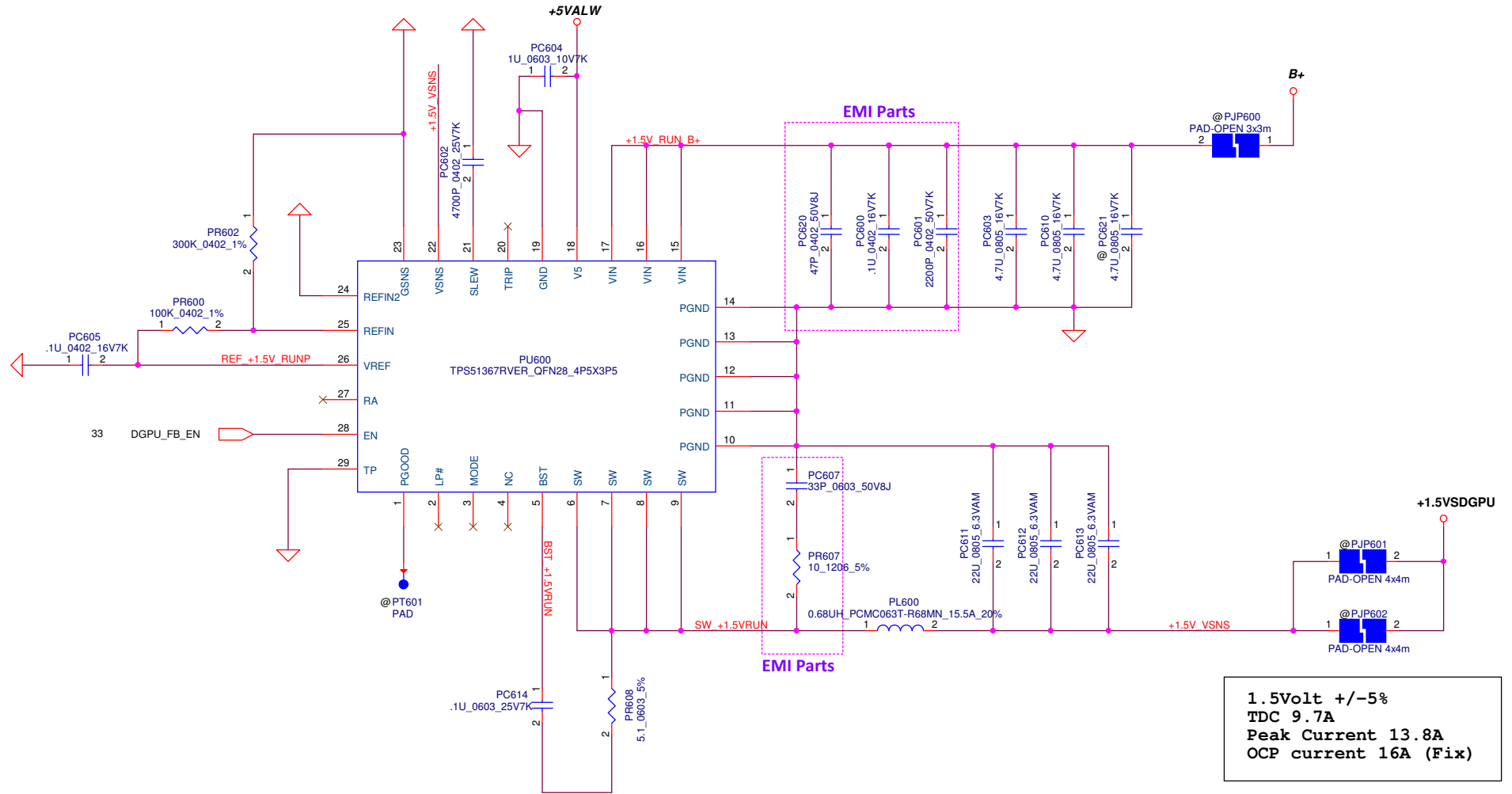
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<b>Compal Electronics, Inc.</b>		
<b>+1.35V MEN/+0.675V DDR VTT</b>		
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		<b>Compal Electronics, Inc.</b>	
		<b>PWR-V1.05S_VCCPP</b>	
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Date:	Wednesday, September 04, 2013	Sheet	56 of 62
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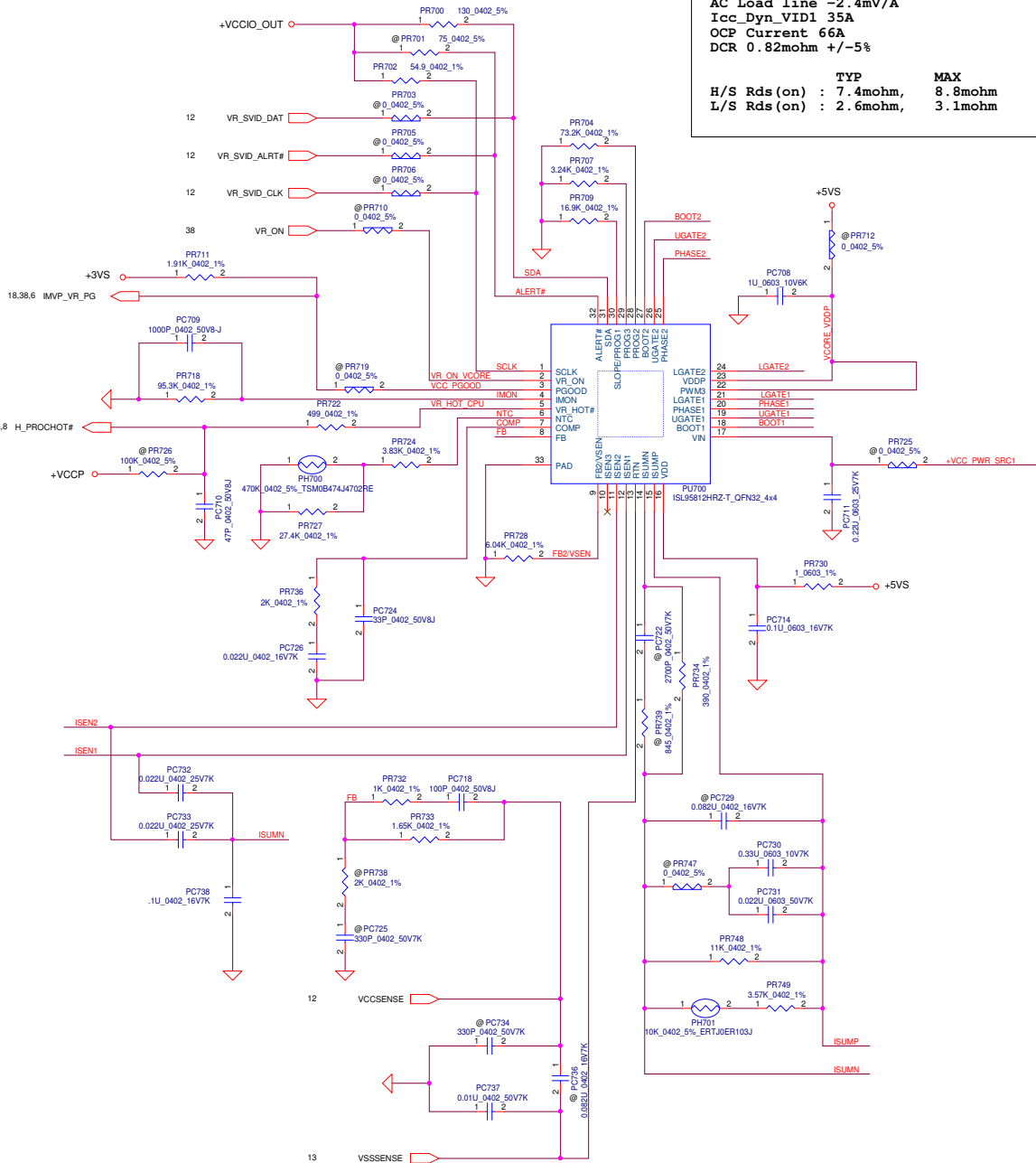
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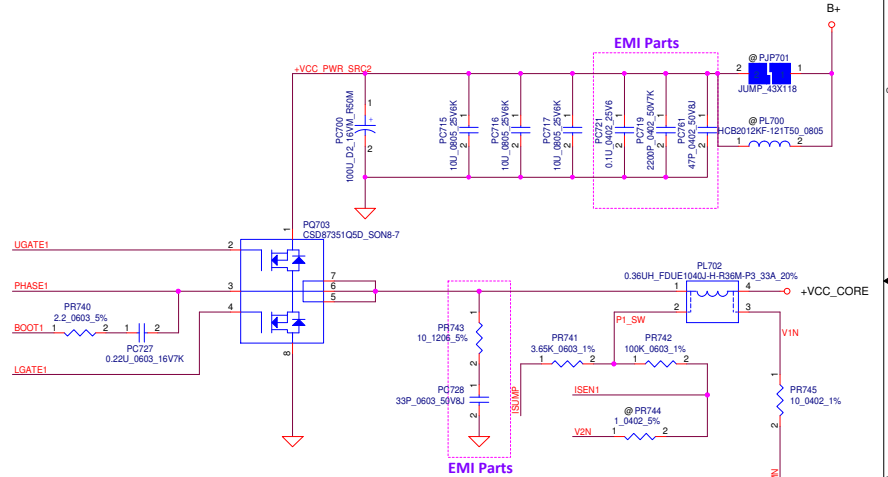
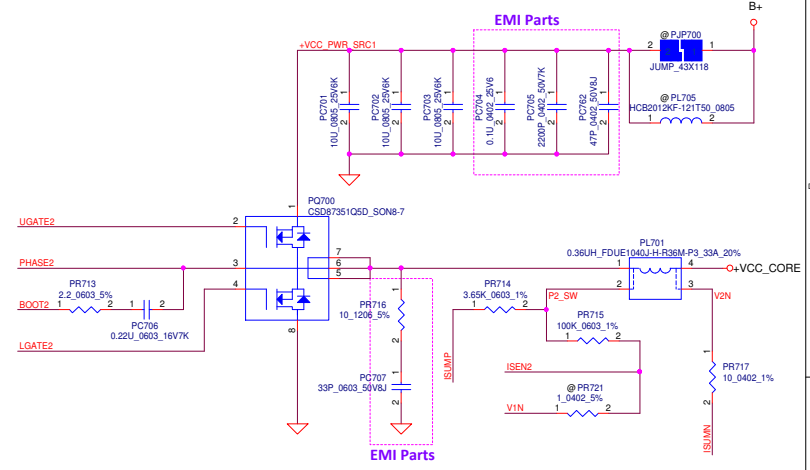
			<b>Compal Electronics, Inc.</b>	
			<b>PWR +1.5VRUN</b>	
Size	Document Number			Rev
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VCC\_core (Base on PDD rev 1.0)(1.8V)  
 TDC 21A  
 TDC PL2 (40Sec):26A  
 Peak Current 55A  
 DC Load line -1.5mV/A  
 AC Load line -2.4mV/A  
 Icc\_Dyn\_VID1 35A  
 OCP Current 66A  
 DCR 0.82mohm +/-5%

H/S Rds(on) : 7.4mohm, 8.8mohm  
 L/S Rds(on) : 2.6mohm, 3.1mohm



Local sense put on HW site



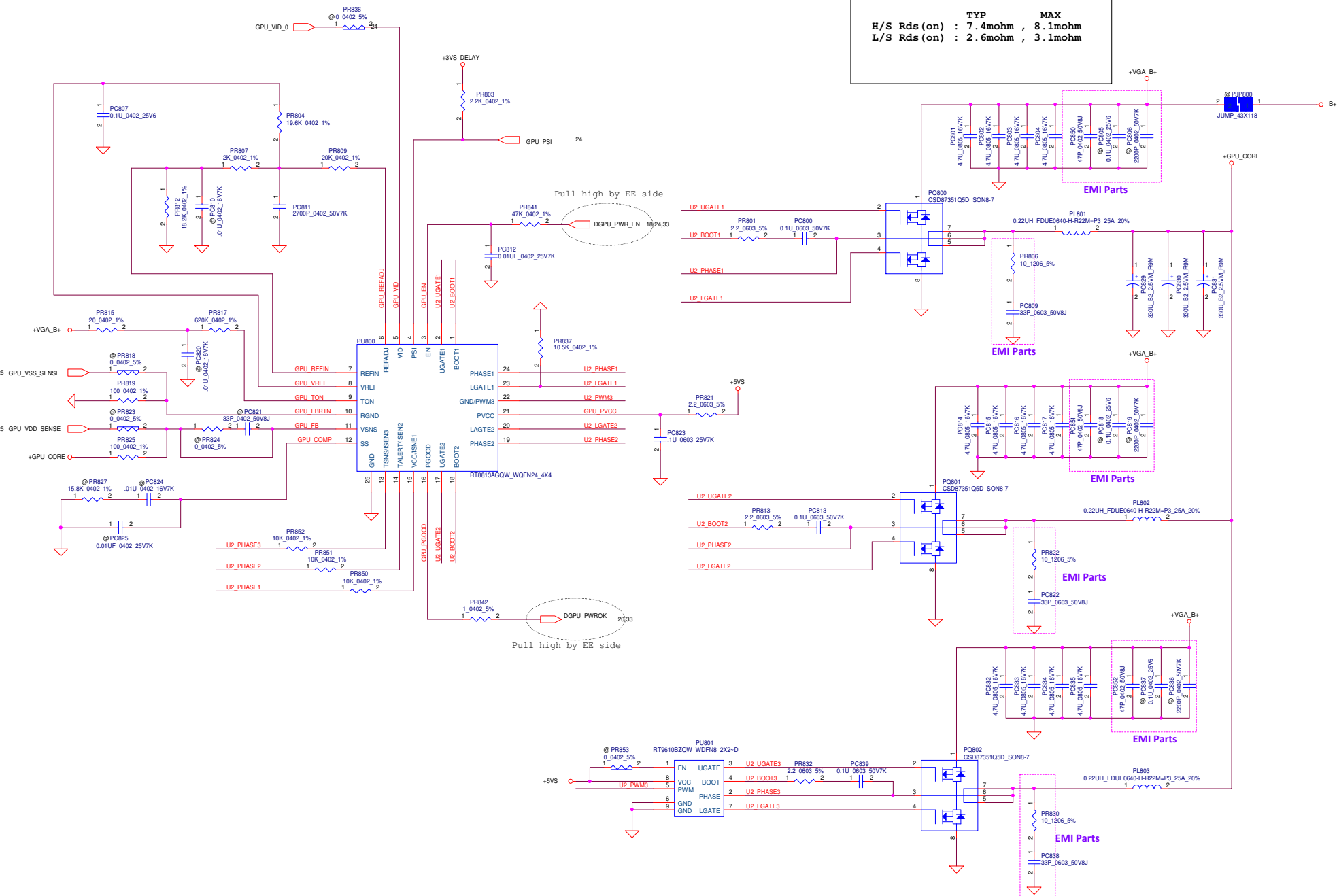
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		<b>Compal Electronics, Inc.</b> <b>+VCC CORE</b>	
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**GPU\_CORE (0.95V)**  
**TDC 45A**  
**Peak Current 75A**  
**OCV current 86A**  
**DCR 0.97mohm +/- 5%**

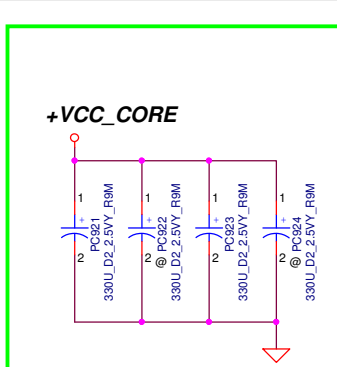
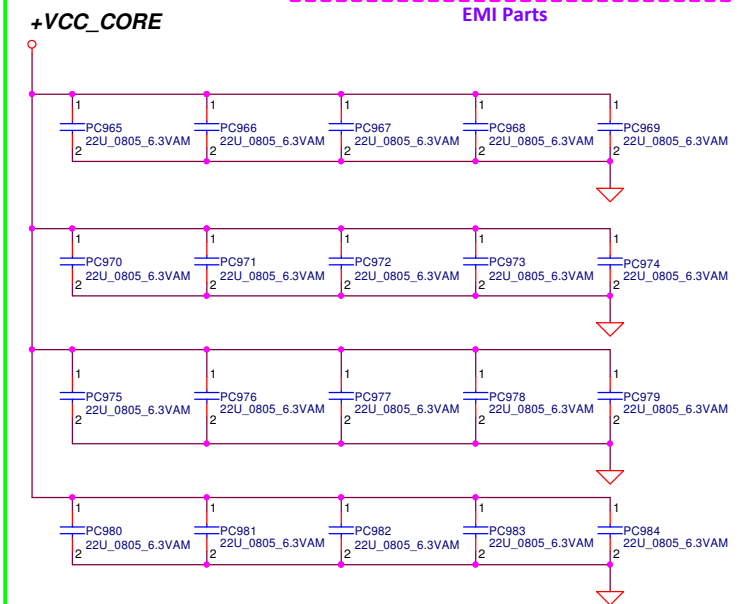
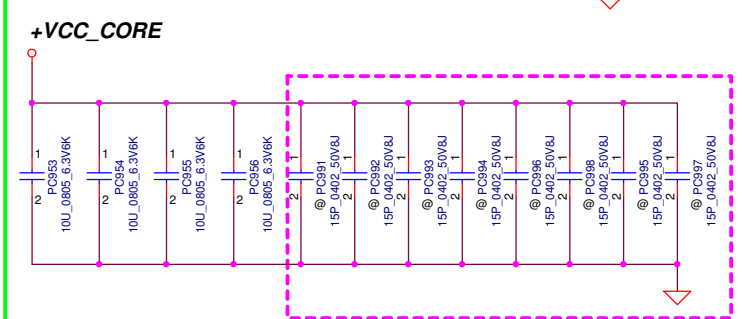
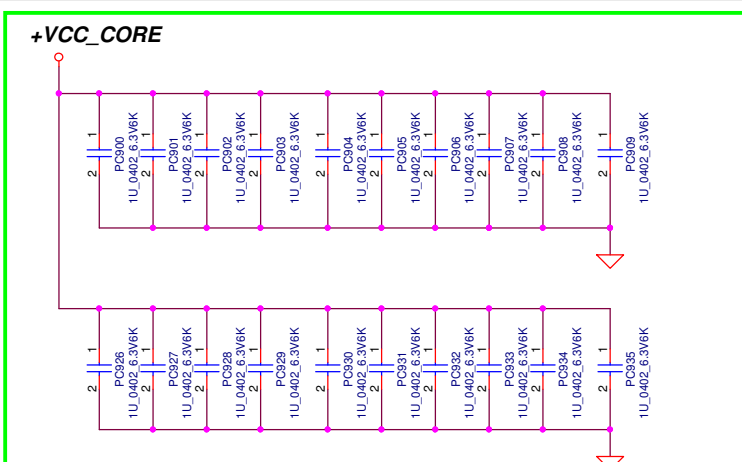
**TYP      MAX**  
**H/S Rds (on) : 7.4mohm , 8.1mohm**  
**L/S Rds (on) : 2.6mohm , 3.1mohm**



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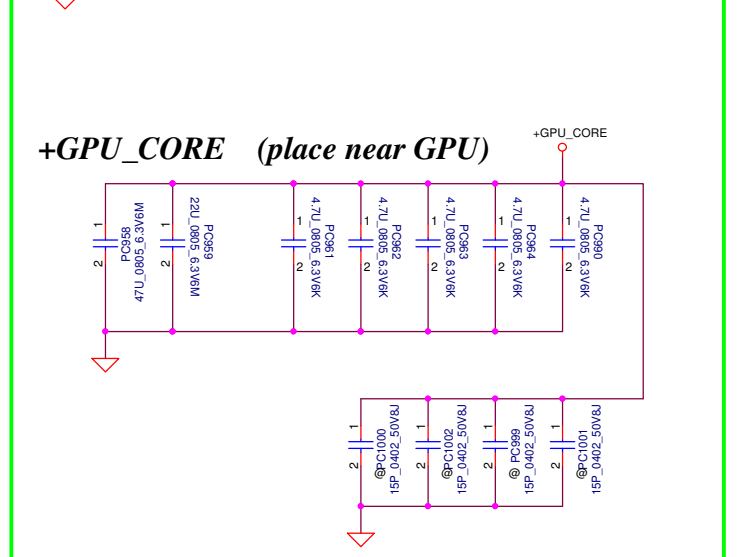
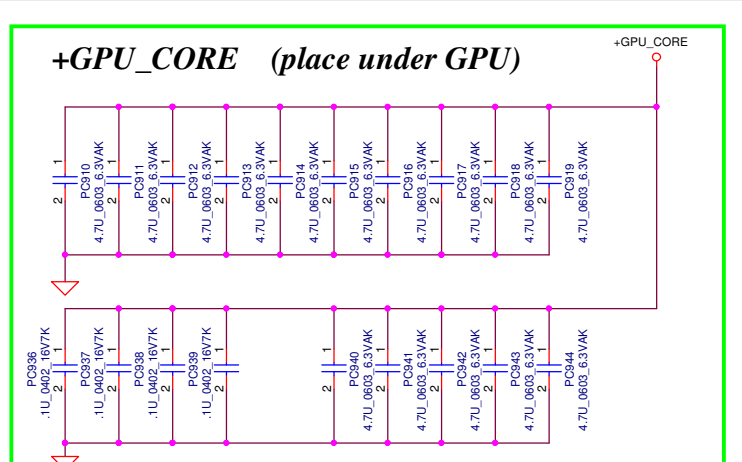
		<b>Compal Electronics, Inc.</b>	
		<b>VGA CORE</b>	
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Based on PDDG rev 1.1 Table 5-2.

Design guide:  
+VCC\_CORE  
1. 470uF\*4 (SGA0000420L)  
2. 22uF\*20 (SE000008L80)  
3. 10uF\*4 (SE160106M8L)  
4. 1uF\*20 (SE000000K8L)

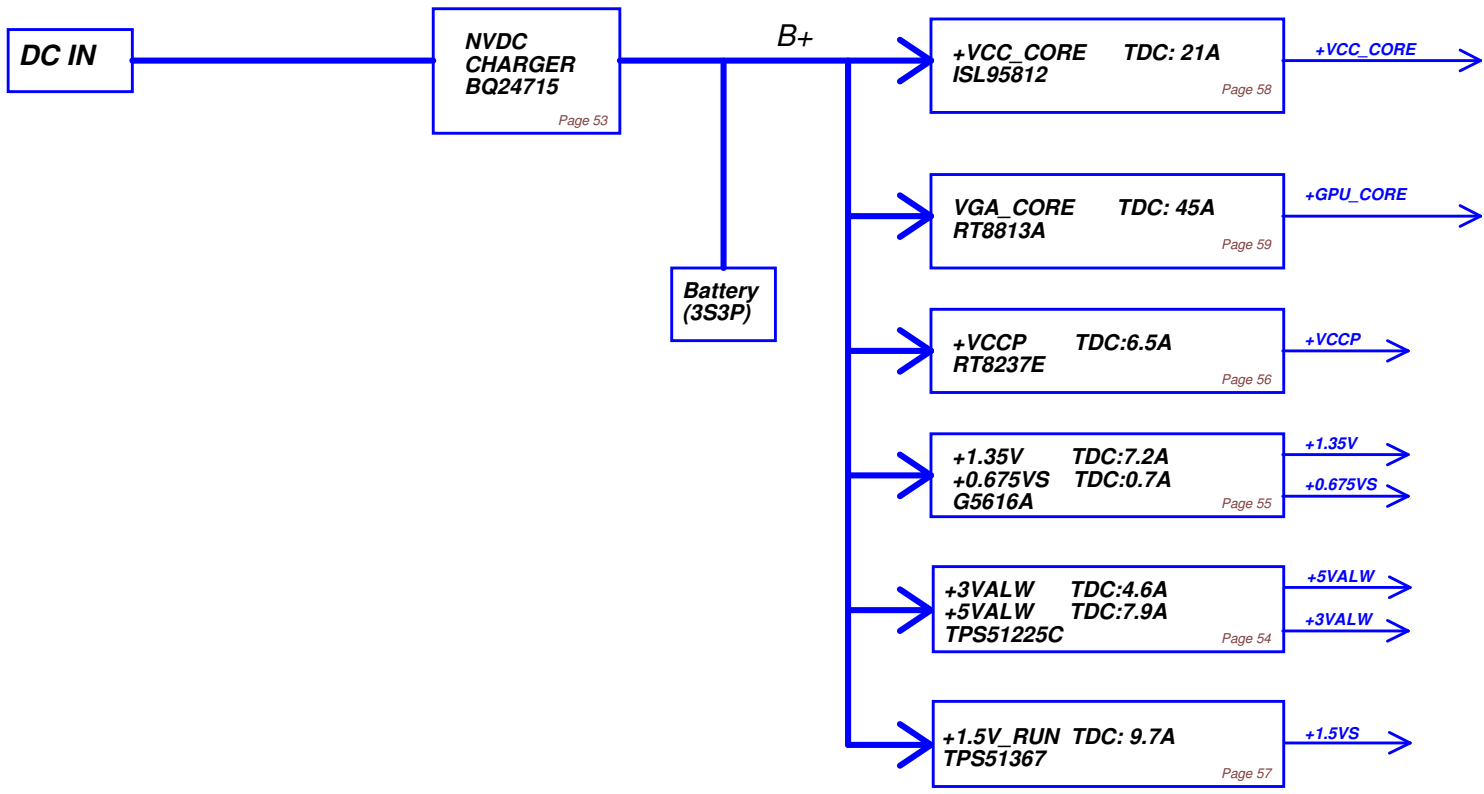


Under:  
1. 4.7uF\*10 (SE000008L80)  
2. 0.1uF\*4 (SE160106M8L)  
Near:  
1. 4.7uF\*5 (SE093475K80)  
2. 22uF\*1 (SE000001120)  
3. 47uF\*1 (SE000000PL0L)  
4. 33uF\*1 (SGA20331E10)


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		<b>Compal Electronics, Inc.</b>	
		<b>PROCESSOR DECOUPLING</b>	
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			<b>Compal Electronics, Inc.</b>	
			<b>POWER BLOCK DIAGRAM</b>	
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[AC in]

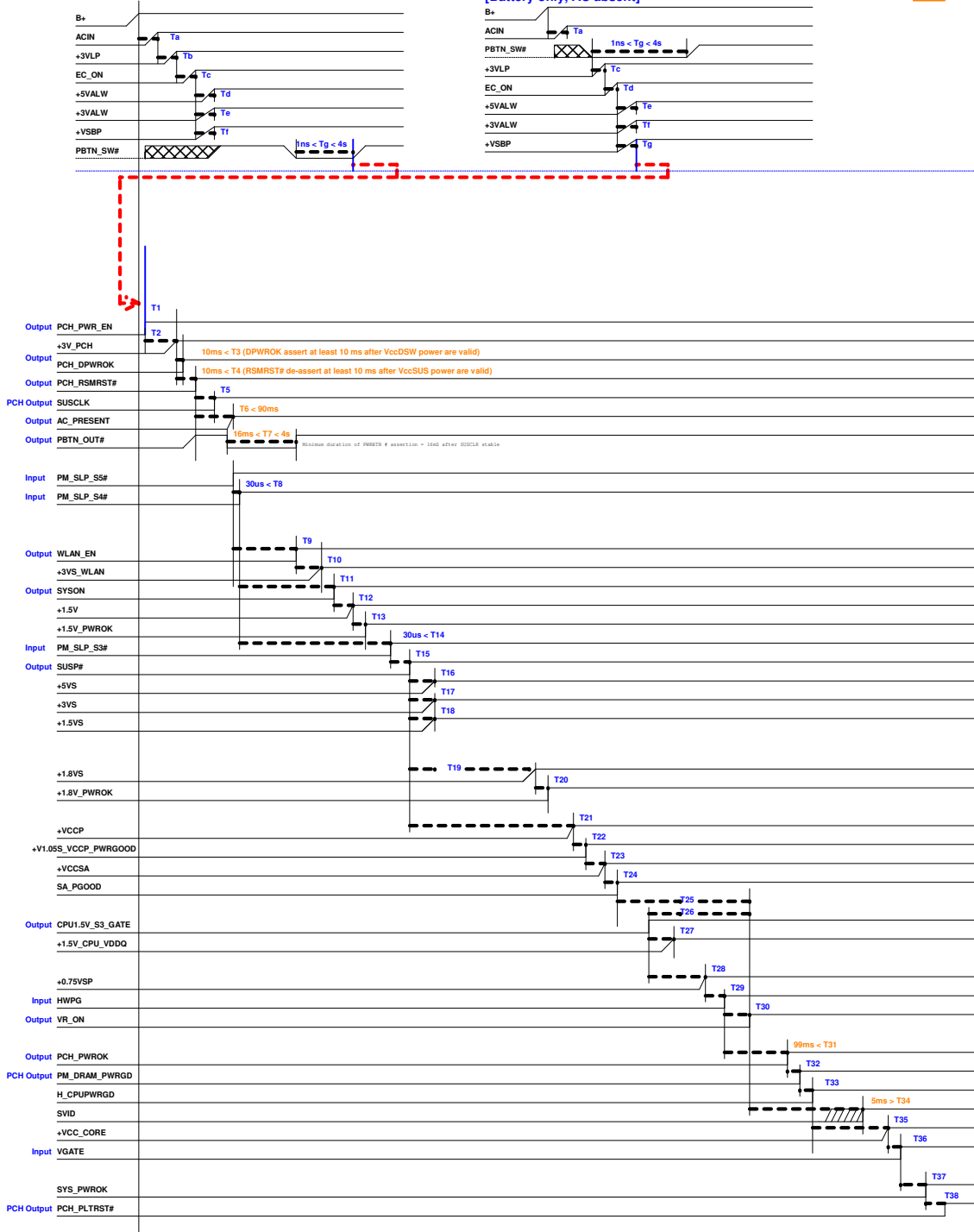
[Battery only, AC absent]

EC pay attention timing

# Discrete Power On Sequence

[AC in]

[Battery only, AC absent]



ITEM	Measure Point	Time
Ta	B+	To
Tb	ACIN	To
Tc	+3VLP	To
Td	EC_ON	To
Te	+5VALW	To
Tf	+3VALW	To
Tg	+VSBP	To
Tg	PBTN_SW#	Low pulse width

ITEM	Measure Point	Time
Ta	B+	To
Tb	PBTN_SW#	Low pulse width
Tc	PBTN_SW#	To
Td	+3VLP	To
Te	EC_ON	To
Tf	EC_ON	To
Tg	EC_ON	To

ITEM	Measure Point	Time
T1	PBTN_SW#	To
T2	PCH_PWR_EN	To
T3	+3V_PCH	To
T4	+3V_PCH	To
T5	PCH_RSMRST#	To
T6	SUSCLK	To
T7	AC_PRESENT	To
T8	PBTN_OUT#	To
T9	PM_SLP_S5#	To
T10	PM_SLP_S4#	To
T11	WLAN_EN	To
T12	+1.5V	To
T13	+1.5V_PWRK	To
T14	PM_SLP_S3#	To
T15	SUSP#	To
T16	+5VS	To
T17	+3VS	To
T18	+1.8VS	To
T19	+1.8VS	To
T20	+1.8V_PWRK	To
T21	+VCCP	To
T22	+V1.05S_VCCP_PWRGOOD	To
T23	+VCCSA	To
T24	SA_PGOOD	To
T25	VR_ON	To
T26	CPU1.5V_S3_GATE	To
T27	+1.5V_CPU_VDDQ	To
T28	+0.75VSP	To
T29	HWPG	To
T30	VR_ON	To
T31	PCH_PWRK	To
T32	PM_DRAM_PWRGD	To
T33	H_CPUPWRGD	To
T34	SWID	To
T35	+VCC_CORE	To
T36	VGATE	To
T37	SYS_PWRK	To
T38	PCH_PLTRST#	To
T39	DGPU_PWREN	To
T40	+3VS_DELAY	To
T41	+GPU_CORE	To
T42	+1.5VSDGPU	To
T43	+1.05VSDGPU	To

## GPU power on sequence

