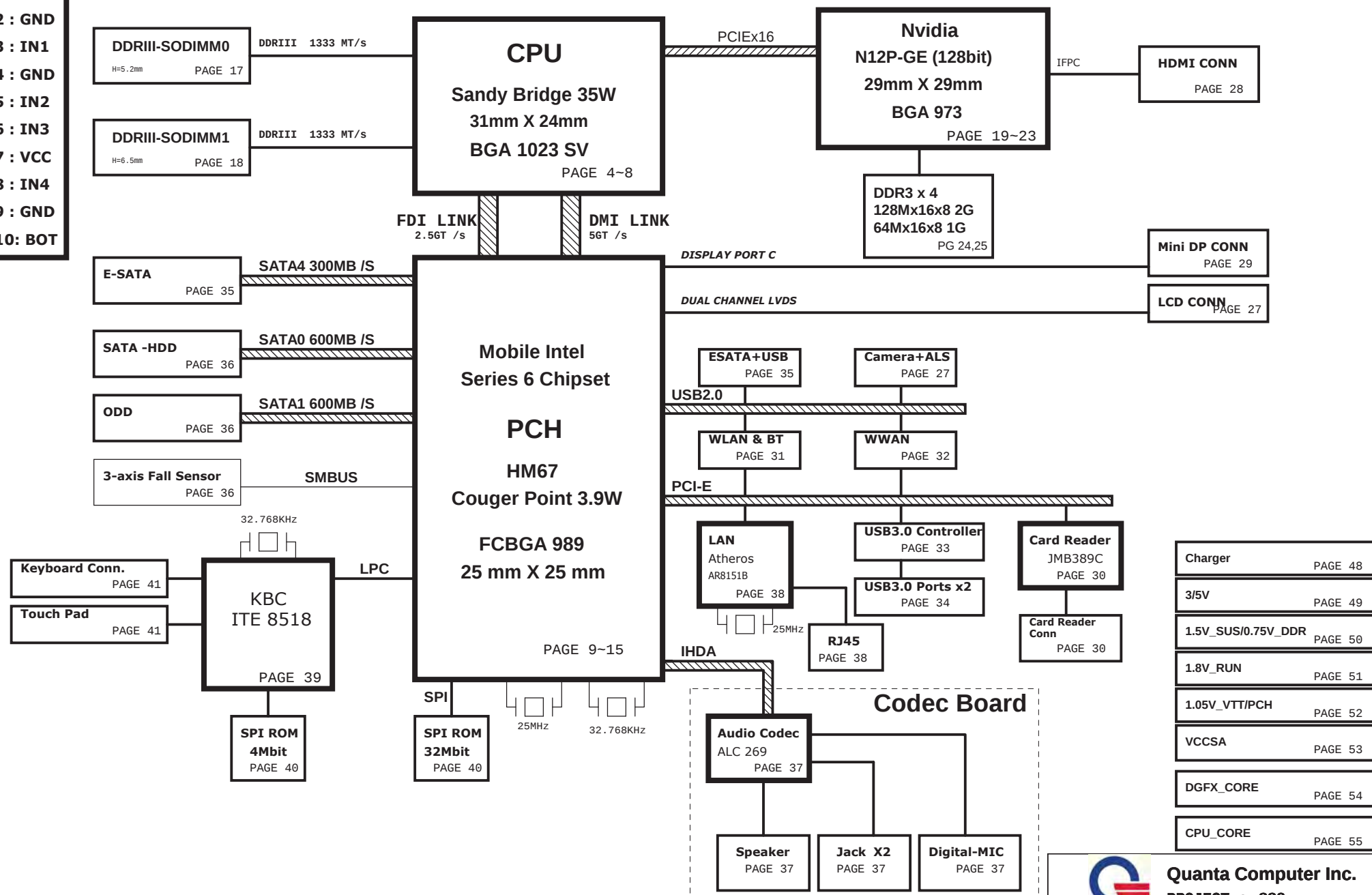


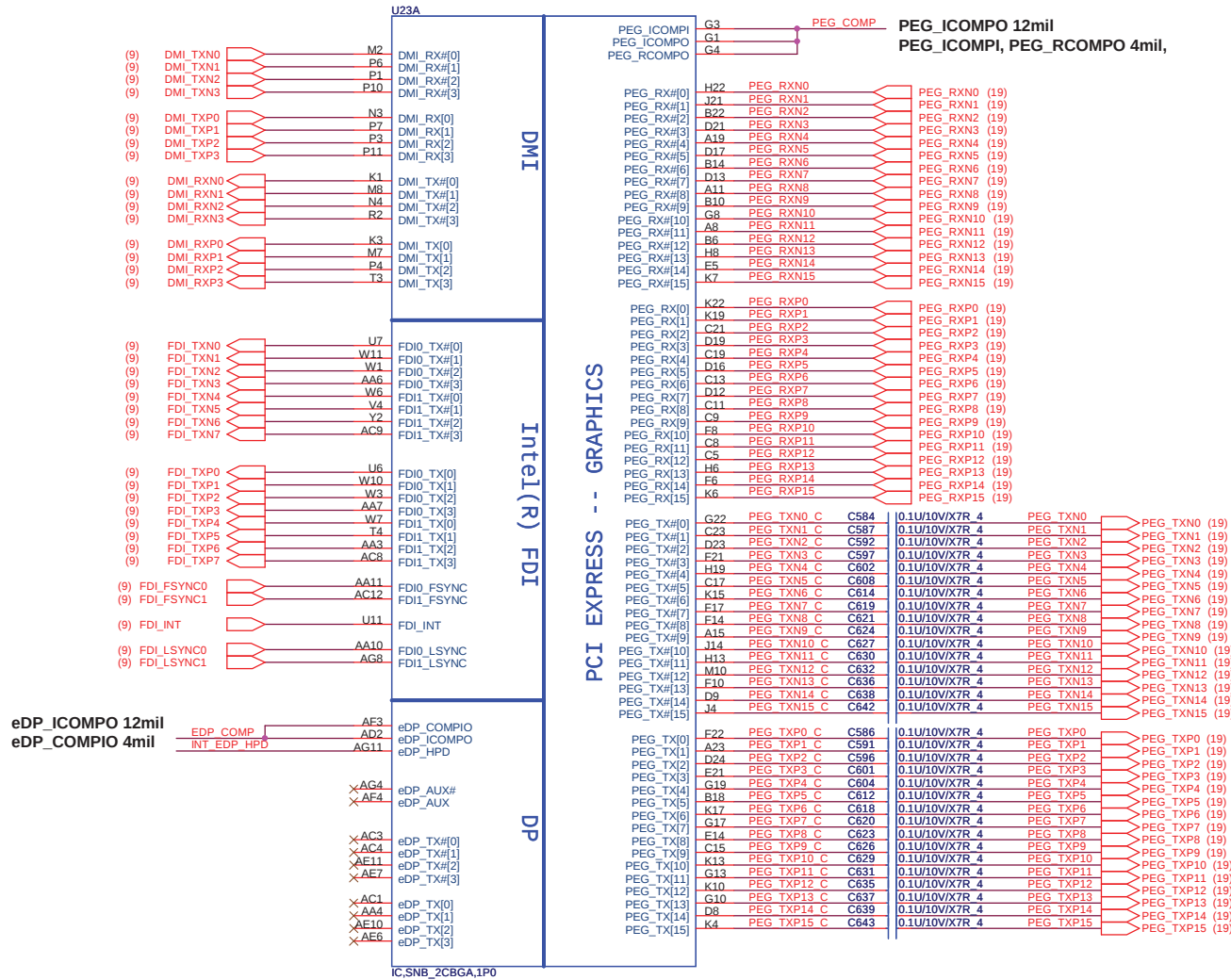
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : GND
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : VCC
LAYER 8 : IN4
LAYER 9 : GND
LAYER 10: BOT



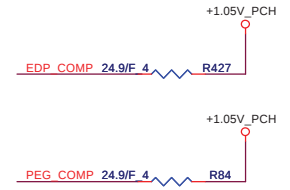
power State					
S0					
S1					
S3					
S4/S5 AC					
S4/S5 DC Only					
AC/DC No Exist					



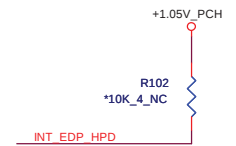
Sandy Bridge Processor (DMI, PEG, FDI)



DP & PEG Compensation

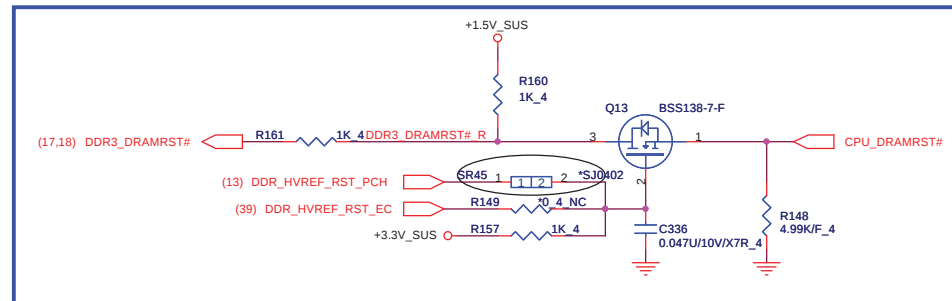


eDP Hot-plug (Disable)



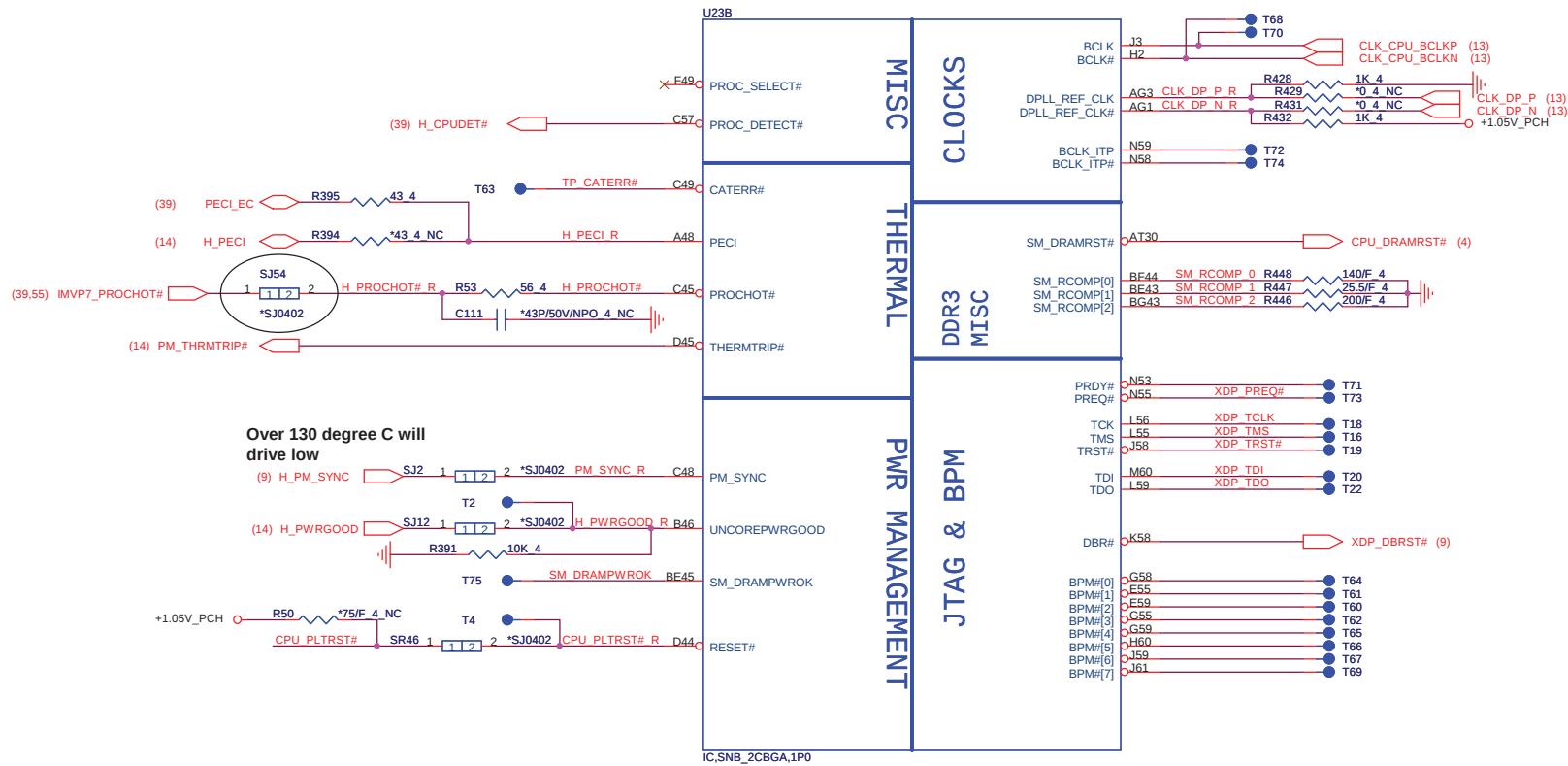
CAD Note: Place PU resistor within 2 inches of CPU

HPD PU/PD resistor values based on CRB and different to DG



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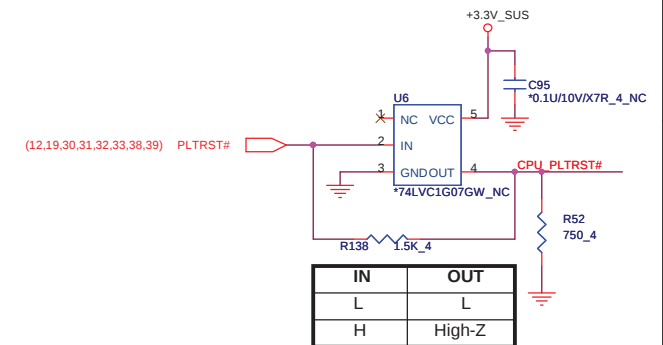
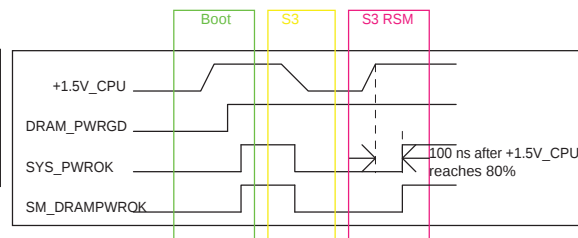
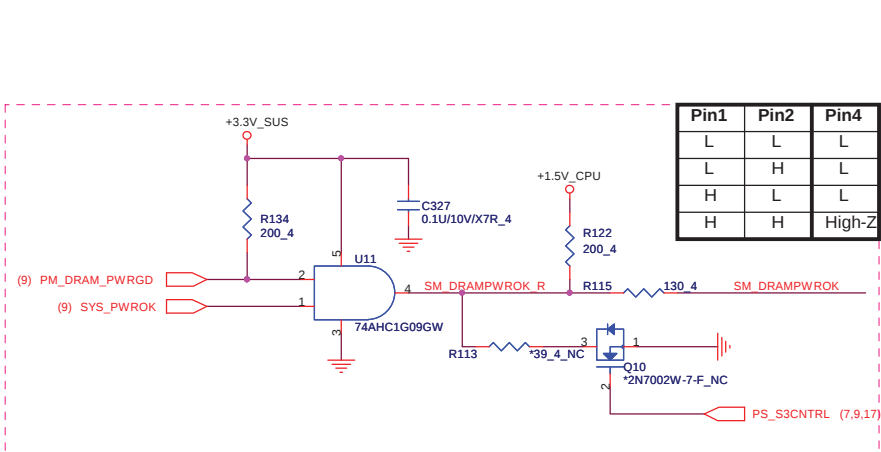
Sandy Bridge Processor (CLK,MISC,JTAG)



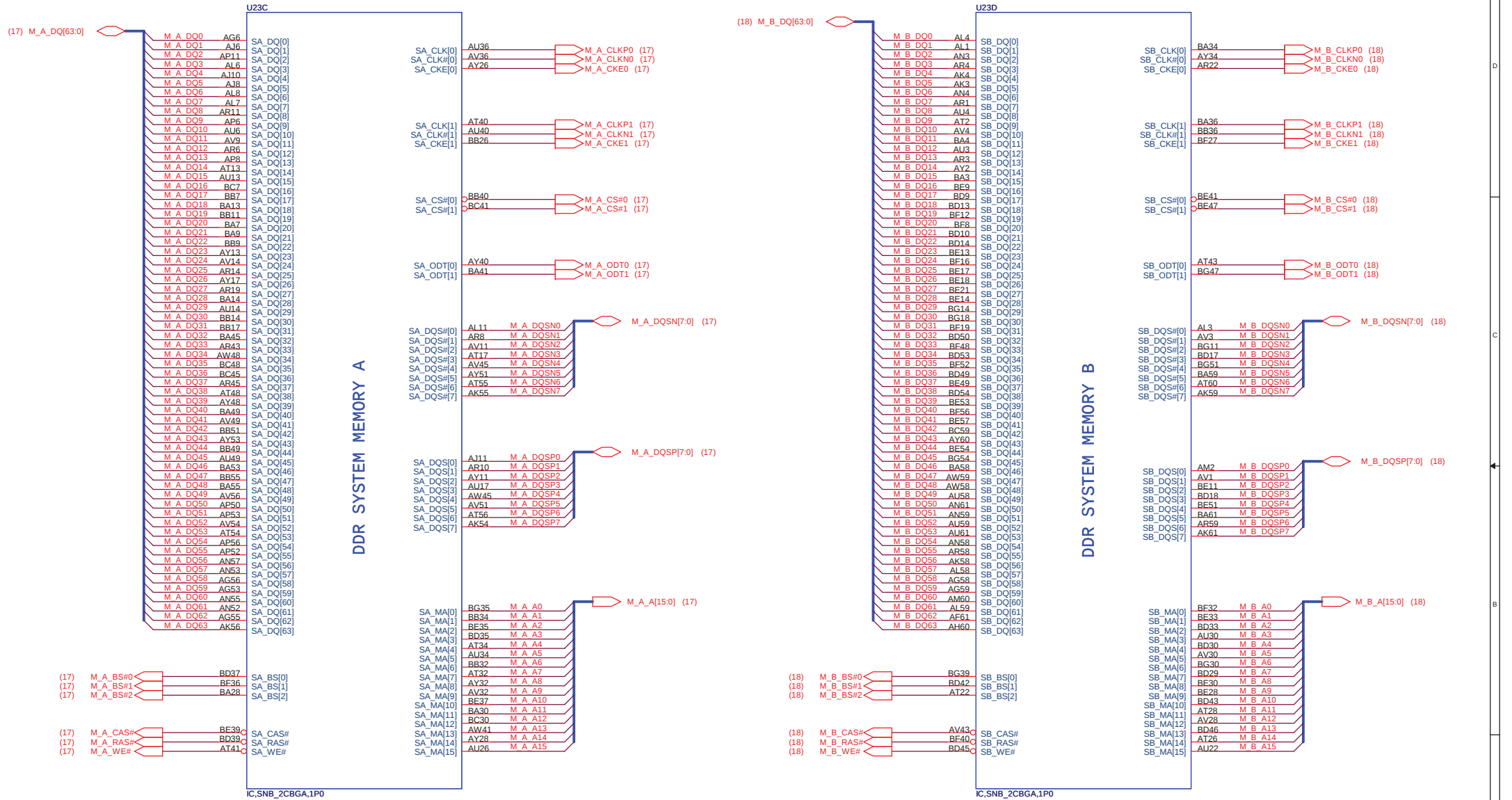
Option for Prochot# function
68 ohm for unused, 62 ohm for used

Signal	Resistor	Jumper Status
H_PROCHOT#	R56	68 4 NC
R_PROCHOT#	R49	62 4 NC
XDP_TMS	R420	51 4
XDP_TDI	R423	51 4
XDP_TDO	R422	51 4
XDP_PREQ#	R425	51 4 NC
XDP_TCLK	R421	51 4
XDP_TRST#	R417	51 4

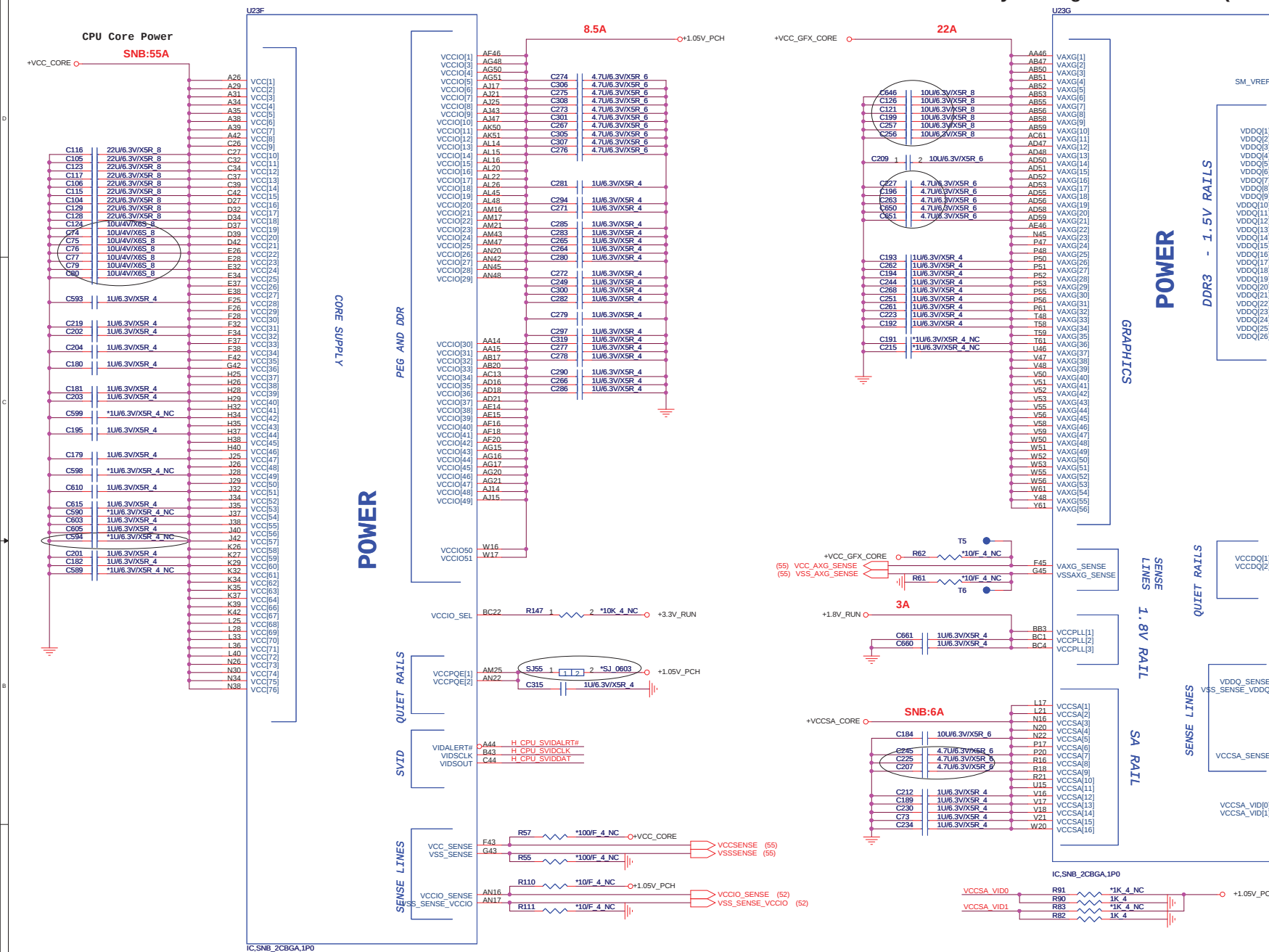
When MP, JTAG PU/PP resistor can be removed? (Yes Intel, TDI, TDO, TMS, TRST#, TCK, PREQ#, PRDY#)



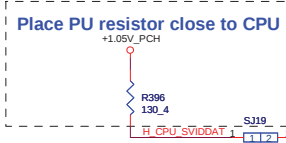
Sandy Bridge Processor (DDR3)



3	4
Sandy Bridge Processor (POWER)	



Layout note: need routing together and ALERT need between CLK and DATA

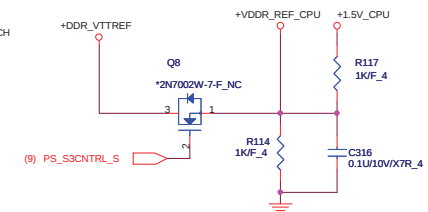


SVID DATA

Close to VR

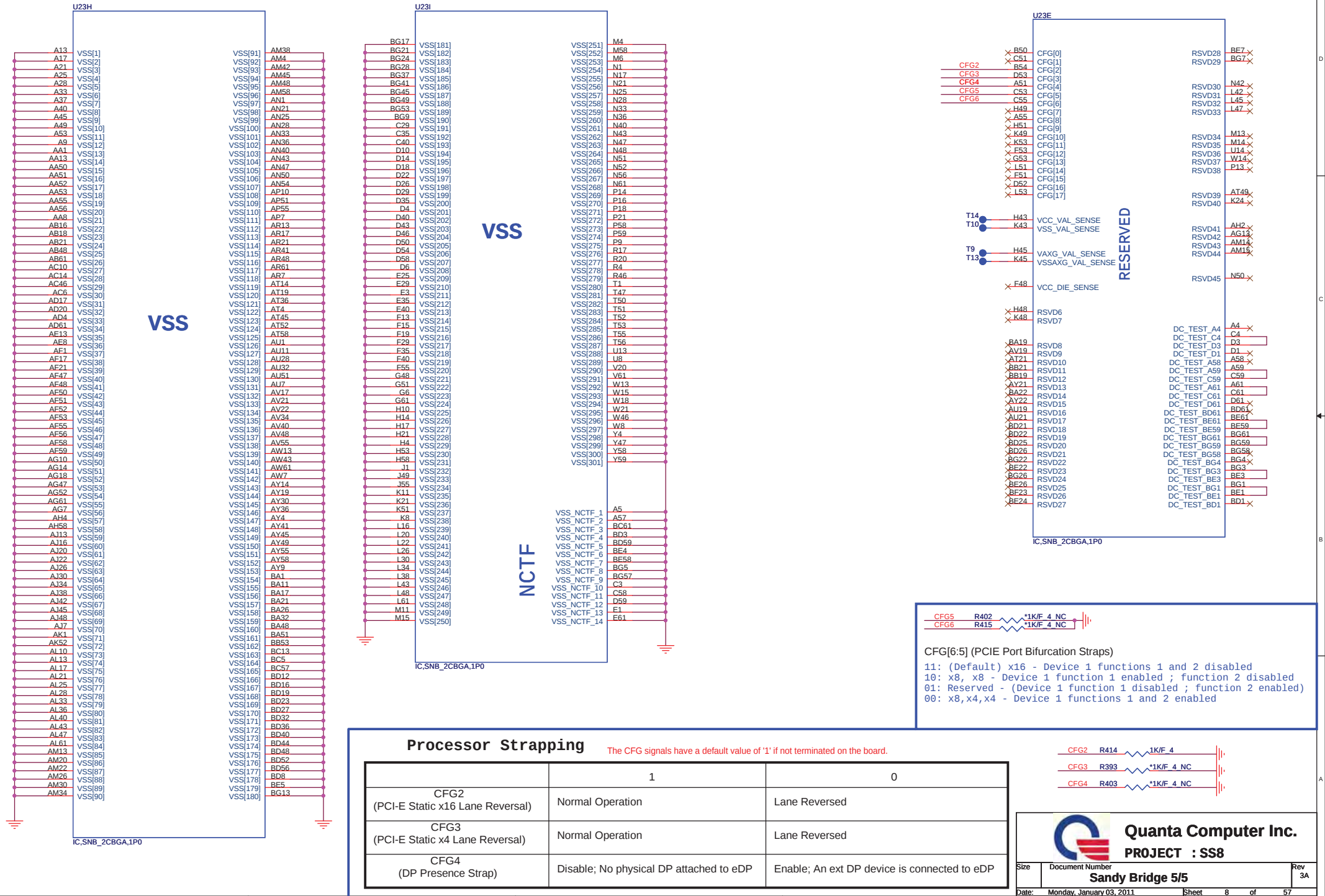


SVID ALERT



Sandy Bridge Processor (GND)

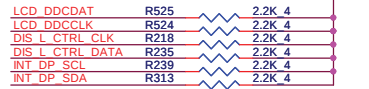
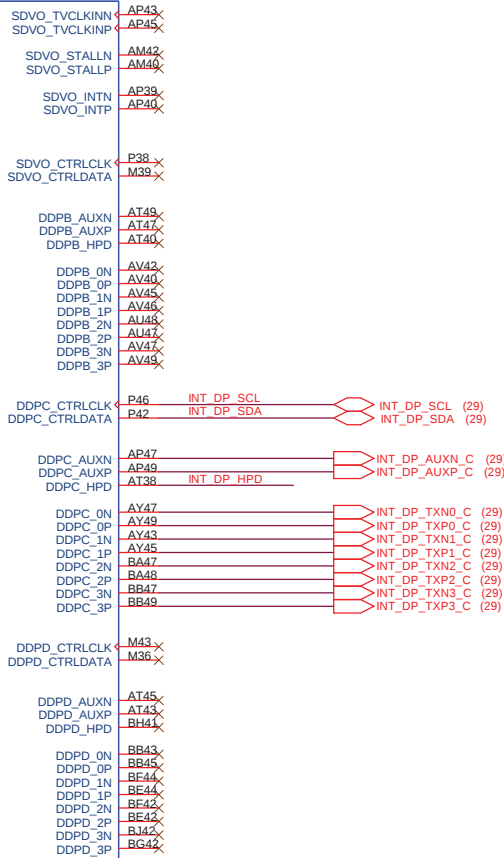
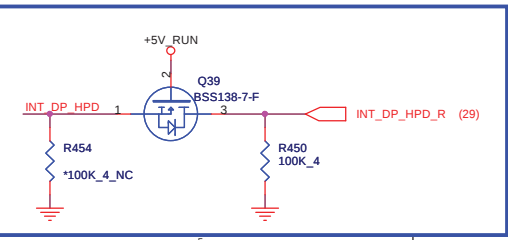
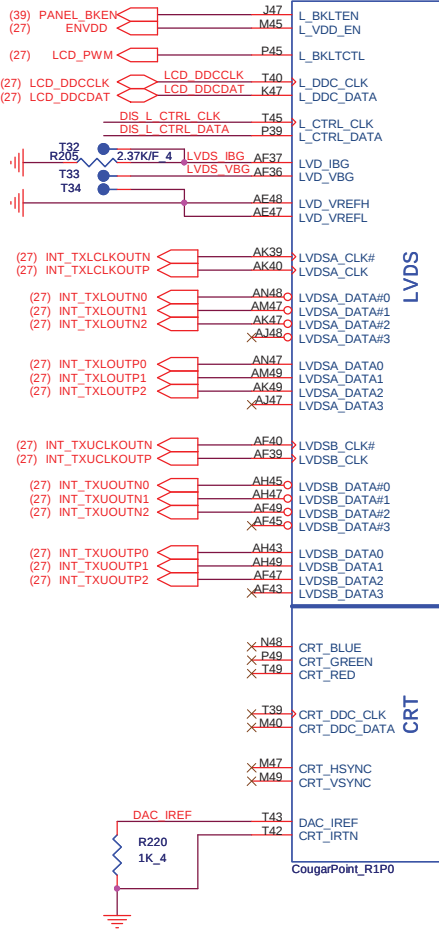
Sandy Bridge Processor (RESERVED, CFG)



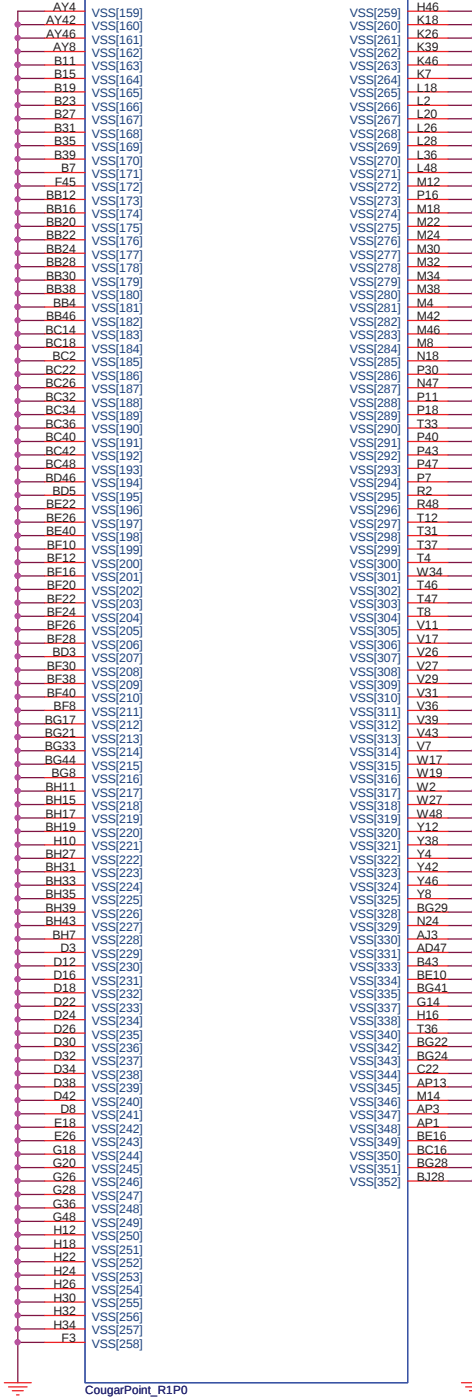
Cougar Point (LVDS, DDI)

Cougar Point (GND)

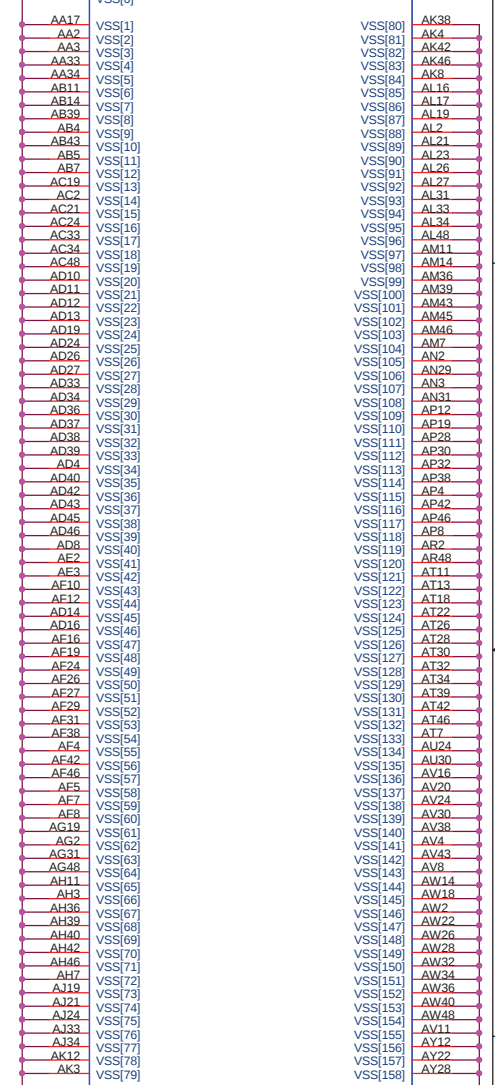
U27D



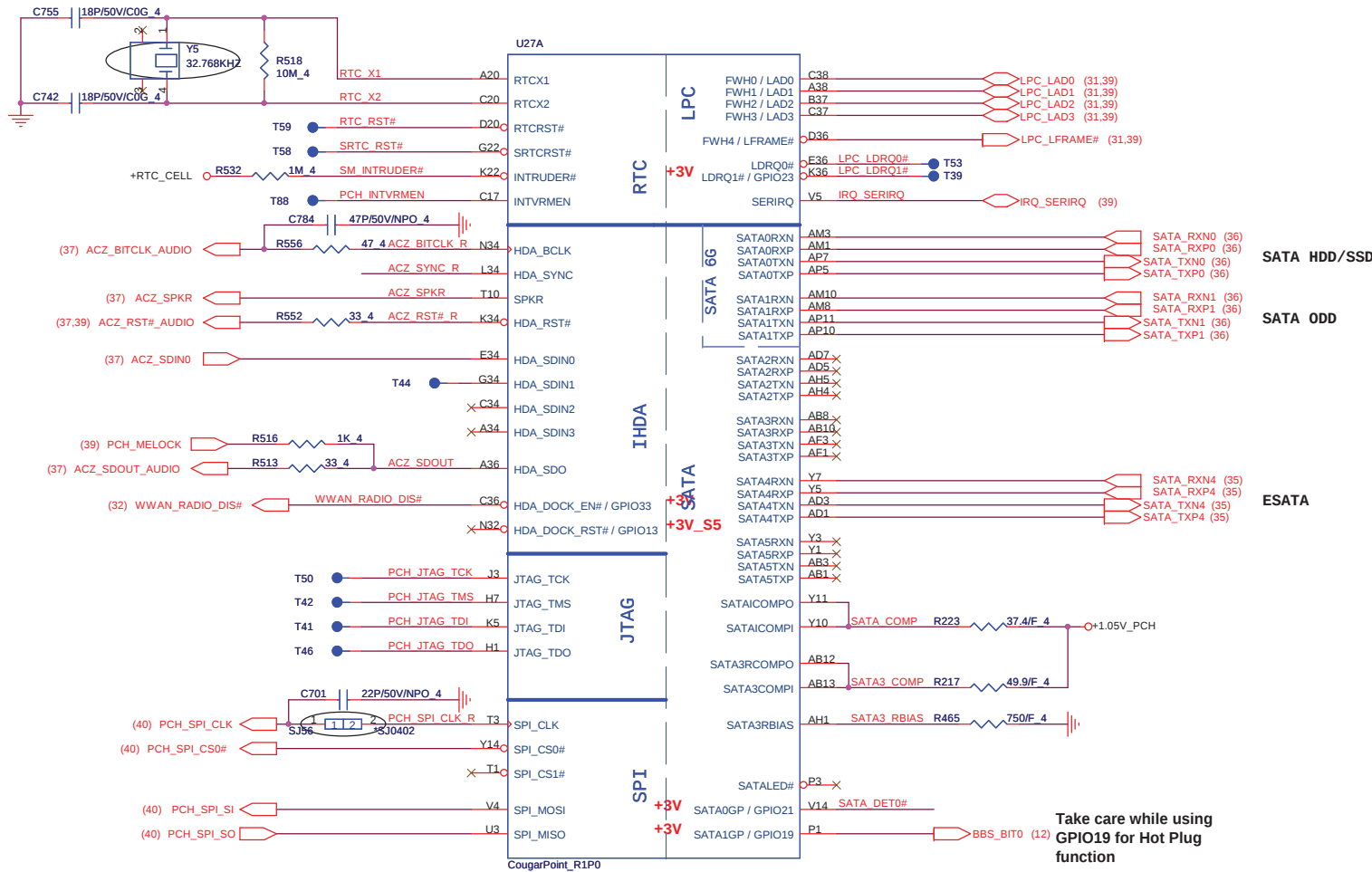
U27I



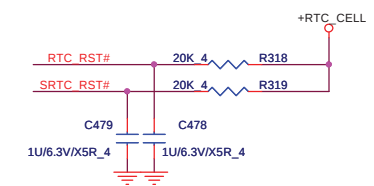
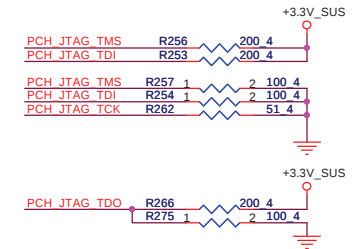
U27H



Cougar Point (HDA, JTAG, SATA)



PCH JTAG Debug (CLG)



Take care while using GPIO19 for Hot Plug function

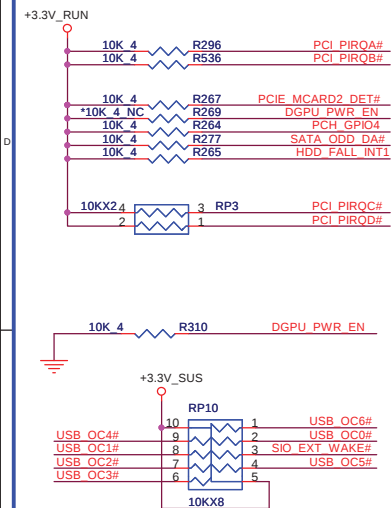
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN R478 *1K_4 NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R504 *1K_4 NC ACZ_SDOUT
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R548 330K_4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	(37) ACZ_SYNC_AUDIO R537 33_4 ACZ_SYNC_R

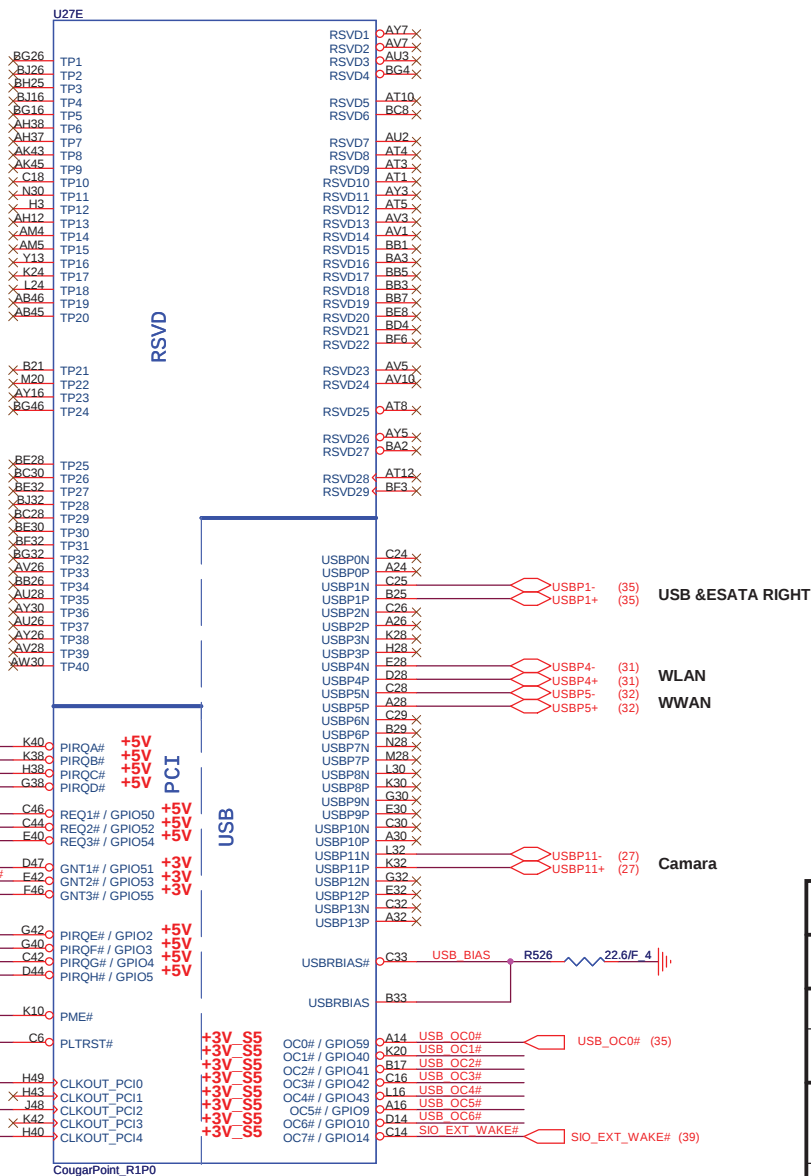


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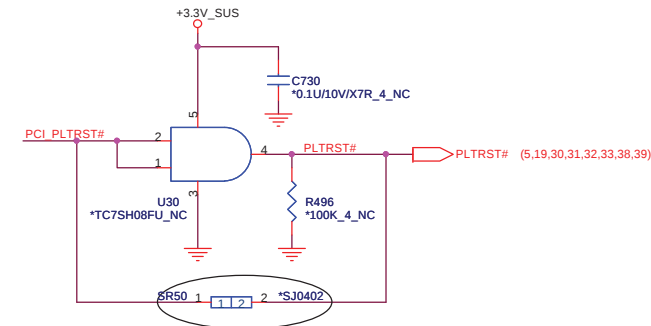
PCI/USBOC# Pull-up(CLG)

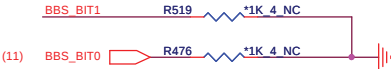


Cougar Point-M (PCI, USB, NVRAM)



PLTRST#(CLG)



Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
												
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>Bit 0</th><th>Bit 1</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										
												
Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]												



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U27B

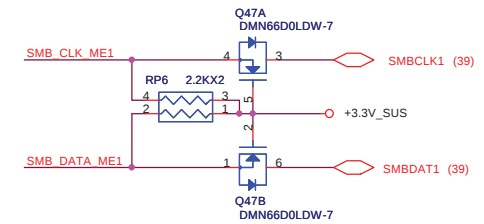


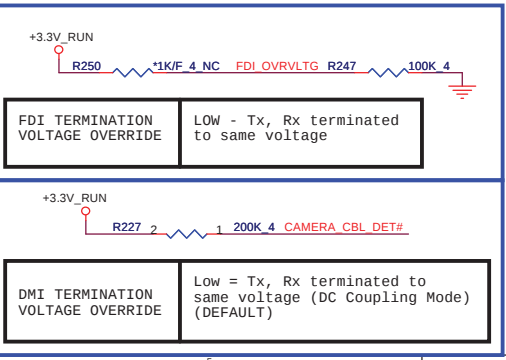
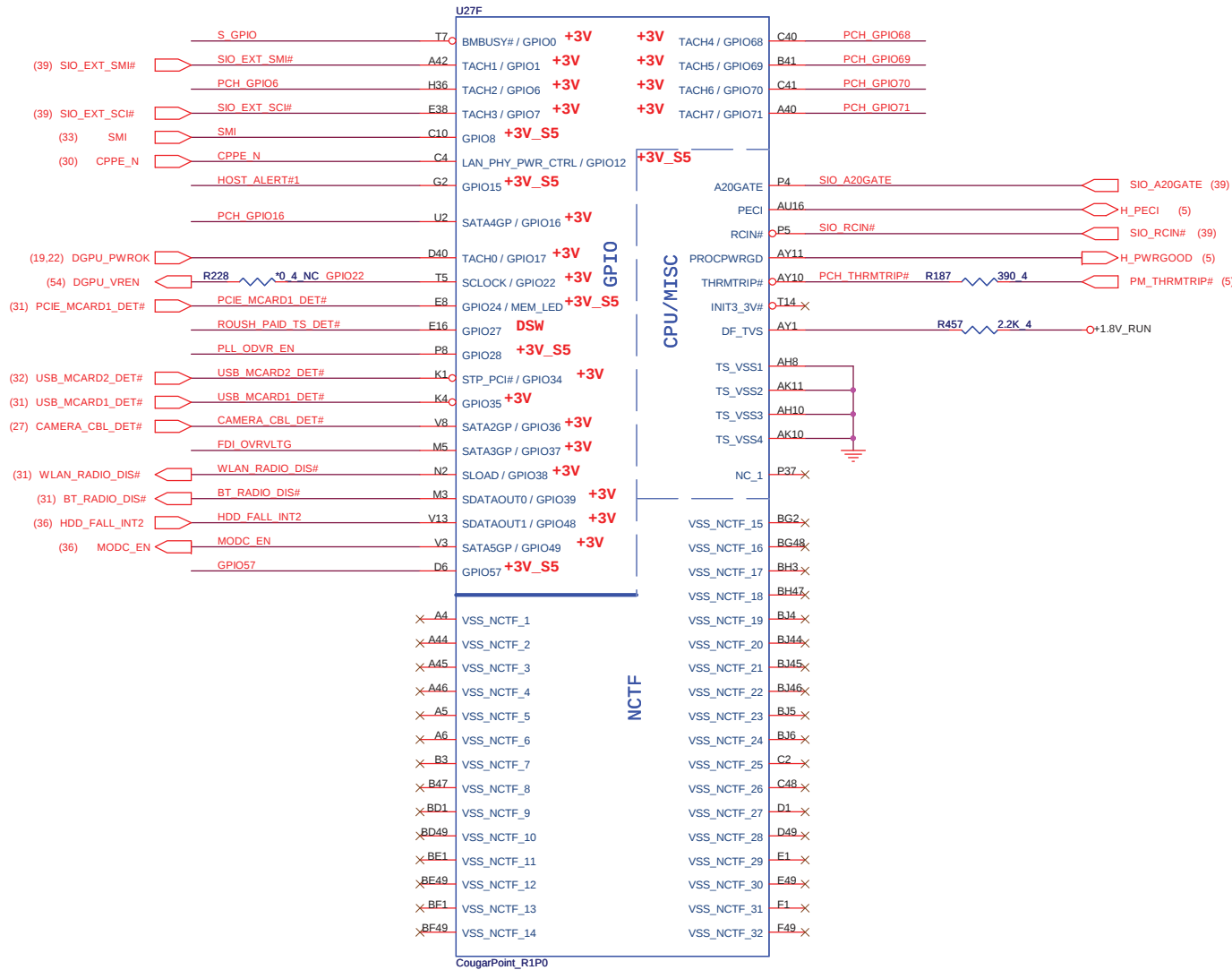
Figure 10: Pinmux connections for the i.MX8M Mini. The diagram shows various pinmux configurations for different functional blocks. Each configuration includes a pin name, a resistor value, a pull-up/pull-down value, and a pin number. The connections are as follows:

- PCIE CLK REQ0# (R489, 10K, 4) to +3.3V_SUS
- PCIE CLK REQ4# (R288, 10K, 4) to +3.3V_SUS
- PCIE CLK REQ5# (R276, 10K, 4) to +3.3V_SUS
- PEG B CLKREQ# (R284, 10K, 4) to +3.3V_SUS
- PCIE CLK REQ6# (R230, 10K, 4) to +3.3V_SUS
- PCIE CLK REQ7# (R286, 10K, 4) to +3.3V_SUS
- PCIE CLK REQ3# (R497, 10K, 4) to +3.3V_SUS
- PCIE CLK REQ1# (R483, 10K, 4) to +3.3V_RUN
- PCIE CLK REQ2# (R222, 10K, 4) to +3.3V_RUN
- PEG A CLKREQ# (R241, 10K, 4) to +3.3V_SUS
- PEG A CLKREQ# (R249, 10K, 4 NC) to +3.3V_SUS
- PCH GPIO14 (R297, 10K, 4) to +3.3V_SUS
- PCH SMB_ALERT# (R287, 10K, 4) to +3.3V_SUS
- SMBCLK (R309, 2.2K, 4) to +3.3V_SUS
- SMBDATA (R308, 2.2K, 4) to +3.3V_SUS
- SMLDCLK (R278, 2.2K, 4) to +3.3V_SUS
- SMLDADATA (R289, 2.2K, 4) to +3.3V_SUS



Cougar Point (GPIO, VSS_NCTF, RSVD)

GPIO Pull-up/Pull-down(CLG)



Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite	RSMRST#	0 = Disable (Default) 1 = Enable

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Cougar Point 6/7

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Rev 3A

COUGAR POINT (POWER)

VccADAC = 1mA(8mils)

VccCORE = 1.14A(50mils)

need 1206?

VccIO = 2.925 A(120mils)

VccVRM(1.5V) = 0.16 A(10mils)

VccDMI = 0.042 A(10mils)

VccVRM(1.5V) = 0.16 A(10mils)

VccDMI = 0.042 A(10mils)

VccDMI = 0.042 A(10mils)

VccDMI = 0.042 A(10mils)

VccDMI = 0.042 A(10mils)

VccDMI = 0.042 A(10mils)

VccDMI = 0.042 A(10mils)

VccDMI = 0.042 A(10mils)

VccDMI = 0.042 A(10mils)

POWER

VCC CORE

LVDS

HVCMOS

DMI

VCCIO

DFT / SPI

FDI

CougarPoint_R1P0

CougarPoint_R1P0

CougarPoint_R1P0

CougarPoint_R1P0

CougarPoint_R1P0

CougarPoint_R1P0

CougarPoint_R1P0

Cougar Point (POWER)

POWER

VCC CORE

LVDS

HVCMOS

DMI

VCCIO

DFT / SPI

FDI

USB

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

RTD

RTD

RTD

RTD

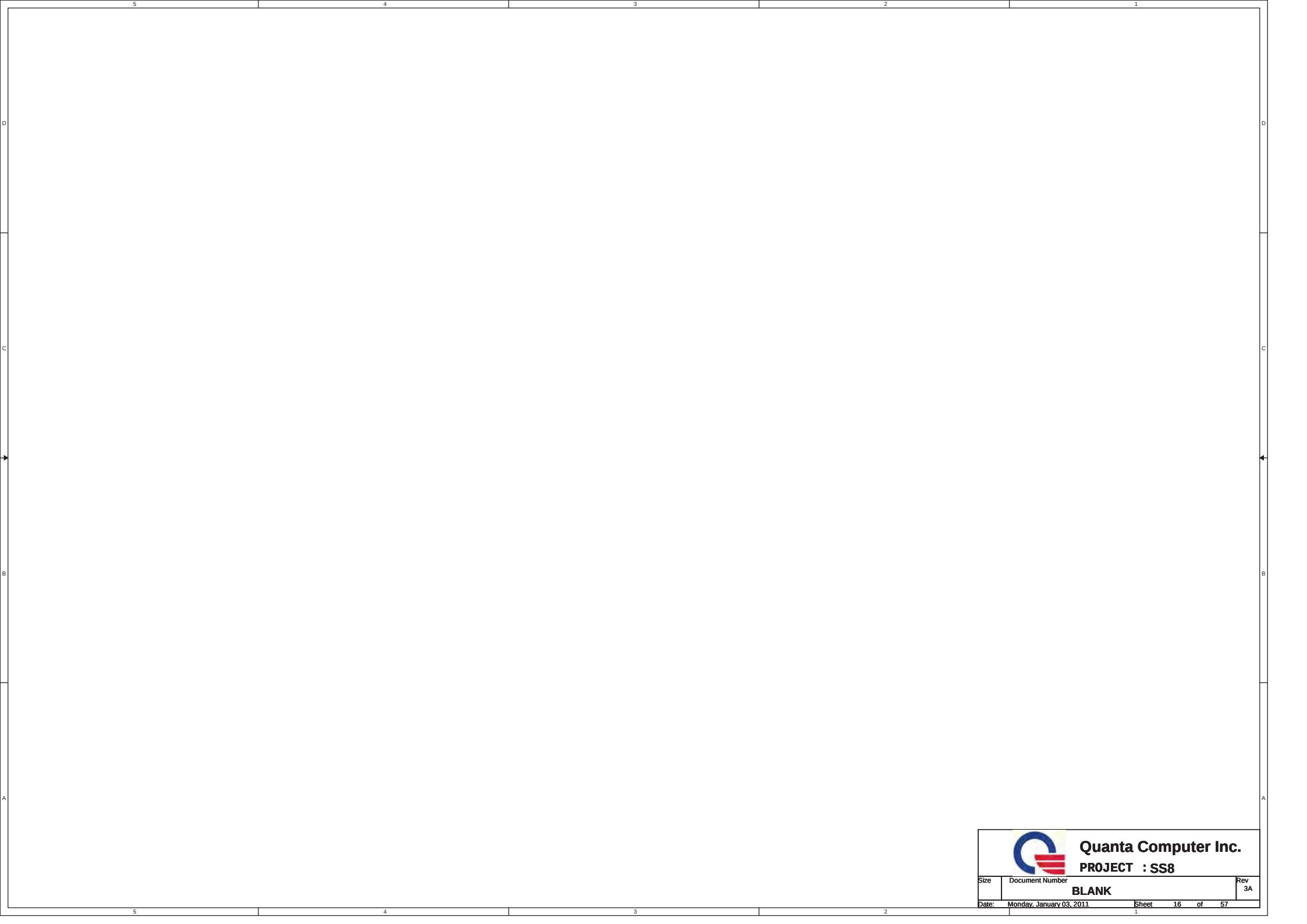
RTD

RTD

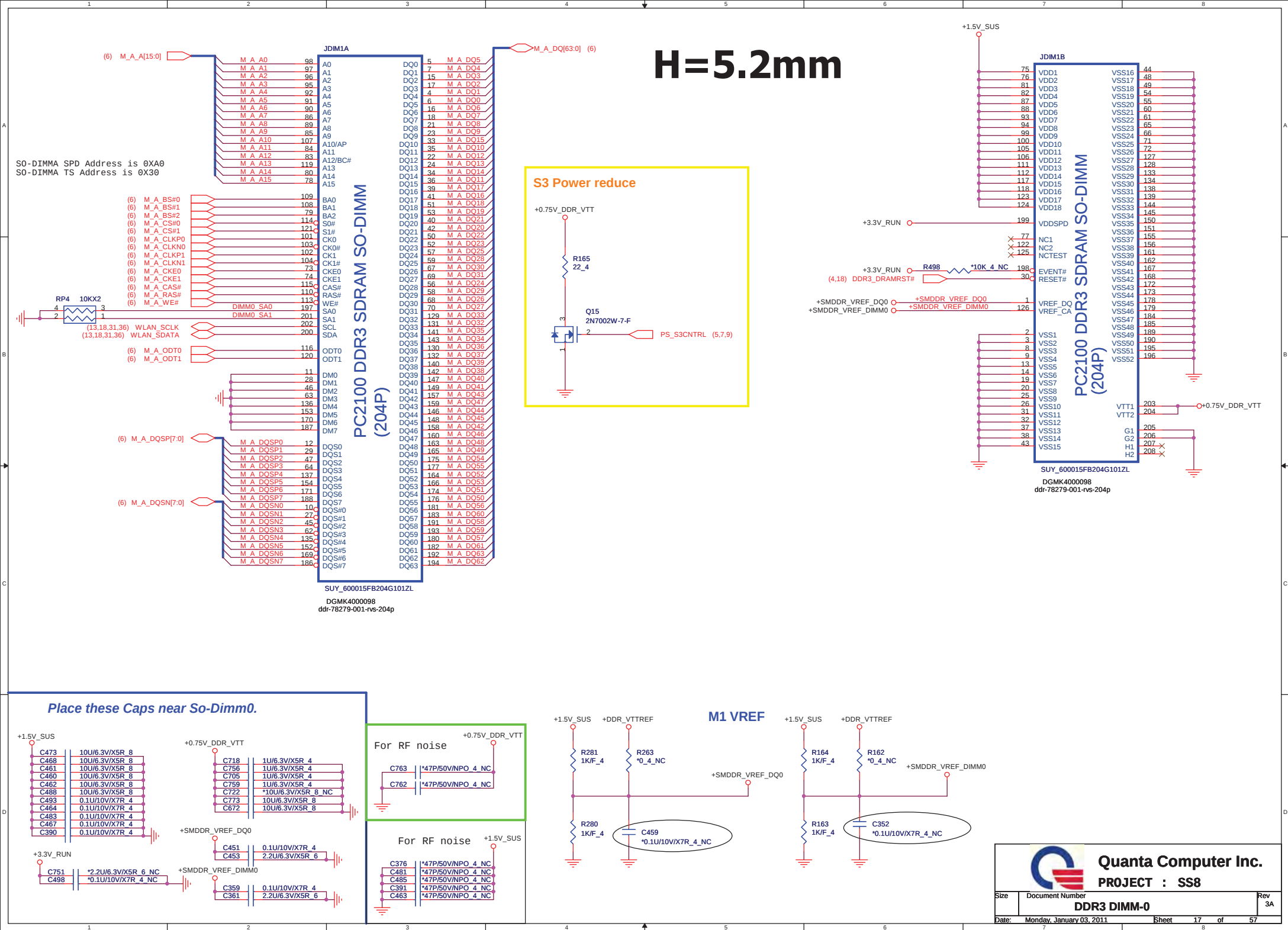
RTD

RTD

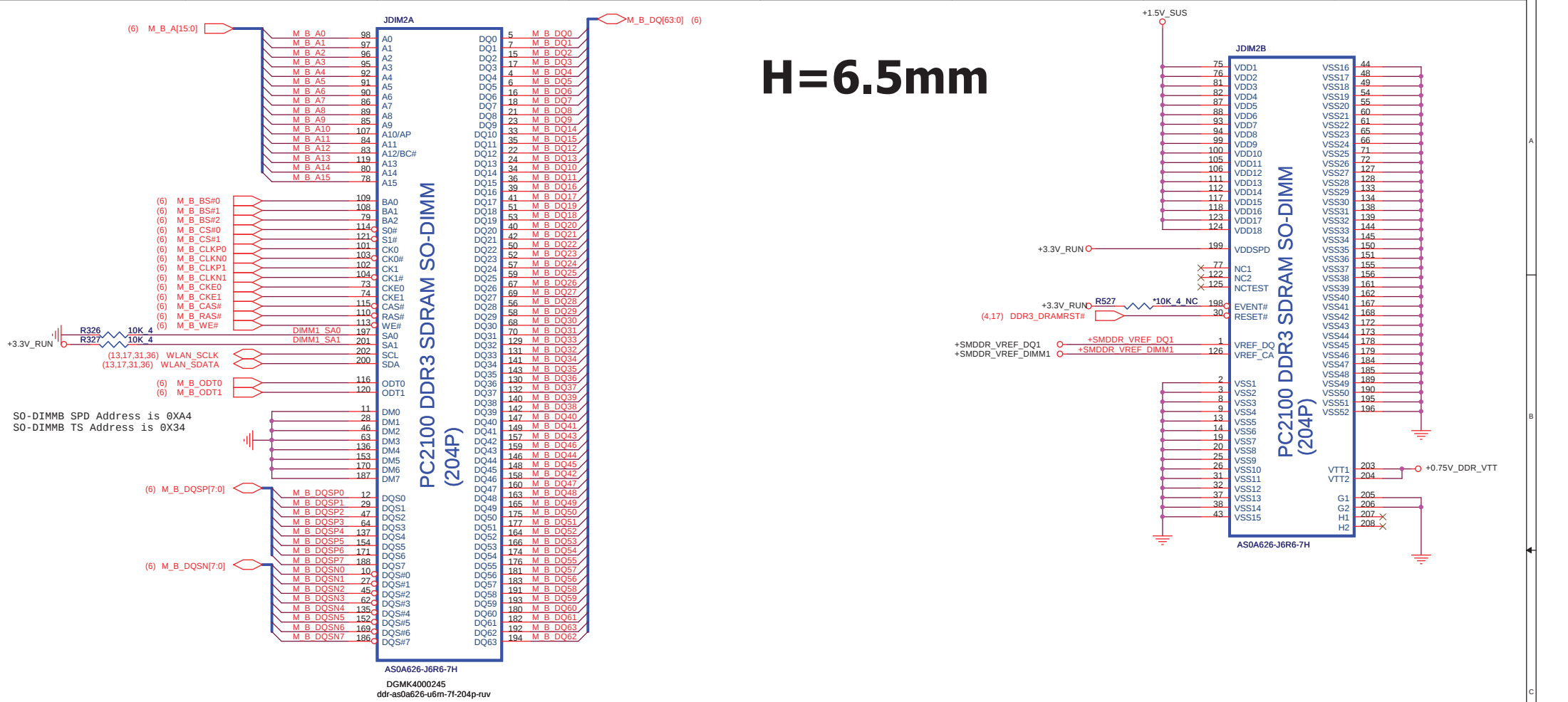
RTD



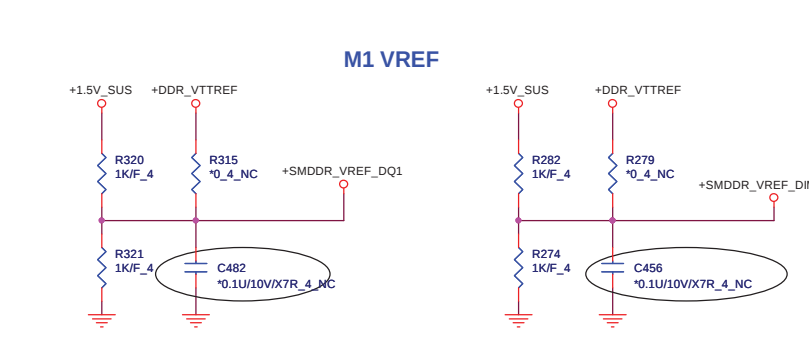
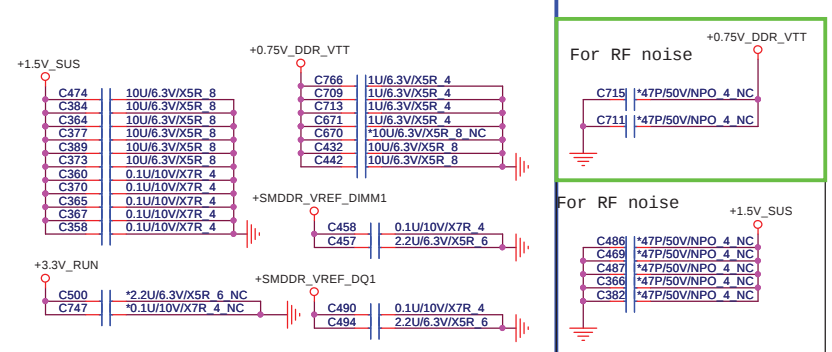
		Quanta Computer Inc.	
		PROJECT : SS8	
Size	Document Number		Rev
	BLANK		3A
Date:	Monday, January 03, 2011		Sheet 16 of 57



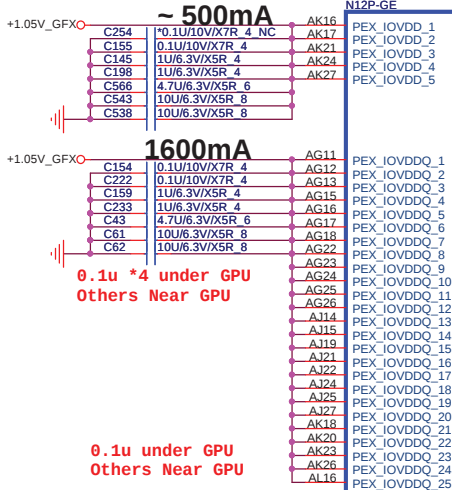
H=6.5mm



Place these Caps near So-Dimm1.

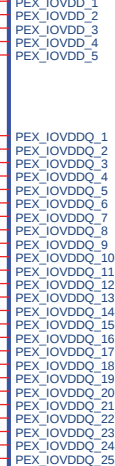


PEX_IOVDD+PEX_IOVDDQ >2.2A

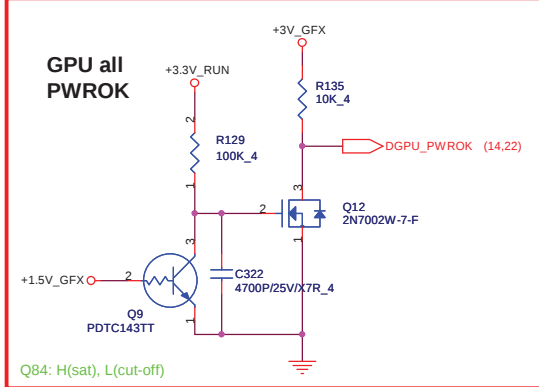
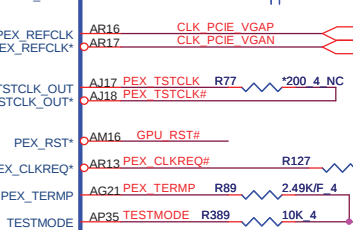
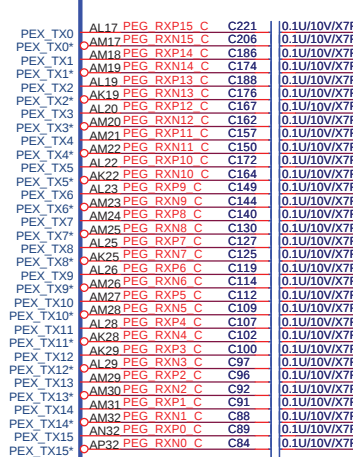
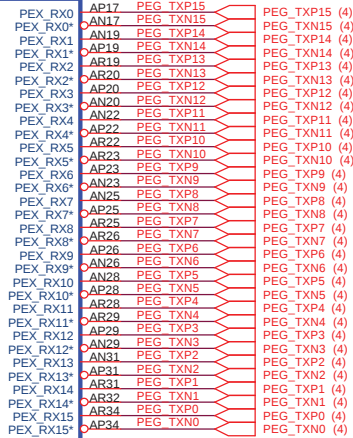
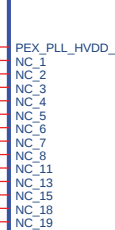
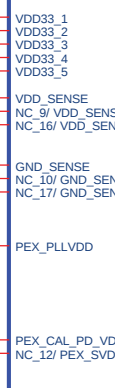


U22A

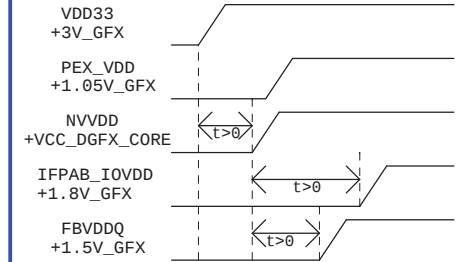
N12P-GE



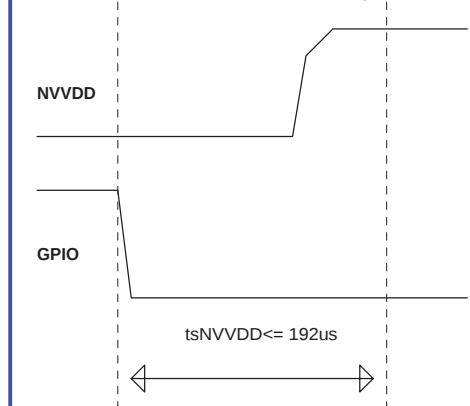
PCI EXPRESS



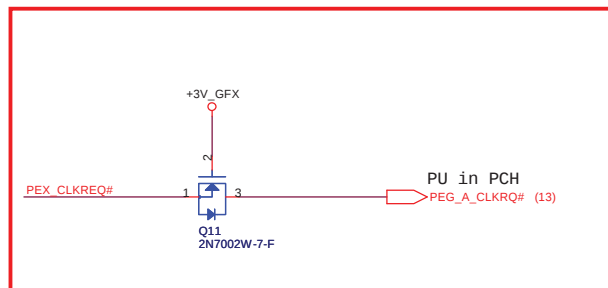
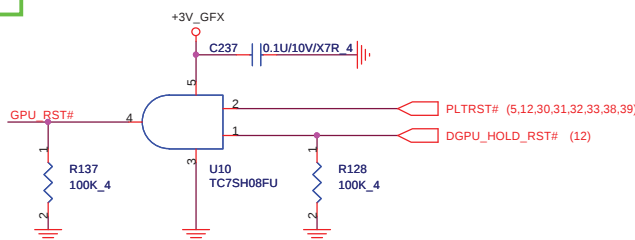
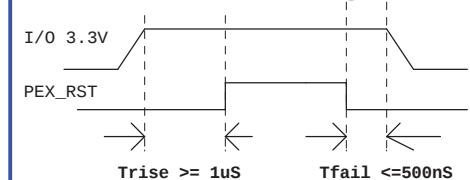
Power up sequence



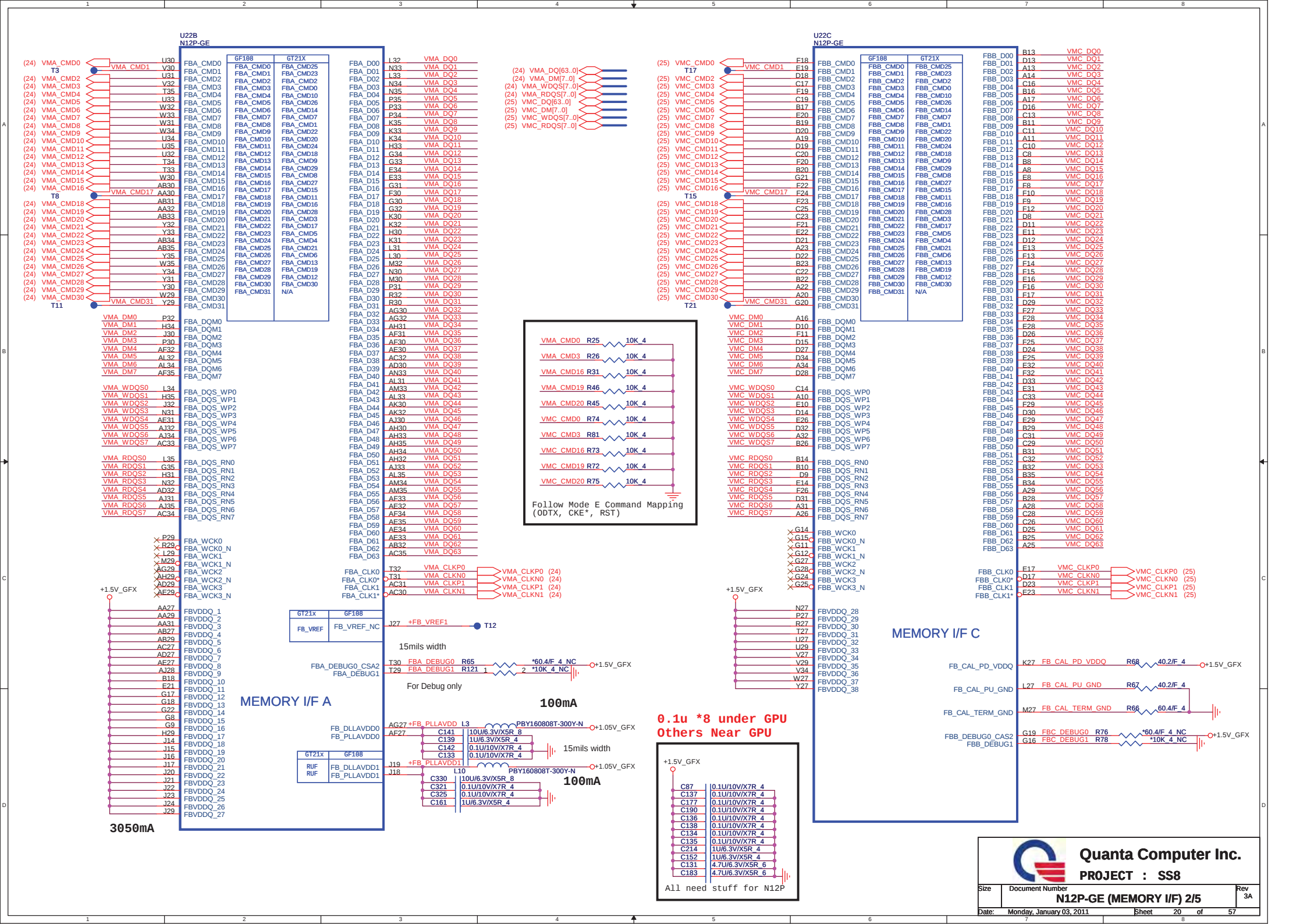
NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time

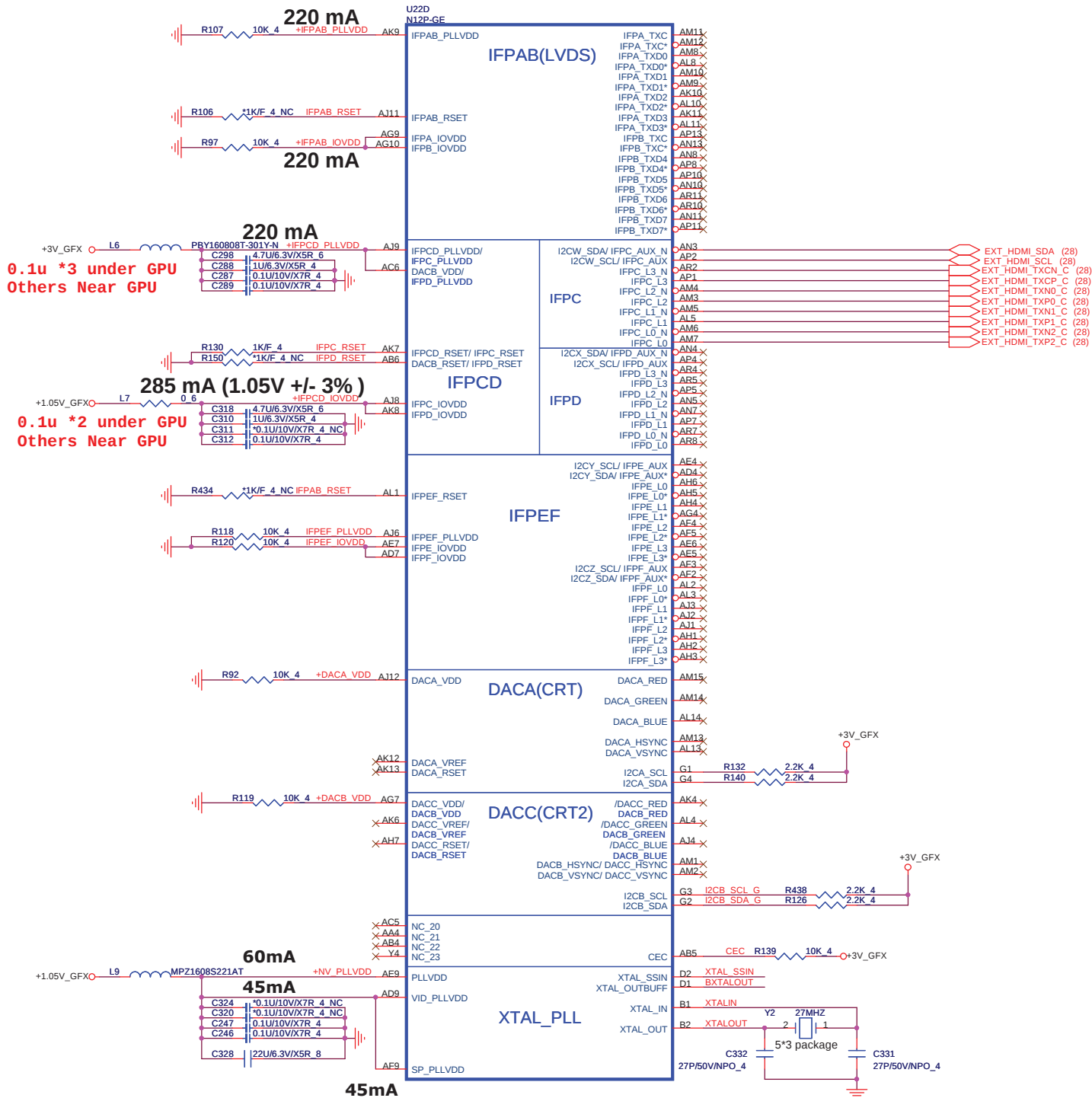


PEX_RST timing



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N12P-GE
(MIOB NC)

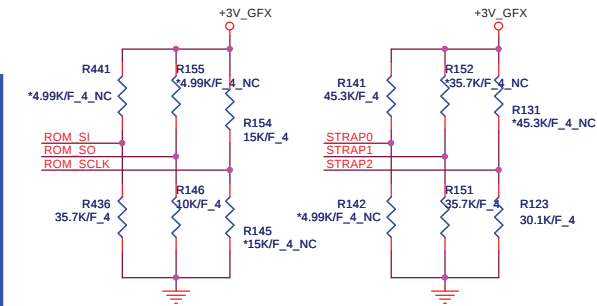
NC R96

CHIP	PCI_DEVID:	STRAP2	ROM_SCLK
N12P-GE	0xDF5	0101 PD 30K	1010 PU 15K

Default: N12P-GE

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1% (0402)]
15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F 4: CS32002FB29 [RES CHIP 20K 1/16W +1% (0402)]

30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1% (0402)]
35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1% (0402)]
45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0101
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

Default: Hynix VRAM 2G (0110)

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Quanta P/N	Vendor P/N	ROM_SI
0000	Reserved	Reserved			PD 5K
0001	DDR3 64Mx16, 900MHz	Hynix	AKD5LZWTW02	H5TQ1G63DFR-11C	PD 10K
0010	DDR3 64Mx16, 900MHz	Hynix	AKD5LGTW500	K4W1G1646E-HC11	PD 15K
0011	DDR3 128Mx16, 900MHz	Samsung	AKD5MGWTTW00	H5TQ2G63BFR-11C	PD 20K
0110	DDR3 128Mx16, 900MHz	Hynix	AKD5MGWTTW00	K4W2G1646C-HC11	PD 35K
0111	Reserved	Reserved			PD 45K

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVD VID0
6	OUT	N/A	NVVD VID1
7	OUT	N/A	NVVD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

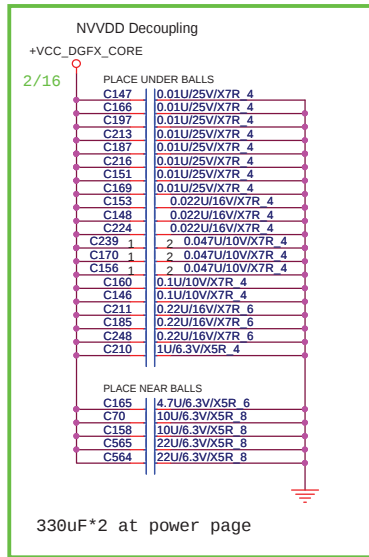
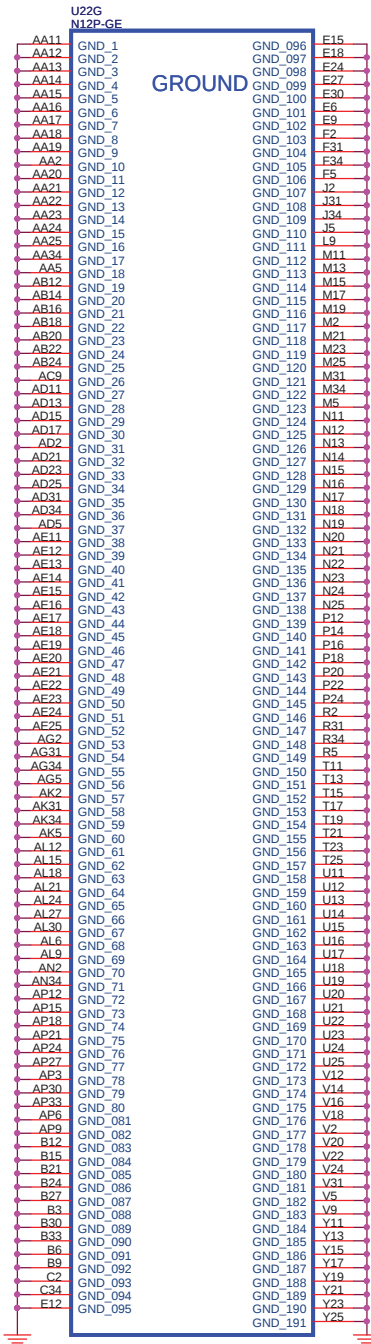
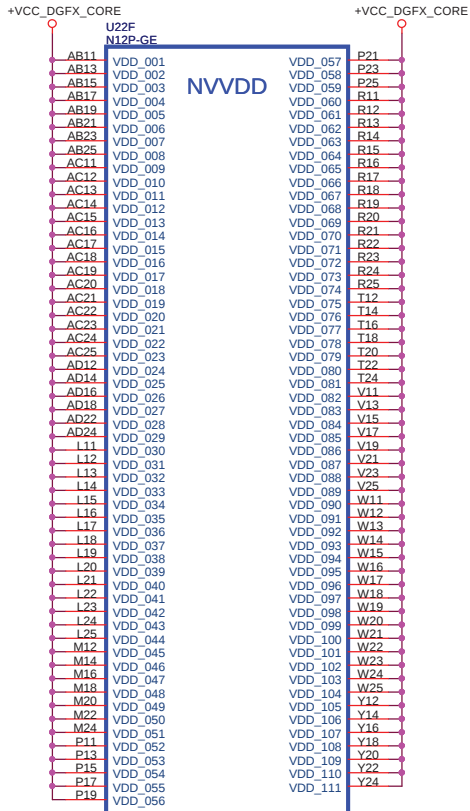


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(12,28) EXT_HDMI_HPD_Q

(14,19) DGPU_PWROK



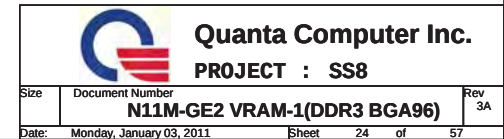


(20) VMA_DQ[63..0]

(20) VMA_DM[7..0]

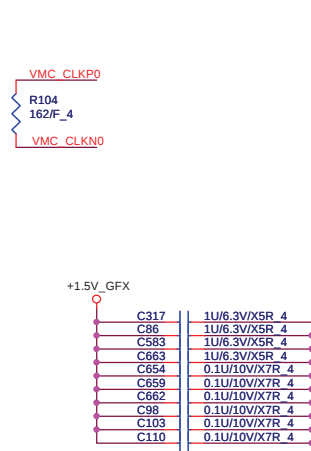
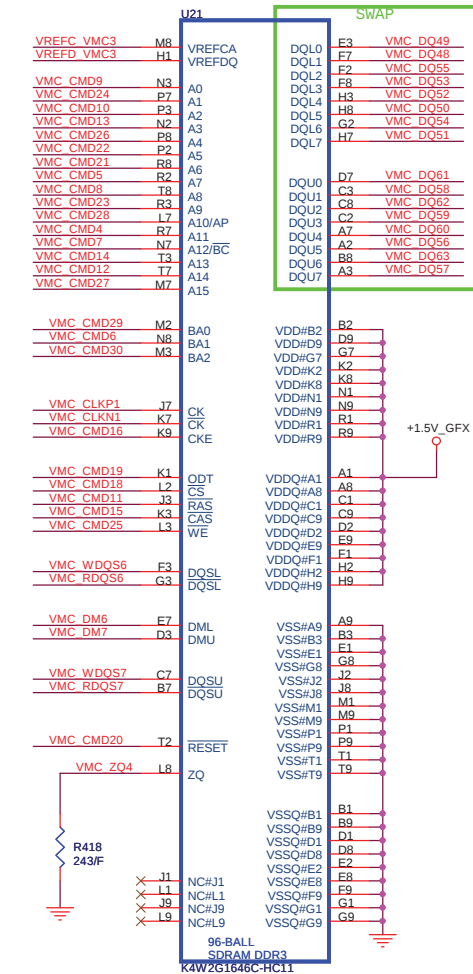
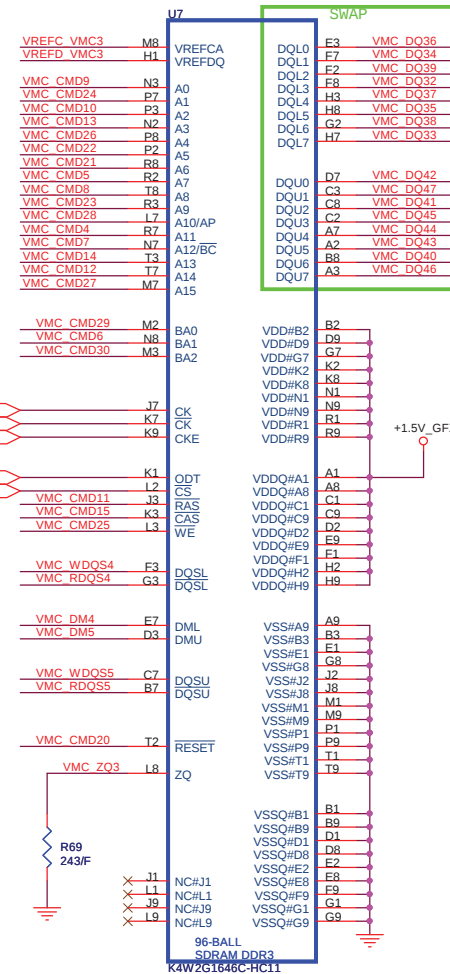
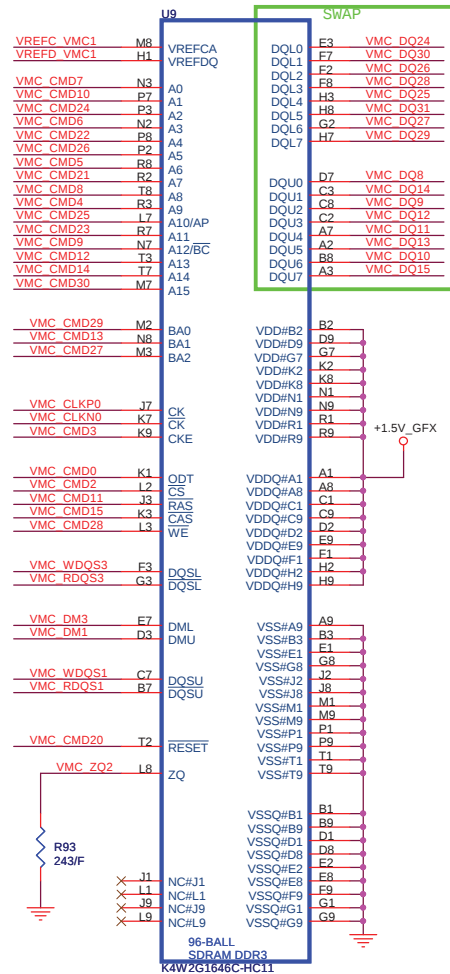
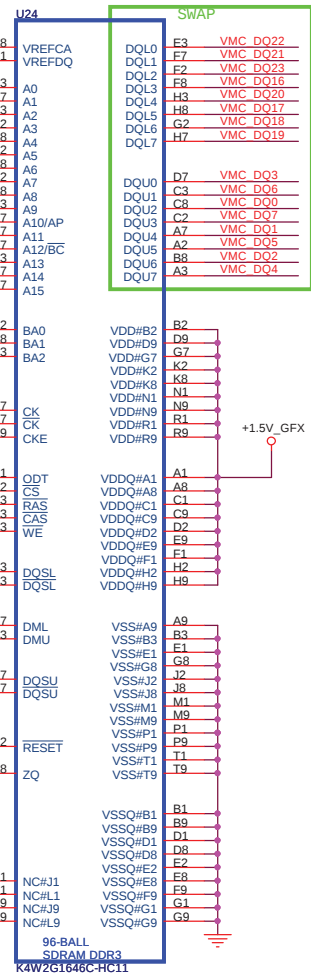
(20) VMA_WDQS[7..0]

(20) VMA_RDQS[7..0]

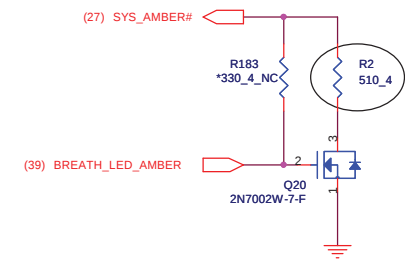
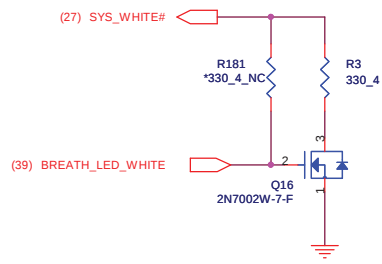
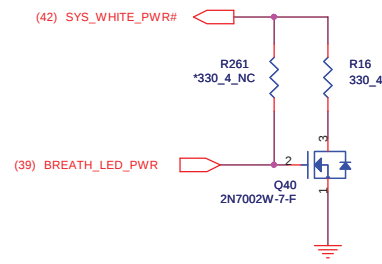
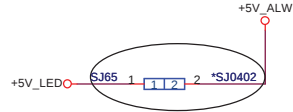
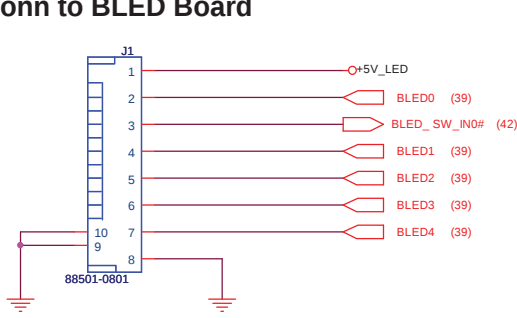


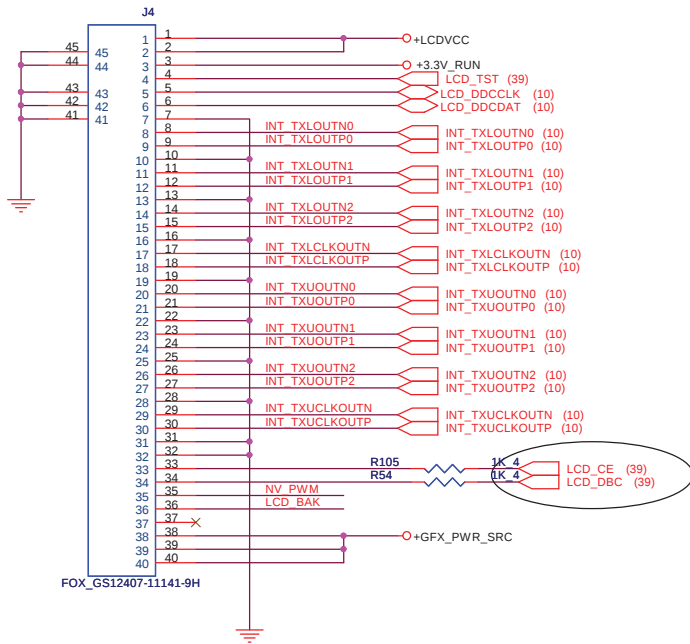
(20) VMC_DQ[63..0]
(20) VMC_DM[7..0]
(20) VMC_WDQS[7..0]
(20) VMC_RDQS[7..0]

CHANNEL B: 512MB/1024MB DDR3



Conn to BLED Board

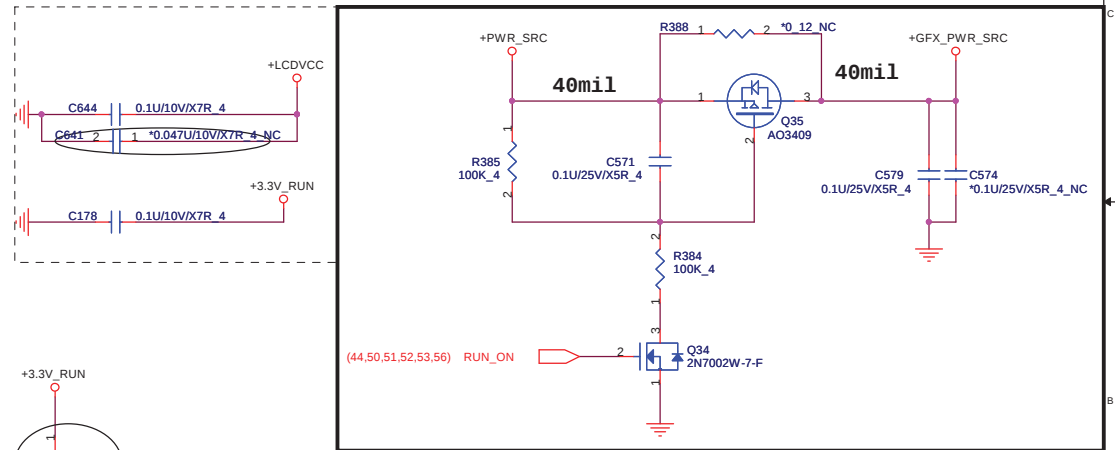
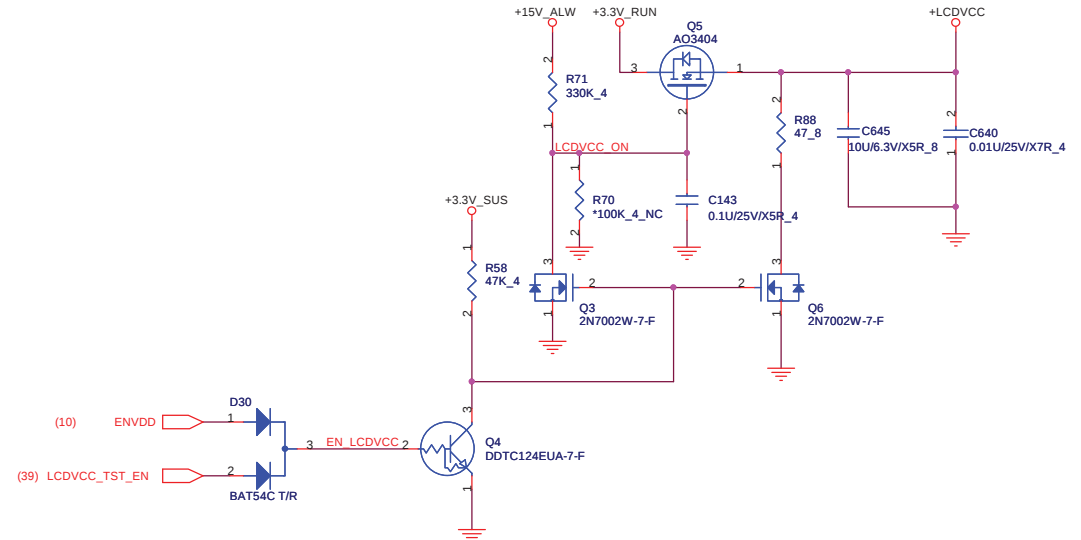
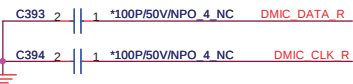
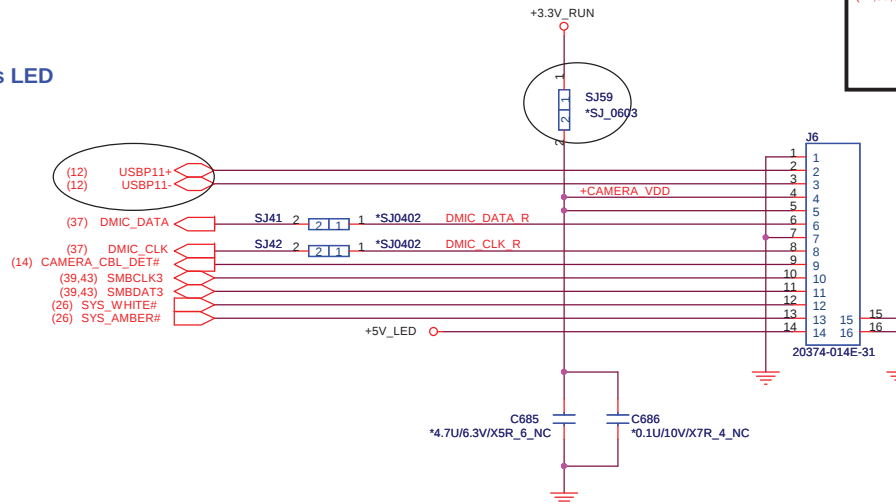
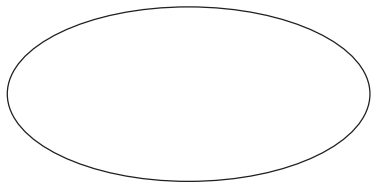




EMC Reserve

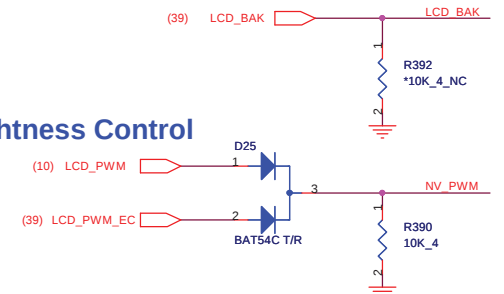
INT_TXCLKOUTN	R411	1	2	*100_4 NC	INT_TXCLKOUTP
INT_TXLOUTN2	R412	1	2	*100_4 NC	INT_TXLOUTP2
INT_TXLOUTN1	R416	1	2	*100_4 NC	INT_TXLOUTP1
INT_TXLOUTN0	R419	1	2	*100_4 NC	INT_TXLOUTP0
INT_TXUCLKOUTN	R400	1	2	*100_4 NC	INT_TXUCLKOUTP
INT_TXUOUTN2	R407	1	2	*100_4 NC	INT_TXUOUTP2
INT_TXUOUTN1	R408	1	2	*100_4 NC	INT_TXUOUTP1
INT_TXUOUTN0	R410	1	2	*100_4 NC	INT_TXUOUTP0

Array Microphone & Camera & System Status LED



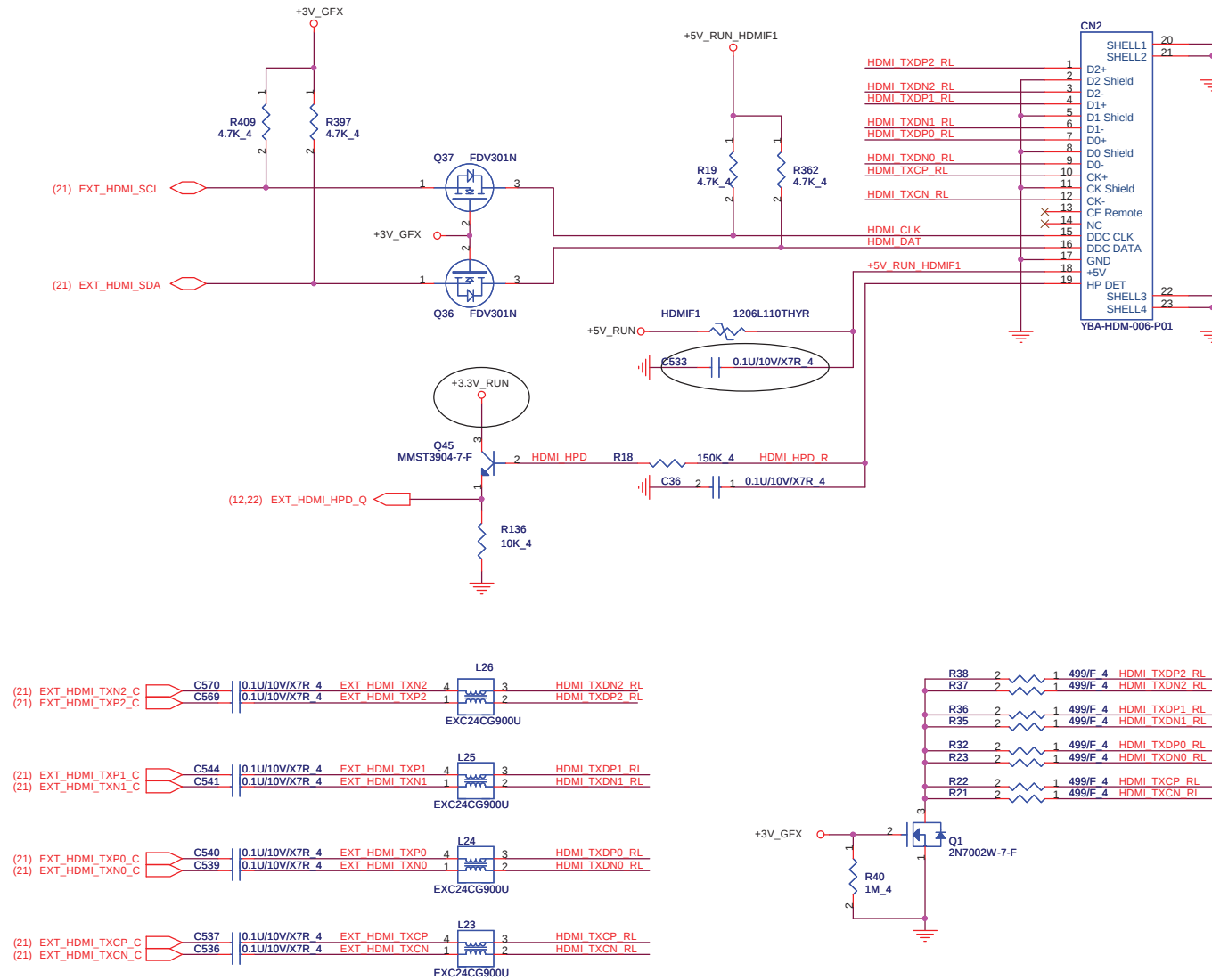
Backlight Enable

Brightness Control



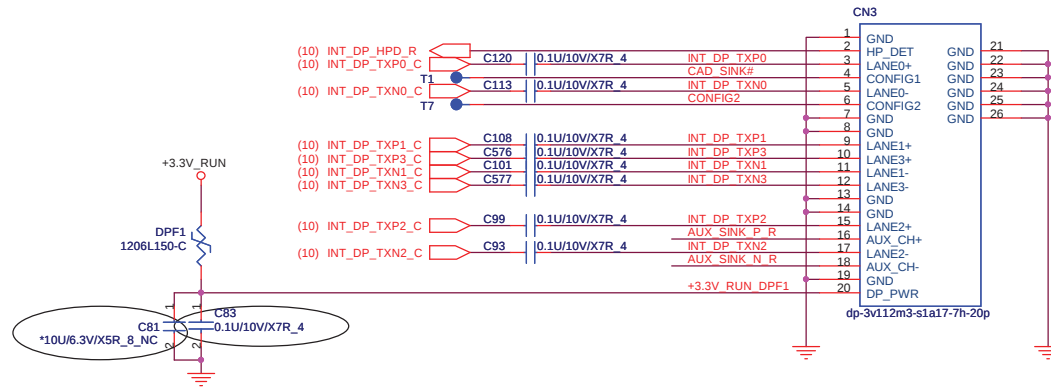
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HDMI

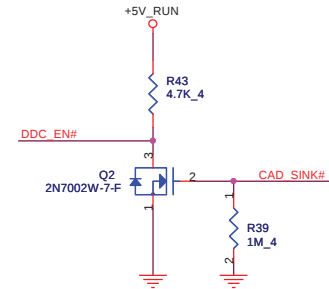
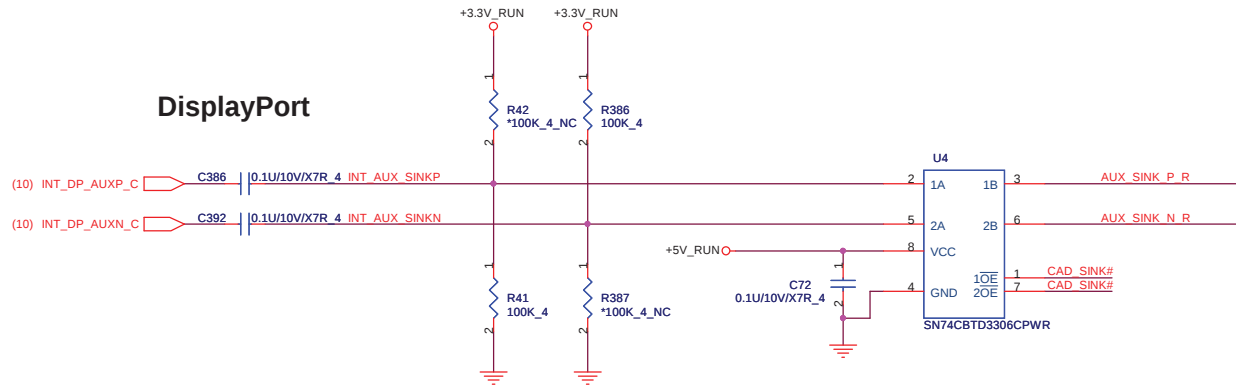


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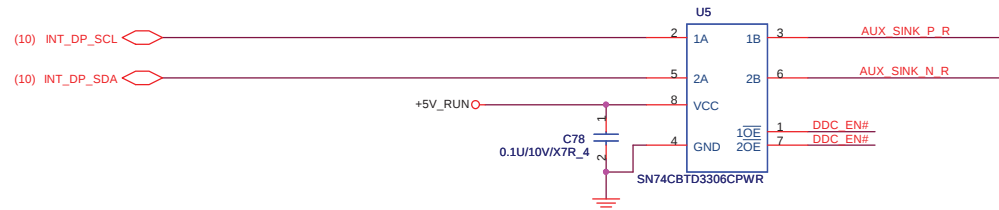
MINI DISPLAY PORT CONNECTOR



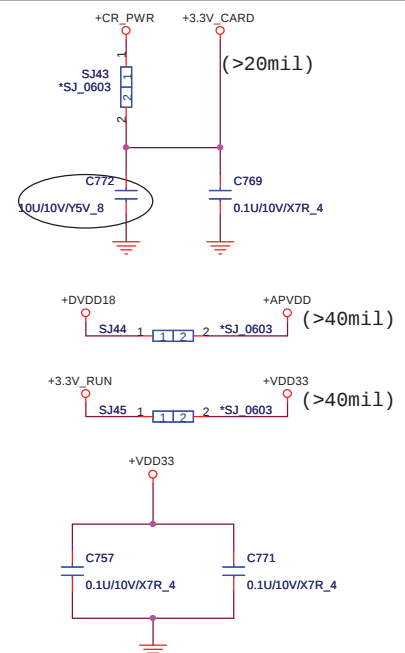
DisplayPort



HDMI



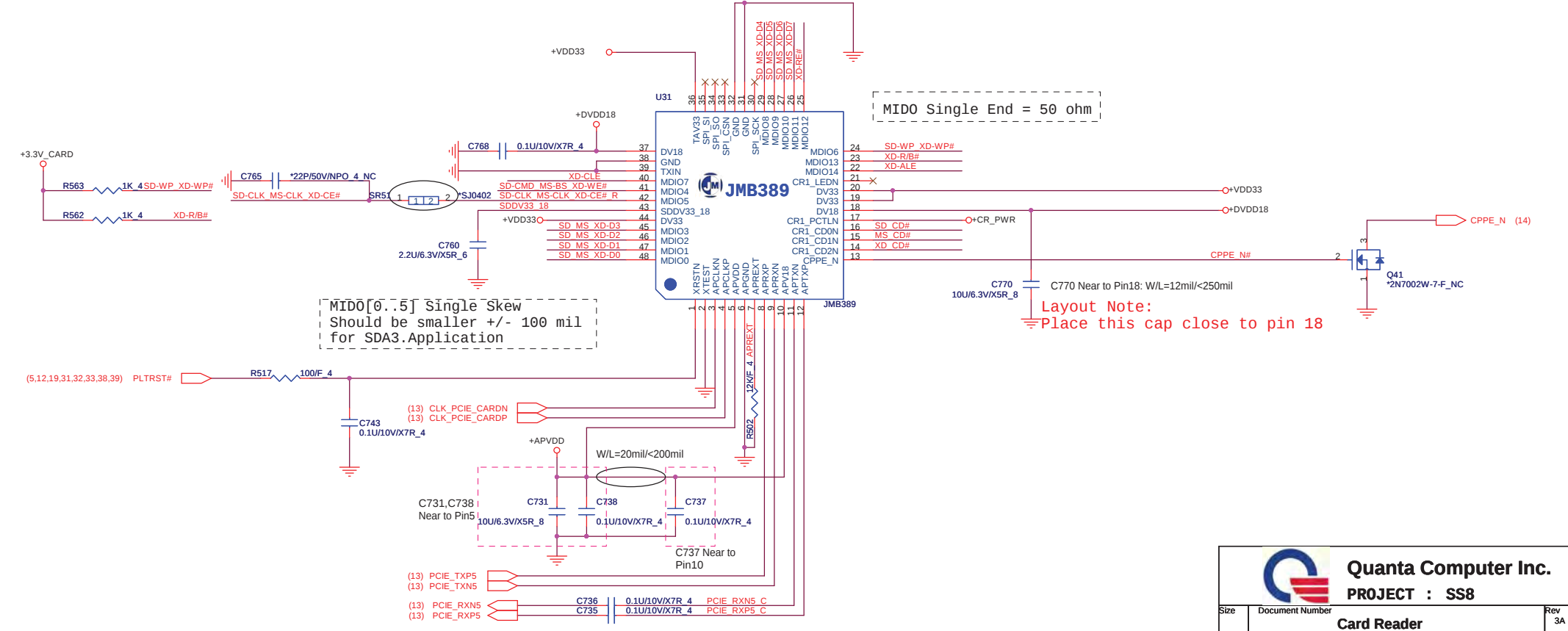
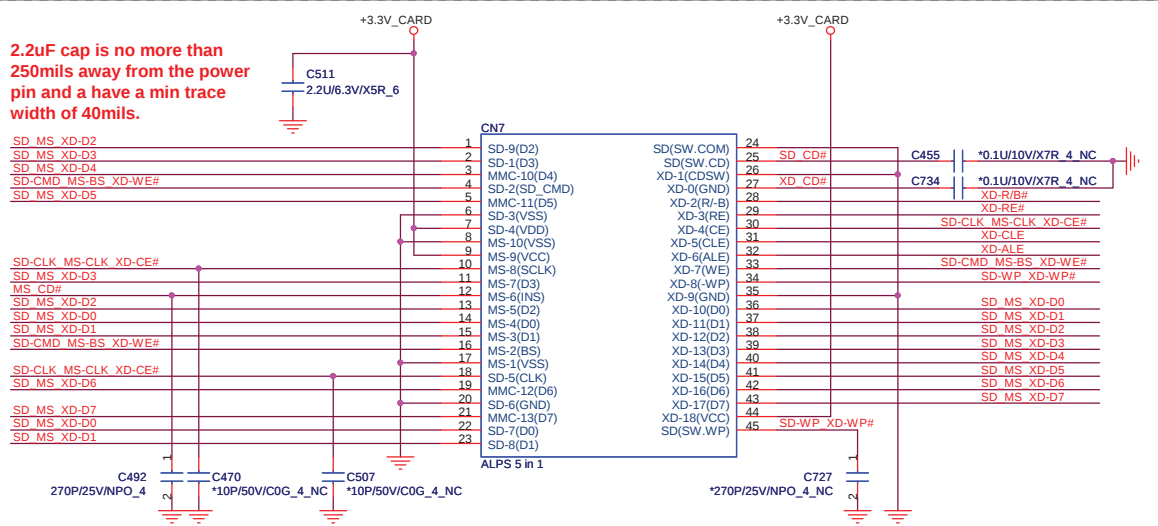
Quanta Computer Inc.
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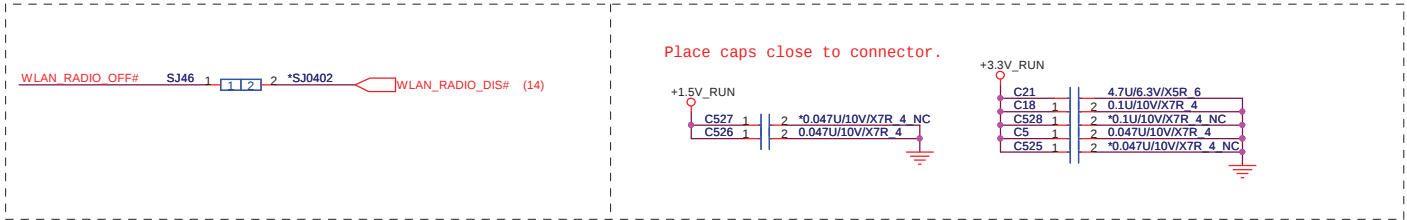


Card Reader interface signal mapping

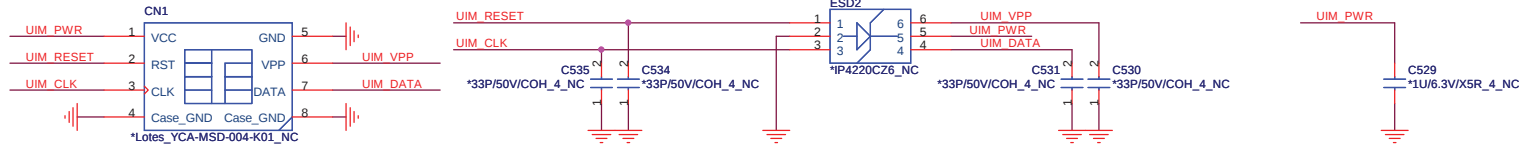
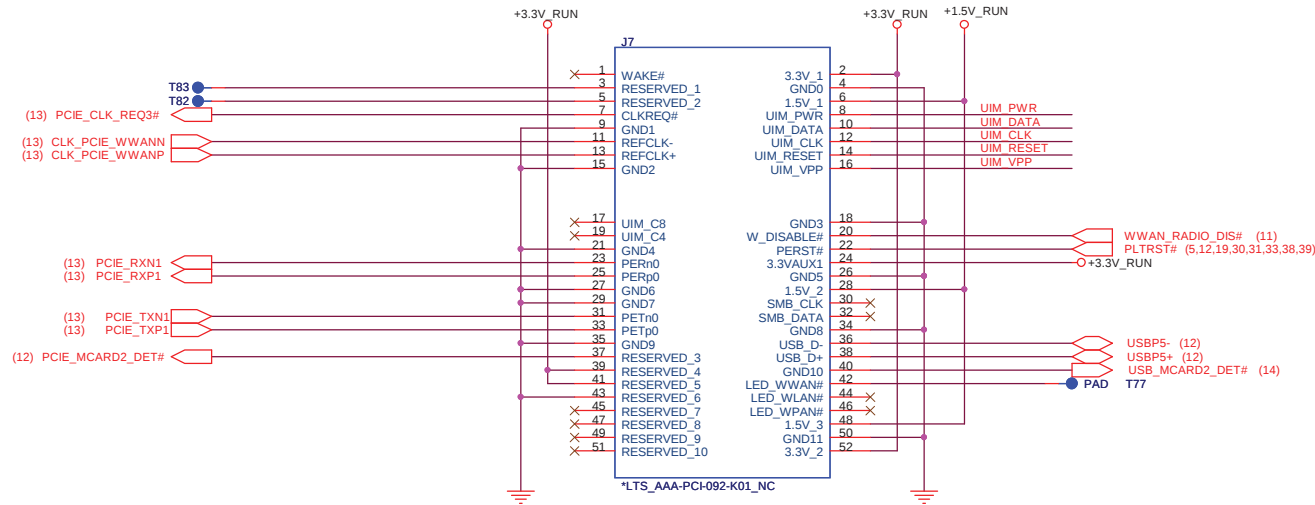
PIN	Default	SD / MMC	MS	XD
MDI008	SD/MMC/MS/XD	SD_D0	MS_D0	XD_D0
MDI001		SD_D1	MS_D1	XD_D1
MDI002		SD_D2	MS_D2	XD_D2
MDI003		SD_D3	MS_D3	XD_D3
MDI004		SD_CMD	MS_BS	XD_WE#
MDI005		SD_CLK	MS_CLK	XD_CE#
MDI006		SD_WP		XD_WP#
MDI007				XD_CLE
MDI008		MMC_D4	MS_D4	XD_D4
MDI009		MMC_D5	MS_D5	XD_D5
MDI010		MMC_D6	MS_D6	XD_D6
MDI011		MMC_D7	MS_D7	XD_D7
MDI012				XD_RE#
MDI013				XD_R/B#
MDI014				XD_ALE
CR1_LEDN		SD_LED#	MS_LED#	XD_LED#
CR1_PCTLN		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		
CR1_CD1			MS_CD#	
CR1_CD2				XD_CD#

2.2uF cap is no more than 250mils away from the power pin and a have a min trace width of 40mils.



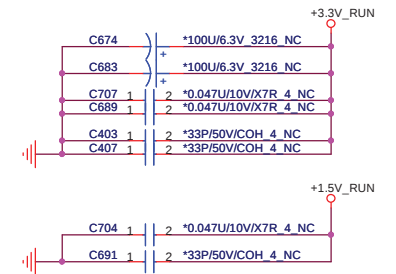


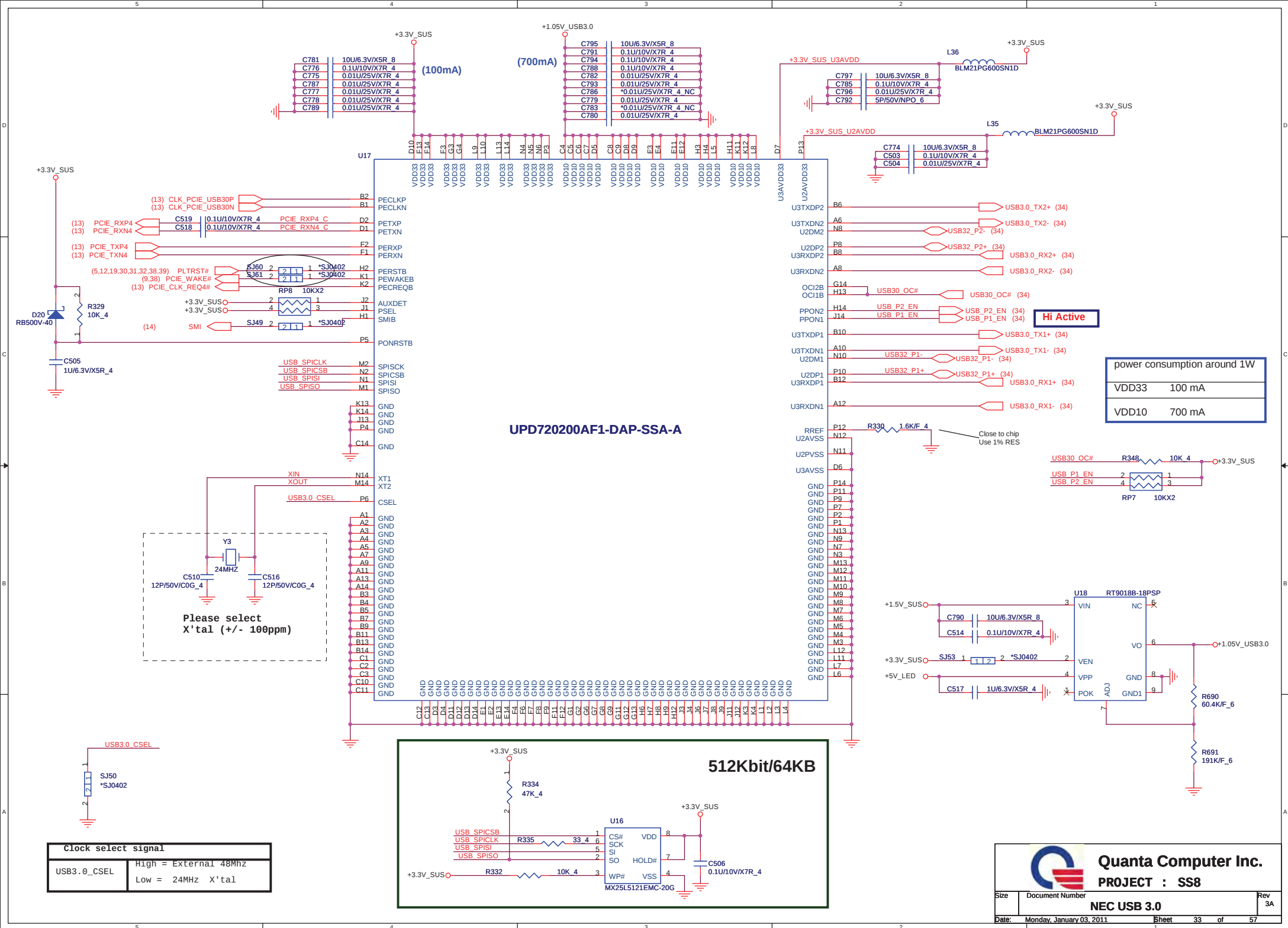
MiniCard WWAN connector

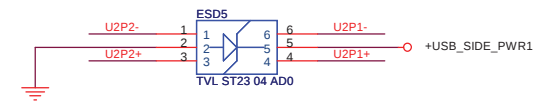
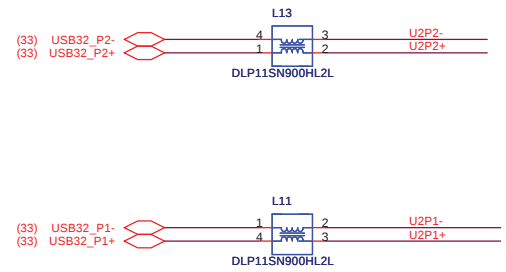
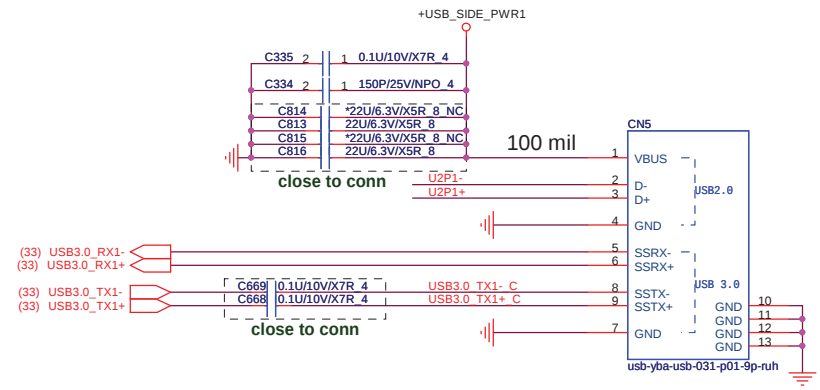
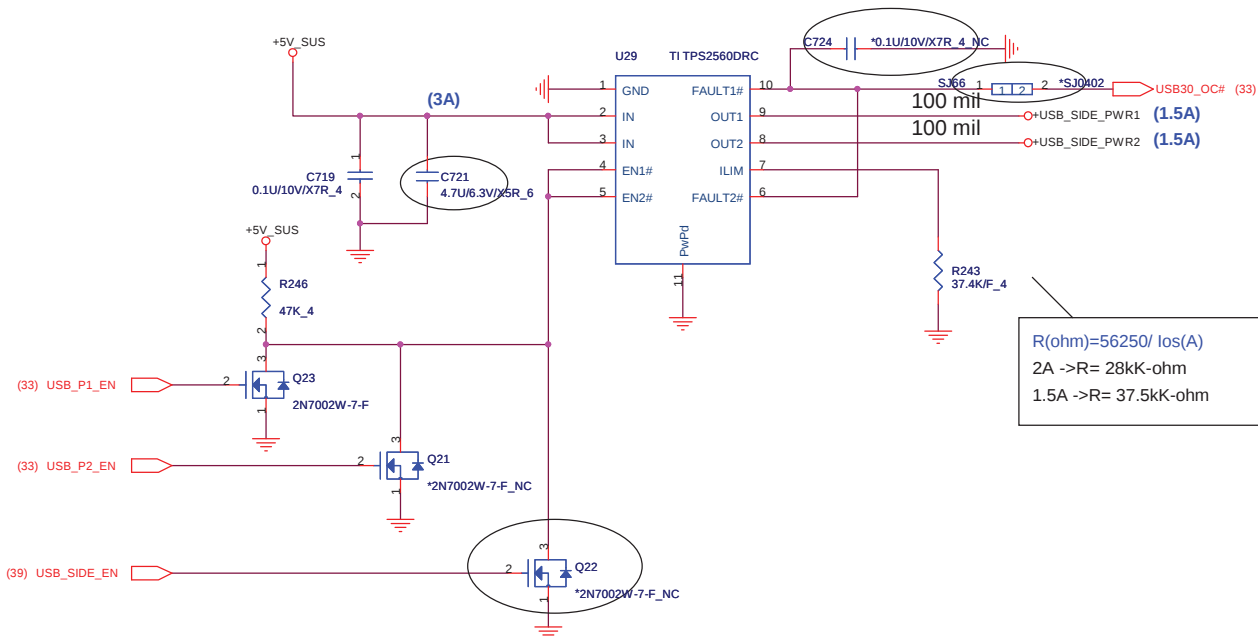


Place as close as possible to JSIM1 connector

Place caps close to connector.





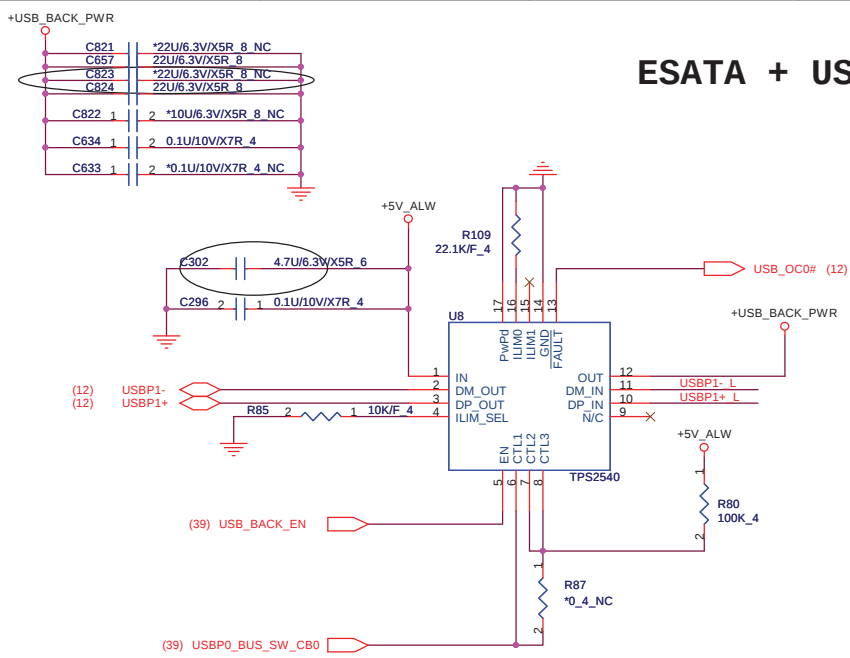


Copy from XM2

U12 IP4284CZ10-TB			
USB3.0 TX1+ C	1-	NC	10 USB3.0 TX1+ C
USB3.0 TX1- C	2	1+	9 USB3.0 TX1- C
	3	GND	8
USB3.0 RX1+	4	2-	7 USB3.0 RX1+
USB3.0 RX1-	5	2+	6 USB3.0 RX1-

U14 IP4284CZ10-TB			
USB3.0 TX2+ C	1-	NC	10 USB3.0 TX2+ C
USB3.0 TX2- C	2	1+	9 USB3.0 TX2- C
	3	GND	8
USB3.0 RX2+	4	2-	7 USB3.0 RX2+
USB3.0 RX2-	5	2+	6 USB3.0 RX2-

ESATA + USB Conn + Power share

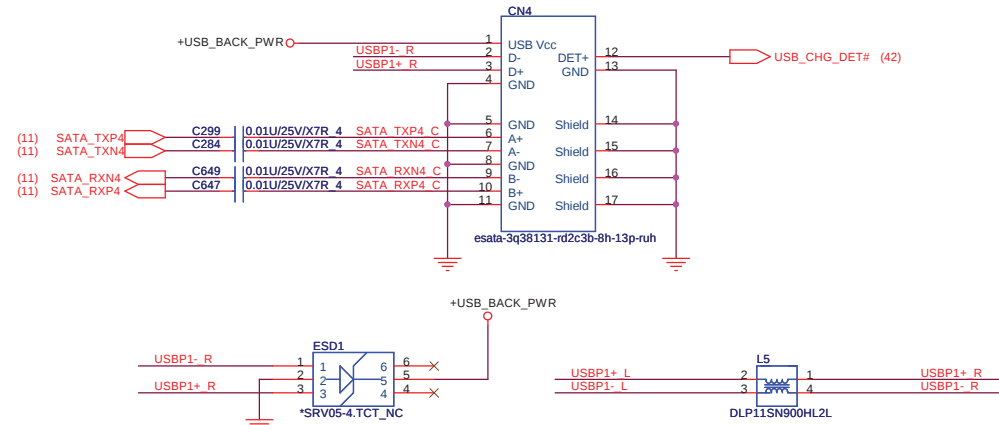


ES(PG1.0): Stuff R87, Un-Stuff R80
MP(PG1.1): Un-Stuff R87, Stuff R80

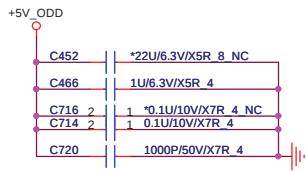
USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

	R109	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

E-SATA Conn

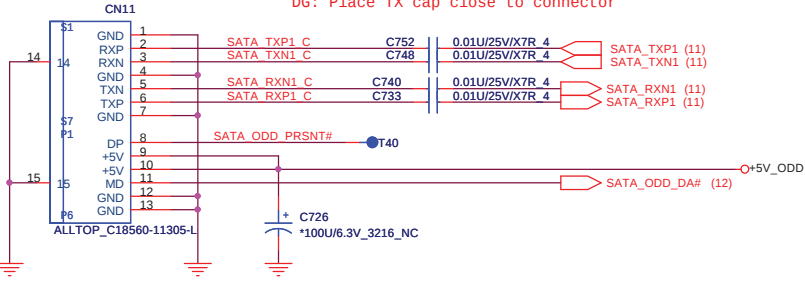


Place caps close to CN11.

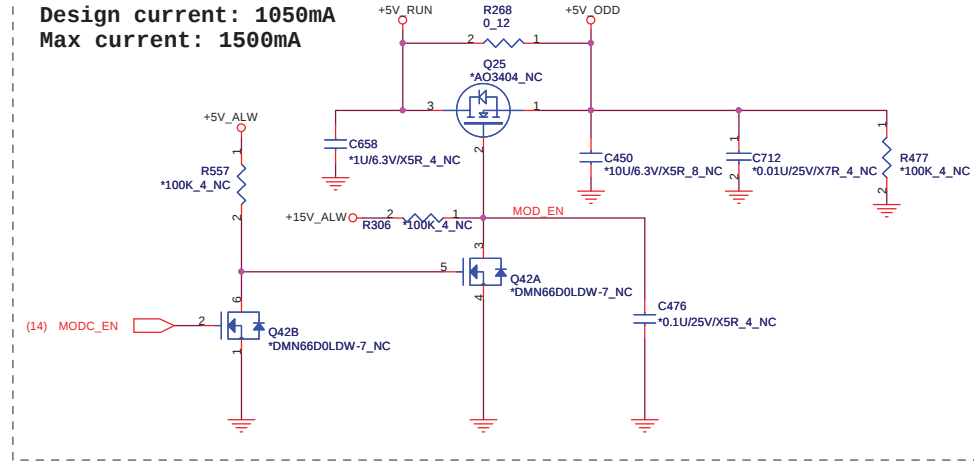


ODD Connector

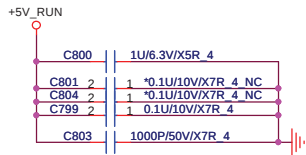
DG: Place TX cap close to connector



Design current: 1050mA
Max current: 1500mA

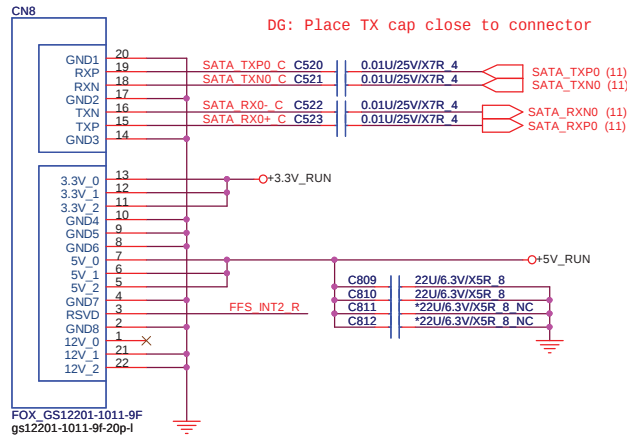


Place caps close to CN8.

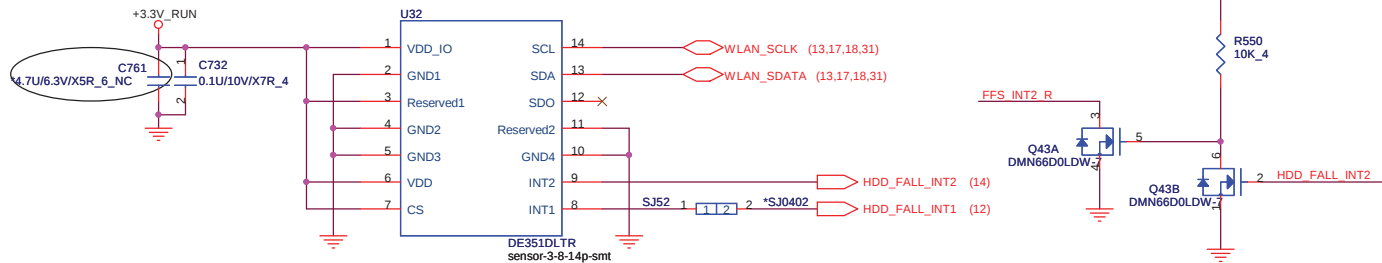


SATA Connector.

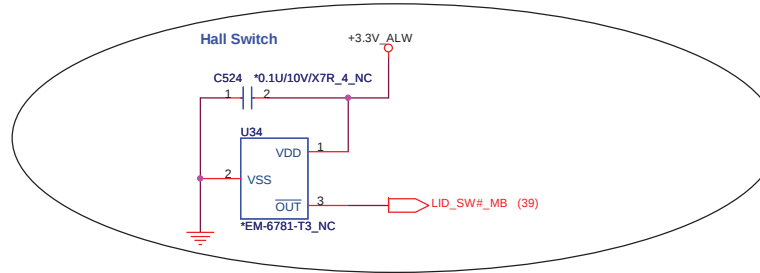
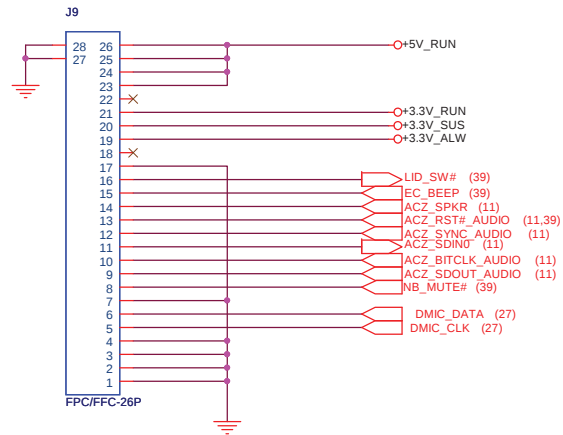
DG: Place TX cap close to connector



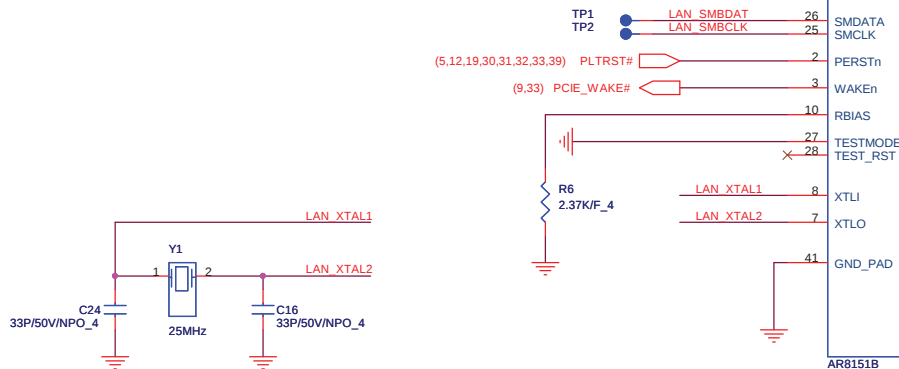
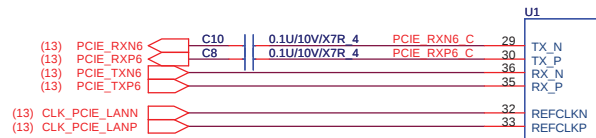
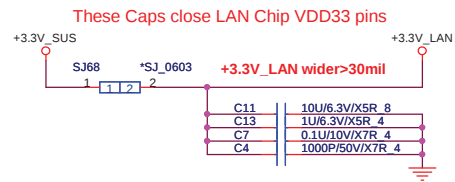
3-axis Fall Sensor (HDD data protector)



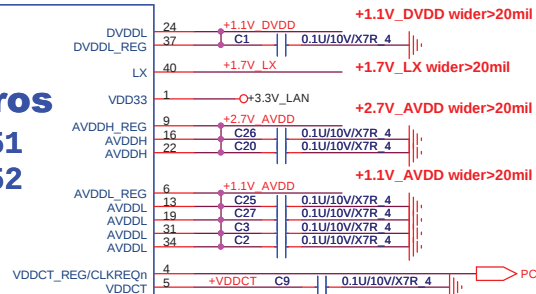
CONNECT TO AUDIO BOARD



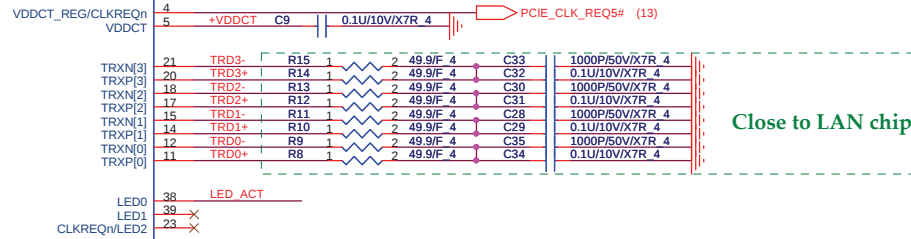
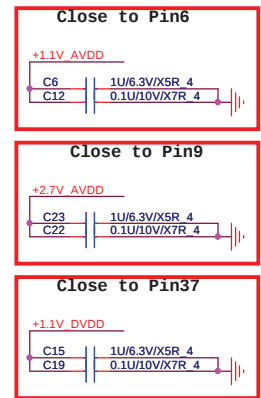
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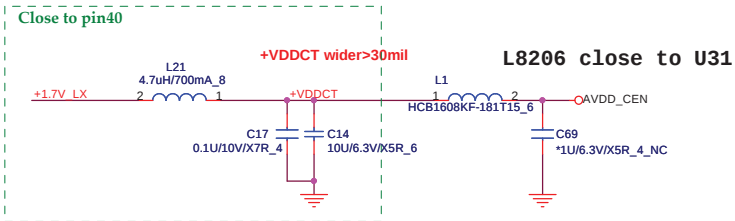
Atheros
AR8151
AR8152



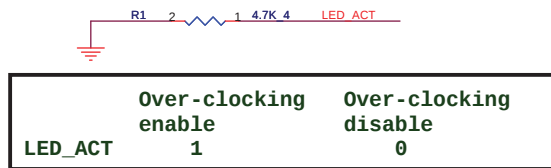
Netlist delete
Pin13 &19



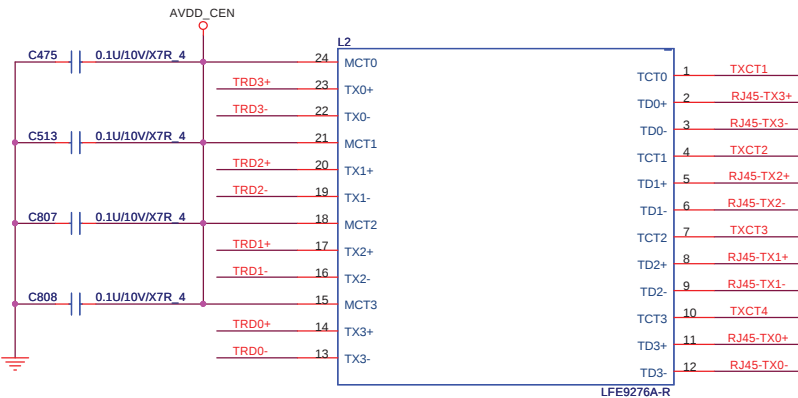
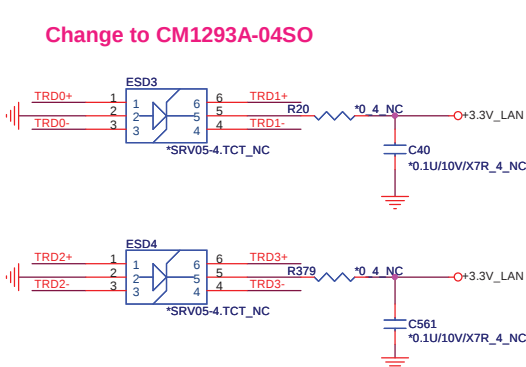
Close to LAN chip



L8206 close to U31

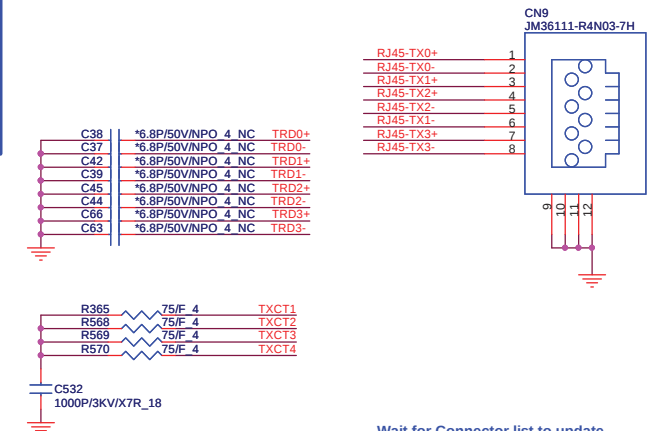


Change to CM1293A-04SO



LFE9276A-R

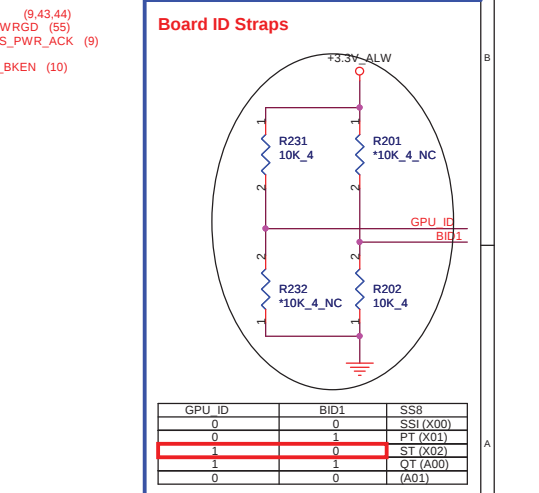
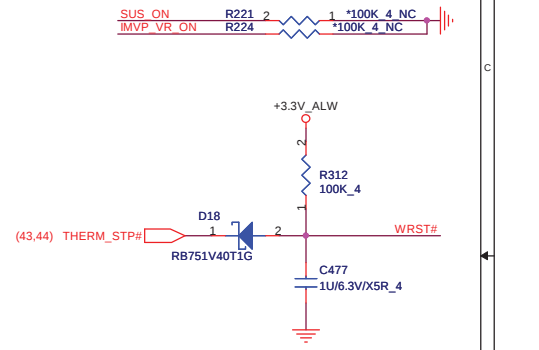
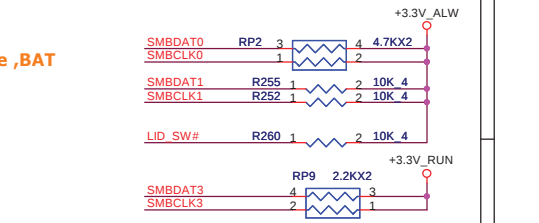
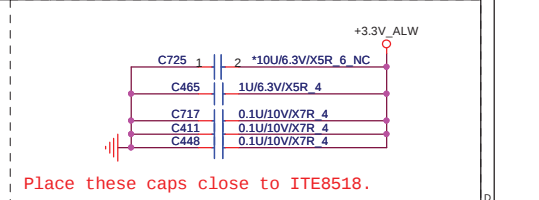
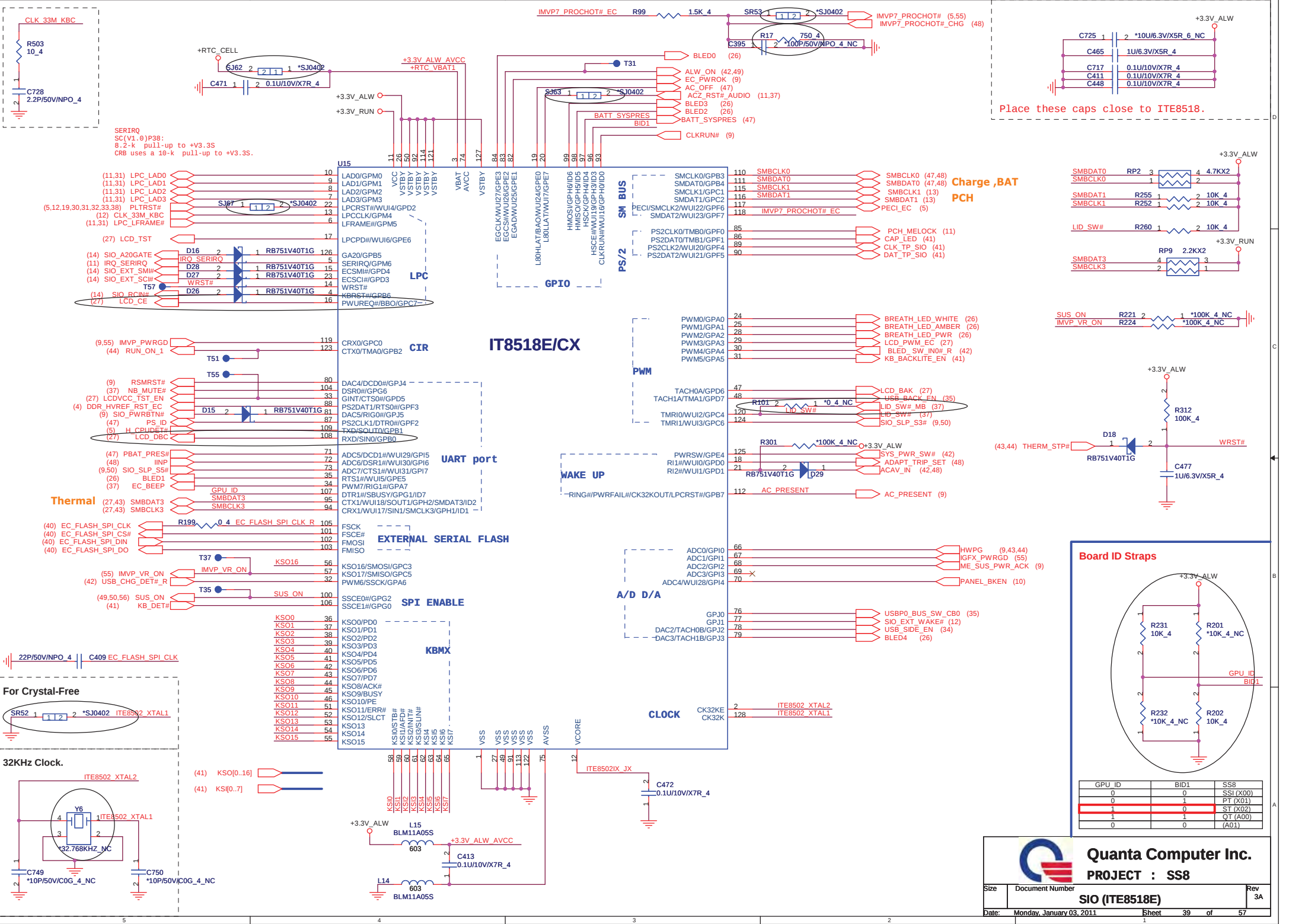
RJ-45 Connector



Wait for Connector list to update



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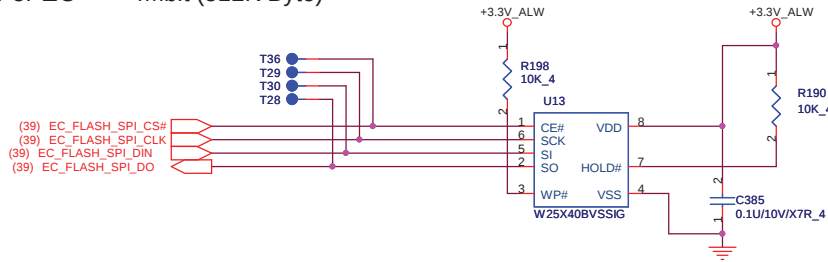


GPU_ID	BID1	SS8
0	0	SSI(X00)
0	1	ST(X01)
1	0	ST(X02)
1	1	QT(A00)
0	0	(A01)

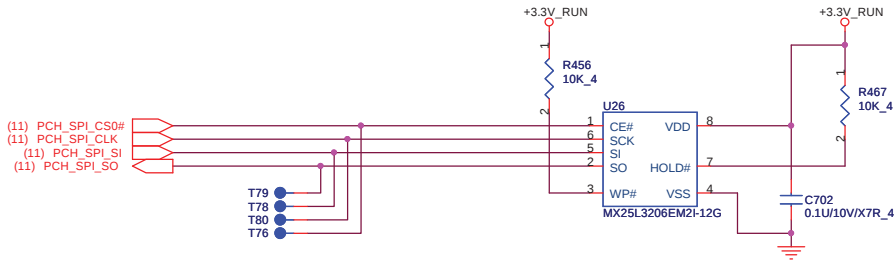
Quanta Computer Inc.
PROJECT : SS8
SIO (ITE8518E)

Size	Document Number	Rev
		3A
Date	Monday, January 03, 2011	Sheet 39 of 57

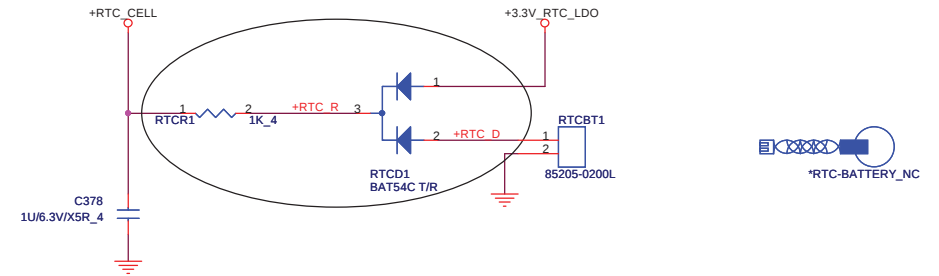
For EC 4Mbit (512K Byte)



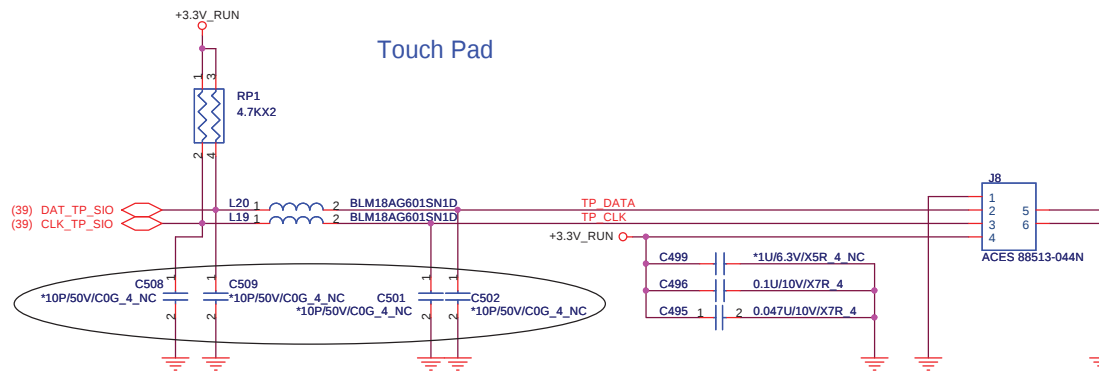
For PCH 32Mbit (4M Byte)



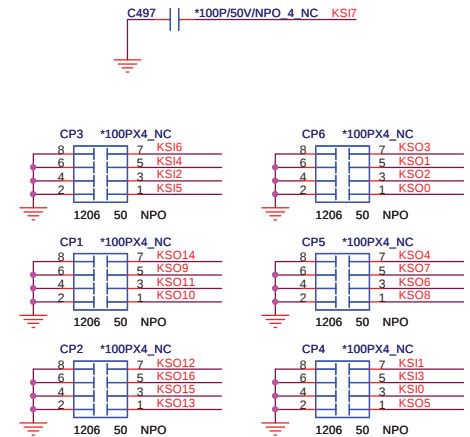
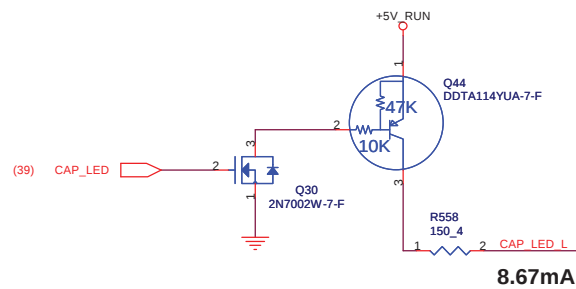
RTC BATTERY



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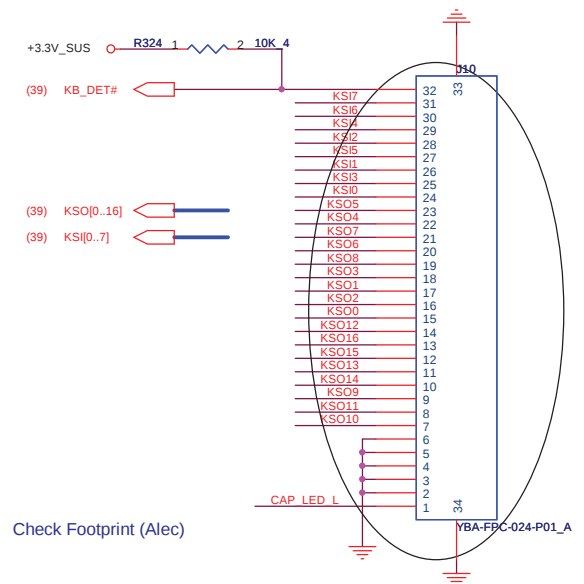


$V_{i(on_max)} = -1.4V$
 $V_{i(off_min)} = -0.3$



100P CAPS CLOSE TO JKB1

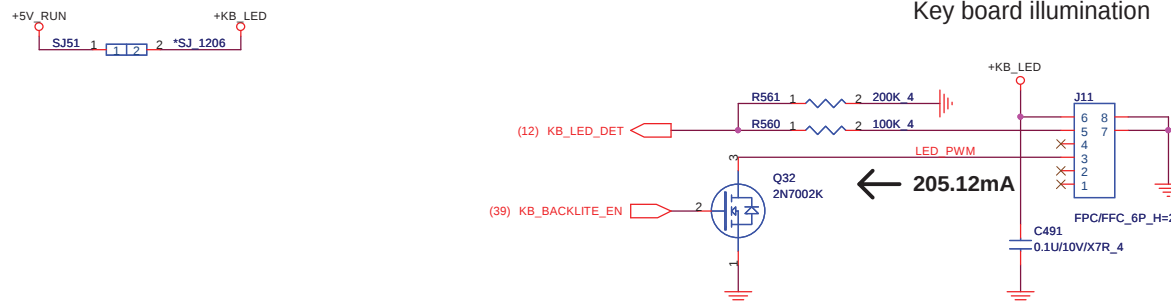
KEYBOARD CONNECTOR



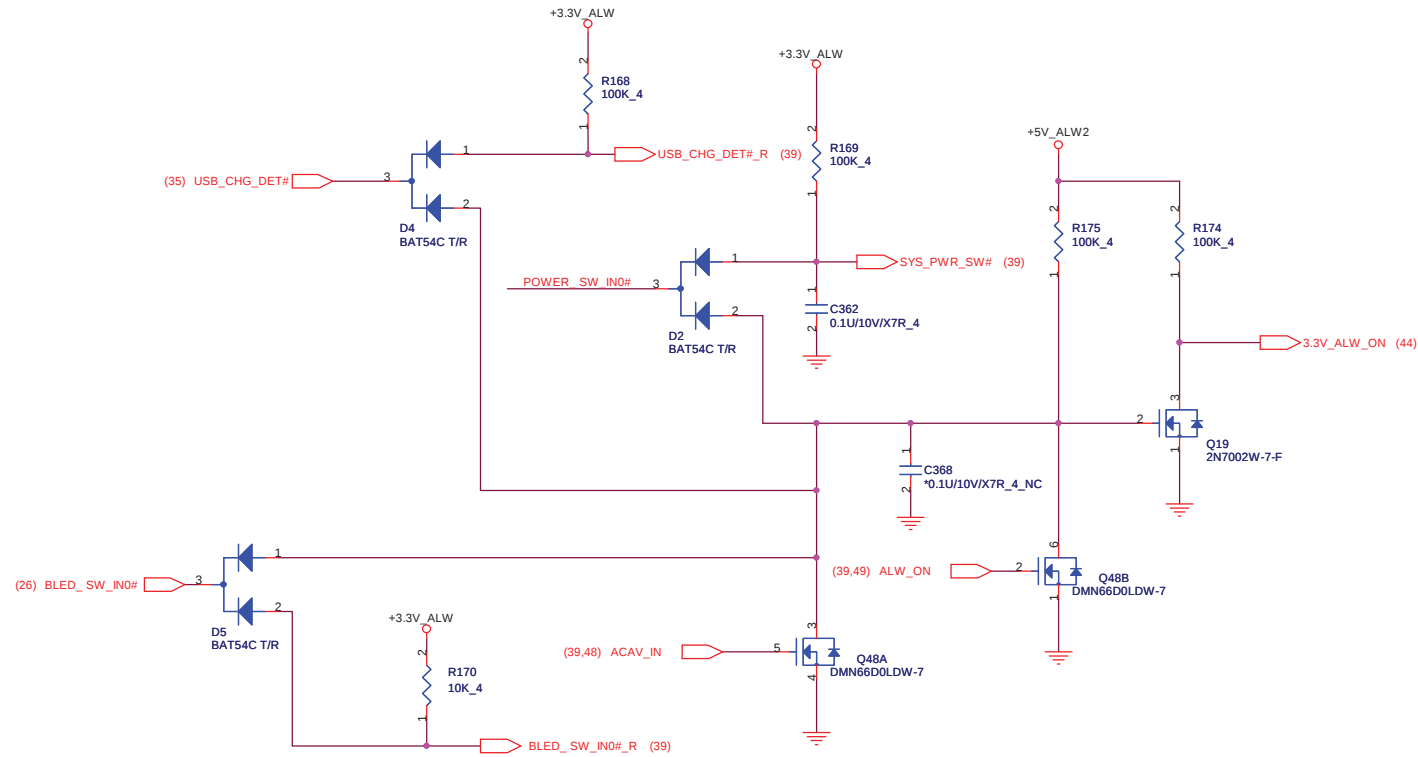
Conn Copy From SS7

+KB_LED power trace width >10 mil

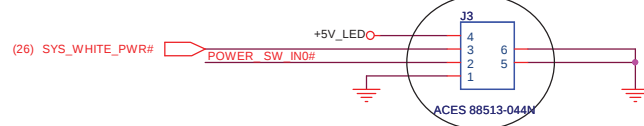
Key board illumination



3VALW ON POWER LOGIC



Conn to PWR Board



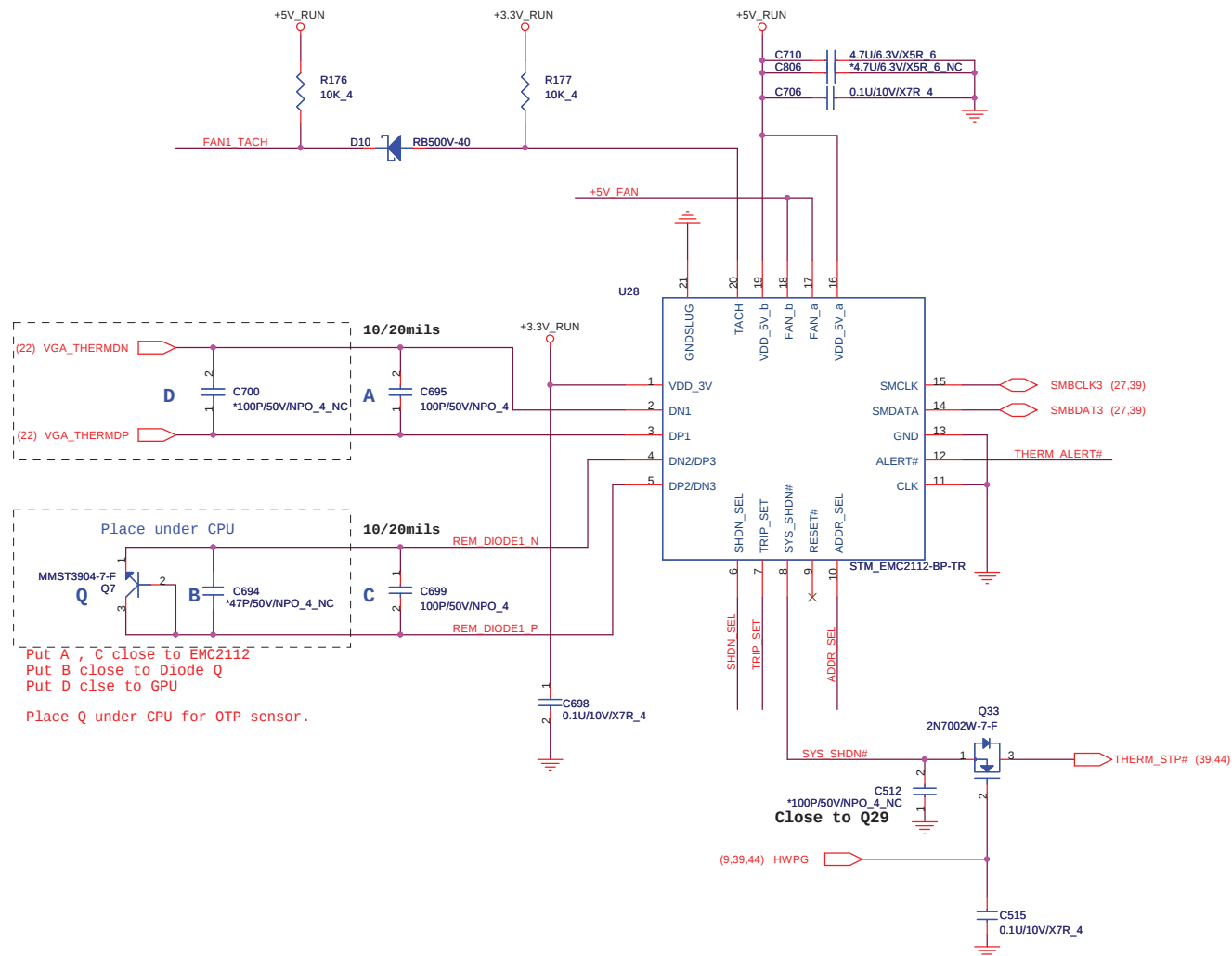
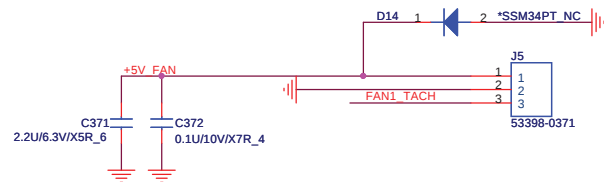
Status White LED

Solid White= System On, Normal Activity
 Solid White= Charging (system on);
 Solid White= Charging (system off or hibernate and battery charge <98%);
 OFF= Charging (system off or hibernate and battery charge > 98%);
 "Breathing White " = System in Standby (S3);
 Off = System Off (or in Hibernate);



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FAN CONTROL



EMC2112 internal diode should be set 90 degree C (EC)

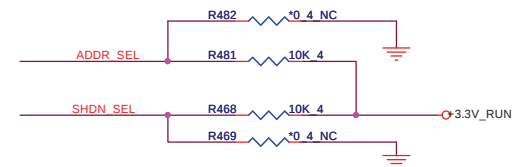


OTP Trip Point: 90 °C
OTP Hysteresis: 85 °C (Vincent)

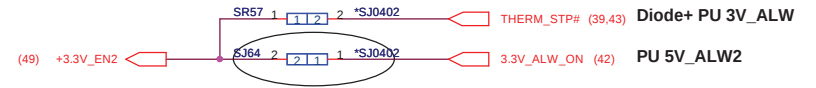
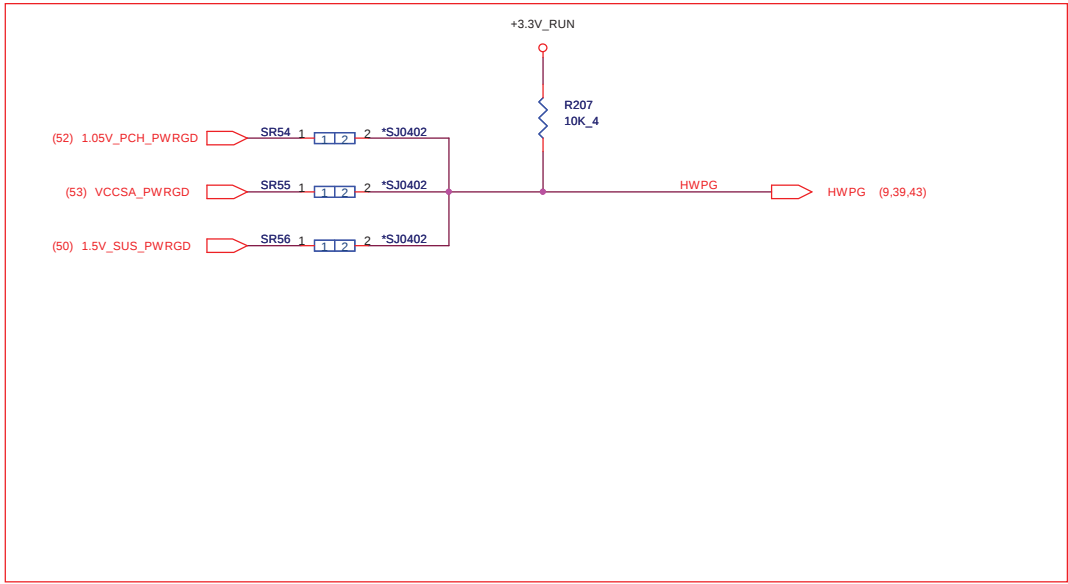
Need to check with BIOS

ADDR_SEL
HIGH: 0101 110xb
OPN: 0111 101xb
GND: 0101 111xb

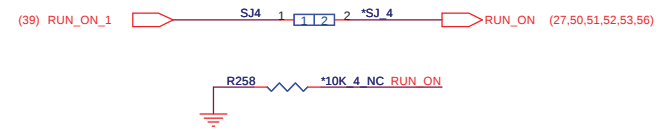
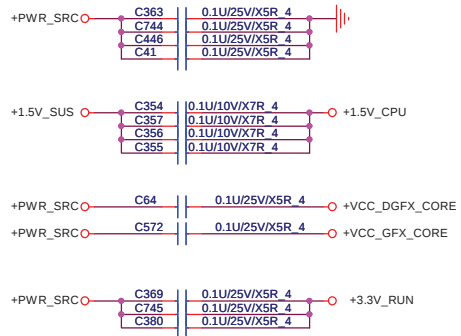
SHDN_SEL
HIGH: External Diode 2 Mode
OPN: AMD CPU/Diode Mode
GND: Intel Transistor Mode



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Stitch Cap



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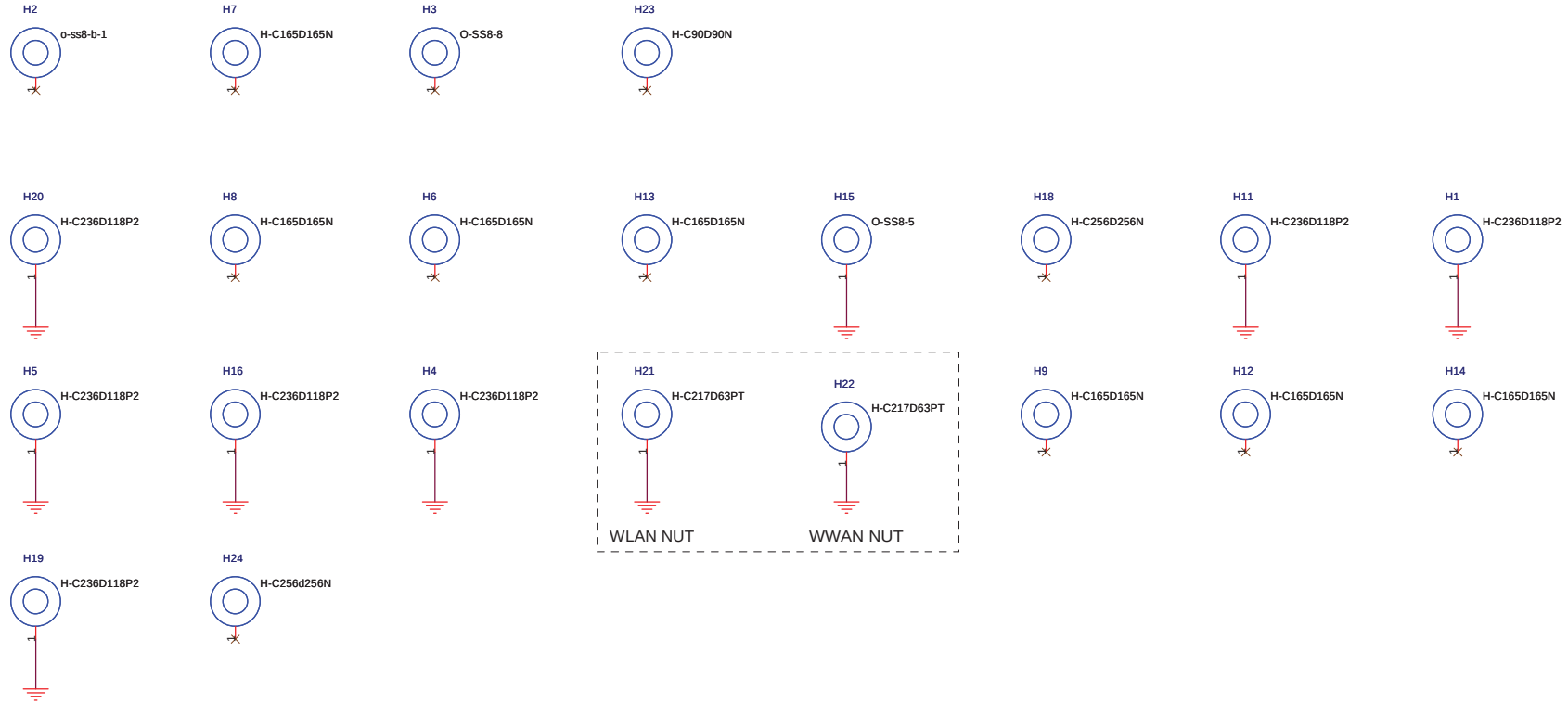
Size	Document Number	Rev
		3A
Date:	Monday, January 03, 2011	Sheet 44 of 57

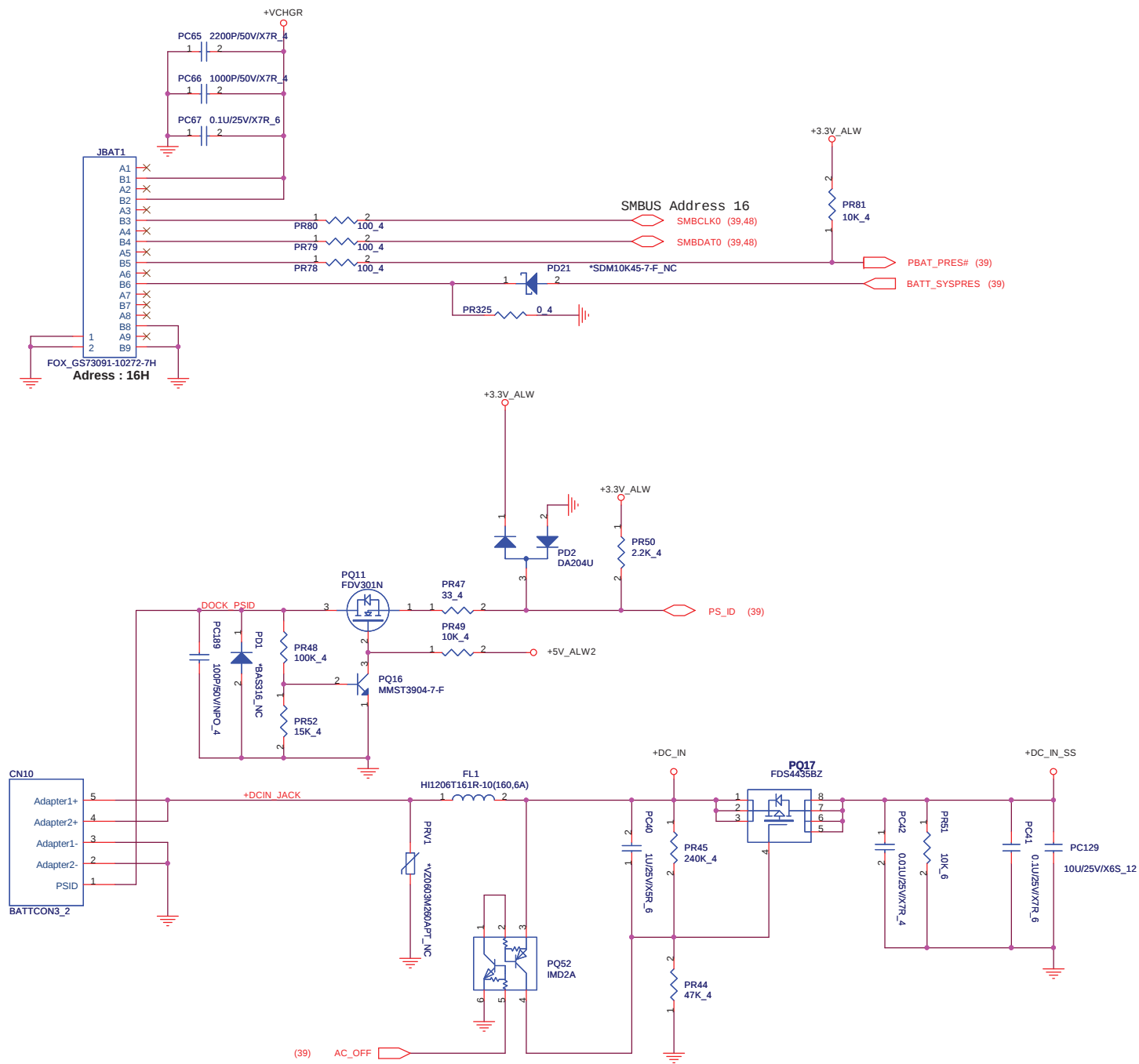
System Reset Circuit

CPU XDP

PCH XDP

Del 0420

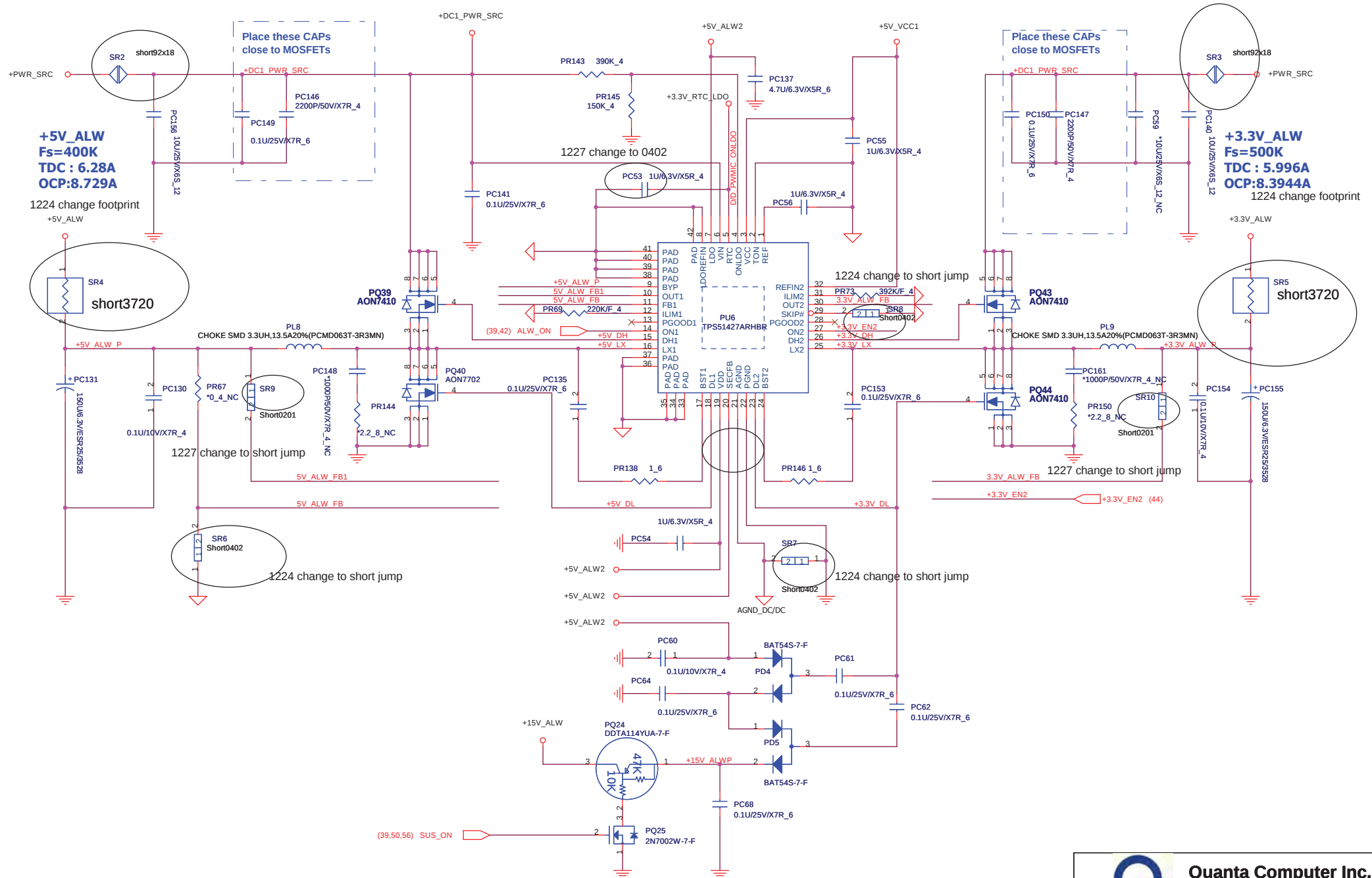




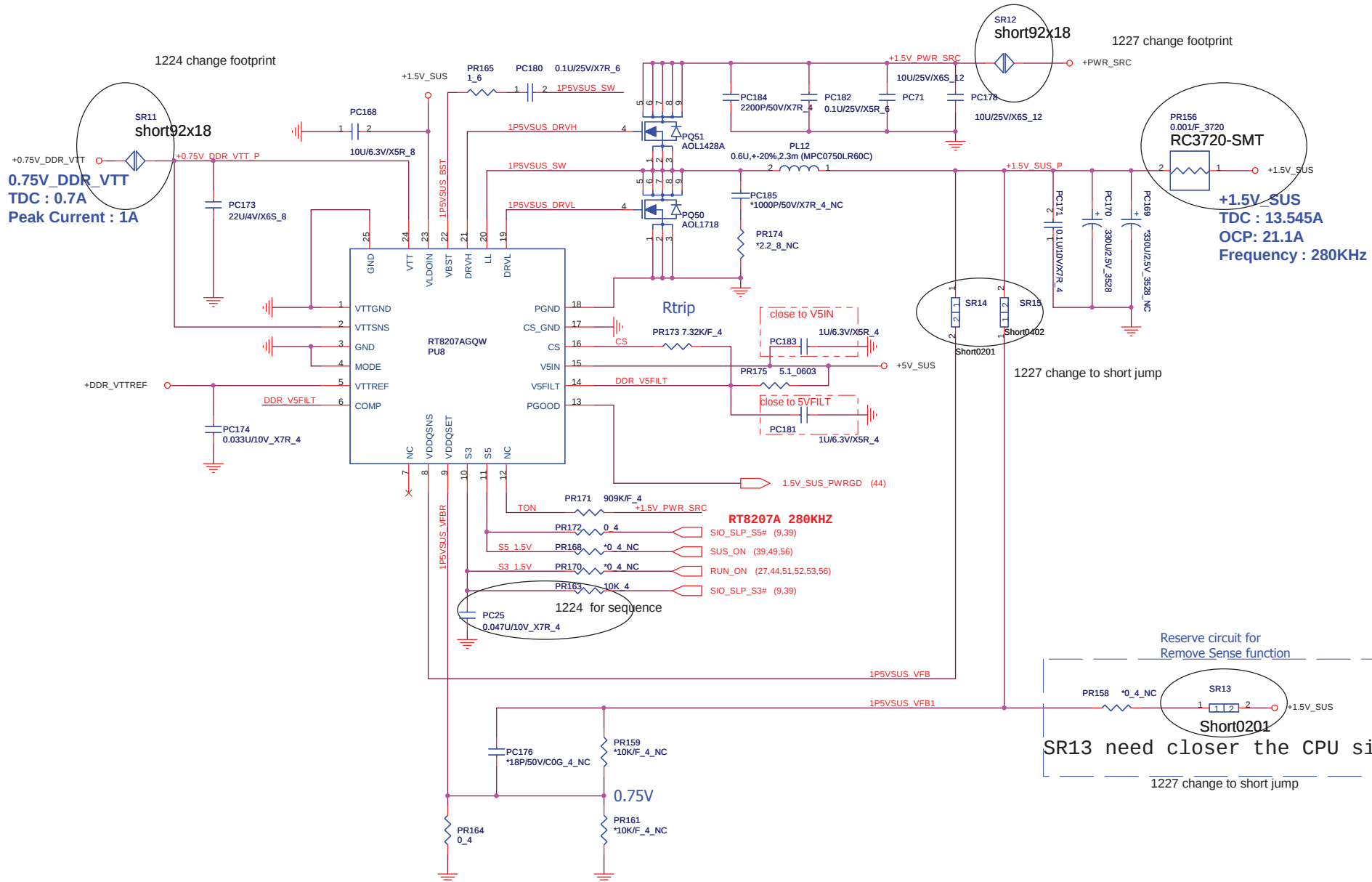
Quanta Computer Inc.
PROJECT : SS8

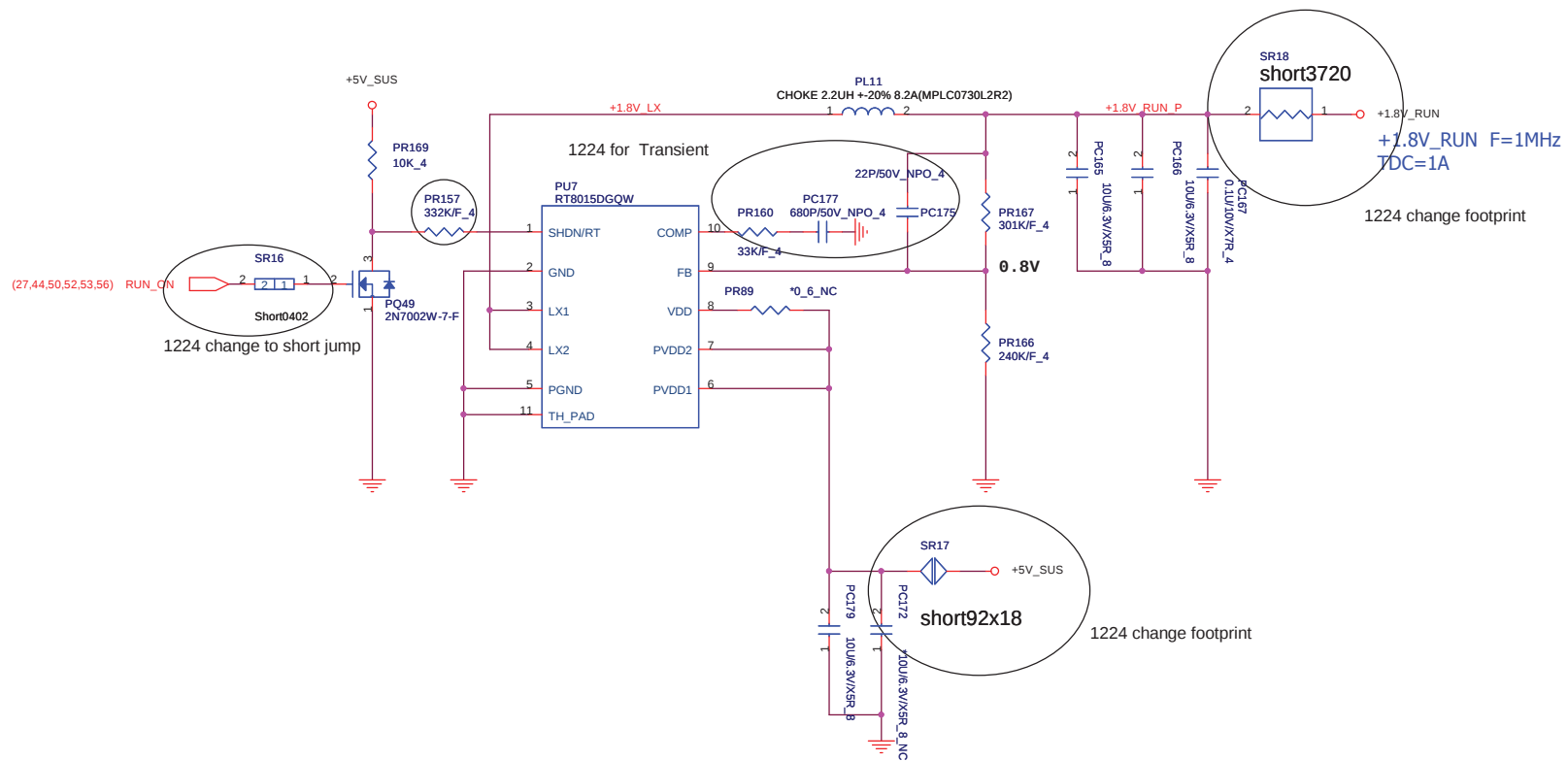
Size	Document Number	Rev
	DC IN / BATT	3A
Date:	Monday, January 03, 2011	Sheet 47 of 57

+3.3V_ALW / +5V_SUS / +15V_ALW (TPS51427ARHBR)



+1.5V_SUS (RT8207AGQW)

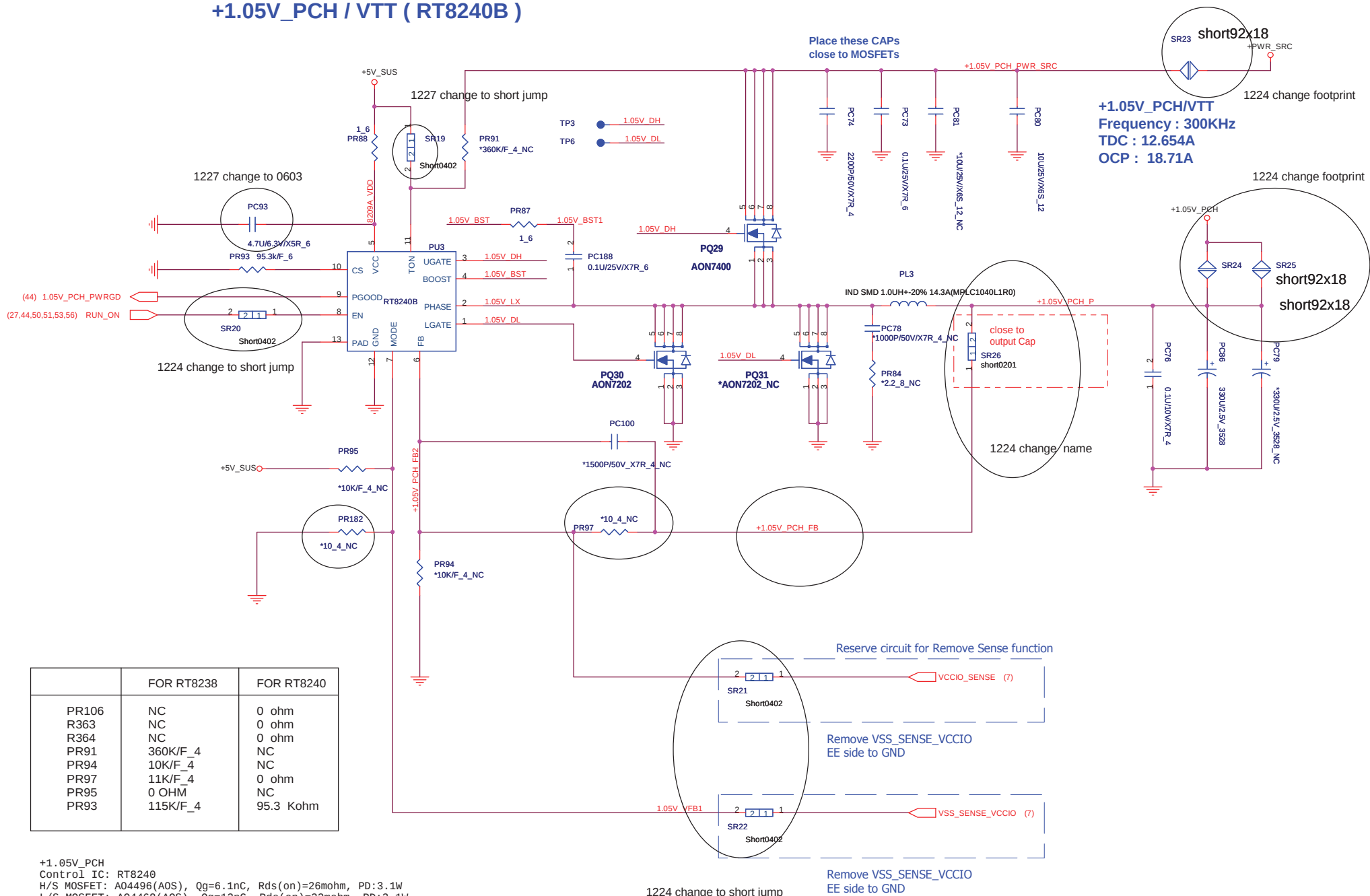




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PROJECT : SS8

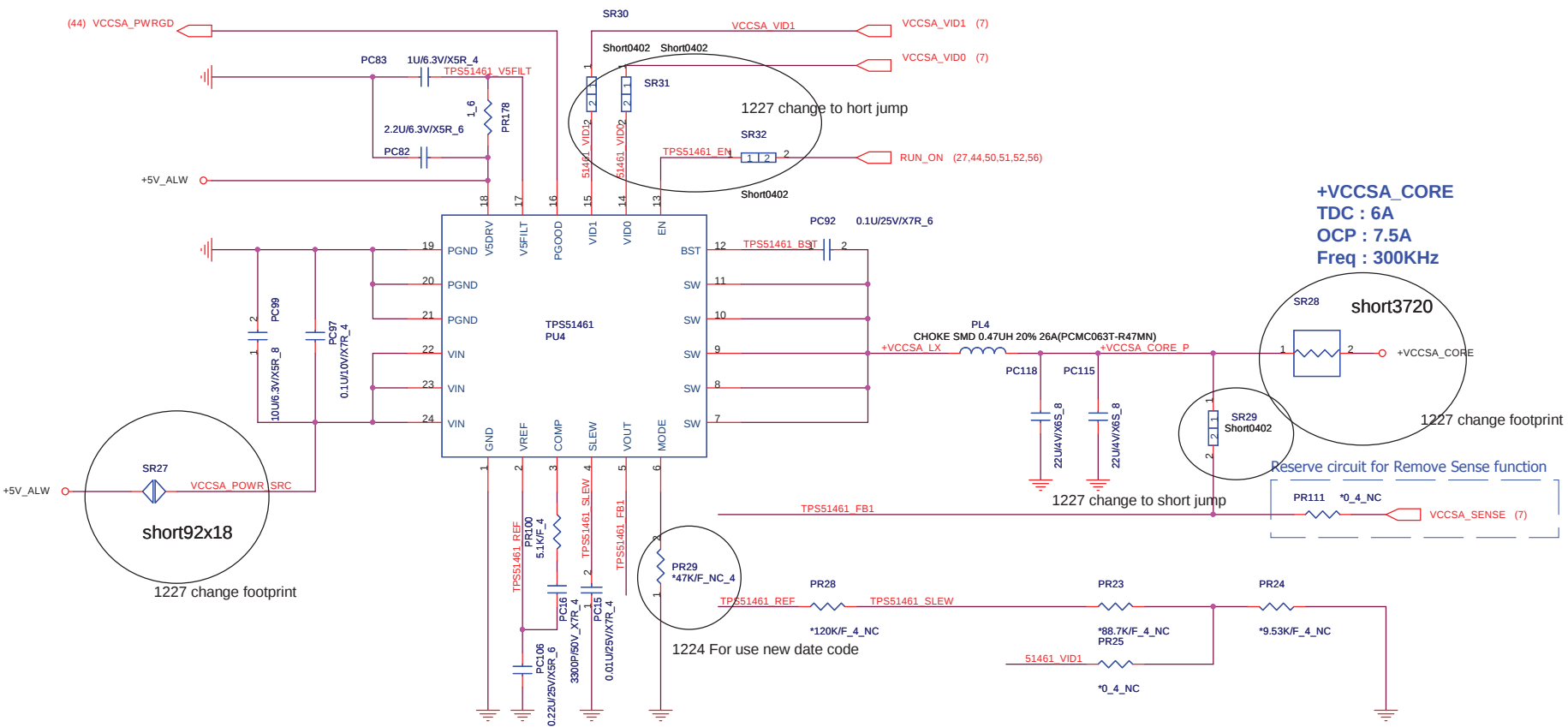
Size	Document Number	Rev
	1.8V_RUN (RT8015AGQW)	3A
Date:	Monday, January 03, 2011	Sheet 51 of 57

+1.05V_PCH / VTT (RT8240B)



+1.05V_PCH
Control IC: RT8240
H/S MOSFET: A04496(AOS), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: A04468(AOS), Qg=12nC, Rds(on)=22mohm, PD:3.1W
Inductor: 1.5UH+20% 9A (10D40F-1R5M)(TTA), DCR=10.5mohm
Output Cap: 1*390U, 2.5V(20%, 105C, 6.3*5.8), ESR=10mohm

	FOR RT8238	FOR RT8240
PR106	NC	0 ohm
R363	NC	0 ohm
R364	NC	0 ohm
PR91	360K/F_4	NC
PR94	10K/F_4	NC
PR97	11K/F_4	0 ohm
PR95	0 OHM	NC
PR93	115K/F_4	95.3 Kohm



+VCCSA_CORE
TDC : 6A
OCP : 7.5A
Freq : 300KHz

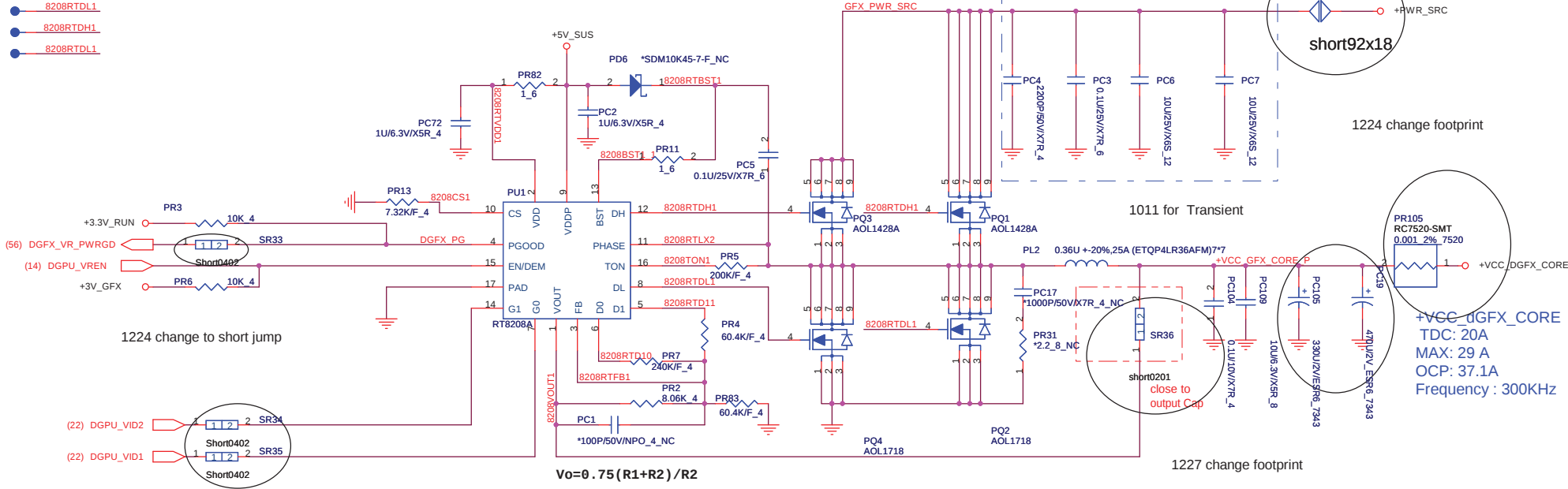
short92x18
1227 change footprint

short3720
1227 change footprint

+VCCSA	VCCSA_VID1	
0.8V	High	
0.9V	Low	Apply now

+VCC_dGFX_CORE (RT8208A)

- TP4 8208RTDH1
- TP8 8208RTDL1
- TP7 8208RTDH1
- TP5 8208RTDL1



+VCC_GFX_CORE
Control IC: RT8208A
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.36uH +-20% 45A(MP0104F-R36H1)(Delta), DCR=0.89mohm
Output Cap: 2*390u, 2.5V(20%, 105C, 6.3*5.8), ESR=10mohm

DGPU_VID1	DGPU_VID2	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	NA (0.875V)
LOW	HIGH	0.95V
HIGH	HIGH	0.975V

TON1	PR211 = 200K
FREQ	297K

