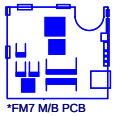

FM7 Hepburn Intel Discrete GFX

VER : D3B

POWER

SYSTEM RESET CIRCUIT PG 44

BATT CHARGER PG 46

RUN POWER SW +3.3V_SUS/+5V_SUS +5V/+3.3V/+1.8V PG 53

AC/BATT CONNECTOR PG 54

Penryn (478 Micro-FCPGA) PG 3,4

1066 MHz FSB

FAN & THERMAL SMSC1423 PG 39

CLOCK SLG8SP513V (QFN-64) PG 17

POWER

REGULATOR +1.5V_RUN/+1.05V_VCCP PG 48

REGULATOR +1.8V_SUS/+1.25V_RUN /+0.9V_DDR_VTT PG 49

CPU VR PG 51

DC/DC +3.3V_ALW/+5V_ALW/ +15V_ALW PG 52

VGA Core PG 50

CANTIGA 1329 uFCBGA PG 5,6,7,8,9,10

DDR2-SODIMM1 PG 15,16

667/800 MHZ DDR II

DDR2-SODIMM2 PG 15,16

667/800 MHZ DDR II

PCIEx16

GDDR2 x 4 (256M 64bits) PG 23

ATI M82-SCE PCI EXPRESS GFX PG 18,19,20,21,22

LVDS — **Panel Connector** PG 26

HDMI — **HDMI CONN.** PG 26

VGA — **CRT CONN.** PG 27

SATA-ODD PG 36 — SATA

SATA-HDD PG 36 — SATA

DMI interface

ICH9-M 676 BGA PG 11,12,13,14

USB2.0 x 4 — **USB conn x 4** PG 35

PCIEx1 — **LAN BCM5784M** PG 42 — **RJ45/Magnetics** PG 43

PCIEx1 / USB2.0 — **EXPRESS-CARD** R5538 PG 30

E-SATA Combo with USB CONN PG 35 — **PI2EQX3211BHE** PG 35 — SATA

PCIEx2 / USB2.0 — **MINI-CARD** WLAN PG 34

PCIEx1 / USB2.0 — **MINI-CARD** WWAN PG 33

USB2.0 — **MINI-CARD** WPAN PG 33

IHDA / USB2.0 — **AUDIO/AMP** 92HD73C PG 40 — **Camera + D-MIC** PG 41

Biometric PG 38

LPC — **KBC** ITE8512 PG 31

CIR TSOP36136TR PG 37

18X8 — **Keyboard** PG 37

SPI — **FLASH 2Mbyts** PG 32

PS/2 — **Touchpad** PG 37

USER INTERFACE PG 38

Audio SPK conn PG 40

Audio Jacks x3 PG 41

33MHz PCI — **8-in-1 Card Reader** R5C833 PG 28

1394 — **1394 CONN.** PG 29

Card Reader CONN. PG 30

QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number FM6	Rev 3A
Date: Thursday, July 31, 2008	Sheet 1 of 58	

Table of Contents

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,50,51,52,56	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+5V_ALW2	+5V	37,38,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,26,30,37,38,43,48,49, 50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,26,27,36,37,38,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,26,27,28,30, 31,33,34,36,38,39,40,41,42,53,56	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,53,56	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.2V_LOM	+1.25V	42	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.1V_GFX_PCIE	+1.1V	21,50	VGA POWER	RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48,56	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51,56	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	

GND PLANE	PAGE	DESCRIPTION
8731AGND	46	
AGND_0.9V	49	
AGND_DC/DC	52	
AGND_DC2	48	
AGND_DDR	49	
AGND_ISL6260	51	
GND	ALL	

QUANTA COMPUTER

Title	Index & Power Status	
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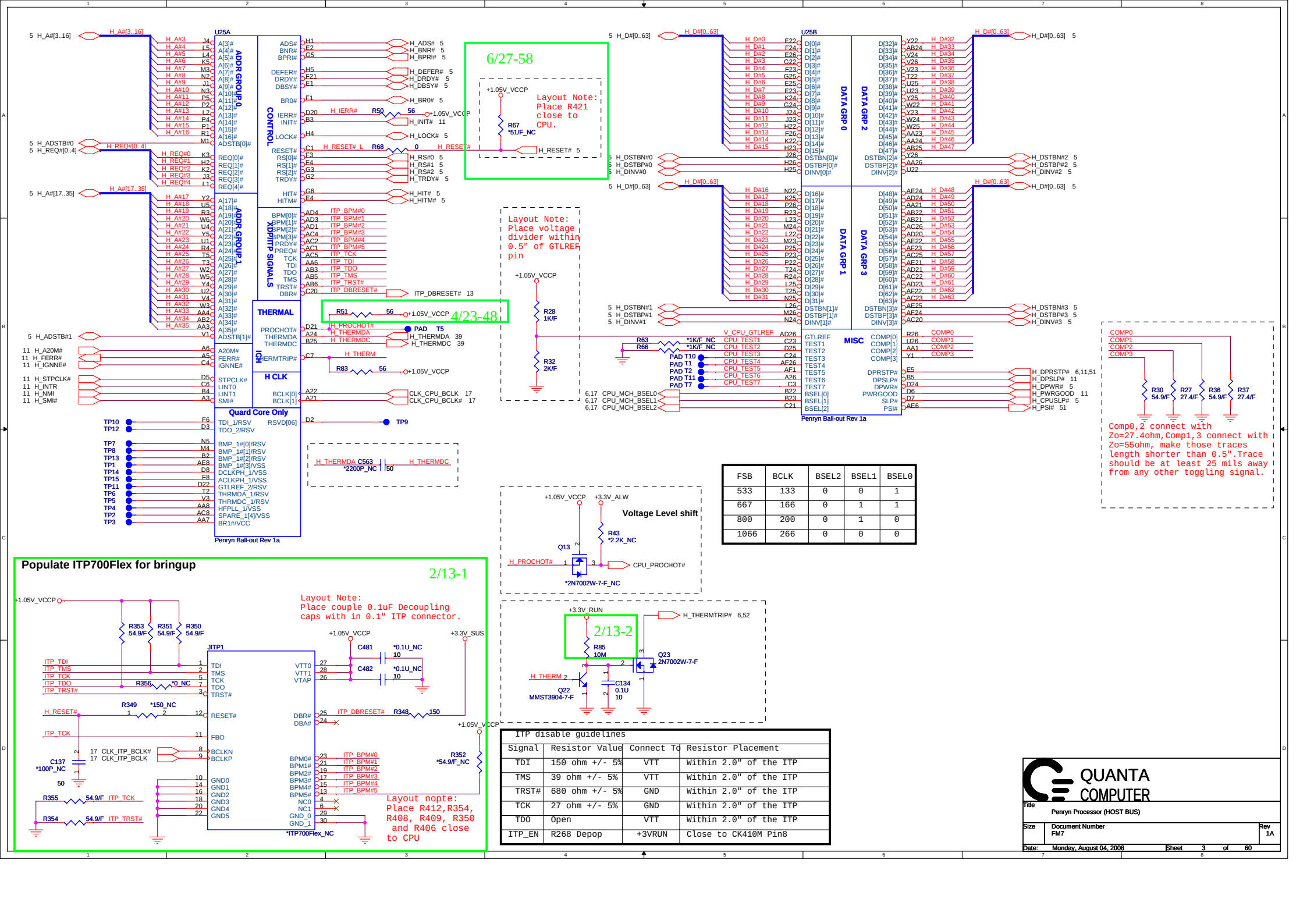


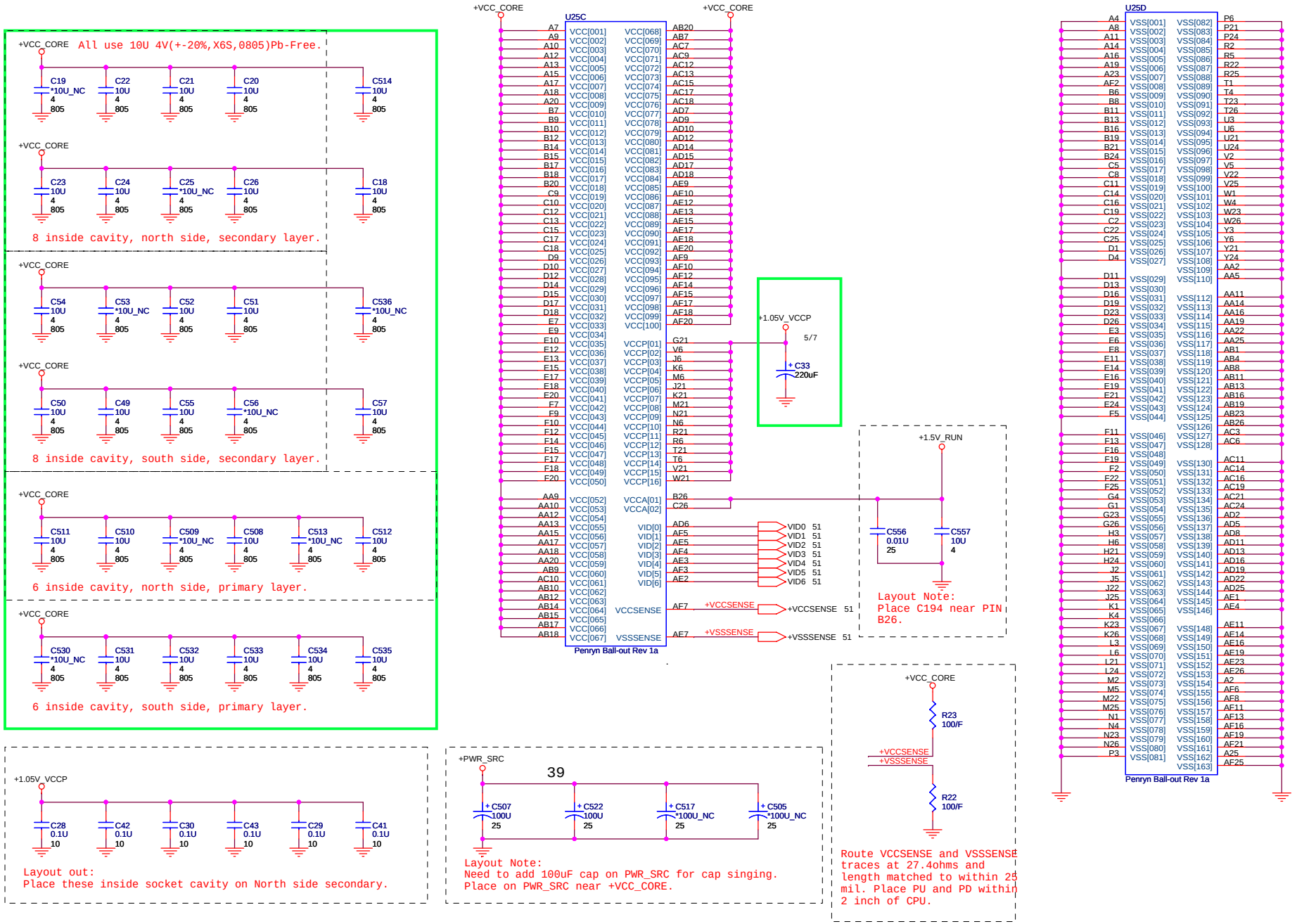
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8

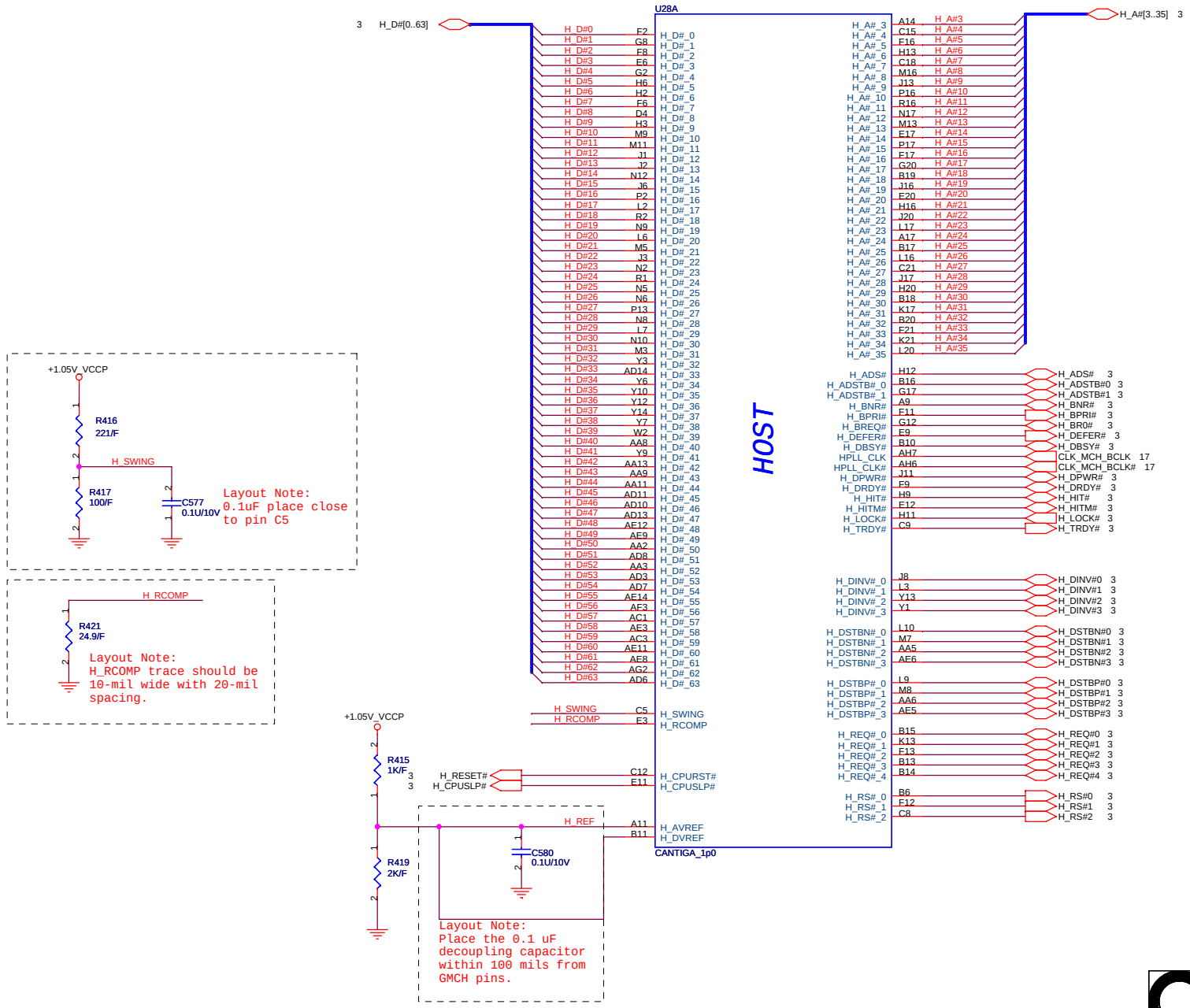
QUANTA COMPUTER

Title	Penryn Processor (HOST BUS)	
Size	Document Number FM7	Rev 1A
Date: Monday, August 04, 2008	Sheet 3 of 60	



Title	Penryn Processor (HOST BUS)		
Size	Document Number FM7		Rev 1A
Date:	Monday, August 04, 2008	Sheet 4 of 60	

QUANTA COMPUTER



Title	Cantiga (HOST)		
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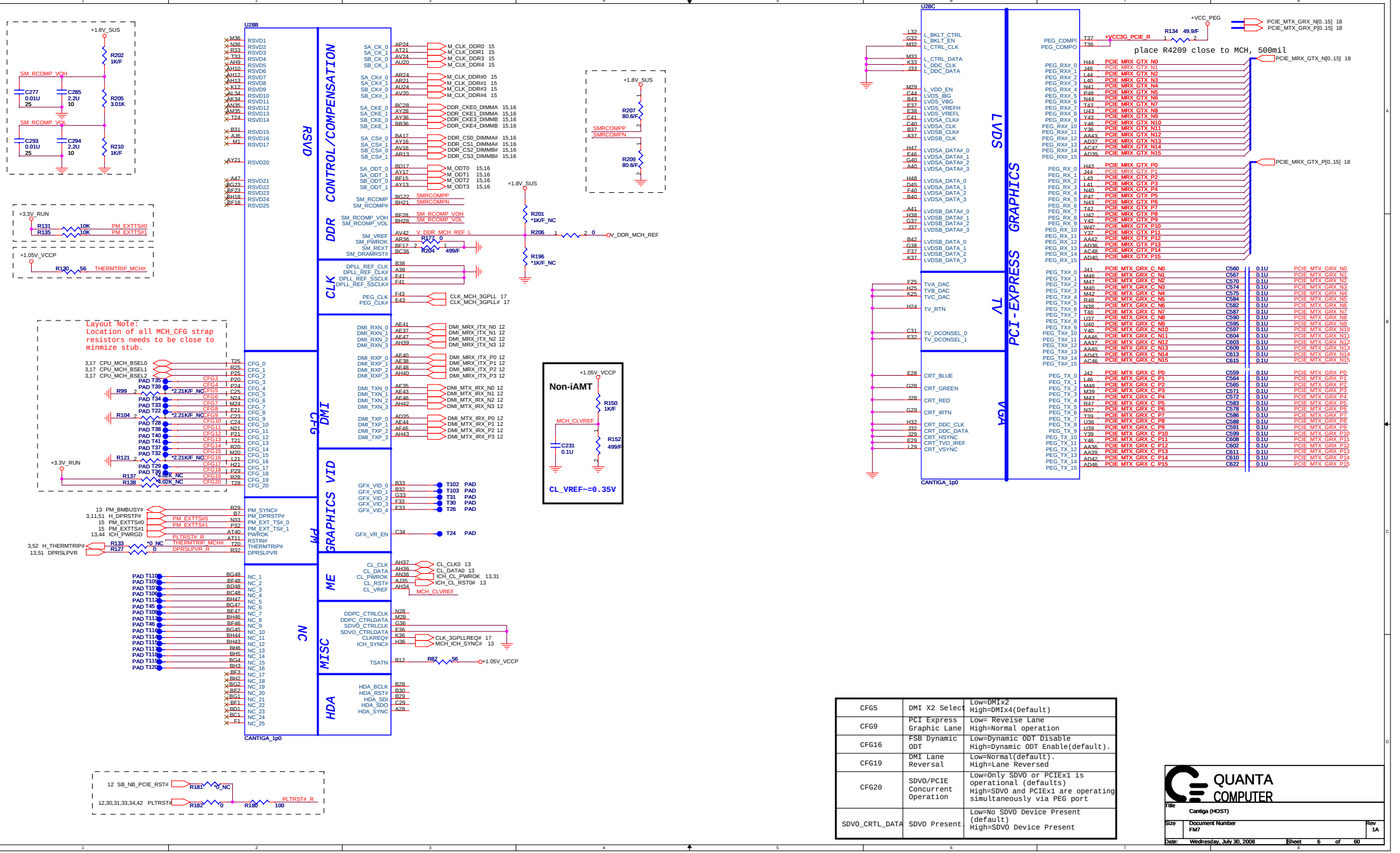
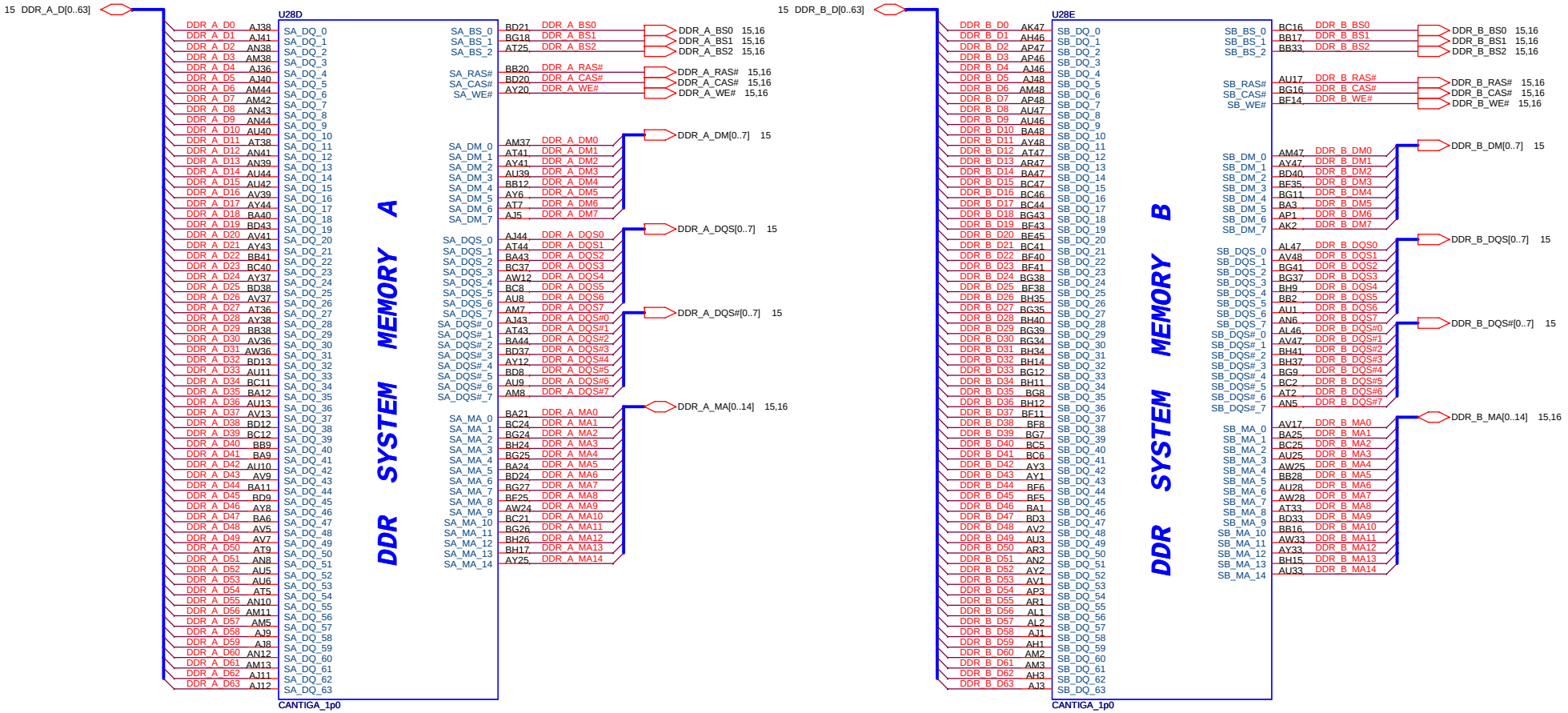
QUANTA COMPUTER



CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present



QUANTA COMPUTER

Title	Cantiga (HOST)	
Size	Document Number FM7	Rev 1A
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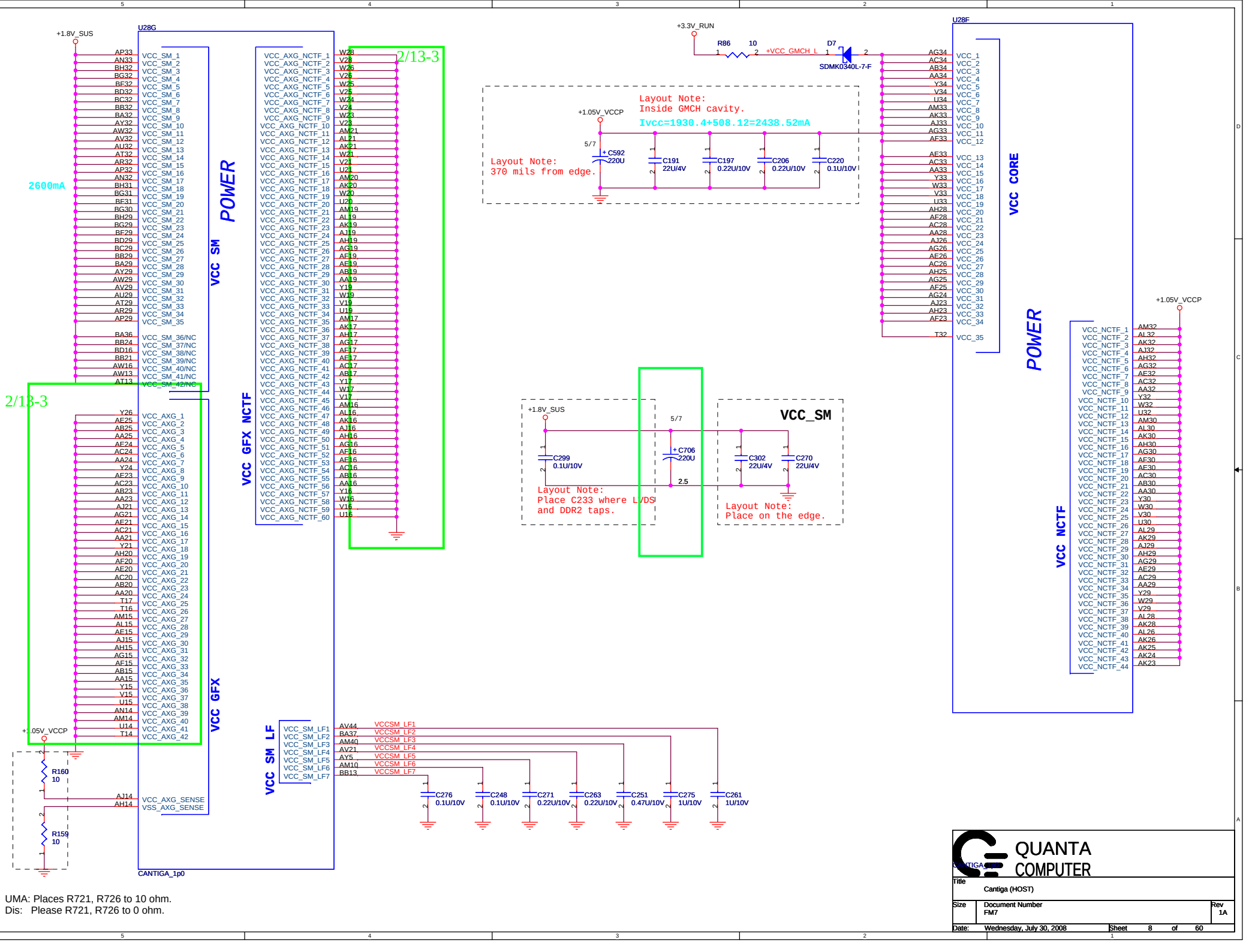

UMA: Places R721, R726 to 10 ohm.
Dis: Please R721, R726 to 0 ohm.

QUANTA COMPUTER

Title	Cantiga (HOST)	
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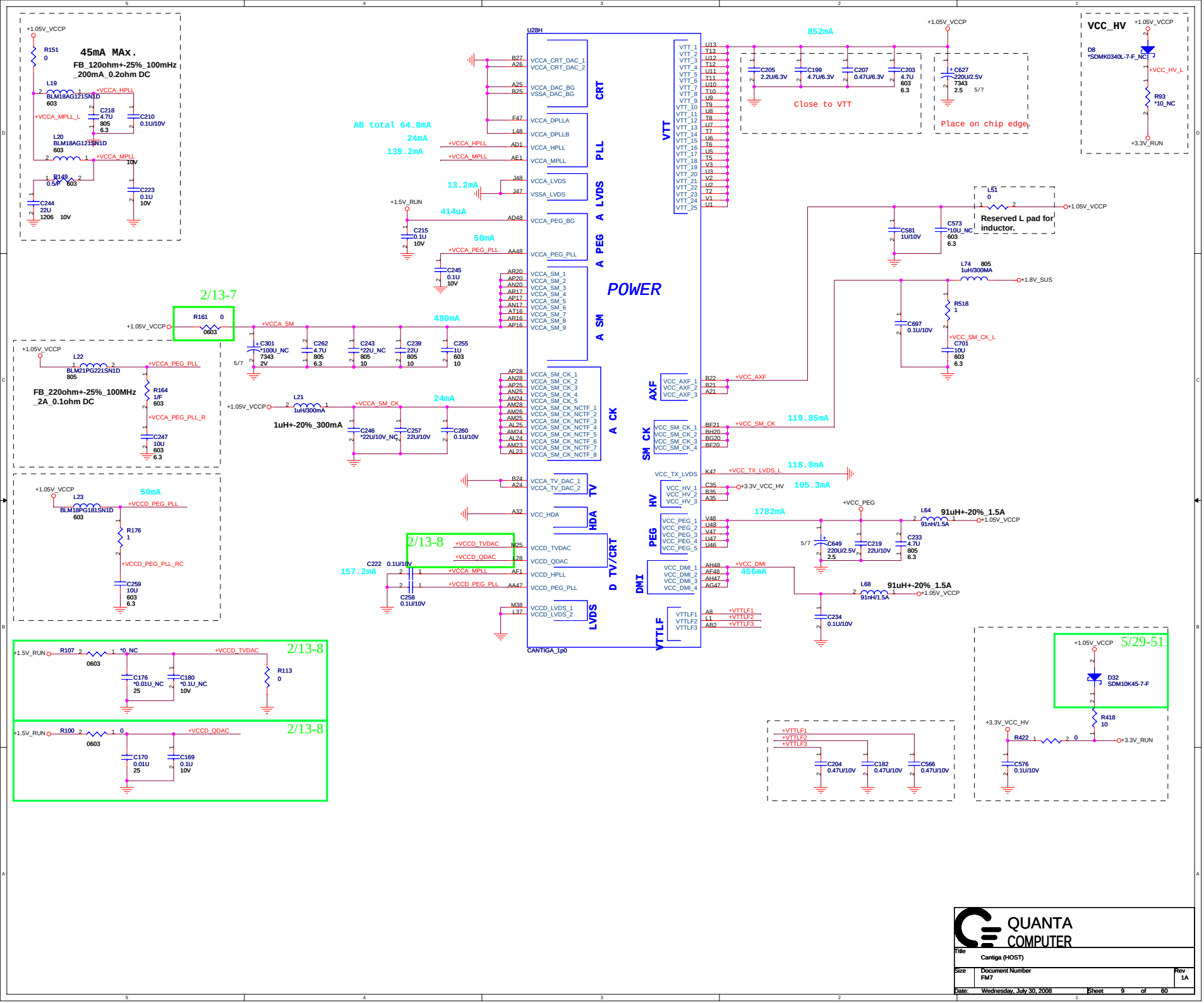
45mA MAx.
FB_120ohm+-25%_100mHz
_200mA_0.2ohm DC
FB_220ohm+-25%_100MHz
_2A_0.1ohm DC
1uH+-20%_300mA
91uH+-20%_1.5A
AB total 64.8mA
24mA
139.2mA
13.2mA
414uA
50mA
480mA
24mA
119.85mA
118.8mA
105.3mA
1782mA
456mA
157.2mA
852mA
Close to VTT
Place on chip edge.
Reserved L pad for inductor.
2/13-7
2/13-8
2/13-8
5/29-51
U28H
POWER
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
CANTIGA_1p0
VCC_HV
D8 *SDMK0340L-7-F_NC
D32 SDM10K45-7-F
QUANTA COMPUTER
Title: Cantiga (HOST)
Size: Document Number FM7
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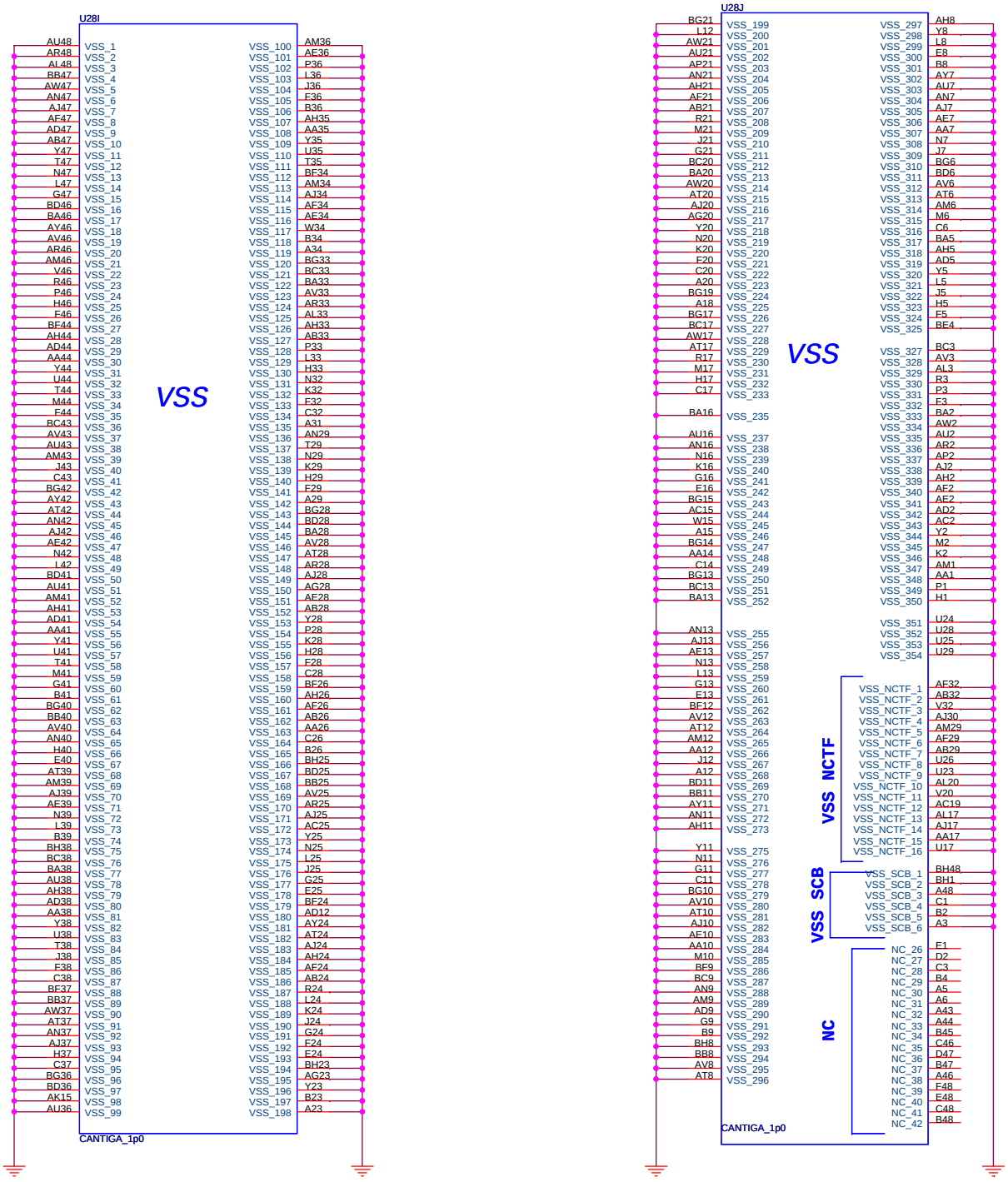
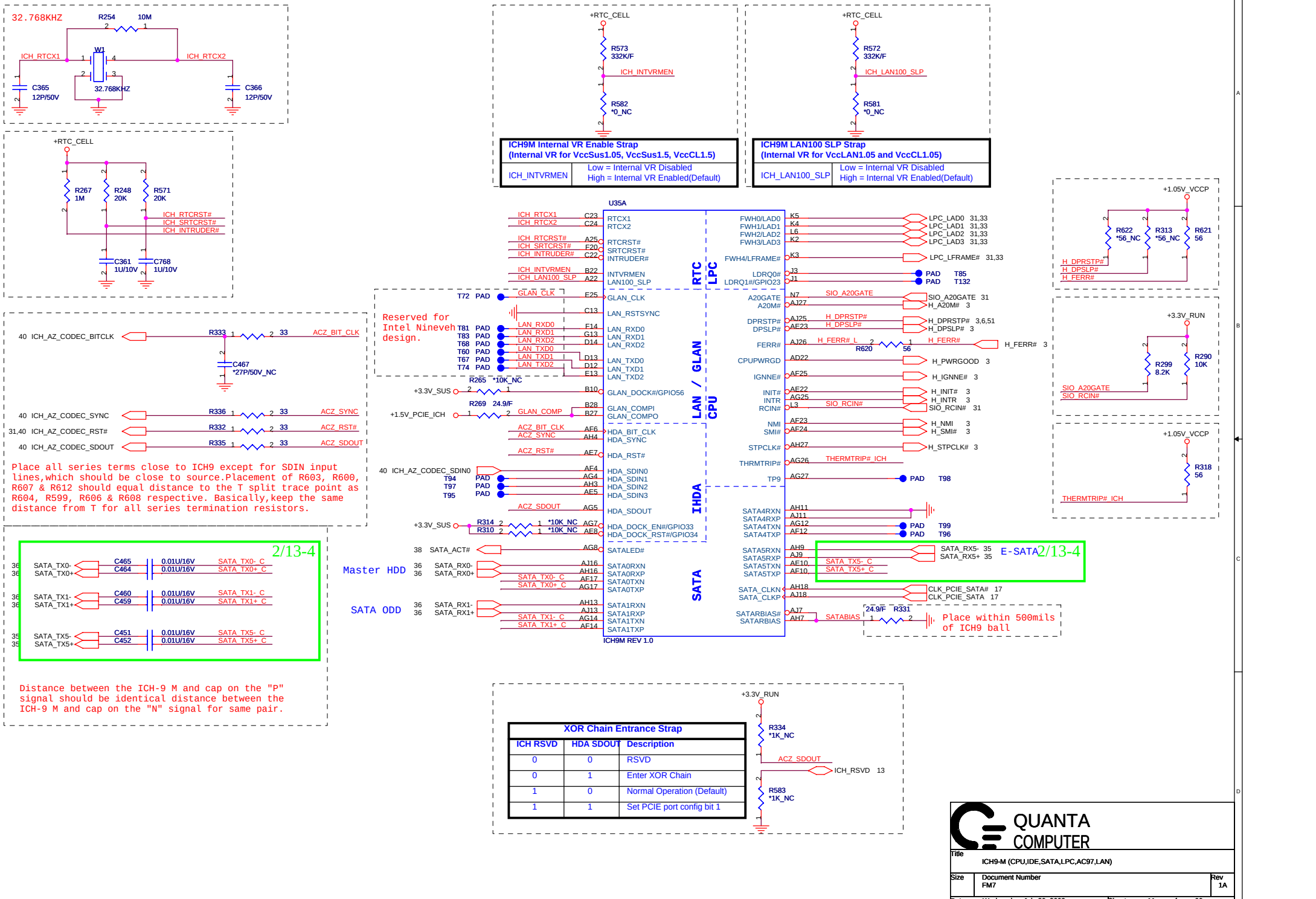


QUANTA COMPUTER		
Title	Cantiga (HOST)	
Size	Document Number FM7	Rev 1A
Date: Wednesday, July 30, 2008	Sheet 10 of 60	


32.768KHZ
R254 10M
W1
ICH_RTCX1
ICH_RTCX2
C365 12P/50V
32.768KHZ
C366 12P/50V
+RTC_CELL
R267 1M
R248 20K
R571 20K
ICH_RTCRST#
ICH_SRTCRST#
ICH_INTRUDER#
C361 1U/10V
C768 1U/10V
+RTC_CELL
R573 332K/F
ICH_INTVRMEN
R582 *0_NC
ICH9M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)
ICH_INTVRMEN
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
+RTC_CELL
R572 332K/F
ICH_LAN100_SLP
R581 *0_NC
ICH9M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)
ICH_LAN100_SLP
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
U35A
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
RTC
LPC
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN / GLAN
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
CPU
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
IHDA
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA
ICH9M REV 1.0
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP9
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
Reserved for Intel Nineveh design.
T72 PAD
T81 PAD
T83 PAD
T68 PAD
T60 PAD
T67 PAD
T74 PAD
R265 *10K_NC
+3.3V_SUS
R269 24.9/F
+1.5V_PCIE_ICH
GLAN_COMP
40 ICH_AZ_CODEC_BITCLK
R333 33
ACZ_BIT_CLK
C467 *27P/50V_NC
40 ICH_AZ_CODEC_SYNC
R336 33
ACZ_SYNC
31,40 ICH_AZ_CODEC_RST#
R332 33
ACZ_RST#
40 ICH_AZ_CODEC_SDOUT
R335 33
ACZ_SDOUT
Place all series terms close to ICH9 except for SDIN input lines,which should be close to source.Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respective. Basically,keep the same distance from T for all series termination resistors.
40 ICH_AZ_CODEC_SDIN0
T94 PAD
T97 PAD
T95 PAD
+3.3V_SUS
R314 *10K_NC
R310 *10K_NC
38 SATA_ACT#
Master HDD
SATA ODD
36 SATA_RX0-
36 SATA_RX0+
SATA_TX0- C
SATA_TX0+ C
36 SATA_RX1-
36 SATA_RX1+
SATA_TX1- C
SATA_TX1+ C
2/13-4
SATA_TX0-
SATA_TX0+
C465 0.01U/16V
C464 0.01U/16V
SATA_TX0- C
SATA_TX0+ C
SATA_TX1-
SATA_TX1+
C460 0.01U/16V
C459 0.01U/16V
SATA_TX1- C
SATA_TX1+ C
SATA_TX5-
SATA_TX5+
C451 0.01U/16V
C452 0.01U/16V
SATA_TX5- C
SATA_TX5+ C
Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.
+3.3V_RUN
R334 *1K_NC
ACZ_SDOUT
ICH_RSVD 13
R583 *1K_NC
XOR Chain Entrance Strap
ICH RSVD
HDA SDOUT
Description
0 0 RSVD
0 1 Enter XOR Chain
1 0 Normal Operation (Default)
1 1 Set PCIE port config bit 1
LPC_LAD0 31,33
LPC_LAD1 31,33
LPC_LAD2 31,33
LPC_LAD3 31,33
LPC_LFRAME# 31,33
PAD T85
PAD T132
SIO_A20GATE 31
H_A20M# 3
H_DPRSTP# 3,6,51
H_DPSLP# 3
H_FERR# 3
H_PWRGOOD 3
H_IGNNE# 3
H_INIT# 3
H_INTR 3
SIO_RCIN# 31
H_NMI 3
H_SMI# 3
H_STPCLK# 3
THERMTRIP# ICH
PAD T98
PAD T99
PAD T96
E-SATA
2/13-4
SATA_RX5- 35
SATA_RX5+ 35
SATA_TX5- C
SATA_TX5+ C
CLK_PCIE_SATA# 17
CLK_PCIE_SATA 17
24.9/F R331
SATABIAS
Place within 500mils of ICH9 ball
+1.05V_VCCP
R622 *56_NC
R313 *56_NC
R621 56
H_DPRSTP#
H_DPSLP#
H_FERR#
+3.3V_RUN
R299 8.2K
R290 10K
SIO_A20GATE
SIO_RCIN#
+1.05V_VCCP
R318 56
THERMTRIP# ICH
R620 56
QUANTA COMPUTER
Title
ICH9-M (CPU,IDE,SATA,LPC,AC97,LAN)
Size
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FM7
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1A
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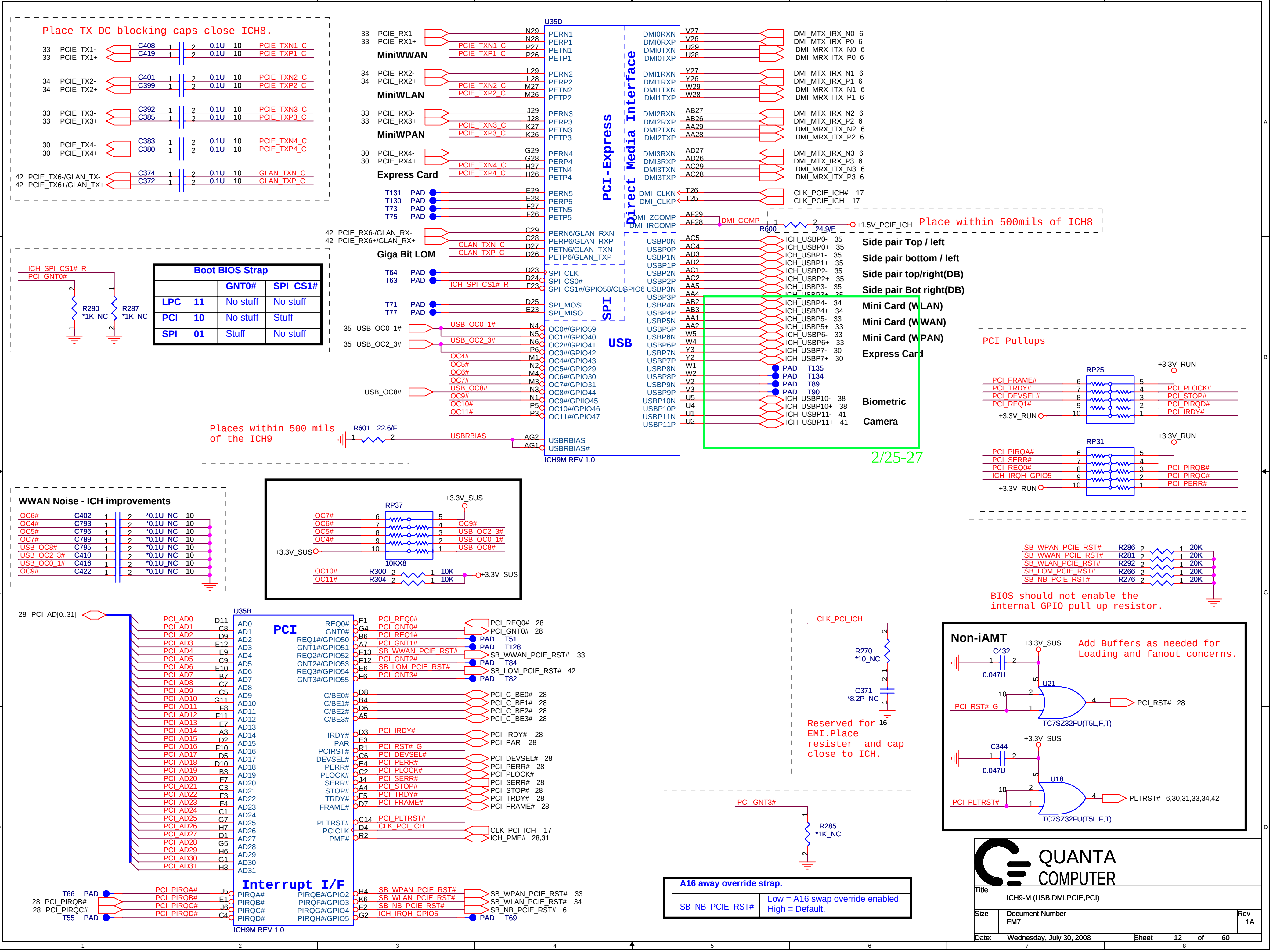
Place TX DC blocking caps close ICH8.
PCIE_TX1- PCIE_TX1+ C408 C419 0.1U PCIE_TXN1_C PCIE_TXP1_C
PCIE_TX2- PCIE_TX2+ C401 C399 0.1U PCIE_TXN2_C PCIE_TXP2_C
PCIE_TX3- PCIE_TX3+ C392 C385 0.1U PCIE_TXN3_C PCIE_TXP3_C
PCIE_TX4- PCIE_TX4+ C383 C380 0.1U PCIE_TXN4_C PCIE_TXP4_C
PCIE_TX6-/GLAN_TX- PCIE_TX6+/GLAN_TX+ C374 C372 0.1U GLAN_TXN_C GLAN_TXP_C
U35D
MiniWWAN
MiniWLAN
MiniWPAN
Express Card
Giga Bit LOM
PCI-Express
Direct Media Interface
SPI
USB
Place within 500mils of ICH8
R600 24.9/F +1.5V_PCIE_ICH
Side pair Top / left
Side pair bottom / left
Side pair top/right(DB)
Side pair Bot right(DB)
Mini Card (WLAN)
Mini Card (WWAN)
Mini Card (WPAN)
Express Card
Biometric
Camera
2/25-27
ICH9M REV 1.0
Places within 500 mils of the ICH9
R601 22.6/F USBRBIAS
Boot BIOS Strap
		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff
ICH_SPI_CS1#_R PCI_GNT0# R280 *1K_NC R287 *1K_NC
PCI Pullups
RP25 RP31 +3.3V_RUN
WWAN Noise - ICH improvements
*0.1U_NC
RP37 10KX8 +3.3V_SUS
R300 R304 10K
BIOS should not enable the internal GPIO pull up resistor.
SB_WPAN_PCIE_RST# R286 20K
SB_WWAN_PCIE_RST# R281 20K
SB_WLAN_PCIE_RST# R292 20K
SB_LOM_PCIE_RST# R266 20K
SB_NB_PCIE_RST# R276 20K
U35B
PCI
Interrupt I/F
ICH9M REV 1.0
CLK_PCI_ICH R270 *10_NC C371 *8.2P_NC
Reserved for EMI.Place resister and cap close to ICH.
PCI_GNT3# R285 *1K_NC
A16 away override strap.
SB_NB_PCIE_RST# Low = A16 swap override enabled. High = Default.
Non-iAMT
Add Buffers as needed for Loading and fanout concerns.
C432 0.047U U21 TC7SZ32FU(T5L,F,T) PCI_RST#
C344 0.047U U18 TC7SZ32FU(T5L,F,T) PLTRST#
QUANTA COMPUTER
Title ICH9-M (USB,DMI,PCIE,PCI)
Size Document Number FM7 Rev 1A
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2/13-5 2/18-19

+3.3V_SUS

Non-iAMT

RP23

ICH_SMBCLK

ICH_SMBDATA

2.2KX2

2/13-5 2/18-19

Non-iAMT

+3.3V_SUS

ASF 2.0

RP24

ICH_SMLINK0

ICH_SMLINK1

*10KX2_NC

Non-iAMT

+3.3V_SUS

R252 *10K_NC RSV_ICH_CL_RST1#

R274 10K ICH_RI#

R253 10K SIO_EXT_SCI#

R279 1K PCIE_WAKE#

ICH_SMBCLK R250 0 ICH_SMLINK0

ICH_SMBDATA R251 0 ICH_SMLINK1

+3.3V_RUN

R283 8.2K

CLKRUN#

R282 *10_NC

Option to " Disable " clkrun. Pulling it down will keep the clks running.

U35C

30,33,34 ICH_SMBCLK

30,33,34 ICH_SMBDATA

T52 PAD

T59 PAD

T54 PAD

ICH_SMBCLK G16

ICH_SMBDATA A13

RSV_ICH_CL_RST1# E17

ICH_SMLINK0 C17

ICH_SMLINK1 B18

ICH_RI# F19

T88 PAD

RSV_LPCPD# R4

3 ITP_DBRESET# G19

6 PM_BMBUSY# M6

34 USB_MCARD1_DET# USB_MCARD1_DET# A17

17 H_STP_PCI# A14

17 H_STP_CPU# E19

28,31 CLKRUN# CLKRUN# L4

30,33,34,42 PCIE_WAKE# PCIE_WAKE# E20

28,31 IRQ_SERIRQ IRQ_SERIRQ M5

39 THERM_ALERT# THERM_ALERT# AJ23

31,44,51 IMVP_PWRGD IMVP_PWRGD D21

T53 PAD A20

TP8

SMBCLK

SMBDATA

LINKALERT#/GPIO60/CLGPIO3

SMLINK0

SMLINK1

RI#

SUS_STAT#/LPCPD#

SYS_RESET#

PMSYNC#/GPIO0

SMBALERT#/GPIO11

STP_PCI#/GPIO15

STP_CPU#/GPIO25

CLKRUN#/GPIO32

WAKE#

SERIRQ

THRM#

VRMPWRGD

SMB

SATA GPIO

Clocks

SYS GPIO

Power MGT

SATA0GP/GPIO21 AH23

SATA1GP/GPIO19 AE19

SATA4GP/GPIO36 AE21

SATA5GP/GPIO37 AD20

CLK14 H1 CLK_ICH_14M CLK_ICH_14M 17

CLK48 AF3 CLK_ICH_48M CLK_ICH_48M 17

SUSCLK P1 ICH_SUSCLK PAD T133

SLP_S3# C16 SIO_SLP_S3# 31

SLP_S4# E16 PAD T78

SLP_S5# G17 SIO_SLP_S5# 31

S4_STATE#/GPIO26 C10

PWROK G20 ICH_PWRGD ICH_PWRGD 6,44

DPRSLPVR DPRSLPVR 6,51

DPRSLPVR/GPIO16 M2

BATLOW# B13 ICH_BATLOW#

PWRBTN# R3 SIO_PWRBTN# 31

LAN_RST# D20 RSV_ICH_LAN_RST# PAD T70

RSMRST# D22 ICH_RSMRST# ICH_RSMRST# 31

CK_PWRGD R5 CLK_PWRGD 17

CLPWROK R6 ICH_CL_PWROK ICH_CL_PWROK 6,31

SLP_M# B16 PAD T57

CL_CLK0 F24

CL_CLK1 B19 RSV_ICH_CL_CLK1 PAD T76

CL_DATA0 F22 CL_DATA0 6

CL_DATA1 C19 RSV_ICH_CL_DATA1 PAD T58

CL_VREF0 C25 CL_VREF0

CL_VREF1 A19 CL_VREF1

CL_RST0# F21 ICH_CL_RST0# 6

CL_RST1# D18 CL_RST1# PAD T79

MEM_LED/GPIO24 A16 RSV_GPIO24 PAD T61

ALERT#/GPIO10 C18 RSV_GPIO10 PAD T65

NETDETECT/GPIO14 C11 RSV_GPIO14 PAD T62

WOL_EN/GPIO9 C20 RSV_WOL_EN PAD T56

R264 8.2K

+3.3V_SUS

+3.3V_RUN

R328 8.2K

R580 8.2K

+3.3V_SUS

2/13-5

Non-iAMT

Place these close to ICH8.

CLK_ICH_48M

R321 *10_NC

C454 *4.7P_NC

50

CLK_ICH_14M

R590 *10_NC

C780 *4.7P_NC

50

2/13-5

ICH_PWRGD R291 10K

DPRSLPVR R594 100K

ICH_RSMRST# R277 10K

RSV_ICH_LAN_RST# R268 10K

ICH_CL_PWROK R303 1M

+3.3V_SUS

RSV_GPIO10 R249 10K

2/25-29 6/11-53

37 KB_LED_DET#

34 PCIE_MCARD1_DET#

R319 0

PCIE_MCARD1_DET# R288 4.7K

T127 PAD

33 USB_MCARD2_DET# USB_MCARD2_DET# AG19

33 USB_MCARD3_DET# USB_MCARD3_DET# AH21

31 SIO_EXT_WAKE# AG21

31 SIO_EXT_SMI# SIO_EXT_SMI# A21

31 SIO_EXT_SCI# SIO_EXT_SCI# C12

C21

AE18

K1

33 PCIE_MCARD2_DET# PCIE_MCARD2_DET# AF8

33 PCIE_MCARD3_DET# PCIE_MCARD3_DET# AJ22

34 WLAN_RADIO_DIS# A9

41 CAMERA_CBL_DET# D19

17 SATA_CLKREQ# L1

18 PLTRST_DELAY# PLTRST_DELAY# AE19

33 WPAN_RADIO_DIS_MINI# AG22

33 WWAN_RADIO_DIS# AF21

T138 PAD AH24

T125 PAD A8

GPIO

Controller Link

TACH1/GPIO1

TACH2/GPIO6

TACH3/GPIO7

GPIO8

LANPHYPC/GPIO12

ENGDET/GPIO13

TACH0/GPIO17

GPIO18

GPIO20

SCLOCK/GPIO22

QRT_STATE0/GPIO27

QRT_STATE1/GPIO28

SATACLKREQ#/GPIO35

SLOAD/GPIO38

SDATAOUT0/GPIO39

SDATAOUT1/GPIO48

GPIO49

GPIO57/CLGPIO5

40 SPKR SPKR M7

6 MCH_ICH_SYNC# MCH_ICH_SYNC# R AJ24

11 ICH_RSVD B21

T136 PAD TP9 AH20

T137 PAD TP10 AJ20

T139 PAD TP11 AJ21

SPKR

MCH_ICH_SYNC#

TP3

TP9

TP10

TP11

MISC

ICH9M REV 1.0

Non-iAMT

+3.3V_RUN

+3.3V_ALV +3.3V_SUS

R263 3.24K/F

R575 *3.24K/F_NC

R576 *3.24K/F_NC

CL_VREF0

CL_VREF1

C359 0.1U

R256 453/F

C771 *0.1U_NC

R578 *453/F_NC

10

10

CL_VREF0/1 ~=0.405V

DIS:ALW

UMA:SUS (19)

R323 10K PLTRST_DELAY#

7/30-68

+3.3V_RUN

R247 1.91K/F IMVP_PWRGD

R329 100K USB_MCARD2_DET#

R626 100K USB_MCARD3_DET#

R289 100K PCIE_MCARD1_DET#

R324 100K PCIE_MCARD2_DET#

R635 100K PCIE_MCARD3_DET#

+3.3V_RUN

R624 *10K_NC MCH_ICH_SYNC# R

R296 10K IRQ_SERIRQ

R625 10K THERM_ALERT#

+3.3V_SUS

R257 10K RSV_WOL_EN

R574 10K SIO_EXT_SMI#

R579 100K USB_MCARD1_DET#

+3.3V_RUN

R293 *1K_NC

SPKR

No Reboot strap.

SPKR	Low = Default. High = No Reboot.

SMbus address D2

These are for backdrive issue.

Non-iAMT

+3.3V_RUN

RP17 2.2KX2

30,33,34 ICH_SMBDATA

Q31

2N7002W-7-F

MEM_SDATA 15

+3.3V_RUN

30,33,34 ICH_SMBCLK

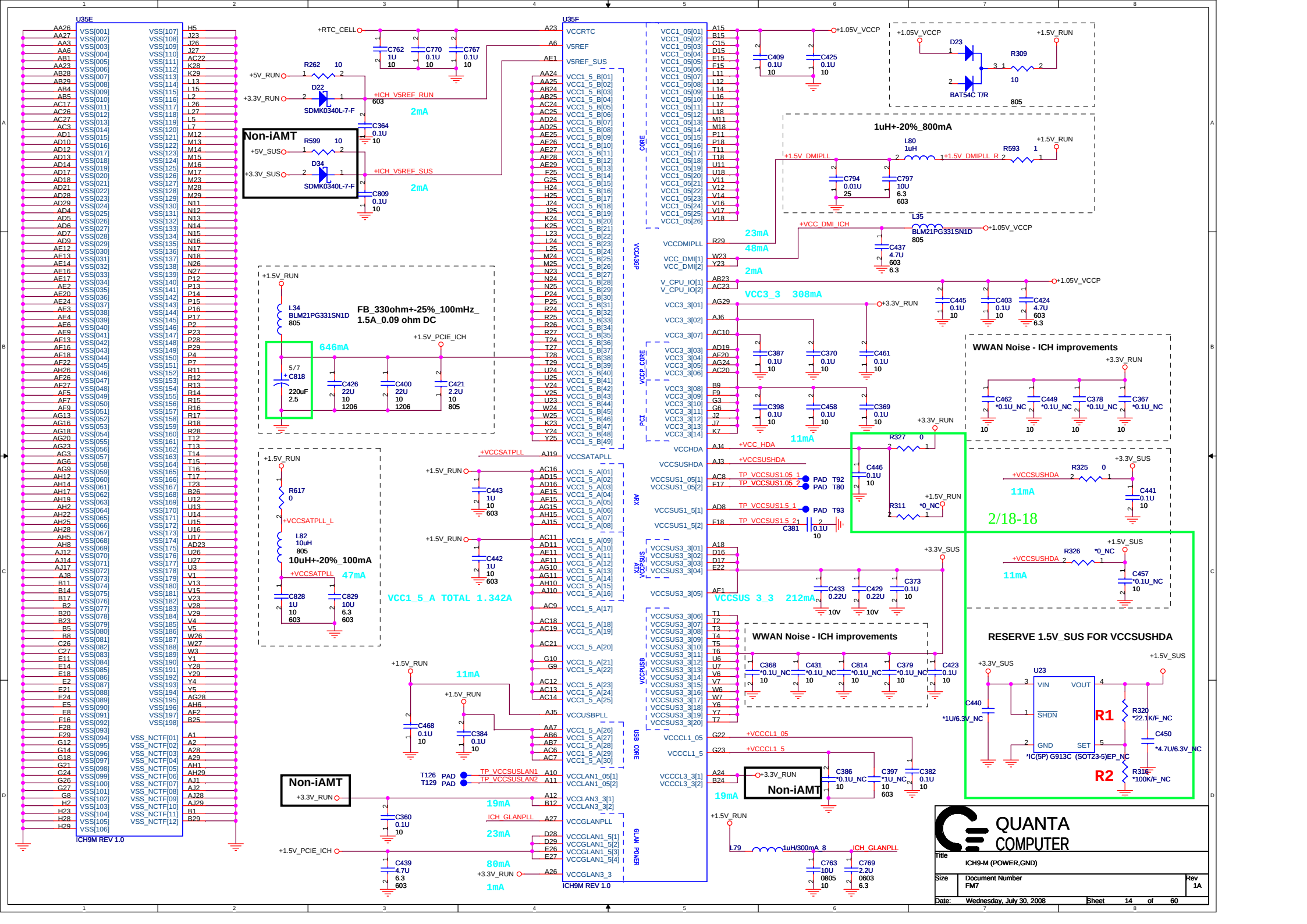
Q32

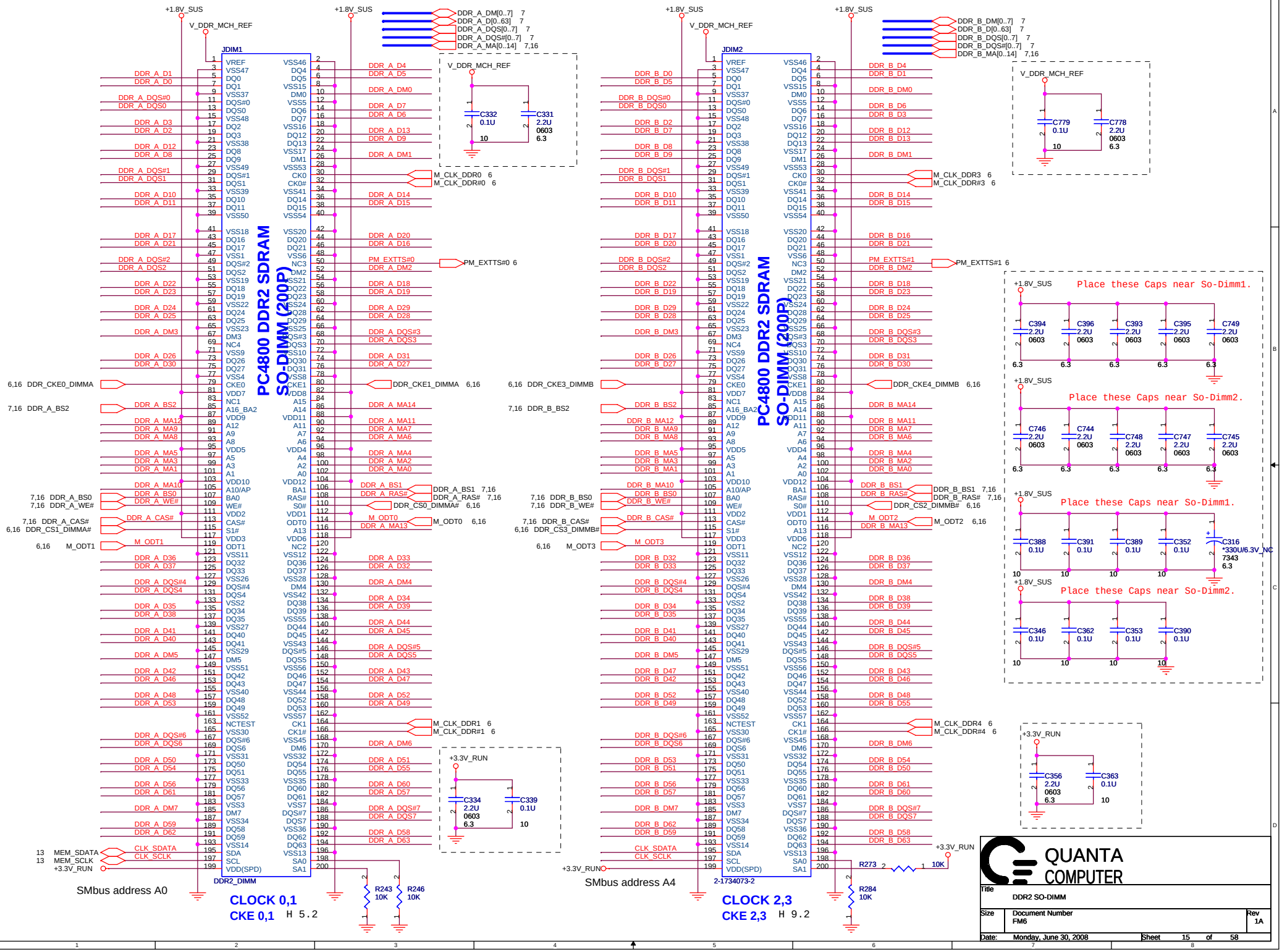
2N7002W-7-F

MEM_SCLK 15

QUANTA COMPUTER

Title	ICH9-M (PM,GPIO,SMB,CL)	
Size	Document Number FM7	Rev 1A
Date: Wednesday, July 30, 2008	Sheet 13 of 60	


U35E
ICH9M REV 1.0
U35F
ICH9M REV 1.0
Non-iAMT
Non-iAMT
Non-iAMT
FB_330ohm+-25%_100mHz_
1.5A_0.09 ohm DC
10uH+-20%_100mA
1uH+-20%_800mA
WWAN Noise - ICH improvements
WWAN Noise - ICH improvements
RESERVE 1.5V_SUS FOR VCCSUSHDA
VCC1_5_A TOTAL 1.342A
VCCSUS 3_3 212mA
VCC3_3 308mA
2/18-18
QUANTA COMPUTER
ICH9-M (POWER,GND)
Document Number FM7
Rev 1A
Wednesday, July 30, 2008
Sheet 14 of 60


JDIM1
PC4800 DDR2 SDRAM
SO-DIMM (200P)
DDR2_DIMM
SMbus address A0
CLOCK 0,1
CKE 0,1 H 5.2
JDIM2
PC4800 DDR2 SDRAM
SO-DIMM (200P)
2-1734073-2
SMbus address A4
CLOCK 2,3
CKE 2,3 H 9.2
Place these Caps near So-Dimm1.
Place these Caps near So-Dimm2.
Place these Caps near So-Dimm1.
Place these Caps near So-Dimm2.
QUANTA COMPUTER
DDR2 SO-DIMM
FM6
1A
Monday, June 30, 2008
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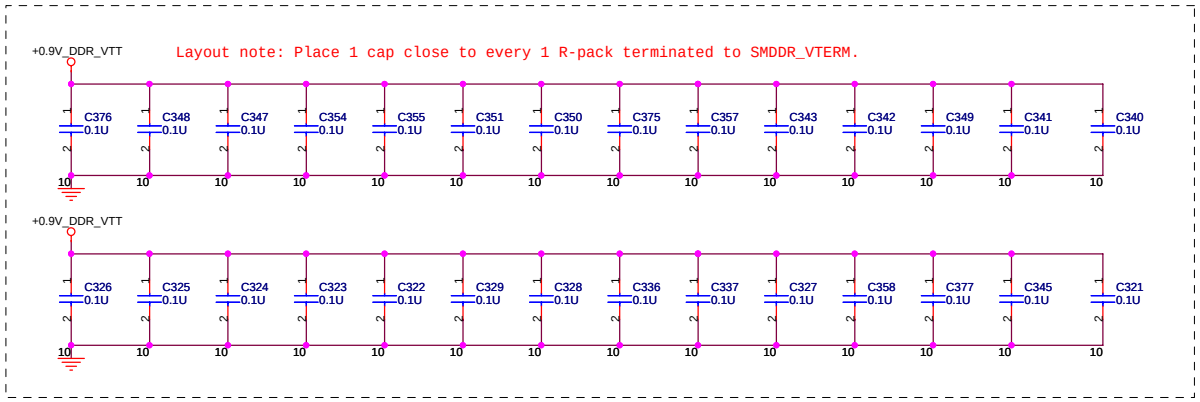

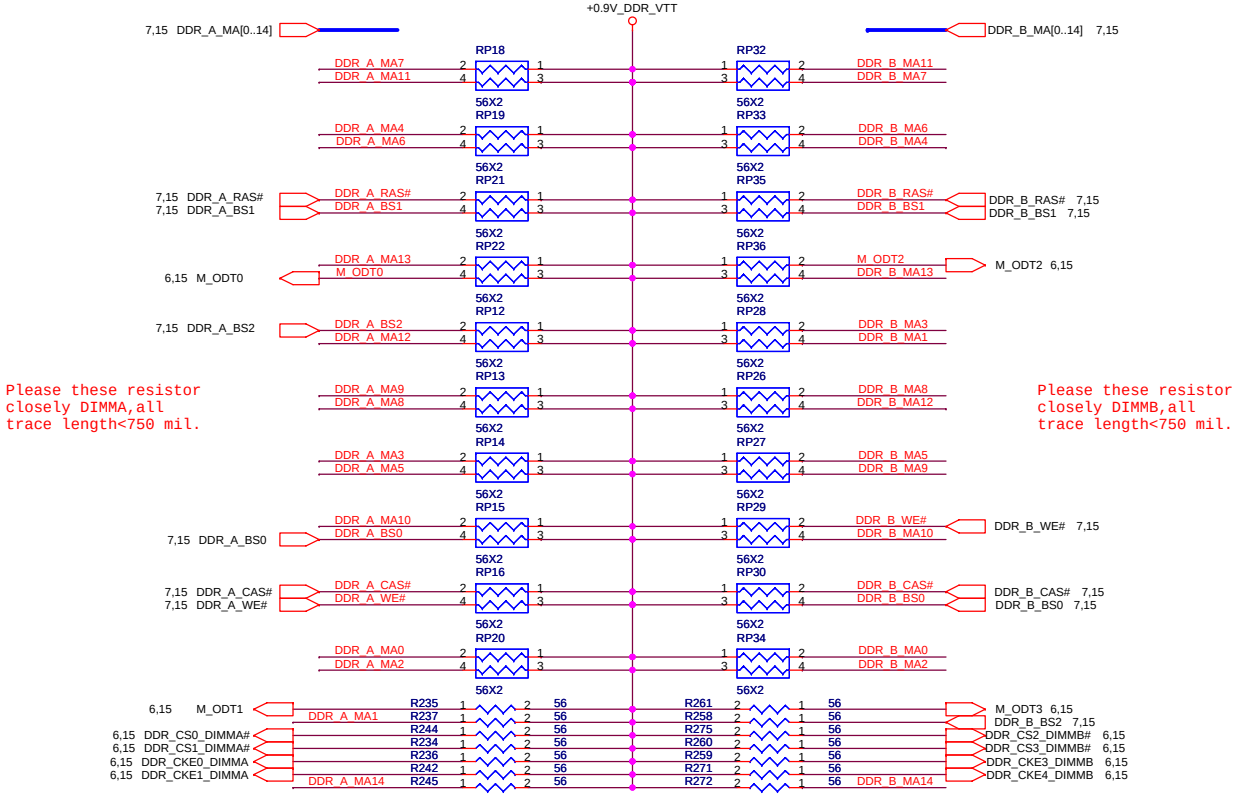

QUANTA COMPUTER

Title	DDR2 RES. ARRAY	
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Add capacitor pads for improving WWAN.

C694 20P 50 CLK_ICH_48M
C666 *27P_NC 50 CLK_ICH_14M
C679 *27P_NC 50 CLK_PCI_8512
C272 *27P_NC 50 CLK_PCI_PCCARD
C689 *27P_NC 50 CLK_PCI_ICH

Y3
CLK_XTAL_IN — 14.318MHZ — CLK_XTAL_OUT
C653 33P 50
C652 33P 50
14.318MHz

U31
CK505
QFN64
SLG8SP513V

+CK_VDD_PCI 9 VDD_PCI
4 VDD_REF
+CK_VDD_PLL3 23 VDD_PLL3
+CK_VDD_48 16 VDD_48
+CK_VDD_SRC 46 VDD_SRC
62 VDD_CPU
+CK_VDD_MAIN 19 VDD_IO
27 VDD_IO
33 VDD_IO
43 VDD_IO
52 VDD_IO
56 VDD_IO
15 GND
18 GND
22 GND
26 GND
30 GND
36 GND
49 GND
59 GND
1 GND
8 CR#_A/PCI-0
10 CR_B/PCI-1
11 TME/PCI-2
12 SRC5_EN/PCI-3
13 27M_SEL/PCI-4
14 ITP_EN/PCIF-5#
17 FSA/USB48
64 FSB/TEST_MODE
5 FSC/TEST_SEL/REF
55 RESET#
63 CK_PWRGD/PD#
2 XOUT
3 XIN
6 SDATA
7 SCLK
65 GND

CPU-0 61 CPU_BCLK — RP40 0x2 — CLK_CPU_BCLK 3
CPU-0# 60 CPU_BCLK# — CLK_CPU_BCLK# 3
CPU-1 58 MCH_BCLK — RP39 0x2 — CLK_MCH_BCLK 5
CPU-1# 57 MCH_BCLK# — CLK_MCH_BCLK# 5
SRC-8/CPU_ITP 54 PCIE_MINI1 — RP38 0x2 — CLK_PCIE_MINI1 34
SRC-8#/CPU_ITP# 53 PCIE_MINI1# — CLK_PCIE_MINI1# 34
SRC-0/DOT96 20 DOT96_SSC — RP9 0x2 — CLK_PCIE_VGA 18
SRC-0#/DOT96# 21 DOT96_SSC# — CLK_PCIE_VGA# 18
SRC-1/SE1 24 27M_NSS — R510 33 — CLK_VGA_27M_NSS 19
SRC-1#/SE2 25 27M_SS — R509 *33_NC — CLK_VGA_27M_SS 19
SRC-2/SATA 28 PCIE_SATA — RP10 0x2 — CLK_PCIE_SATA 11
SRC-2#/SATA# 29 PCIE_SATA# — CLK_PCIE_SATA# 11
CR#_C/SRC-3 31 PCIE_MINI3 — RP45 0x2 — CLK_PCIE_MINI3 33
CR#_D/SRC-3# 32 PCIE_MINI3# — CLK_PCIE_MINI3# 33
SRC-4 34 MCH_3GPLL — RP44 0x2 — CLK_MCH_3GPLL 6
SRC-4# 35 MCH_3GPLL# — CLK_MCH_3GPLL# 6
PCI_STOP#/SRC-5 45 — H_STP_PCI# 13
CPU_STOP#/SRC5-5# 44 — H_STP_CPU# 13
SRC-6 48 PCIE_EXPCARD — RP41 0x2 — CLK_PCIE_EXPCARD 30
SRC-6# 47 PCIE_EXPCARD# — CLK_PCIE_EXPCARD# 30
CR#_F/SRC-7 51 MINI1CLK_REQ# C — R464 475/F — MINI1CLK_REQ# — MINI1CLK_REQ# 34
CR#_E/SRC-7# 50 CARD_CLK_REQ# C — R466 475/F — CARD_CLK_REQ# — CARD_CLK_REQ# 30
SRC-9 37 PCIE_MINI2 — RP43 0x2 — CLK_PCIE_MINI2 33
SRC-9# 38 PCIE_MINI2# — CLK_PCIE_MINI2# 33
SRC-10 41 PCIE_ICH — RP42 0x2 — CLK_PCIE_ICH 12
SRC-10# 42 PCIE_ICH# — CLK_PCIE_ICH# 12
CR#_H/SRC-11 40 PCIE_LOM — RP8 0x2 — CLK_PCIE_LOM 42
CR#_G/SRC-11# 39 PCIE_LOM# — CLK_PCIE_LOM# 42

2/20-21
2/21-24

Only for debug
7/30-70

13 SATA_CLKREQ# — SATA_CLKREQ# — R487 475/F
6 CLK_3GPLLREQ# — CLK_3GPLLREQ# — R489 475/F
33 CLK_LPC_DEBUG — CLK_LPC_DEBUG — R189 *22_NC
28 CLK_PCI_PCCARD — CLK_PCI_PCCARD — R190 33
31 CLK_PCI_8512 — CLK_PCI_8512 — R492 33
12 CLK_PCI_ICH — CLK_PCI_ICH — R499 33
13 CLK_ICH_48M — CLK_ICH_48M — R508 33
3,6 CPU_MCH_BSEL0 — L73 BLM18AG601SN1D — R507 2.2K — FSA
3,6 CPU_MCH_BSEL1 — R471 0 — FSB
3,6 CPU_MCH_BSEL2 — L65 BLM18AG601SN1D — R477 10K — FSC
13 CLK_ICH_14M — CLK_ICH_14M — R481 33
13 CLK_PWRGD

SATA_CLKREQ# C
CLK_3GPLLREQ# C
PCI_PCCARD
PCI_SIO
27M_SEL
PCI_ICH

2/13-6

CLK_XTAL_OUT
CLK_XTAL_IN
CLK_SDATA
CLK_SCLK

+3.3V_RUN
H_STP_PCI# R167 10K
H_STP_CPU# R174 10K

+3.3V_RUN
CLK_3GPLLREQ# R490 10K
SATA_CLKREQ# R488 10K
CARD_CLK_REQ# R469 10K
MINI1CLK_REQ# R463 10K
PCI_PCCARD R188 *10K_NC

PCI_SIO R493 *10K_NC
PCI_ICH R501 *10K_NC

3 CLK_ITP_BCLK — RP6 *0x2_NC — PCIE_MINI1
3 CLK_ITP_BCLK# — PCIE_MINI1#

+3.3V_RUN
R198 *10K_NC
PCI_ICH
R200 *10K_NC

R188 POP: For Internal pull-low.
R191 POP: For internal pull-high.

+3.3V_RUN
R495 10K
27M_SEL
R497 *10K_NC

UMA without iAMT

+3.3V_RUN
L71 BLM21PG600SN1D 0805 120 ohms@100Mhz
+CK_VDD_MAIN
C693 0.1U 10
C692 0.1U 10
C691 0.1U 10
C661 0.1U 10
C642 0.1U 10
C641 0.1U 10
C690 *10U_NC 0603 6.3

L72 BLM21PG600SN1D 0805 120 ohms@100Mhz
R474 2.2
+CK_VDD_PCI
C662 0.1U 10
C269 0.1U 10
2/19-20

R506 2.2
+CK_VDD_PLL3
C695 0.1U 10

R504 2.2
+CK_VDD_48
C687 0.1U 10
C688 4.7U 0603 6.3

R162 2.2
+CK_VDD_SRC
C659 0.1U 10
C254 0.1U 10
2/19-20

Non-iAMT

SMbus address D2

These are for backdrive issue.

+3.3V_RUN
RP7 2.2KX2
26,31,39 SMBDAT1 — Q26 2N7002W-7-F — CLK_SDATA
+3.3V_RUN
26,31,39 SMBCLK1 — Q28 2N7002W-7-F — CLK_SCLK

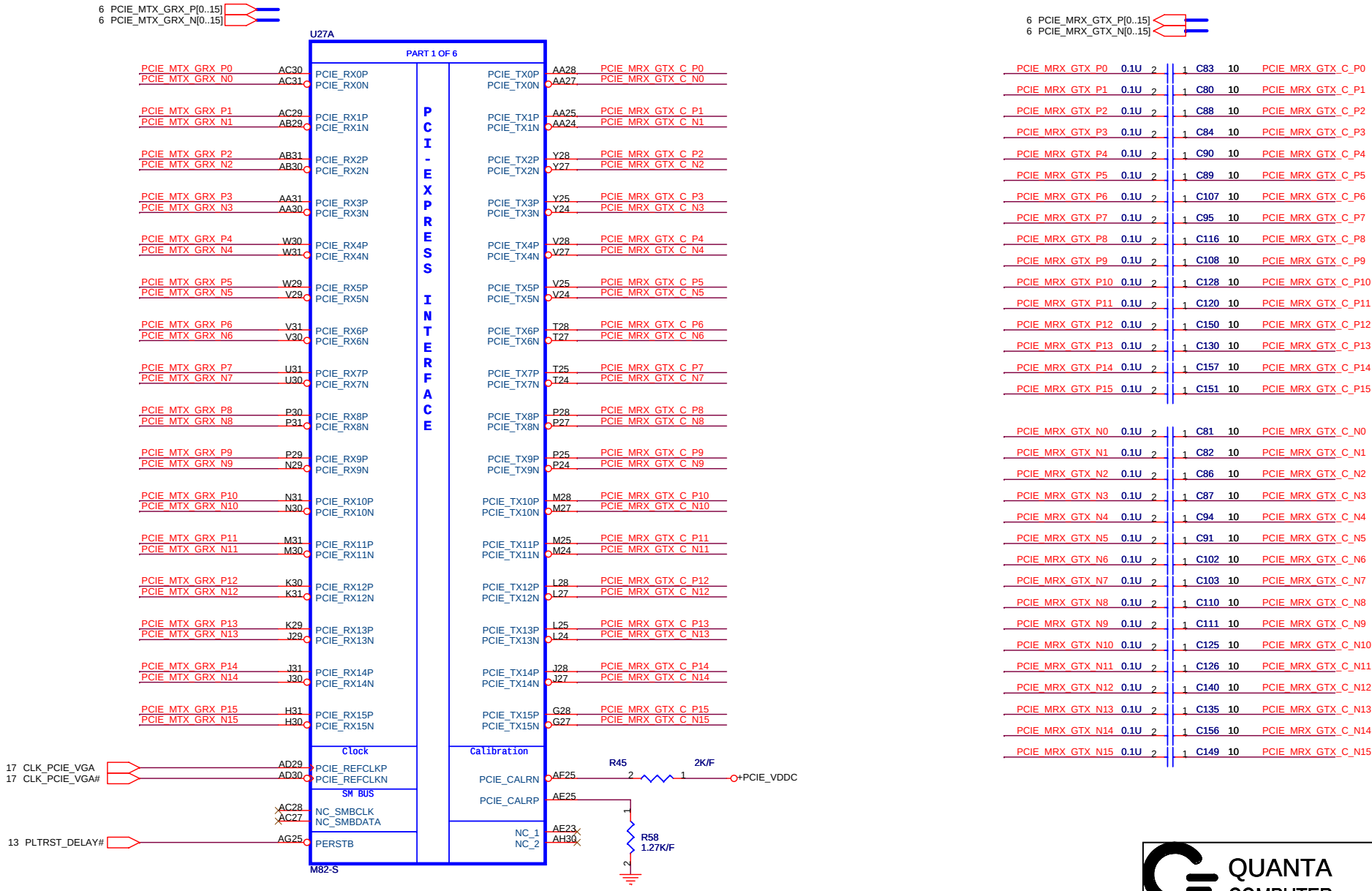
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL

27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

QUANTA COMPUTER

Title	CLOCK GENERATOR	
Size	Document Number FM6	Rev 2A
Date: Wednesday, July 30, 2008	Sheet 17 of 58	


6 PCIE_MTX_GRX_P[0..15]
6 PCIE_MTX_GRX_N[0..15]
U27A
PART 1 OF 6
PCI-EXPRESS INTERFACE
PCIE_MTX_GRX_P0 AC30 PCIE_RX0P
PCIE_MTX_GRX_N0 AC31 PCIE_RX0N
PCIE_MTX_GRX_P1 AC29 PCIE_RX1P
PCIE_MTX_GRX_N1 AB29 PCIE_RX1N
PCIE_MTX_GRX_P2 AB31 PCIE_RX2P
PCIE_MTX_GRX_N2 AB30 PCIE_RX2N
PCIE_MTX_GRX_P3 AA31 PCIE_RX3P
PCIE_MTX_GRX_N3 AA30 PCIE_RX3N
PCIE_MTX_GRX_P4 W30 PCIE_RX4P
PCIE_MTX_GRX_N4 W31 PCIE_RX4N
PCIE_MTX_GRX_P5 W29 PCIE_RX5P
PCIE_MTX_GRX_N5 V29 PCIE_RX5N
PCIE_MTX_GRX_P6 V31 PCIE_RX6P
PCIE_MTX_GRX_N6 V30 PCIE_RX6N
PCIE_MTX_GRX_P7 U31 PCIE_RX7P
PCIE_MTX_GRX_N7 U30 PCIE_RX7N
PCIE_MTX_GRX_P8 P30 PCIE_RX8P
PCIE_MTX_GRX_N8 P31 PCIE_RX8N
PCIE_MTX_GRX_P9 P29 PCIE_RX9P
PCIE_MTX_GRX_N9 N29 PCIE_RX9N
PCIE_MTX_GRX_P10 N31 PCIE_RX10P
PCIE_MTX_GRX_N10 N30 PCIE_RX10N
PCIE_MTX_GRX_P11 M31 PCIE_RX11P
PCIE_MTX_GRX_N11 M30 PCIE_RX11N
PCIE_MTX_GRX_P12 K30 PCIE_RX12P
PCIE_MTX_GRX_N12 K31 PCIE_RX12N
PCIE_MTX_GRX_P13 K29 PCIE_RX13P
PCIE_MTX_GRX_N13 J29 PCIE_RX13N
PCIE_MTX_GRX_P14 J31 PCIE_RX14P
PCIE_MTX_GRX_N14 J30 PCIE_RX14N
PCIE_MTX_GRX_P15 H31 PCIE_RX15P
PCIE_MTX_GRX_N15 H30 PCIE_RX15N
PCIE_TX0P AA28 PCIE_MRX_GTX_C_P0
PCIE_TX0N AA27 PCIE_MRX_GTX_C_N0
PCIE_TX1P AA25 PCIE_MRX_GTX_C_P1
PCIE_TX1N AA24 PCIE_MRX_GTX_C_N1
PCIE_TX2P Y28 PCIE_MRX_GTX_C_P2
PCIE_TX2N Y27 PCIE_MRX_GTX_C_N2
PCIE_TX3P Y25 PCIE_MRX_GTX_C_P3
PCIE_TX3N Y24 PCIE_MRX_GTX_C_N3
PCIE_TX4P V28 PCIE_MRX_GTX_C_P4
PCIE_TX4N V27 PCIE_MRX_GTX_C_N4
PCIE_TX5P V25 PCIE_MRX_GTX_C_P5
PCIE_TX5N V24 PCIE_MRX_GTX_C_N5
PCIE_TX6P T28 PCIE_MRX_GTX_C_P6
PCIE_TX6N T27 PCIE_MRX_GTX_C_N6
PCIE_TX7P T25 PCIE_MRX_GTX_C_P7
PCIE_TX7N T24 PCIE_MRX_GTX_C_N7
PCIE_TX8P P28 PCIE_MRX_GTX_C_P8
PCIE_TX8N P27 PCIE_MRX_GTX_C_N8
PCIE_TX9P P25 PCIE_MRX_GTX_C_P9
PCIE_TX9N P24 PCIE_MRX_GTX_C_N9
PCIE_TX10P M28 PCIE_MRX_GTX_C_P10
PCIE_TX10N M27 PCIE_MRX_GTX_C_N10
PCIE_TX11P M25 PCIE_MRX_GTX_C_P11
PCIE_TX11N M24 PCIE_MRX_GTX_C_N11
PCIE_TX12P L28 PCIE_MRX_GTX_C_P12
PCIE_TX12N L27 PCIE_MRX_GTX_C_N12
PCIE_TX13P L25 PCIE_MRX_GTX_C_P13
PCIE_TX13N L24 PCIE_MRX_GTX_C_N13
PCIE_TX14P J28 PCIE_MRX_GTX_C_P14
PCIE_TX14N J27 PCIE_MRX_GTX_C_N14
PCIE_TX15P G28 PCIE_MRX_GTX_C_P15
PCIE_TX15N G27 PCIE_MRX_GTX_C_N15
Clock
17 CLK_PCIE_VGA AD29 PCIE_REFCLKP
17 CLK_PCIE_VGA# AD30 PCIE_REFCLKN
SM BUS
AC28 NC_SMBCLK
AC27 NC_SMBDATA
13 PLTRST_DELAY# AG25 PERSTB
Calibration
PCIE_CALRN AF25
PCIE_CALRP AE25
NC_1 AE23
NC_2 AH30
R45 2K/F
+PCIE_VDDC
R58 1.27K/F
M82-S
6 PCIE_MRX_GTX_P[0..15]
6 PCIE_MRX_GTX_N[0..15]
PCIE_MRX_GTX_P0 0.1U C83 10 PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1 0.1U C80 10 PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2 0.1U C88 10 PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3 0.1U C84 10 PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4 0.1U C90 10 PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5 0.1U C89 10 PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6 0.1U C107 10 PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7 0.1U C95 10 PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8 0.1U C116 10 PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9 0.1U C108 10 PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10 0.1U C128 10 PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11 0.1U C120 10 PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12 0.1U C150 10 PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13 0.1U C130 10 PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14 0.1U C157 10 PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15 0.1U C151 10 PCIE_MRX_GTX_C_P15
PCIE_MRX_GTX_N0 0.1U C81 10 PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1 0.1U C82 10 PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2 0.1U C86 10 PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3 0.1U C87 10 PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4 0.1U C94 10 PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5 0.1U C91 10 PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6 0.1U C102 10 PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7 0.1U C103 10 PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8 0.1U C110 10 PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9 0.1U C111 10 PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10 0.1U C125 10 PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11 0.1U C126 10 PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12 0.1U C140 10 PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13 0.1U C135 10 PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14 0.1U C156 10 PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15 0.1U C149 10 PCIE_MRX_GTX_C_N15
QUANTA COMPUTER
Title
VGA-M82-S (PCIe)
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MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	X	0	0	0
256MB	X	0	0	1
64MB	X	0	1	0
512MB	X	1	0	0

Memory Straps	RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0
400MHz 256MB(32M*16) Samsung	0	0	1	0
400MHz 256MB(32M*16) Hynix	0	0	1	1
500MHz 256MB(32M*16) Samsung	0	1	1	0
500MHz 256MB(32M*16) Qimonda	0	1	0	0

+3.3V_DELAY

R431 10K RAM_CFG0
R432 *10K_NC RAM_CFG1
R433 *10K_NC RAM_CFG2
R96 *10K_NC RAM_CFG3

+1.8V_RUN

R401 *10K_NC RAM_TYPE_CFG0
R402 *10K_NC RAM_TYPE_CFG1
R403 10K RAM_TYPE_CFG2
R400 *10K_NC RAM_TYPE_CFG3

GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	ATI Usage	FM6 Usage
GPIO0	PCIE FULL TX OUTPUT SWING	X	1
GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	1
GPIO2	ATI reserved configuration straps.	RSVD	0
GPIO3	ATI reserved configuration straps.	RSVD	0
GPIO4	DEBUG SIGNALS MUXED OUT	0	0
GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
GPIO6	ATI Internal use only	0	0
GPIO10	Serial ROM clock to ROM.		0
ATI Usage recommended settings	0= DO NOT INSTALL RESISTOR, X = DESIGN DEPENDANT, RSVD = ATI RESERVED (DO NOT INSTALL)		

+3.3V_DELAY

R80 10K GPIO0
R420 10K GPIO1
R424 *10K_NC GPIO2
R79 *10K_NC GPIO3
R425 *10K_NC GPIO4
R423 *10K_NC GPIO5
R101 *10K_NC GPIO6
R430 *10K_NC GPIO10

R97 10K HDMI_HD_EN
R102 *10K_NC TEMP_FAIL#
R78 10K GFX_CLKREQ#
R410 10K VGAHSYNC

R84 10K TEMP_FAIL#

U27B
PART 2 OF 6
M82-S

INTEGRATED TMDS/DP PORT
EXT TMDS DVO
GENERAL PURPOSE I/O
DAC1 / CRT
DAC2 (TV/CRT2)
SERIAL BUSES
PLL & XTAL
TEST
THERMAL

AJ4 TXCM_DPA0P
AJ5 TXCP_DPA0N
AL5 TX0M_DPA1P
AK5 TX0P_DPA1N
AL6 TX1M_DPA2P
AK6 TX1P_DPA2N
AK8 TX2M_DPA3P
AL8 TX2P_DPA3N
AD9 DVALID
AE7 PSYNC_NEW
AK4 DVPCNTL_MVP_0
AL3 DVPCNTL_MVP_1
V2 DVPCNTL_0
V1 DVPCNTL_1
W3 DVPCNTL_2
W1 DVPCLK
Y1 DVPDATA_0
Y2 DVPDATA_1
Y3 DVPDATA_2
AA2 DVPDATA_3
AA3 DVPDATA_4
AB1 DVPDATA_5
AB2 DVPDATA_6
AB3 DVPDATA_7
AC1 DVPDATA_8
AC3 DVPDATA_9
AD1 DVPDATA_10
AD2 DVPDATA_11
AD3 DVPDATA_12
AE3 DVPDATA_13
AG3 DVPDATA_14
AH3 DVPDATA_15
AG1 DVPDATA_16
AH2 DVPDATA_17
AH1 DVPDATA_18
AJ3 DVPDATA_19
AJ1 DVPDATA_20
AJ2 DVPDATA_21
AK2 DVPDATA_22
AK3 DVPDATA_23
Y4 GPIO_0
V3 GPIO_1
V4 GPIO_2
V5 GPIO_3
U3 GPIO_4
U2 GPIO_5
T4 GPIO_6
T5 GPIO_7_BLON
T7 GPIO_8_ROMSO
T8 GPIO_9_ROMSI
R1 GPIO_10_ROMSCK
R2 GPIO_11
R3 GPIO_12
P1 GPIO_13
P3 GPIO_14_HPD2
N1 GPIO_15_PWRCNTL0
N2 GPIO_16_SSIN
P4 GPIO_17_THERMAL_INT
P7 GPIO_18_HPD3
P8 GPIO_19_CTF
P5 GPIO_20_PWRCNTL1
V7 GPIO_21_BB_EN
N3 GPIO_22_ROMCSB
Y5 GPIO_23_CLKREQB
M4 GPIO_24_JMODE
M5 GPIO_25_TDI
M7 GPIO_26_TCK
M8 GPIO_27_TMS
L8 GPIO_28_TDO
Y8 GEN_A
Y7 GEN_B
V8 GEN_C
AH6 GEN_D_HPD4
AG6 GEN_E
AC11 VREFG
AH12 DPLL_PVDD
AG12 DPLL_PVSS
AH31 PCIE_PVDD
A9 MPVDD
B9 MPVSS
AE12 DPLL_VDDC
AJ31 XTALIN
AJ30 XTALOUT
AH26 TESTEN
AD12 PLLTEST
AK9 TXCM_DPB0P
AL9 TXCP_DPB0N
AJ9 TX0M_DPB1P
AJ10 TX0P_DPB1N
AL10 TX1M_DPB2P
AK10 TX1P_DPB2N
AL11 TX2M_DPB3P
AK11 TX2P_DPB3N
AL7 DPA_PVDD
AK7 DPA_PVSS
AE11 DPB_PVDD
AE11 DPB_PVSS
AJ12 DPA_VDDR_1
AJ13 DPA_VDDR_2
AK13 DPB_VDDR_1
AL13 DPB_VDDR_2
AL12 DPB_VSSR_5
AK12 DPB_VSSR_4
AJ11 DPB_VSSR_3
AH9 DPB_VSSR_2
AH11 DPB_VSSR_1
AJ8 DPA_VSSR_5
AE7 DPA_VSSR_4
AG7 DPA_VSSR_3
AJ7 DPA_VSSR_2
AH7 DPA_VSSR_1
AG11 DP_CALR
AA8 HPD1
AL28 R
AK28 RB
AL27 G
AK27 GB
AL26 B
AK26 BB
AK29 HSYNC
AK30 VSYNC
AJ28 RSET
AL29 AVDD
AH28 AVSSQ
AJ27 VDD1DI
AJ26 VSS1DI
AL17 R2
AK17 R2B
AL15 G2
AK15 G2B
AL14 B2
AK14 B2B
AJ17 C
AJ15 Y
AJ14 COMP
AE16 V2SYNC
AE16 H2SYNC
AH14 A2VDD
AH16 A2VDDQ
AG16 A2VSSQ
AF18 VDD2DI
AE18 VSS2DI
AG14 R2SET
AA5 SCL
AA4 SDA
AJ29 DDC1DATA
AH29 DDC1CLK
AC5 DDC2DATA
AC4 DDC2CLK
AF4 DDC3DATA_DP3_AUXN
AH4 DDC3CLK_DP3_AUXP
AF9 DDC4DATA_DP4_AUXN
AG9 DDC4CLK_DP4_AUXP
AE14 TS_FDO
AE5 DPLUS
AE4 DMINUS

+TPVDD
+DPA_VDDR
+DPB_VDDR
VIP_3
R413 0
R73 150
VGA_RED 27
VGA_GRN 27
VGA_BLU 27
VGAHSYNC
VGAVSYNC 27
R59 499/F
+AVDD
+VDD1D_2D
+A2VDD
+A2VDDQ
R404 715/F
LCD_DDCDAT
LCD_DDCCLK
HDMI_SDA 26
HDMI_SCL 26
G_DAT_DDC2 27
G_CLK_DDC2 27
R61 0
R60 0
VGA_THERMDP 22
VGA_THERMDN 22

HDMI_CLK- 26
HDMI_CLK+ 26
HDMI_TX0- 26
HDMI_TX0+ 26
HDMI_TX1- 26
HDMI_TX1+ 26
HDMI_TX2- 26
HDMI_TX2+ 26

LVDS
HDMI
CRT

+3.3V_DELAY
R76 10K
R82 10K
Q19 MMST3904-7-F
Q41 DTC114TUAT106
R373 100K
HDMI_DET 26

2/13-9
3/28-36

VGA_BLU
VGA_GRN
VGA_RED
R406 150/F
R407 150/F
R408 150/F

DIS only
Layout Note:
Place 150 ohm termination resistors close to ATI CHIP.

2/25-28

1108.21

+3.3V_DELAY
LCD_DDCDAT R397 2.2K
LCD_DDCCLK R396 2.2K

31 PANEL_BKEN
50 GFX_CORE_CNTRL0
22 THERMAL_INT#
20 TEMP_FAIL#
50 GFX_CORE_CNTRL1
20 BB_ENA
CLK_VGA_27M_SSIN_R
R105 *0_NC
T17 PAD
T101 PAD
T104 PAD
GFX_CLKREQ#
R438 1K
T18 PAD
T25 PAD
T19 PAD
T20 PAD
T15 PAD
T14 PAD
T16 PAD
T8 PAD
T9 PAD

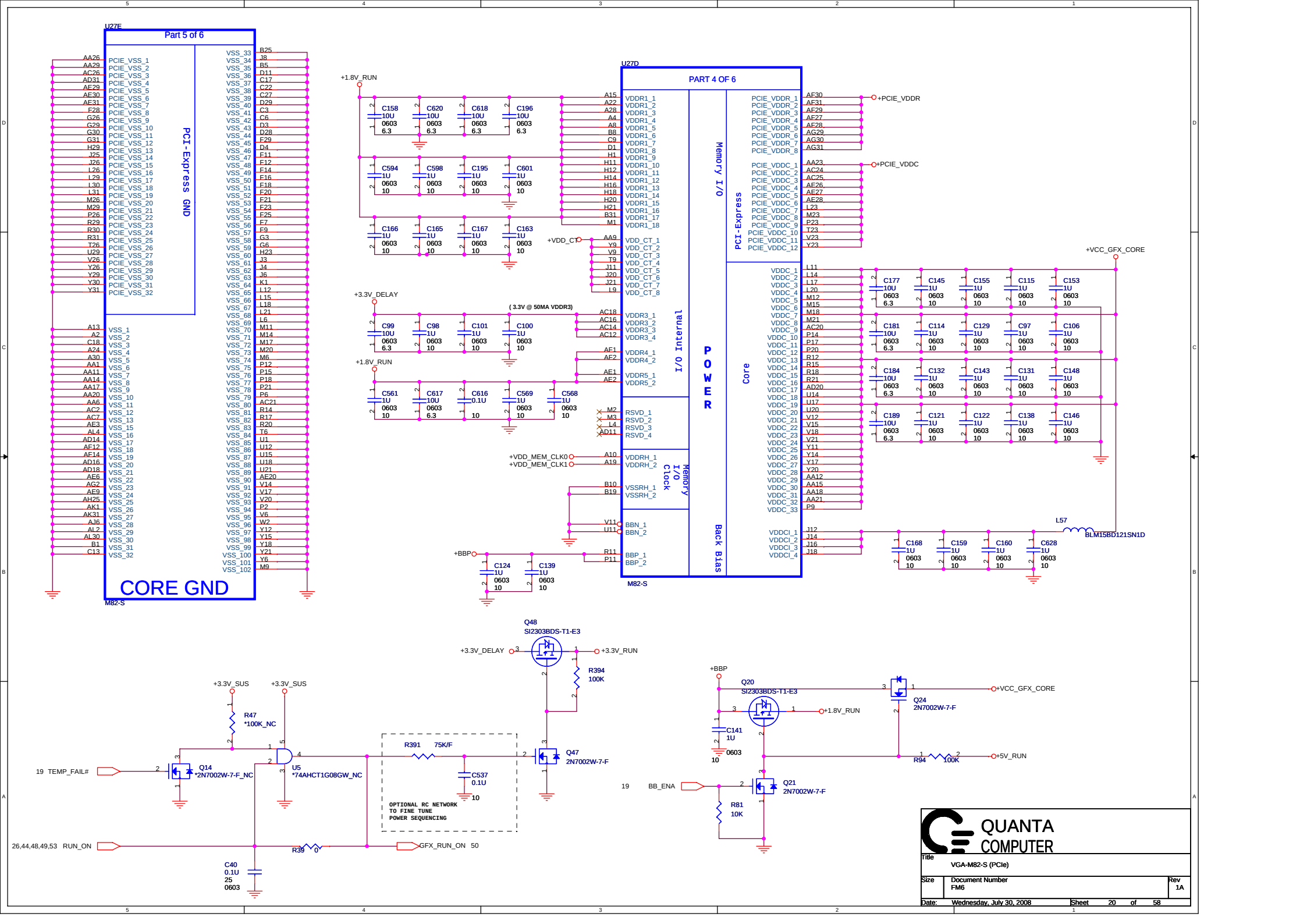
+1.8V_RUN
R75 499/F
R74 249/F
C93 0.1U
10

22 OSC_SPREAD
17 CLK_VGA_27M_SS
17 CLK_VGA_27M_NSS
22 OSC_OUT
R389 *0_NC
R398 *0_NC
R399 100/F
R412 120/F
R411 0
R393 *10K_NC
R388 *0_NC
R387 *0_NC
Y2 *27MHZ_NC
R390 1M_NC
C524 *18P_NC
C520 *18P_NC
50
50

+DPLL_PVDD
+PCIE_PVDD
+MPVDD
+DPLL_VDDC
XTAIN
XTAOUT
R46 1K

QUANTA COMPUTER

Title	VGA-G86GLM (VIDEO)	
Size	Document Number FM6	Rev 2A
Date: Monday, June 30, 2008	Sheet 19 of 58	


U27E
Part 5 of 6
PCI Express GND
PCIE_VSS_1
PCIE_VSS_2
PCIE_VSS_3
PCIE_VSS_4
PCIE_VSS_5
PCIE_VSS_6
PCIE_VSS_7
PCIE_VSS_8
PCIE_VSS_9
PCIE_VSS_10
PCIE_VSS_11
PCIE_VSS_12
PCIE_VSS_13
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PCIE_VSS_23
PCIE_VSS_24
PCIE_VSS_25
PCIE_VSS_26
PCIE_VSS_27
PCIE_VSS_28
PCIE_VSS_29
PCIE_VSS_30
PCIE_VSS_31
PCIE_VSS_32
VSS_1
VSS_2
VSS_3
VSS_4
VSS_5
VSS_6
VSS_7
VSS_8
VSS_9
VSS_10
VSS_11
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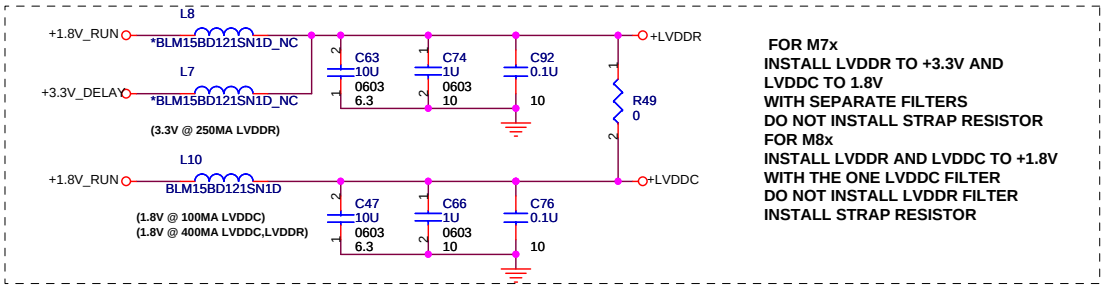
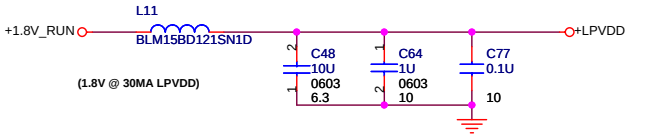
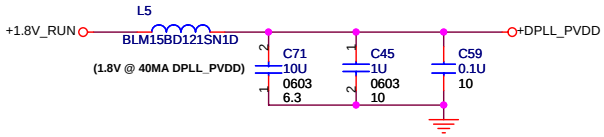
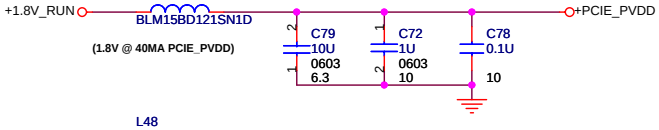
VSS_95
VSS_96
VSS_97
VSS_98
VSS_99
VSS_100
VSS_101
VSS_102
CORE GND
M82-S
U27D
PART 4 OF 6
Memory I/O
PCI-Express
I/O Internal
POWER
Core
Memory I/O Clock
Back Bias
VDDR1_1
VDDR1_2
VDDR1_3
VDDR1_4
VDDR1_5
VDDR1_6
VDDR1_7
VDDR1_8
VDDR1_9
VDDR1_10
VDDR1_11
VDDR1_12
VDDR1_13
VDDR1_14
VDDR1_15
VDDR1_16
VDDR1_17
VDDR1_18
VDD_CT_1
VDD_CT_2
VDD_CT_3
VDD_CT_4
VDD_CT_5
VDD_CT_6
VDD_CT_7
VDD_CT_8
VDDR3_1
VDDR3_2
VDDR3_3
VDDR3_4
VDDR4_1
VDDR4_2
VDDR5_1
VDDR5_2
RSVD_1
RSVD_2
RSVD_3
RSVD_4
VDDRH_1
VDDRH_2
VSSRH_1
VSSRH_2
BBN_1
BBN_2
BBP_1
BBP_2
PCIE_VDDR_1
PCIE_VDDR_2
PCIE_VDDR_3
PCIE_VDDR_4
PCIE_VDDR_5
PCIE_VDDR_6
PCIE_VDDR_7
PCIE_VDDR_8
PCIE_VDDC_1
PCIE_VDDC_2
PCIE_VDDC_3
PCIE_VDDC_4
PCIE_VDDC_5
PCIE_VDDC_6
PCIE_VDDC_7
PCIE_VDDC_8
PCIE_VDDC_9
PCIE_VDDC_10
PCIE_VDDC_11
PCIE_VDDC_12
VDDC_1
VDDC_2
VDDC_3
VDDC_4
VDDC_5
VDDC_6
VDDC_7
VDDC_8
VDDC_9
VDDC_10
VDDC_11
VDDC_12
VDDC_13
VDDC_14
VDDC_15
VDDC_16
VDDC_17
VDDC_18
VDDC_19
VDDC_20
VDDC_21
VDDC_22
VDDC_23
VDDC_24
VDDC_25
VDDC_26
VDDC_27
VDDC_28
VDDC_29
VDDC_30
VDDC_31
VDDC_32
VDDC_33
VDDCI_1
VDDCI_2
VDDCI_3
VDDCI_4
M82-S
+1.8V_RUN
+3.3V_DELAY
+VDD_CT
+VDD_MEM_CLK0
+VDD_MEM_CLK1
+BBP
+PCIE_VDDR
+PCIE_VDDC
+VCC_GFX_CORE
(3.3V @ 50MA VDDR3)
C158 10U 0603 6.3
C620 10U 0603 6.3
C618 10U 0603 6.3
C196 10U 0603 6.3
C594 1U 0603 10
C598 1U 0603 10
C195 1U 0603 10
C601 1U 0603 10
C166 1U 0603 10
C165 1U 0603 10
C167 1U 0603 10
C163 1U 0603 10
C99 10U 0603 6.3
C98 1U 0603 10
C101 1U 0603 10
C100 1U 0603 10
C561 1U 0603 10
C617 10U 0603 6.3
C616 0.1U 0603 10
C569 1U 0603 10
C568 1U 0603 10
C124 1U 0603 10
C139 1U 0603 10
C177 10U 0603 6.3
C145 1U 0603 10
C155 1U 0603 10
C115 1U 0603 10
C153 1U 0603 10
C181 10U 0603 6.3
C114 1U 0603 10
C129 1U 0603 10
C97 1U 0603 10
C106 1U 0603 10
C184 10U 0603 6.3
C132 1U 0603 10
C143 1U 0603 10
C131 1U 0603 10
C148 1U 0603 10
C189 10U 0603 6.3
C121 1U 0603 10
C122 1U 0603 10
C138 1U 0603 10
C146 1U 0603 10
C168 1U 0603 10
C159 1U 0603 10
C160 1U 0603 10
C628 1U 0603 10
L57
BLM15BD121SN1D
Q48
SI2303BDS-T1-E3
R394 100K
Q47 2N7002W-7-F
R391 75K/F
C537 0.1U 10
OPTIONAL RC NETWORK TO FINE TUNE POWER SEQUENCING
+3.3V_SUS
R47 *100K_NC
Q14 *2N7002W-7-F_NC
U5 *74AHCT1G08GW_NC
19 TEMP_FAIL#
26,44,48,49,53 RUN_ON
R39 0
GFX_RUN_ON 50
C40 0.1U 25 0603
Q20
SI2303BDS-T1-E3
Q24 2N7002W-7-F
C141 1U 0603 10
R94 100K
+5V_RUN
19 BB_ENA
Q21 2N7002W-7-F
R81 10K
QUANTA COMPUTER
Title
VGA-M82-S (PCIe)
Size
Document Number
FM6
Rev
1A
Date: Wednesday, July 30, 2008
Sheet 20 of 58

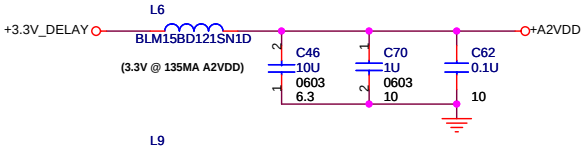


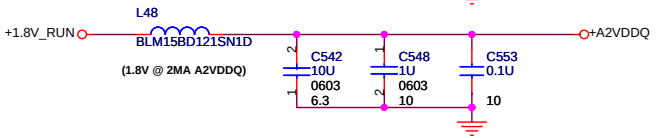
FOR M7x
INSTALL LVDDR TO +3.3V AND
LVDDC TO 1.8V
WITH SEPARATE FILTERS
DO NOT INSTALL STRAP RESISTOR
FOR M8x
INSTALL LVDDR AND LVDDC TO +1.8V
WITH THE ONE LVDDC FILTER
DO NOT INSTALL LVDDR FILTER
INSTALL STRAP RESISTOR

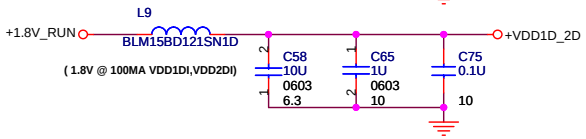


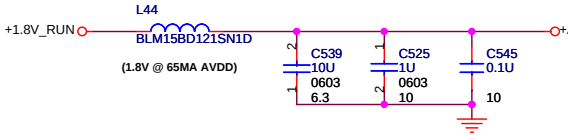


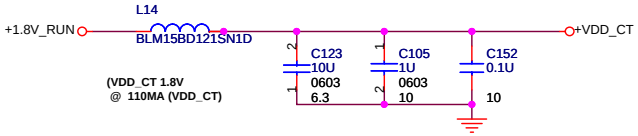


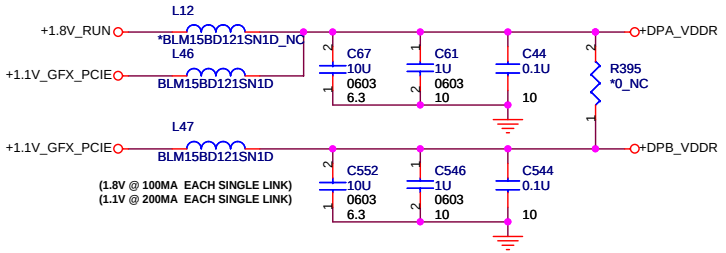






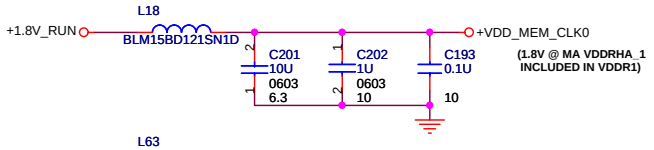


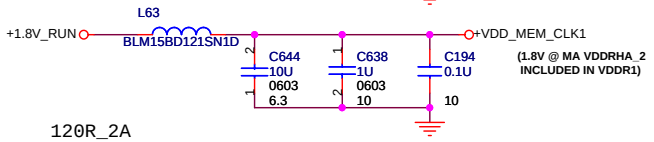




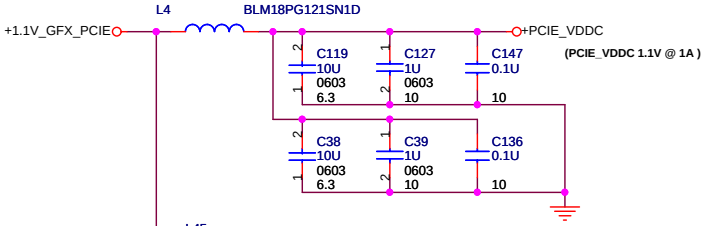
FOR M8x
INSTALL DPA_VDDR TO +1.1V AND
DPB_VDDR TO +1.1V
WITH SEPARATE FILTERS
DO NOT INSTALL STRAP RESISTOR
FOR M7x
INSTALL DPA_VDDR AND DPB_VDDR TO +1.8V
WITH THE ONE DPA_VDDR FILTER
DO NOT INSTALL DPB_VDDR FILTER
INSTALL STRAP RESISTOR

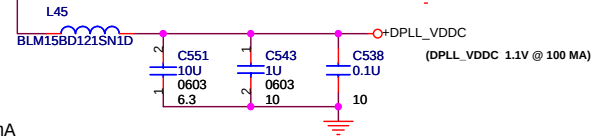
PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE



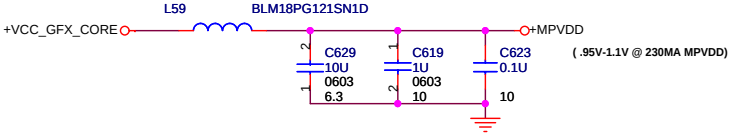


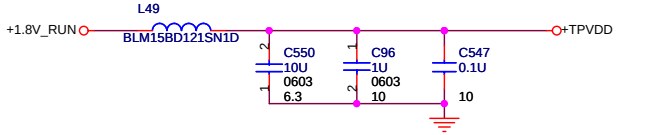
120R_2A





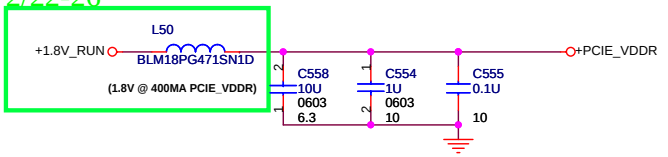
120R_450mA





2/22-26

(1.8V@ 20mA for Single link and 40mA for Dual-Link)



QUANTA COMPUTER

Title	VGA-M82-S (PCIe)	
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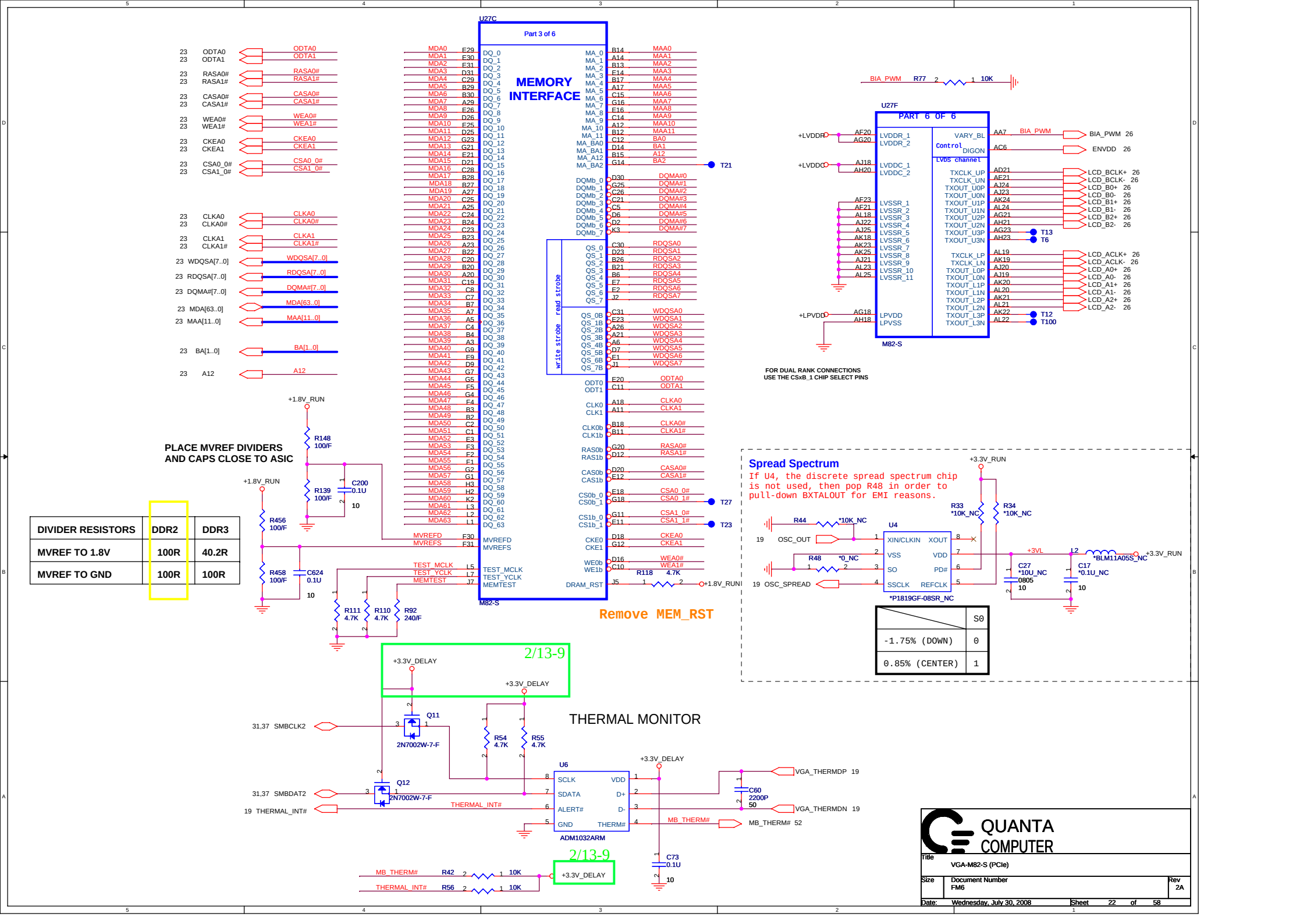
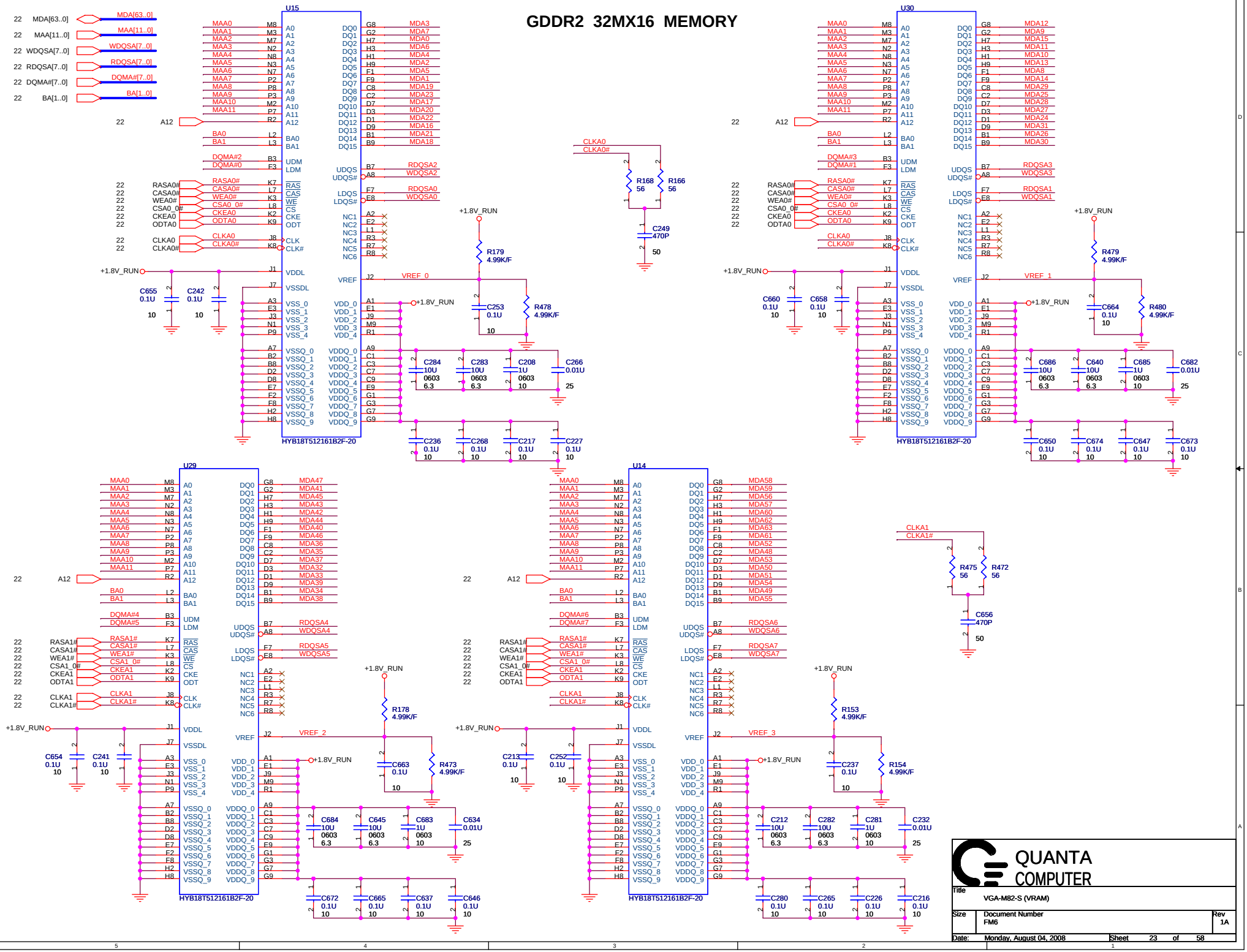

MEMORY INTERFACE
Part 3 of 6
M82-S
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC
DIVIDER RESISTORS | DDR2 | DDR3
MVREF TO 1.8V | 100R | 40.2R
MVREF TO GND | 100R | 100R
Remove MEM_RST
THERMAL MONITOR
ADM1032ARM
2N7002W-7-F
PART 6 OF 6
FOR DUAL RANK CONNECTIONS USE THE CSxB_1 CHIP SELECT PINS
Spread Spectrum
If U4, the discrete spread spectrum chip is not used, then pop R48 in order to pull-down BXTALOUT for EMI reasons.
*P1819GF-08SR_NC
-1.75% (DOWN) 0
0.85% (CENTER) 1
QUANTA COMPUTER
VGA-M82-S (PCIe)
FM6
Wednesday, July 30, 2008

GDDR2 32MX16 MEMORY



QUANTA COMPUTER

Title	VGA-M82-S (VRAM)	
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GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	ATI Usage	FM6 Usage
GPIO0	PCIE FULL TX OUTPUT SWING	X	1
GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	1
GPIO2	ATI reserved configuration straps.	RSVD	0
GPIO3	ATI reserved configuration straps.	RSVD	0
GPIO4	DEBUG SIGNALS MUXED OUT	0	0
GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
GPIO6	ATI Internal use only	0	0
GPIO10	Serial ROM clock to ROM.		0
ATI Usage recommended settings	0= DO NOT INSTALL RESISTOR, X = DESIGN DEPENDANT, RSVD = ATI RESERVED (DO NOT INSTALL)		

QUANTA COMPUTER

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Title	VGA-M82-S (PCIe)	
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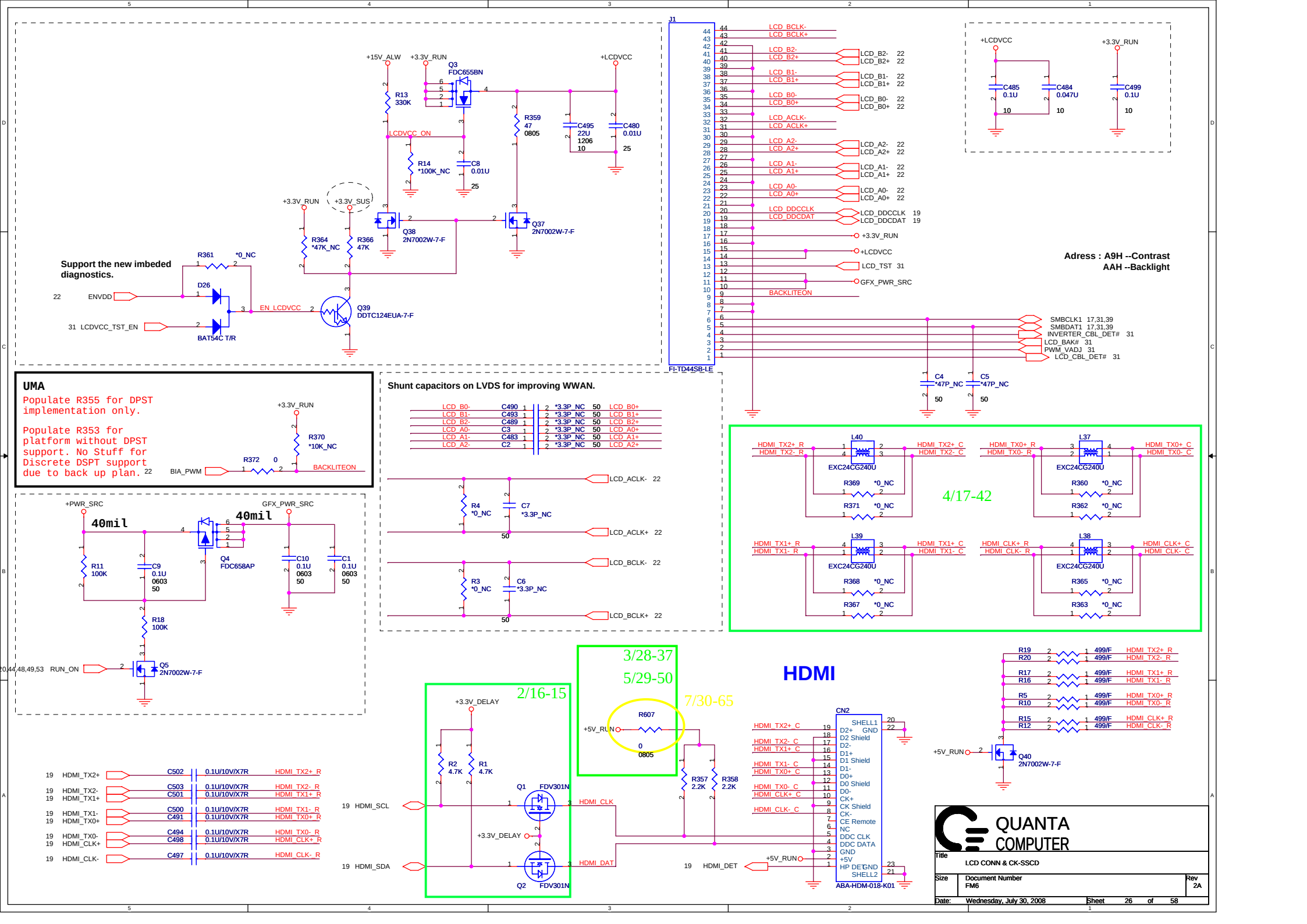
Support the new imbeded diagnostics.
ENVDD
LCDVCC_TST_EN
EN_LCDVCC
BAT54C T/R
Q39 DDTC124EUA-7-F
Q38 2N7002W-7-F
Q37 2N7002W-7-F
Q3 FDC655BN
LCDVCC_ON
+15V_ALW
+3.3V_RUN
+3.3V_SUS
+LCDVCC
J1
FI-TD44SB-LE
LCD_BCLK-
LCD_BCLK+
LCD_B2-
LCD_B2+
LCD_B1-
LCD_B1+
LCD_B0-
LCD_B0+
LCD_ACLK-
LCD_ACLK+
LCD_A2-
LCD_A2+
LCD_A1-
LCD_A1+
LCD_A0-
LCD_A0+
LCD_DDCCLK
LCD_DDCDAT
LCD_TST
GFX_PWR_SRC
BACKLITEON
SMBCLK1 17,31,39
SMBDAT1 17,31,39
INVERTER_CBL_DET# 31
LCD_BAK# 31
PWM_VADJ 31
LCD_CBL_DET# 31
Adress : A9H --Contrast
AAH --Backlight
UMA
Populate R355 for DPST implementation only.
Populate R353 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.
BIA_PWM
BACKLITEON
Shunt capacitors on LVDS for improving WWAN.
LCD_ACLK-
LCD_ACLK+
LCD_BCLK-
LCD_BCLK+
HDMI_TX2+_R
HDMI_TX2-_R
HDMI_TX0+_R
HDMI_TX0-_R
HDMI_TX1+_R
HDMI_TX1-_R
HDMI_CLK+_R
HDMI_CLK-_R
EXC24CG240U
4/17-42
+PWR_SRC
GFX_PWR_SRC
40mil
Q4 FDC658AP
RUN_ON
Q5 2N7002W-7-F
2/16-15
3/28-37
5/29-50
7/30-65
+3.3V_DELAY
+5V_RUN
Q1 FDV301N
Q2 FDV301N
HDMI_SCL
HDMI_SDA
HDMI_CLK
HDMI_DAT
HDMI_DET
HDMI
CN2
ABA-HDM-018-K01
Q40 2N7002W-7-F
QUANTA COMPUTER
Title
LCD CONN & CK-SSCD
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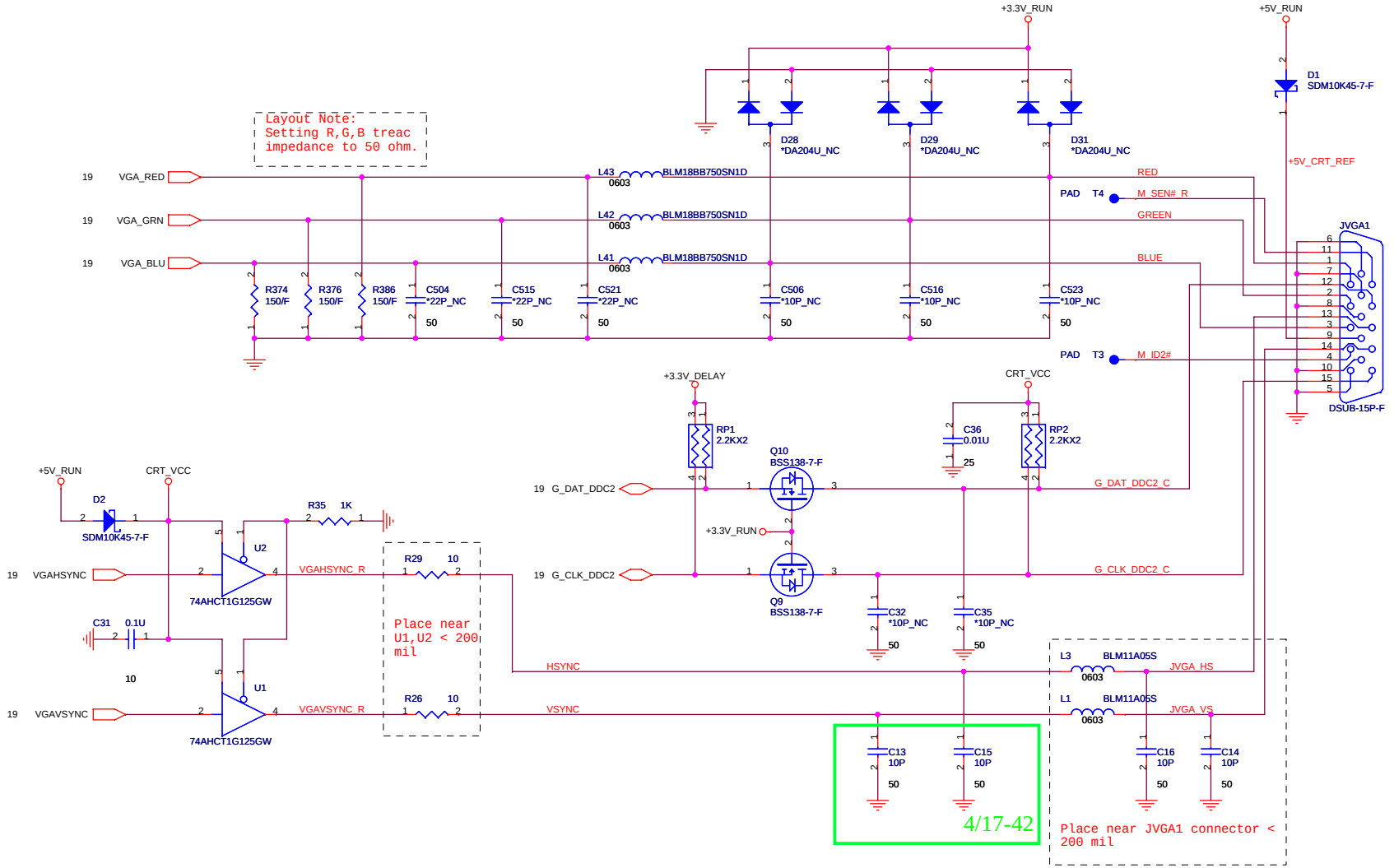

QUANTA COMPUTER

Title	CRT&TV CONN	
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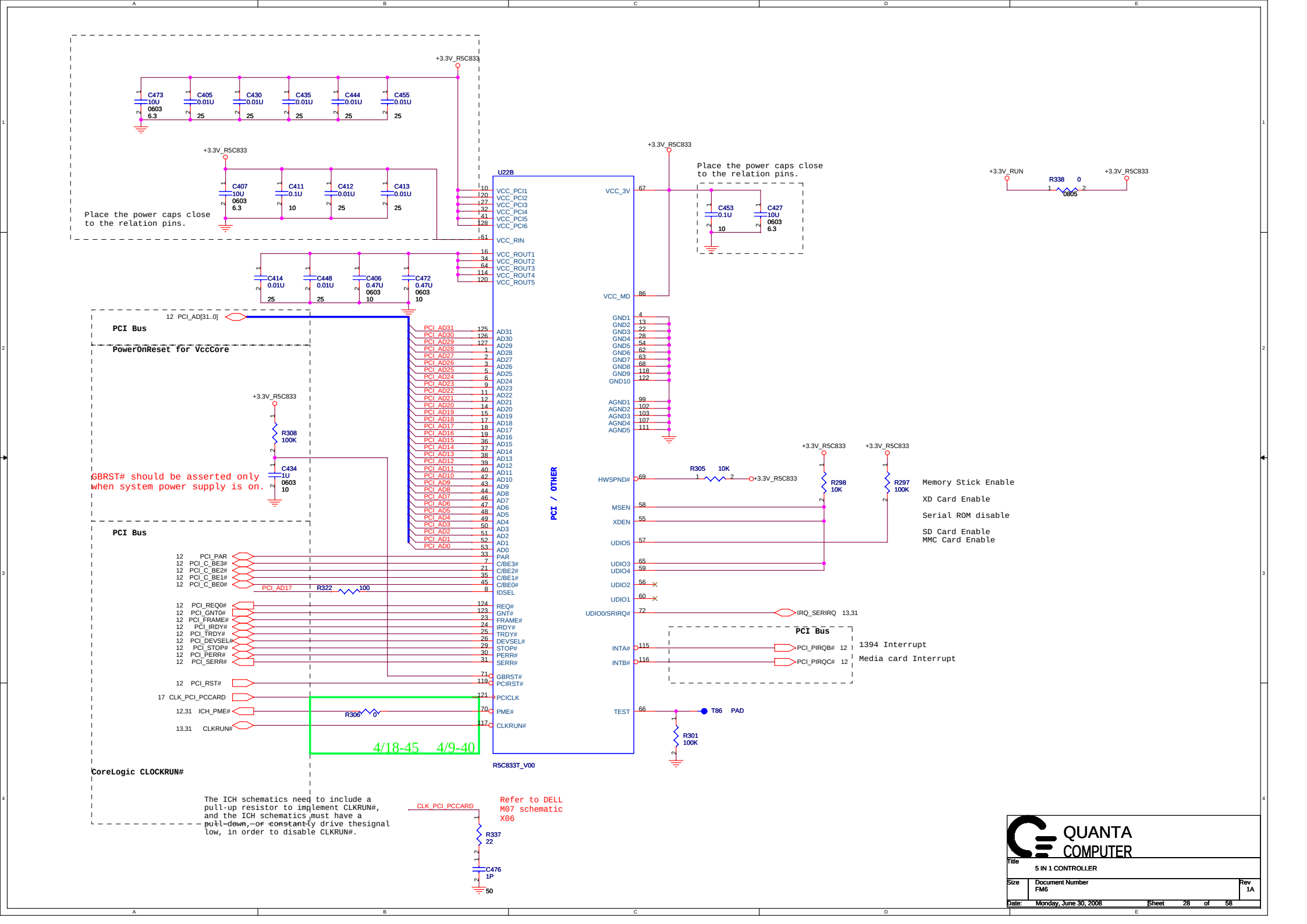
+3.3V_R5C833
C473 10U 0603 6.3
C405 0.01U 25
C430 0.01U 25
C435 0.01U 25
C444 0.01U 25
C455 0.01U 25
Place the power caps close to the relation pins.
C407 10U 0603 6.3
C411 0.1U 10
C412 0.01U 25
C413 0.01U 25
C414 0.01U 25
C448 0.01U 25
C406 0.47U 0603 10
C472 0.47U 0603 10
U22B
VCC_PCI1
VCC_PCI2
VCC_PCI3
VCC_PCI4
VCC_PCI5
VCC_PCI6
VCC_RIN
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5
VCC_3V
VCC_MD
C453 0.1U 10
C427 10U 0603 6.3
Place the power caps close to the relation pins.
+3.3V_RUN
R338 0 0805
+3.3V_R5C833
12 PCI_AD[31..0]
PCI Bus
PowerOnReset for VccCore
R308 100K
C434 1U 0603 10
GBRST# should be asserted only when system power supply is on.
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
PAR
C/BE3#
C/BE2#
C/BE1#
C/BE0#
IDSEL
PCI / OTHER
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
AGND1
AGND2
AGND3
AGND4
AGND5
HWSPND#
R305 10K
MSEN
XDEN
UDIO5
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SRIRQ#
IRQ_SERIRQ 13,31
R298 10K
R297 100K
Memory Stick Enable
XD Card Enable
Serial ROM disable
SD Card Enable
MMC Card Enable
PCI Bus
INTA#
INTB#
PCI_PIRQB# 12
PCI_PIRQC# 12
1394 Interrupt
Media card Interrupt
12 PCI_PAR
12 PCI_C_BE3#
12 PCI_C_BE2#
12 PCI_C_BE1#
12 PCI_C_BE0#
PCI_AD17
R322 100
12 PCI_REQ0#
12 PCI_GNT0#
12 PCI_FRAME#
12 PCI_IRDY#
12 PCI_TRDY#
12 PCI_DEVSEL#
12 PCI_STOP#
12 PCI_PERR#
12 PCI_SERR#
REQ#
GNT#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PERR#
SERR#
12 PCI_RST#
GBRST#
PCIRST#
17 CLK_PCI_PCCARD
PCICLK
12,31 ICH_PME#
R306 0
PME#
13,31 CLKRUN#
CLKRUN#
TEST
T86 PAD
R301 100K
4/18-45 4/9-40
R5C833T_V00
CoreLogic CLOCKRUN#
The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive thesignal low, in order to disable CLKRUN#.
CLK_PCI_PCCARD
R337 22
C476 1P
Refer to DELL M07 schematic X06
QUANTA COMPUTER
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5 IN 1 CONTROLLER
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80 mils

+3.3V_RUN_PHY

L36 BLM18PG181SN1D 0603 modify +3.3V_R5C833

C474 10U 0603 6.3
C469 0.1U 10
C470 0.01U 25
C471 1000P 50

Place these caps as close to the R5C833 as possible.

U22A

AVCC_PHY1 98
AVCC_PHY2 106
AVCC_PHY3 110
AVCC_PHY4 112

AS CLOSE AS POSSIBLE TO R5C833

TPBIAS0 113

C835 0.33U 0603 16
C825 0.01U 25
R615 56.2/F
R616 56.2/F

TPBN0 104 TPB0N
TPBP0 105 TPB0P
TPAN0 108 TPA0N
TPAP0 109 TPA0P

R614 56.2/F
R613 56.2/F
C834 270P 25
R633 5.11K/F

Circuit area : As small as possible.

*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

J6
1 TPB0N
2 TPB0P
3 TPA0N
4 TPA0P
5
6
7
8
06FFS-SP-TF(LF)(SN)

GUARD GND

C456 22P 50 1394_XI 94 XI
Y1 24.576MHZ
C463 22P 50 1394_XO 95 XO

Populate C455 for R5C832 chipset.

C466 *0.01U_NC RICOH_FIL0 96 FIL0
R339 10K/F RICOH_REXT 101 REXT
C475 0.01U RICOH_VREF 100 VREF

Place these caps as close to the U26 as possible.

IEEE1394/SD

MDIO17 87 XD/MMS_DATA7 30
MDIO16 92 XD/MMS_DATA6 30
MDIO15 89 XD/MMS_DATA5 30
MDIO14 91 XD/MMS_DATA4 30
MDIO13 90 SD/XD/MS_DATA3 30
MDIO12 93 SD/XD/MS_DATA2 30
MDIO11 81 SD/XD/MS_DATA1 30
MDIO10 82 SD/XD/MS_DATA0 30

MDIO05 75 XD_WP# 30
MDIO08 88 SD/XD/MS_CMD 30
MDIO19 83 XD_ALE 30
MDIO18 85 XD_CLE 30
MDIO02 78 XD_CE# 30

MDIO03 77 SD_WP#(XDR/B#) 30
MDIO00 80 SD_CD# SD_CD# 30 D25 BAS316
MDIO01 79 MS_INS# MS_INS# 30 D24 BAS316
MDIO09 84 SD/XD/MS_CLK 30
MDIO04 76 MC_PWR_CTRL_0 30
MDIO06 74 T91 PAD
MDIO07 73

+3.3V_R5C833
R307 *10K_NC
close to the Chip
XD_CDSW# 30

97 RSV

R5C833T_V00

33

Title	IEEE 1394		
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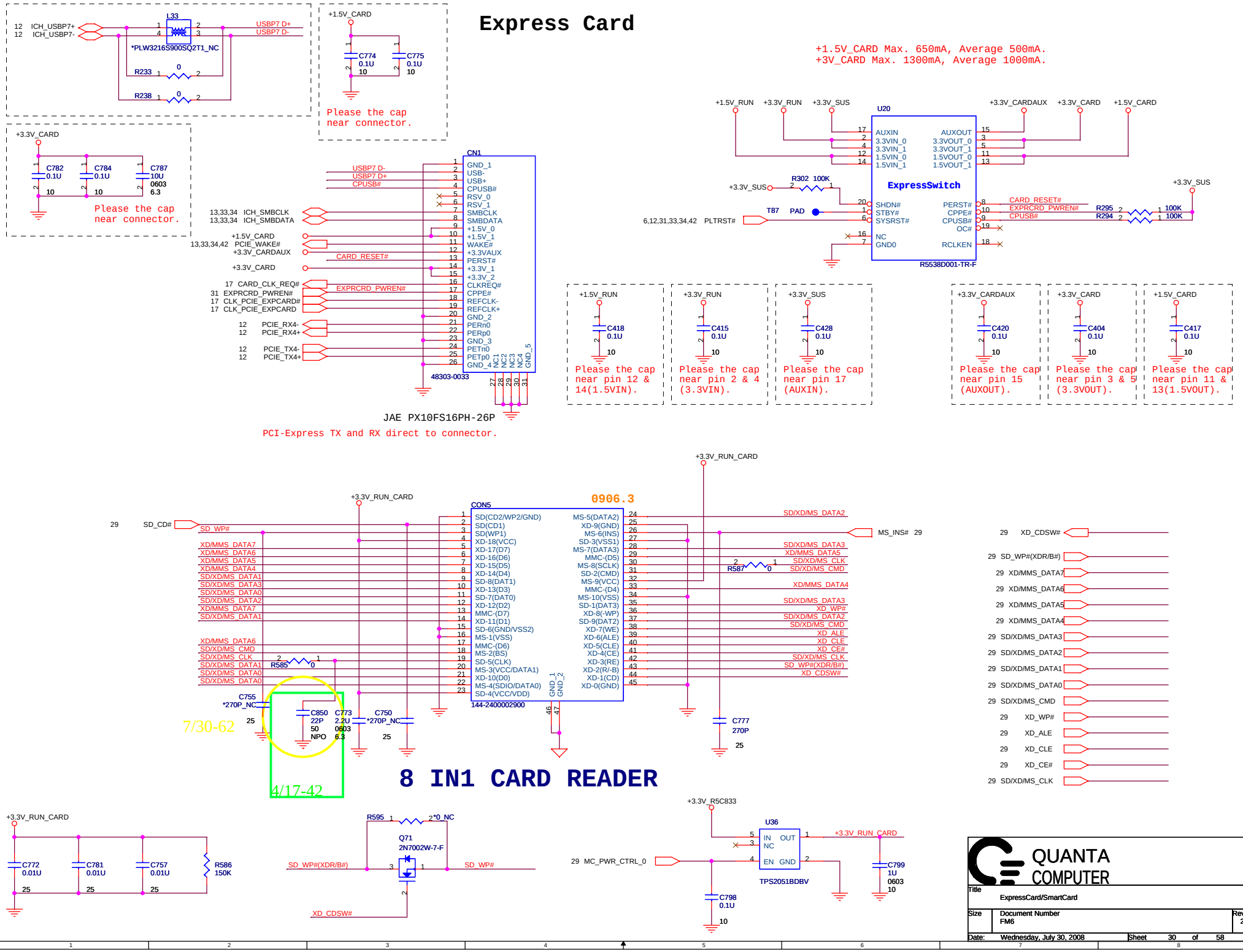
Express Card

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



Title	ExpressCard/SmartCard
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QUANTA COMPUTER

ITE8512E LQFP-128L

U9

KEYBOARD
KSO[0..16] 37
KSI[0..7] 37
LED_MASK# 38
KSO16 57
KSO15 56
KSO14 55
KSO13 54
KSO12 53
KSO11 52
KSO10 51
KSO9 46
KSO8 45
KSO7 44
KSO6 43
KSO5 42
KSO4 41
KSO3 40
KSO2 39
KSO1 38
KSO0 37
KSO17/GPC5
KSO16/GPC3
KSO15
KSO14
KSO13
KSO12/SLCT
KSO11/ERR
KSO10/PE
KSO9/BUSY
KSO8/ACK
KSO7/PD7
KSO6/PD6
KSO5/PD5
KSO4/PD4
KSO3/PD3
KSO2/PD2
KSO1/PD1
KSO0/PD0
KSI7 65
KSI6 64
KSI5 63
KSI4 62
KSI3 61
KSI2 60
KSI1 59
KSI0 58
KSI7
KSI6
KSI5
KSI4
KSI3/SLIN
KSI2/INIT
KSI1/AFD
KSI0/STB

+3.3V_ALW
C154 10U 0603 6.3
C185 0.1U 10
C631 0.1U 10
C211 0.1U 10
C579 0.1U 10
Place these caps close to ITE8512.

ADC/DAC
VBAT1 3
VCC 11
VSTBY1 26
VSTBY2 50
VSTBY3 92
VSTBY4 114
VSTBY5 121
VSTBY6 127
+3.3V_RUN
+3.3V_ALW
+RTC_CELL
R125 0
R124 *0_NC
C186 0.1U 10
ADC0/GPI0 66
ADC1/GPI1 67
ADC2/GPI2 68
ADC3/GPI3 69
ADC4/GPI4 70
ADC5/GPI5 71
ADC6/GPI6 72
ADC7/GPI7 73
HWPG 66
LCD_CBL_DET# 69
INVERTER_CBL_DET# 70
ADP_OC 72
SIO_SLP_S5# 73
HWPG 44
IMVP6_PROCHOT# 51
LCD_CBL_DET# 26
INVERTER_CBL_DET# 26
PBAT_PRES# 54
SIO_SLP_S5# 13
DAC0/GPJ0 76
DAC1/GPJ1 77
DAC2/GPJ2 78
DAC3/GPJ3 79
DAC4/GPJ4 80
DAC5/GPJ5 81
R109 0
D12 SDMK0340L-7-F
ADAPT_TRIP_SEL 46
SIO_EXT_WAKE# 13
LAN_DISABLE# 42
EXPRCRD_PWREN# 30
ICH_RSMRST# 13
SIO_PWRBTN# 13

PWM
PWM0/GPA0 24
PWM1/GPA1 25
PWM2/GPA2 28
PWM3/GPA3 29
PWM4/GPA4 30
PWM5/GPA5 31
PWM6/GPA6 32
PWM7/GPA7 34
TACH0/GPD6 47
TACH1/GPD7 48
TMRI0/WUI2/GPC4 120
TMRI1/WUI3/GPC6 124
BREATH_LED# 38
BAT2_LED# 38
FAN1_PWM 39
PWM_VADJ 26
BAT1_LED# 38
KB_BACKLITE_EN 37
CAP_LED# 37
BEEP 40
FAN1_TACH 39
PANEL_BKEN 19
LID_SW# 37
MEDIA_INT# 37

LPC
11,40 ICH_AZ_CODEC_RST#
6,12,30,33,34,42 PLTRST#
17 CLK_PCI_8512
11,33 LPC_LFRAME#
11,33 LPC_LAD0
11,33 LPC_LAD1
11,33 LPC_LAD2
11,33 LPC_LAD3
R623 *0_NC
R447 0
LPCRST/WUI4/GPD2
LPCCLK
LFRAME
LAD0
LAD1
LAD2
LAD3
13,28 CLKRUN#
13,28 IRQ_SERIRQ
CLKRUN/GPH0/ID0
SERIRQ
IRQ_SERIRQ
D11 SDMK0340L-7-F
D10 SDMK0340L-7-F
D14 SDMK0340L-7-F
13 SIO_EXT_SCI#
11 SIO_A20GATE
26 LCD_TST
ECSMI/GPD4
ECSCI/GPD3
GA20/GPB5
LPCPD/WUI6/GPE6
11 SIO_RCIN#
26 LCD_BAK#
D13 SDMK0340L-7-F
WRST#
LCD_BAK#
KBRST/GPB6
WRST
PWUREQ/GPC7
2/16-17
7/30-67
R651 0
R640 *0_NC
40 NB_MUTE#
11,40 ICH_AZ_CODEC_RST#
6,12,30,33,34,42 PLTRST#
L80HLAT/GPE0
L80LLAT/WUI7/GPE7
Charge and BAT
CLK, LCD and Thermal
G_Thermal
and Media button

IR/UART
RXD/GPB0 108
TXD/GPB1 109
CRX0/GPC0 119
CTX0/GPB2 123
CRX1/GPH1/ID1 94
CTX1/GPH2/ID2 95
IMVP_VR_ON
WIRELESS_ON/OFF# 38
AUX_EN_WOWL 34
CIRRX 37
RUN_ON_1 44
HDDC_EN 36
IMVP_VR_ON 51

SMBUS
46,54 SMBCLK0
46,54 SMBDAT0
17,26,39 SMBCLK1
17,26,39 SMBDAT1
22,37 SMBCLK2
22,37 SMBDAT2
SMBCLK0 110
SMBDAT0 111
SMBCLK1 115
SMBDAT1 116
SMBCLK2 117
SMBDAT2 118
SMCLK0/GPB3
SMDAT0/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
SMCLK2/GPF6
SMDAT2/GPF7

LPC/FWH FLASH
FLFRAME/GPG2/LF 100
FLRST/GPG0/ITM 106
FLAD3/GPG6 104
FLAD2/SO 103
FLAD1/SI 102
FLAD0/SCE 101
FLCLK 105
SUS_ON
SUS_ON 49,53
KB_DET# 37
ICH_CL_PWROK 6,13
EC_FLASH_SPI_DO 32
EC_FLASH_SPI_DIN 32
EC_FLASH_SPI_CS# 32
EC_FLASH_SPI_CLK 32

PS/2
13,44,51 IMVP_PWRGD
44 RESET_OUT#
37 NUM_LED#
37 CLK_TP_SIO
37 DAT_TP_SIO
PS2CLK0/GPF0 85
PS2DAT0/GPF1 86
PS2CLK1/GPF2 87
PS2DAT1/GPF3 88
PS2CLK2/GPF4 89
PS2DAT2/GPF5 90

EGPC
EGAD/GPE1 82
EGCS/GPE2 83
EGCLK/GPE3 84
PS_ID 54
5V_ALW_ON 52
SNIFFER_GREEN# 38

GPIO
GPH3/ID3 96
GPH4/ID4 97
GPH5/ID5 98
GPH6/ID6 99
GPG1/ID7 107
USB_SIDE_EN#
USB_BACK_EN#
BID1
CHIPSET_ID1
USB_SIDE_EN# 35
USB_BACK_EN# 35
MODC_EN 36

RI1/WUI0/GPD0 18
RI2/WUI1/GPD1 21
WUI5/GPE5 35
SIO_SLP_S3# 13
ACAV_IN 46
SNIFFER_PWR_SW# 38
RING/PWRFAIL/LPCRST/GPB7 112
PWRSW/GPE4 125
MAIN_PWR_SW# 38
GINT/GPD5 33
LCDVCC_TST_EN 26

CK32K
CK32KE
ITE8512_XTAL1 128
ITE8512_XTAL2 2
ITE8512IX_JX
VSS1 1
VSS2 12
VSS3 27
VSS4 49
VSS5 91
VSS6 113
VSS7 122
AVCC 74
AVSS 75
ITE8512E
LQFP128-16X16-4-FX2

+3.3V_ALW
D9 SDMK0340L-7-F
R119 100K
WRST#
39,52 THERM_STP#
C174 1U 0603 10
+3.3V_ALW
L15 BLM11A05S 0603
L16 BLM11A05S 0603
C164 0.1U 10

32KHz Clock.
ITE8512_XTAL2
R132 0
W2
ITE8512_XTAL1
C188 18P 50
32.768KHZ
C198 18P 50

CLK_PCI_8512
R115 10
C175 2.2P 50

ITE8512IX_JX
C171 *1U_NC 0603 10
C172 0.1U 10
2/13-12
3/28-38
ITE8512IX pin12 connect to GND.
ITE8512JX pin12 connect to 0.1uF, 1uF.

RESET_OUT#
R347 1K
6/30-59

+3.3V_ALW
SMBDAT0 SMBCLK0 RP3 2.2KX2
SMBDAT1 SMBCLK1 RP4 10KX2
SMBDAT2 SMBCLK2 RP5 2.2KX2
SIO_SLP_S5# R95 *100K_NC
SUS_ON R144 100K
HWPG R652 100K
IMVP_VR_ON R129 *100K_NC
ADP_OC R90 0 *0_NC IINP 46
R89 ADAPT_OC 46
+3.3V_RUN
LCD_CBL_DET# R435 10K
INVERTER_CBL_DET# R446 10K
IRQ_SERIRQ R450 10K
LCD_BAK# R449 *10K_NC

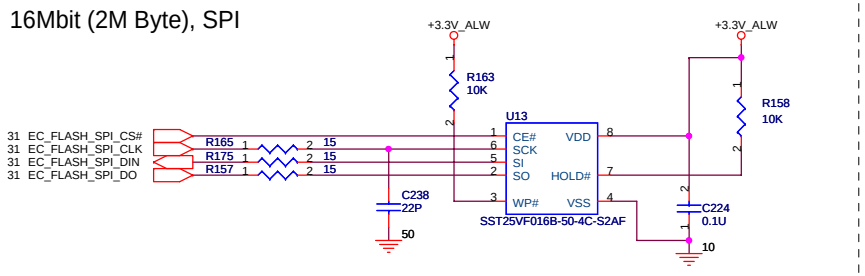
Board ID Straps
Discrete
+3.3V_ALW
R128 10K
R116 *10K_NC
R142 10K
R141 10K
USB_BACK_EN#
BID1
CHIPSET_ID1
USB_SIDE_EN#
R136 *10K_NC
R117 10K
R143 *10K_NC
R140 *10K_NC
UMA
VGA_IDENTIFY
USB_SIDE_EN#
1 = Discrete Gfx.
0 = UMA.
BID0

CHIPSET_ID1	BID1	USB_BACK_EN#	FM6B(UMA)	FM6 (Dis)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	QT (A00)	QT (A00)
0	0	0	(A01)	(A01)
0	0	1		

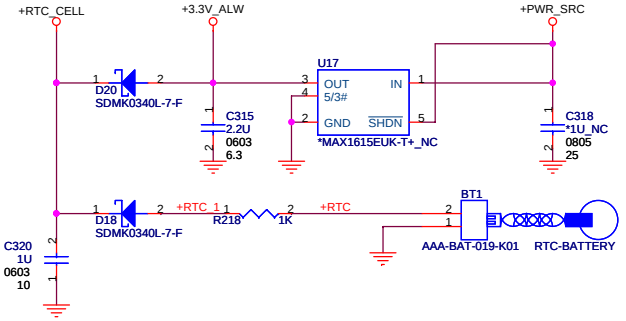
QUANTA COMPUTER

Title	Ultra I/O Controller ECE5028	
Size	Document Number FM6	Rev 3A
Date: Monday, August 04, 2008	Sheet 31 of 58	

16Mbit (2M Byte), SPI

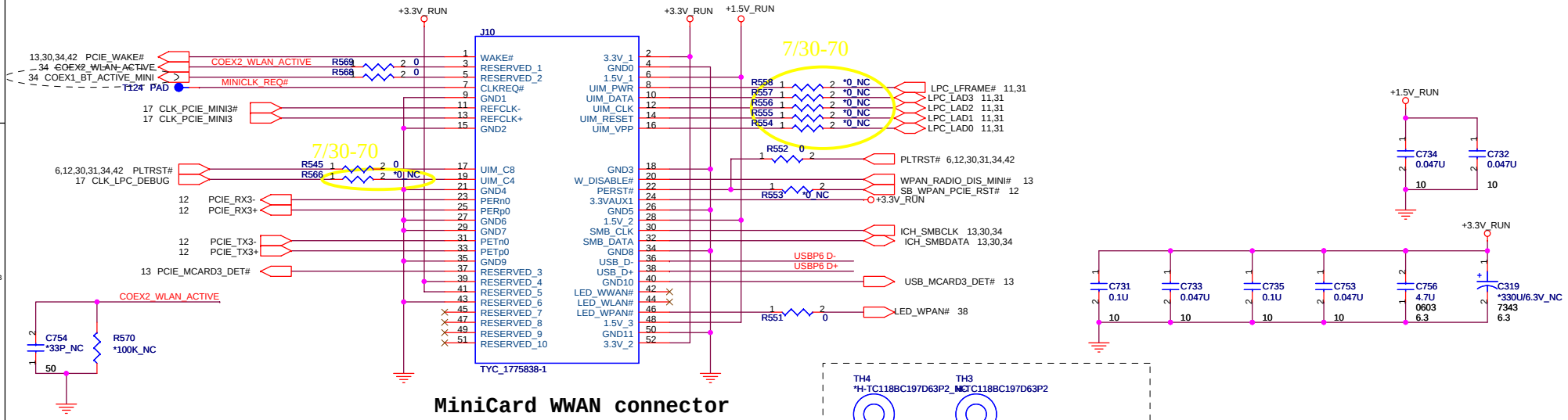


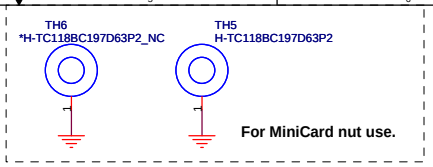
RTC BATTERY

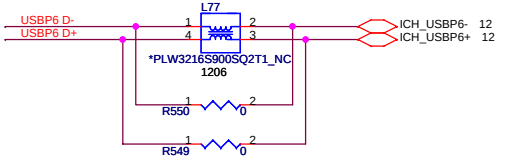


QUANTA COMPUTER		
Title	Ultra I/O Controller ECE5028	
Size	Document Number FM6	Rev 3A
Date: Monday, June 30, 2008	Sheet 32 of 58	

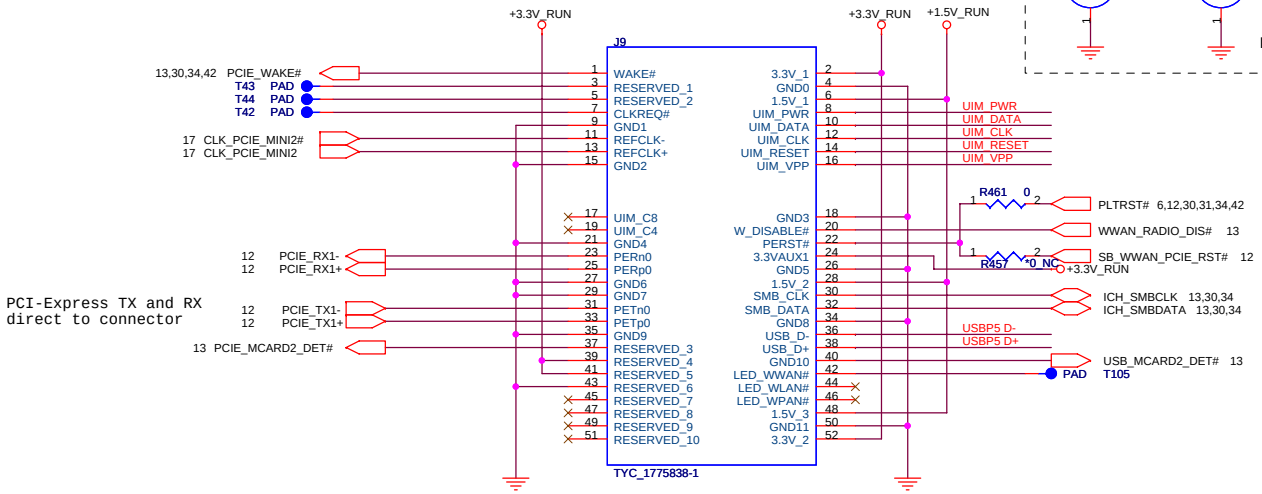
MiniCard Robson, BT. UWB connector

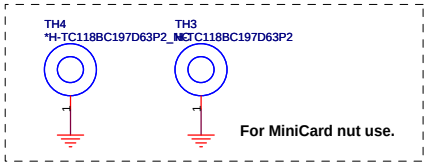


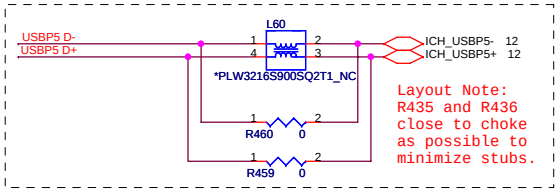


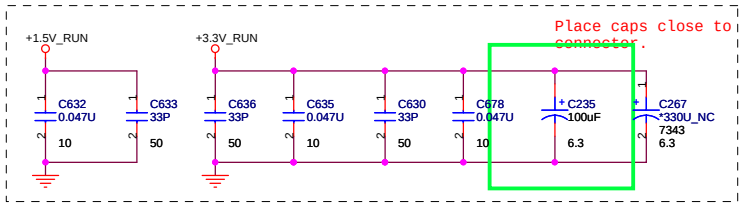


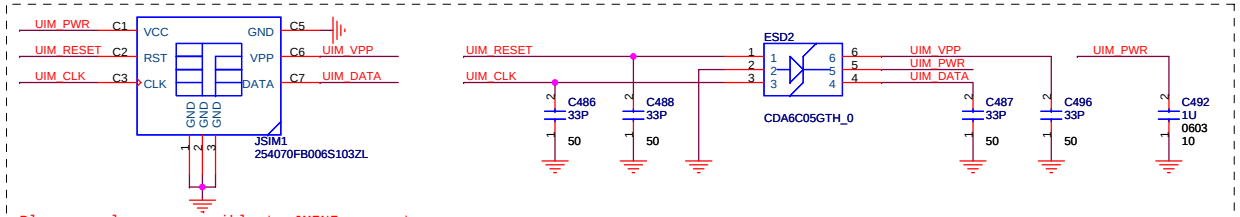
MiniCard WWAN connector











QUANTA COMPUTER

Title	MINI-PCI	
Size	Document Number FM6	Rev 2A
Date: Friday, August 01, 2008	Sheet 33 of 58	

MiniCard WLAN connector

TH2 *H-TC177BC197D83P2_NC
TH1 -TC177BC197D83P2

For MiniCard nut use.

J11 TYC_1775838-1

13,30,33,42 PCIE_WAKE#	1	WAKE#	3.3V_1	2	+3.3V_WLAN
33 COEX2_WLAN_ACTIVE	3	RESERVED_1	GND0	4	
33 COEX1_BT_ACTIVE_MIN	5	RESERVED_2	1.5V_1	6	+1.5V_RUN
17 MINI1CLK_REQ#	7	CLKREQ#	UIM_PWR	8	
	9	GND1	UIM_DATA	10	
17 CLK_PCIE_MINI1#	11	REFCLK-	UIM_CLK	12	
17 CLK_PCIE_MINI1	13	REFCLK+	UIM_RESET	14	
	15	GND2	UIM_VPP	16	
	17	UIM_C8	GND3	18	
	19	UIM_C4	W_DISABLE#	20	WLAN_RADIO_OFF#
	21	GND4	PERST#	22	
12 PCIE_RX2-	23	PERn0	3.3VAUX1	24	
12 PCIE_RX2+	25	PERp0	GND5	26	
	27	GND6	1.5V_2	28	
12 PCIE_TX2-	29	GND7	SMB_CLK	30	WLAN_SMBCLK
12 PCIE_TX2+	31	PETn0	SMB_DATA	32	WLAN_SMBDATA
	33	PETp0	GND8	34	
13 PCIE_MCARD1_DET#	35	GND9	USB_D-	36	USBP4 D-
	37	RESERVED_3	USB_D+	38	USBP4 D+
	39	RESERVED_4	GND10	40	USB_MCARD1_DET# 13
	41	RESERVED_5	LED_WWAN#	42	
	43	RESERVED_6	LED_WLAN#	44	LED_WLAN_OUT# 38
	45	RESERVED_7	LED_WPAN#	46	
	47	RESERVED_8	1.5V_3	48	
	49	RESERVED_9	GND11	50	
	51	RESERVED_10	3.3V_2	52	

MINI1CLK_REQ# → R565 0 / R567 0 → MINI1CLK_REQ#

C752 220P 50

R544 0 → PLTRST# 6,12,30,31,33,42

R548 *0_NC → SB_WLAN_PCIE_RST# 12

Non-iAMT: T123 PAD, T122 PAD, T121 PAD

PCI-Express TX and RX direct to connector

USBP4 D- / USBP4 D+ → L78 *PLW3216S900SQ2T1_NC 1206 → ICH_USBP4- 12, ICH_USBP4+ 12

R560 0, R559 0

RP46 2.2KX2

WLAN_SMBCLK → Q62 *2N7002W-7-F_NC → ICH_SMBCLK 13,30,33 (R546 *0_NC)

WLAN_SMBDATA → Q61 *2N7002W-7-F_NC → ICH_SMBDATA 13,30,33 (R562 *0_NC)

Suport for WoW

WLAN_RADIO_OFF# → D33 SDMK0340L-7-F → WLAN_RADIO_DIS# 13 (R537 *0_NC)

Prevent backdrive when WoW is enabled.

+PWR_SRC, +3.3V_ALW, +3.3V_WLAN, +3.3V_RUN

Q60 *FDC655BN_NC, R547 0 0805

R542 *100K_NC, R538 *100K_NC

Q59B *2N7002DW-7-F_NC, Q59A *2N7002DW-7-F_NC

31 AUX_EN_WOWL

R543 *200K_NC, R534 *470K_NC, R532 *100K_NC, C713 *4700P_NC 0603 50

+1.5V_RUN: C736 0.047U 10, C738 0.047U 10

+3.3V_WLAN: C737 0.1U 10, C739 0.047U 10, C740 0.1U 10, C751 0.047U 10, C730 4.7U 0805 10, C317 *330U/6.3V_NC 7343 6.3

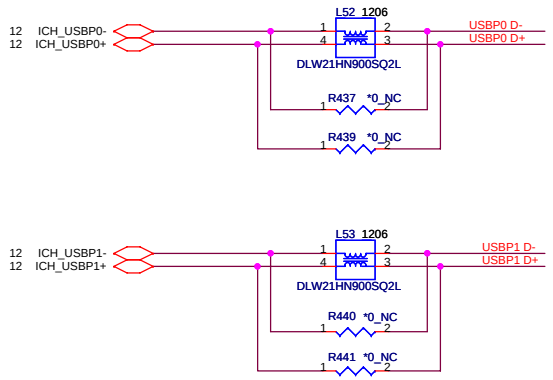
Place caps close to connector.

QUANTA COMPUTER

Title	MDC CONN.		
Size	Document Number FM6		Rev 1A
Date:	Friday, August 01, 2008	Sheet 34 of 58	

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

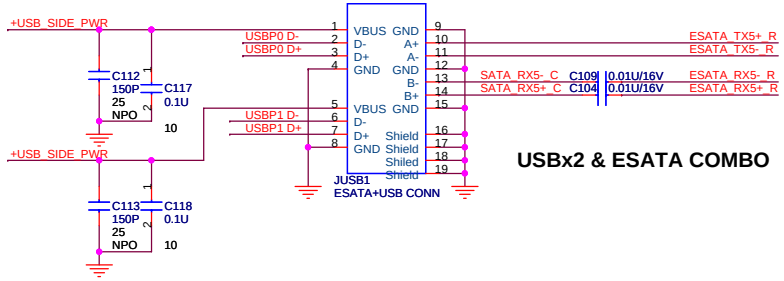
2/22-25
4/17-42



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Side External USBX2

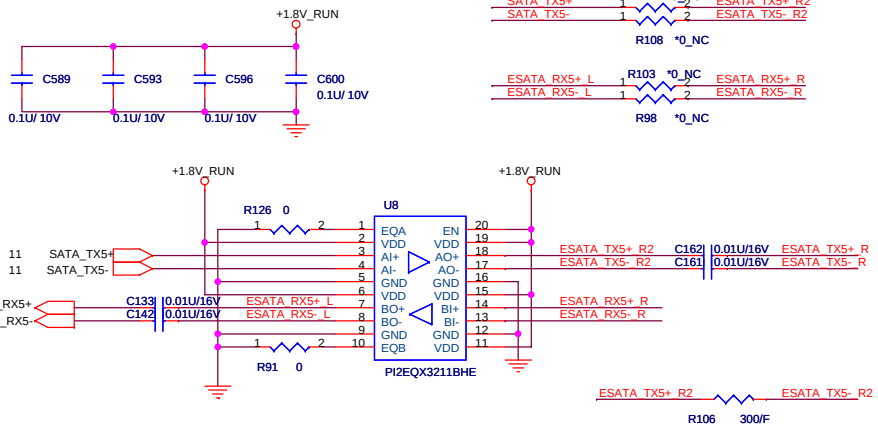
2/13-4



USBx2 & ESATA COMBO

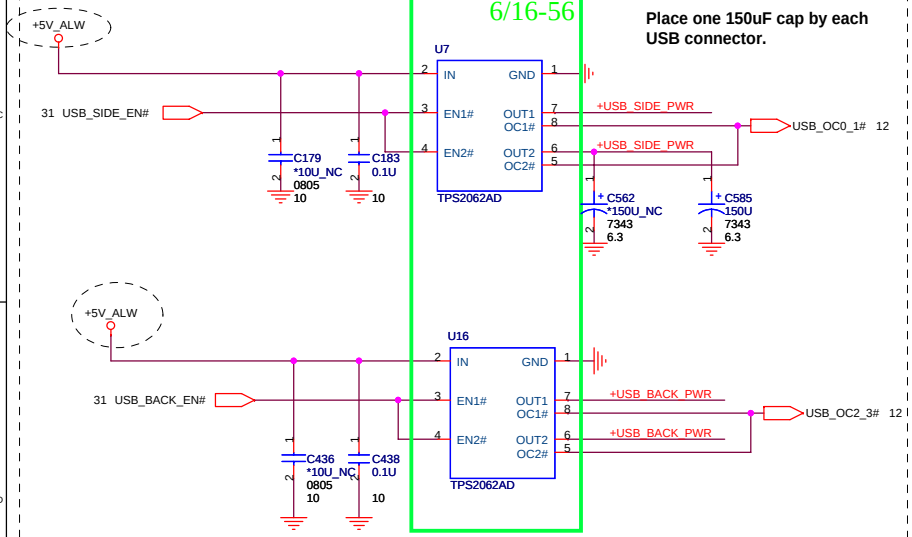
5/29-52
2/20-22

E-SATA Re-driver



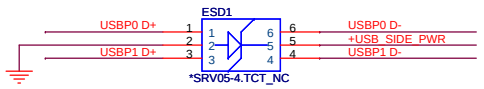
6/16-56

Place one 150uF cap by each USB connector.

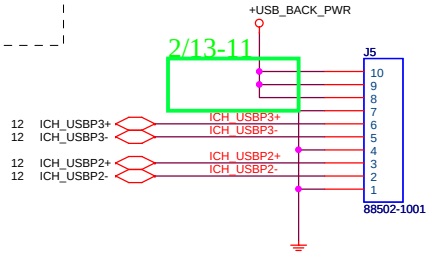


Each channel is 1A

Place ESD diodes as close as USB connector.



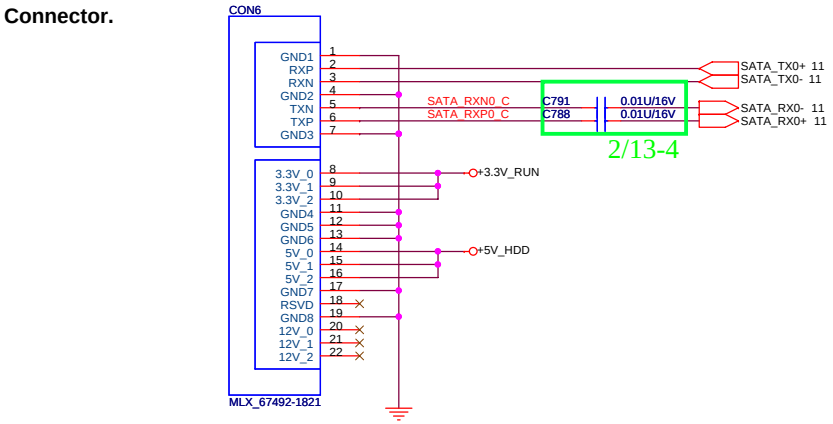
MB side

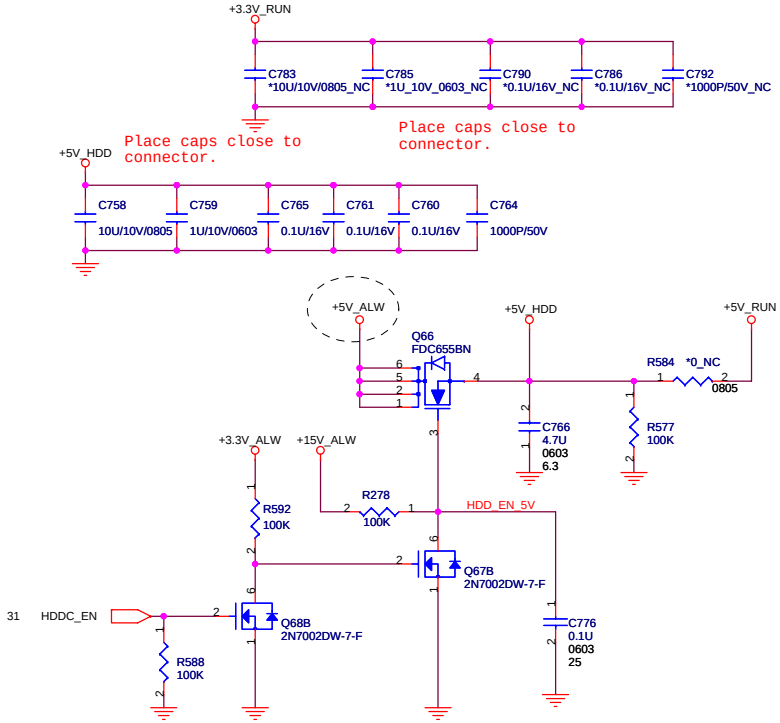


QUANTA COMPUTER

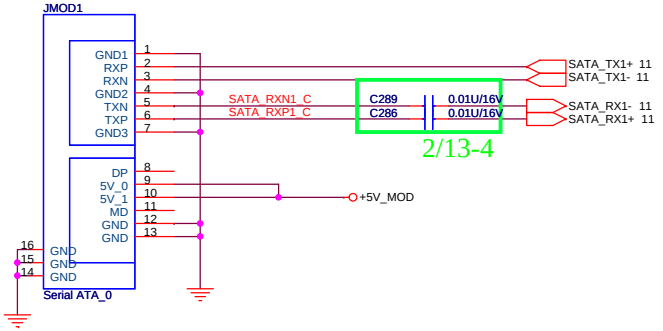
Title	SERIAL PORT & USB	
Size	Document Number FM6	Rev 3A
Date: Wednesday, July 30, 2008	Sheet 35 of 58	

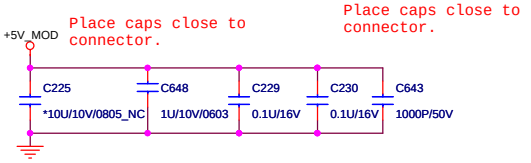
SATA Connector.

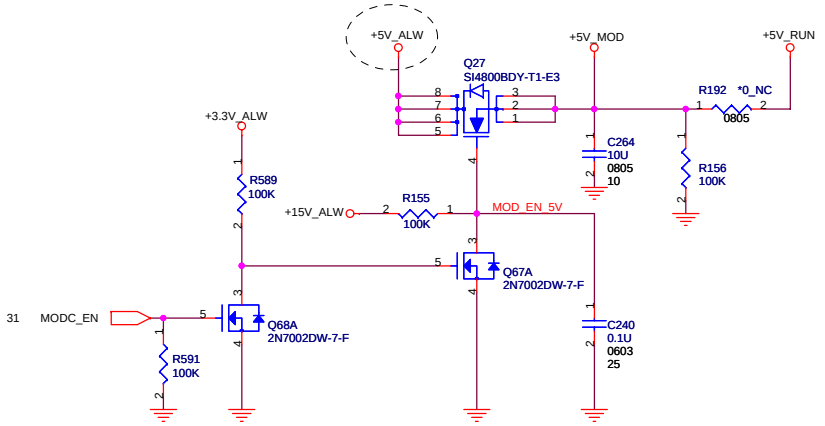




ODD Connector

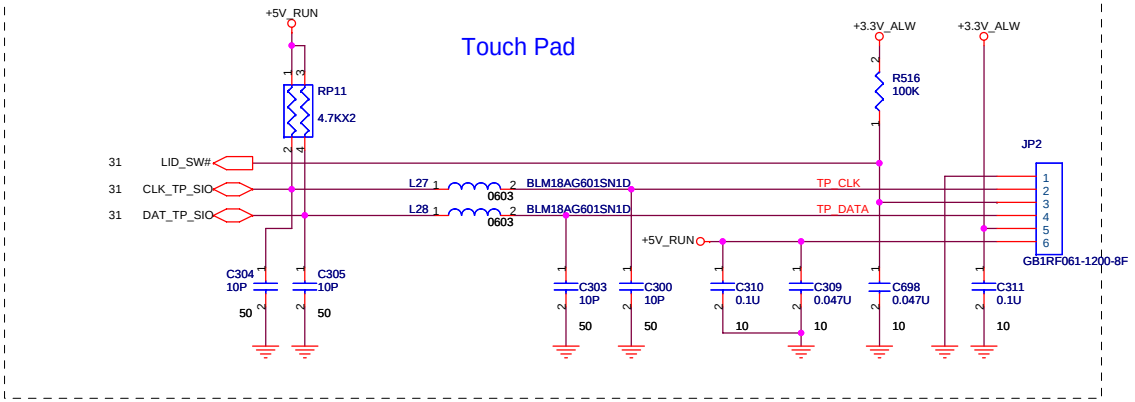




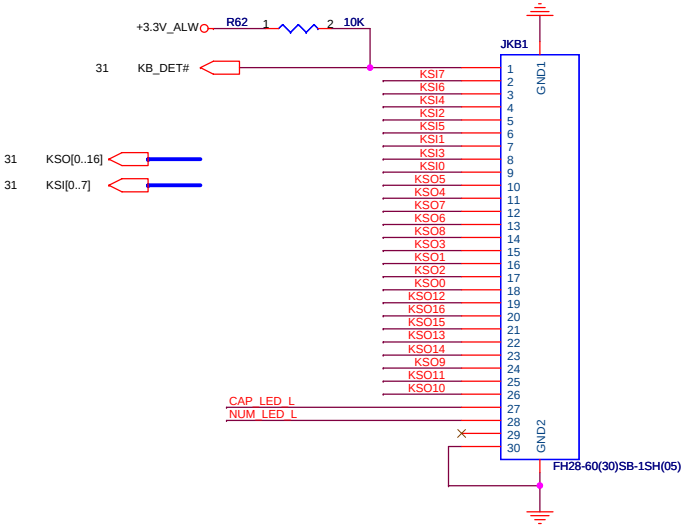


QUANTA COMPUTER		
Title: SATA (HDD&CD_ROM)		
Size	Document Number FM6	Rev 2A
Date: Wednesday, July 30, 2008	Sheet 36 of 58	

Touch Pad



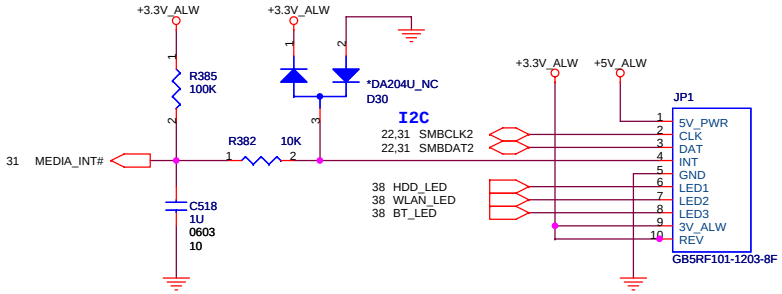
KEYBOARD CONNECTOR

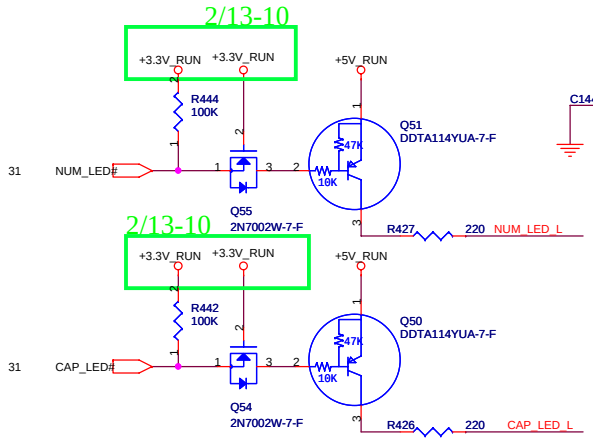


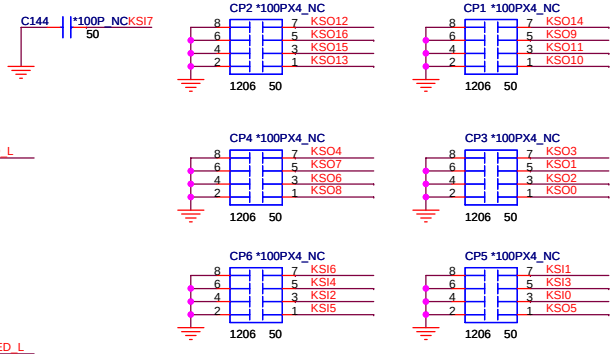
Media Button

2/13-10

Change to P/N:DFFC10FR138
F/T:88501-1001-10P-L(0816)

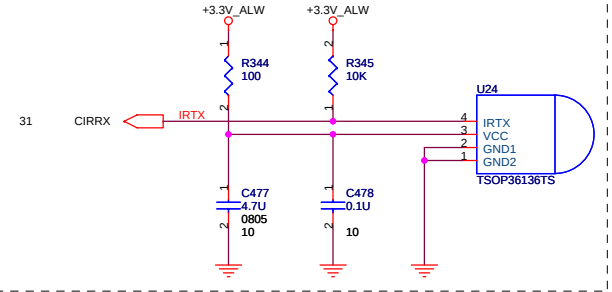




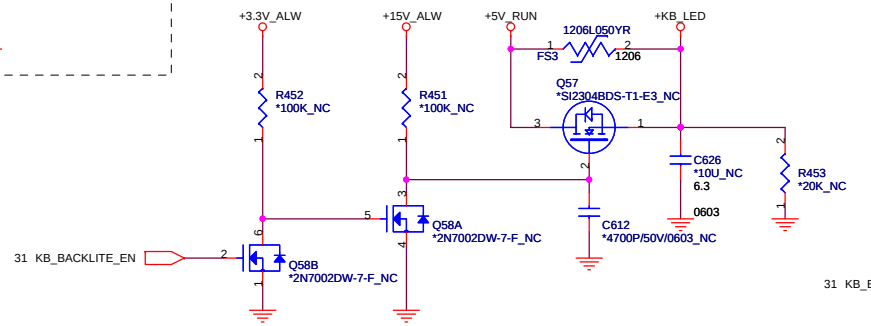


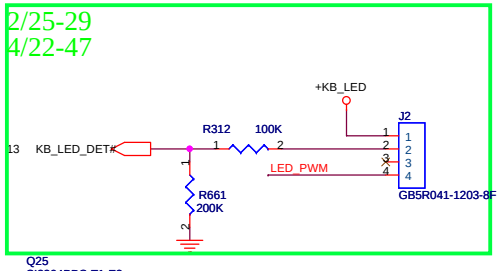
100P CAPS CLOSE TO JKB1

Consumer IR



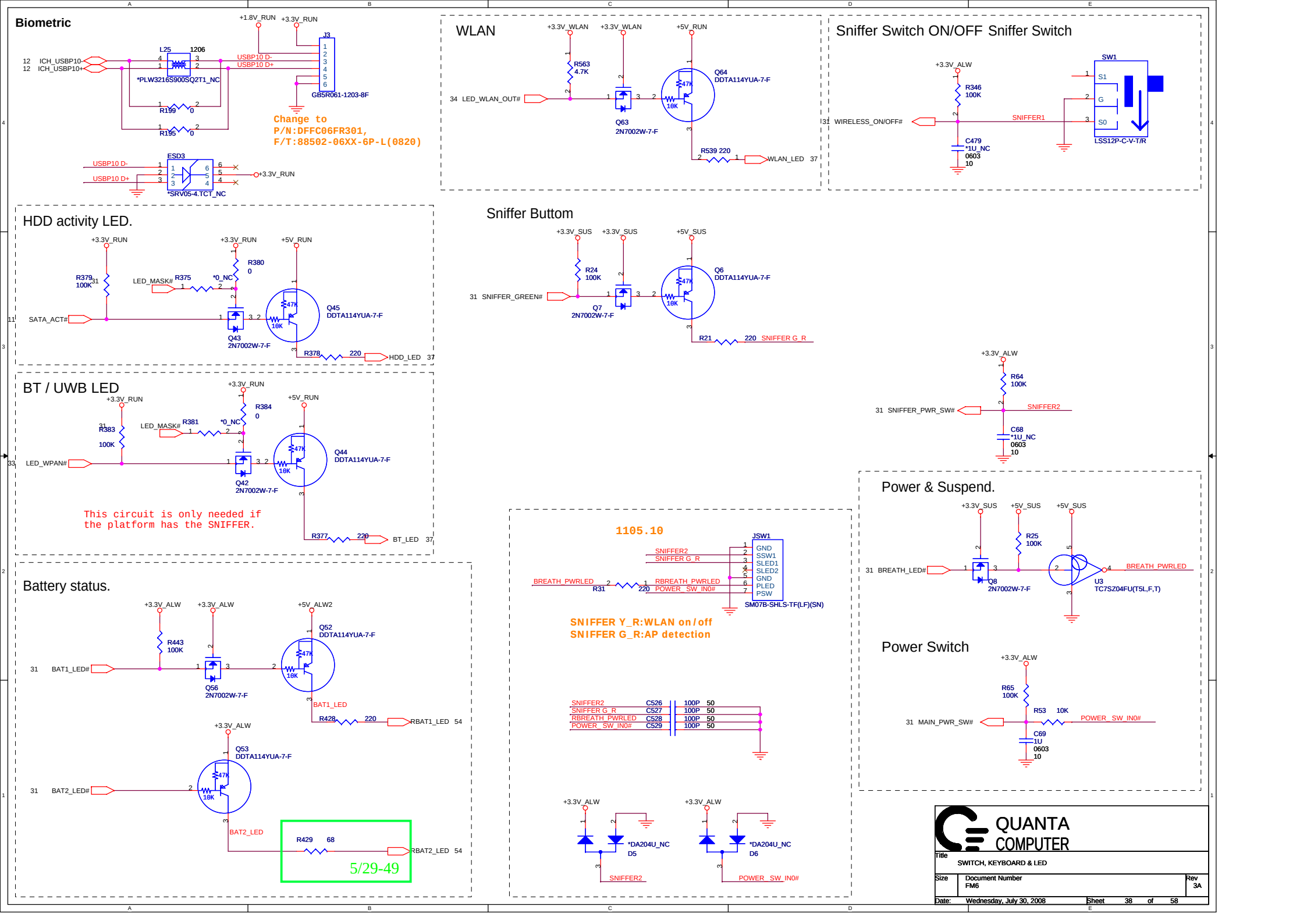
Key board Illumination

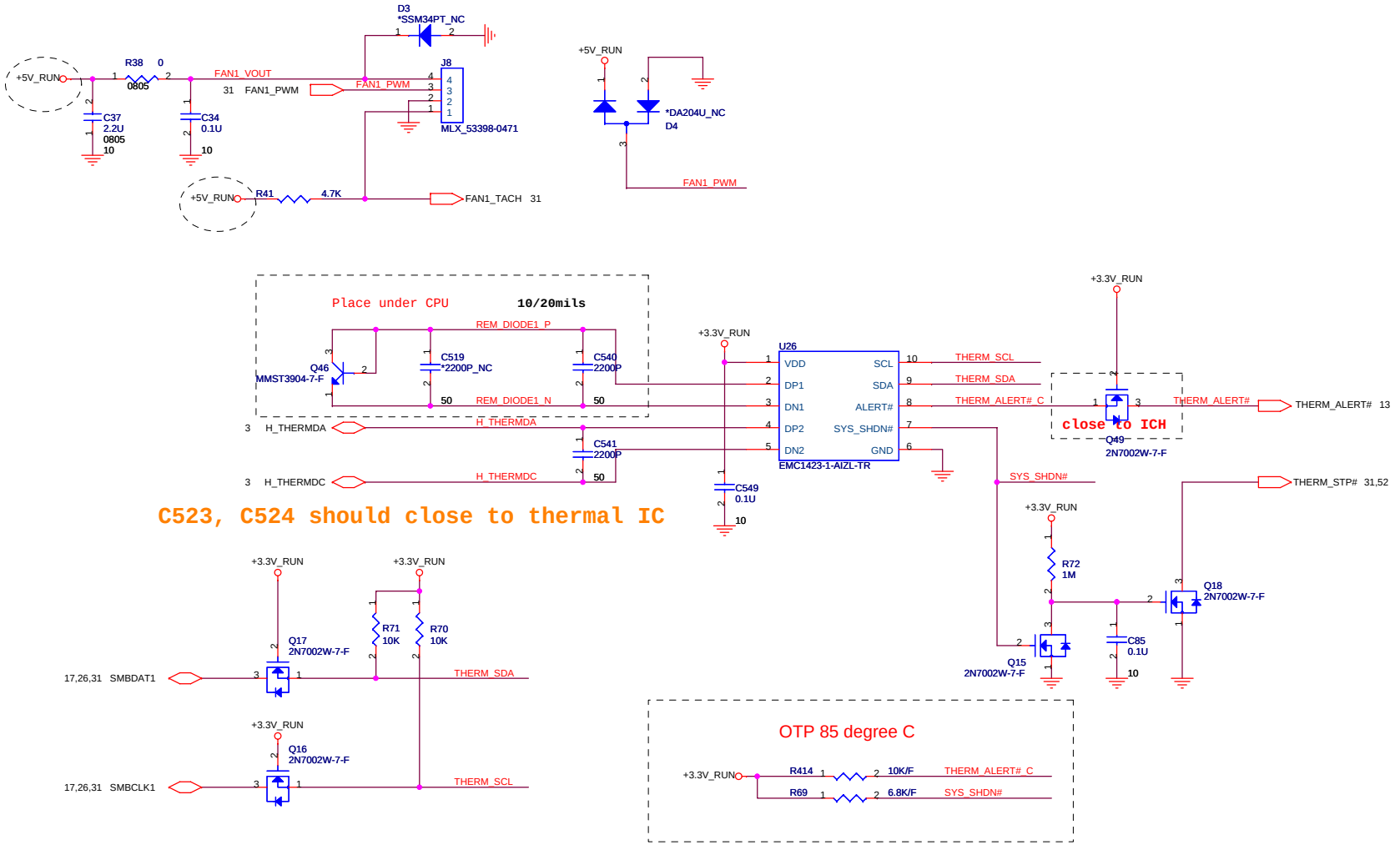




QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
Size	Document Number FM6	Rev 3A
Date: Wednesday, July 30, 2008	Sheet 37 of 58	


Biometric
+1.8V_RUN
+3.3V_RUN
J3
L25
1206
12 ICH_USBP10-
12 ICH_USBP10+
USBP10 D-
USBP10 D+
*PLW3216S900SQ2T1_NC
GB5R061-1203-8F
R199 0
R195 0
Change to
P/N:DFFC06FR301,
F/T:88502-06XX-6P-L(0820)
ESD3
USBP10 D-
USBP10 D+
+3.3V_RUN
*SRV05-4.TCT_NC
WLAN
+3.3V_WLAN
+3.3V_WLAN
+5V_RUN
R563 4.7K
34 LED_WLAN_OUT#
Q64 DDTA114YUA-7-F
Q63 2N7002W-7-F
R539 220
WLAN_LED 37
Sniffer Switch ON/OFF Sniffer Switch
+3.3V_ALW
R346 100K
31 WIRELESS_ON/OFF#
SNIFFER1
SW1
S1
G
S0
LSS12P-C-V-T/R
C479 *1U_NC 0603 10
HDD activity LED.
+3.3V_RUN
+3.3V_RUN
+5V_RUN
R379 100K
31
LED_MASK#
R375 *0_NC
R380 0
11 SATA_ACT#
Q45 DDTA114YUA-7-F
Q43 2N7002W-7-F
R378 220
HDD_LED 37
Sniffer Buttom
+3.3V_SUS
+3.3V_SUS
+5V_SUS
R24 100K
31 SNIFFER_GREEN#
Q6 DDTA114YUA-7-F
Q7 2N7002W-7-F
R21 220 SNIFFER G_R
BT / UWB LED
+3.3V_RUN
+3.3V_RUN
+5V_RUN
R384 0
R383 100K
31
LED_MASK#
R381 *0_NC
33 LED_WPAN#
Q44 DDTA114YUA-7-F
Q42 2N7002W-7-F
This circuit is only needed if
the platform has the SNIFFER.
R377 220
BT_LED 37
+3.3V_ALW
R64 100K
31 SNIFFER_PWR_SW#
SNIFFER2
C68 *1U_NC 0603 10
Power & Suspend.
+3.3V_SUS
+5V_SUS
+5V_SUS
R25 100K
31 BREATH_LED#
Q8 2N7002W-7-F
U3 TC7SZ04FU(T5L,F,T)
BREATH_PWRLED
Power Switch
+3.3V_ALW
R65 100K
R53 10K
31 MAIN_PWR_SW#
POWER_SW_IN0#
C69 1U 0603 10
Battery status.
+3.3V_ALW
+3.3V_ALW
+5V_ALW2
R443 100K
31 BAT1_LED#
Q52 DDTA114YUA-7-F
Q56 2N7002W-7-F
BAT1_LED
R428 220
RBAT1_LED 54
+3.3V_ALW
Q53 DDTA114YUA-7-F
31 BAT2_LED#
BAT2_LED
R429 68
RBAT2_LED 54
5/29-49
1105.10
JSW1
SNIFFER2
SNIFFER G_R
BREATH_PWRLED
R31 220
RBREATH_PWRLED
POWER_SW_IN0#
GND
SSW1
SLED1
SLED2
GND
PLED
PSW
SM07B-SHLS-TF(LF)(SN)
SNIFFER Y_R:WLAN on/off
SNIFFER G_R:AP detection
SNIFFER2 C526 100P 50
SNIFFER G_R C527 100P 50
RBREATH_PWRLED C528 100P 50
POWER_SW_IN0# C529 100P 50
+3.3V_ALW
*DA204U_NC
D5
SNIFFER2
+3.3V_ALW
*DA204U_NC
D6
POWER_SW_IN0#
QUANTA COMPUTER
Title
SWITCH, KEYBOARD & LED
Size
Document Number
FM6
Rev
3A
Date: Wednesday, July 30, 2008
Sheet 38 of 58



QUANTA COMPUTER

Title	FAN & THERMAL	
Size	Document Number FM6	Rev 1A
Date: Wednesday, July 30, 2008	Sheet 39 of 58	

INTERNAL SPEAKER AMP

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

2/16-16

TPA6040A4
QFN 32PIN

Layout Note:
Place close
U34 pin 23.

Layout Note:
Close to U35 Pin 34

Layout Note:
Place close to
pin 18.

Layout Note:
Place close U34.

EMI Request

AZALIA (HD) CODEC

FB_60ohm+-25%_100MHz
_3A_0.05ohm DC

Depop R561,C786
for using 92HD73C

Layout Note:
Close to U35 Pin 13

Depop R603, R617, R578,R616
Pop R602, R619, R562 ,R601,
for using 92HD73C
R602,R617 close to U35, Let DVDD width be 10-mils

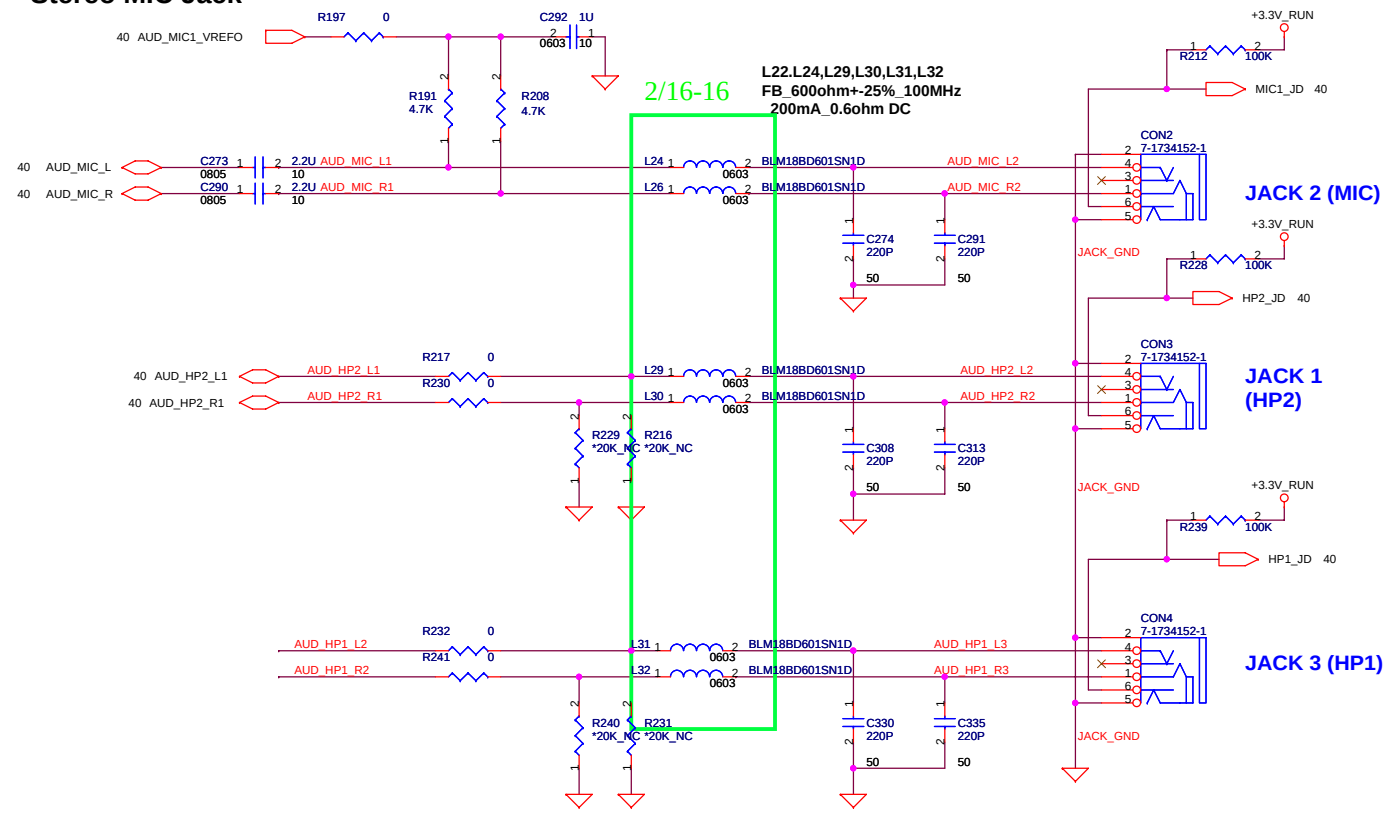
Close to U35
7/10-61

92HD73C

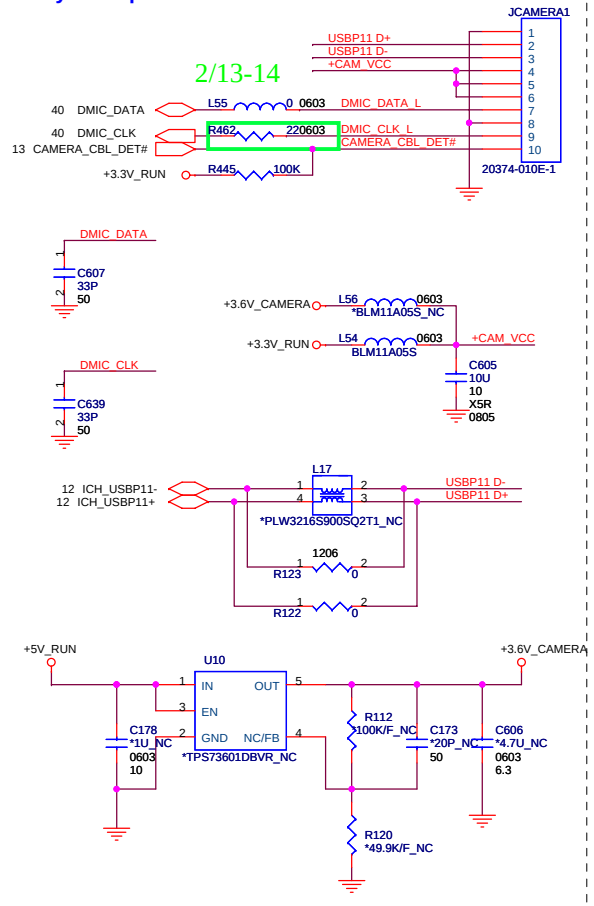
QUANTA COMPUTER

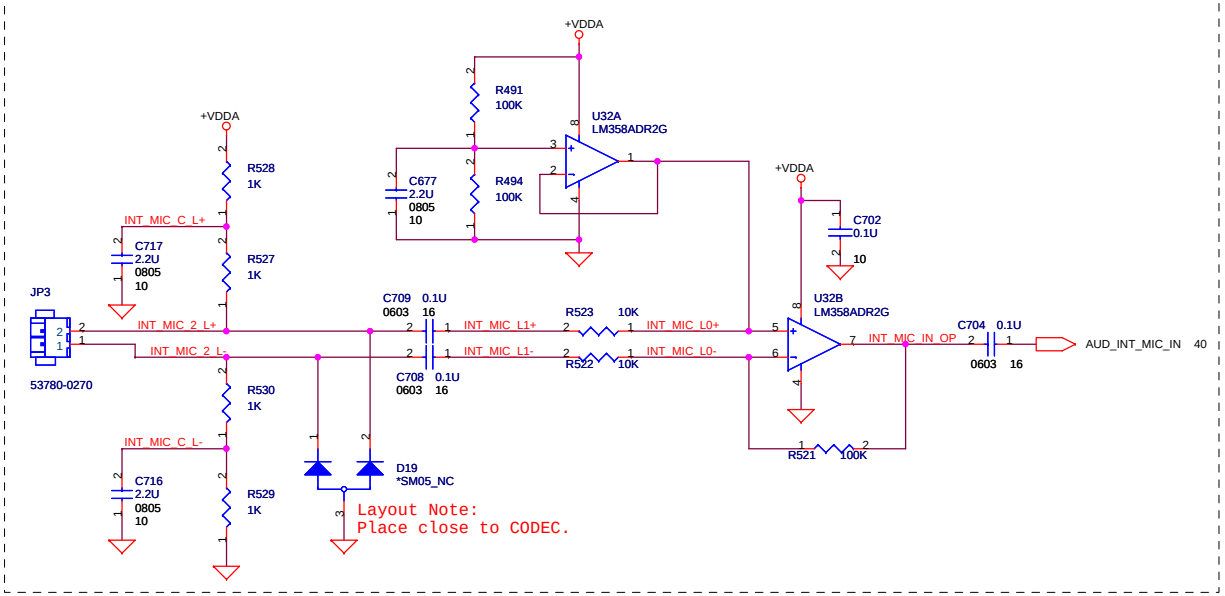
Title	Azelia CODEC	
Size	Document Number FM6	Rev 2A
Date: Wednesday, July 30, 2008	Sheet 40 of 58	

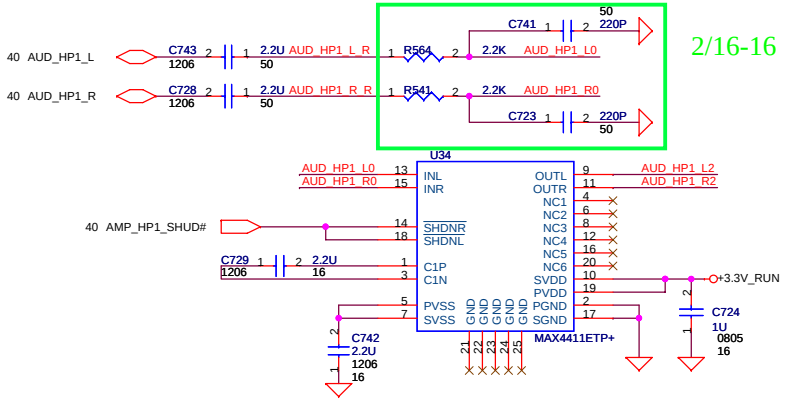
Headphone Jack
Stereo MIC Jack



Array Microphone & Camera







QUANTA COMPUTER

Title	AUDIO CONN	
Size	Document Number FM6	Rev 2A
Date: Monday, August 04, 2008	Sheet 41 of 58	

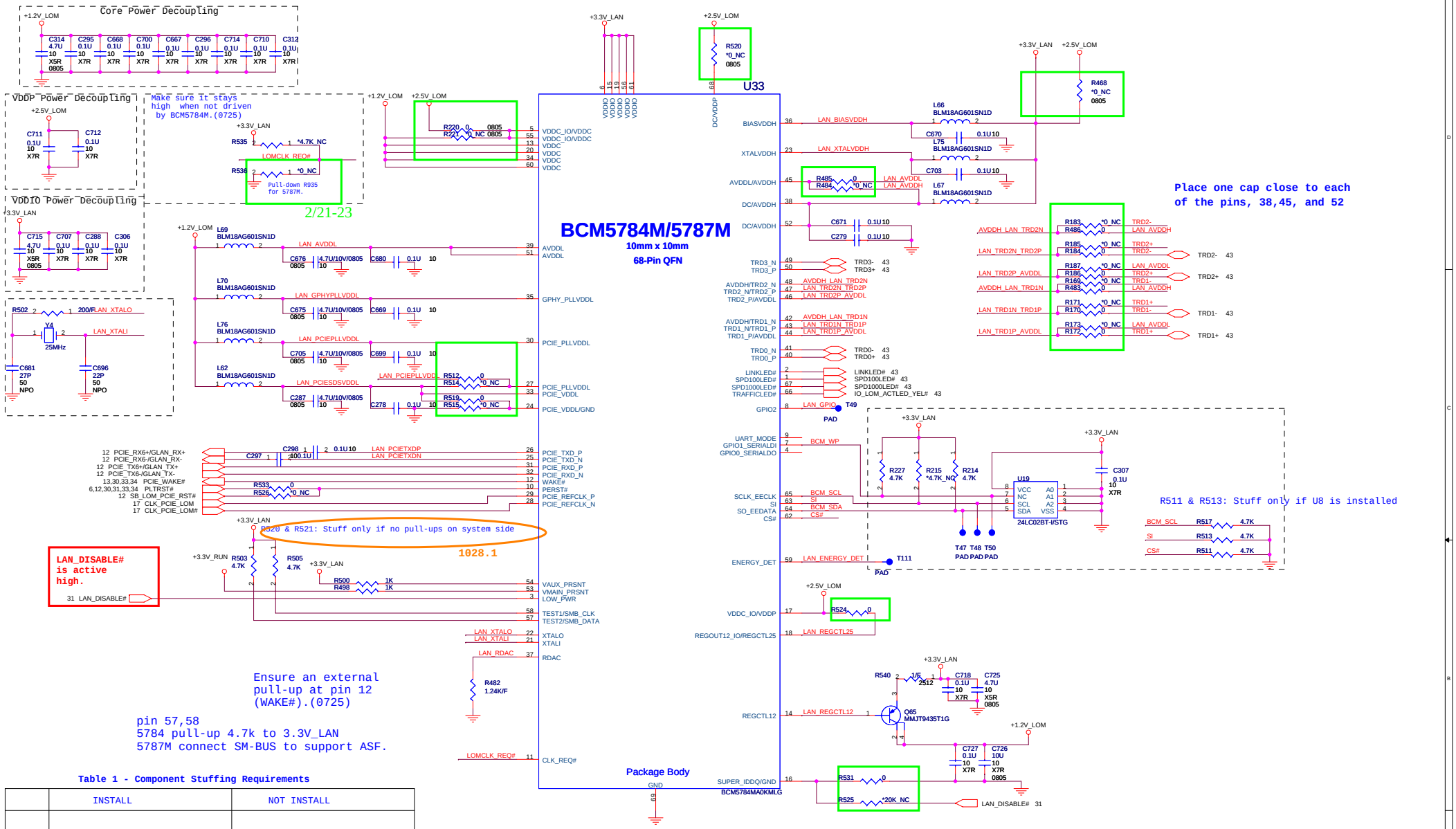


Table 1 - Component Stuffing Requirements

	INSTALL	NOT INSTALL
5787M	R221,R487,R488,Q55,C671,C672, C686,C687,R174,R176,R178,R169, R171,R173,R459,R443,R492	R209,R485,R491,R496,R461,R175, R177,R458,R170,R172,R460,R451
5784	R209,R485,R491,R496,R461,R175, R177,R458,R170,R172,R460,R451	R221,R487,R488,Q55,C671,C672, C686,C687,R174,R176,R178,R169, R171,R173,R459,R443,R492

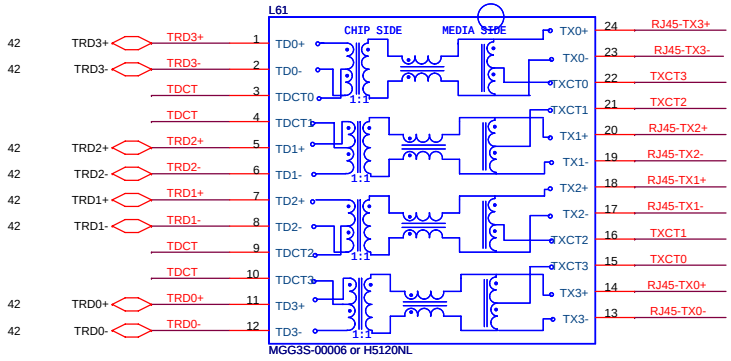
	5784M	5787M
R503	39k	0
R497	20k	*20k_NC

QUANTA COMPUTER

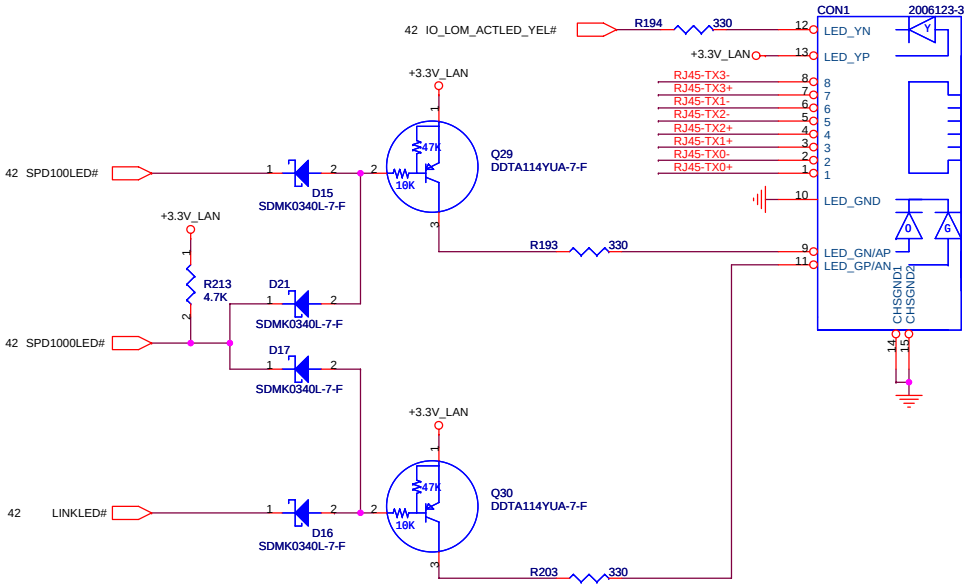
Title	LAN	
Size	Document Number FM6	Rev 3A
Date: Monday, June 30, 2008	Sheet 42 of 58	

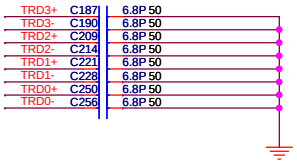
TRANSFORM

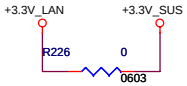
TRANSFORM

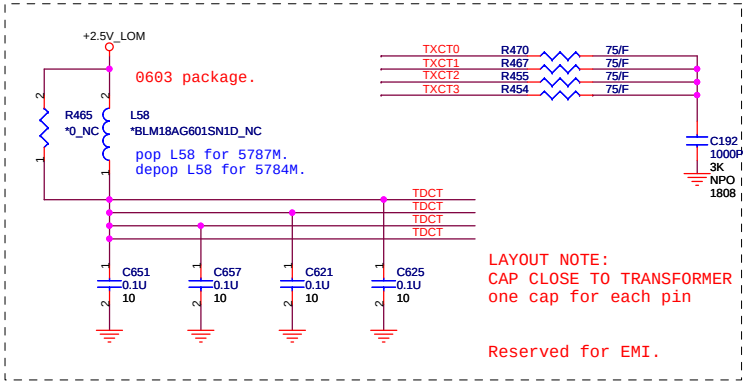


RJ-45 Connector



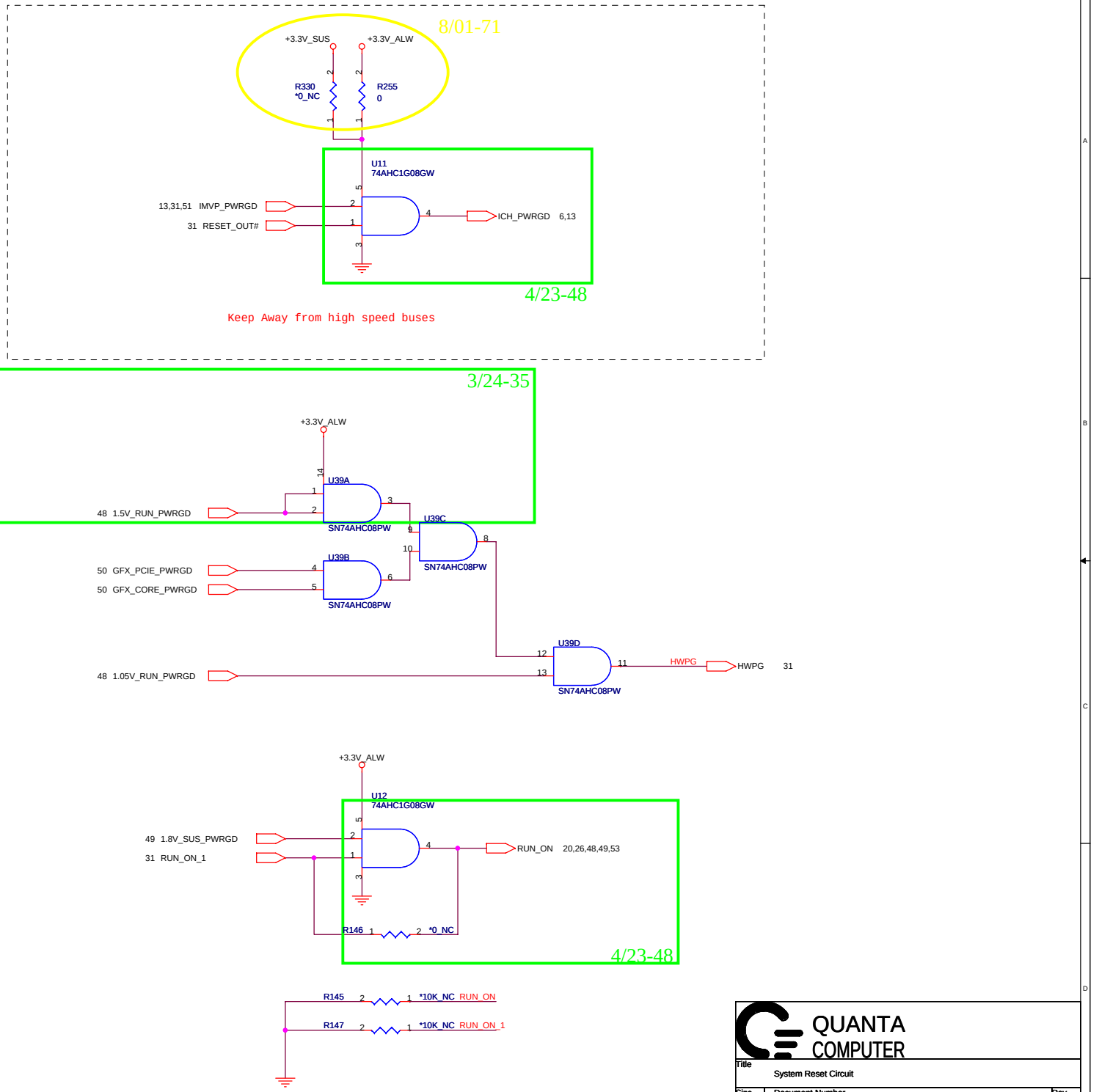






QUANTA COMPUTER

Title	LAN SWITCH	
Size	Document Number FM6	Rev 3A
Date: Monday, June 30, 2008	Sheet 43 of 58	



QUANTA COMPUTER

Title	System Reset Circuit	
Size	Document Number FM6	Rev 2A
Date: Friday, August 01, 2008	Sheet 44 of 58	

QUANTA COMPUTER

Title	Battery Selector	
Size	Document Number FM6	Rev 1A
Date: Monday, June 30, 2008	Sheet 45 of 58	

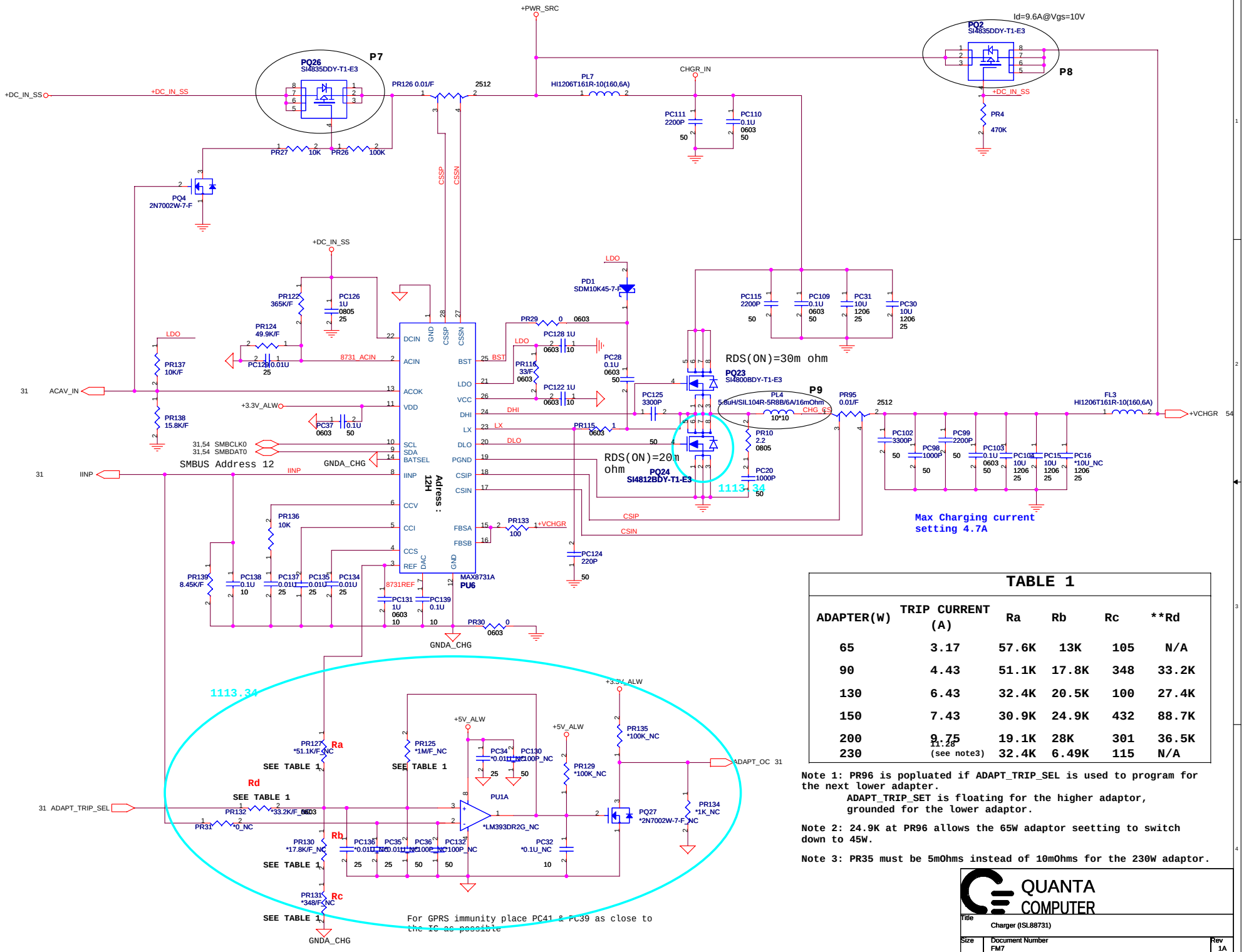


TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	Ra	Rb	Rc	**Rd
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28 (see note3)	32.4K	6.49K	115	N/A

Note 1: PR96 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR96 allows the 65W adaptor seetting to switch down to 45W.

Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.

QUANTA COMPUTER

Title	Charger (ISL88731)	
Size	Document Number FM7	Rev 1A
Date: Wednesday, July 30, 2008	Sheet 46 of 60	

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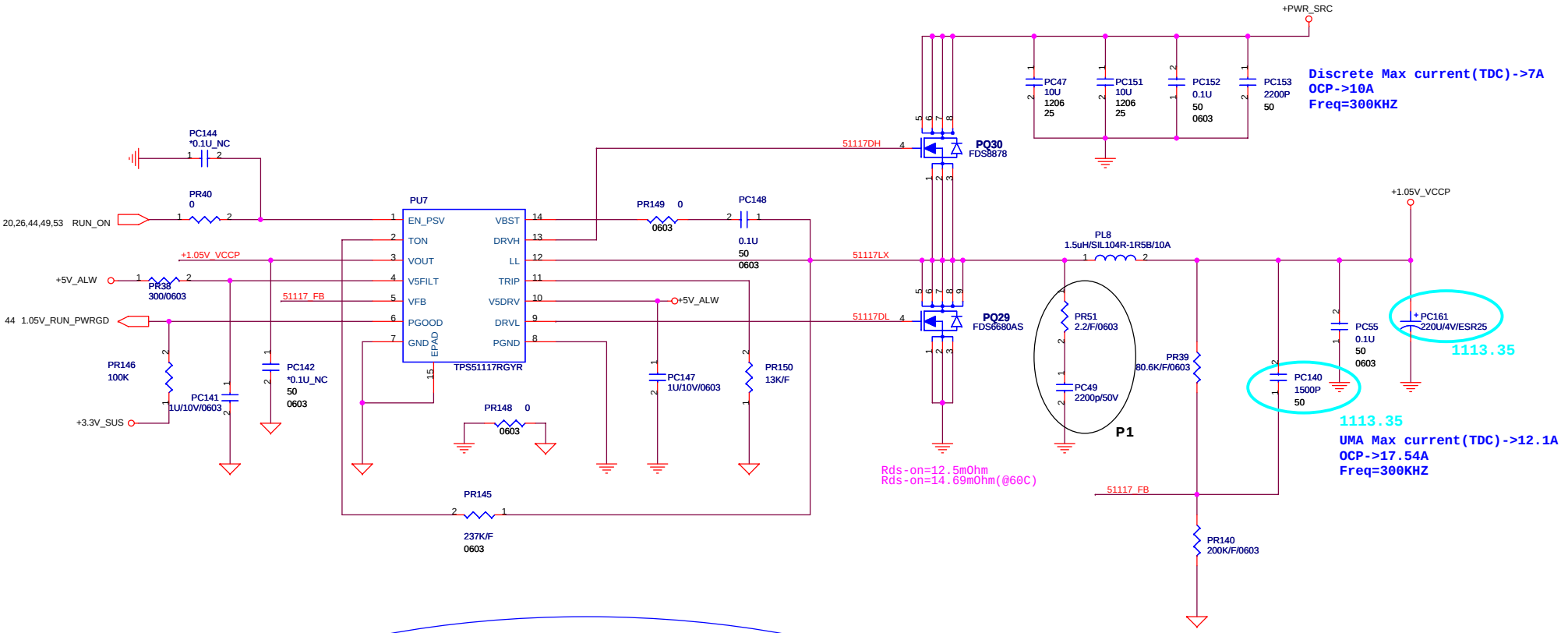
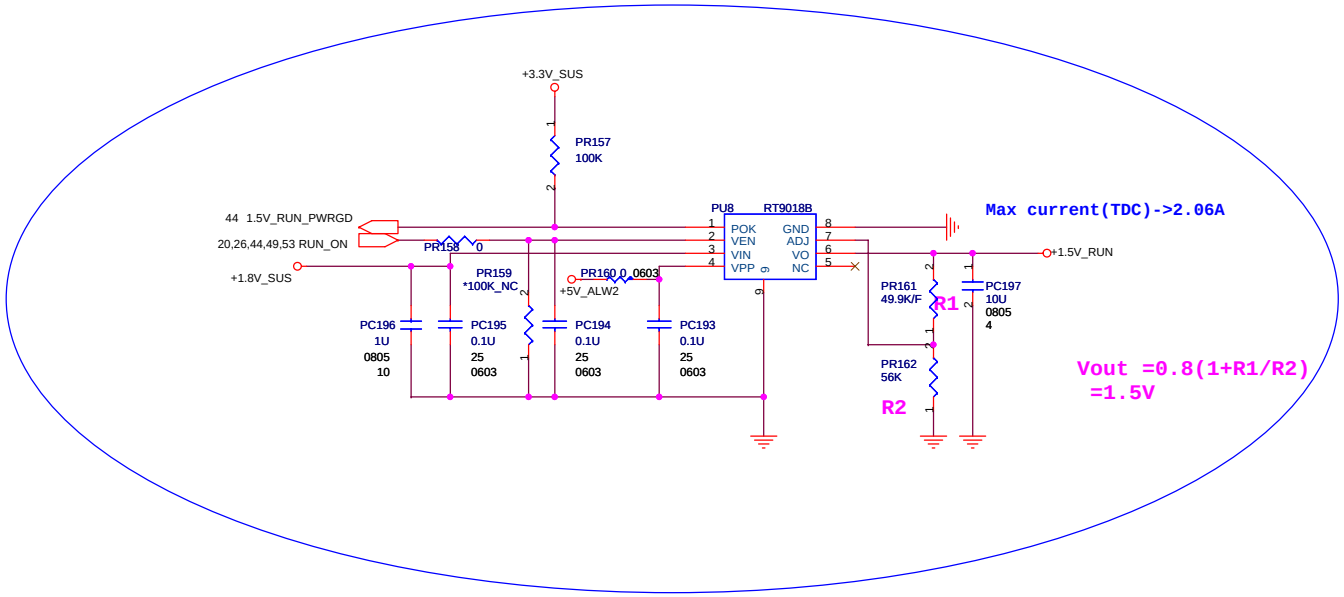
QUANTA COMPUTER

Title		
Size	Document Number FM7	Rev 1A
Date: Monday, June 30, 2008	Sheet 47 of 60	

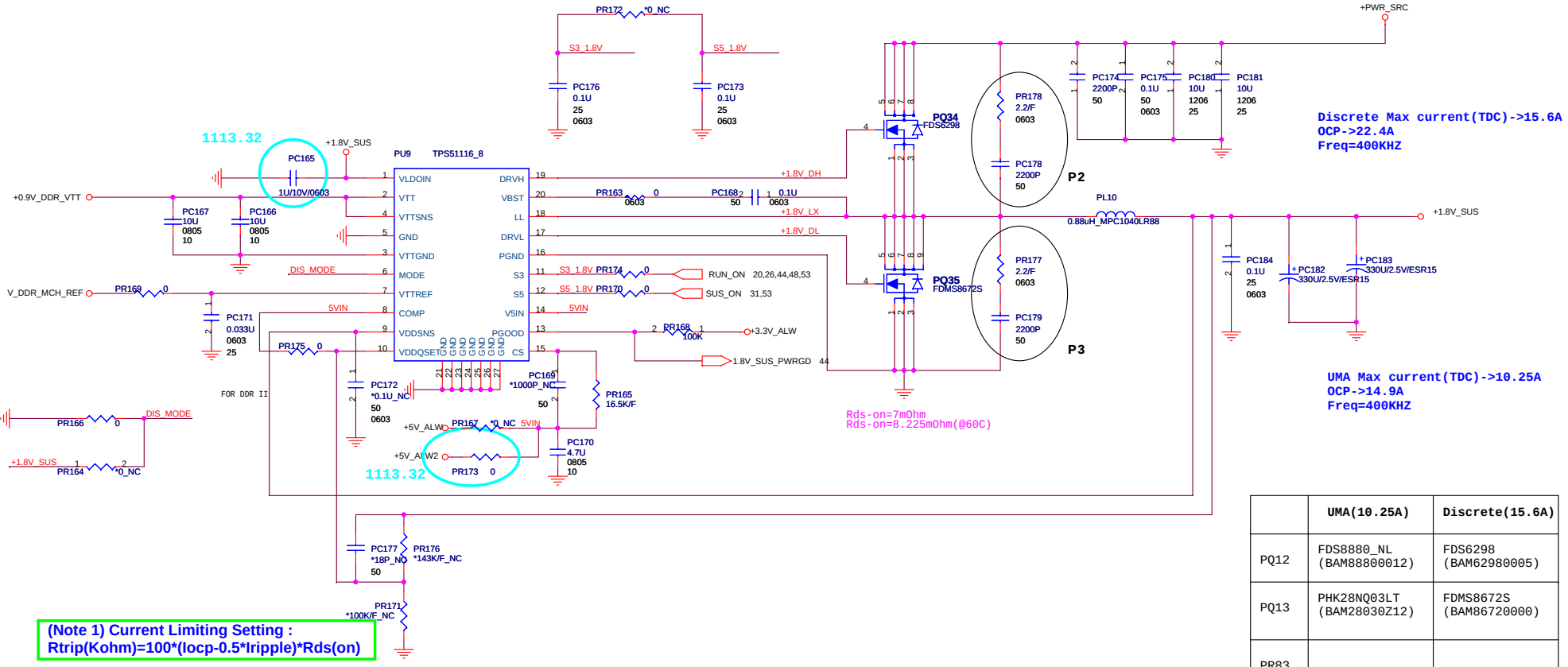




	UMA(12.1A)	Discrete(7A)
PQ22	FDS8880_NL (BAM88800012)	FDS8878 (BAM88780020)
PQ25	FDS6676AS_NL (BAM66760026)	FDS6680AS (BAM66800061)
PL25	SIL105RA-1R5-R (CV-15F0MZ08)	SIL104R-1R5PF (DC-15A00010)
PR452	9.09K/F (CS29092FB27)	10K/F (CS31002FB26)

QUANTA COMPUTER

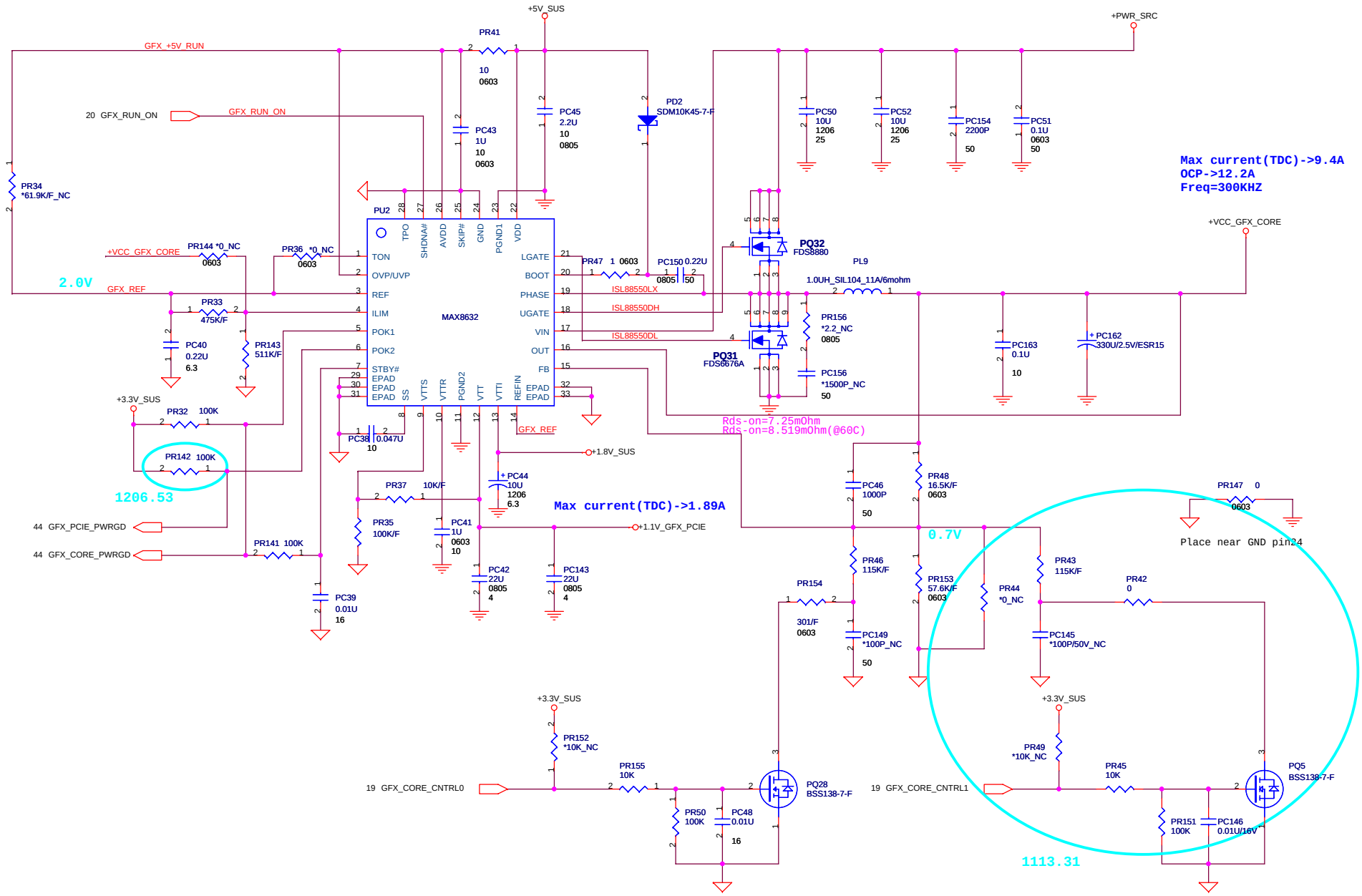
Title	1.05_VCCP & 1.5V_RUN	
Size	Document Number FM7	Rev 1A
Date: Wednesday, July 30, 2008	Sheet 48 of 60	



	UMA(10.25A)	Discrete(15.6A)
PQ12	FDS8880_NL (BAM88800012)	FDS6298 (BAM62980005)
PQ13	PHK28NQ03LT (BAM28030Z12)	FDMS8672S (BAM86720000)
PR83		

QUANTA COMPUTER

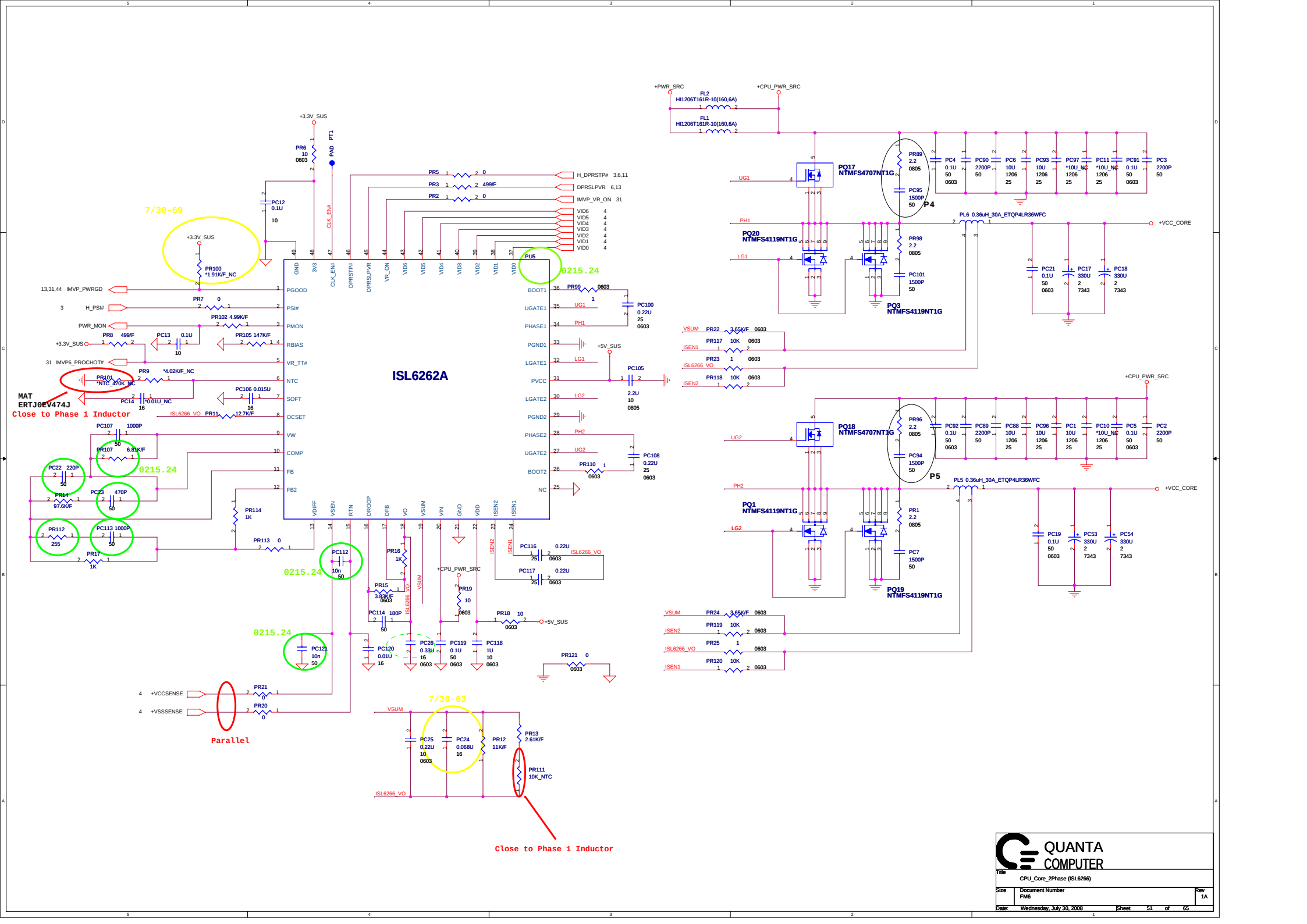
Title	1.8VSUS & 0.9VTT (TPS51116)	
Size	Document Number FM7	Rev 1A
Date: Thursday, July 31, 2008	Sheet 49 of 60	



GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9
HIGH	LOW	1.0V
HIGH	HIGH	1.1V

QUANTA COMPUTER

Title	VGA DC/DC	
Size	Document Number FM7	Rev 1A
Date: Wednesday, July 30, 2008	Sheet 50 of 60	


ISL6262A
+3.3V_SUS
+PWR_SRC
+CPU_PWR_SRC
+VCC_CORE
+5V_SUS
H_DPRSTP# 3,6,11
DPRSLPVR 6,13
IMVP_VR_ON 31
13,31,44 IMVP_PWRGD
3 H_PSI#
PWR_MON
31 IMVP6_PROCHOT#
PQ17 NTMFS4707NT1G
PQ20 NTMFS4119NT1G
PQ3 NTMFS4119NT1G
PQ18 NTMFS4707NT1G
PQ1 NTMFS4119NT1G
PQ19 NTMFS4119NT1G
P4
P5
PL6 0.36uH_30A_ETQP4LR36WFC
PL5 0.36uH_30A_ETQP4LR36WFC
FL2 HI1206T161R-10(160,6A)
FL1 HI1206T161R-10(160,6A)
7/30-69
7/30-63
0215.24
MAT ERTJ0EV474J
Close to Phase 1 Inductor
Parallel
Close to Phase 1 Inductor
4 +VCCSENSE
4 +VSSSENSE
QUANTA COMPUTER
Title CPU_Core_2Phase (ISL6266)
Size
Document Number FM6
Rev 1A
Date: Wednesday, July 30, 2008
Sheet 51 of 65

DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs

Max current->6A
OCP->8.3A
Freq=400KHZ

Max current->6.2A
OCP->8.63A
Freq=300KHZ

Rds-on=20mOhm
Rds-on=23.5mOhm(@60C)

Rds-on=20mOhm
Rds-on=23.5mOhm(@60C)

6/17-57
4/18-44

Title	3VALW,5V,3V, Power On
Size	Document Number FM7
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Date:	Thursday, July 31, 2008
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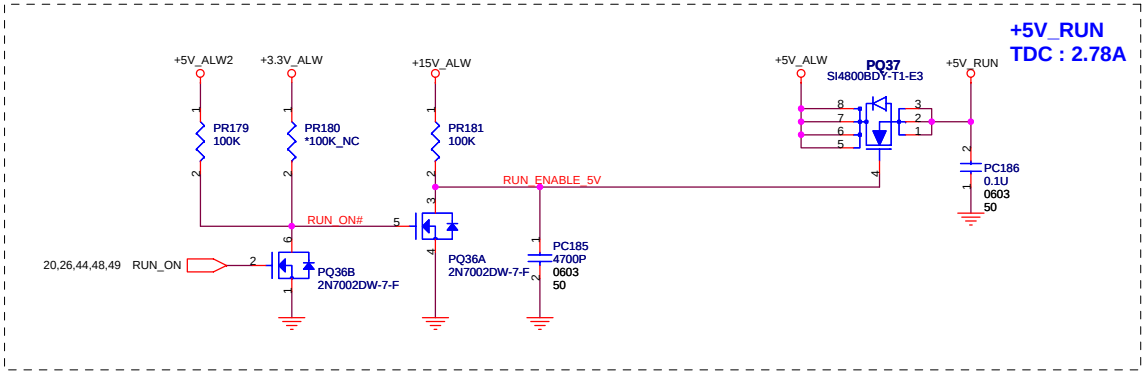
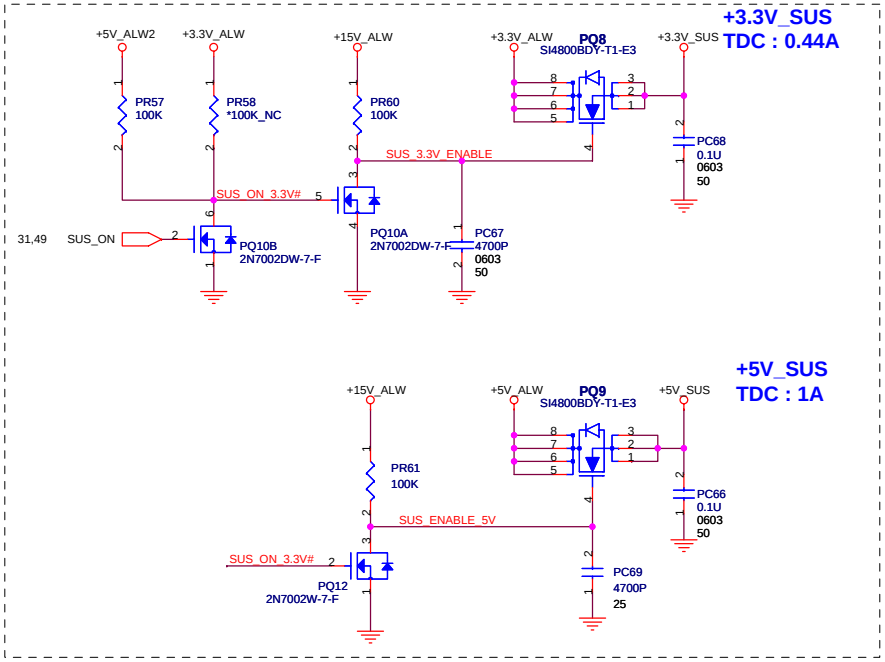
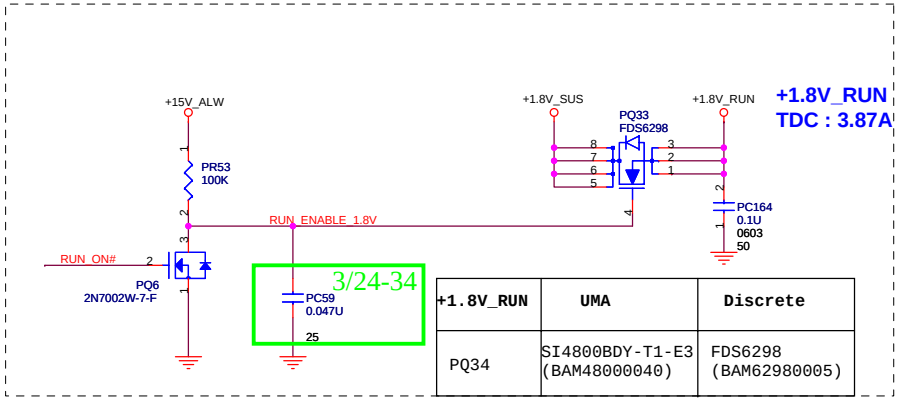
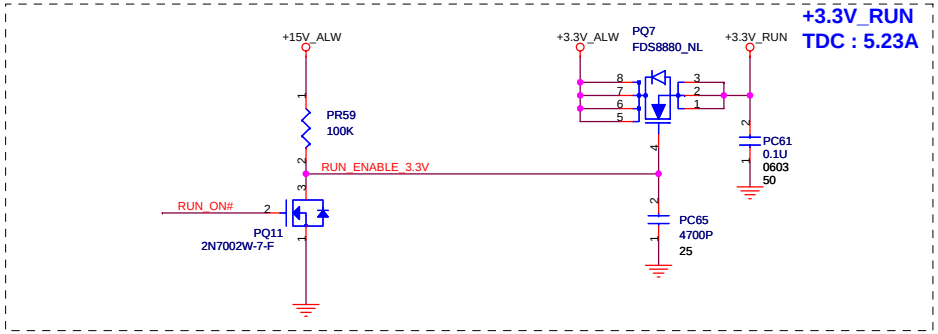
QUANTA COMPUTER

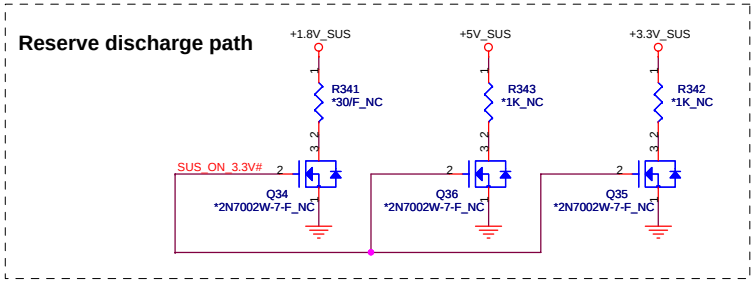


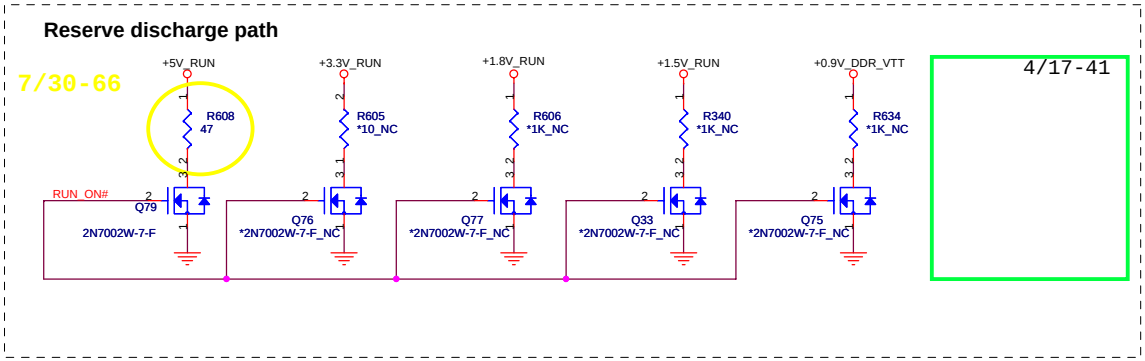




+1.8V_RUN	UMA	Discrete
PQ34	SI4800BDY-T1-E3 (BAM48000040)	FDS6298 (BAM62980005)

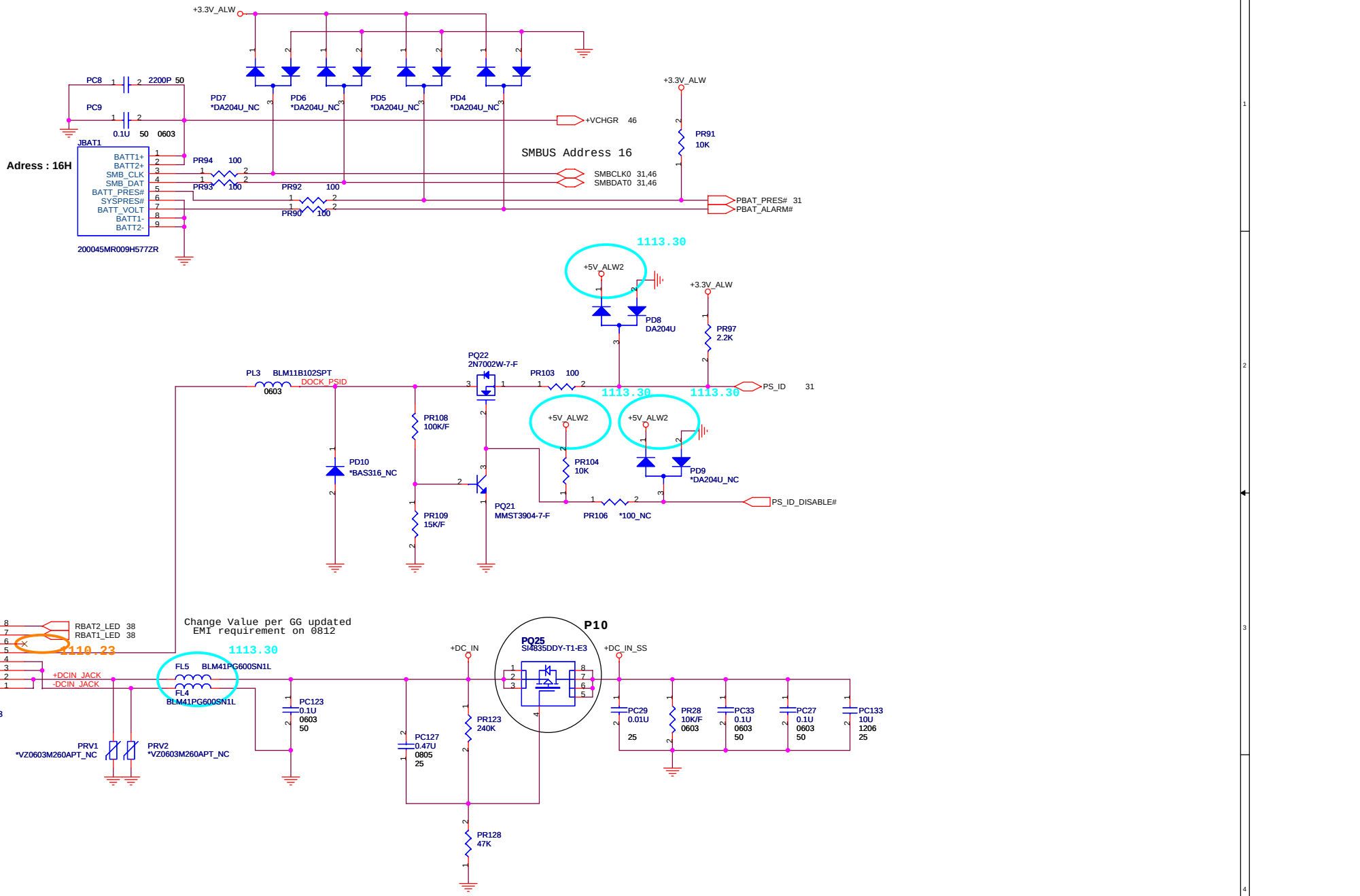






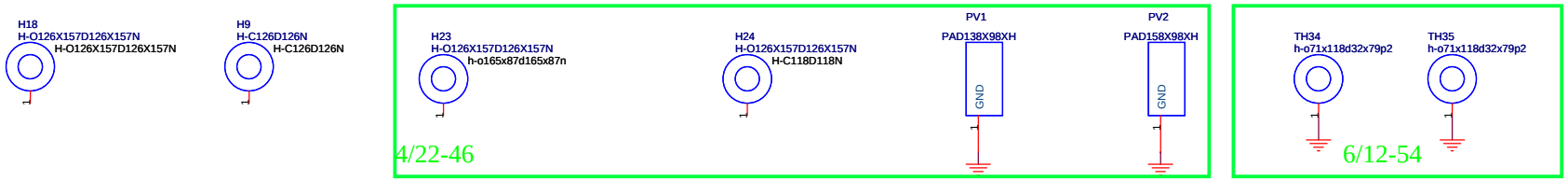
QUANTA COMPUTER

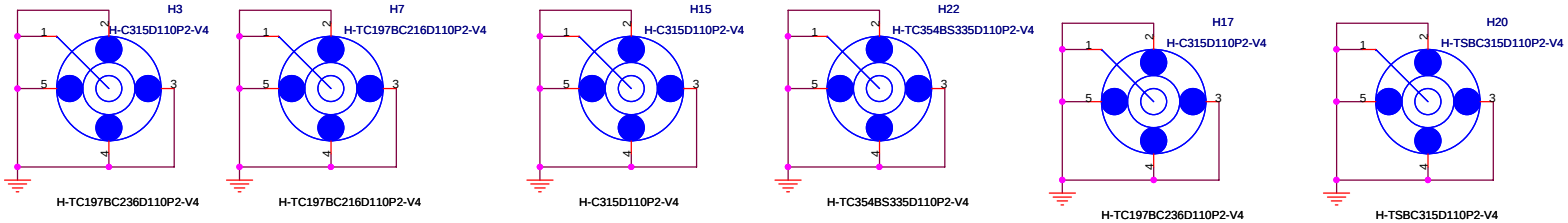
Title	RUN POWER SW	
Size	Document Number FM7	Rev 1A
Date: Wednesday, July 30, 2008	Sheet 53 of 60	

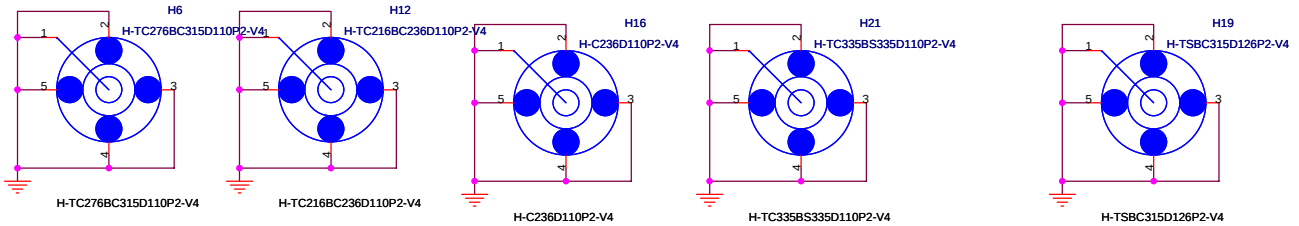


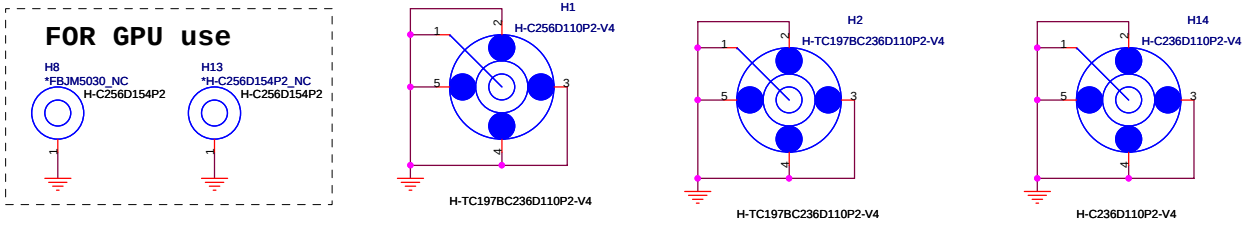
QUANTA COMPUTER

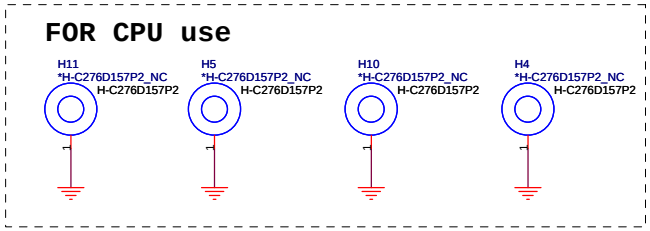
Title	DCIN,BATT CONNECTOR	
Size	Document Number FM7	Rev 1A
Date: Wednesday, July 30, 2008	Sheet 54 of 60	









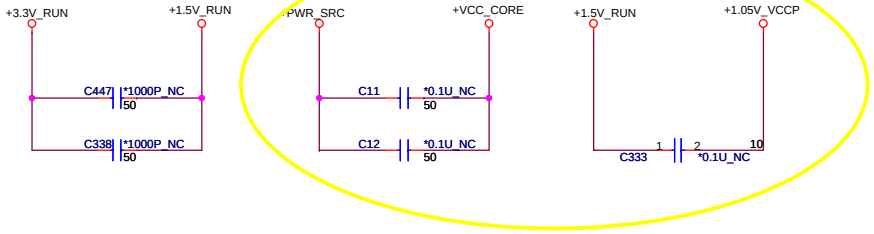


QUANTA COMPUTER

Title	SCREW PAD	
Size	Document Number FM6	Rev 2A
Date: Monday, June 30, 2008	Sheet 55 of 58	

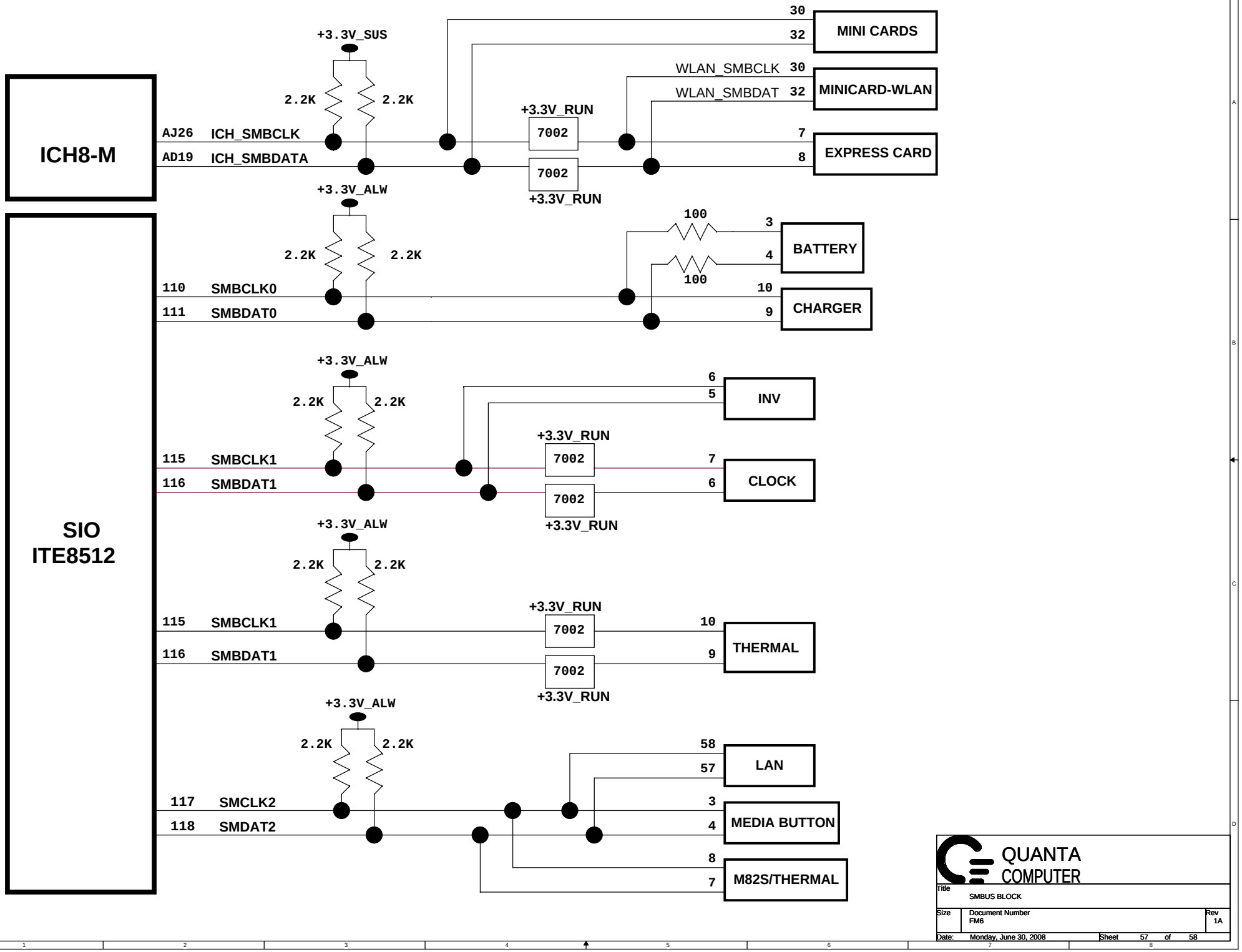
Reserved for EMI.

0906.1



QUANTA COMPUTER

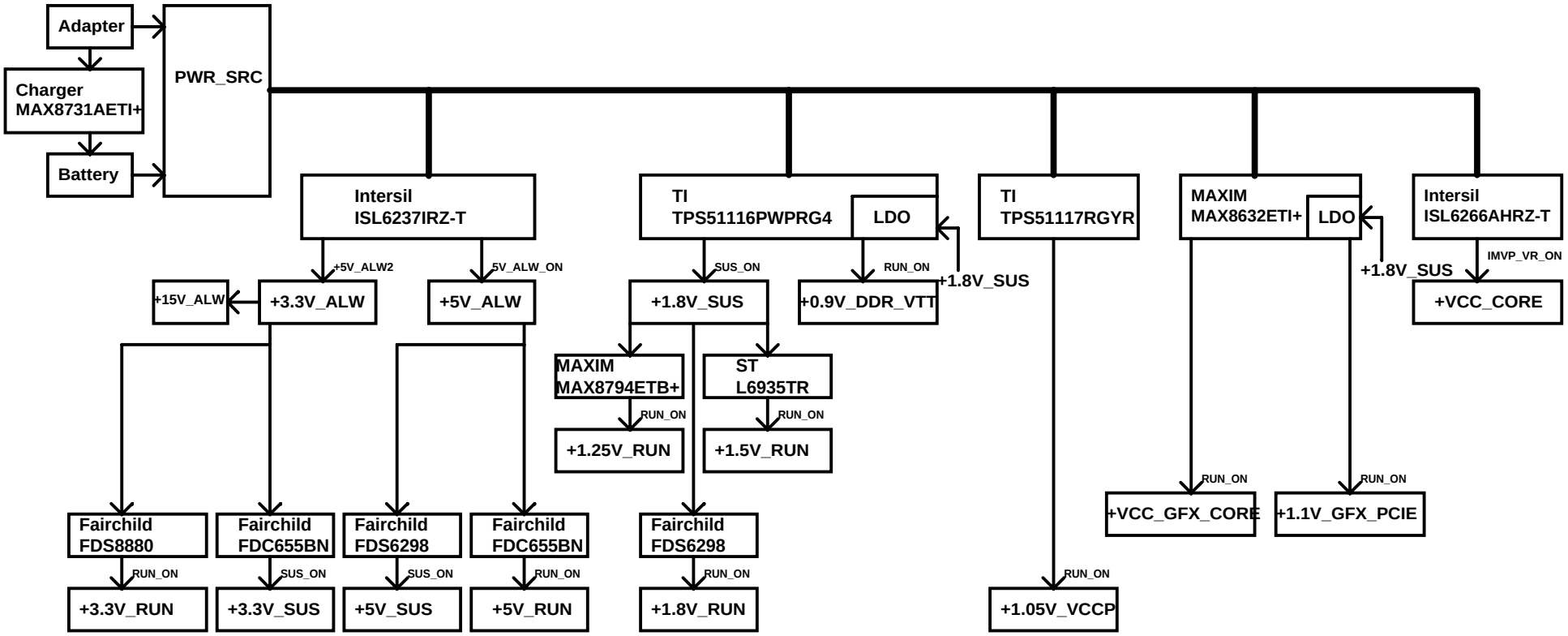
Title	EMI CAP	
Size	Document Number FM6	Rev 1A
Date: Monday, June 30, 2008	Sheet 56 of 58	



QUANTA COMPUTER

Title	SMBUS BLOCK	
Size	Document Number FM6	Rev 1A
Date: Monday, June 30, 2008	Sheet 57 of 58	

VER : 1A



QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number FM6	Rev 1A
Date: Monday, June 30, 2008	Sheet 58 of 58	

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
FM7	1	3	2-13-08				Debug port needs to be updated for MV	Change the BOM, and add a pull hign circuit on ITP_BPM#5
	2	3	2-13-08				H_THERM circuit has risk	Change the BOM in order to make it same with FM6
	3	8	2-13-08				VCC_AXG and VCC_AXG_NCTF are different with MV DG	Change VCC_AXG, and VCC_AXG_NCTF to ground
	4	11, 35	2-13-08				Add E-SATA function	Refer to page 11 and 35
	5	13	2-13-08				Some power rails don't mach with DG	Refer to page 13
	6	17	2-13-08				BSEL0, BSEL1, and BSEL2's seris resisters don't mach with DG	Refer to page 17
	7	9	2-13-08				VCCA_SM doesn't mach with DG	Add 0-ohm in order to make it same with other project
	8	9	2-13-08				VCCD_TVDAC and VCCD_QDAC are different with DG	Grond VCCD_TVDAC and update another circuit for VCCD_QDAC
	9	19,22	2-13-08				Change the power rail for avoiding leakage during power up	Change +3.3V_RUN to +3.3V_DELAY
	10	37	2-13-08				MMB vender changed it's F/W to fix the LED flash issue. Change Num/Cap LED circuit for avoiding leakage voltage	Change the circuit, refer to page 37
	11	35	2-13-08				Fulfill reliability's request	Add one more power pin on connector
	12	31	2-13-08				New chip version for ITE	Change the circuit
	13	40,42	2-13-08				Change chip version for Codec and LOM	Done
	14	41	2-13-08				Approve DMIC'S performance according to IDT's recommendation	Change o-ohm to 22-ohm
	15	26	2-16-08				DDC BUS for HDMI Certificate	Add Level Shift on DDC BUS of HDMI
	16	40,41	2-16-08				Need to meet WLP4.0	Refer to page 40 and 41
	17	31	2-16-08				Add audio solution for PO noise issue when loading driver	Connect ICH_AZ_CODEC_RST# to SIO.22
	18	14	2-18-08				Reserve +1.5V_SUS for VCCSUSHDA	Add a LDO and reserve 0-ohm for +1.5V_SUS
	19	13	2-18-08				Avoid leakage voltage	Follow the SR FM6 design
	20	17	2-19-08				After FAE review, modify circuit in order to let wave form smooth	Add two 0.1u cap
	21	17	2-20-08				After FAE review, modify circuit for single end nets	change 0-ohm to 33-ohm, add pull high resister
	22	35	2-20-08				Add E-SATA redriver function	Refer to page 35
	23	42	2-21-08				According to FAE, stub a resister	Refer to page 42
	24	17	2-21-08				In order to meet spec, we need to swap two signals	Refer to page 17
	25	35	2-22-08				Co-work with GM3 team and decide to take USB charger function off	Refer to page 35
	26	21	2-22-08				According to realiability team request, change BOM	Change L51
	27	12	2-25-08				Need to meet Dell USB port requirement	Refer to page 12
	28	19	2-25-08				FAE's suggestion is add ground	Refer to page 19
	29	13,37	2-25-08				Add one pin for LCD inventer det	Refer to pages
	30	30	3-03-08				Footprint is wrong for express card	Refer to FM6 footprint
	31	32 35	3-24-08				Change locations for USB and Coin Battery for safty requirement	Refer to those pages
	32	26 35	3-24-08				Change BOM for HDMI and E-sata	Refer to those pages
	33	49	3-24-08				Del 1.25V power rail	Refer to page 49
	34	53	3-24-08				Change BOM for correcting power sequence	Refer to page 53

QUANTA COMPUTER

Title	Change List	
Size	Document Number FM7	Rev 1A
Date: Wednesday, June 18, 2008	Sheet 1 of 6	

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
FM7	35	44	3-24-08				Change system reset circuit	Refer to page 44
	36	19	3-28-08				Change HDMI detect circuit	Refer to page 19
	37	26	3-28-08				In order to pass HDMI 7-13 item	Change diode, which has only 2pF internal capacitance
	38	31	3-28-08				ITE EC hardware issue	Del a cap
	39	1,31	4-03-08				Get schematic ready for PT build	Change block diagram and Board ID strap pin
	40	28	4-09-08				Leakage voltage issue	Change 0-ohm to diode
	41	53	4-17-08				1.25V_RUN discharge voltage is no need	Remove it
	42	30,35 26 27	4-17-08				EMI Issue	Refer to pages
	P1	48	4-17-08				For EMI suggested	populate 2.2ohm in PR56 and 1500pf in PC49
	P2	49	4-17-08				For EMI suggested	populate 2.2ohm in PR178 and 1500pf in PC178
	P3	49	4-17-08				For EMI suggested	populate 2.2ohm in PR177 and 1500pf in PC179
	P4	51	4-17-08				For EMI suggested	populate 2.2ohm in PR89 and 1500pf in PC95
	P5	51	4-17-08				For EMI suggested	populate 2.2ohm in PR96 and 1500pf in PC94
	P6	48	4-17-08				LDO cost issue	Change one LDO to another vender
	43		4-18-08				Change connectors PN due to connector list changes J2,JP1,JP2,J3,JSIM1,J5,J6,BT1., AND JDIM2	Refer to locations
	44	52	4-18-08				ATI OTP circuit redesigned	Refer to page 52
	45	28	4-18-08				the leakage voltage can be solved by EC	Change diode back to resister
	46	55	4-22-08				Layout team request two hole footprints and EMI spring	Refer to page 55
	47	37	4-22-08				K/B B/L circuit change to high active	Refer to page 37
	48	3 44	4-23-08				BOM change for CPU and system reset circuit	Change Resister value to 56 ohm for prochot pin and AND gate PN

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Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
FM7	49	38	5-29-08				The brightness is not light enough	Change R432 from 220 ohm to 68 ohm
	50	26	5-29-08				Secound sources team ask to change the diode PN.	Change D27 to another PN, which use on the other pages
	51	9	5-29-08				The diode PN is not on DELL PSL	Change PN
	52	35	5-29-08				Remove E-sata redriver	Refer to page 35
	53	13	6-11-08				Dell asks us to support KB_DET function	Add 0-ohm, which make the schematic work
	54	55	6-12-08				EMI request to change EMI spring PN and location Factory asks us to have a housing for CIR	Rerer to page 55
	55	40	6-16-08				Audio codec has new version	Change PN
	56	35	6-16-08				USB power IC is going to pass UL, so we will need to change it to new one	Change PN
	57	52	6-17-08				DELL's request on thermal detect pin	Refer to page 52
	58	3	6-27-08				Follow INTEL CRB and schematic checl list 2.0	De-pop H_RESET# PU resistor

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Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
FM7	59	31	6-30-08				1.System not stable2.RTC time reset3.BIOS crash issue4.RTC discharge then system can boot.	Add 1K pull-down on KBC 8512 pin 87 RESET_OUT#
	60	35,48,49, 50,52	7-10-08				FM7 forward to QT status	Remove all debug power jumps
	61	40	7-10-08				Pin 1 V_high is lower than +VDDA*0.7	Change U41 P/N to ALCT1G86000,cause its Vih=2V
	62	30	7-30-08				MS card test fail, and EMI request	Change 27P to 22P
	63	51	7-30-08				Power Team ask to change the value from 0.022u to 0.068u	Refer to the Page 51
	64	31	7-30-08				Board ID Straps	Change Board ID Straps
	65	26	7-30-08				Fix 7-13 HDMI issue	Add 0805 0 ohm at D27 location
	66	53	7-30-08				Fix 7-13 HDMI issue	Pop Q79, R608 and R608=47
	67	31	7-30-08				Cold boot issue	Refer tp Page 31
	68	13	7-30-08				Change the power from +3.3V_SUS to +3.3_RUN	Change the value of R247(1.91K)
	69	51	7-30-08				Change the power from +3.3V_SUS to +3.3_RUN	Del PR100
	70	17,33	7-30-08				Remove debug function	Refer tp P17,P33
	71	44	8-01-08				Reserve 3.3V_SUS and 3.3V_ALW power	Refer tp P44

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