

Compal Confidential

Schematic Document

MCP79-MX

2009 / 02 / 19 Rev:1.0

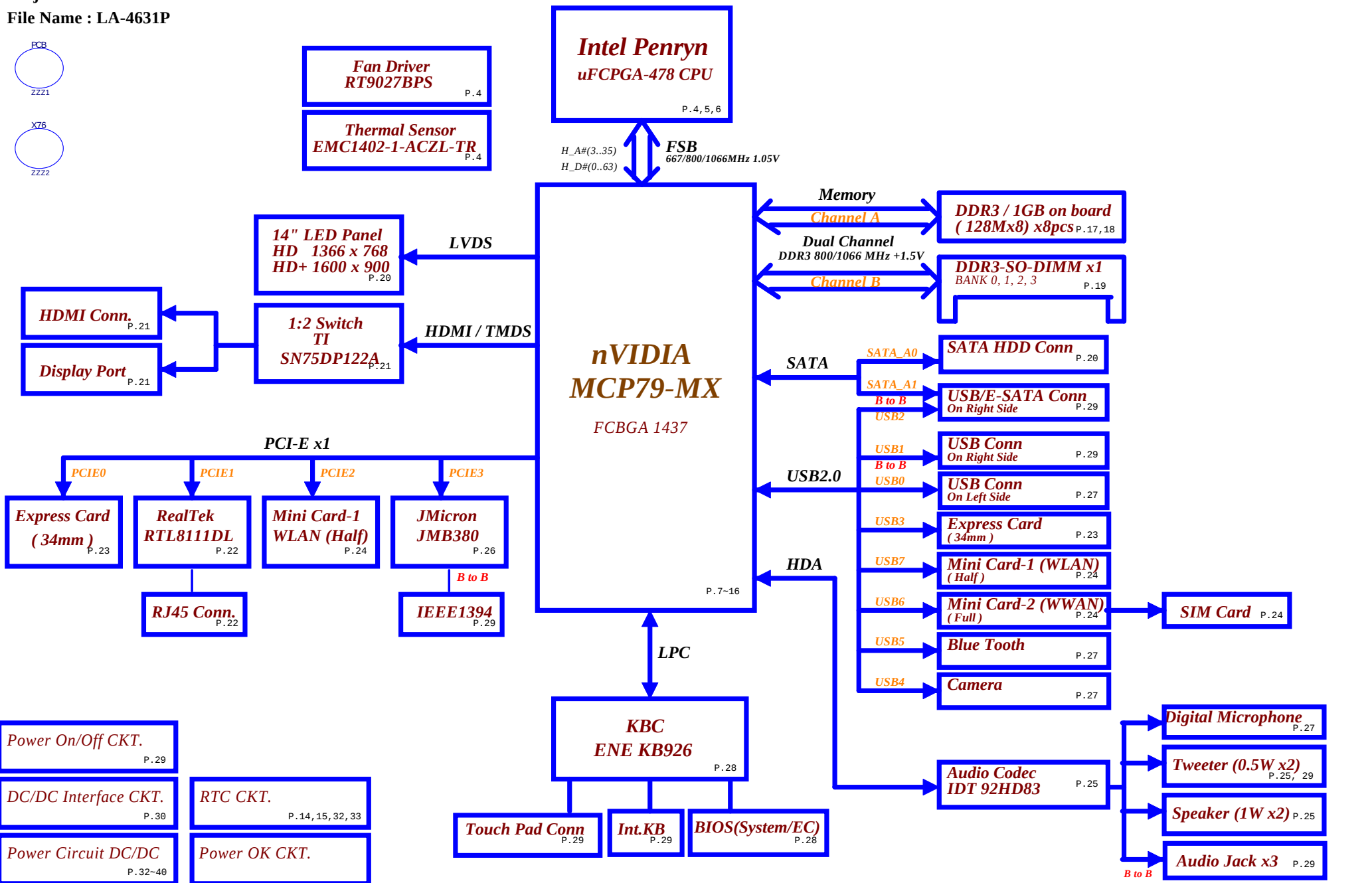
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Cover Sheet	
2009/02/19		2009/12/31		Document Number	
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Compal confidential

Project Code: KCM00

File Name : LA-4631P

Braxton 14"

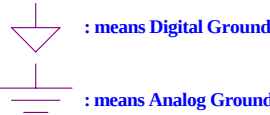


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Issued Date	2009/02/19	Deciphered Date	2009/12/31	Block Diagram	
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Voltage Rails 0 MEANS ON X MEANS OFF

power plane	State				
		+B	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +1.8VS +1.1VS +VCCP +1.0VS +0.75VS +CPU_CORE +1.5VS
S0	0	0	0	0	0
S1	0	0	0	0	0
S3	0	0	0	0	X
S5 S4/AC	0	0	X	X	X
S5 S4/ Battery only	0	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

Symbol Note :



@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	18K +/- 5%	0.436 V	0.503 V	0.538 V
2	33K +/- 5%	0.712 V	0.819 V	0.875 V
3	56K +/- 5%	1.036 V	1.185 V	1.264 V
4	100K +/- 5%	1.453 V	1.650 V	1.759 V
5	200K +/- 5%	1.935 V	2.200 V	2.341 V
6	NC	2.500 V	3.300 V	3.300 V
7				

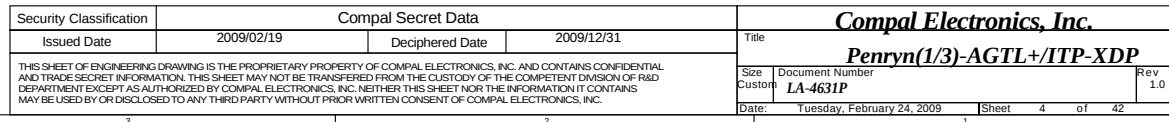
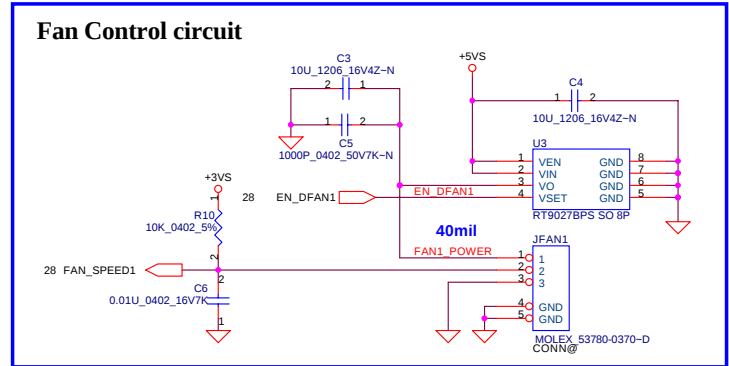
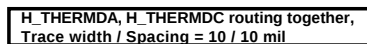
BOARD ID Table

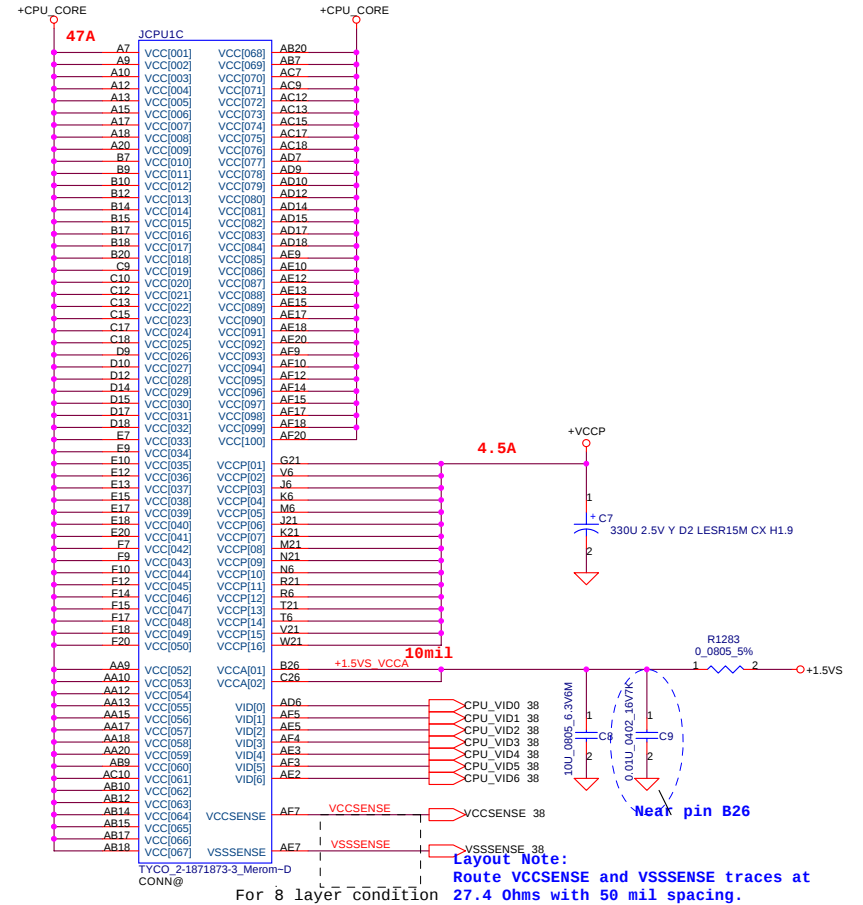
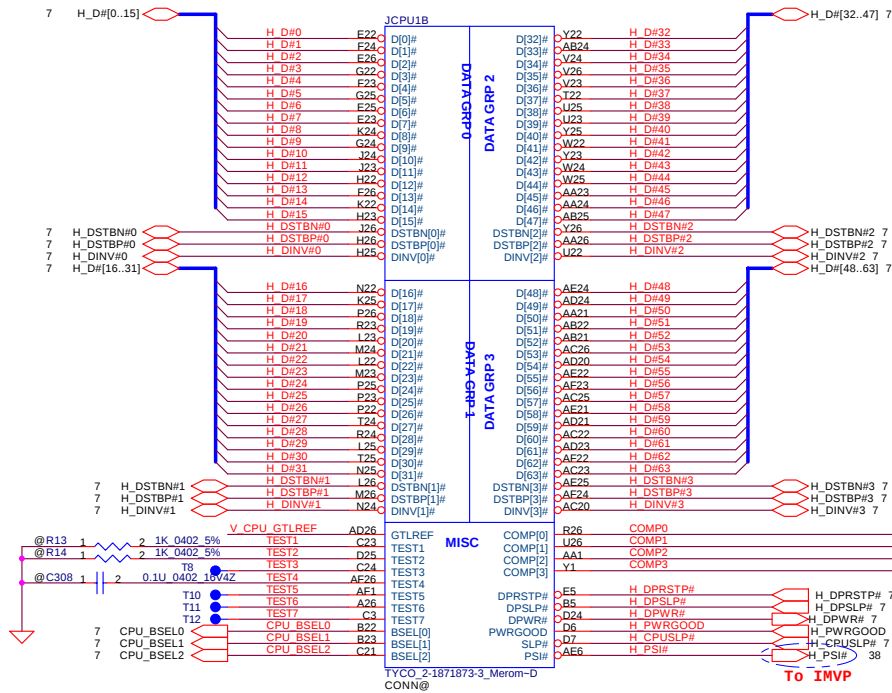
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	1.0
6	
7	

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	EXP CARD	MINI CARD1	MINI CARD2
EC_SMB_CK1 EC_SMB_DA1	KB926	X	V	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	V	X	X	X	X
MEM_SMBCLK MEM_SMBDATA	MCP79	X	X	X	X	V	X	X	X
MCP_SMB_CLK MCP_SMB_DATA	MCP79	X	X	X	X	X	V	V	V

MINI CARD 1 RESERVED +3VALW TO PULL HIGH

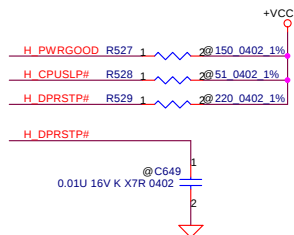




layout note: Rout H_DPRSTP# from ICH9 to IMPV6 then to GMCH & CPU

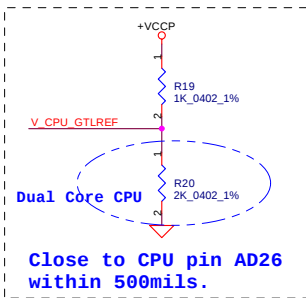
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



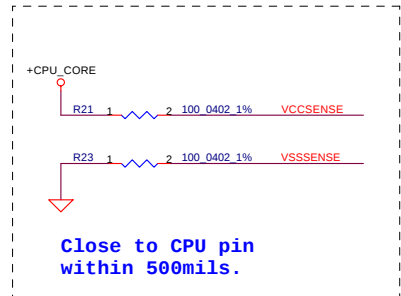
49.9 25.5 29.9 25.5

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4



For 6 layer
Z=27.4 ohm
VCCSENSE, VSSSENSE/ 14mils (MS),
16mils (SL) width, 7mils space, 25mils
space to other signals Mismatch =25mils.

Length match within 25 mils.
The trace width/space/other is
20/7/25.



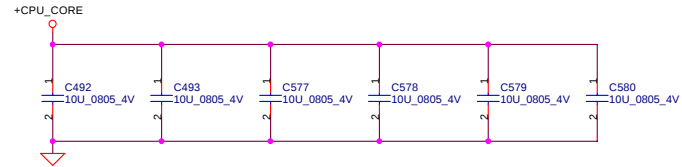
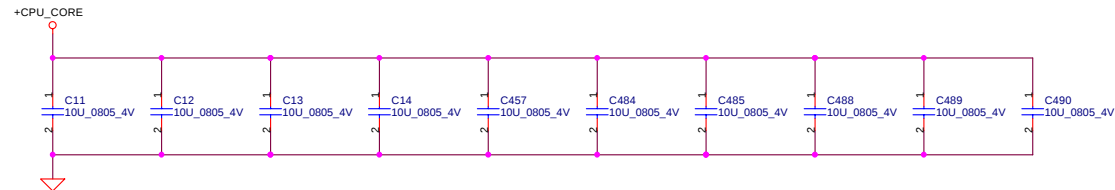
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Near CPU CORE regulator

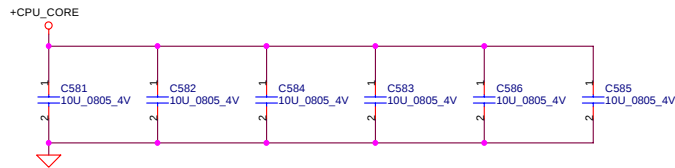
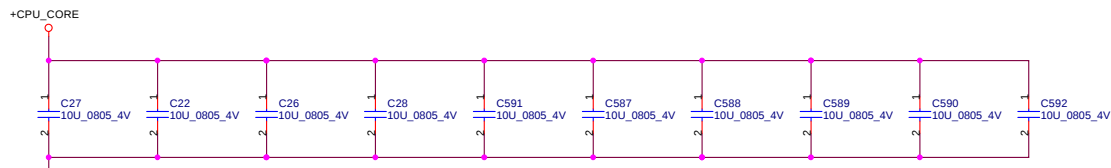
ESR <= 1.5m ohm
Capacitor > 1980uF

JCPU1D		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
A62	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B13	VSS[012]	U3
B16	VSS[013]	U6
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	V2
C5	VSS[017]	V5
C8	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W4
C19	VSS[022]	W23
C2	VSS[023]	W26
C22	VSS[024]	Y3
C25	VSS[025]	Y6
D1	VSS[026]	Y21
D4	VSS[027]	Y24
D8	VSS[028]	AA2
D11	VSS[029]	AA5
D16	VSS[030]	AA11
D19	VSS[031]	AA12
D23	VSS[032]	AA14
D26	VSS[033]	AA16
E3	VSS[034]	AA19
E6	VSS[035]	AA22
E8	VSS[036]	AA25
E11	VSS[037]	AB1
E14	VSS[038]	AB4
E16	VSS[039]	AB8
E19	VSS[040]	AB11
E21	VSS[041]	AB13
E24	VSS[042]	AB16
F5	VSS[043]	AB19
F8	VSS[044]	AB23
F11	VSS[045]	AB26
F13	VSS[046]	AC3
F16	VSS[047]	AC6
F19	VSS[048]	AC8
F2	VSS[049]	AC11
F22	VSS[050]	AC14
F25	VSS[051]	AC16
G4	VSS[052]	AC19
G1	VSS[053]	AC21
G23	VSS[054]	AC24
G26	VSS[055]	AD2
H3	VSS[056]	AD5
H6	VSS[057]	AD8
H21	VSS[058]	AD11
H24	VSS[059]	AD13
J2	VSS[060]	AD16
J5	VSS[061]	AD19
J22	VSS[062]	AD22
J25	VSS[063]	AD25
K1	VSS[064]	AE1
K4	VSS[065]	AE4
K23	VSS[066]	AE8
K26	VSS[067]	AE11
L3	VSS[068]	AE14
L6	VSS[069]	AE16
L21	VSS[070]	AE19
L24	VSS[071]	AE23
M2	VSS[072]	AE26
M5	VSS[073]	A2
M22	VSS[074]	AF6
M25	VSS[075]	AF8
N1	VSS[076]	AF11
N4	VSS[077]	AF13
N23	VSS[078]	AF16
N26	VSS[079]	AF19
P3	VSS[080]	A25
	VSS[081]	AF25

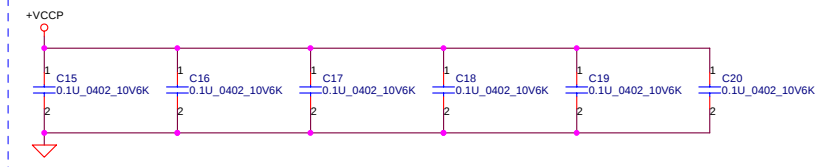
TYCO_2-1871873_3_Merom-D
CONN@



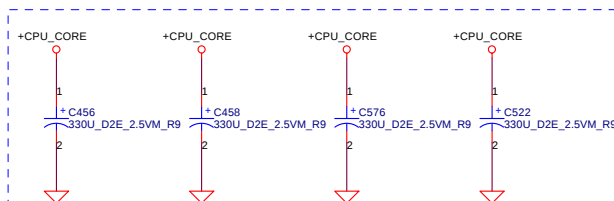
16pcs on TOP side



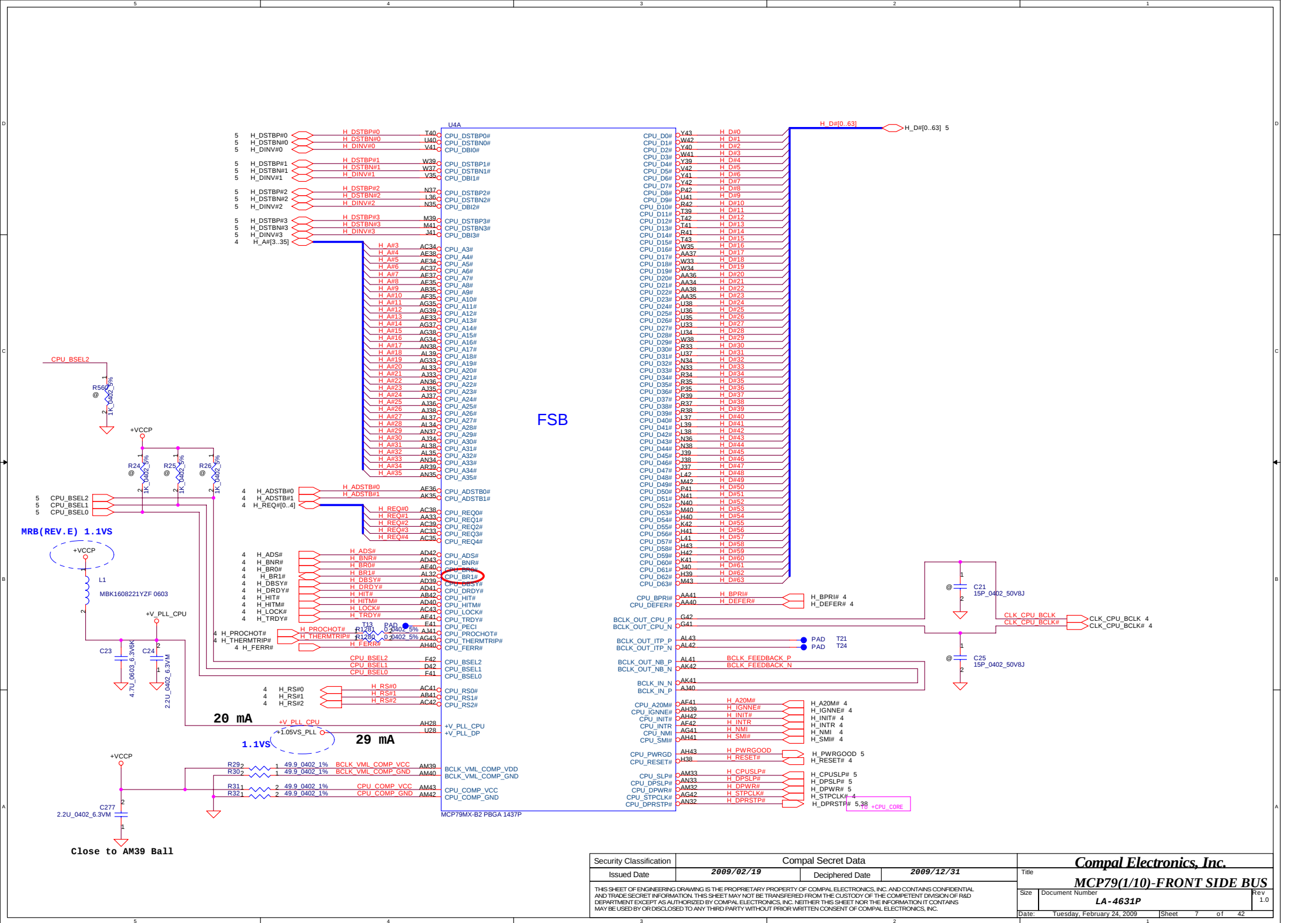
16pcs on bottom side

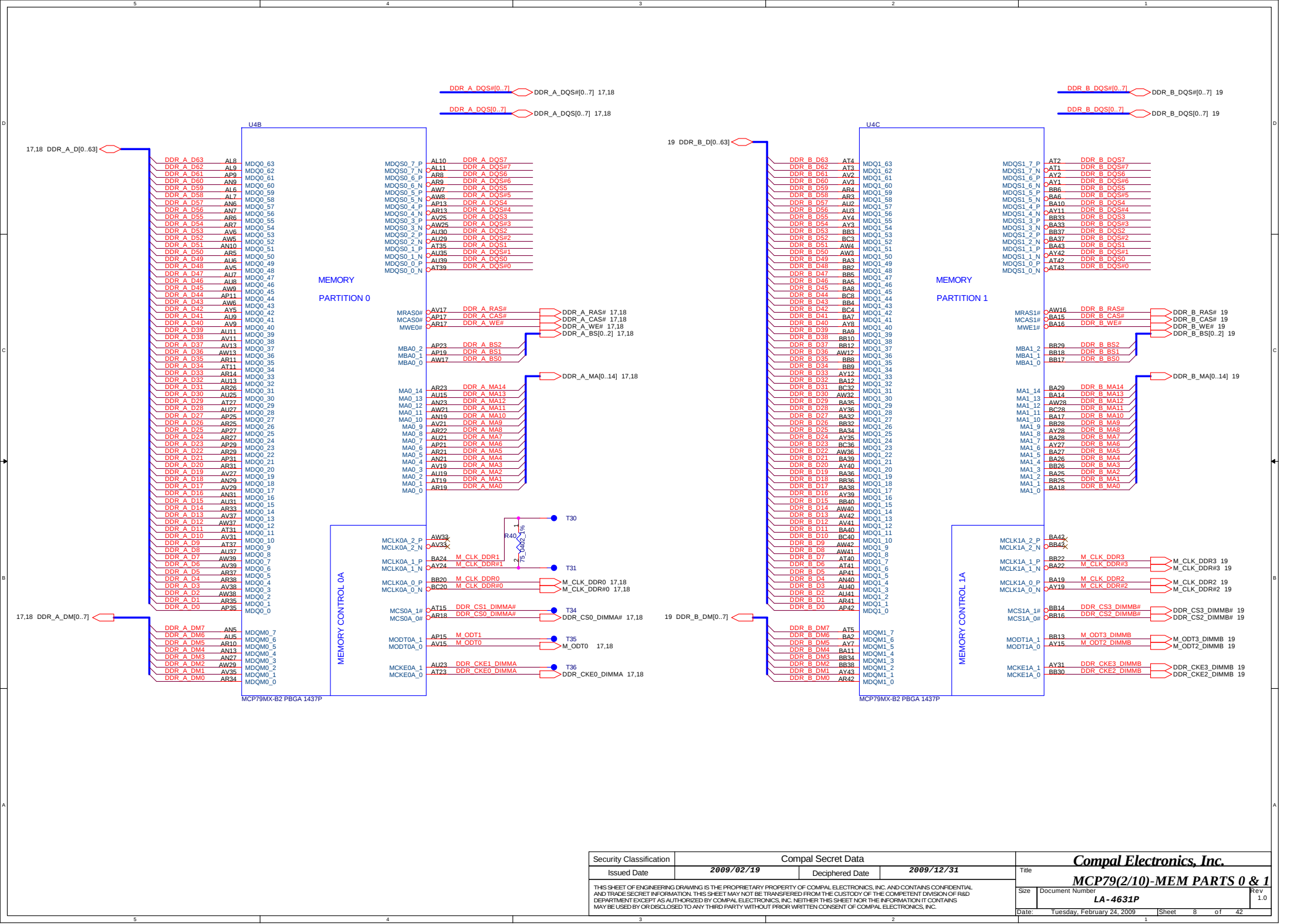


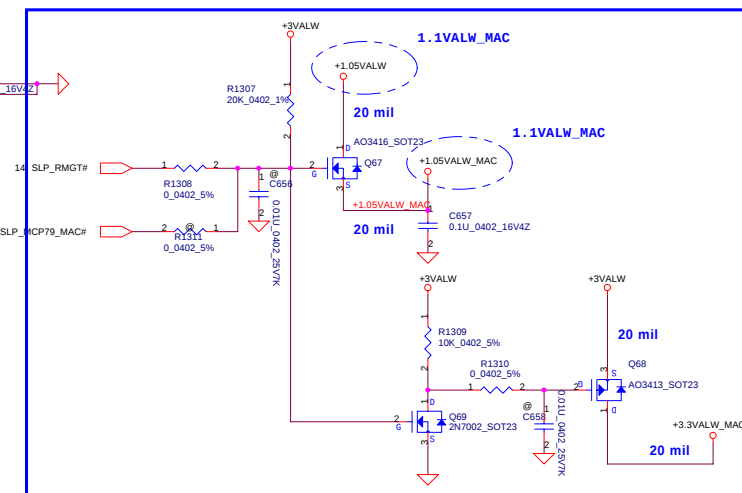
Place these caps inside the
socket cavity on Bottom side.
(North side Secondary)



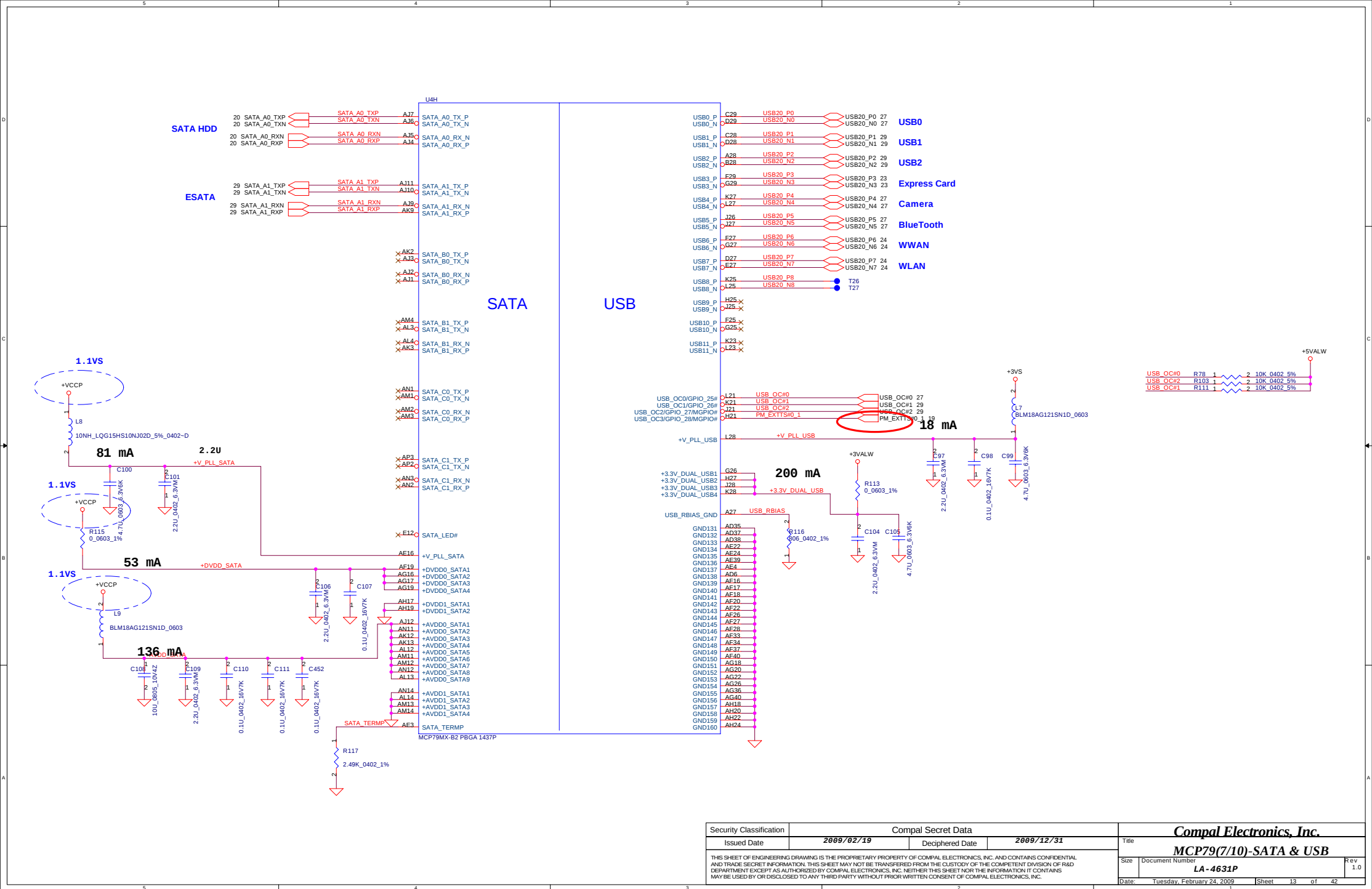
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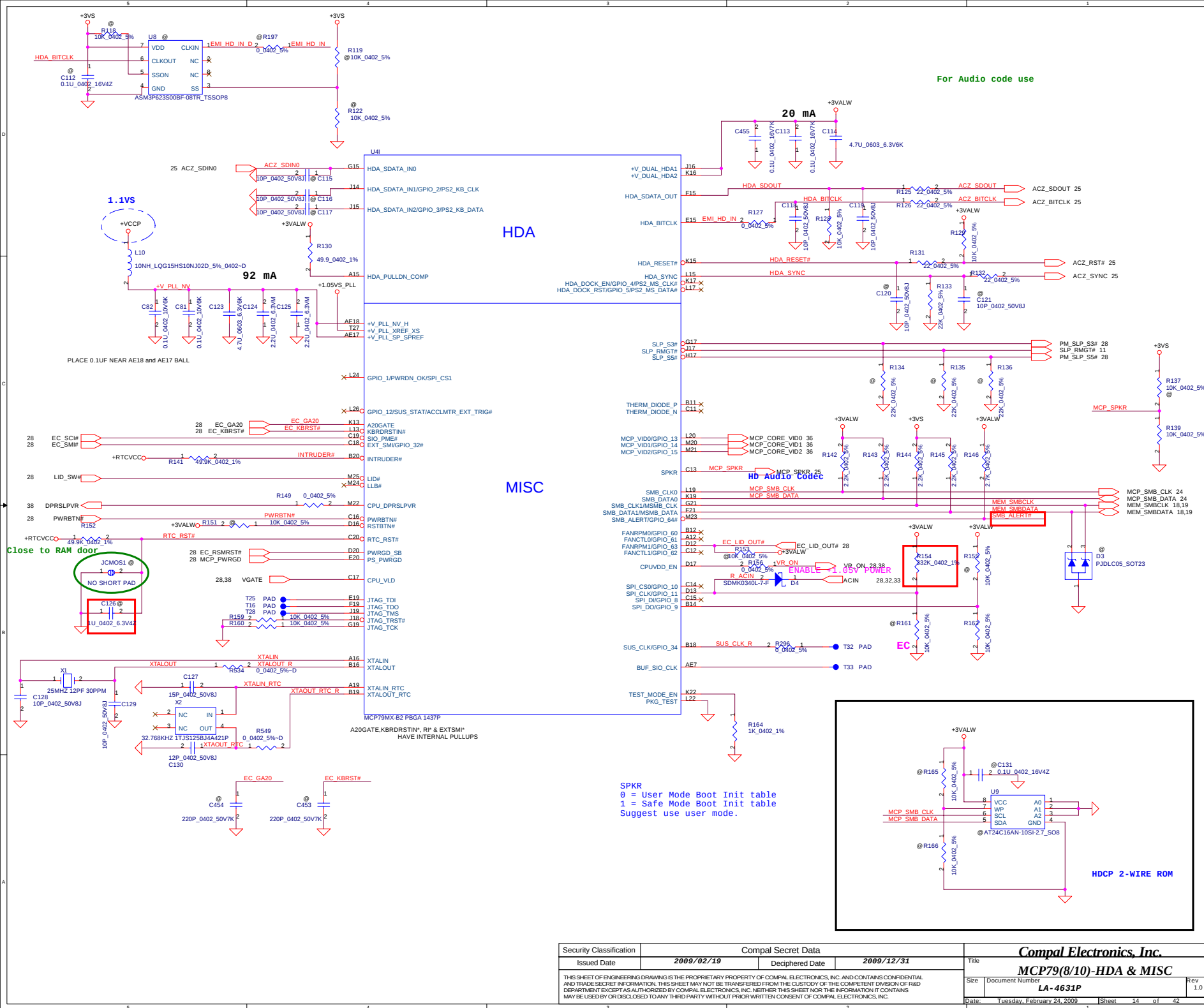




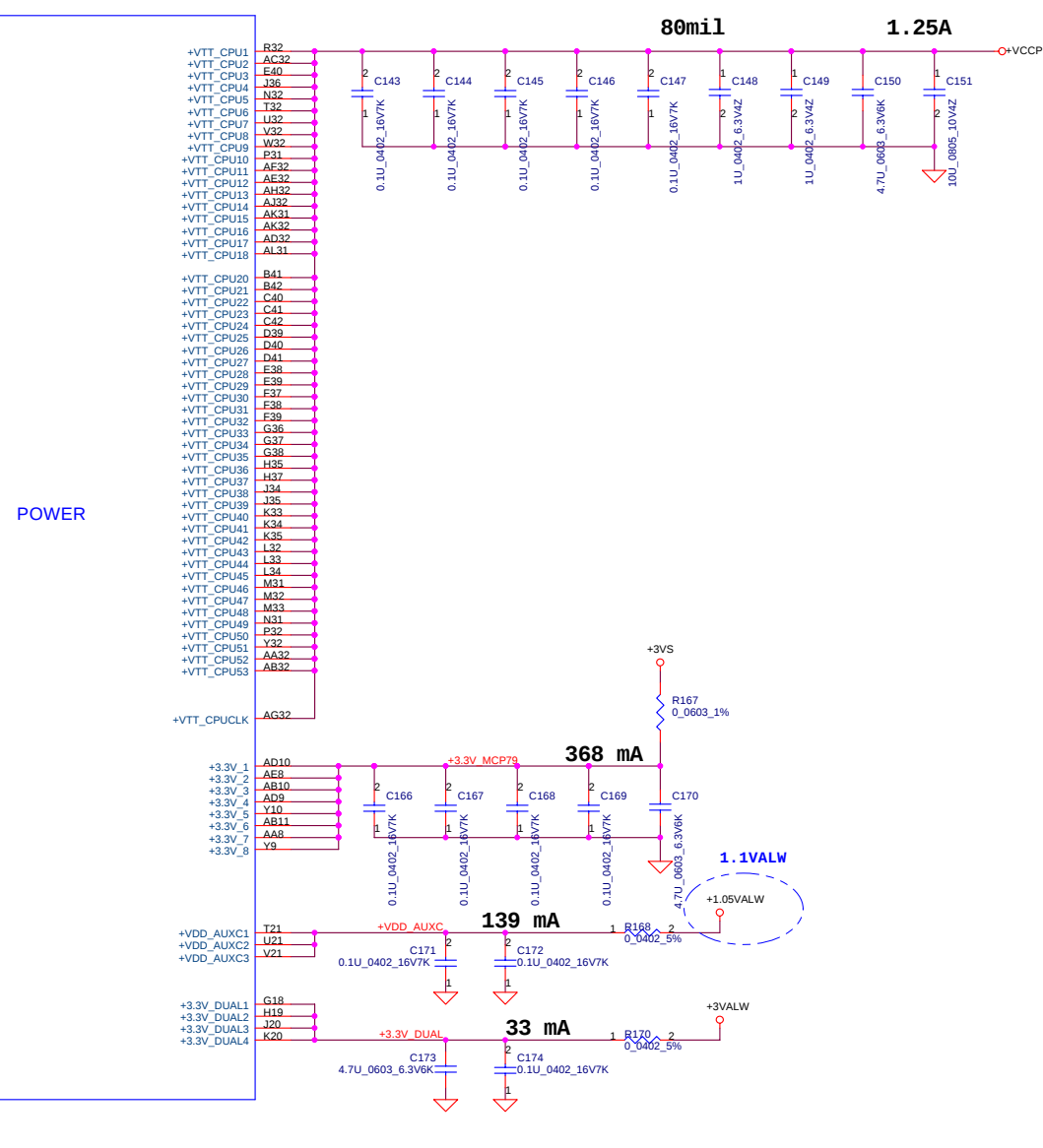
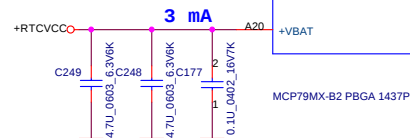
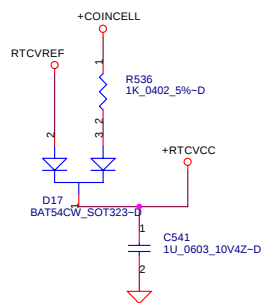
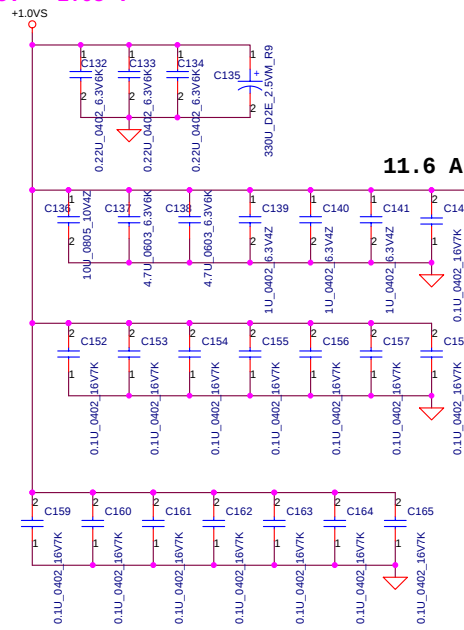


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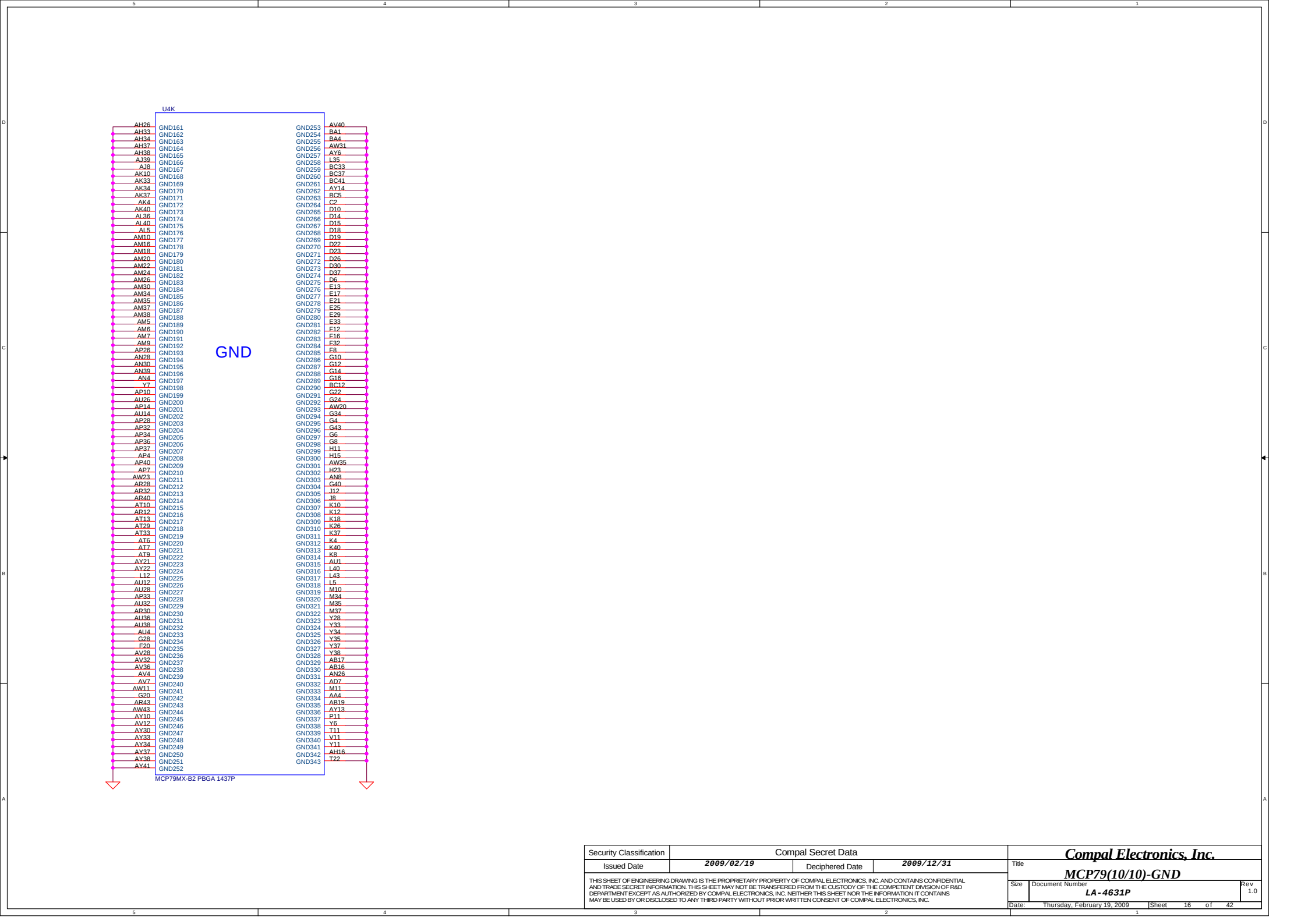




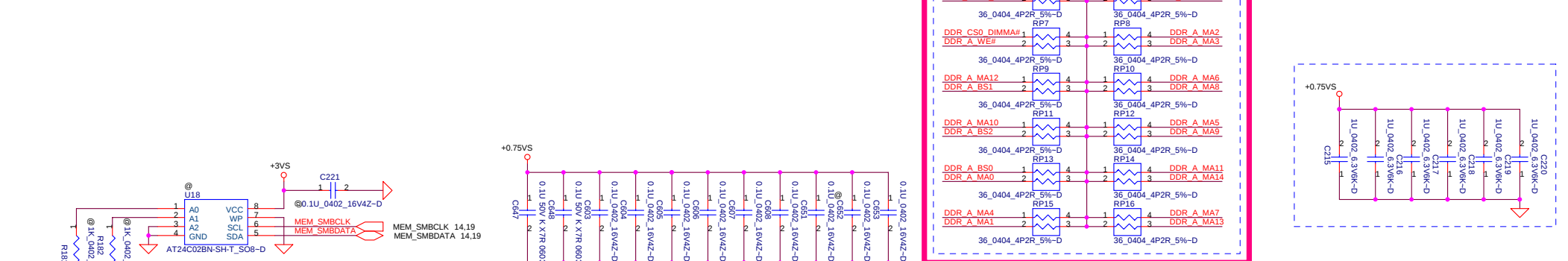
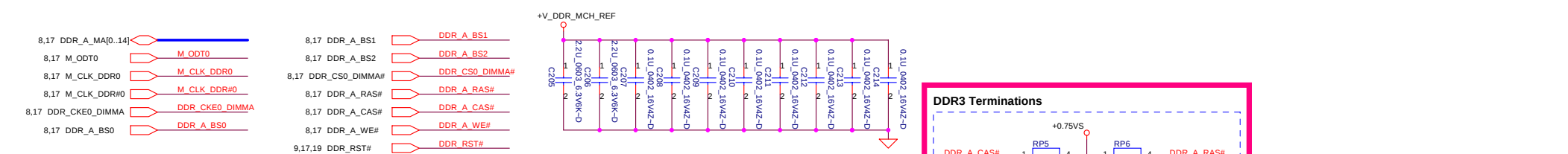
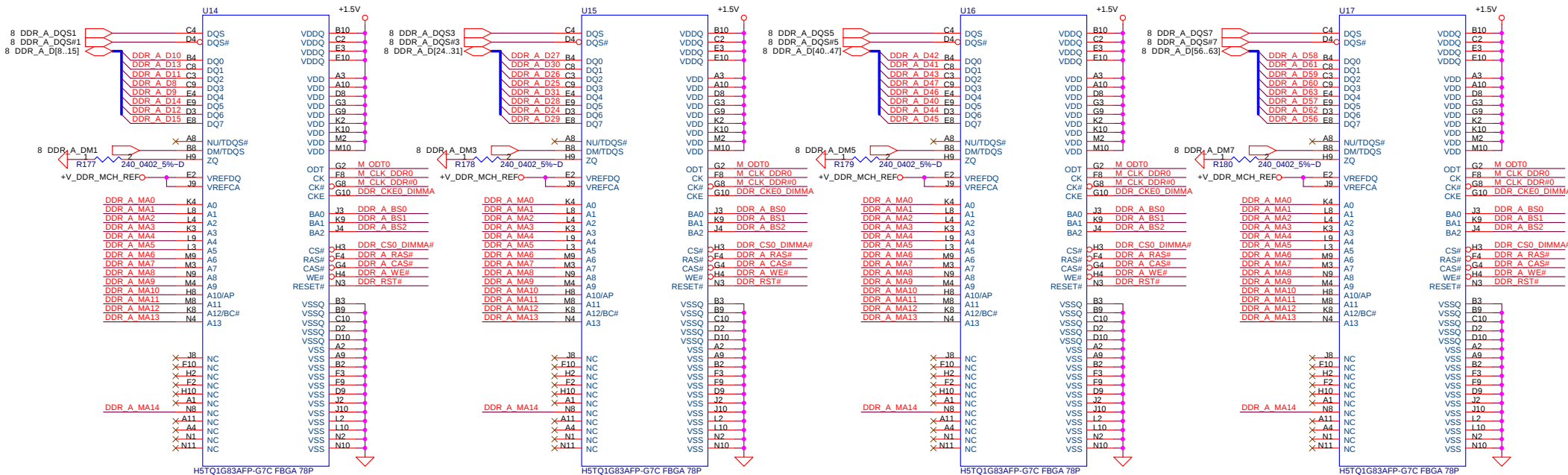
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Place decaps close end termination resistors, one decap for 4 resistors

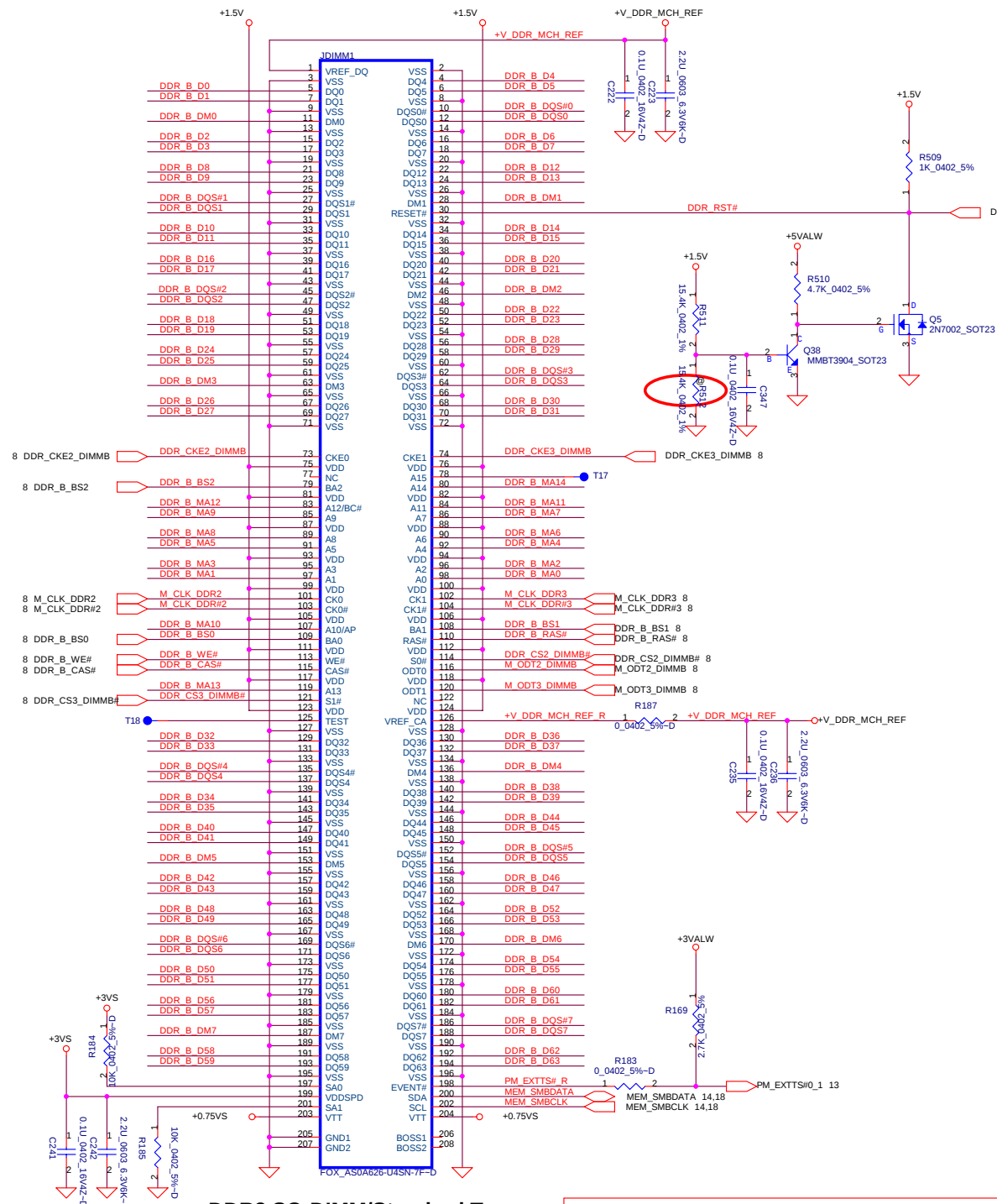
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Compal Electronics, Inc.

DDRIII-Memory Down (Bottom)

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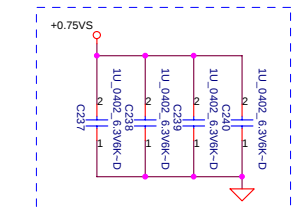
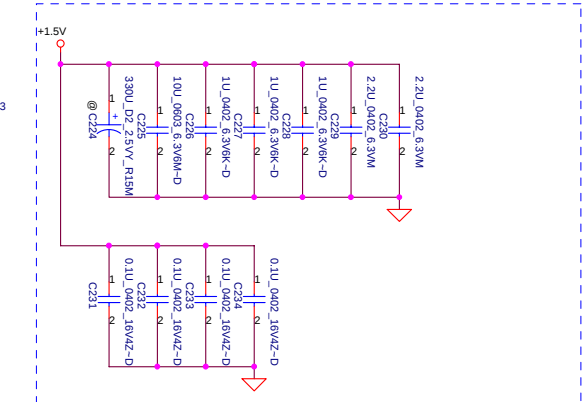


DDR3 SO-DIMM/Standard Type

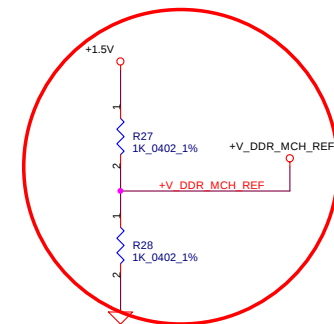
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- 8 DDR_B_D[0..63]
- 8 DDR_B_DQS[0..7]
- 8 DDR_B_DQS[0..7]
- 8 DDR_B_DM[0..7]
- 8 DDR_B_MA[0..14]

Place close to SO-DIMM



Place close to JDIMM pin 203 and 204



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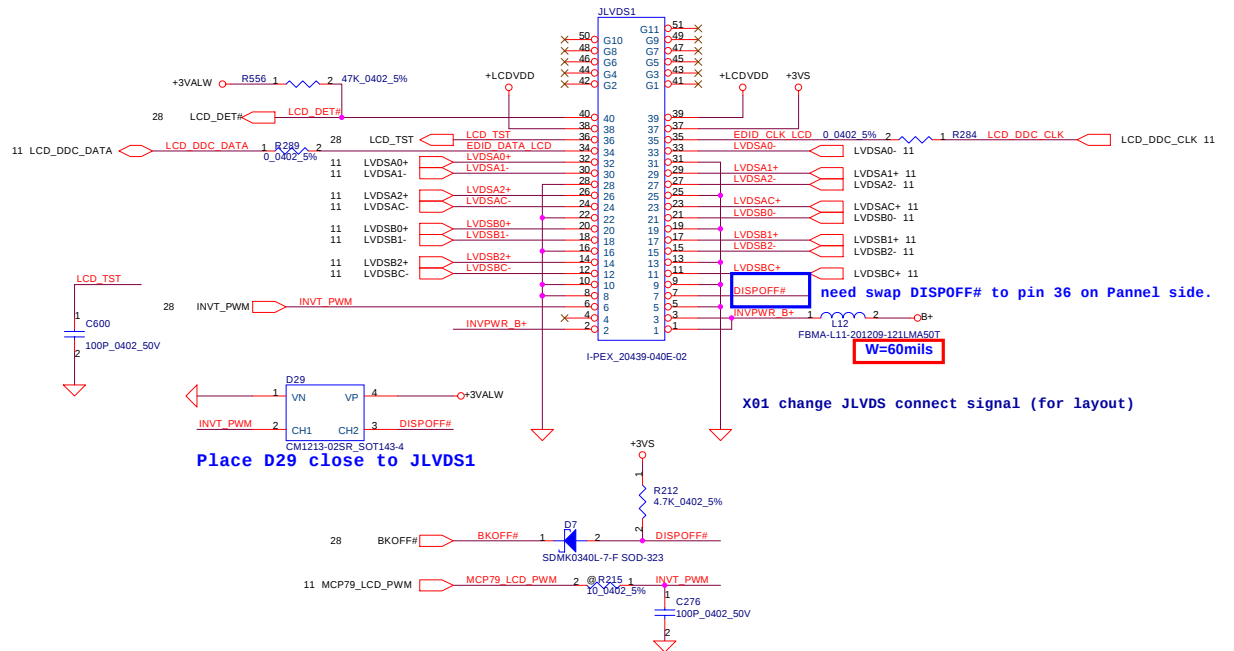
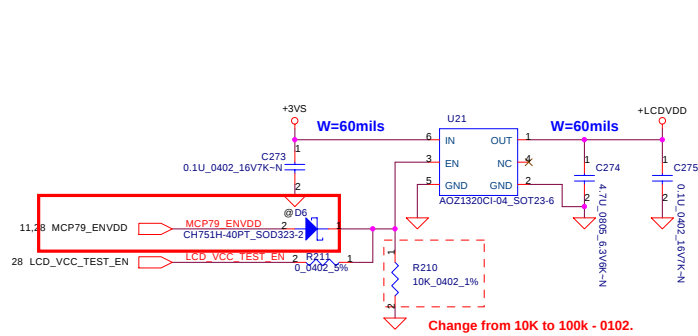
Compal Electronics, Inc.

DDR3 SO-DIMM SLOT

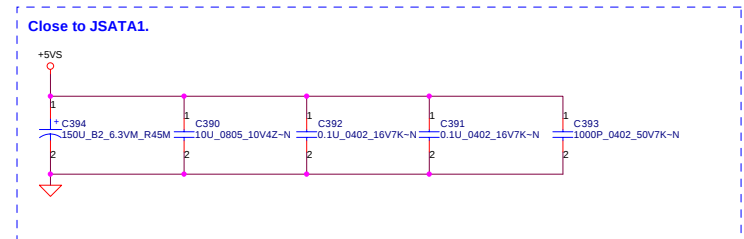
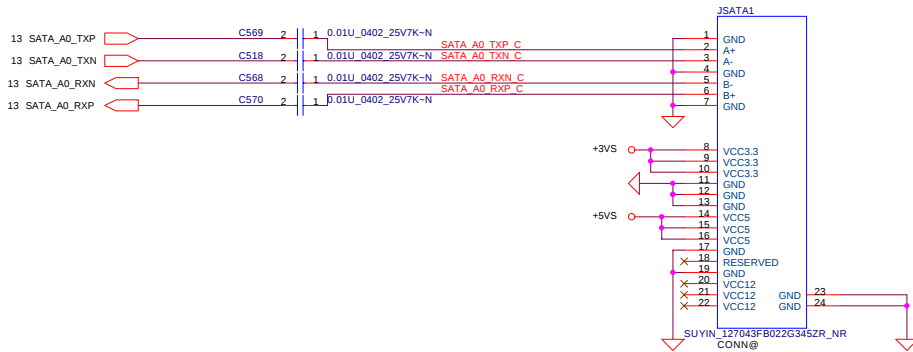


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LCD



SATA HDD

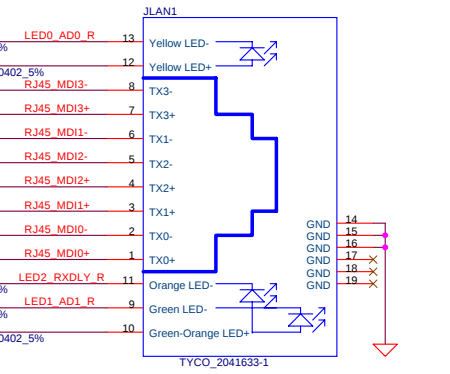
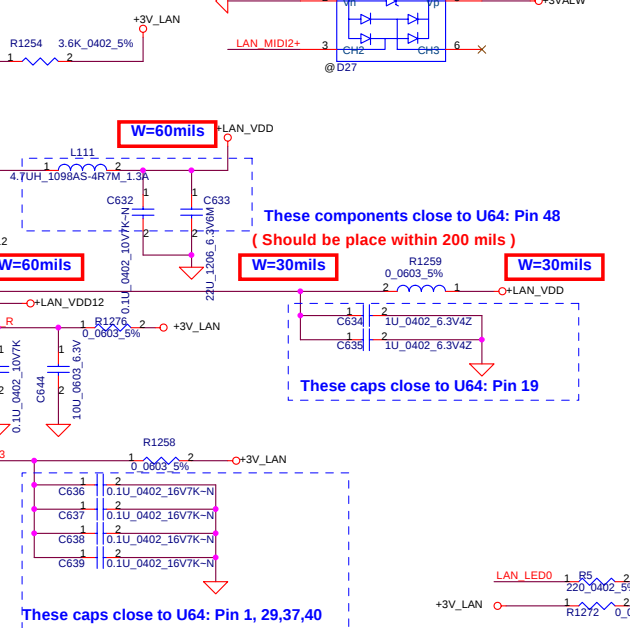
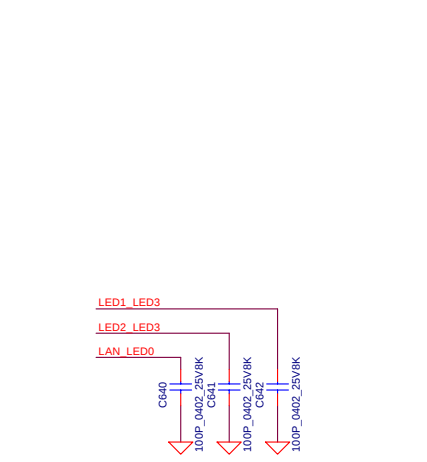
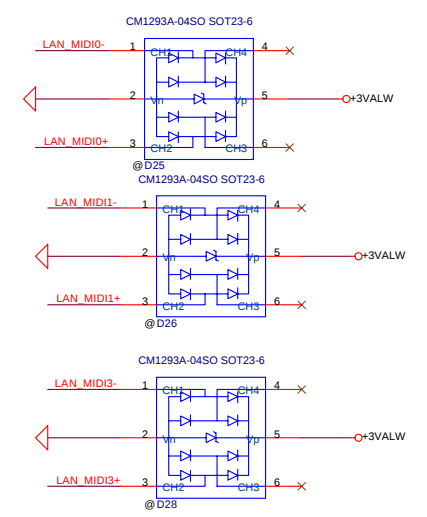
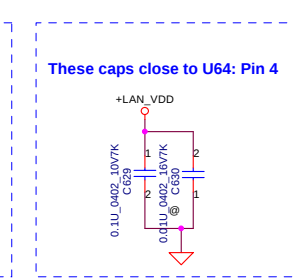
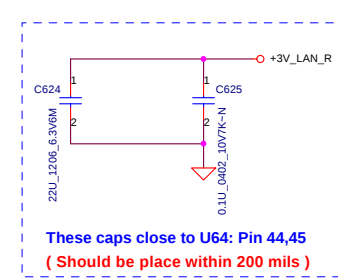
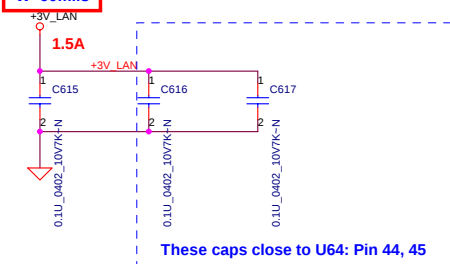


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Figure 10 shows four schematic diagrams of the input channels of the Superworld OCE20121207ZF. Each diagram represents a different input channel, labeled with a transformer component (L23, L24, L25, L26). The input signals are VGA, DVI, TXD1, TXD2, TXC, TXD0, TXD1+, TXD2+, TXD0+, TXD1+. The output signals are DVI, TXC, TXD0, TXD1. The input signals are connected to the primary winding of the transformer, and the output signals are connected to the secondary winding. The input signals are labeled as VGA, DVI, TXD1, TXD2, TXC, TXD0, TXD1+, TXD2+, TXD0+, TXD1+.

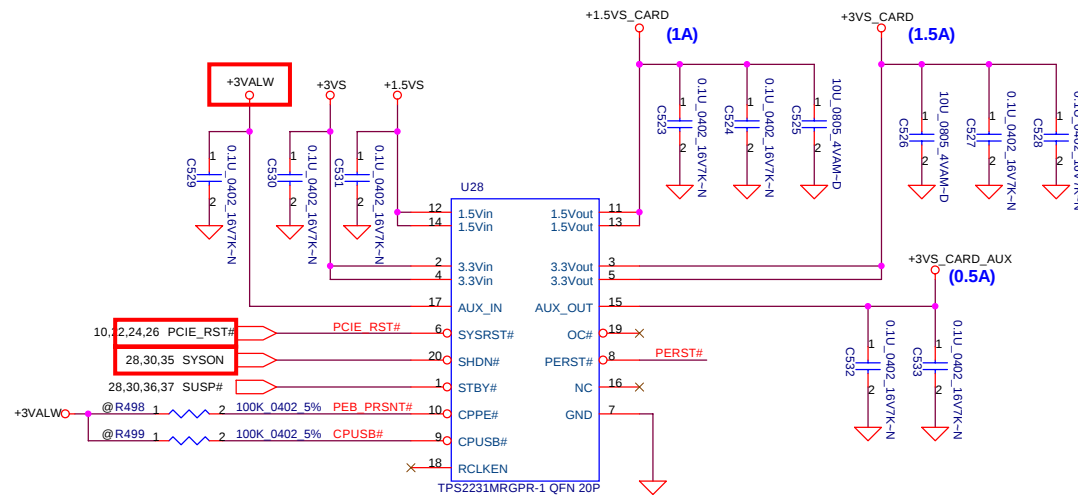
HDMI/Display Port Conn.

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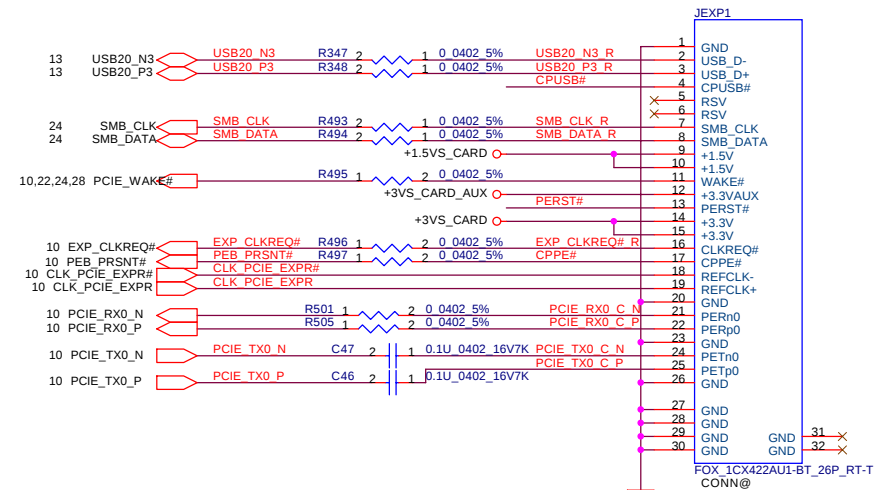


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Express Card Power Switch

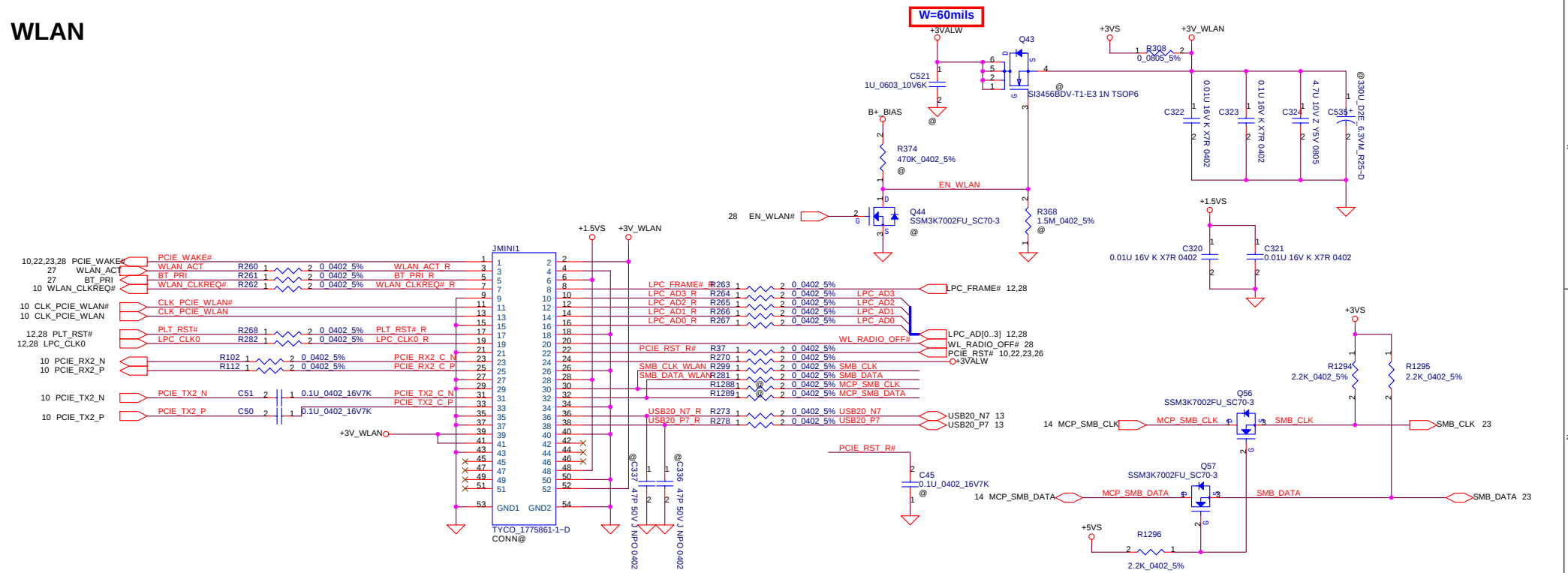
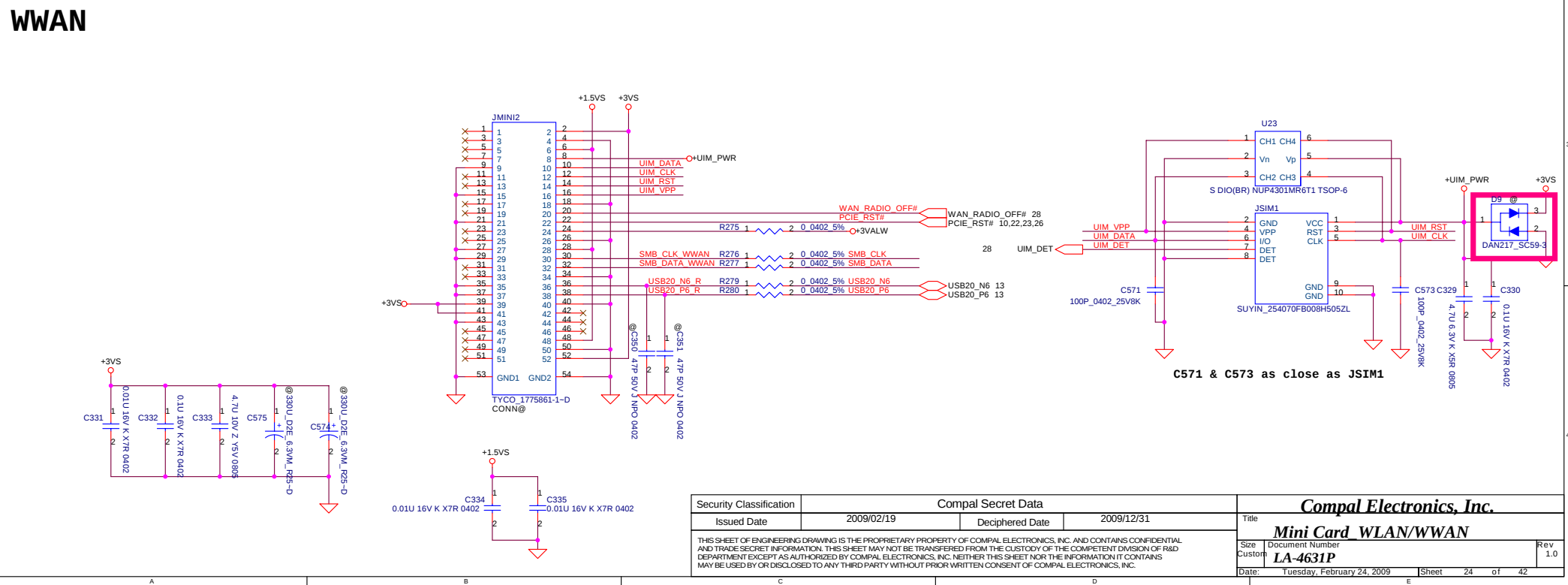


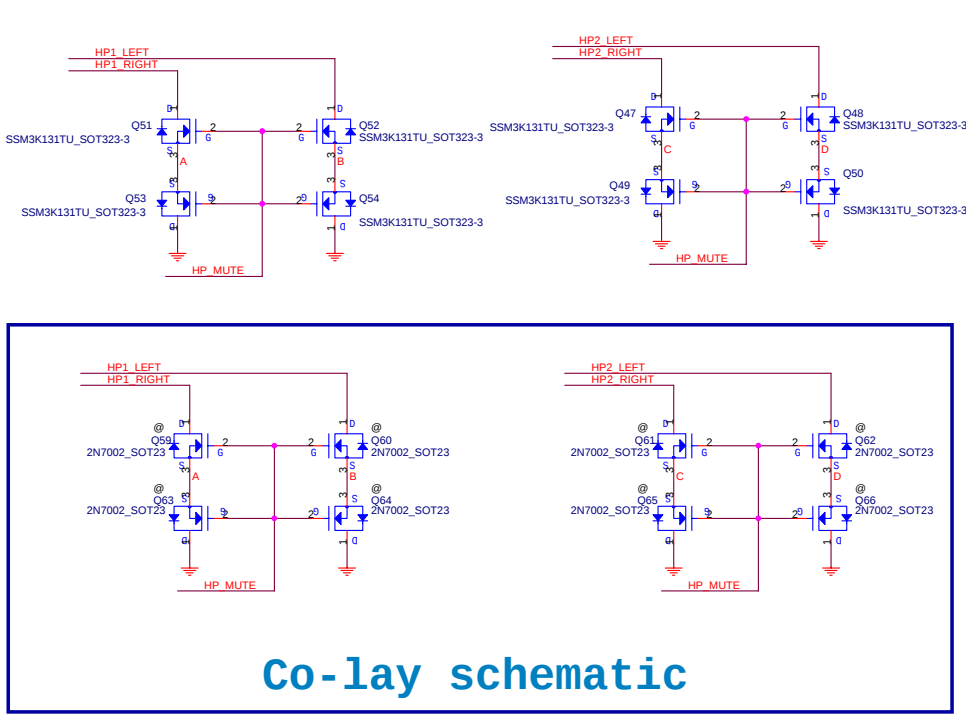
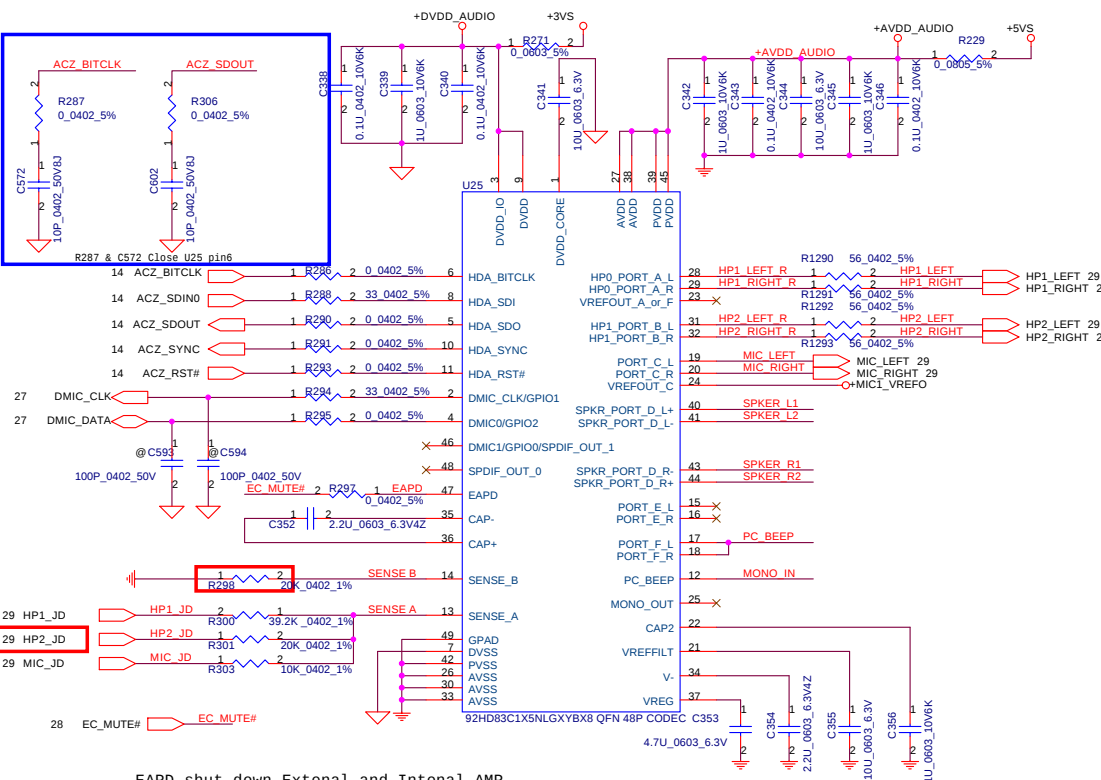
Express Card



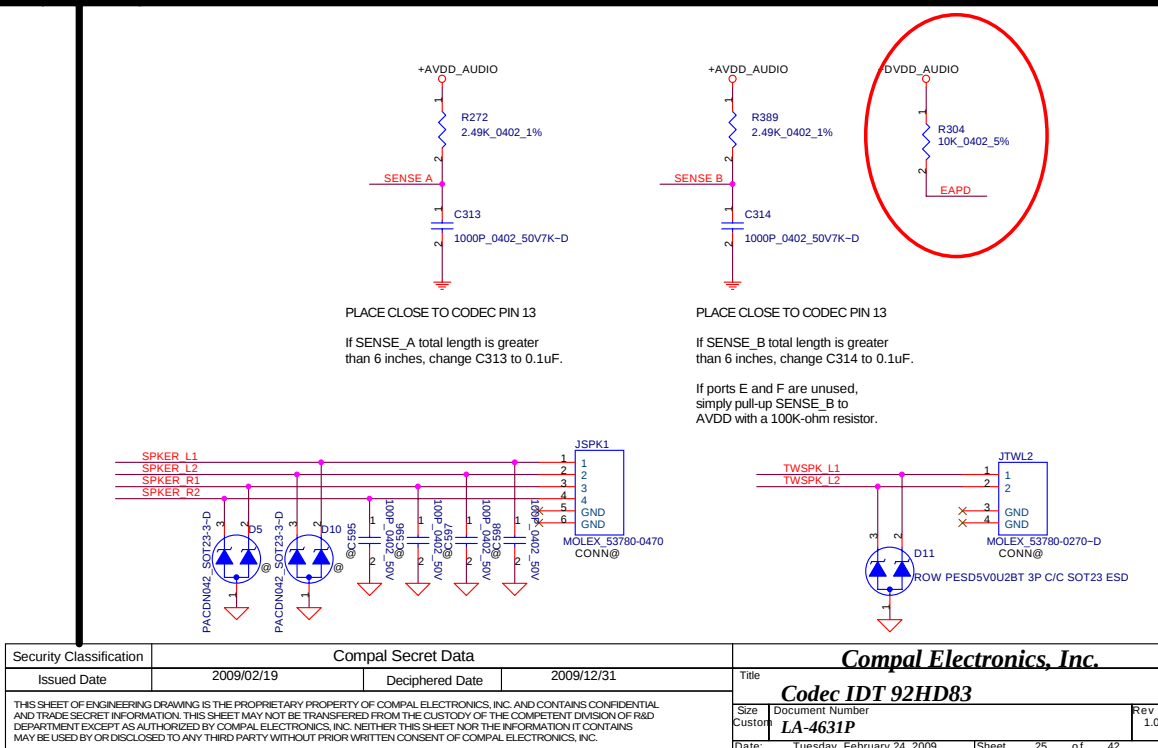
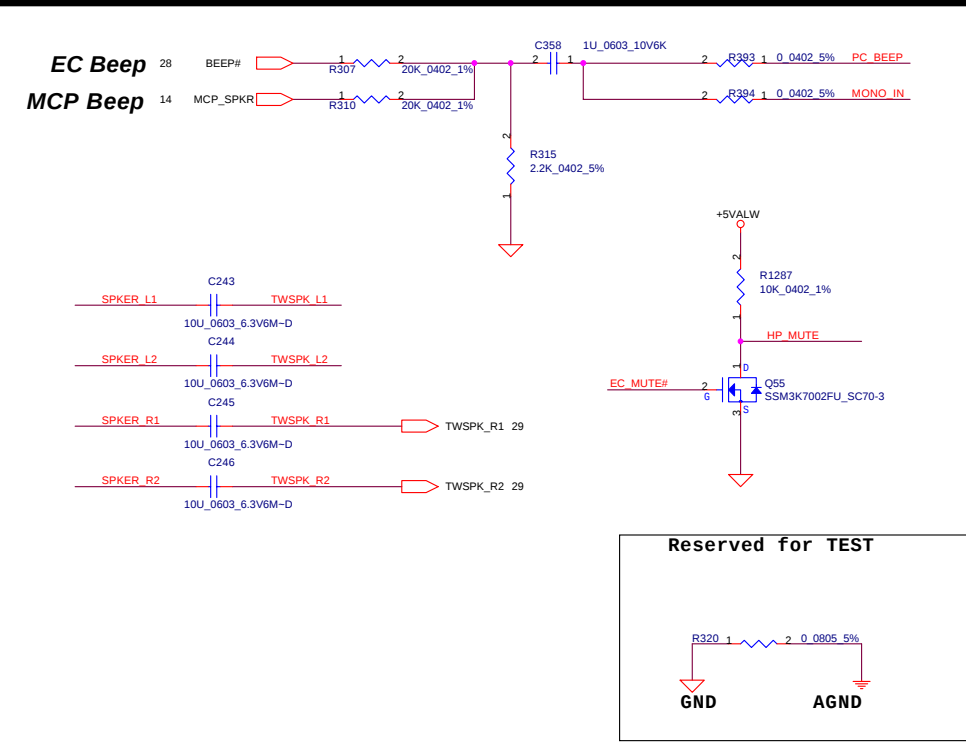
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WLAN

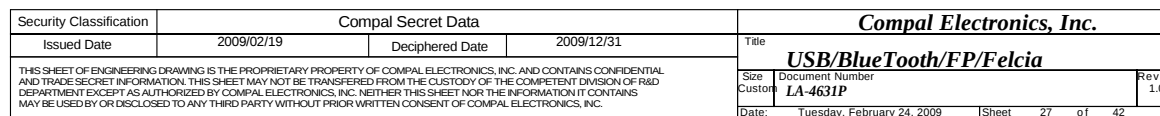
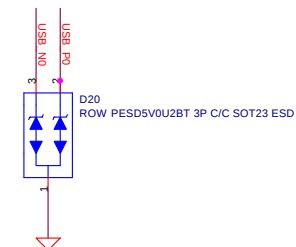
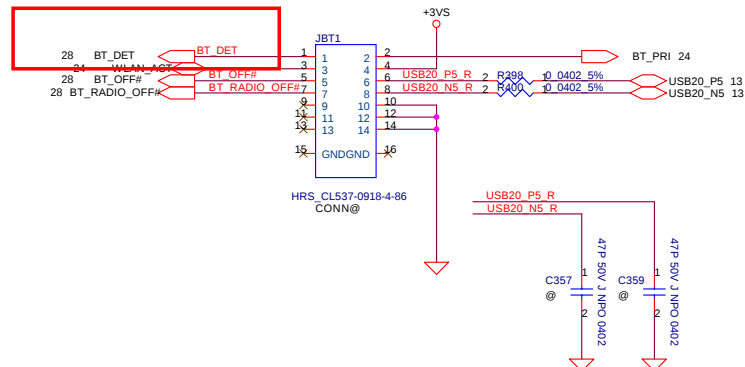
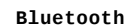
**WWAN**

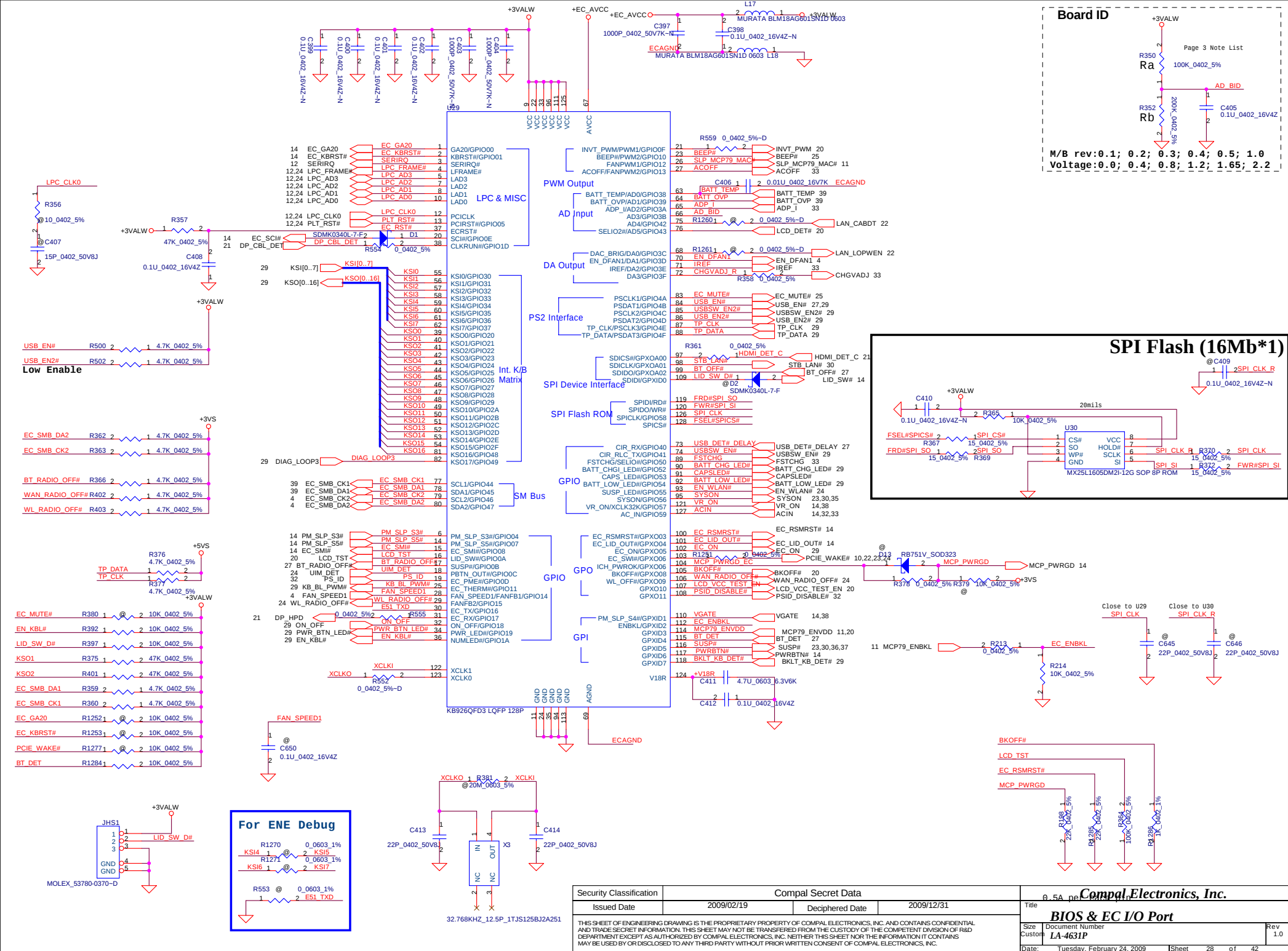


Co-lay schematic



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[illegible]

INT_KB_Conn.1

INT_KB_Conn.1

Diagram showing connections for JKB1, KSI0-KSI16, KSO0-KSO16, and DIAG_LOOP3. The diagram includes a table of pin numbers and labels, and a note "For EMI".

Pin	Label	Pin	Label
1	KSI7	1	KSO6
2	KSI8	2	KSO7
3	KSI9	3	KSO8
4	KSI4	4	KSO9
5	KSI2	5	KSO10
6	KSI5	6	KSO11
7	KSI1	7	KSO12
8	KSI3	8	KSO13
9	KSI0	9	KSO14
10	KSI6	10	KSO15
11	KSI16	11	KSO16
12	KSI12	12	
13	KSI8	13	
14	KSI4	14	
15	KSI0	15	
16	KSI16	16	
17	KSI12	17	
18	KSI8	18	
19	KSI4	19	
20	KSI0	20	
21	KSI16	21	
22	KSI12	22	
23	KSI8	23	
24	KSI4	24	
25	KSI0	25	
26	KSI16	26	
27	KSI12	27	
28	KSI8	28	
29	KSI4	29	
30	KSI0	30	
31	KSI16	31	
32	KSI12	32	

For EMI

B to B Conn.

B to B Conn.

Diagram showing connections for JBTB1, USB20_N1, USB20_P1, USB20_N2, USB20_P2, SATA A1_TXP, SATA A1_TXN, SATA A1_RXN, SATA A1_RXP, IEEE_TPBI1N, IEEE_TPBI1P, IEEE_TPA1N, IEEE_TPA1P, USB_OC#1, USB_OC#2, USB_EN#, USB_EN2#, USB_DETECT#, BATT_CHG_LED#, BATT_LOW_LED#, PWR_BTN_LED#, PWR_ON-OFF_BTN#, USB_SW_EN2#, and 5VALW, 3VALW, MIC_JD, MIC_RIGHT, MIC_LEFT, HP2_JD, HP2_RIGHT, HP2_LEFT, HP1_JD, HP1_RIGHT, HP1_LEFT, TWSPK_R1, TWSPK_R2.

Touch PAD/B Conn.

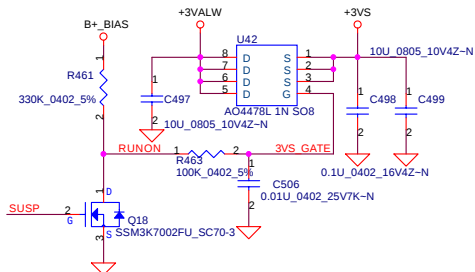
Touch PAD/B Conn.

Diagram showing connections for TP_DATA, TP_CLK, C440, C442, C441, D16, and JTP1.

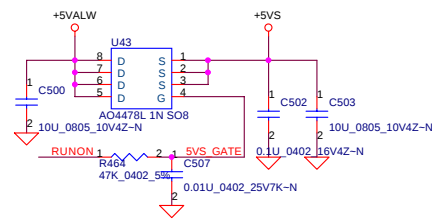
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				Date:	Tuesday, February 24, 2009	Sheet	29 of 42

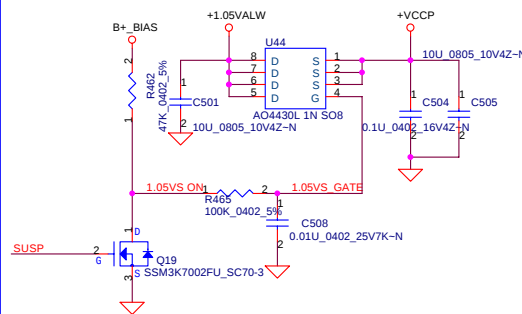
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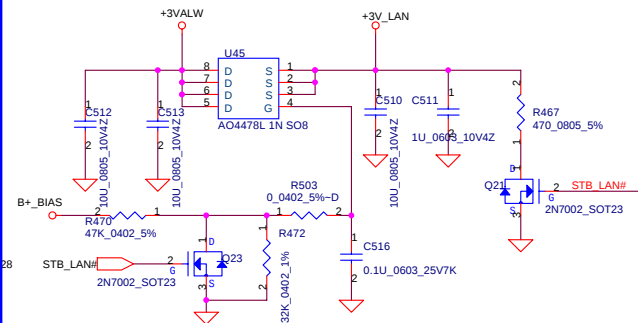
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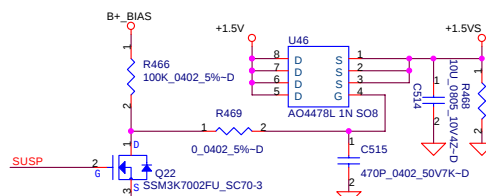
+1.05VALW to +VCCP Transfer



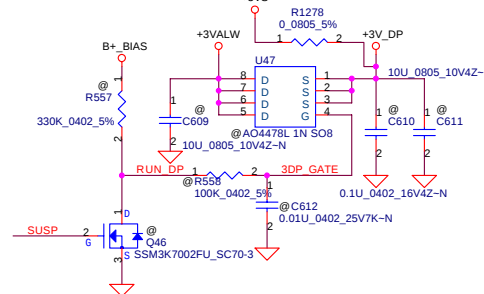
+3VALW TO +3V_LAN



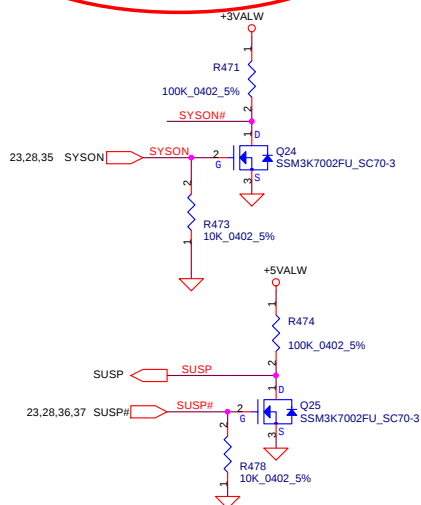
+1.5V to +1.5VS Transfer



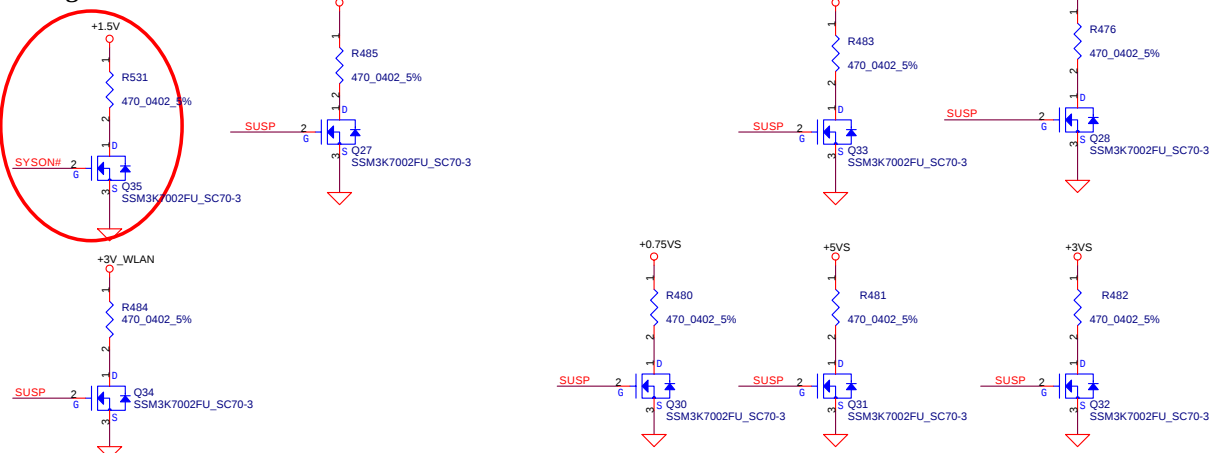
+3VALW to +3V_DP Transfer



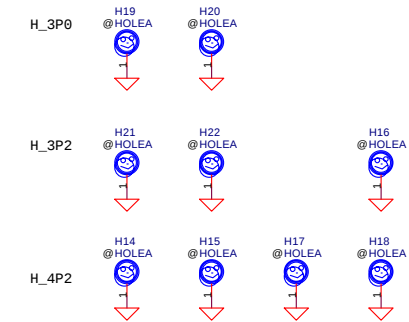
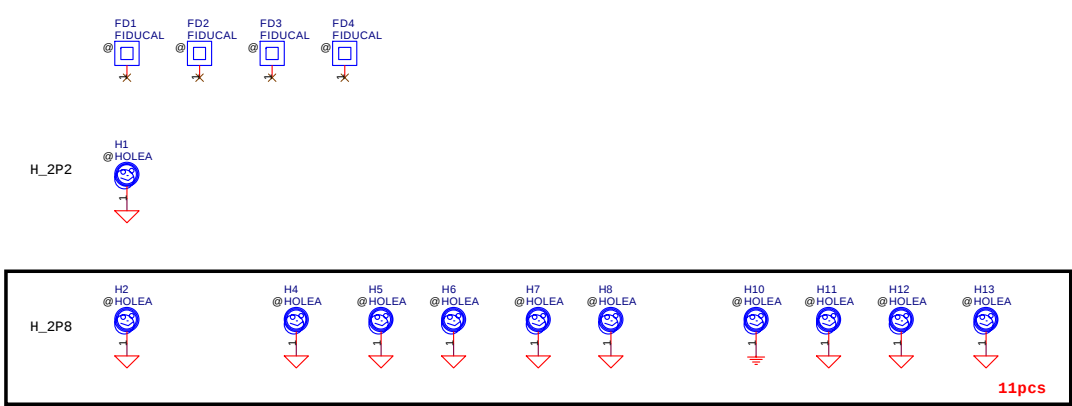
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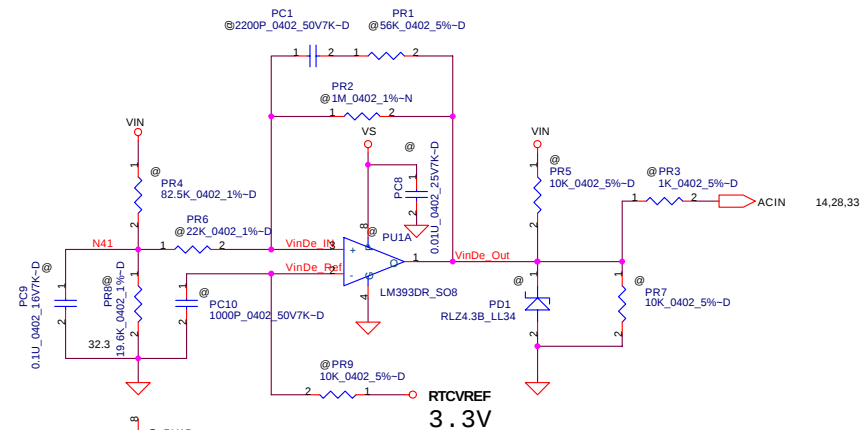
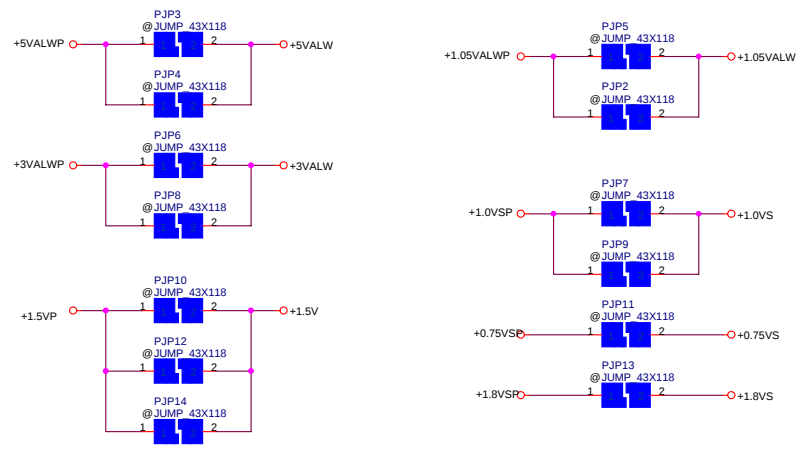
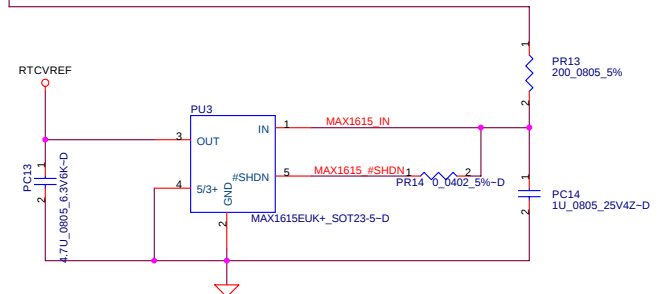
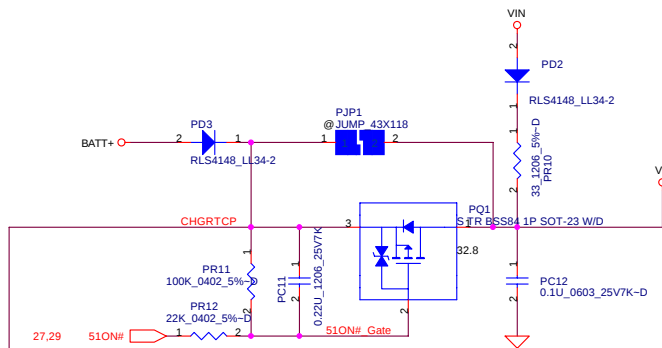
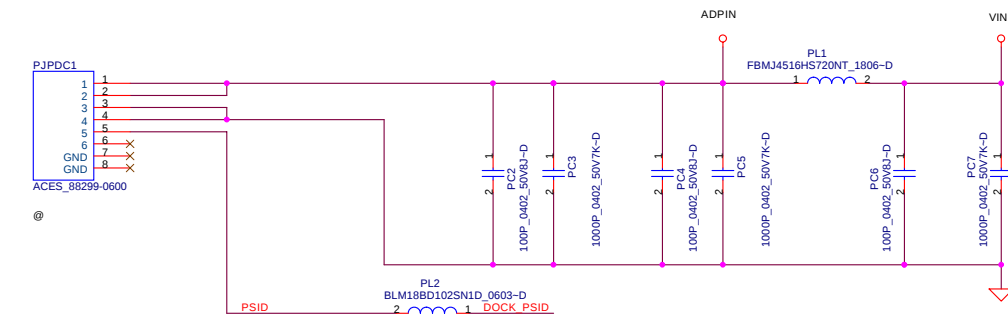
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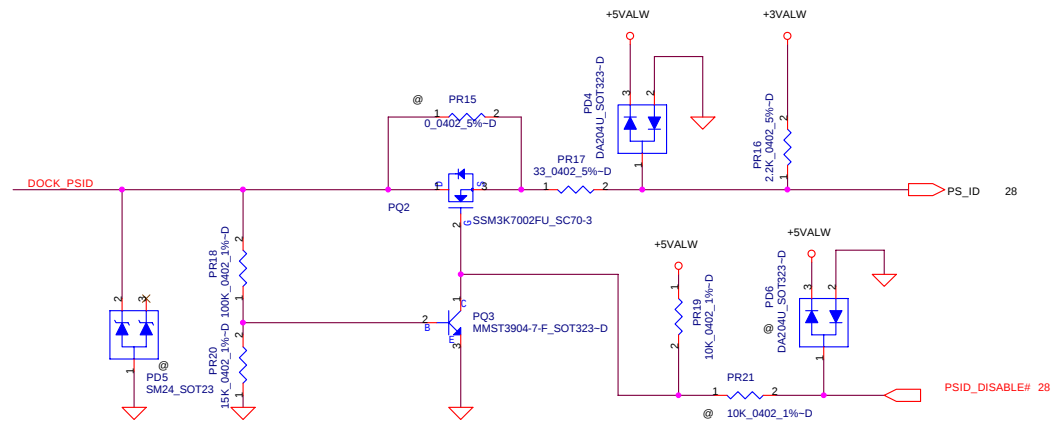
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								DC/DC Circuits			
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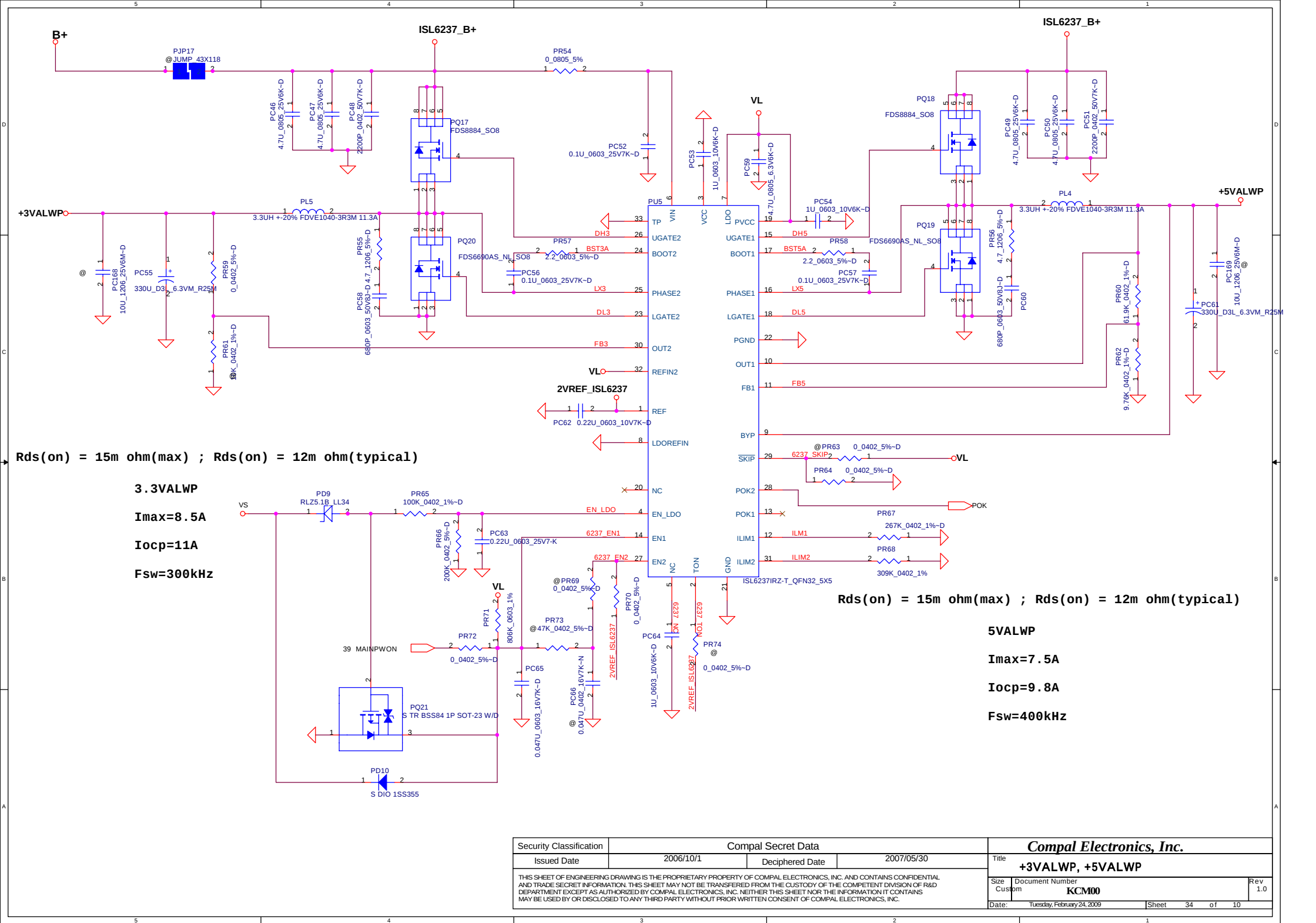
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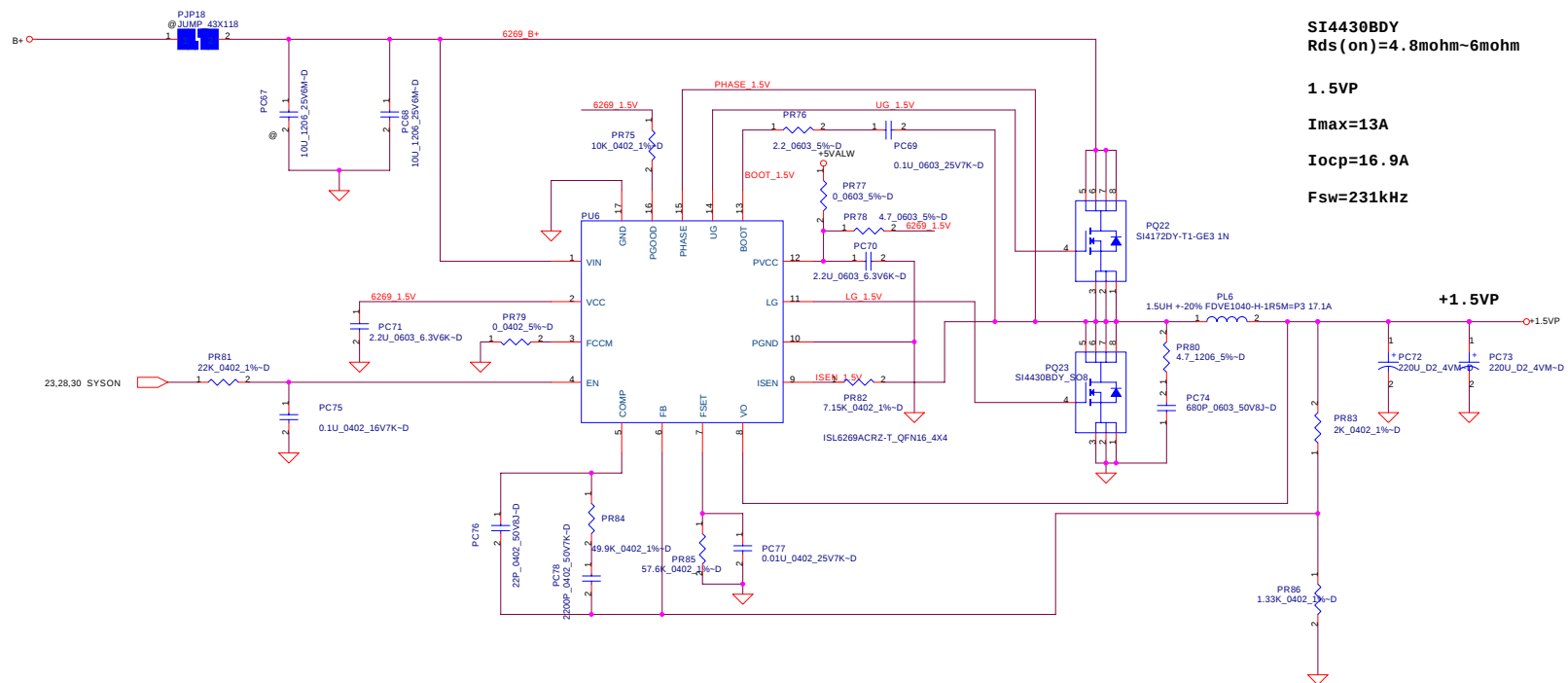


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H ->L	17.597	17.210	16.813

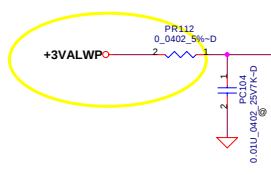
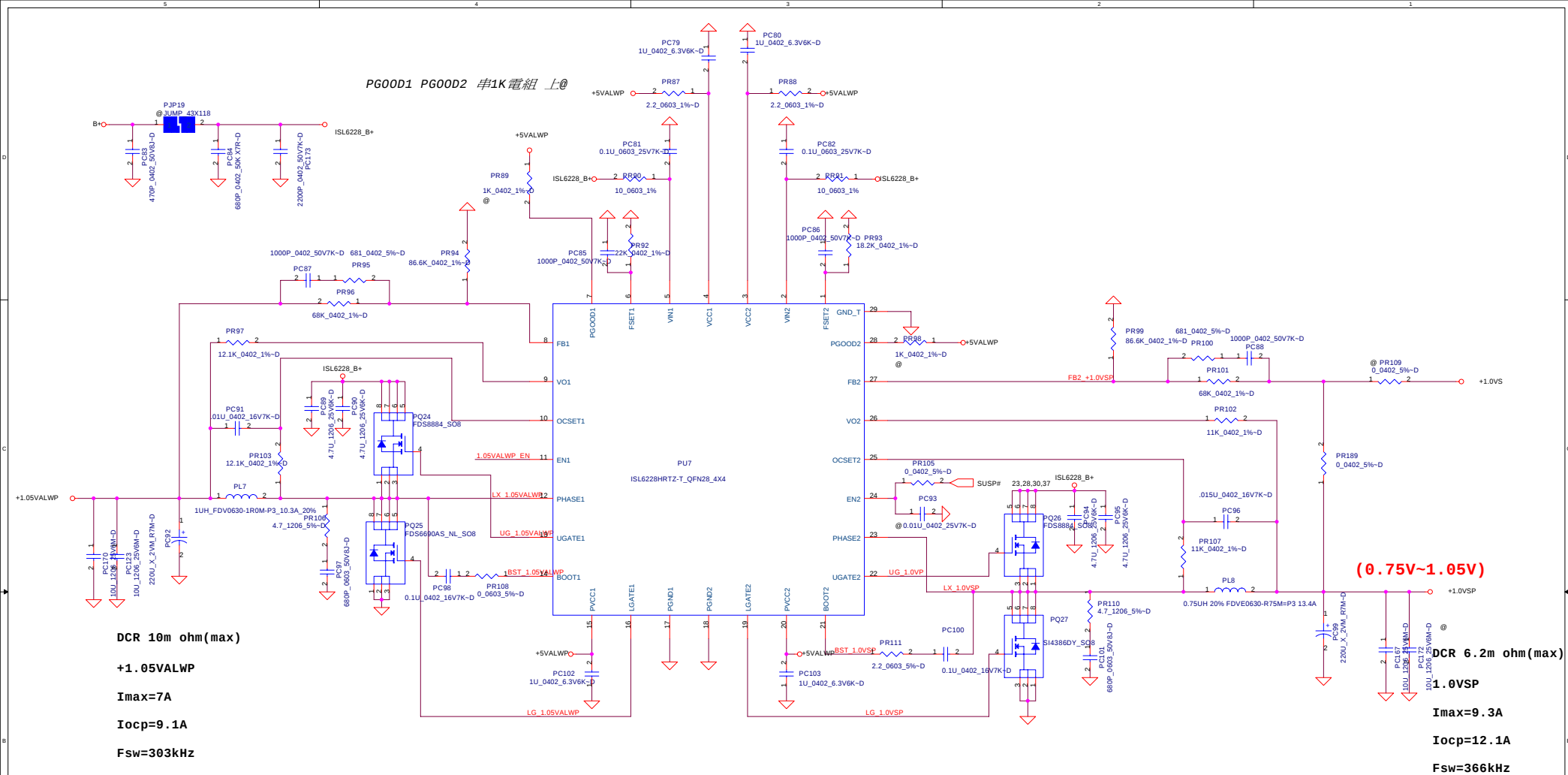


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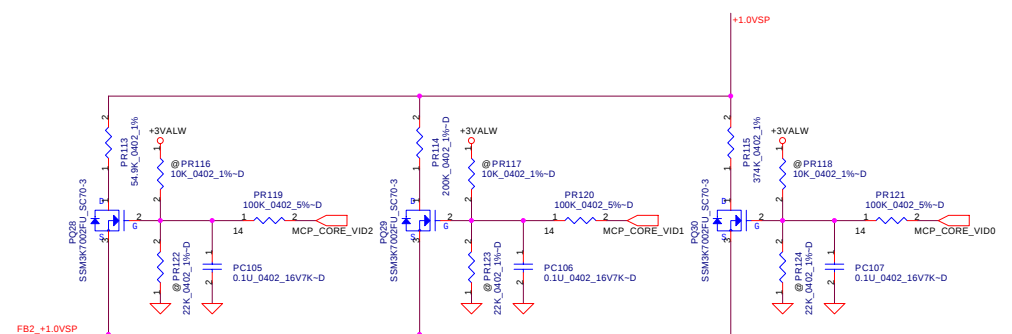


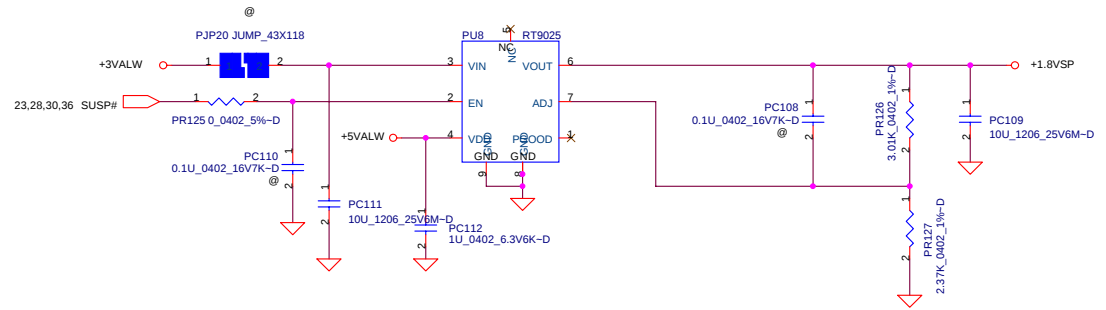


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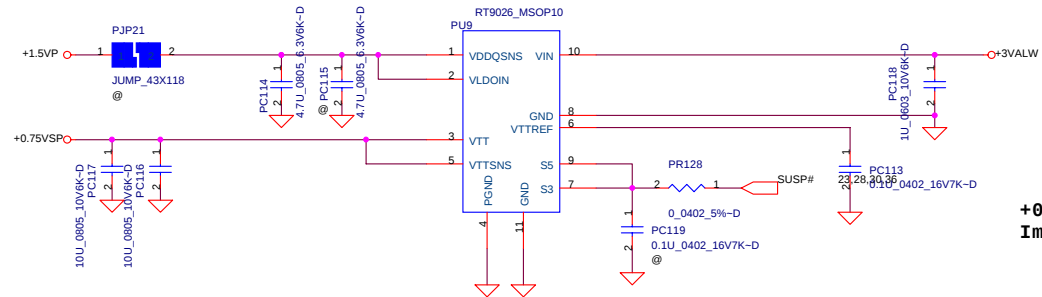


VID2	VID1	VID0	voltage
L	L	L	1.05
L	L	H	0.98
L	H	L	0.90
L	H	H	0.87
H	L	L	0.80
H	L	H	0.79
H	H	L	0.77
H	H	H	0.75



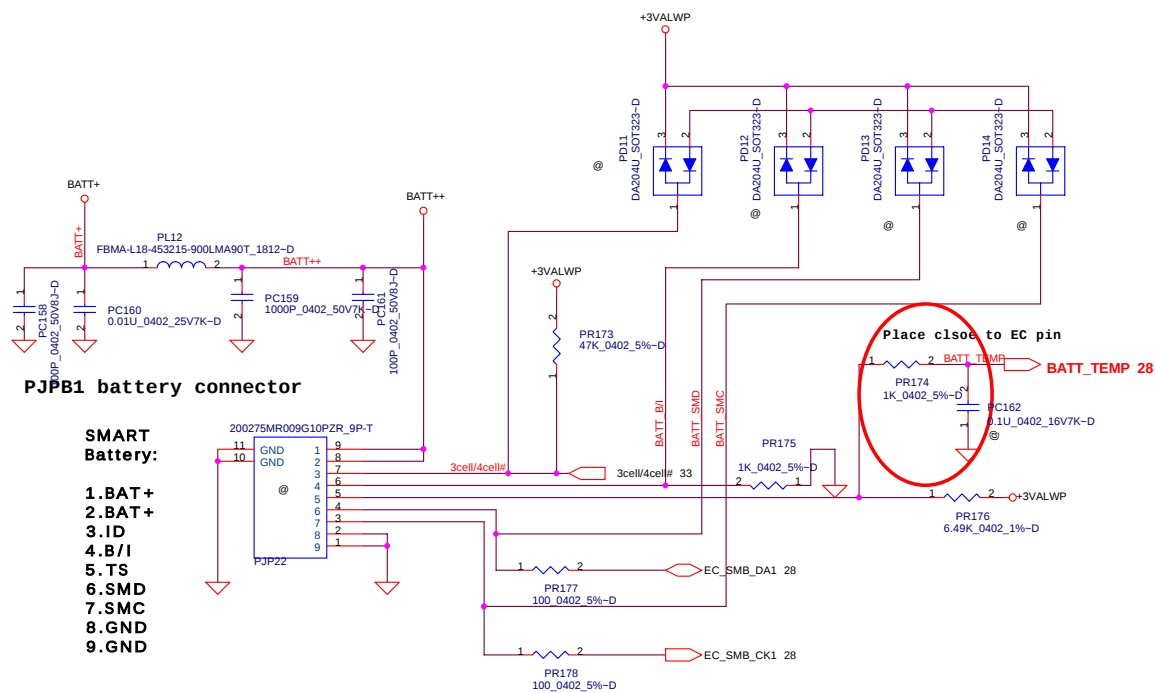


+1.8VSP
I_{max}=0.3A



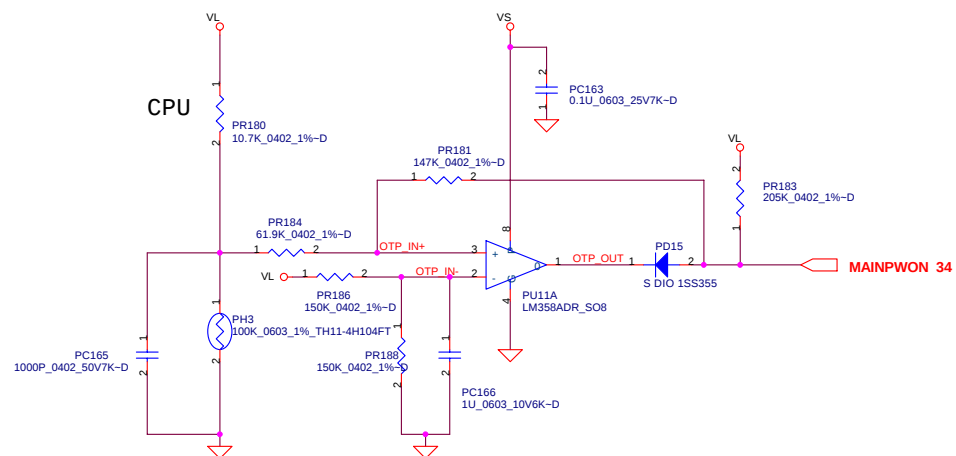
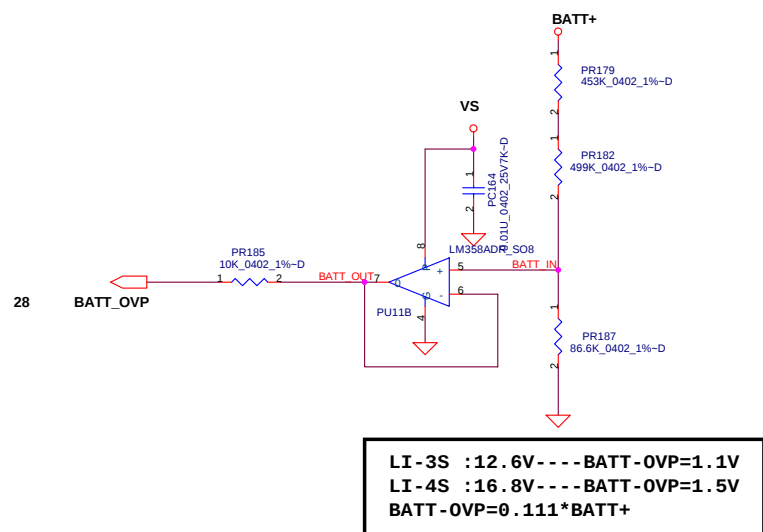
+0.75VSP
I_{max}=1.5A

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CPU

PH1 under CPU bottom side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C

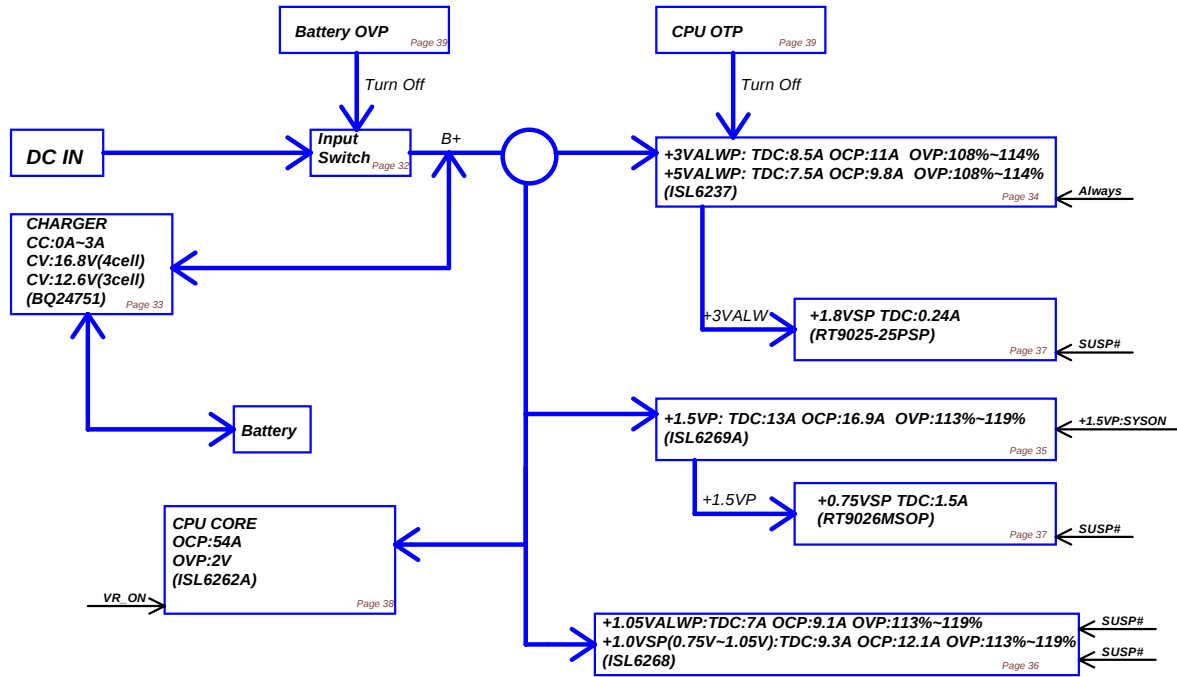


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1	p37	+0.75VSP/1.8VSP	08/10/15	compal	source shortage	pu9	
2	p33	charger	08/10/15	compal	design change	PQ6 PQ8	
3	p32	DCIN / Precharge	08/10/15	compal	meet PSL	PQ2	
4	p33	charger	08/10/15	compal	meet PSL	PQ16	
5	p32	DCIN / Precharge	08/10/15	compal	meet PSL	PQ1	
6	p33	charger	08/10/15	compal	meet PSL	PQ12	
7	p34	+3VALWP/+5VALWP	08/10/15	compal	meet PSL	PQ21	
8	p33	charger	08/10/15	compal	meet PSL	PR22 PR29	
9	p37	+0.75VSP/1.8VSP	08/10/15	compal	adjust 1.8V output voltage	PR127 PR124	
10	p33	charger	08/10/15	compal	adjust charge current to 3.1A	PR38	
11	p33	charger	08/10/15	compal	adjust CP set for ICPP function	PR38	
12	p34	+3VALWP/+5VALWP	08/10/15	compal	meet choke component current limit	PL4 PL5	
13	p32	DCIN / Precharge	08/10/15	compal	meet PSL	PL1	
14	p38	CPU_CORE	08/10/15	compal	meet PSL	PL9	
15	p39	BATTERY CONN	08/10/15	compal	meet PSL	PL12	
16	p33	charger	08/10/22	compal	design change	PQ6 PQ8	
17	p35	+1.5VSP	08/10/22	compal	reduce L/S MOS Vds	PQ22	
18	p36	+1.05VALWP/1.0VP	08/10/22	compal	Add remote sense function	PR189	
19	p36	+1.05VALWP/1.0VP	08/10/22	compal	adjust output voltage	pr94	
20	p36	+1.05VALWP/1.0VP	08/10/22	compal	design change	PL8	
21	p35	+1.5VSP	08/10/22	compal	design change	PL6	
22	p33	charger	08/10/22	compal	EMI request	PL13	
23	ALL	every power	08/10/22	compal	reduce output ripple	PC123 PC167 PC168 PC169 PC170	
24	ALL	every power	08/10/22	compal	sunbber for EMI request	PR30 PR106 PR55 PR56 PR80 PR110 PR105 PR155	
25	ALL	every power	08/10/22	compal	sunbber for EMI request	PC33 PC58 PC60 PC74 PC97 PC101 PC134 PC144	
26	P34 P35	every power	08/10/22	compal	increase boost resistor value form 0 ohm to 2.2 ohm for EMI request	PR57 PR58 Pr76	
27	p39	BATTERY CONN	08/12/03	compal	adjust OTP set	PR183	
28	p33	charger	08/12/03	compal	DFX request	PQ10 PQ11 PQ13 PQ14 PQ15	
29	p36	+1.05VALWP/1.0VP	08/12/03	compal	adjust +1.0VSP OCP set	PR102 PR107	
30	p36	+1.05VALWP/1.0VP	08/12/03	compal	adjust +1.0VSP output voltage	PR99	
31	p35	+1.5VSP	08/12/12	compal	design change(already trail run in PT phase)	PQ22	
32	p39	BATTERY CONN	08/12/12	compal	adjust OTP set	PR183	
33	p33	charger	08/12/31	compal	reduce AC-IN inrush current	PR24 PR25	
34	p36	+1.05VALWP/1.0VP	08/12/31	compal	WWAN issue	PC173 PC174 PC175	
34	p34	+3VALWP/+5VALWP	08/12/31	compal	adjust +5VALWP voltage	PR62 change frome 10k to 9.62k	

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Braxton Power block



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1	19	P19-DDR3_S0-DIMM SLOT	2008/09/22	nVidia	can't use S0-DIMM	change S0-DIMM SA0 to pull high & SA1 to pull down	0.2
2	20	P20-LCD/SATA HDD	2008/09/25	Compal	can't read EDID for Panel	change JLVDS1 Pin 37 from +LCDVDD TO +3VS	0.2
3	21	P21-HDMI/Display Port	2008/10/07	Compal	Change DP122 to DP122A	change R440 from 4.64K to 5.11K and R438 from 5.11K to 6.49K	0.2
4	12	P12-MCP79(6/10)_PCI/LPC	2008/10/13	Compal	can't select on board SPD data	ADD R191,R192,R193 TO SELECT ON BOARD MEMORY VENDOR	0.2
5	28	P28-EC_KB926/BIOS/Reed SW	2008/10/20	Compal		Change EC_SMB_DA1 and EC_SMB_CK1 from +5VALW to +3VALW	0.2
6	18	P18-1GB/2GB_DDR3_On Board	2008/12/04	nVidia	On board Ram unstable	Add 0.1uF cap between Termination Resistor and +0.75VS	0.4
7	14	P14-MCP79(8/10)_HDA/MISC	2009/02/03	Dell	saving power consumption	change +3VALW to +3VS on MEM_SMBCLK & MEM_SMBDATA	1.0
8	24	P24-Mini Card_WLAN/WWAN	2009/02/04	Dell		reserve SMBus from MCP79	1.0
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