Wistron CONFIDENTIAL

MODEL NAME : ***Diaz UMA***

Project Code: ***91.4AR01.001***

PCB NO : ***08217-1***

Diaz Intergrate Intel GM Schematics Document

uFCPGA Mobile Merom

Intel Crestline-GM + ICH8M

REV : A00

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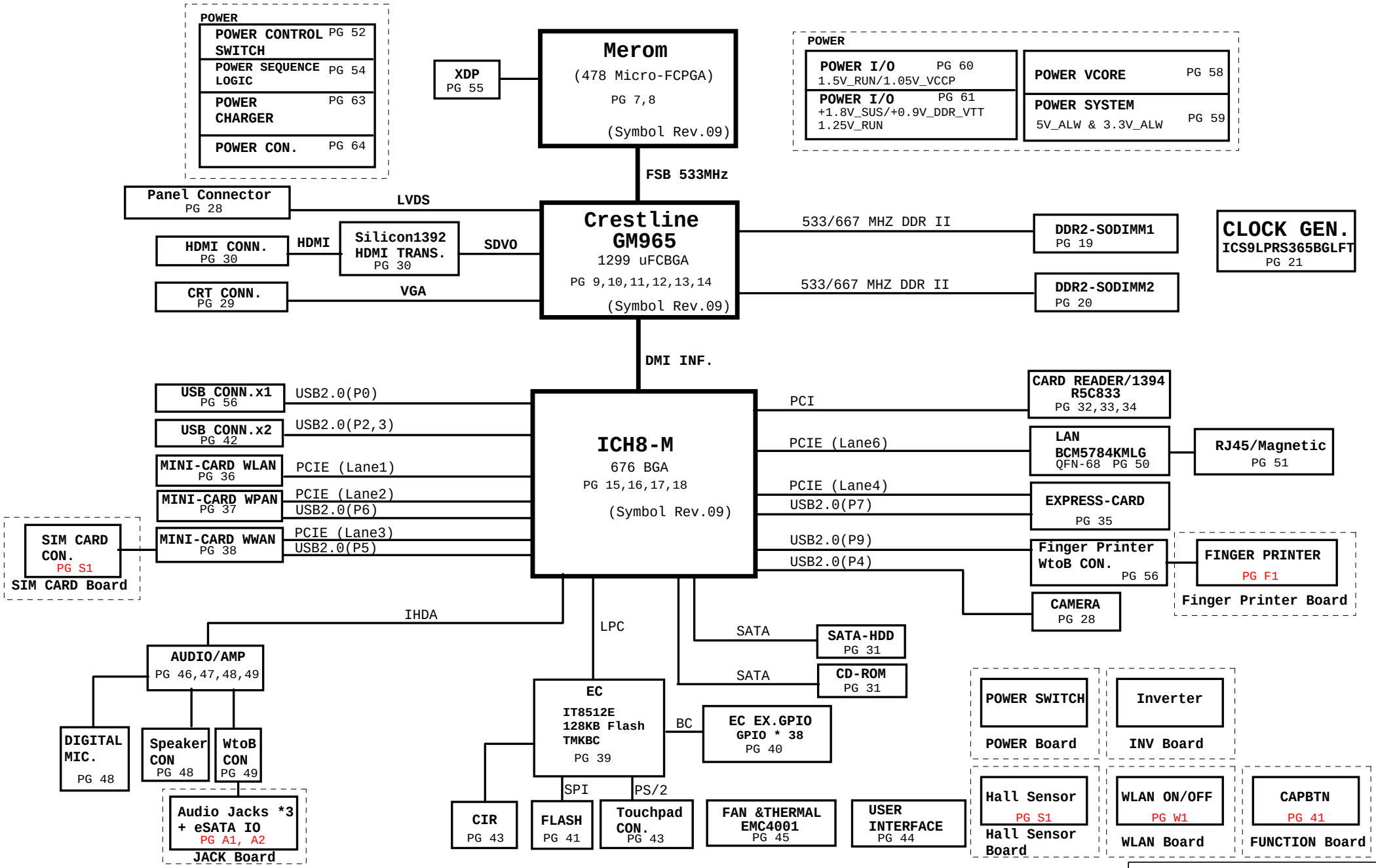
Diaz Block Diagram of Intel GM



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BLOCK DIAGRAM		
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52	POWER CONTROL SWITCH	
53	Power Button Board	
54	Power Sequence Logic	
55	XDP	
56	USB PORT ,eSATA, FINGER	
57	SIM Board	
58-64	Power circuit	

Pg#	Description	DNI LIST
65	SCREW PAD	
A1	AUDIO_JACK	
A2	USB PORT & eSATA	
C1	CAPBTN	
F1	Fingerprint (AES2810)	
L1	LID Board	
S1	SIM Board	
W1	Wireless Switch Board	

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Footprint Definition

Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

Layout Note

For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

PCI TABLE

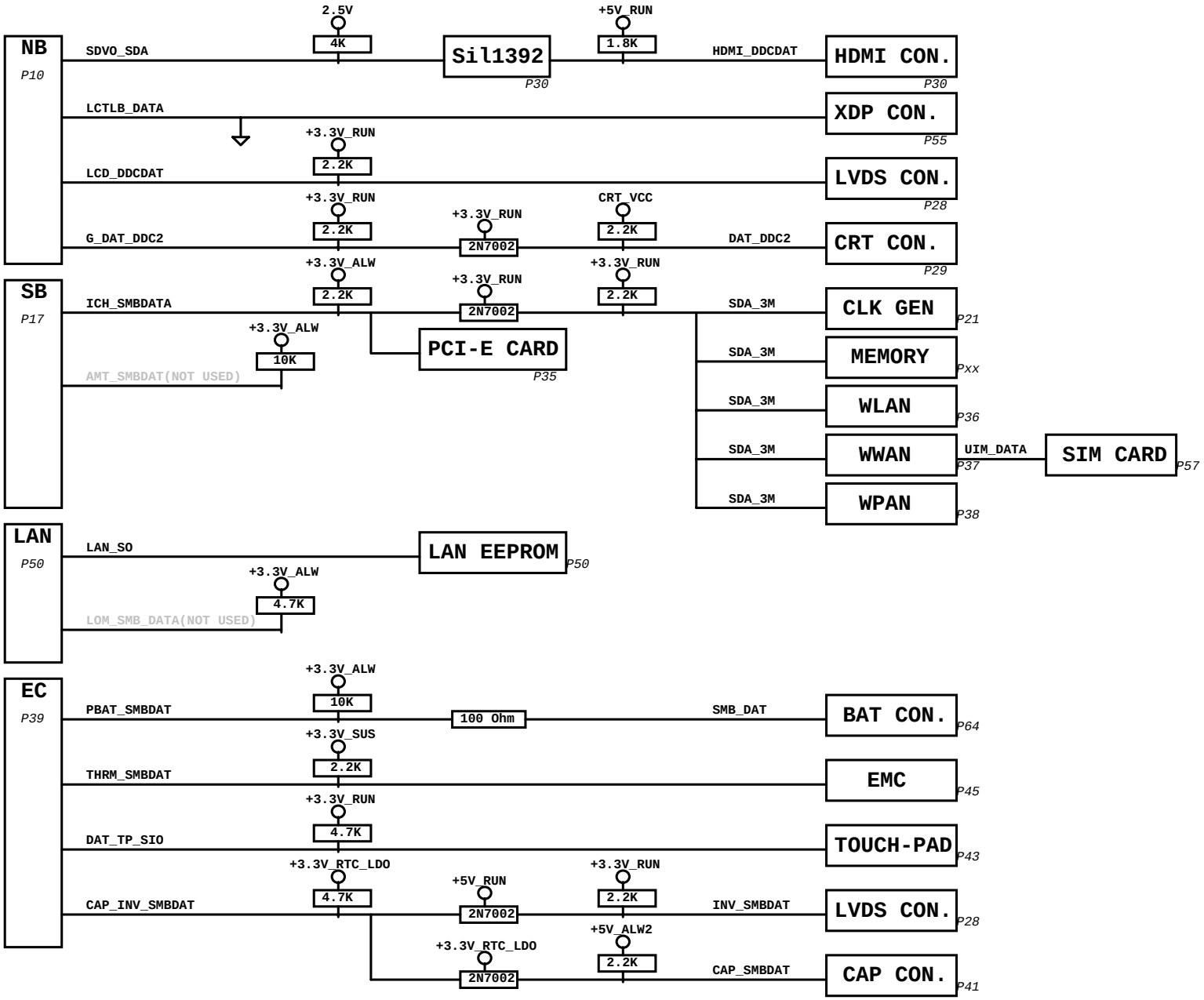
PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

PCI Express TABLE

Lane 1	WLAN / Mini Card
Lane 2	WPAN / Mini Card
Lane 3	WWAN / Mini Card
Lane 4	ExpressCard
Lane 5	
Lane 6	LAN BCM5784KMLG

USB TABLE

ICH8-0 (EHCI#1)	User1 (Single port , in USB BD)
ICH8-1 (EHCI#1)	
ICH8-2 (EHCI#1)	User2 (Dual port-bottom , in I/O BD)
ICH8-3 (EHCI#1)	User3 (Dual port-top , in I/O BD)
ICH8-4 (EHCI#1)	Camera
ICH8-5 (EHCI#1)	WWAN / Mini Card
ICH8-6 (EHCI#2)	WPAN / Mini Card
ICH8-7 (EHCI#2)	ExpressCard
ICH8-8 (EHCI#2)	Note : No USB for WLAN
ICH8-9 (EHCI#2)	Finger Printer



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Title		
SM BUS		
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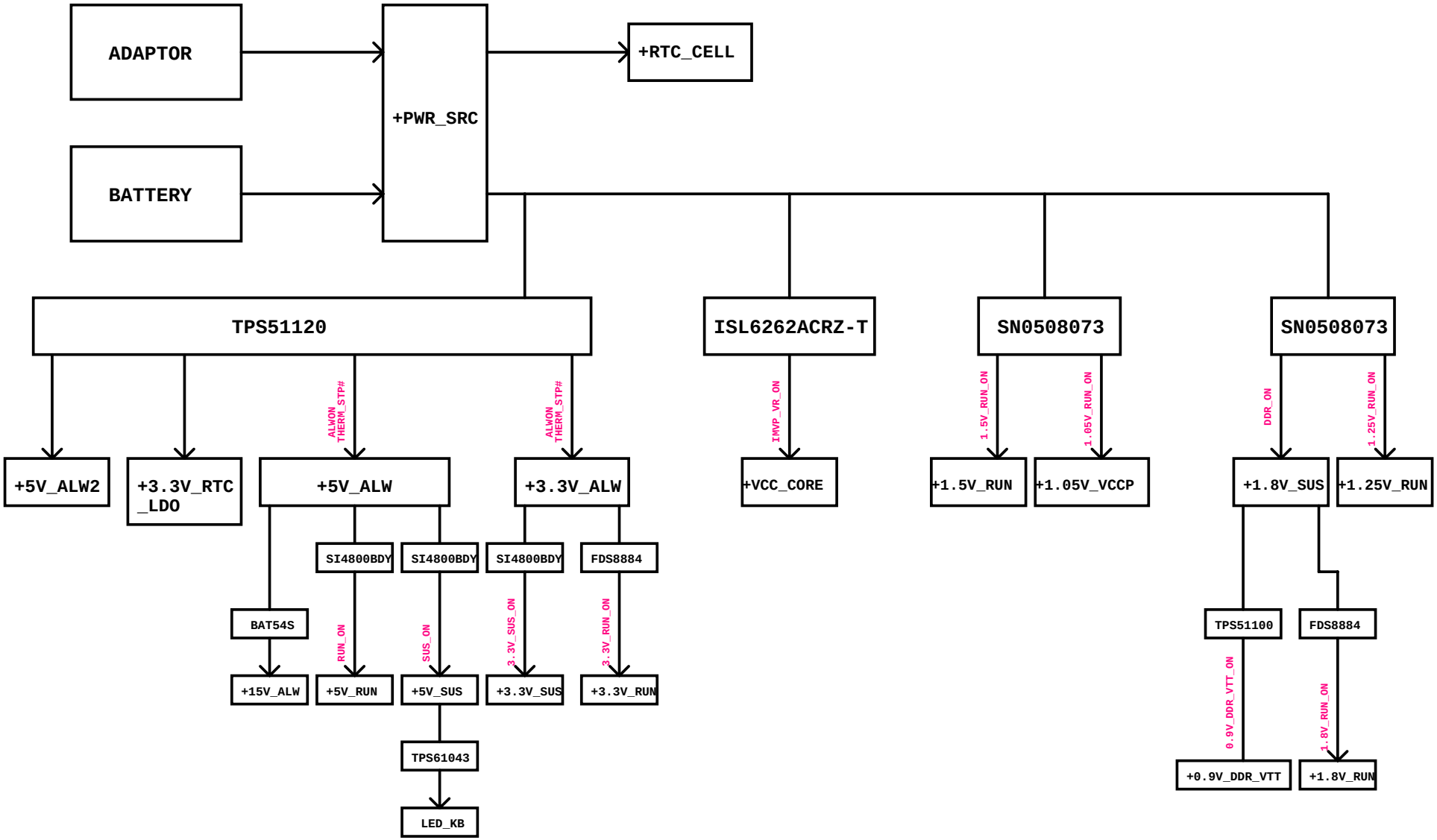

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Title	Intel UMA POWER RAIL	
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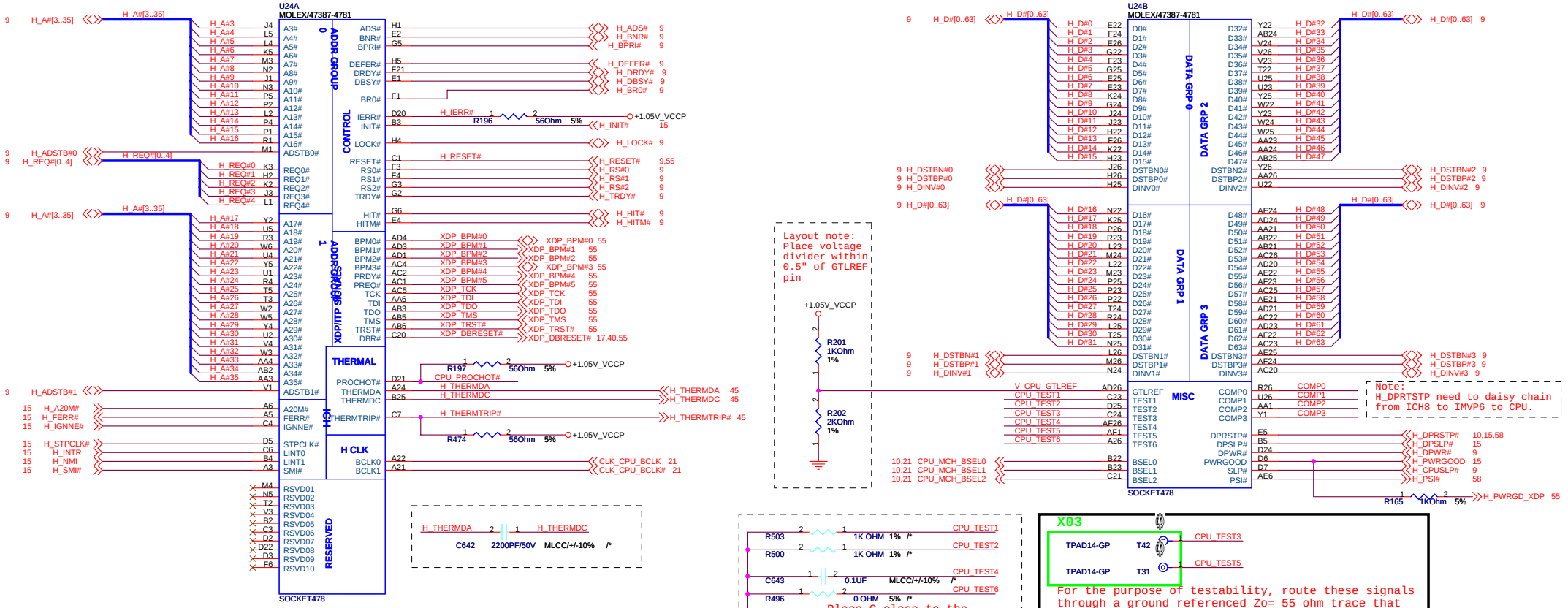

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

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Title: MEROM CPU (1)

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All use 10U 4V (+-20% , X5R , 0805)Pb-Free.

+VCC_CORE

C629 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C604 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C311 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C318 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C611 10UF/6.3V MLCC/+/-20% pt_c0805_h53

+VCC_CORE

C353 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C339 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C627 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C615 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C349 10UF/6.3V MLCC/+/-20% pt_c0805_h53

8 inside cavity, north side, secondary layer.

+VCC_CORE

C336 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C334 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C352 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C599 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C357 10UF/6.3V MLCC/+/-20% pt_c0805_h53

+VCC_CORE

C310 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C605 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C330 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C613 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C628 10UF/6.3V MLCC/+/-20% pt_c0805_h53

8 inside cavity, south side, secondary layer.

+VCC_CORE

C308 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C351 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C626 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C625 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C623 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C322 10UF/6.3V MLCC/+/-20% pt_c0805_h53

6 inside cavity, north side, primary layer.

+VCC_CORE

C350 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C312 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C621 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C345 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C313 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C335 10UF/6.3V MLCC/+/-20% pt_c0805_h53

6 inside cavity, south side, primary layer.

+1.05V_VCCP

C596 0.1UF/10V MLCC/+/-10%
C595 0.1UF/10V MLCC/+/-10%
C632 0.1UF/10V MLCC/+/-10%
C362 0.1UF/10V MLCC/+/-10%
C633 0.1UF/10V MLCC/+/-10%
C307 0.1UF/10V MLCC/+/-10%

Layout out:
Place these inside socket cavity on North side secondary.

+VCC_CORE

CE4 220UF/2V pt_c7343d_h75 SANYO/2TPF220M7
CE3 220UF/2V pt_c7343d_h75 SANYO/2TPF220M7

100U/25V *4 Remove to POWER CIRCUIT .

+VCC_CORE

U24C MOLEX/47387-4781

A7	VCC001	VCC068	AB20
A9	VCC002	VCC069	AB7
A10	VCC003	VCC070	AC7
A12	VCC004	VCC071	AC9
A13	VCC005	VCC072	AC12
A15	VCC006	VCC073	AC13
A17	VCC007	VCC074	AC15
A18	VCC008	VCC075	AC17
A20	VCC009	VCC076	AC18
B7	VCC010	VCC077	AD7
B9	VCC011	VCC078	AD9
B10	VCC012	VCC079	AD10
B12	VCC013	VCC080	AD12
B14	VCC014	VCC081	AD14
B15	VCC015	VCC082	AD15
B17	VCC016	VCC083	AD17
B18	VCC017	VCC084	AD18
B20	VCC018	VCC085	AE9
C9	VCC019	VCC086	AE10
C10	VCC020	VCC087	AE12
C12	VCC021	VCC088	AE13
C13	VCC022	VCC089	AE15
C15	VCC023	VCC090	AE17
C17	VCC024	VCC091	AE18
C18	VCC025	VCC092	AE20
D9	VCC026	VCC093	AF9
D10	VCC027	VCC094	AF10
D12	VCC028	VCC095	AF12
D14	VCC029	VCC096	AF14
D15	VCC030	VCC097	AF15
D17	VCC031	VCC098	AF17
D18	VCC032	VCC099	AF18
E7	VCC033	VCC100	AF20
E9	VCC034		
E10	VCC035	VCCP01	G21
E12	VCC036	VCCP02	V6
E13	VCC037	VCCP03	J6
E15	VCC038	VCCP04	K6
E17	VCC039	VCCP05	M6
E18	VCC040	VCCP06	J21
E20	VCC041	VCCP07	K21
F7	VCC042	VCCP08	M21
F9	VCC043	VCCP09	N21
F10	VCC044	VCCP10	N6
F12	VCC045	VCCP11	R21
F14	VCC046	VCCP12	R6
F15	VCC047	VCCP13	T21
F17	VCC048	VCCP14	T6
F18	VCC049	VCCP15	V21
F20	VCC050	VCCP16	W21
AA7	VCC051		
AA9	VCC052	VCCA01	B26
AA10	VCC053	VCCA02	C26
AA12	VCC054		
AA13	VCC055	VID0	AD6
AA15	VCC056	VID1	AE5
AA17	VCC057	VID2	AE5
AA18	VCC058	VID3	AF4
AA20	VCC059	VID4	AF3
AB9	VCC060	VID5	AF3
AC10	VCC061	VID6	AE2
AB10	VCC062		
AB12	VCC063		
AB14	VCC064	VCCSENSE	AF7
AB15	VCC065		
AB17	VCC066		
AB18	VCC067	VSSSENSE	AF7

SOCKET478

VID0 58
VID1 58
VID2 58
VID3 58
VID4 58
VID5 58
VID6 58
VCCSENSE VCCSENSE 58
VSSSENSE VSSSENSE 58

+1.05V_VCCP

CE2 220UF/4V pt_c7343d_h79 +/-20%

+1.5V_RUN

C644 0.01UF/25V MLCC/+/-10% pt_c0603
C645 10UF/6.3V MLCC/+/-20% pt_c0805_h53

Layout Note:
Place 0.01U/25V near PIN B26.

+VCC_CORE

R177 100Ohm 1%
VCCSENSE
VSSSENSE
R176 100Ohm 1%

Route VCCSENSE and VSSSENSE traces at 27.4ohms with 50 mils spacing and length matched to within 25 mil. Place PU and PD within 1 inch of CPU.

U24D MOLEX/47387-4781

A4	VSS001	VSS082	P6
A8	VSS002	VSS083	P21
A11	VSS003	VSS084	P24
A14	VSS004	VSS085	R2
A16	VSS005	VSS086	R5
A19	VSS006	VSS087	R22
A23	VSS007	VSS088	R25
AF2	VSS008	VSS089	T1
B6	VSS009	VSS090	T4
B8	VSS010	VSS091	T23
B11	VSS011	VSS092	T26
B13	VSS012	VSS093	U3
B16	VSS013	VSS094	U6
B19	VSS014	VSS095	U21
B21	VSS015	VSS096	U24
B24	VSS016	VSS097	V2
C5	VSS017	VSS098	V5
C8	VSS018	VSS099	V22
C11	VSS019	VSS100	V25
C14	VSS020	VSS101	W1
C16	VSS021	VSS102	W4
C19	VSS022	VSS103	W23
C2	VSS023	VSS104	W26
C22	VSS024	VSS105	Y3
C25	VSS025	VSS106	Y6
D1	VSS026	VSS107	Y21
D4	VSS027	VSS108	Y24
D8	VSS028	VSS109	AA2
D11	VSS029	VSS110	AA5
D13	VSS030	VSS111	AA8
D16	VSS031	VSS112	AA11
D19	VSS032	VSS113	AA14
D23	VSS033	VSS114	AA16
D26	VSS034	VSS115	AA19
E3	VSS035	VSS116	AA22
E6	VSS036	VSS117	AA25
E8	VSS037	VSS118	AB1
E11	VSS038	VSS119	AB4
E14	VSS039	VSS120	AB8
E16	VSS040	VSS121	AB11
E19	VSS041	VSS122	AB13
E21	VSS042	VSS123	AB16
E24	VSS043	VSS124	AB19
F5	VSS044	VSS125	AB23
F8	VSS045	VSS126	AB26
F11	VSS046	VSS127	AC3
F13	VSS047	VSS128	AC6
F16	VSS048	VSS129	AC8
F19	VSS049	VSS130	AC11
F2	VSS050	VSS131	AC14
F22	VSS051	VSS132	AC16
F25	VSS052	VSS133	AC19
G4	VSS053	VSS134	AC21
G1	VSS054	VSS135	AC24
G23	VSS055	VSS136	AD2
G26	VSS056	VSS137	AD5
H3	VSS057	VSS138	AD8
H6	VSS058	VSS139	AD11
H21	VSS059	VSS140	AD13
H24	VSS060	VSS141	AD16
J2	VSS061	VSS142	AD19
J5	VSS062	VSS143	AD22
J22	VSS063	VSS144	AD25
J25	VSS064	VSS145	AE1
K1	VSS065	VSS146	AE4
K4	VSS066	VSS147	AE8
K23	VSS067	VSS148	AE11
K26	VSS068	VSS149	AE14
L3	VSS069	VSS150	AE16
L6	VSS070	VSS151	AE19
L21	VSS071	VSS152	AF23
L24	VSS072	VSS153	AF26
M2	VSS073	VSS154	A2
M5	VSS074	VSS155	AF6
M22	VSS075	VSS156	AF8
M25	VSS076	VSS157	AF11
N1	VSS077	VSS158	AF13
N4	VSS078	VSS159	AF16
N23	VSS079	VSS160	AF19
N26	VSS080	VSS161	AF21
P3	VSS081	VSS162	A25
		VSS163	AF25

SOCKET478

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Title: MEROM CPU (2)

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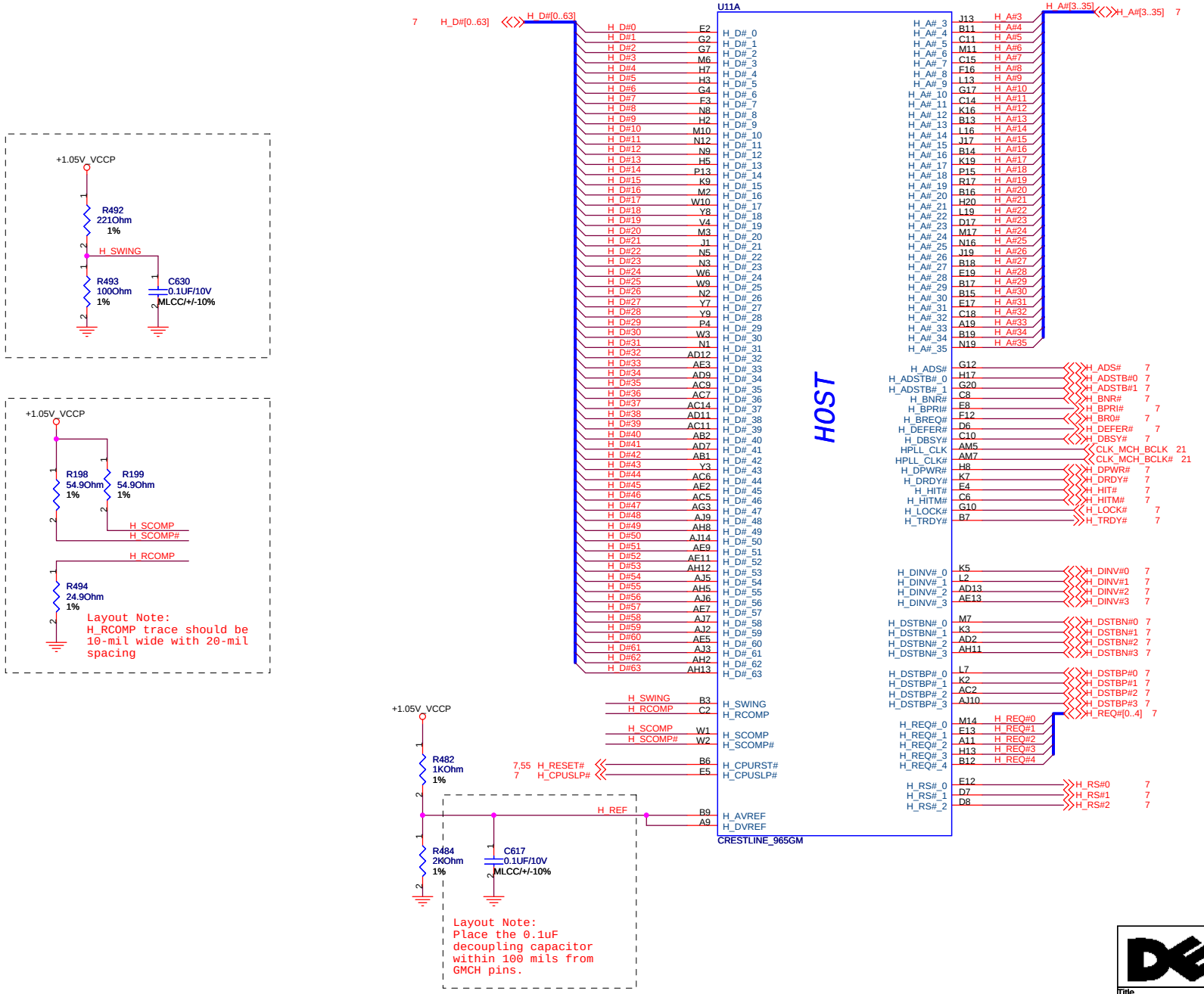

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Title: Crestline(HOST)

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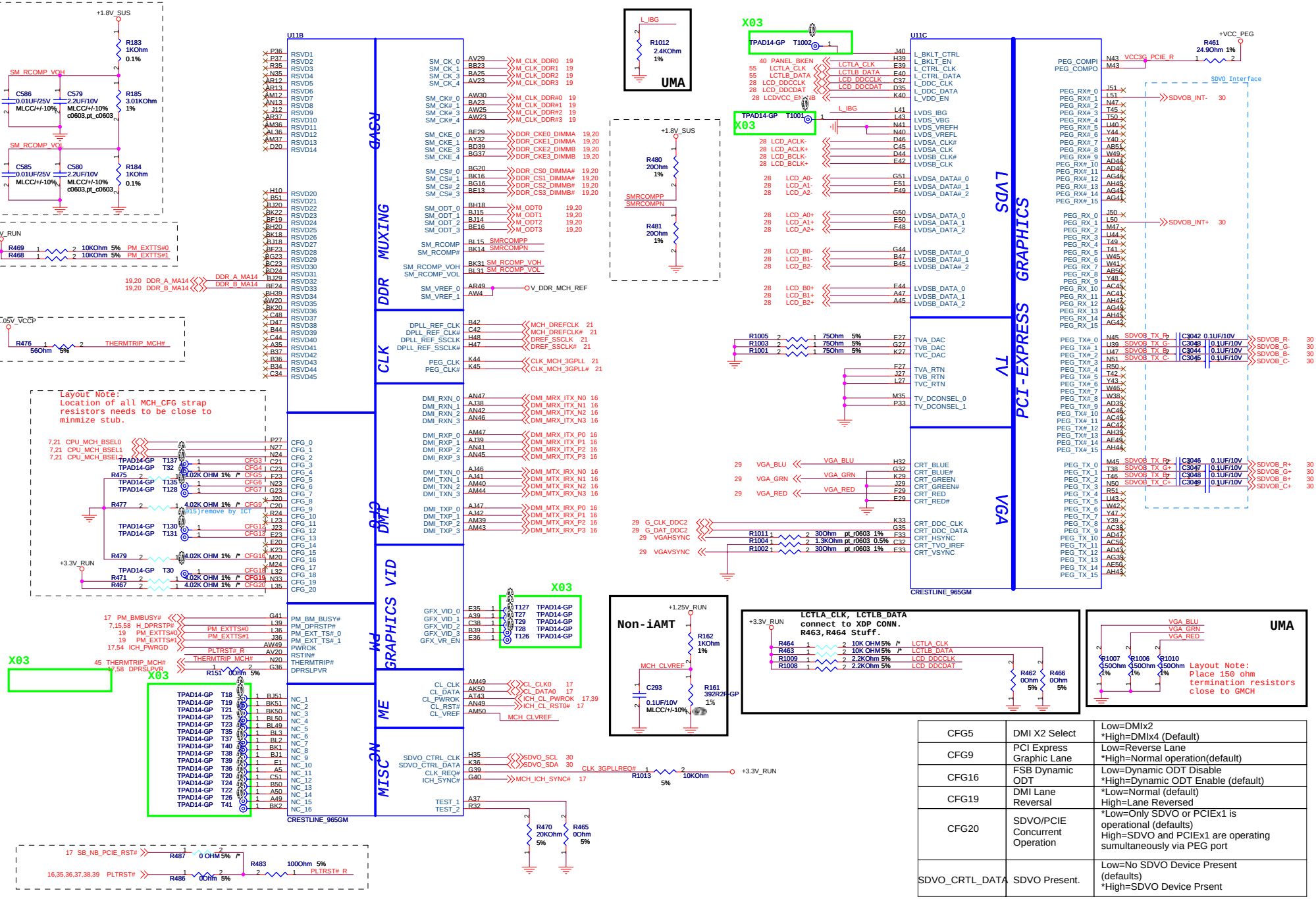

CFG5	DMI X2 Select	Low=DMIx2 *High=DMIx4 (Default)
CFG9	PCI Express Graphic Lane	Low=Reverse Lane *High=Normal operation(default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable *High=Dynamic ODT Enable (default)
CFG19	DMI Lane Reversal	*Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	*Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating sumultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present.	Low=No SDVO Device Present (defaults) *High=SDVO Device Prsent

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Title: Crestline(VGA,DMI)

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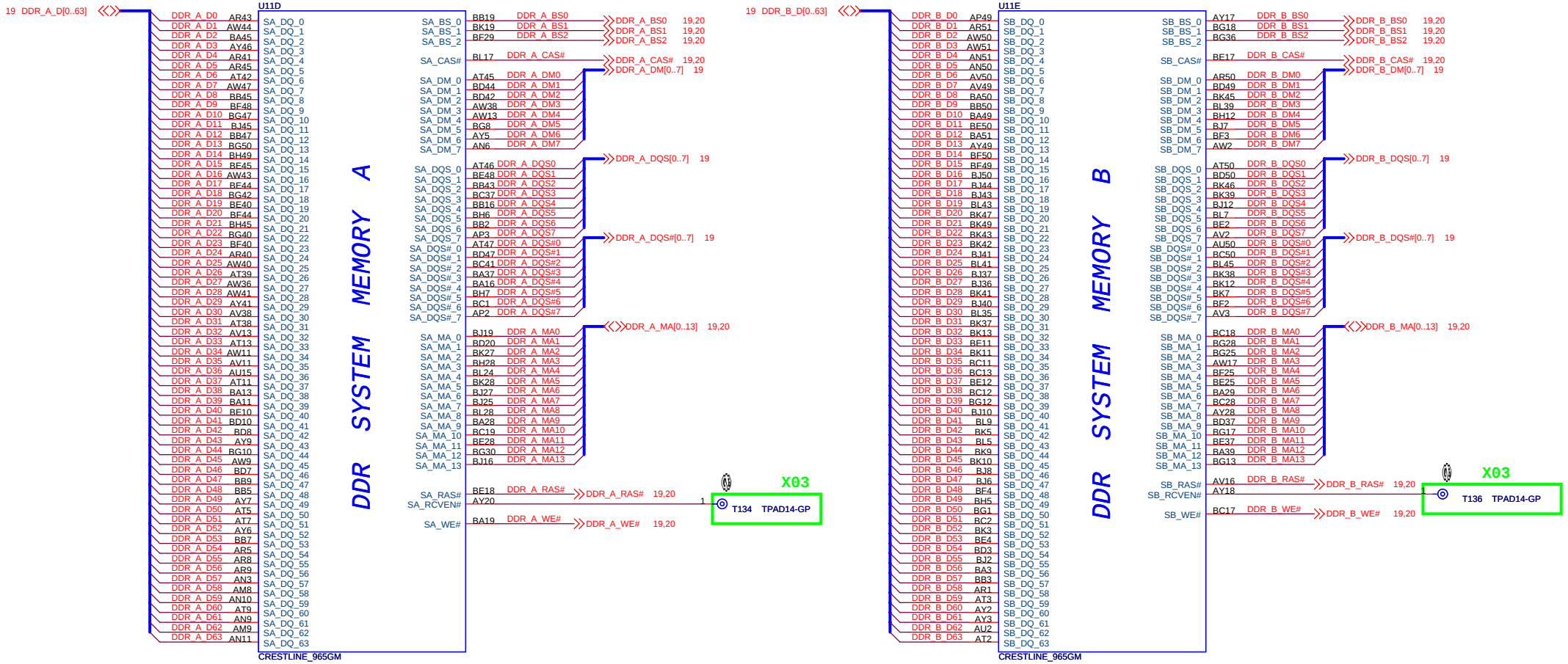

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Title		
	Crestline(DDR2)	
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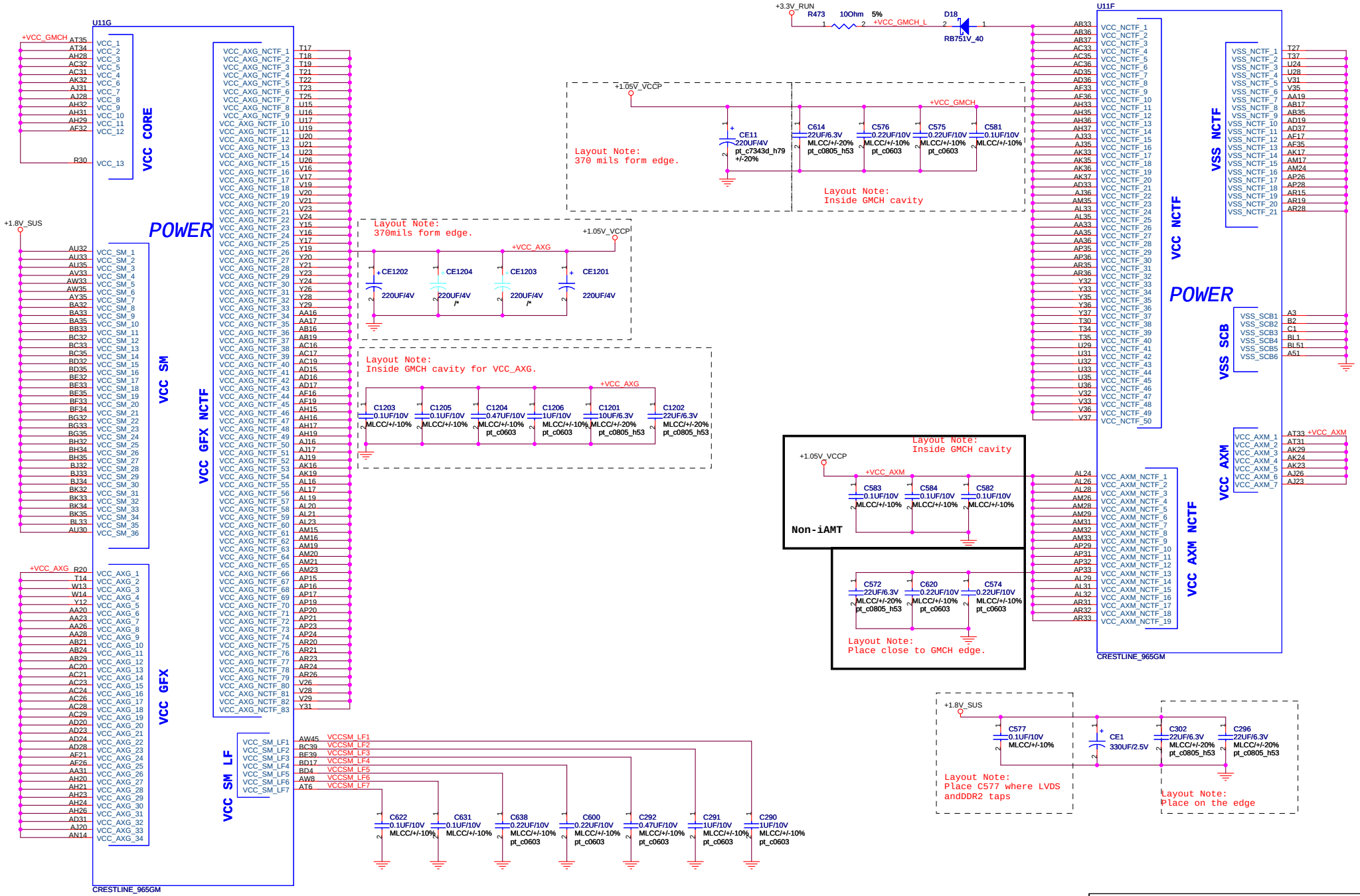

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Title	Crestline(VCC,NCTF)	
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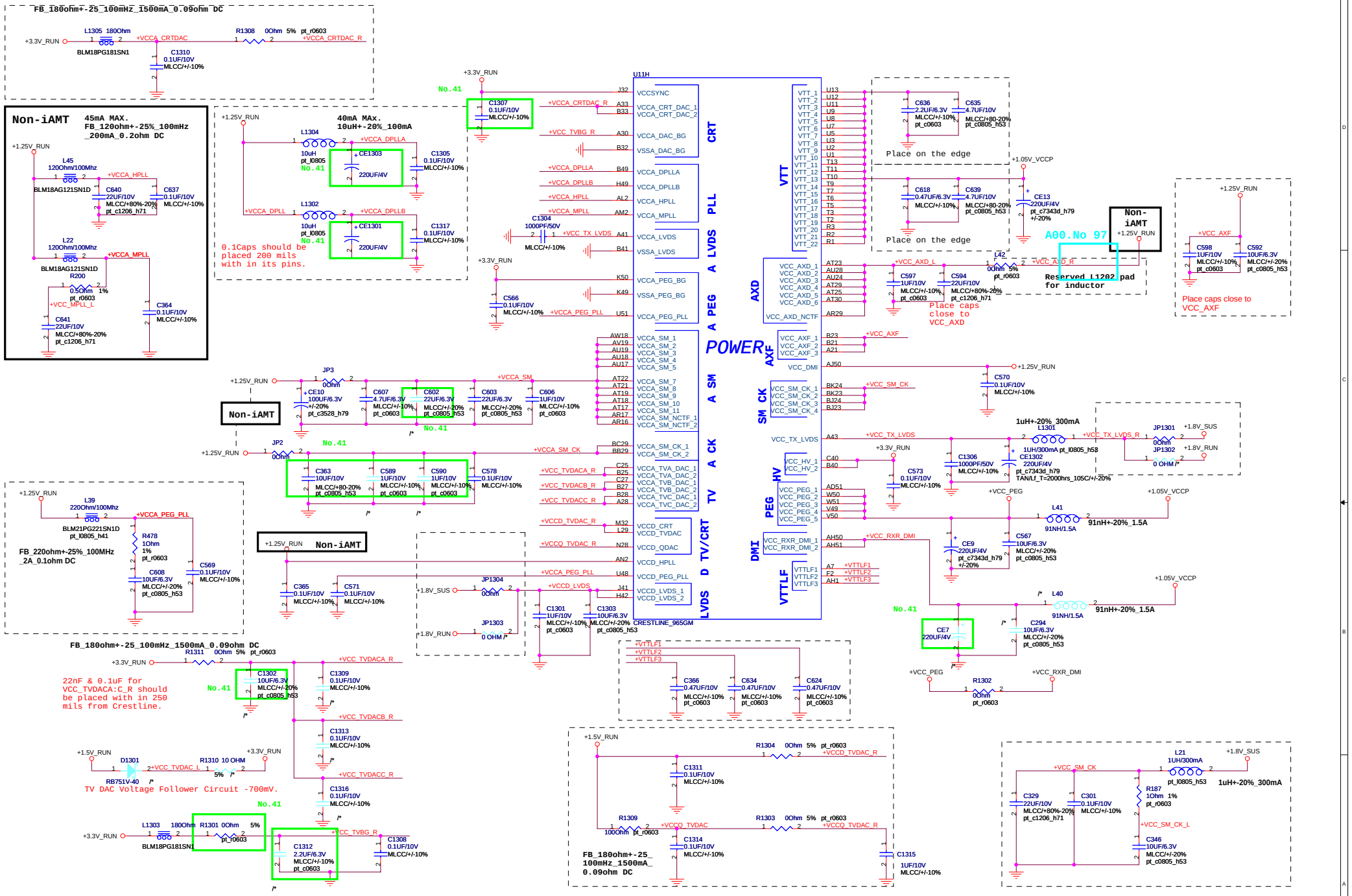

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Title: Crestline(POWER)

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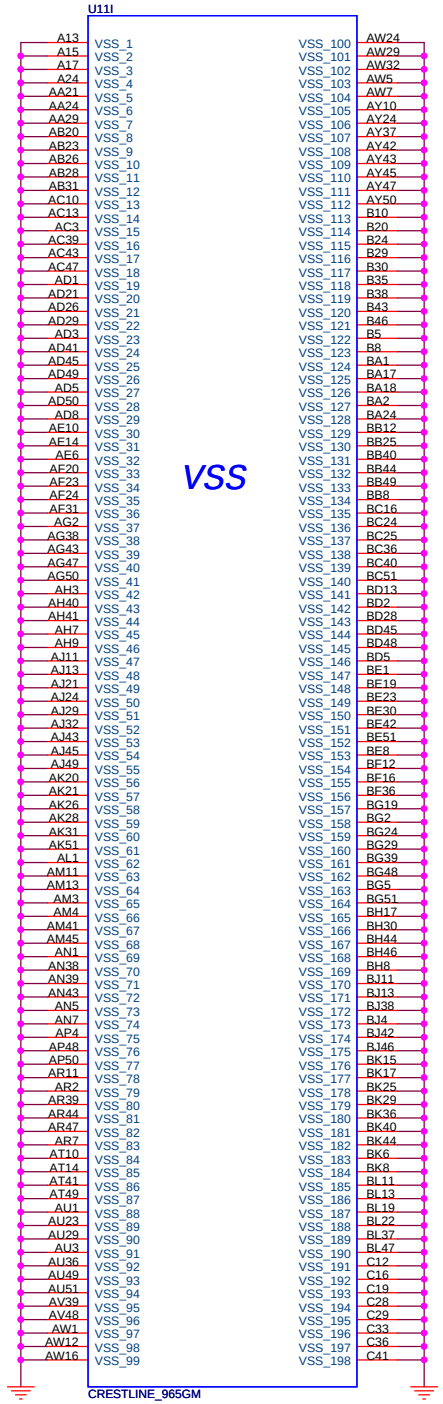

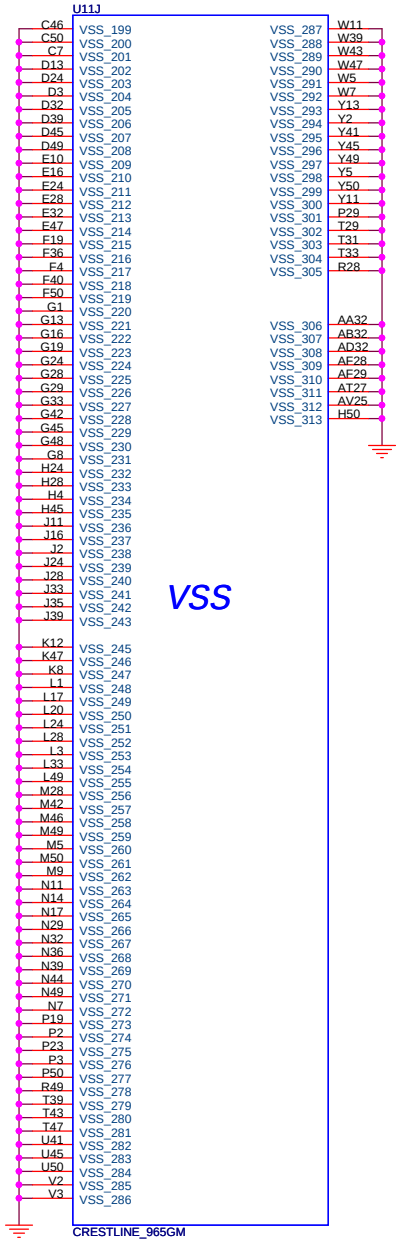

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Title	Crestline(VSS)	
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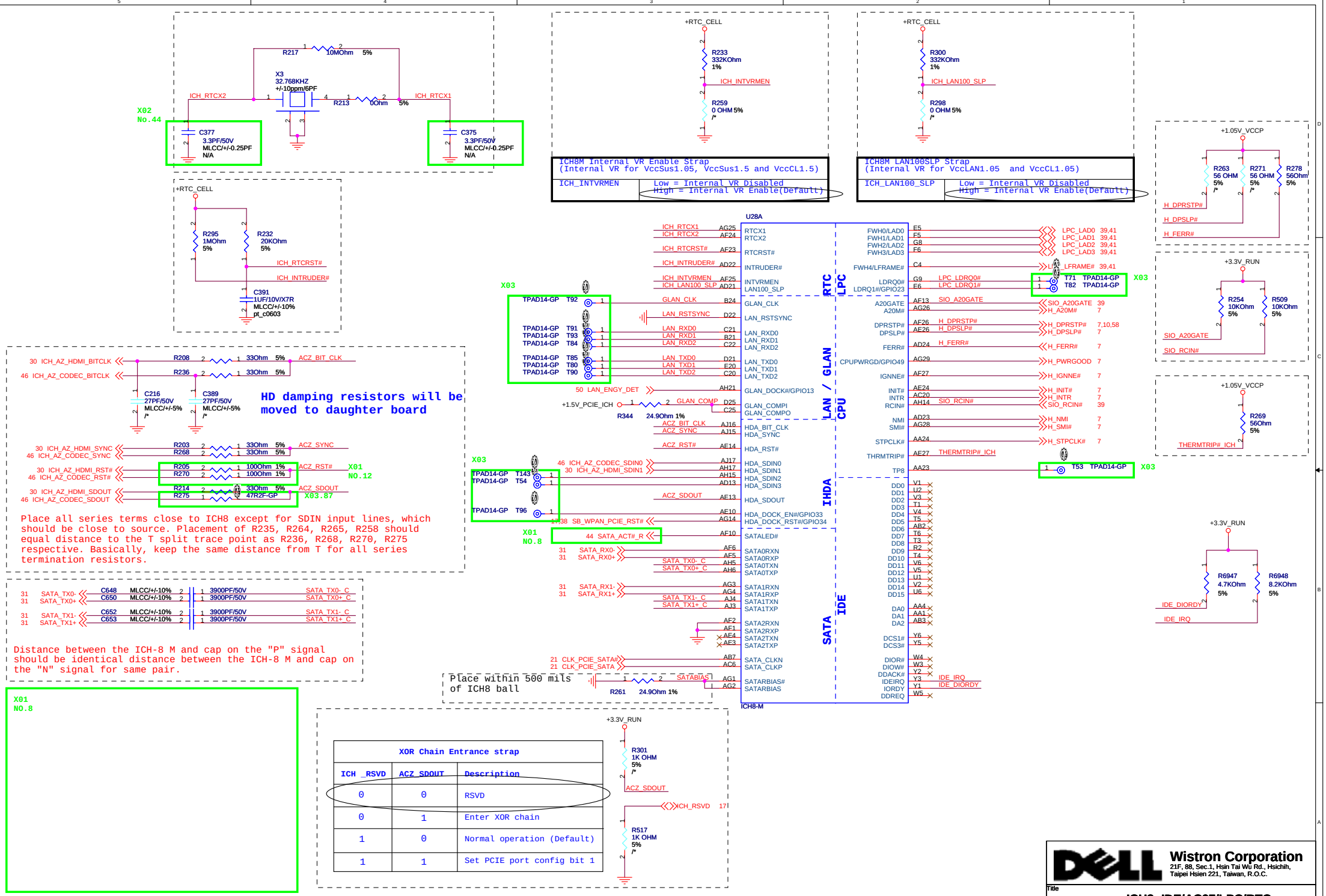
R217 10MOhm 5%
X3 32.768KHZ +/-10ppm/6PF
R213 0Ohm 5%
ICH_RTCX2
ICH_RTCX1
X02 No.44
C377 3.3PF/50V MLCC/+/-0.25PF N/A
C375 3.3PF/50V MLCC/+/-0.25PF N/A
+RTC_CELL
R233 332KOhm 1%
ICH_INTVRMEN
R259 0 OHM 5% /*
ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5 and VccCL1.5)
ICH_INTVRMEN
Low = Internal VR Disabled
High = Internal VR Enable(Default)
+RTC_CELL
R300 332KOhm 1%
ICH_LAN100_SLP
R298 0 OHM 5% /*
ICH8M LAN100SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)
ICH_LAN100_SLP
Low = Internal VR Disabled
High = Internal VR Enable(Default)
+1.05V_VCCP
R263 56 OHM 5% /*
R271 56 OHM 5% /*
R278 56Ohm 5%
H_DPRSTP#
H_DPSLP#
H_FERR#
+RTC_CELL
R295 1MOhm 5%
R232 20KOhm 5%
ICH_RTCRST#
ICH_INTRUDER#
C391 1UF/10V/X7R MLCC/+/-10% pt_c0603
+3.3V_RUN
R254 10KOhm 5%
R509 10KOhm 5%
SIO_A20GATE
SIO_RCIN#
U28A
RTC
LPC
GLAN
LAN / CPU
IHDA
SATA
IDE
ICH8-M
X03
TPAD14-GP T92
TPAD14-GP T91
TPAD14-GP T93
TPAD14-GP T84
TPAD14-GP T85
TPAD14-GP T80
TPAD14-GP T90
TPAD14-GP T143
TPAD14-GP T54
TPAD14-GP T96
X01 NO.8
X01 NO.12
X03.87
30 ICH_AZ_HDMI_BITCLK
46 ICH_AZ_CODEC_BITCLK
R208 33Ohm 5%
R236 33Ohm 5%
ACZ_BIT_CLK
C216 27PF/50V MLCC/+/-5% /*
C389 27PF/50V MLCC/+/-5% /*
HD damping resistors will be moved to daughter board
30 ICH_AZ_HDMI_SYNC
46 ICH_AZ_CODEC_SYNC
R203 33Ohm 5%
R268 33Ohm 5%
ACZ_SYNC
30 ICH_AZ_HDMI_RST#
46 ICH_AZ_CODEC_RST#
R205 100Ohm 1%
R270 100Ohm 1%
ACZ_RST#
30 ICH_AZ_HDMI_SDOUT
46 ICH_AZ_CODEC_SDOUT
R214 33Ohm 5%
R275 47R2F-GP
ACZ_SDOUT
Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R235, R264, R265, R258 should equal distance to the T split trace point as R236, R268, R270, R275 respective. Basically, keep the same distance from T for all series termination resistors.
31 SATA_TX0-
31 SATA_TX0+
C648 MLCC/+/-10% 3900PF/50V
C650 MLCC/+/-10% 3900PF/50V
SATA_TX0- C
SATA_TX0+ C
31 SATA_TX1-
31 SATA_TX1+
C652 MLCC/+/-10% 3900PF/50V
C653 MLCC/+/-10% 3900PF/50V
SATA_TX1- C
SATA_TX1+ C
Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.
X01 NO.8
ICH_RTCX1 AG25
ICH_RTCX2 AF24
ICH_RTCRST# AF23
ICH_INTRUDER# AD22
ICH_INTVRMEN AF25
ICH_LAN100_SLP AD21
GLAN_CLK B24
LAN_RSTSYNC D22
LAN_RXD0 C21
LAN_RXD1 B21
LAN_RXD2 C22
LAN_TXD0 D21
LAN_TXD1 E20
LAN_TXD2 C20
50 LAN_ENGY_DET AH21
+1.5V_PCIE_ICH
GLAN_COMP D25
C25
R344 24.9Ohm 1%
ACZ_BIT_CLK AJ16
ACZ_SYNC AJ15
ACZ_RST# AE14
46 ICH_AZ_CODEC_SDIN0 AJ17
30 ICH_AZ_HDMI_SDIN1 AH17
AH15
AD13
ACZ_SDOUT AE13
AE10
17 38 SB_WPAN_PCIE_RST# AG14
44 SATA_ACT#_R AF10
31 SATA_RX0- AF6
31 SATA_RX0+ AF5
SATA_TX0- C AH5
SATA_TX0+ C AH6
31 SATA_RX1- AG3
31 SATA_RX1+ AG4
SATA_TX1- C AJ4
SATA_TX1+ C AJ3
AF2
AF1
AE4
AE3
21 CLK_PCIE_SATA# AB7
21 CLK_PCIE_SATA AC6
Place within 500 mils of ICH8 ball
SATABIAS AG1
AG2
R261 24.9Ohm 1%
FWH0/LAD0 E5
FWH1/LAD1 F5
FWH2/LAD2 G8
FWH3/LAD3 F6
FWH4/LFRAME# C4
LDRQ0# G9
LDRQ1#/GPIO23 E6
A20GATE AF13
A20M# AG26
DPRSTP# AF26
DPSLP# AE26
FERR# AD24
CPUPWRGD/GPIO49 AG29
IGNNE# AF27
INIT# AE24
INTR AC20
RCIN# AH14
NMI AD23
SMI# AG28
STPCLK# AA24
THRMTRIP# AE27
TP8 AA23
DD0 V1
DD1 U2
DD2 V3
DD3 T1
DD4 V4
DD5 T5
DD6 AB2
DD7 T6
DD8 T3
DD9 R2
DD10 T4
DD11 V6
DD12 V5
DD13 U1
DD14 V2
DD15 U6
DA0 AA4
DA1 AA1
DA2 AB3
DCS1# Y6
DCS3# Y5
DIOR# W4
DIOW# W3
DDACK# Y2
IDEIRQ Y3
IORDY Y1
DDREQ W5
LPC_LAD0 39,41
LPC_LAD1 39,41
LPC_LAD2 39,41
LPC_LAD3 39,41
LFRAME# 39,41
T71 TPAD14-GP
T82 TPAD14-GP
LPC_LDRQ0#
LPC_LDRQ1#
SIO_A20GATE 39
H_A20M# 7
H_DPRSTP# 7,10,58
H_DPSLP# 7
H_FERR# 7
H_PWRGOOD 7
H_IGNNE# 7
H_INIT# 7
H_INTR 7
SIO_RCIN# 39
H_NMI 7
H_SMI# 7
H_STPCLK# 7
THERMTRIP# ICH
T53 TPAD14-GP
IDE_IRQ
IDE_DIORDY
+3.3V_RUN
R6947 4.7KOhm 5%
R6948 8.2KOhm 5%
IDE_DIORDY
IDE_IRQ
+3.3V_RUN
R301 1K OHM 5% /*
ACZ_SDOUT
ICH_RSVD 17
R517 1K OHM 5% /*
XOR Chain Entrance strap
ICH _RSVD | ACZ_SDOUT | Description
0 | 0 | RSVD
0 | 1 | Enter XOR chain
1 | 0 | Normal operation (Default)
1 | 1 | Set PCIE port config bit 1
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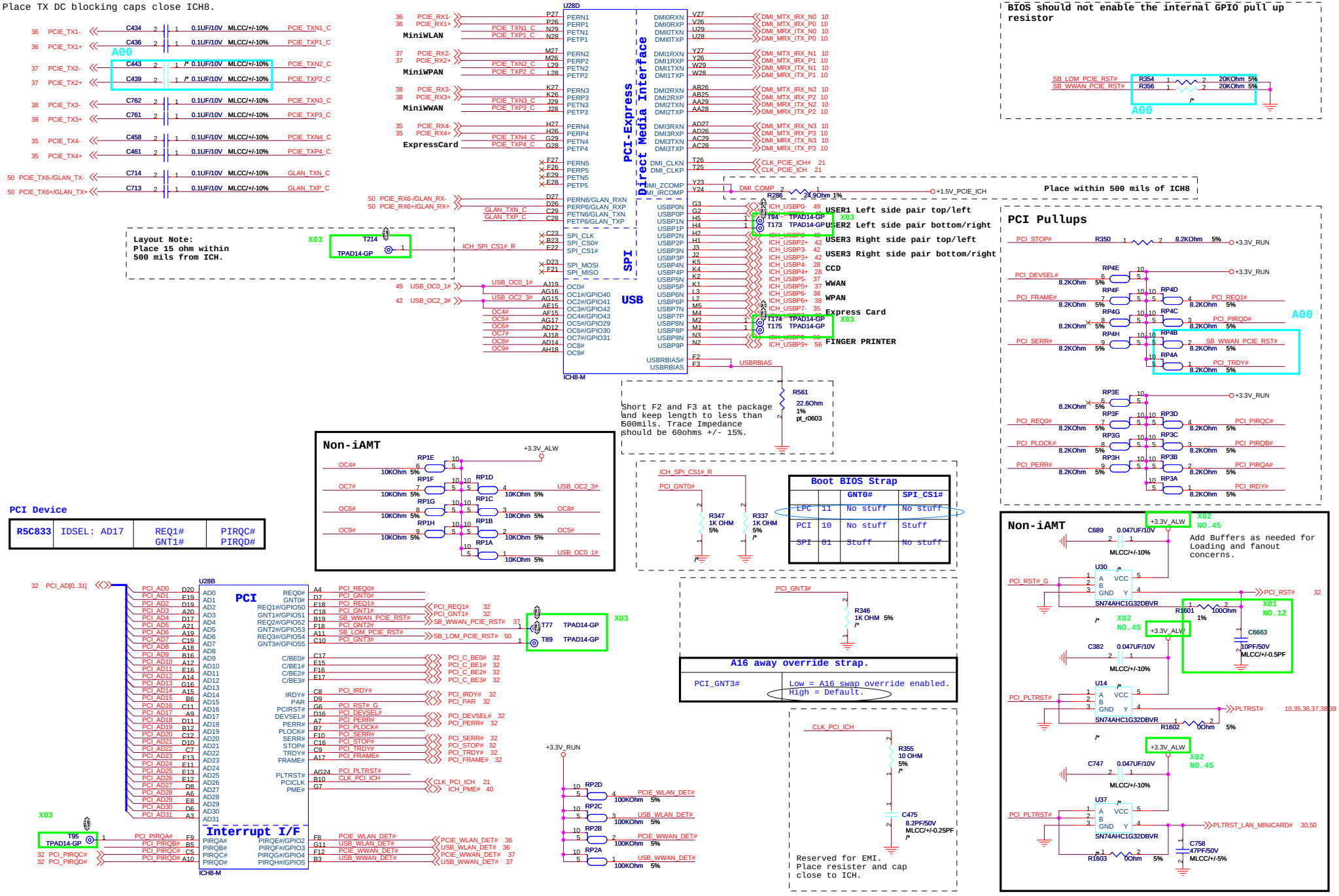
Title
ICH8: IDE/AC97/LPC/RTC
Size Custom
Document Number Diaz-UMA
Rev A00
Date: Tuesday, August 19, 2008
Sheet 15 of 68

Place TX DC blocking caps close ICH8.



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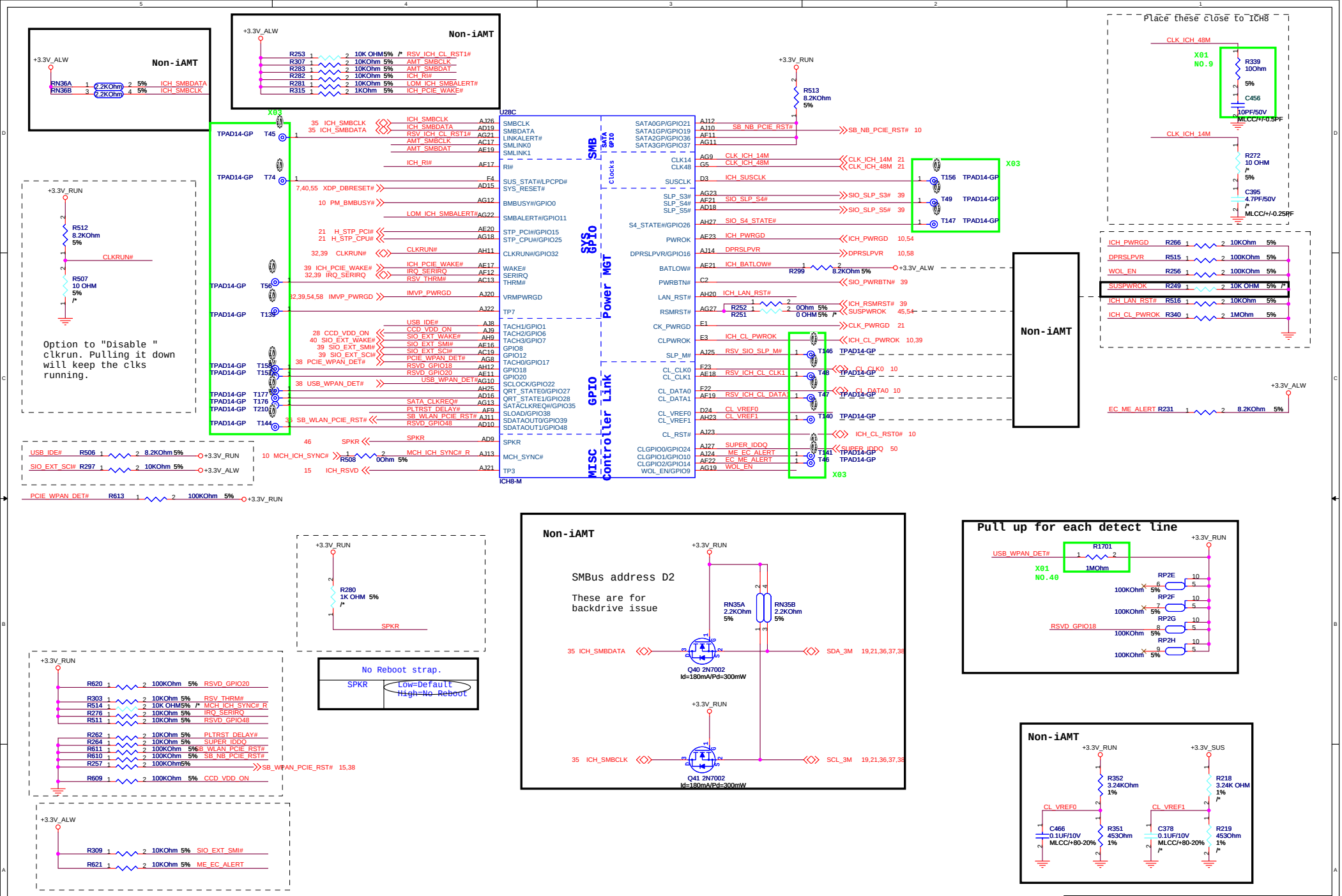
Title: ICH8: PCI/INT/DMI/USB

Size: Custom | Document Number: Diaz-UMA | Rev: A00

Date: Tuesday, August 19, 2008 | Sheet 16 of 68



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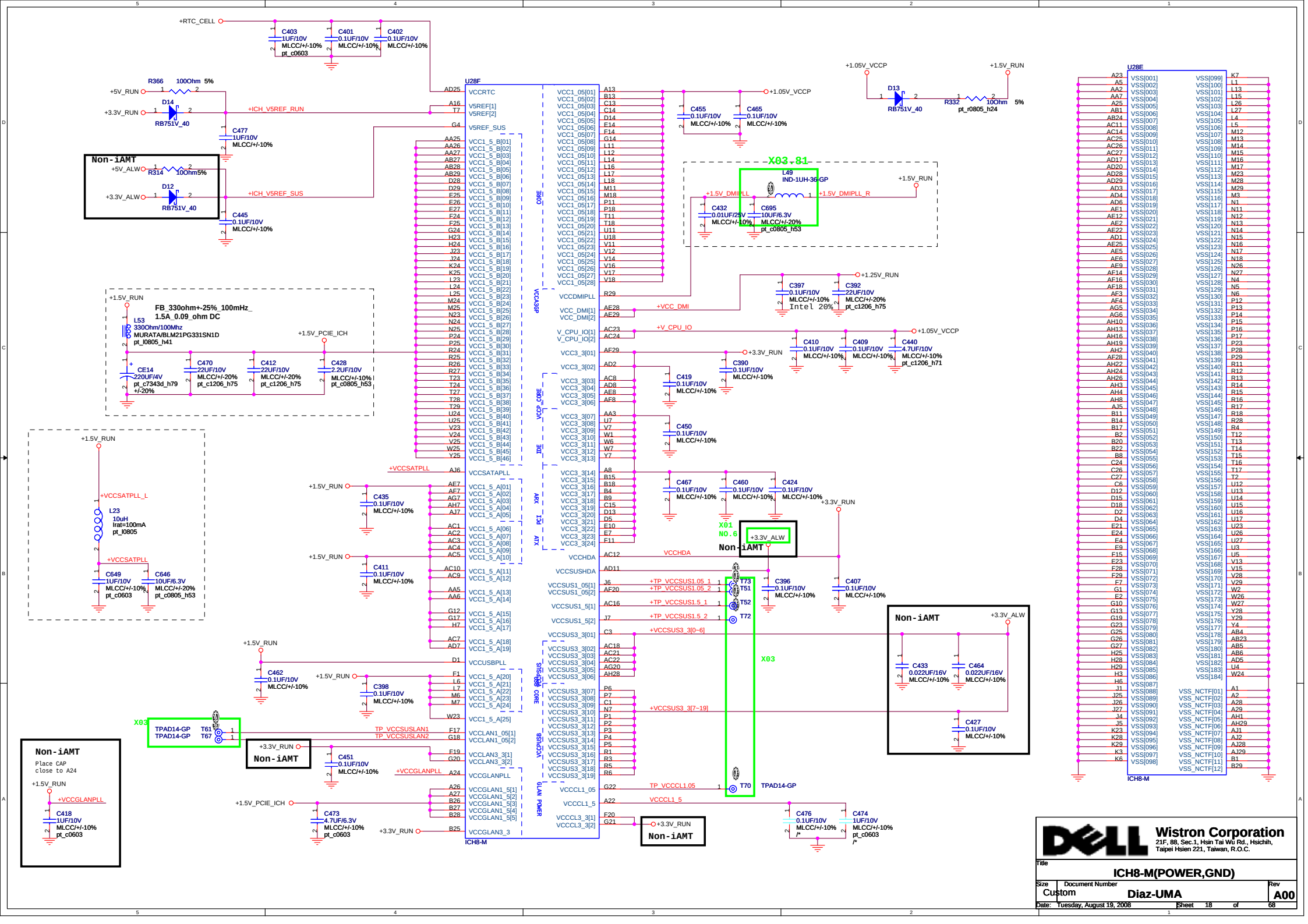
Title: ICH8: SMB/PWR/CLK/GPIO

Size: Custom | Document Number: Diaz-UMA | Rev: A00

Date: Tuesday, August 19, 2008 | Sheet 17 of 68


U28F
ICH8-M
U28E
ICH8-M
+RTC_CELL
C403 1UF/10V MLCC/+/-10% pt_c0603
C401 0.1UF/10V MLCC/+/-10%
C402 0.1UF/10V MLCC/+/-10%
R366 100Ohm 5%
+5V_RUN
+3.3V_RUN
D14 RB751V_40
+ICH_V5REF_RUN
C477 1UF/10V MLCC/+/-10%
Non-iAMT
+5V_ALW
R314 10Ohm5%
+3.3V_ALW
D12 RB751V_40
+ICH_V5REF_SUS
C445 0.1UF/10V MLCC/+/-10%
+1.5V_RUN
FB_330ohm+-25%_100mHz_ 1.5A_0.09_ohm DC
L53 330Ohm/100Mhz MURATA/BLM21PG331SN1D pt_l0805_h41
+1.5V_PCIE_ICH
CE14 220UF/4V pt_c7343d_h79 +/-20%
C470 22UF/10V MLCC/+/-20% pt_c1206_h75
C412 22UF/10V MLCC/+/-20% pt_c1206_h75
C428 2.2UF/10V MLCC/+/-10% pt_c0805_h53
+VCCSATPLL_L
L23 10uH Irat=100mA pt_l0805
+VCCSATPLL
C649 1UF/10V MLCC/+/-10% pt_c0603
C646 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C435 0.1UF/10V MLCC/+/-10%
C411 0.1UF/10V MLCC/+/-10%
C462 0.1UF/10V MLCC/+/-10%
C398 0.1UF/10V MLCC/+/-10%
X03
TPAD14-GP T61
TPAD14-GP T67
TP_VCCSUSLAN1
TP_VCCSUSLAN2
+3.3V_RUN
Non-iAMT
C451 0.1UF/10V MLCC/+/-10%
+VCCGLANPLL
Non-iAMT
Place CAP close to A24
C418 1UF/10V MLCC/+/-10% pt_c0603
C473 4.7UF/6.3V MLCC/+/-10% pt_c0603
+1.05V_VCCP
C455 0.1UF/10V MLCC/+/-10%
C465 0.1UF/10V MLCC/+/-10%
D13 RB751V_40
R332 10Ohm 5% pt_r0805_h24
+1.5V_RUN
X03-81
L49 IND-1UH-36-GP
+1.5V_DMIPLL
+1.5V_DMIPLL_R
C432 0.01UF/25V MLCC/+/-10%
C695 10UF/6.3V MLCC/+/-20% pt_c0805_h53
+1.25V_RUN
C397 0.1UF/10V MLCC/+/-10% Intel 20%
C392 22UF/10V MLCC/+/-20% pt_c1206_h75
+VCC_DMI
+V_CPU_IO
+1.05V_VCCP
C410 0.1UF/10V MLCC/+/-10%
C409 0.1UF/10V MLCC/+/-10%
C440 4.7UF/10V MLCC/+/-10% pt_c1206_h71
+3.3V_RUN
C390 0.1UF/10V MLCC/+/-10%
C419 0.1UF/10V MLCC/+/-10%
C450 0.1UF/10V MLCC/+/-10%
C467 0.1UF/10V MLCC/+/-10%
C460 0.1UF/10V MLCC/+/-10%
C424 0.1UF/10V MLCC/+/-10%
+3.3V_RUN
X01 NO.6
+3.3V_ALW
Non-iAMT
VCCHDA
C396 0.1UF/10V MLCC/+/-10%
C407 0.1UF/10V MLCC/+/-10%
+TP_VCCSUS1.05_1
+TP_VCCSUS1.05_2
+TP_VCCSUS1.5_1
+TP_VCCSUS1.5_2
T73
T51
T52
T72
+VCCSUS3_3[0~6]
X03
Non-iAMT
+3.3V_ALW
C433 0.022UF/16V MLCC/+/-10%
C464 0.022UF/16V MLCC/+/-10%
C427 0.1UF/10V MLCC/+/-10%
+VCCSUS3_3[7~19]
TP_VCCCL1.05
T70
TPAD14-GP
VCCCL1_5
C476 0.1UF/10V MLCC/+/-10% /*
C474 1UF/10V MLCC/+/-10% pt_c0603 /*
+3.3V_RUN
Non-iAMT
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Title
ICH8-M(POWER,GND)
Size Custom
Document Number Diaz-UMA
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Date: Tuesday, August 19, 2008
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A is required to route to Top SODIMM for AMT to function
Ch.A SODIMM needs to be populated for Intel AMT support.

TOP

CON14

FOXCONN/AS0A426-N2RN-7F

REV

CLOCK 0 , 1
CKE 0 , 1

SMbus address A0

Non-iAMT

BOT

CON15

FOXCONN/AS0A426-NARN-7F

REV

CLOCK 2 , 3
CKE 2 , 3

SMbus address A4

Non-iAMT

Please these Caps near So-Dimm1

Please these Caps near So-Dimm2

Please these Caps near So-Dimm1

Please these Caps near So-Dimm2

Non-iAMT

Non-iAMT

Non-iAMT

Non-iAMT

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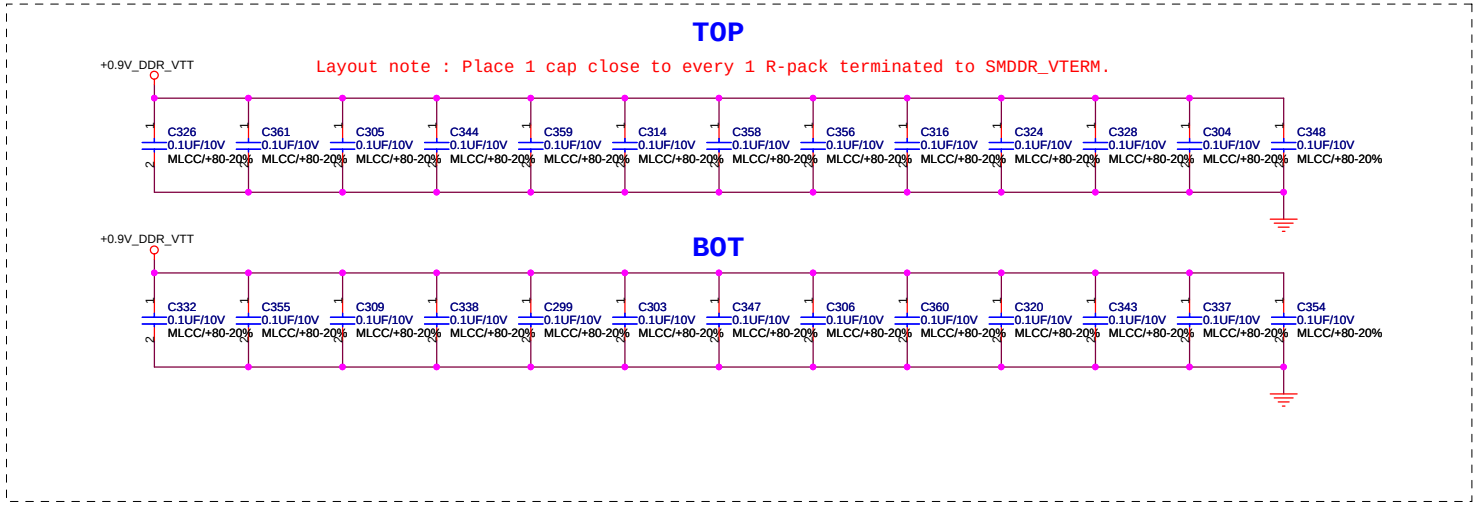
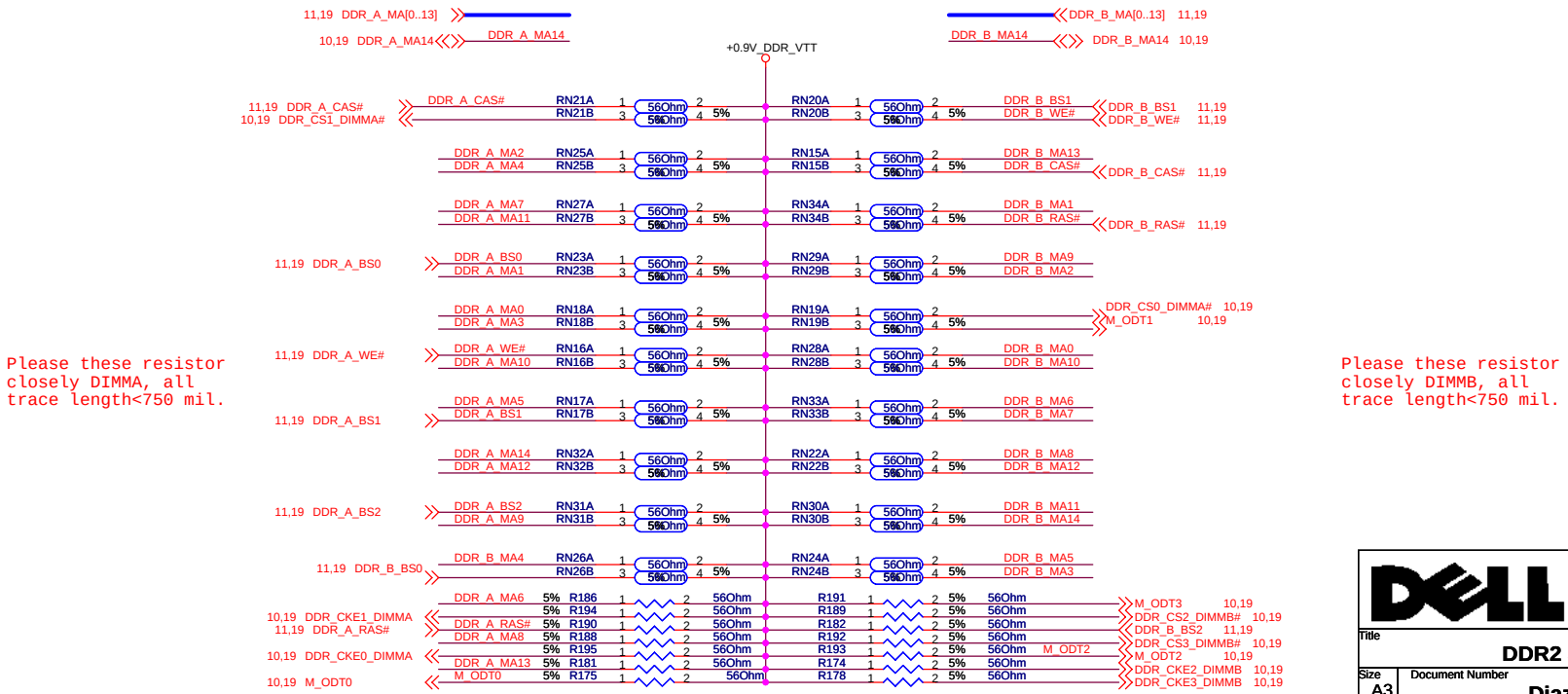
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 SO-DIMM (0)

Size: Custom | Document Number: Diaz-UMA | Rev: A00

Date: Tuesday, August 19, 2008 | Sheet 19 of 68





Please these resistor closely DIMMA, all trace length<750 mil.

Please these resistor closely DIMMB, all trace length<750 mil.

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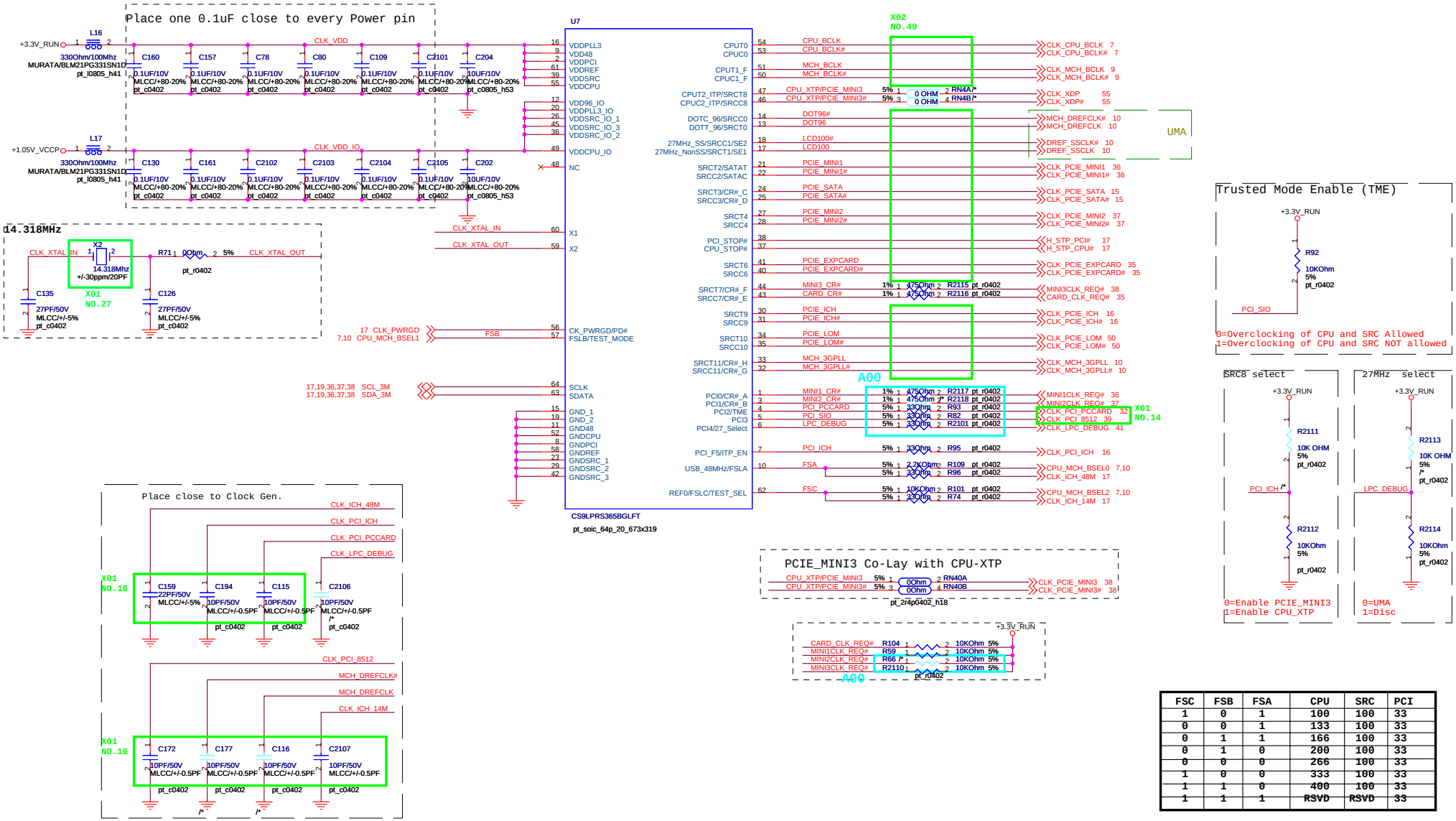
Title: DDR2 SO-DIMM (1)

Size: A3 | Document Number: Diaz-UMA | Rev: A00

Date: Tuesday, August 19, 2008 | Sheet 20 of 68



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	RSVD	33

LPC_DEBUG=SEL_27M(Disc. VGA) or LCDCLK#

LPC_DEBUG(PIN 6)	Pin13	Pin14	Pin17	Pin18
0 = UMA	DOT96T	DOT96C	LCD100T	LCD100C
1 = Disc.	SRC0T	SRC0C	27M_NSS	27M_SS
GRFX down				

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Title: CLK GEN. ICS9LPRS365BGLFT

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Date: Tuesday, August 19, 2008 | Sheet 21 of 68

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Size A3	Document Number Diaz-UMA	Rev A00
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Title	BLANK PAGE
Size	A3
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Title		
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Size A3	Document Number Diaz-UMA	Rev A00
Date: Tuesday, August 19, 2008	Sheet 24 of 68	

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Size A3	Document Number Diaz-UMA	Rev A00
Date: Tuesday, August 19, 2008	Sheet 25 of 68	

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Title	BLANK PAGE	
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Title	BLANK PAGE	
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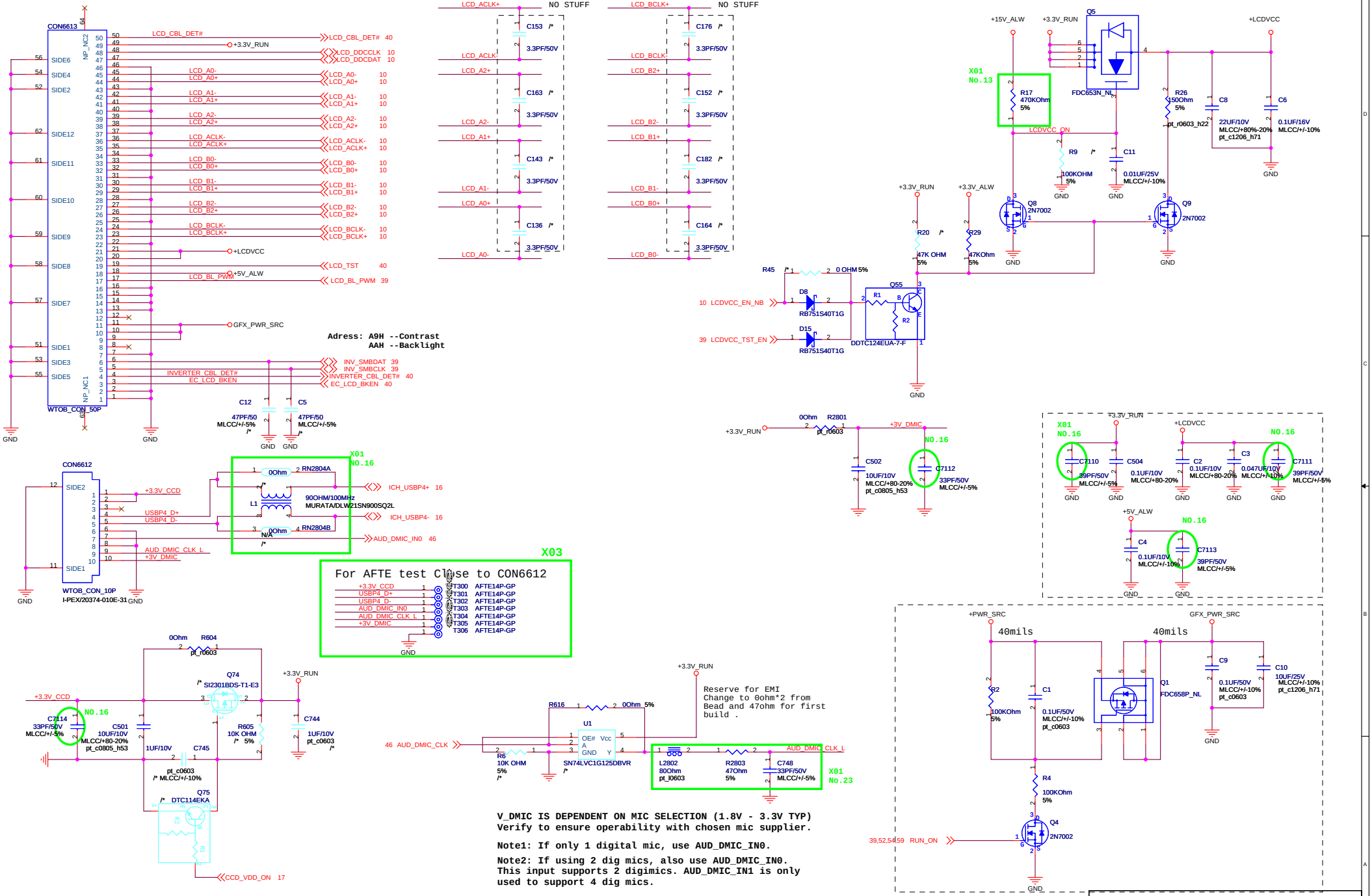

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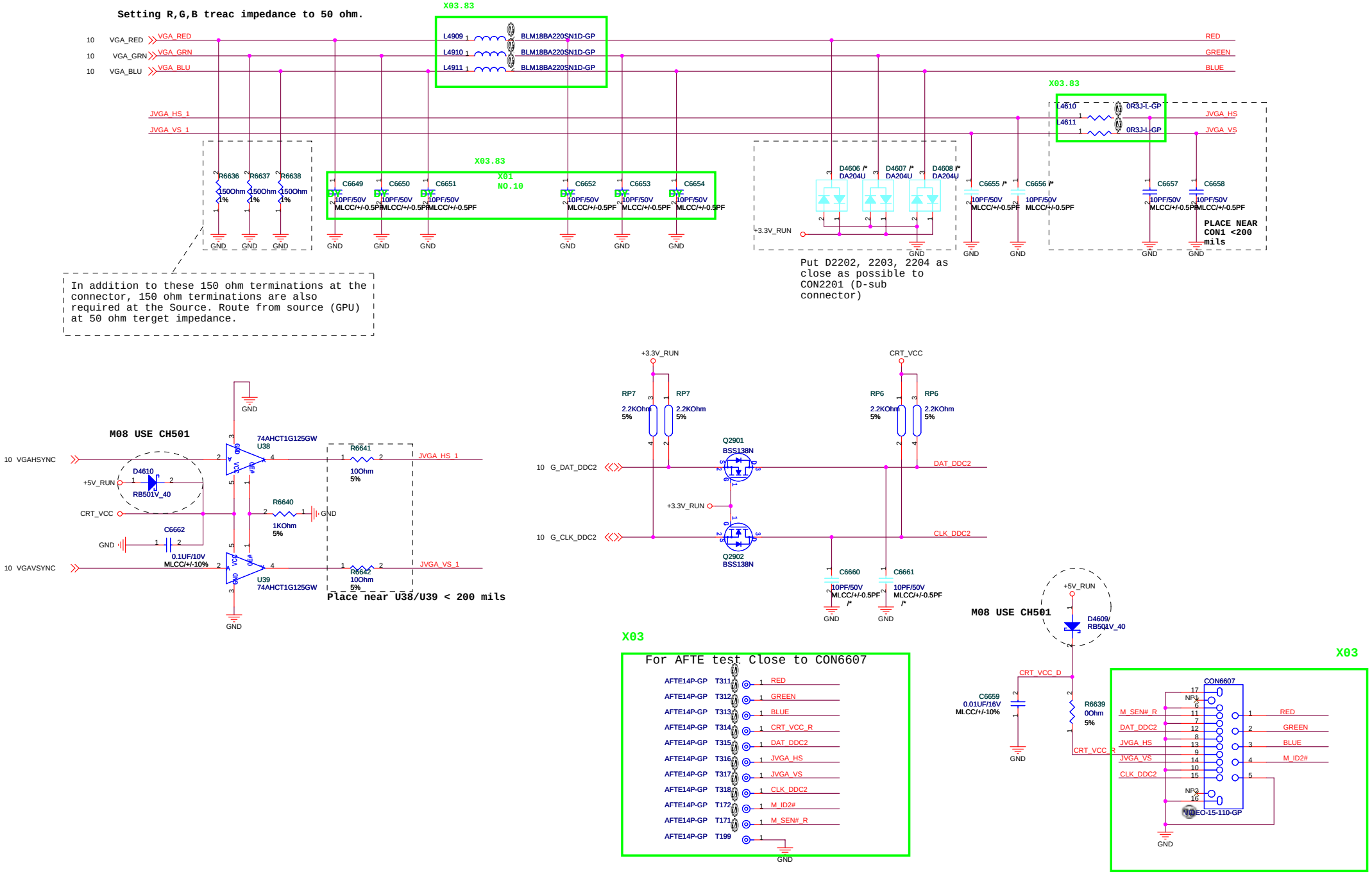
Title: **LVDS CON**

Size	Document Number	Rev
Custom	Diaz-UMA	A00

Date: Tuesday, August 19, 2008 Sheet 28 of 68

Setting R,G,B treac impedance to 50 ohm.



In addition to these 150 ohm terminations at the connector, 150 ohm terminations are also required at the Source. Route from source (GPU) at 50 ohm terget impedance.

Put D2202, 2203, 2204 as close as possible to CON2201 (D-sub connector)

M08 USE CH501

10 VGAHSYNC
+5V_RUN
D4610 RB501V_40
CRT_VCC
GND
C6662 0.1UF/10V MLCC/+/-10%
10 VGAVSYNC
74AHCT1G125GW U38
U39 74AHCT1G125GW
R6641 10Ohm 5%
R6640 1KOhm 5%
R6642 10Ohm 5%
JVGA_HS_1
JVGA_VS_1
Place near U38/U39 < 200 mils

M08 USE CH501

X03

For AFTE test Close to CON6607

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Title: VGA CRT CON

Size	Document Number	Rev
Custom	Diaz-UMA	A00

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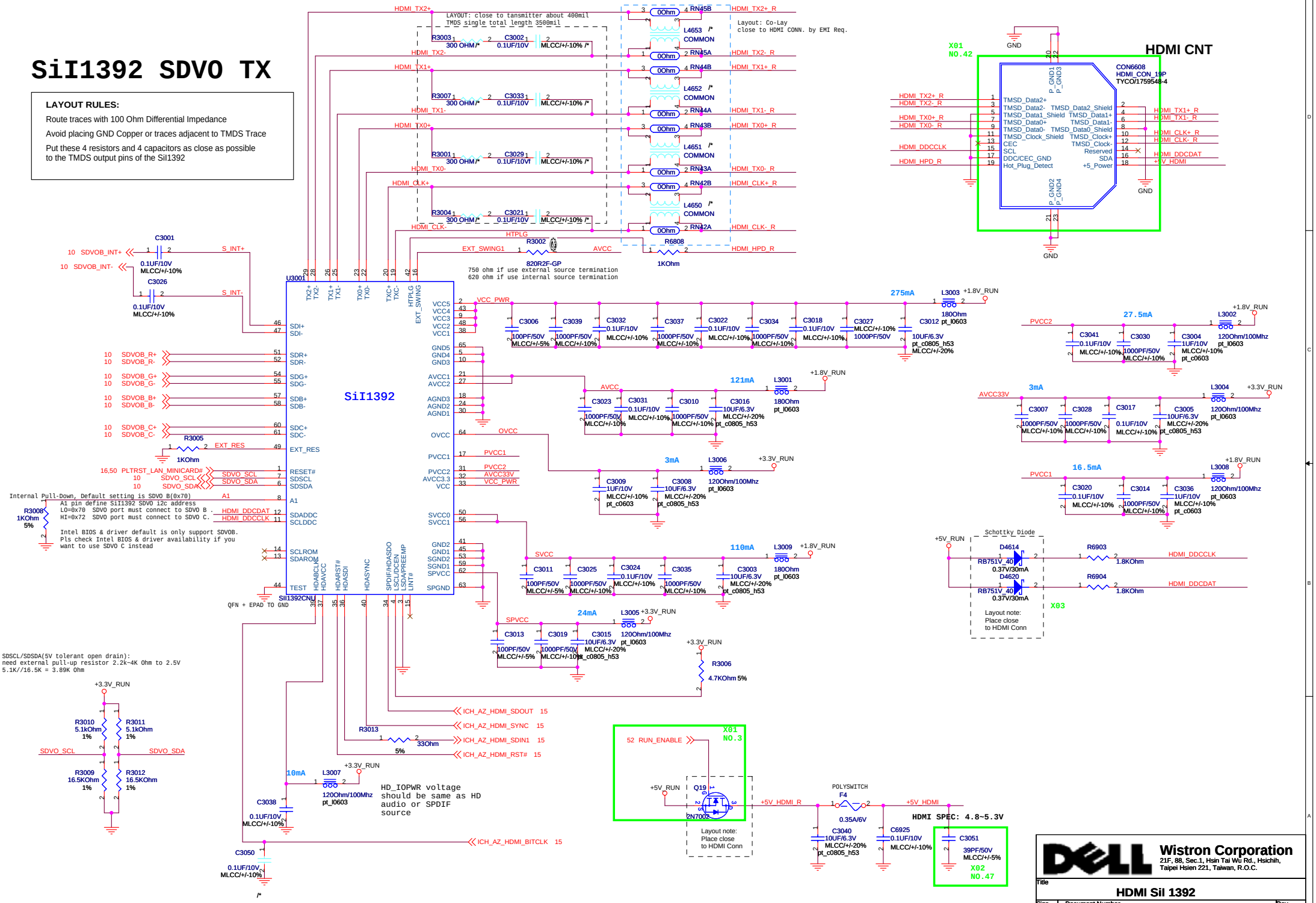
SiI1392 SDVO TX

LAYOUT RULES:

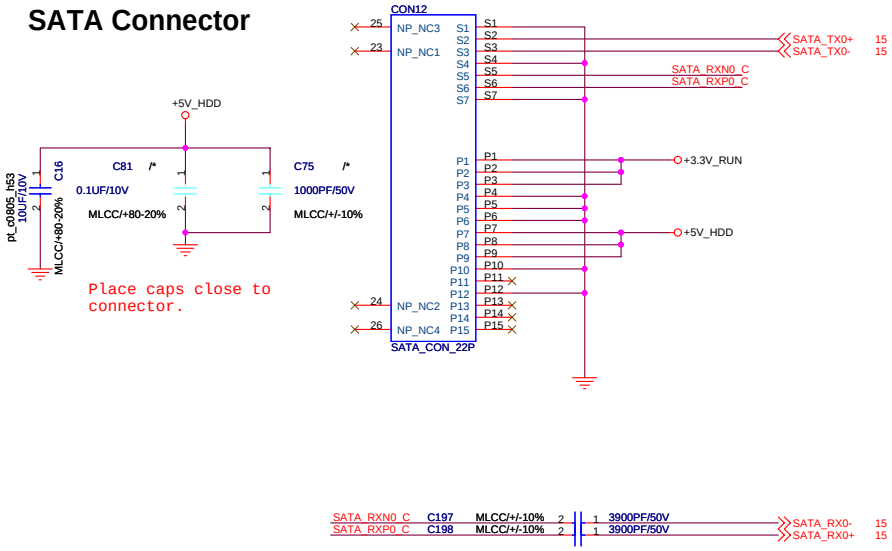
Route traces with 100 Ohm Differential Impedance

Avoid placing GND Copper or traces adjacent to TMDS Trace

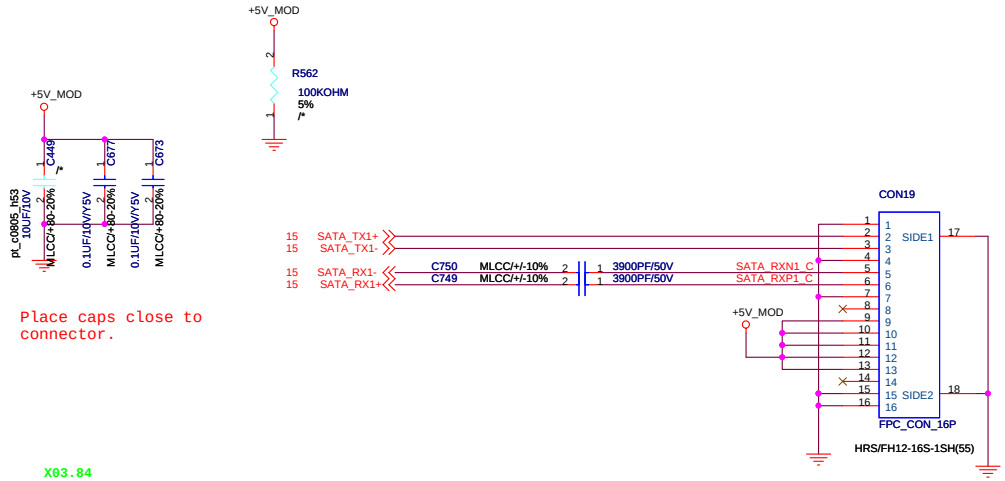
Put these 4 resistors and 4 capacitors as close as possible to the TMDS output pins of the Sil1392



SATA Connector

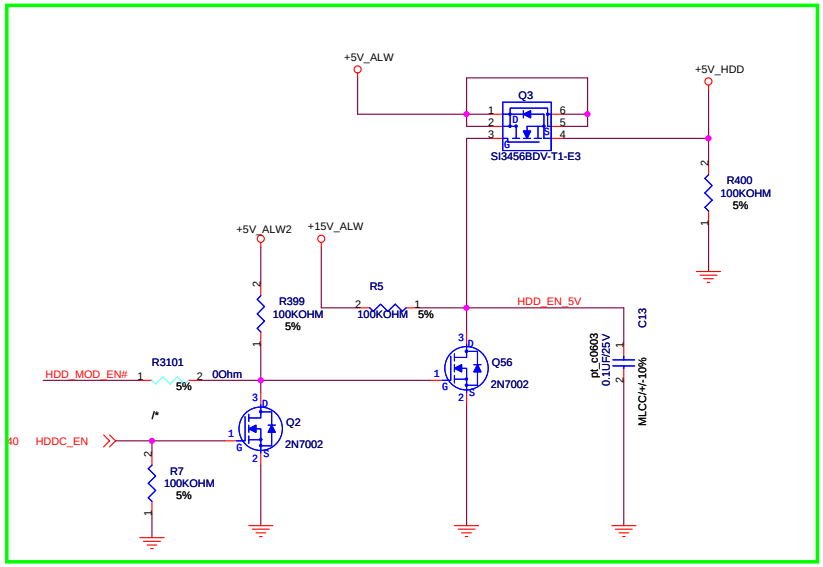


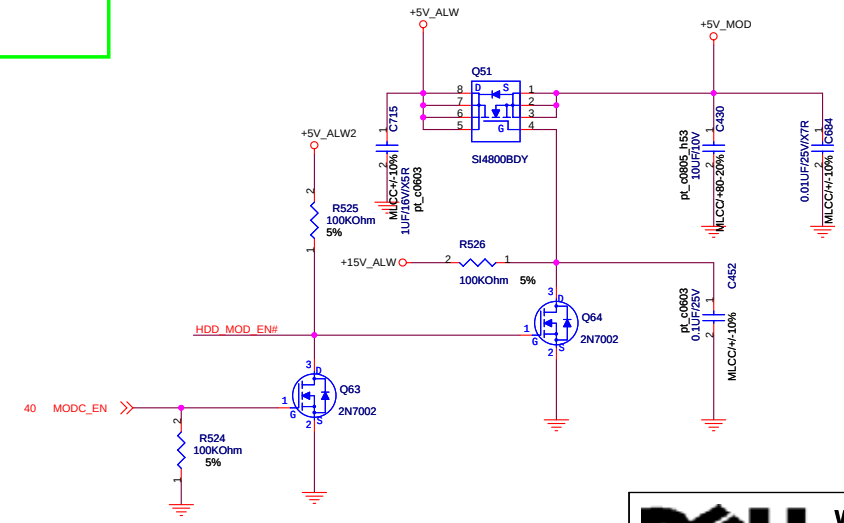
ODD Connector



X03.84

N0.32





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Title: SATA(HDD & CD_ROM)

Size	Document Number	Rev
Custom	Diaz-UMA	A00

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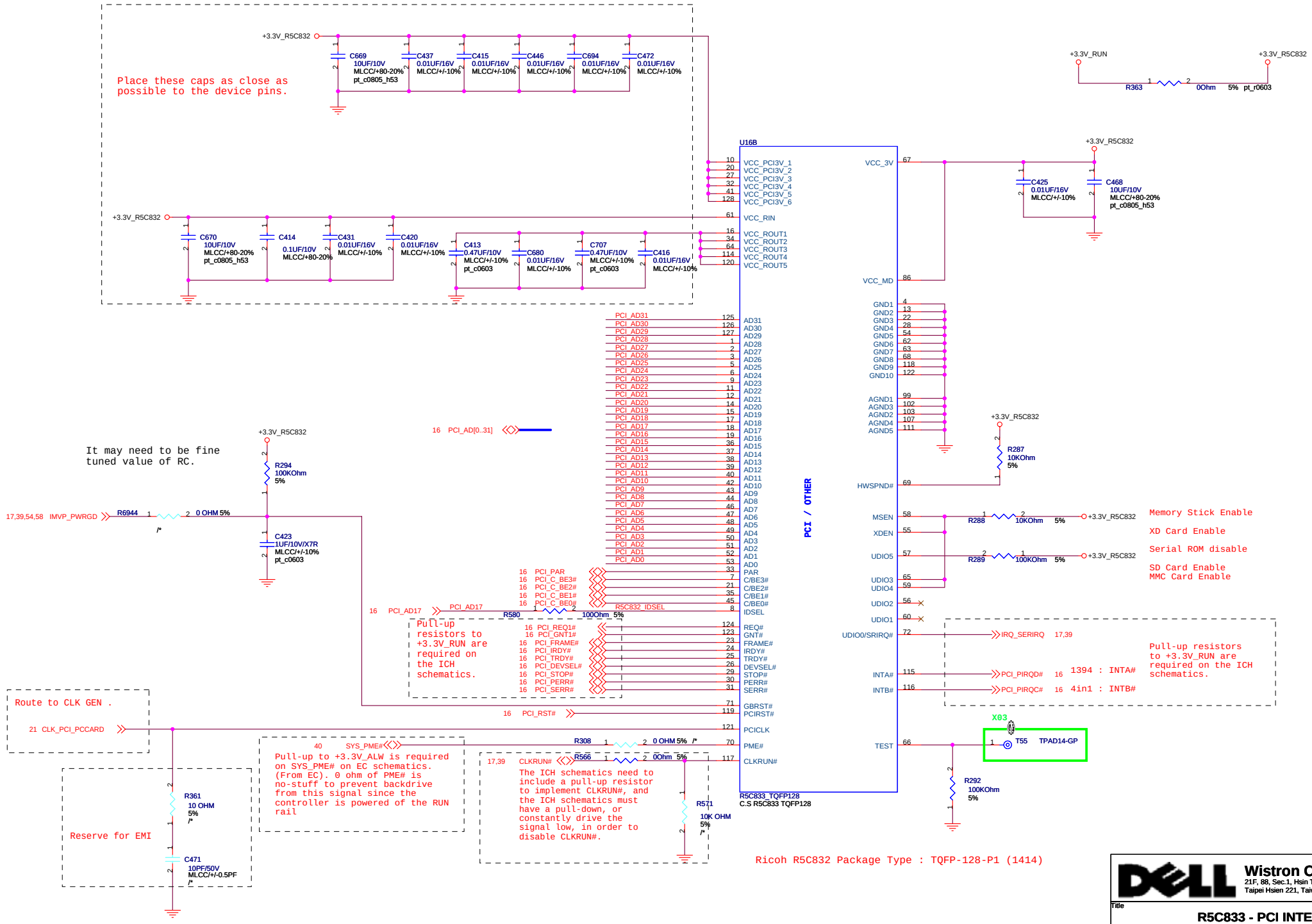

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Title: **R5C833 - PCI INTERFACE**

Size	Document Number	Rev
Custom	Diaz-UMA	A00

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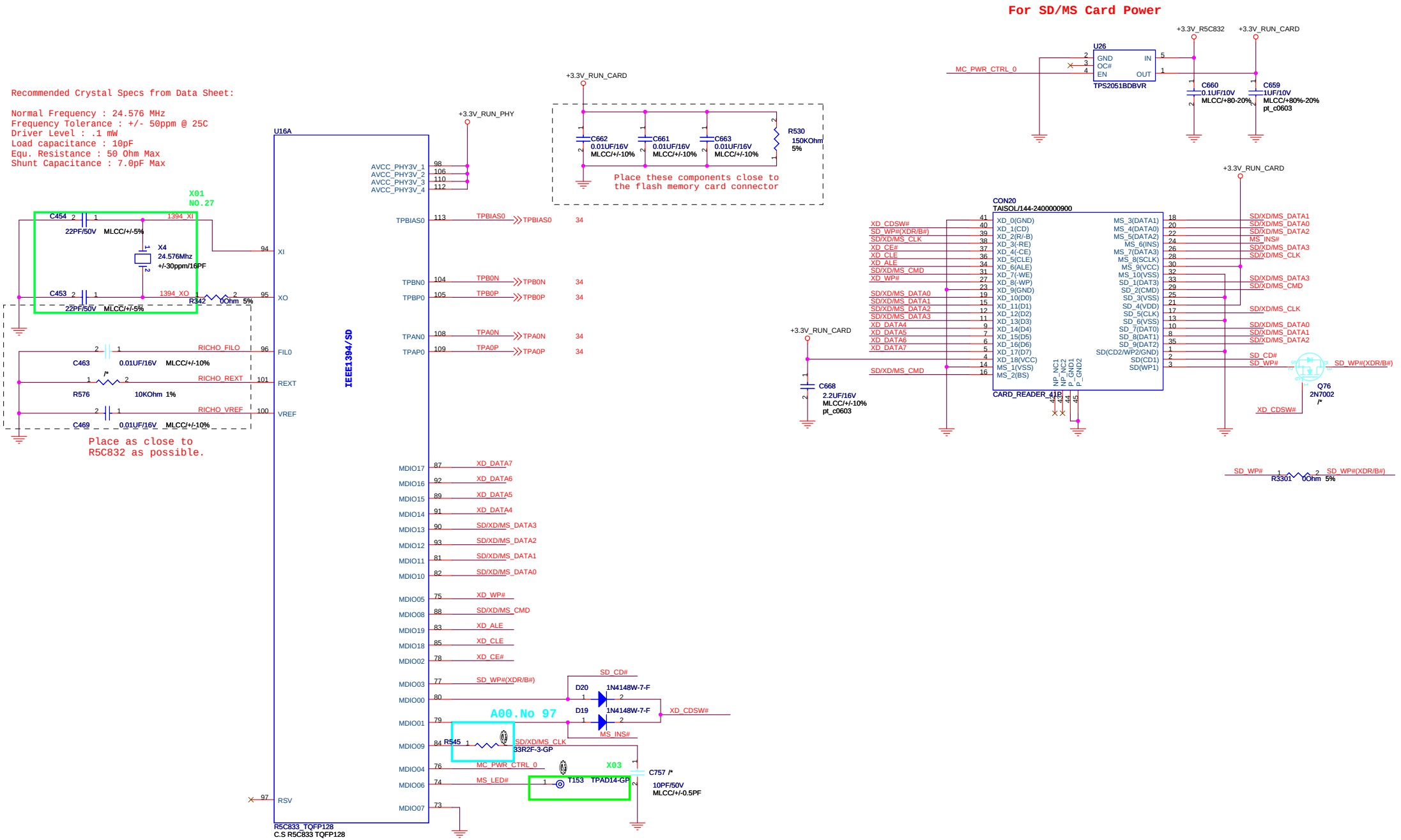

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Title: R5C833 - FLASH MEMORY PART

Size: Custom | Document Number: Diaz-UMA | Rev: A00

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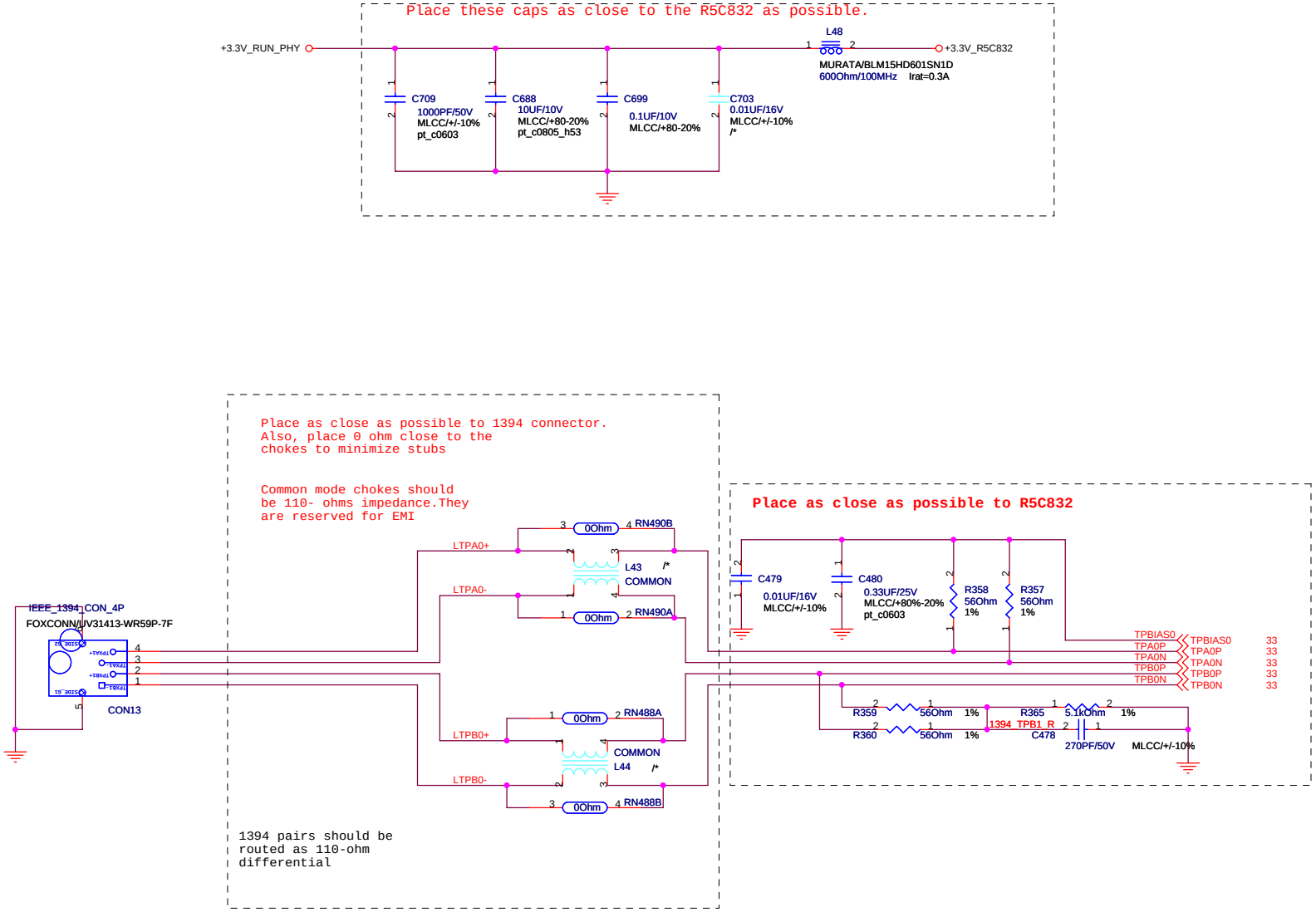

(20071005)for choke & 0ohm colayout

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Title: **R5C833 - IEEE1394 PART**

Size: A3 | Document Number: **Diaz-UMA** | Rev: **A00**

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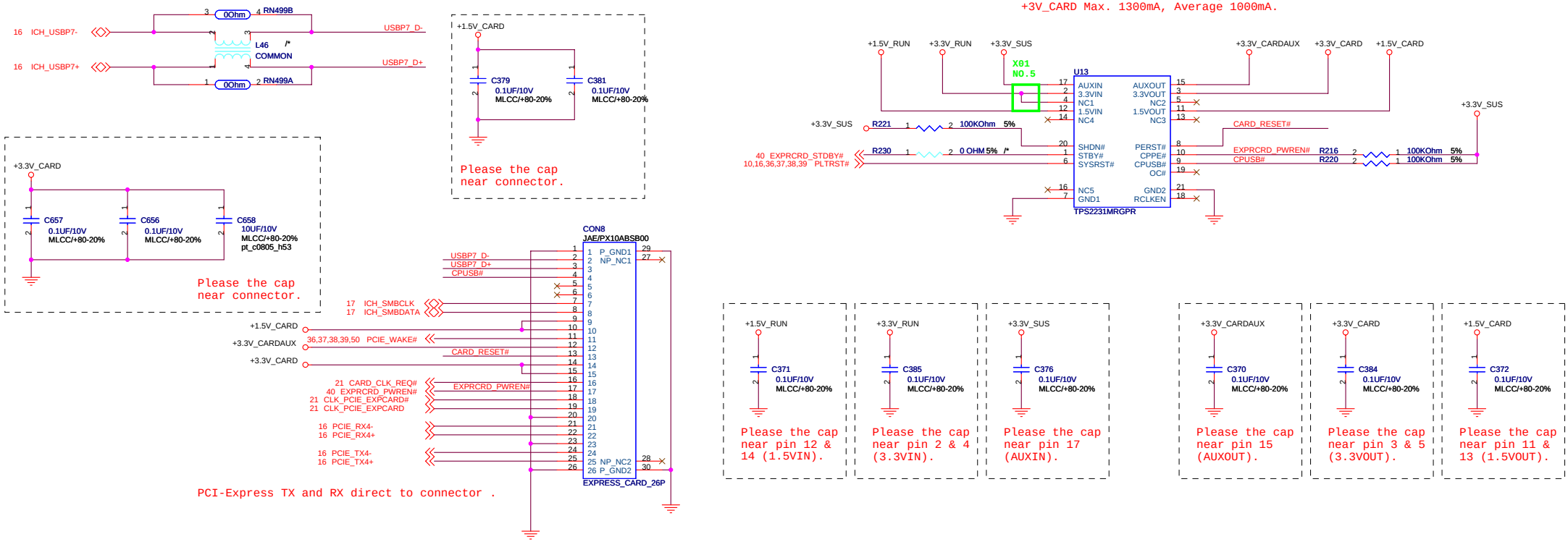
Express Card



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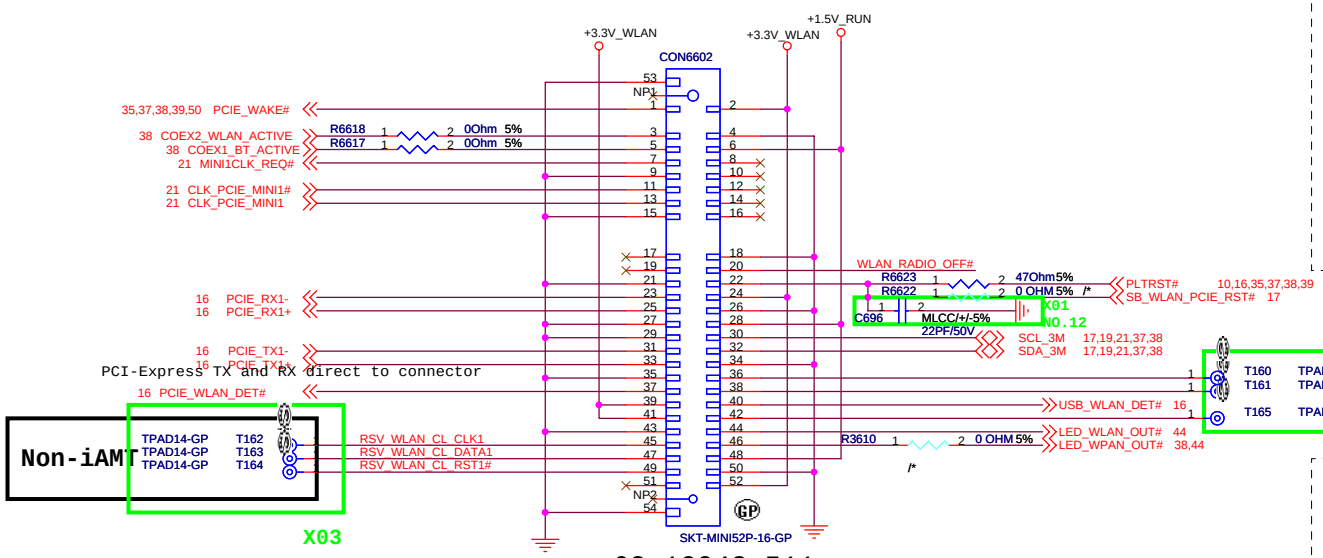
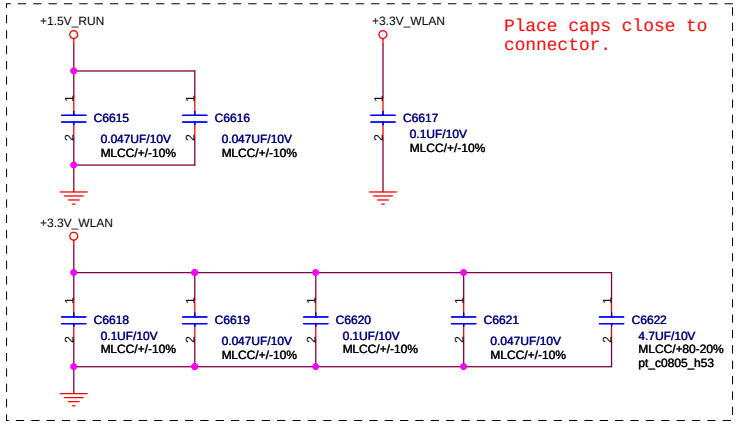
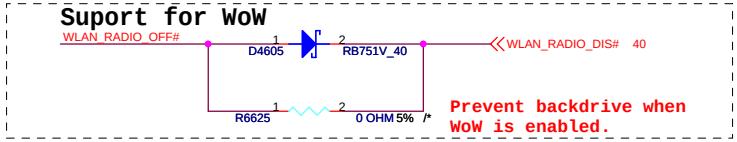
Title		
PCI-Express Card		
Size: Custom	Document Number: Diaz-UMA	Rev: A00
Date: Tuesday, August 19, 2008	Sheet 35 of 68	

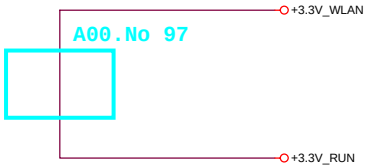


DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81







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Title: MINI CARD - Kedron

Size: A3 | Document Number: Diaz-UMA | Rev: A00

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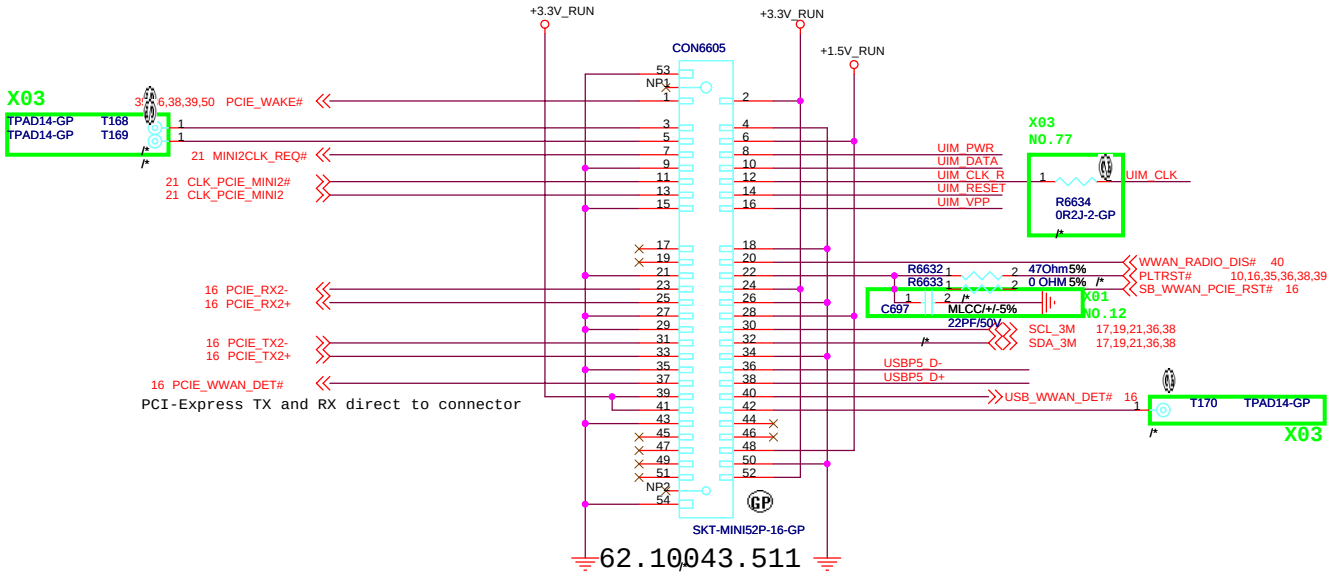
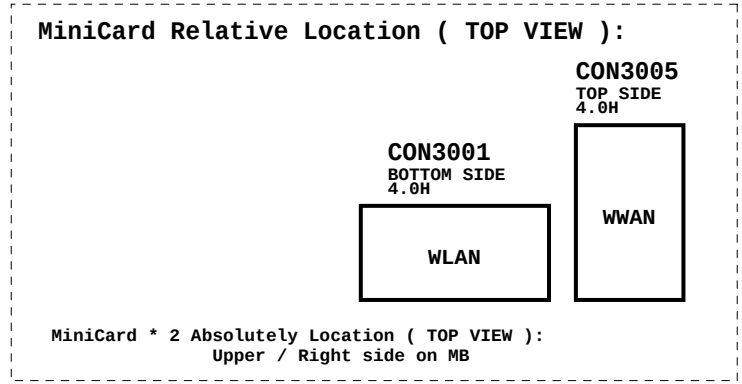
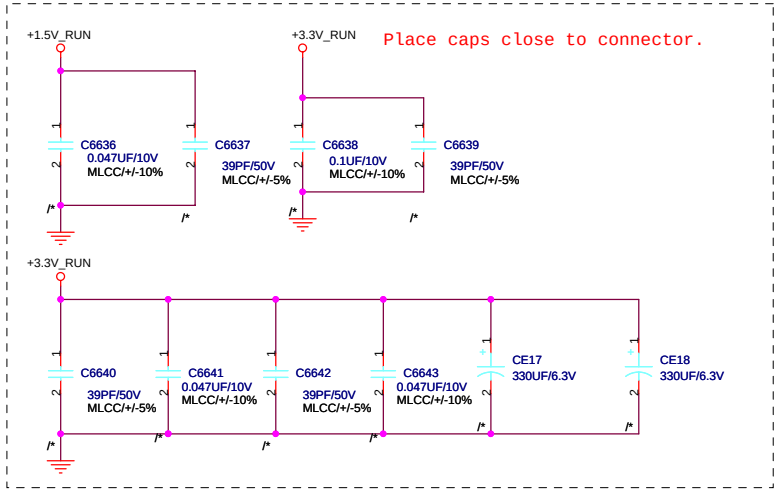
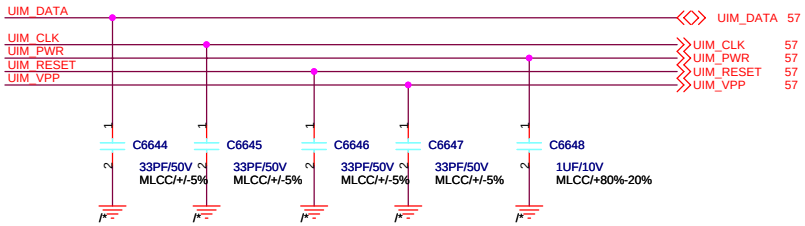
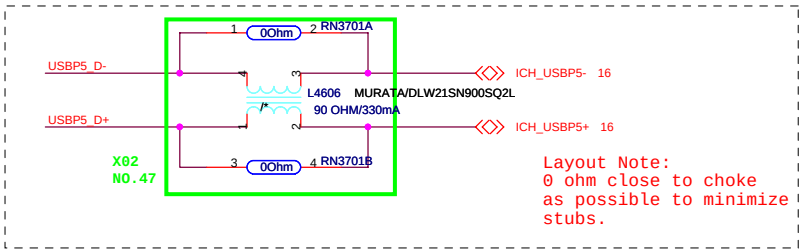
MiniCard WWAN connector











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Title		
MINI CARD - Robson		
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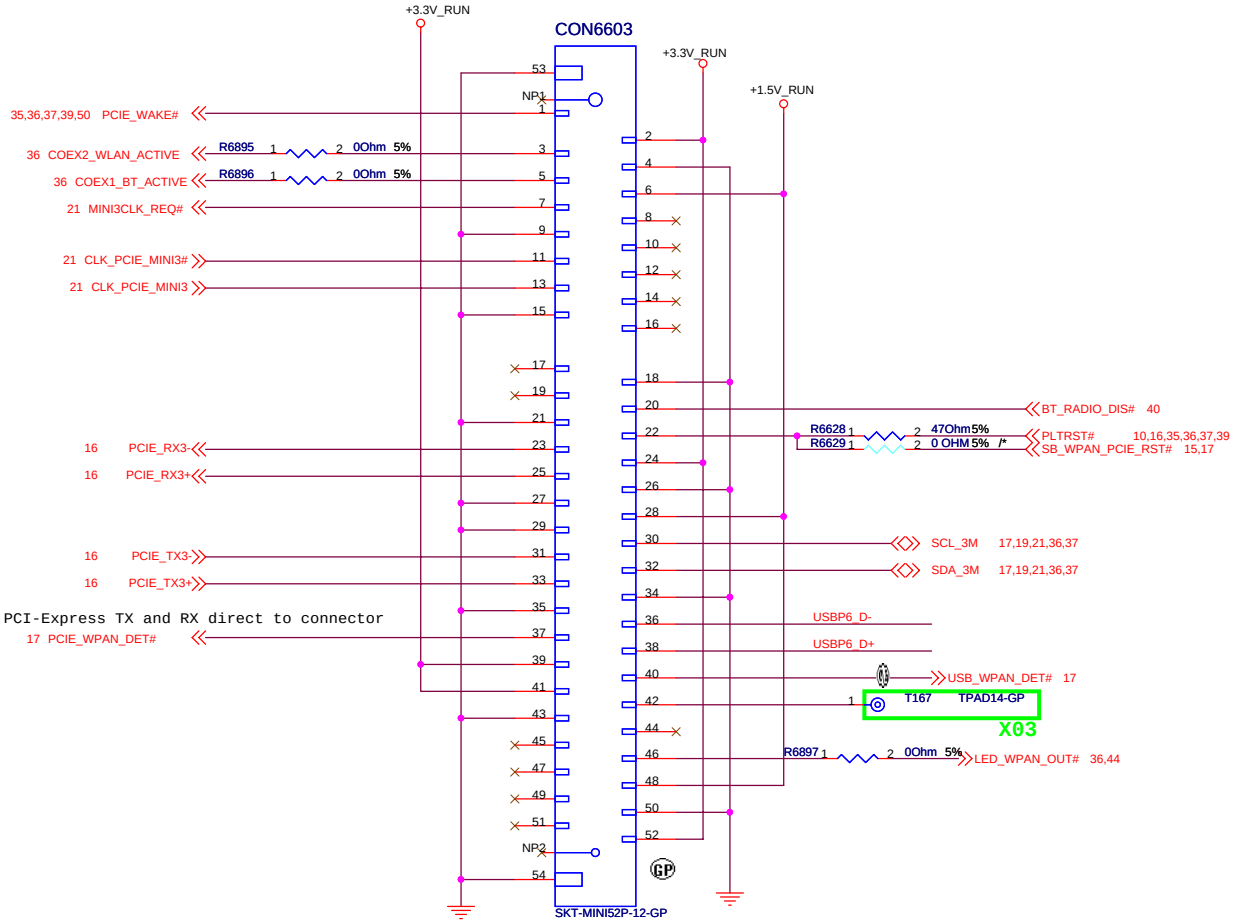
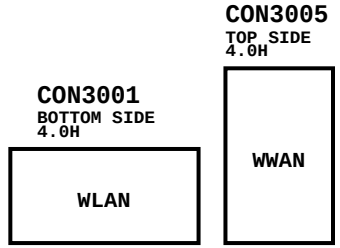
MiniCard WPAN connector

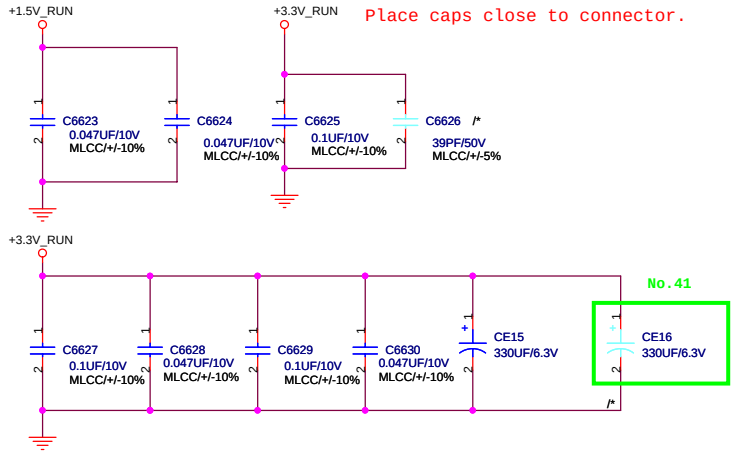


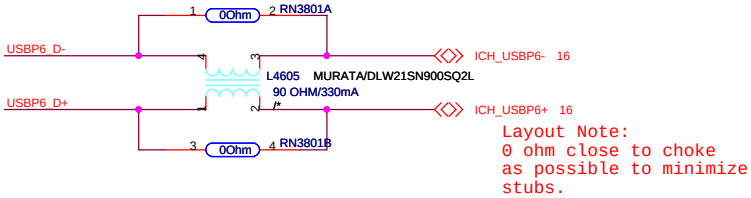
62.10043.441

MiniCard Relative Location (TOP VIEW):



MiniCard * 2 Absolutely Location (TOP VIEW):
Upper / Right side on MB





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Title		
MINI CARD - Robson		
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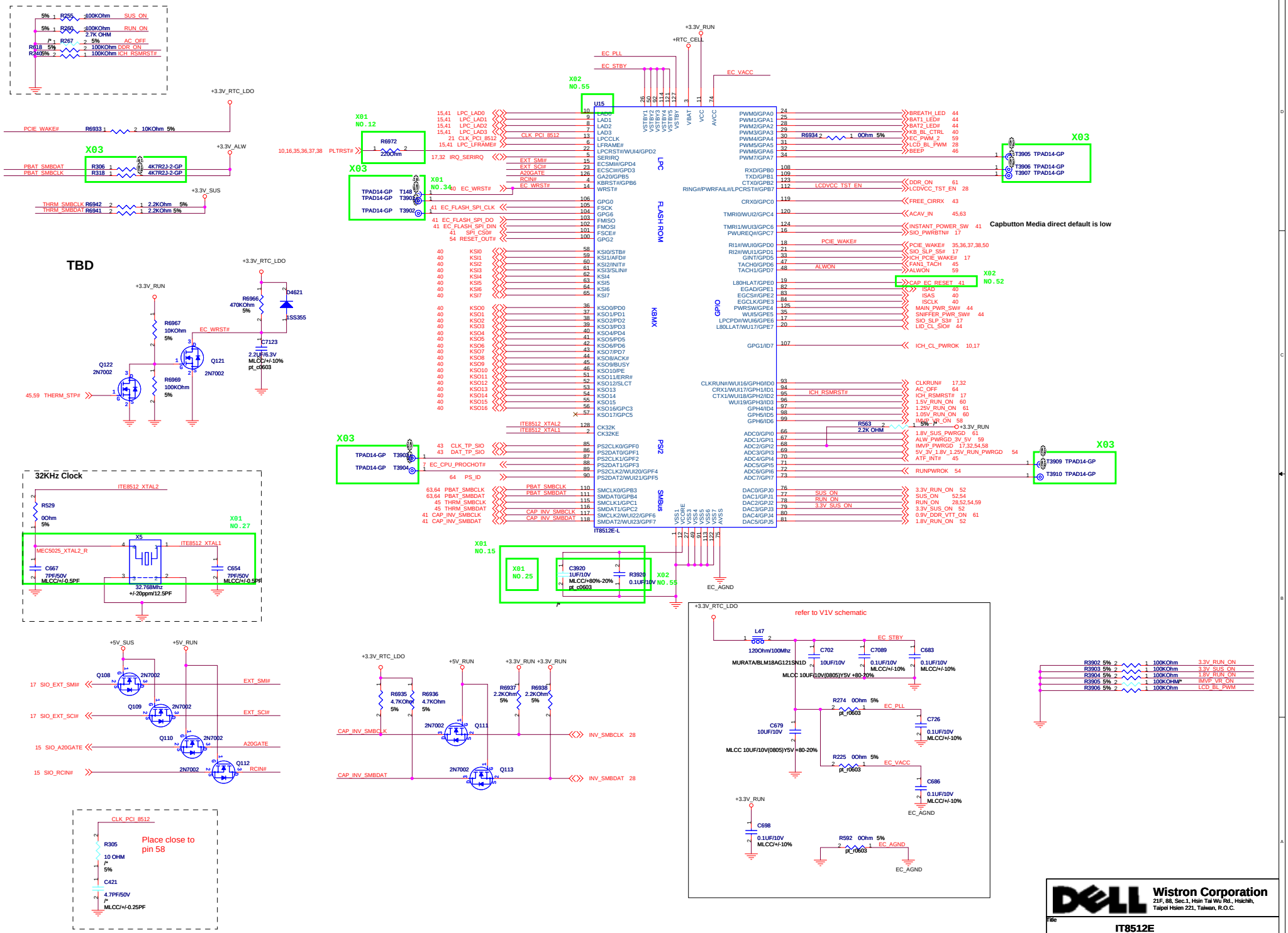
U15
IT8512E-L
LPC
FLASH ROM
KBMX
PS/2
SMBus
GPIO
X01 NO.12
X01 NO.34
X02 NO.55
X02 NO.52
X03
X01 NO.27
X01 NO.15
X01 NO.25
TBD
32KHz Clock
X5
32.768Mhz
+/-20ppm/12.5PF
Capbutton Media direct default is low
refer to V1V schematic
Place close to pin 58
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Title
IT8512E
Size
Custom
Document Number
Diaz-UMA
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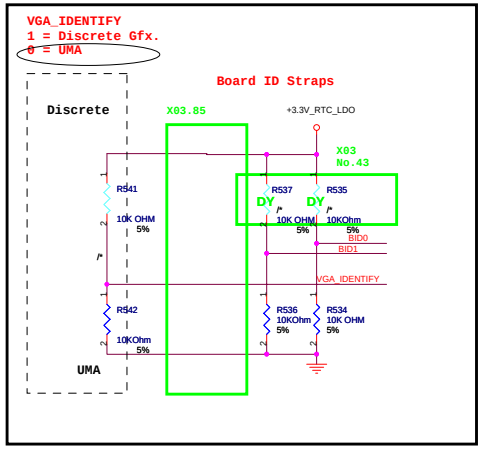
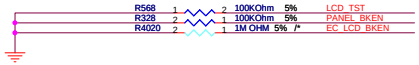
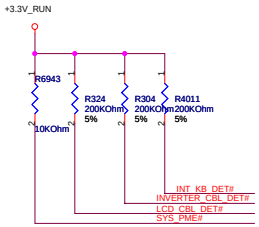
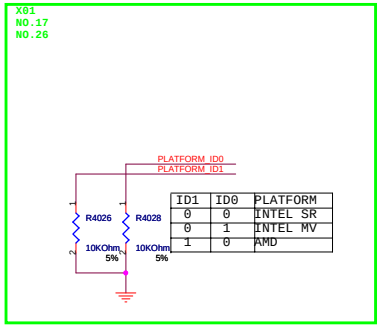


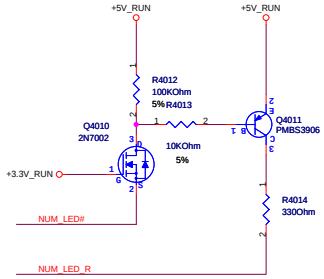
BID1	BID0	M/B VER
0	0	A00
0	1	A01
1	0	A02
1	1	A03

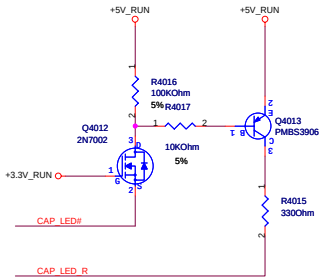


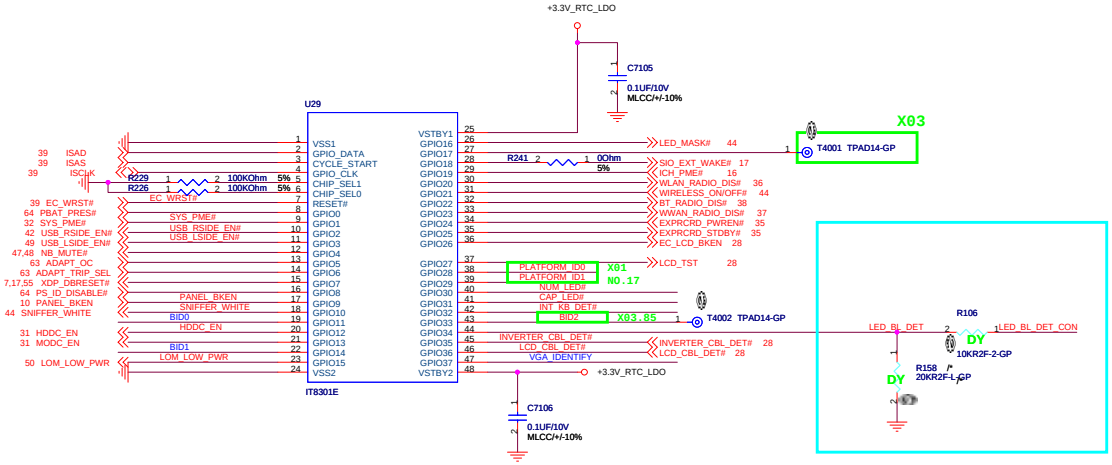




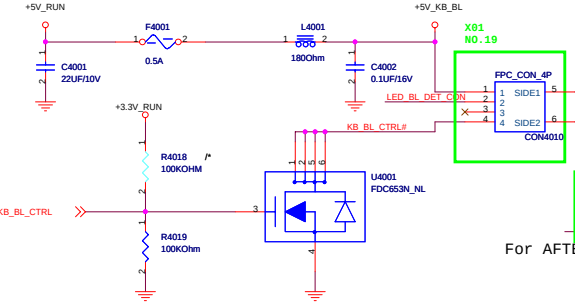
ID1	ID0	PLATFORM
0	0	INTEL SR
0	1	INTEL MV
1	0	AMD

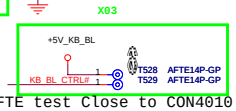






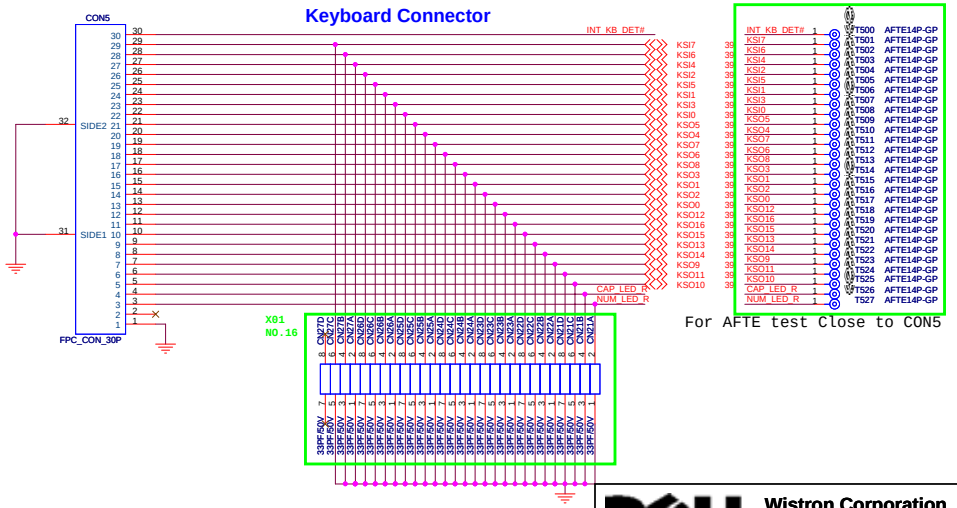
LED Connector





For AFTE test Close to CON4010

Keyboard Connector



For AFTE test Close to CON5

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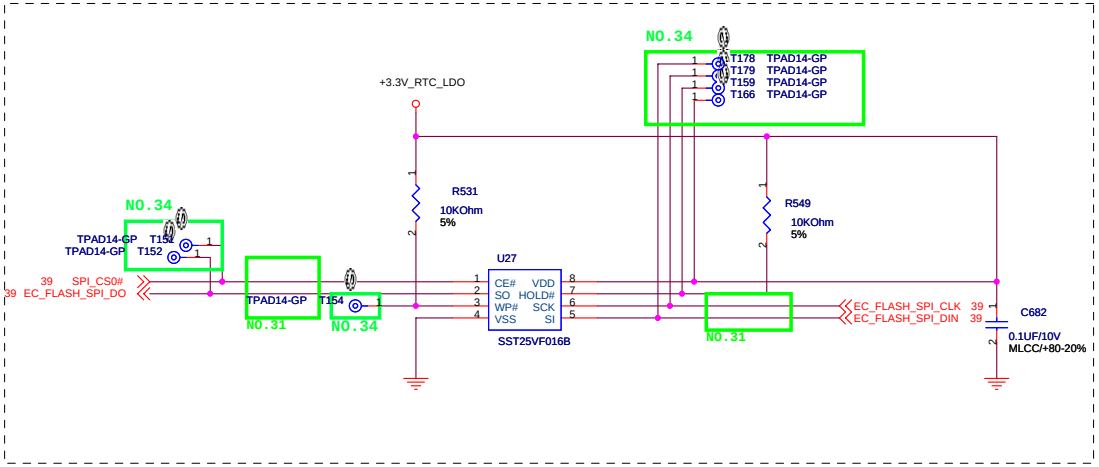
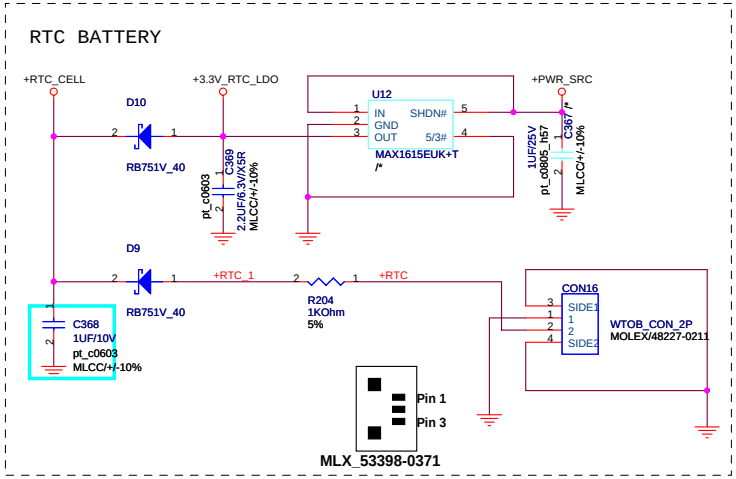
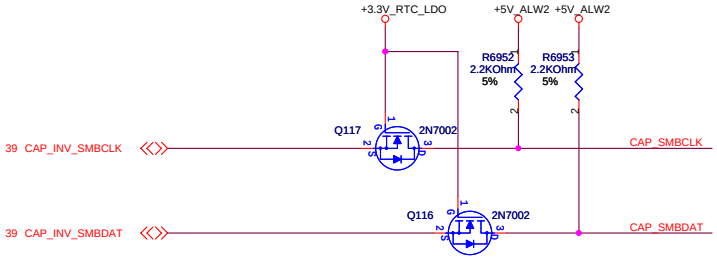
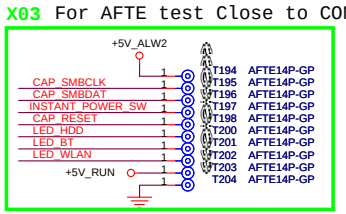
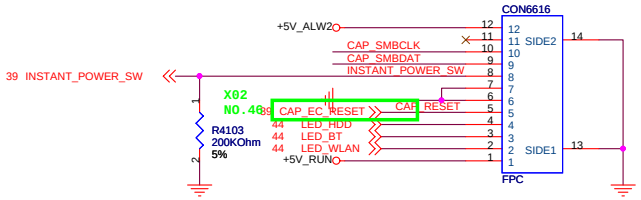


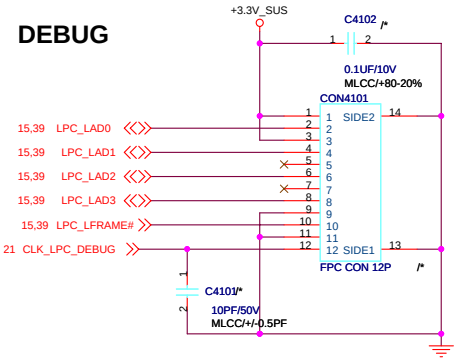








CAPBTN CON.



Note:
+5V_ALW2 => for Capbutton PSOC and Media direct LED only.
+5V_RUN => for Capbutton LED and Photo sensor.

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Title: FLASH & RTC

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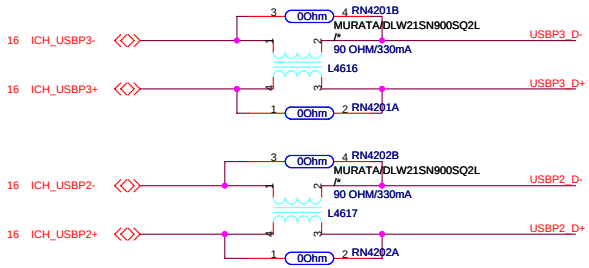
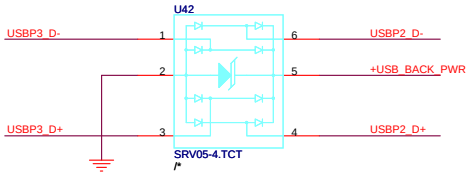
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .

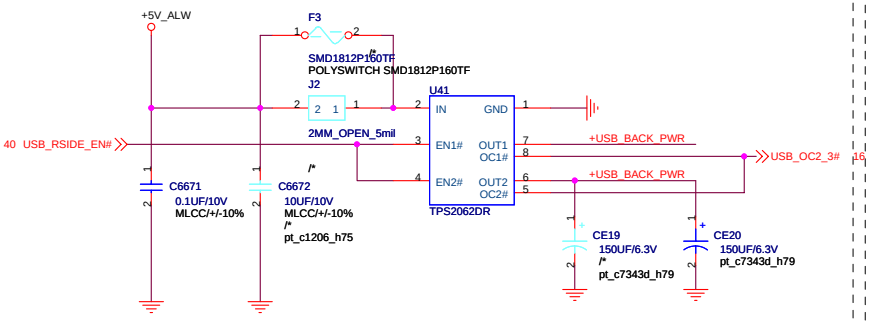


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

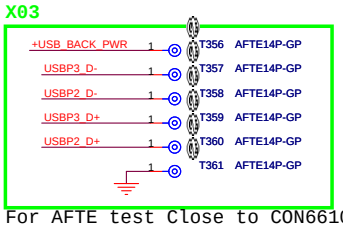


Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C (1pf vs 3pf).

Place one 150uF cap by each USB connector

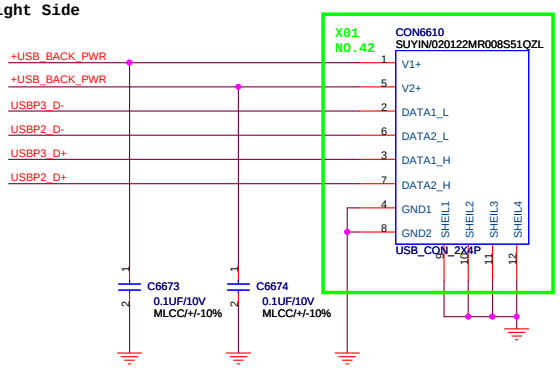


Each channel is 1A



For AFTE test Close to CON6610

Right Side



Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines. Add PADS ONLY until proven diodes are really needed.

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Title		
USB PORT x 2		
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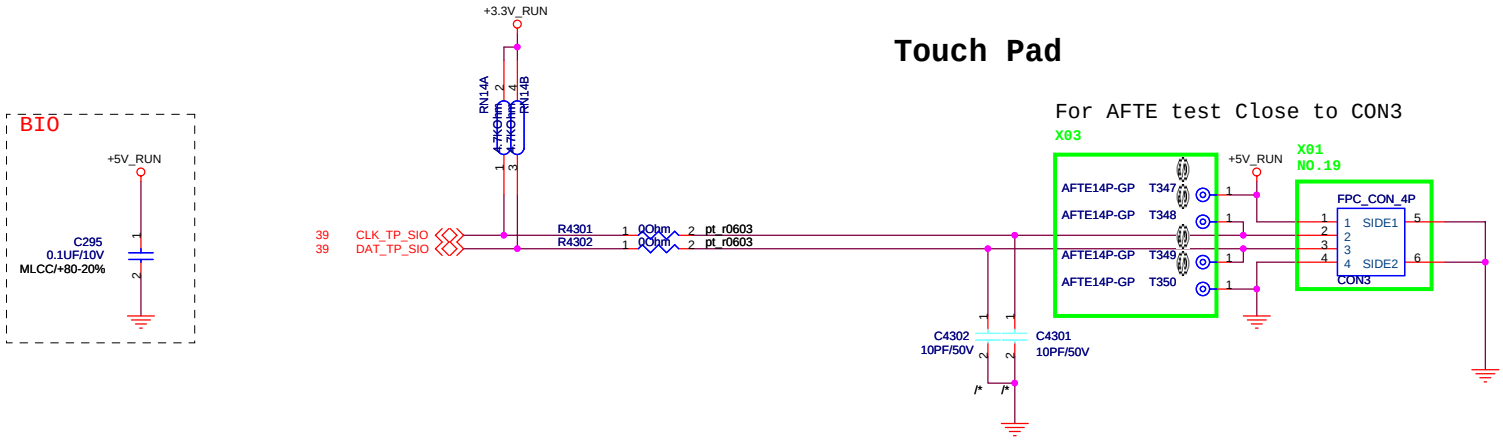
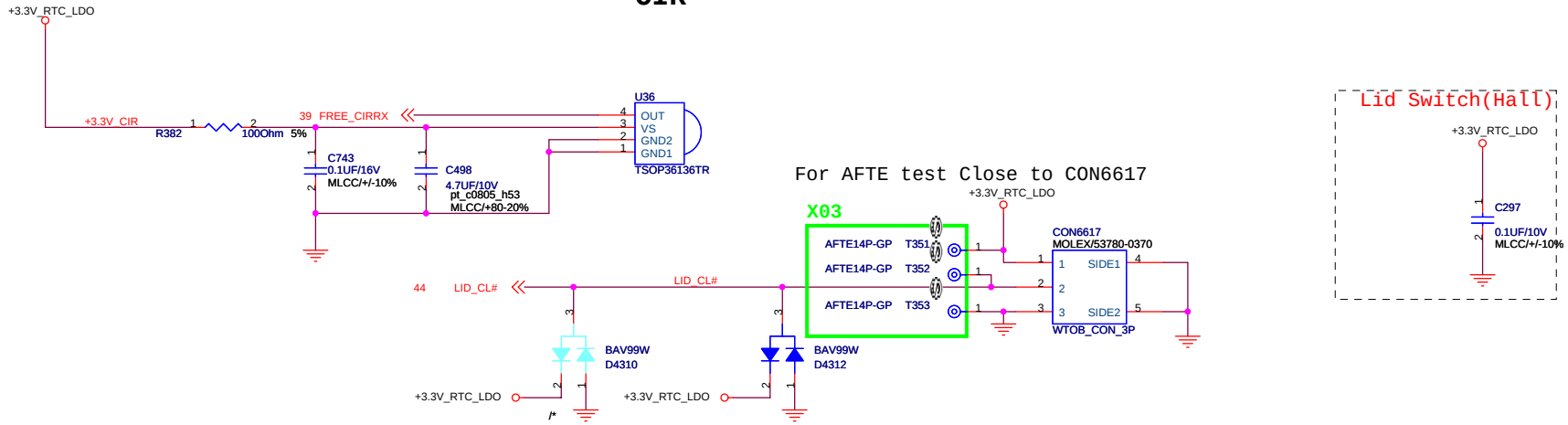
Touch Pad



CIR



HALL SENSOR

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Title	TOUCH PAD & BT & CIR & LID	
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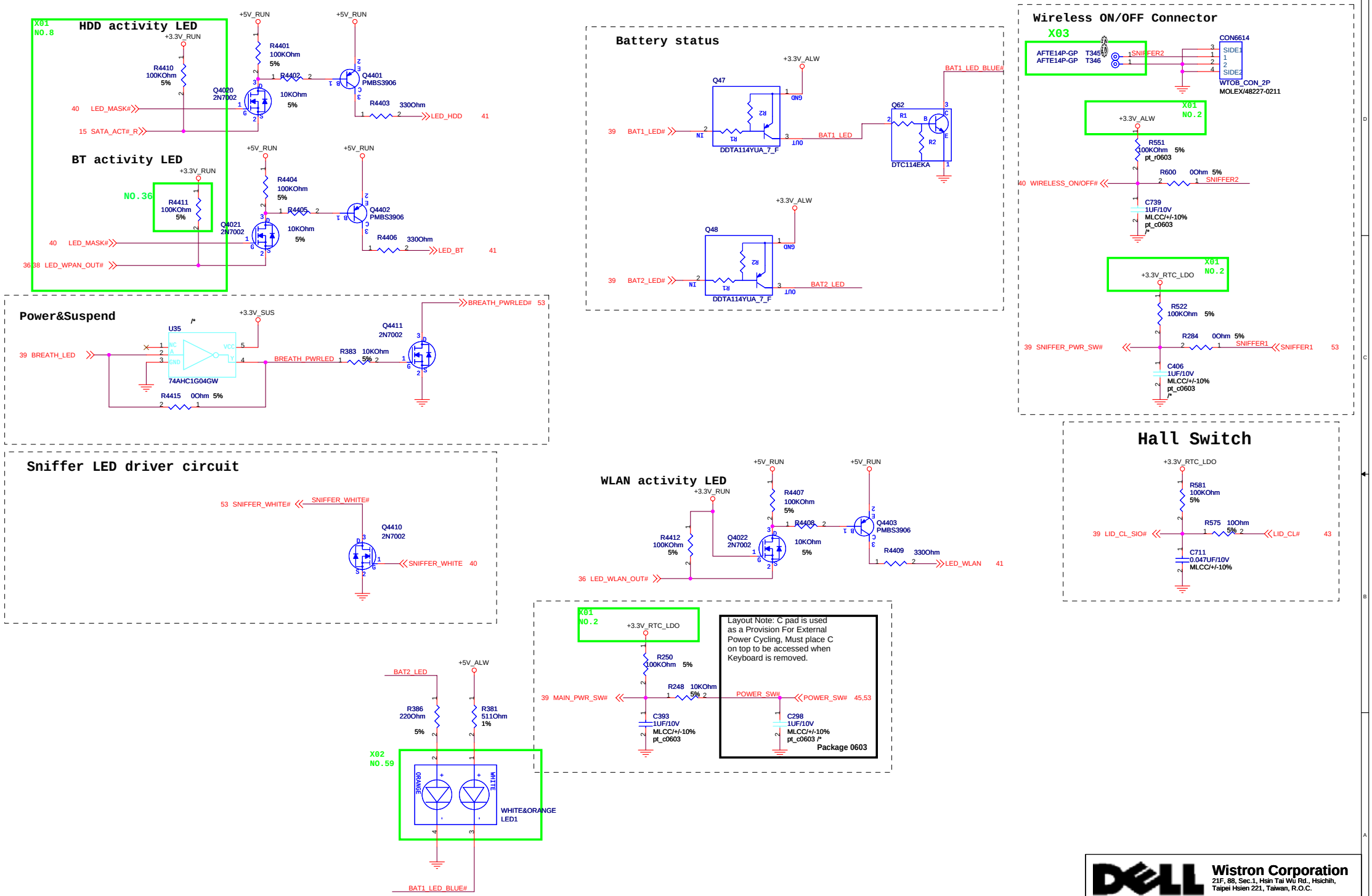

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Title: SWITCH & LED

Size: Custom | Document Number: Diaz-UMA | Rev: A00

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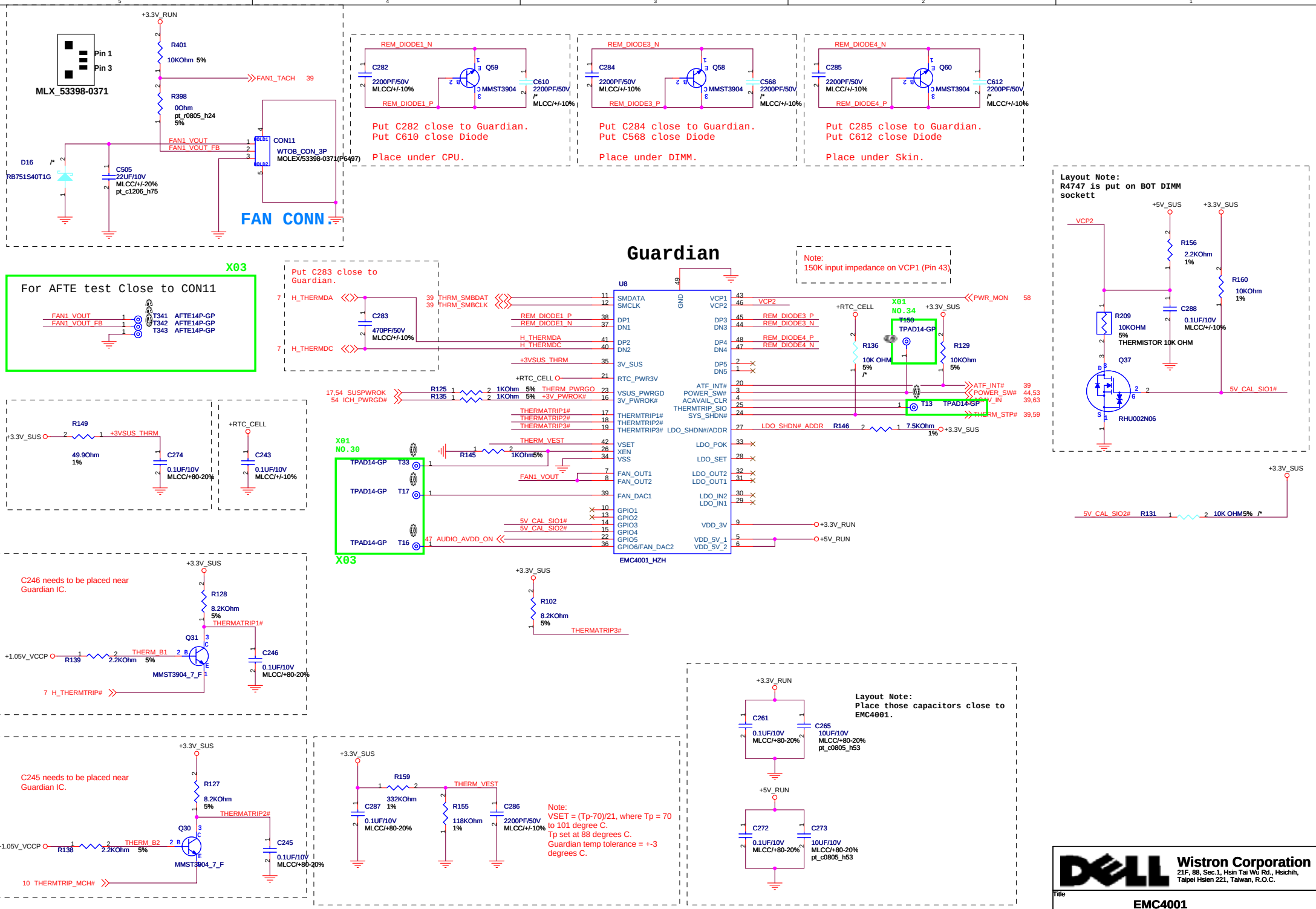

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Title: EMC4001

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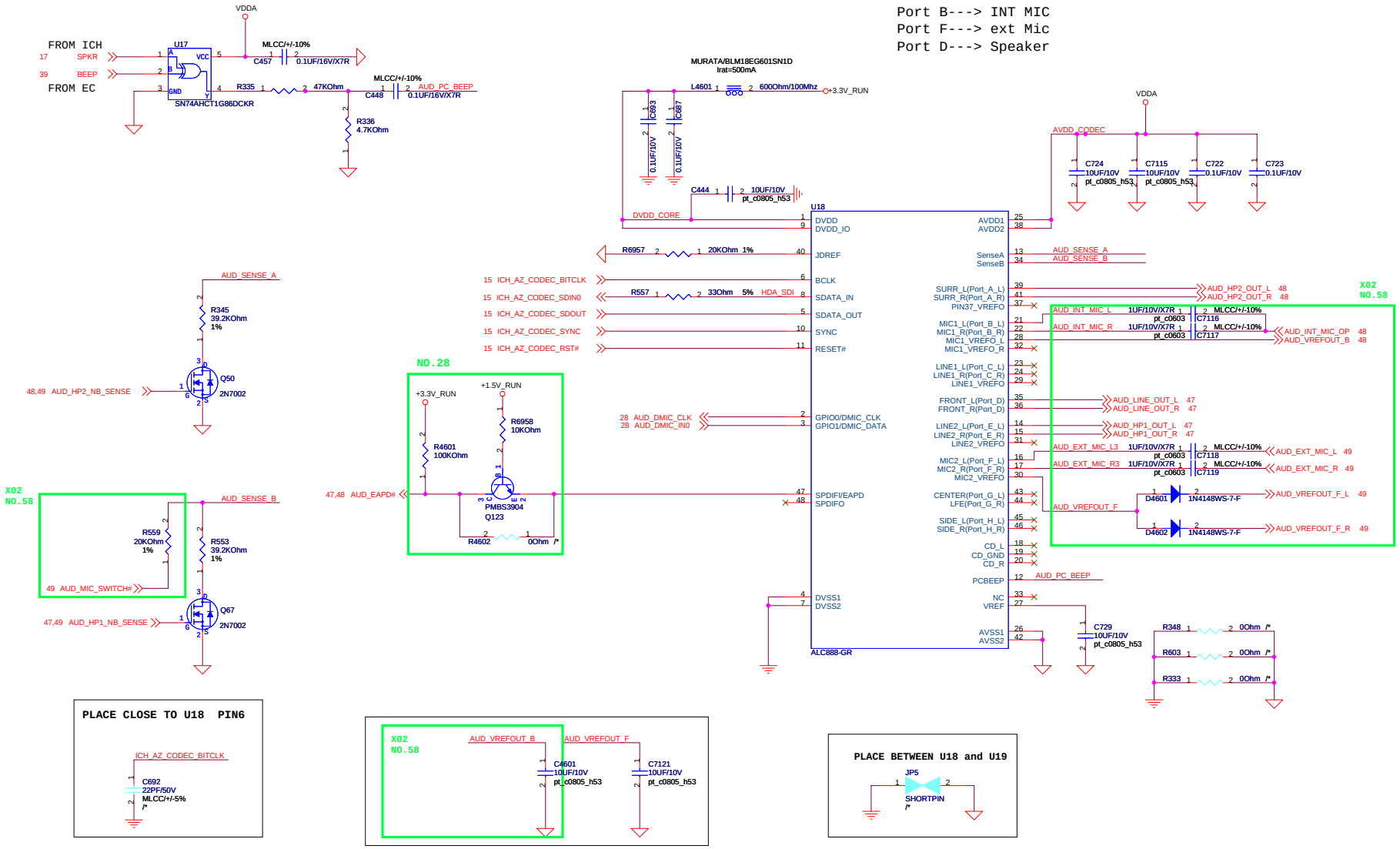
Port A---> HP2
Port E---> HP1
Port B---> INT MIC
Port F---> ext Mic
Port D---> Speaker



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **ALC888**

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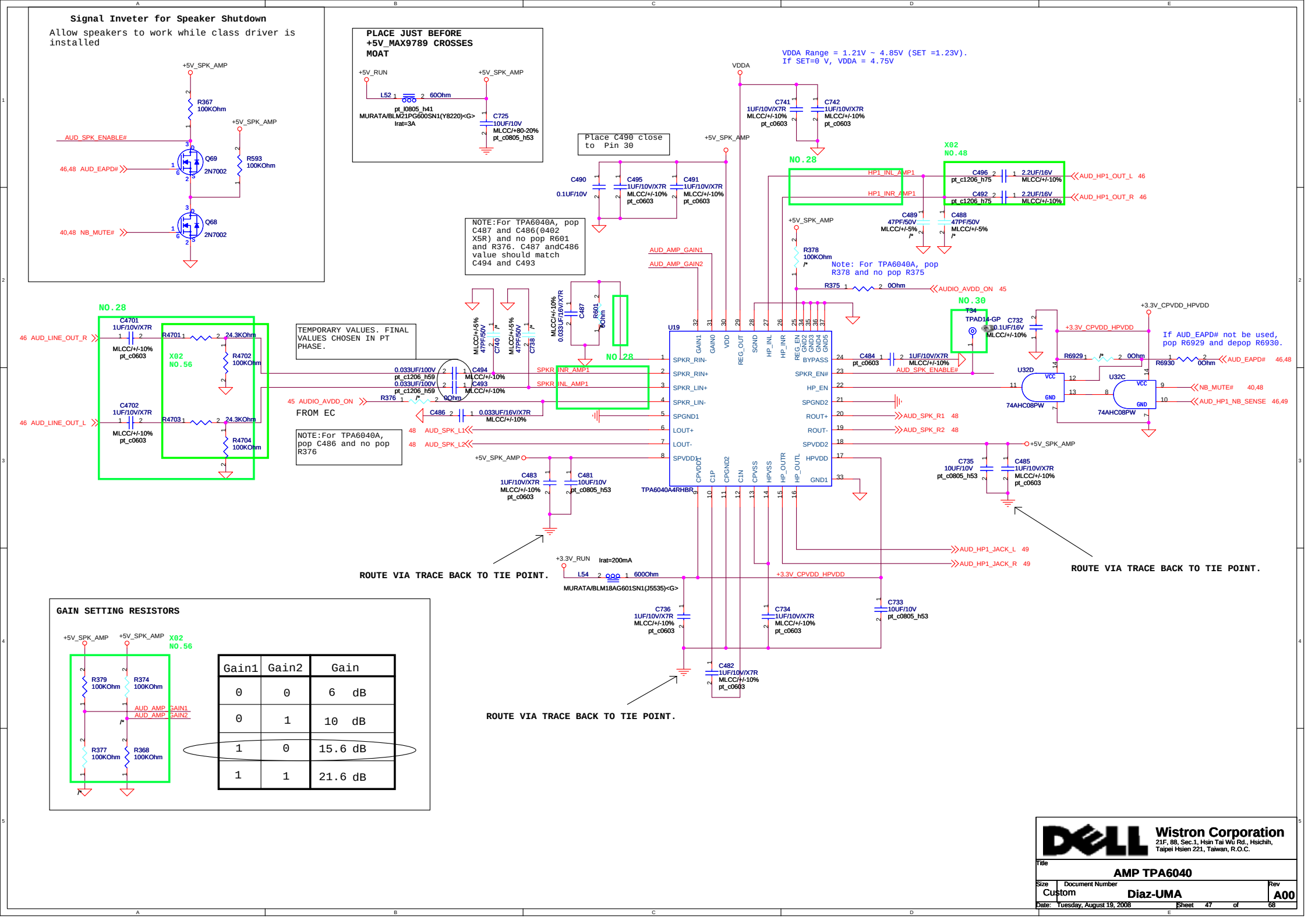
Signal Inveter for Speaker Shutdown
Allow speakers to work while class driver is installed
+5V_SPK_AMP
R367 100KOhm
AUD_SPK_ENABLE#
46,48 AUD_EAPD#
Q69 2N7002
R593 100KOhm
40,48 NB_MUTE#
Q68 2N7002
PLACE JUST BEFORE +5V_MAX9789 CROSSES MOAT
+5V_RUN
L52 60Ohm
pt_l0805_h41
MURATA/BLM21PG600SN1(Y8220)<G>
Irat=3A
C725 10UF/10V MLCC/+80-20% pt_c0805_h53
VDDA Range = 1.21V ~ 4.85V (SET =1.23V).
If SET=0 V, VDDA = 4.75V
VDDA
C741 1UF/10V/X7R MLCC/+/-10% pt_c0603
C742 1UF/10V/X7R MLCC/+/-10% pt_c0603
Place C490 close to Pin 30
C490 0.1UF/10V
C495 1UF/10V/X7R MLCC/+/-10% pt_c0603
C491 1UF/10V/X7R MLCC/+/-10% pt_c0603
NO.28
X02 NO.48
HP1_INL_AMP1
HP1_INR_AMP1
C496 pt_c1206_h75 2.2UF/16V MLCC/+/-10%
C492 pt_c1206_h75 2.2UF/16V MLCC/+/-10%
AUD_HP1_OUT_L 46
AUD_HP1_OUT_R 46
C489 47PF/50V MLCC/+/-5% /*
C488 47PF/50V MLCC/+/-5% /*
NOTE:For TPA6040A, pop C487 and C486(0402 X5R) and no pop R601 and R376. C487 andC486 value should match C494 and C493
AUD_AMP_GAIN1
AUD_AMP_GAIN2
R378 100KOhm /*
Note: For TPA6040A, pop R378 and no pop R375
R375 0Ohm
AUDIO_AVDD_ON 45
NO.30
T34 TPAD14-GP
C732 0.1UF/16V MLCC/+/-10%
+3.3V_CPVDD_HPVDD
If AUD_EAPD# not be used, pop R6929 and depop R6930.
R6929 0Ohm
R6930 0Ohm
AUD_EAPD# 46,48
U32D 74AHC08PW
U32C 74AHC08PW
NB_MUTE# 40,48
AUD_HP1_NB_SENSE 46,49
NO.28
46 AUD_LINE_OUT_R
C4701 1UF/10V/X7R MLCC/+/-10% pt_c0603
R4701 24.3KOhm
X02 NO.56
R4702 100KOhm
46 AUD_LINE_OUT_L
C4702 1UF/10V/X7R MLCC/+/-10% pt_c0603
R4703 24.3KOhm
R4704 100KOhm
TEMPORARY VALUES. FINAL VALUES CHOSEN IN PT PHASE.
MLCC/+/-5% 47PF/50V C740 /*
MLCC/+/-5% 47PF/50V C738 /*
MLCC/+/-10% 0.033UF/16V/X7R C487
R601 0Ohm
NO.28
0.033UF/100V pt_c1206_h59
C494 MLCC/+/-10%
C493 MLCC/+/-10%
SPKR_INR_AMP1
SPKR_INL_AMP1
45 AUDIO_AVDD_ON
R376 0Ohm /*
FROM EC
C486 0.033UF/16V/X7R MLCC/+/-10%
NOTE:For TPA6040A, pop C486 and no pop R376
48 AUD_SPK_L1
48 AUD_SPK_L2
U19
SPKR_RIN-
SPKR_RIN+
SPKR_LIN+
SPKR_LIN-
SPGND1
LOUT+
LOUT-
SPVDD1
GAIN1 GAIN0 VDD REG_OUT SGND HP_INL HP_INR REG_EN GND2 GND3 GND4 GND5
BYPASS
SPKR_EN#
HP_EN
SPGND2
ROUT+
ROUT-
SPVDD2
HPVDD
GND1
CPVDD1 C1P CPGND2 C1N CPVSS HPVSS HP_OUTR HP_OUTL
TPA6040A4RHBR
C484 pt_c0603 1UF/10V/X7R MLCC/+/-10%
AUD_SPK_ENABLE#
AUD_SPK_R1 48
AUD_SPK_R2 48
+5V_SPK_AMP
C483 1UF/10V/X7R MLCC/+/-10% pt_c0603
C481 10UF/10V pt_c0805_h53
C735 10UF/10V pt_c0805_h53
C485 1UF/10V/X7R MLCC/+/-10% pt_c0603
AUD_HP1_JACK_L 49
AUD_HP1_JACK_R 49
ROUTE VIA TRACE BACK TO TIE POINT.
ROUTE VIA TRACE BACK TO TIE POINT.
+3.3V_RUN Irat=200mA
L54 600Ohm
MURATA/BLM18AG601SN1(J5535)<G>
+3.3V_CPVDD_HPVDD
C736 1UF/10V/X7R MLCC/+/-10% pt_c0603
C734 1UF/10V/X7R MLCC/+/-10% pt_c0603
C733 10UF/10V pt_c0805_h53
C482 1UF/10V/X7R MLCC/+/-10% pt_c0603
ROUTE VIA TRACE BACK TO TIE POINT.
GAIN SETTING RESISTORS
+5V_SPK_AMP
X02 NO.56
R379 100KOhm
R374 100KOhm
AUD_AMP_GAIN1
AUD_AMP_GAIN2
R377 100KOhm
R368 100KOhm
Gain1 Gain2 Gain
0 0 6 dB
0 1 10 dB
1 0 15.6 dB
1 1 21.6 dB
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Title
AMP TPA6040
Size Custom
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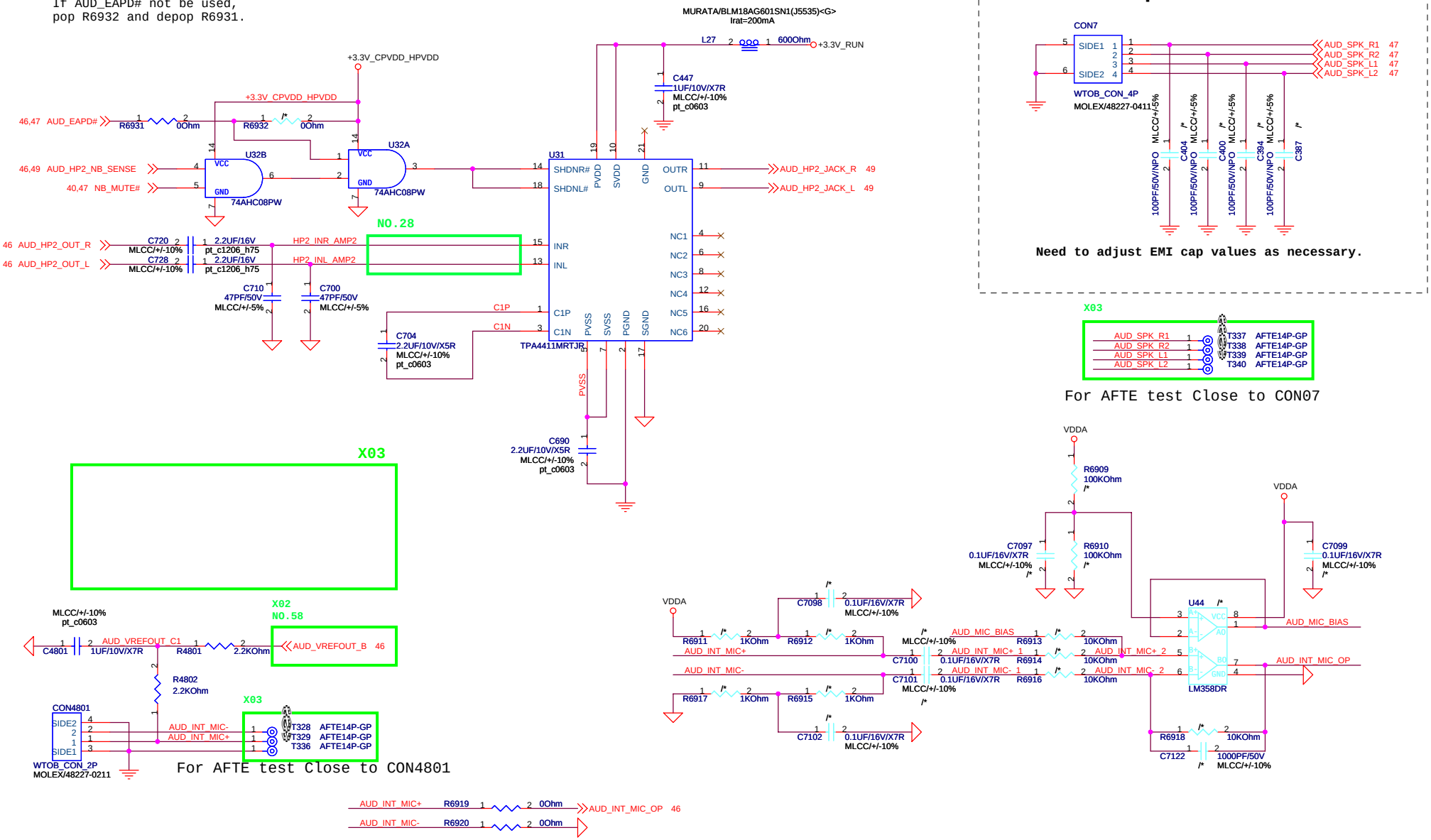
Maxim:1.8V ~ 3.6V
TI:1.8V ~ 4.5V

NOTE: MAKE SURE THERMAL PAD (Pin21)UNDER MAX4411 IS NOT CONNECTED TO GND

If AUD_EAPD# not be used, pop R6932 and depop R6931.



Speaker CON

Need to adjust EMI cap values as necessary.

For AFTE test Close to CON07

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Title	AMP MAX4411 & MIC_AMP	
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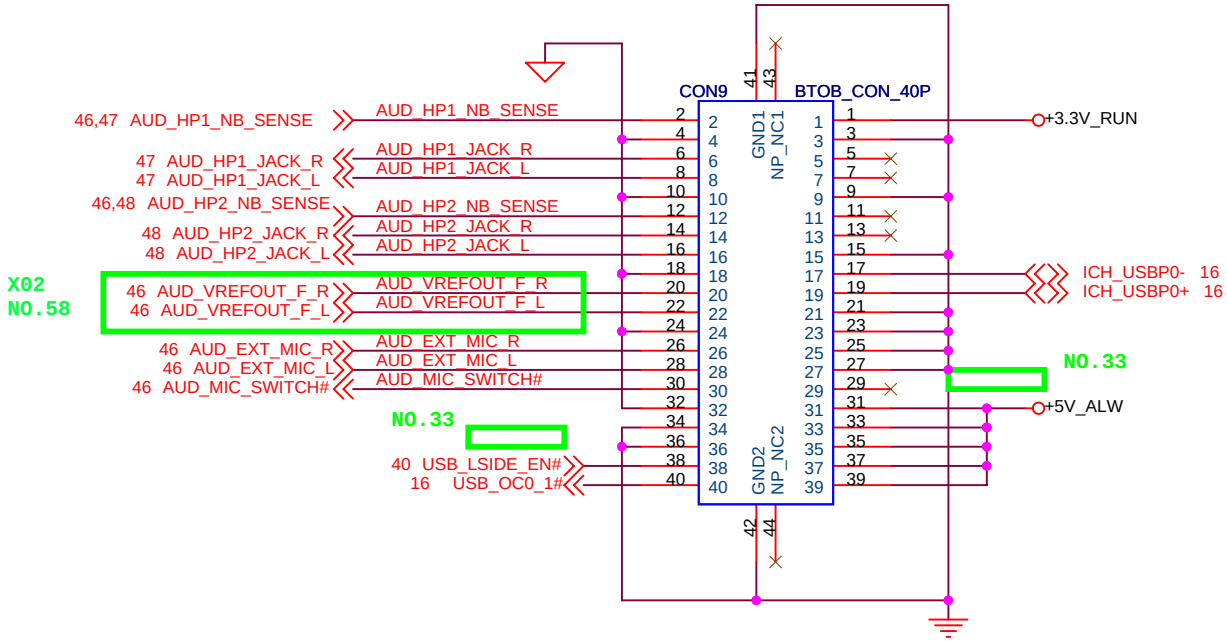

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Title: **AUDIO BtoB CON**

Size	Document Number	Rev
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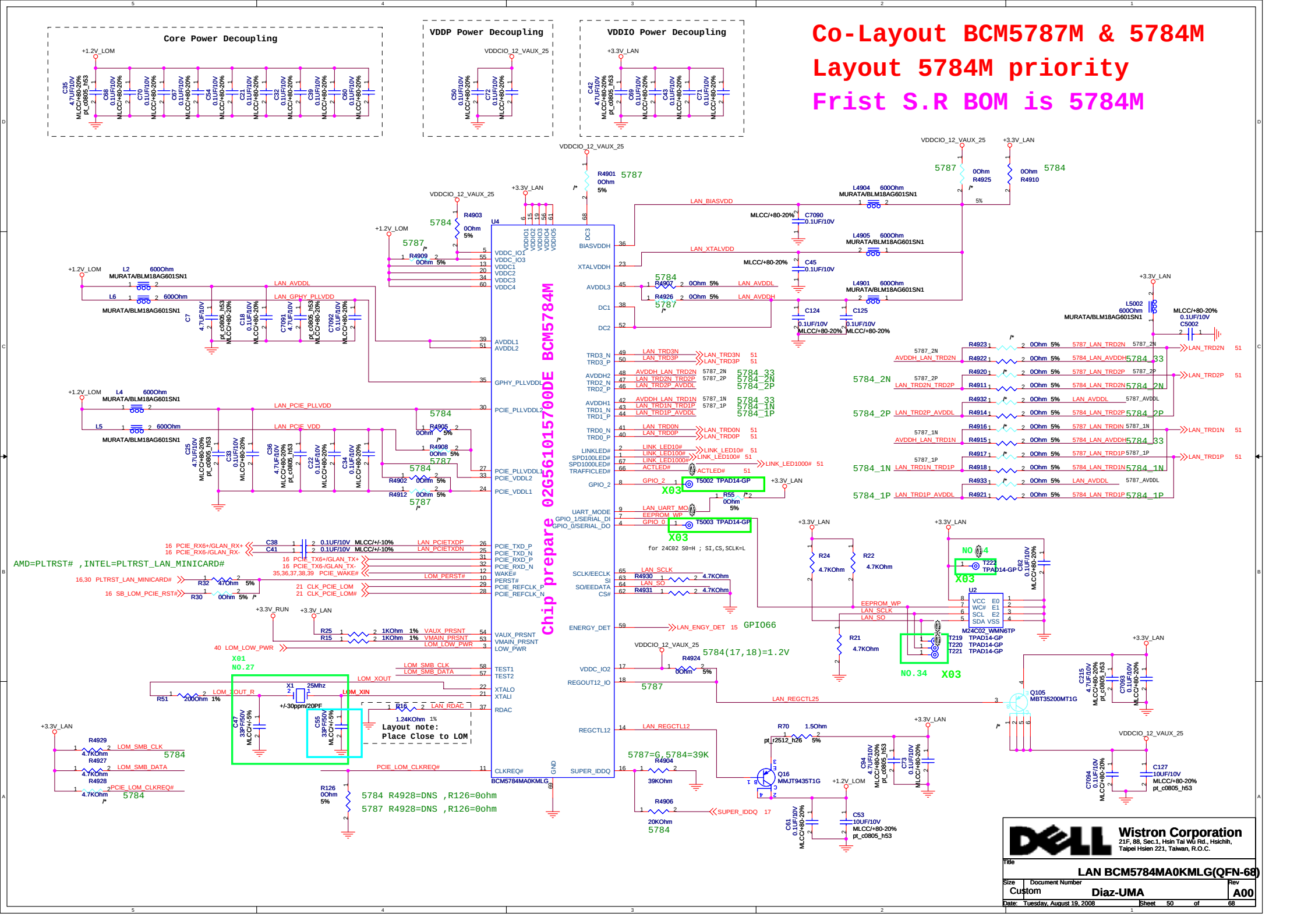
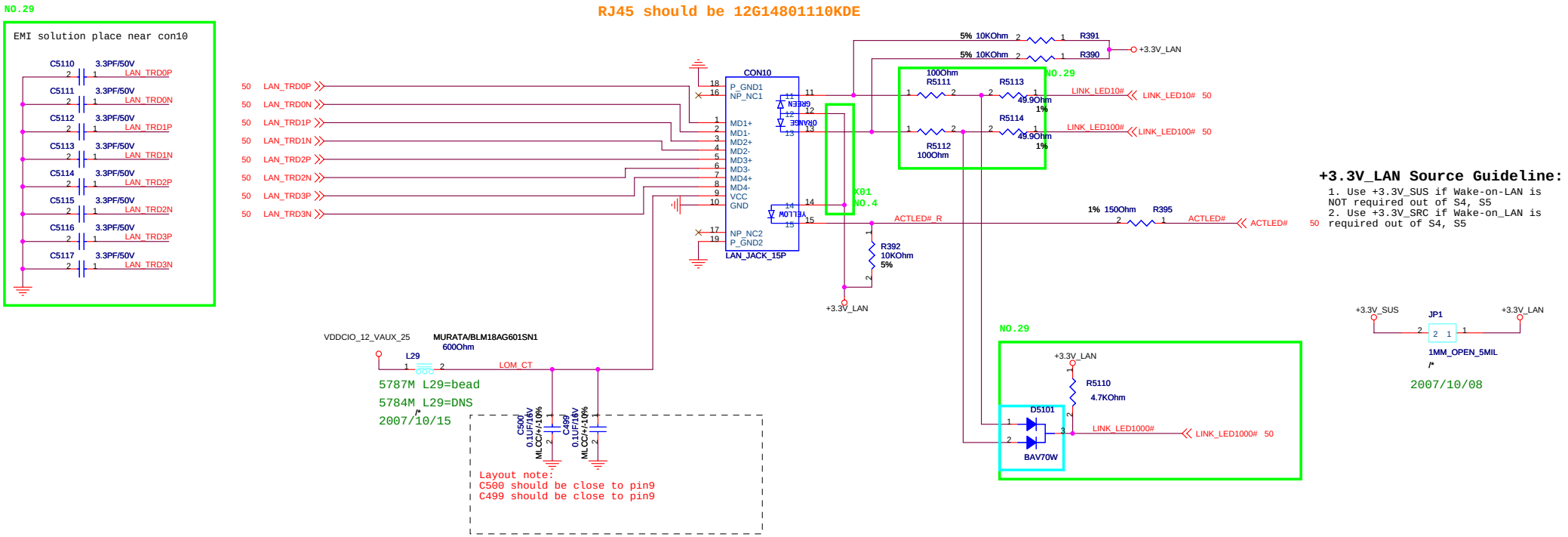
Co-Layout BCM5787M & 5784M
Layout 5784M priority
Frist S.R BOM is 5784M



This BOM is 5784M

require S3 support wake on LAN 2007/10/05

RJ45 should be 12G14801110KDE



+3.3V_LAN Source Guideline:

1. Use +3.3V_SUS if Wake-on-LAN is NOT required out of S4, S5
2. Use +3.3V_SRC if Wake-on_LAN is required out of S4, S5

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Title: Magnetics and RJ-45			
Size: Custom	Document Number: Diaz-UMA		Rev: A00
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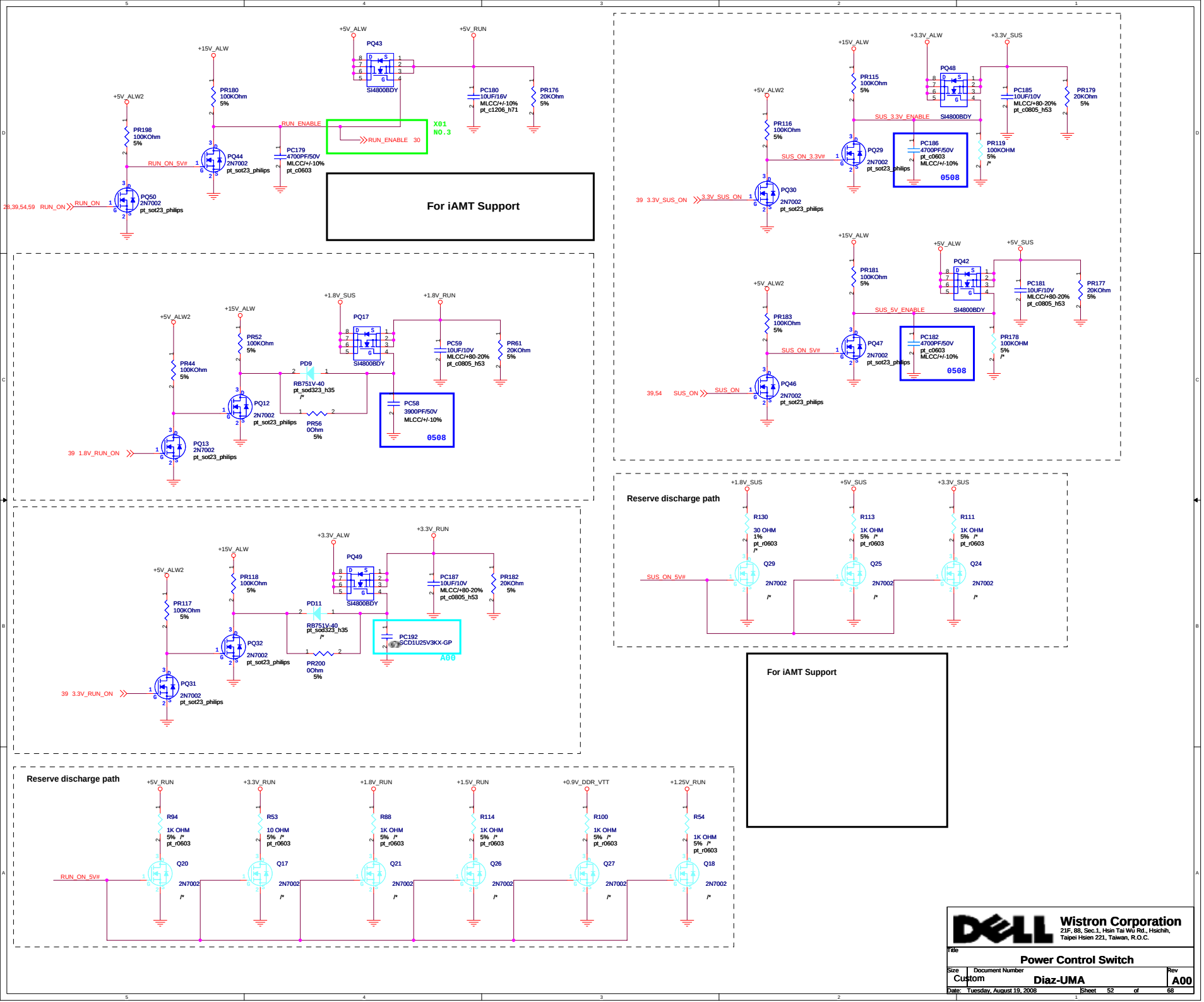

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Title	Power Control Switch	
Size: Custom	Document Number: Diaz-UMA	Rev: A00
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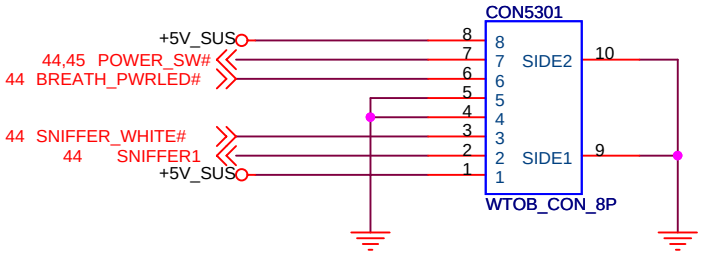

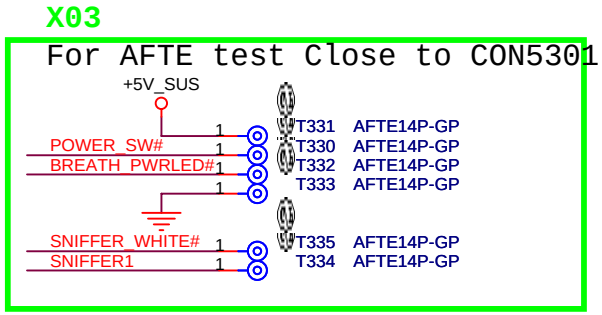

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Buttom Board**

Size	Document Number	Rev
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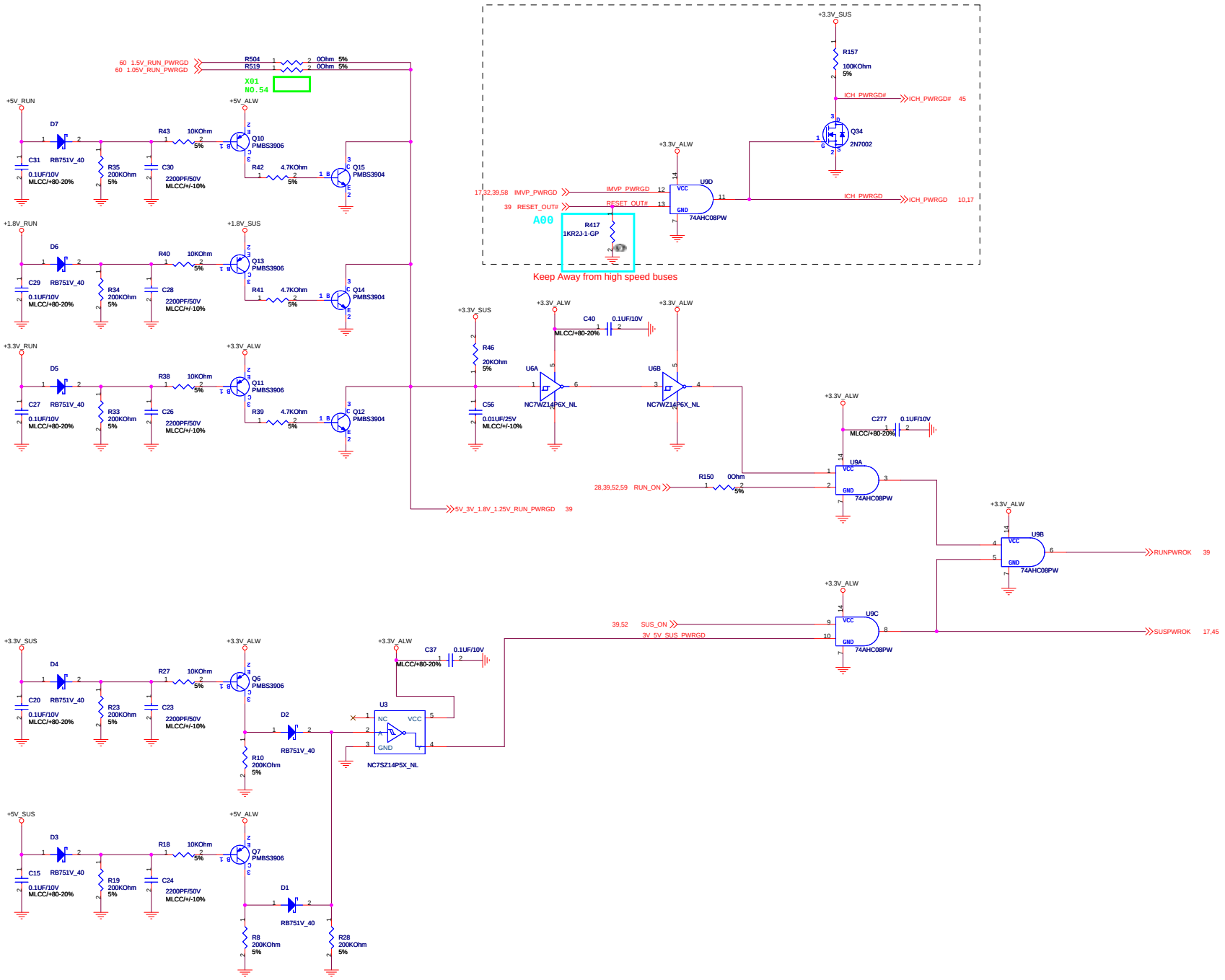

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Title		
Power Sequence Logic		
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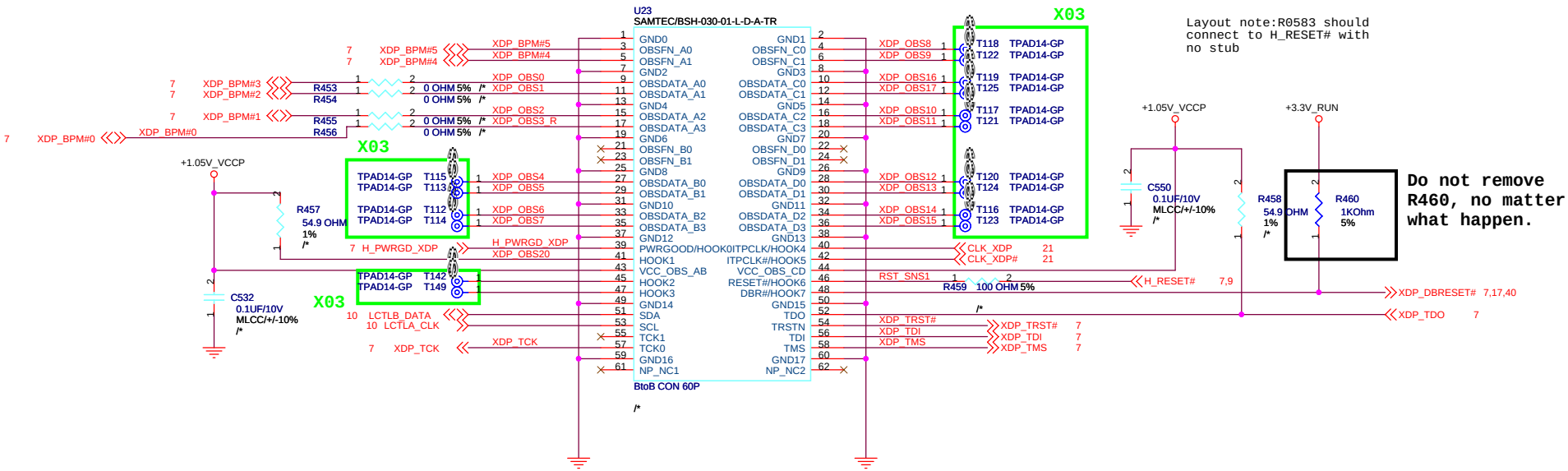
XDP



CAD NOTE:
Place the XDP connector on the primary side of the CRB and place all components near the connector.

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Title		
XDP		
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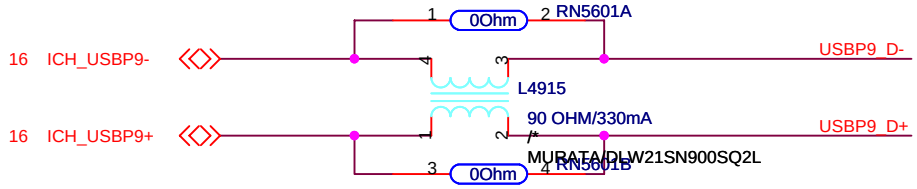
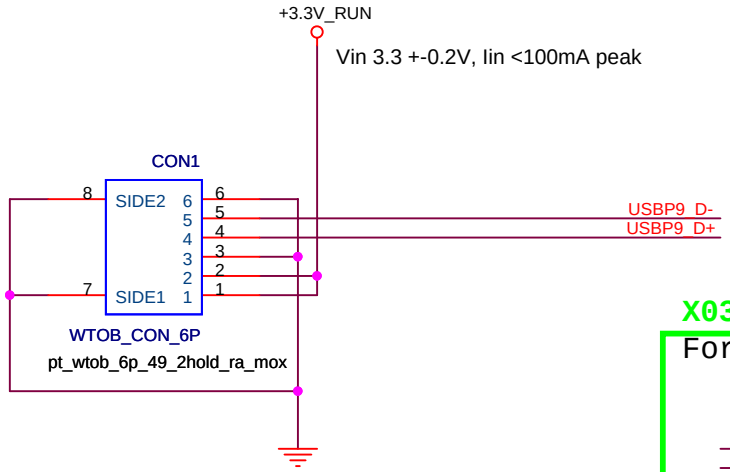
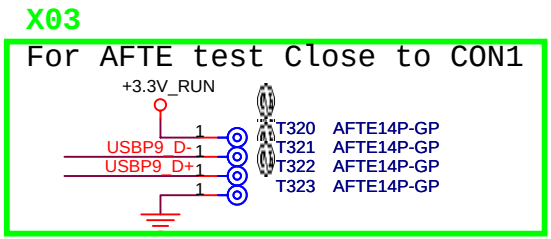
FINGER PRINTER







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Title		
FINGER PRINTER Port		
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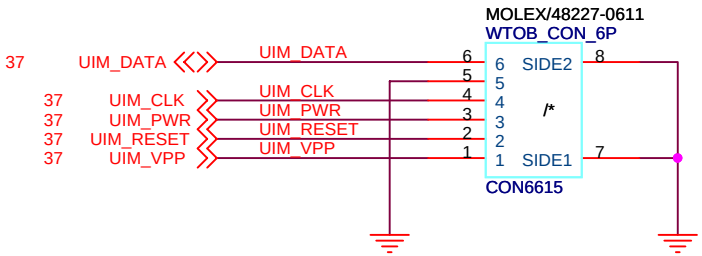
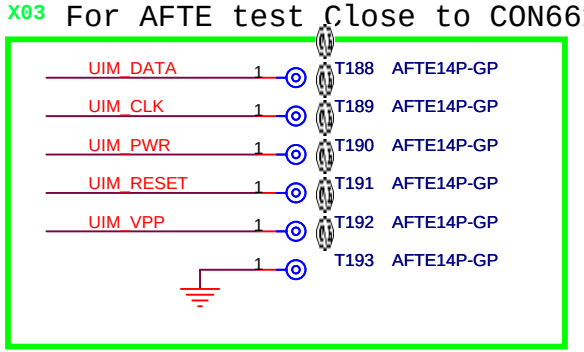


X03 For AFTE test Close to CON6615



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Title: **SIM CARD**

Size	Document Number	Rev
A4	Diaz-UMA	A00

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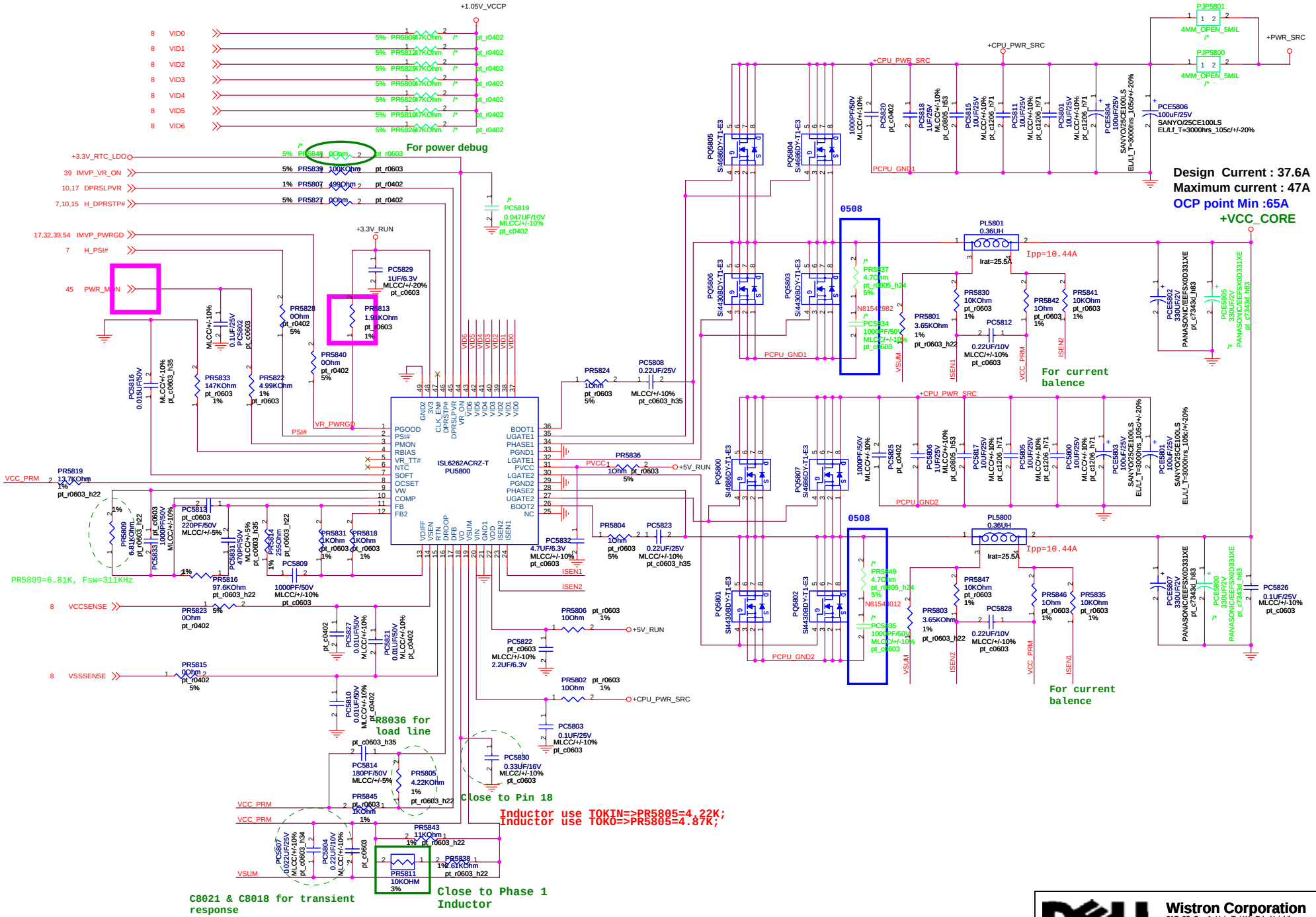

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Title: POWER_VCORE

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Custom	Diaz-UMA	A00

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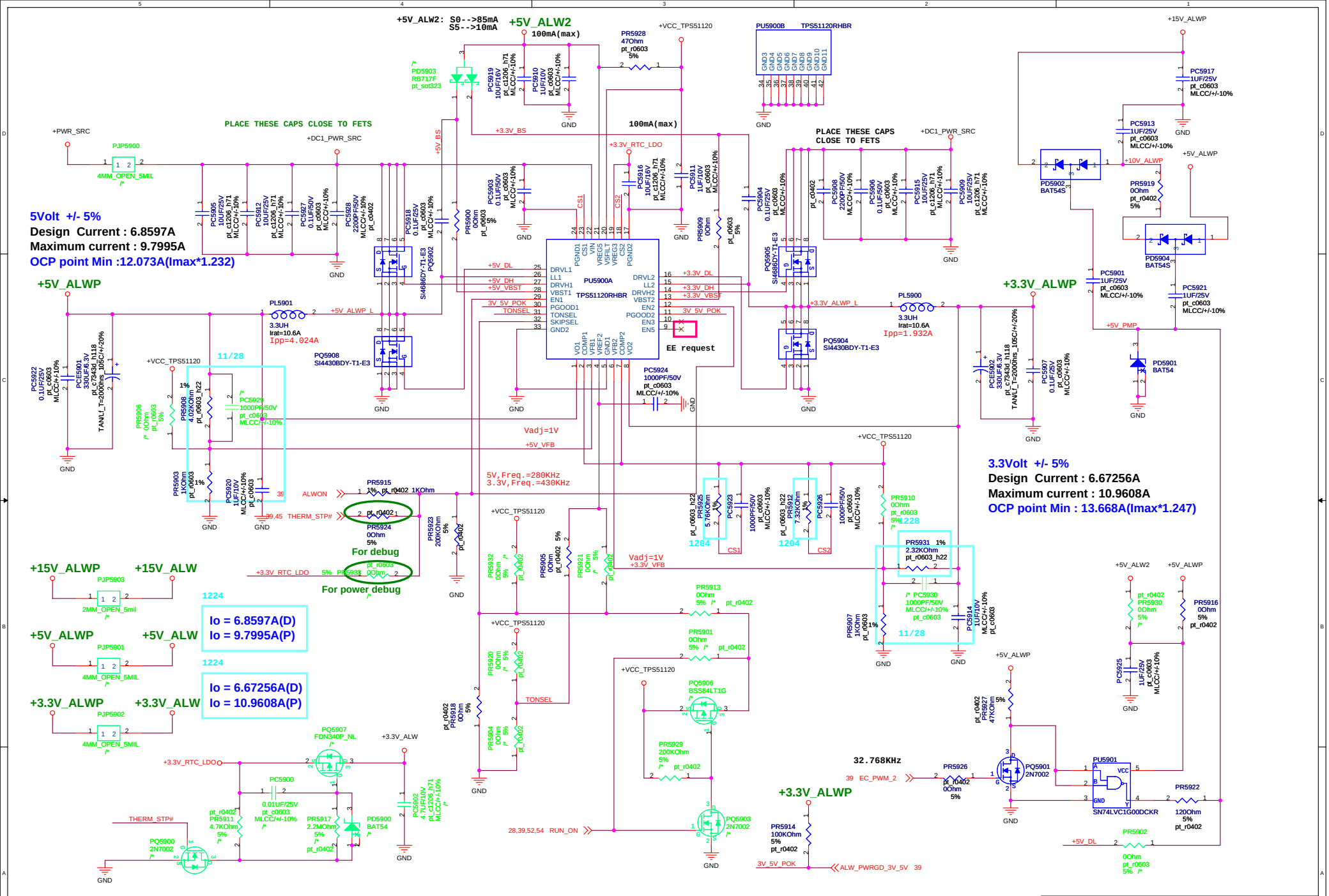
+5V_ALW2: S0-->85mA
S5-->10mA
+5V_ALW2
100mA(max)
PR5928
47Ohm
pt_r0603
5%
+VCC_TPS51120
PU5900B TPS51120RHBR
+15V_ALWP
PC5917
1UF/25V
pt_c0603
MLCC/+/-10%
PD5903
RB717F
pt_sot323
PC5919
10UF/16V
pt_c1206_h71
MLCC/+/-10%
PC5910
1UF/10V
pt_c0603
MLCC/+/-10%
GND
PLACE THESE CAPS CLOSE TO FETS
+PWR_SRC
PJP5900
4MM_OPEN_5MIL
+DC1_PWR_SRC
+3.3V_BS
+5V_BS
+3.3V_RTC_LDO
PLACE THESE CAPS
CLOSE TO FETS
+DC1_PWR_SRC
PC5913
1UF/25V
pt_c0603
MLCC/+/-10%
+5V_ALWP
+10V_ALWP
PD5902
BAT54S
PR5919
0Ohm
pt_r0402
5%
PD5904
BAT54S
5Volt +/- 5%
Design Current : 6.8597A
Maximum current : 9.7995A
OCP point Min :12.073A(Imax*1.232)
PC5905
10UF/25V
pt_c1206_h71
MLCC/+/-10%
PC5912
10UF/25V
pt_c1206_h71
MLCC/+/-10%
PC5927
0.1UF/50V
pt_c0603
MLCC/+/-10%
PC5928
220PF/50V
MLCC/+/-10%
pt_c0402
PC5918
0.1UF/25V
pt_c0603
MLCC/+/-10%
PR5900
0Ohm
pt_r0603
5%
PC5903
0.1UF/50V
pt_c0603
MLCC/+/-10%
PC5916
10UF/16V
pt_c1206_h71
MLCC/+/-10%
PC5911
1UF/10V
pt_c0603
MLCC/+/-10%
PR5909
0Ohm
pt_c0603
5%
PC5904
0.1UF/25V
pt_c0603
MLCC/+/-10%
PC5908
2200PF/50V
MLCC/+/-10%
PC5906
0.1UF/50V
pt_c0603
MLCC/+/-10%
PC5915
10UF/25V
pt_c1206_h71
MLCC/+/-10%
PC5909
10UF/25V
pt_c1206_h71
MLCC/+/-10%
PQ5905
SI4686DY-T1-E3
PQ5902
SI4686DY-T1-E3
+5V_ALWP
PL5901
3.3UH
Irat=10.6A
Ipp=4.024A
+5V_ALWP_L
PU5900A
TPS51120RHBR
DRVL1
LL1
DRVH1
VBST1
EN1
PGOOD1
TONSEL
SKIPSEL
GND2
PGND1
CS1
VIN
VREG5
VREF1
VREG3
CS2
PGND2
DRVL2
LL2
DRVH2
VBST2
EN2
PGOOD2
EN3
EN5
VO1
COMP1
VFB1
VREF2
GND1
VFB2
COMP2
VO2
+5V_DL
+5V_DH
+5V_VBST
3V_5V_POK
TONSEL
+3.3V_DL
+3.3V_DH
+3.3V_VBST
3V_5V_POK
EE request
PC5924
1000PF/50V
pt_c0603
MLCC/+/-10%
PQ5904
SI4430BDY-T1-E3
PQ5908
SI4430BDY-T1-E3
+3.3V_ALWP_L
PL5900
3.3UH
Irat=10.6A
Ipp=1.932A
+3.3V_ALWP
PC5901
1UF/25V
pt_c0603
MLCC/+/-10%
PC5921
1UF/25V
pt_c0603
MLCC/+/-10%
+5V_PMP
PD5901
BAT54
PC5922
0.1UF/25V
pt_c0603
MLCC/+/-10%
PC5901
330UF/6.3V
pt_c7343d_h118
TANUL_T=2000hrs_105C/+/-20%
+VCC_TPS51120
11/28
PR5906
0Ohm
pt_c0603
5%
PR5908
4.02KOhm
pt_c0603_h22
PC5929
1000PF/50V
pt_c0603
MLCC/+/-10%
PC5902
330UF/6.3V
pt_c7343d_h118
TANUL_T=2000hrs_105C/+/-20%
PC5907
0.1UF/25V
pt_c0603
MLCC/+/-10%
Vadj=1V
+5V_VFB
3.3Volt +/- 5%
Design Current : 6.67256A
Maximum current : 10.9608A
OCP point Min : 13.668A(Imax*1.247)
PR5903
1KOhm
pt_c0603
1%
PC5920
1UF/10V
MLCC/+/-10%
pt_c0603
ALWON
PR5915
1%
pt_r0402
1KOhm
THERM_STP#
PR5924
0Ohm
5%
For debug
PR5923
200KOhm
5%
pt_r0402
5V,Freq.=280KHz
3.3V,Freq.=430KHz
PR5925
5.76KOhm
1%
PC5923
1000PF/50V
pt_c0603
MLCC/+/-10%
PR5912
7.32KOhm
1%
PC5926
1000PF/50V
pt_c0603
MLCC/+/-10%
1204
CS1
CS2
PR5910
0Ohm
pt_r0603
5%
1228
PR5931 1%
2.32KOhm
pt_r0603_h22
PC5930
1000PF/50V
MLCC/+/-10%
pt_c0603
PC5914
1UF/10V
MLCC/+/-10%
pt_c0603
PR5907
1KOhm
pt_r0603
1%
11/28
+15V_ALWP
+15V_ALW
PJP5903
2MM_OPEN_5mil
+3.3V_RTC_LDO
PR5933
0Ohm
5%
For power debug
PR5932
0Ohm
5%
PR5905
0Ohm
pt_r0402
5%
PR5921
0Ohm
5%
Vadj=1V
+3.3V_VFB
PR5913
0Ohm
5%
pt_r0402
1224
Io = 6.8597A(D)
Io = 9.7995A(P)
+5V_ALWP
+5V_ALW
PJP5901
4MM_OPEN_5MIL
PR5901
0Ohm
5%
pt_r0402
PR5930
0Ohm
5%
PR5916
0Ohm
5%
pt_r0402
PC5925
1UF/25V
pt_c0603
MLCC/+/-10%
1224
Io = 6.67256A(D)
Io = 10.9608A(P)
+3.3V_ALWP
+3.3V_ALW
PJP5902
4MM_OPEN_5MIL
PR5920
0Ohm
5%
pt_r0402
PR5918
0Ohm
5%
PR5904
0Ohm
5%
TONSEL
PQ5906
BSS84LT1G
PR5929
200KOhm
5%
pt_r0402
PQ5907
FDN340P_NL
+3.3V_ALW
PC5900
0.01UF/25V
pt_c0603
MLCC/+/-10%
PR5911
4.7KOhm
5%
PR5917
2.2MOhm
5%
pt_r0402
PD5900
BAT54
PC5902
4.7UF/10V
pt_c1206_h71
MLCC/+/-10%
PQ5900
2N7002
PQ5903
2N7002
28,39,52,54 RUN_ON
PR5914
100KOhm
5%
pt_r0402
3V_5V_POK
ALW_PWRGD_3V_5V 39
32.768KHz
39 EC_PWM_2
PR5926
0Ohm
5%
PR5927
47KOhm
5%
PQ5901
2N7002
PU5901
SN74LVC1G00DCKR
PR5922
120Ohm
5%
pt_r0402
PR5902
0Ohm
5%
+5V_DL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
POWER_SYSTEM 5V_ALW&3.3V_ALW
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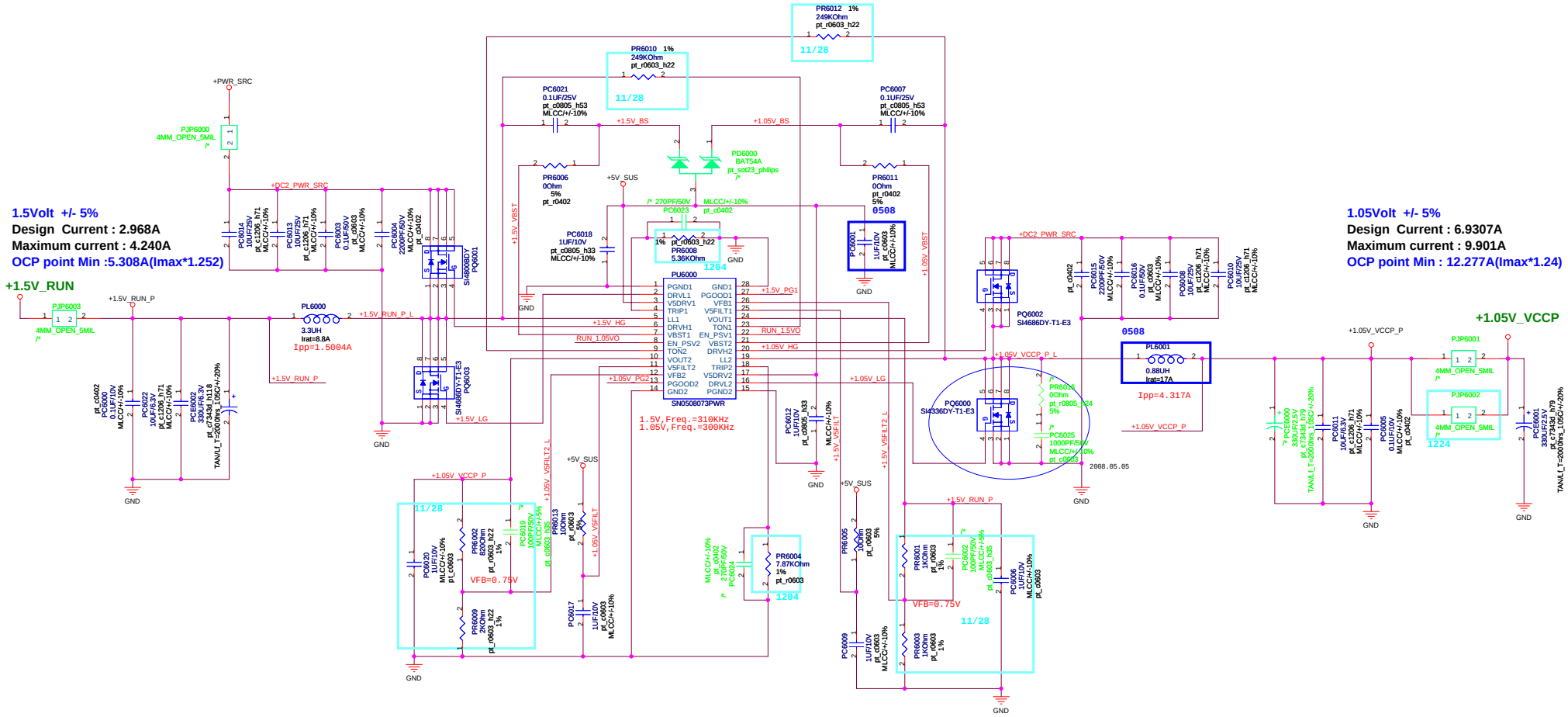
Document Number
Diaz-UMA
Rev
A00
Date: Tuesday, August 19, 2008
Sheet 59 of 68



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Title: POWER_I/O_1.5VS & 1.05VS

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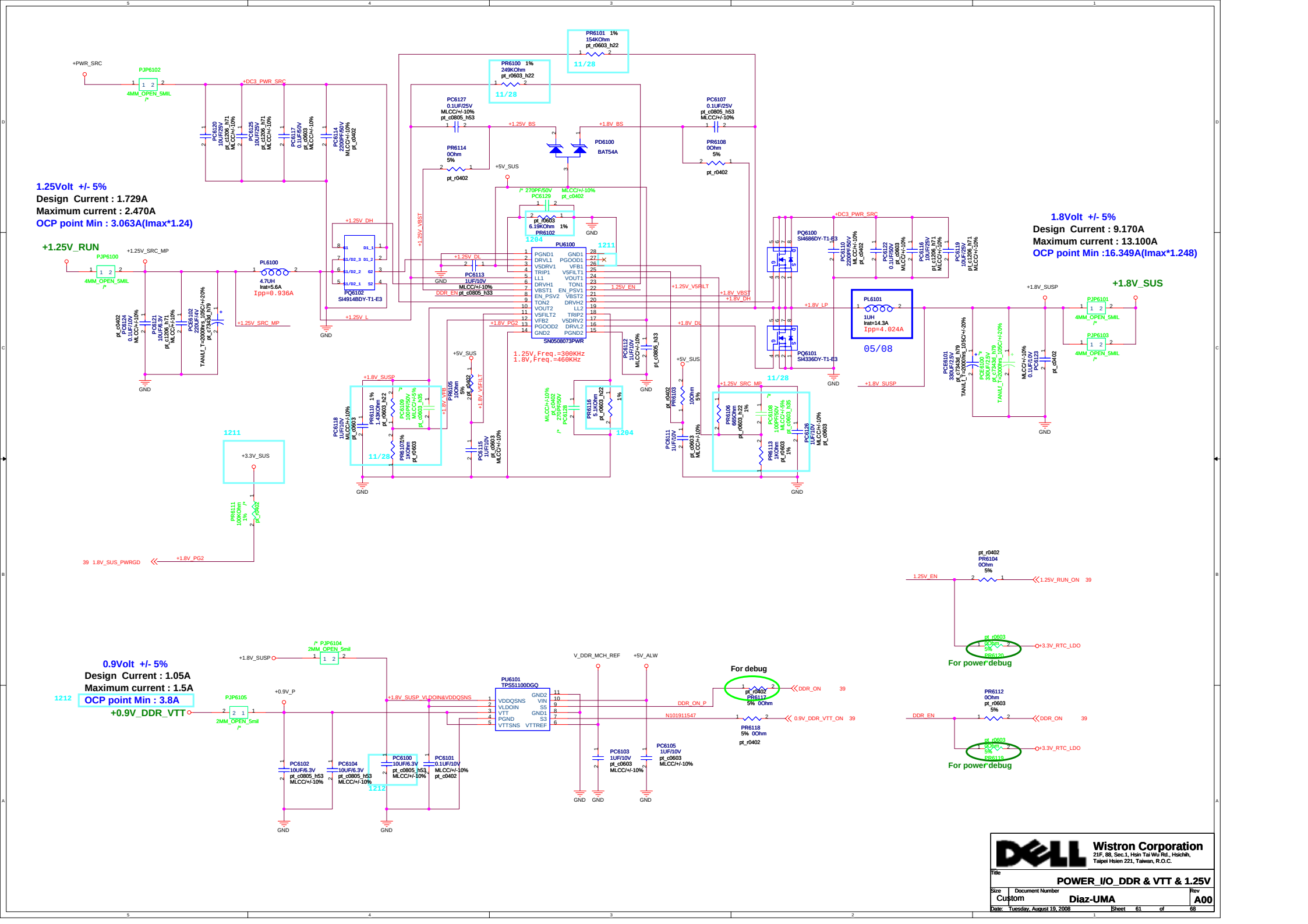
1.25Volt +/- 5%
Design Current : 1.729A
Maximum current : 2.470A
OCP point Min : 3.063A(Imax*1.24)
+1.25V_RUN
1.8Volt +/- 5%
Design Current : 9.170A
Maximum current : 13.100A
OCP point Min :16.349A(Imax*1.248)
+1.8V_SUS
0.9Volt +/- 5%
Design Current : 1.05A
Maximum current : 1.5A
OCP point Min : 3.8A
+0.9V_DDR_VTT
PU6100
SN0508073PWR
1.25V,Freq.=300KHz
1.8V,Freq.=460KHz
PU6101
TPS51100DGQ
PL6100
PL6101
PQ6100
PQ6101
PQ6102
PD6100
BAT54A
For debug
For power debug
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
POWER_I/O_DDR & VTT & 1.25V
Size
Custom
Document Number
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Title	BLANK PAGE
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Date:	Tuesday, August 19, 2008
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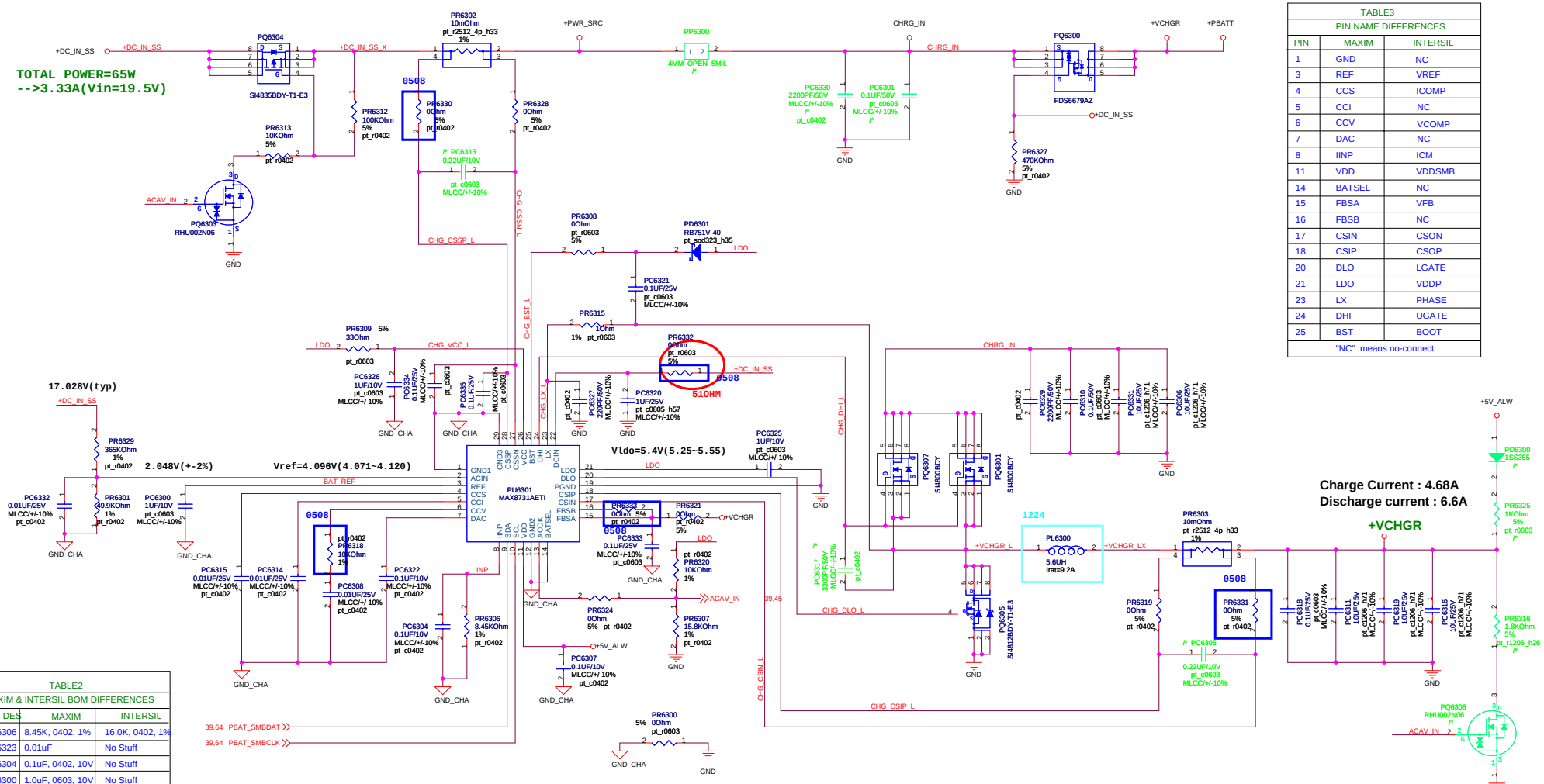
TOTAL POWER=65W
-->3.33A(Vin=19.5V)
17.028V(typ)
2.048V(+-2%)
Vref=4.096V(4.071~4.120)
Vldo=5.4V(5.25~5.55)
Charge Current : 4.68A
Discharge current : 6.6A
+VCHGR
PU6301
MAX8731AETI
PL6300
5.6UH
Irat=9.2A
PU6300
LM393DR
PQ6300
FDS6679AZ
PQ6304
SI4835BDY-T1-E3
PQ6303
RHU002N06
PQ6306
RHU002N06
PQ6302
2N7002
PD6301
RB751V-40
PD6300
1SS355
PR6302
10mOhm
PR6303
10mOhm
PR6315
10Ohm
PR6332
510OHM
PR6309
33Ohm
PR6329
365KOhm
PR6301
39.9KOhm
PR6300
PR6312
100KOhm
PR6313
10KOhm
PR6327
470KOhm
PR6328
PR6330
PR6331
PR6319
PR6316
1.8KOhm
PR6325
1KOhm
PR6322
1KOhm
PR6314
PR6317
51.1KOhm
PR6326
33.2KOhm
PR6311
17.8KOhm
PR6305
348Ohm
PR6310
1Ohm
PR6304
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PR6324
PR6307
15.8KOhm
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PR6321
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PR6308
PC6321
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PC6333
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PC6309
100PF/50V
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348Ohm
PC6313
0.22UF/10V
PC6305
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PC6301
0.1UF/50V
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2200PF/50V
PC6317
330PF/50V
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0.1UF/25V
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2200PF/50V
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PC6331
10UF/25V
PC6315
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0.01UF/16V
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PC6300
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PC6323
0.01UF/16V
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PC6302
100PF/50V
PC6322
1KOhm
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PR6329
365KOhm
PR6309
33Ohm
PR6326
1UF/10V
PR6334
0.1UF/25V
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0.1UF/25V
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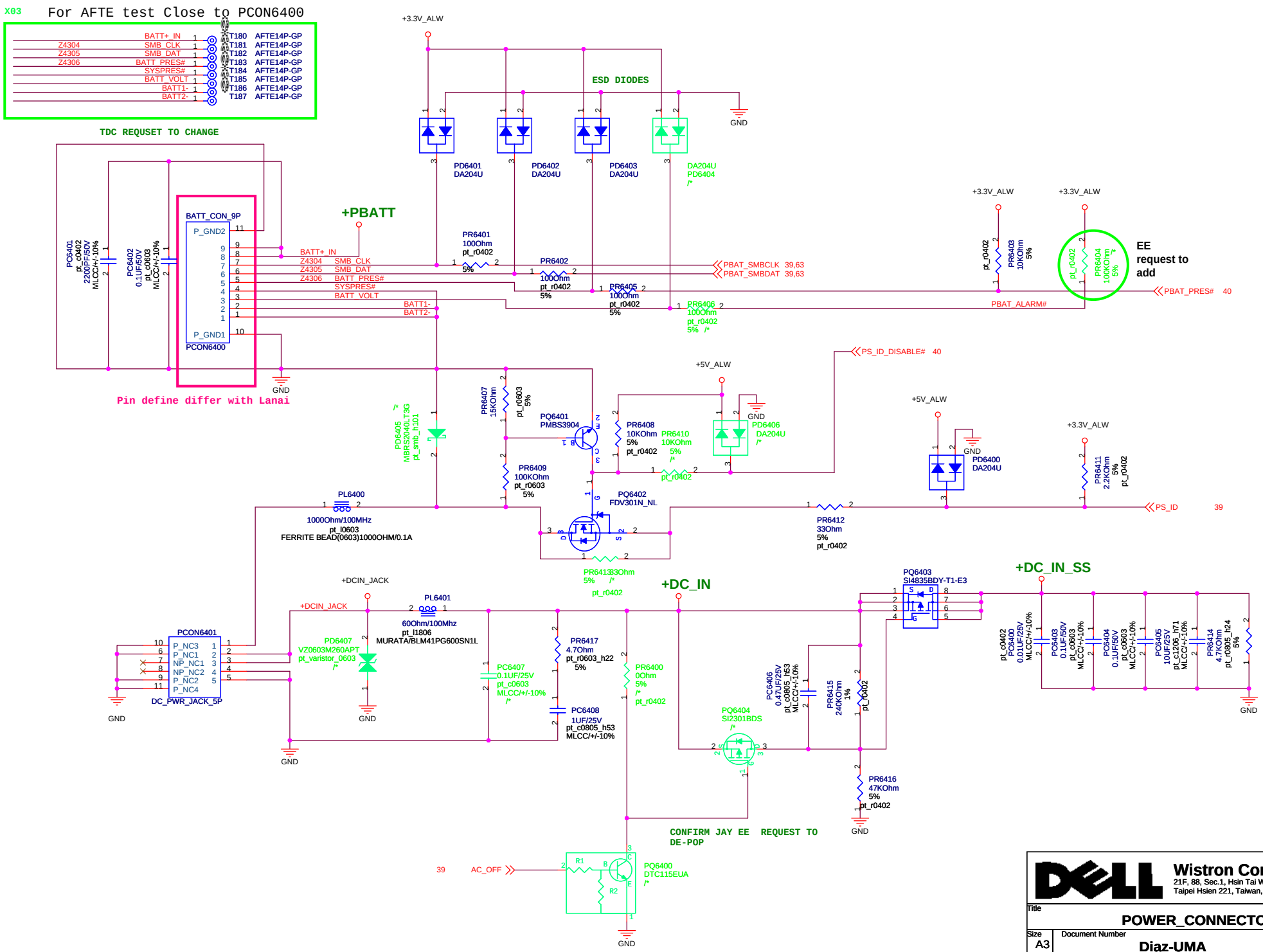

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER_CONNECTOR
Size	A3
Document Number	Diaz-UMA
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Date:	Tuesday, August 19, 2008
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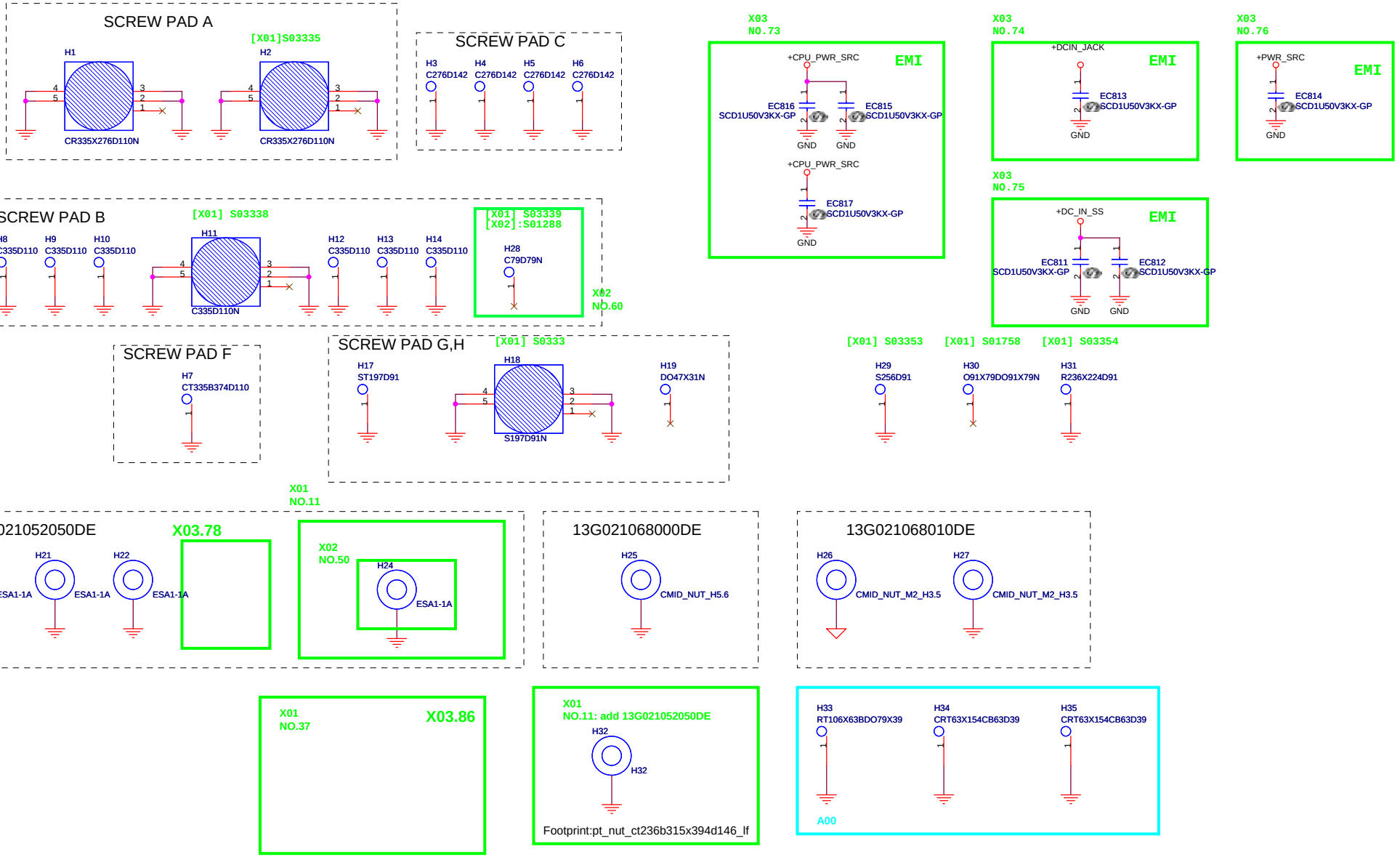

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	SCREW PAD	
Size A3	Document Number Diaz-UMA	Rev A00
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Version Change list for EE Circuit

Item	Page	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	all	X00 release	10/24/2007		X00 release		X00
2	44	Switch power pull	11/30/2007	AA EE	Change main power switch and sniffer power switch power plane to +3.3V_RTC_LDO	Change +RTC_SELL to +3.3V_RTC_LDO	X01
3	30	HDMI power	11/30/2007	AA EE	Modify power diode to MOSFET for leakage current that can lower forwad voltage and match HDMI 5V voltage range	Replace D4612 by Q19 and connect Q19 gate to RUN_ENABLE	X01
4	51	LAN LED	11/30/2007	AA EE	Changed LAN Jack (CON10) pin12 to +3.3V_LAN	Changed LAN Jack (CON10) pin12 to +3.3V_LAN	X01
5	35	Express card power switch	11/30/2007	AA EE	Express Card power switch (U13) pin4 should be connected to +3.3V_RUN for the purpose of using RICOH/R5538 as 2nd source	Connect U13 pin4 to +3.3V_RUN	X01
6	18	ICH8	11/30/2007	AA EE	ICH8 pin AD11 VCCSUSHDA modify to +3.3V_ALW for +3.3V_RUN to solve S5 leackage issue	Connect ICH8 pin AD11 to +3.3V_ALW	X01
7	A1,A2	Audio Board	11/30/2007	AA EE	1.AH1change to NPTH;2.ACON5 change to 12G142001113DE; 3.AU3 pin1 rename to USBP0_D+_U;4.AU3 pin3 rename to USBP0_D-_U	1.AH1change to NPTH;2.ACON5 change to 12G142001113DE; 3.AU3 pin1 rename to USBP0_D+_U;4.AU3 pin3 rename to USBP0_D-_U	X01
8	15,44	LED mask circuit	12/05/2007	AA EE	1.Delete sniffer LED mask circuit 2.modify SATA and WPAN LED circuit.	1.Delete R246,R247,Q43 2.modify SATA and WPAN LED circuit	X01
9	17	CLK_ICH_48M	12/06/2007	AA EE	To improve 48MHz clock signal integrity , pop R339, change C456 to 10pF from 4.7pF and make it stuff.	Pop R339, change C456 to 10pF from 4.7pF and make it stuff.	X01
10	29	CRT signals	12/06/2007	AA EE	Fine tune CRT signals	Change C6649~C6654 to 10pF.	X01
11	65	Screw Hole	12/06/2007	AA EE	Added screw hole by NB thermal solution & ME request	Added H32, changed H24	X01
12	16,35, 50	Reset signals	12/06/2007	AA EE	To improve RESET signals integrity	1. Audio:ICH_AZ_CODEC_RST#, R270=100 ohm 2. HDMI:ICH_AZ_HDMI_RST#, R205=100ohm 3. RICOH:PCI_RST#, R1601=100 ohm, add C6663=10pF 4. WLAN:PLTRST#, add C696=22pF 5. WWAN:PLTRST#, add C697=22pF 6. EC:PLTRST#, add R6972=220ohm	X01
13	28	+LCDVCC	12/06/2007	AA EE	Fine tune LVDS power sequence T1 time	Change R17 to 470K ohm from 330K ohm	X01
14	21	PCI Clock	12/10/2007	AA EE	Fine tune PCI clock slew rate by EA	Swap net name: CLK_PCI_PCCARD & CLK_PCI_8512	X01
15	39	EC power	12/10/2007	AA EE	update EC pin12 net by vender request changed list for batter quality.	Added C3901=0.1uF, C3902=1uF, R3907=0 ohm	X01
16	21,28, 40	EMI component	12/10/2007	AA EE	modify compoment by EMI Comm Team request.	P21: add C2107、C115、C159、C172、C194 P28: add C7110~7111、C7113, C7112 (33pF)、C7114(33pF) P28: remove R2804A/B, add L1 P40: add CN21、CN22、CN23、CN24、CN25、CN26、CN28	X01
17	40	Platform ID	12/10/2007	AA EE	add platform indicator circuit	add R4025~28, net name: PLATFORM_ID[0:1]	X01
18	54	Power Sequence	12/10/2007	AA EE	Flow power circuit.	Remove R73 & net name: 1.25V_RUN_PWRGD	X01
19	40,43	Connector	12/10/2007	AA EE	Changed Connector by ME request.	page 40 -> change CON4010 page 43 -> change CON3	X01
20	C1	CAPBTN I2C	12/12/2007	AA EE	Fine tune CAPBTN I2C timing.	1.Change I2C damping R (CBT_R795) from 330ohm to 100ohm 2.Add through holes CBT_H15(s01291) & CBT_H28(s03350)	X01
21	F1	FingerPrinter LDO	12/12/2007	AA EE	Fine tune LDO performance.	1.F_U3, Pin3(CE pin) connects with Pin1(Vin) 2.F_U3, Pin4(ECO pin) connects with Pin1(Vin)	X01
22	S1	SIM Screw Hole	12/12/2007	AA EE	ME update DXF	change screw hole SH2 & SH3 & SCON1	
23	28	Digital MIC	12/13/2007	AA EE	DMIC clock EMI solution modify	1.R2802 change to 80ohm bead(follow Lanai P/N) 2.R2803 change to 47ohm 3.Mount C748 (33P)	
24	A2	Audio Board	12/14/2007	AA EE	Update eSATA connector for USB function only.	changed ACON5 = 12G142001115DE	
25	39	IT8512E	12/15/2007	AA EE	Del C3921 (IT8512E I version pop 0ohm, J version pop 0.1uF)	Del C3921	
26	40	Platform ID	12/15/2007	AA EE	Del R4025,R4027 to force PCB platform type (Intel SR)	Del R4025,R4027	
27	21,33, 39,50	XTAL	12/15/2007	AA EE	Change XTAL for better capability	(1) X4 24.576MHz change to 07G010222452DE,C453 change to 22pF,C454 change to 22pF (2) X1 25MHz change to 07G010222509DE, C47,C55 change to 33pF (3) X2 14.318MHz change to 07G01021143CDE , (4) X5 32.768KHz change to 07G01020327ADE, change C667,C654 to 15pF	
28	46~48	Audio	12/18/2007	AA EE	Modify Audio BOM	1.Unmount R4602 2.Mount R4601,Q123,R6958 3.Delete R6964,R6965,R6960,R6961,R6970,R6962,R6963,R6971 4.Add R4701,R4702,R4703,R4704,C4701,C4702	
29	50~51	LAN	12/18/2007	AA EE	Modify schematic for triple LED control & EMI solution	1.Add R5110~R5114,D5101; del T5004, add LINK_LED1000# 2.Add C5110~C5117	
30	45,47	Test Point	12/18/2007	AA EE	Add test point for factory ICT team request	Add T33 in U19.23 & T34 in U8.26	
31	41	SPI Flash	12/18/2007	AA EE	Remove SPI Flash dymp RES.	Remove R310, R316, R317, R4102	

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Item	Page	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
32	31	HDD/ODD Power	2007/12/18	AA EE	Modify HDD/ODD power circuit by customer request	1.unmount JP4, R3101 2.POP BOM: R5, R7, R399, R400, C13, Q2, Q3, Q56	X01
33	49,A1 A2	USB charged	2007/12/19	AA EE	Remove USB charged circuit by customer request	1.Delete AU2 2.rename USBP0_D-_U & USBP0_D+_U to USBP0_D- & USBP0_D+ 3.connect CON9,ACON1 pin36 to DGND, pin29 NC.	X01
34	39,41 45,50	Test Point	2007/12/19	AA EE	Add test point by ICT factory request	1.Add T151,T152,T159,T166,T178,T179 for U27 signal pin 2.Add T222,T219,T220,T221 for U2 signal pin 3.Add T148 at U15 pin14, T150 at U8 pin3	X01
35	A2	Audio Board	2007/12/20	AA EE	Modify USB differential signals.	1.Delete AL7 2.rename USBP0_D+ & USBP0_D- to AICH_USBP0+3 & AICH_USBP0-	X01
36	44	WPAN LED	2007/12/21	AA EE	Pop BOM for WPAN LED support	POP BOM: R4411(100K Ohm)	X01
37	65	Screw Hole	2007/12/25	AA EE	add screw hole for IR Blockade	Add: H32, H33	X01
38	C1	CAPBTN	2007/12/25	AA EE	update CAPBTN Circuit by customer ID modified	Swap net SNS_REWIND & SNS_PLAY, LED_REWIND# & LED_PLAY#	X01
39	F1	FingerPrint Screw	2007/12/25	AA EE	Screw hole (NPTH) modified the internal diameter to 1.7mm and the external diameter to 3mm	Modify F_H1, F_H2	X01
40	17	WPAN CTRL	2007/12/26	AA EE	Modify WPAN detect signals by different WLAN module support.	changed net USB_WPAN_DET# to R1701 & pull up to +3.3V_RUN	X01
41	13,38	Cost Down Plan	2007/12/27	AA EE	Cost Down Plan	CE1303, CE1301 => Change to POSCAP 220U/4V De-pop => C602, C589, C590, C1302, C1312, CE7 C363 => Change 10uF/10V Y5V C1309 => Pop 0.1uF R1301 => Change to 0 ohm De-pop => CE16	X01
42	30,42	Connector	2007/12/28	AA EE	By ME connector changed list	Changed CON6610 = 12G13141108ADE Changed CON6608 = 12G24110193RDE	X01
43	40	Board ID	2008/02/14	AA EE	Changed pcb id to X02	Changed pcb id to X02	X02
44	15	XTAL	2008/02/14	AA EE	Modify C375,C377 per XTAL report	Change C375,C377 to 3.3pF	X02
45	16	ICH8 reset signal	2008/02/14	AA EE	U14, U30, U37: power modify to +3.3V_ALW from +3.3V_RUN	U14, U30, U37: power modify to +3.3V_ALW from +3.3V_RUN	X02
46	41,C1	CapBTN	2008/02/14	AA EE	Add CapBTN IC reset signal	1. Add CBT_RESET pin,add two jumpers on the CapBtn board. 2. Sense pad modify to elliptic through hole 3. Add a reserved 10uF capacitor parallel to +5V_ALW2 on the CapBtn board	X02
47	30,37	Comm. team solution	2008/02/14	AA Comm. Team	Add comm. team solutions	1.Pop L4606, depop RN3701 by comm. team request 2.CMIU: Add C3051 39PF close to C6925	X02
48	47,A1	Audio	2008/02/14	AA EE	Modify ACON2,ACON3,ACON4 footprint. Change value of C492,C496 to improve AP performance	1.ACON4 PCB footprint change to pt_phone_j_6p_4hd_col_lf 2.ACON3,ACON2 footprint change to pt_phone_j_6p_4h_col_lf 3.C492 and C496 Bom change to 2.2U(11G236122511310DE) from 1UF	X02
49	21	Clock	2008/02/18	AA EE	Delete reserved resistors	Delete RN1, RN2, RN3, RN5, RN6, RN7, RN8, RN9, RN10, RN11	X02
50	65	Nut	2008/02/18	AA ME	Swap PN of H23,H24 base on updated DXF	Swap PN of H23,H24	X02
51	C1	CAPBTN	2008/02/19	AA EE	LED Mute/VD/VU of power rail update	LED Mute/VD/VU are connect to +5V_ALW2 power rail	X02
52	39	EC	2008/02/19	AA EE	Support CAPBTN reset signals.	modify net_name U15.109: CAP_EC_RESET, Delete: T3907	X02
53	F1	Finger Print	2008/02/19	AA EE	update F_X1 footprint	update F_X1 footprint: modify pin1 indication	X02
54	C1	CAPBTN	2008/02/19	AA EE	Modify level shift circuit & Hole	1.Add elliptic through holes for BT, WiFi, and HDD LEDs 2.Change CBT_C1 to PT footprint	X02
55	39	EC	2008/02/19	AA EE	Modify Chip version.	update Chip version: 06G042005012DE,option R3920,mount C3920	X02
56	47	Speaker gain	2008/02/21	AA EE	Fine tune gain	1.Unmount R374,R377 and Mount R379,R368 2.R4701,R4703 change 24.3Kohm and R4702,R4704 mount 100Kohm	X02
57	F1	Finger Print	2008/02/22	AA EE	Add Test Point by Factory Request	Add F_T14 Test Point	X02
58	46	Audio	2008/02/22	AA EE	Modify Audio solve pop issue	Modify Audio Circuit	X02
59	44	Switch LED	2008/02/25	AA EE	Modify LED Color by customer request	LED1 changed to 07G01520097SDE, WHITE&ORANGE	X02
60	60,61	POWER	2008/05/7	W EE	PL6001 12.4A change to 17A ;PL6101 14.3A change to 17A;Add PC6001(1u/10V)	Modify power Circuit	X02
61	58	POWER	2008/05/7	W EE	PR5817 change location to PR5837(4.7R 0805);PC5824 change location to PC5834(1000PF/50V); PR5821 change location to PR5849(4.7R 0805);PC5834 change location to PR5835(1000PF/50V);	Modify power Circuit	X02
62	61	POWER	2008/05/7	W EE	PU6101 Pin6,PIN7 swap	Modify power Circuit	X02
63	60	POWER	2008/05/7	W EE	PQ6004(SI4430BDY)change location to PQ6000 (SI4336DY) add PR6016(DY)0R 0805;PC6025(DY) 1000PF/50V;	Modify power Circuit	X02
64	60	POWER	2008/05/7	W EE	POP PC182,POP PC186;PC58 change to 3900pf	Modify power SW Circuit	X02
65	61	POWER	2008/05/7	W EE	POP PR6330(0R),POP PR6332(0R),POP PR6318(10K),POP PR6333(0R),PR6331(0R)	Modify power Circuit	X02
66		POWER	2008/05/7	W EE	DZ1 GM M/B Close GAP (J2,J3,PJP5800,PJP5801,PJP5900,PJP5901,PJP5902,PJP5903,PJP6000,PJP6001,PJP6002,PJP6003, PJP6100,PJP6101,PJP6102,PJP6103,PJP6104,PJP6105,PJP6200,PJP6201,PJP6202,PJP6203,PP6300) DZ1 GM CAPBTN Board Close GAP(CBT_JP1,CBT_JP2) DZ1 GM Audio Board Close GAP(AJ1)	Close power GAP	X02
67	29	CRT	2008/05/16	W EE	Q2901,Q2902 "BSS138N" change to "2N7002"	cahnge part X02	

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Item	Page	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
68	60,61	POWER	2008/06/30	W EE	PR6004 change to 7.87Kohm;PR6100 change to 249Kohm;PR6116 change to 5.1Kohm	cahnge part	X03
69	40	Board ID	2008/06/30	W EE	Board ID change to X03=> R534"Dummy";POP "R535"	cahnge PCB ID	X03
70	L1	Lid Board	2008/06/30	W EE	LID Board: add HALL1 connect" 20.F0866.003"	cahnge part	X03
71	A2	Aduio Board	2008/06/30	W EE	Audio Board :ACON5 change to " PN:12G142001115DE" waiting wistron P/N	cahnge part	X03
72	66~74	I/O Board	2008/07/04	W EE	I/O board schematic remove	independence I/O board shecmatic for layout ME issue	X03
73	65	For EMI	2008/07/04	W EMI	For EMI :+CPU_PWR_SRC add EC816,EC815,EC817 0.1u/50V EMI CAP	EMI solution	X03
74	65	For EMI	2008/07/04	W EMI	For EMI :+DCIN_JACK add EC813 0.1u/50V EMI CAP	EMI solution	X03
75	65	For EMI	2008/07/04	W EMI	For EMI :+DC_IN_SS add EC811,EC812 0.1u/50V EMI CAP	EMI solution	X03
76	65	For EMI	2008/07/04	W EMI	For EMI :+PWR_SRC add EC814 0.1u/50V EMI CAP	EMI solution	X03
77	37	SIM CARD	2008/07/04	W EE	For SI : UIM_CLK add R6634 0R	For SI	X03
78	65	HOLD	2008/07/07	W ME	Cost down remove H23	remove part	X03
79		For ATE	2008/07/07	W ME	all test point change to "ZZ.PAD14.001" page 7 test point T31,42 change to "ZZ.PAD14.001" page 10 test point T127,T27,T29,T28,T126,T18,T19,T21,T25,T23,T35,T37,T40,T38,T39,T36,T20,T24, T22,T26,T41,T137,T32,T135,T128,T130,T131,T30,T1002,T1001 page 11 test point T134,T136 page 15 test point T92,T91,T93,T84,T85,T80,T90,T143,T54,T96,T71,T82,T53 page 16 test point T74,T175,T77,T89,T214,T95 page 17 test point T45,T74,T56,T139,T158,T157,T177,T176,T210,T144,T156,T49,T147,T146,T48,T47 ,T140,T141,T46 page 18 test point T61,T67,T70,T72,T52,T51,T73 page 32 test point T55 page 33 test point T153 page 36 test point T160,T161,T162,T163,T164,T165 page 37 test point T168,T169,T170 page 38 test point T167 page 39 test point T148,T390,T3902,T3905,T3906,T3907,T3909,T3910,T3903,T3904 page 40 test point T4001,T4005 page 41 test point T178,T179,T159,T166,T151,T152,T154 page 45 test point T33,T17,T16,T150,T13 page 50 test point T222,T219,T220,T221,T5002,T5003 page 55 test point T118,T122,T119,T125,T117,T121,T120,T124,T116,T123,T115,T113,T112,T114,T142,T149	New ATE test point change to 14 mils	X03
80		For AFTE	2008/07/07	W ME	Add AFTE test point "ZZ.AFT14.101" Page29 add AFTE test point T311,T312,T313,T314,T315,T316,T317,T318,T171,T172 Page 40 add AFTE test point T500~T529 "ZZ.AFT14.101" for Con5&CON4010 Page 42 add AFTE test point T356~T361 "ZZ.AFT14.101" for Con6610 Page 43 add AFTE test point T347,T348,T349,T350 "ZZ.AFT14.101" for Con663 Page 43 add AFTE test point T351,T352,T353 "ZZ.AFT14.101" for Con6617 Page 44 add AFTE test point T345~T346 "ZZ.AFT14.101" for Con6614 Page 45 add AFTE test point T341,T342,T343 "ZZ.AFT14.101" for Con11 Page 48 add AFTE test point T328,T329,T336 "ZZ.AFT14.101" for Con4801 Page 48 add AFTE test point T337,T338,T339,T340 change to "ZZ.AFT14.101" for Con7 Page 48 add AFTE test point T331,T330,T332,T333,T335,T334 "ZZ.AFT14.101" for Con5301 Page 56 add AFTE test point T320,T321,T322,T323 "ZZ.AFT14.101" for Con1 Page 57 add AFTE test point T188,T189,T190,T191,T192,T193 "ZZ.AFT14.101" for Con6615 Page 64 add AFTE test point T180~T187 "ZZ.AFT14.101" for PCon6400	New AFTE test point change to 14 mils	X03
81	18	Board ID	2008/07/07	W ME	Page 18 L49 change to "68.1R090.10A" ;	change bead dimension	X03
82	29	For ME	2008/07/07	W ME	page 29 con6607 change to wisntron P/N "20.20768.015"	ME modify PCB foot pin	X03
83	29	For SI	2008/07/07	W ME	Page29 L4909,L4910,L4911 CHANGE TO "68.00143.111" BLM18BA220SN1D-GP L4610,L4611 change to "63.R0033.L03" 0R DUMMY C6649,C6650;C6651;C6652;C6653;C6654	For SI issue	X03
84	31	For EE	2008/07/07	W ME	Page 31 remvoe J4 power GAP	Sparate HDD and ODD powe plane	X03
85	40	Board Id	2008/07/07	W ME	page 40 add R538(DY),R539(DY) connect to U29 PIn43 "BID2" for next stage board ID	for board ID	X03
86	65	For ME	2008/07/07	W ME	PAGE 65 REMOVE H33,H34	IR trace issue	X03
87	15	For SI	2008/07/07	W ME	page 15 change R275 to 47R"64.47R05.6DL" for ICH_AZ_CODEC_SDOUT;	For SI issue	X03
88	39	For SI	2008/07/08	W ME	R308,R308 change to 4.7K R	For SI issue	X03
89	65	For ME	2008/08/01	W ME	Page 65 H33,H34,H35 for IR Hold	IR HOLD change	A00
90	33	For SI	2008/08/01	W EE	Page 33 R545 change to 33R	For R5C833 SI Singel	A00
91	30	For SI	2008/08/01	W EE	Page 30 R3002 change to 820R	for HDMI singel	A00
92	52	For Boot	2008/08/01	W EE	Page 52 PC192 change to 0.1u	Drop	A00
93	40	For KB detect	2008/08/01	W EE	Page 40 add R106 10K and R158 20K for LED_BL_DET Page 40 remove BID2 change Board VER to 00	add KB B/L Detect	A00
94	40	For Board ID	2008/08/01	W EE	Page 54 add R417 1KR RESET_OUT# to GND	Board change	A00
95	54	For Boot	2008/08/01	W EE	WWAN remove	for Boot	A00
96	16,21 37,57	Remove WWAN	2008/08/01	W EE	Page 16 DY R356 ,RP4 connect SB_WWAN_PCIE_RST# to +3.3V_RUN Page 16 DY C443,C439 for WWAN remove Page 21 DY R2118,R66 Page 37 DY CON6605,C6644,C6645,C6646,C6647,C6648,C6636,C6637,C6638,C6639,C6640,C6641,C6642,C6643,CE17,CE18 Page 57 DY CON6615	Remove WWAN	A00
97	13,36	For Layout	2008/08/01	W EE	Page 36 Remove J3,Page 13 remove J4	Remove J3 modify for Layout	

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