Hepburn AMD UMA

VER : A00

POWER

REGULATOR +1.5V_RUN/+1.1V_RUN PG 50	**CPU VR** PG 53	**SYSTEM RESET CIRCUIT** PG 45	**BATT CHARGER** PG 47
REGULATOR +1.8V_SUS/+1.2V_ALW /+0.9V_DDR_VTT PG 49	**DC/DC** +3.3V_ALW/+5V_ALW +15V_ALW/+5V_SUS PG 52	**AC/BATT CONNECTOR** PG 54	**RUN POWER SW** +5V/+3.3V/+1.8V/+1.2V_RUN +3.3V/+1.2V_SUS PG 46
VCC_NB 1.2V_ALW_SUS PG 51,54	**+2.5V_RUN** PG 60	**M82_POWER** PG 55	

FAN & THERMAL EMC1423 PG 29

CLOCK SLG8SP628VTR(QFN) PG 25

DDRII-SODIMM1 PG 16,17

DDRII-SODIMM2 PG 16,17

800 MHz DDR II

AMD S1G2 64 X2 (638 S1 socket) PG 3,4,5,6

HT_LINK

Panel Connector PG 26 — LVDS

HDMI CONN. PG 28 — HDMI

CRT CONN. PG 27 — VGA

Side Port Memory PG 11

RS780M 528 FCBGA 21mmX21mm PG 7,8,9,10,11

PCIEx1 — **LAN 5784M** PG 33 — **RJ45/Magnetics** PG 34

PCIEx1 — **EXPRESS-CARD** R5538 PG 37

PCIEx2 — **MINI-CARD** WLAN PG 39

PCIEx1 — **MINI-CARD** WWAN PG 40

MINI-CARD WPAN PG 39

SATA - HDD PG 30 — SATA

Fixed SATA ODD PG 34 — SATA

A_LINK

SB700 528 BGA 21mmX21mm PG 12,13,14,15

USB2.0 x 4 — **USB conn x 4** PG 38

USB2.0 — **Biometric** PG 44

33MHz PCI — **8-in-1 Card Reader** R5C833 PG 35 — 1394 — **1394 CONN.** PG 36

Card Reader CONN. PG 36

E-SATA+USB CONN PG 38 — SATA, USB2.0

Azalia — **AUDIO/AMP** IDT_92HD73C PG 31

USB2.0 — **Camera + D-MIC** PG 32

A-MIC PG 32

SPK conn PG 31

Audio Jacks x3 PG 32

LPC — **KBC** ITE8512 PG 42

CIR PG 43 TSOP36136TS

18X8 — **Keyboard** PG 43

SPI — **USER INTERFACE** PG 44

SPI — FLASH 16Mbits PG 41

PS/2 — **Touchpad** PG 43

QUANTA COMPUTER

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Pg#	Description
1	Schematic Block Diagram
2	Index/Power States and USB/PCI/PCIe map
3-6	CPU page
7-11	RS780M page
12-15	SB700 page
16-17	DDRII SO-DIMM(200P)
18-23	Blank
24	LCD/CRT HYBRID
25	Clock Generator
26	LCD Conn.
27	CRT Conn
28	HDMI
29	FAN /THERMAL
30	SATA (HDD&CD_ROM)
31-32	Audio CODEC(92HD73)/Phone Jack
33-34	LOM /Switch
35-36	PC CARD/1394
37	EXPRESS
38	USB
39	Mini Card
40	WWAN
41	Flash ROM, RTC
42	ITE8512
43	TP/KB/CIR/BT
44	Switch,Keyboard & LED
45	System Reset Circuit
46	RUN POWER
47	Battery Charger
48	DCIN,Batt
49	1.8V_SUS,0.9VTT
50	1.5V_RUN AND 1.1V_RUN
51	+VCC_NB
52	+3.3V_ALW/+5V_SUS
53	VCC_VCORE
54	+1.2V_ALW_SUS
55	Blank
56	Power Rail for system
57	Power Sequence Diagram
58	SMBUS BLOCK
59	Stitch caps and Screw hole.

USB PORT# DESTINATION

SB700	0	Left side USB.
	1	Left side USB.
	2	IO board
	3	IO board
	4	WLAN
	5	WWAN
	6	WPAN
	7	EXPRESS
	10	Biometric
	11	Camera

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CardBus	AD17	REQ#1/GNT#1	IRQ_SERIRQ IRQD

PCI EXPRESS	DESTINATION
Lane 1	WLAN
Lane 2	WPAN
Lane 3	LOM
Lane 4	EXPRESS CARD
Lane 5	WWAN

POWER STATES

State \ Signal	SLP S3#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON)	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF)	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW	+5V_SUS +3.3V_SUS +1.8V_SUS +0.9V_DDR_VTT +1.2V_ALW_SUS	+5V_RUN +3.3V_RUN +2.5V_RUN +1.8V_RUN +1.2V_RUN +1.5V_RUN +VCC_CORE +NB_VCORE
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4 on Battery	OFF	OFF	OFF

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(19)

+1.2V_RUN

	C481	C489	C490	C483	C486	C484	C487
	10U	10U	10U	0.22U	0.22U	180P	180P
	10	10	10	10	10	50	50
	X7R	X7R	X7R	X7R	X7R	NPO	NPO
	0805	0805	0805	0603	0603		

Place close to socket

*** If VLDT is connected only on one side, one 4.7uF C101 cap should be added to the island side**

U24A

+1.2V_RUN

+1.2V_RUN

500mA

HT LINK

	D1	VLDT_A0	VLDT_B0	AE2	
	D2	VLDT_A1	VLDT_B1	AE3	
	D3	VLDT_A2	VLDT_B2	AE4	
	D4	VLDT_A3	VLDT_B3	AE5	
7 HT_CADIN0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	HT_CADOUT0 7
7 HT_CADIN#0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	HT_CADOUT#0 7
7 HT_CADIN1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	HT_CADOUT1 7
7 HT_CADIN#1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	HT_CADOUT#1 7
7 HT_CADIN2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	HT_CADOUT2 7
7 HT_CADIN#2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	HT_CADOUT#2 7
7 HT_CADIN3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	HT_CADOUT3 7
7 HT_CADIN#3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	HT_CADOUT#3 7
7 HT_CADIN4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	HT_CADOUT4 7
7 HT_CADIN#4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	HT_CADOUT#4 7
7 HT_CADIN5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	HT_CADOUT5 7
7 HT_CADIN#5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	HT_CADOUT#5 7
7 HT_CADIN6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	HT_CADOUT6 7
7 HT_CADIN#6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	HT_CADOUT#6 7
7 HT_CADIN7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	HT_CADOUT7 7
7 HT_CADIN#7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	HT_CADOUT#7 7
7 HT_CADIN8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD4	HT_CADOUT8 7
7 HT_CADIN#8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	HT_CADOUT#8 7
7 HT_CADIN9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	HT_CADOUT9 7
7 HT_CADIN#9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	HT_CADOUT#9 7
7 HT_CADIN10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	HT_CADOUT10 7
7 HT_CADIN#10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	HT_CADOUT#10 7
7 HT_CADIN11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	HT_CADOUT11 7
7 HT_CADIN#11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	HT_CADOUT#11 7
7 HT_CADIN12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	HT_CADOUT12 7
7 HT_CADIN#12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	HT_CADOUT#12 7
7 HT_CADIN13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	HT_CADOUT13 7
7 HT_CADIN#13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	HT_CADOUT#13 7
7 HT_CADIN14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	HT_CADOUT14 7
7 HT_CADIN#14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	HT_CADOUT#14 7
7 HT_CADIN15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	HT_CADOUT15 7
7 HT_CADIN#15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	HT_CADOUT#15 7
7 HT_CLKIN0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	HT_CLKOUT0 7
7 HT_CLKIN#0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	HT_CLKOUT#0 7
7 HT_CLKIN1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	HT_CLKOUT1 7
7 HT_CLKIN#1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	HT_CLKOUT#1 7
7 HT_CTLIN0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	HT_CTLOUT0 7
7 HT_CTLIN#0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	HT_CTLOUT#0 7
7 HT_CTLIN1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	HT_CTLOUT1 7
7 HT_CTLIN#1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	HT_CTLOUT#1 7

FOX_PZ6382A-284S-41F

QUANTA COMPUTER

Title	S1G2 HT I/F	
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VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

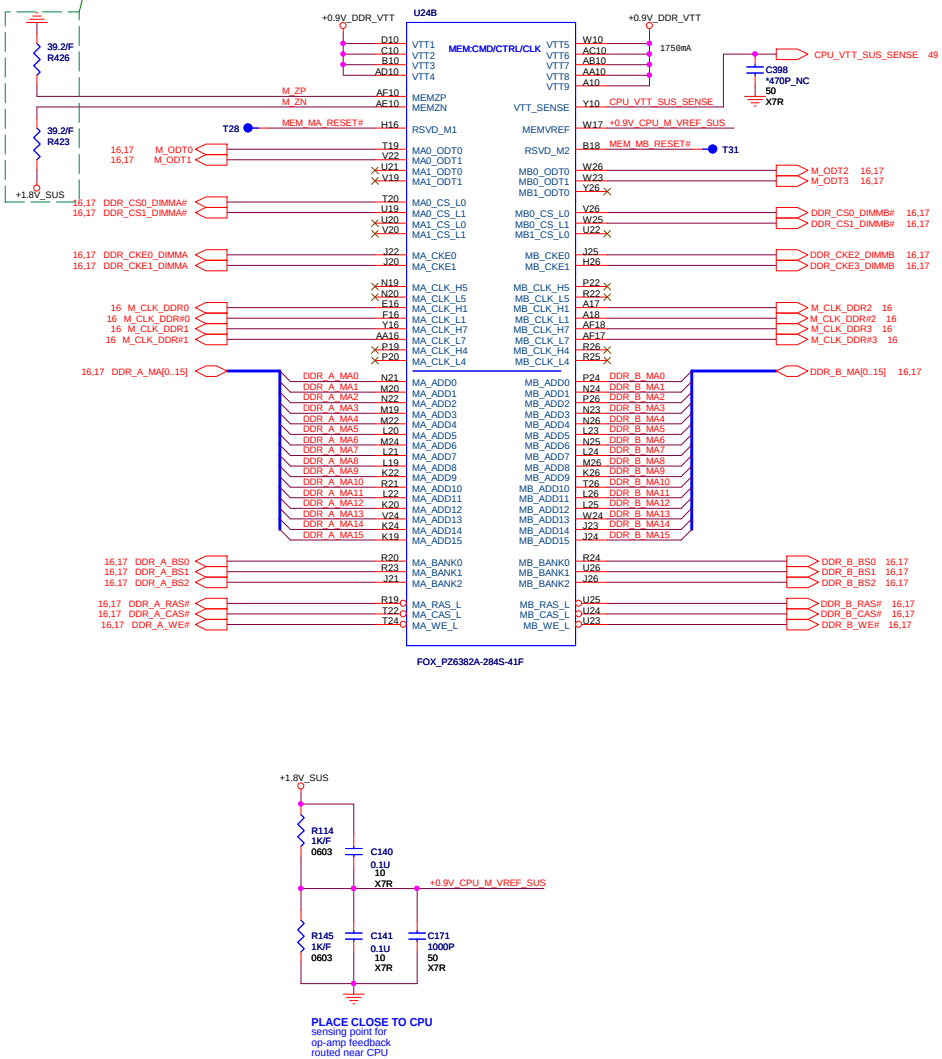
Notes for the SODIMM locations:
DIMMA = CN5
DIMMB = CN6

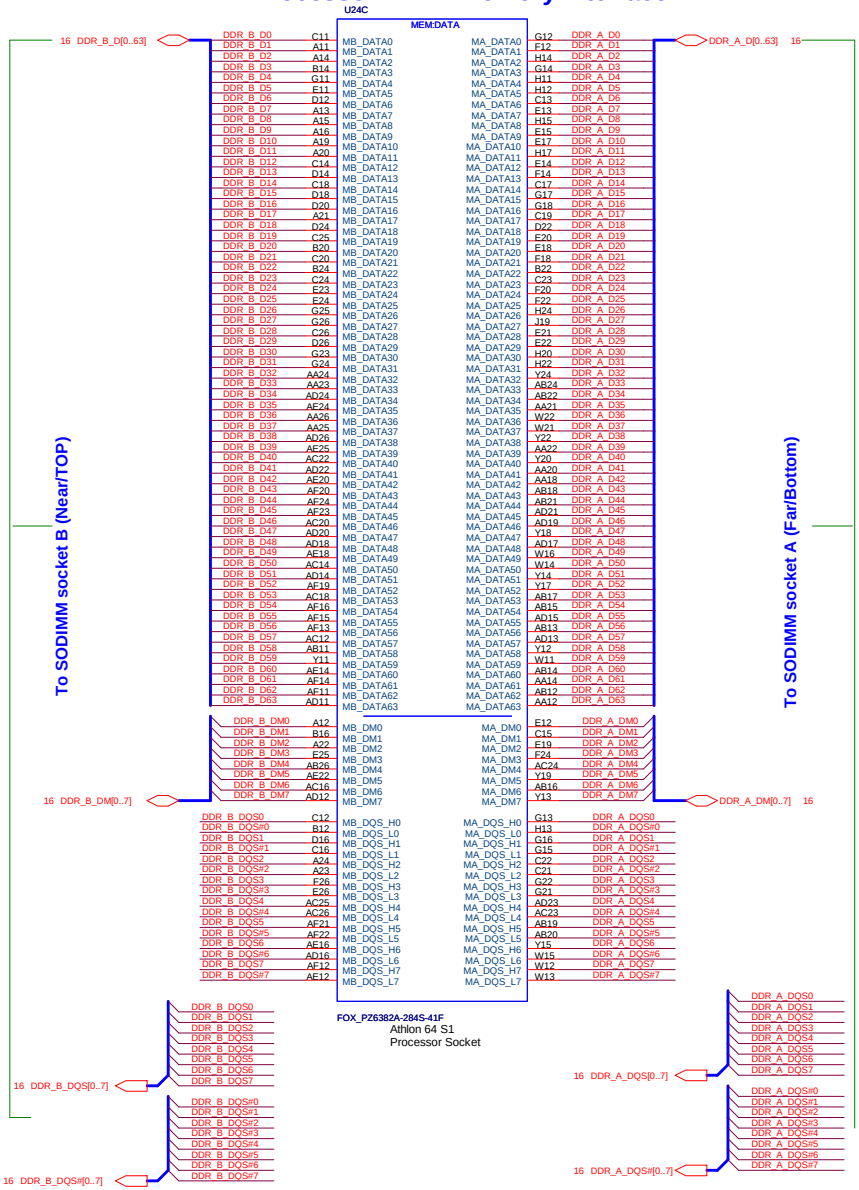
Processor DDR2 Memory Interface

CPU_VTT_SUS_SENSE should be routed as 10mils and 10mils spacing from any adjacent signals in X, Y, Z directions.

KEEP TRACE TO RESISTORS LESS THAN 1.0" FROM CPU PIN

Place Capacitors for +0.9V_CPU_M_VREF_SUS < 1" from the RS780. +0.9V_CPU_M_VREF_SUS trace length < 6", trace width > 15mils and 20mils spacing from any adjacent signals in X, Y, Z directions.





Title	S1G2 DDRII MEMORY	
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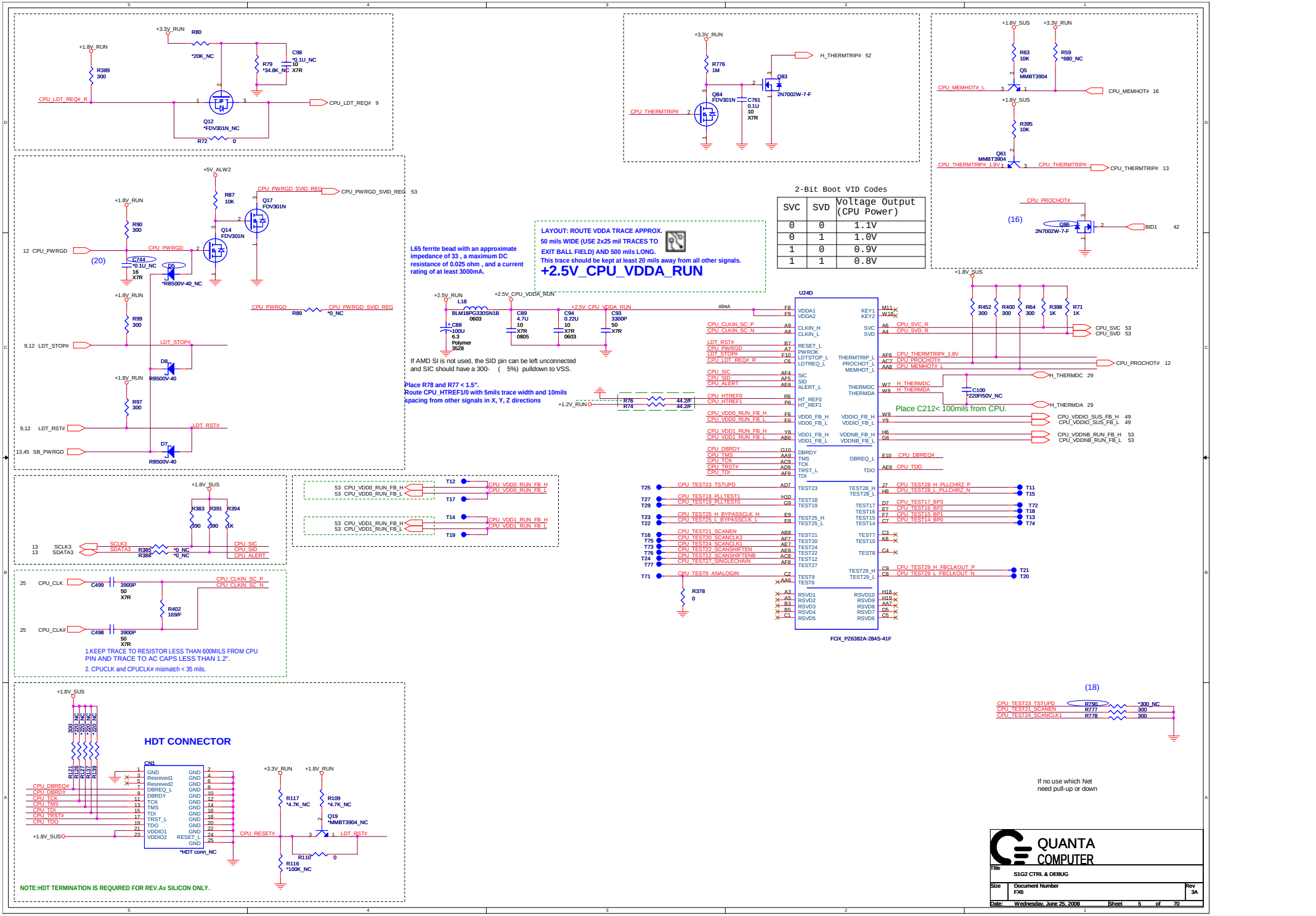
QUANTA COMPUTER


+3.3V_RUN
R80
*20K_NC
+1.8V_RUN
R389
300
C98
*0.1U_NC
10
X7R
R79
*34.8K_NC
CPU_LDT_REQ# R
Q12
*FDV301N_NC
R72
0
CPU_LDT_REQ# 9
+3.3V_RUN
R776
1M
H_THERMTRIP# 52
Q83
2N7002W-7-F
Q84
FDV301N
C761
0.1U
10
X7R
CPU_THERMTRIP#
+1.8V_SUS
+3.3V_RUN
R63
10K
R59
*680_NC
Q5
MMBT3904
CPU_MEMHOT# L
CPU_MEMHOT# 16
+1.8V_SUS
R395
10K
Q61
MMBT3904
CPU_THERMTRIP# 1.8V
CPU_THERMTRIP#
CPU_THERMTRIP# 13
CPU_PROCHOT#
(16)
Q86
2N7002W-7-F
BID1 42
+5V_ALW2
R87
10K
Q17
FDV301N
CPU_PWRGD_SVID_REQ
CPU_PWRGD_SVID_REQ 53
+1.8V_RUN
R90
300
Q14
FDV301N
12 CPU_PWRGD
(20)
C744
*0.1U_NC
16
X7R
D5
*RB500V-40_NC
CPU_PWRGD
R89
*0_NC
CPU_PWRGD_SVID_REQ
+1.8V_RUN
R99
300
9,12 LDT_STOP#
LDT_STOP#
D8
RB500V-40
+1.8V_RUN
R97
300
9,12 LDT_RST#
LDT_RST#
13,45 SB_PWRGD
D7
RB500V-40
L65 ferrite bead with an approximate impedance of 33 , a maximum DC resistance of 0.025 ohm , and a current rating of at least 3000mA.
LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG. This trace should be kept at least 20 mils away from all other signals.
+2.5V_CPU_VDDA_RUN
2-Bit Boot VID Codes
SVC SVD Voltage Output (CPU Power)
0 0 1.1V
0 1 1.0V
1 0 0.9V
1 1 0.8V
+2.5V_RUN
L18
BLM18PG330SN1B
0603
C88
100U
6.3
Polymer
3528
+2.5V_CPU_VDDA_RUN
C89
4.7U
10
X7R
0805
C94
0.22U
10
X7R
0603
C93
3300P
50
X7R
+2.5V_CPU_VDDA_RUN
40mA
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300- (5%) pulldown to VSS.
Place R78 and R77 < 1.5".
Route CPU_HTREF1/0 with 5mils trace width and 10mils spacing from other signals in X, Y, Z directions
+1.2V_RUN
R76
R74
44.2/F
44.2/F
U24D
VDDA1
VDDA2
CLKIN_H
CLKIN_L
RESET_L
PWROK
LDTSTOP_L
LDTREQ_L
SIC
SID
ALERT_L
HT_REF0
HT_REF1
VDD0_FB_H
VDD0_FB_L
VDD1_FB_H
VDD1_FB_L
DBRDY
TMS
TCK
TRST_L
TDI
TEST23
TEST18
TEST19
TEST25_H
TEST25_L
TEST21
TEST20
TEST24
TEST22
TEST12
TEST27
TEST9
TEST6
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
KEY1
KEY2
SVC
SVD
THERMTRIP_L
PROCHOT_L
MEMHOT_L
THERMDC
THERMDA
VDDIO_FB_H
VDDIO_FB_L
VDDNB_FB_H
VDDNB_FB_L
DBREQ_L
TDO
TEST28_H
TEST28_L
TEST17
TEST16
TEST15
TEST14
TEST7
TEST10
TEST8
TEST29_H
TEST29_L
RSVD10
RSVD9
RSVD8
RSVD7
RSVD6
FOX_PZ6382A-284S-41F
CPU_CLKIN_SC_P
CPU_CLKIN_SC_N
LDT_RST#
CPU_PWRGD
LDT_STOP#
CPU_LDT_REQ# R
CPU_SIC
CPU_SID
CPU_ALERT
CPU_HTREF0
CPU_HTREF1
CPU_VDD0_RUN_FB_H
CPU_VDD0_RUN_FB_L
CPU_VDD1_RUN_FB_H
CPU_VDD1_RUN_FB_L
CPU_DBRDY
CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI
CPU_TEST23_TSTUPD
CPU_TEST18_PLLTEST1
CPU_TEST19_PLLTEST0
CPU_TEST25_H_BYPASSCLK_H
CPU_TEST25_L_BYPASSCLK_L
CPU_TEST21_SCANEN
CPU_TEST20_SCANCLK2
CPU_TEST24_SCANCLK1
CPU_TEST22_SCANSHIFTEN
CPU_TEST12_SCANSHIFTENB
CPU_TEST27_SINGLECHAIN
CPU_TEST9_ANALOGIN
R378
0
CPU_DBREQ#
CPU_TDO
CPU_TEST28_H_PLLCHRZ_P
CPU_TEST28_L_PLLCHRZ_N
CPU_TEST17_BP3
CPU_TEST16_BP2
CPU_TEST15_BP1
CPU_TEST14_BP0
CPU_TEST29_H_FBCLKOUT_P
CPU_TEST29_L_FBCLKOUT_N
+1.8V_SUS
R452
300
R400
300
R64
300
R398
1K
R71
1K
CPU_SVC_R
CPU_SVD_R
CPU_SVC 53
CPU_SVD 53
CPU_THERMTRIP# 1.8V
CPU_PROCHOT#
CPU_MEMHOT# L
CPU_PROCHOT# 12
H_THERMDC 29
H_THERMDA 29
C100
*220P/50V_NC
Place C212< 100mils from CPU.
CPU_VDDIO_SUS_FB_H 49
CPU_VDDIO_SUS_FB_L 49
CPU_VDDNB_RUN_FB_H 53
CPU_VDDNB_RUN_FB_L 53
+1.8V_SUS
R383
390
R391
390
R394
1K
13 SCLK3
13 SDATA3
SCLK3
SDATA3
R385
*0_NC
R388
*0_NC
CPU_SIC
CPU_SID
CPU_ALERT
53 CPU_VDD0_RUN_FB_H
53 CPU_VDD0_RUN_FB_L
T12
T17
CPU_VDD0_RUN_FB_H
CPU_VDD0_RUN_FB_L
53 CPU_VDD1_RUN_FB_H
53 CPU_VDD1_RUN_FB_L
T14
T19
CPU_VDD1_RUN_FB_H
CPU_VDD1_RUN_FB_L
25 CPU_CLK
C499
3900P
50
X7R
CPU_CLKIN_SC_P
CPU_CLKIN_SC_N
R402
169/F
25 CPU_CLK#
C498
3900P
50
X7R
1.KEEP TRACE TO RESISTOR LESS THAN 600MILS FROM CPU PIN AND TRACE TO AC CAPS LESS THAN 1.2".
2. CPUCLK and CPUCLK# mismatch < 35 mils.
(18)
CPU_TEST23_TSTUPD
CPU_TEST21_SCANEN
CPU_TEST24_SCANCLK1
R790
R777
R778
*300_NC
300
300
If no use which Net need pull-up or down
+1.8V_SUS
R121 300 *200_NC
R125 300 *200_NC
R127 300 *200_NC
R133 300 *200_NC
R139 300 *200_NC
HDT CONNECTOR
CN1
GND
Resreved1
Resreved2
DBREQ_L
DBRDY
TCK
TMS
TDI
TRST_L
TDO
VDDIO1
VDDIO2
RESET_L
*HDT conn_NC
CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO
+1.8V_SUS
+3.3V_RUN
+1.8V_RUN
R117
*4.7K_NC
R109
*4.7K_NC
Q19
*MMBT3904_NC
CPU_RESET#
LDT_RST#
R110
0
R116
*100K_NC
NOTE:HDT TERMINATION IS REQUIRED FOR REV.Ax SILICON ONLY.
QUANTA COMPUTER
Title
S1G2 CTRL & DEBUG
Size
Document Number
FX6
Rev
3A
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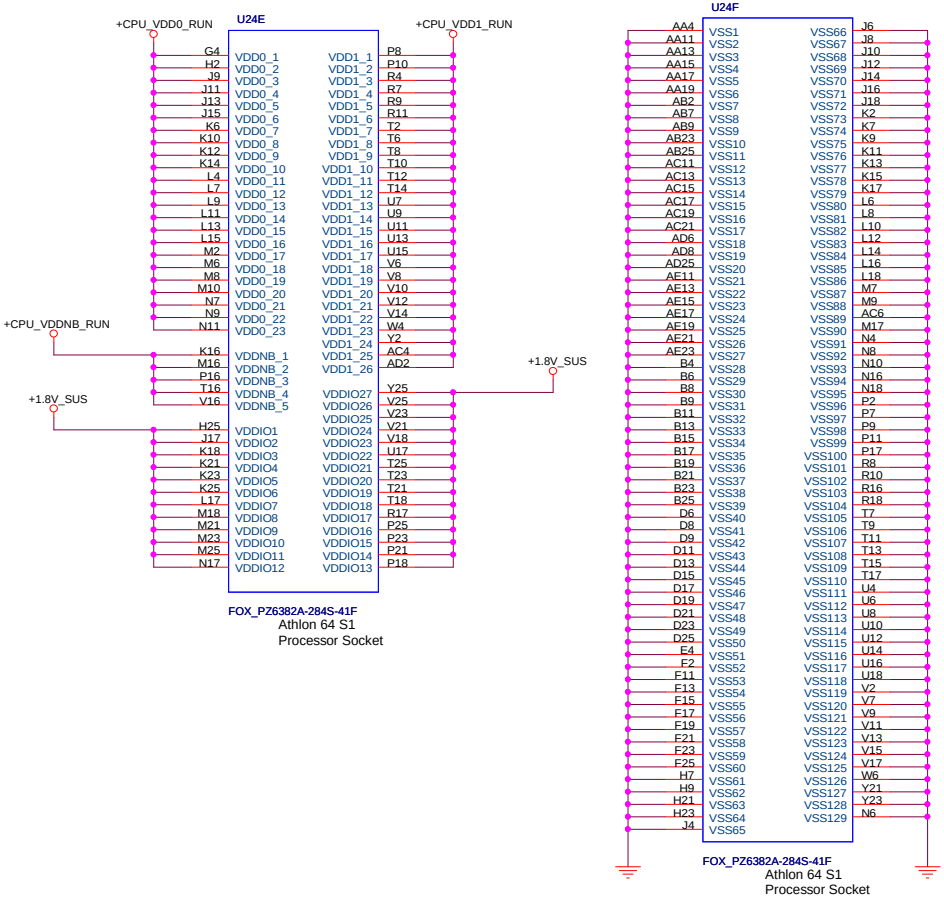
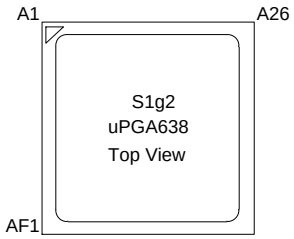
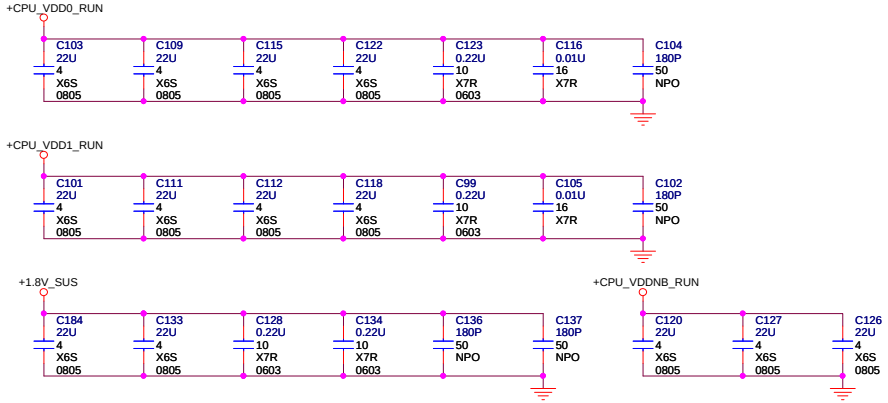
PROCESSOR POWER AND GROUND

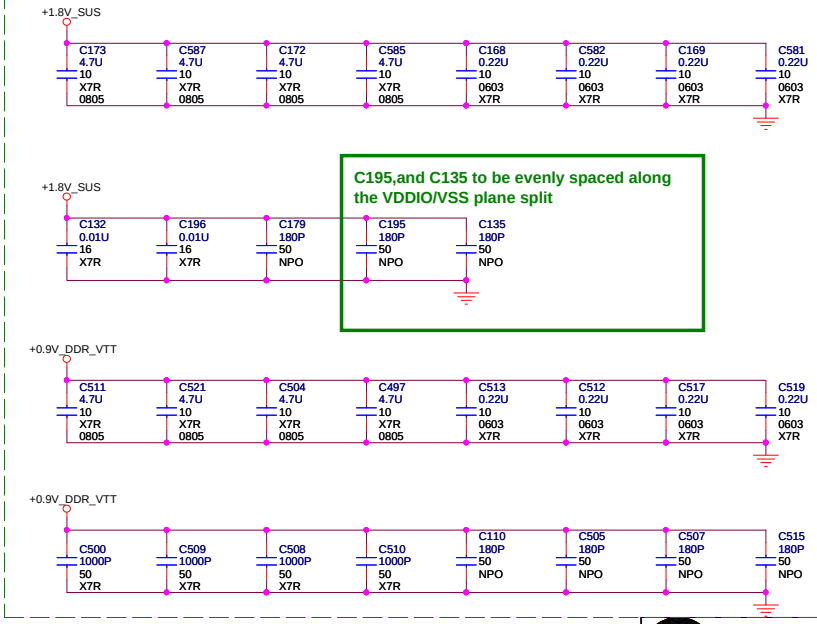




BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



QUANTA COMPUTER

Title	S1G2 PWR & GND	
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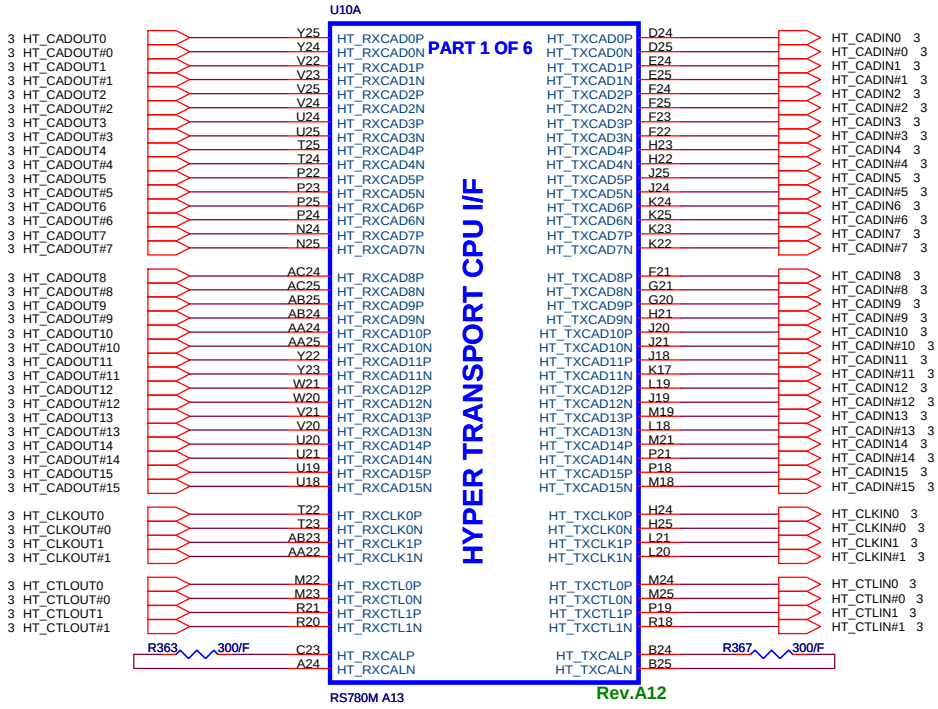

	R363,R367
RS780	301
RX780	1.21K

QUANTA COMPUTER

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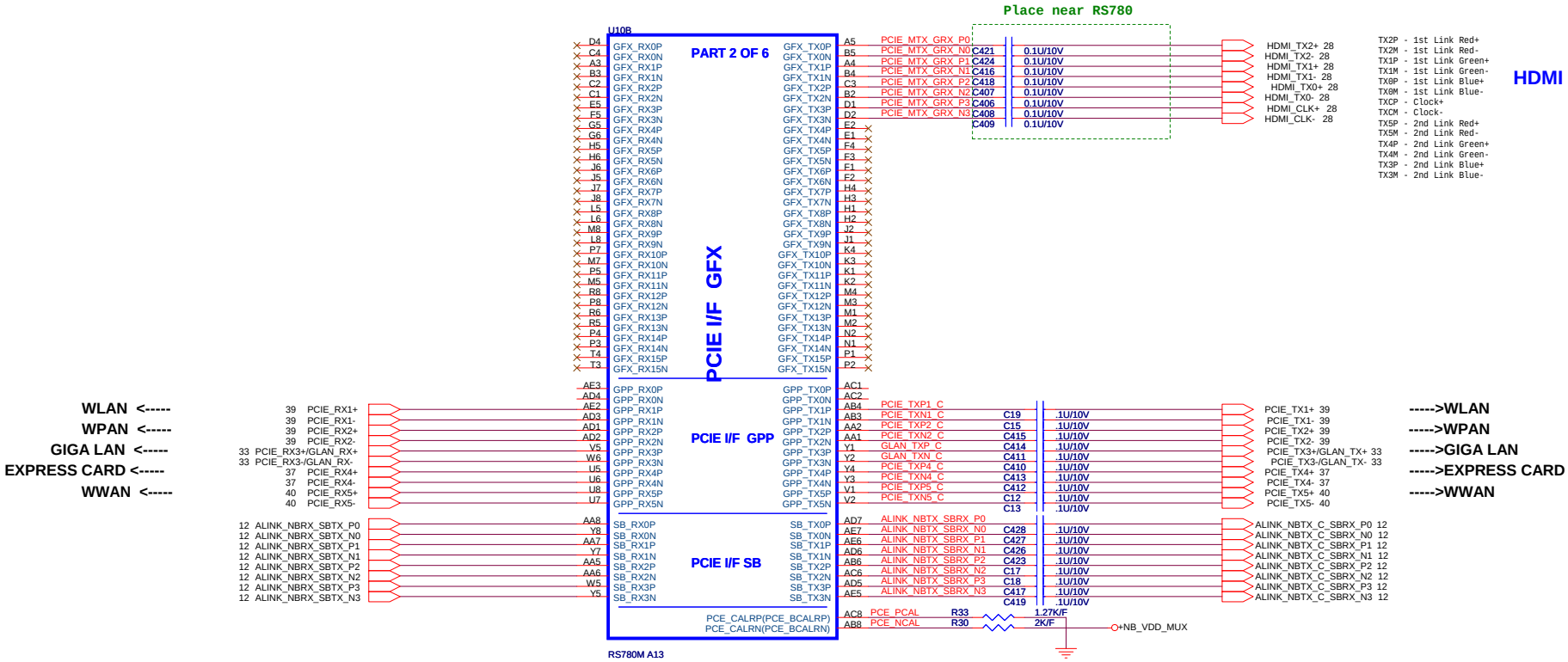

Title	RS780-PCIE I/F
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RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780
AVDD	NC	+3.3V
AVDDDI	NC	+1.8V
AVDDQ	NC	+1.8V
PLLVDD	NC	+1.1V
PLLVDD19	NC	+1.8V
VDDA18PCIEPLL	+1.8V	+1.8V
VDDA18HTPLL	+1.8V	+1.8V
VDDLTP18	NC	+1.8V
VDDLT18	NC	+1.8V
VDDLT33	NC	NC

Close RS780.

LCD_A0+ C463 *10P/50V_NC LCD_A0-
LCD_A1+ C459 *10P/50V_NC LCD_A1-
LCD_A2+ C453 *10P/50V_NC LCD_A2-
LCD_ACLK+ C443 *10P/50V_NC LCD_ACLK-
LCD_B0+ C449 *10P/50V_NC LCD_B0-
LCD_B1+ C447 *10P/50V_NC LCD_B1-
LCD_B2+ C457 *10P/50V_NC LCD_B2-
LCD_BCLK+ C444 *10P/50V_NC LCD_BCLK-

+1.8V_RUN L6 BLM15AG221SN1D 220 ohm @ 100MHz +VDDA18PCIEPLL C21 *10U/10V/0805_NC C20 2.2U 10 X5R 0603
+NB_VDD_MUX L46 BLM15AG221SN1D 220 ohm @ 100MHz 150mA +PLLVDD C434 *10U/10V/0805_NC C436 2.2U 10 X5R 0603
+3.3V_RUN L9 BK1608HS220-T 0603 220 ohm @ 100MHz 135mA +3.3V_AVDD C44 2.2U 10 X5R 0603
+1.8V_RUN L17 BLM15AG221SN1D 220 ohm @ 100MHz +1.8V_HTPLL C84 *10U/10V/0805_NC C85 2.2U 10 X5R 0603
+1.8V_RUN L12 BLM15AG221SN1D 220 ohm @ 100MHz 100mA +PLLVDD18 C69 *10U/10V/0805_NC C67 2.2U 10 X5R 0603
+1.8V_RUN L14 BLM21PG221SN1D 0805 220 ohm @ 100MHz +1.8V_AVDDQ C82 2.2U 10 X5R 0603
+1.8V_RUN R52 0/0805 +1.8V_AVDD C71 2.2U 10 X5R 0603

+1.8V_RUN +VDDG_NB Q52 *BSS138_NL_NC R341 *4.7K_NC NB_LDT_STOP# R637 0
5,12 LDT_STOP#

+1.8V_RUN +VDDG_NB Q3 *BSS138_NL_NC R39 *4.7K_NC NB_ALLOW_LDTSTOP R638 0
5 CPU_LDT_REQ#
12 ALLOW_LDTSTOP

27 VGA_RED
27 VGA_GRN
27 VGA_BLU
R48 140/F R49 150/F R50 150/F
R48,R49,R50 CLOSE TO NB

27 VGAHSYNC
27 VGAVSYNC

+1.1V_RUN Only for RS780 R46 4.7K REFCLK_N R47 4.7K

27 G_DAT_DDC2 INT_VGA_DDCDAT
27 G_CLK_DDC2 INT_VGA_DDCCLK

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
RX780:NB_TV_C; RS780:VSYNC#

RS780	RX780
1 Disable	Enable
0 Enable	Disable

+3.3V_RUN R639 *3K_NC INT_VGAVSYNC
R349 *3K_NC
R369 *3K_NC NB_TV_C

RS780: Enables Side port memory

RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

+3.3V_RUN R347 *3K_NC INT_VGAHSYNC
R346 3K

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RX780: RS780_AUX_CAL RS780:SUS_STAT

12,14,37,39,45 PLTRST# D1 *SDMK0340L-7-F_NC SUS_STAT#_R

R40 0 CLK_NB_14M
C50 49.9/F
AC Term closely clock pin for length: 50 mils

12,14,37,39,45 PLTRST#
5,12 LDT_RST#
R26 0 SYSRESET#
R25 *0_NC

R787 *4.7K_NC SUS_STAT#_R

U1 *AT24C04N-10SU-2.7_NC (NC A1 A2 VSS VCC WP SCL SDA)
+VDDG_NB R10 *10K_NC R8 *2K_NC
LCD_DDCCLK
STRP_DATA
C8 *0.1U_NC 16 X7R
R5 2K

NOTE: ACCESS TO STRAP_DATA and I2C_CLK PINS IS MANDATORY.

+VDDG_NB R23 4.7K R28 4.7K
LCD_DDCCLK
LCD_DDCDAT
C14 *10P/50V_NC C16 *10P/50V_NC

+3.3V_RUN R43 4.7K SUS_STAT#
C54 *10P/50V_NC

U10C — PART 3 OF 6 — RS780M A13

CRT/TVOUT
F12 AVDD1(NC)
E12 AVDD2(NC)
F14 AVDDDI(NC)
G15 AVSSDI(NC)
H15 AVDDQ(NC)
H14 AVSSQ(NC)
F17 C_Pr(DFT_GPIO5)
F17 Y(DFT_GPIO2)
F15 COMP_Pb(DFT_GPIO4)
G18 RED(DFT_GPIO0)
G17 REDb(NC)
E18 GREEN(DFT_GPIO1)
F18 GREENb(NC)
E19 BLUE(DFT_GPIO3)
F19 BLUEb(NC)
A11 DAC_HSYNC(PWM_GPIO4)
B11 DAC_VSYNC(PWM_GPIO6)
E8 DAC_SDA(PCE_TCALRN)
F8 DAC_SCL(PCE_RCALRN)
G14 DAC_RSET(PWM_GPIO1)
T70 T5 T3 T4 T6 T67
INT_VGAHSYNC INT_VGAVSYNC INT_VGA_DDCDAT INT_VGA_DDCCLK
R45 715/F

PLL PWR
A12 PLLVDD(NC)
D14 PLLVDD18(NC)
B12 PLLVSS(NC)
H17 VDDA18HTPLL
D7 VDDA18PCIEPLL1
E7 VDDA18PCIEPLL2

LVTM
D8 SYSRESETb
A10 POWERGOOD
C10 LDTSTOPb
C12 ALLOW_LDTSTOP
R344 300 SYSRESET#
NB_LDT_STOP# NB_ALLOW_LDTSTOP

PM
C25 HT_REFCLKP
C24 HT_REFCLKN
E11 REFCLK_P/OSCIN(OSCIN)
F11 REFCLK_N(PWM_GPIO3)
CLK_NB_14M REFCLK_N

CLOCKS
T2 GFX_REFCLKP
T1 GFX_REFCLKN
U1 GPP_REFCLKP
U2 GPP_REFCLKN
R21 *0_NC R22 *0_NC
V4 GPPSB_REFCLKP(SB_REFCLKP)
V3 GPPSB_REFCLKN(SB_REFCLKN)
RX780->Pop

MIS.
B9 I2C_CLK
A9 I2C_DATA
A8 DDC_CLK0/AUX0P(NC)
B8 DDC_DATA0/AUX0N(NC)
B7 DDC_CLK1/AUX1P(NC)
A7 DDC_DATA1/AUX1N(NC)
T61 T62 T60
B10 STRP_DATA
G11 RSVD
C8 AUX_CAL(NC)
R31 *150/F_NC

TXOUT_L0P(NC) A22 LCD_A0+ 26
TXOUT_L0N(NC) B22 LCD_A0- 26
TXOUT_L1P(NC) A21 LCD_A1+ 26
TXOUT_L1N(NC) B21 LCD_A1- 26
TXOUT_L2P(NC) B20 LCD_A2+ 26
TXOUT_L2N(DBG_GPIO0) A20 T68 LCD_A2- 26
TXOUT_L3P(NC) A19 T7
TXOUT_L3N(DBG_GPIO2) B19 T9
TXOUT_U0P(NC) B18 LCD_B0+ 26
TXOUT_U0N(NC) A18 LCD_B0- 26
TXOUT_U1P(PCIE_RESET_GPIO3) A17 LCD_B1+ 26
TXOUT_U1N(PCIE_RESET_GPIO2) B17 LCD_B1- 26
TXOUT_U2P(NC) D20 LCD_B2+ 26
TXOUT_U2N(NC) D21 LCD_B2- 26
TXOUT_U3P(PCIE_RESET_GPIO5) D18 T8
TXOUT_U3N(NC) D19 T10
TXCLK_LP(DBG_GPIO1) B16 T65 LCD_ACLK+ 26
TXCLK_LN(DBG_GPIO3) A16 T66 LCD_ACLK- 26
TXCLK_UP(PCIE_RESET_GPIO4) D16 LCD_BCLK+ 26
TXCLK_UN(PCIE_RESET_GPIO1) D17 LCD_BCLK- 26

VDDLTP18(NC) A13 +LPVDD
VSSLTP18(NC) B13
C441 0.1U/10V C440 2.2U/10V/0603 +1.8V_RUN L47 BLM15AG221SN1D 220 ohm @ 100MHz
VDDLT18_1(NC) A15 +LVDDR18D
VDDLT18_2(NC) B15
VDDLT33_1(NC) A14
VDDLT33_2(NC) B14
C63 0.1U/10V C64 4.7U/6.3V/0603 +1.8V_RUN L11 BLM15AG221SN1D 220 ohm @ 100MHz
VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22

LVDS_DIGON(PCE_TCALRP) E9 EN_LCDVDD 26
LVDS_BLON(PCE_RCALRP) F7 BIA_PWM 26
LVDS_ENA_BL(PWM_GPIO2) G12 PANEL_BKEN 42
R35 *2.7K_NC R338 *100K_NC

TMDS_HPD(NC) D9 TMDS_HPD
HPD(NC) D10 T1 HDMI_DET 28
TVCLKIN(PWM_GPIO5) D12 R41 0 SUS_STAT# 13
THERMALDIODE_P AE8 NB_THERMDA T63
THERMALDIODE_N AD8 C432 *220P_NC 50
TESTMODE D13 NB_THERMDC T69
R42 1.8K/F

+3.3V_RUN +VDDG_NB R24 0

Place C432 close to U16.

RX780/RS780 DEBUG PIN MAPPING

	RX780	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	AUX_CAL
	COMB_Pb(DFT_GPIO4)	X
	C_Pr(DFT_GPIO5)	X

QUANTA COMPUTER

Title	RS780-LVDS	
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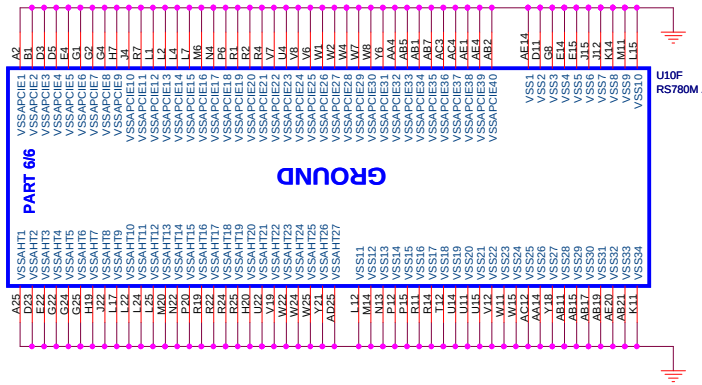
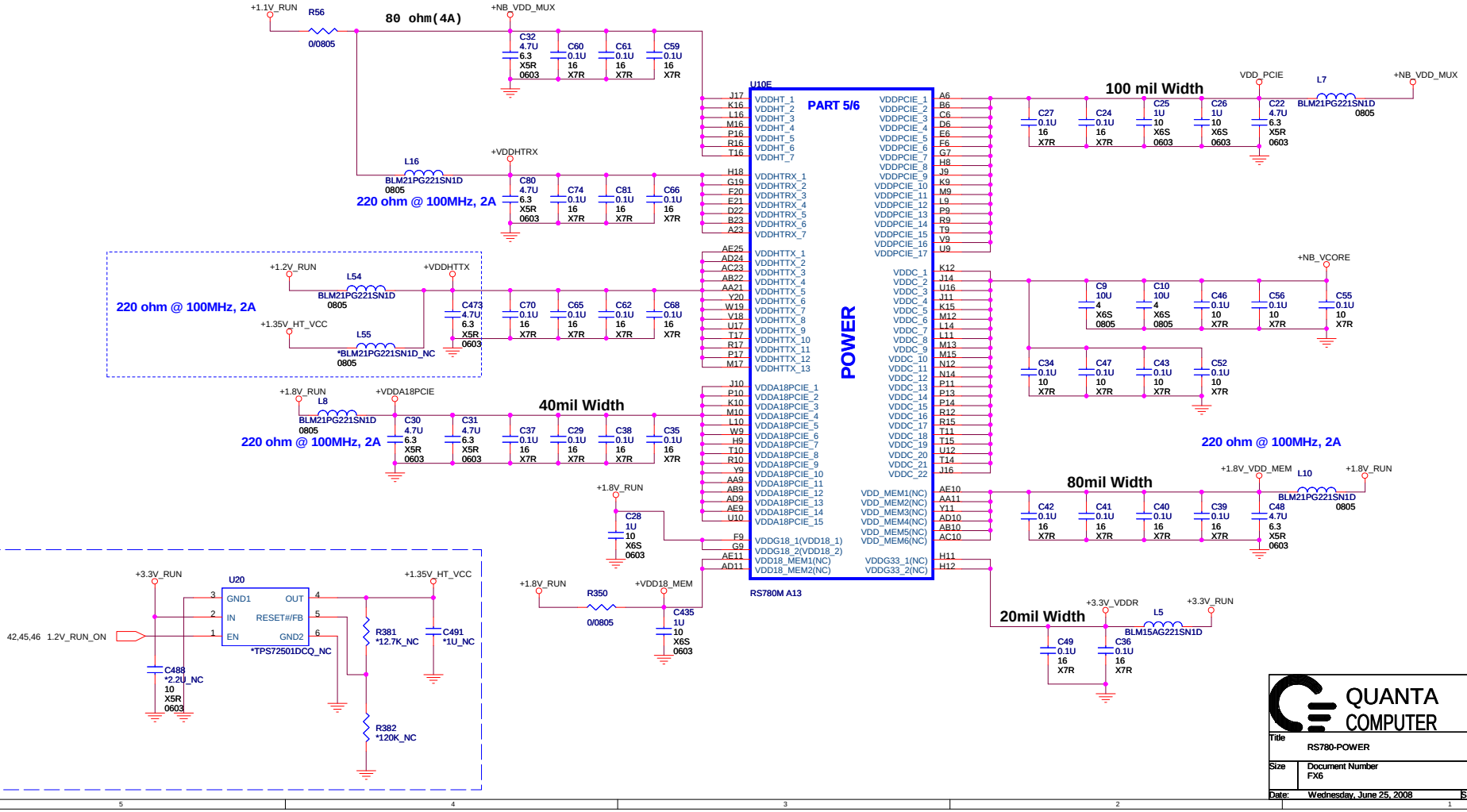
RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V
VDDHTTX	+1.2V	+1.2V
VDDA18PCIE	+1.8V	+1.8V
VDDG18	+1.8V	+1.8V
VDD18_MEM	NC	+1.8V
VDDPCIE	+1.1V	+1.1V
VDDC	+1.1V	+1.1V
VDD_MEM	NC	+1.8V/1.5V DDR2/DDR3
VDDG33	NC	+3.3V





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QUANTA COMPUTER

256-Mbit DDR2 16Mbit*16(4bank)

Bit Swap

U2

MEM_A0 M8 A0 — DQ0 G8 MEM_DQ6
MEM_A1 M3 A1 — DQ1 G2 MEM_DQ2
MEM_A2 M7 A2 — DQ2 H7 MEM_DQ7
MEM_A3 N2 A3 — DQ3 H3 MEM_DQ0
MEM_A4 N8 A4 — DQ4 H1 MEM_DQ1
MEM_A5 N3 A5 — DQ5 H9 MEM_DQ4
MEM_A6 N7 A6 — DQ6 F1 MEM_DQ3
MEM_A7 P2 A7 — DQ7 F9 MEM_DQ5
MEM_A8 P8 A8 — DQ8 C8 MEM_DQ11
MEM_A9 P3 A9 — DQ9 C2 MEM_DQ13
MEM_A10 M2 A10 — DQ10 D7 MEM_DQ10
MEM_A11 P7 A11 — DQ11 D3 MEM_DQ8
MEM_A12 R2 A12 — DQ12 D1 MEM_DQ12
DQ13 D9 MEM_DQ9
MEM_BA0 L2 BA0 — DQ14 B1 MEM_DQ14
MEM_BA1 L3 BA1 — DQ15 B9 MEM_DQ15

MEM_DM1 B3 UDM — UDQS B7 MEM_DQS_P1
MEM_DM0 F3 LDM — UDQS# A8 MEM_DQS_N1

MEM_RAS# K7 RAS — LDQS F7 MEM_DQS_P0
MEM_CAS# L7 CAS — LDQS# E8 MEM_DQS_N0
MEM_WE# K3 WE
MEM_CS# L8 CS
MEM_CKE K2 CKE — NC1 A2
MEM_ODT K9 ODT — NC2 E2
MEM_CLKP — NC3 L1 MEM_BA2
R343 *100_NC — NC4 R3
MEM_CLKN J8 CLK — NC5 R7
K8 CLK# — NC6 R8

+1.8V_MEM_VDDQ — L50 SBK160808G221 — J1 VDDL — VREF J2 MEM_VREF — +1.8V_MEM_VDDQ
J7 VSSDL

C458 1U 10 X5R 0603

A3 VSS_0 — VDD_0 A1
E3 VSS_1 — VDD_1 E1
J3 VSS_2 — VDD_2 J9
N1 VSS_3 — VDD_3 M9
P9 VSS_4 — VDD_4 R1

A7 VSSQ_0 — VDDQ_0 A9
B2 VSSQ_1 — VDDQ_1 C1
B8 VSSQ_2 — VDDQ_2 C3
D2 VSSQ_3 — VDDQ_3 C7
D8 VSSQ_4 — VDDQ_4 C9
E7 VSSQ_5 — VDDQ_5 E9
F2 VSSQ_6 — VDDQ_6 G1
F8 VSSQ_7 — VDDQ_7 G3
H2 VSSQ_8 — VDDQ_8 G7
H8 VSSQ_9 — VDDQ_9 G9

HY5PS561621BFP-25
400M PBGA84
256M EP

Place This CAP near to SDRAM with 0.2".

U10D

PAR 4 OF 6

MEM_A0 AB12 — MEM_A0(NC)
MEM_A1 AE16 — MEM_A1(NC)
MEM_A2 V11 — MEM_A2(NC)
MEM_A3 AE15 — MEM_A3(NC)
MEM_A4 AA12 — MEM_A4(NC)
MEM_A5 AB16 — MEM_A5(NC)
MEM_A6 AB14 — MEM_A6(NC)
MEM_A7 AD14 — MEM_A7(NC)
MEM_A8 AD13 — MEM_A8(NC)
MEM_A9 AD15 — MEM_A9(NC)
MEM_A10 AC16 — MEM_A10(NC)
MEM_A11 AE13 — MEM_A11(NC)
MEM_A12 AC14 — MEM_A12(NC)
T2 Y14 — MEM_A13(NC)

MEM_BA0 AD16 — MEM_BA0(NC)
MEM_BA1 AE17 — MEM_BA1(NC)
MEM_BA2 AD17 — MEM_BA2(NC)

MEM_RAS# W12 — MEM_RASb(NC)
MEM_CAS# Y12 — MEM_CASb(NC)
MEM_WE# AD18 — MEM_WEb(NC)
MEM_CS# AB13 — MEM_CSb(NC)
MEM_CKE AB18 — MEM_CKE(NC)
MEM_ODT V14 — MEM_ODT(NC)

MEM_CLKP V15 — MEM_CKP(NC)
MEM_CLKN W14 — MEM_CKN(NC)

+1.8V_MEM_VDDQ — 40.2/F R355 — MEM_COMP_P AE12 — MEM_COMPP(NC)
40.2/F R354 — MEM_COMP_N AD12 — MEM_COMPN(NC)

SBD_MEM/DVO_I/F

MEM_DQ0/DVO_VSYNC(NC) AA18 MEM_DQ0
MEM_DQ1/DVO_HSYNC(NC) AA20 MEM_DQ1
MEM_DQ2/DVO_DE(NC) AA19 MEM_DQ2
MEM_DQ3/DVO_D0(NC) Y19 MEM_DQ3
MEM_DQ4(NC) V17 MEM_DQ4
MEM_DQ5/DVO_D1(NC) AA17 MEM_DQ5
MEM_DQ6/DVO_D2(NC) AA15 MEM_DQ6
MEM_DQ7/DVO_D4(NC) Y15 MEM_DQ7
MEM_DQ8/DVO_D3(NC) AC20 MEM_DQ8
MEM_DQ9/DVO_D5(NC) AD19 MEM_DQ9
MEM_DQ10/DVO_D6(NC) AE22 MEM_DQ10
MEM_DQ11/DVO_D7(NC) AC18 MEM_DQ11
MEM_DQ12(NC) AB20 MEM_DQ12
MEM_DQ13/DVO_D9(NC) AD22 MEM_DQ13
MEM_DQ14/DVO_D10(NC) AC22 MEM_DQ14
MEM_DQ15/DVO_D11(NC) AD21 MEM_DQ15

MEM_DQS0P/DVO_IDCKP(NC) Y17 MEM_DQS_P0
MEM_DQS0N/DVO_IDCKN(NC) W18 MEM_DQS_N0
MEM_DQS1P(NC) AD20 MEM_DQS_P1
MEM_DQS1N(NC) AE21 MEM_DQS_N1

MEM_DM0(NC) W17 MEM_DM0
MEM_DM1/DVO_D8(NC) AE19 MEM_DM1

IOPLLVDD18(NC) AE23 +1.8V_IOPLLVDD
IOPLLVDD(NC) AE24 +1.1V_IOPLLVDD
IOPLLVSS(NC) AD23
MEM_VREF(NC) AE18 MEM_VREF1

RS780M A13

220 ohm @ 100MHz

L49 BLM15AG221SN1D — +1.8V_RUN
+NB_VDD_MUX
L52 BLM15AG221SN1D

C465 2.2U 10 0603 X7R
C460 2.2U 10 0603 X5R

MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780
IOPLLVDD18	NC	+1.8V
IOPLLVDD	NC	+1.1V

ALL external components connected to SPMEM signals must be removed for RX780.

At least 200mils wide and locate after DDR2 SDRAM

+0.9V_MEM_VTT

MEM_A8 RP24 MEM_A0 — *4P2R-47 — NC C467 0.1U/10V — +1.8V_MEM_VDDQ
C429 0.1U/10V
MEM_A2 RP26 MEM_A6 — *4P2R-47 — NC C433 0.1U/10V — +1.8V_MEM_VDDQ
C431 0.1U/10V
MEM_A7 RP27 MEM_A9 — *4P2R-47 — NC
C469 0.1U/10V — +1.8V_MEM_VDDQ
MEM_A11 RP25 MEM_A4 — *4P2R-47 — NC C442 0.1U/10V
MEM_BA0 RP30 MEM_BA2 — *4P2R-47 — NC
C468 0.1U/10V — +1.8V_MEM_VDDQ
MEM_A10 RP32 MEM_A5 — *4P2R-47 — NC
MEM_BA1 RP31 MEM_A1 — *4P2R-47 — NC C448 0.1U/10V
MEM_A12 RP28 MEM_A3 — *4P2R-47 — NC C454 0.1U/10V — +1.8V_MEM_VDDQ
MEM_CS# RP22 MEM_ODT — *4P2R-47 — NC C437 0.1U/10V
C470 0.1U/10V — +1.8V_MEM_VDDQ
MEM_CAS# RP23 MEM_RAS# — *4P2R-47 — NC C466 *0.1U/10V_NC
MEM_CKE RP29 MEM_WE# — *4P2R-47 — NC C430 0.1U/10V

Only for RS780

+1.8V_MEM_VDDQ — C472 0.1U 10 X7R — R365 1K/F — MEM_VREF
C471 0.1U 10 X7R — R364 1K/F

+1.8V_MEM_VDDQ — C451 0.1U 10 X7R — R359 1K/F — MEM_VREF1
C446 0.1U 10 X7R — R358 1K/F

+0.9V_MEM_VTT

+C86 100U 6.3 3528
C87 22U 6.3 X5R 0805

Q4 BSC032N03S — +0.9V_DDR_VTT

46 1.8V_RUN_ENABLE

+1.8V_MEM_VDDQ

+1.8V_RUN — L45 BLM21PG221SN1D

C420 22U 6.3 X5R 0805
+C425 330U 6.3 7343
C439 1U 6.3 X5R
C445 1U 6.3 X5R
C438 0.1U 10 X7R
C452 0.1U 10 X7R

Local Frame Buffer(64MB) DDRII Power

QUANTA COMPUTER

Title	RS780-SIDE PORT I/O	
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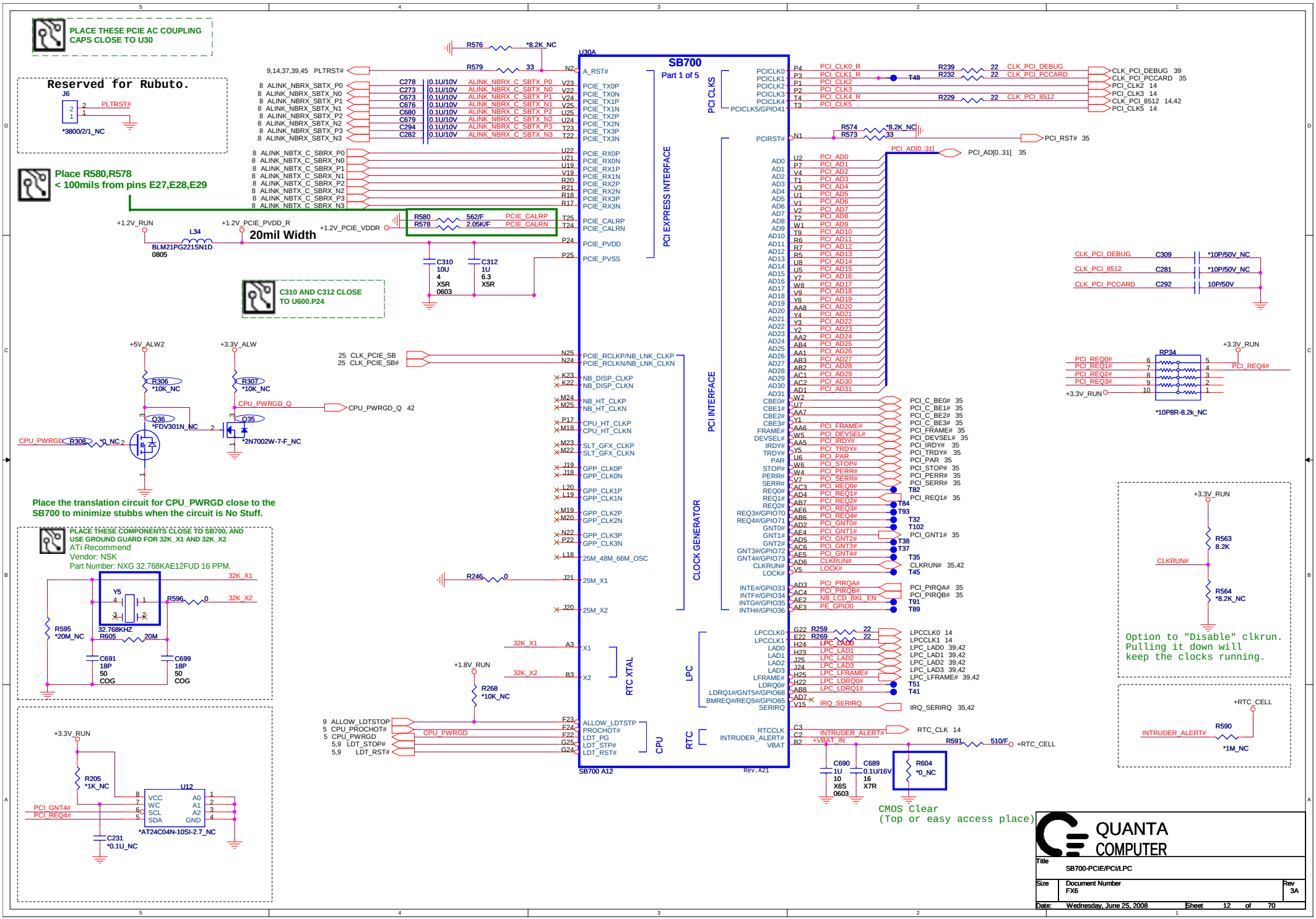
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U30
Reserved for Rubuto.
J6
PLTRST#
*3800/2/1_NC
Place R580,R578
< 100mils from pins E27,E28,E29
20mil Width
L34
BLM21PG221SN1D
0805
C310 AND C312 CLOSE TO U600.P24
Place the translation circuit for CPU_PWRGD close to the SB700 to minimize stubbs when the circuit is No Stuff.
PLACE THESE COMPONENTS CLOSE TO SB700, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.
32.768KHZ
*AT24C04N-10SI-2.7_NC
U30A
SB700
Part 1 of 5
SB700 A12
Rev. A21
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
Option to "Disable" clkrun. Pulling it down will keep the clocks running.
CMOS Clear
(Top or easy access place)
QUANTA COMPUTER
Title
SB700-PCIE/PCI/LPC
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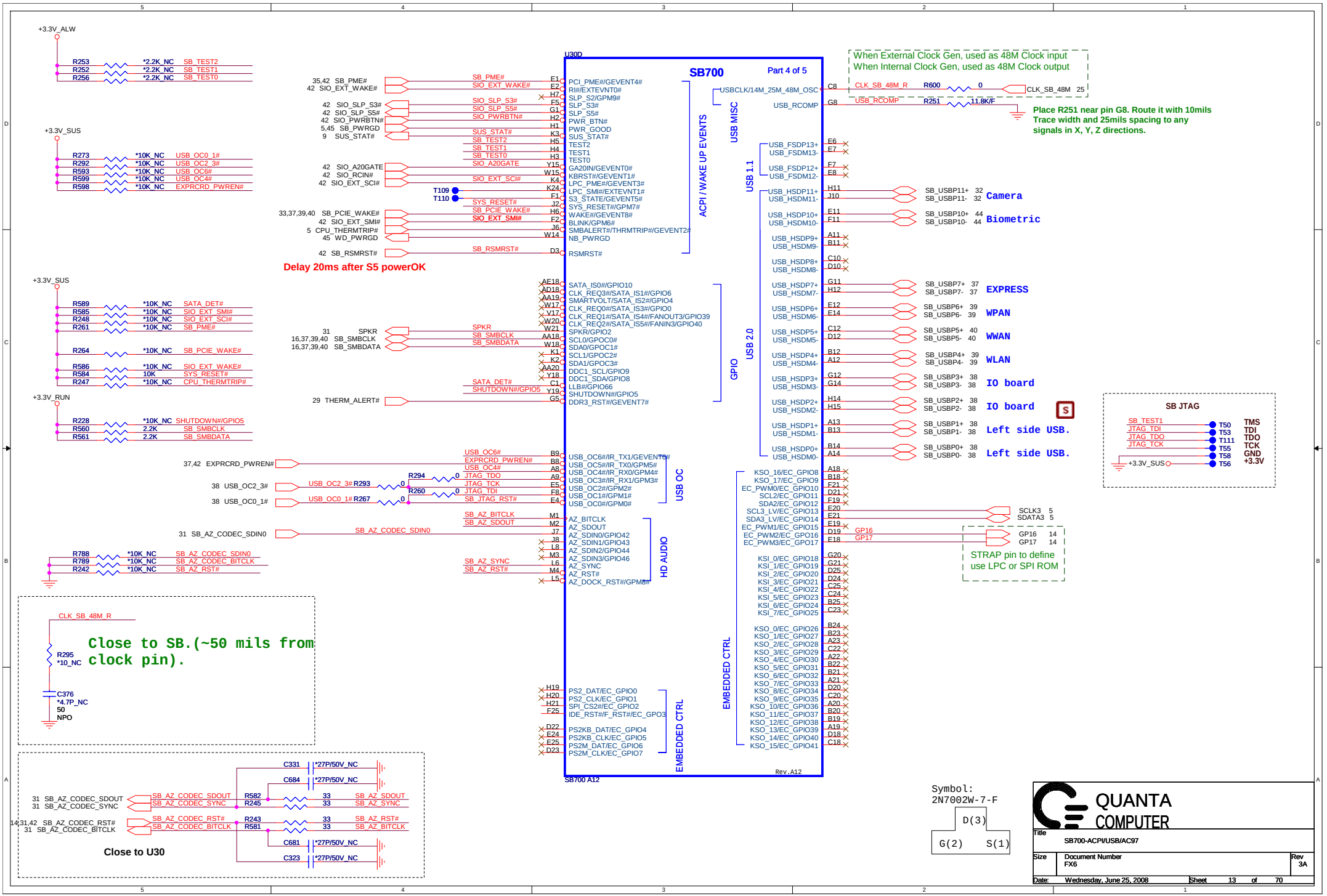
SB700
Part 4 of 5
U30D
SB700 A12
Rev.A12
When External Clock Gen, used as 48M Clock input
When Internal Clock Gen, used as 48M Clock output
Place R251 near pin G8. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
Delay 20ms after S5 powerOK
Camera
Biometric
EXPRESS
WPAN
WWAN
WLAN
IO board
IO board
Left side USB.
Left side USB.
SB JTAG
TMS
TDI
TDO
TCK
GND
+3.3V
STRAP pin to define use LPC or SPI ROM
Close to SB.(~50 mils from clock pin).
Close to U30
Symbol: 2N7002W-7-F
QUANTA COMPUTER
SB700-ACPI/USB/AC97
Document Number FX6
Rev 3A
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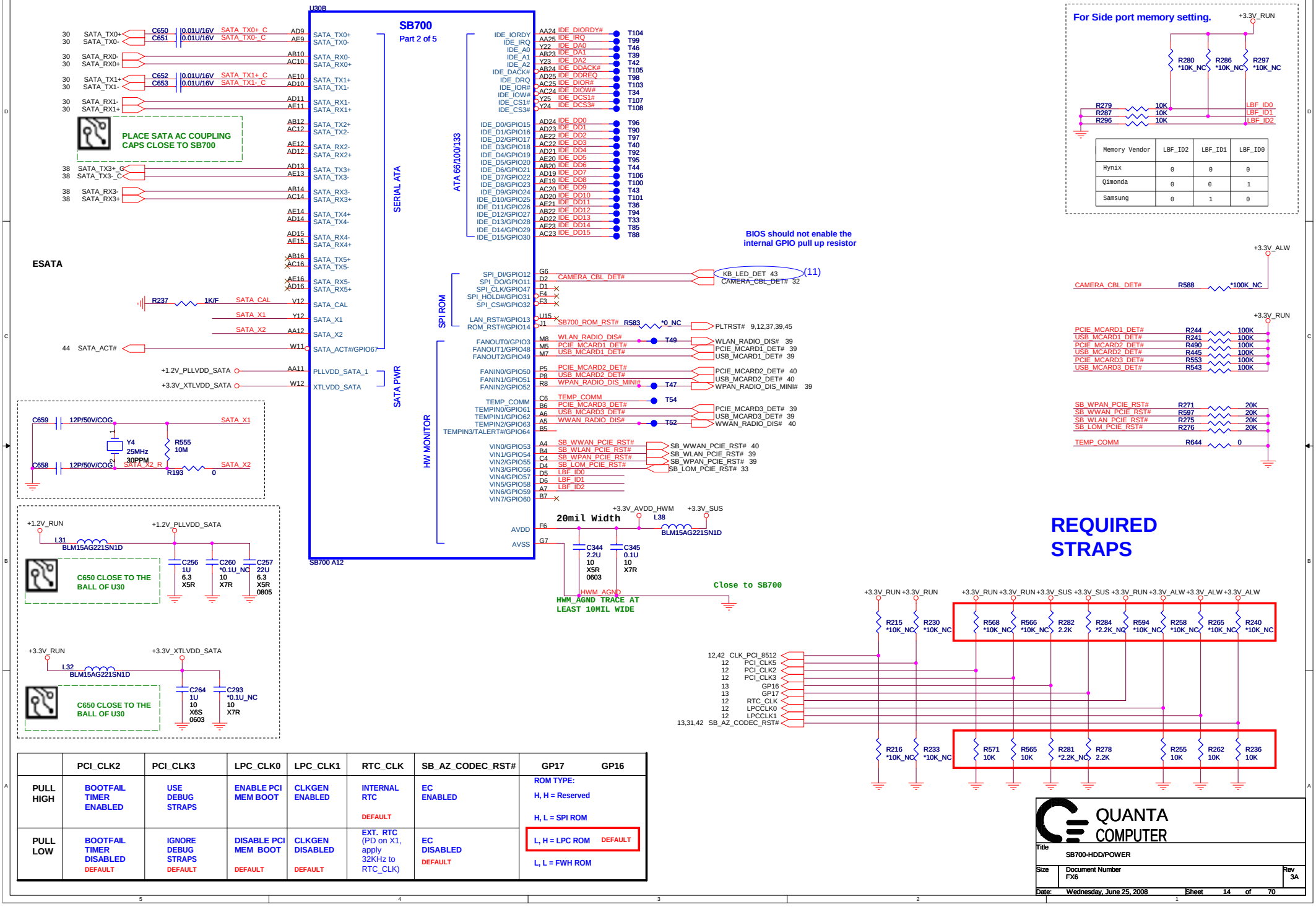
SB700
Part 2 of 5
U30B
SB700 A12
SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR
ESATA
PLACE SATA AC COUPLING CAPS CLOSE TO SB700
BIOS should not enable the internal GPIO pull up resistor
For Side port memory setting.
Memory Vendor | LBF_ID2 | LBF_ID1 | LBF_ID0
Hynix | 0 | 0 | 0
Qimonda | 0 | 0 | 1
Samsung | 0 | 1 | 0
REQUIRED STRAPS
C650 CLOSE TO THE BALL OF U30
C650 CLOSE TO THE BALL OF U30
20mil Width
Close to SB700
HWM_AGND TRACE AT LEAST 10MIL WIDE
PULL HIGH
PULL LOW
BOOTFAIL TIMER ENABLED
USE DEBUG STRAPS
ENABLE PCI MEM BOOT
CLKGEN ENABLED
INTERNAL RTC
EC ENABLED
BOOTFAIL TIMER DISABLED
IGNORE DEBUG STRAPS
DISABLE PCI MEM BOOT
CLKGEN DISABLED
EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)
EC DISABLED
ROM TYPE:
H, H = Reserved
H, L = SPI ROM
L, H = LPC ROM
L, L = FWH ROM
QUANTA COMPUTER
SB700-HDD/POWER
Document Number FX6
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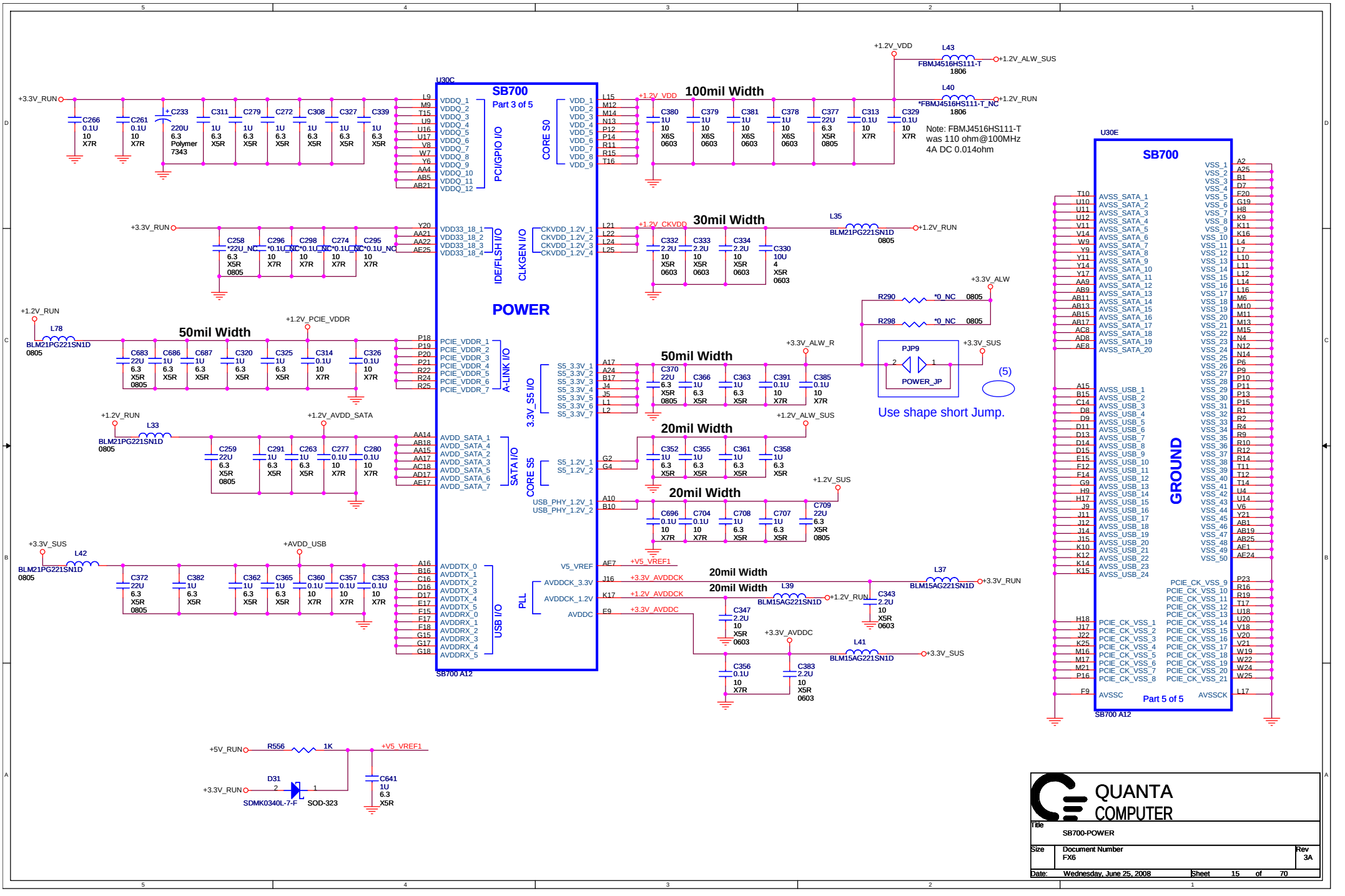
U30C
SB700
Part 3 of 5
POWER
SB700 A12
100mil Width
30mil Width
50mil Width
20mil Width
20mil Width
20mil Width
Note: FBMJ4516HS111-T was 110 ohm@100MHz 4A DC 0.014ohm
Use shape short Jump.
U30E
SB700
GROUND
Part 5 of 5
SB700 A12
QUANTA COMPUTER
Title
SB700-POWER
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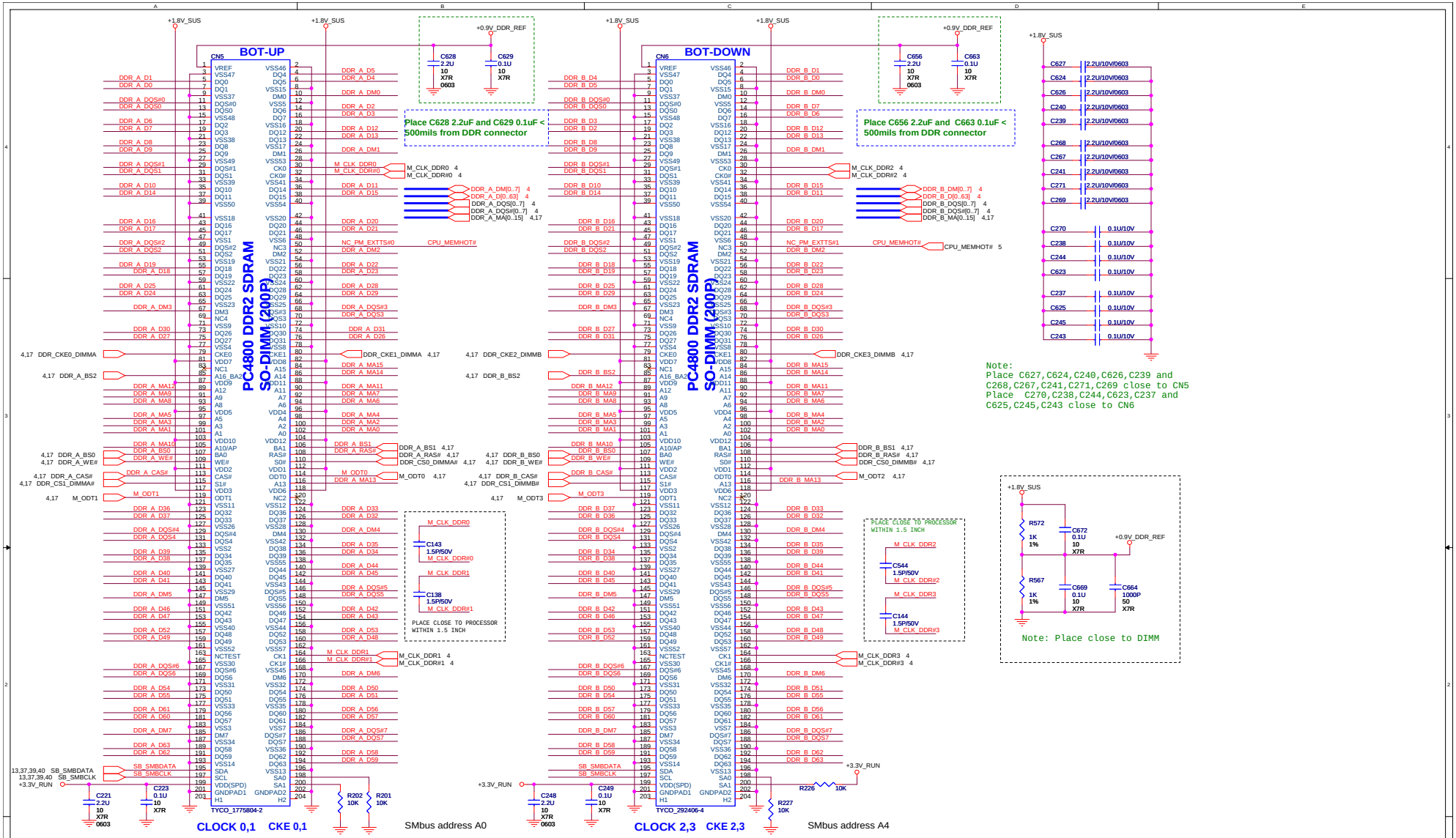
BOT-UP
CN5
PC4800 DDR2 SDRAM SO-DIMM (200P)
TYCO_1775804-2
CLOCK 0,1 CKE 0,1
SMbus address A0
Place C628 2.2uF and C629 0.1uF < 500mils from DDR connector
Place C656 2.2uF and C663 0.1uF < 500mils from DDR connector
BOT-DOWN
CN6
PC4800 DDR2 SDRAM SO-DIMM (200P)
TYCO_292406-4
CLOCK 2,3 CKE 2,3
SMbus address A4
Note:
Place C627,C624,C240,C626,C239 and C268,C267,C241,C271,C269 close to CN5
Place C270,C238,C244,C623,C237 and C625,C245,C243 close to CN6
Note: Place close to DIMM
PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH
QUANTA COMPUTER
DDRII SODIMMX2
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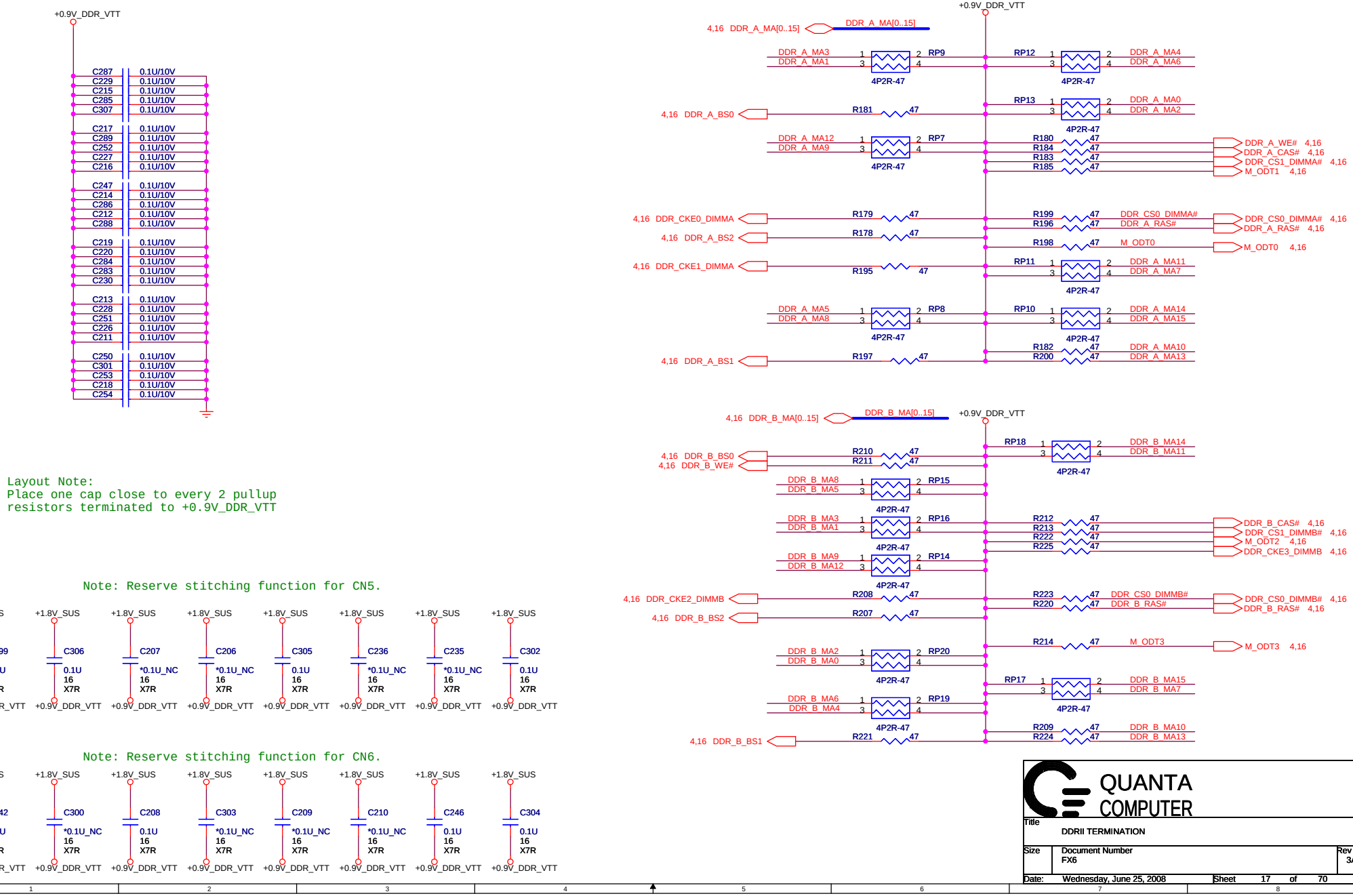
+0.9V_DDR_VTT
C287 0.1U/10V
C229 0.1U/10V
C215 0.1U/10V
C285 0.1U/10V
C307 0.1U/10V
C217 0.1U/10V
C289 0.1U/10V
C252 0.1U/10V
C227 0.1U/10V
C216 0.1U/10V
C247 0.1U/10V
C214 0.1U/10V
C286 0.1U/10V
C212 0.1U/10V
C288 0.1U/10V
C219 0.1U/10V
C220 0.1U/10V
C284 0.1U/10V
C283 0.1U/10V
C230 0.1U/10V
C213 0.1U/10V
C228 0.1U/10V
C251 0.1U/10V
C226 0.1U/10V
C211 0.1U/10V
C250 0.1U/10V
C301 0.1U/10V
C253 0.1U/10V
C218 0.1U/10V
C254 0.1U/10V
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT
Note: Reserve stitching function for CN5.
+1.8V_SUS
C299 0.1U 16 X7R
C306 0.1U 16 X7R
C207 *0.1U_NC 16 X7R
C206 *0.1U_NC 16 X7R
C305 0.1U 16 X7R
C236 *0.1U_NC 16 X7R
C235 *0.1U_NC 16 X7R
C302 0.1U 16 X7R
+0.9V_DDR_VTT
Note: Reserve stitching function for CN6.
+1.8V_SUS
C242 0.1U 16 X7R
C300 *0.1U_NC 16 X7R
C208 0.1U 16 X7R
C303 *0.1U_NC 16 X7R
C209 *0.1U_NC 16 X7R
C210 *0.1U_NC 16 X7R
C246 0.1U 16 X7R
C304 0.1U 16 X7R
+0.9V_DDR_VTT
4,16 DDR_A_MA[0..15]
DDR_A_MA[0..15]
DDR_A_MA3
DDR_A_MA1
RP9
4P2R-47
RP12
DDR_A_MA4
DDR_A_MA6
RP13
DDR_A_MA0
DDR_A_MA2
4,16 DDR_A_BS0
R181 47
DDR_A_MA12
DDR_A_MA9
RP7
R180 47
R184 47
R183 47
R185 47
DDR_A_WE# 4,16
DDR_A_CAS# 4,16
DDR_CS1_DIMMA# 4,16
M_ODT1 4,16
4,16 DDR_CKE0_DIMMA
R179 47
R199 47
R196 47
DDR_CS0_DIMMA# 4,16
DDR_A_RAS# 4,16
4,16 DDR_A_BS2
R178 47
R198 47
M_ODT0 4,16
4,16 DDR_CKE1_DIMMA
R195 47
RP11
DDR_A_MA11
DDR_A_MA7
DDR_A_MA5
DDR_A_MA8
RP8
RP10
DDR_A_MA14
DDR_A_MA15
R182 47
R200 47
DDR_A_MA10
DDR_A_MA13
4,16 DDR_A_BS1
R197 47
4,16 DDR_B_MA[0..15]
DDR_B_MA[0..15]
RP18
DDR_B_MA14
DDR_B_MA11
4,16 DDR_B_BS0
4,16 DDR_B_WE#
R210 47
R211 47
DDR_B_MA8
DDR_B_MA5
RP15
DDR_B_MA3
DDR_B_MA1
RP16
R212 47
R213 47
R222 47
R225 47
DDR_B_CAS# 4,16
DDR_CS1_DIMMB# 4,16
M_ODT2 4,16
DDR_CKE3_DIMMB 4,16
DDR_B_MA9
DDR_B_MA12
RP14
4,16 DDR_CKE2_DIMMB
R208 47
R223 47
R220 47
DDR_CS0_DIMMB# 4,16
DDR_B_RAS# 4,16
4,16 DDR_B_BS2
R207 47
R214 47
M_ODT3 4,16
DDR_B_MA2
DDR_B_MA0
RP20
RP17
DDR_B_MA15
DDR_B_MA7
DDR_B_MA6
DDR_B_MA4
RP19
R209 47
R224 47
DDR_B_MA10
DDR_B_MA13
4,16 DDR_B_BS1
R221 47
QUANTA COMPUTER
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DDRII TERMINATION
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Title: Blank Page		
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Date: Tuesday, June 03, 2008	Sheet 18 of 70	

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Date: Tuesday, June 03, 2008	Sheet 19 of 70	

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Title	Blank Page	
Size: Custom	Document Number: FX6	Rev: 3A
Date: Tuesday, June 03, 2008	Sheet 20 of 70	

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Title	Blank Page	
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600 ohm +-25%@100MHz
25m ohm max DC resistance
1A current rating

Place Decoupling Cap close to GROUP1 each VDD pin as possibble.

+3.3V_CLK(40 mils)

Place Decoupling Cap close to GROUP2 each VDD pin as possibble.

+3.3V_CLK(40 mils)

Need check footprint

Place Decoupling Cap close to each VDD pin as possibble.

Parallel Resonance Crystal

QFN64

SLG8SP628VTR(QFN)

SMbus address D2

These are for backdrive issue.

SEL_HTT66	1	Pin54/53: 66MHz 3.3V single ended HTT clock
	0	Pin54/53: 100MHz differential HTT clock
SEL_SATA	1	Pin42/41: 100MHz No_SSC-Differential SATA clock
	0	Pin42/41: 100MHz SRC clock
SEL_27	1	Pin6/5: 27 MHz / 27_SSC MHz
	0	Pin6/5: 100MHz SRC clock

	OSC 14M_NB		
	LEVEL	R607	R637
RX780	+1.8V	82R	130R
RS780	+1.1V	158R	90.9R

QUANTA COMPUTER

Title	CLOCK GENERATOR	
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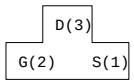
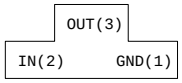
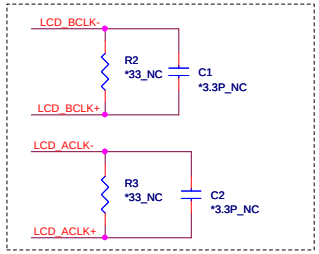
Symbol:
2N7002W-7-F

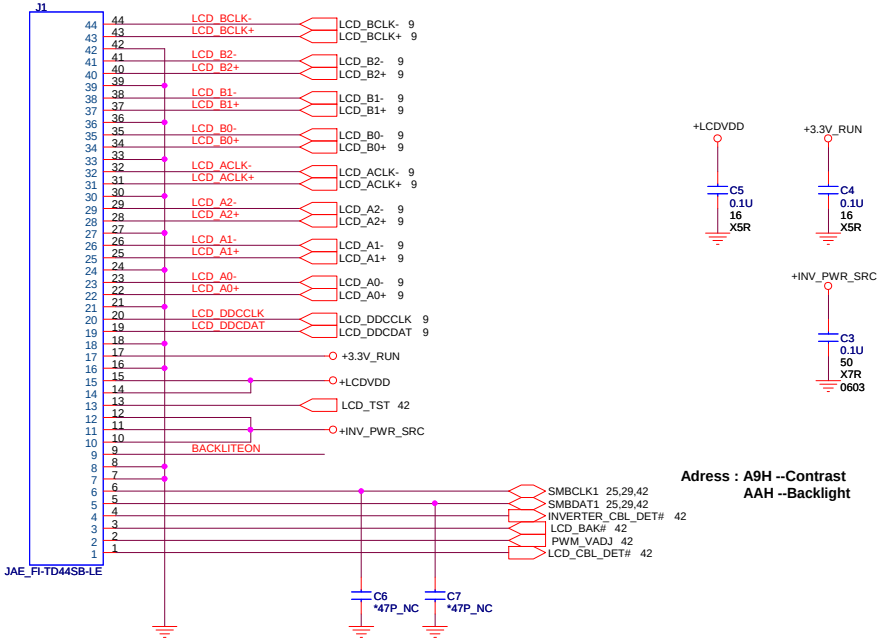


Symbol:
DTC124EUA



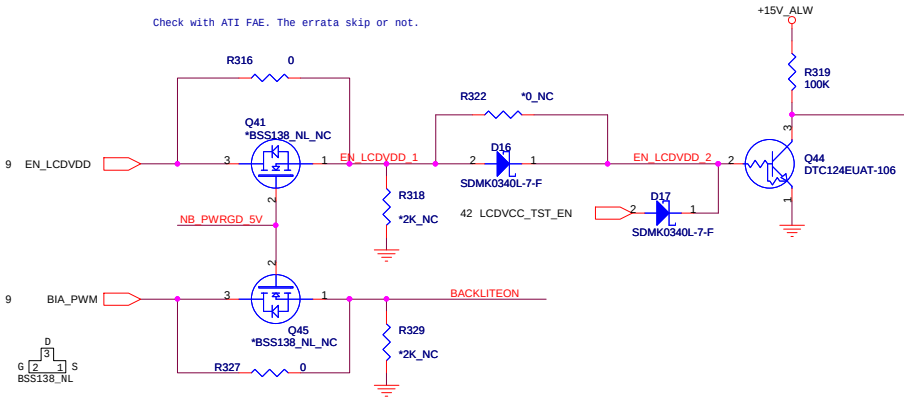
Design current: 560mA
Max current: 800mA

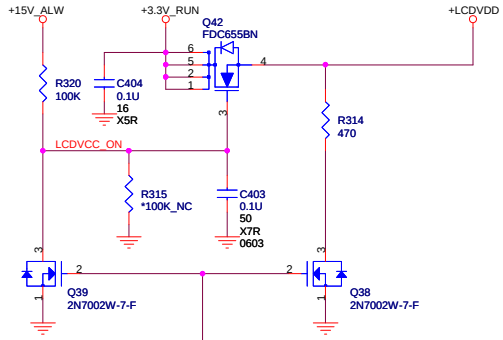


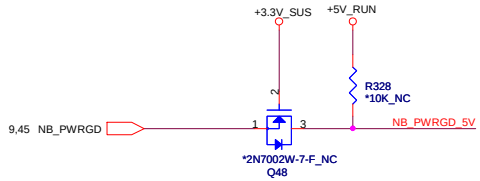


Adress : A9H --Contrast
AAH --Backlight

Check with ATI FAE. The errata skip or not.







QUANTA COMPUTER

Title	LCD CONN,CK-SSCD	
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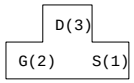
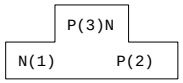
Symbol:
BSS138_NL



Symbol:
DA204U



QUANTA COMPUTER

Title	CRT CONN	
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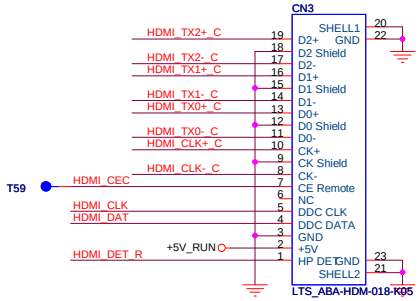
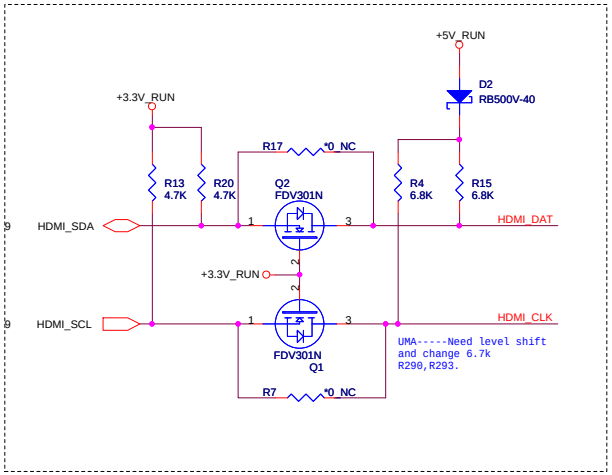
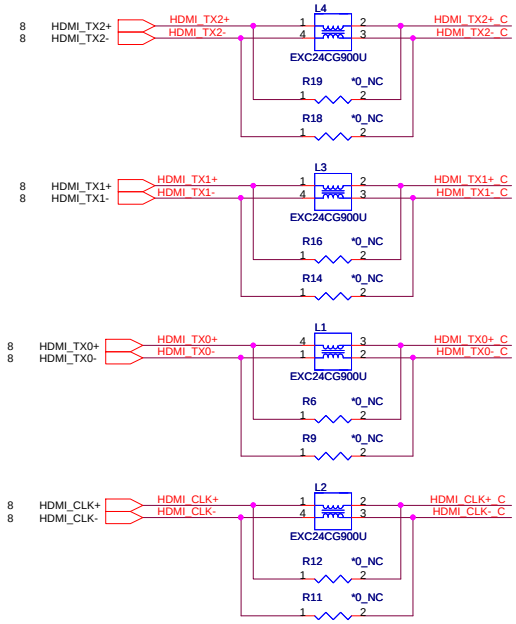
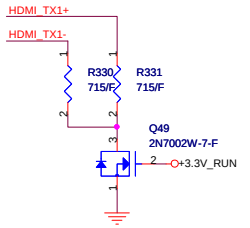
HDMI Connector

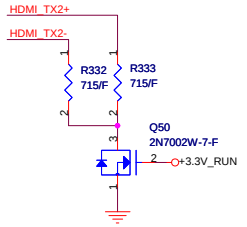


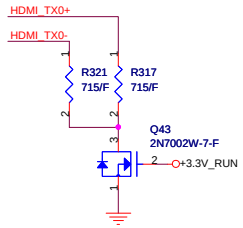


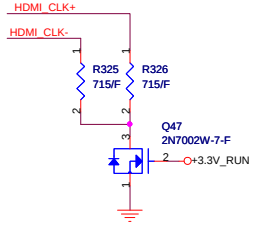


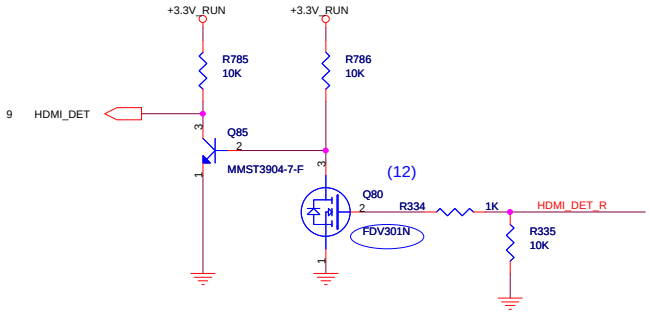
for EMI











QUANTA COMPUTER		
Title: HDMI		
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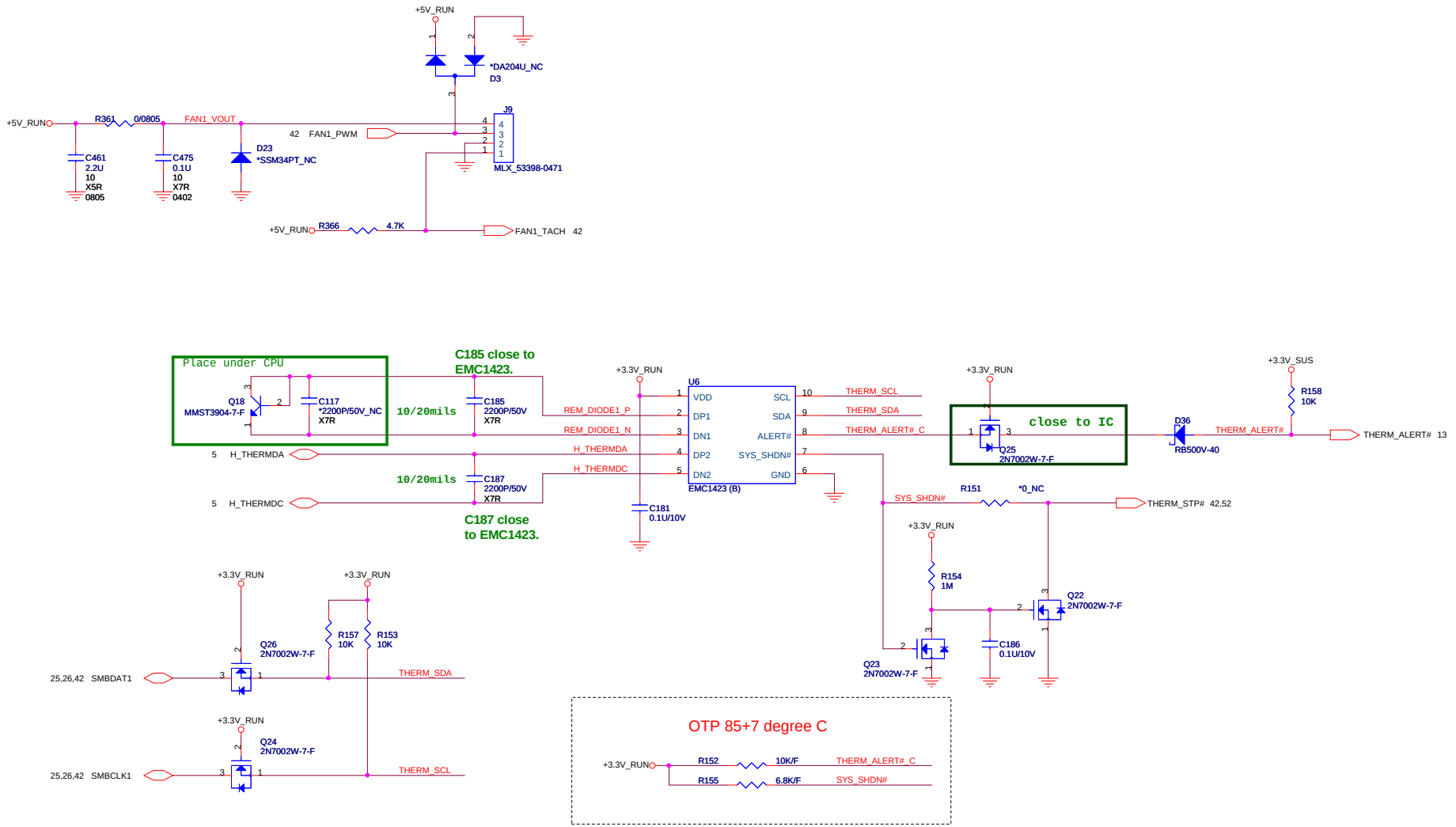

QUANTA COMPUTER

Title	FAN/THERMAL	
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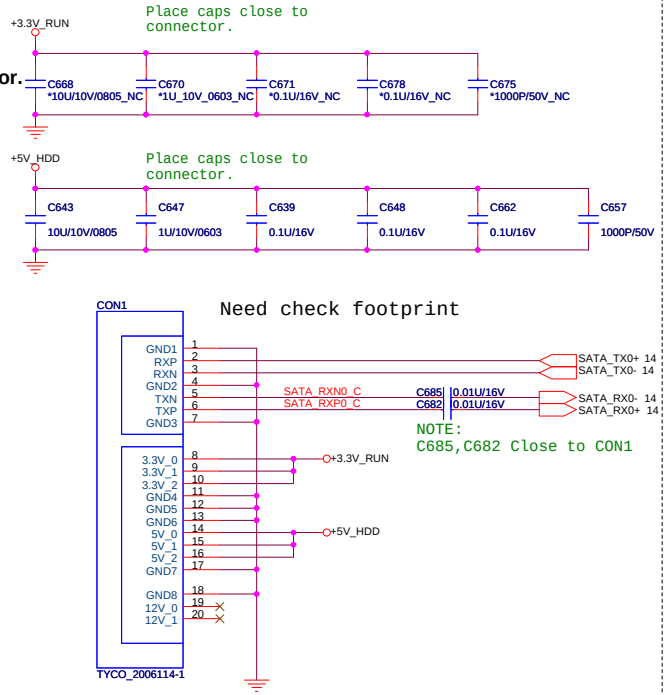
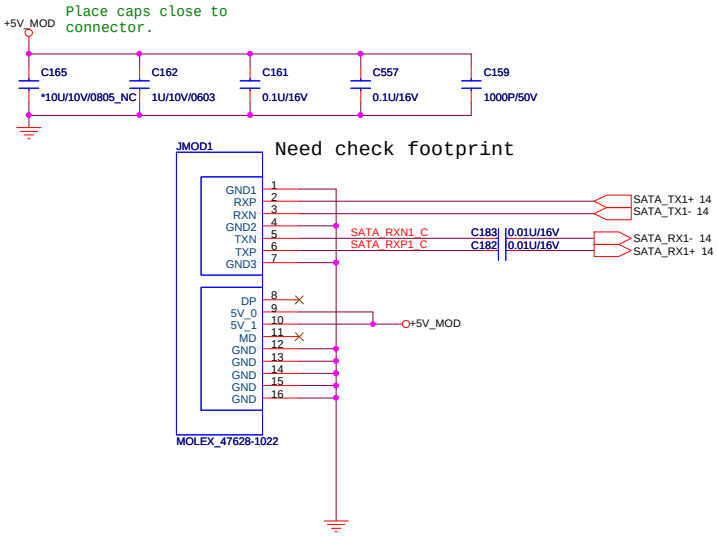
SATA Connector.

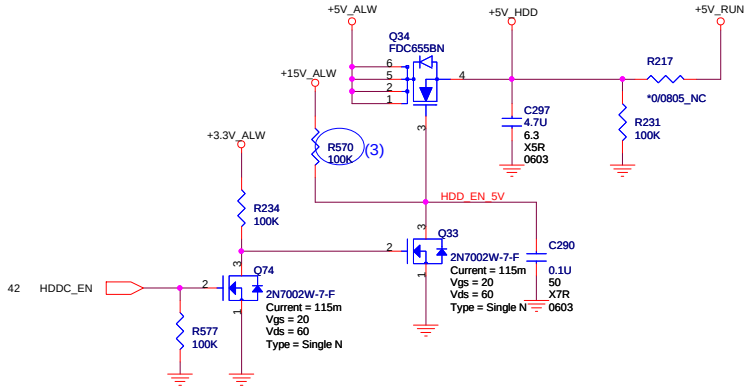


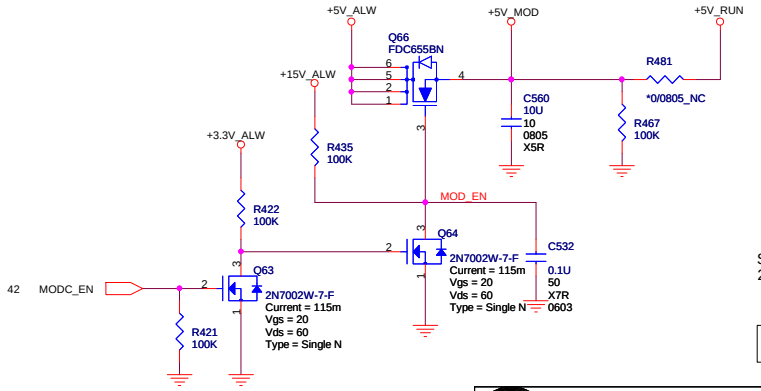
ODD Connector.



Design current: 1050mA
Max current: 1500mA

Design current: 700mA
Max current: 1000mA





Symbol:
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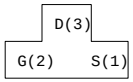

QUANTA COMPUTER

Title	SATA (HDD&CD_ROM)	
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INTERNAL SPEAKER AMP

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

	TPA6040	MAX9789
C719	Pop	Depop
R609	Depop	Pop

AZALIA (HD) CODEC

	TPA6040	MAX9789
C723	Pop	Depop
R616	Depop	Pop

Depop R606,C717 for using 92HD73C

Depop R629, R627, R607,R634
Pop R635, R612, R626 ,R636
for using 92HD73C
R627,R635 close to U32, Let DVDD width be 10-mils

Close to U32.

QUANTA COMPUTER

Title: AZALIA(HD) CODEC

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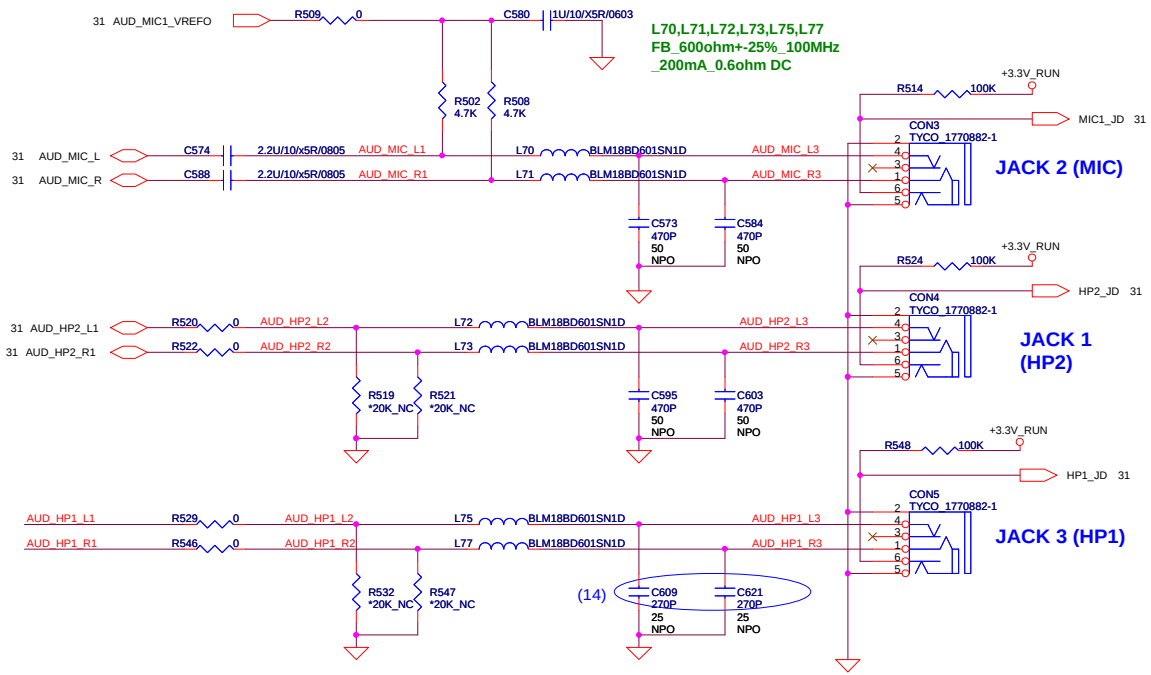
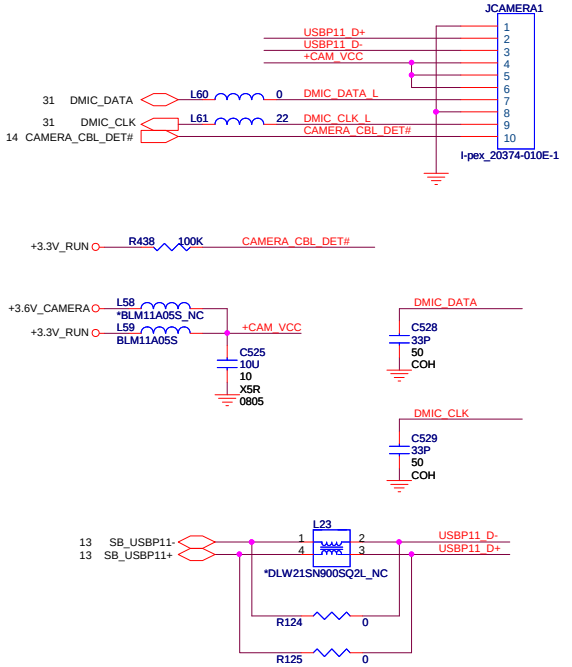
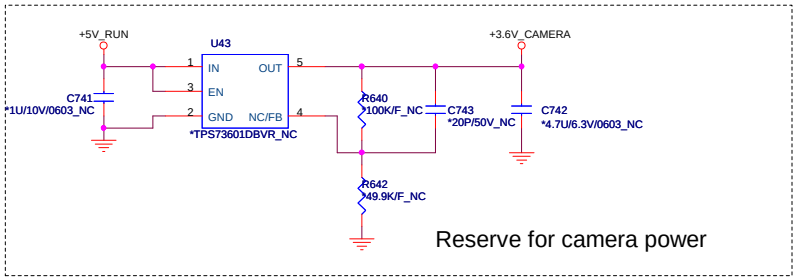
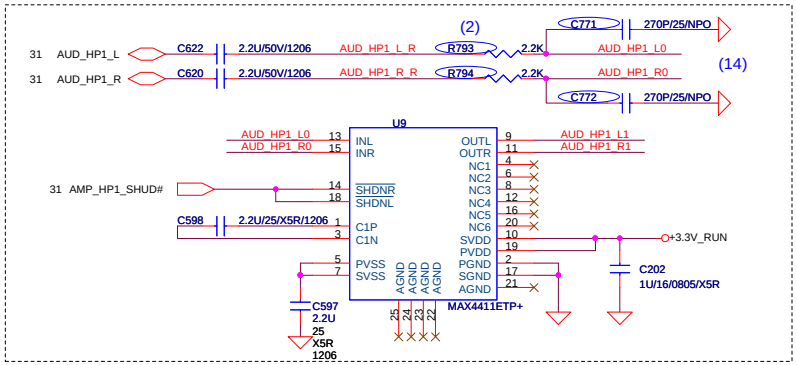
Headphone Jack
Stereo MIC Jack

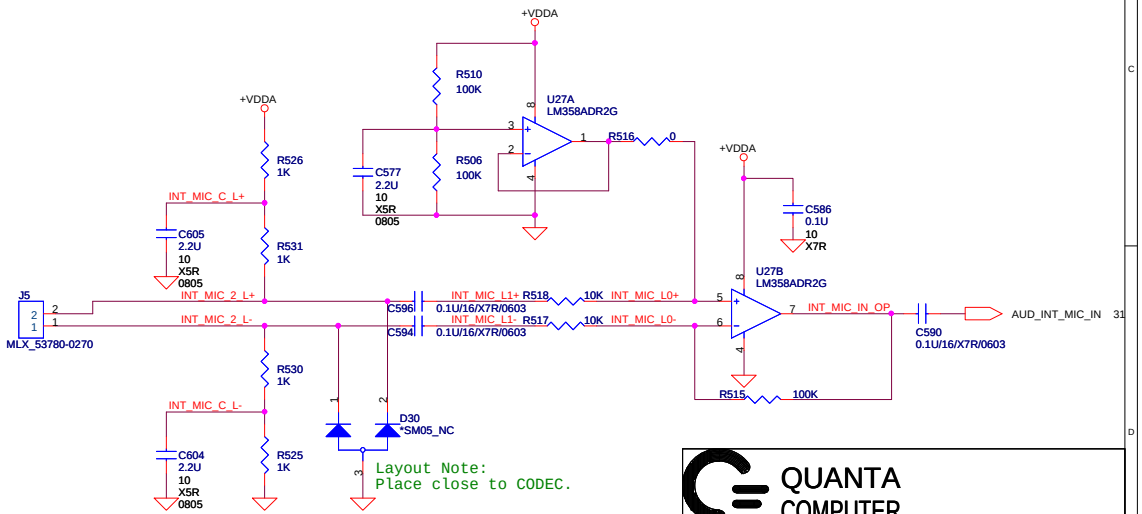


Array Microphone & Camera









QUANTA COMPUTER

Title	AUDIO CONN	
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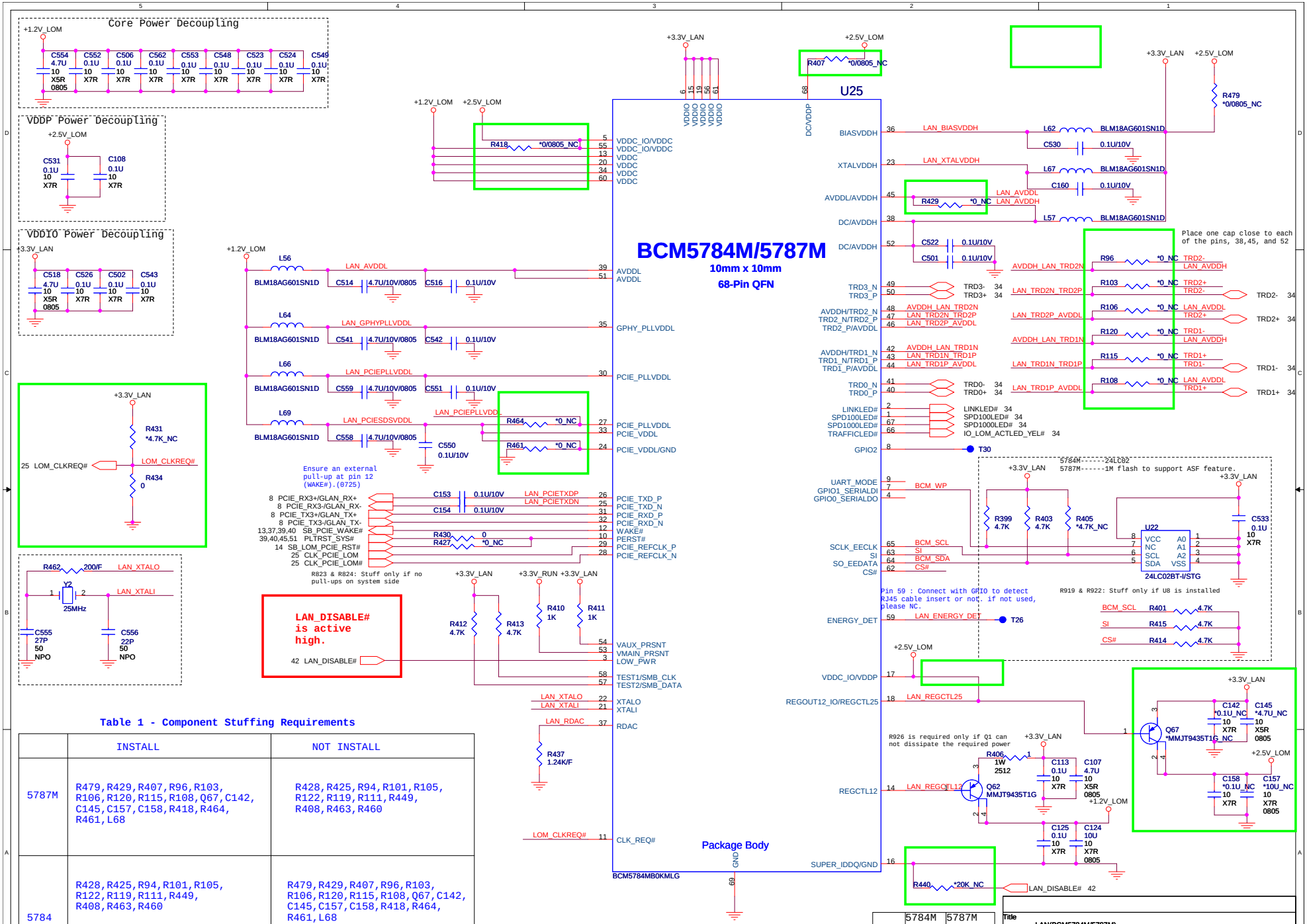

Table 1 - Component Stuffing Requirements

	INSTALL	NOT INSTALL
5787M	R479,R429,R407,R96,R103, R106,R120,R115,R108,Q67,C142, C145,C157,C158,R418,R464, R461,L68	R428,R425,R94,R101,R105, R122,R119,R111,R449, R408,R463,R460
5784	R428,R425,R94,R101,R105, R122,R119,R111,R449, R408,R463,R460	R479,R429,R407,R96,R103, R106,R120,R115,R108,Q67,C142, C145,C157,C158,R418,R464, R461,L68

	5784M	5787M
R439	39k	0
R440	20k	*20k_NC

Title	LAN(BCM5784M/5787M)
Size	Custom
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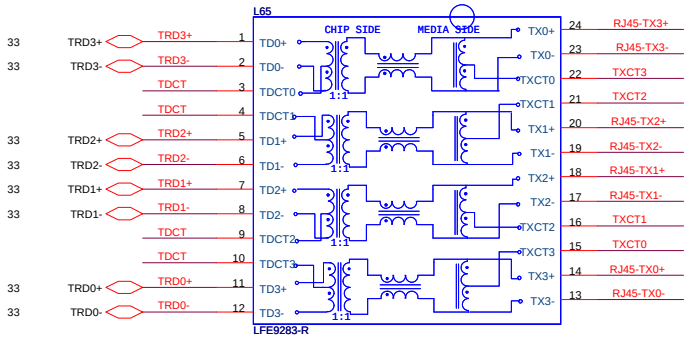
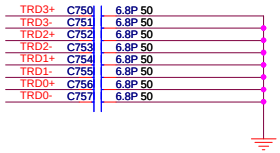
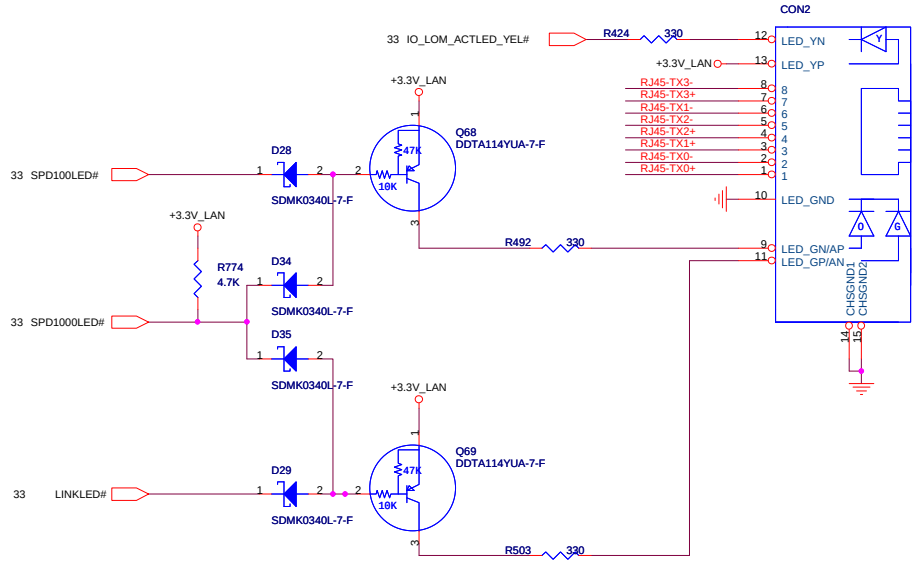
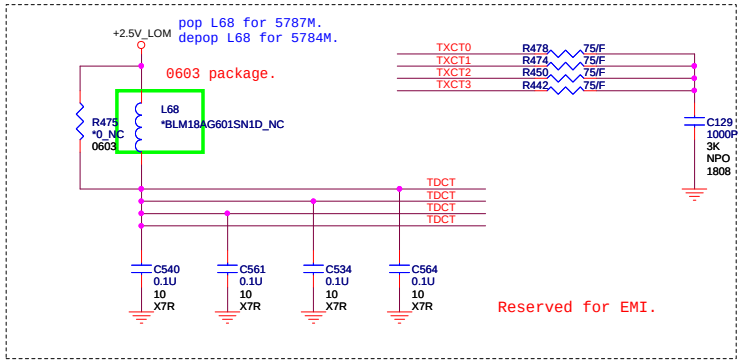
RJ-45 Connector

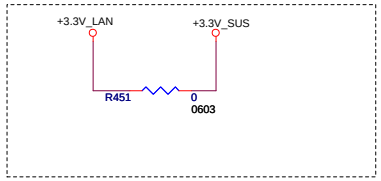
TRANSFORM











QUANTA COMPUTER

Title	LAN SWITCH		
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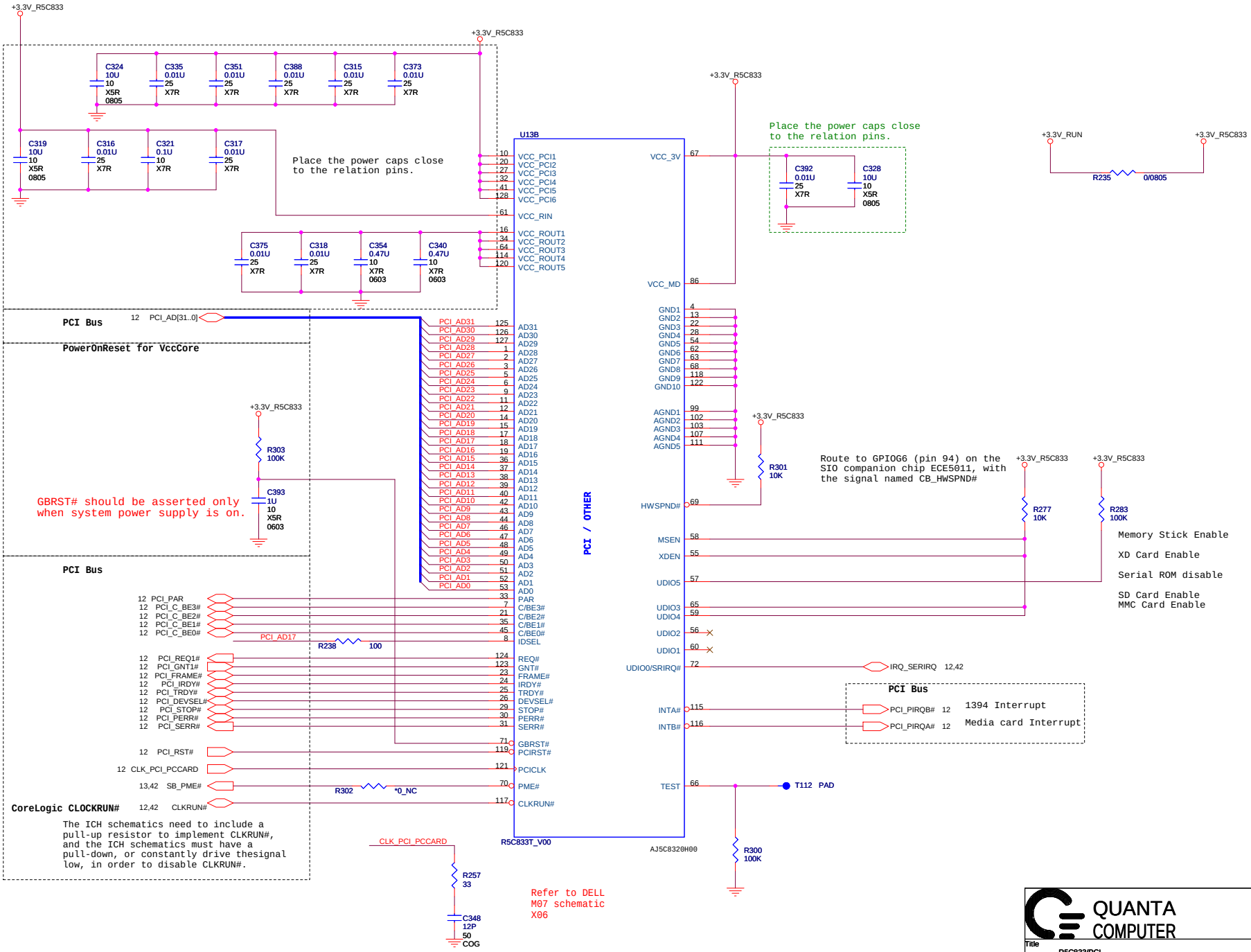
+3.3V_R5C833
C324 10U 10 X5R 0805
C335 0.01U 25 X7R
C351 0.01U 25 X7R
C388 0.01U 25 X7R
C315 0.01U 25 X7R
C373 0.01U 25 X7R
C319 10U 10 X5R 0805
C316 0.01U 25 X7R
C321 0.1U 10 X7R
C317 0.01U 25 X7R
Place the power caps close to the relation pins.
C375 0.01U 25 X7R
C318 0.01U 25 X7R
C354 0.47U 10 X7R 0603
C340 0.47U 10 X7R 0603
U13B
VCC_PCI1
VCC_PCI2
VCC_PCI3
VCC_PCI4
VCC_PCI5
VCC_PCI6
VCC_RIN
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5
VCC_3V
VCC_MD
C392 0.01U 25 X7R
C328 10U 10 X5R 0805
Place the power caps close to the relation pins.
+3.3V_RUN
R235 0/0805
PCI Bus
12 PCI_AD[31..0]
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
PCI / OTHER
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
AGND1
AGND2
AGND3
AGND4
AGND5
+3.3V_R5C833
R301 10K
PowerOnReset for VccCore
+3.3V_R5C833
R303 100K
C393 1U 10 X5R 0603
GBRST# should be asserted only when system power supply is on.
Route to GPIOG6 (pin 94) on the SIO companion chip ECE5011, with the signal named CB_HWSPND#
HWSPND#
+3.3V_R5C833
R277 10K
+3.3V_R5C833
R283 100K
MSEN
XDEN
UDIO5
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SRIRQ#
Memory Stick Enable
XD Card Enable
Serial ROM disable
SD Card Enable
MMC Card Enable
IRQ_SERIRQ 12,42
PCI Bus
INTA#
INTB#
PCI_PIRQB# 12
PCI_PIRQA# 12
1394 Interrupt
Media card Interrupt
PCI Bus
12 PCI_PAR
12 PCI_C_BE3#
12 PCI_C_BE2#
12 PCI_C_BE1#
12 PCI_C_BE0#
PCI_AD17
R238 100
PAR
C/BE3#
C/BE2#
C/BE1#
C/BE0#
IDSEL
12 PCI_REQ1#
12 PCI_GNT1#
12 PCI_FRAME#
12 PCI_IRDY#
12 PCI_TRDY#
12 PCI_DEVSEL#
12 PCI_STOP#
12 PCI_PERR#
12 PCI_SERR#
REQ#
GNT#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PERR#
SERR#
12 PCI_RST#
12 CLK_PCI_PCCARD
13,42 SB_PME#
R302 *0_NC
12,42 CLKRUN#
GBRST#
PCIRST#
PCICLK
PME#
CLKRUN#
CoreLogic CLOCKRUN#
The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive thesignal low, in order to disable CLKRUN#.
CLK_PCI_PCCARD
R257 33
C348 12P 50 COG
R5C833T_V00
AJ5C8320H00
TEST
T112 PAD
R300 100K
Refer to DELL M07 schematic X06
QUANTA COMPUTER
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R5C833/PCI
Size
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FX6
Rev
3A
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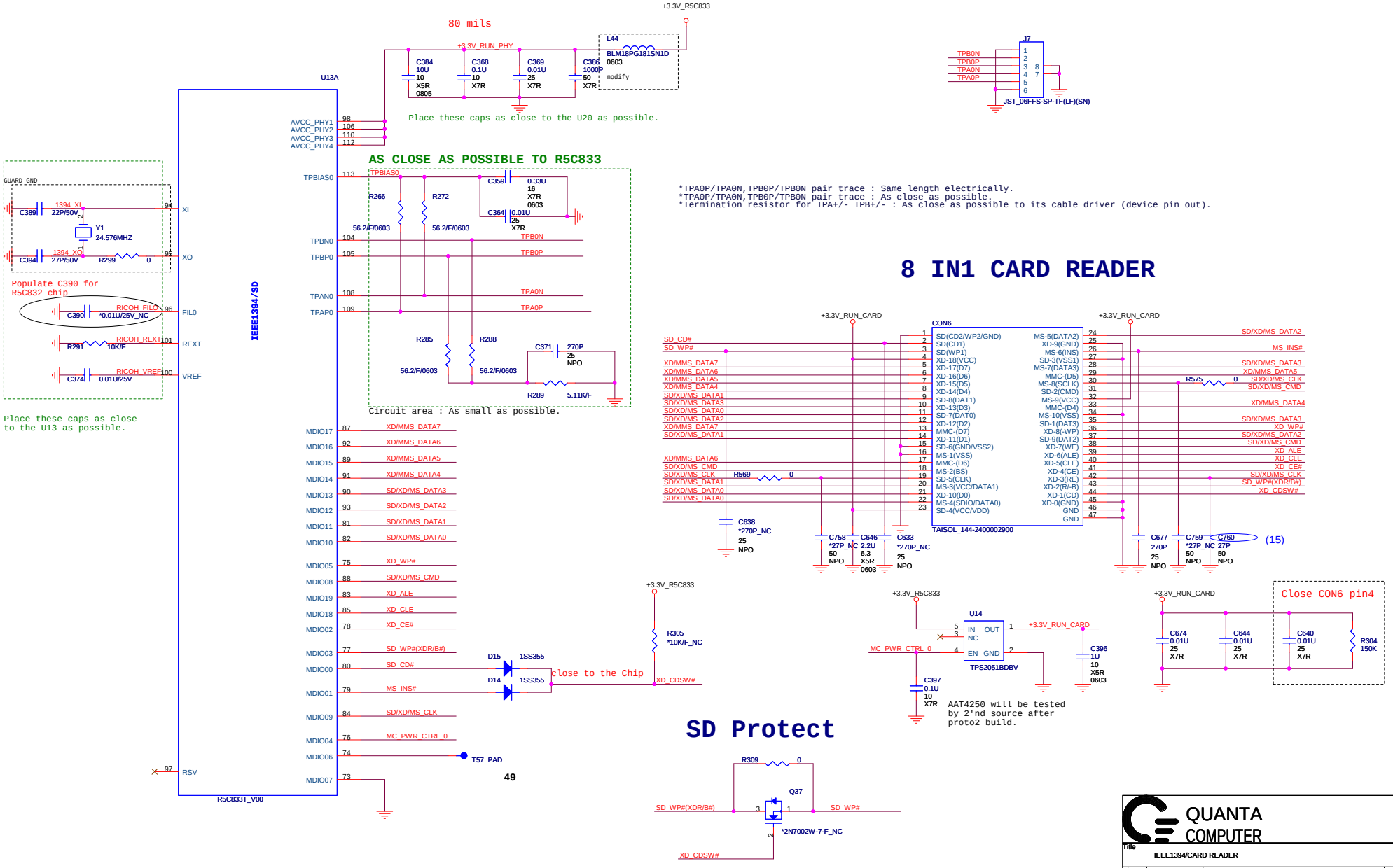

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Title	IEEE1394/CARD READER	
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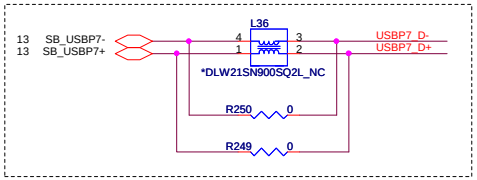
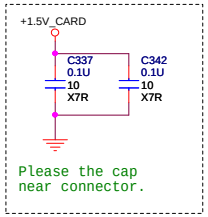
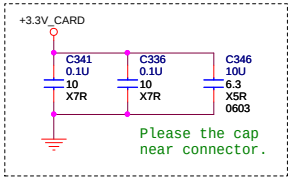
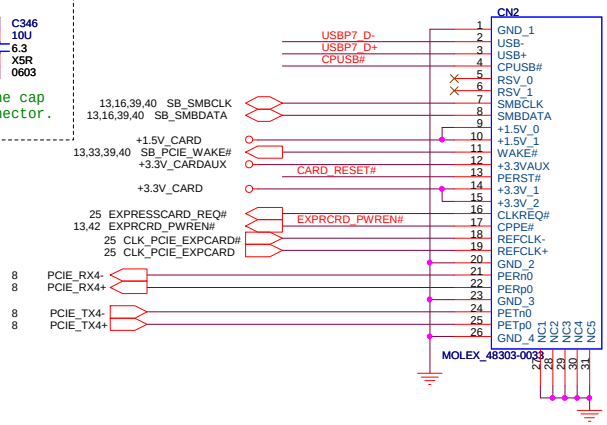
Express Card



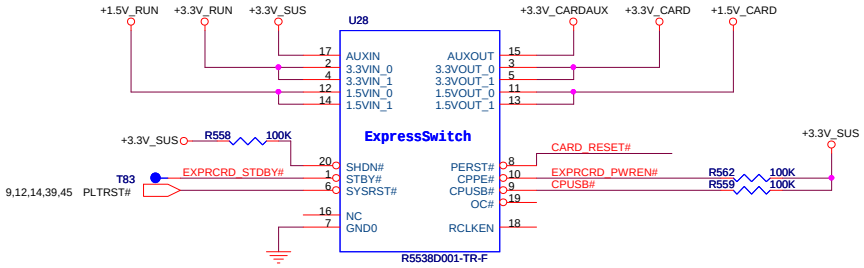


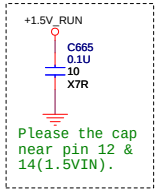


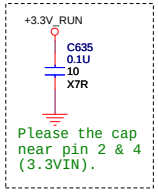


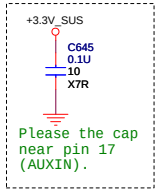
PCI-Express TX and RX direct to connector.

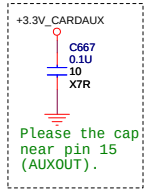
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

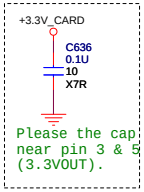


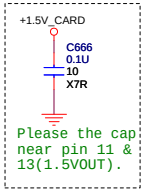












QUANTA COMPUTER

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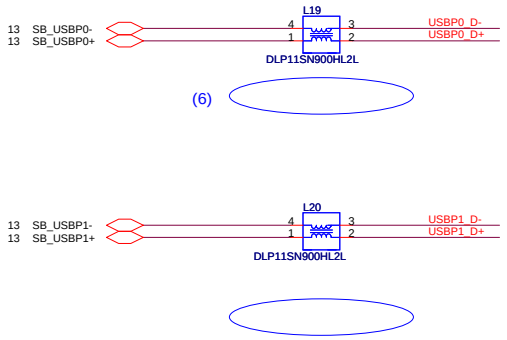
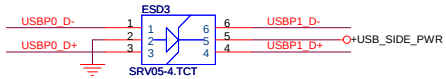
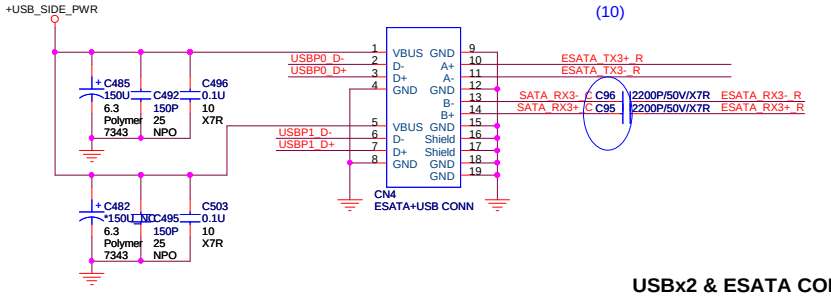
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



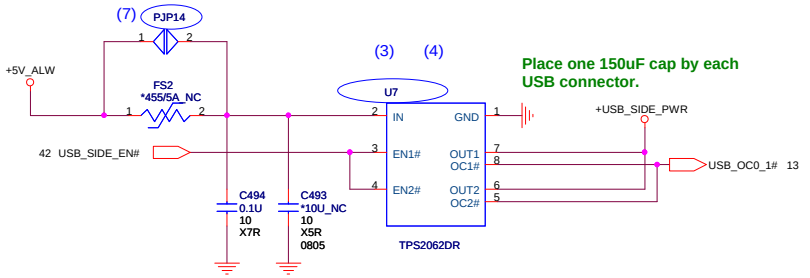
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

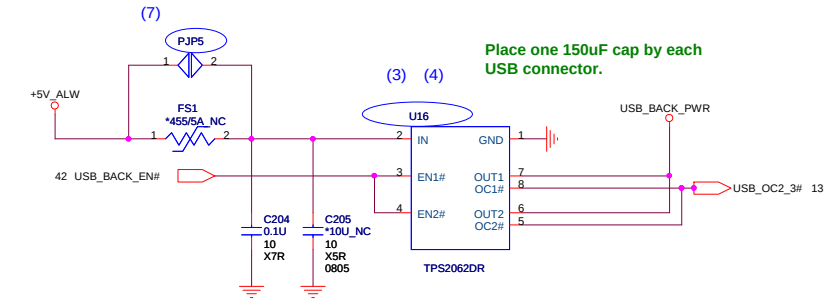


Side External USBX2

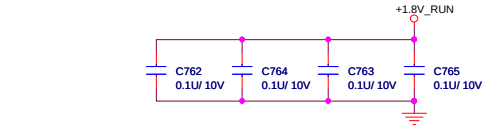


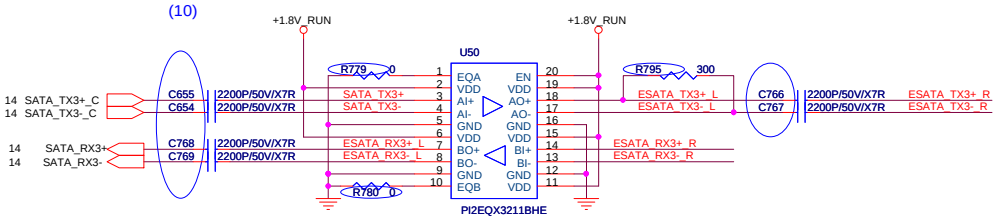
USBx2 & ESATA COMBO

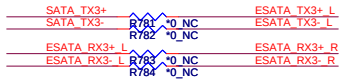




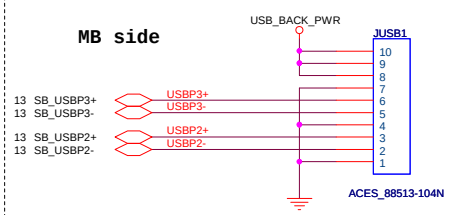
E-SATA Re-driver







MB side



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MiniCard WLAN connector

TH21 H-TC118BC197D63P2
TH22 H-TC118BC197D63P2

J12
LTS_AAA-PCI-041-K01

13,33,37,40 SB_PCIE_WAKE#
COEX2_WLAN_ACTIVE
COEX1_BT_ACTIVE_MINI
25 MINI1CLK_REQ#
MINI1CLK_REQ#
25 CLK_PCIE_MINI1#
25 CLK_PCIE_MINI1
C637 220P 50 X7R
8 PCIE_RX1-
8 PCIE_RX1+
8 PCIE_TX1-
8 PCIE_TX1+
14 PCIE_MCARD1_DET#
PCI-Express TX and RX direct to connector

Non-iAMT
T87 PAD
T86 PAD
T81 PAD
RSV_ICH_CL_CLK1
RSV_ICH_CL_DATA1
RSV_ICH_CL_RST1#

R173 0 PLTRST_SYS# 33,40,45,51
R176 *0_NC WLAN_RADIO_OFF#
SB_WLAN_PCIE_RST# 14
WLAN_SMBCLK
WLAN_SMBDATA
USBP4_D-
USBP4_D+
USB_MCARD1_DET#
USB_MCARD1_DET# 14
LED_WLAN_OUT# 44

USBP4_D-
USBP4_D+
L74 *DLW21SN900SQ2L_NC
SB_USBP4- 13
SB_USBP4+ 13
R528 0
R527 0
Layout Note: R528 and R527 close to choke as possible to minimize stubs.

+3.3V_WLAN
RP6 4P2R-2.2K
WLAN_SMBCLK
Q29 *2N7002W-7-F_NC
SB_SMBCLK 13,16,37,40
R446 *0_NC
WLAN_SMBDATA
Q30 *2N7002W-7-F_NC
SB_SMBDATA 13,16,37,40
R174 *0_NC

Suport for WoW

WLAN_RADIO_OFF#
D13 SDMK0340L-7-F
WLAN_RADIO_DIS# 14
R170 *0_NC
Prevent backdrive when WoW is enabled.

DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

+3.3V_WLAN
+3.3V_RUN
R557 0_0805

Place caps close to connector.
C619 0.1U 10 X7R
C608 0.047U 10 X7R
C613 0.1U 10 X7R
C612 0.047U 10 X7R
C606 4.7U 10 X5R 0805
C642 *330U_NC 6.3 POSCAP 7343
+1.5V_RUN
C610 0.047U 10 X7R
C611 0.047U 10 X7R

+PWR_SRC
R175 *100K_NC
R171 *100K_NC
+3.3V_ALW
+3.3V_WLAN
Q27 *SI3456DV_NC
WLAN_ENABLE
Q28A
Q28B
*2N7002DW-7-F_NC
42 AUX_EN_WOWL
R177 *100K_NC
R172 *200K_NC
R169 *470K_NC
C203 *4700P_NC 50 X7R 0603

MiniCard WPAN connector

J11
LTS_AAA-PCI-041-K01

13,33,37,40 SB_PCIE_WAKE#
COEX2_WLAN_ACTIVE
COEX1_BT_ACTIVE_MINI
25 MINI2CLK_REQ#
MINI2CLK_REQ#
25 CLK_PCIE_MINI2#
25 CLK_PCIE_MINI2
COEX2_WLAN_ACTIVE
R191 *100K_NC
C225 *33P_NC 50 COH
(17)
R187 *0_NC
R552 *0_NC
9,12,14,37,45 PLTRST#
12 CLK_PCI_DEBUG
8 PCIE_RX2-
8 PCIE_RX2+
8 PCIE_TX2-
8 PCIE_TX2+
14 PCIE_MCARD3_DET#
PCI-Express TX and RX direct to connector

(17)
R539 *0_NC LPC_LFRAME# 12,42
R538 *0_NC LPC_LAD3 12,42
R537 *0_NC LPC_LAD2 12,42
R536 *0_NC LPC_LAD1 12,42
R535 *0_NC LPC_LAD0 12,42
R541 0 PLTRST_SYS# 33,40,45,51
R540 *0_NC WPAN_RADIO_DIS_MINI# 14
SB_WPAN_PCIE_RST# 14
+3.3V_RUN
C615 *100P_NC 50 X7R
SB_SMBCLK 13,16,37,40
SB_SMBDATA 13,16,37,40
USBP6_D-
USBP6_D+
USB_MCARD3_DET#
USB_MCARD3_DET# 14
LED_WPAN#
LED_WPAN# 44

Place caps close to connector.
+1.5V_RUN
C618 0.047U 10 X7R
C617 0.047U 10 X7R
+3.3V_RUN
C616 0.1U 10 X7R
C614 0.047U 10 X7R
C632 0.1U 10 X7R
C634 0.047U 10 X7R
C607 4.7U 10 X5R 0805

MINI2CLK_REQ#
C630 220P 50 X7R

TH16 H-TC118BC197D63P2
TH15 H-TC118BC197D63P2

USBP6_D-
USBP6_D+
L76 *DLW21SN900SQ2L_NC
SB_USBP6- 13
SB_USBP6+ 13
R545 0
R544 0
Layout Note: R545 and R544 close to choke as possible to minimize stubs.

QUANTA COMPUTER

Title	MINI CARD	
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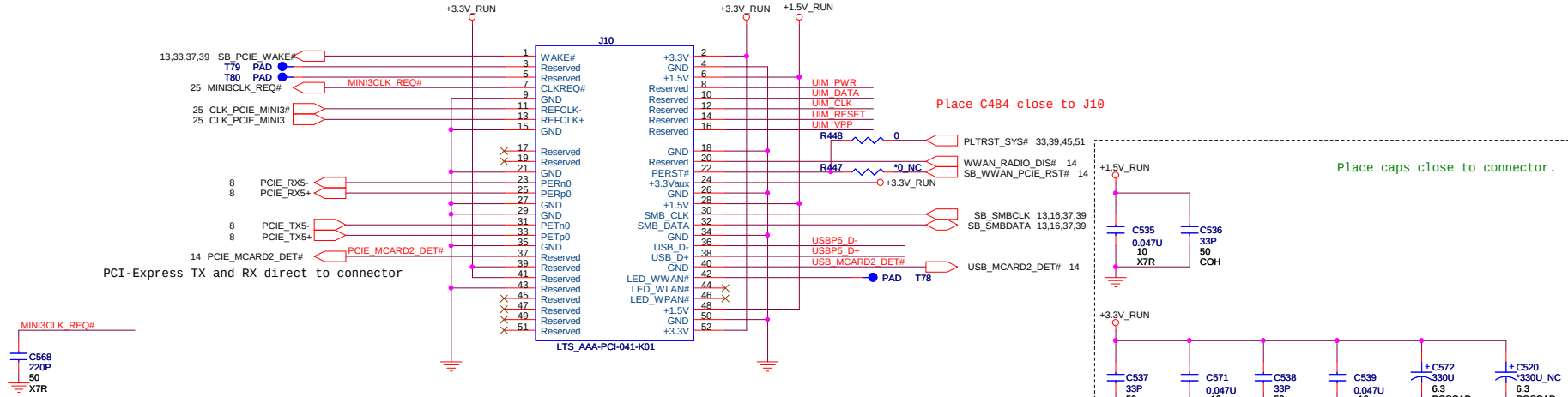
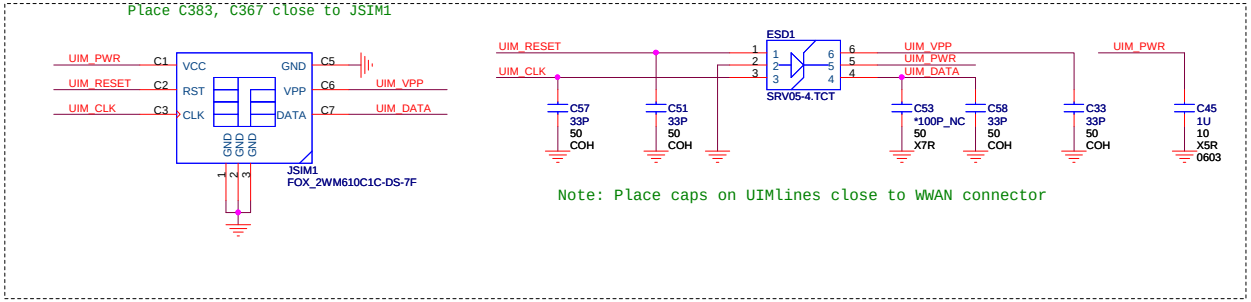
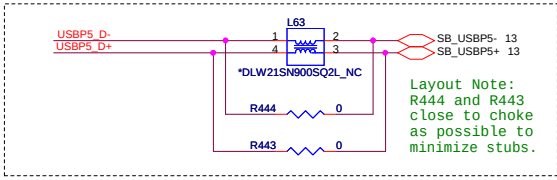
TH7
H-TC118BC197D63P2

TH8
H-TC118BC197D63P2

MiniCard WWAN connector







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Title	WWAN	
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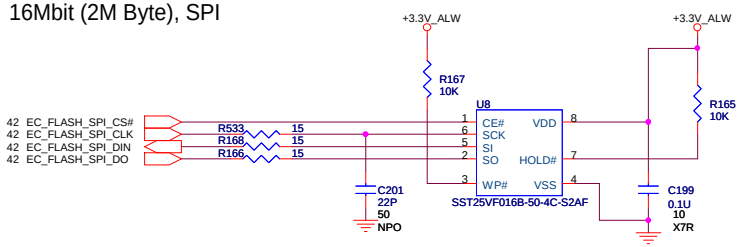
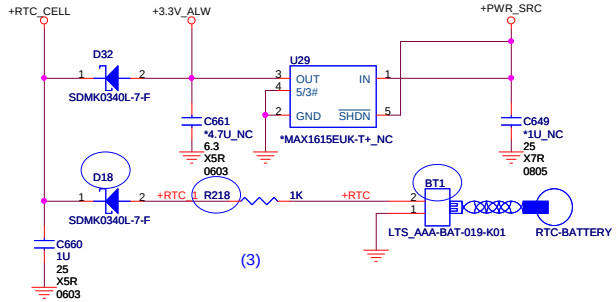
16Mbit (2M Byte), SPI



RTC BATTERY



QUANTA COMPUTER		
Title: FLASH /RTC		
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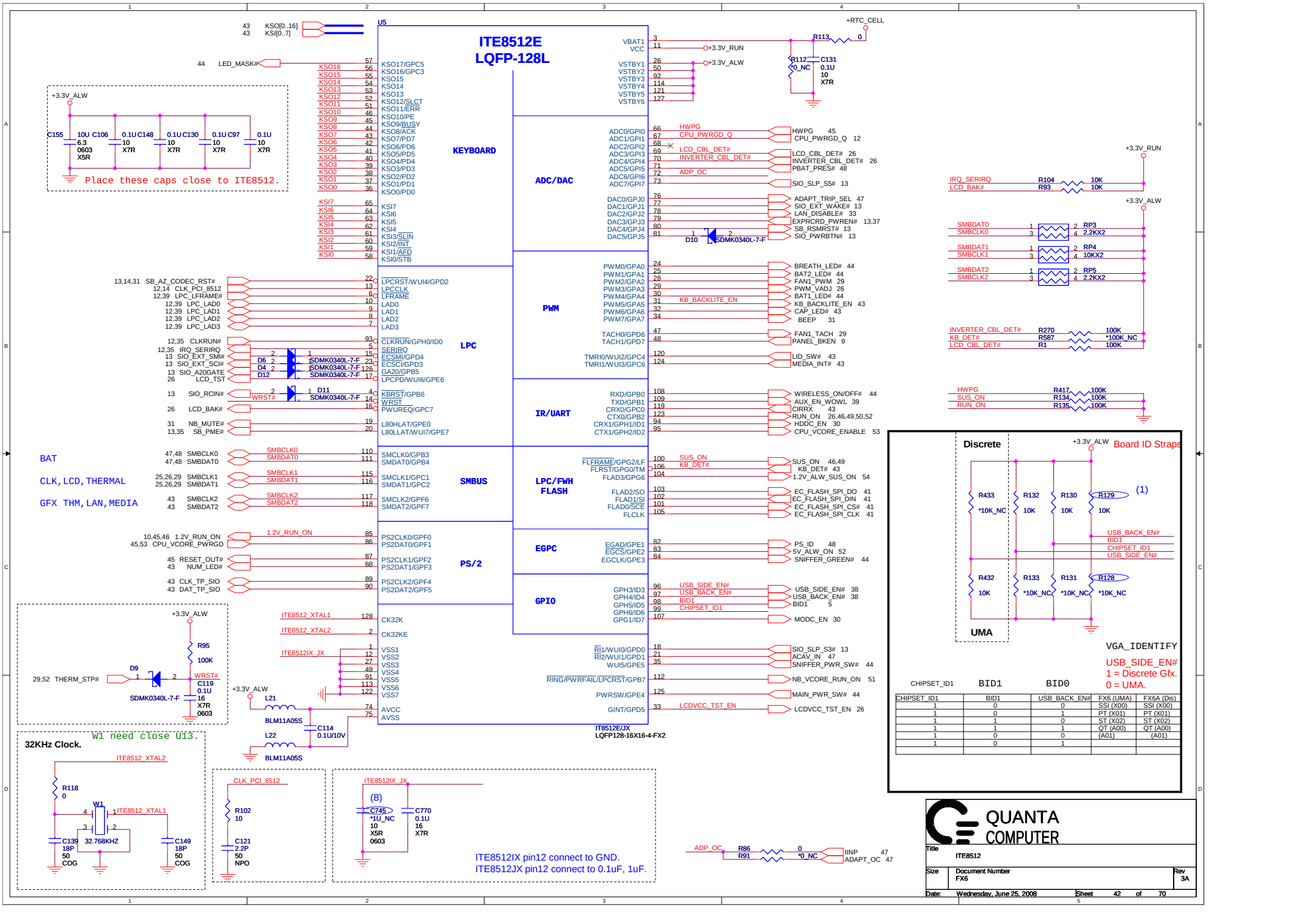
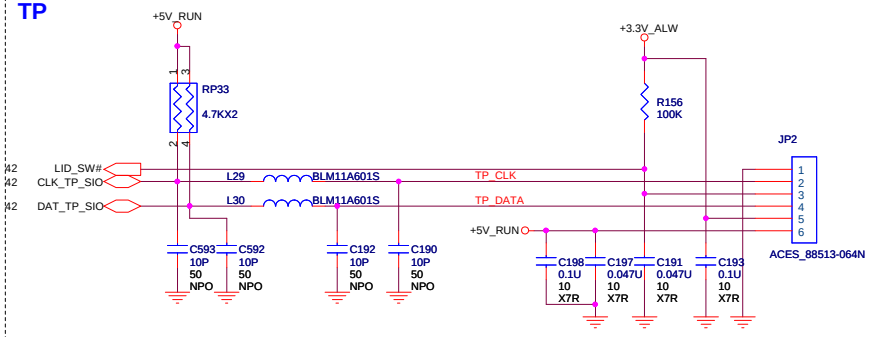
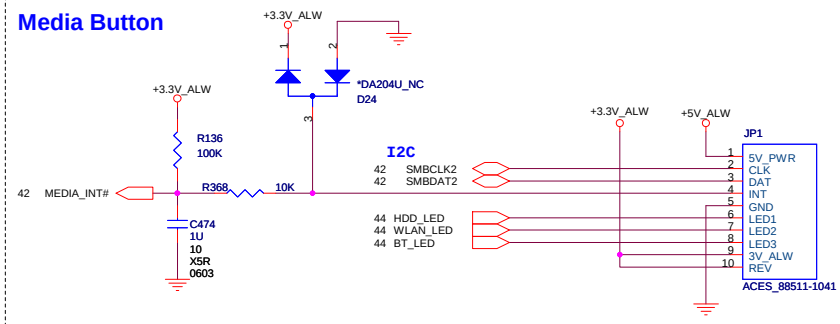

ITE8512E
LQFP-128L
U5
KEYBOARD
ADC/DAC
PWM
LPC
IR/UART
SMBUS
LPC/FWH FLASH
EGPC
PS/2
GPIO
IT8512E/JX
LQFP128-16X16-4-FX2
Place these caps close to ITE8512.
BAT
CLK, LCD, THERMAL
GFX THM, LAN, MEDIA
W1 need close U13.
32KHz Clock.
ITE8512IX pin12 connect to GND.
ITE8512JX pin12 connect to 0.1uF, 1uF.
Board ID Straps
Discrete
UMA
VGA_IDENTIFY
USB_SIDE_EN#
1 = Discrete Gfx.
0 = UMA.
CHIPSET_ID1 BID1 BID0
QUANTA COMPUTER
Title ITE8512
Size Document Number FX6 Rev 3A
Date: Wednesday, June 25, 2008 Sheet 42 of 70

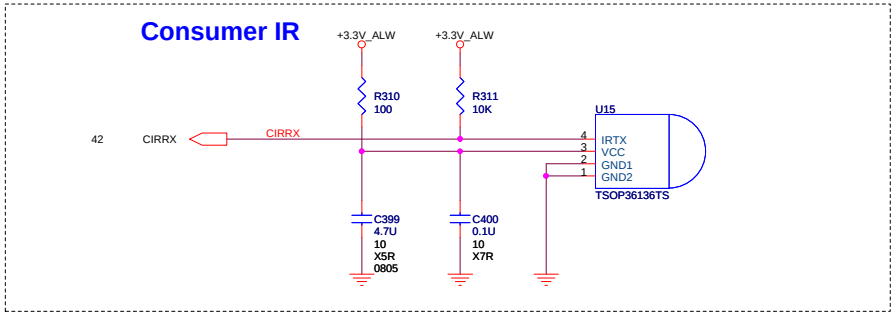
TP

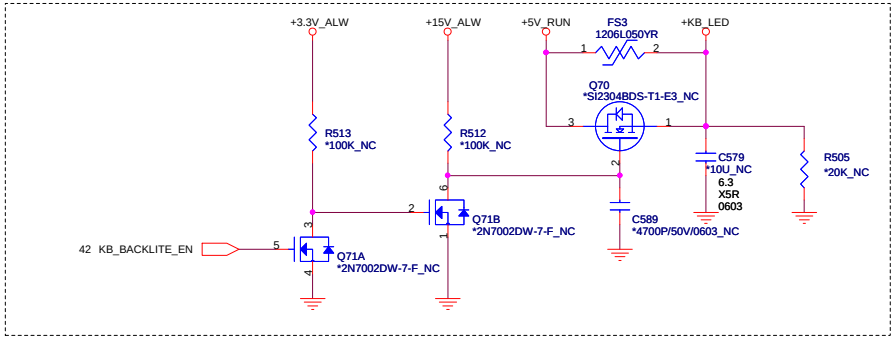


Media Button

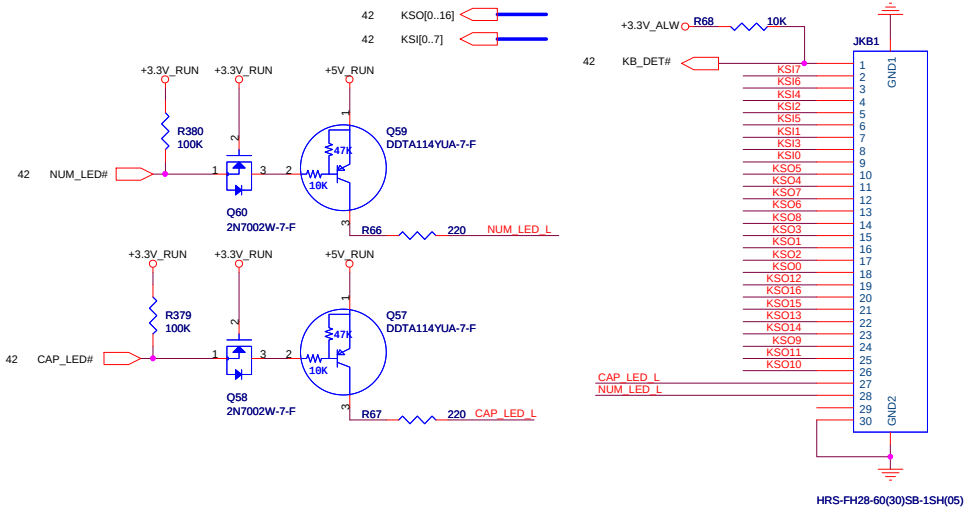


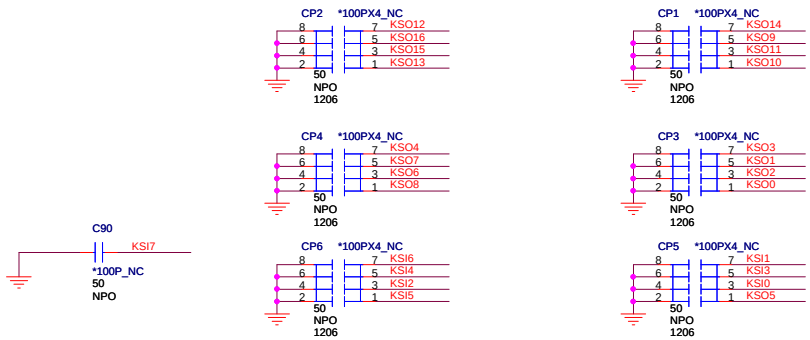
Consumer IR





KEYBOARD CONNECTOR

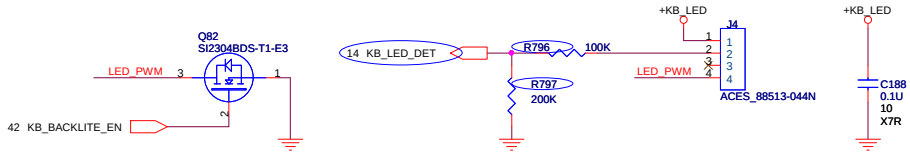




100P CAPS CLOSE TO JKB1

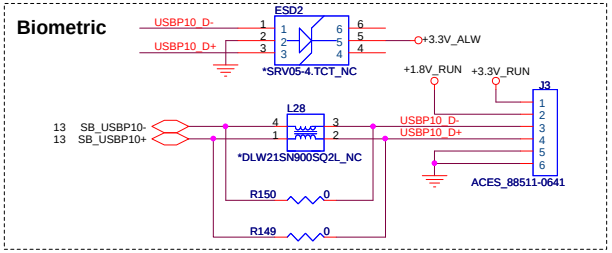
Key board Illumination

(11)

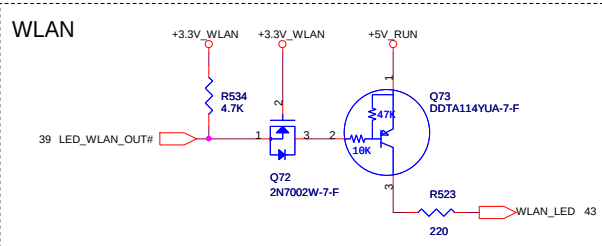


QUANTA COMPUTER		
Title: TP/KB/CIR/BT		
Size:	Document Number: FX6	Rev: 3A
Date: Wednesday, June 25, 2008	Sheet 43 of 70	

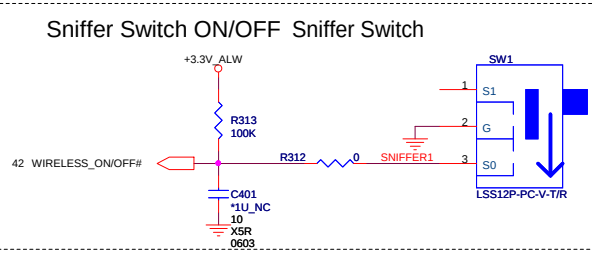
Biometric



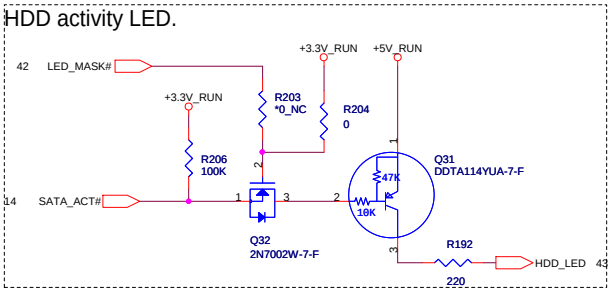
WLAN



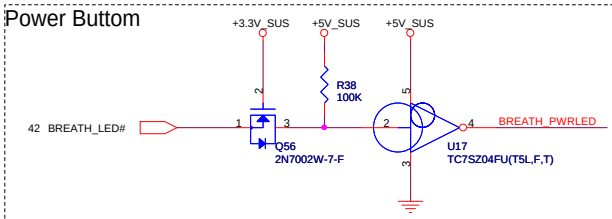
Sniffer Switch ON/OFF Sniffer Switch



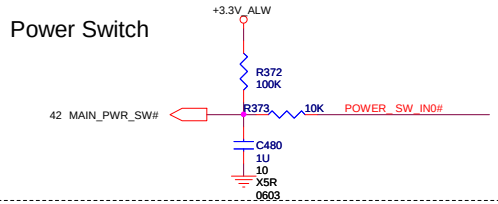
HDD activity LED.



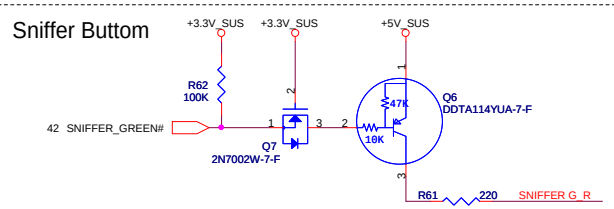
Power Buttom



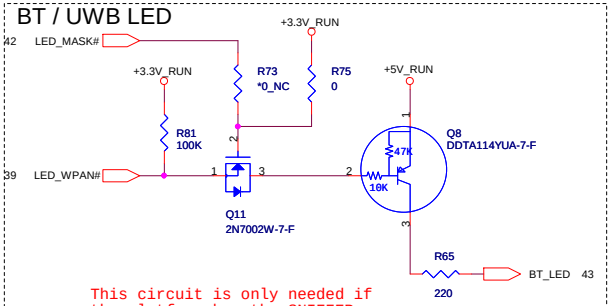
Power Switch



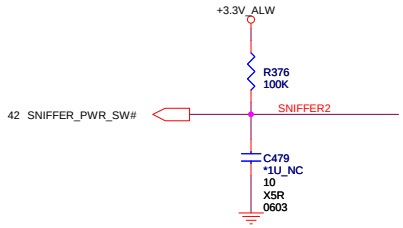
Sniffer Buttom



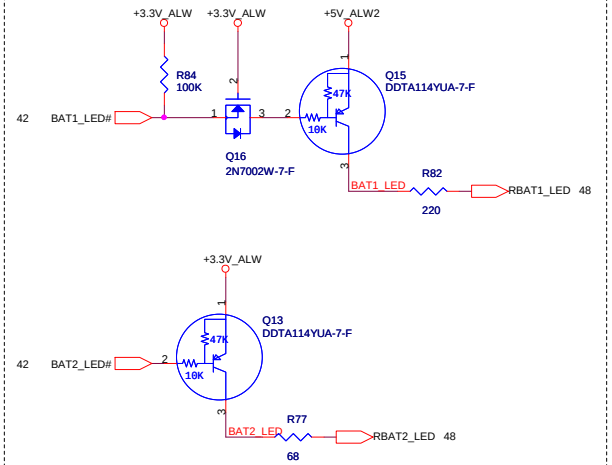
BT / UWB LED

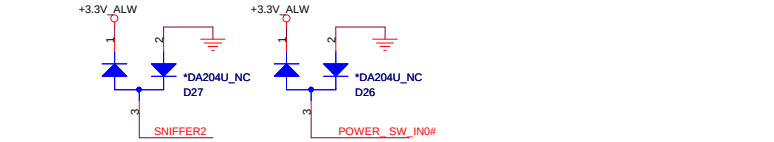


This circuit is only needed if the platform has the SNIFFER.

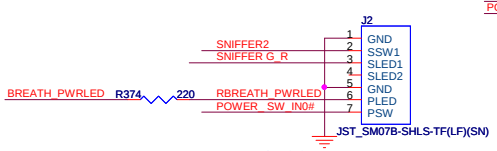


Battery status.





SNIFFER2	C746	100P/50/X7R
SNIFFER G_R	C747	100P/50/X7R
RBREATH_PWRLED	C748	100P/50/X7R
POWER_SW_IN0#	C749	100P/50/X7R



SNIFFER Y_R:WLAN on/off
SNIFFER G_R:AP detection

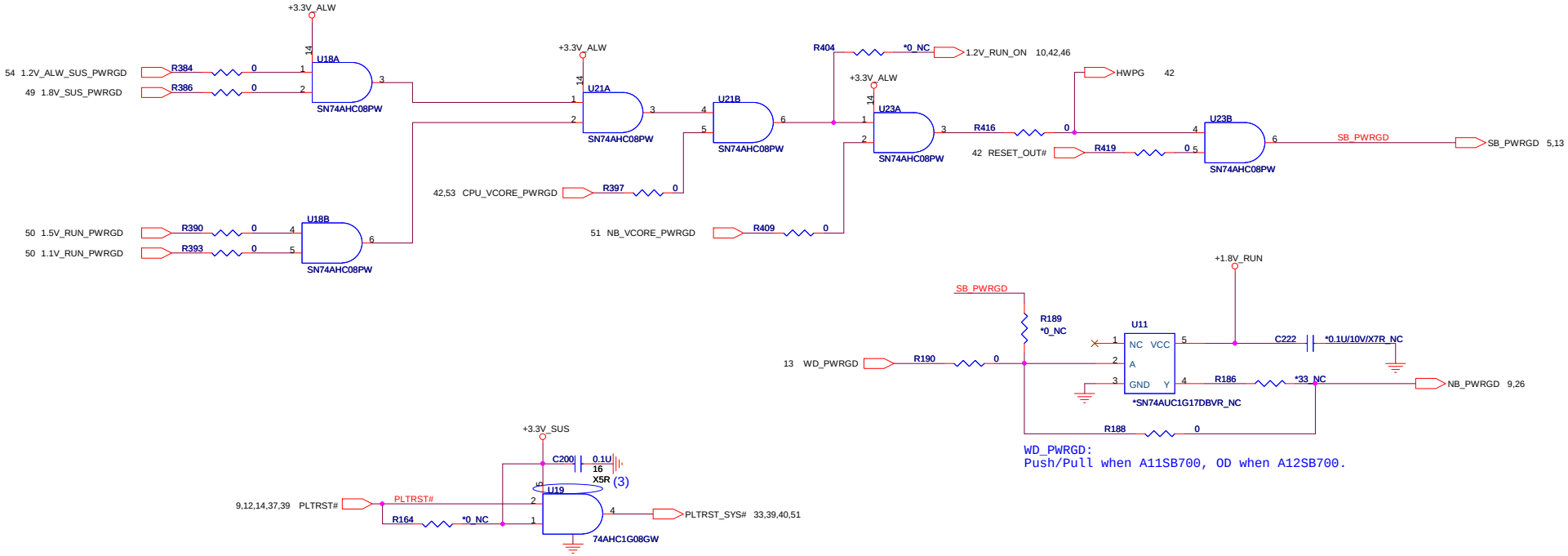
QUANTA COMPUTER

Title	SWITCH/LED		
Size	Document Number FX6		Rev 3A
Date:	Wednesday, June 25, 2008	Sheet 44 of 70	

Symbol:
2N7002W-7-F

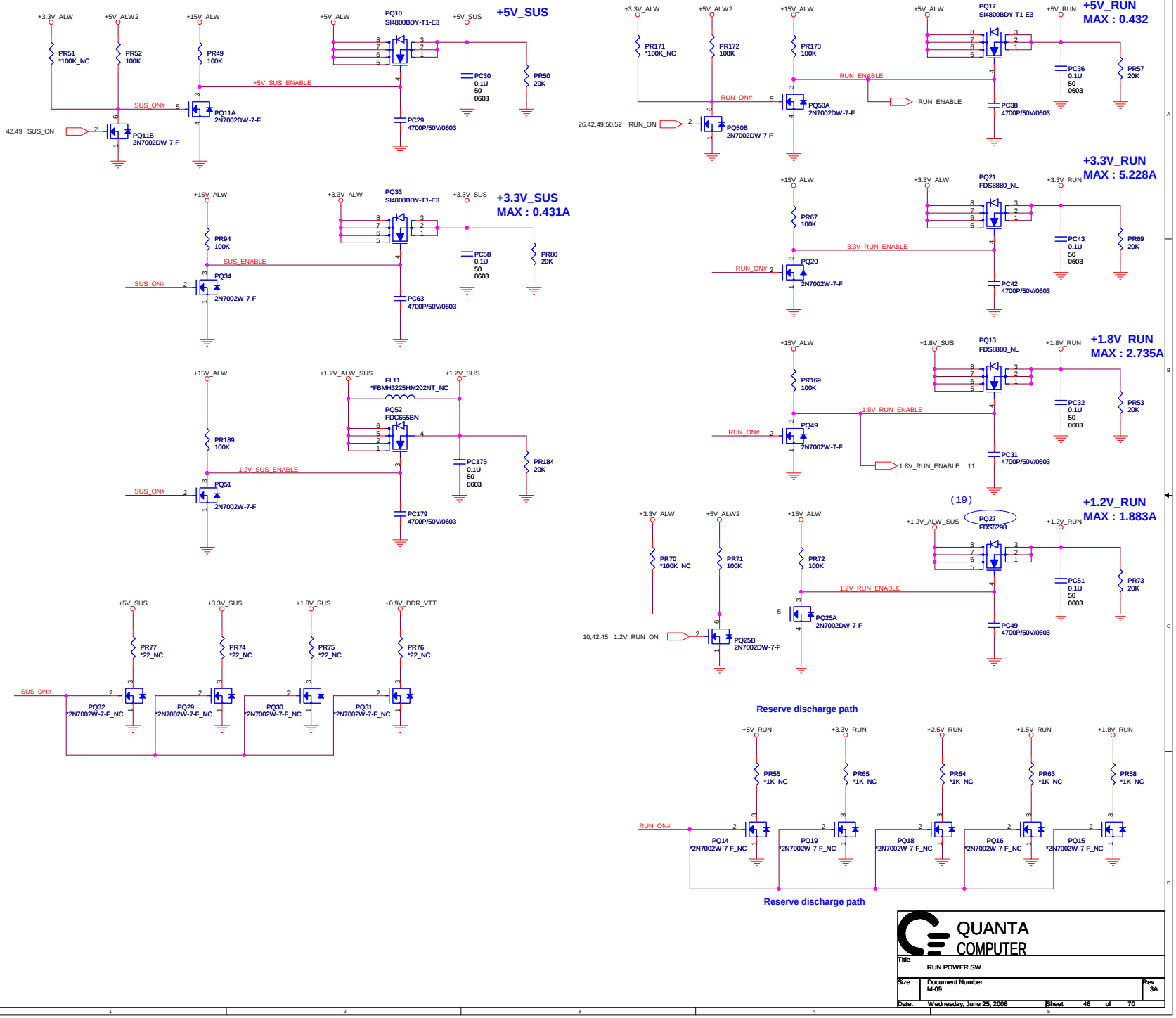
D(3)

G(2) S(1)



QUANTA COMPUTER

Title	System Reset Circuit	
Size	Document Number FX6	Rev 3A
Date: Wednesday, June 25, 2008	Sheet 45 of 70	



QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number M-09	Rev 3A
Date: Wednesday, June 25, 2008	Sheet 46 of 70	

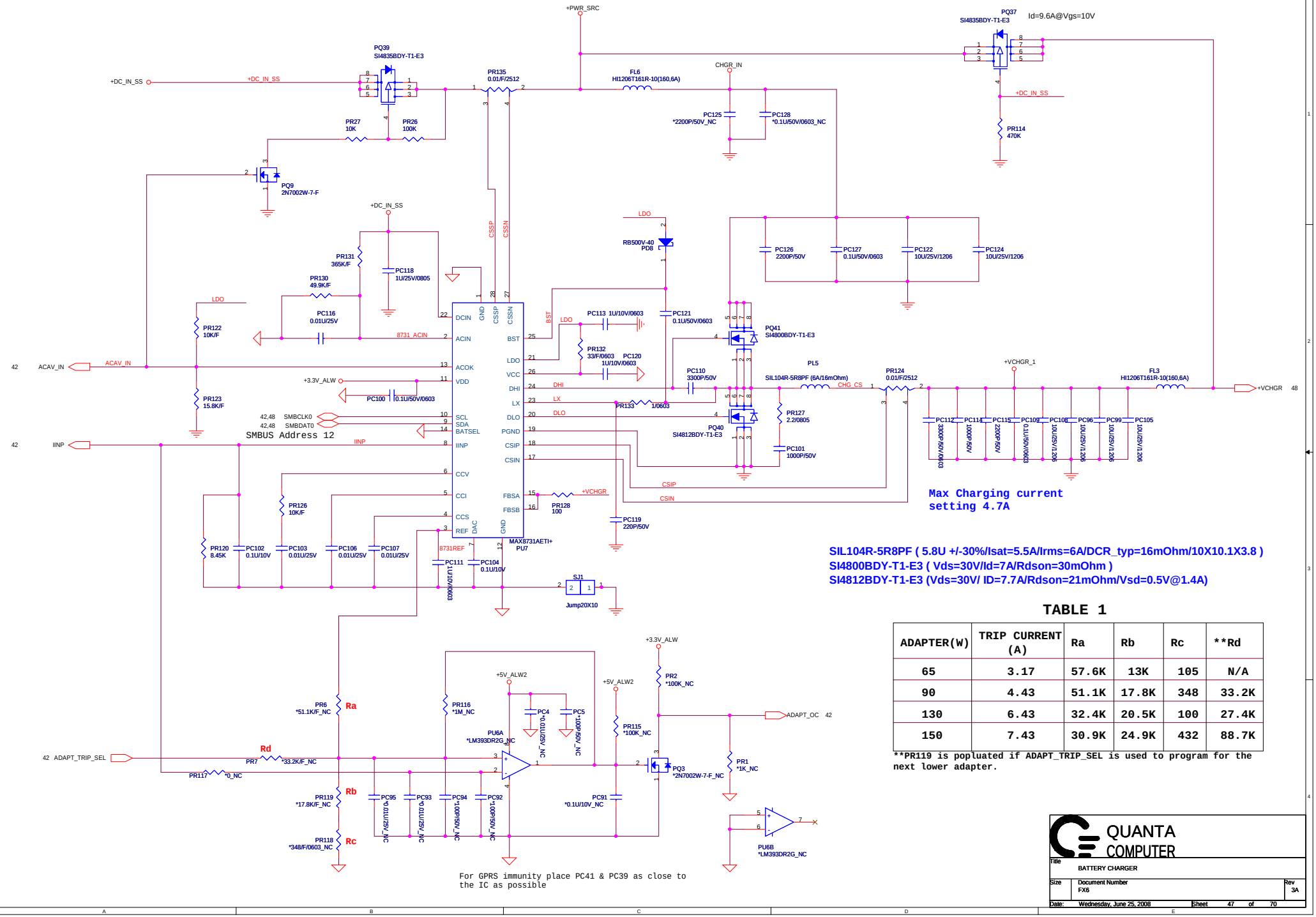


TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	Ra	Rb	Rc	**Rd
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K

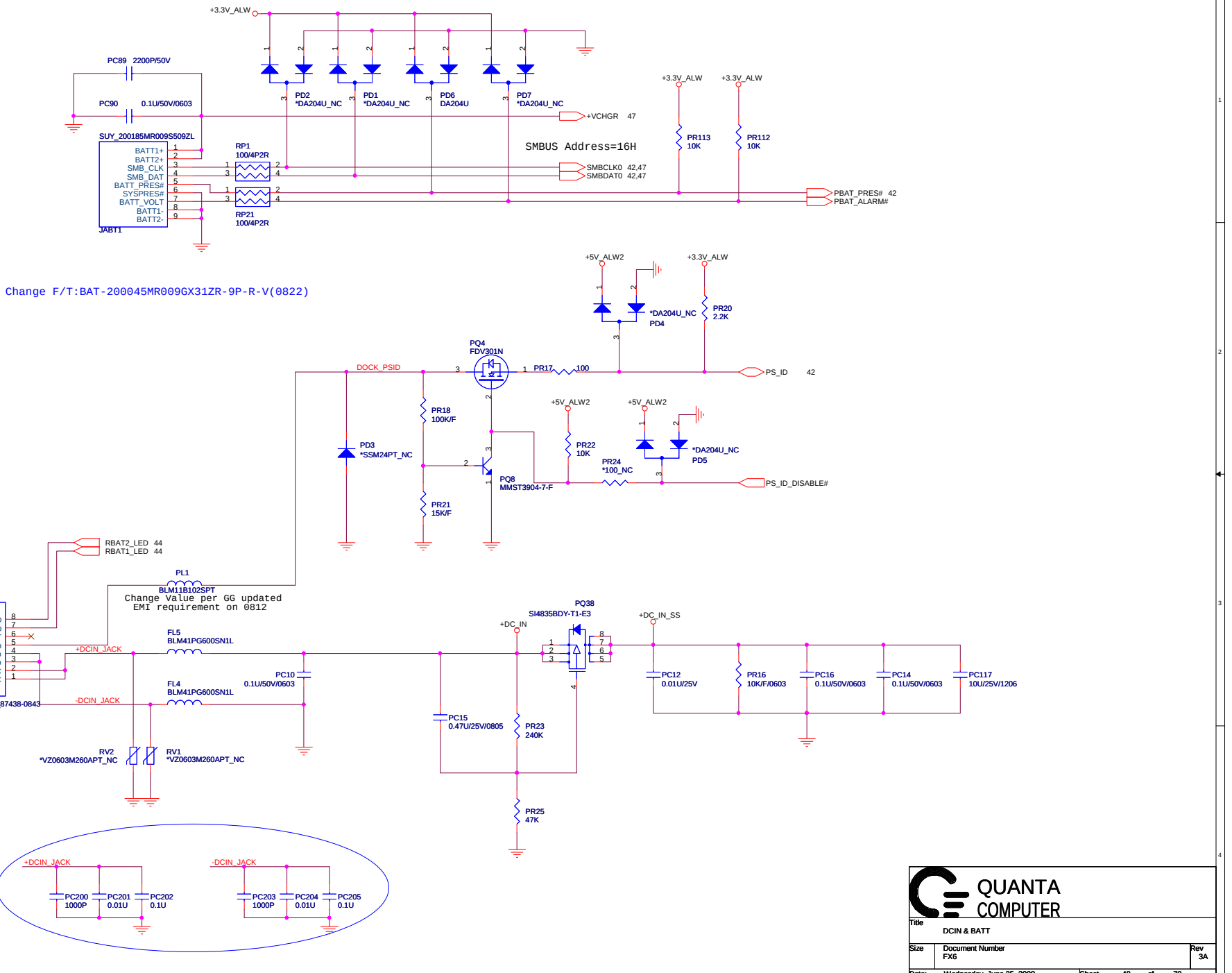
**PR119 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

QUANTA COMPUTER

Title: BATTERY CHARGER

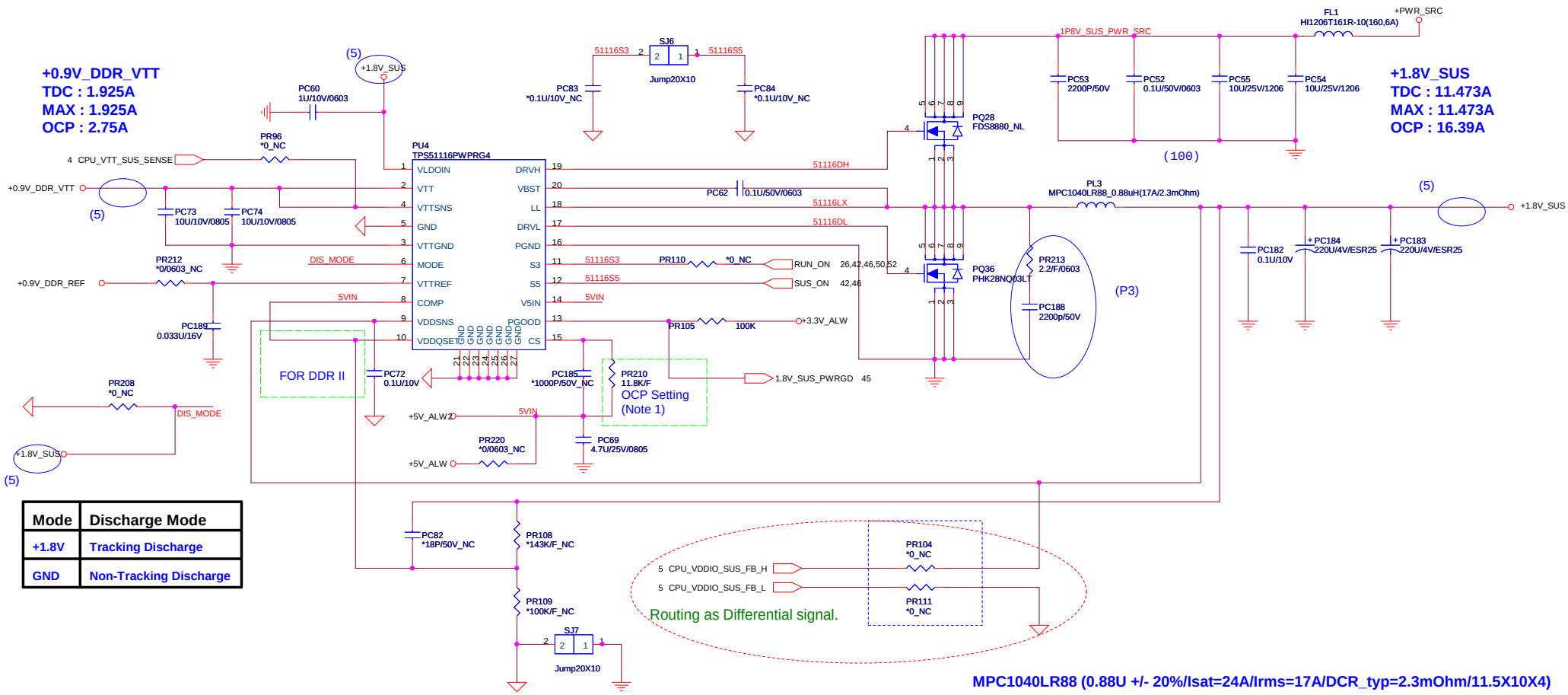
Size | Document Number: FX6 | Rev: 3A

Date: Wednesday, June 25, 2008 | Sheet 47 of 70



QUANTA COMPUTER

Title	DCIN & BATT	
Size	Document Number FX6	Rev 3A
Date: Wednesday, June 25, 2008	Sheet 48 of 70	


+0.9V_DDR_VTT
TDC : 1.925A
MAX : 1.925A
OCP : 2.75A
+1.8V_SUS
TDC : 11.473A
MAX : 11.473A
OCP : 16.39A
PU4
TPS51116PWPRG4
VLDOIN
VTT
VTTSNS
GND
VTTGND
MODE
VTTREF
COMP
VDDSNS
VDDQSET
DRVH
VBST
LL
DRVL
PGND
S3
S5
V5IN
PGOOD
CS
PC60 1U/10V/0603
PR96 *0_NC
PC73 10U/10V/0805
PC74 10U/10V/0805
PR212 *0/0603_NC
PC189 0.033U/16V
PR208 *0_NC
PC72 0.1U/10V
PC83 *0.1U/10V_NC
PC84 *0.1U/10V_NC
SJ6
Jump20X10
PC62 0.1U/50V/0603
PR110 *0_NC
PR105 100K
PC185 *1000P/50V_NC
PR210 11.8K/F
OCP Setting
(Note 1)
PR220 *0/0603_NC
PC69 4.7U/25V/0805
FOR DDR II
PQ28 FDS8880_NL
PQ36 PHK28NQ03LT
PR213 2.2/F/0603
PC188 2200p/50V
FL1 HI1206T161R-10(160,6A)
PC53 2200P/50V
PC52 0.1U/50V/0603
PC55 10U/25V/1206
PC54 10U/25V/1206
PL3 MPC1040LR88_0.88uH(17A/2.3mOhm)
PC182 0.1U/10V
PC184 220U/4V/ESR25
PC183 220U/4V/ESR25
PC82 *18P/50V_NC
PR108 *143K/F_NC
PR109 *100K/F_NC
SJ7
PR104 *0_NC
PR111 *0_NC
Routing as Differential signal.
MPC1040LR88 (0.88U +/- 20%/Isat=24A/Irms=17A/DCR_typ=2.3mOhm/11.5X10X4)
Frequency=400KHz, I_ripple=4.54A, Rtrip=11.8Kohm
(Note 1) Current Limiting Setting :
Rtrip(Kohm)=100*(Iocp-0.5*Iripple)*Rds(on)
Mode
Discharge Mode
+1.8V
Tracking Discharge
GND
Non-Tracking Discharge
QUANTA COMPUTER
Title
1.8V_SUS&0.9VTT
Size
Document Number
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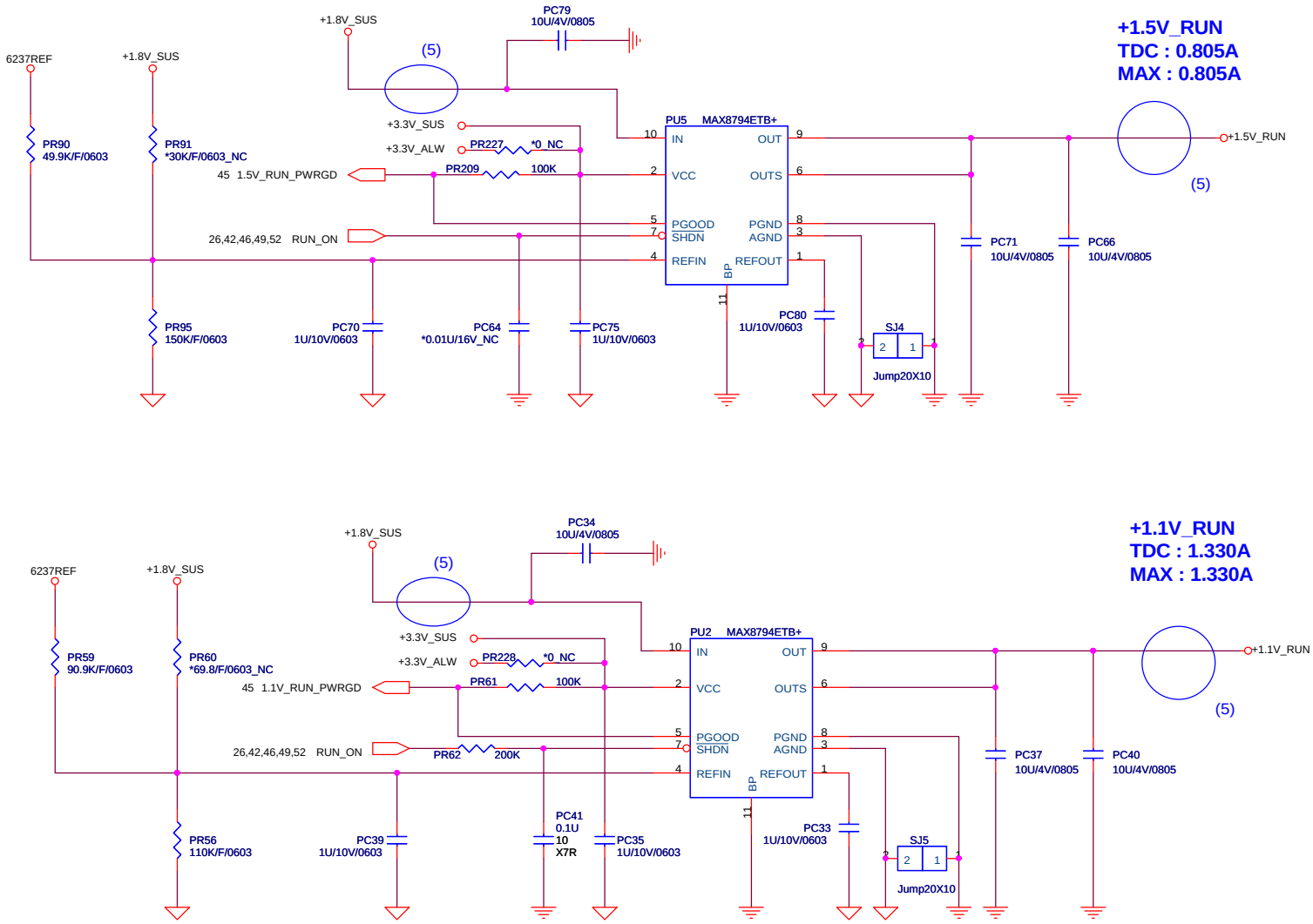
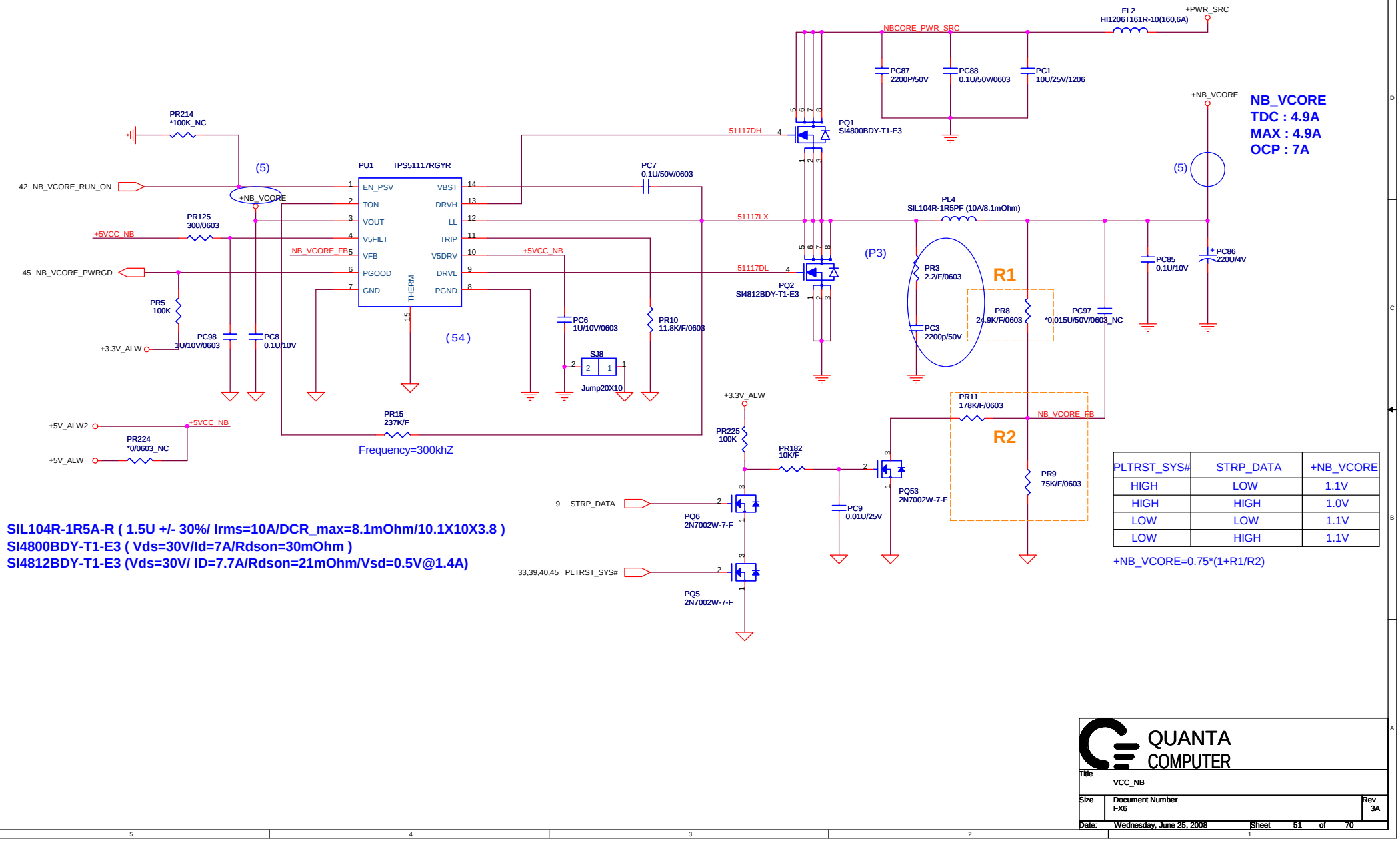


QUANTA COMPUTER

Title	1.5V_RUN&1.1V_RUN	
Size	Document Number FX6	Rev 3A
Date: Wednesday, June 25, 2008	Sheet 50 of 70	



PLTRST_SYS#	STRP_DATA	+NB_VCORE
HIGH	LOW	1.1V
HIGH	HIGH	1.0V
LOW	LOW	1.1V
LOW	HIGH	1.1V

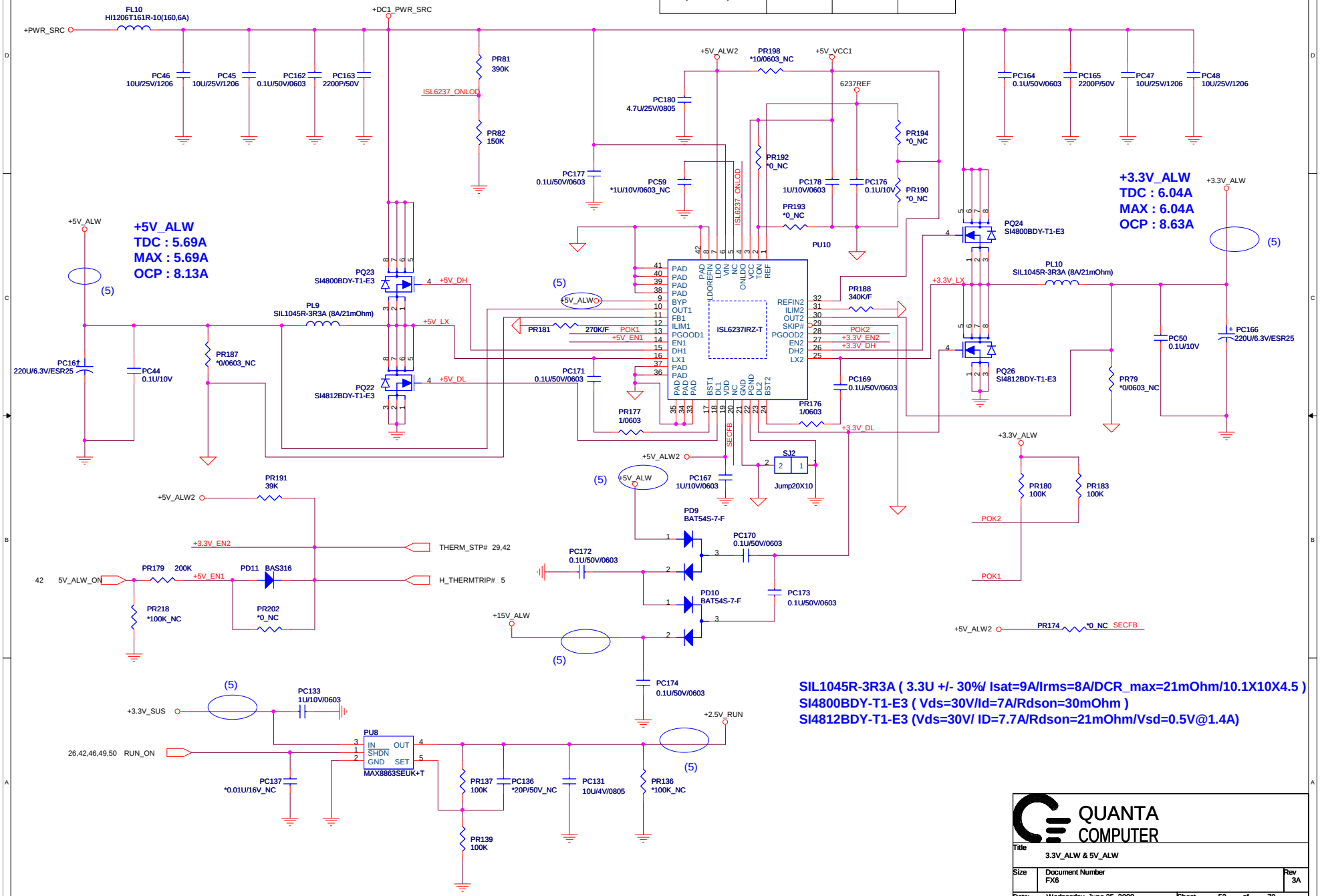
+NB_VCORE=0.75*(1+R1/R2)

SIL104R-1R5A-R (1.5U +/- 30%/ Irms=10A/DCR_max=8.1mOhm/10.1X10X3.8)
SI4800BDY-T1-E3 (Vds=30V/Id=7A/Rdson=30mOhm)
SI4812BDY-T1-E3 (Vds=30V/ ID=7.7A/Rdson=21mOhm/Vsd=0.5V@1.4A)

QUANTA COMPUTER

Title	VCC_NB	
Size	Document Number FX6	Rev 3A
Date: Wednesday, June 25, 2008	Sheet 51 of 70	

TON	GND	OPEN	VCC
Frequency (KHz) (5V/3.3V)	400/500	400/300	200/300



ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

CPU_VDDNB_RUN
TDC : 2.1A
OCP : 3A

PL7 MPLC0730L3R3 (5.7A/30mOhm)
PQ44 SI4914DY-T1-E3
FL8 HI1206T161R-10(160,6A)
FL7 HI1206T161R-10(160,6A)
FL9 HI1206T161R-10(160,6A)
PL6 ETQP4LR36WFC_0.36UH
PL8 ETQP4LR36WFC_0.36UH
PU9 ISL6265HRTZ-T

Pin 49 is GND Pin

+CPU_VDD0_RUN
TDC : 18A

+CPU_VDD1_RUN
TDC : 18A

Close to CPU socket

Close to CPU socket

Option for Uni-plane

Title	CPU_CORE_POWER
Size	Document Number FX6
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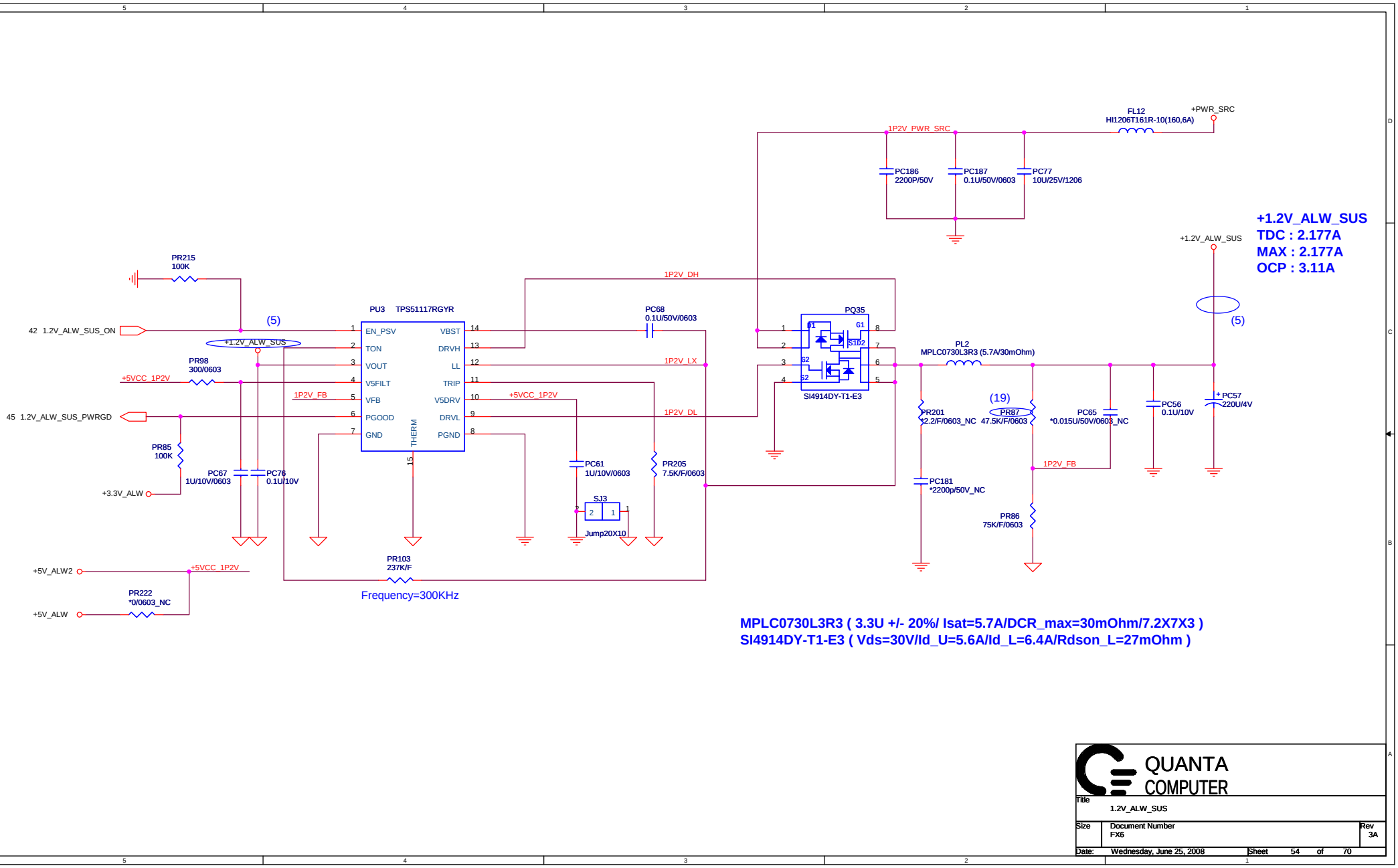
QUANTA COMPUTER



QUANTA COMPUTER

Title	1.2V_ALW_SUS	
Size	Document Number FX6	Rev 3A
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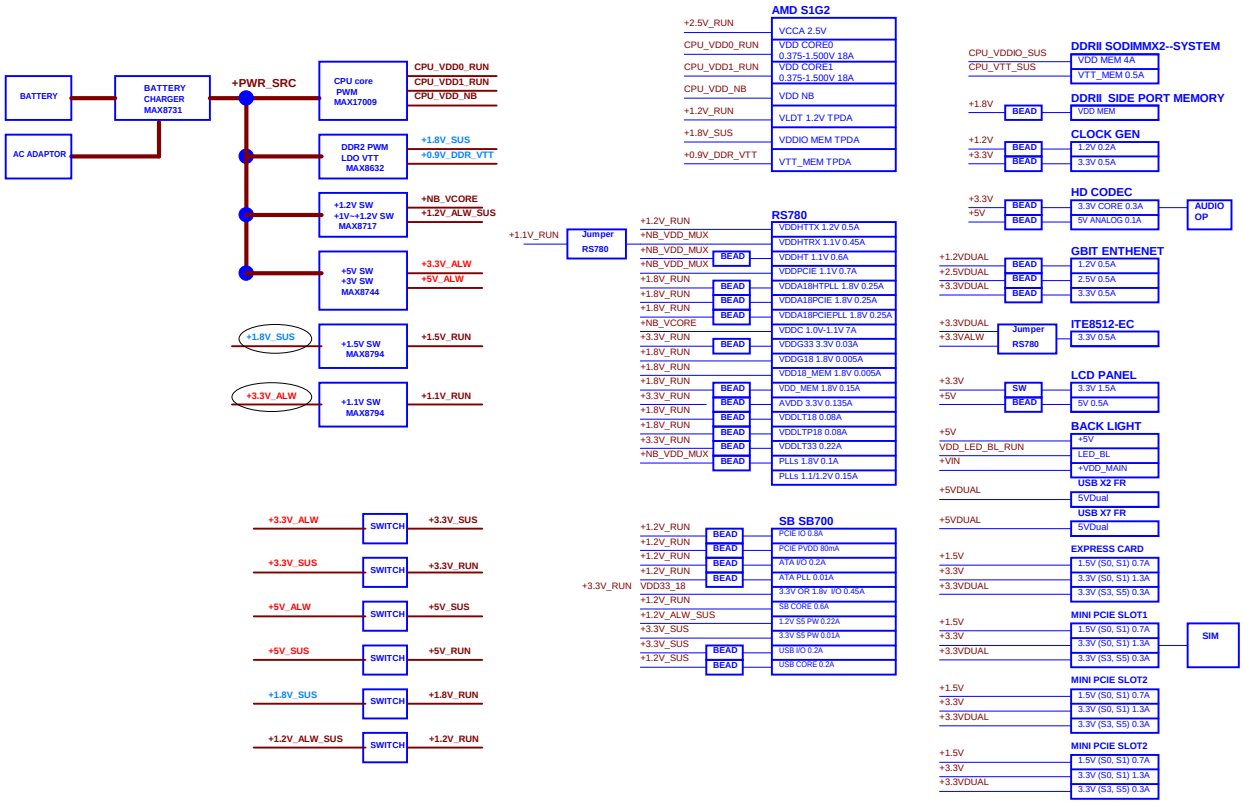
QUANTA COMPUTER

Title	VGA_M82	
Size	Document Number FX6	Rev 3A
Date: Tuesday, June 03, 2008	Sheet 55 of 70	

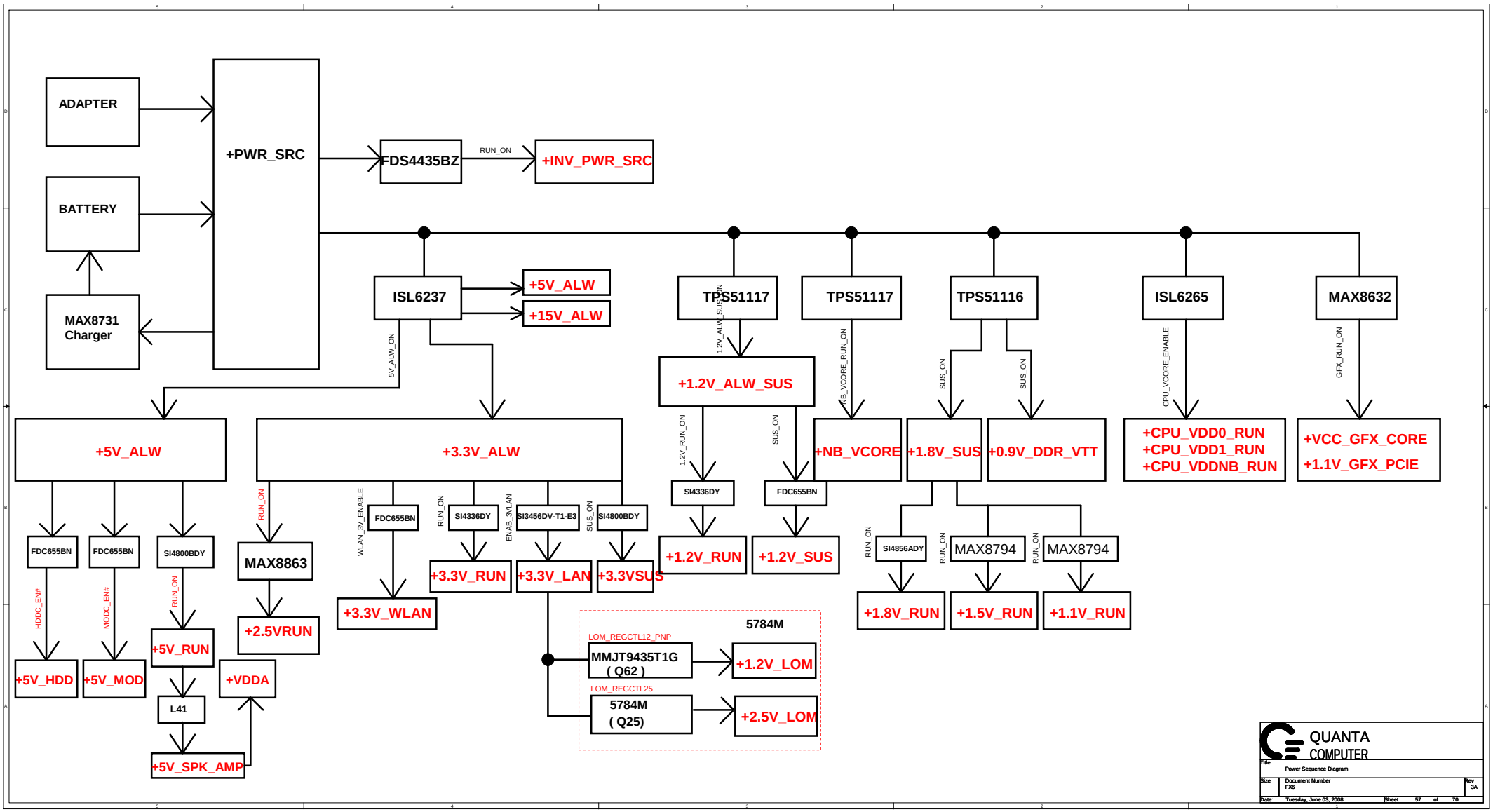


QUANTA COMPUTER

Title: Power Rail for system

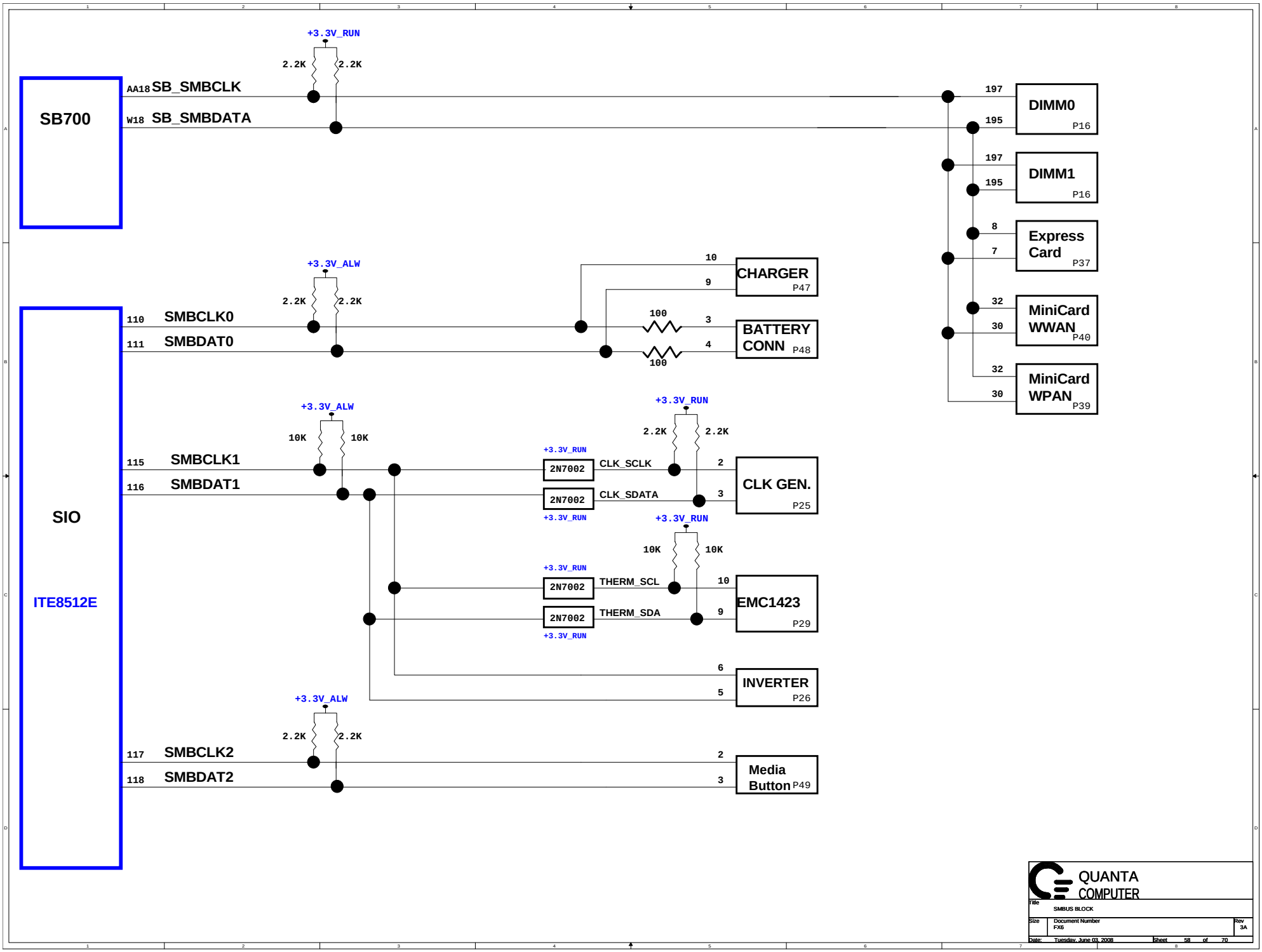
Size	Document Number	Rev
A	PWI	3A

Date: Tuesday, June 03, 2008 Sheet 56 of 70



QUANTA COMPUTER

Title: Power Sequence Diagram		
Size	Document Number FX6	Rev 3A
Date: Tuesday, June 03, 2008	Sheet 57 of 70	


SB700
AA18 SB_SMBCLK
W18 SB_SMBDATA
+3.3V_RUN
2.2K
2.2K
197
DIMM0
195
P16
197
DIMM1
195
P16
8
Express Card
7
P37
32
MiniCard WWAN
30
P40
32
MiniCard WPAN
30
P39
SIO
ITE8512E
110 SMBCLK0
111 SMBDAT0
+3.3V_ALW
2.2K
2.2K
100
100
10
9
CHARGER
P47
3
4
BATTERY CONN
P48
115 SMBCLK1
116 SMBDAT1
+3.3V_ALW
10K
10K
+3.3V_RUN
2.2K
2.2K
2N7002
CLK_SCLK
2N7002
CLK_SDATA
2
3
CLK GEN.
P25
+3.3V_RUN
10K
10K
2N7002
THERM_SCL
2N7002
THERM_SDA
10
9
EMC1423
P29
6
5
INVERTER
P26
117 SMBCLK2
118 SMBDAT2
+3.3V_ALW
2.2K
2.2K
2
3
Media Button
P49
QUANTA COMPUTER
Title
SMBUS BLOCK
Size
Document Number
FX6
Rev
3A
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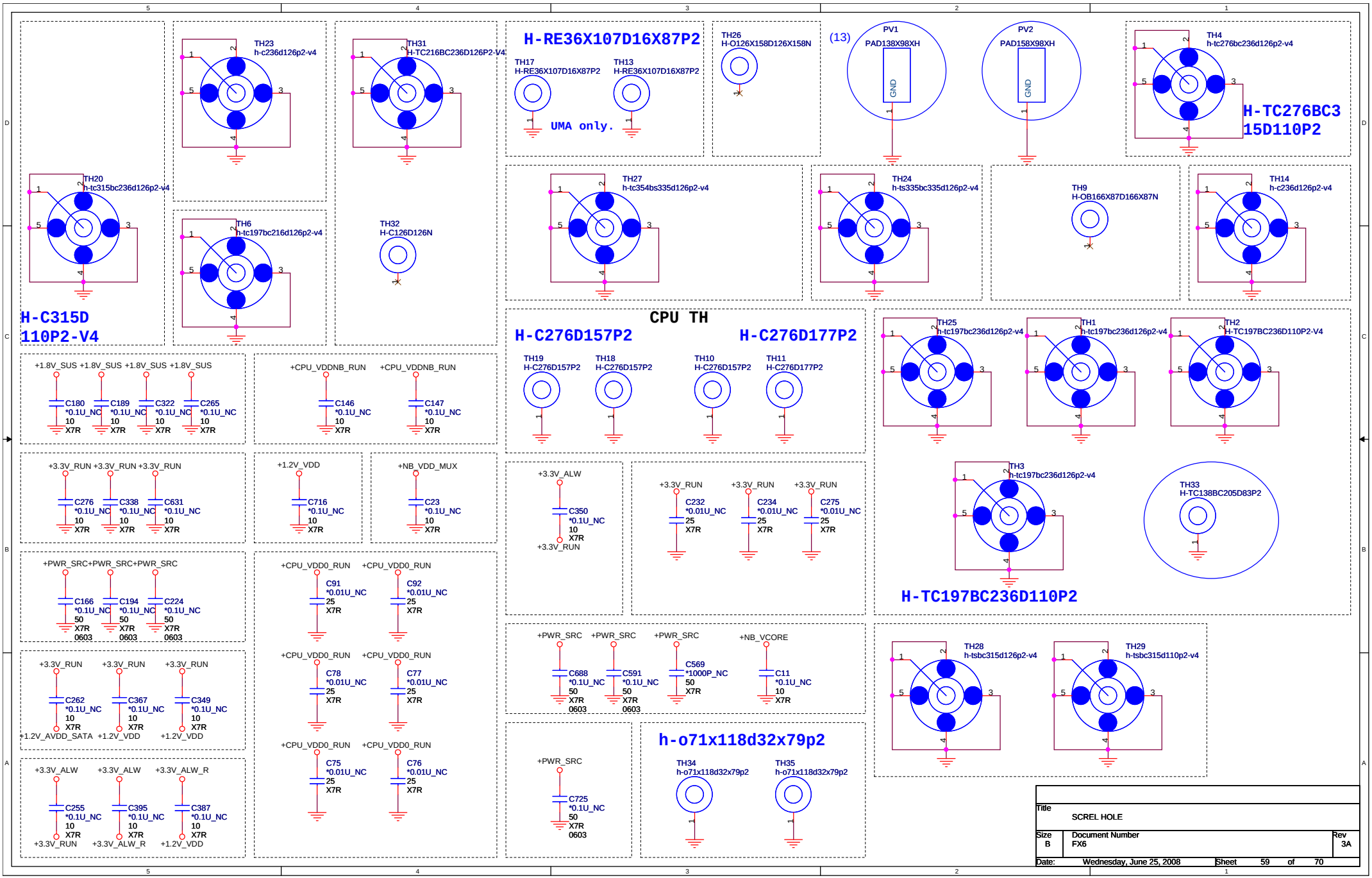
H-C315D
110P2-V4
TH20
h-tc315bc236d126p2-v4
TH23
h-c236d126p2-v4
TH6
h-tc197bc216d126p2-v4
TH31
H-TC216BC236D126P2-V4
TH32
H-C126D126N
H-RE36X107D16X87P2
TH17
H-RE36X107D16X87P2
TH13
H-RE36X107D16X87P2
UMA only.
TH26
H-O126X158D126X158N
(13)
PV1
PAD138X98XH
PV2
PAD158X98XH
GND
TH4
h-tc276bc236d126p2-v4
H-TC276BC3
15D110P2
TH27
h-tc354bs335d126p2-v4
TH24
h-ts335bc335d126p2-v4
TH9
H-OB166X87D166X87N
TH14
h-c236d126p2-v4
CPU TH
H-C276D157P2
H-C276D177P2
TH19
H-C276D157P2
TH18
H-C276D157P2
TH10
H-C276D157P2
TH11
H-C276D177P2
TH25
h-tc197bc236d126p2-v4
TH1
h-tc197bc236d126p2-v4
TH2
H-TC197BC236D110P2-V4
TH3
h-tc197bc236d126p2-v4
TH33
H-TC138BC205D83P2
H-TC197BC236D110P2
+1.8V_SUS +1.8V_SUS +1.8V_SUS +1.8V_SUS
C180 *0.1U_NC 10 X7R
C189 *0.1U_NC 10 X7R
C322 *0.1U_NC 10 X7R
C265 *0.1U_NC 10 X7R
+CPU_VDDNB_RUN +CPU_VDDNB_RUN
C146 *0.1U_NC 10 X7R
C147 *0.1U_NC 10 X7R
+3.3V_RUN +3.3V_RUN +3.3V_RUN
C276 *0.1U_NC 10 X7R
C338 *0.1U_NC 10 X7R
C631 *0.1U_NC 10 X7R
+1.2V_VDD
C716 *0.1U_NC 10 X7R
+NB_VDD_MUX
C23 *0.1U_NC 10 X7R
+3.3V_ALW
C350 *0.1U_NC 10 X7R
+3.3V_RUN
+3.3V_RUN +3.3V_RUN +3.3V_RUN
C232 *0.01U_NC 25 X7R
C234 *0.01U_NC 25 X7R
C275 *0.01U_NC 25 X7R
+PWR_SRC+PWR_SRC+PWR_SRC
C166 *0.1U_NC 50 X7R 0603
C194 *0.1U_NC 50 X7R 0603
C224 *0.1U_NC 50 X7R 0603
+CPU_VDD0_RUN +CPU_VDD0_RUN
C91 *0.01U_NC 25 X7R
C92 *0.01U_NC 25 X7R
+CPU_VDD0_RUN +CPU_VDD0_RUN
C78 *0.01U_NC 25 X7R
C77 *0.01U_NC 25 X7R
+CPU_VDD0_RUN +CPU_VDD0_RUN
C75 *0.01U_NC 25 X7R
C76 *0.01U_NC 25 X7R
+PWR_SRC +PWR_SRC +PWR_SRC +NB_VCORE
C688 *0.1U_NC 50 X7R 0603
C591 *0.1U_NC 50 X7R 0603
C569 *1000P_NC 50 X7R
C11 *0.1U_NC 10 X7R
+3.3V_RUN +3.3V_RUN +3.3V_RUN
C262 *0.1U_NC 10 X7R
C367 *0.1U_NC 10 X7R
C349 *0.1U_NC 10 X7R
+1.2V_AVDD_SATA +1.2V_VDD +1.2V_VDD
+3.3V_ALW +3.3V_ALW +3.3V_ALW_R
C255 *0.1U_NC 10 X7R
C395 *0.1U_NC 10 X7R
C387 *0.1U_NC 10 X7R
+3.3V_RUN +3.3V_ALW_R +1.2V_VDD
+PWR_SRC
C725 *0.1U_NC 50 X7R 0603
h-o71x118d32x79p2
TH34
h-o71x118d32x79p2
TH35
h-o71x118d32x79p2
TH28
h-tsbc315d126p2-v4
TH29
h-tsbc315d110p2-v4
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				X00-1		
1	25	8/13/2007	EE	CLK_NB_14MB need resistor to a voltage divider. RS780 voltage level is +1.1V.	Chagne R607 from 33 ohm to 158/F, added R637 90.9/F, depop R608 10k for RS780.	X00-1
2	4	8/13/2007	EE	Remove R516 0 ohm reserved resistor for MEMVREF. FX6/GX3 use 1.8V/2	Remove R516 0 ohm.	X00-1
3	5,12	8/13/2007	EE	CPU_LDT_REQ#R should pull up to +1.8V_SUS.	POP R38 and Depop R415.	X00-1
4	8,51	8/13/2007	EE	Connect STRP_DATA to VCORE PWM of NB for Power play.	Connect STRP_DATA from U23.B10 to PQ1.2.	X00-1
5	13	8/13/2007	EE	IDE_RST#/F_RST#/IMC_GPO3 defaults to output driven low.	Remove R720 20k.	X00-1
6	14	8/13/2007	EE	GP16,GP17 for ROM sel. Hepburn connect to EC spi rom. For SB, EC is on LPC bus.	Depop R430 and pop R420. For LPC.	X00-1
7	14	8/13/2007	EE	ATI recommend that AVDD should tie to +3.3V_S5 power rail.	Chagne L46 from +3.3V_SUS to +3.3V_ALW.	X00-1
8	14	8/13/2007	EE	ATI recommend that AZ_RST#, LPCCLK0, LPCCLK1 should pull up to +3.3V_S5 with a 10-k.	Chagne R378,R396,R408 from +3.3V_SUS to +3.3V_ALW.	X00-1
9	8	8/13/2007	EE	S1G2 didn't use DDR_CS2_DIMMA/B# pin.	Remove DDR_CS2_DIMMA/B# from CN5,CN6	X00-1
				Chagne from X00-1 to X00-2		
10	08	8/14/2007	EE	Follow ATI recommend.	Change Q59,Q20 from MMBT3904 to FDV301N and remove R54,R492.	X00-2
11	5	8/14/2007	EE	Follow ATI recommend.	Modify VID table.	X00-2
12	16	8/14/2007	EE	Remove single net DDR_CS3_DIMMA/B#	Remove single net CN5.120,CN6.120	X00-2
13	5	8/14/2007	EE	Change the CPU_PWRGD,LDT_STOP#, LDT_RST# from +1.8V_RUN to +1.8V_SUS.	Pull-up R193,R180,R184 from +1.8V_RUN to +1.8V_SUS(VDDIO).	X00-2
14	5	8/14/2007	EE	Follow ATI recommend.CPU pin C2 need pull-down with 0 ohm.	Pop R536 0 ohm.	X00-2
15	5	8/14/2007	EE	To save the space. There is no need to have these resister in Griffin system.	Remove R556,R169,R161,R554,R553,R555,R172,R191,R165,R168,R196,R205	X00-2
16	5	8/14/2007	EE	Follow ATI.The HDT we have (you have) right now is Purple Possum system. It's 1.8V level design.	Pop R213 0 ohm and depop R212,Q35,R216.	X00-2
17	5,53	8/14/2007	EE	CPU_PWRGD_SVID_REG should be level shifted to 3.3V for the ISL6265. Vih(min) is 2V.	Added Q76,R161.	X00-2
18	5	8/14/2007	EE	Diode D7 blocks a low input to the CPU MEMHOT_L so the circuit would not work as drawn	Remove D7 and reserved R159 680 ohm for DDRII thermal IC in the future.	X00-2
19	19	8/14/2007	EE	HDMI strap is on Hsync.Add 10k-ohm PU (to 3.3V) on VGAHSYNC before buffer U6. Discrete only.	Pull up R191 10k ohm to +3.3V_RUN at VGASYNC	X00-2
20	8,28	8/14/2007	EE	DDC3 is 5V tolerance. There is no need to add level shifters, Discrete only.	Remove R18,R19,R22,R30,Q12,Q18. Remove off page HDMI_SCL,HDMI_SDA.Add TP on U23.A8	X00-2
21	39	8/14/2007	EE	For LPC connect to WPAN socket: Reserve 0ohm, and NC when PD.	Added R720,R763~R766 0 ohm for LPC signals.	X00-2
				Chagne from X00-2 to X00-3		
22	29	8/15/2007	EE	Reserve the caps for any noise coupling issue happening.	Depop C338 and close Q37. Added C920 and close EMC1423.	X00-3
23	29	8/15/2007	EE	Added Q77 2N7002 isolation circuit.	Added Q77 instead R406 ohm and change Q42 from +3.3V_SUS to +3.3V_RUN.	X00-3
24						X00-3
25						X00-3
26	49	8/15/2007	P	FAE Suggetion for OCP setting	Change PR97 from 7.15K to 8.45K	X00-3
27	52	8/15/2007	P	Charge pump from +5V LDO, might cause high ripple voltage	Add P112 to reduce ripple voltage	X00-3
28	52	8/15/2007	P	PR219 no need such hige rating component	Change PR219 from 0805 to 0603 and remove one	X00-3

PROJECT : Hepburn	DOC. NO. : 204	REV: X00			QUANTA COMPUTER
APPROVED BY : Cory Lin	CHECKED BY: Cory Lin	DRAWN BY : Leo Tseng	DATE : Aug. 13 , 2007	SHEET 1 OF 11	

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29	52	8/15/2007	P	PC474 should populated for filter	Populate PC474	X00-3
30	52	8/15/2007	P	Reserve feedback circuit for testing	Add PR169 and PR218	X00-3
31	28	8/15/2007	EE	No need to implement shunt resistors for HDMI on M82S Discrete only.	Remove R159,R160,R163,R164 180 ohm.	X00-3
32	36	8/15/2007	EE	Follow vendor review. Added RC to include more different memory card.	Pop C860 270pF and added C921 0.01u, R456 150k.	X00-3
33	19,27	8/15/2007	EE	Follow M82-S reference schematic. Discrete only.	There is double PU for CRT DDC.Remove R522,R519 2.2k and change R520,R486,R521,R485 to 2.2k.	X00-3
				Chagne from X00-3 to X00-4		
34	42	8/16/2007	P	Load switch voltage drop is out of spec.	Change PQ13 from SI4800BDY to SI4856BDY	X00-4
35	42	8/16/2007	P	Load switch voltage drop is out of spec.	Change PQ29 from SI4800BDY to SI4336DY	X00-4
36	42	8/16/2007	P	Load switch voltage drop is out of spec.	Change PQ20 from SI4800BDY to SI4336DY	X00-4
37	5,29	8/16/2007	EE	Follow SMSC feedback.	Change C341 from 220p to 2200p and depop C212	X00-4
38	15	8/16/2007	EE	Follow ATI SB700 checklist.	Change C518,C519,C529 to 1uF, C524 to 22uF.	X00-4
39	15	8/16/2007	EE	Follow ATI SB700 checklist.	Change C496,C494,C495,C489 to 2.2uF.	X00-4
			EE	**Chagne from X00-4 to X00-5**		
40	19	8/17/2007	EE	Move CLK_VGA_27M_SS to GPIO16 and reserved it for spread spectrum. Discrete only.	Reserved R196 0 ohm for EXT CLK GEN.	X00-5
41	29,43,44	8/17/2007	EE	Added ESD diode.	Added D35,D36,D37,D38	X00-5
42	38	8/17/2007	EE	Follow ATI SB700 checklist.	Change C96,C208 from 0.01u to 0.1u to meet SB700 checklist.	X00-5
				Chagne from X00-5 to X00-6		
43	8	8/20/2007	EE	Change VGAH(V)SYNC to INT_VGAH(V)SYNC from PU to PD for disable side prot memry. Discrete only.	Depop R497 and pop R500.	X00-6
44	25	8/20/2007	EE	It's no need to reserve 49.9 ohm and change R243,R235 from 47.5 to 0 ohm, depop R236 261/F.	Remove 49.9 ohm, change R243,R235 from 47.5 to 0 ohm and depop R236.	X00-6
45	25	8/20/2007	EE	Follow FAE feedback. Added Decoupling caps for U16's VDDIO.	Added Decoupling caps C685,C924~C930 and L93 for U16's VDDIO.	X00-6
46	12,20	8/20/2007	EE	Follow ATI FAE recommend. Set GPIO to turn on M82 +3.3V_DELAY. Discrete only.	Connect GFX_RUN_ON from SB700 pin AC6 to R513.	X00-6
47	12,14,18	8/20/2007	EE	Follow ATI FAE recommend to change the M82 reset signal for power express. Discrete only.	Added R458,R457,D39,D40,R205 for power express.	X00-6
48	14	8/20/2007	EE	Follow ATI FAE recommend.	Change R421,R429 from 10k to 2.2k.	X00-6
49	34	8/20/2007	EE	Follow BCM FAE recommend to remove external RC termination.	Remove (R690~R697 and C794~C797)	X00-6
50	33	8/20/2007	EE	Follow BCM recommend to add the required grounding for all the package signals and powertermination.	Add U29 pin 69 thermal GND pad.	X00-6
				Chagne from X00-6 to X00-7		
51	42	8/21/2007	EE	Follow Card reader vendor recommend to add PU resistor for IRQ_SERIRQ.	Add R267 10K ohm to pull-up +3.3V_RUN.	X00-7
52	41	8/21/2007	EE	There is no +3.3V_RTC_LDO power rail.	Change the +3.3V_RTC_LDO to +3.3V_ALW.	X00-7
53	21	8/21/2007	EE	Added +1.8V_GFX power rail for M82-S power express Discrete only.	Change the M82-S +1.8V_RUN to +1.8V_GFX and added +1.8V_GFX power switch.	X00-7
54	51	8/21/2007	P	Connect thermal pad to AGND	Add pin15 to AGND	X00-7
55	52	8/21/2007	P	Preserve component for MAX8778	Add PC115	X00-7
56	54	8/21/2007	P	Connect thermal pad to AGND	Add pin15 to AGND	X00-7

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57	55	8/21/2007	P	Change feedback resistor for 1.1V output	Change PR66 to 63.4K	X00-7
58	55	8/21/2007	P	Change feedback resistor for +1.1V_GFX_PCIE output	Change PR68 to 4.53K	X00-7
				Chagne from X00-7 to X00-8		
59	12,35	8/22/2007	EE	Change the PCI_PIRQD to PCI_PIRQB. ATI must use INTH#/GPIO36 to control M82-S reset signal.	Change the PCI_PIRQD to PCI_PIRQB and move to U31.AC4	X00-8
60	12	8/22/2007	EE	ATI use INTH#/GPIO36 (PE_GPIO0) to control M82-S reset signal.	Added PE_GPIO0 on U31.AE3 to control M82-S reset.	X00-8
61	48	8/22/2007	P	Pin define is wrong.	Change JABT1 pin define	X00-8
62	48	8/22/2007	P	Remove AC_OFF function	Remove PQ24	X00-8
63	9	8/23/2007	EE	Remove resistor for RX780.	Remove R490,R42,R84,R32,R63,R112,R119,R131 for RX780.	X00-8
64	22	8/23/2007	EE	Added level shift on M82-S thermal IC SMBUS2. Discrete only.	Added Q88,Q87 and remove R144,R137 0 ohm.	X00-8
65	34	8/23/2007	EE	Follow FM6 to modify the +3.3V_LAN power source form +3.3V_ALW to +3.3V_SUS.	Depop +3.3V_ALW to +3.3V_LAN switch circuit and added R767 to connect +3.3V_SUS to +3.3V_LAN.	X00-8
66	55	8/23/2007	EE	We don't use RUNPWROK and use GFX_RUN_ON to turn on GFX power.	Remove PR169.	X00-8
67	12	8/23/2007	EE	Follow ATI checklist. Reserved J13 for Rubuto.	Added J13 for Rubuto system.	X00-8
68	34	8/23/2007	EE	Follow Dell. Change the LED signals.	LINKLED connect to G_LED.SPD100LED connect to amber LED.	X00-8
				Chagne from X00-8 to X00-9		
69	9	8/24/2007	EE	Check the CLK GEN vendor (RT&CLG). They don't have PA_RS7X0A1 issue.	Remove R29,R33,R37,R34 and connect to GPP_SB_REFCLK directly from CLK GEN SB_SRC CLK.	X00-9
70	26	8/24/2007	EE	Added OR gate to support backlight from EC and NB.	Added U225,C932 and pop R464.	X00-9
71	45	8/24/2007	EE	Added AND gate in system reset circuit.	Remove R204,R209 and added U226,U227.	X00-9
72	31,32	8/24/2007	EE	Change the audio to IDT STAC9228/92HD73C.	Change the audio to IDT STAC9228/92HD73C.	X00-9
73	25	8/24/2007	EE	Follow RS780 check list to change the ferrite bead for CLK GEN power.	Change the L34 ,L93 and added L107,L108 to FBM-11-160808-601A10T	X00-9
74	11	8/24/2007	EE	Follow RS780 check list.	Added C997,C998 1U and change L15 from 4.7U to 1U.	X00-9
				Chagne from X00-9 to X00-10		
75	22,26	8/28/2007	EE	Added reduce WWAN interference solution.	Added C1001~C1008, R835,R836.	X00-10
76	42,43	8/28/2007	EE	Chagne MEDIA_INT to active low. MEDIA_INT# need pull-up +3.3V_ALW.	Move R217 to page 43, pull-up to +3.3V_ALW. Added RC to MEDIA_INT#.	X00-10
77	44	8/28/2007	EE	Chagne power switch and sniffer switch power rail.	Chagne R461,R21 from +RTC_CELL to +3.3V_ALW.	X00-10
78	42,53	8/28/2007	EE	Chagne CPU_VCORE_PWRGD pull up power rail.	Chagne PR35 from +3.3V_ALW to +3.3V_SUS and depop R574.	X00-10
79	43	8/28/2007	EE	Added the NUM, CAP low active circuit and swap keyboard signals.	Added CP7 and Q80,Q82,Q81,Q83,R834,R832.	X00-10
80	39	8/28/2007	EE	Depop debug board's 0 ohm.	Depop debug board's 0 ohm R322,R685,R720,R763,R764,R765,R766	X00-10
81	30	8/28/2007	EE	ODD SATA is not need +3.3V_RUN. Remove +3.3V_RUN decoup caps for ODD SATA.	Remove R745,R747,R307,R744,R313.	X00-10
82	46	8/28/2007	P	USB Charger Function	Add +5V_ALW to +5V_SUS Load Switch for USB Charger	X00-10
83	52	8/28/2007	P	USB Charger Function	Change +5V_ALW to +5V_ALW2	X00-10
84	52	8/28/2007	P	USB Charger Function	Change +5V_SUS to +5V_ALW	X00-10
85	52	8/28/2007	P	USB Charger Function	Remove PR213 and PD1	X00-10

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86	52	8/28/2007	P	USB Charger Function	Change +3.3V_DL to +5V_DL	X00-10
87	51	8/28/2007	P	FAE Suggest 237K for 300KHz frequency	Change from 178K to 237K	X00-10
88	54	8/28/2007	P	FAE Suggest 237K for 300KHz frequency	Change from 178K to 237K	X00-10
89	49	8/28/2008	P	FAE Suggest connect to GND	Change to connect to GND	X00-10
90	49	8/28/2008	EE	Follow AMD recomment. Added buffer work around circuit to NB_PWRGD.	Added U234 buffer to seperate NB_PWRGD and WD_PWRGD.	X00-10
				Chagne from X00-10 to X00-11		
91	25	8/29/2008	EE	Added MINI3CLK_REQ#,EXPRESSCARD_REQ# pull-up resistor.	Added R837,R859 10k pull up to +3.3V_RUN.	X00-11
92	9	8/29/2008	EE	pop R495 and remove PANEL_BKEN from RS7800	pop R495 0 ohm and remove R806.	X00-11
93	28,44	8/29/2008	EE	Add ESD, Choke for Biometric and HDMI.	Add ESD3 for Biometric and L109~L112 for HDMI.	X00-11
94	24	8/29/2008	EE	Follow AMD recomment. Change the voltage level for hybrid IC SEL pin.	Change R89 from 0 ohm to 8.2k ohm.	X00-11
95	10	8/30/2008	EE	Add work around TPS72501 to create 1.35V to RS780 VDDHTTX power rail. RS780 Rev.A11 only.	Used TPS72501 to create +1.35V_HT_VCC and added L113 for option.	X00-11
96	9	8/30/2008	EE	Added PD resistor 2.7k for INT_EN_LCDVDD.	Added R863 2.7k for INT_EN_LCDVDD.	X00-11
97	10	8/30/2008	EE	Follow ATI checklist. Added L114 to reduce noise for VDDPCIE.	Added L114 to VDD_PCIE.	X00-11
98	46	8/30/2007	P	For more suitable RDSON	Change to SI4800BDY	X00-11
99	48	8/30/2007	P	Footprint is not correct	Change to new footprint "BAT-200045MR009H577ZR-9P-R-V"	X00-11
100	49	8/30/2007	P	MPL104S-0R9 is not PSL	Change to MPC1040LR88	X00-11
101	52	8/30/2007	P	Reserve GPIO for USB Charger	Add 5V_ALW_ON GPIO for USB charger enable	X00-11
102	52	8/30/2007	P	FAE suggest connect to +3.3V_DL	Connect to +3.3V_DL	X00-11
103	52	8/30/2007	P	For Uni material	Change to 0.1u/0603	X00-11
104	53	8/30/2007	P	MPL73-3R3 is not PSL	Change to MPLC0730L3R3	X00-11
105	53	8/30/2007	**P**	FAE Suggest PR43=18K, PR42=100K	Change to PR43=18K, PR42=100K	X00-11
106	53	8/30/2007	**P**	FAE Suggest PR198=16.2K, PR205=4.02K	Change to PR198=16.2K, PR205=4.02K	X00-11
107	53	8/30/2007	**P**	FAE Suggest PR199=16.2K, PR200=4.02K	Change to PR199=16.2K, PR200=4.02K	X00-11
108	54	8/30/2007	**P**	MPL73-4R7 is not PSL	Change to MPLC0730L4R7	X00-11
109	54	8/30/2007	**P**	For High=1.0, Low=0.9 Output	Change PR207 to 20K/F	X00-11
110	55	8/30/2007	**P**	For High=1.0, Low=0.9 Output	Change PR64 to 69.8K/F	X00-11
111	56	8/30/2007	P	For High=1.0, Low=0.9 Output	Change PR66 to 22.6K/F	X00-11
				Chagne from X00-11 to X00-12		
112	32	8/31/2007	EE	Follow ME feedback. Used MIC connector in MB side.	Pop J14 and remove M1	X00-12
113	19,20	8/31/2007	EE	Follow ATI FAE. Reserved GFX thermal protect function.	Added U241,Q98,Q99,R870,R871.R872	X00-12
114	53	9/1/2007	P	FAE Suggest to remove sense resistor for saving space	Remove PR179, PR180	X00-12
115	53	9/1/2007	P	FAE Suggest to remove sense resistor for saving space	Remove PR194, PR195	X00-12

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116	55	9/01/2008	P	Change to hight rating mosfet for 9.4A	Change to FDS8880_NL	
117	55	9/01/2008	P	Change to hight rating mosfet for 9.4A	Change to FDS6676AS_NL	
118	55	9/01/2008	P	Change to hight rating mosfet for 9.4A	Change to SIL104R-1R0	
119	47	9/01/2008	P	Cancel this function. It's no use.	Remove PR74, PQ15	
120	29	9/01/2008	EE	Follow FAE feedback. Pull up resistor to +3.3V_SUS.	Added R877 10k ohm to pull up +3.3V_SUS.	X00-12
121	36	9/01/2008	EE	Follow FAE feedback. Added C1032 270p_NC to SD_CD#	Added C1032 270p_NC to CON5 pin 2 SD_CD#.	X00-12
122	15	9/01/2008	EE	Follow AMD feedback. Change SB700 VDD power rail from +1.2V_RUN to +1.2V_ALW_SUS.	Added L90 and connect to +1.2V_ALW_SUS. Depop L39.	X00-12
123	24	9/01/2008	EE	Follow AMD feedback. Change R89 from 0 ohm to 8.2k ohm.	Change R89 from 0 ohm to 8.2k ohm.	X00-12
124	26	9/01/2008	EE	Reserved caps for reduce SMBUS1 overshoot and under shoot.	Reserved C1011,C1012 47p in J1 pin5,6	X00-12
125	52	9/03/2008	P	Reserved for MAX8778	Add PR114	X00-12
126	55	9/03/2008	P	Reserved snubber	Add PR245, PC211	X00-12
127	42	9/03/2008	EE	ITE 8512 FAE concern pin 126,pin 23,pin 4,pin 15 have leakage .	Added D43~D46 to U13 pin 126, pin 23, pin 4, pin 15.	X00-12
128	5	9/03/2008	EE	Follow AMD feedback. Added 2 * MOSFET for CPU_PWRGD_SVID_REG level shift.	Added Q100,R881and modify Q76 to gate by CPU_PWRGD.	X00-12
				Chagne from X00-12 to X00-13		X00-12
129	49,51,54	9/04/2008	P	Dell suggest to add 0.1u cap near IC feedback pin to reduce feedback noise.	Add 0.1u cap	X00-13
130	51	9/04/2008	P	FAE suggest to add PR460,PC451 and PQ115 for voltage shift function.	Aadd PR460,PC451 and PQ115 for voltage shift function.	X00-13
131	19	9/04/2008	EE	Follow ATI feedback.	Reserved R889 1M for Y2 27Mhz.	X00-13
132	42	9/04/2008	EE	Added D47	Added D47 to connect WRST# and THERM_STP#	X00-13
133	33	9/04/2008	EE	Reserved BCM5784M SUPER_IDDQ circuit.	Reserved R888 20k ohm.	X00-13
134	9,27	9/04/2008	EE	Add RS780 CRT I2C function.	Connect U13 pin E8,F8 to CRT DDC bus.	X00-13
135	9,28	9/04/2008	EE	Add RS780 HDMI I2C function.	Connect U13 pin A8,B8 to HDMI DDC bus and Added level shift(R886,R887,Q101,Q102)	X00-13
				Chagne from X00-13 to X00-14		
136	31	9/05/2008	EE	Added 4 * 0 ohm for EMI.	Added R898~R901 to JSPK1.	X00-14
137	55	9/05/2008	EE	Footprint is different with PL9 sepc.	Change PL9 footprint to SIL104.	X00-14
138	24	9/05/2008	EE	ATI has update power express circuit.	Added R890~R897and depop Q3~Q10.	X00-14
139	13,39	9/05/2008	EE	Added SB_USBP8 to WLAN.	Added L115, R902, R903.	X00-14
140				**Chagne from X00-14 to X00-15**		X00-15
141	43	9/06/2008	EE	Added KB BACKLITE power switch circuit.	Added Q104,Q103,C1033,C1034,R190,R907,R908,R909 to option +KB_LED power source.	X00-15
142	43	9/06/2008	EE	Added TP power rail and change LID_SW# power rail	Added C385 and PU to +3.3V_SUS to JP2.5. Change R455 to +3.3V_ALW.	X00-15
				Chagne from X00-15 to X00-16		
143	9	9/11/2008	EE	There is on need pull-up resistor to work around for RS780 A11.	Depop R416	X00-16
144	44	9/12/2008	EE	There is not work in DC IN LED for SSI build.	Depop Q16, Q17, R44, R45	X00-16

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Item	Page#	Date	T	Issue Description	Solution Description	Rev
145	9	9/14/2007	EE	Follow ATI FAE feedback. Change the RS780 strap pin.	Depop R419 and pop R420.	X00-16
				Chagne from X00-16 to X01-1		
1	9	10/01/2007	EE	Follow ATI FAE feedback. Don't need LDT_STOP#, CPU_LDT_REQ# level shift.	Depop the level shift Q52,Q3,R341,R39 and added R637, R638 0 ohm.	X01-1
2	9	10/01/2007	EE	Follow ATI FAE feedback. Change the RS780 debug strap pin.	Added R639 3k ohm to PU +3.3V_RUN and depop the R349.	X01-1
3	12	10/26/2007	EE	Follow AMD SCL.	Depop R694 1M ohm.	X01-1
P1	52	10/30/2007	P	ALW_PWRGD_3V_5V is dummy net	Remove PR178,PR182 and change connect to +3.3V_ALW	X01-1
P2	51	10/30/2007	P	NB_VCORE will OVP when voltage switch	Follow FAE suggestion to put PR178 and PR182	X01-1
P3	47,48	10/30/2007	P	+5V_ALW issue when USB charger disabled in S5	Change +5V_ALW to +5V_ALW2 for below terminal PU6.8, PR115,PR22, PD4.1, PD5.1	X01-1
P4	47	10/30/2007	P	To solve EE noise made by charger	Change charger output Cap 10U/25V from X6S to X5R CAP (PN: CH6104K9207)	X01-1
P5	51	10/30/2007	P	Change capacitor to resistor for reserve pull low	Change PC11 to PR214	X01-1
P6	54	10/30/2007	P	1.2V_ALW_SUS_ON is floating	Add a resistor PR215 to pull low	X01-1
P7	47,51,52	10/30/2007	P	SI4810 EOL Issue	Change PQ40,PQ2,PQ22,PQ26 to SI4812	X01-1
P8	51,54	10/30/2007	P	To reduce Vo jitter issue	Change PC57 and PC86 to 220u/2.5V/ESR15	X01-1
4	10	10/31/2007	EE	RS780M change form A11 to A12 and don't need work around.	Pop L54 and Depop L55,C488,U20,R381,R382,C491.	X01-1
5	13,37,42	10/31/2007	EE	Added Express card power enable on SB700. It's for Express card hot plug.	Change U30.B8 from USB_OC5# to EXPRCRD_PWREN# and connect to CN2.	X01-1
6	28	10/31/2007	EE	Follow ANT HDMI detect circuit.	Added Q80, and remove R336,D19	X01-1
7	32	10/31/2007	EE	Added +3.6V_CAMERA Camera power circuit	Added U43,C741,C743,C742,R640,R642.Remove C527. Modify JCAMERA1 pin define and L58 power rail.	X01-1
8	38	10/31/2007	EE	Added USB charge circuit for leakage.	Added Q81,R643,U44,U45.	X01-1
9	42	10/31/2007	EE	Swap U5.31 NUM_LED# and U9.98 KB_BACKLITE_EN	Swap U5.31 NUM_LED# and U5.98 KB_BACKLITE_EN	X01-1
10	44	10/31/2007	EE	Depop SNIFFER_YELLOW LED circuit. and Swap WIRELESS_ON/OFF#, SNIFFER_PWR_SW# circuit.	Depop R377,Q55,Q54,R371 and Swap R376 SNIFFER_PWR_SW#, R313 WIRELESS_ON/OFF# signals	X01-1
11	43	10/31/2007	EE	Change KB_LED pwoer ciruit.	Pop R507, Add Q82 and Depop R513,R512,Q71,Q70,C589,C579,R505 and modify J4 pin define.	X01-1
12	9,45	10/31/2007	EE	Depop SB700 A11 WD_PWRGD work around circuit.	Depop U11,C222,R186 and pop R186,R344	X01-1
13	42	11/01/2007	EE	Change GPIO and remove SNIFFER_YELLOW function.	Move 5V_ALW_ON to U5.83, Move NUM_LED# to U5.88 and remove R377,Q55,Q54,R371	X01-1
				Chagne from X01-1 to X01-2		
14	5,12	11/01/2007	EE	+5V_ALW issue when USB charger disabled in S5	Change R87,R306 from +5V_ALW to +5V_ALW2.	X01-2
15	33,34	11/02/2007	EE	Change BCM5787M to BCM5784M.	Change BCM5787M to BCM5784M.	X01-2
16	31	11/02/2007	EE	Change STAC9228 to 92HD73C.	Change STAC9228 to 92HD73C.	X01-2
17	14	11/05/2007	EE	Follow ATI SCL and feedback.	Added R644 0 ohm connect U30.C6 TEMP_COMM to GND.	X01-2
18	13,39	11/05/2007	EE	Change WLAN from USB port 8 to USB port 4.	Change WLAN from SB_USBP8+/- to SB_USBP4+/- and Move to U30.B12,U30.A12.	X01-2
19	38	11/05/2007	EE	Co-lay USB Q-switch and 0 ohm	Reserved R645~R648 0 ohm with U44 pin 2,3,5,6,U45 pin 2,3,5,6.	X01-2
P1	52	10/30/2007	P	ALW_PWRGD_3V_5V is dummy net	Remove PR178,PR182 and change connect to +3.3V_ALW	X01-2
P2	51	10/30/2007	P	NB_VCORE will OVP when voltage switch	Follow FAE suggestion to put PR178 and PR182	X01-2

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Item	Page#	Date	T	Issue Description	Solution Description	Rev
P3	47,48	10/30/2007	P	+5V_ALW issue when USB charger disabled in S5	Change +5V_ALW to +5V_ALW2 for below terminal PU6.8, PR115,PR22, PD4.1, PD5.1	X01-2
P4	47	10/30/2007	P	To solve EE noise made by charger	Change charger output Cap 10U/25V from X6S to X5R CAP (PN: CH6104K9207)	X01-2
P5	51	10/30/2007	P	Change capacitor to resistor for reserve pull low	Change PC11 to PR214	X01-2
P6	54	10/30/2007	P	1.2V_ALW_SUS_ON is floating	Add a resistor PR215 to pull low	X01-2
P7	47,51,52	10/30/2007	P	SI4810 EOL Issue	Change PQ40,PQ2,PQ22,PQ26 to SI4812	X01-2
P8	51,54	10/30/2007	P	To reduce Vo jitter issue	Change PC57 and PC86 to 220u/2.5V/ESR15	X01-2
P9	46	11/05/2007	P	Modify +5V_SUS load switch	Remove PQ12	X01-2
P10	53	11/05/2007	P	FAE suggest to reserve	Add PR241	X01-2
P11	54	11/05/2007	P	Modify current limit value	Change PR228 from 10K to 5.9K	X01-2
P12	49,51,53,54,55	11/05/2007	P	To solve power good glitch issue	Connect IC power to +5V_ALW2	X01-2
P13	49	11/05/2007	P	Set tracking discharge mode	PR206 populate and PR208 NC	X01-2
P14	52	11/05/2007	P	5V_ALW_ON pull low at initial state	Add PR218	X01-2
P15	53	11/05/2007	P	CPU_VCORE_ENABLE pull low at initial state	Add PR219	X01-2
20	42,44,48	11/06/2007	EE	Remove DC IN LED circuit and change signal name DCIN_DETECT_LED# to CHIPSET_ID1.	Remove R37,Q10,Q9,R69 and change U5.99 signal name DCIN_DETECT_LED# to CHIPSET_ID1.	X01-2
P16	51,54	11/06/2007	P	For space saving.	Remove PC2,PC81.	X01-2
21	42	11/07/2007	EE	Add BID1 to EC pin98	Connect R130,R131 to U5.98	X01-2
22	25,42	11/07/2007	EE	Remove double pull-up resistor.	Remove R107,RP2,R455	X01-2
				Chagne from X01-2 to X01-3		
23	5	11/09/2007	EE	Solve glitch from CPU_PWRGD.	Added C744 0.1uF on CPU_PWRGD.	X01-3
24	14,42	11/09/2007	EE	Solve S5 leakage.	Connect L38 from +3.3V_ALW to +3.3V_SUS and remove R92 for SIO_SLP_S5#.	X01-3
P17	49,51,54	11/12/2007	P	Reserve for solving giltch issue caused by IC power rail	Add PR220,PR221,PR222,PR223,PR224	X01-3
P18	51	11/12/2007	P	Follow AMD FAE suggest +NB_VCORE dynamic voltage design	Remove PQ7,PC13,PR19,PR12	X01-3
P19	54	11/12/2007	P	To solve jitter issue	Change PL2 from 4R7 to 3R3	X01-3
25	43	11/14/2007	EE	Follow ANT reference to solve S3 leakage.	Change R389,R99,R97,R90 pull-up from +1.8V_SUS to +1.8V_RUN.	X01-3
26	12	11/15/2007	EE	Solve CPU_PWRGD voltage too low(+1.5V).	Change Q36 from MMBT3904 to FDV301N.	X01-3
27	42	11/15/2007	EE	Check with power team and EC. The charge IC INP pin can be read with EC ADC function.	Pop R86 0 ohm and depop R91 0 ohm.	X01-3
28	14,33,36,42	11/15/2007	EE	Follow XTAL vendor feedback to change the XTAL caps.	Change C139, C149 to 18pF. C394 to 27pF. C556 to 22pF, C658, C659 to 12pF	X01-3
29	43	11/15/2007	EE	Follow Dell recommend.	Change R507 0 ohm to FS3.	X01-3
30	31,32	11/16/2007	EE	Follow IDT recommend to change caps for batter Audio Precision.	Change C730, C724, C622, C620 from 1uF to 2.2uF.	X01-3
31	5,12	11/16/2007	EE	Follow ANT 3.2 reference schematic to remove CPU_PROCHOT# level shift.	Remove R441, R436, Q65.	X01-3
				Chagne from X01-3 to X01-4		
32	9	11/19/2007	EE	Update RS780M symbol.	Update U16 symbol.	X01-4

PROJECT : Hepburn	DOC. NO. : 204	REV: X01		QUANTA COMPUTER
APPROVED BY : Cory Lin	CHECKED BY: Cory Lin	DRAWN BY : Leo Tseng	DATE : Sep. 19 , 2007	SHEET 7 OF 11

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P20	46	11/19/2007	P	Reduce RUN/SUS PW switch circuit.	Remove PR(89,93,197,200,170,168,68,66) and change PQ(34,51,49,20) to 2N7002W-7-F.	X01-4
P21	46	11/19/2007	P	Reduce RUN/SUS PW switch circuit.	PC58,PC32,PC43,PC51,PC30,PC36,PC175 from 10U/1206 to 0.1U/0603	X01-4
33	44	11/19/2007	EE	Sniffer should be during S5.Dell define our Sniffer switch need to stay 'ON' after the WiFi can be enable.	change R313 to +3.3V_ALW.	X01-4
34	14	11/19/2007	EE	Follow AMD SB700 design guideline to add series resistor.	Add R649, R650 4.99 ohm at U39 AD13,AE13 SATA_TX3+/- for ESATA signals.	X01-4
35	14	11/20/2007	EE	Depop Q-switch function on PT build.	Depop Q81,R643,U44,U45 and pop R645~R648.	X01-4
P22	47	11/20/2007	P	UL schemaitc are going to be replaced by EC control	UL schemaitc components are NC	X01-4
P23	49	11/20/2007	P	Reduce Jitter	Change PC183 and PC184 from 330u/ESR15 to 220u/ESR25	X01-4
P24	52	11/20/2007	P	PC168 is no use for schematic	Remove PC168	X01-4
P25	53	11/20/2007	P	To reduce input ripple	Add PC190 and PC191	X01-4
P26	47,48	11/20/2007	P	2nd Source suggest to change	Change PD8 to RB500V-40 , PQ4 to FDV301N	X01-4
36	42	11/21/2007	EE	Follow ITE feedback to reserve caps for ITE8512JX.	Add C745, R651 to U9 pin 12.	X01-4
37	38	11/21/2007	EE	Change USB Q-switch power rail from +3.3V_RUN to +3.3V_SUS.	Change U44 pin 8, U45 pin 8 from +3.3V_RUN to +3.3V_SUS, Q81 pin2 from RUN_ON to SUS_ON.	X01-4
38	33,34	11/21/2007	EE	Modify LAN 1000 LED circuit to solve BCM5784M LED issue.	Add D36,R774 to solve BCM5784M 1000 LED issue.	X01-4
39	28	11/22/2007	EE	Change HDMI connector symbol.	Change CN3 connector symbol.	X01-4
40	28	11/22/2007	EE	Remove these 20K ohm resistors because it is for desktop design or codec internal headphone amplifier.	Depop R519, R521, R532, and R547.	X01-4
41	38	11/22/2007	EE	For EMI solution to pop choke.	Pop L19,L20 and depop R78, R83,R85,R88.	X01-4
42	50	11/23/2007	EE	Base on RS780M T13 timing. +1.8V_RUN rise need before then +1.1V_RUN.	Change PR62 from 0 ohm to 200k ohm and depop PC41 from 0.01u to 0.1u.	X01-4
P27	53	11/24/2007	P	EMI Solution	Add PC168,PC192,PC193,PC197,PC198,PC199,PC194,PC195,PC196	X01-4
P28	48	11/24/2007	P	For ESD protect	EMI Suggestion PD6 populate	X01-4
43	25	11/23/2007	EE	EMI Solution	EMI Suggestion C565, C575 populate	X01-4
44	12	11/23/2007	EE	EMI Solution	EMI Suggestion C292 populate	X01-4
45	32	11/23/2007	EE	EMI Solution	EMI Suggestion C573,C584,C595,C603 change form 220pF to 470pF.	X01-4
46	32	11/23/2007	EE	IDT had found out the resonance on portA and suggested change 220pF to 47pF for EMI.	Change C621, C609 from 220pF to 47pF.	X01-4
				Chagne from X01-4 to X01-5		
47	41	11/26/2007	EE	BT1 connector pin define is different before.	Change BT1 pin 2 to GND, pin 1 to +RTC.	X01-5
48	42	11/26/2007	EE	Sniffer power switch needs to wake up EC, when battery only. So it needs to use WUI pin.	Swap U5.108 SNIFFER_PWR_SW# and U5.35 WIRELESS_ON/OFF#	X01-5
49	36	11/26/2007	EE	EMI Solution	Add C758~C760 27pF for EMI solution.	X01-5
P29	51	11/26/2007	P	FAE suggest to reserve RC to slow down voltage switch	add the R/C at PQ53 to slow down PQ53 switcher to against OVP, and remove R/C in front of PQ5	X01-5
P30	51,54	11/26/2007	P	Got more performance for jitter issue	Change PC97 and PC72 from 220u/2.5V/ESR15 to 220u/4V/ESR40	X01-5
50	32	11/26/2007	EE	Follow FAE suggest.	Change U9 pin 21~25 to NC.	X01-5
51	38	11/26/2007	EE	EMI Solution	Populate ESD3 for EMI suggest.	X01-5
52	5	11/26/2007	EE	Solve system shut down issue from CPU_THERMTRIP#.	Add Q83,Q84,R776,C761 and connect H_THERMTRIP# to 3V, 5V ALW circuit.	X01-5

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53	12	11/28/2007	EE	Follow ANT 3.2 schematic.	Depop R576, R574.	X01-5
54	33	11/28/2007	EE	Follow Broadcom FAE feedback. BCM5784M CLKREQ# can't work.	Pop R434 ohm and depop R431 4.7k ohm before CLKREQ can work.	X01-5
				Chagne from X01-5 to X02-1		
1	5	12/28/2007	EE	Follow AMD Griffin sighting Dec 18.pdf to reserve resistor for system hang or shut downboot issue.	Add R777,R778 and pop R121 300 ohm resistor for system hang or shut down issue.	X02-1
2	43	1/2/2008	EE	Change MMB pin 1 power source to 5V_ALW to fix LED flash issue when AC/Bat plug in.	Change JP1.1 from +5V_ALW2 to +5V_ALW.	X02-1
3	43	1/4/2008	EE	Change Num, Cap power rail to +5V_RUN to fix Num, Cap LED flash issue when AC/Bat plug in.	Change Q57~Q60, R380, R379 power rail to +5V_RUN.	X02-1
4	38	1/10/2008	EE	Fulfill Reliability team request.	Connect JUSB1.8 to USB_BACK_PWR.	X02-1
5	43	1/11/2008	EE	Avoid system can enter S3 mode but wake up fail problem.	Change the lid switch IC power source from 3.3V_SUS to 3.3V_ALW.	X02-1
6	32	1/11/2008	EE	Change L61 to 22 ohm. It will help DMIC_CLK_L performance.	Change L61 to from 0 ohm to 22 ohm.	X02-1
7	38	1/11/2008	EE	Remove USB charge function.	Remove R643, Q81, U44, U45, R645~R648.	X02-1
8	38	1/14/2008	EE	Follow AMD AN_SB700AB5. Added re-driver IC to increase signal stress for ESATA.	Remove R649,R650 4.99 ohm. Added U50 3211B,R769~R784 0 ohm, C762~C765 0.1u, C766~C769 0.01u.	X02-1
9	28	1/14/2008	EE	Modify HDMI detect circuit.	Added Q85,R785,R786.	X02-1
10	42	1/14/2008	EE	Change EC from ITE8512IX to ITE8512JX. The pin12 need connect to 0.1uF, 1uF.	Change R651 to C770 0.1u, pop C745 1u for EC ITE8512 rev change.	X02-1
11	12,14,	1/16/2008	EE	Follow DELL recommand to void the PCICLK5 emission issue even AMD solved it in BIOS code	Move R232 22 ohm and CLK_PCI_PCCARD signal form PCICLK5 to PCICLK1.	X02-1
P1	47	1/21/2008	P	Change to X6S material due to not support pulse charge	Change PC105, PC99, PC96 and PC108 to X6S material	X02-1
P2	51	1/21/2008	P	Derating team suggest for WCETPA	Change PR10 from 10K ohm to 11.8K ohm.	X02-1
P3	52	1/21/2008	P	Derating team suggest for WCETPA	Change PR188 from 294K ohm to 340K ohm.	X02-1
P4	54	1/21/2008	P	Derating team suggest for WCETPA	Change PR205 from 5.9K ohm to 7.5K ohm.	X02-1
				Chagne from X02-1 to X02-2		
12	28	1/29/2008	EE	DDC Capacitance over spec 50pf. We will add level shift circuit to reduce Capacitance.	Change Q1, Q2 to FDV301N. It will reduce the DDC Capacitance.	X02-2
13	15	1/29/2008	EE	Follow AMD feedback.IDE and Flash Interface Not Implemented: Decoupling caps not used.	Depop C258, C296, C298, C274, C295.	X02-2
14	15	1/29/2008	EE	Follow AMD SB700 checklist item 1-34, 1-35.	Change L35 to BLM21PG221SN1D, C330 to 10U.	X02-2
15	9, 13	1/29/2008	EE	Follow AMD RS780M item 8-7, SB700 item 7-1, 7-2 checklist to reserve PD resistor.	Reserve R787 4.7k ohm and R788, R789 10k ohm.	X02-2
16	12	1/30/2008	EE	Follow AMD SB700 checklist item 12-4 to depop RP34.	Depop RP34 8.2k ohm.	X02-2
17	9	1/30/2008	EE	Follow AMD SB700 checklist item 24-17. Change PU resistor to 300 ohm.	Change R344 4.7k to 300 ohm.	X02-2
18	13	1/30/2008	EE	Follow AMD SB700 checklist item 24-24. Depop PU resistor.	Depop R264 10k ohm.	X02-2
19	11	1/30/2008	EE	Follow AMD checklist item 17-2, 17-4, 17-6. Depop termination resistors.	Depop R343, RP22~RP32 47 ohm.	X02-2
20	9	1/30/2008	EE	Follow AMD checklist item 18-31. Depop PD resistors.	Depop R338 100k ohm.	X02-2
21	28	1/30/2008	EE	Follow EMI suggest to pop comon mode choke for HDMI.	Pop L1~L4 EXC24CG240Uand depop R6, R9, R11, R12, R14, R16, R18, R19 ohm.	X02-2
22	28	1/30/2008	EE	HDMI test Voltage level fail.	Change R317, R321, R325, R326, R330~R333 to 715 ohm.	X02-2
23	38	1/30/2008	EE	Follow EMI suggest to pop comon mode choke for USB.	Pop L19, L20 DLP11SN900HL2L. Depop R78, R83, R85, R88 0 ohm.	X02-2
24	29	1/30/2008	EE	OTP change to 85C.THERM_ALERT#_C and SYS_SHDN# leakage will affect OTP thermal limit.	Change OTP resistor to 10k, 6.8k ohm. Add D35 to prevent leakage.	X02-2

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25	27	1/31/2008	EE	Follow EMI suggest to pop caps for CRT.	Pop C455, C462, C476 22pF and C456, C464, C478, C79, C72 10pF.	X02-2
26	9,25	2/1/2008	EE	Follow CLK Gen vendor feedback to solve EA fail.	Change R146 to 43.2 ohm, R40 to 0 ohm, C50 to 49.9 ohm.	X02-2
P5	53	2/1/2008	EE	To solve transient response fail	Change PC17~PC19, PC21, PC22, PC26.	X02-2
27	27	2/1/2008	EE	Follow AMD AN_RS780G1.pdf. DAC Output Imbalance.	Change R48, R370 to 140 ohm.	X02-2
28	42	2/12/2008	EE	Use ITE8512 pin 22 detect SB_AZ_CODEC_RST# to mute speaker pop noise.	Connect SB_AZ_CODEC_RST# and U5 pin 22.	X02-2
29	5	2/12/2008	EE	Follow ANT 4.1d. CPU_TEST23_TSTUPD need PD 300 ohm.	PD R790 300 ohm for CPU_TEST23_TSTUPD.	X02-2
30	43	2/12/2008	EE	Add JP1 pin 10 to +3.3V_ALW, let +3.3V_ALW get lower drop voltage on MMB side.	Add JP1 pin 10 to +3.3V_ALW.	X02-2
P6	50,52	2/13/2008	P	Change PU2, PU5 and PU8 VCC power rail to reduce S5 power consumption.	Change PJP2.1 to +3.3V_SUS and add PR226~PR229 0 ohm.	X02-2
31	38	2/22/2008	EE	Pop ESATA re-driver for stress ESATA signals on formal build.	Pop C726~C765, U50, depop R781~R784 and change C654, C655, C768, C769 to 0.01u.	X02-2
32	31	2/22/2008	EE	Dell recommend change caps for IDT AP test on formal build.	Change C712, C713 to 6800pF.	X02-2
				Chagne from X02-2 to A00-1		
1	42	3/14/2008	EE	Chagne board ID for A00.	Pop R129 and depop R128.	A00-1
P1	53	3/14/2008	P	Follow EMI suggest.	Pop PC192, PC198, PC195 0.01u and PC193, PC196, PC199 0.1u.	A00-1
2	31,32	3/14/2008	EE	Need meet WLP4.0 : 1. Add 2.2K-ohm resistors to prevent amplifier clipping.	Add R791~R794 2.2k ohm.	A00-1
				Need meet WLP4.0 : 2. Add 220PF capacitors to allow proper dynamic range measurent.	Add C771, C772 220pF and pop C726, C727 to 220pF.	A00-1
3	7~11,27,30, 38,45	3/17/2008	EE	Follow Safety request. Change USB power control IC location same as FM6 location.	Swap U7, U19 and U10, U16 location. U7 and U16 are 2062AD. Swap D33 and D18, R218 and R570	A00-1
4	38	3/18/2008	EE	TI can't finish some necessary legal submission for new 2062AD. Change to old part 2062DR.	Change U7, U16 to 2062DR (AL002062005).	A00-1
5	15,49,50,51 ,52,55	3/18/2008	EE	Remove Power Jump for QT build.	Remove PJP1~PJP4, PJP6~PJP8, PJP10~PJP13, PJP15~PJP17 and short PJP9.	A00-1
6	38	3/18/2008	EE	Follow QSMC request to remove USB co-lay 0 ohm.	Remove R78, R83, R85, R88 0 ohm.	A00-1
7	38	3/18/2008	EE	Change the USB Power Jump to short pad fp.	Change PJP5, PJP14 fp to SHORT-10A.	A00-1
8	42	3/19/2008	EE	Follow IT8512JX glitch.doc FA report. Depop 1uF for ITE8512JX pin 12.	Depop C745 1uF.	A00-1
10	38	3/20/2008	EE	Pericom request. Add 300ohm to reduce output swing, change AC caps to 2.2nF and set EQ to GND.	Add R795 300 ohm. Chagne C95,C96,C654,C655,C766~C769 to 2.2nF and PD U50 pin1, pin10 to GND.	**A00-1**
11	14, 43	3/20/2008	EE	Follow Dell request. Add LED KB BK detect function.	Add R796 100k ohm , PD R797 200k ohm to J4 pin2 and connect to U30 pin G6.	A00-1
12	28	3/20/2008	EE	Change to FDV301N will pass HDMI 7-12 HDMI detect test.	Change Q80 from MM3904 to FDV301N.	A00-1
13	59	3/26/2008	EE	Follow EMI team request, add two EMI SPRING near sniffer switch area and HDMI connector.	Add PV1 near SW1 and PV2 near CN3.	A00-1
14	32	3/26/2008	EE	Follow IDT request, change 220pF to 270pF will over 80db on DTM.	Change C609, C621, C771, C772 from 220pF to 270pF.	**A00-1**
15	36	3/27/2008	EE	Follow EMI team request, add a 27p capacitor for 8 in 1 card reader.	Pop C760 27pF for EMI.	A00-1
P2	48	3/27/2008	EE	Follow EMI team request, add two set of 1000pF, 0.01uF, 0.1uF on J8 +DCIN_JACK , -DCIN_JACK.	Add PC200~PC202 on J8 +DCINI_JACK, PC203~PC205 on J8 -DCIN_JACK.	A00-1
P3	49, 51	3/27/2008	EE	Follow EMI team request, pop PR3, PC3 for NB_VCORE and pop PR213, PC188 for +1.8V_SUS	pop PR3, PC3 for NB_VCORE and pop PR213, PC188 for +1.8V_SUS	A00-1
16	5, 42	3/27/2008	EE	Use BID1 to control CPU_PROCHOT#. When system need change state to P1 by HTC.	Add Q86 2N7002W-7-F and remove R420 0 ohm for use BID1 to control CPU_PROCHOT#.	A00-1