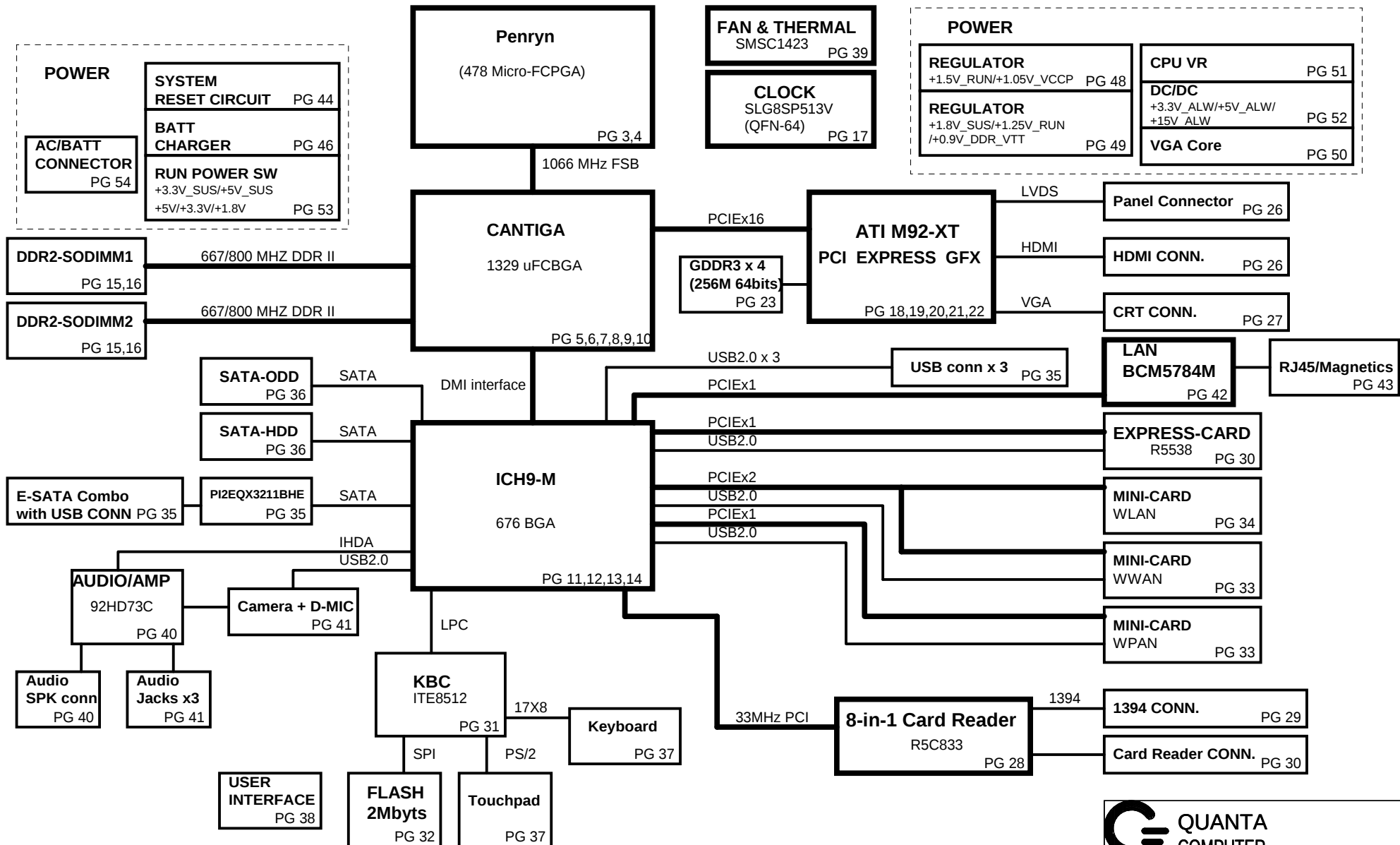


FM8 Hanks Intel Discrete GFX

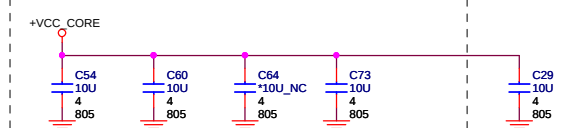
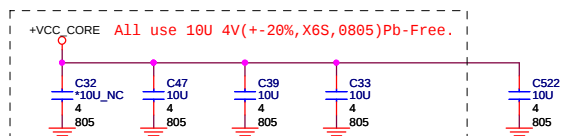
VER : 3A
PWA:W021J
PWB:W018J



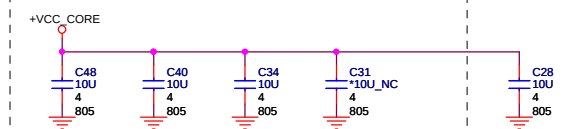
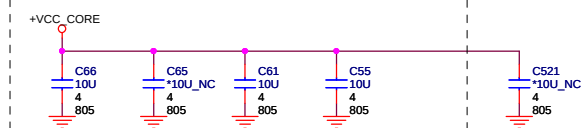
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	Penryn
5-10	Cantiga
11-14	ICH9M
15-16	DDRII SO-DIMM(200P)
17	Clock Generator
18-23	M92-S2-XT
24	BLANK PAGE
25	BLANK PAGE
26	LCD CONN / HDMI CONN
27	CRT CONN
28	5C833/PCI
29	IEEE1394
30	Express/Card Reader
31	SIO (ITE8512)
32	FLASH / RTC
33	MINI-Card (WPAN, WWAN)
34	MINI-Card (WLAN)
35	USB
36	SATA (HDD & CD_ROM)
37	TP / KEYBOARD
38	SWITCH / LED
39	FAN / THERMAL
40	Azelia CODEC
41	AUDIO CONN
42	LAN (RTL8111B/8111C)
43	LAN RJ-45 / TRANSFORM
44	System Reset Circuit
45	Blank Page
46	Changer (MAX8731A)
47	Blank Page
48	1.05VCCP & 1.5VRUN
49	1.8VSUS & 0.9VTT
50	VGA_M82
51	CPU_ISL6266 (2PHASE)
52	MAX8744 (+5V,3.3V)
53	Run Power Switch
54	DCin & Batt
55	PAD & SCREW
56	EMI CAP
57	SMBUS BLOCK
58	Power Block Diagram

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,50,51,52	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,31,32,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	38,48,49,52,53,54	LARGE POWER	RUN_ON	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,35,36,38,50,51,52,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,26,30,38,43,48,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53	SODIMM POWER	SUS_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	14,20,26,27,36,37,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,6,8,9,11,12,13,14,15,17,20,22,26,27,28,30,31,33,34,36,39,40,41,42,51,53	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,31,33,34,48,53	CALISTOGA/ICH9 POWER	RUN_ON	
+1.2V_LOM	+1.25V	42	LOM POWER	+3.3V_LAN	
+1.1V_GFX_PCIE	+1.1V	21,50	VGA POWER	RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN	
+5V_HDD	+5V	36	HDD Power	HDDC_EN	

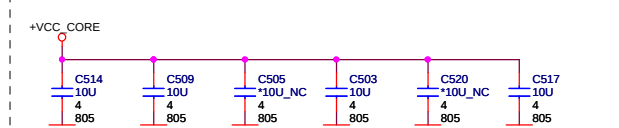
GND PLANE	PAGE	DESCRIPTION
 GND_CHG	46	
 GND_1.05V	47	
 GND_VGA	50	
 GND_SIGNAL	51	
 AGND_DC/DC	52	
 GND	ALL	



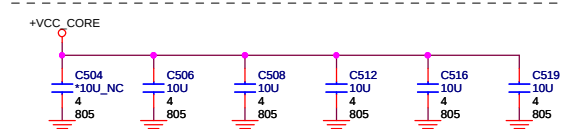
8 inside cavity, north side, secondary layer.



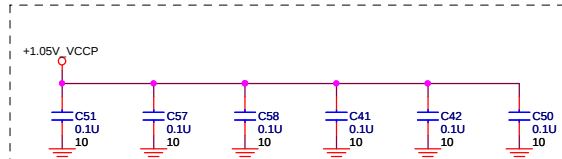
8 inside cavity, south side, secondary layer.



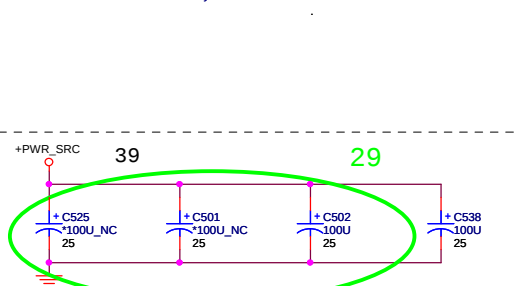
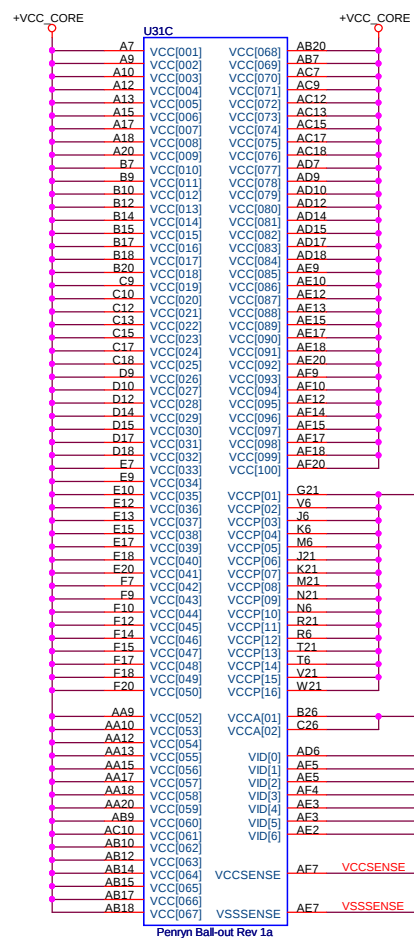
6 inside cavity, north side, primary layer.



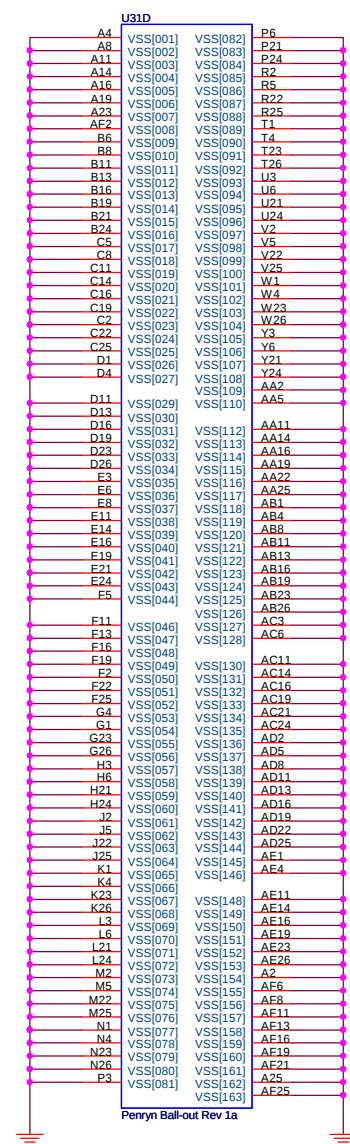
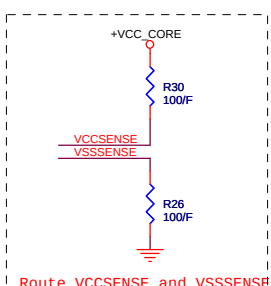
6 inside cavity, south side, primary layer.

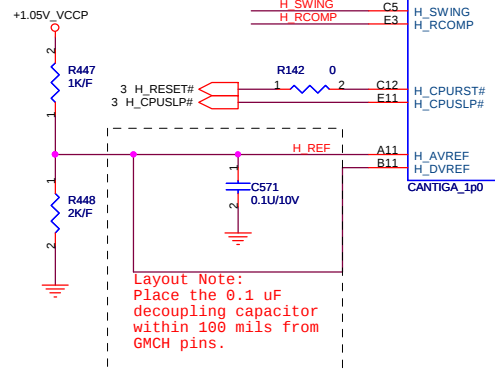
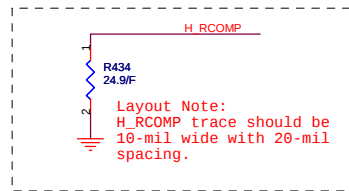
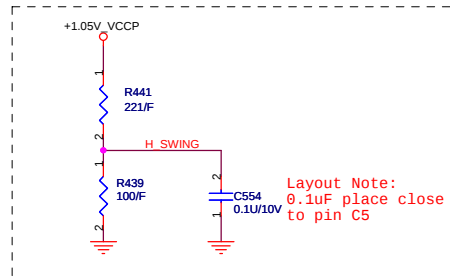


Layout out:
Place these inside socket cavity on North side secondary.



Layout Note:
Need to add 100uF cap on PWR_SRC for cap singing.
Place on PWR_SRC near +VCC CORE.





H D#0	F2	H D# 0
H D#1	G8	H D# 1
H D#2	F8	H D# 2
H D#3	E6	H D# 3
H D#4	G2	H D# 4
H D#5	H6	H D# 5
H D#6	H2	H D# 6
H D#7	F6	H D# 7
H D#8	D4	H D# 8
H D#9	H3	H D# 9
H D#10	M9	H D# 10
H D#11	M11	H D# 11
H D#12	J1	H D# 12
H D#13	J2	H D# 13
H D#14	N12	H D# 14
H D#15	J6	H D# 15
H D#16	P2	H D# 16
H D#17	L2	H D# 17
H D#18	R2	H D# 18
H D#19	N9	H D# 19
H D#20	L6	H D# 20
H D#21	M5	H D# 21
H D#22	J3	H D# 22
H D#23	N2	H D# 23
H D#24	R1	H D# 24
H D#25	N5	H D# 25
H D#26	N6	H D# 26
H D#27	P13	H D# 27
H D#28	N8	H D# 28
H D#29	L7	H D# 29
H D#30	N10	H D# 30
H D#31	M3	H D# 31
H D#32	Y3	H D# 32
H D#33	AD14	H D# 33
H D#34	Y6	H D# 34
H D#35	Y10	H D# 35
H D#36	Y12	H D# 36
H D#37	Y14	H D# 37
H D#38	Y7	H D# 38
H D#39	W2	H D# 39
H D#40	AA8	H D# 40
H D#41	Y9	H D# 41
H D#42	AA13	H D# 42
H D#43	AA9	H D# 43
H D#44	AA11	H D# 44
H D#45	AD11	H D# 45
H D#46	AD10	H D# 46
H D#47	AD13	H D# 47
H D#48	AE12	H D# 48
H D#49	AE9	H D# 49
H D#50	AA2	H D# 50
H D#51	AD8	H D# 51
H D#52	AA3	H D# 52
H D#53	AD3	H D# 53
H D#54	AD7	H D# 54
H D#55	AE14	H D# 55
H D#56	AE3	H D# 56
H D#57	AC1	H D# 57
H D#58	AE3	H D# 58
H D#59	AC3	H D# 59
H D#60	AE11	H D# 60
H D#61	AE8	H D# 61
H D#62	AG2	H D# 62
H D#63	AD6	H D# 63

HOST

H_A#_3	A14	H_A#3
H_A#_4	C15	H_A#4
H_A#_5	F16	H_A#5
H_A#_6	H13	H_A#6
H_A#_7	C18	H_A#7
H_A#_8	M16	H_A#8
H_A#_9	J13	H_A#9
H_A#_10	P16	H_A#10
H_A#_11	R16	H_A#11
H_A#_12	N17	H_A#12
H_A#_13	M13	H_A#13
H_A#_14	E17	H_A#14
H_A#_15	P17	H_A#15
H_A#_16	F17	H_A#16
H_A#_17	G20	H_A#17
H_A#_18	B19	H_A#18
H_A#_19	J16	H_A#19
H_A#_20	E20	H_A#20
H_A#_21	H16	H_A#21
H_A#_22	J20	H_A#22
H_A#_23	L17	H_A#23
H_A#_24	A17	H_A#24
H_A#_25	B17	H_A#25
H_A#_26	L16	H_A#26
H_A#_27	C21	H_A#27
H_A#_28	J17	H_A#28
H_A#_29	H20	H_A#29
H_A#_30	B18	H_A#30
H_A#_31	K17	H_A#31
H_A#_32	B20	H_A#32
H_A#_33	F21	H_A#33
H_A#_34	K21	H_A#34
H_A#_35	L20	H_A#35

H_ADS#_0	H12	H_ADS# 3
H_ADSTB#_0	B16	H_ADSTB# 3
H_ADSTB#_1	G17	H_ADSTB#1 3
H_BNR#_0	A9	H_BNR# 3
H_BPR#_0	F11	H_BPR# 3
H_BRO#_0	G12	H_BRO# 3
H_DEFER#_0	E9	H_DEFER# 3
H_DBSY#_0	B10	H_DBSY# 3
H_PLI_CLK#	AH7	CLK_MCH_BCLK 17
H_DPWR#_0	AH6	CLK_MCH_BCLK# 17
H_DRDY#_0	J11	H_DPWR# 3
H_HIT#_0	E9	H_DRDY# 3
H_HITM#_0	H9	H_HIT# 3
H_LOCK#_0	E12	H_HITM# 3
H_TRDY#_0	H11	H_LOCK# 3
H_TRDY#_1	C9	H_TRDY# 3

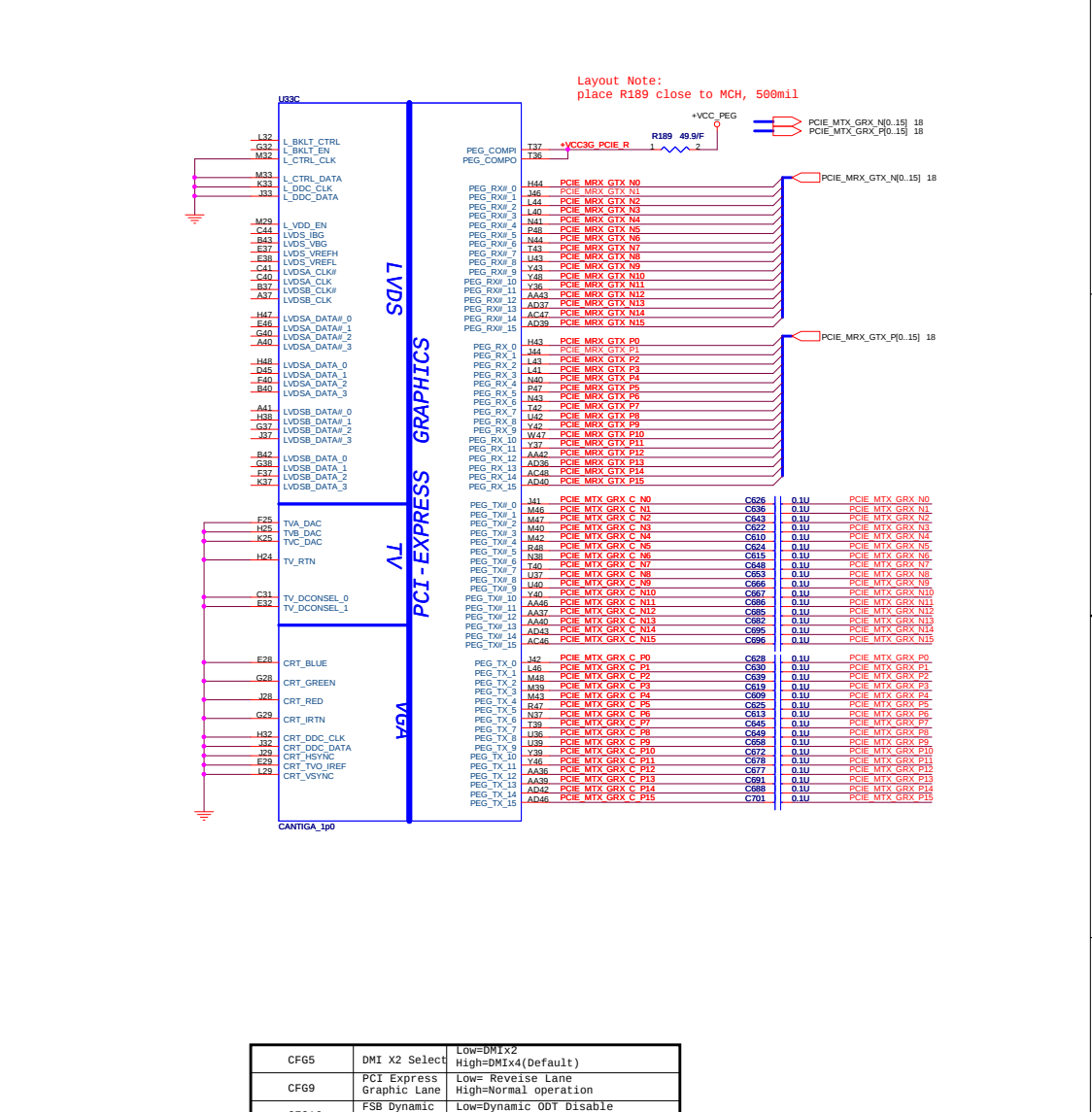
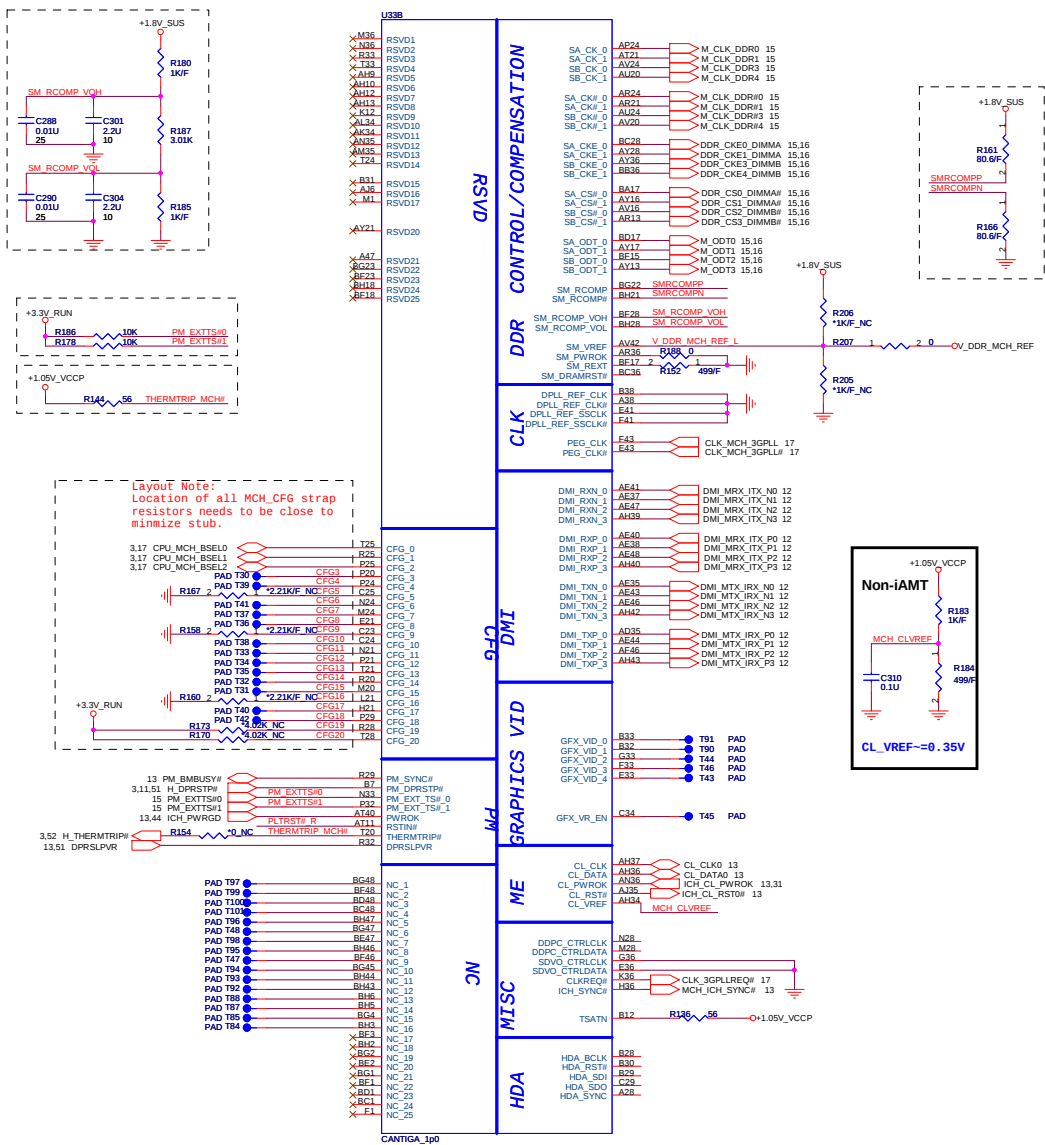
H_DINV#_0	J8	H_DINV#0 3
H_DINV#_1	L3	H_DINV#1 3
H_DINV#_2	Y13	H_DINV#2 3
H_DINV#_3	Y1	H_DINV#3 3

H_DSTBN#_0	L10	H_DSTBN#0 3
H_DSTBN#_1	M7	H_DSTBN#1 3
H_DSTBN#_2	AA5	H_DSTBN#2 3
H_DSTBN#_3	AE6	H_DSTBN#3 3

H_DSTBP#_0	L9	H_DSTBP#0 3
H_DSTBP#_1	M8	H_DSTBP#1 3
H_DSTBP#_2	AA6	H_DSTBP#2 3
H_DSTBP#_3	AE5	H_DSTBP#3 3

H_REQ#_0	B15	H_REQ#0 3
H_REQ#_1	K13	H_REQ#1 3
H_REQ#_2	F13	H_REQ#2 3
H_REQ#_3	B13	H_REQ#3 3
H_REQ#_4	B14	H_REQ#4 3

H_RS#_0	B6	H_RS#0 3
H_RS#_1	E12	H_RS#1 3
H_RS#_2	C8	H_RS#2 3



CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High= Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIe1 is operational (defaults) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present



QUANTA
COMPUTER

File		Cantiga (H0ST)	
Size	Document Number	Rev	
FMB		2A	
Date:	Friday, November 21, 2008	Sheet	6 of 58

15 DDR_A_D[0..63]

U33D
DDR A D0 AJ38 SA_DQ_0
DDR A D1 AJ41 SA_DQ_1
DDR A D2 AN38 SA_DQ_2
DDR A D3 AM38 SA_DQ_3
DDR A D4 AJ36 SA_DQ_4
DDR A D5 AJ40 SA_DQ_5
DDR A D6 AM44 SA_DQ_6
DDR A D7 AM42 SA_DQ_7
DDR A D8 AN43 SA_DQ_8
DDR A D9 AN44 SA_DQ_9
DDR A D10 AU40 SA_DQ_10
DDR A D11 AT38 SA_DQ_11
DDR A D12 AN41 SA_DQ_12
DDR A D13 AN39 SA_DQ_13
DDR A D14 AU44 SA_DQ_14
DDR A D15 AU42 SA_DQ_15
DDR A D16 AV39 SA_DQ_16
DDR A D17 AY44 SA_DQ_17
DDR A D18 BA40 SA_DQ_18
DDR A D19 BD43 SA_DQ_19
DDR A D20 AV41 SA_DQ_20
DDR A D21 AY43 SA_DQ_21
DDR A D22 BB41 SA_DQ_22
DDR A D23 RC40 SA_DQ_23
DDR A D24 AY37 SA_DQ_24
DDR A D25 RD38 SA_DQ_25
DDR A D26 AV37 SA_DQ_26
DDR A D27 AT36 SA_DQ_27
DDR A D28 AY38 SA_DQ_28
DDR A D29 BB38 SA_DQ_29
DDR A D30 AY36 SA_DQ_30
DDR A D31 AW36 SA_DQ_31
DDR A D32 BD13 SA_DQ_32
DDR A D33 AU11 SA_DQ_33
DDR A D34 BC11 SA_DQ_34
DDR A D35 BA12 SA_DQ_35
DDR A D36 AU13 SA_DQ_36
DDR A D37 AV13 SA_DQ_37
DDR A D38 BD12 SA_DQ_38
DDR A D39 BC12 SA_DQ_39
DDR A D40 BB9 SA_DQ_40
DDR A D41 BA9 SA_DQ_41
DDR A D42 AU10 SA_DQ_42
DDR A D43 AV9 SA_DQ_43
DDR A D44 BA11 SA_DQ_44
DDR A D45 BD9 SA_DQ_45
DDR A D46 AV8 SA_DQ_46
DDR A D47 BA6 SA_DQ_47
DDR A D48 AV5 SA_DQ_48
DDR A D49 AV7 SA_DQ_49
DDR A D50 AT9 SA_DQ_50
DDR A D51 AN8 SA_DQ_51
DDR A D52 AU5 SA_DQ_52
DDR A D53 AU6 SA_DQ_53
DDR A D54 AT5 SA_DQ_54
DDR A D55 AN10 SA_DQ_55
DDR A D56 AM11 SA_DQ_56
DDR A D57 AM5 SA_DQ_57
DDR A D58 A19 SA_DQ_58
DDR A D59 AJ8 SA_DQ_59
DDR A D60 AN12 SA_DQ_60
DDR A D61 AM13 SA_DQ_61
DDR A D62 AJ11 SA_DQ_62
DDR A D63 AJ12 SA_DQ_63

CANTIGA_1p0

DDR SYSTEM MEMORY A

SA_BS_0
SA_BS_1
SA_BS_2
SA_RAS#
SA_CAS#
SA_WE#

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7
SA_DQS#_0
SA_DQS#_1
SA_DQS#_2
SA_DQS#_3
SA_DQS#_4
SA_DQS#_5
SA_DQS#_6
SA_DQS#_7

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14

BD21 DDR A BS0
BG18 DDR A BS1
AT25 DDR A BS2
BB20 DDR A RAS#
BD20 DDR A CAS#
AY20 DDR A WE#

AM37 DDR A DM0
AT41 DDR A DM1
AY41 DDR A DM2
AU39 DDR A DM3
BB12 DDR A DM4
AY6 DDR A DM5
AT7 DDR A DM6
AJ5 DDR A DM7

AJ44 DDR A DQS0
AT44 DDR A DQS1
BA43 DDR A DQS2
RC37 DDR A DQS3
AW12 DDR A DQS4
BC8 DDR A DQS5
AU8 DDR A DQS6
AM7 DDR A DQS7

AJ43 DDR A DQS#0
AT43 DDR A DQS#1
BA44 DDR A DQS#2
BD37 DDR A DQS#3
AY12 DDR A DQS#4
BD8 DDR A DQS#5
AU9 DDR A DQS#6
AM8 DDR A DQS#7

BA21 DDR A MA0
BC24 DDR A MA1
BG24 DDR A MA2
BH24 DDR A MA3
BG25 DDR A MA4
BA24 DDR A MA5
BD24 DDR A MA6
BG27 DDR A MA7
BE25 DDR A MA8
AW24 DDR A MA9
BC21 DDR A MA10
BG26 DDR A MA11
BH26 DDR A MA12
BH17 DDR A MA13
AY25 DDR A MA14

15 DDR_B_D[0..63]

U33E
DDR B D0 AK47 SB_DQ_0
DDR B D1 AH42 SB_DQ_1
DDR B D2 AP42 SB_DQ_2
DDR B D3 AP46 SB_DQ_3
DDR B D4 AJ46 SB_DQ_4
DDR B D5 AJ48 SB_DQ_5
DDR B D6 AM48 SB_DQ_6
DDR B D7 AP48 SB_DQ_7
DDR B D8 AU47 SB_DQ_8
DDR B D9 AU46 SB_DQ_9
DDR B D10 BA48 SB_DQ_10
DDR B D11 AY48 SB_DQ_11
DDR B D12 AT47 SB_DQ_12
DDR B D13 AR47 SB_DQ_13
DDR B D14 BA47 SB_DQ_14
DDR B D15 RC47 SB_DQ_15
DDR B D16 RC46 SB_DQ_16
DDR B D17 BC44 SB_DQ_17
DDR B D18 BC43 SB_DQ_18
DDR B D19 BE43 SB_DQ_19
DDR B D20 BE45 SB_DQ_20
DDR B D21 BC41 SB_DQ_21
DDR B D22 BE40 SB_DQ_22
DDR B D23 BE41 SB_DQ_23
DDR B D24 BC38 SB_DQ_24
DDR B D25 BE38 SB_DQ_25
DDR B D26 BH35 SB_DQ_26
DDR B D27 BG35 SB_DQ_27
DDR B D28 BH40 SB_DQ_28
DDR B D29 BG39 SB_DQ_29
DDR B D30 BG34 SB_DQ_30
DDR B D31 BH34 SB_DQ_31
DDR B D32 BH14 SB_DQ_32
DDR B D33 BG12 SB_DQ_33
DDR B D34 BH11 SB_DQ_34
DDR B D35 BG8 SB_DQ_35
DDR B D36 BH12 SB_DQ_36
DDR B D37 BE11 SB_DQ_37
DDR B D38 BE8 SB_DQ_38
DDR B D39 BG7 SB_DQ_39
DDR B D40 BC5 SB_DQ_40
DDR B D41 BC6 SB_DQ_41
DDR B D42 AY3 SB_DQ_42
DDR B D43 AY1 SB_DQ_43
DDR B D44 BE6 SB_DQ_44
DDR B D45 BE5 SB_DQ_45
DDR B D46 BA1 SB_DQ_46
DDR B D47 BD3 SB_DQ_47
DDR B D48 AV2 SB_DQ_48
DDR B D49 AU3 SB_DQ_49
DDR B D50 AR3 SB_DQ_50
DDR B D51 AN2 SB_DQ_51
DDR B D52 AY2 SB_DQ_52
DDR B D53 AV1 SB_DQ_53
DDR B D54 AP3 SB_DQ_54
DDR B D55 AR1 SB_DQ_55
DDR B D56 AL1 SB_DQ_56
DDR B D57 AL2 SB_DQ_57
DDR B D58 AJ1 SB_DQ_58
DDR B D59 AH1 SB_DQ_59
DDR B D60 AM2 SB_DQ_60
DDR B D61 AM3 SB_DQ_61
DDR B D62 AH3 SB_DQ_62
DDR B D63 AJ3 SB_DQ_63

CANTIGA_1p0

DDR SYSTEM MEMORY B

SB_BS_0
SB_BS_1
SB_BS_2
SB_RAS#
SB_CAS#
SB_WE#

SB_DM_0
SB_DM_1
SB_DM_2
SB_DM_3
SB_DM_4
SB_DM_5
SB_DM_6
SB_DM_7

SB_DQS_0
SB_DQS_1
SB_DQS_2
SB_DQS_3
SB_DQS_4
SB_DQS_5
SB_DQS_6
SB_DQS_7
SB_DQS#_0
SB_DQS#_1
SB_DQS#_2
SB_DQS#_3
SB_DQS#_4
SB_DQS#_5
SB_DQS#_6
SB_DQS#_7

SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
SB_MA_7
SB_MA_8
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14

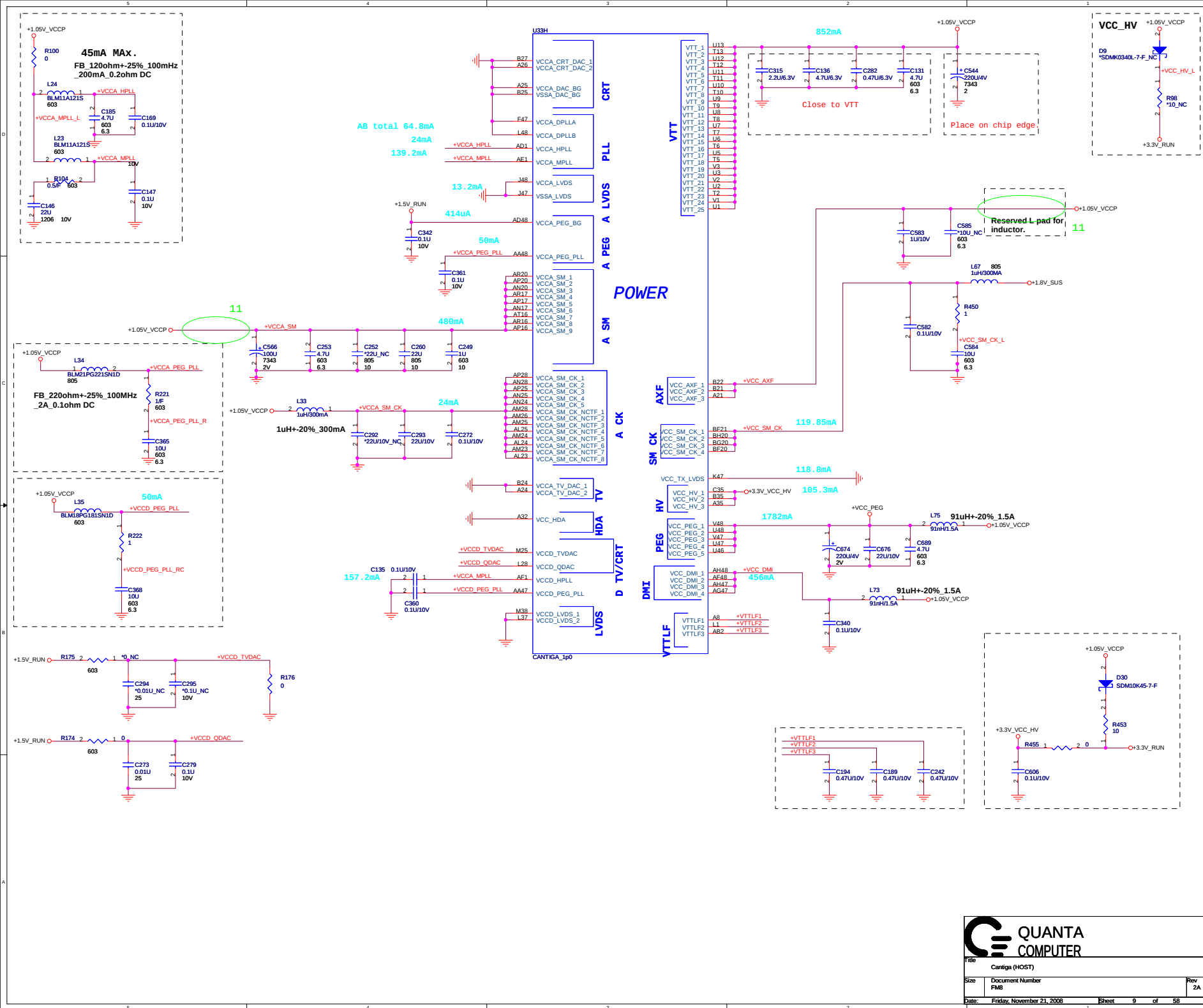
BC16 DDR B BS0
BB17 DDR B BS1
BB33 DDR B BS2
AU17 DDR B RAS#
BG16 DDR B CAS#
BF14 DDR B WE#

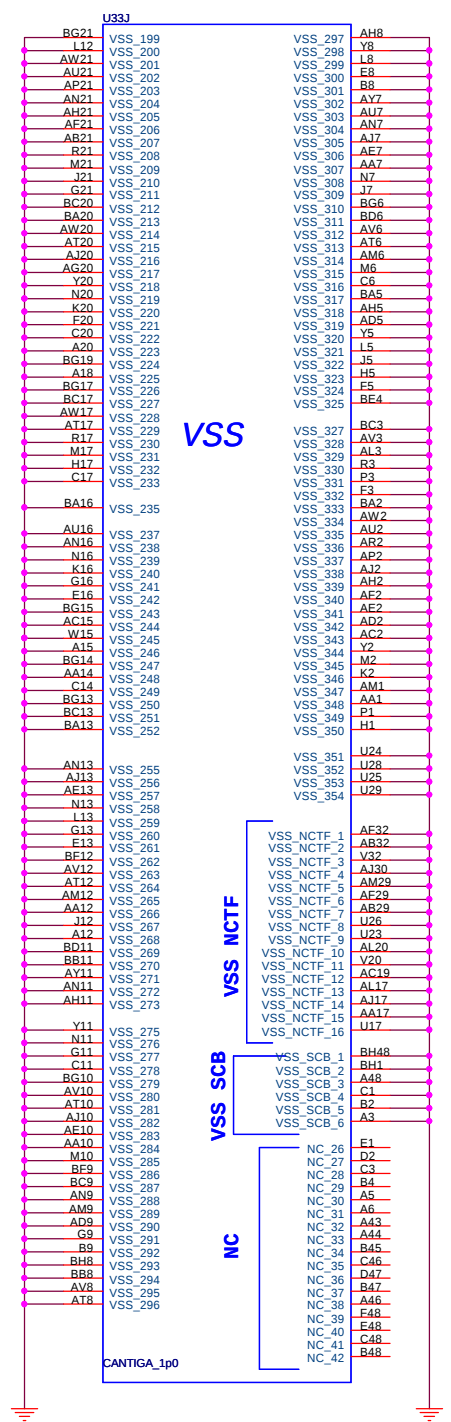
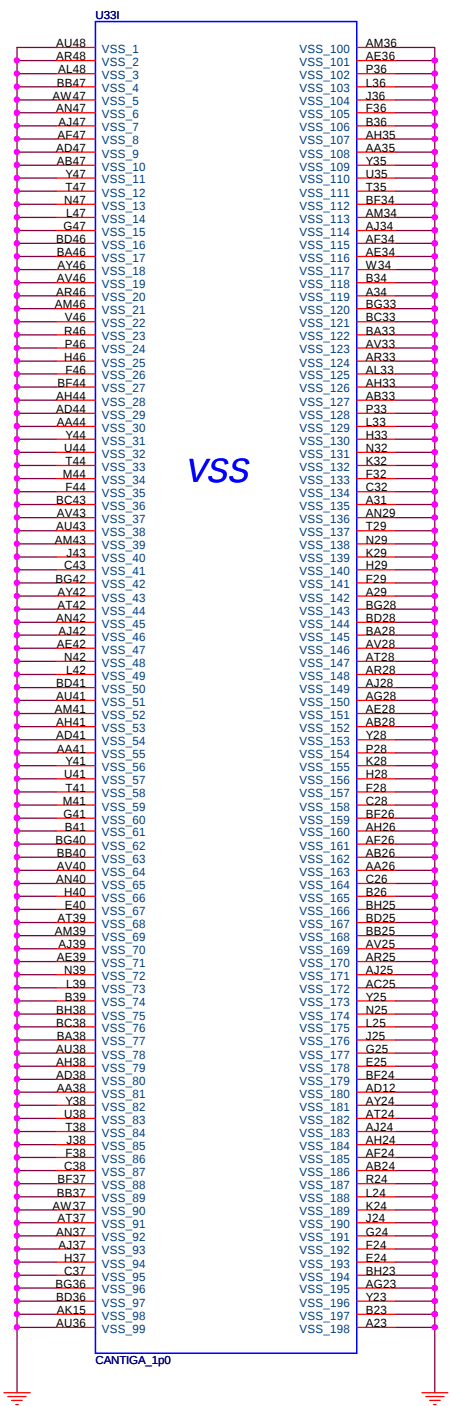
AM47 DDR B DM0
AY47 DDR B DM1
BD40 DDR B DM2
BE35 DDR B DM3
BG11 DDR B DM4
BA3 DDR B DM5
AP1 DDR B DM6
AK2 DDR B DM7

AL47 DDR B DQS0
AV48 DDR B DQS1
BG41 DDR B DQS2
BG37 DDR B DQS3
BH9 DDR B DQS4
BB2 DDR B DQS5
AU1 DDR B DQS6
AN6 DDR B DQS7
AL46 DDR B DQS#0
AY47 DDR B DQS#1
BH41 DDR B DQS#2
BH37 DDR B DQS#3
BG9 DDR B DQS#4
BC2 DDR B DQS#5
AT2 DDR B DQS#6
AN5 DDR B DQS#7

BA25 DDR B MA0
BC25 DDR B MA1
AU25 DDR B MA2
AW25 DDR B MA3
BB28 DDR B MA4
AU28 DDR B MA5
AW28 DDR B MA6
AT33 DDR B MA7
BD33 DDR B MA8
BB16 DDR B MA9
AW33 DDR B MA10
AY33 DDR B MA11
BH15 DDR B MA12
AU33 DDR B MA13
AU33 DDR B MA14



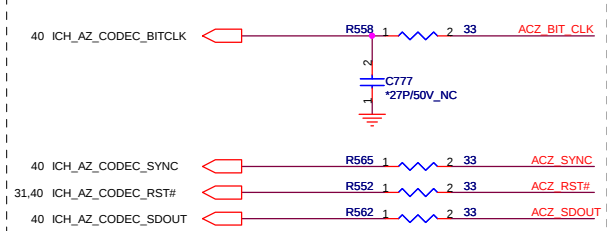
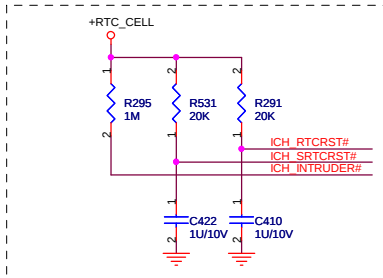
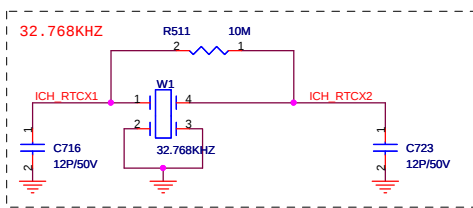




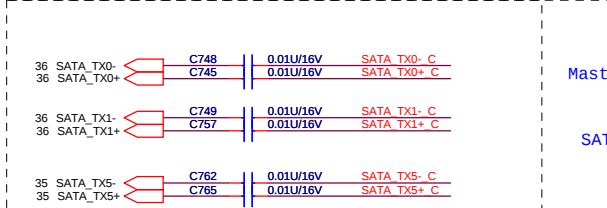


QUANTA
COMPUTER

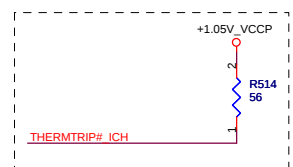
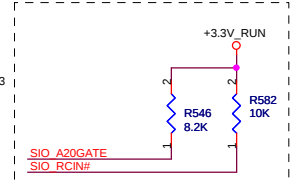
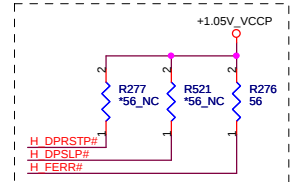
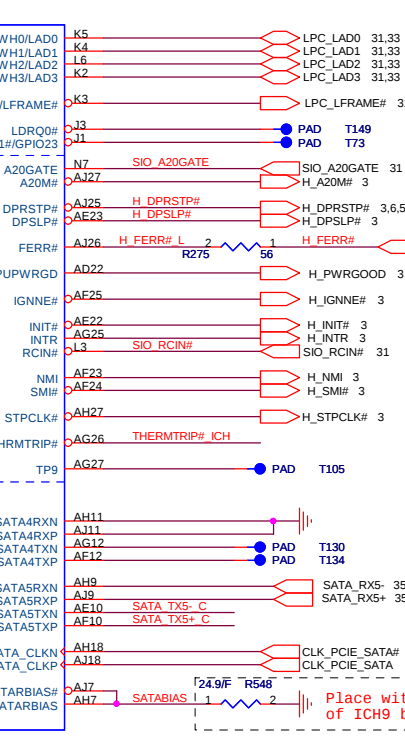
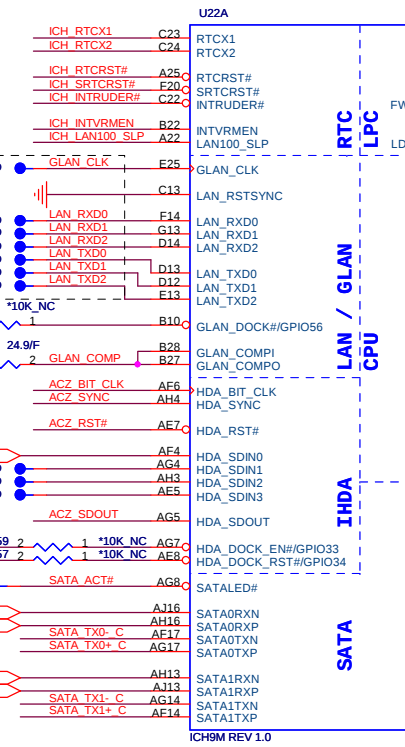
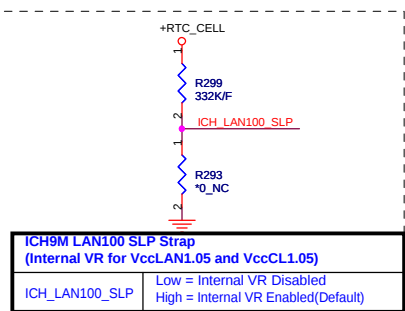
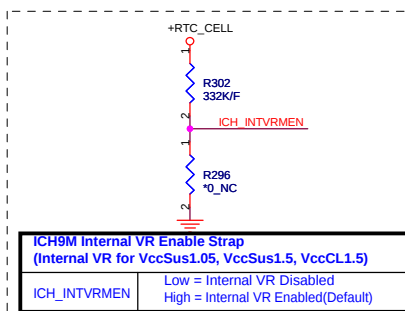
Title Cantiga (HOST)		
Size FMS	Document Number	Rev 2A
Date: Friday, November 21, 2008	Sheet 10	of 58



Place all series terms close to ICH9 except for SDIN input lines, which should be close to source. Placement of R558, R565, R552 & R562 should equal distance to the T split trace. Basically, keep the same distance from T for all series termination resistors.



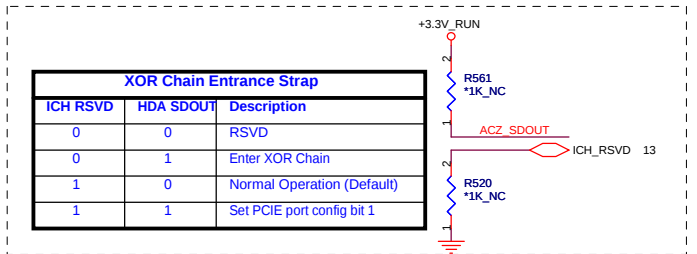
Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.

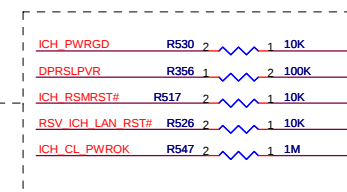
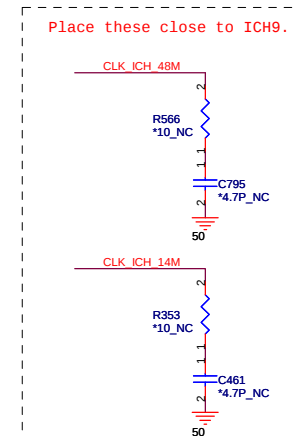
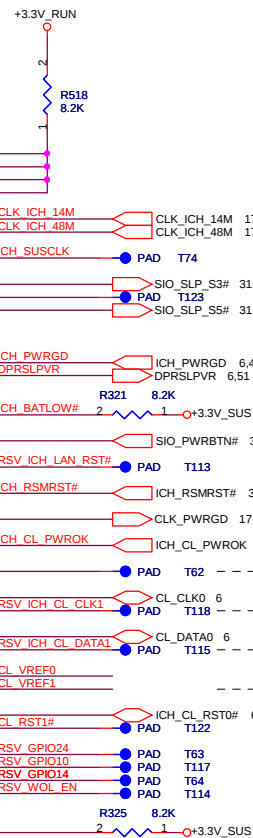
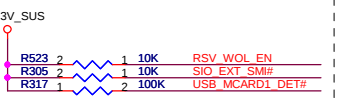
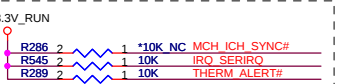
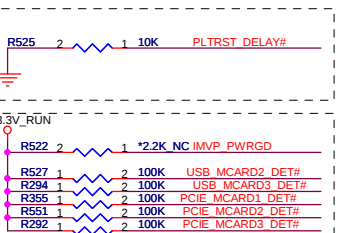
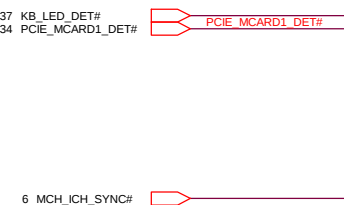
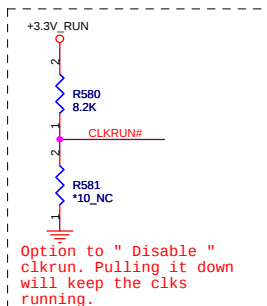
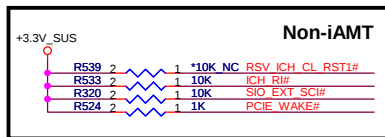
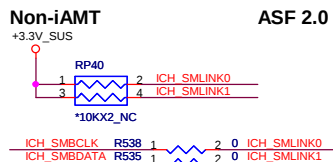
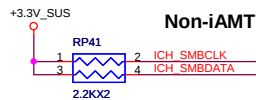


Master HDD

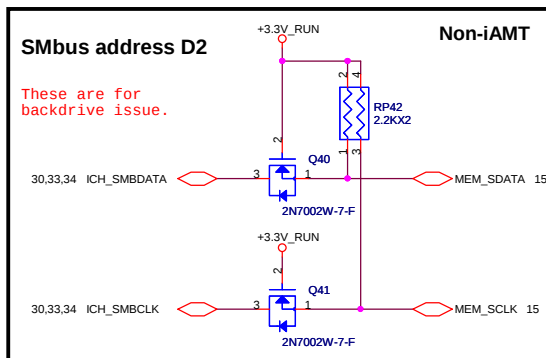
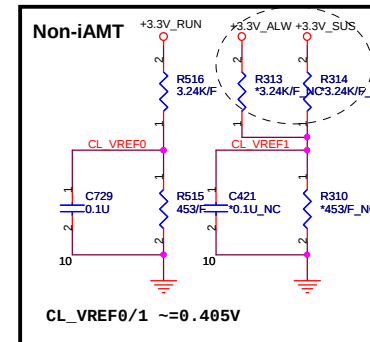
SATA ODD

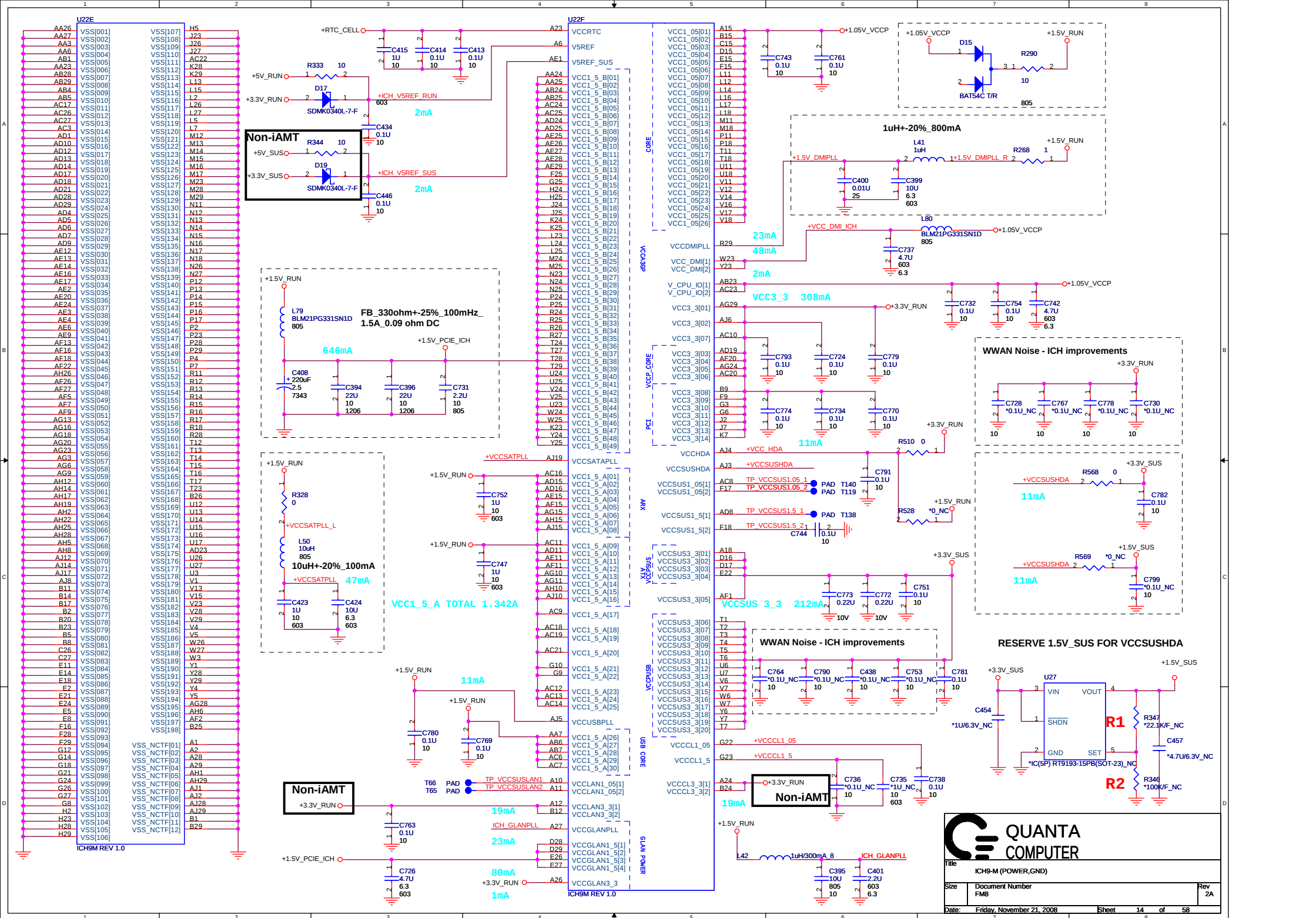
E-SATA

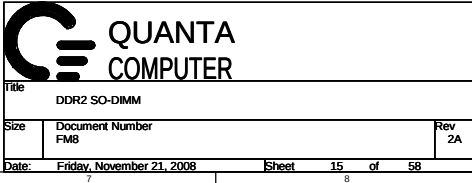


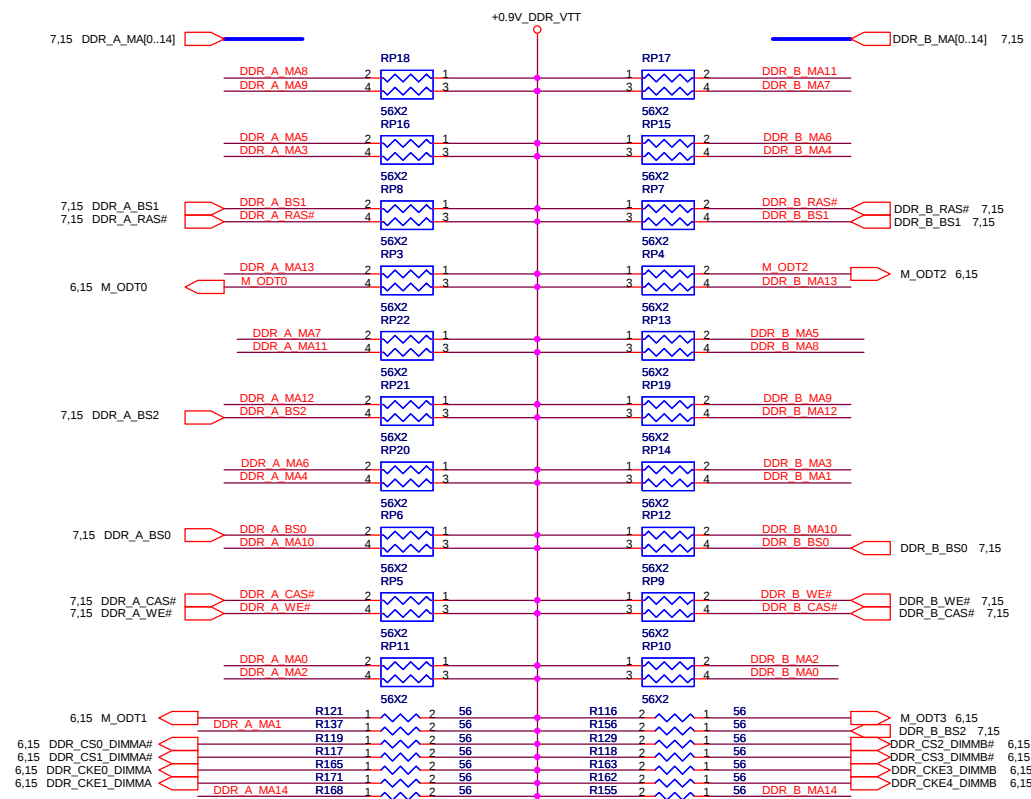
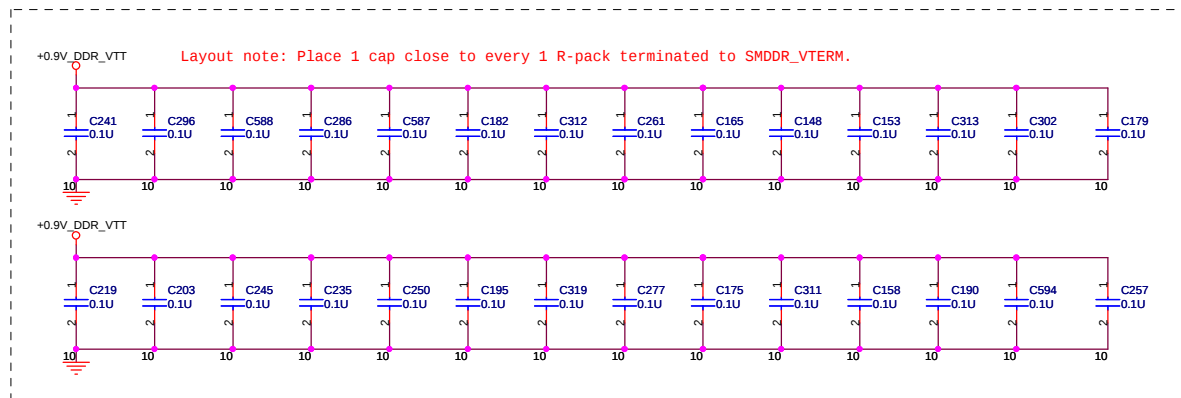


**DIS:ALW
UMA:SUS**





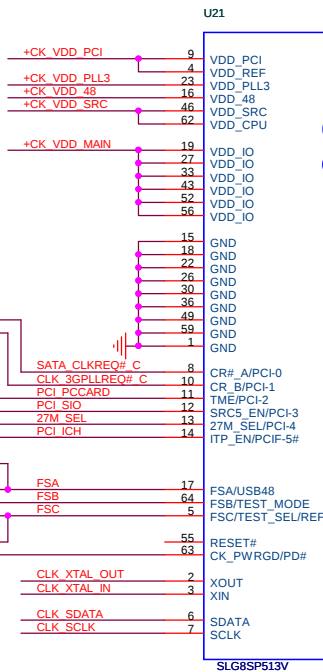
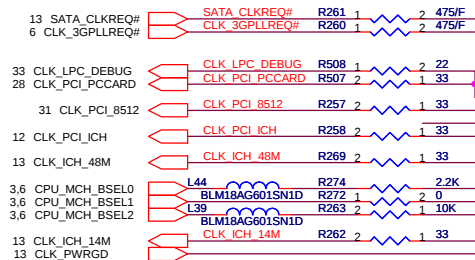
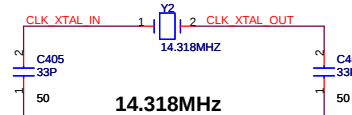
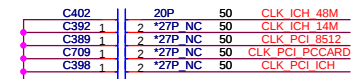




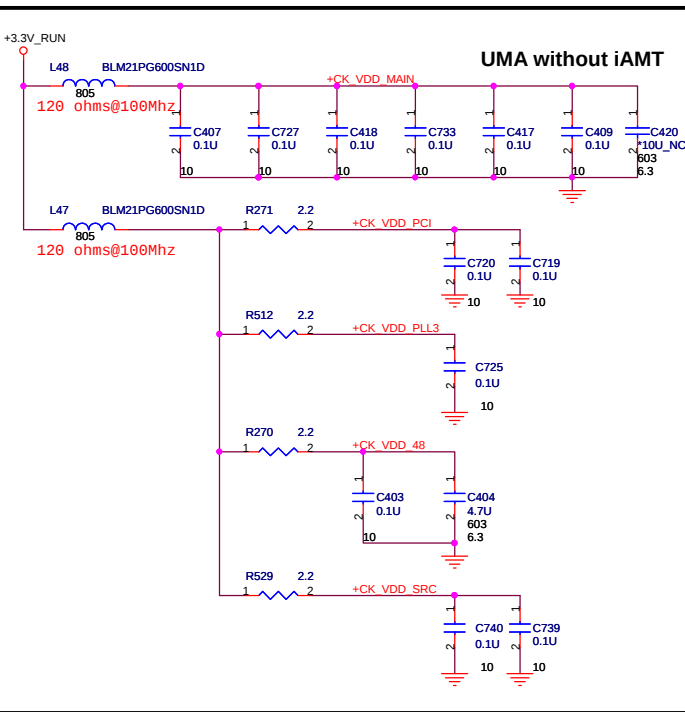
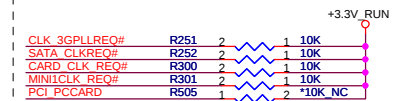
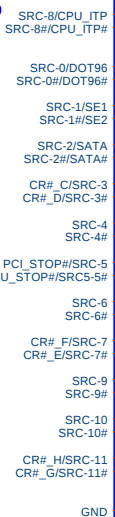
Layout notice:
Please these resistor
closely DIMMA,all
trace length<750 mil.

Layout notice:
Please these resistor
closely DIMMB,all
trace length<750 mil.

Add capacitor pads for improving WWAN.

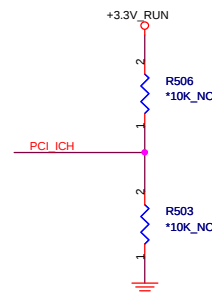
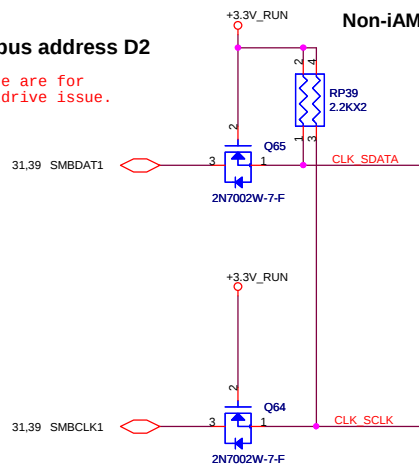


CK505
QFN64



SMBus address D2

These are for
backDrive issue.



R506 POP: For Internal pull-low.
R503 POP: For internal pull-high.

27M_SEL

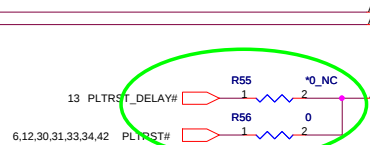
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

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6 PCIE_MTX_GRX_P0..15]
6 PCIE_MTX_GRX_N0..15]

6 PCIE_MRX_GTX_P0..15]
6 PCIE_MRX_GTX_N0..15]

100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing.
Clock must be provided less than 400ns
after CLKREQ# is asserted



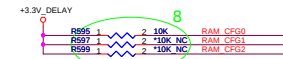
43

M92-S2 XT AJ072800T04 100-C61675(216-0728004)
M92-S2 AJ072800T03 100-C61643(216-0728003)

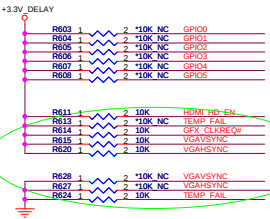
QUANTA COMPUTER logo and title block. Title: VGA-M92-XT (PCIe). Size: Document Number FM8. Date: Friday, November 21, 2008. Sheet 18 of 58. Rev 2A.

MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GP109	CFG2 GP1013	CFG1 GP1012	CFG0 GP1011
128MB		0	0	0
256MB		0	0	1
64MB		0	1	0
512MB		1	0	0

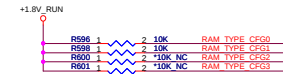
8



GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	FMS setting
GPIO0	GPIO0 - TX_PRRS_EN (Transmitter Power Savings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO1 - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO2 - BIF_GEN2_EN (5.0 GT/s Enable) 0: Default (Driver Controlled Gen2) 1: Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO_5_AC_BATT 0: Battery saving mode = 0.9V 1: AC (Performance mode) = 3.3V	0
GPIO6	ATI Internal use only	0



19 48



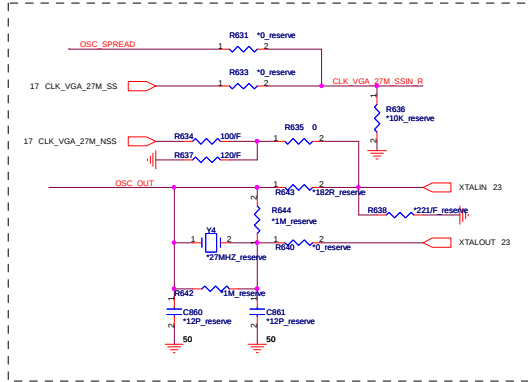
38

Memory Straps	RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Quanta PN (WinBuy)	Vendor PN	31 level PN
800MHz 512MB(32M*32) Samsung	0	0	1	0	AKD5LWGT501	AKD5LWGT504	K4J103240Q-HC12	31FM8MB0030
900MHz 512MB(32M*32) Qimonda	0	0	1	1	AKD5LWFT^03	AKD5LWFT^00	HYB18H16321AF-11	31FM8MB0000
800MHz 256MB(16M*32) Samsung	0	0	0	1	AKD5FWGT500	AKD5FWGT503	K4J523240H-HC12	31FM8MB0040
900MHz 256MB(16M*32) Hynix	0	0	0	0	AKD5FWHTW03	AKD5FWHTW06	H5RS5223CFR-11C	31FM8MB0020

36 48

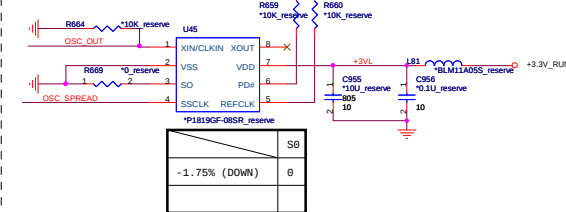
31

51

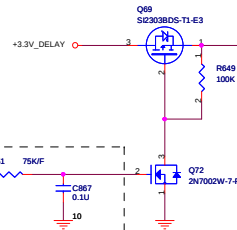


Spread Spectrum

If U4, the discrete spread spectrum chip is not used, then pop R48 in order to pull-down BXTALOUT for EMI reasons.

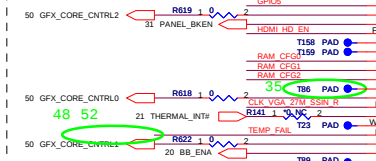


S0	
-1.75% (DOWN)	0

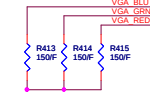
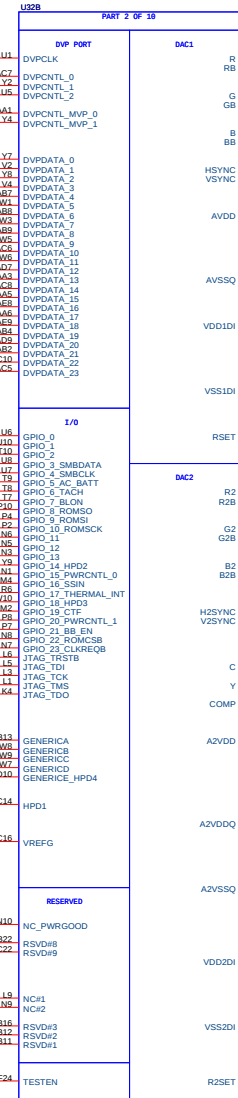
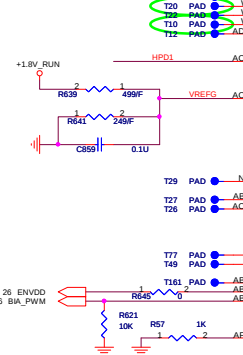


As M82 design, for GPIO use

RAM TYPE CFG0
RAM TYPE CFG1
RAM TYPE CFG2
RAM TYPE CFG3



35



DIS only
Layout Note:
Place 150 ohm
termination resistors
close to ATI CHIP.

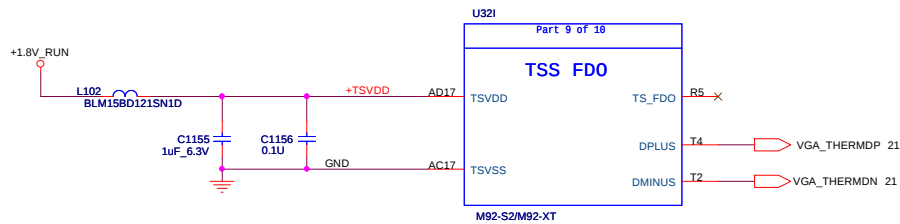
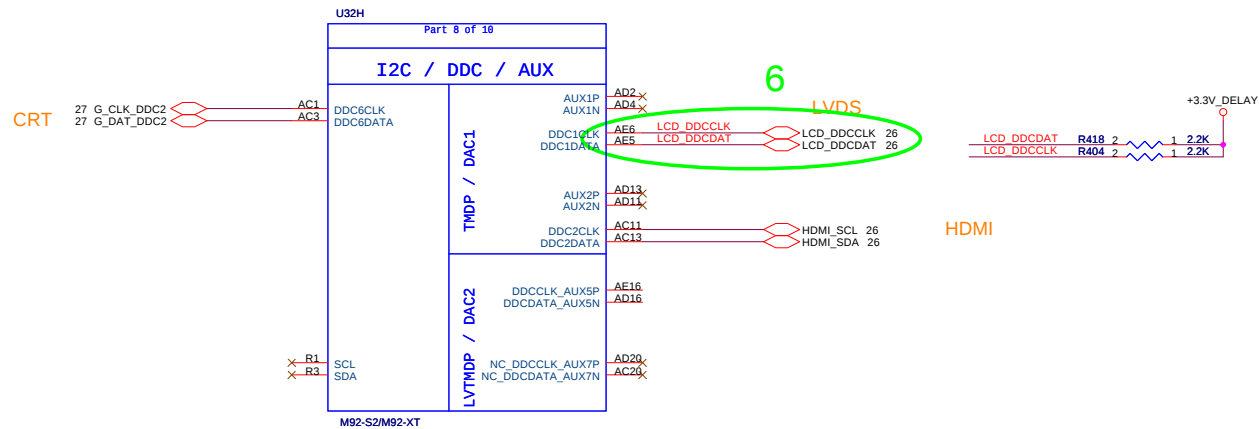
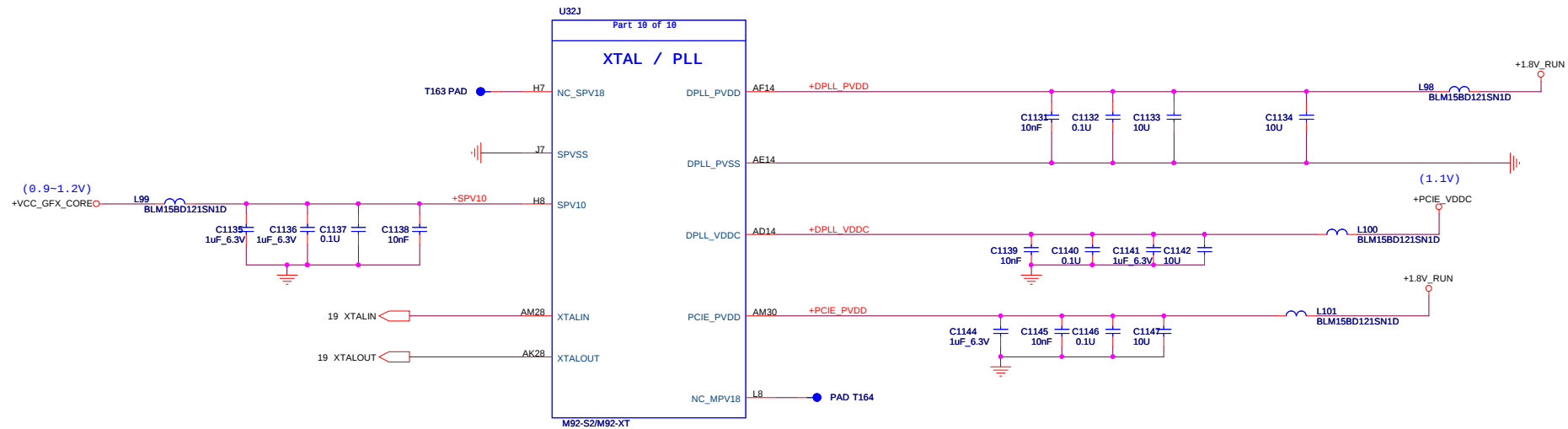


Part	VGA-M82-XT (PCIe)	Rev	2A
Size	Document Number		
Date	Friday, November 21, 2008	Sheet	19 of 58

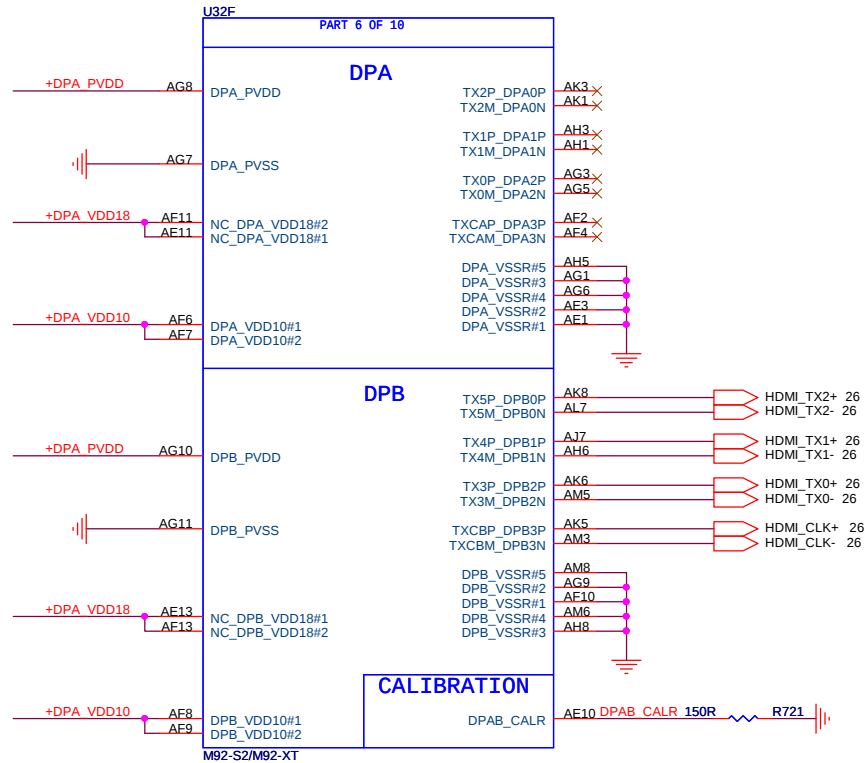
U32C

[illegible]

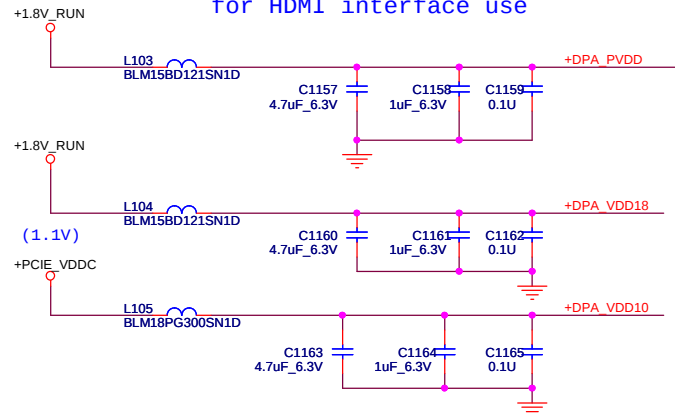
DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



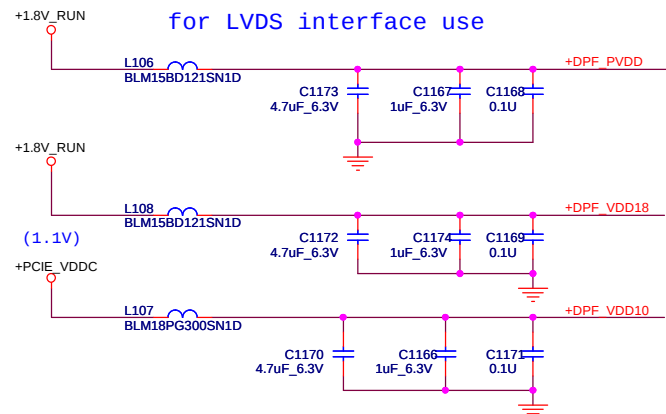
TMDP(HDMI) INTERFACE



for HDMI interface use



for LVDS interface use



Title		
VGA-M92-XT (PCIe)		
Size	Document Number	Rev
	FM8	2A
Date:	Friday, November 21, 2008	Sheet 24 of 58



Title	
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VGA-M82-S (PCIe)

Size

Document Number FM8

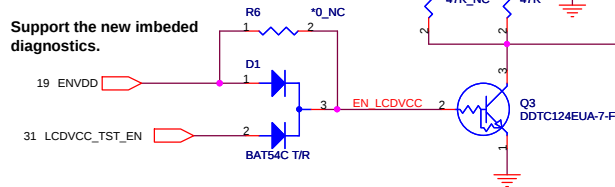
Rev	
-----	--

REV
2A

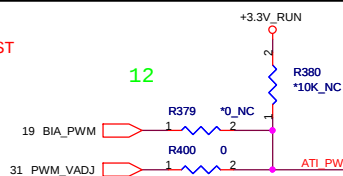
Date: Friday, November 21, 2008

Sheet 25 of 58

Support the new imbedded diagnostics.

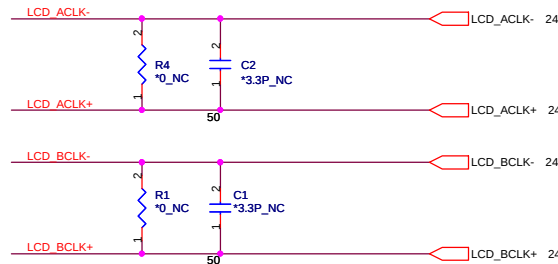


Populate R379 for DPST implementation only.

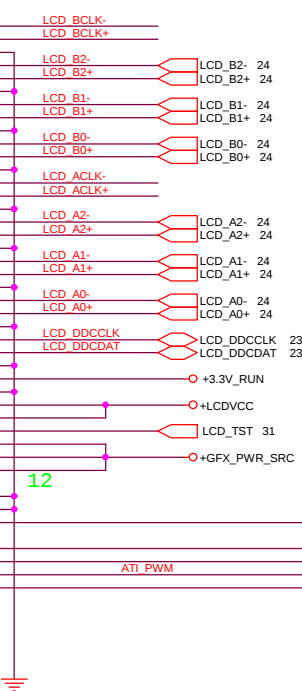
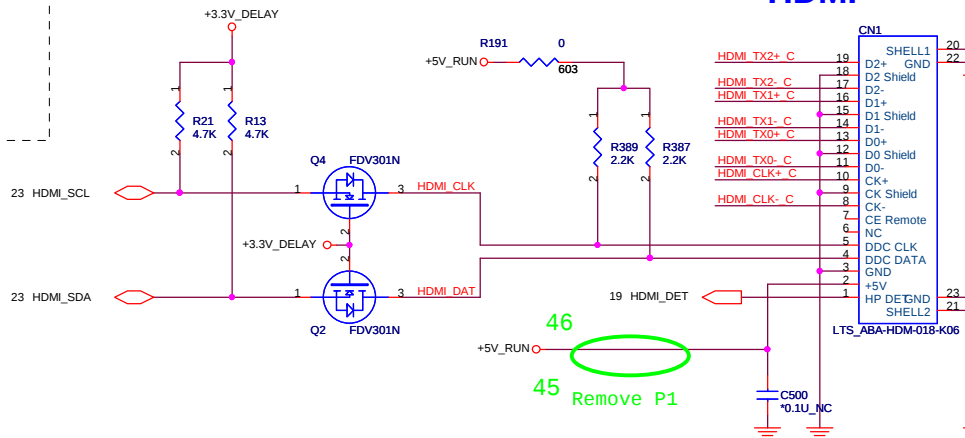


Shunt capacitors on LVDS for improving WWAN.

LCD_B0-	C16	1	2	*3.3P NC	50	LCD_B0+
LCD_B1-	C10	1	2	*3.3P NC	50	LCD_B1+
LCD_B2-	C15	1	2	*3.3P NC	50	LCD_B2+
LCD_A0-	C13	1	2	*3.3P NC	50	LCD_A0+
LCD_A1-	C12	1	2	*3.3P NC	50	LCD_A1+
LCD_A2-	C3	1	2	*3.3P NC	50	LCD_A2+

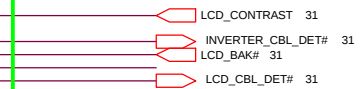


24	HDMI_TX2+	C25	0.1U10V/X7R	HDMI_TX2+ R
24	HDMI_TX2-	C26	0.1U10V/X7R	HDMI_TX2- R
24	HDMI_TX1+	C23	0.1U10V/X7R	HDMI_TX1+ R
24	HDMI_TX1-	C22	0.1U10V/X7R	HDMI_TX1- R
24	HDMI_TX0+	C27	0.1U10V/X7R	HDMI_TX0+ R
24	HDMI_TX0-	C30	0.1U10V/X7R	HDMI_TX0- R
24	HDMI_CLK+	C21	0.1U10V/X7R	HDMI_CLK+ R
24	HDMI_CLK-	C20	0.1U10V/X7R	HDMI_CLK- R

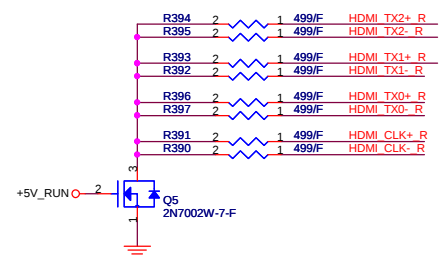
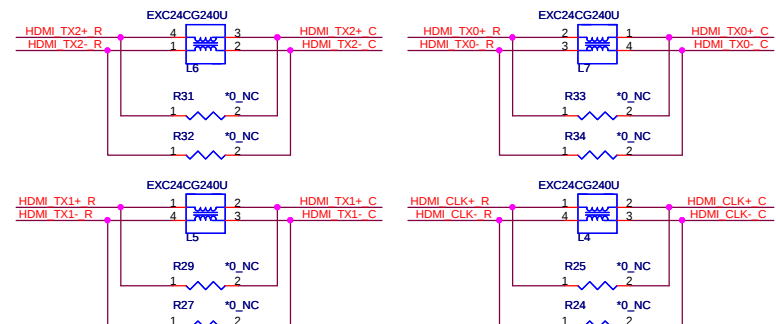


(3)08/22: delete SM Bus and add contrast function

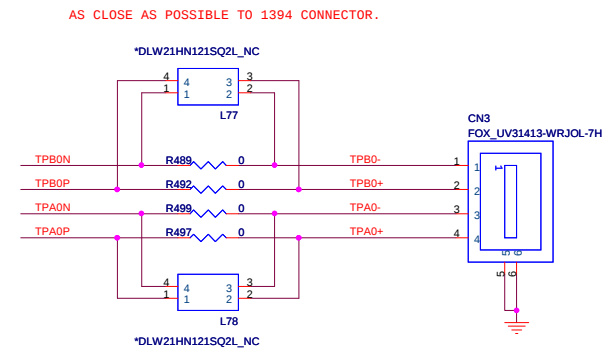
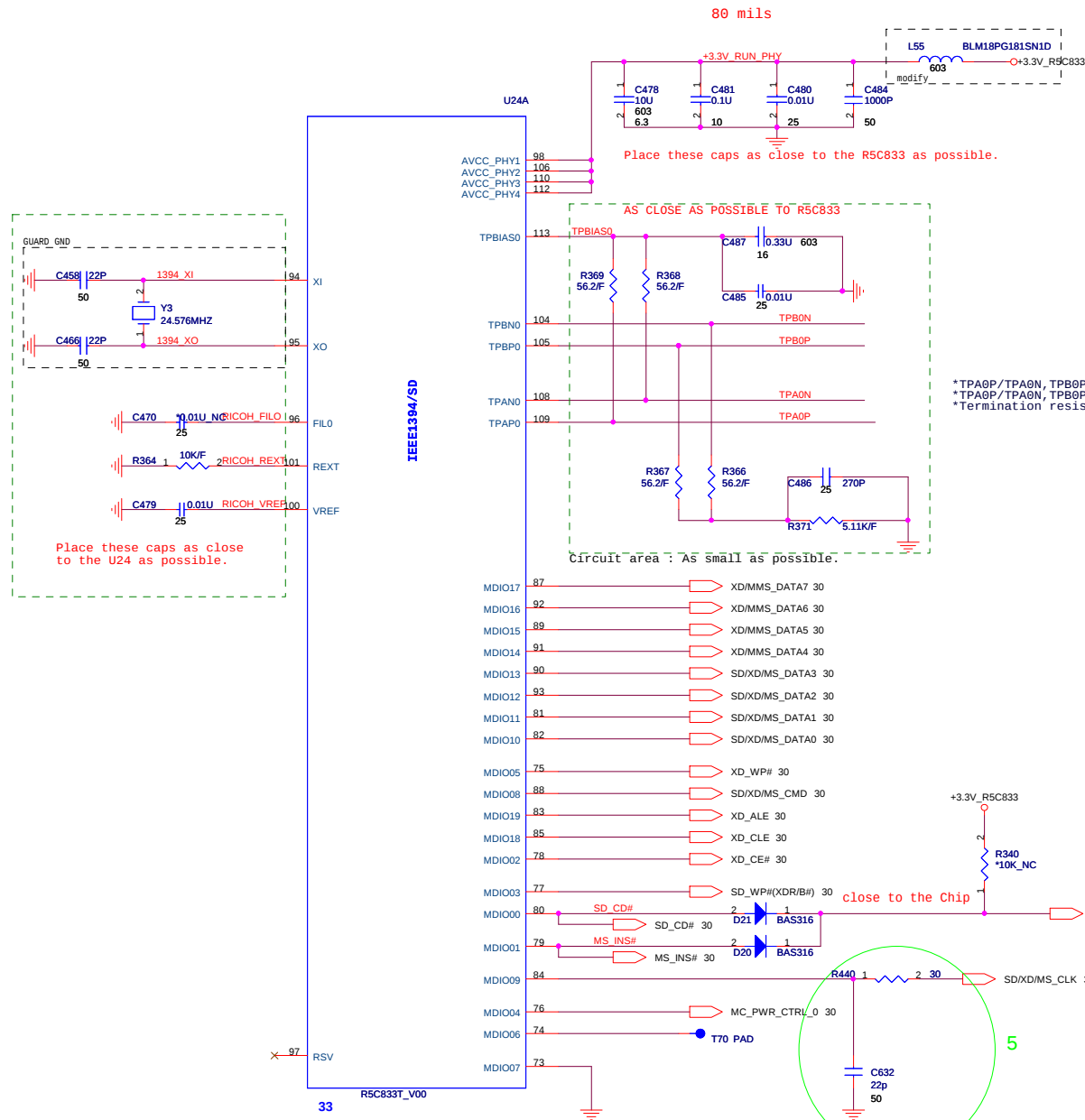
Address : A9H --Contrast
AAH --Backlight



HDMI

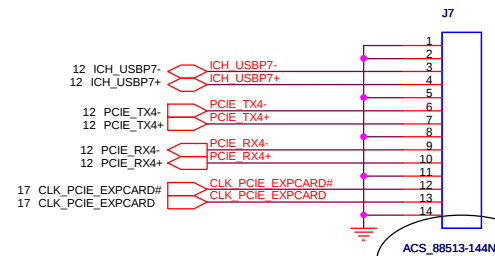
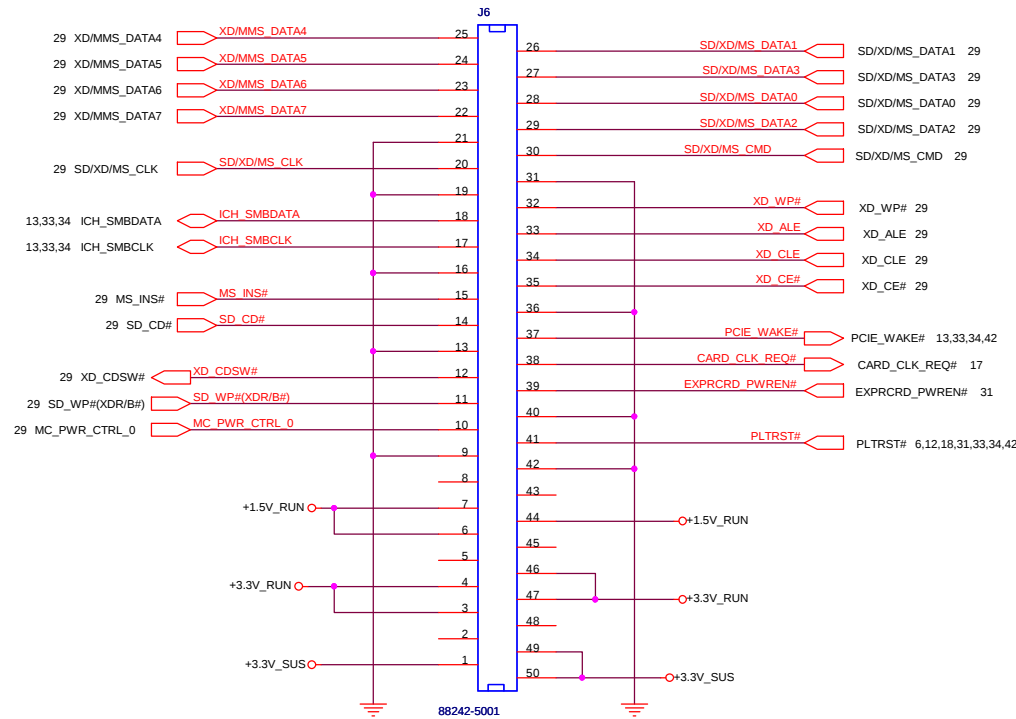


Title LCD CONN & CK-SSCD		
Size	Document Number FM8	Rev 2A
Date: Friday, November 21, 2008	Sheet 26	of 58



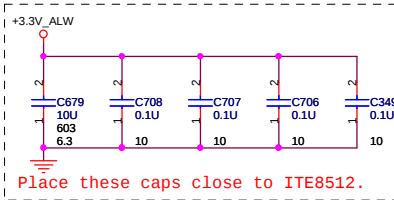
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

Express Card/CARD READER



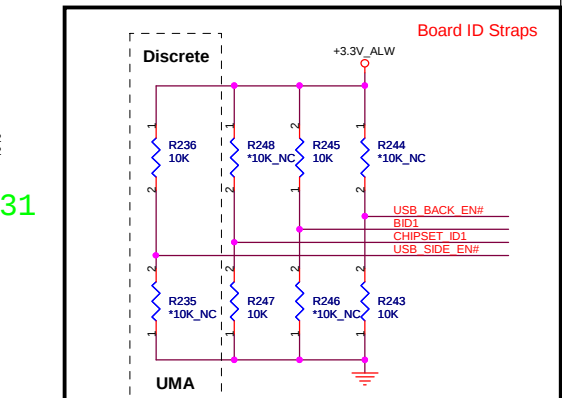
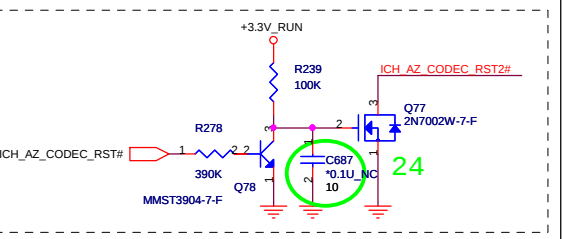
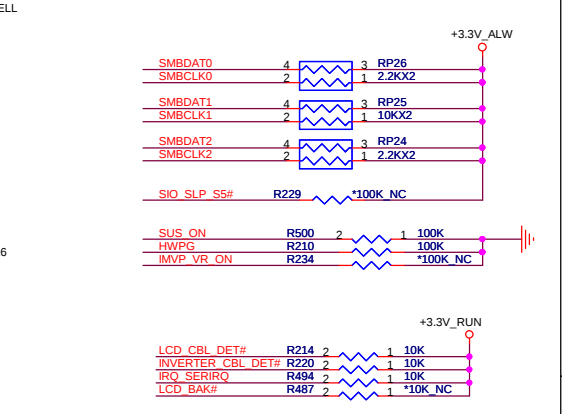
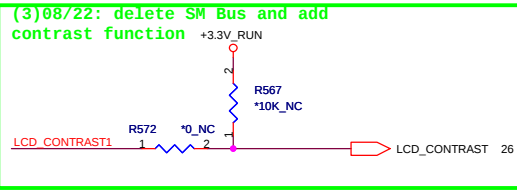
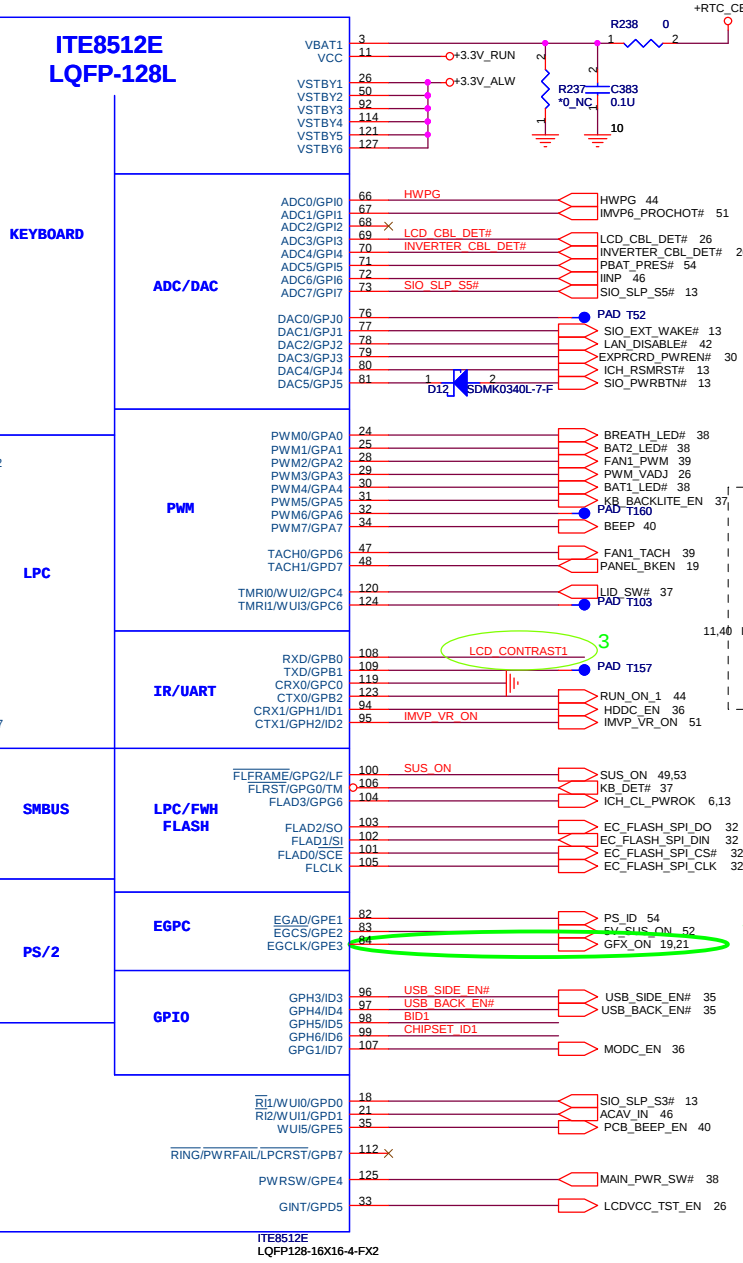
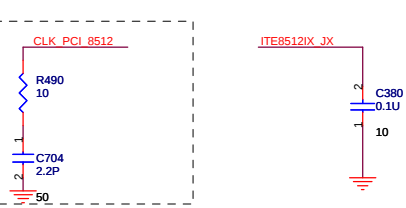
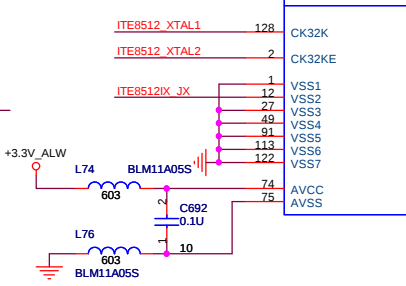
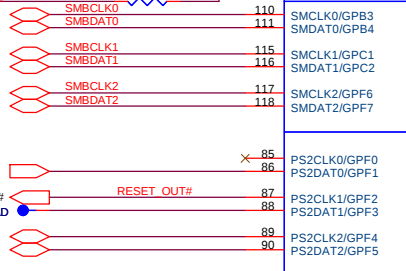
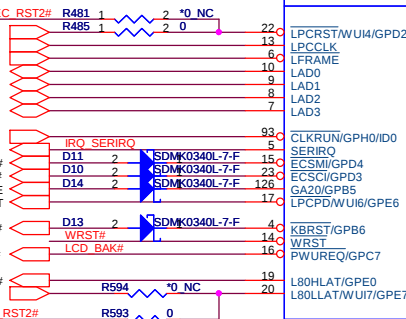
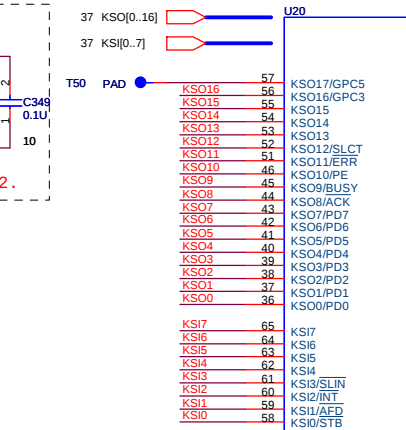
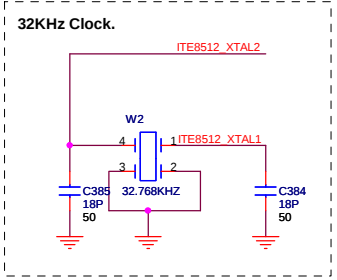
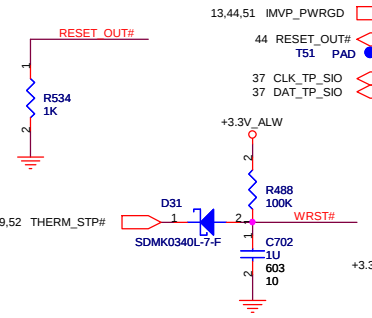
8/28:change PN to 88513-144N

QUANTA COMPUTER		
Title: ExpressCard/SmartCard		
Size: FMS	Document Number: FMS	Rev: 2A
Date: Friday, November 21, 2008	Sheet: 30	of 58



Place these caps close to ITE8512.

Charge and BAT
CLK, LCD and Thermal
G_Thermal
and Media button



VGA_IDENTIFY

BID0

CHIPSET ID1	BID1	USB BACK_EN#	FM6B(UMA)	FM6(Ds)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	QT (A00)	QT (A00)
0	0	0	(A01)	(A01)
0	0	1		

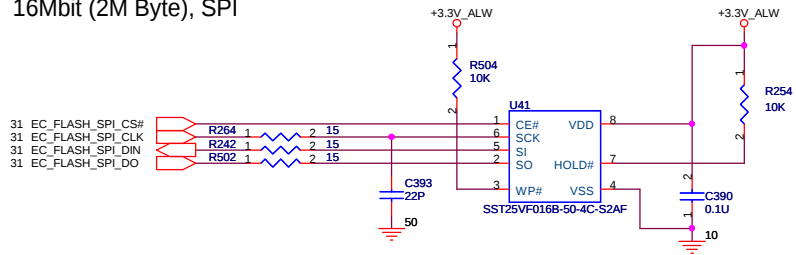
QUANTA COMPUTER

Ultra I/O Controller ECE5028

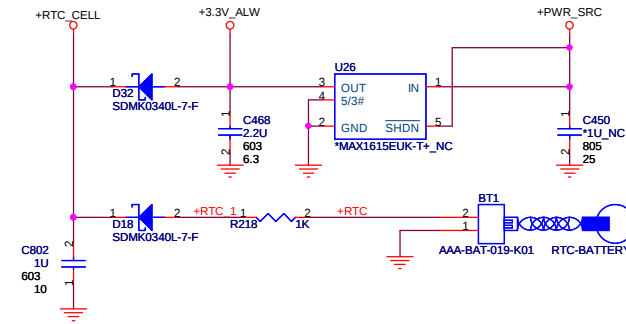
Size: Document Number: FMB Rev: 2A

Date: Friday, November 21, 2008 Sheet: 31 of 58

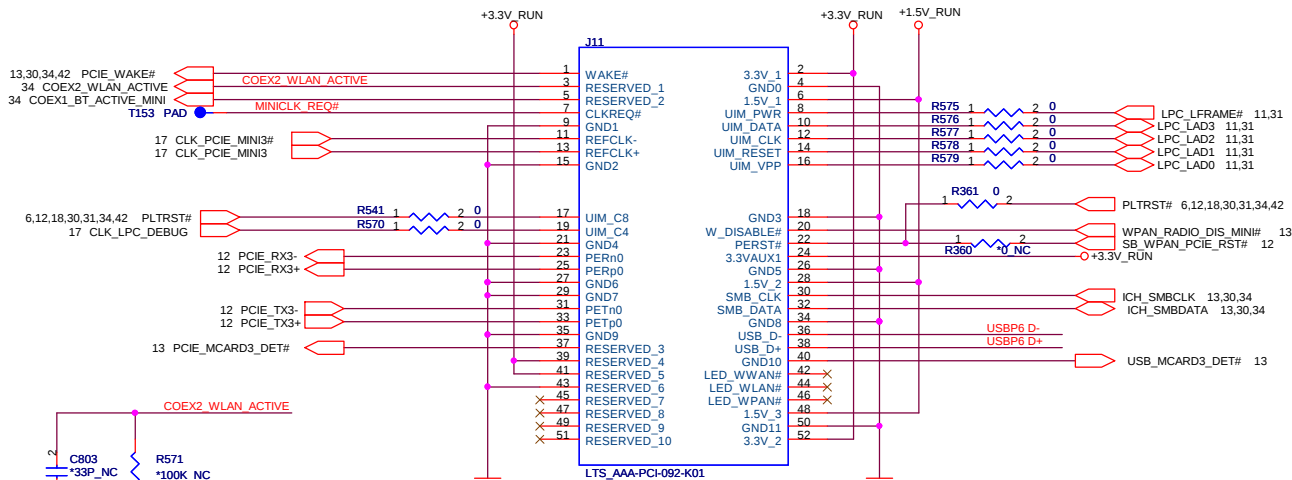
16Mbit (2M Byte), SPI



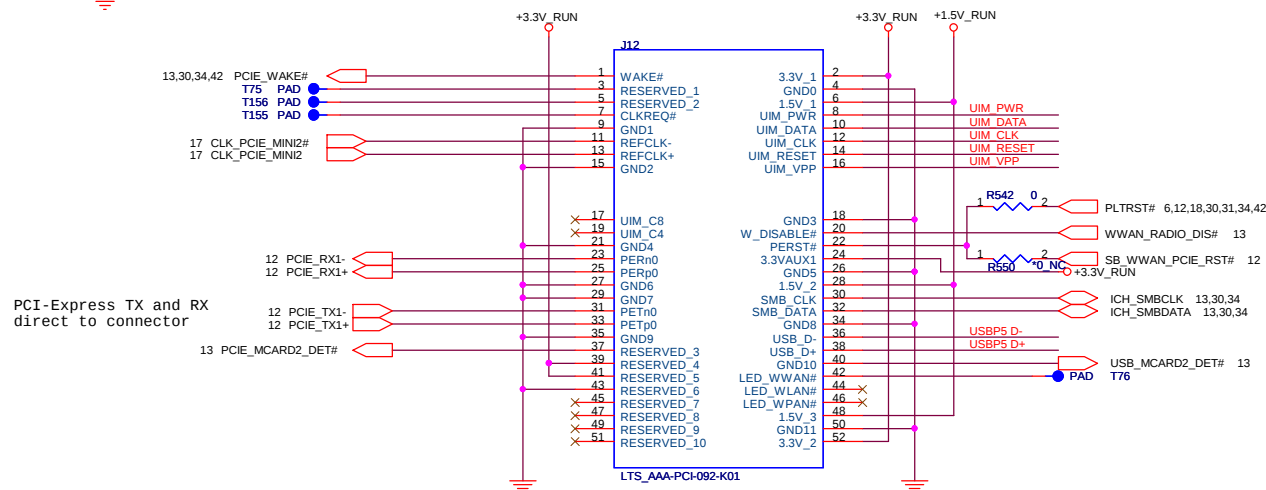
RTC BATTERY



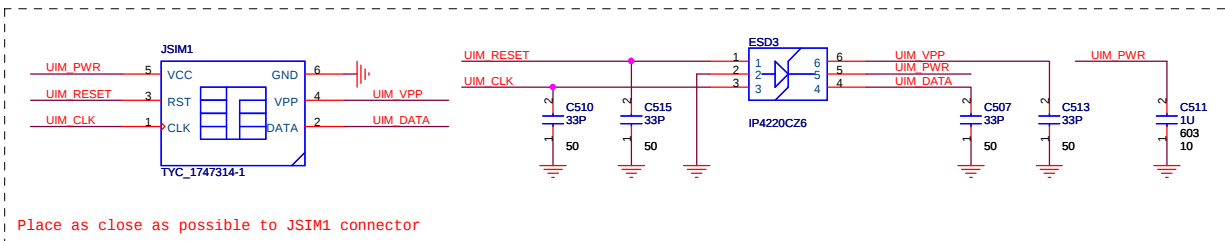
MiniCard Robson, BT. UWB connector



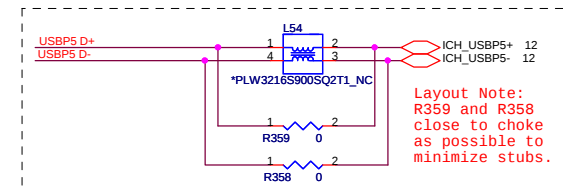
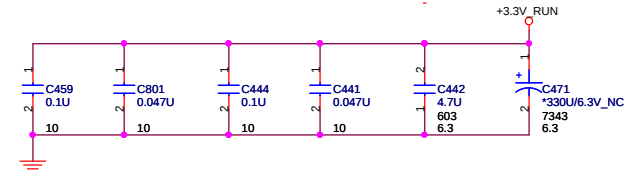
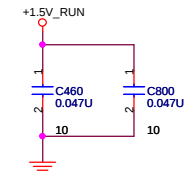
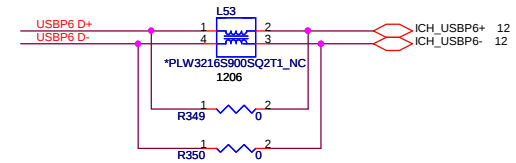
MiniCard WWAN connector



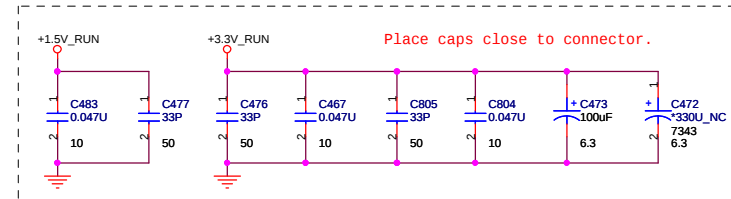
PCI-Express TX and RX direct to connector



Place as close as possible to JSIM1 connector



Layout Note:
R359 and R358
close to choke
as possible to
minimize stubs.

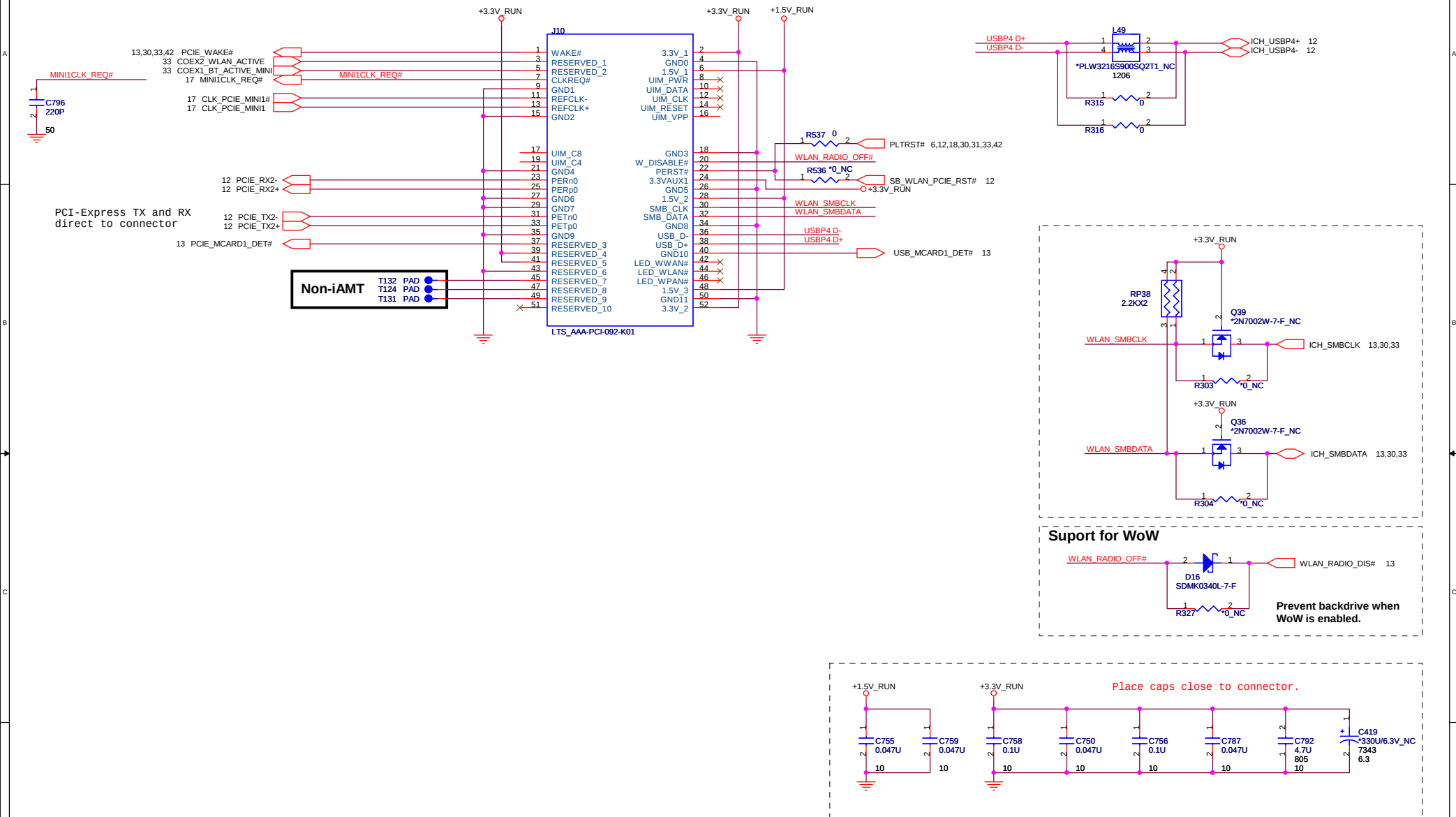


Place caps close to connector.



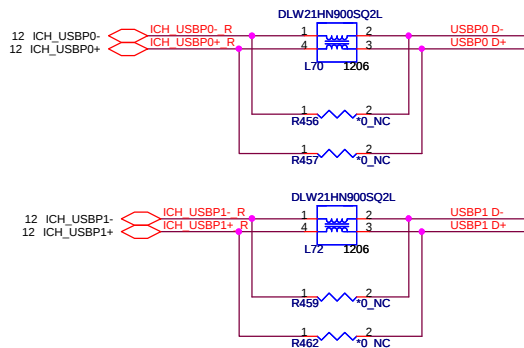
Title			MINI-PCI
Size	Document Number	Rev	
FMB		2A	
Date:	Friday, November 21, 2008	Sheet	33 of 58

MiniCard WLAN connector



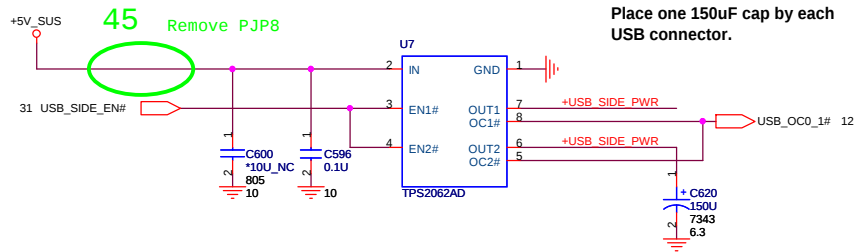
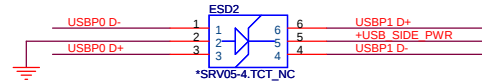
Title			MDC CONN.
Size	Document Number	Rev	
FMS		2A	
Date:	Friday, November 21, 2008	Sheet	34 of 58

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

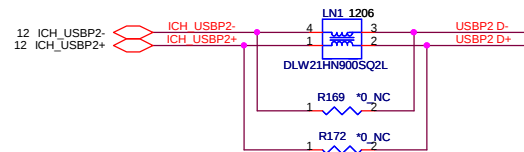


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

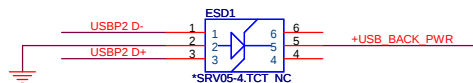
Place ESD diodes as close as USB connector.



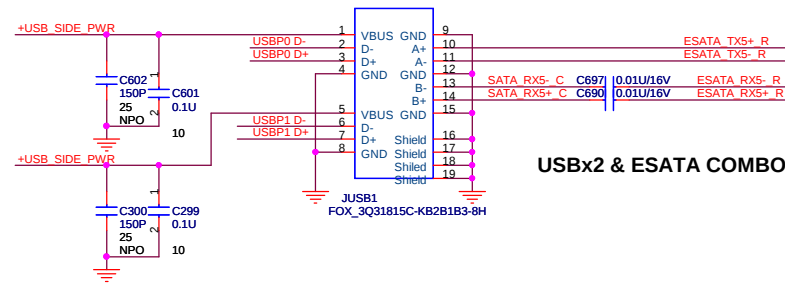
Place one 150uF cap by each USB connector.



Place ESD diodes as close as USB connector.

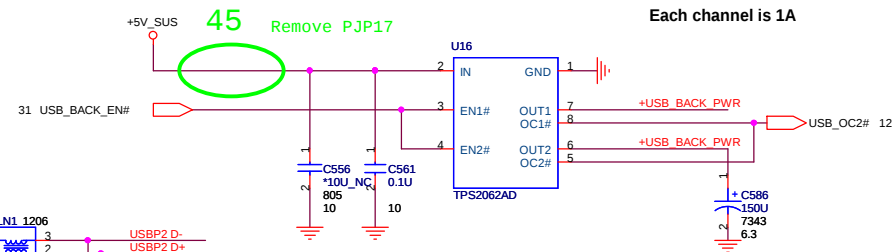
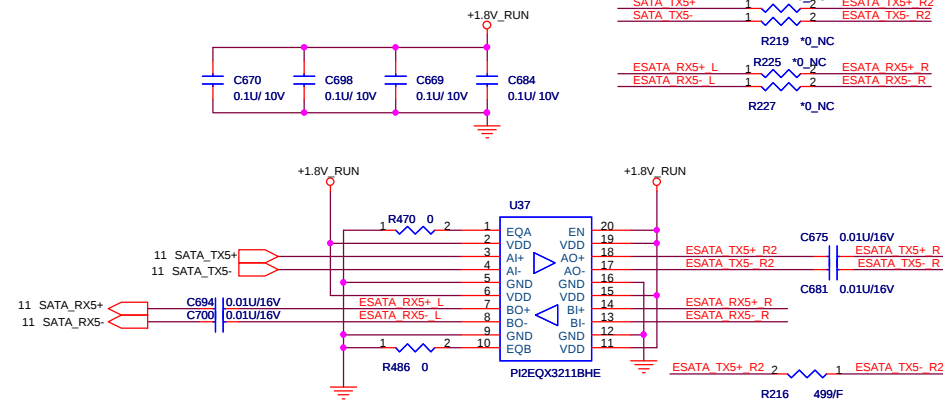


Side External USBX2

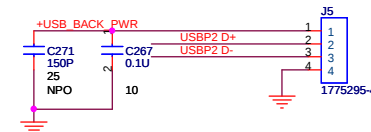


USBx2 & ESATA COMBO

E-SATA Re-driver

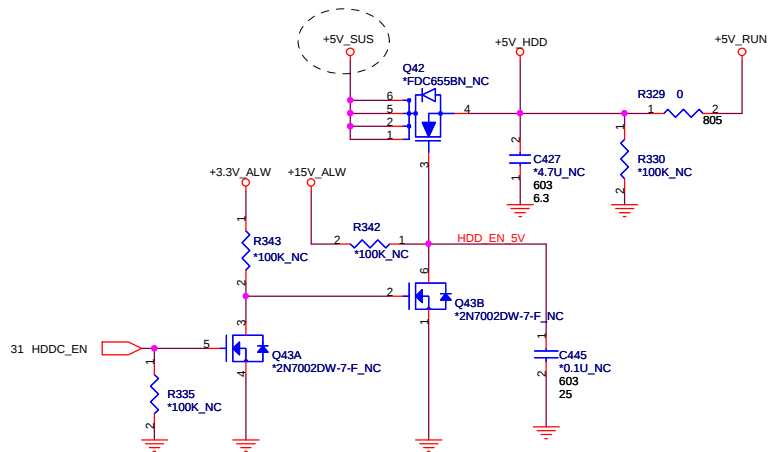
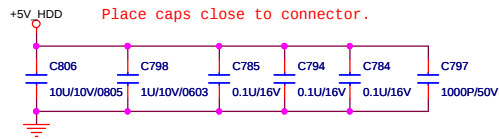
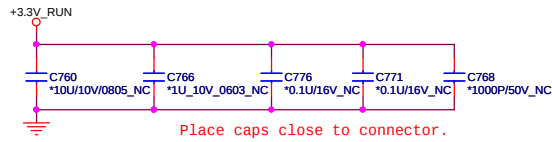
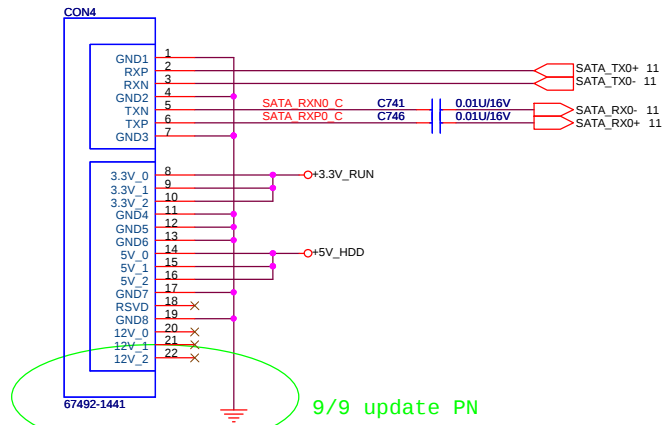


Each channel is 1A

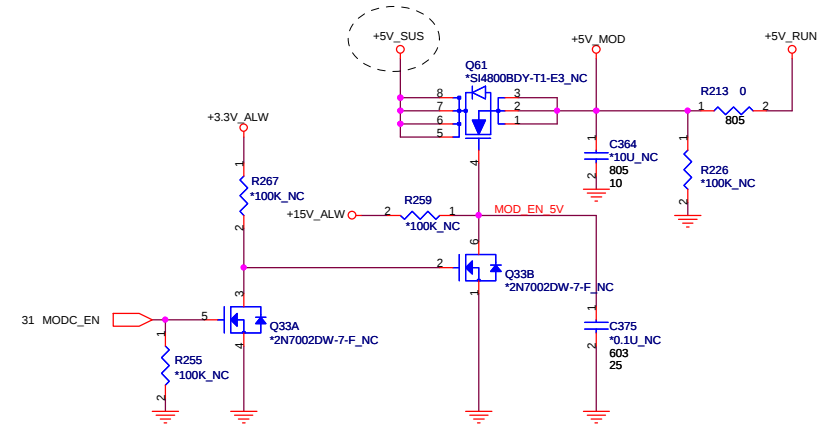
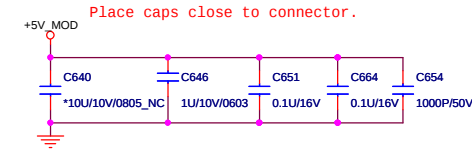
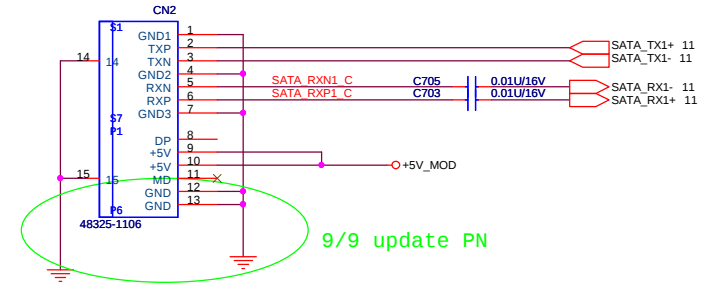


Title			SERIAL PORT & USB
Size	Document Number	Rev	
	FMB	2A	
Date:	Friday, November 21, 2008	Sheet	35 of 58

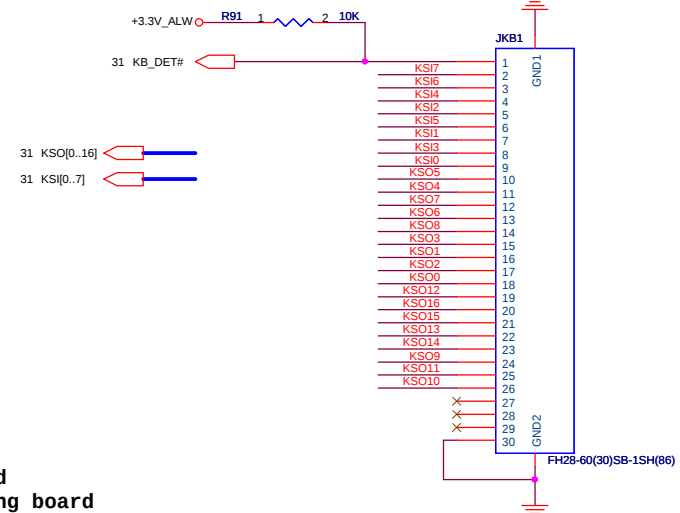
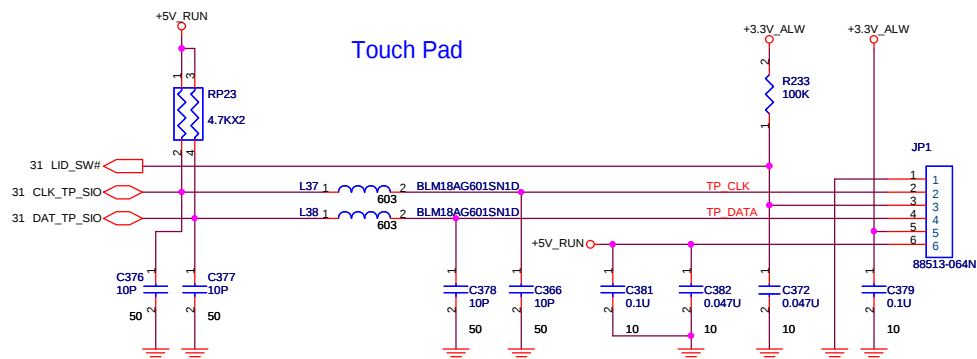
SATA Connector.



ODD Connector

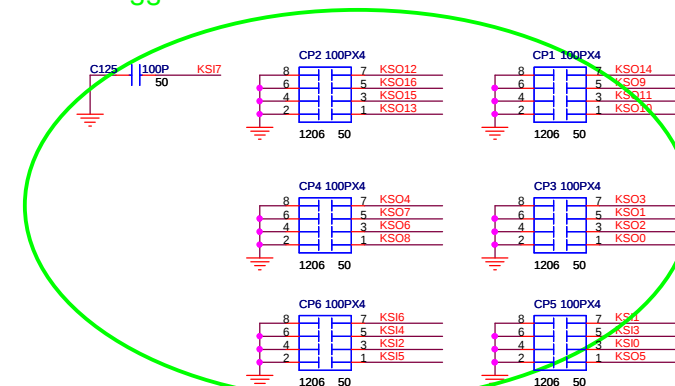


Title			SATA (HDD&CD_ROM)
Size	Document Number	Rev	
	FMB	2A	
Date:	Friday, November 21, 2008	Sheet	36 of 58



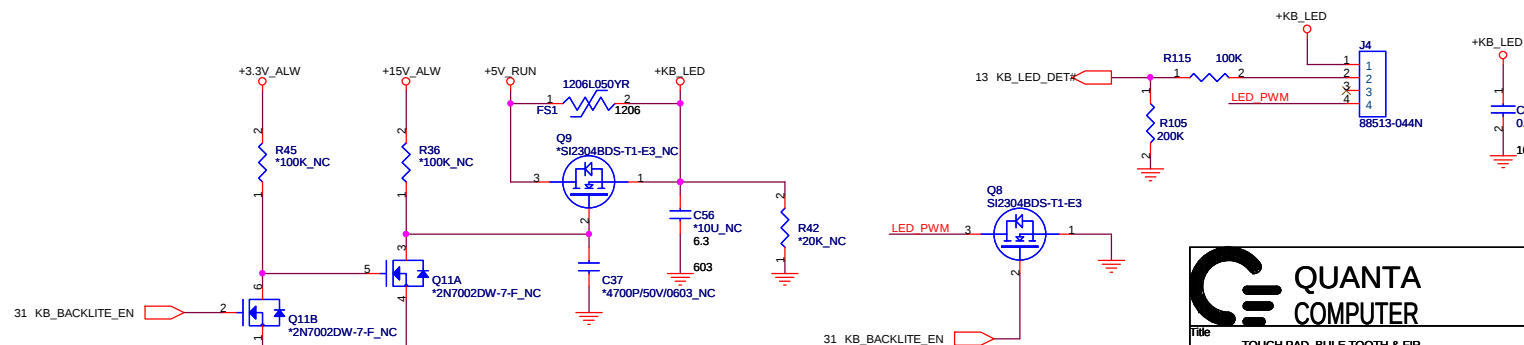
08-05 add
For running board

33

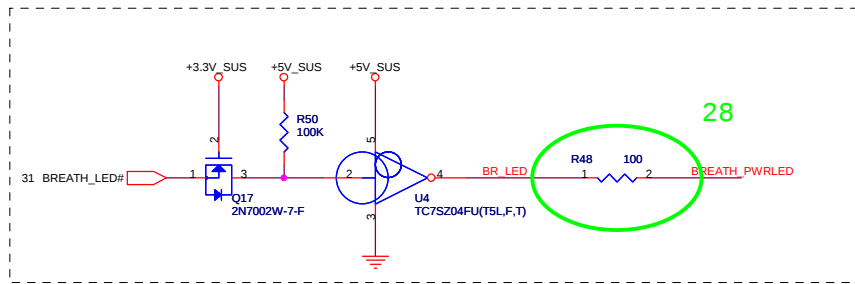
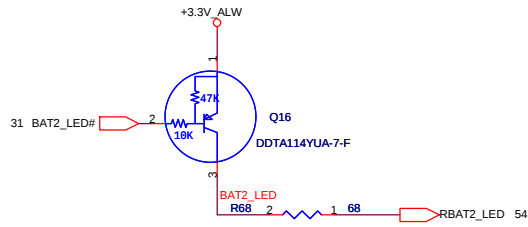
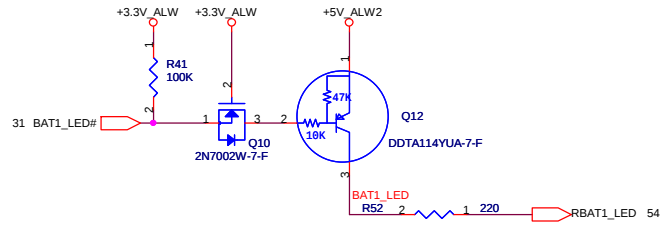


100P CAPS CLOSE TO JKB1

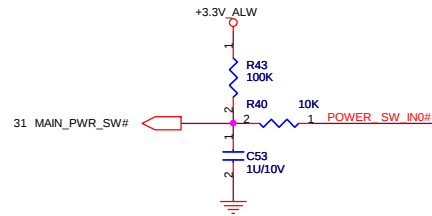
Key board Illumination



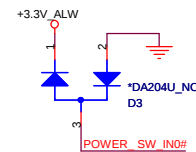
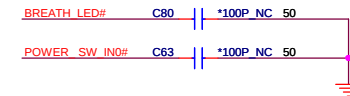
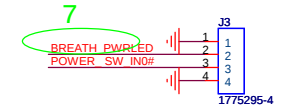
Battery status.

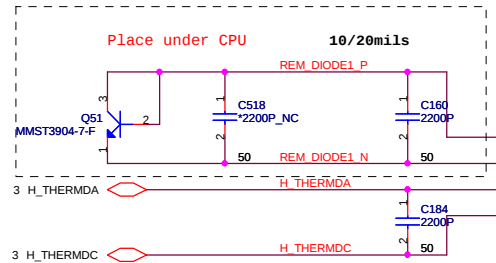
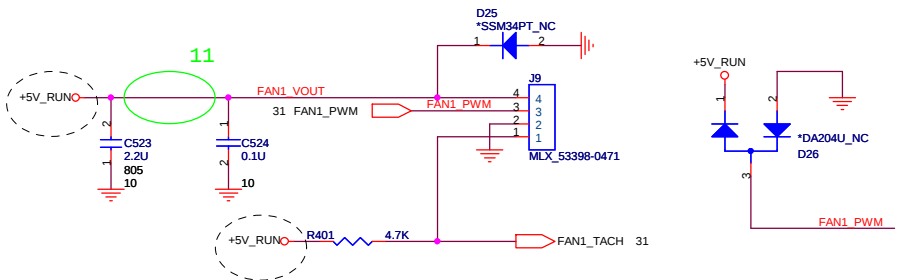


Power Switch

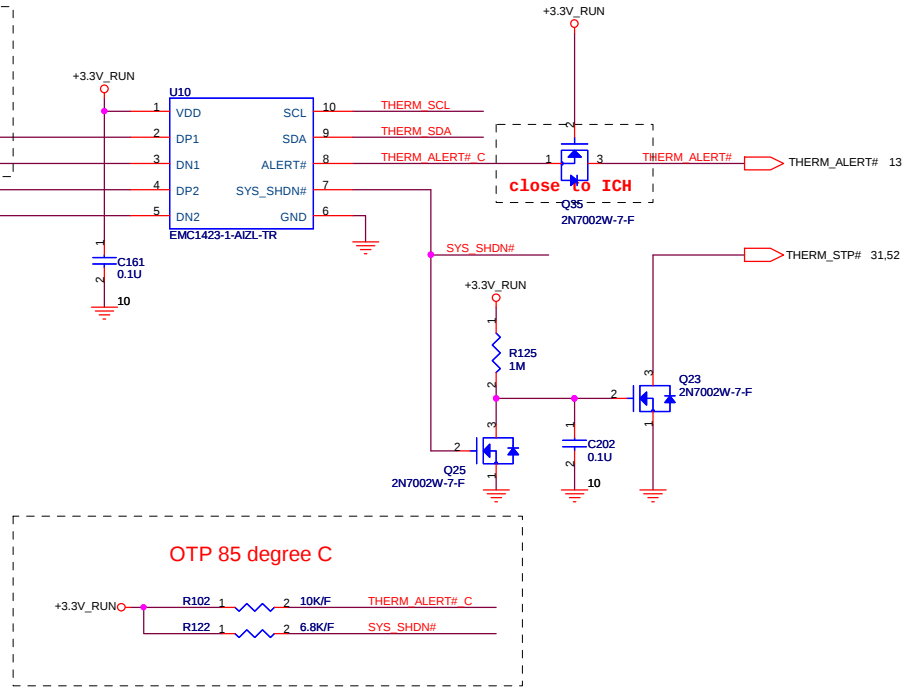
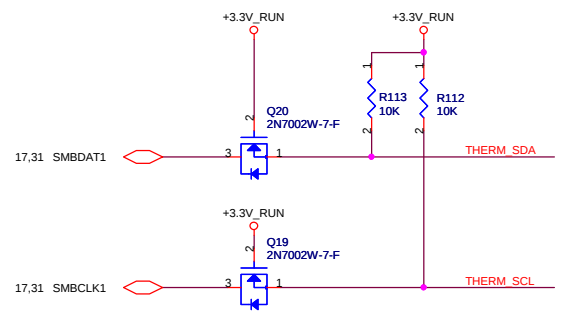


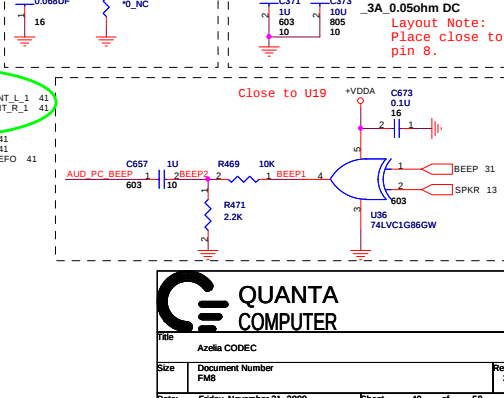
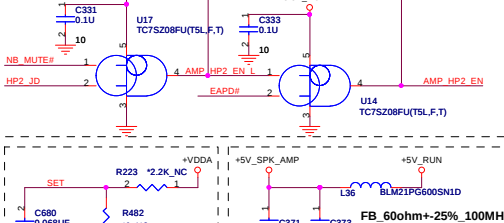
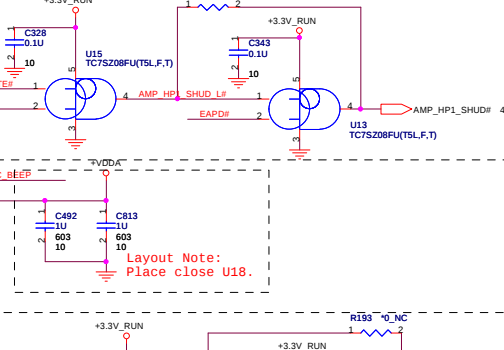
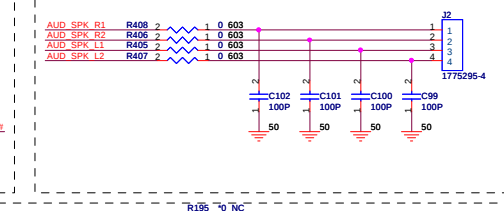
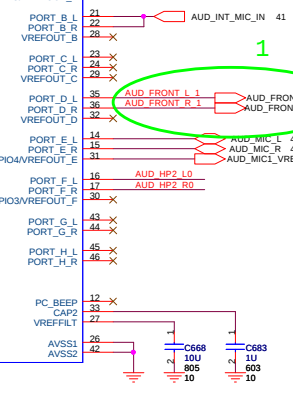
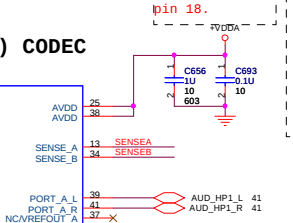
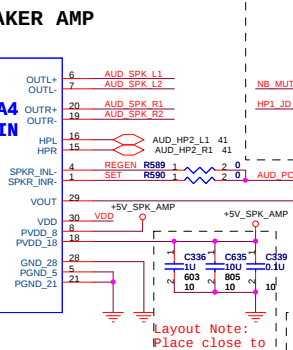
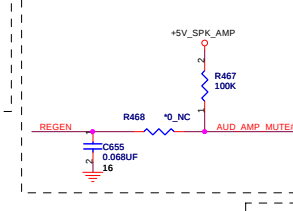
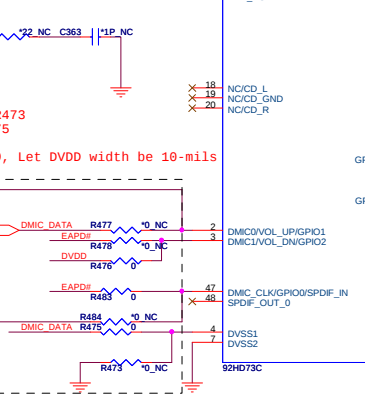
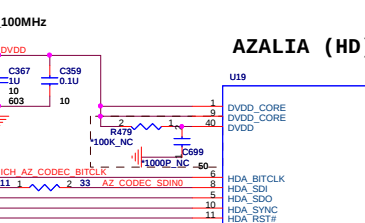
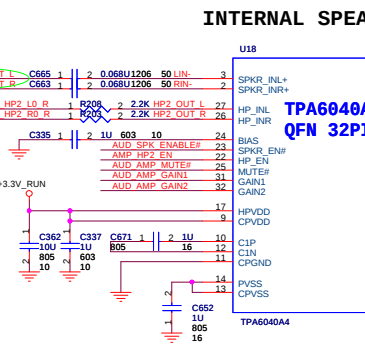
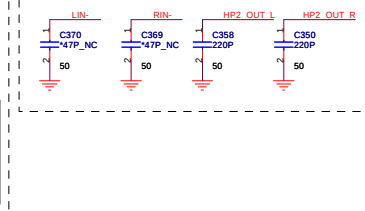
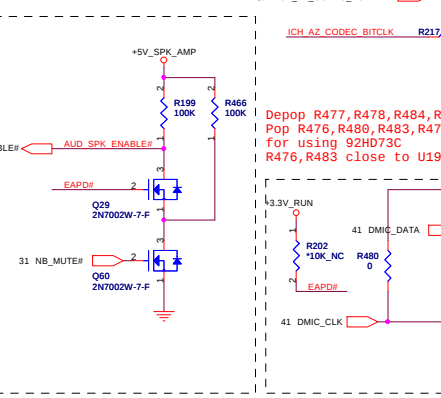
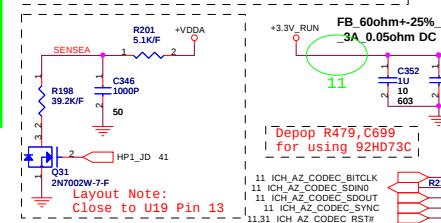
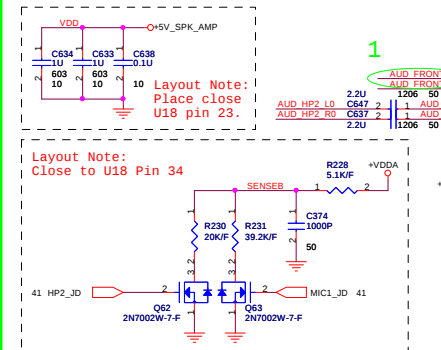
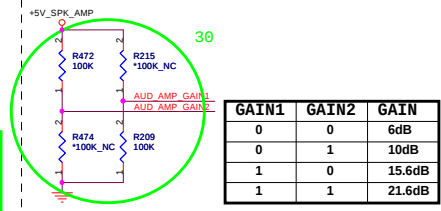
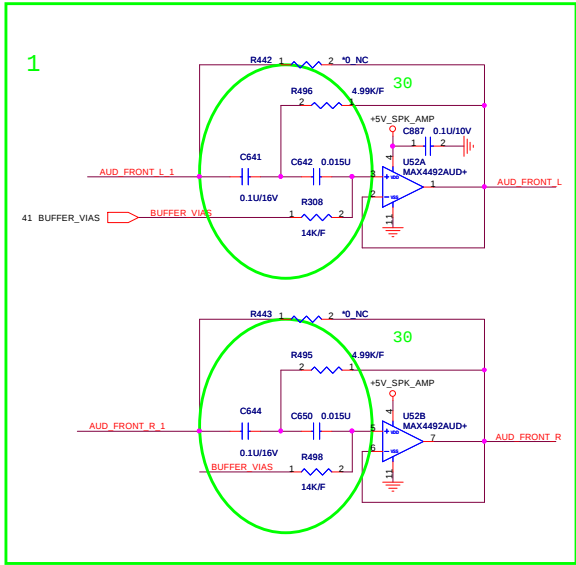
Power button cable



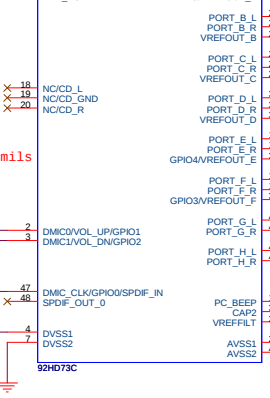
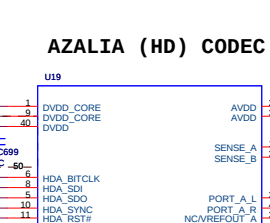
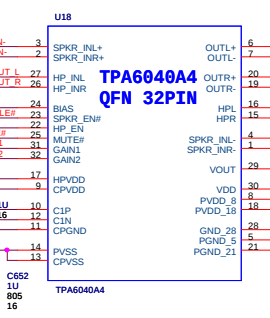


Cap should close to thermal IC

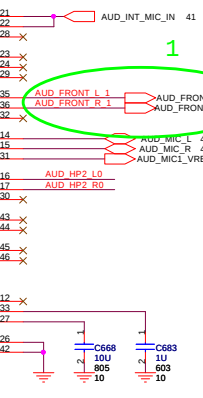
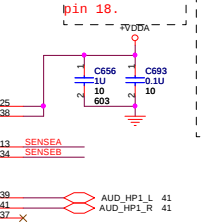
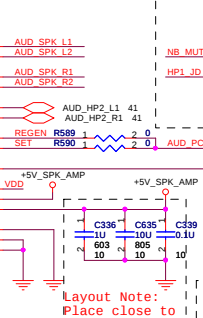




INTERNAL SPEAKER AMP



AZALIA (HD) CODEC

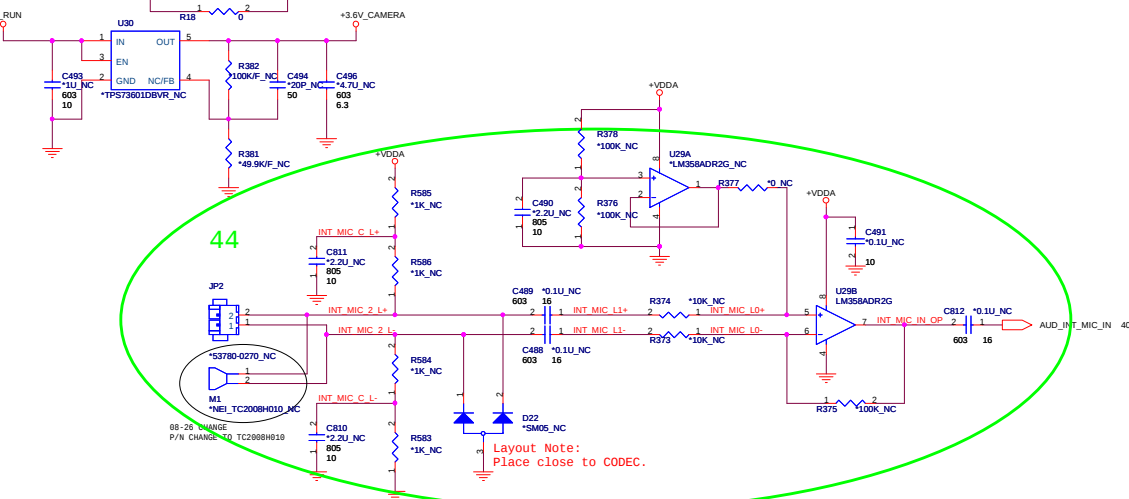
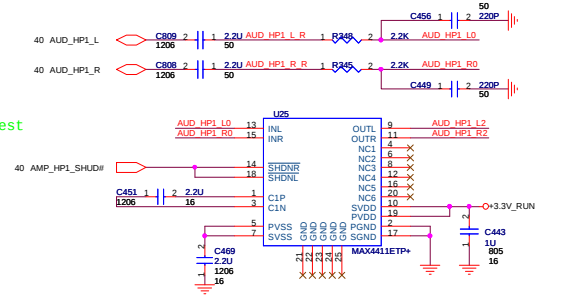
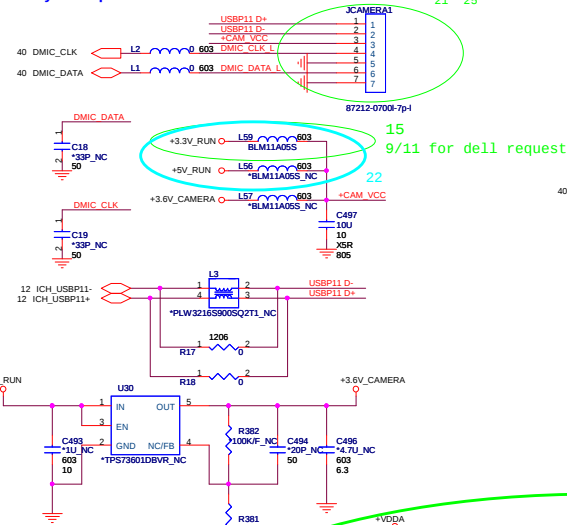
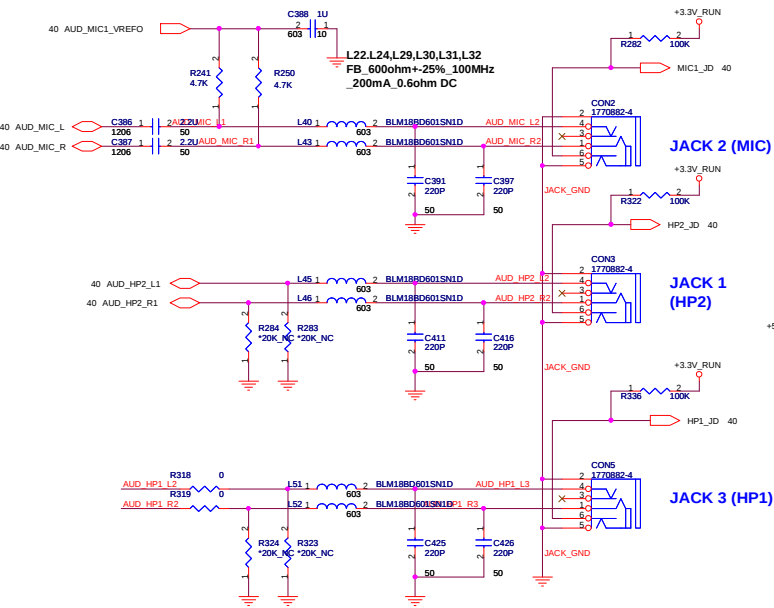


QUANTA

COMPUTER

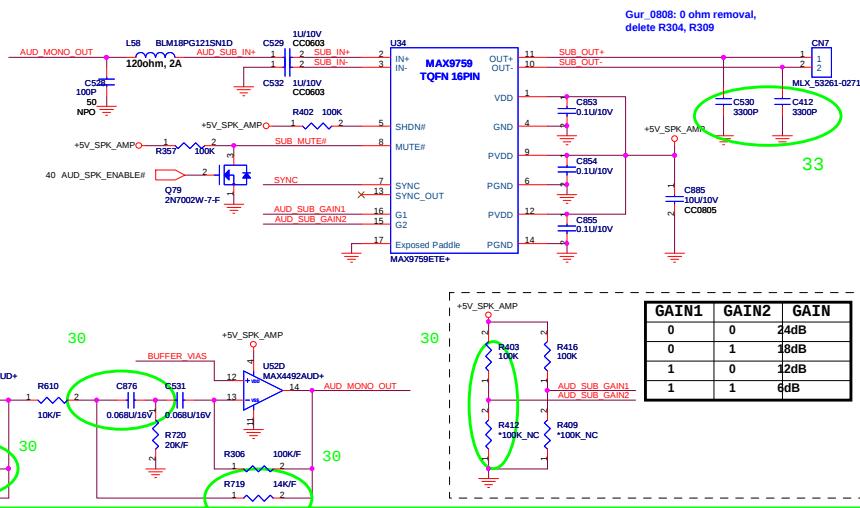
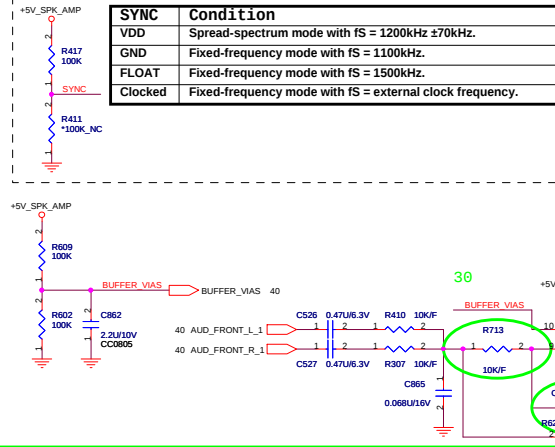
File	Azalia CODEC	Rev	2A
Size	Document Number		
	PMB		
Date	Friday, November 21, 2008	Sheet	40 of 58

Headphone Jack
Stereo MIC Jack

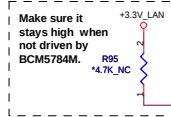
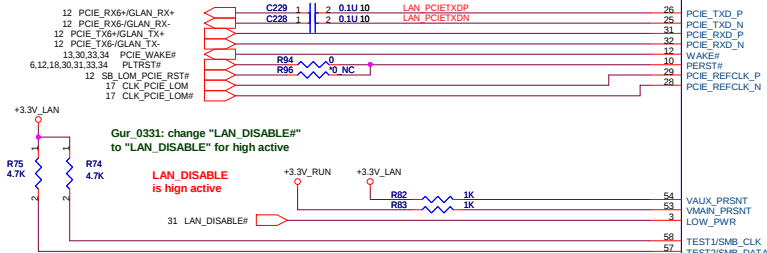
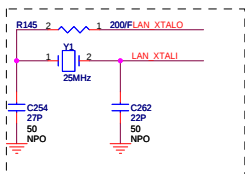
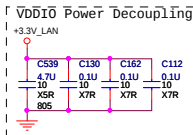
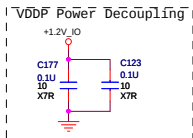
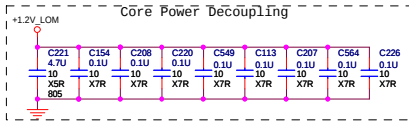


INTERNAL SUBWOOFER AMP

SYNC	Condition
VDD	Spread-spectrum mode with $f_S = 1200\text{kHz} \pm 70\text{kHz}$.
GND	Fixed-frequency mode with $f_S = 1100\text{kHz}$.
FLOAT	Fixed-frequency mode with $f_S = 1500\text{kHz}$.
Clocked	Fixed-frequency mode with $f_S = \text{external clock frequency}$.



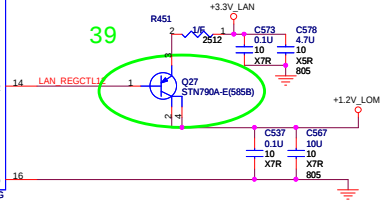
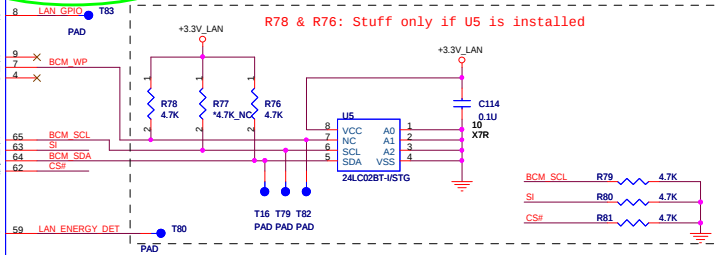
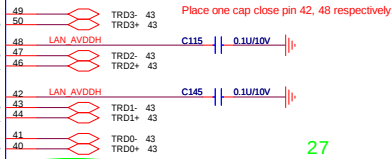
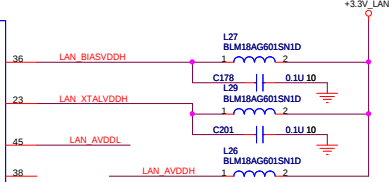
GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB



BCM5784M
10mm x 10mm
68-Pin QFN

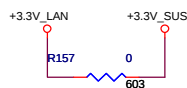
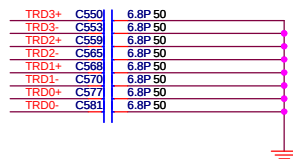
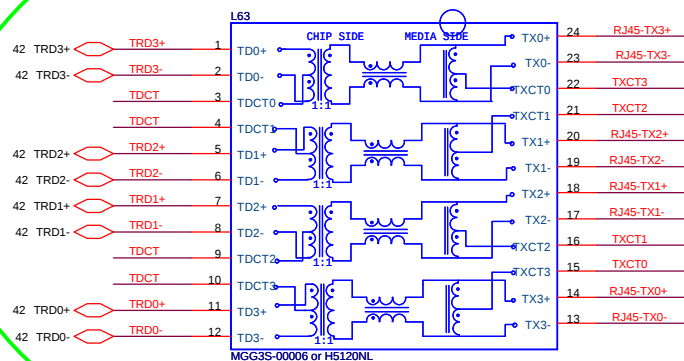
Note: thermal pad

U9



50

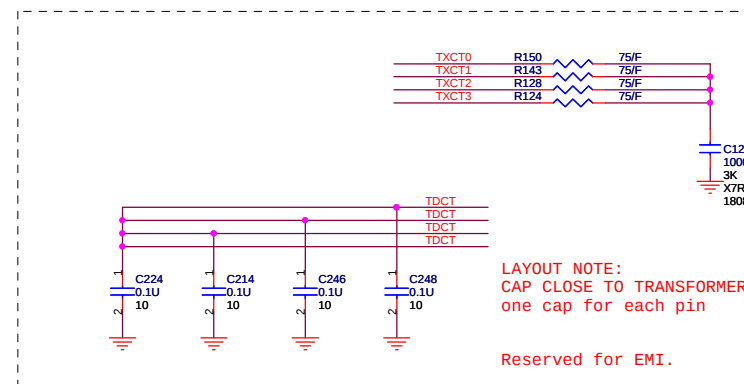
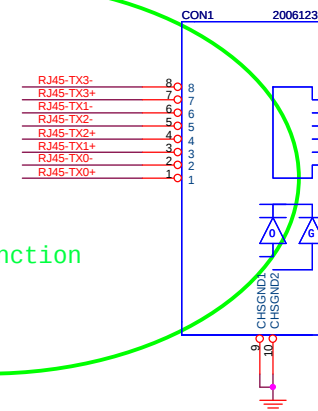
TRANSFORM

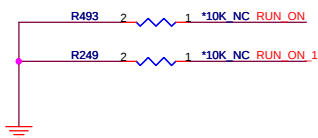
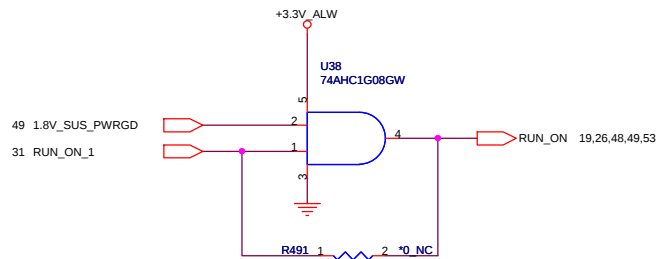
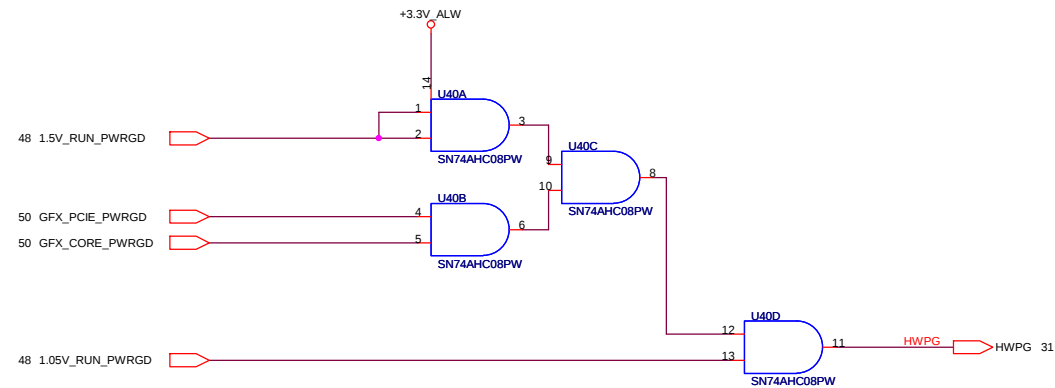
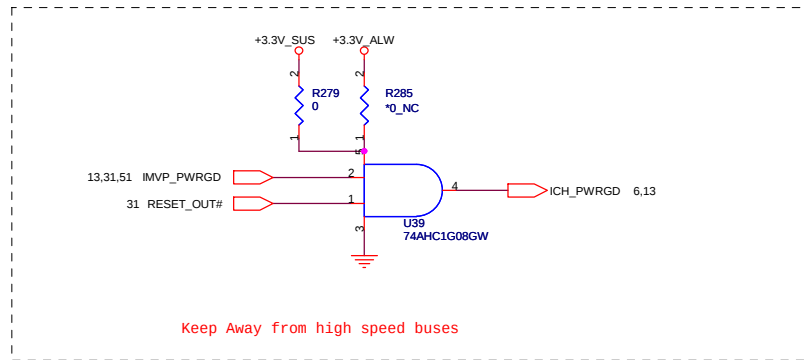


RJ-45 Connector

27

Remove LAN LED function



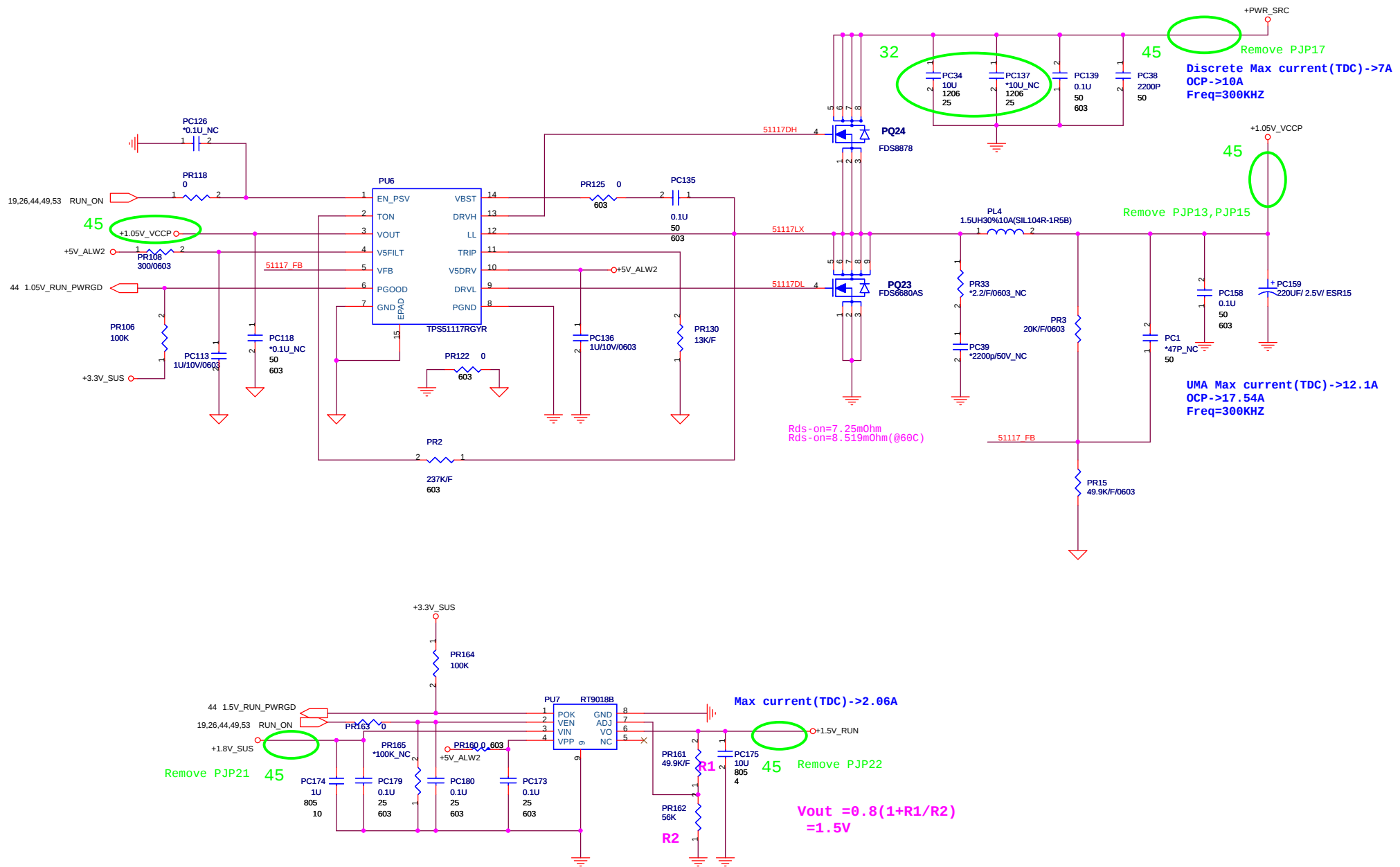


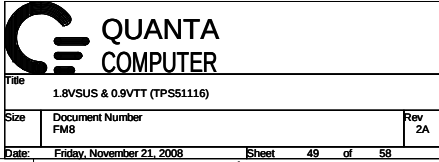
	1	2	3	4	5
A					
B					
C					
D					

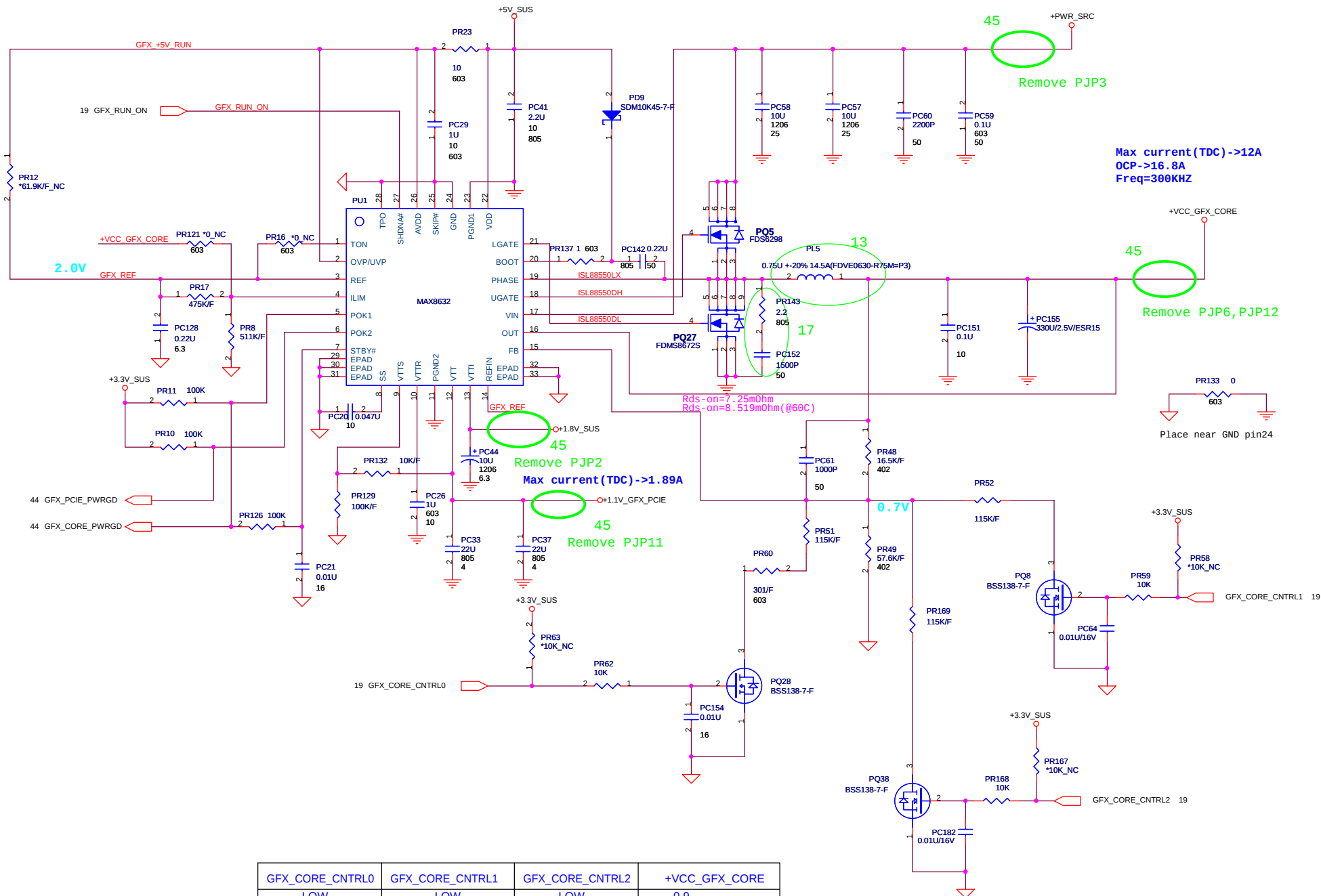
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Title Battery Selector		
Size	Document Number FM8	Rev 2A
Date:	Friday, November 21, 2008	Sheet 45 of 58

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NUMBER SAME AS DISCRETE**

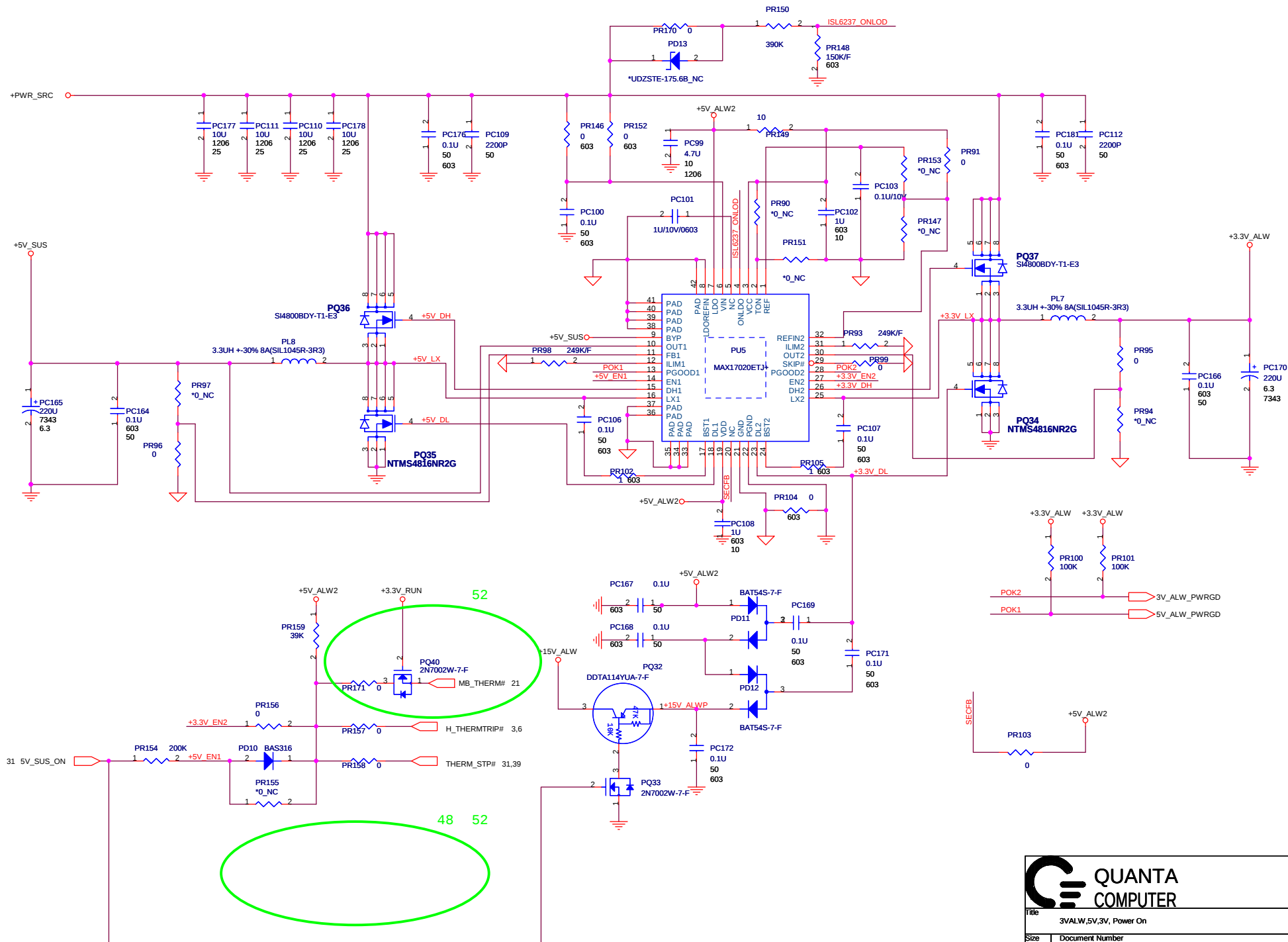
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Title		
Size	Document Number	Rev
FMS		2A
Date:	Friday, November 21, 2008	Sheet 47 of 58

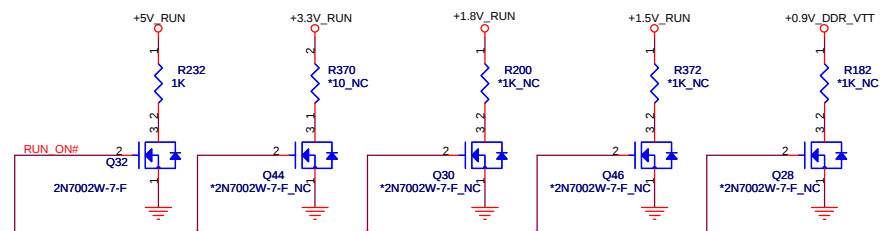
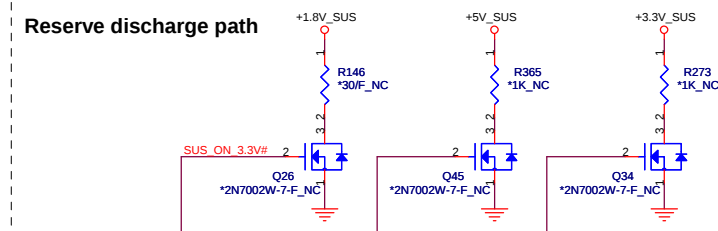
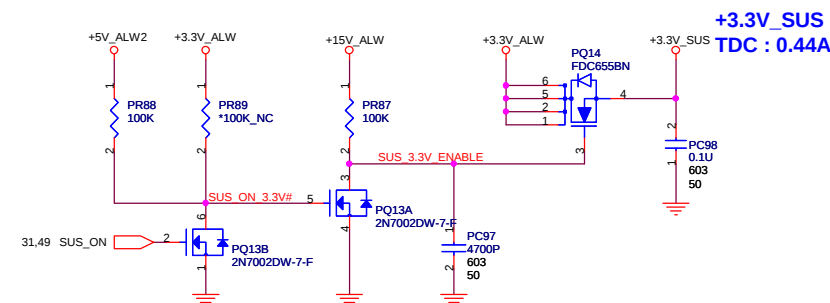




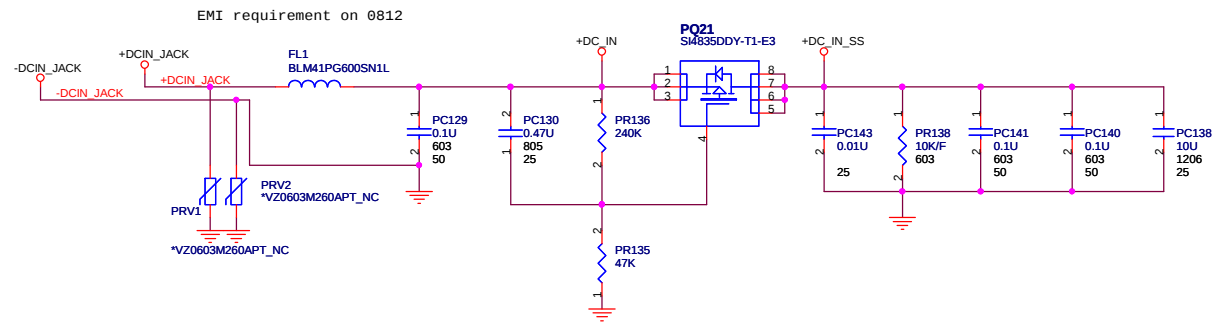
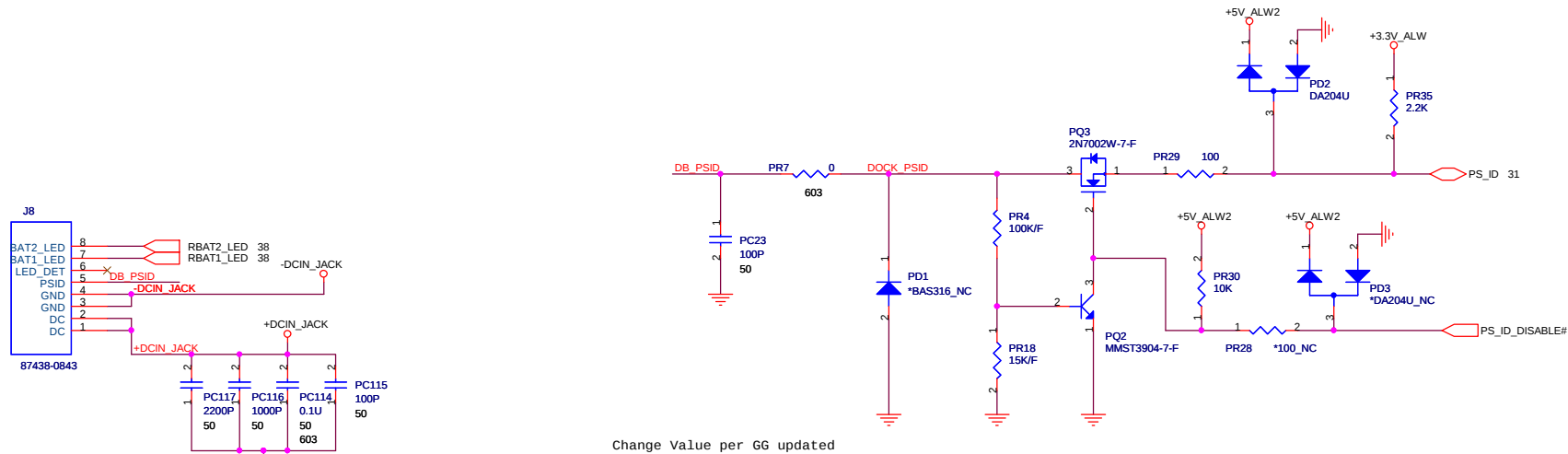
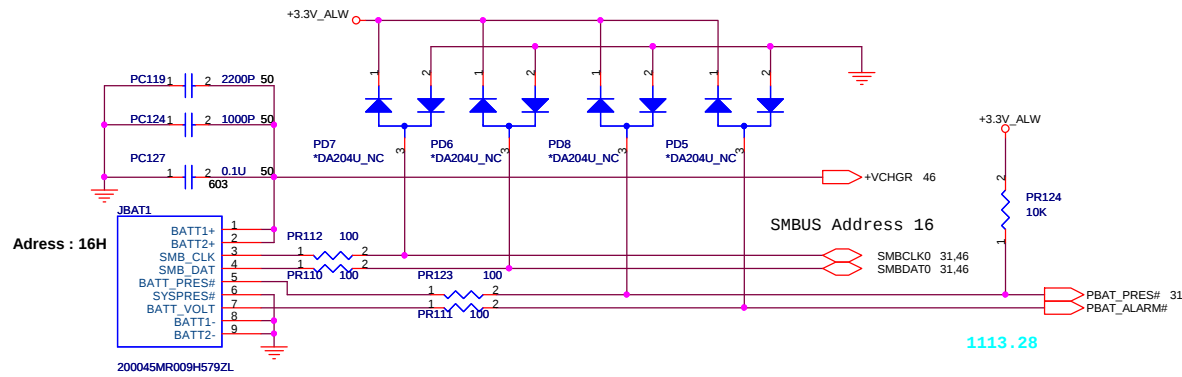


GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	GFX_CORE_CNTRL2	+VCC_GFX_CORE
LOW	LOW	LOW	0.9
HIGH	LOW	LOW	1.0V
HIGH	HIGH	LOW	1.1V
HIGH	HIGH	HIGH	1.2V

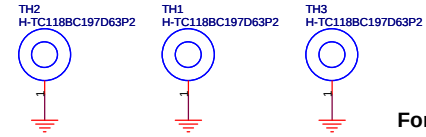
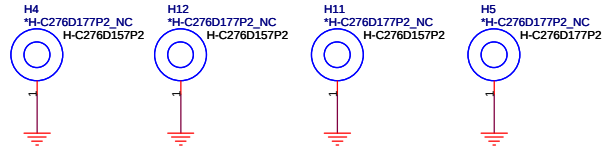




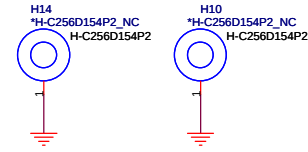
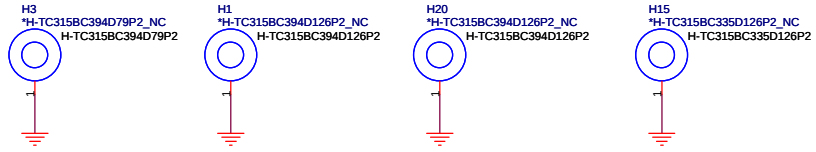
Title			
RUN POWER SW			
Size	Document Number		Rev
	FM8		2A
Date:	Friday, November 21, 2008	Sheet	53 of 58



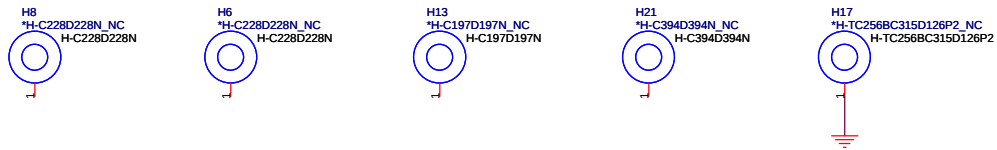
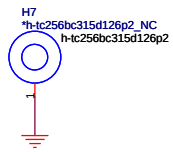
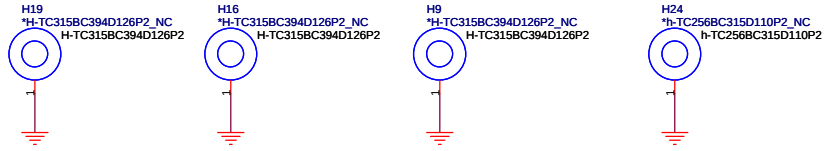
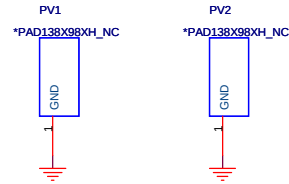
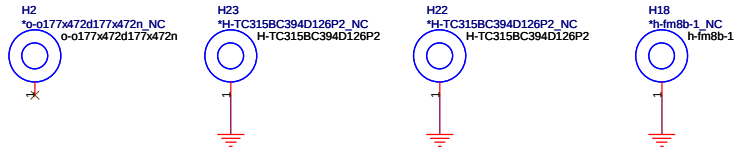
FOR CPU use



For MiniCard nut use.
on 31' header



For GPU nut use.



Title			SCREW PAD
Size	Document Number	Rev	
	FMB	2A	
Date:	Friday, November 21, 2008	Sheet	55 of 58

Reserved for EMI.



QUANTA
COMPUTER

Title		
EMI CAP		
Size	Document Number	Rev
FMS		2A
Date:	Friday, November 21, 2008	Sheet 56 of 58

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SIO
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