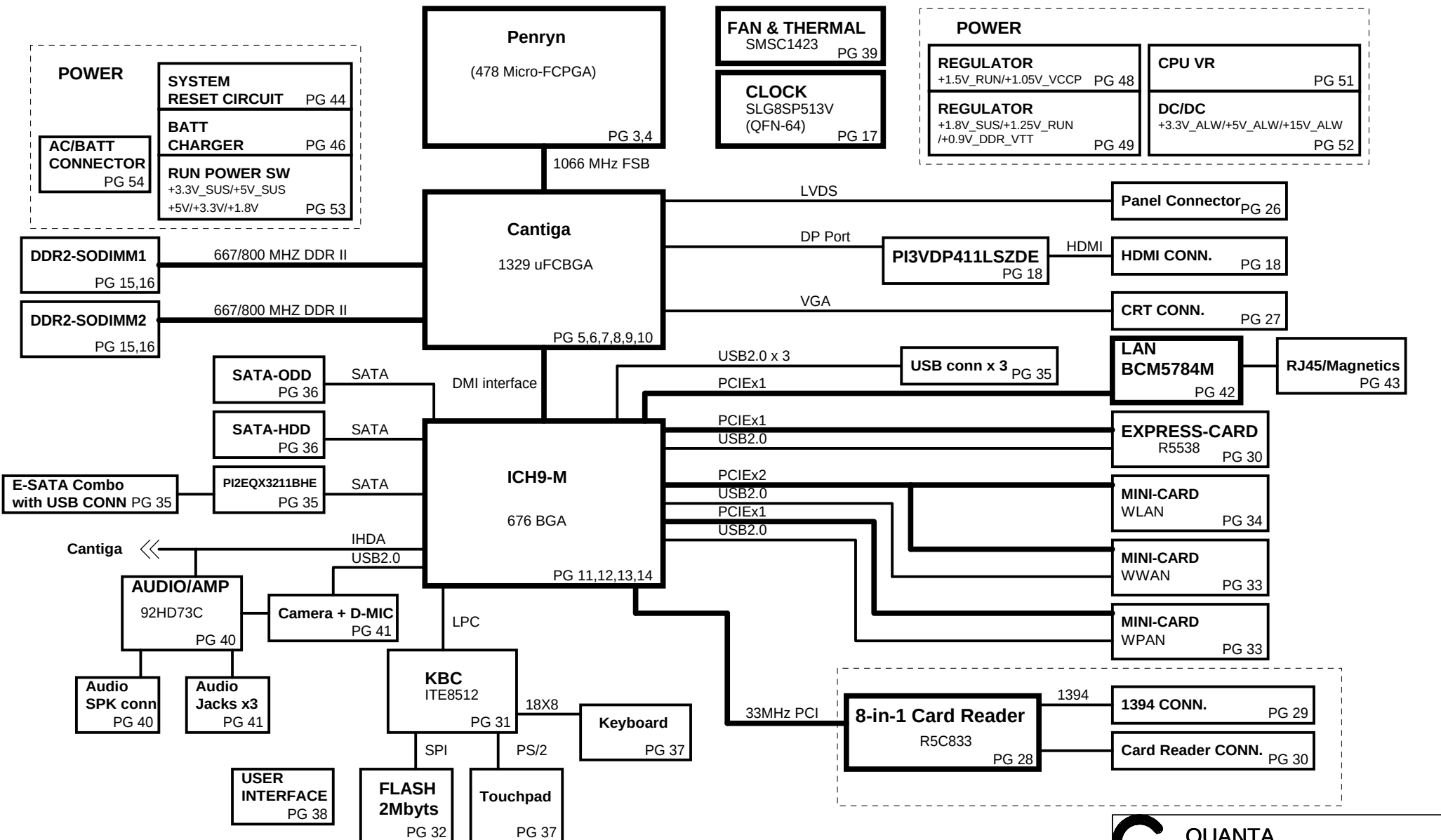


*FM8B MB PCB_NC

FM8B Hanks Intel UMA

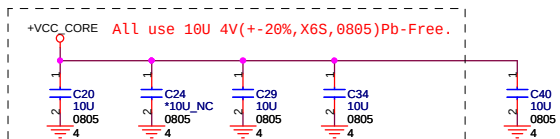
VER : 3A
PWA: W028J
PWA: D178M
PWB: W026J



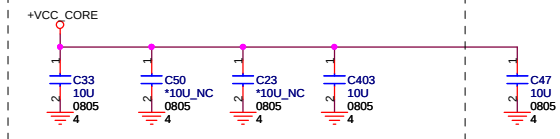
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	Merom
5-10	Crestline
11-14	ICH9
15-16	DDRII SO-DIMM(200P)
17	Clock Generator
18	HDMI
26	LCD Conn. & SSP
27	CRT Conn
36	SATA Conn
28-30	CARD READER/Conn & 1394
30	Express Card & Card reade
33	Mini Card
31	SIO (ITE8512)
32	FLASH/RTC
35	USB
37	TP / KEYBOARD
38	SWITCH /LED
39	FAN & Thermal
40-41	Audio CODEC(ALC888)/Phone Jack
42-43	LOM / Switch
44	System Reset Circuit
46	Battery Selector & Charger
48	1.05VCCP / 1.5VRUN
49	DDR2_1.8VSUS, 0.9V
51	CPU_ISL6262(2phase)
52	MAX8744 (+5.5V,+3,3V)
53	RUN Power Switch
54	DCIN,Batt
55	PAD& SCREW
56	EMI CAP
57	SMBUS BLOCK
58	Power Block Dianram

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,51,52	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	38,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,36,38,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,26,30,37,38,43,48,49,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,53	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,18,27,36,37,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,6,8,9,11,13,14,15,16,17,18 26,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	35,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,40,48,53	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+PBATT	+10V~+17V		MAIN BATTERY	CHG_PBATT	
+SBATT	+10V~+17V		SECOND BATTERY	CHG_SBATT	

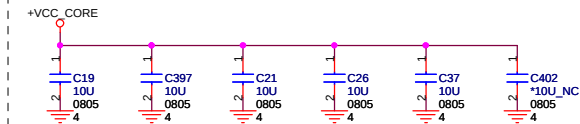
GND PLANE	PAGE	DESCRIPTION
⏏ 8731AGND	46	
⏏ AGND_0.9V	49	
⏏ AGND_DC/DC	52	
⏏ AGND_DC2	48	
⏏ AGND_DDR	49	
⏏ AGND_ISL6260	51	
⏏ GND	ALL	



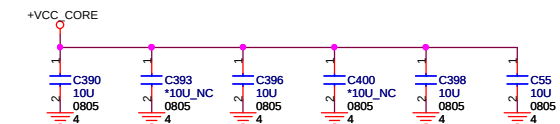
8 inside cavity, north side, secondary layer.



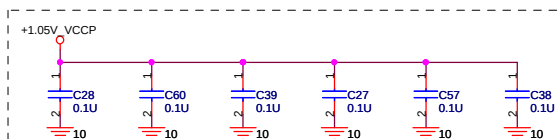
8 inside cavity, south side, secondary layer.



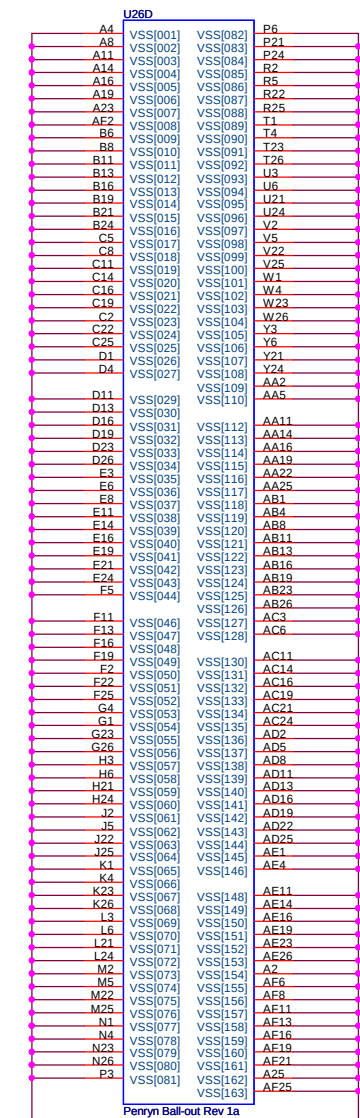
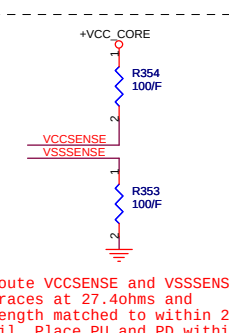
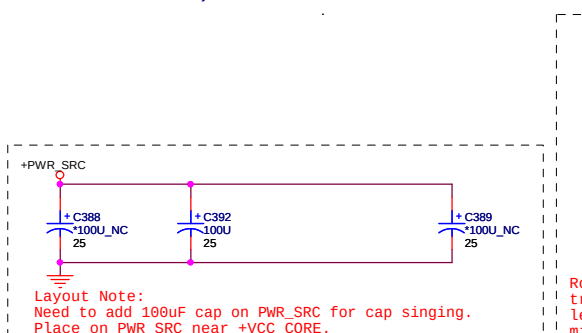
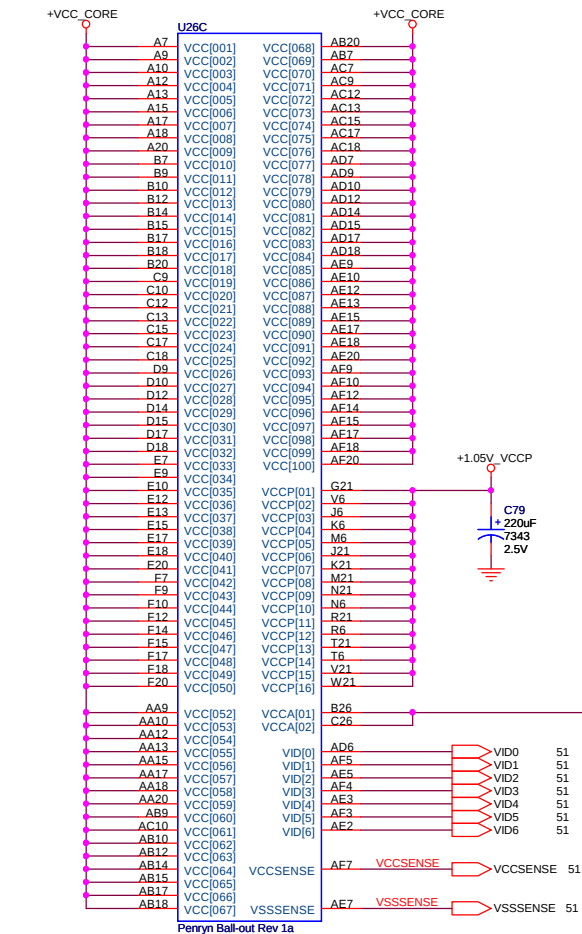
6 inside cavity, north side, primary layer.

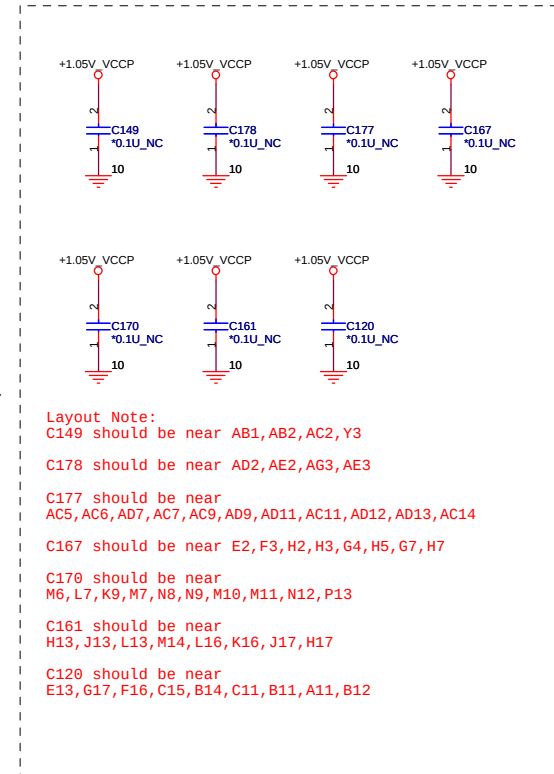
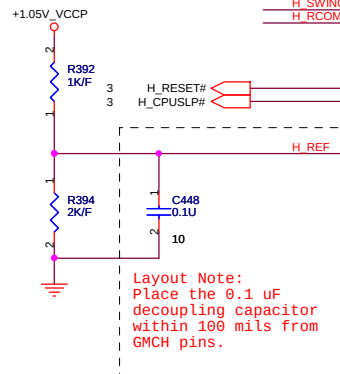
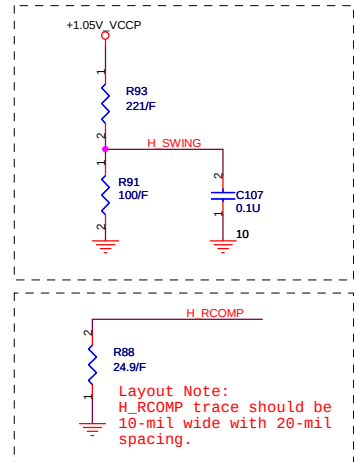


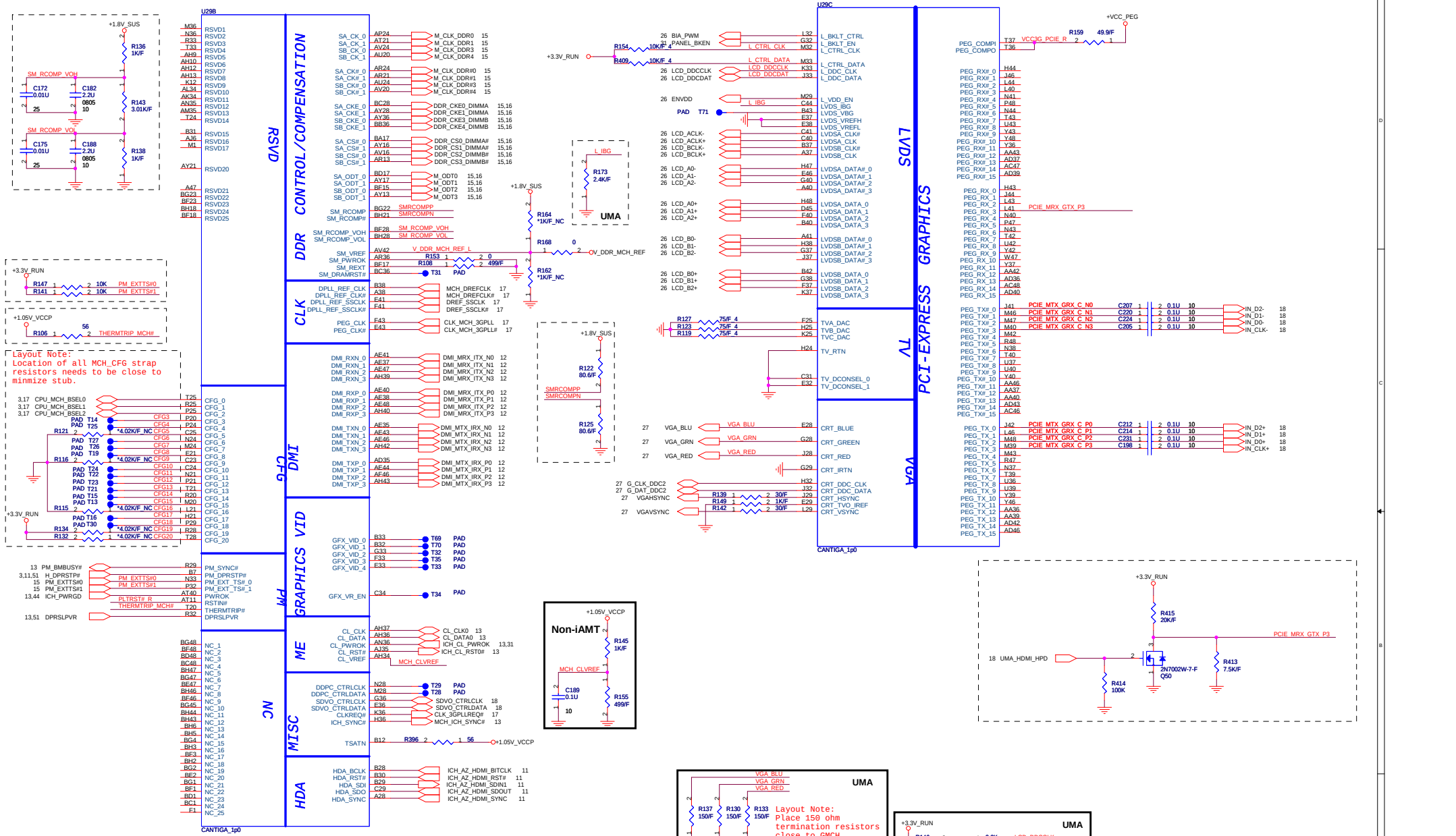
6 inside cavity, south side, primary layer.



Layout out:
Place these inside socket cavity on North side secondary.







CFG5	DMI X2 Select	Low=DMIX2 High=DMIX4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEi1 is operational (defaults) High=SDVO and PCIEi1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present

15 DDR_A_D[0..63]

U29D

DDR A D0	AJ38	SA_DQ_0
DDR A D1	AJ41	SA_DQ_1
DDR A D2	AN38	SA_DQ_2
DDR A D3	AM38	SA_DQ_3
DDR A D4	AJ36	SA_DQ_4
DDR A D5	AJ40	SA_DQ_5
DDR A D6	AM44	SA_DQ_6
DDR A D7	AM42	SA_DQ_7
DDR A D8	AN43	SA_DQ_8
DDR A D9	AN44	SA_DQ_9
DDR A D10	AU40	SA_DQ_10
DDR A D11	AT38	SA_DQ_11
DDR A D12	AN41	SA_DQ_12
DDR A D13	AN39	SA_DQ_13
DDR A D14	AU44	SA_DQ_14
DDR A D15	AU42	SA_DQ_15
DDR A D16	AV39	SA_DQ_16
DDR A D17	AY44	SA_DQ_17
DDR A D18	BA40	SA_DQ_18
DDR A D19	BD43	SA_DQ_19
DDR A D20	AV41	SA_DQ_20
DDR A D21	AY43	SA_DQ_21
DDR A D22	BA41	SA_DQ_22
DDR A D23	BC40	SA_DQ_23
DDR A D24	AY37	SA_DQ_24
DDR A D25	BD38	SA_DQ_25
DDR A D26	AV37	SA_DQ_26
DDR A D27	AT36	SA_DQ_27
DDR A D28	AY38	SA_DQ_28
DDR A D29	BD39	SA_DQ_29
DDR A D30	AV36	SA_DQ_30
DDR A D31	AW36	SA_DQ_31
DDR A D32	BD13	SA_DQ_32
DDR A D33	AU11	SA_DQ_33
DDR A D34	BC11	SA_DQ_34
DDR A D35	BA12	SA_DQ_35
DDR A D36	AU13	SA_DQ_36
DDR A D37	AV13	SA_DQ_37
DDR A D38	BD12	SA_DQ_38
DDR A D39	BC12	SA_DQ_39
DDR A D40	BA9	SA_DQ_40
DDR A D41	BA9	SA_DQ_41
DDR A D42	AU10	SA_DQ_42
DDR A D43	AV9	SA_DQ_43
DDR A D44	BA11	SA_DQ_44
DDR A D45	BD9	SA_DQ_45
DDR A D46	AY8	SA_DQ_46
DDR A D47	BA6	SA_DQ_47
DDR A D48	AV5	SA_DQ_48
DDR A D49	AV7	SA_DQ_49
DDR A D50	AT9	SA_DQ_50
DDR A D51	AN8	SA_DQ_51
DDR A D52	AU5	SA_DQ_52
DDR A D53	AU6	SA_DQ_53
DDR A D54	AT5	SA_DQ_54
DDR A D55	AN10	SA_DQ_55
DDR A D56	AM11	SA_DQ_56
DDR A D57	AM5	SA_DQ_57
DDR A D58	AJ9	SA_DQ_58
DDR A D59	AJ8	SA_DQ_59
DDR A D60	AN12	SA_DQ_60
DDR A D61	AM13	SA_DQ_61
DDR A D62	AJ11	SA_DQ_62
DDR A D63	AJ12	SA_DQ_63

CANTIGA_1p0

DDR SYSTEM MEMORY A

SA_BS_0	BD21	DDR A BS0
SA_BS_1	BG18	DDR A BS1
SA_BS_2	AT25	DDR A BS2
SA_RAS#	BB20	DDR A RAS#
SA_CAS#	BD20	DDR A CAS#
SA_WE#	AY20	DDR A WE#
SA_DM_0	AM37	DDR A DM0
SA_DM_1	AT41	DDR A DM1
SA_DM_2	AY41	DDR A DM2
SA_DM_3	AU39	DDR A DM3
SA_DM_4	BB12	DDR A DM4
SA_DM_5	AY6	DDR A DM5
SA_DM_6	AT7	DDR A DM6
SA_DM_7	AJ5	DDR A DM7
SA_DQS_0	AJ44	DDR A DQS0
SA_DQS_1	AT44	DDR A DQS1
SA_DQS_2	BA43	DDR A DQS2
SA_DQS_3	BC37	DDR A DQS3
SA_DQS_4	AW12	DDR A DQS4
SA_DQS_5	BC8	DDR A DQS5
SA_DQS_6	AU8	DDR A DQS6
SA_DQS_7	AM7	DDR A DQS7
SA_DQS#_0	AJ43	DDR A DQS#0
SA_DQS#_1	BA44	DDR A DQS#1
SA_DQS#_2	BD37	DDR A DQS#2
SA_DQS#_3	AY12	DDR A DQS#3
SA_DQS#_4	BD8	DDR A DQS#4
SA_DQS#_5	AU9	DDR A DQS#5
SA_DQS#_6	AM8	DDR A DQS#6
SA_DQS#_7	BA21	DDR A MA0
SA_MA_0	BC24	DDR A MA1
SA_MA_1	BG24	DDR A MA2
SA_MA_2	BH24	DDR A MA3
SA_MA_3	BG25	DDR A MA4
SA_MA_4	BA24	DDR A MA5
SA_MA_5	BD24	DDR A MA6
SA_MA_6	BG27	DDR A MA7
SA_MA_7	BF25	DDR A MA8
SA_MA_8	AW24	DDR A MA9
SA_MA_9	BC21	DDR A MA10
SA_MA_10	BG26	DDR A MA11
SA_MA_11	BH26	DDR A MA12
SA_MA_12	BH17	DDR A MA13
SA_MA_13	AY25	DDR A MA14

15 DDR_B_D[0..63]

U29E

DDR B D0	AK47	SB_DQ_0
DDR B D1	AH46	SB_DQ_1
DDR B D2	AP47	SB_DQ_2
DDR B D3	AP46	SB_DQ_3
DDR B D4	AJ46	SB_DQ_4
DDR B D5	AJ48	SB_DQ_5
DDR B D6	AM48	SB_DQ_6
DDR B D7	AP48	SB_DQ_7
DDR B D8	AU47	SB_DQ_8
DDR B D9	AU46	SB_DQ_9
DDR B D10	BA48	SB_DQ_10
DDR B D11	AY48	SB_DQ_11
DDR B D12	AT47	SB_DQ_12
DDR B D13	AR47	SB_DQ_13
DDR B D14	BA47	SB_DQ_14
DDR B D15	BC47	SB_DQ_15
DDR B D16	BC46	SB_DQ_16
DDR B D17	BC44	SB_DQ_17
DDR B D18	BG43	SB_DQ_18
DDR B D19	BF43	SB_DQ_19
DDR B D20	BE45	SB_DQ_20
DDR B D21	BC41	SB_DQ_21
DDR B D22	BF40	SB_DQ_22
DDR B D23	BE41	SB_DQ_23
DDR B D24	BG38	SB_DQ_24
DDR B D25	BF38	SB_DQ_25
DDR B D26	BH35	SB_DQ_26
DDR B D27	BG35	SB_DQ_27
DDR B D28	BH40	SB_DQ_28
DDR B D29	BG39	SB_DQ_29
DDR B D30	BG34	SB_DQ_30
DDR B D31	BH34	SB_DQ_31
DDR B D32	BH14	SB_DQ_32
DDR B D33	BG12	SB_DQ_33
DDR B D34	BH11	SB_DQ_34
DDR B D35	BG8	SB_DQ_35
DDR B D36	BH12	SB_DQ_36
DDR B D37	BF11	SB_DQ_37
DDR B D38	BF8	SB_DQ_38
DDR B D39	BG7	SB_DQ_39
DDR B D40	BC5	SB_DQ_40
DDR B D41	BC6	SB_DQ_41
DDR B D42	AY3	SB_DQ_42
DDR B D43	AY1	SB_DQ_43
DDR B D44	BF6	SB_DQ_44
DDR B D45	BF5	SB_DQ_45
DDR B D46	BA1	SB_DQ_46
DDR B D47	BD3	SB_DQ_47
DDR B D48	AV2	SB_DQ_48
DDR B D49	AU3	SB_DQ_49
DDR B D50	AR3	SB_DQ_50
DDR B D51	AN2	SB_DQ_51
DDR B D52	AY2	SB_DQ_52
DDR B D53	AV1	SB_DQ_53
DDR B D54	AP3	SB_DQ_54
DDR B D55	AR1	SB_DQ_55
DDR B D56	AL1	SB_DQ_56
DDR B D57	AL2	SB_DQ_57
DDR B D58	AJ1	SB_DQ_58
DDR B D59	AH1	SB_DQ_59
DDR B D60	AM2	SB_DQ_60
DDR B D61	AM3	SB_DQ_61
DDR B D62	AH3	SB_DQ_62
DDR B D63	AJ3	SB_DQ_63

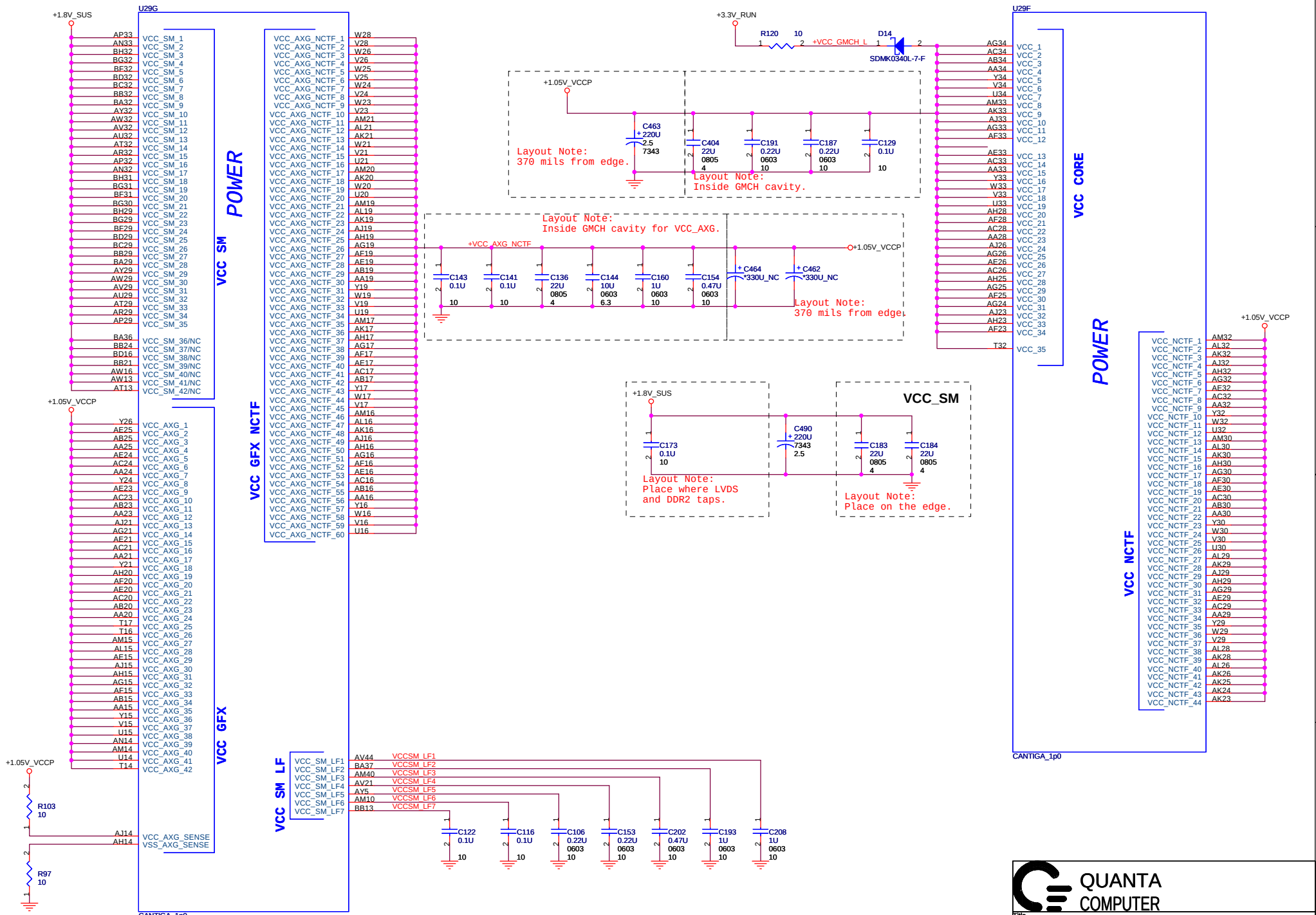
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DDR SYSTEM MEMORY B

SB_BS_0	BC16	DDR B BS0
SB_BS_1	BB17	DDR B BS1
SB_BS_2	BB33	DDR B BS2
SB_RAS#	AU17	DDR B RAS#
SB_CAS#	BG16	DDR B CAS#
SB_WE#	BF14	DDR B WE#
SB_DM_0	AM47	DDR B DM0
SB_DM_1	AY47	DDR B DM1
SB_DM_2	BD40	DDR B DM2
SB_DM_3	BF35	DDR B DM3
SB_DM_4	BG11	DDR B DM4
SB_DM_5	BA3	DDR B DM5
SB_DM_6	AP1	DDR B DM6
SB_DM_7	AK2	DDR B DM7
SB_DQS_0	AL47	DDR B DQS0
SB_DQS_1	AV48	DDR B DQS1
SB_DQS_2	BG41	DDR B DQS2
SB_DQS_3	BG37	DDR B DQS3
SB_DQS_4	BH9	DDR B DQS4
SB_DQS_5	BB2	DDR B DQS5
SB_DQS_6	AU1	DDR B DQS6
SB_DQS_7	AN6	DDR B DQS7
SB_DQS#_0	AL46	DDR B DQS#0
SB_DQS#_1	AV47	DDR B DQS#1
SB_DQS#_2	BH41	DDR B DQS#2
SB_DQS#_3	BH37	DDR B DQS#3
SB_DQS#_4	BG9	DDR B DQS#4
SB_DQS#_5	BC2	DDR B DQS#5
SB_DQS#_6	AT2	DDR B DQS#6
SB_DQS#_7	AN5	DDR B DQS#7
SB_MA_0	AV17	DDR B MA0
SB_MA_1	BA25	DDR B MA1
SB_MA_2	BC25	DDR B MA2
SB_MA_3	AU25	DDR B MA3
SB_MA_4	AW25	DDR B MA4
SB_MA_5	BB28	DDR B MA5
SB_MA_6	AU28	DDR B MA6
SB_MA_7	AW28	DDR B MA7
SB_MA_8	AT33	DDR B MA8
SB_MA_9	BD33	DDR B MA9
SB_MA_10	BB16	DDR B MA10
SB_MA_11	AW33	DDR B MA11
SB_MA_12	AY33	DDR B MA12
SB_MA_13	BH15	DDR B MA13
SB_MA_14	AJ33	DDR B MA14



Title Crestline (DDR2)		
Size FMB8	Document Number FMB8	Rev 3A
Date: Thursday, October 09, 2008	Sheet 7	of 58

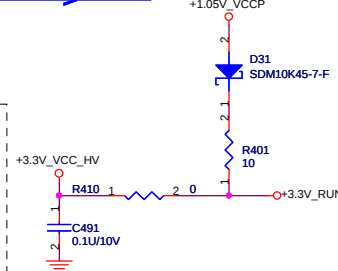
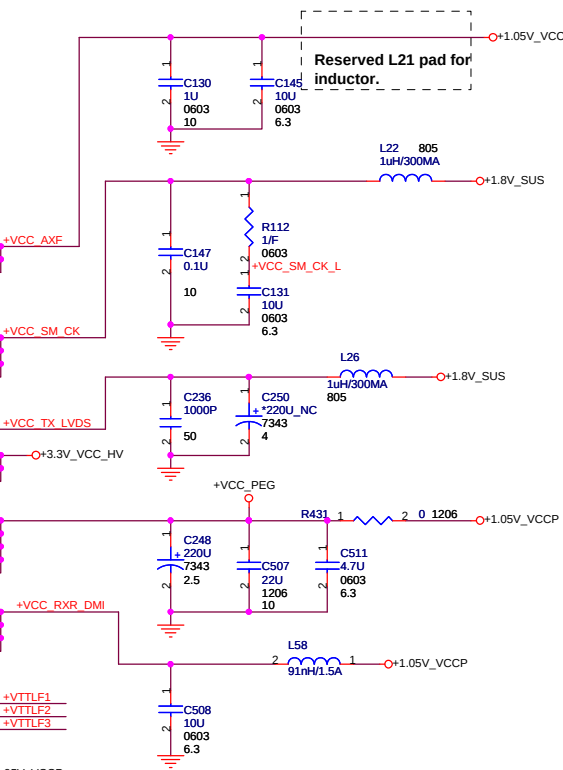
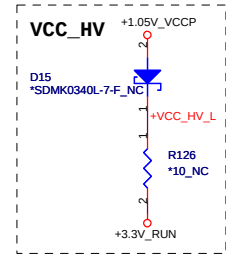
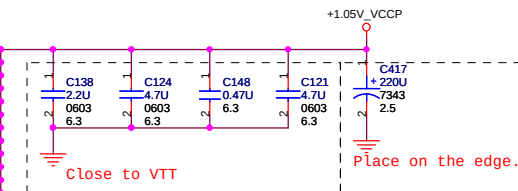
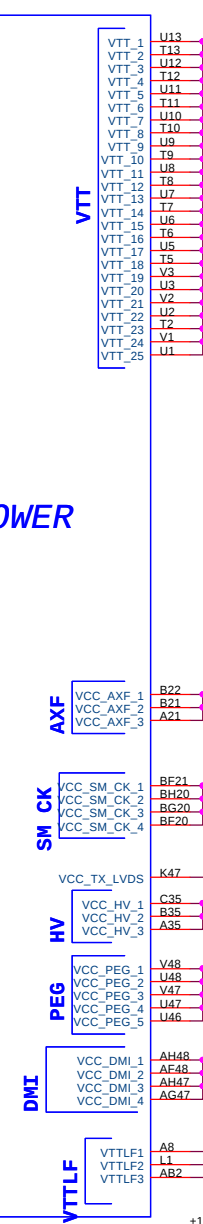
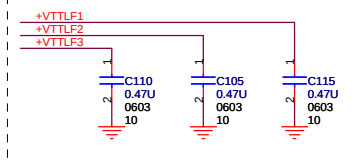
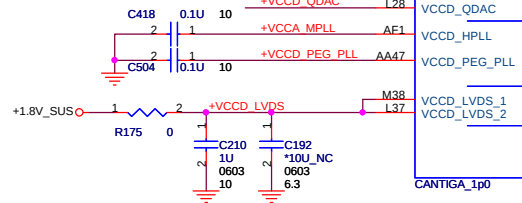
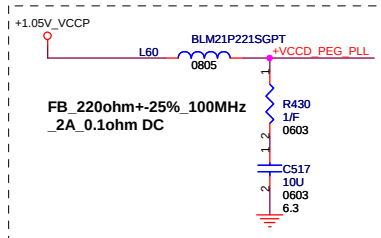
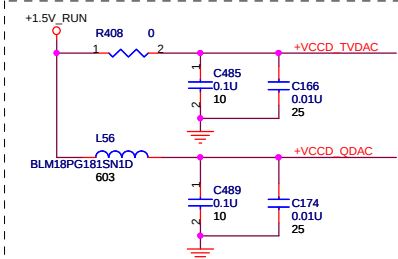
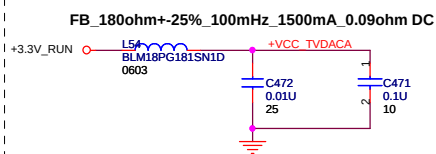
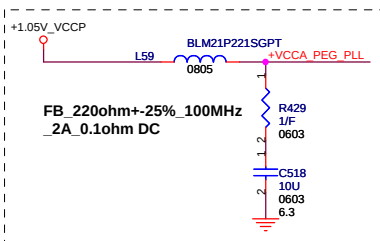
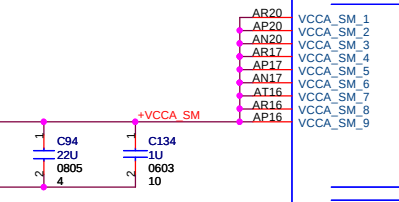
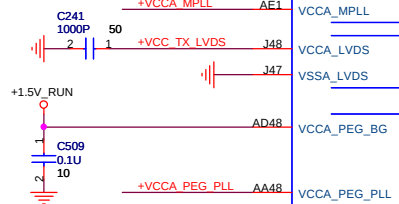
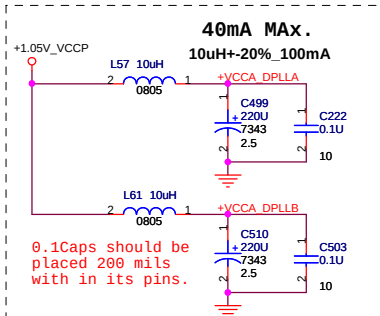
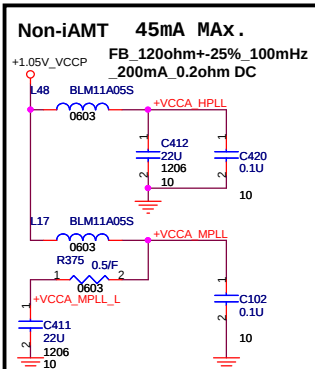
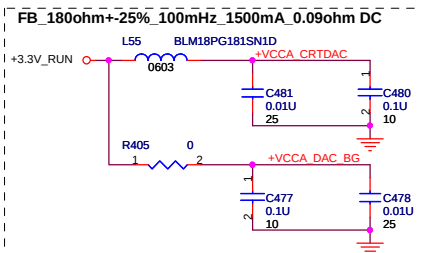


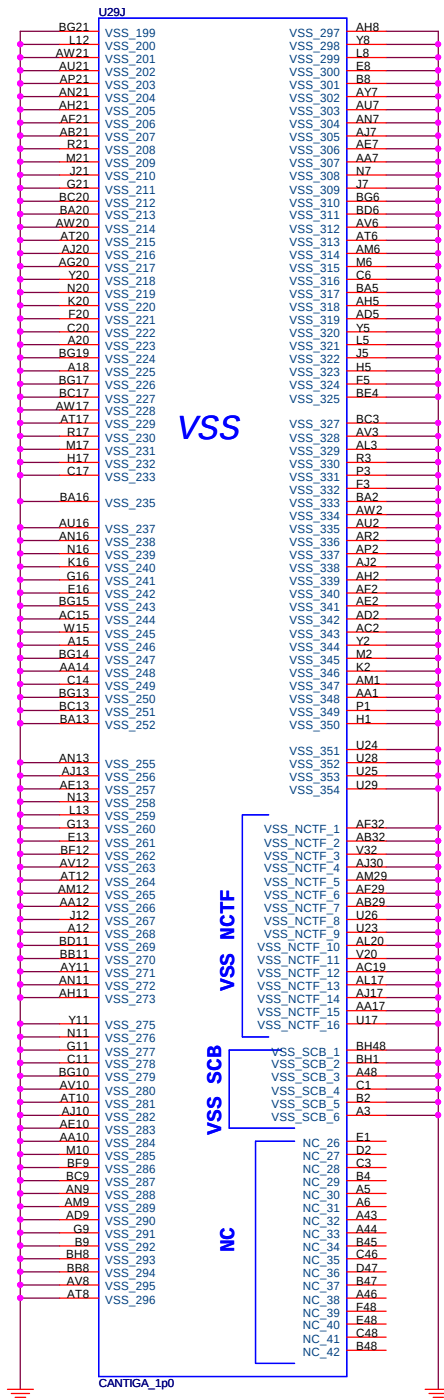
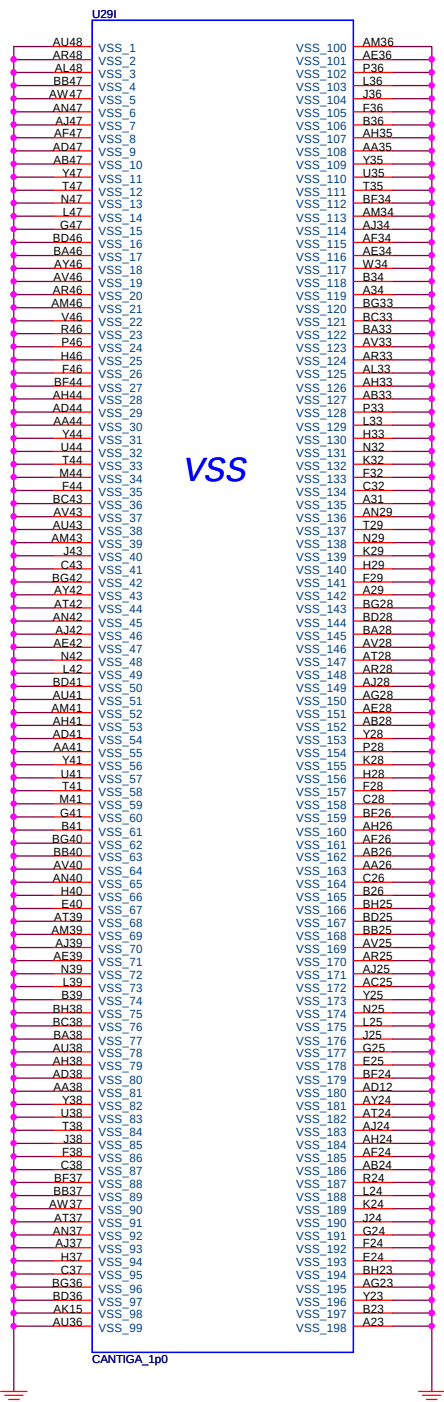
UMA: Places R103, R97 to 10 ohm.
DIS: Please R103, R97 to 0 ohm.



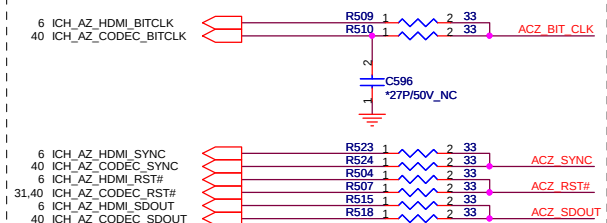
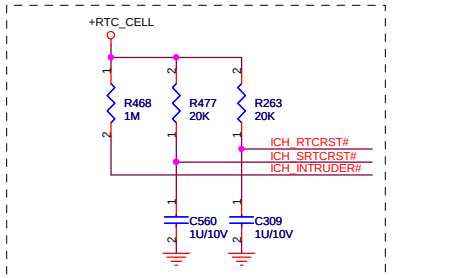
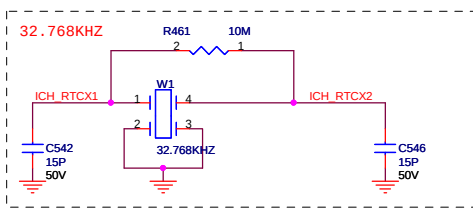
QUANTA
COMPUTER

Title Crestline (VCC,NCTF)		
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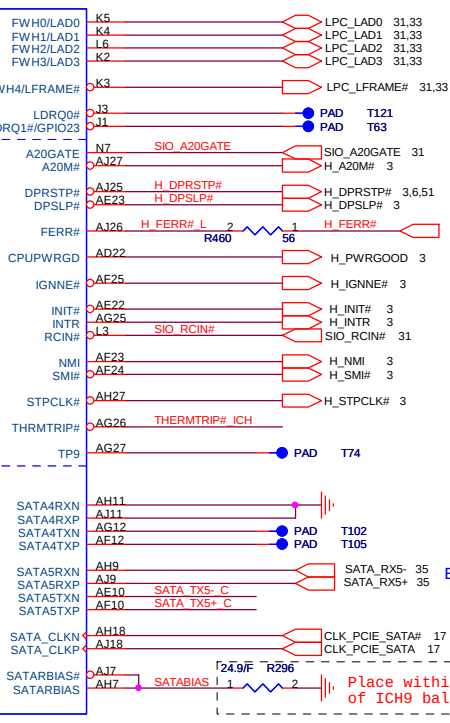
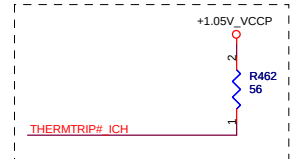
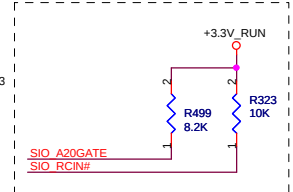
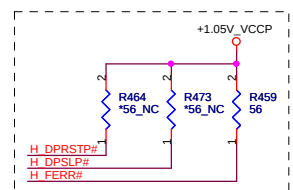
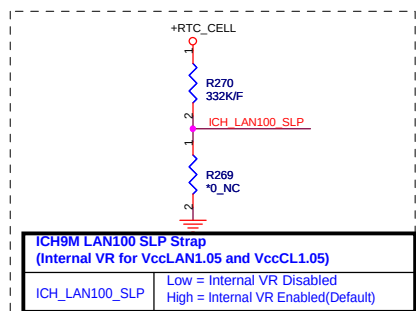
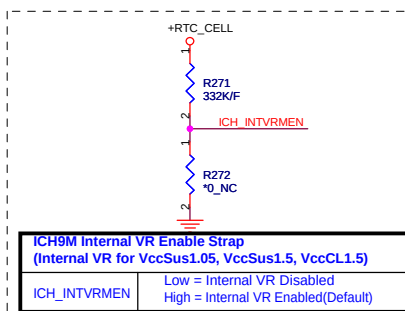
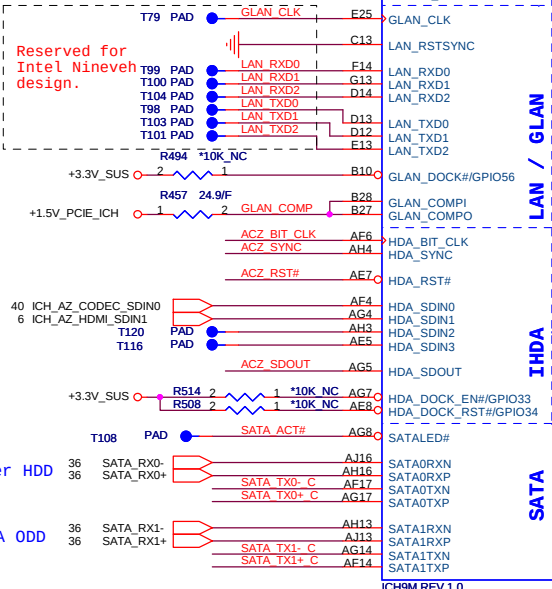
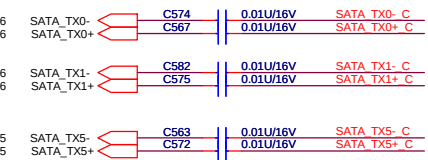




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Title Crestline (VSS)		
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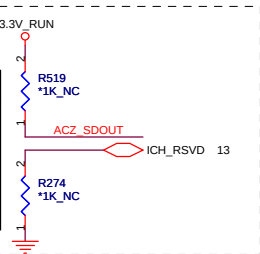
Place all series terms close to ICH9 except for SDIN input lines, which should be close to source. Placement of R523, R524, R509 & R510 should equal distance to the T split trace point as R504 & R507, R515 & R516 respectively. Basically, keep the same distance from T for all series termination resistors.

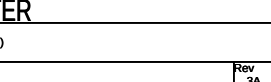


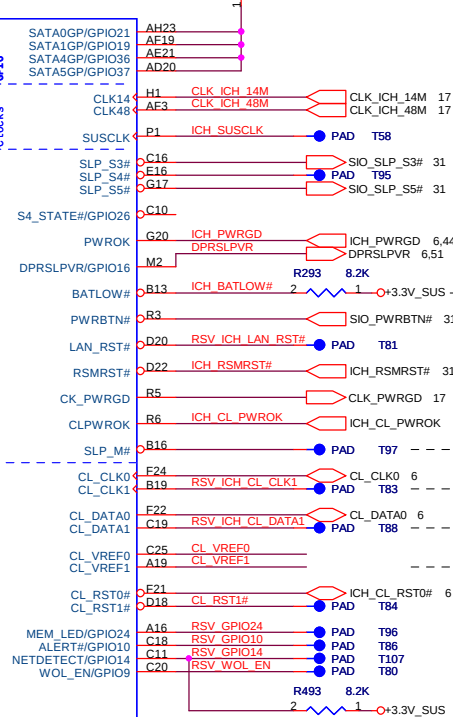
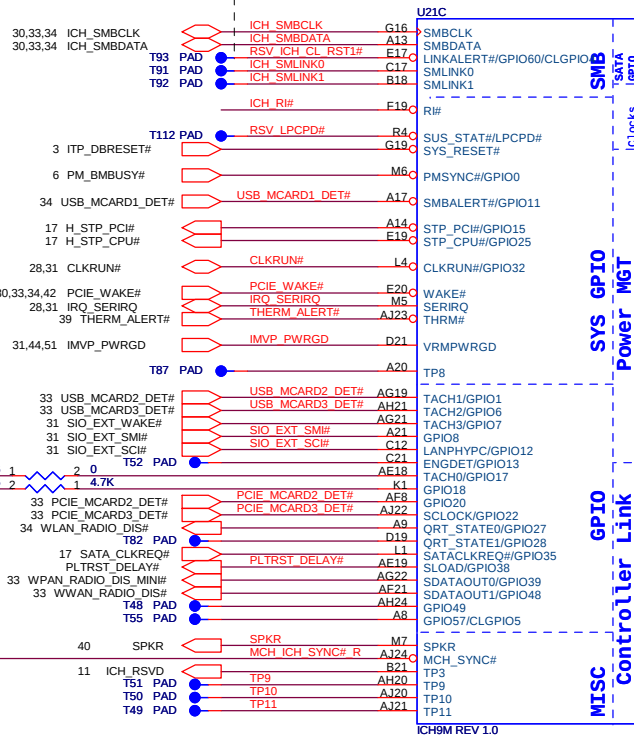
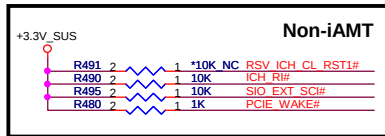
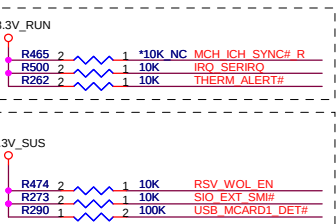
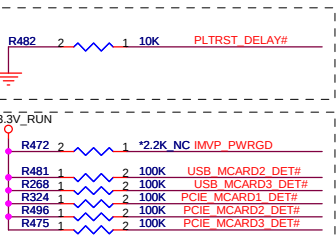
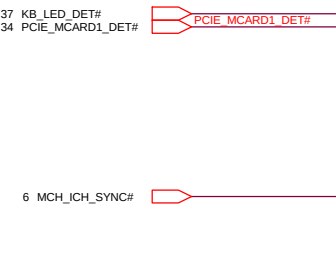
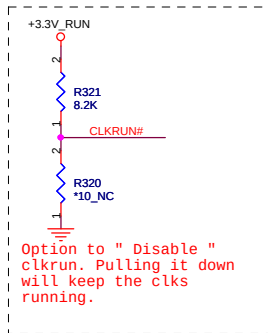
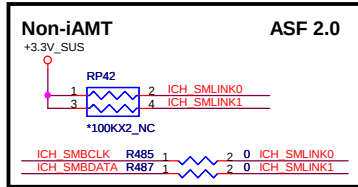
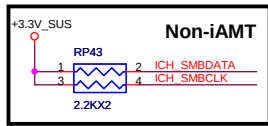
E-SATA



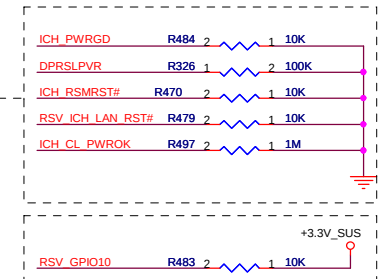
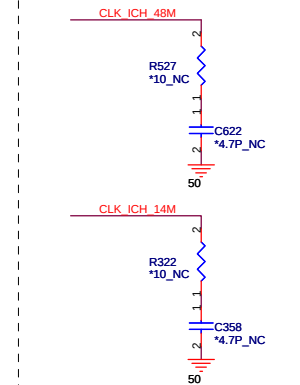
XOR Chain Entrance Strap		
ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIe port config bit 1



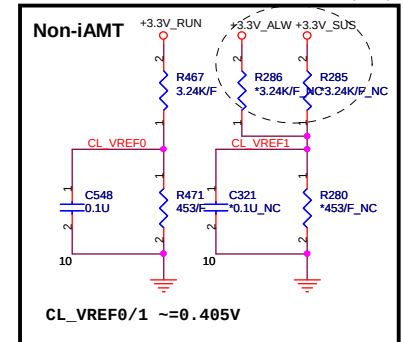




Place these close to ICH9.

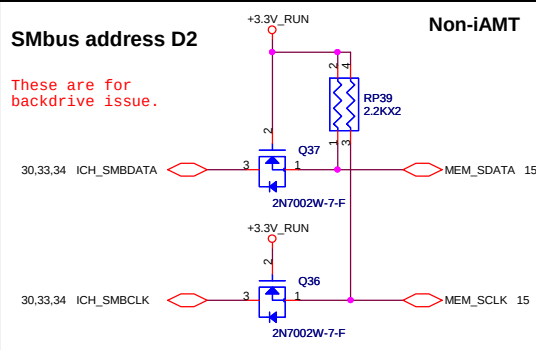


DIS:ALW
UMA:SUS (19)



SMBus address D2

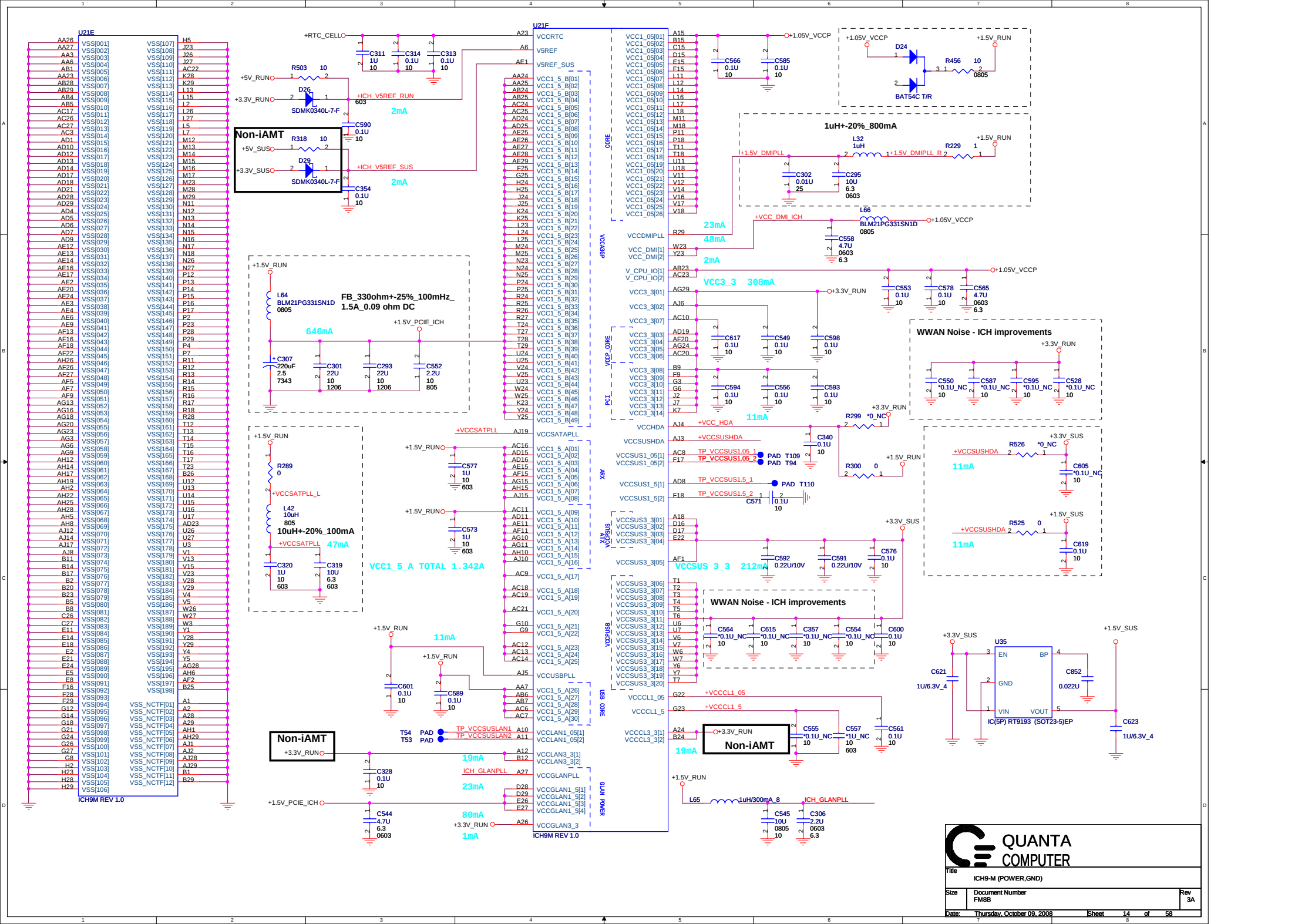
These are for backdrive issue.



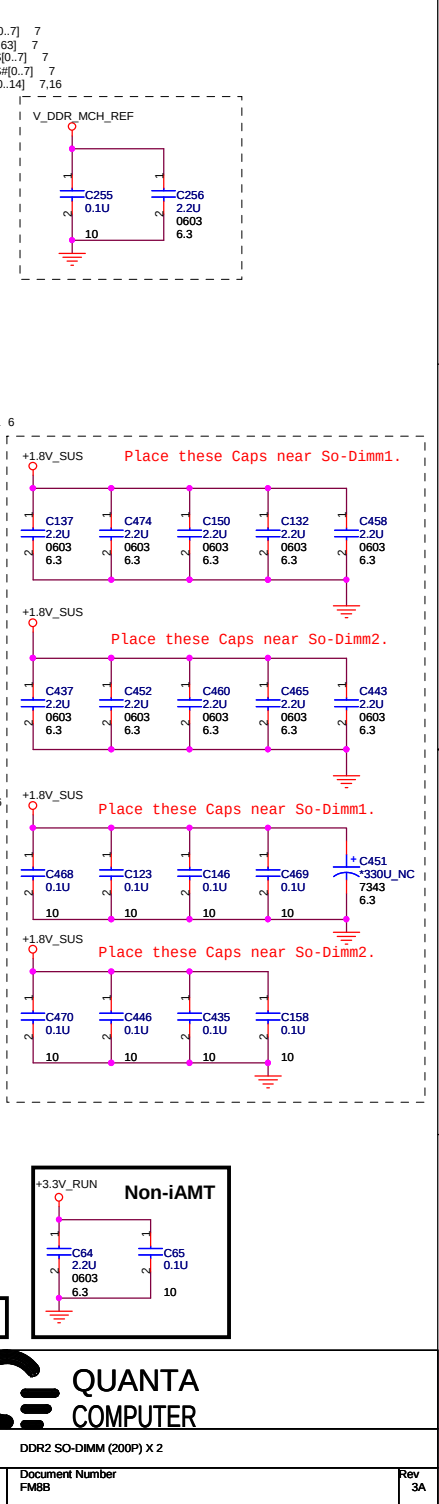
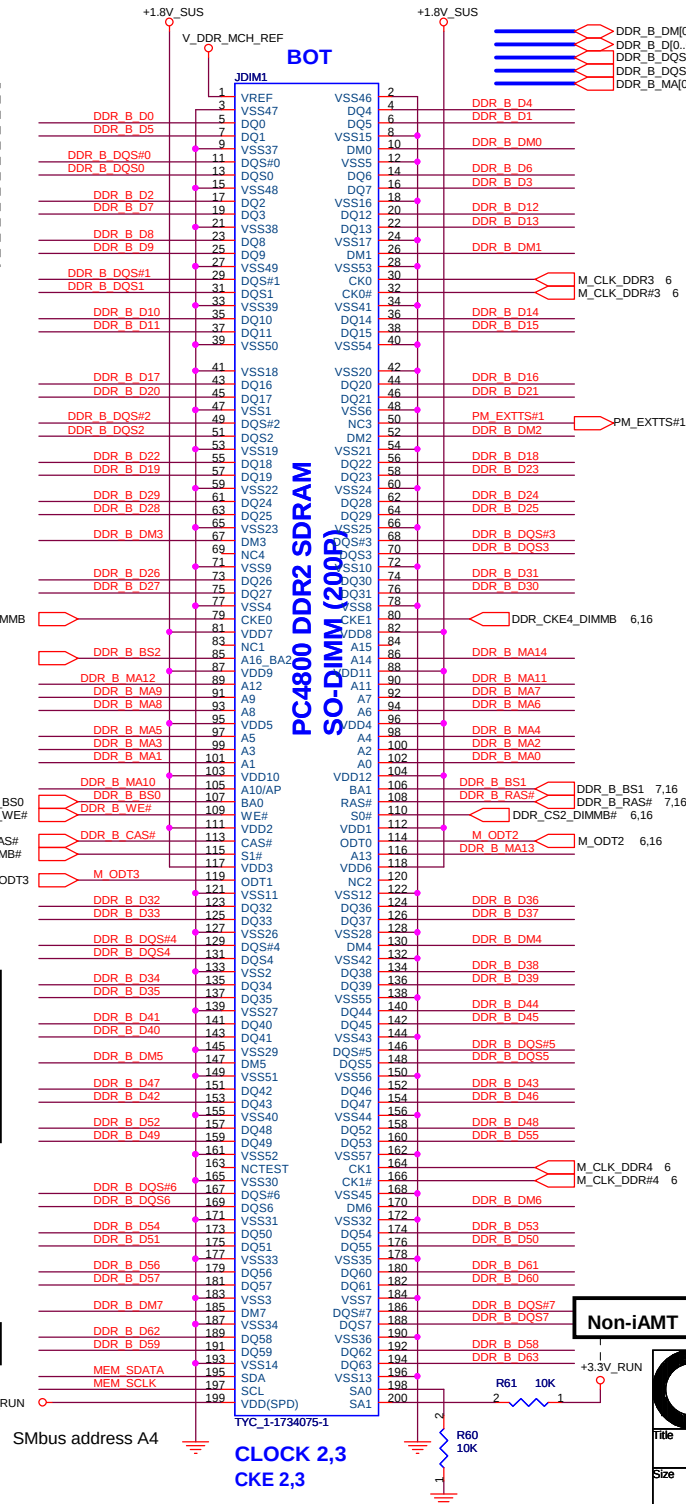
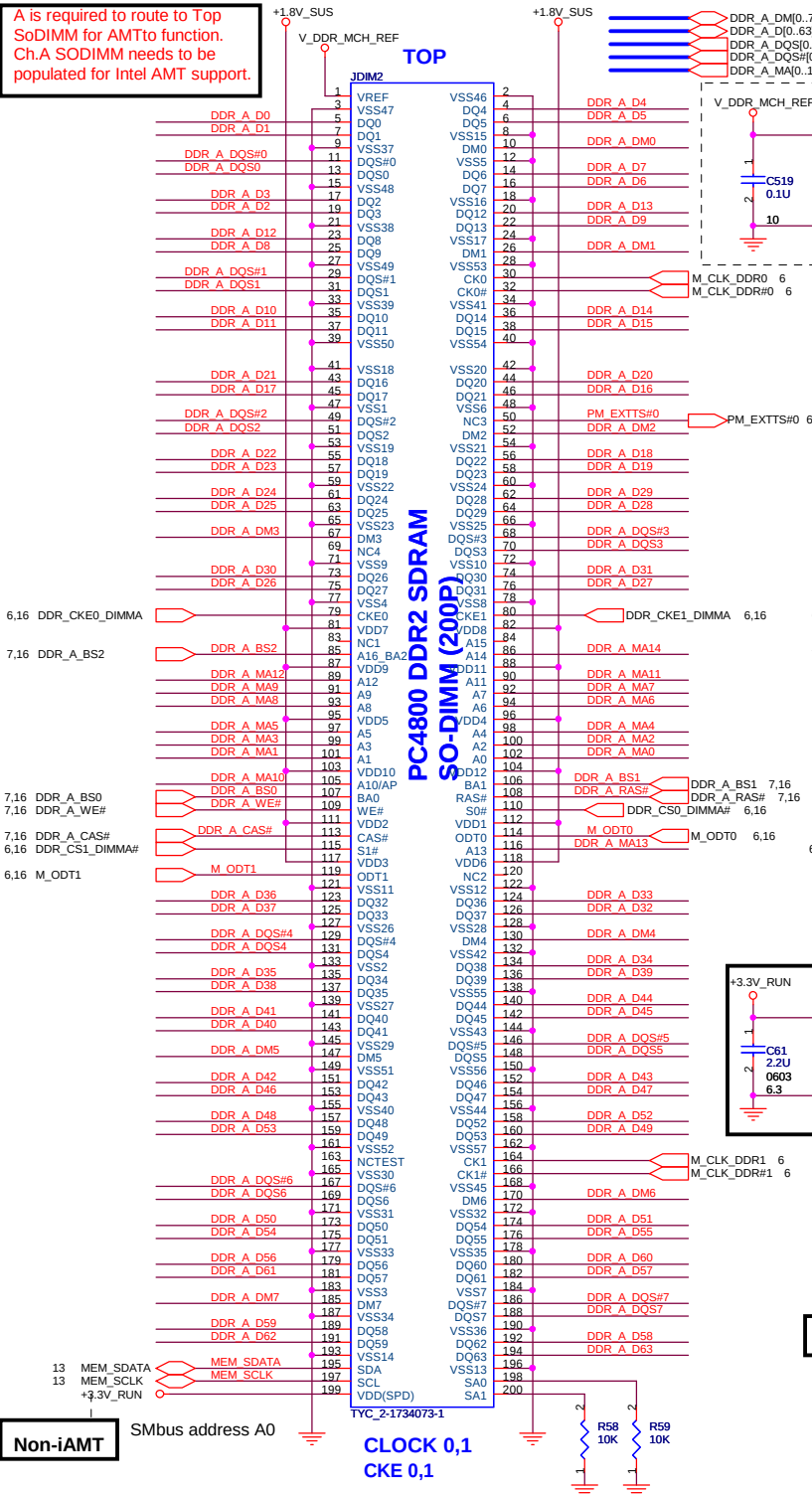
No Reboot strap.

SPKR Low = Default. High = No Reboot.

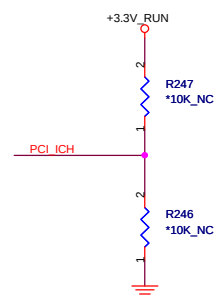
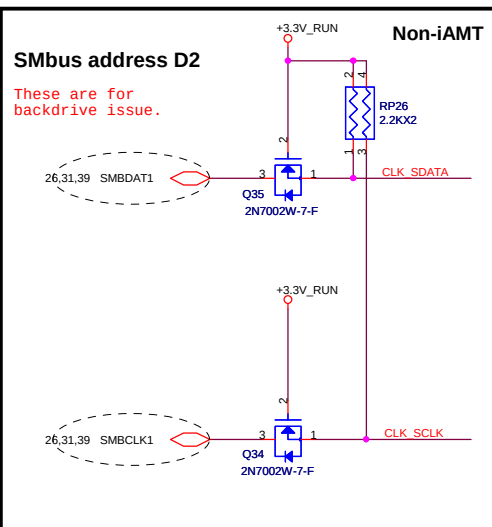
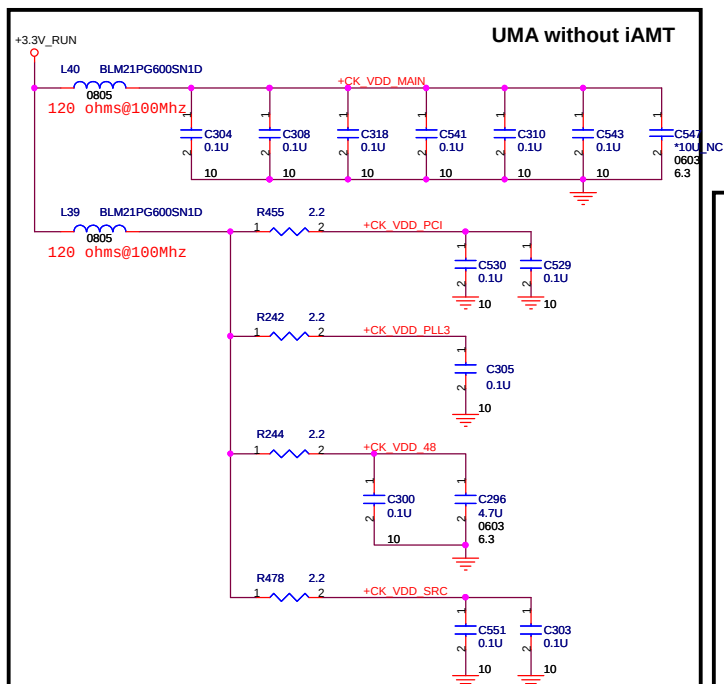
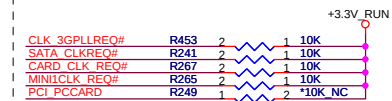
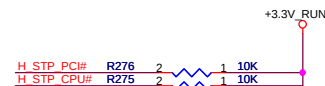
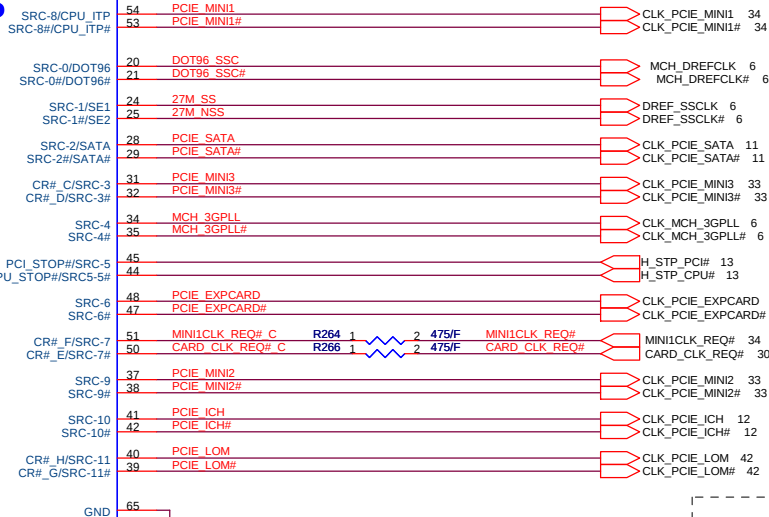
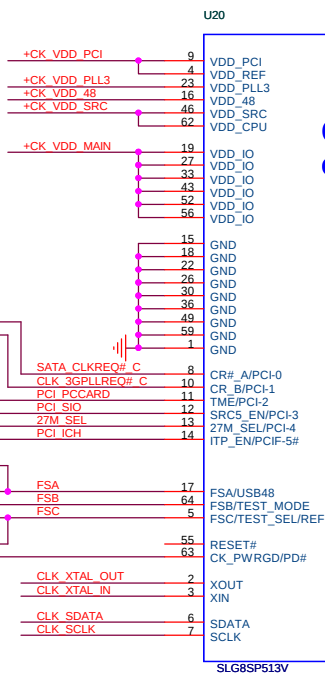
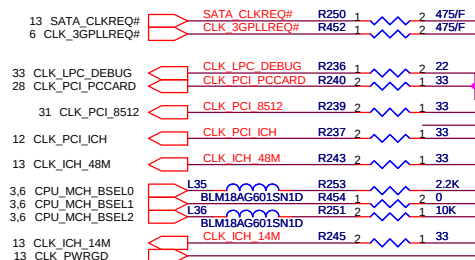
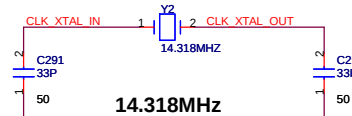




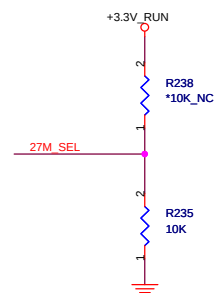
A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.



C299		20P	50	CLK	ICH	48M
C292	1	2	*27P_NC	50	CLK	ICH 14M
C289	1	2	*27P_NC	50	CLK	PCI 8512
C290	1	2	*27P_NC	50	CLK	PCI_PCCARD
C288	1	2	*27P_NC	50	CLK	PCI_ICH



R246 POP: For Internal pull-low.
R235 POP: For internal pull-high.



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL				
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout



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CLOCK GENERATOR

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NUMBER SAME AS DISCRETE**

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	A	B	C	D	E
4					
3					
2					
1					

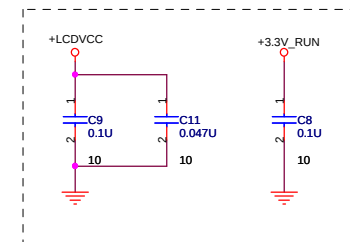
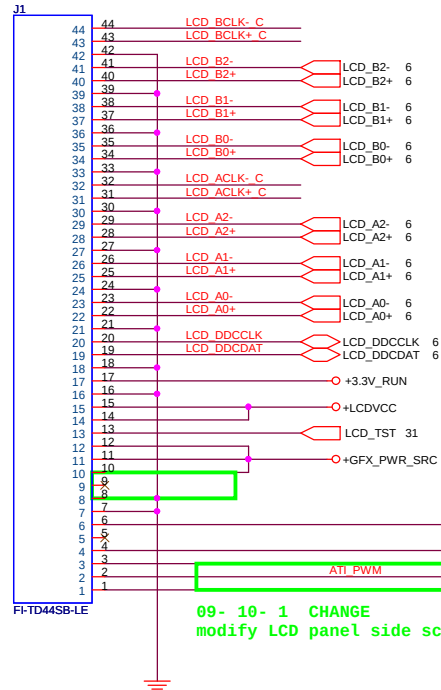
 QUANTA COMPUTER		
Title FLASH, RTC & KC		
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	1	2	3	4	5
A					
B					
C					
D					

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Title Battery Selector		
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1	2	3	4	5	6	7	8
A							
B							
C							
D							

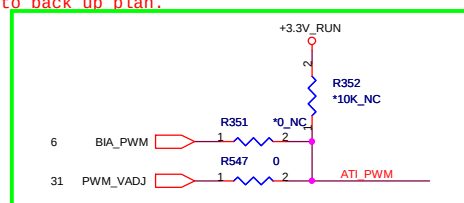
 QUANTA COMPUTER		
Title Docking Station CONN.		
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Adress : A9H --Contrast
AAH --Backlight



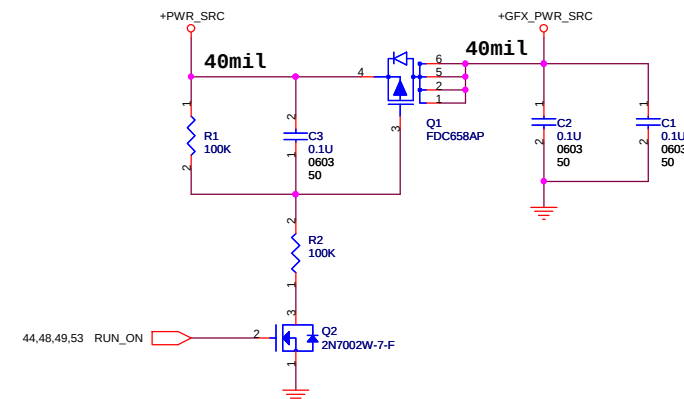
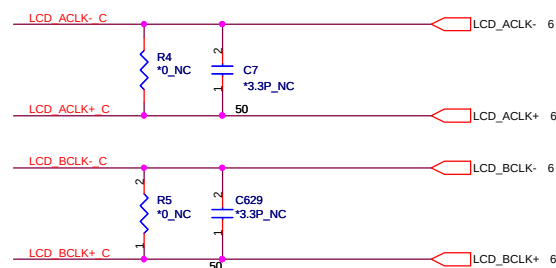
Populate R352 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.



```
09- 10- 1  CHANGE
modify LCD panel side schematic for DPST .
```

Shunt capacitors on LVDS for improving WWAN.

LCD B0-	C628	1	2	*3.3P	NC	50	LCD B0+
LCD B1-	C366	1	2	*3.3P	NC	50	LCD B1+
LCD B2-	C627	1	2	*3.3P	NC	50	LCD B2+
LCD A0-	C384	1	2	*3.3P	NC	50	LCD A0+
LCD A1-	C386	1	2	*3.3P	NC	50	LCD A1+
LCD A2-	C385	1	2	*3.3P	NC	50	LCD A2+



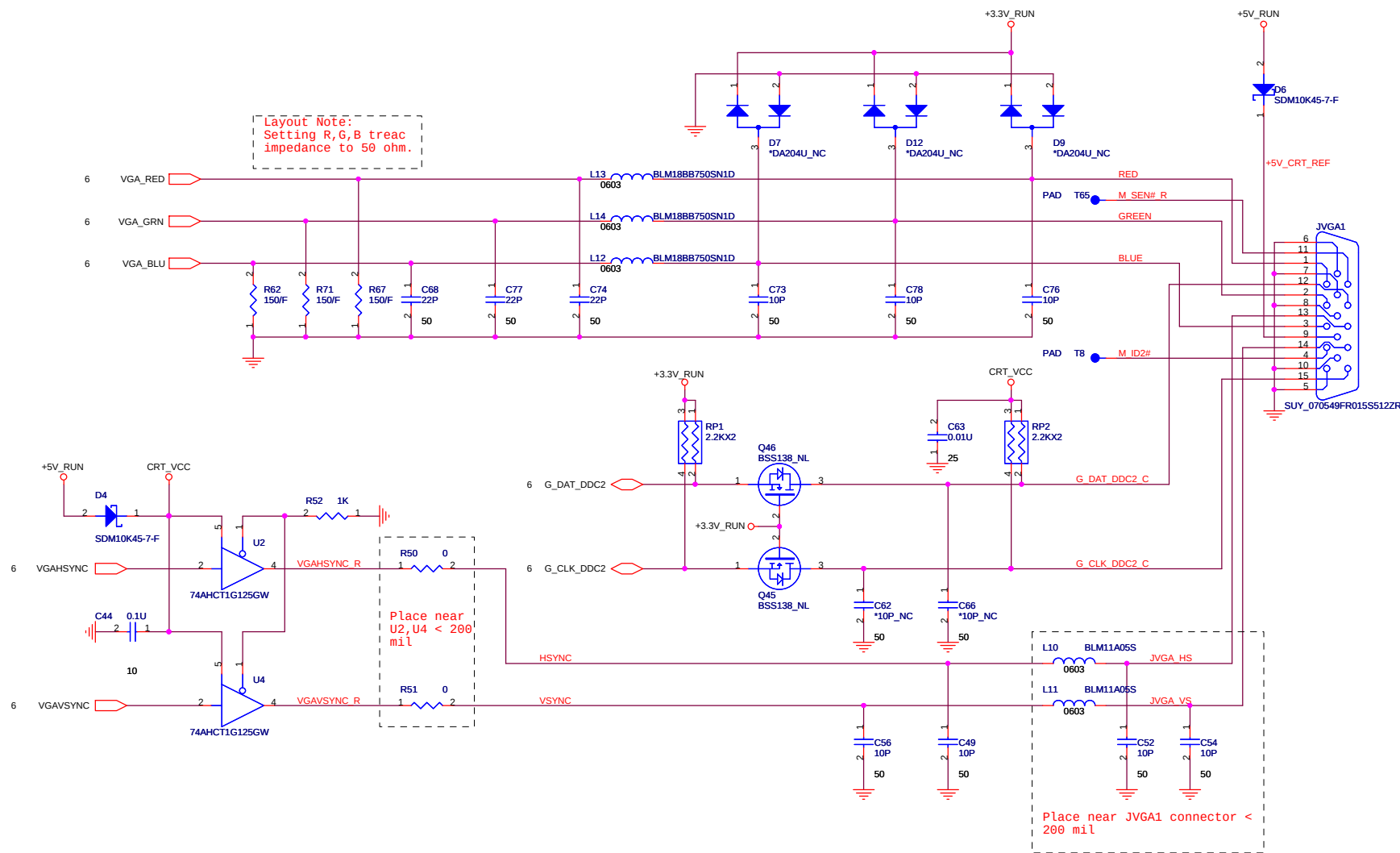
Title LCD CONN & CK-SSCD

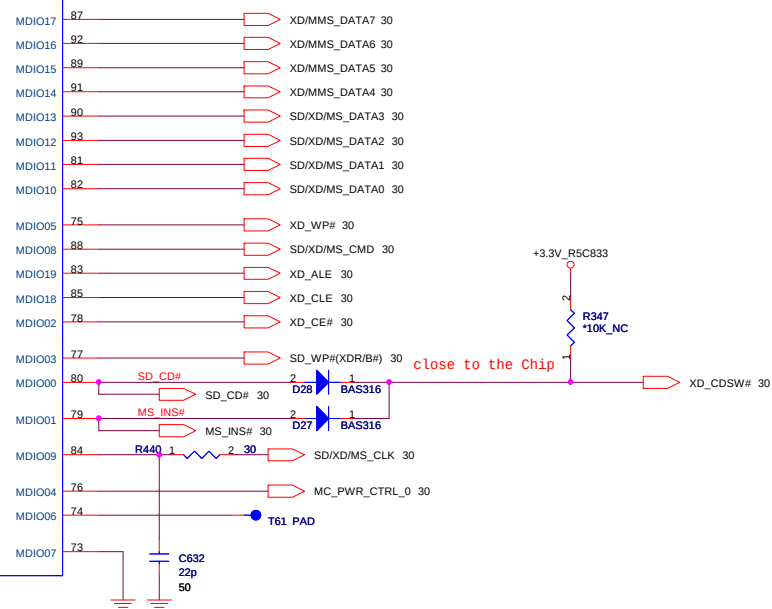
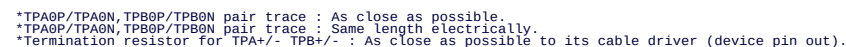
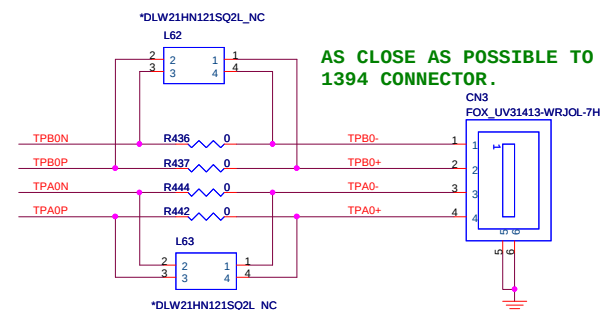
Size	Docun FM8B
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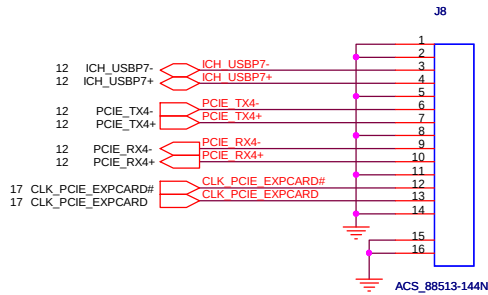
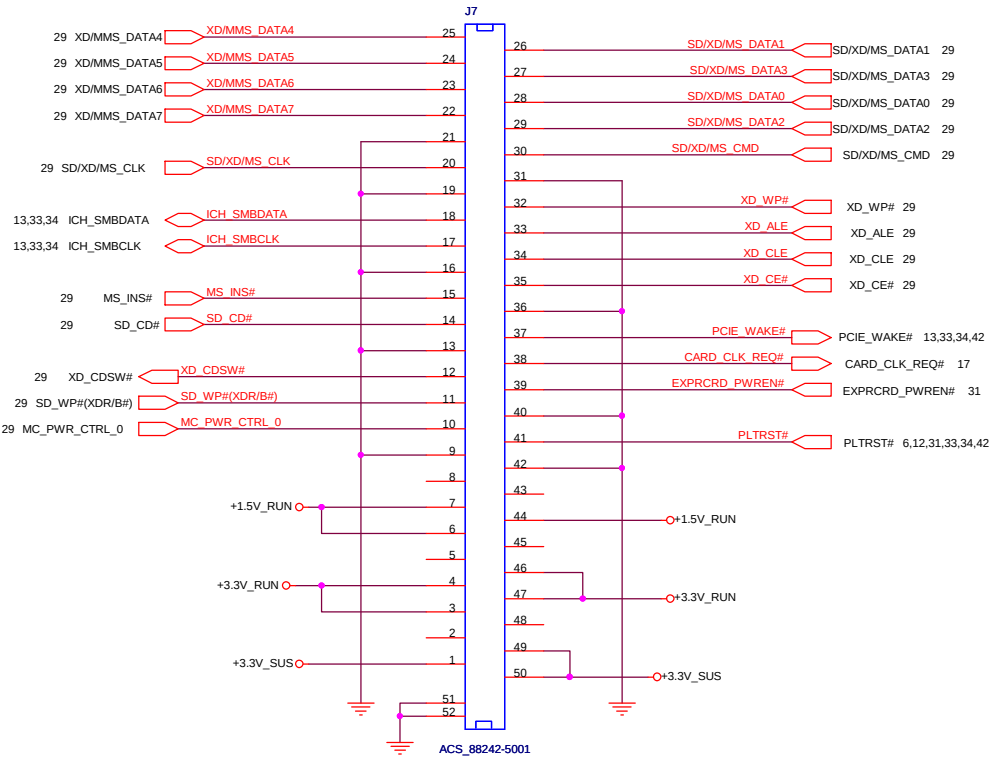
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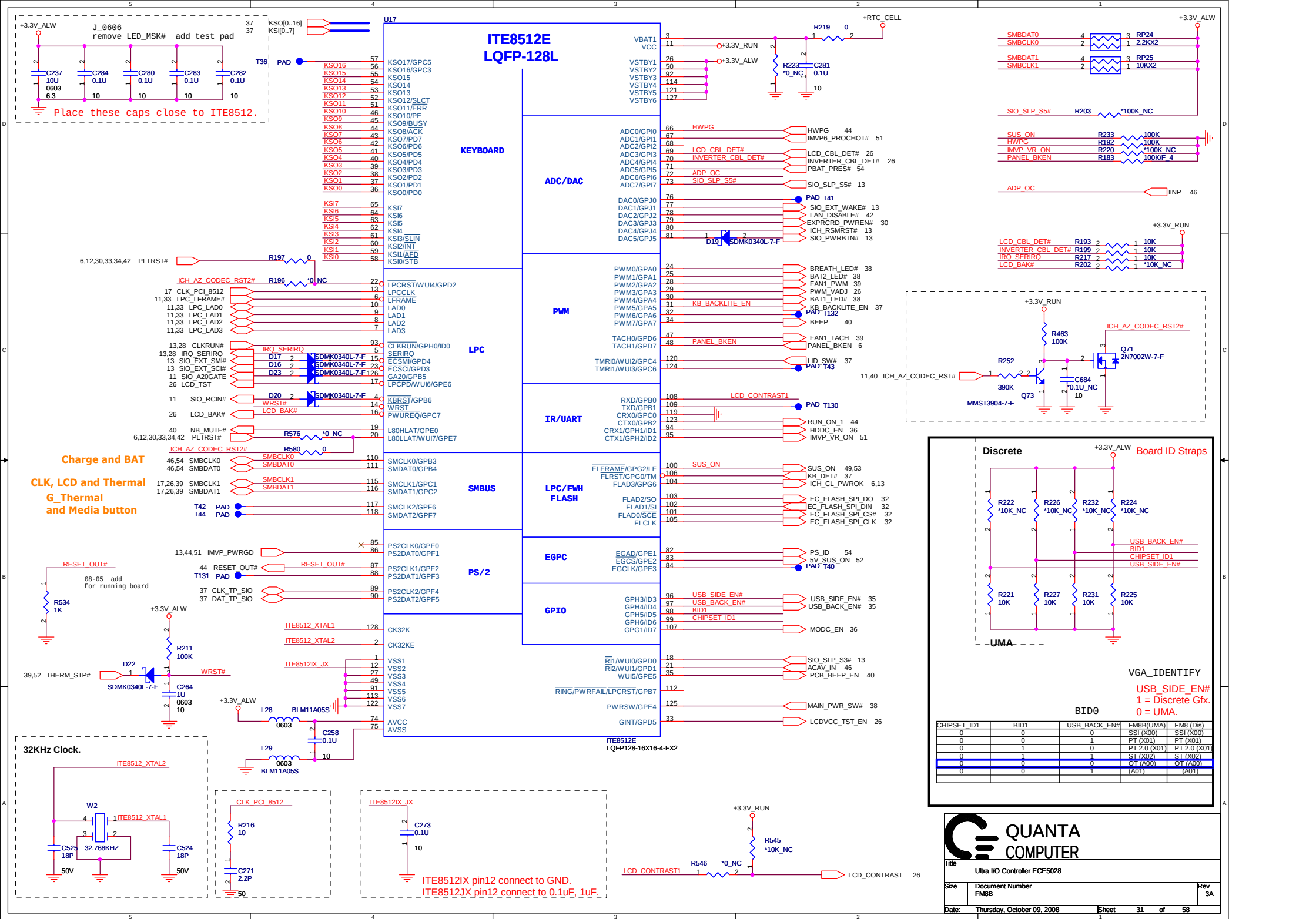
Express Card/CARD READER



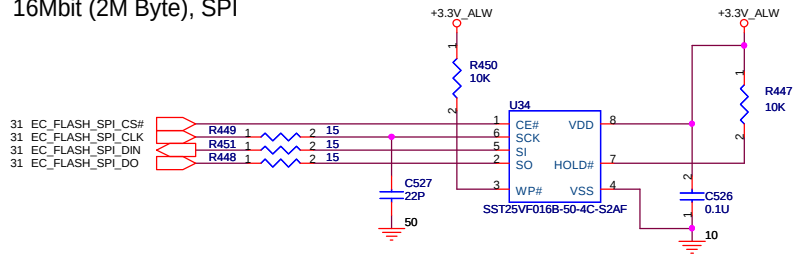


QUANTA
COMPUTER

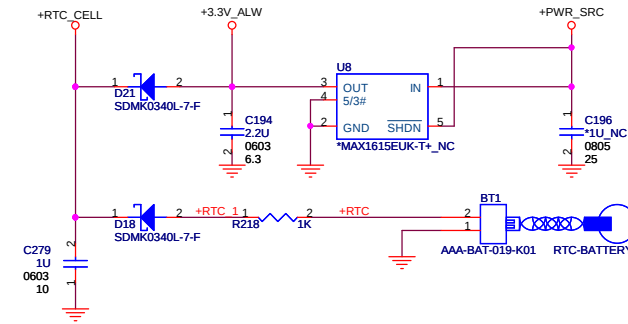
Title ExpressCard/SmartCard		
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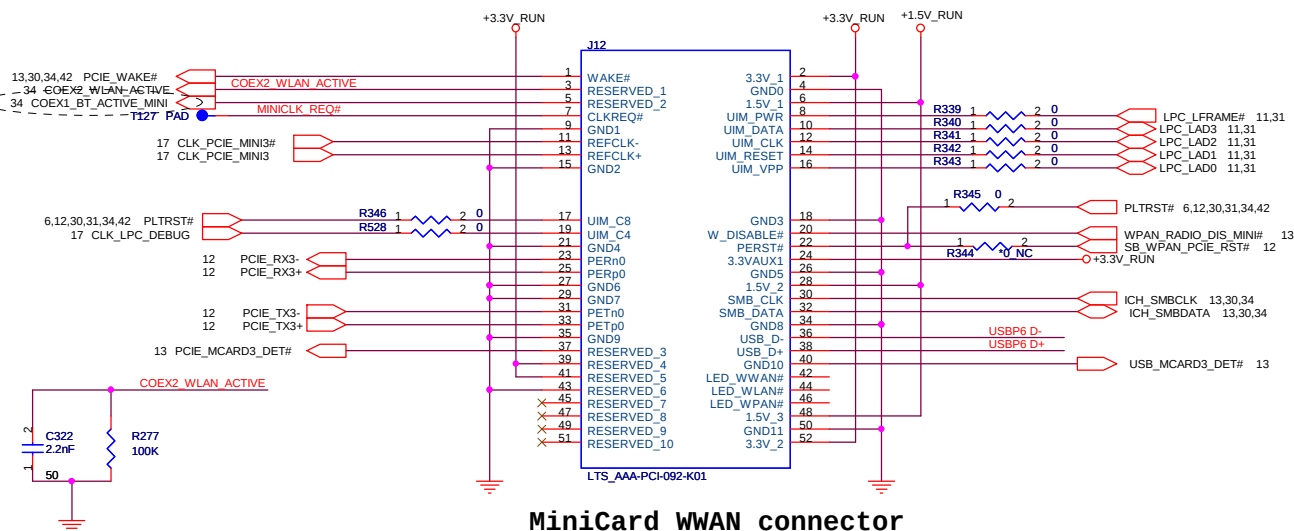
16Mbit (2M Byte), SPI



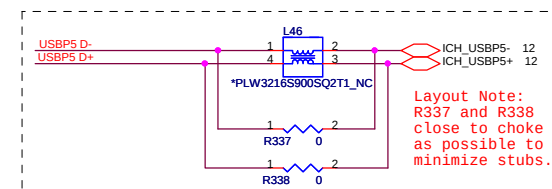
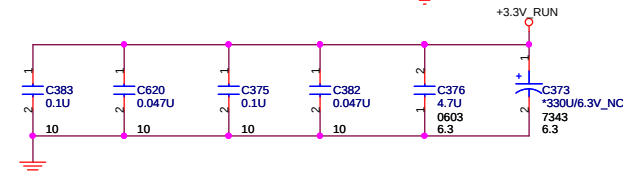
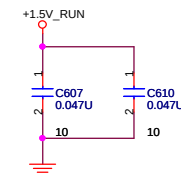
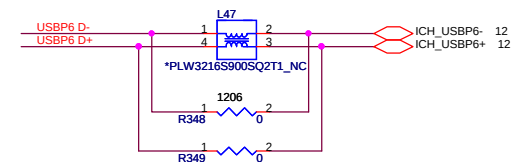
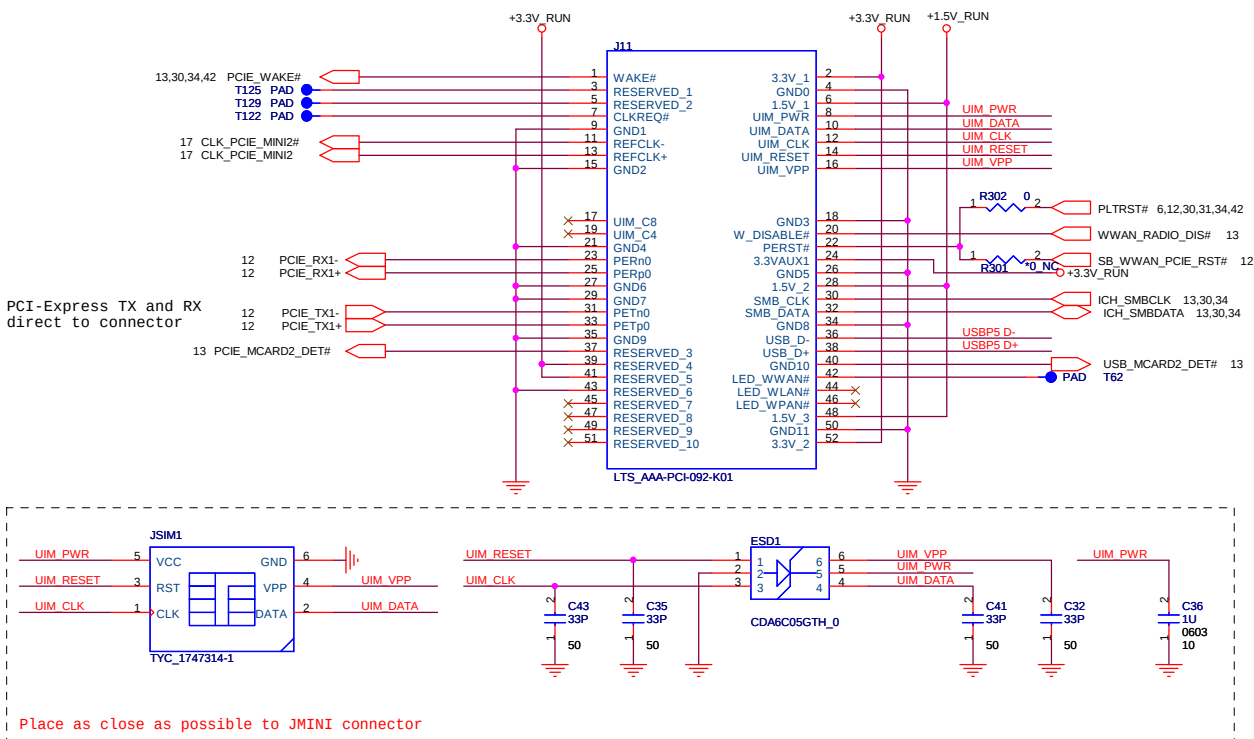
RTC BATTERY



MiniCard Robson, BT. UWB connector

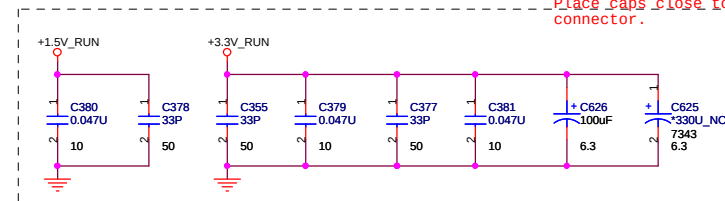


MiniCard WWAN connector



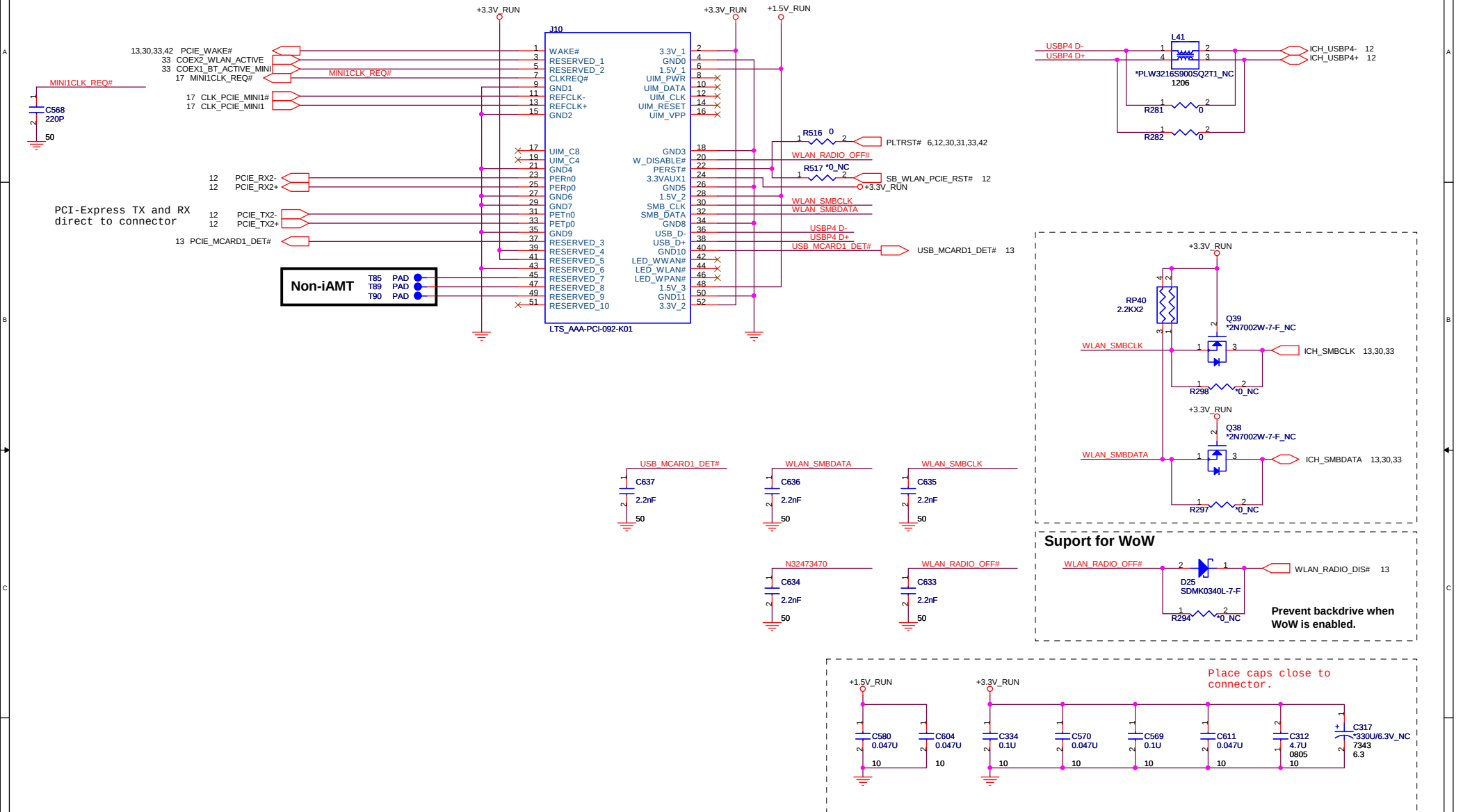
Layout Note:
R337 and R338
close to choke
as possible to
minimize stubs

Place caps close to
connector.



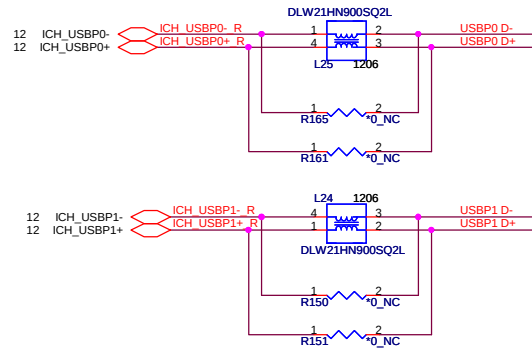
Title			
MINI-PCI			
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MiniCard WLAN connector



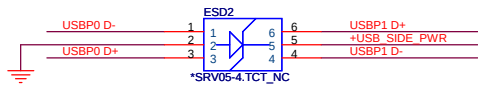
Title		
MDC CONN.		
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External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

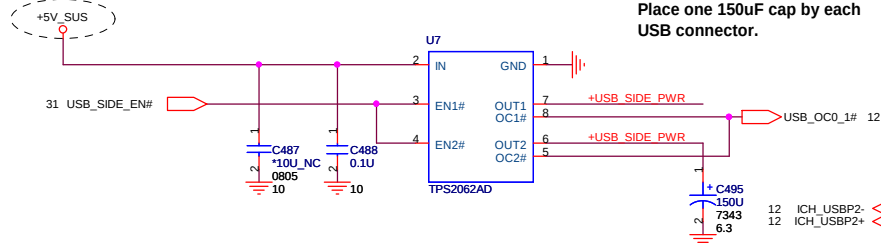


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

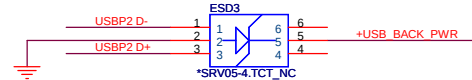
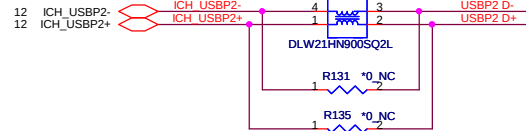
Place ESD diodes as close as USB connector.



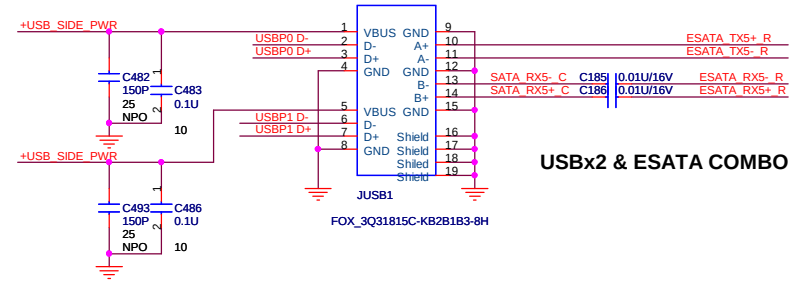
08 - 06 Del
remove fuse and Jump in the same time



Place one 150uF cap by each USB connector.

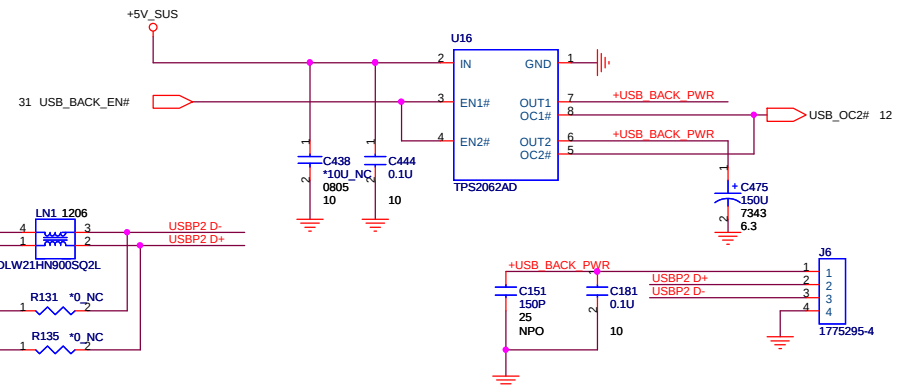
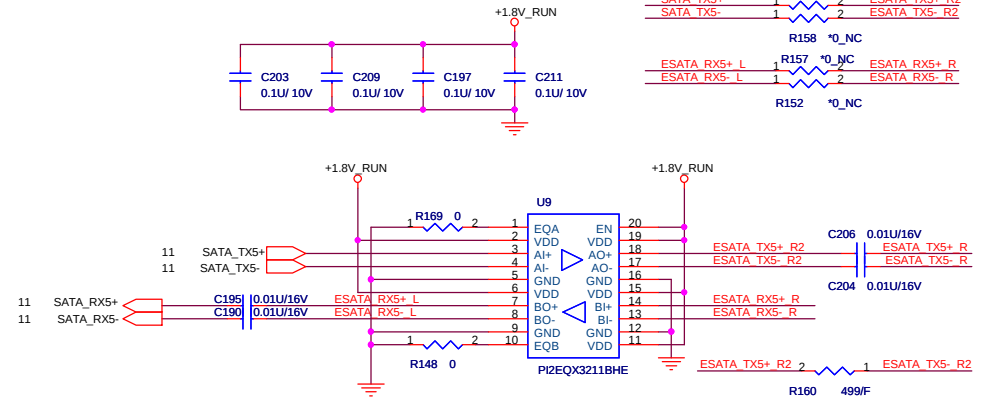


Side External USBX2



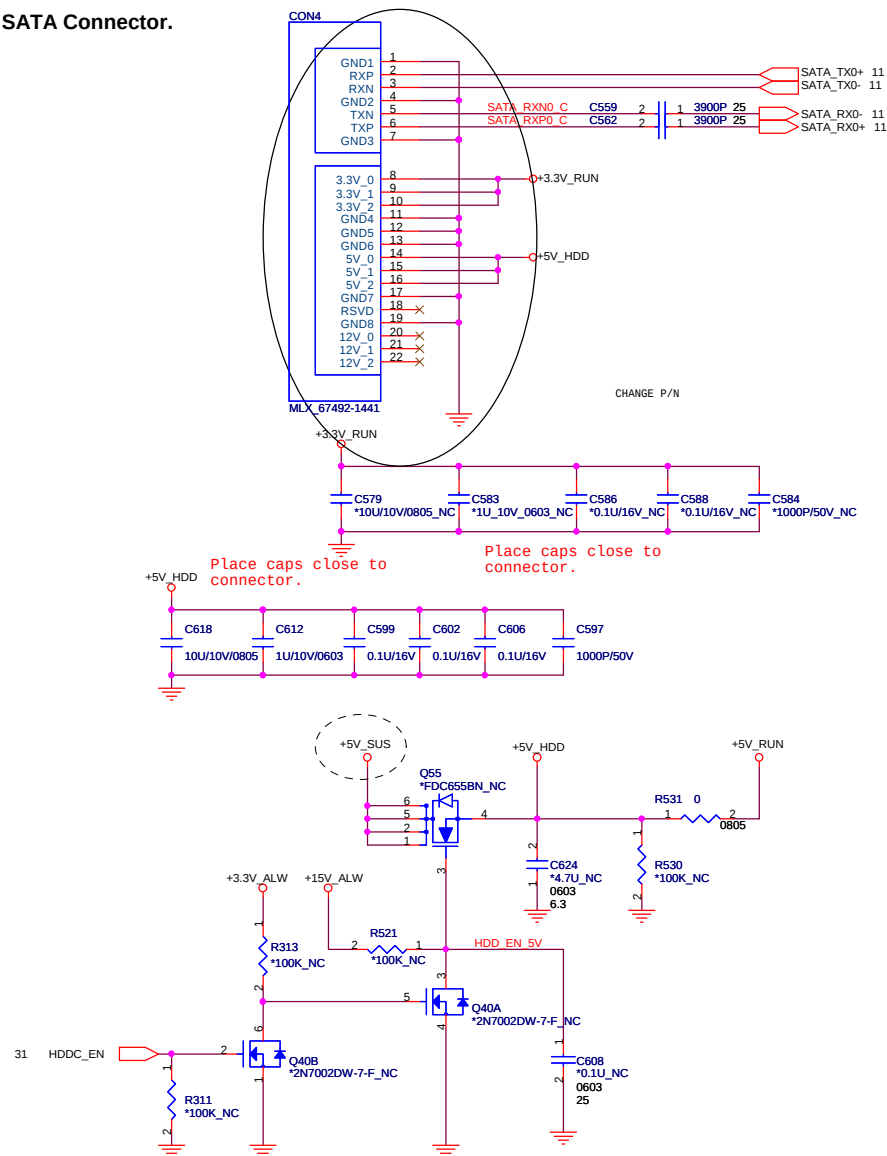
USBx2 & ESATA COMBO

E-SATA Re-driver

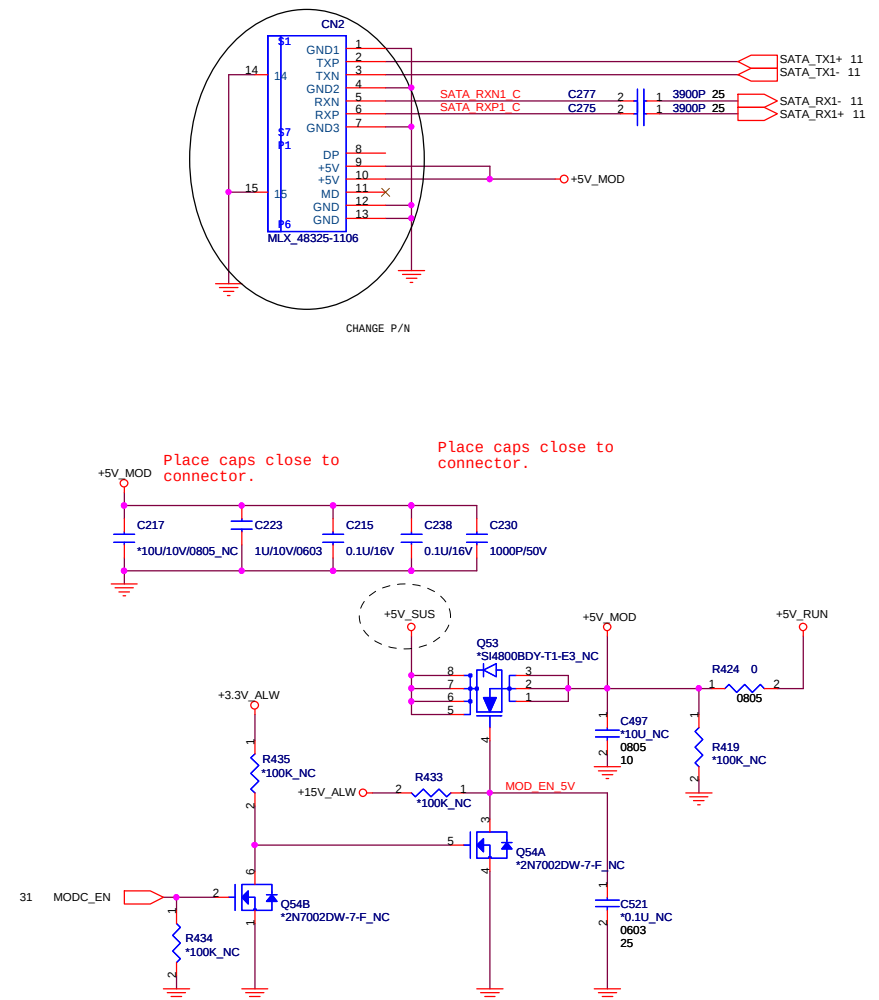


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SATA Connector.



ODD Connector



Title	SATA (HDD&CD_ROM)
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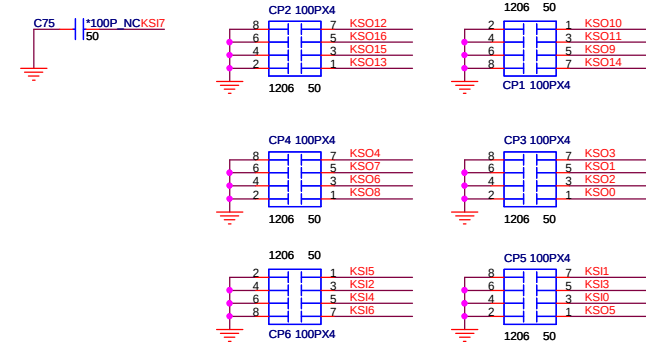
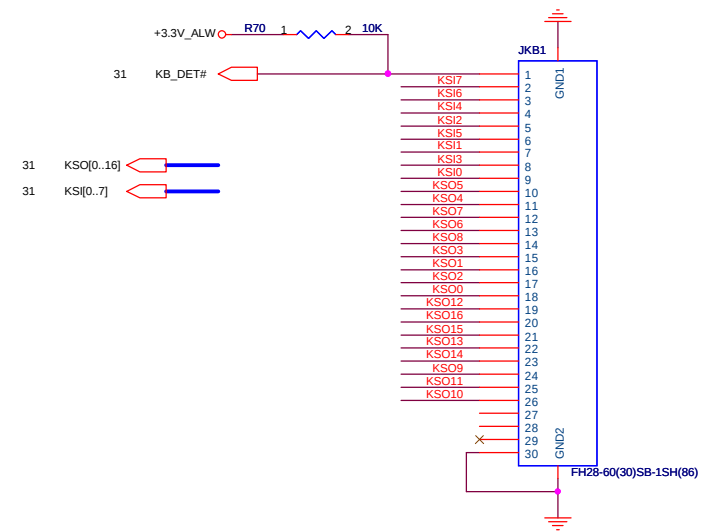
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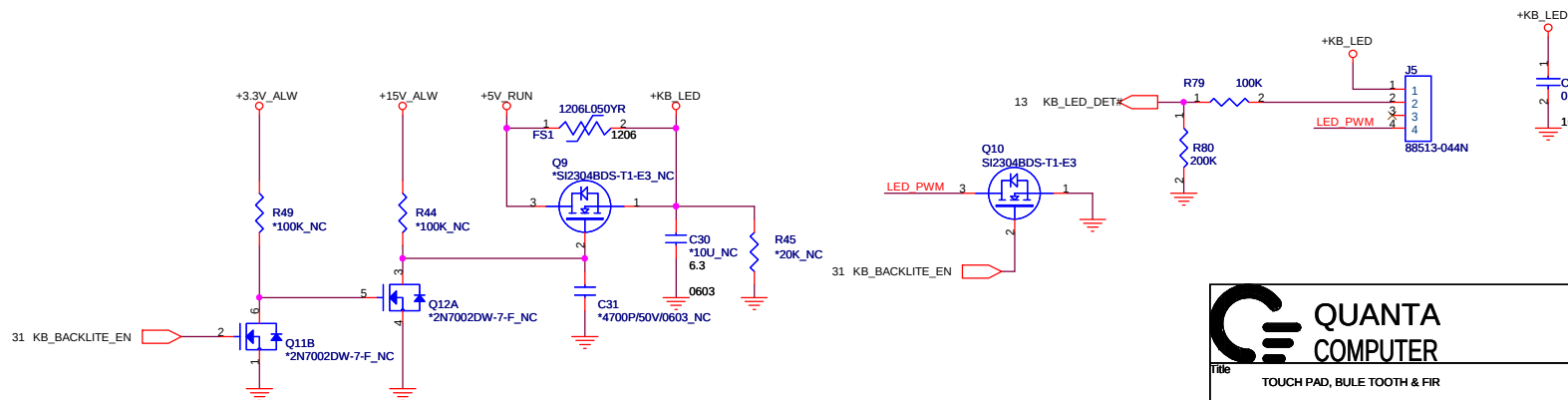
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KEYBOARD CONNECTOR



100P CAPS CLOSE TO JKB1

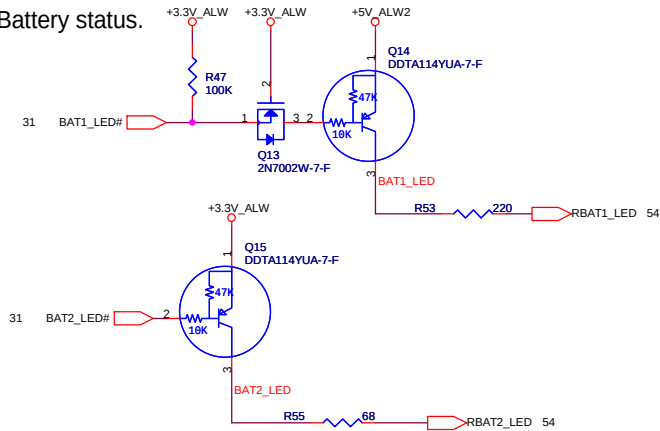
Key board Illumination



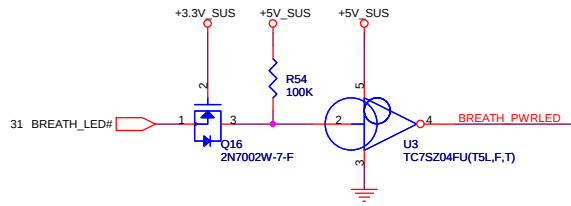
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Title		
TOUCH PAD, BULE TOOTH & FIR		
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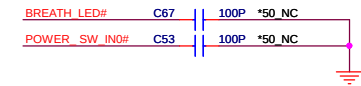
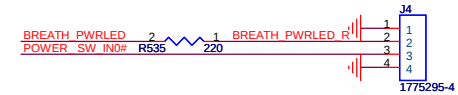
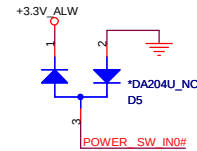
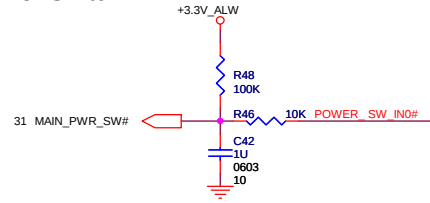
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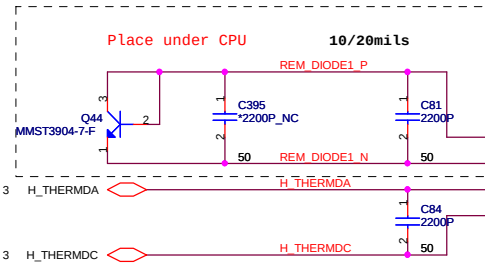
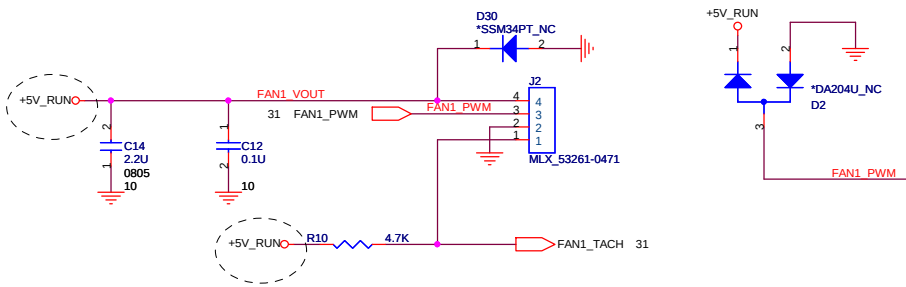


Power & Suspend.

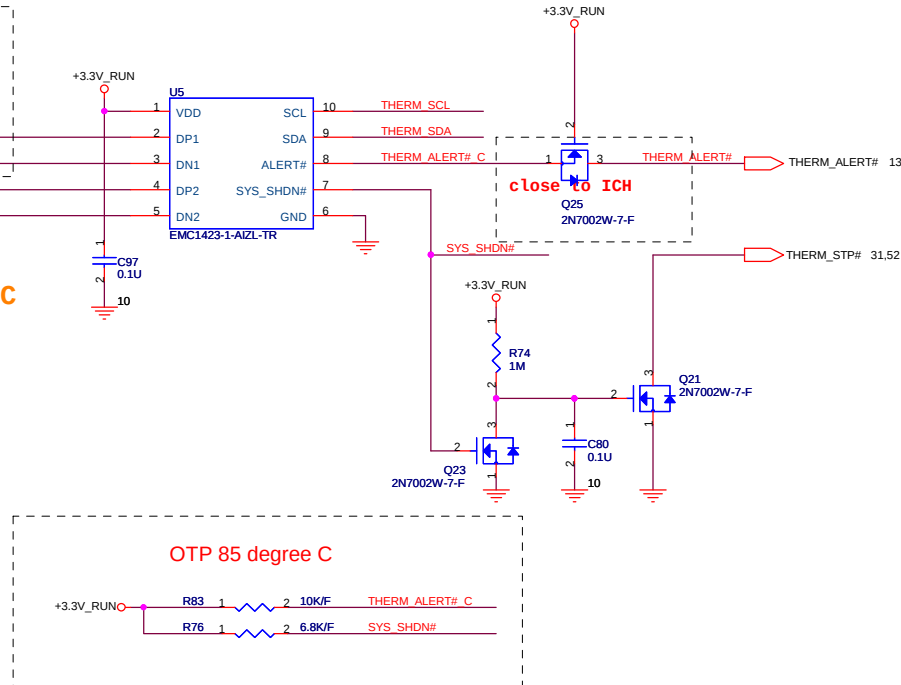
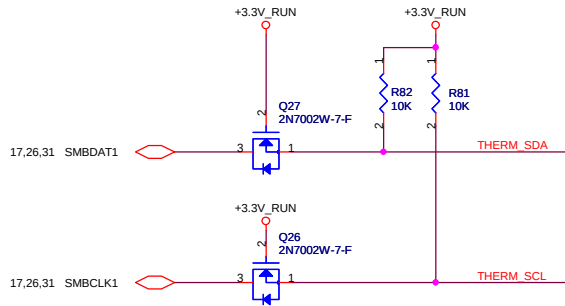


Power Switch

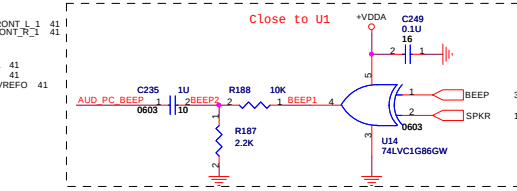
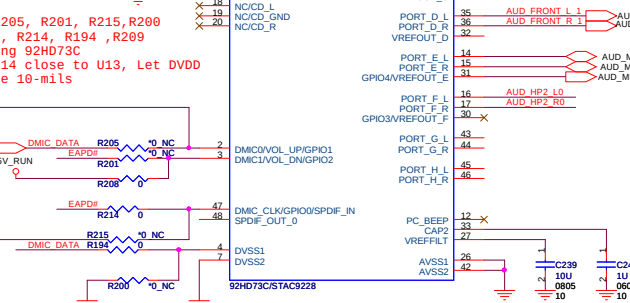
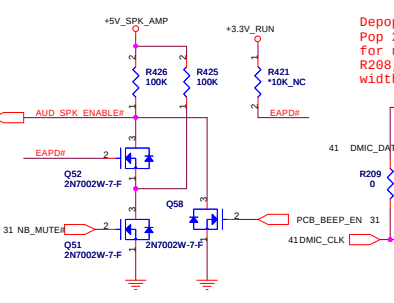
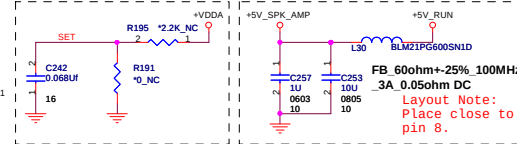
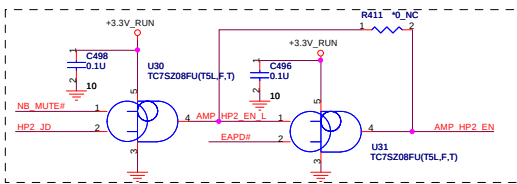
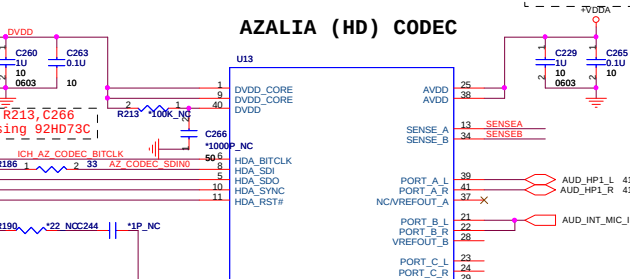
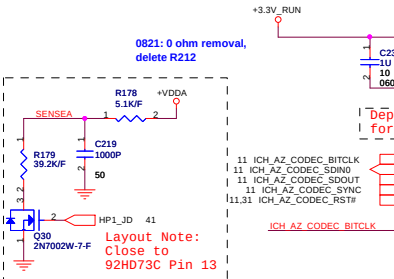
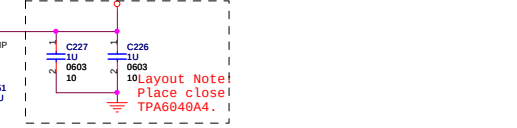
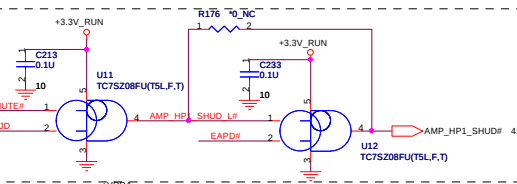
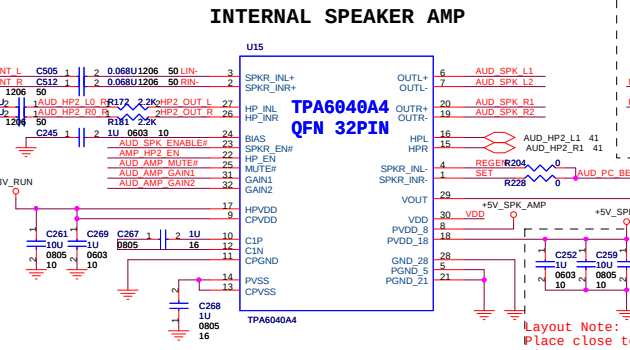
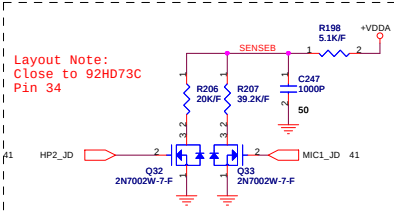
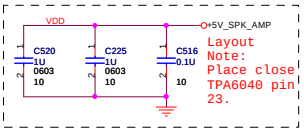
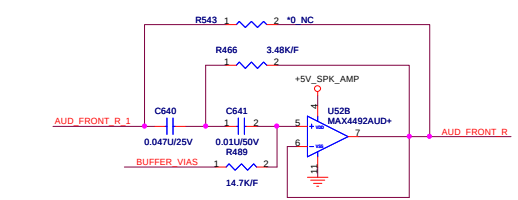
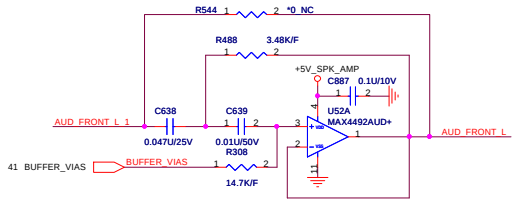
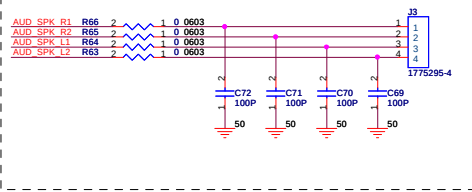
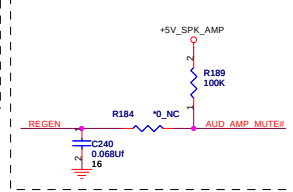
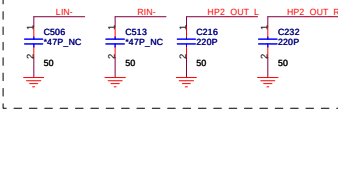
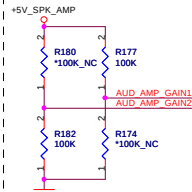




C458, C459 should close to thermal IC



GAIN1	GAIN2	6dB
0	0	10dB
1	0	15.6dB
1	1	21.6dB



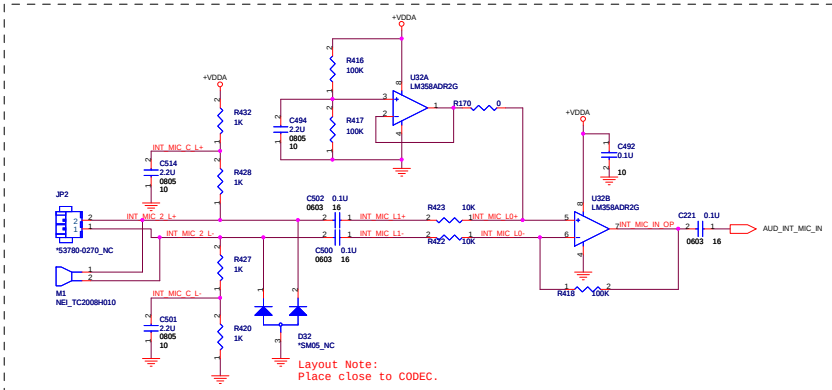
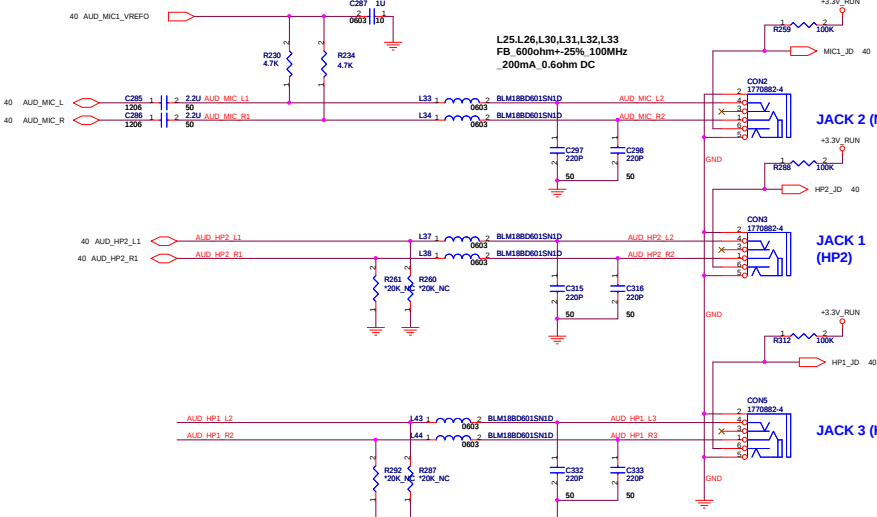
QUANTA COMPUTER

File: Azella CODEC

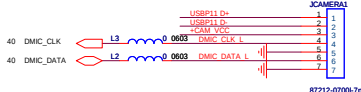
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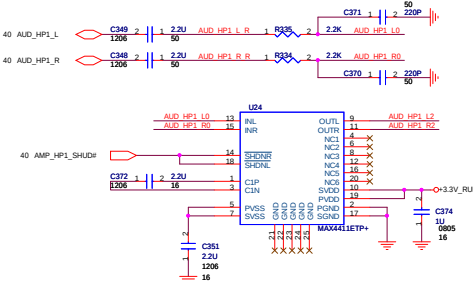
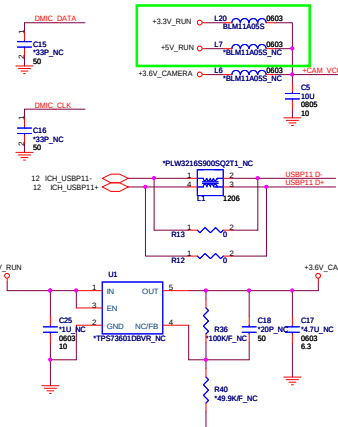
Headphone Jack
Stereo MIC Jack



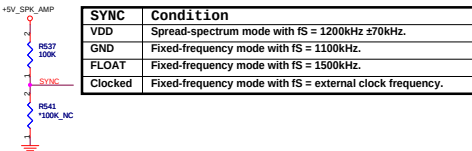
Layout Note:
Place close to CODEC.



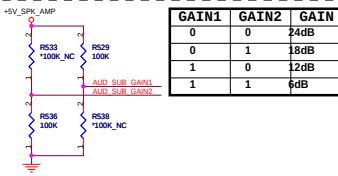
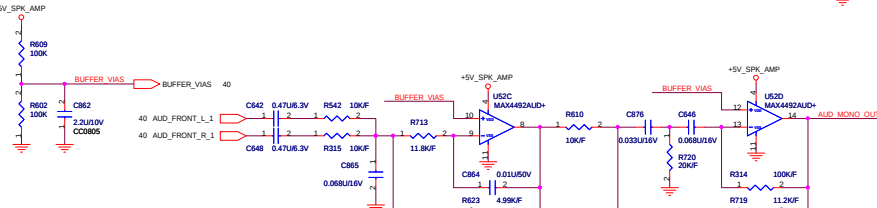
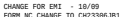
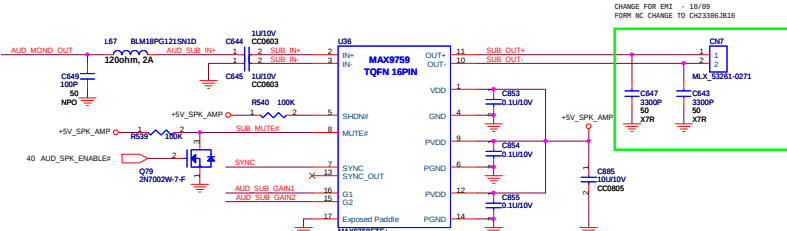
09 -10 - 34
use 3.3V for Camera power which can save one LDO and connector change from 6pin to 7pin



INTERNAL SUBWOOFER AMP



SYNC	Condition
VDD	Spread-spectrum mode with $f_S = 1200\text{kHz} \pm 70\text{kHz}$.
GND	Fixed-frequency mode with $f_S = 1100\text{kHz}$.
FLOAT	Fixed-frequency mode with $f_S = 1500\text{kHz}$.
Clocked	Fixed-frequency mode with $f_S =$ external clock frequency.



GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB



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AUDIO CONN

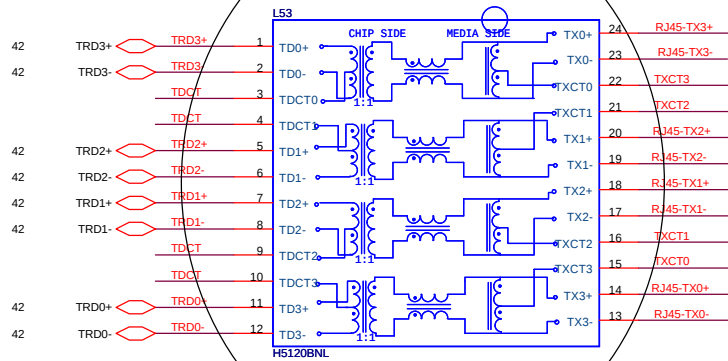
Case	Document Number
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Document Number
FM88

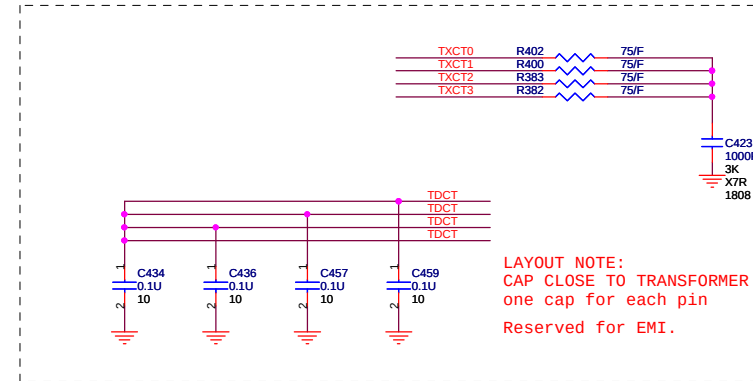
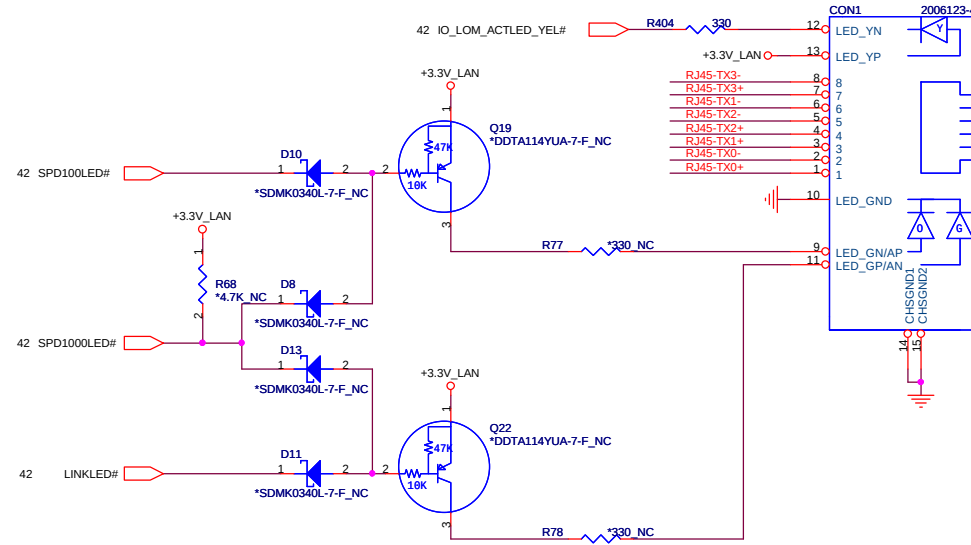
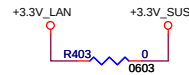
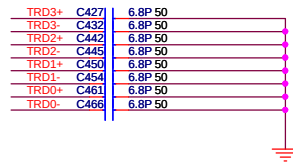
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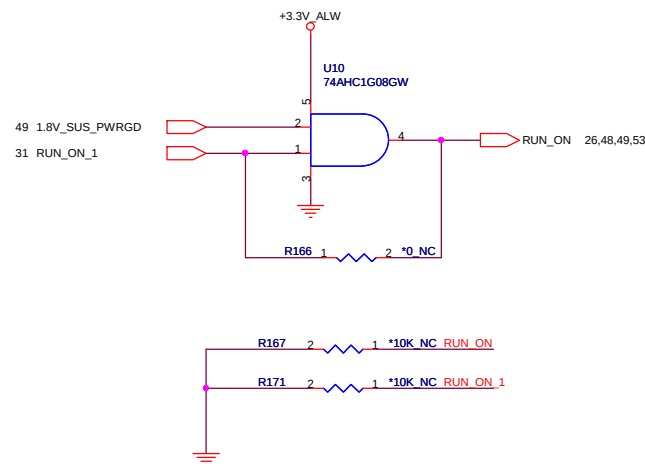
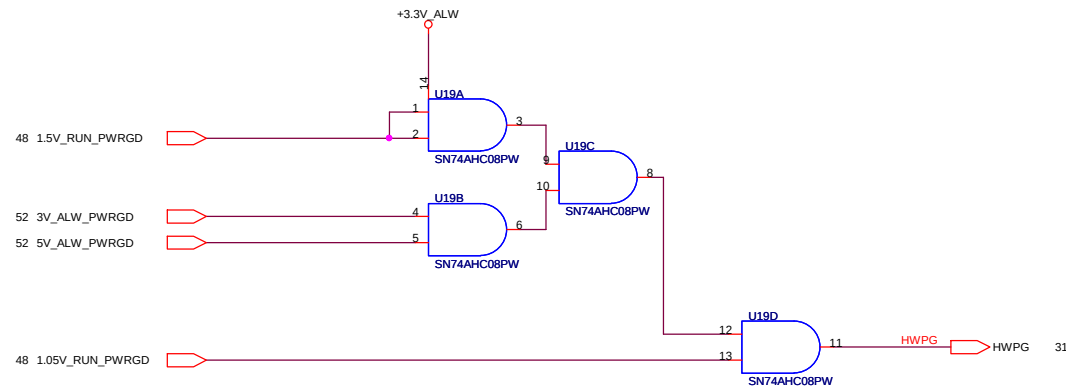
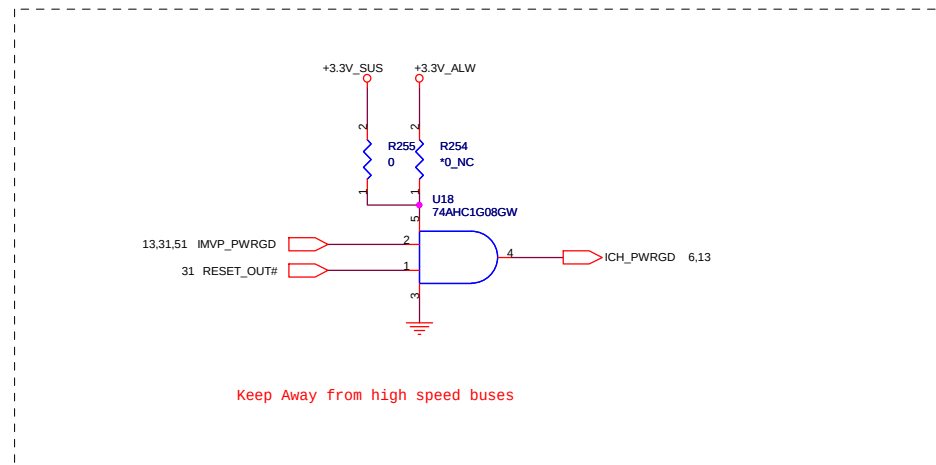
RJ-45 Connector

TRANSFORM



CHANGE FOR EA
FORM DTA CHANGE TO PLE H5120BNL





1	2	3	4	5	6	7	8
A							
B							
C							
D							

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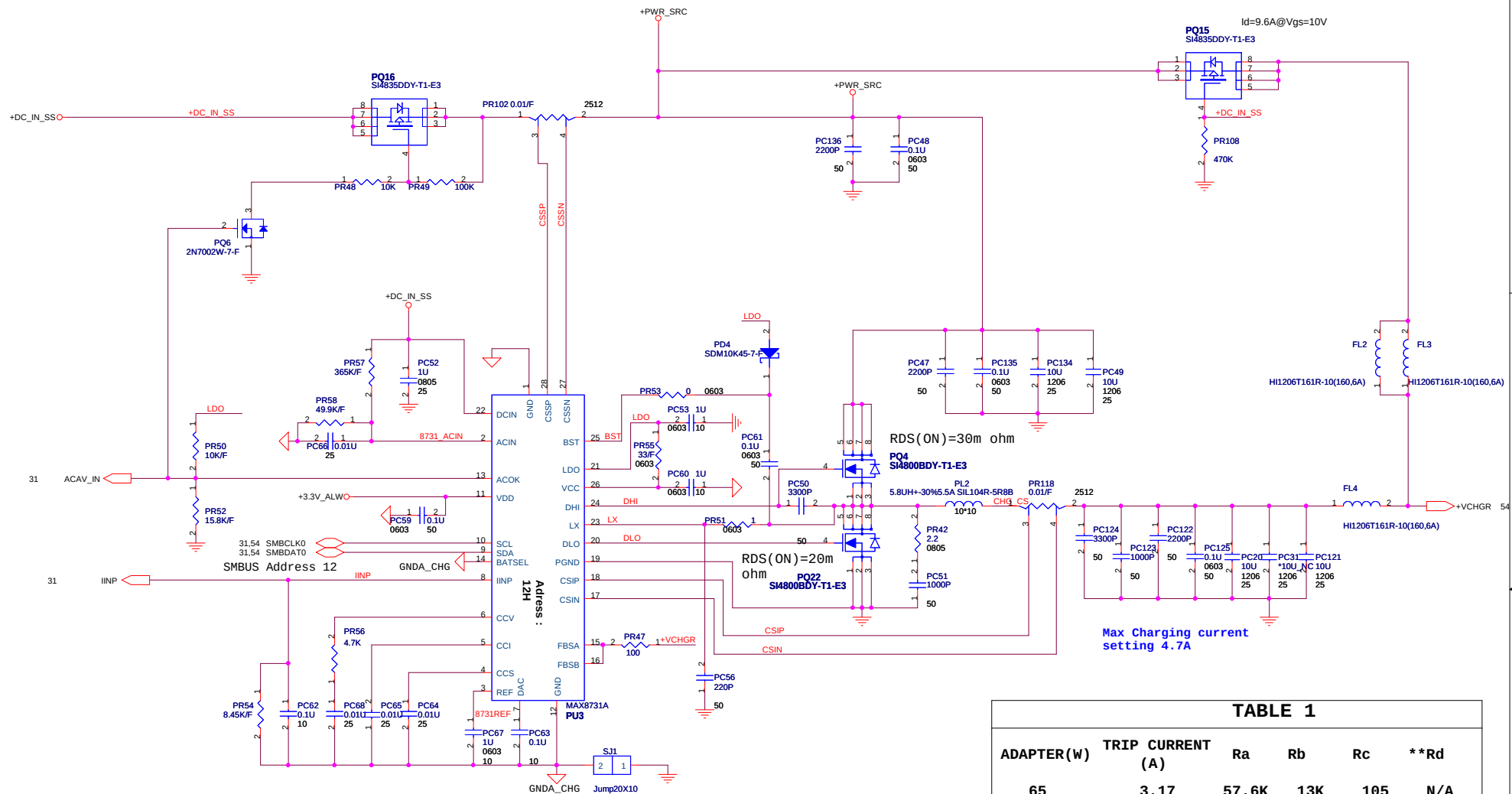


TABLE 1					
ADAPTER(W)	TRIP CURRENT (A)	Ra	Rb	Rc	**Rd
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	(see note3)	32.4K	6.49K	115	N/A

Note 1: PR96 is populated if ADAPT_TRIP_SEL is used to program for the next lower adaptor.

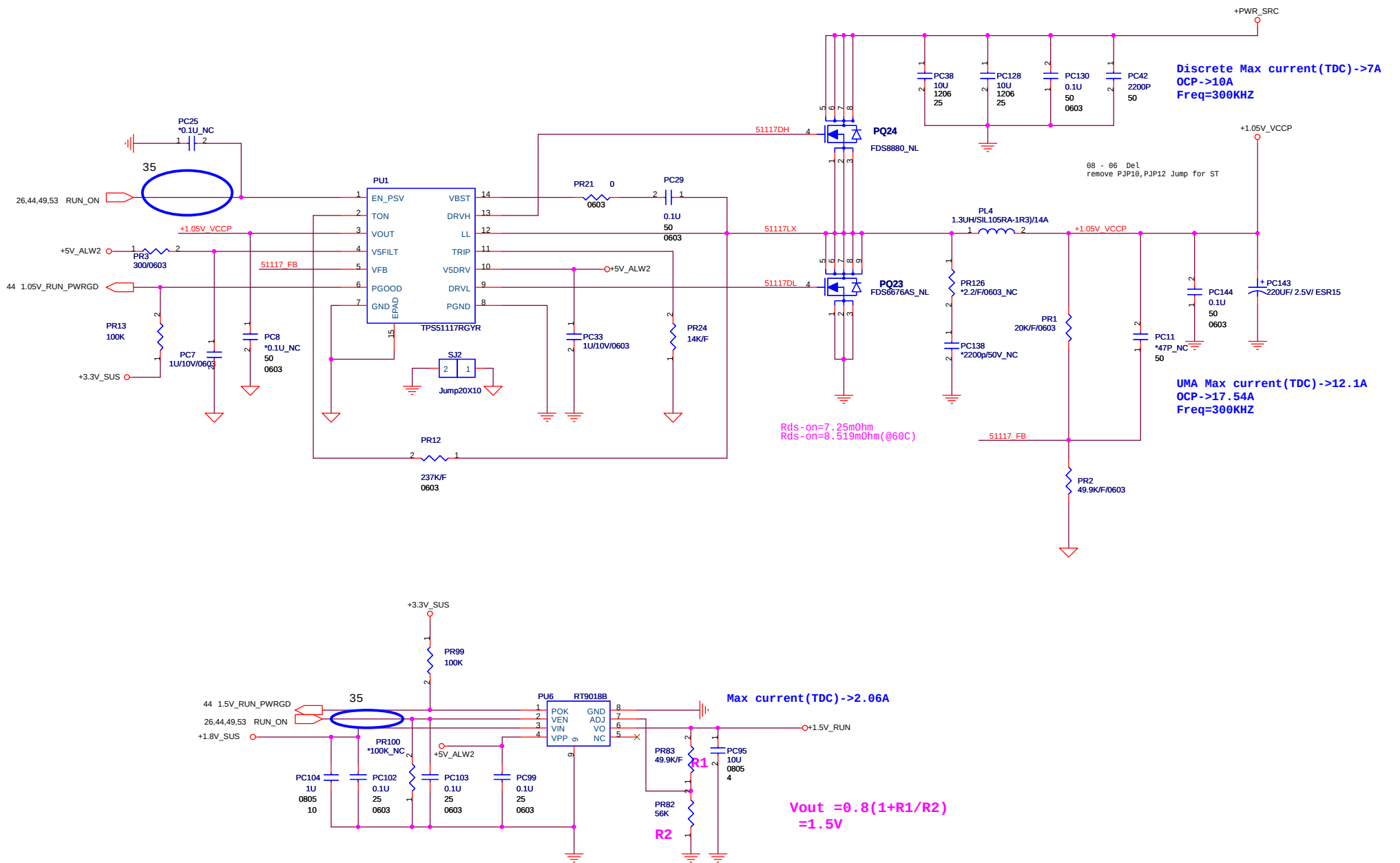
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

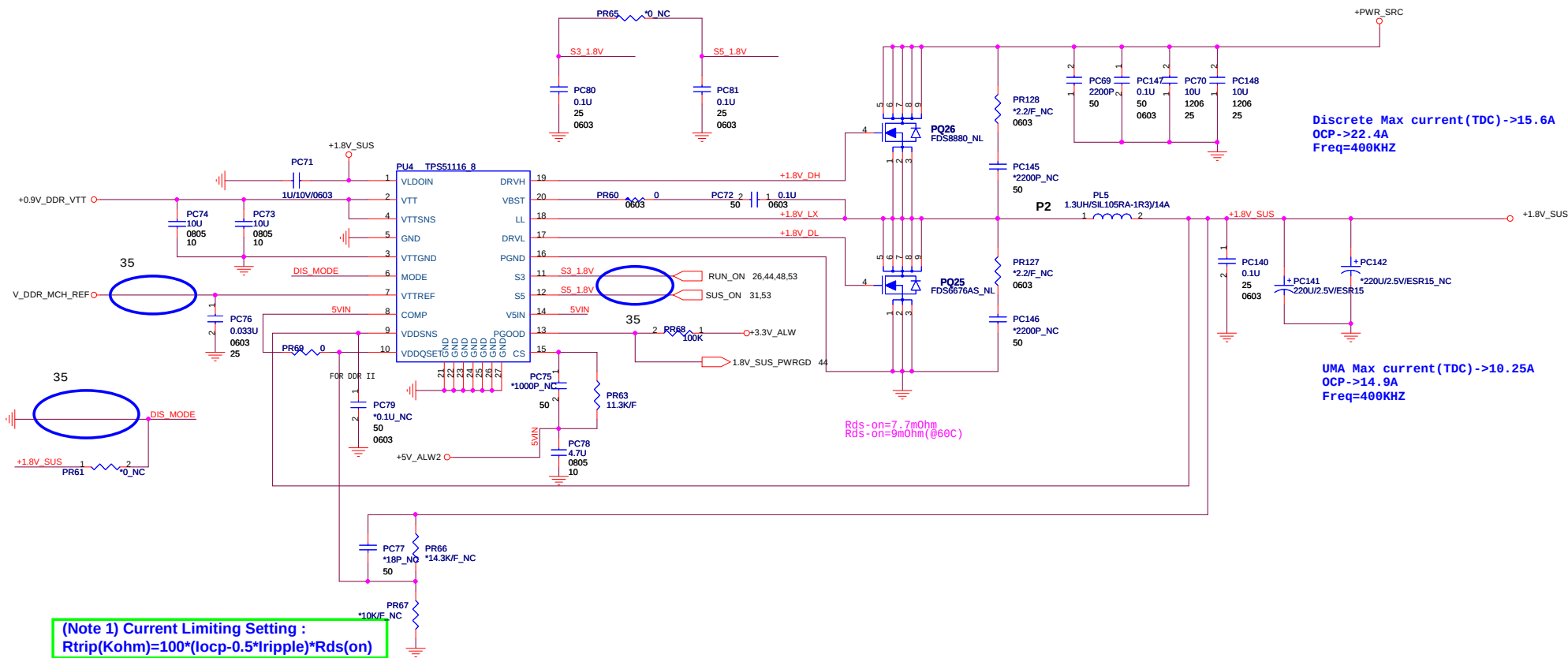
Note 2: 24.9K at PR96 allows the 65W adaptor setting to switch down to 45W.

Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.

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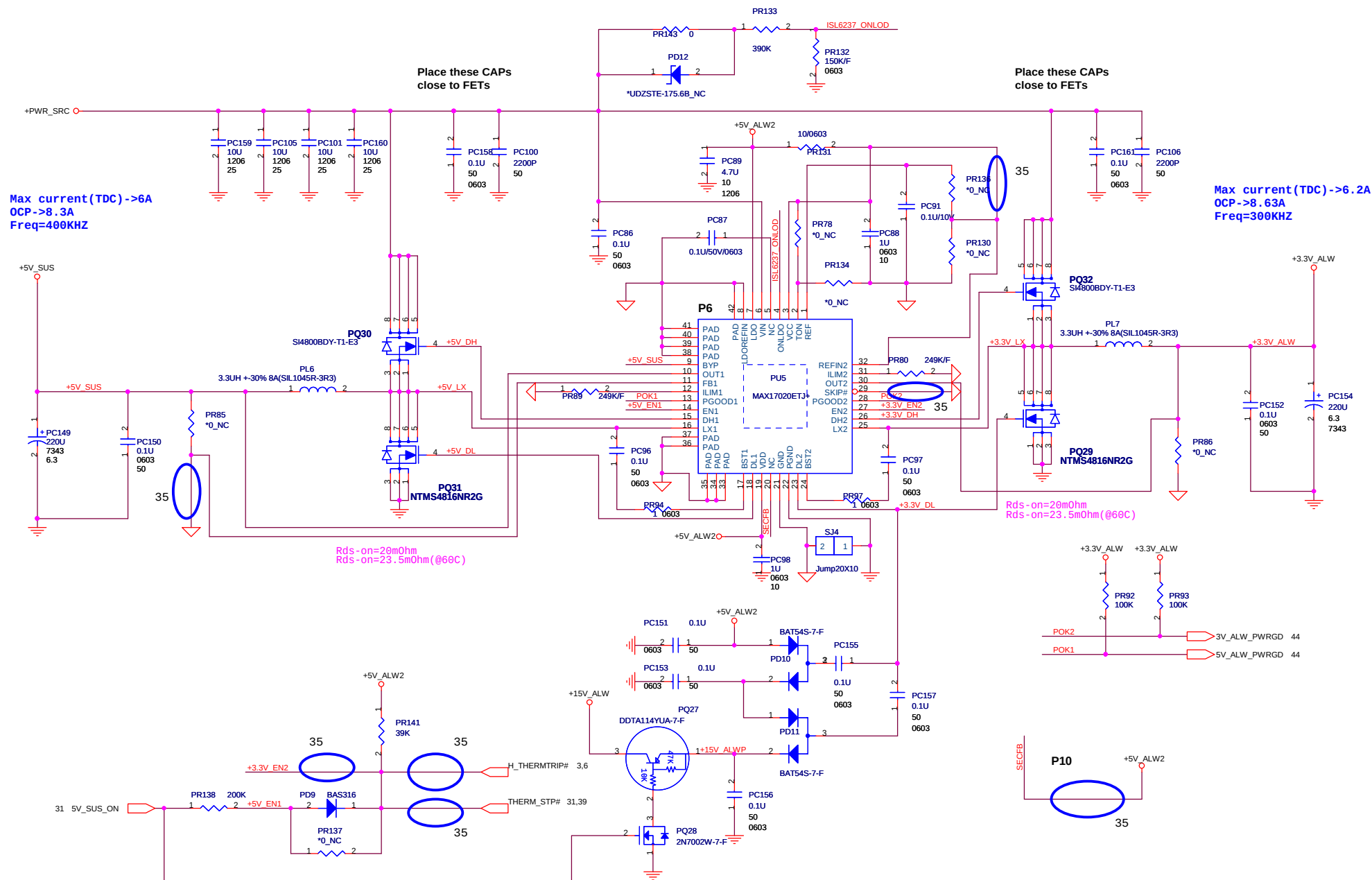




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DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW



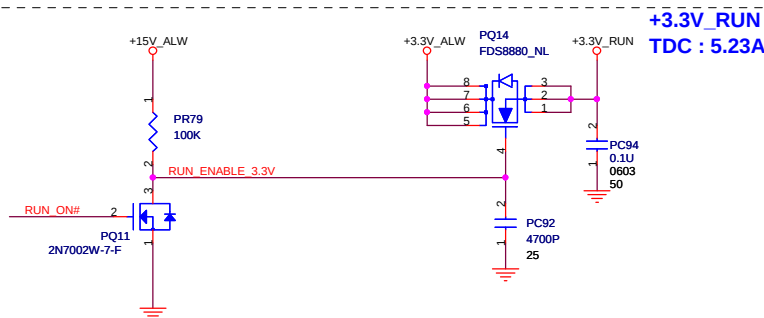
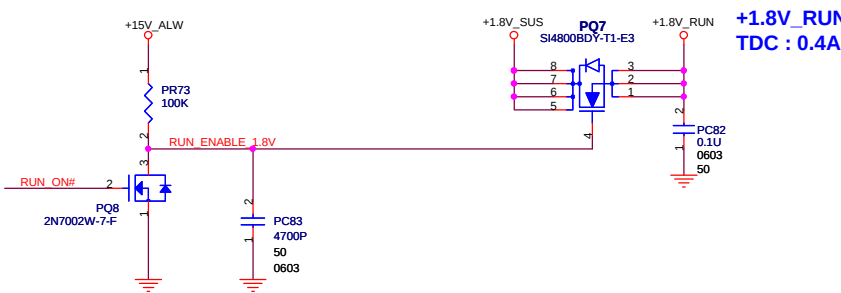
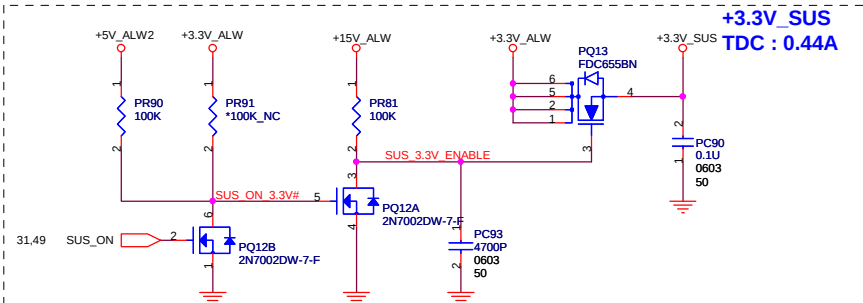
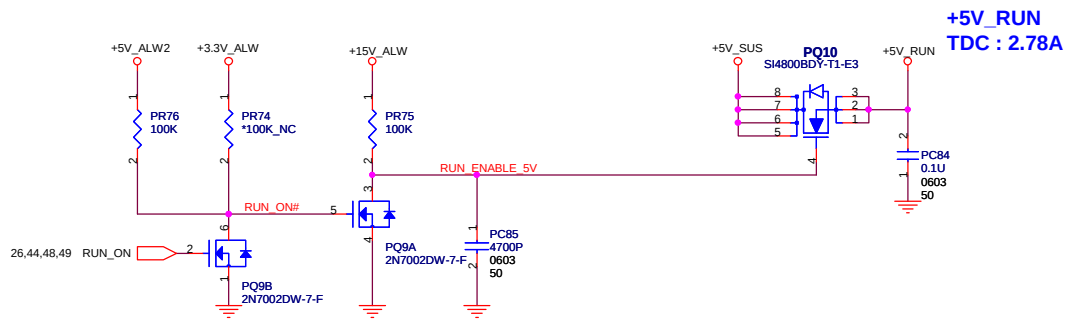
Title	3VALW,5V,3V, Power On
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Size	Docum FM8B
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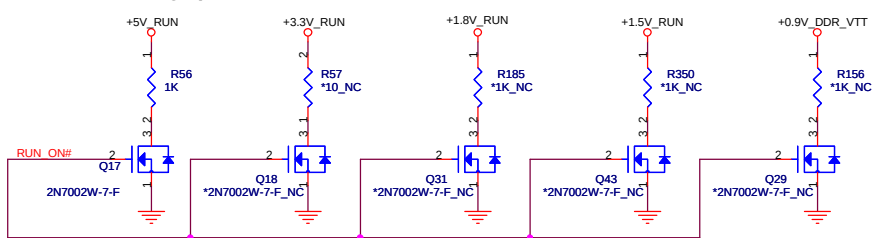
Date: Thursday, October 09, 2008

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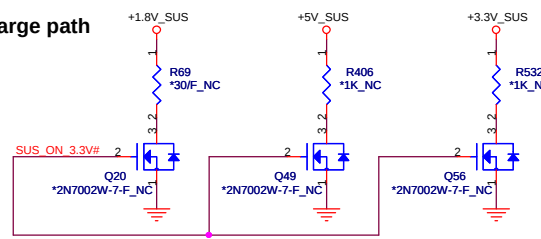
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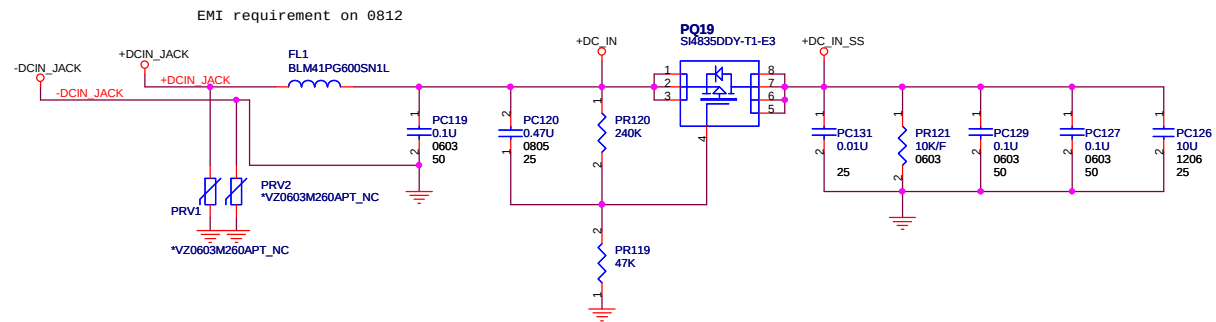
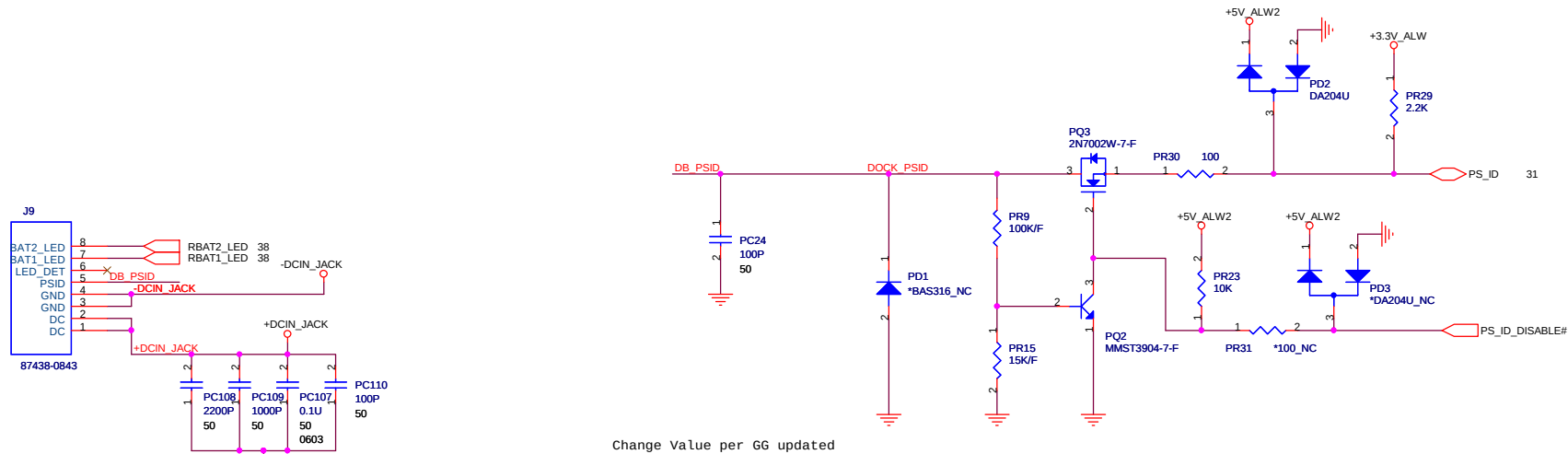
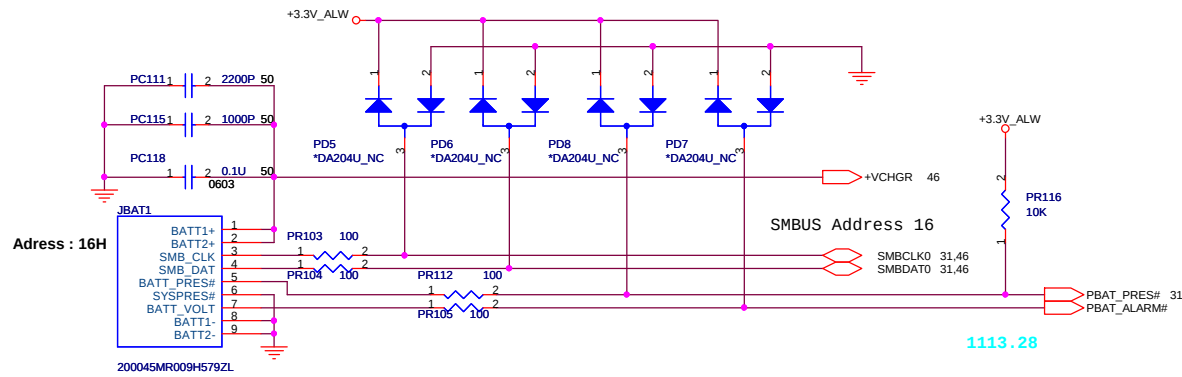


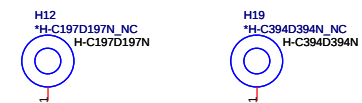
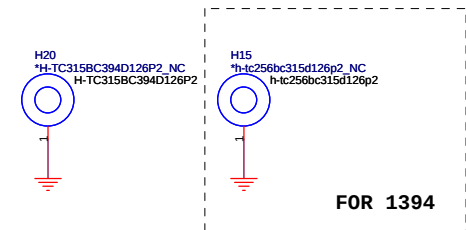
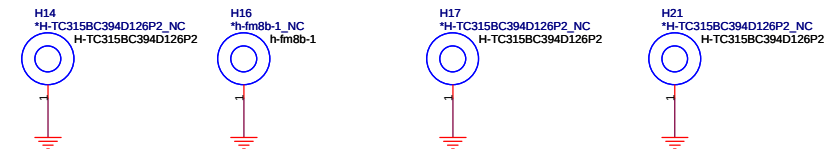
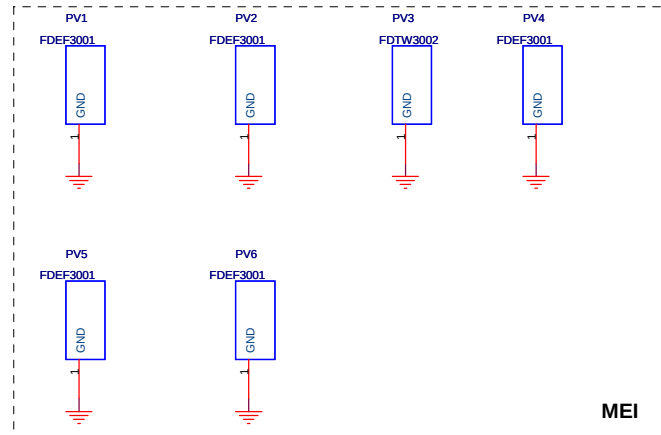
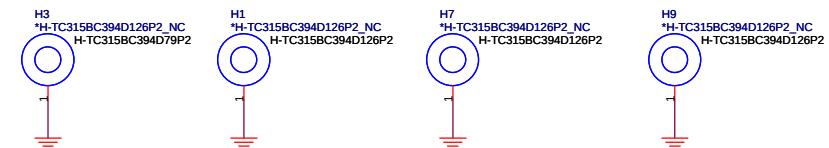
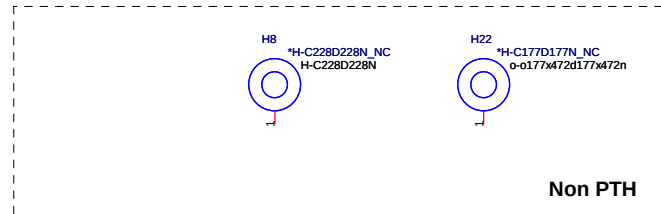
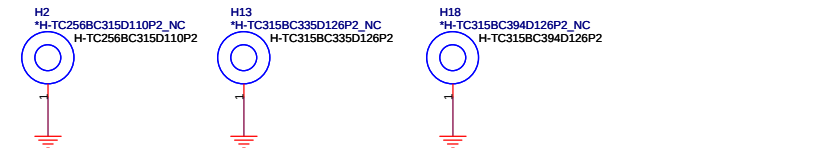
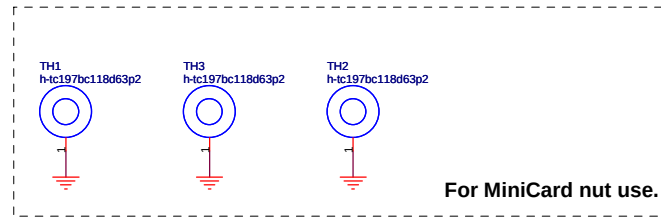
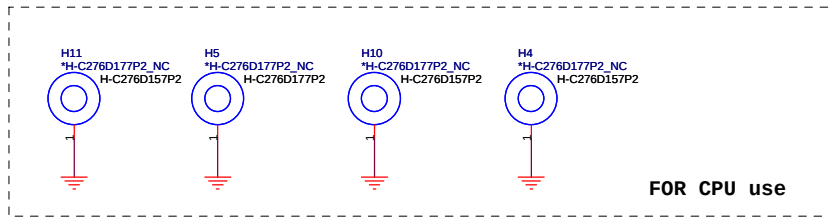
Reserve discharge path



Reserve discharge path







Reserved for EMI.

Stitching caps.



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EMI CAP		
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