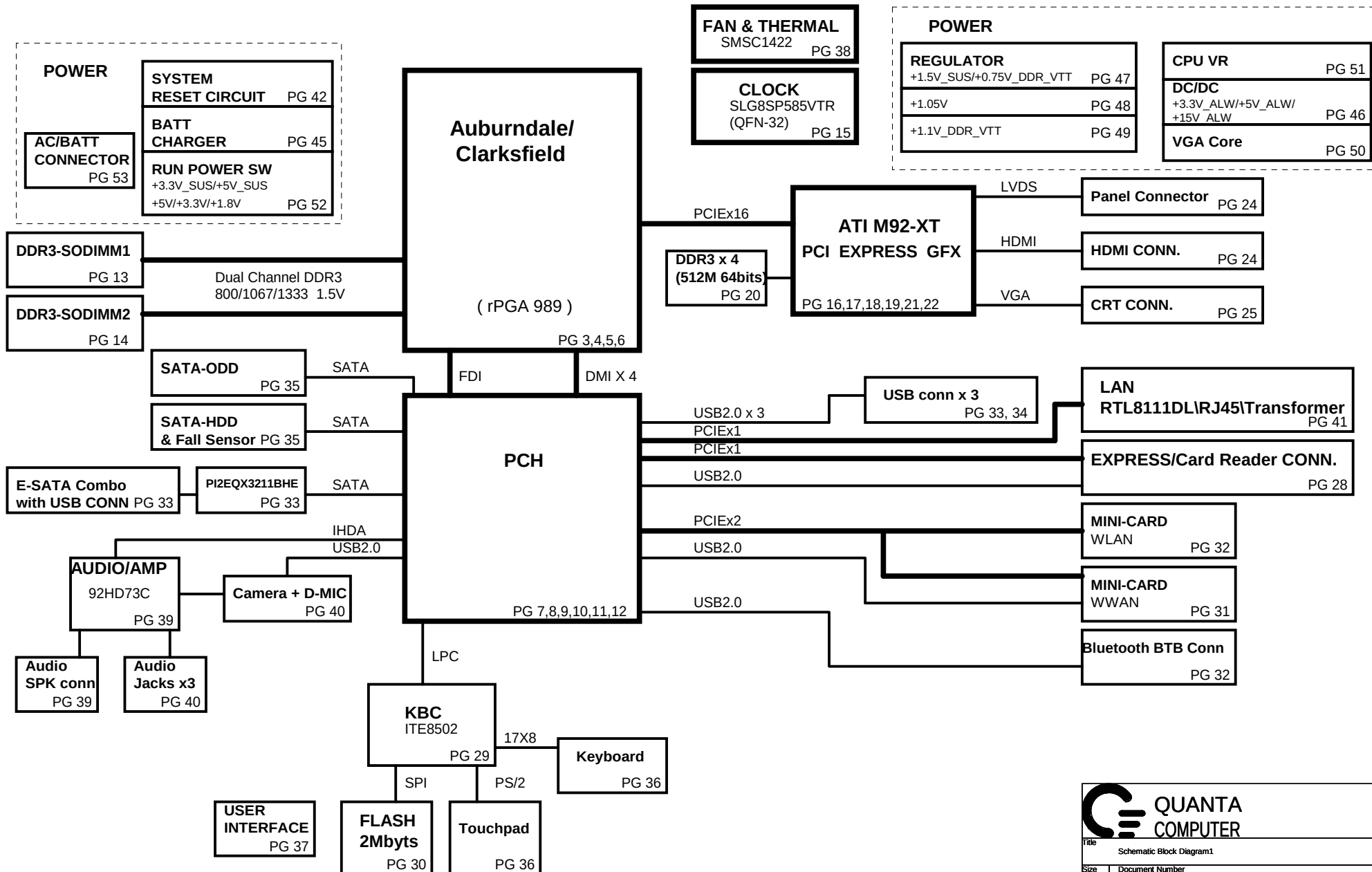


FM9 XXXX Intel Discrete GFX

VER : 1A

PWA:

PWB:



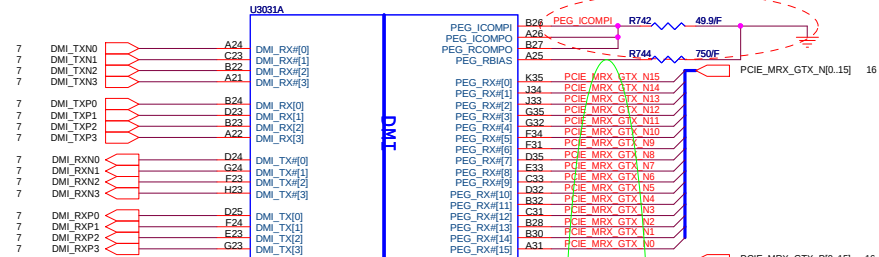
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-6	Clarksfield/Auburndale
7-12	PCH
13-14	DDRIII SO-DIMM(204P)
15	Clock Generator
16-22	M92-S2-XT
23	BLANK PAGE
24	LCD CONN / HDMI CONN
25	CRT CONN
26	OZ888GS0L3N
27	BLANK PAGE
28	Express/CRard/1394
29	SIO (ITE8512)
30	FLASH / RTC
31	MINI-Card (WWAN)
32	MINI-Card (WLAN/WPAN)
33	Left PUSB/ESATA
34	Right USB
35	SATA (HDD & CD_ROM)
36	TP / KEYBOARD
37	SWITCH / LED
38	FAN / THERMAL
39	Azelia CODEC
40	AUDIO CONN
41	LAN(RTL8111DL/RJ-45)
42	System Reset Circuit
43	Blank Page
44	1.8V_RUN(RT9018/RT9024)
45	Charger (ISL88731)
46	3V/5V (TPS51427A)
47	1.5_DDR/0.75(TPS51116)
48	1.05V_PCH(TPS51218)
49	1.1_VTT(TPS51218)
50	VGA_M92-XT(MAX8792)
51	V_CORE(ISL62882)
52	Run Power Switch
53	DCin & Batt
54	PAD & SCREW
55	EMI CAP
56	SMBUS BLOCK
57	THERMAL MAP
58	Power Block Diagram
59	XDP

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+3.3V_ALW	+3.3V	08,29,30,35,36,37,42,44,45,46,47,52,53	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	37,46,53	LARGE POWER	RUN_ON	S0~S5
+3.3V_LAN	+3.3V	41	LAN POWER	AUX_ON	
+5V_SUS	+5V	11,33,34,35,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	7,09,10,11,13,14,19,24,26,28,29,37,41,42,44,48,49,50,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.8V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.9V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,59	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,26,44,52	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	CALISTOGA/ICH9 POWER	RUN_ON	
+1.8V_RUN_GFX	+1.25V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN	
+5V_HDD	+5V	36	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,59			
+1.1V_GFX_PCIE	+1.1V	18,50			

GND PLANE	PAGE	DESCRIPTION
⏏ GND_CHG	46	
⏏ GND_1.05V	47	
⏏ GND_VGA	50	
⏏ GND_SIGNAL	51	
⏏ AGND_DC/DC	52	
⏏ GND	ALL	

AUBURNDALE/CLARKSFIELD PROCESSOR (DMI, PEG, FDI)

SC(V1.0),P11: Should be shorted at the pins and then routed to one end of the $49.9\text{-}\Omega \pm 1\%$ resistor, pulled-down to GND on the board.

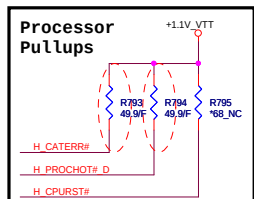
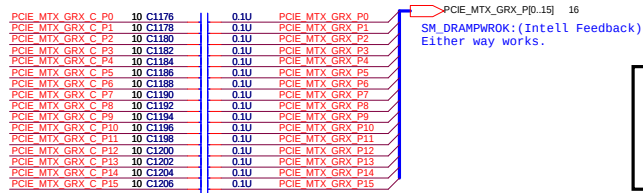
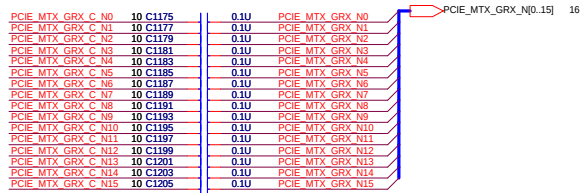
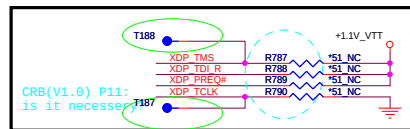
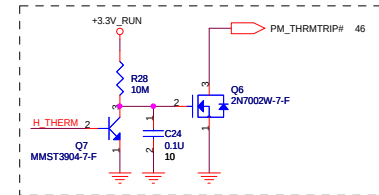


SC(V1.0),P17,35:
This signal should be connected to
the processor's VCCPWRGOOD_1
and VCCPWRGOOD_0 input to
indicate when the processor power is valid.

```
VTT_PWR_GOOD
SC(V1.0)P18:
VTT_1.1 VR power good signal
to processor. Signal voltage level
is 1.1 V.
```

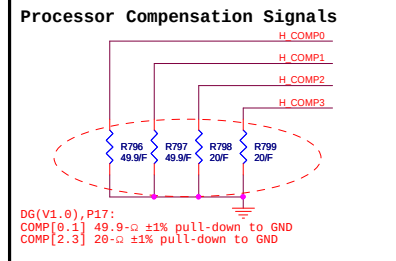
RSTIN#:
 DG(V1.11)(Doc.# 414044)_P10:-
 Need a voltage divider
 network to scale down from
 3.3V (PCH driven) to 1.05V/1.1V (Clarksfield/Auburndale)

SM_DRAMPWROK
DG(V1.0) P311&SC(V1.0) P18:recommend 4.75-ka
pull-up to DDR3 Power Rail (VDDQ) of +v1.5U
and a 12-ka pull-down to ground to convert
to processor's VTT level.
CRB(V1.0) P11:CRB uses a 3.3V (always ON) rail
for 1K and 1K combination. CRB Implementation
is different for the Calpella Platform Design Guide.
Customers to
follow the latest Calpella Platform Design
Guide for DRAMPWROK Implementation.



SC(1.0V),P17:
H_PROCHOT#D
use: pull to 68 ohm
if it isn'tt used: pull to 50 ohm

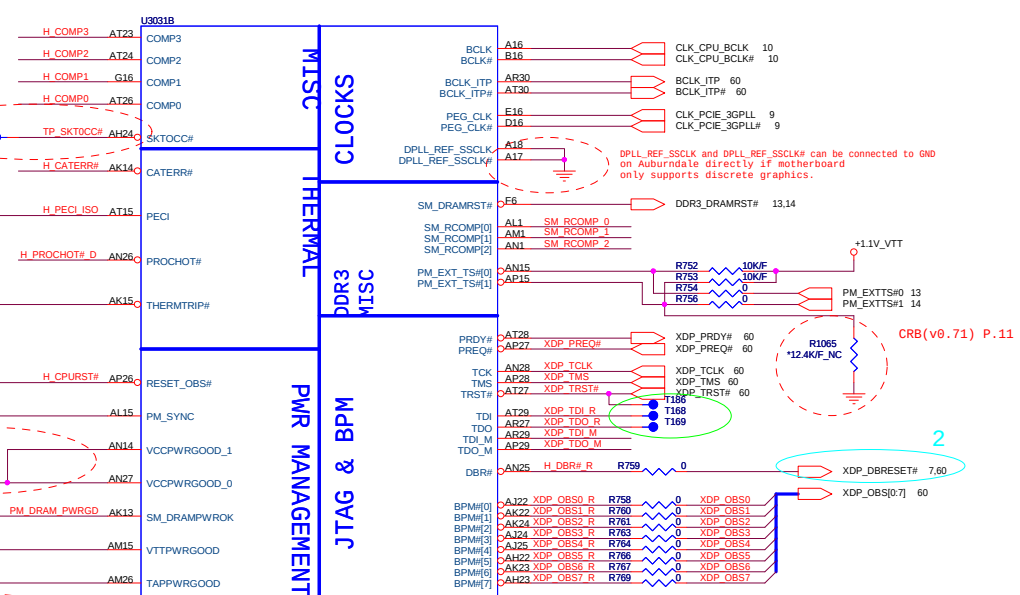
SC(1.0V), P17:
H_CATERR#
49.9-Ω ±1% Pull-Up to the VTT rail
(+V1, 10 VTT)



DG(V1.0), P17:

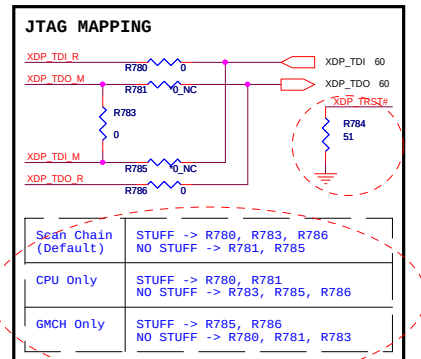
COMP[0.1]	49.9- Ω $\pm$ 1% pull-down to GND
COMP[2.3]	20- Ω $\pm$ 1% pull-down to GND

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

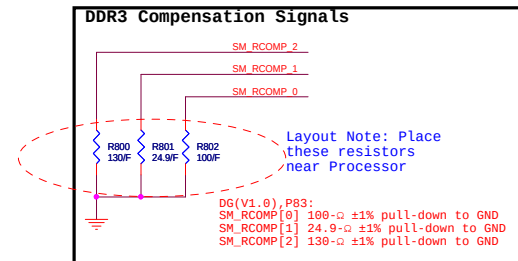


SC(V1.0) P22:Connected to the DBR# pin of the Processor.50-Ω to 5-kΩ pull-up to 3.3VS
CRB(V1.0) P11,P71:CRB uses a 1-kΩ pull-up to 3.3VS.
On the CRB this signal is ANDed with Master Reset to generate SYS_RESET.

DBR#:(Intell feedback)
Nothing wrong w/ CRB design. If you want to connect it to PCH directly, make sure pull high to 3.3V (S0) main power.



DG(v1.0) table 27 - TRST#
SC(v1.0)p22:
should be routed as a single
daisy chain to all loads and
terminated at the end of the trace
51 $\Omega \pm 5\%$ pull down resistor.
CRB(v1.0)p11



02
D/F

Layout Note: Place these resistors near Processor

DG(V1.0),P83:
SM_RCOMP[0] 100-Ω ±1% pull-down to GND
SM_RCOMP[1] 24.9-Ω ±1% pull-down to GND
SM_RCOMP[2] 130-Ω ±1% pull-down to GND

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

U3031C

SA_DQ[0] A10
SA_DQ[1] C10
SA_DQ[2] C7
SA_DQ[3] A7
SA_DQ[4] B10
SA_DQ[5] D10
SA_DQ[6] E10
SA_DQ[7] A8
SA_DQ[8] D8
SA_DQ[9] E10
SA_DQ[10] E6
SA_DQ[11] F7
SA_DQ[12] E9
SA_DQ[13] B7
SA_DQ[14] E7
SA_DQ[15] C6
SA_DQ[16] H10
SA_DQ[17] G8
SA_DQ[18] K7
SA_DQ[19] J8
SA_DQ[20] G7
SA_DQ[21] G10
SA_DQ[22] J7
SA_DQ[23] J10
SA_DQ[24] L7
SA_DQ[25] M8
SA_DQ[26] L9
SA_DQ[27] L6
SA_DQ[28] K8
SA_DQ[29] N8
SA_DQ[30] P9
SA_DQ[31] AH5
SA_DQ[32] AE5
SA_DQ[33] AK6
SA_DQ[34] AK7
SA_DQ[35] AE6
SA_DQ[36] AG5
SA_DQ[37] AJ7
SA_DQ[38] AJ6
SA_DQ[39] AI10
SA_DQ[40] AJ8
SA_DQ[41] AL10
SA_DQ[42] AK12
SA_DQ[43] AK8
SA_DQ[44] AL7
SA_DQ[45] AK11
SA_DQ[46] AL8
SA_DQ[47] AM6
SA_DQ[48] AM10
SA_DQ[49] AR11
SA_DQ[50] AL11
SA_DQ[51] AM9
SA_DQ[52] AN9
SA_DQ[53] AP12
SA_DQ[54] AM12
SA_DQ[55] AN12
SA_DQ[56] AM13
SA_DQ[57] AT14
SA_DQ[58] AT12
SA_DQ[59] AL13
SA_DQ[60] AR14
SA_DQ[61] AP14
SA_DQ[62] AP14
SA_DQ[63] AP14

DDR SYSTEM MEMORY A

SA_CLK[0] AA6
SA_CLK[1] AA7
SA_CKE[0] P7
SA_CLK[1] Y6
SA_CLK[1] Y5
SA_CKE[1] P6
SA_CS#[0] AE2
SA_CS#[1] AE8
SA_ODT[0] AD8
SA_ODT[1] AF9
SA_DM[0] B9
SA_DM[1] D7
SA_DM[2] H7
SA_DM[3] M7
SA_DM[4] AG6
SA_DM[5] AM7
SA_DM[6] AN10
SA_DM[7] AN13
SA_DQS#[0] C9
SA_DQS#[1] F8
SA_DQS#[2] J8
SA_DQS#[3] N9
SA_DQS#[4] AH7
SA_DQS#[5] AK9
SA_DQS#[6] AP11
SA_DQS#[7] AT13
SA_DQS[0] C8
SA_DQS[1] F9
SA_DQS[2] H9
SA_DQS[3] M9
SA_DQS[4] AH8
SA_DQS[5] AK10
SA_DQS[6] AN11
SA_DQS[7] AR13
SA_MA[0] Y3
SA_MA[1] W1
SA_MA[2] AA8
SA_MA[3] AA3
SA_MA[4] V1
SA_MA[5] AA9
SA_MA[6] V8
SA_MA[7] T1
SA_MA[8] Y9
SA_MA[9] U6
SA_MA[10] AD4
SA_MA[11] T2
SA_MA[12] U8
SA_MA[13] AG8
SA_MA[14] T3
SA_MA[15] V9
M_A_CLK0 13
M_A_CLK# 13
M_A_CKE0 13
M_A_CLK1 13
M_A_CLK# 13
M_A_CKE1 13
M_A_CS0# 13
M_A_CS1# 13
M_A_ODT0 13
M_A_ODT1 13
M_A_DM[7:0] 13
M_A_DQS#[7:0] 13
M_A_DQS[7:0] 13
M_A_DQS[7:0] 13
M_A_A[15:0] 13

Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

U3031D

SB_DQ[0] B5
SB_DQ[1] A5
SB_DQ[2] C3
SB_DQ[3] B3
SB_DQ[4] E4
SB_DQ[5] A6
SB_DQ[6] C4
SB_DQ[7] D1
SB_DQ[8] D2
SB_DQ[9] F2
SB_DQ[10] F1
SB_DQ[11] C2
SB_DQ[12] F5
SB_DQ[13] F3
SB_DQ[14] G4
SB_DQ[15] H6
SB_DQ[16] G2
SB_DQ[17] J6
SB_DQ[18] J3
SB_DQ[19] G1
SB_DQ[20] G5
SB_DQ[21] J2
SB_DQ[22] J1
SB_DQ[23] J5
SB_DQ[24] K2
SB_DQ[25] L3
SB_DQ[26] M1
SB_DQ[27] K5
SB_DQ[28] K4
SB_DQ[29] M4
SB_DQ[30] N5
SB_DQ[31] AE3
SB_DQ[32] AE1
SB_DQ[33] A3
SB_DQ[34] AK1
SB_DQ[35] AG4
SB_DQ[36] AG3
SB_DQ[37] AJ4
SB_DQ[38] AH4
SB_DQ[39] AK3
SB_DQ[40] AK4
SB_DQ[41] AM6
SB_DQ[42] AN2
SB_DQ[43] AK5
SB_DQ[44] AK2
SB_DQ[45] AM4
SB_DQ[46] AM3
SB_DQ[47] AP3
SB_DQ[48] AN5
SB_DQ[49] AT4
SB_DQ[50] AN6
SB_DQ[51] AN4
SB_DQ[52] AN3
SB_DQ[53] AT5
SB_DQ[54] AT6
SB_DQ[55] AN7
SB_DQ[56] AP6
SB_DQ[57] AP8
SB_DQ[58] AT9
SB_DQ[59] AT7
SB_DQ[60] AP9
SB_DQ[61] AR10
SB_DQ[62] AR10
SB_DQ[63] AT10
M_B_DQ0 13
M_B_DQ1 13
M_B_DQ2 13
M_B_DQ3 13
M_B_DQ4 13
M_B_DQ5 13
M_B_DQ6 13
M_B_DQ7 13
M_B_DQ8 13
M_B_DQ9 13
M_B_DQ10 13
M_B_DQ11 13
M_B_DQ12 13
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M_B_DQ14 13
M_B_DQ15 13
M_B_DQ16 13
M_B_DQ17 13
M_B_DQ18 13
M_B_DQ19 13
M_B_DQ20 13
M_B_DQ21 13
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M_B_DQ25 13
M_B_DQ26 13
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M_B_DQ57 13
M_B_DQ58 13
M_B_DQ59 13
M_B_DQ60 13
M_B_DQ61 13
M_B_DQ62 13
M_B_DQ63 13
M_B_BS0 14
M_B_BS1 14
M_B_BS2 14
M_B_CAS# 14
M_B_RAS# 14
M_B_WE# 14

DDR SYSTEM MEMORY - B

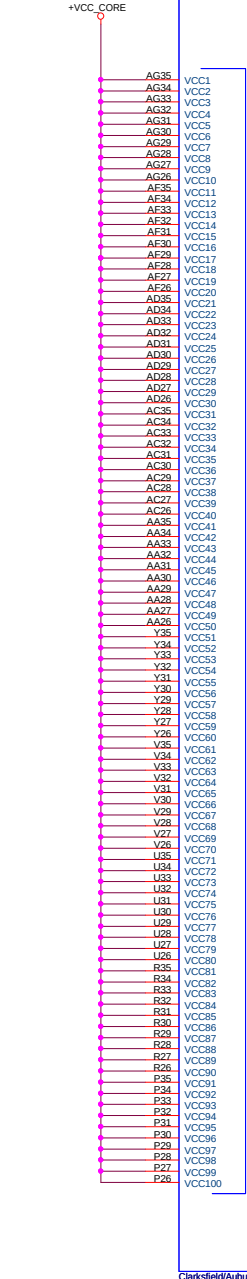
SB_CLK[0] W8
SB_CLK[1] V7
SB_CKE[0] W9
SB_CKE[1] V6
SB_CS#[0] AB8
SB_CS#[1] AD8
SB_ODT[0] AC7
SB_ODT[1] AD1
SB_DM[0] D4
SB_DM[1] E1
SB_DM[2] H3
SB_DM[3] K1
SB_DM[4] AH1
SB_DM[5] AL2
SB_DM[6] AR4
SB_DM[7] AT8
SB_DQS#[0] D5
SB_DQS#[1] E4
SB_DQS#[2] J4
SB_DQS#[3] L4
SB_DQS#[4] AH2
SB_DQS#[5] AL4
SB_DQS#[6] AR5
SB_DQS#[7] AR8
SB_DQS[0] C5
SB_DQS[1] E3
SB_DQS[2] H4
SB_DQS[3] M5
SB_DQS[4] AG2
SB_DQS[5] AL5
SB_DQS[6] AP5
SB_DQS[7] AR7
SB_MA[0] U5
SB_MA[1] V2
SB_MA[2] T5
SB_MA[3] V3
SB_MA[4] R1
SB_MA[5] T8
SB_MA[6] R2
SB_MA[7] R6
SB_MA[8] R4
SB_MA[9] R5
SB_MA[10] AB5
SB_MA[11] P3
SB_MA[12] R3
SB_MA[13] AF7
SB_MA[14] P5
SB_MA[15] N1
M_B_CLK0 14
M_B_CLK# 14
M_B_CKE0 14
M_B_CLK1 14
M_B_CLK# 14
M_B_CKE1 14
M_B_CS0# 14
M_B_CS# 14
M_B_ODT0 14
M_B_ODT1 14
M_B_DM[7:0] 14
M_B_DQS#[7:0] 14
M_B_DQS[7:0] 14
M_B_DQS[7:0] 14
M_B_A[15:0] 14

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.



Title AUBURNDA 2/4		
Size F1M9	Document Number	Rev 1A
Date Thursday, February 26, 2009	Sheet 4	of 64

CPU Core Power

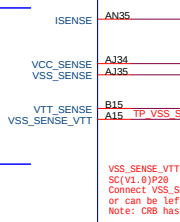
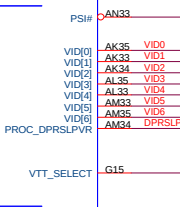
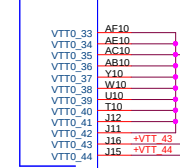
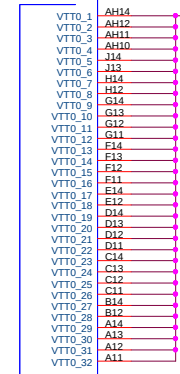


1.1V RAIL POWER

CPU CORE SUPPLY

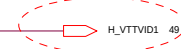
CPU VIDS

SENSE LINES



VTT0_43, VTT0_44:
CRB(V1.0)P13
Why add 0ohm?? Is it trace width control??

VTT0_43, VTT0_44: (Intel feedback)
They are connected to hidden page for intel validation purpose.



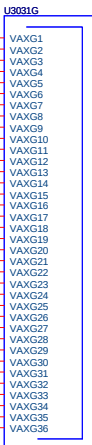
VTT_SELECT:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
180- ±1% pull-down to GND near processor

PROC_DPRSPLVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options in the design for the Turbo functionality. The stuffing and no-stuffing of the resistors will depend on the POC configuration of AUB and CLF.
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

Note:
For Validating IMVP VR R814 should be STUFF and R827 NO_STUFF

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



GRAPHICS

DDR3

1.1V

1.8V

SENSE LINES

DDR3 - 1.5V RAILS

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

1.8V

1.1V

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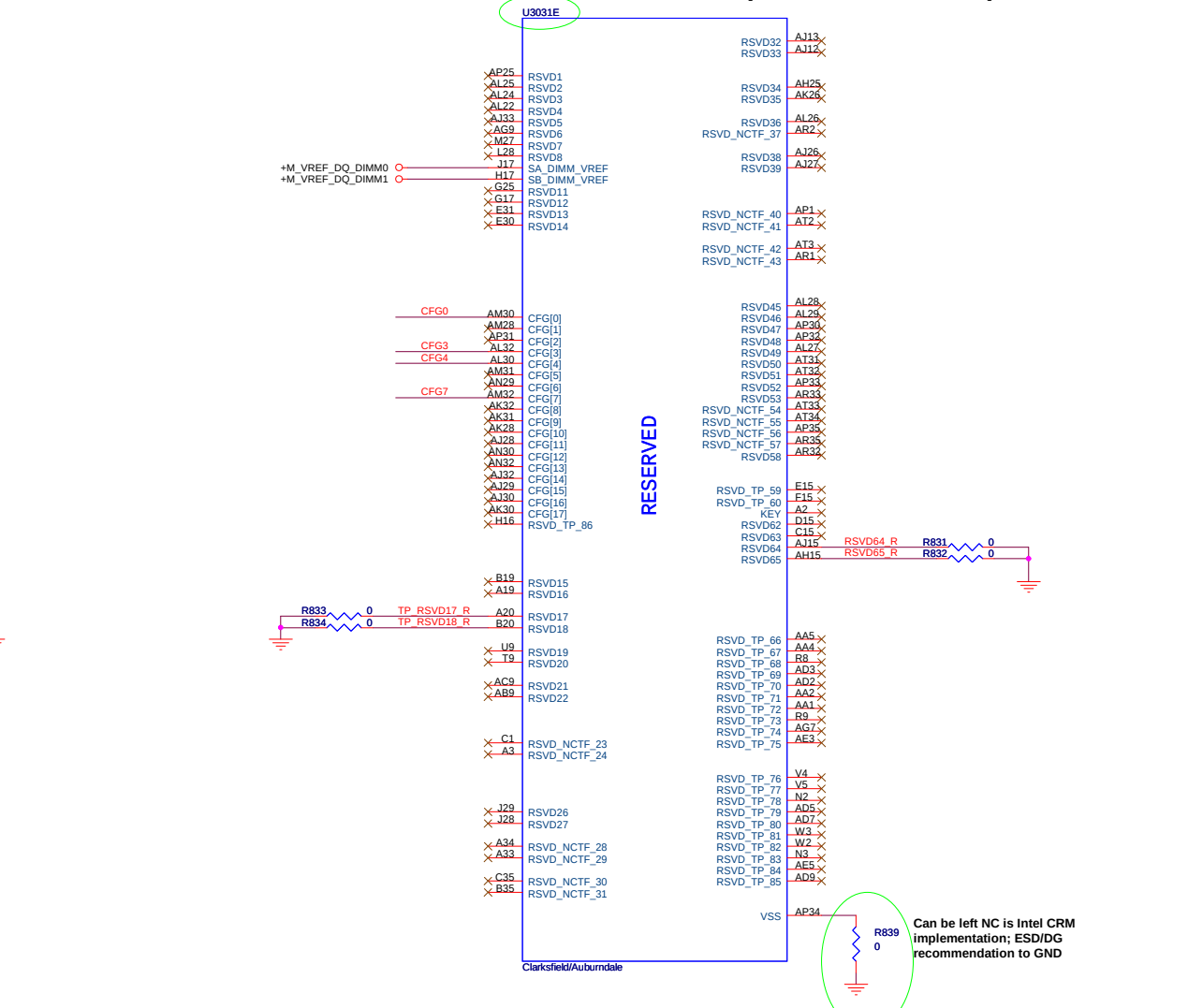
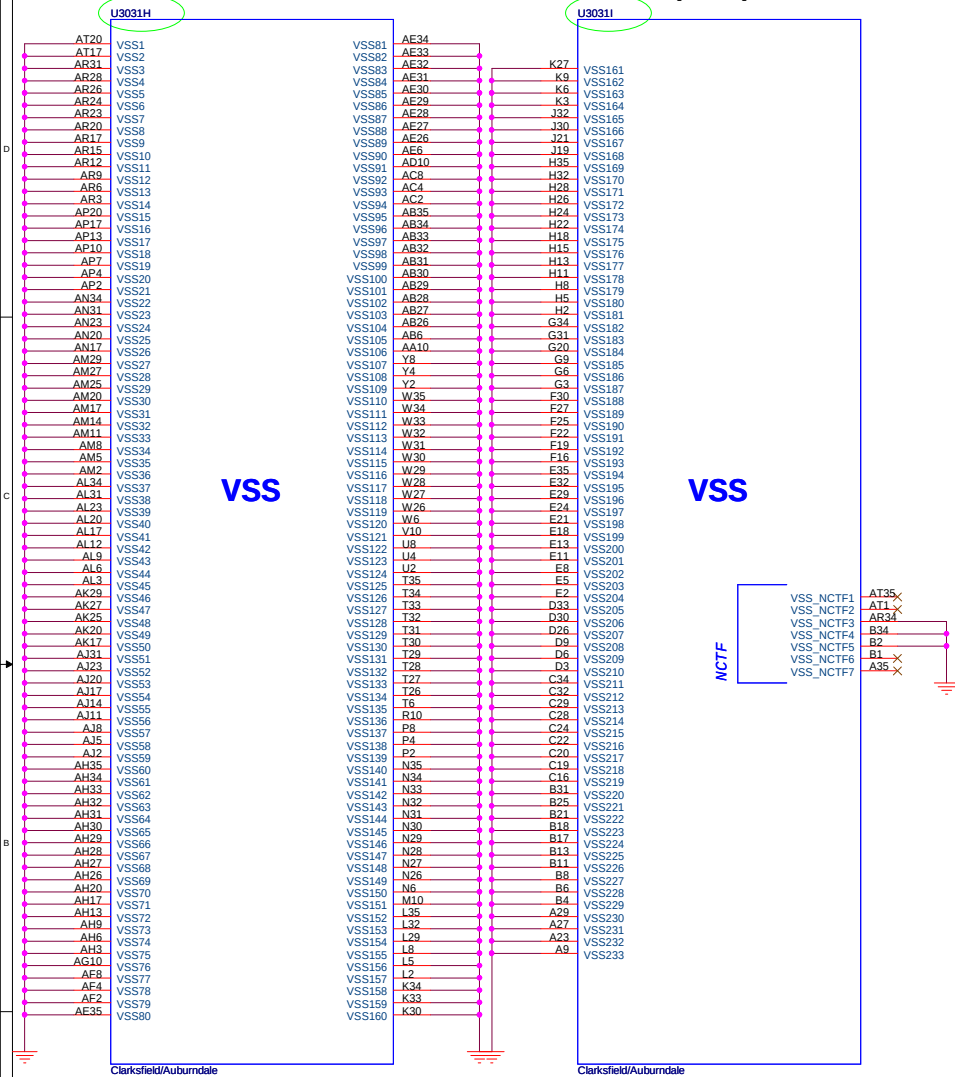
1.1V

1.8V

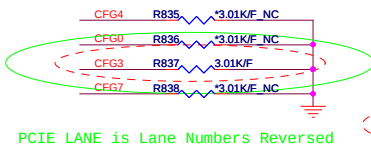
1.1V

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



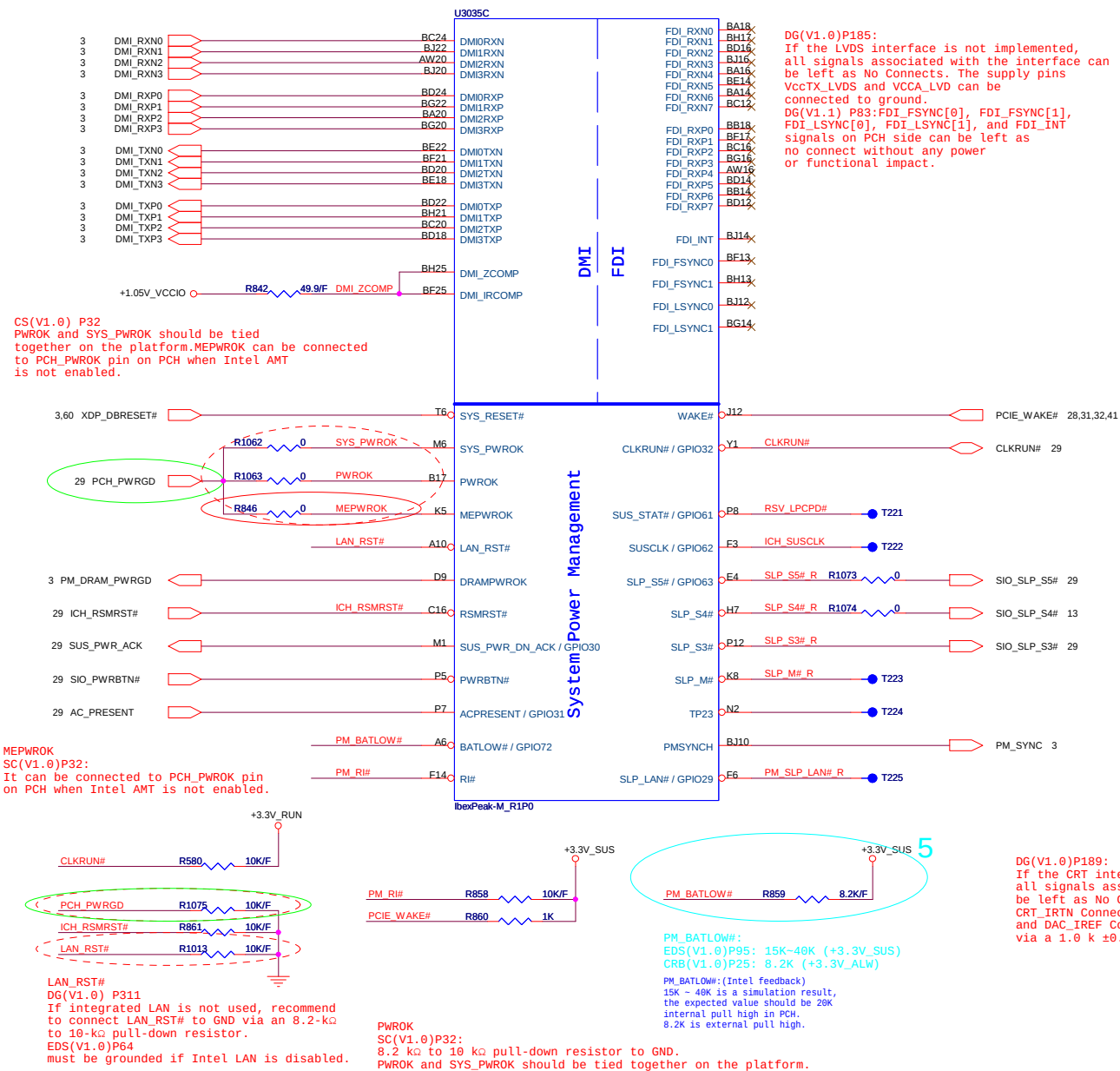
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



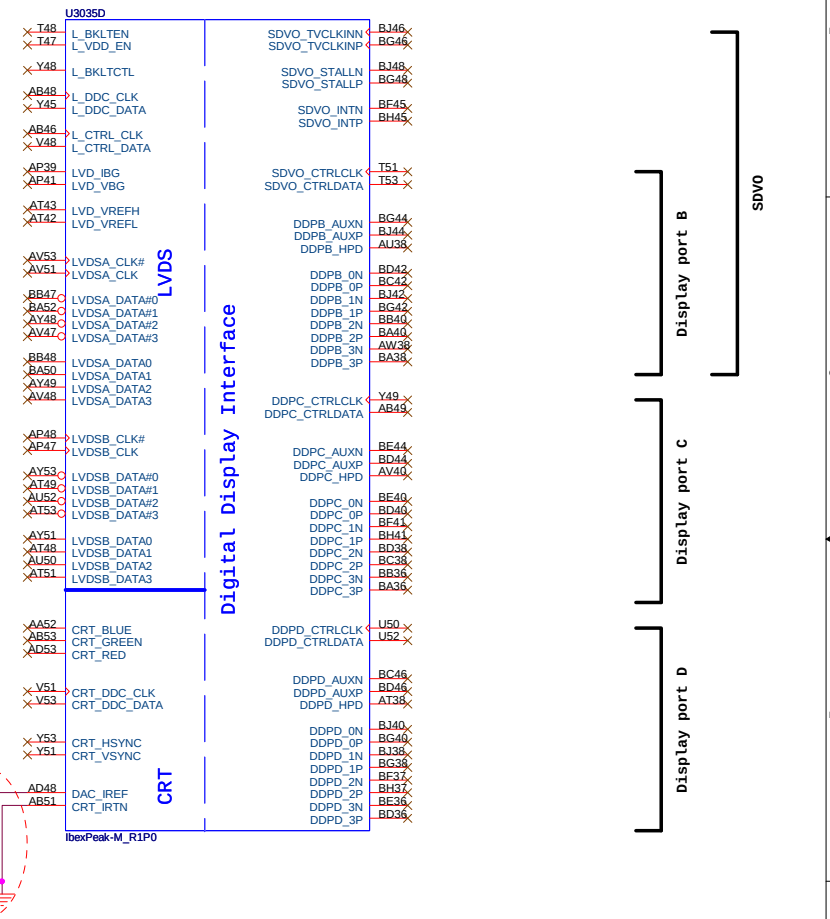
QUANTA
COMPUTER

Title AUBURNDA 4/4		
Size FM9	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009		Sheet 6 of 64

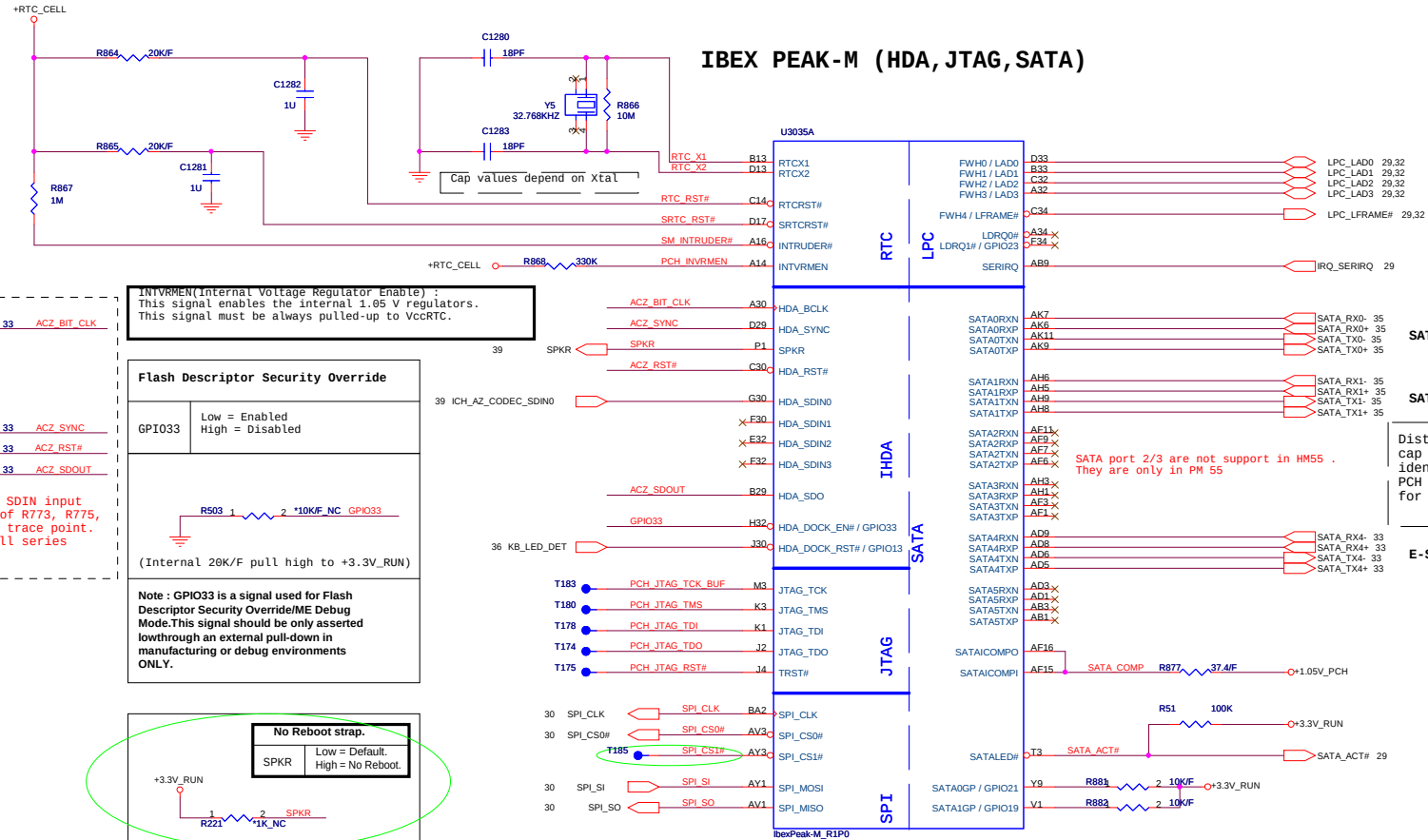
IBEX PEAK-M (DMI, FDI, GPIO)



IBEX PEAK-M (LVDS, DDI)



IBEX PEAK-M (HDA, JTAG, SATA)



IBEX PEAK-M 1/6

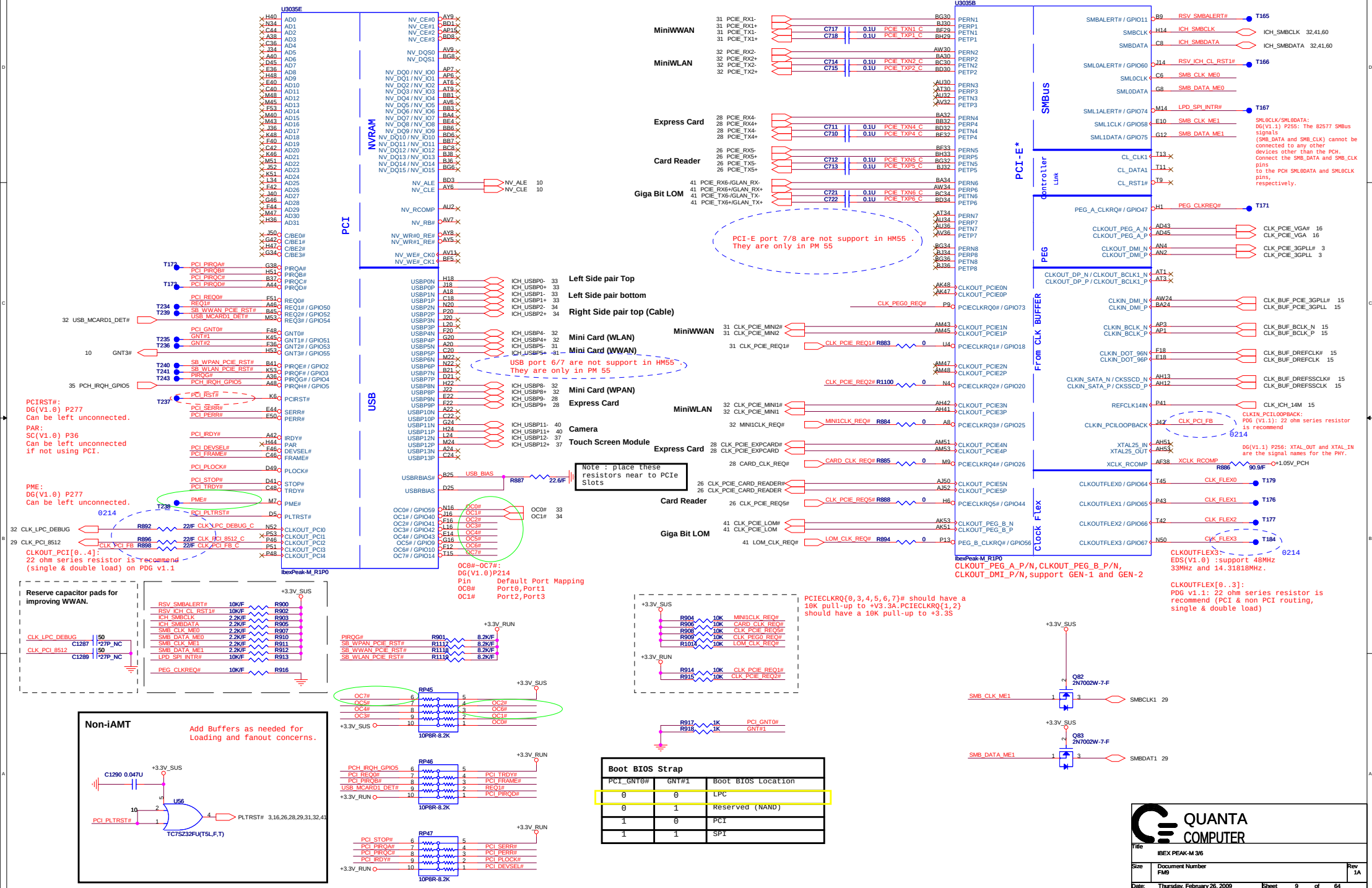
Size	Document Number	Rev
FM9		1A

Date: Thursday, February 26, 2009 Sheet 8 of 64

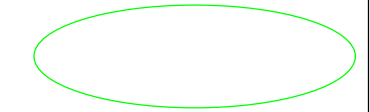
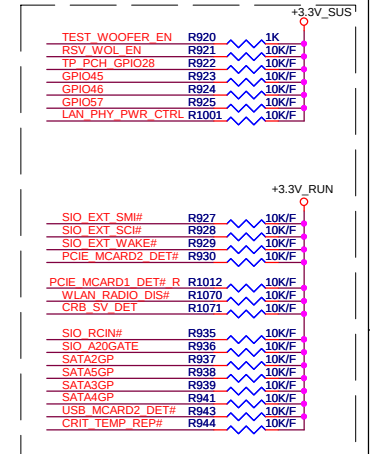
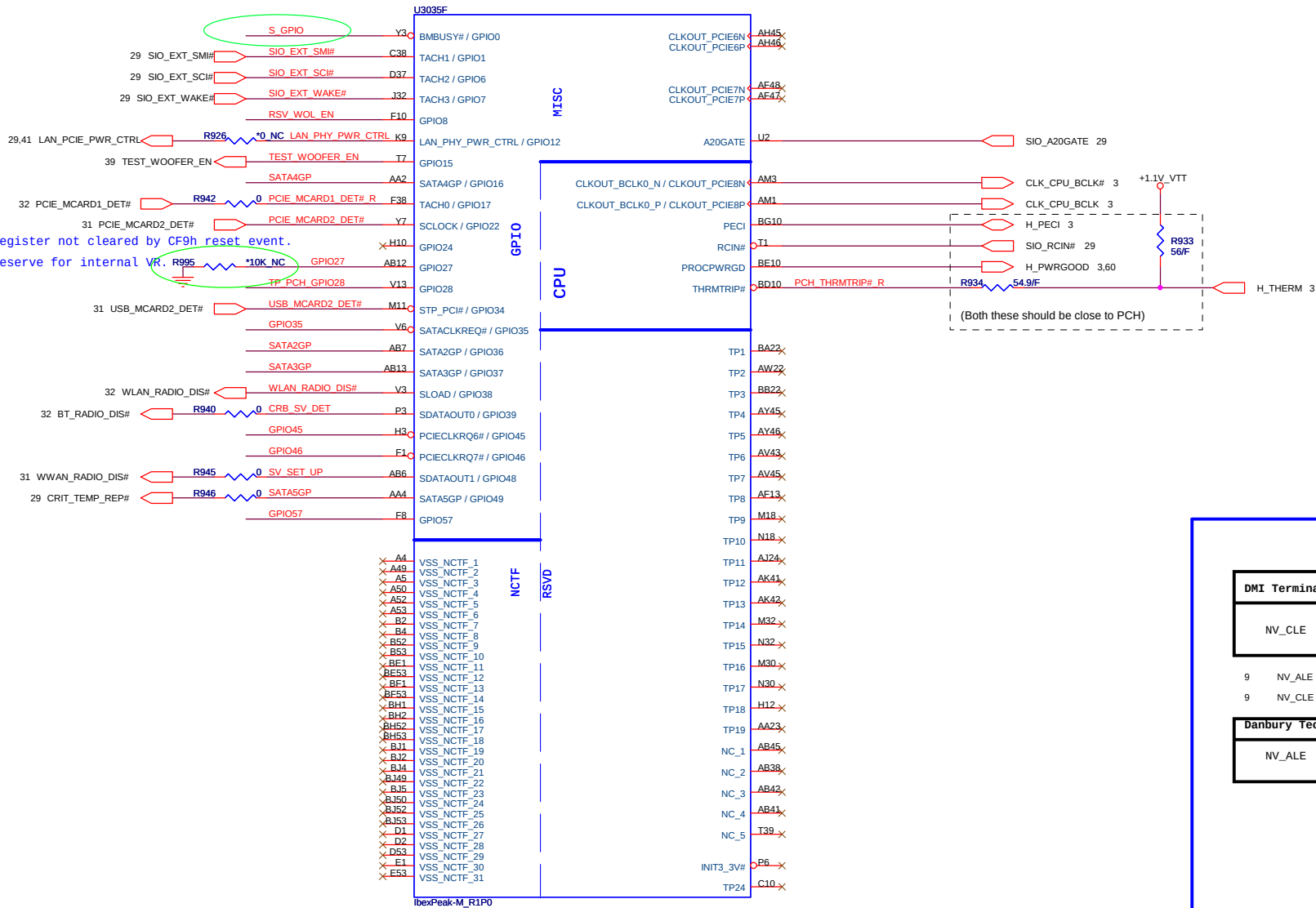
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.

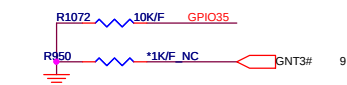


IBEX PEAK-M (GPIO, VSS_NCTF, RSVD)



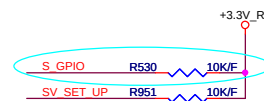
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP	1-X High = Strong (Default)
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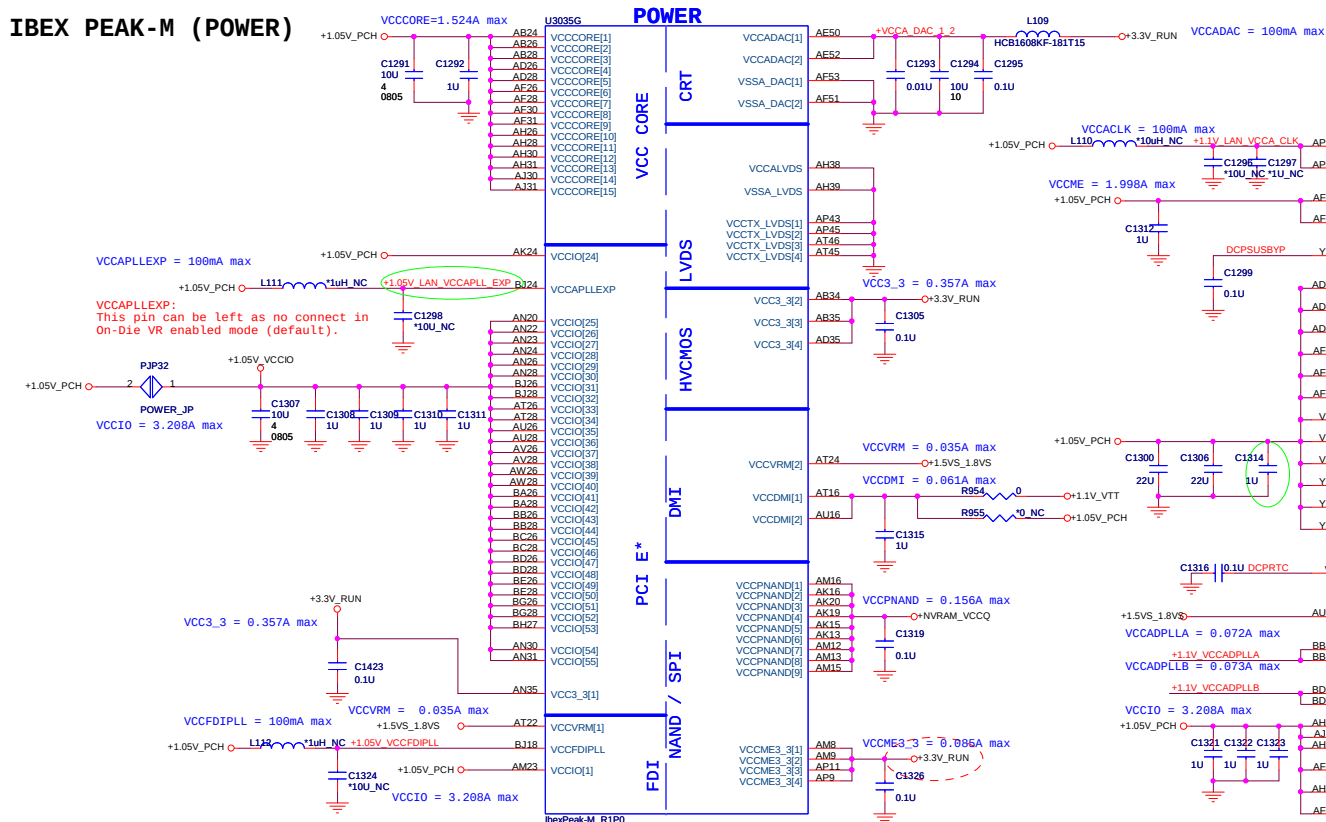
BMBUSY#:
 If not used, require a weak pull-up (8.2- kΩ to 10 kΩ) to Vcc3_3.
 CRB(V1.0)P28: it has 1K PU and 180 ohm on this net for validation purpose.

BMBUSY#:(Intel feedback)
 Follow CRB checklist, 1K is
 for intel BIOS validation purpose.

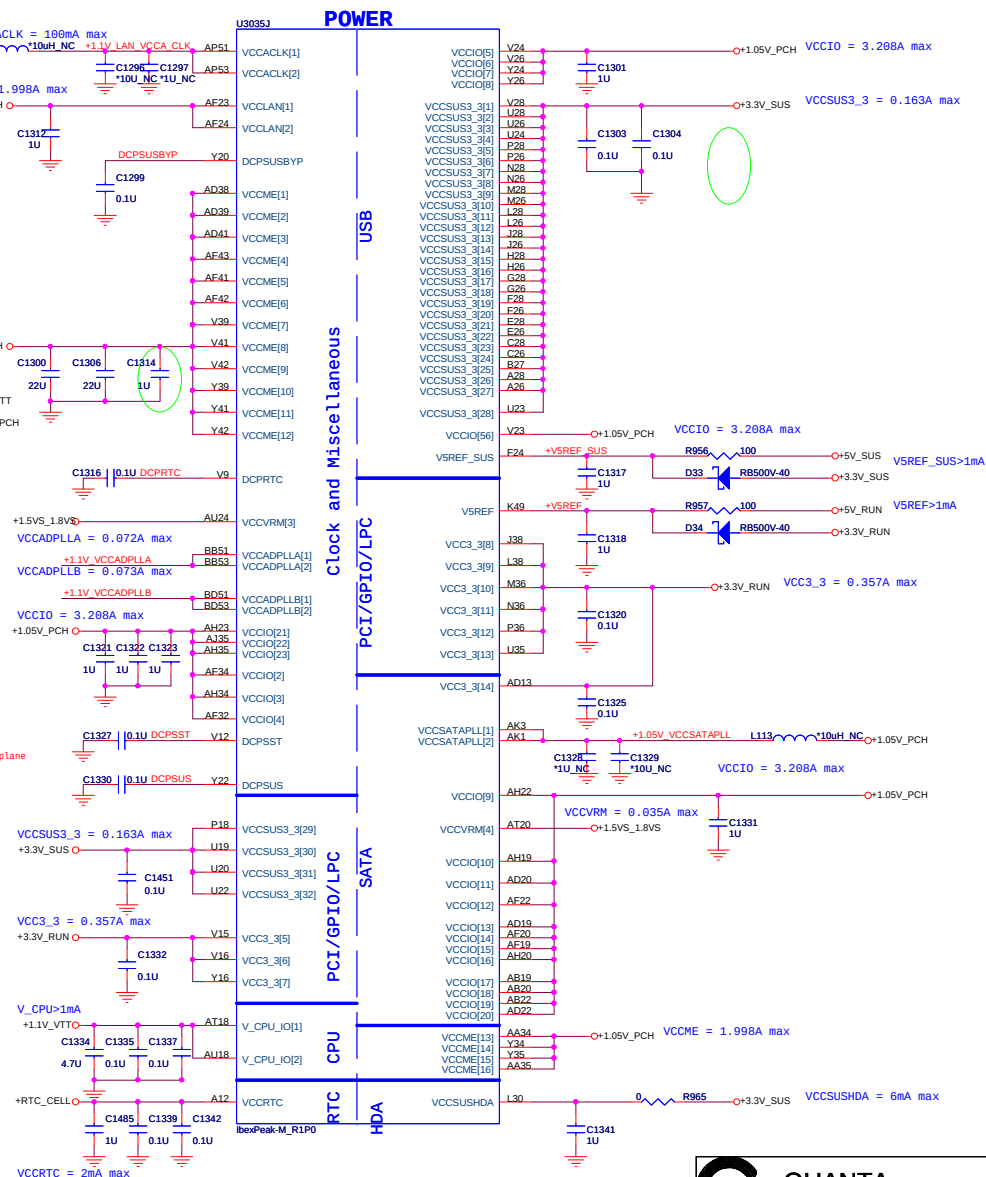
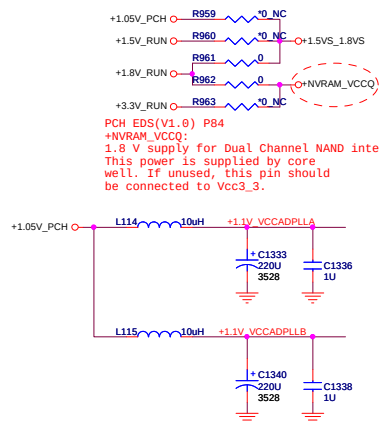


Title			
IBEX PEAK-M 4/6			
Size	Document Number	Rev	
	FM9	1A	
Date:	Thursday, February 26, 2009	Sheet	10 of 64

IBEX PEAK-M (POWER)

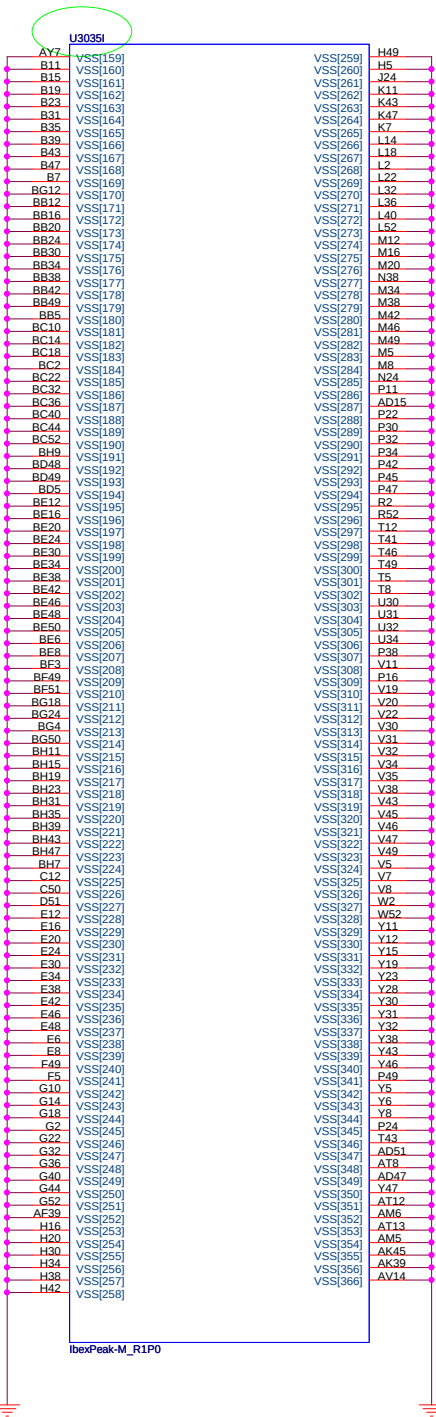
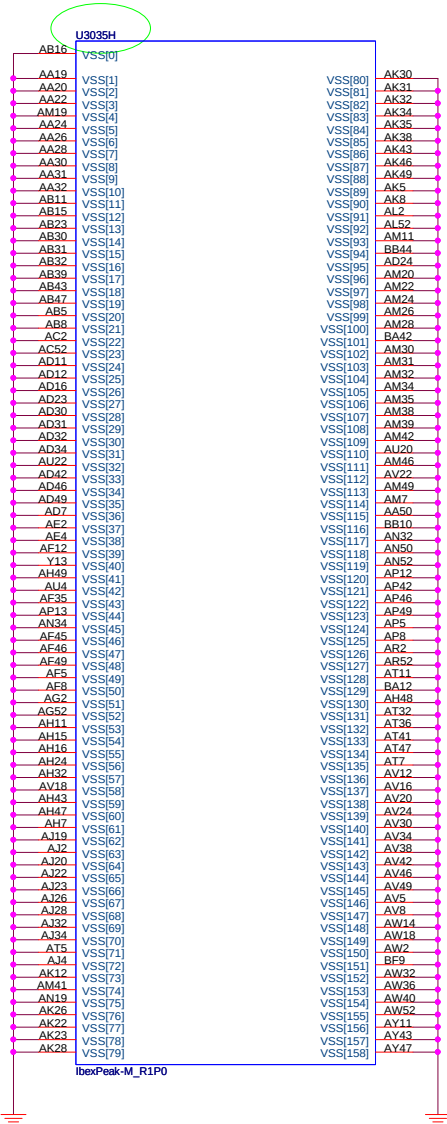


```
VCCME3_3:
EDS(V1.0)P84:supply for the Intel Management Engine.This is a separate power plane
that may or may not be powered in S3-S5 states.
This plane must be on in S0
and other times the Intel Management Engine is used.
```

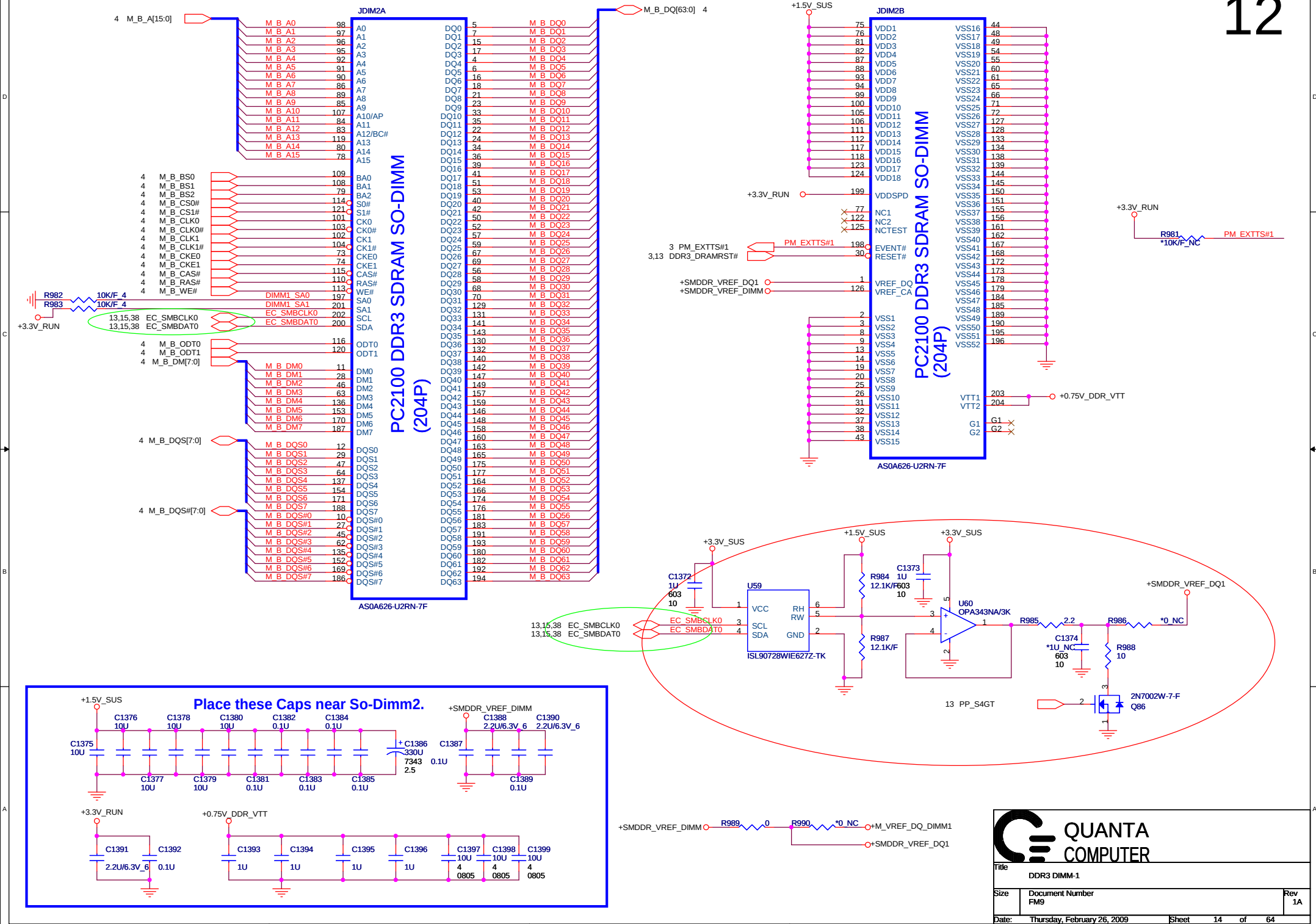


Title			
IBEX PEAK-M 5/6			
Size	Document Number		Rev
	FM9		1A
Date:	Thursday, February 26, 2009	Sheet	11 of 64

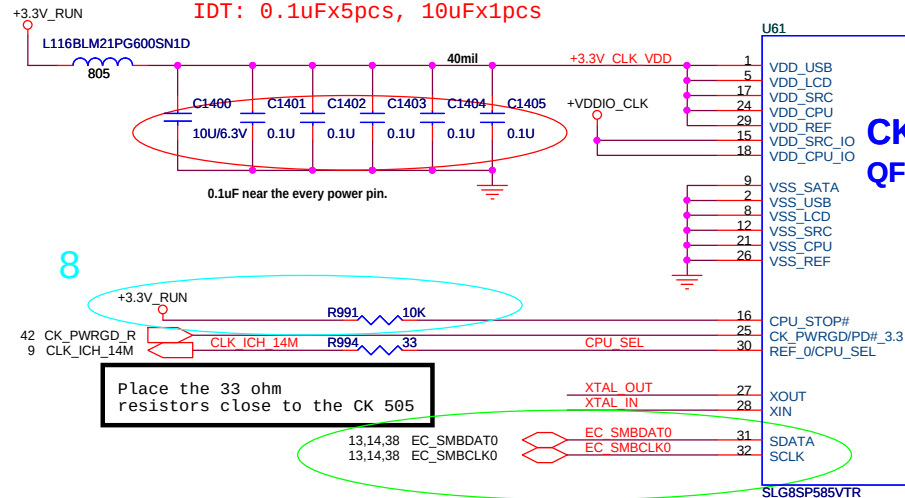
IBEX PEAK-M (GND)



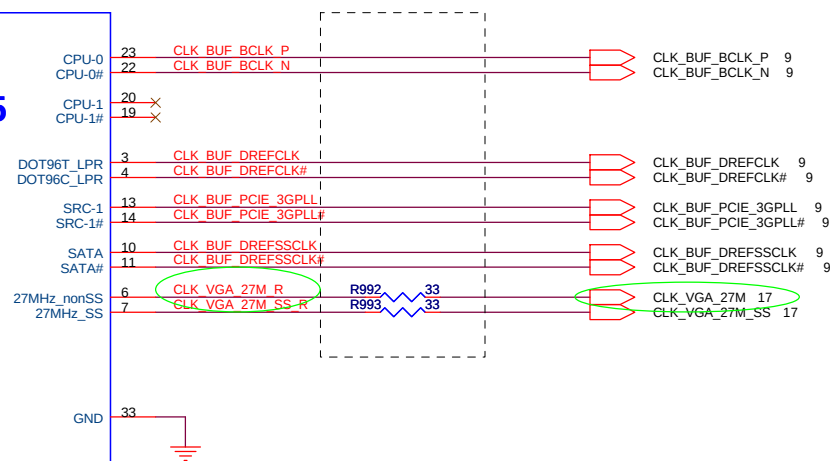




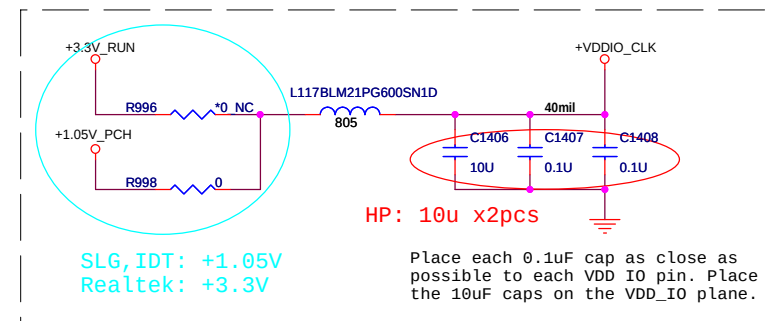
Realtek: 0.1uF x 6pcs, 22uF x 1pcs
IDT: 0.1uF x 5pcs, 10uF x 1pcs



Place within 0.5" of CLKGEN

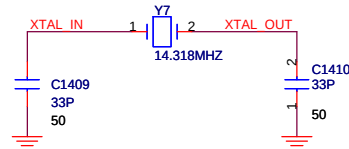


Realtek: 0.1uF x 3pcs, 22uF x 1pcs
IDT: 0.1uF x 2pcs, 10uF x 1pcs



+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.
Realtek date sheet (V1.2) P11: Min 1.05V, Max 3.3V.
IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.

Add capacitor pads for improving WWAN.



SLG, IDT: +1.05V
Realtek: +3.3V

PIN	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet (V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet (V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

3 PCIE_MTX_GRX_P[0..15]
3 PCIE_MTX_GRX_N[0..15]

PCIE_MTX_GRX_P0 AE30
PCIE_MTX_GRX_N0 AE31

PCIE_MTX_GRX_P1 AE29
PCIE_MTX_GRX_N1 AD28

PCIE_MTX_GRX_P2 AD30
PCIE_MTX_GRX_N2 AC31

PCIE_MTX_GRX_P3 AC29
PCIE_MTX_GRX_N3 AB28

PCIE_MTX_GRX_P4 AB30
PCIE_MTX_GRX_N4 AA31

PCIE_MTX_GRX_P5 AA29
PCIE_MTX_GRX_N5 Y28

PCIE_MTX_GRX_P6 Y30
PCIE_MTX_GRX_N6 W31

PCIE_MTX_GRX_P7 W28
PCIE_MTX_GRX_N7 V28

PCIE_MTX_GRX_P8 V30
PCIE_MTX_GRX_N8 U31

PCIE_MTX_GRX_P9 U29
PCIE_MTX_GRX_N9 T28

PCIE_MTX_GRX_P10 T30
PCIE_MTX_GRX_N10 R31

PCIE_MTX_GRX_P11 R29
PCIE_MTX_GRX_N11 P28

PCIE_MTX_GRX_P12 P30
PCIE_MTX_GRX_N12 N31

PCIE_MTX_GRX_P13 N29
PCIE_MTX_GRX_N13 M28

PCIE_MTX_GRX_P14 M30
PCIE_MTX_GRX_N14 L31

PCIE_MTX_GRX_P15 L29
PCIE_MTX_GRX_N15 K30

U32A

PART 1 OF 10

PCI-EXPRESS INTERFACE

PCIE_REFCLKP
PCIE_REFCLKN

PERSTB
M92-S2M92-XT

M92-S2 XT AJ072800T04 100-C61675(216-0728004)
M92-S2 AJ072800T03 100-C61643(216-0728003)

3 PCIE_MRX_GTX_P[0..15]
3 PCIE_MRX_GTX_N[0..15]

PCIE_MRX_GTX_P0 0.1U 2 1 C814 10 PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1 0.1U 2 1 C815 10 PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2 0.1U 2 1 C816 10 PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3 0.1U 2 1 C817 10 PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4 0.1U 2 1 C818 10 PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5 0.1U 2 1 C819 10 PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6 0.1U 2 1 C820 10 PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7 0.1U 2 1 C821 10 PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8 0.1U 2 1 C822 10 PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9 0.1U 2 1 C823 10 PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10 0.1U 2 1 C824 10 PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11 0.1U 2 1 C825 10 PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12 0.1U 2 1 C826 10 PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13 0.1U 2 1 C827 10 PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14 0.1U 2 1 C828 10 PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15 0.1U 2 1 C829 10 PCIE_MRX_GTX_C_P15

PCIE_MRX_GTX_N0 0.1U 2 1 C830 10 PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1 0.1U 2 1 C831 10 PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2 0.1U 2 1 C832 10 PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3 0.1U 2 1 C833 10 PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4 0.1U 2 1 C834 10 PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5 0.1U 2 1 C835 10 PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6 0.1U 2 1 C836 10 PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7 0.1U 2 1 C837 10 PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8 0.1U 2 1 C838 10 PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9 0.1U 2 1 C839 10 PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10 0.1U 2 1 C840 10 PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11 0.1U 2 1 C841 10 PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12 0.1U 2 1 C842 10 PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13 0.1U 2 1 C843 10 PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14 0.1U 2 1 C844 10 PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15 0.1U 2 1 C845 10 PCIE_MRX_GTX_C_N15

100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing.
clock must be provided less than 400ns
after CLKREQ# is asserted

9 CLK_PCIE_VGA
9 CLK_PCIE_VGA#

9,26,28,29,31,32,41 PLTRST#

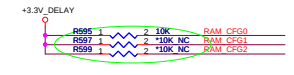
(1.1V)
+PCIE_VDDC

PCIE_CALRN AA22 PCIE_CALRN 2.0K R591
PCIE_CALRP Y22 PCIE_CALRP 1.27K R592

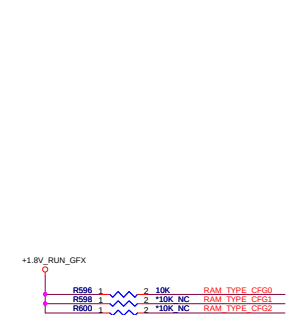
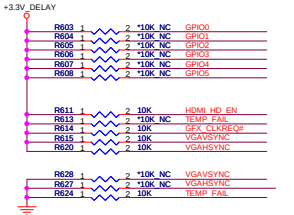


Title VGA-M92-XT (PCIe)			
Size	Document Number FM9	Rev 1A	
Date:	Thursday, February 26, 2009	Sheet	16 of 64

MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GP109	CFG2 GP1013	CFG1 GP1012	CFG0 GP1011
128MB	0	0	0	0
256MB	0	0	0	1
64MB	0	0	1	0
512MB	1	0	0	0

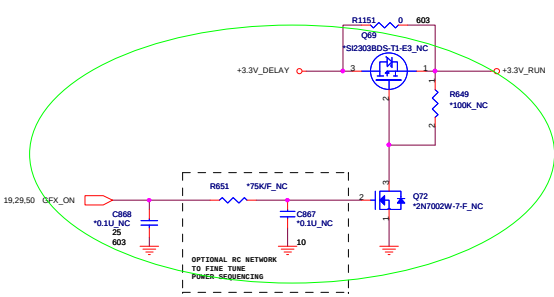


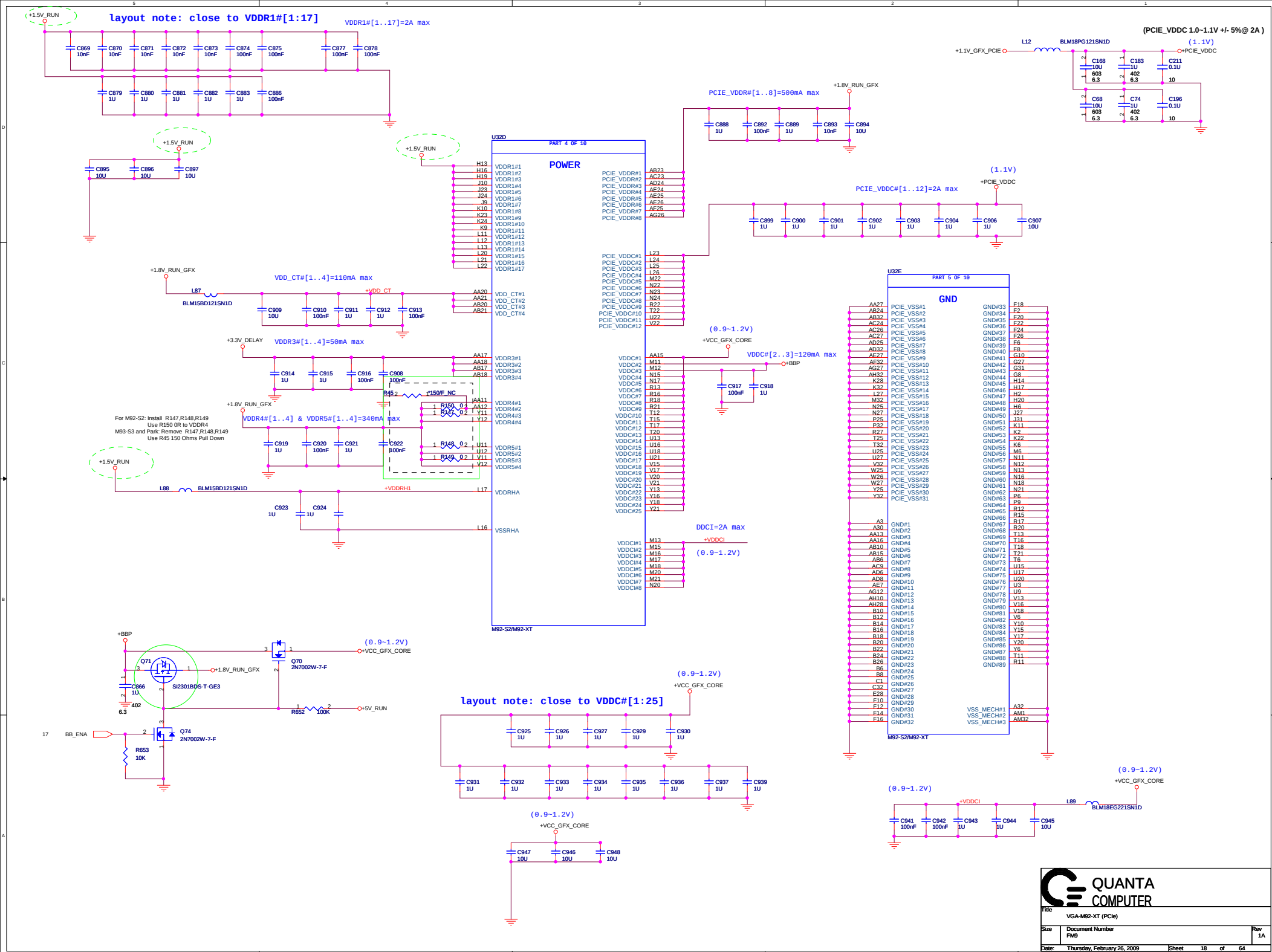
GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	FM9 setting
GPIO0	GPIO0 - TX_PWDN_EN (Transmitter Power Savings Enable) 0: 50% Tx output swing (Default setting for Desktop) 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO1 - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO2 - BIF_GEN2_EN (5.0 GT/s Enable) 0: Default (Driver Controlled Gen2) 1: Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO 5 AC_BATT 0: Battery saving mode = 0.9 V 1: AC (Performance mode) = 3.3 V	0
GPIO6	ATI Internal use only	0



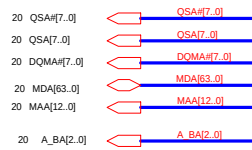
Memory Straps	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Quanta PN (winBuy)	Vendor PN	31 level PN
800MHz	0	0	1	AKD5LGGT502		K4W1G1646E-HC12	
512MB(64M*16) Samsung	0	0	1	AKD5LGGT502		K4W1G1646E-HC12	
800MHz	0	1	0	AKD5LZGTW00		H5TQ1G63BFR-12C	
512MB(64M*16) Hynix	0	1	0	AKD5LZGTW00		H5TQ1G63BFR-12C	

5

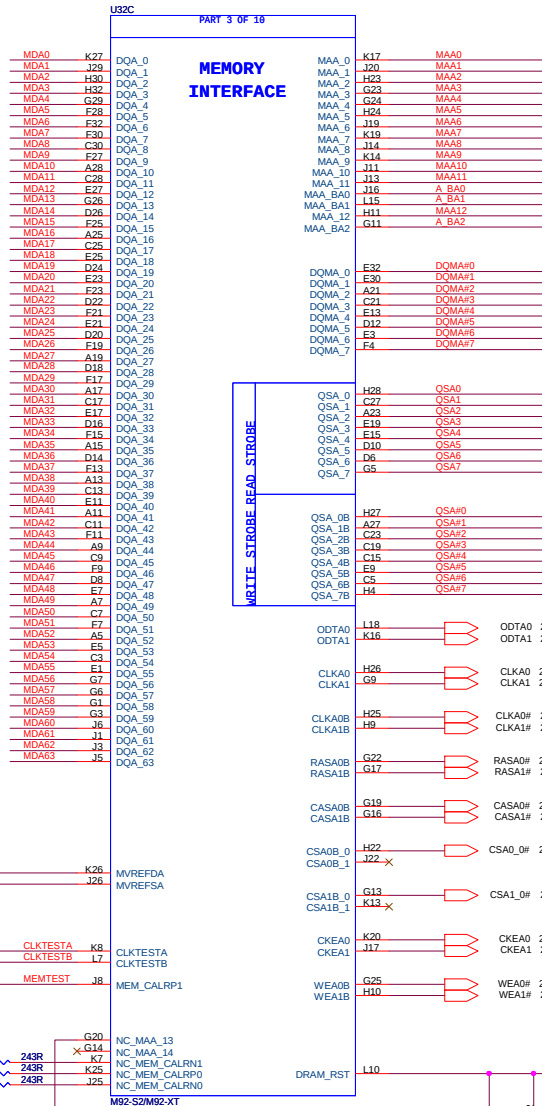
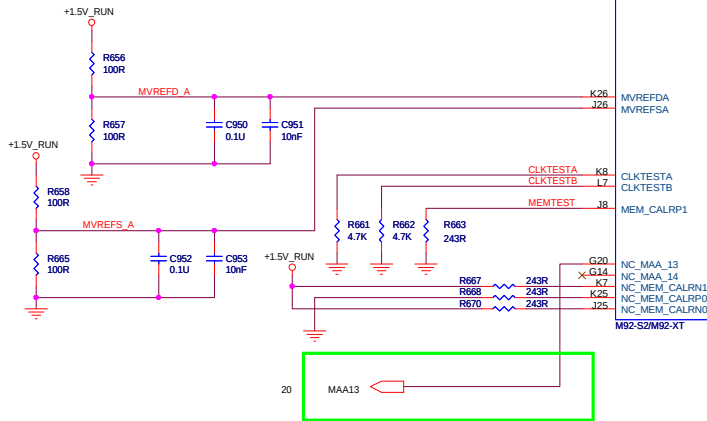


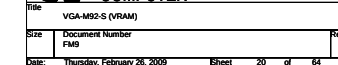


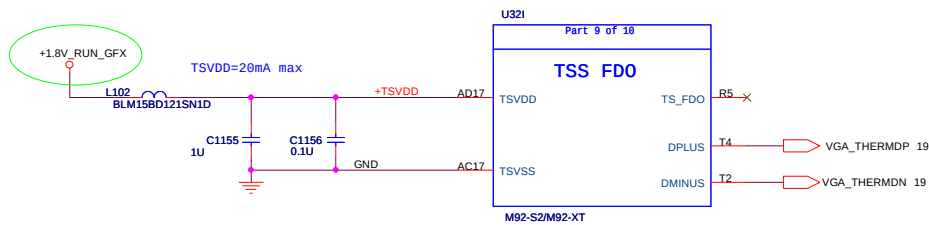
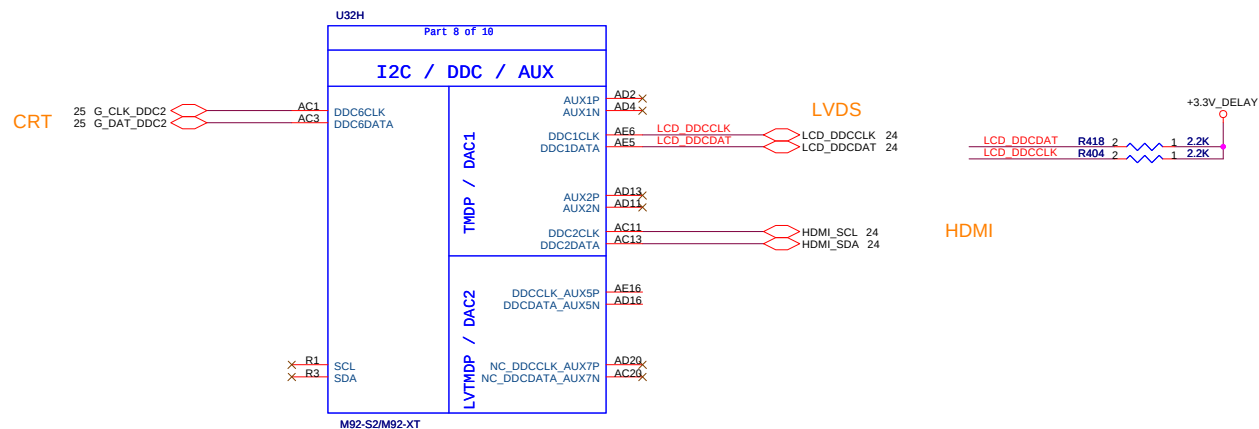
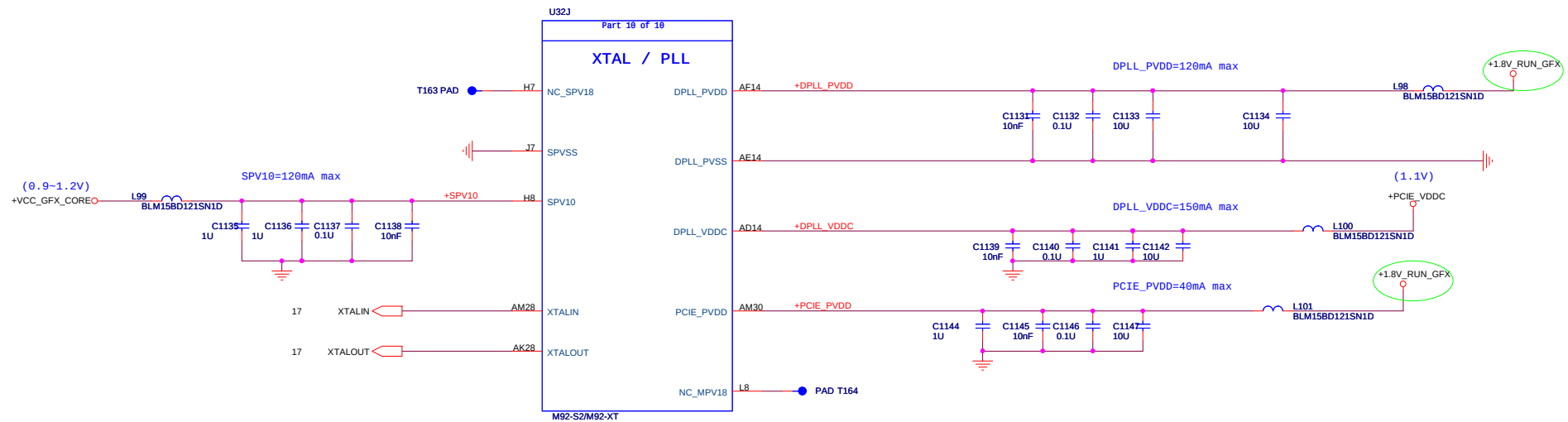
MEMORY INTERFACE



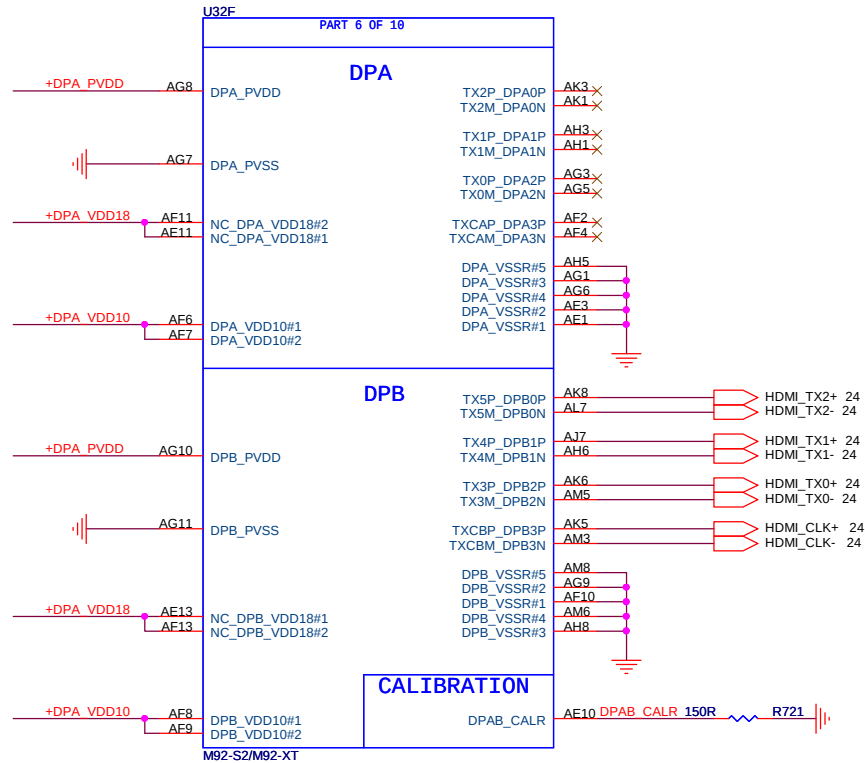
DIVIDER RESISTORS	DDR3
MVREF TO 1.5V	100R
MVREF TO GND	100R



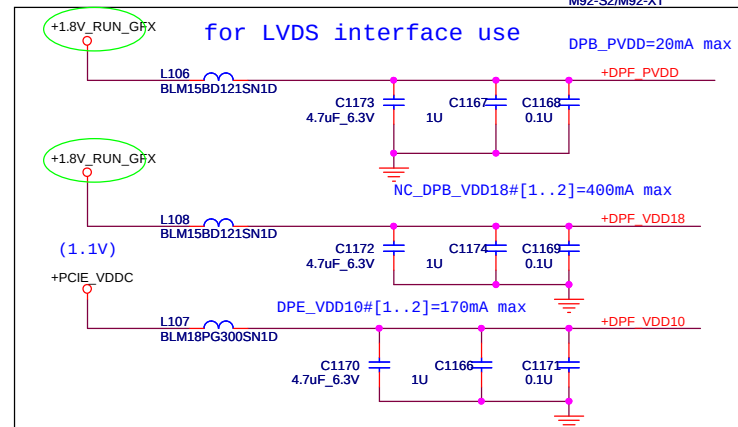
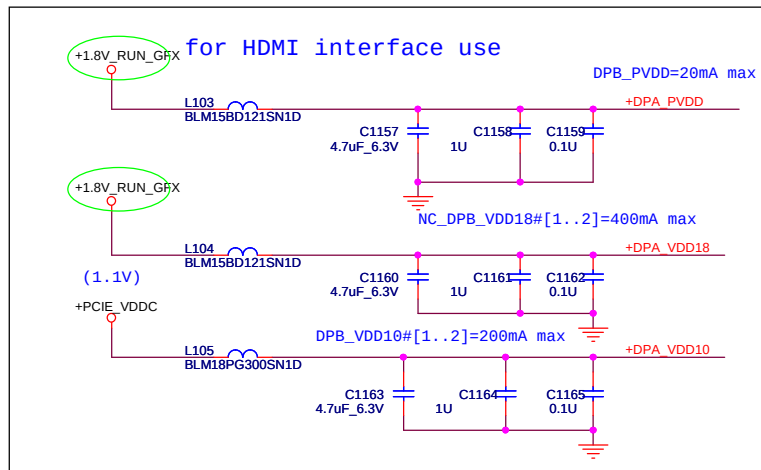
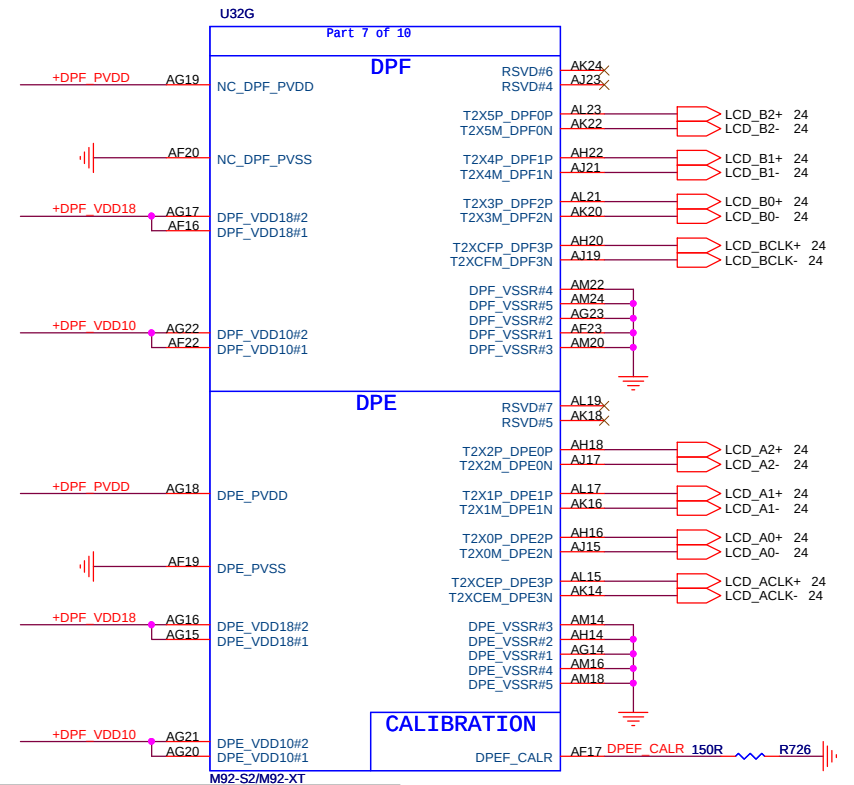




TMDP(HDMI) INTERFACE



LVDS INTERFACE



Title		
VGA-M92-XT (PCIe)		
Size	Document Number	Rev
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Date:	Thursday, February 26, 2009	Sheet 22 of 64



Title

VGA-M82-S (PCIe)

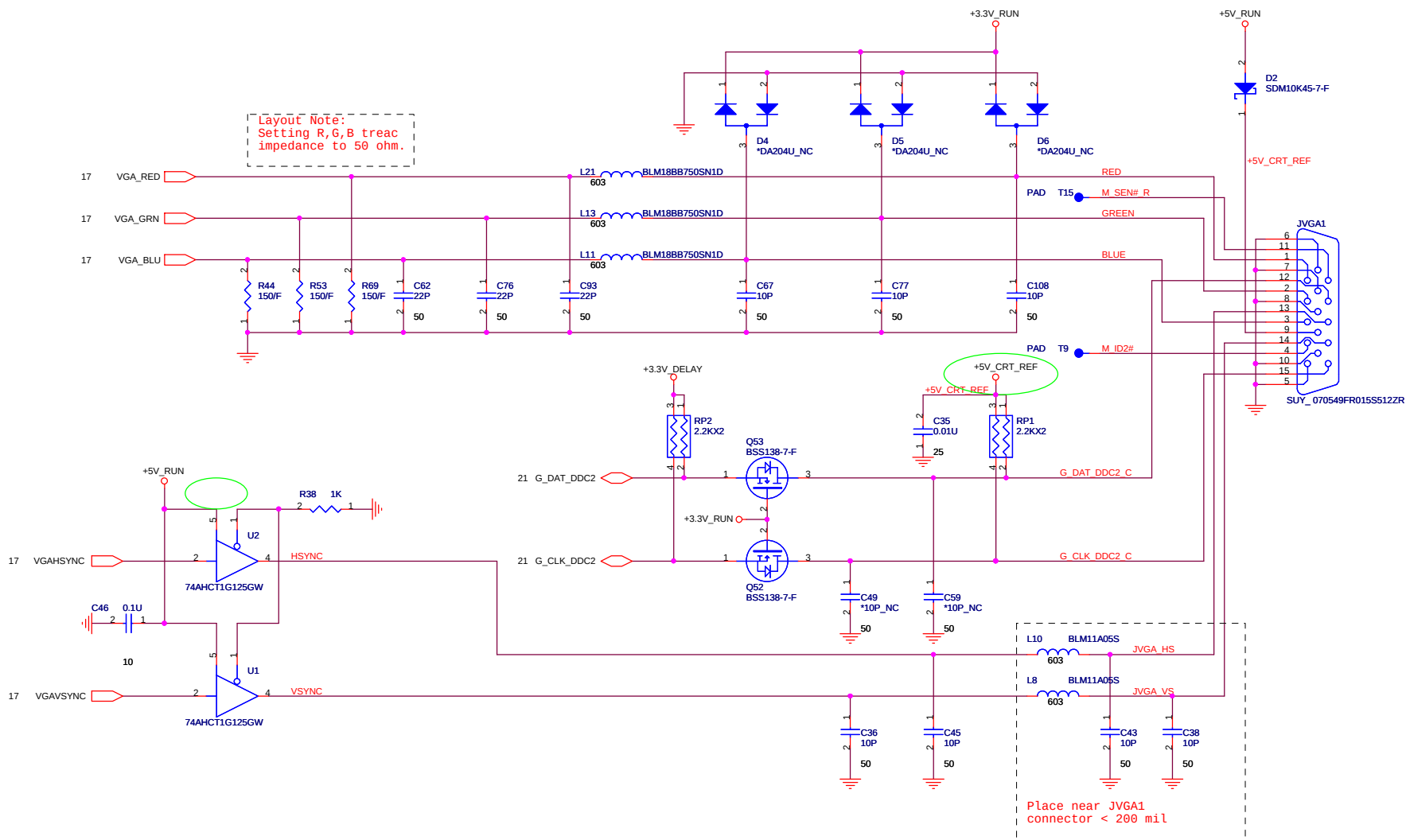
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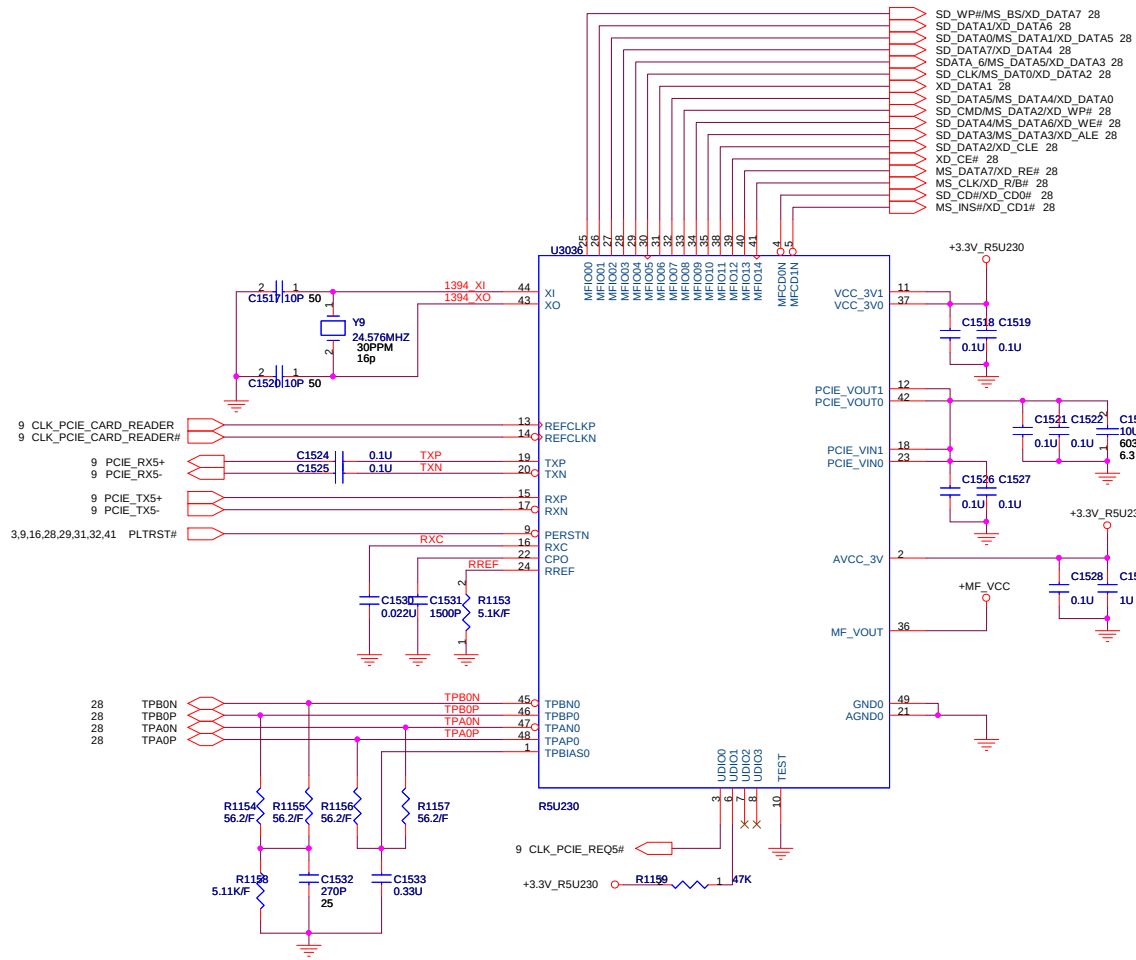
Document Number FM9

Rev	1A
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Date: Thursday, February 26, 2009

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MFIO Pin Assignment Table

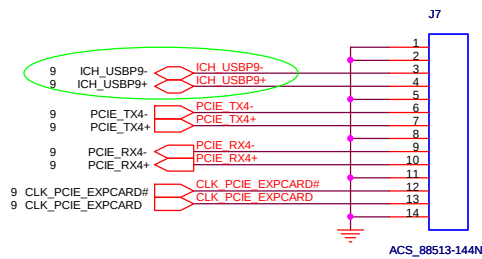
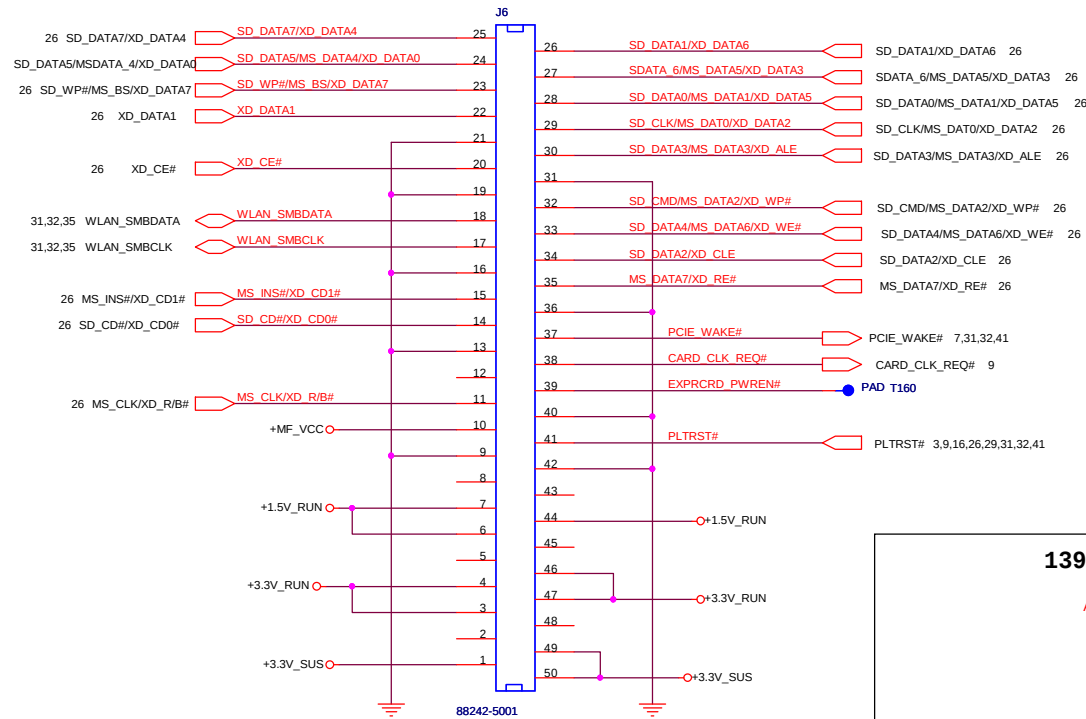
MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	CLK	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	CLK	R/B#



	A	B	C	D	E
1					
2					
3					
4					

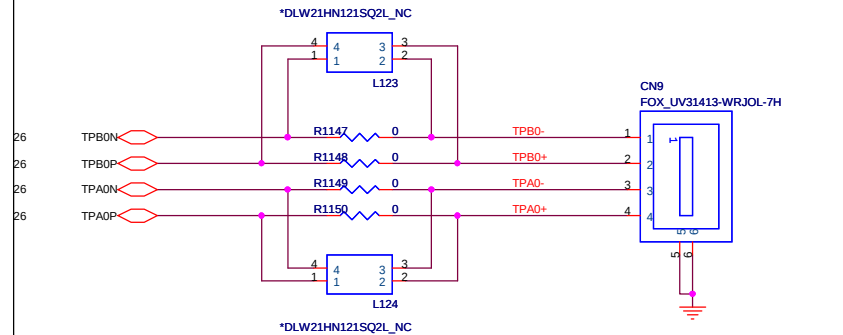
 QUANTA COMPUTER		
Title IEEE 1394		
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009		
Sheet 27 of 64		

Express Card/CARD READER



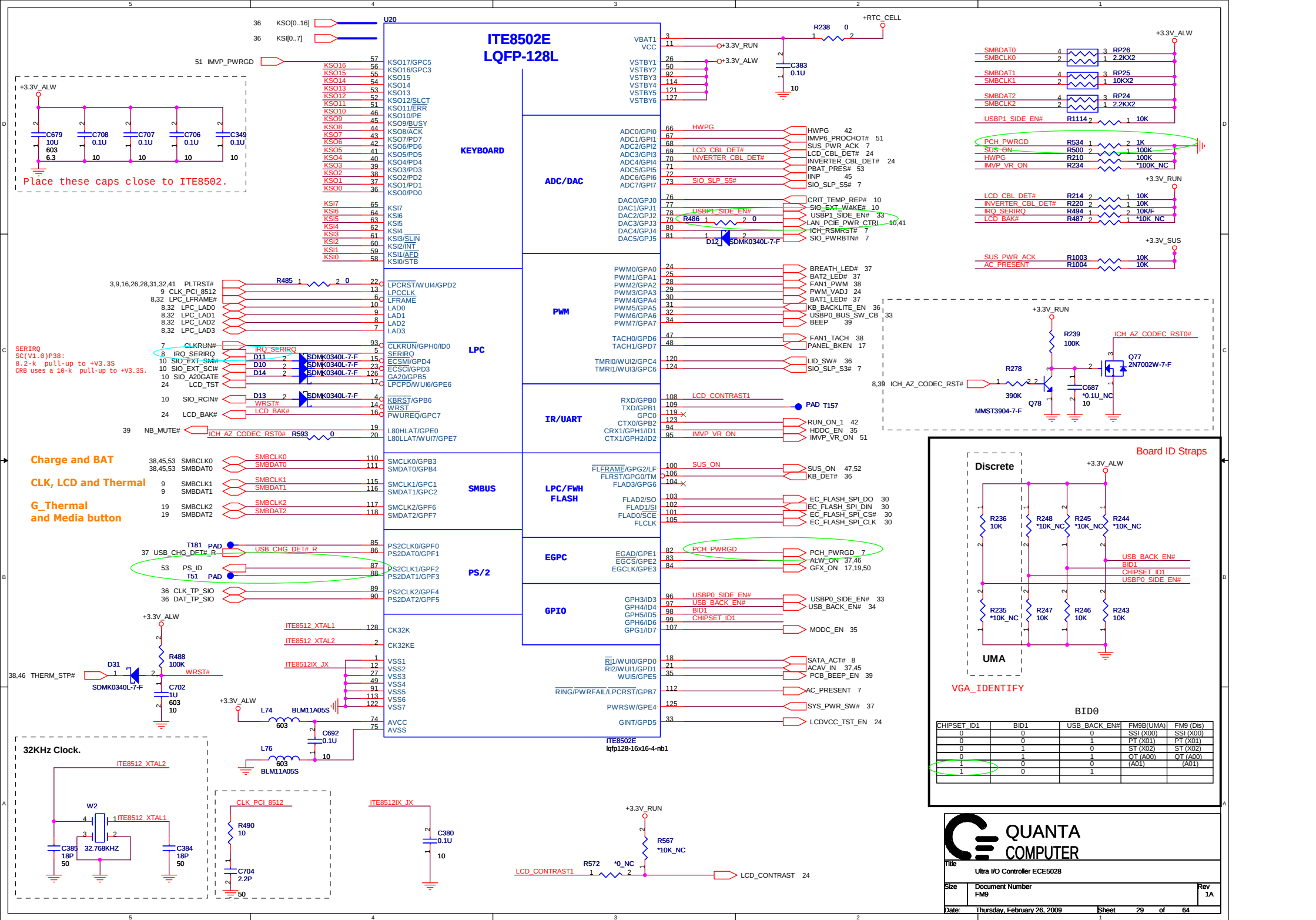
1394 CONNECTOR

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

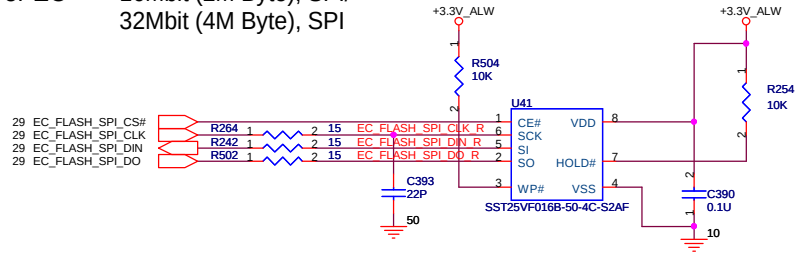


*TPA0P/TPA0N, TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N, TPB0P/TPB0N pair trace : Same length electrically.

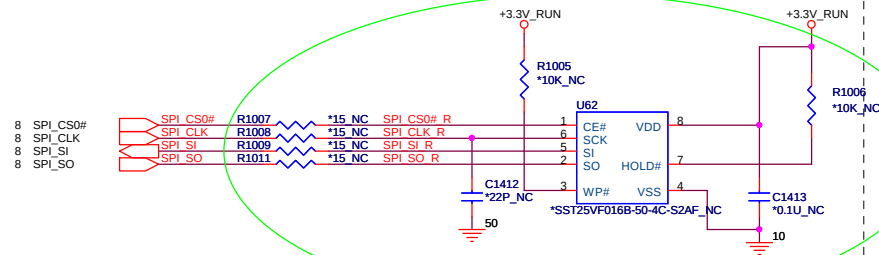




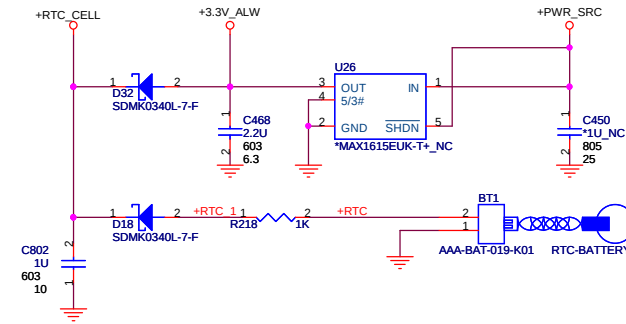
For EC 16Mbit (2M Byte), SPI/
32Mbit (4M Byte), SPI



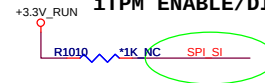
For PCH 16Mbit (2M Byte), SPI/
32Mbit (4M Byte), SPI



RTC BATTERY



iTPM ENABLE/DISABLE



TPM Function	R712
Enable	Mount
Disable	NC (Default)



Title Ultra I/O Controller ECE5028

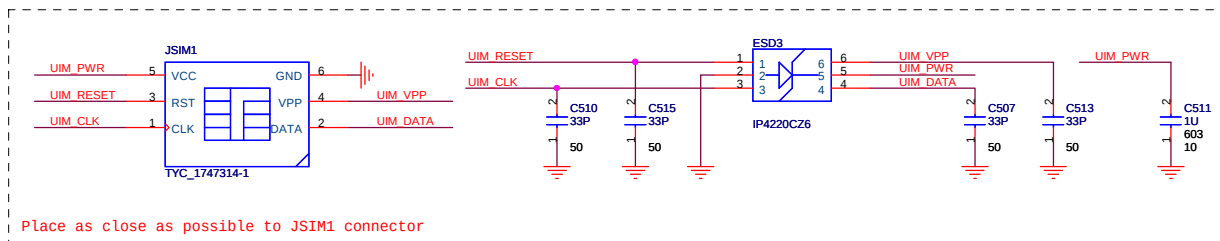
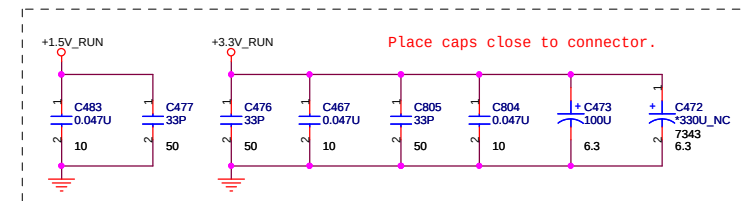
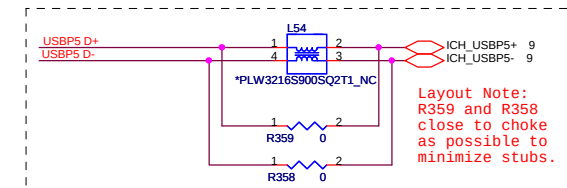
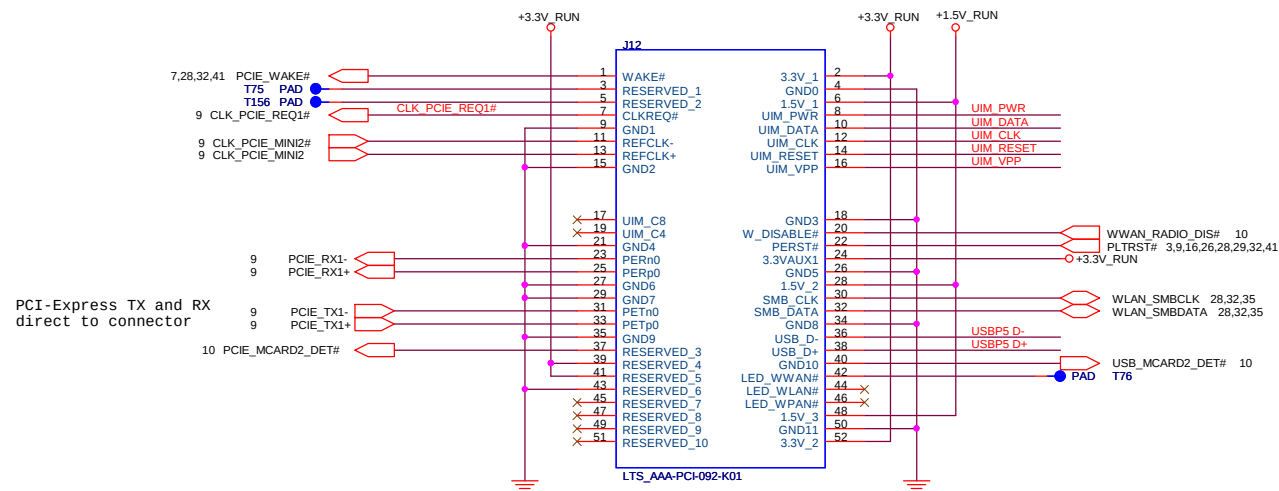
Size Document Number FM9

Date: Thursday, February 26, 2009

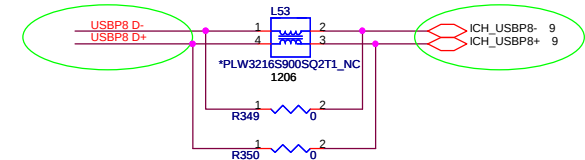
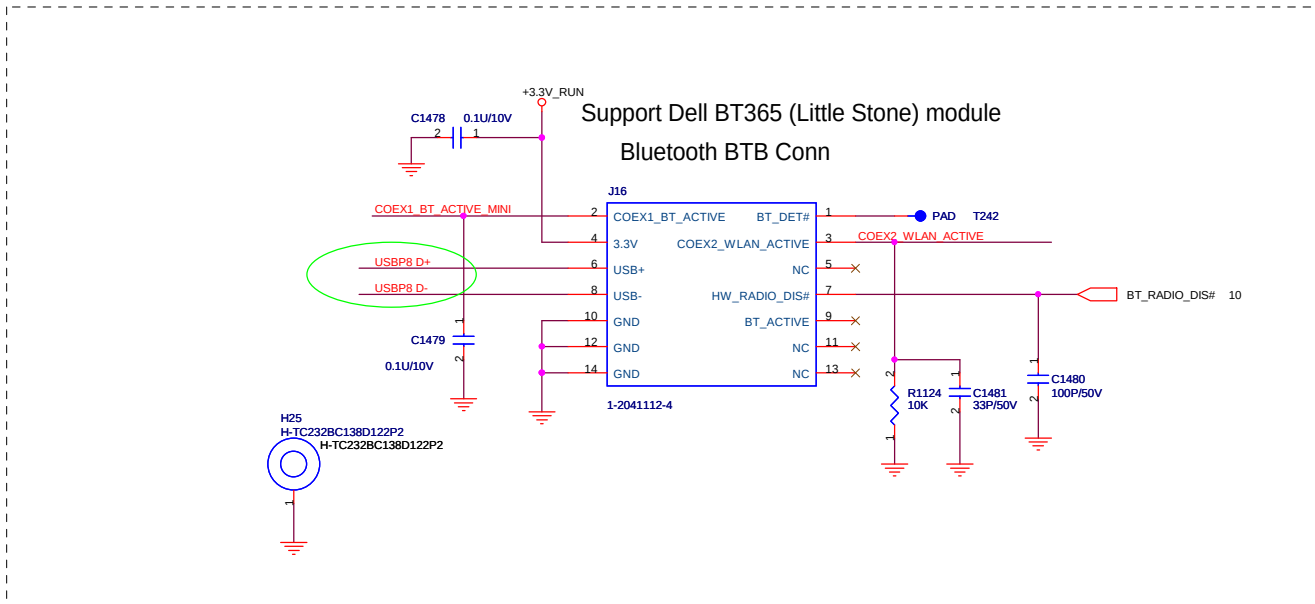
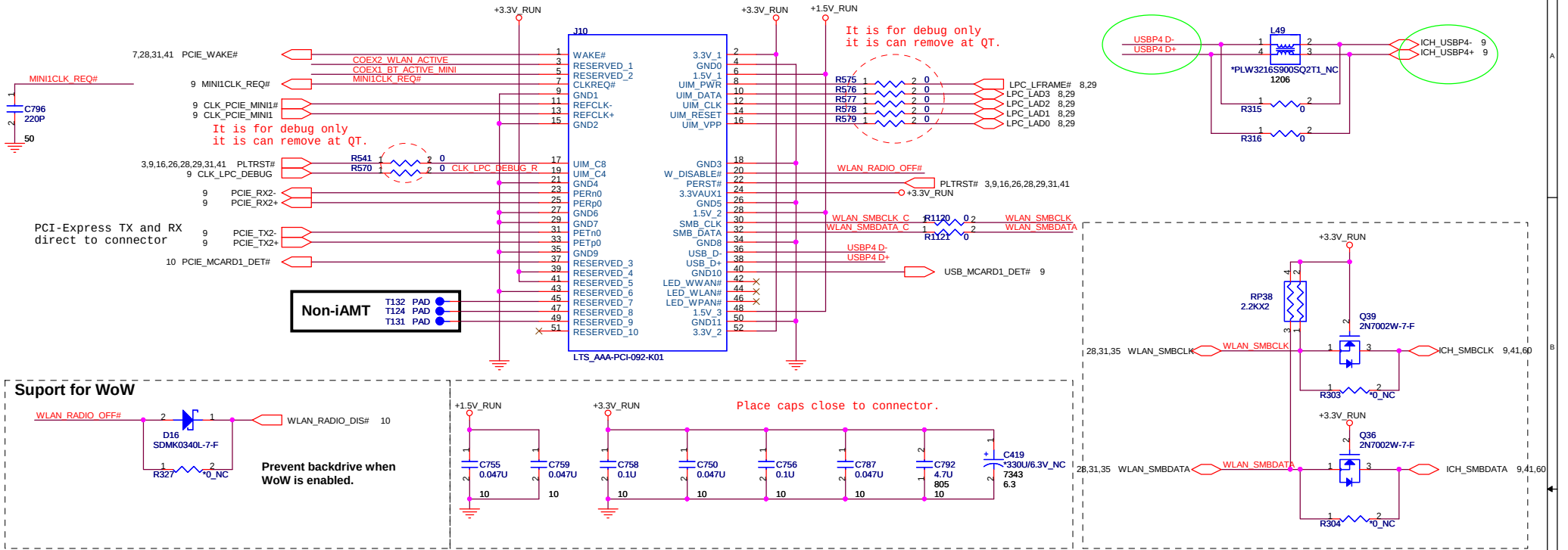
Sheet 30 of 64

Rev 1A

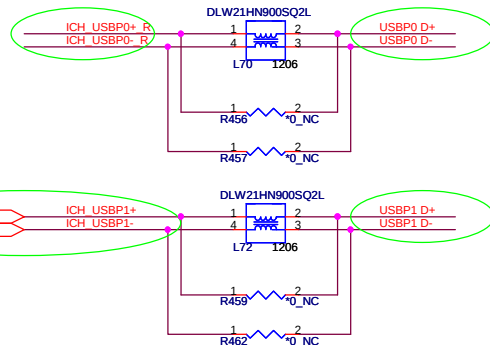
MiniCard WWAN connector



MiniCard WLAN connector

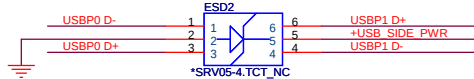


External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



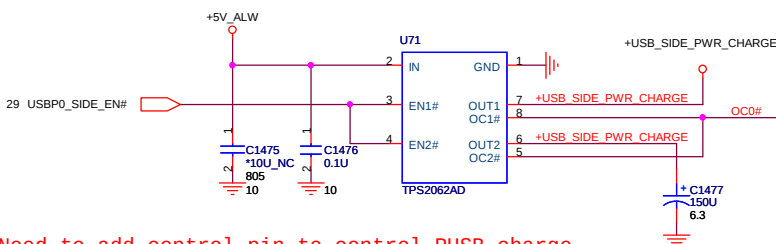
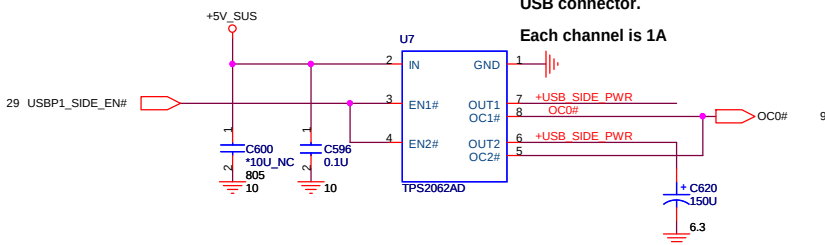
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



Place one 150uF cap by each USB connector.

Each channel is 1A

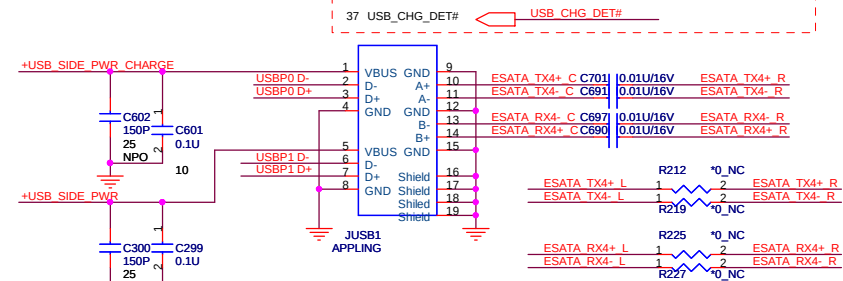


Need to add control pin to control PUBS charge

Support USBP1 charge function.
JUSB1 need to add USB_CHG_DET# pin wire to EC GPIO to detect USB device.

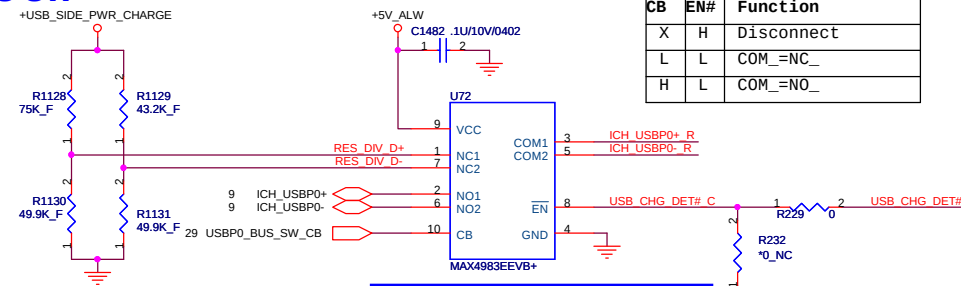
Side External USBX2

For USP1 USB PWR CHARGE, JUSB1 need add USB_CHG_DET#



Please put those on the same side of MB PCB
USBx2 & ESATA COMBO & PWR CHARGE

USB BUS SW



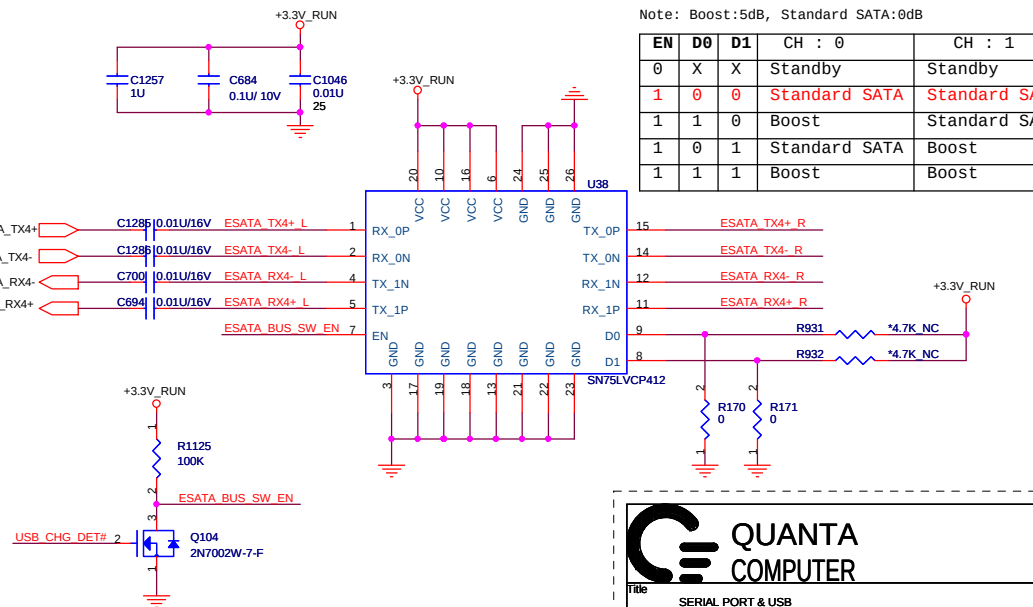
(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

CB	EN#	Function
X	H	Disconnect
L	L	COM_=NC_
H	L	COM_=NO_

E-SATA Re-driver

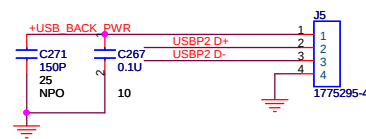
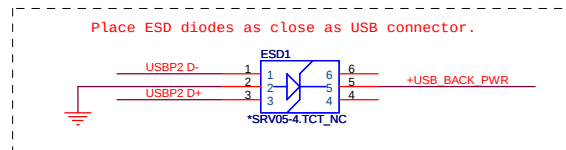
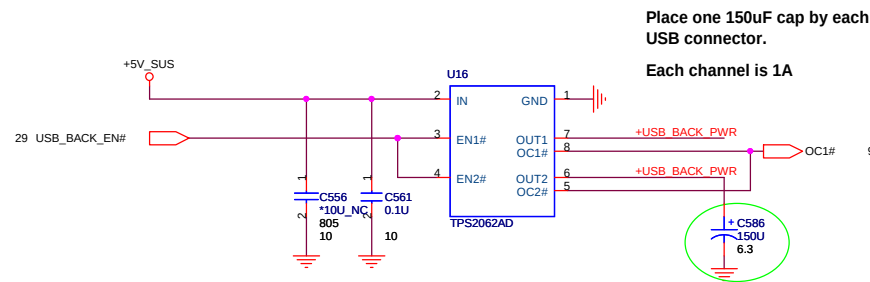
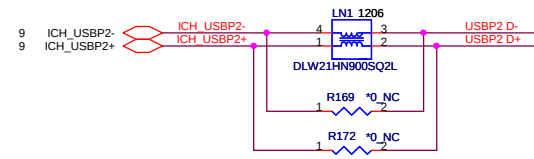
Please put those on the same side of MB PCB

Note: Boost:5dB, Standard SATA:0dB

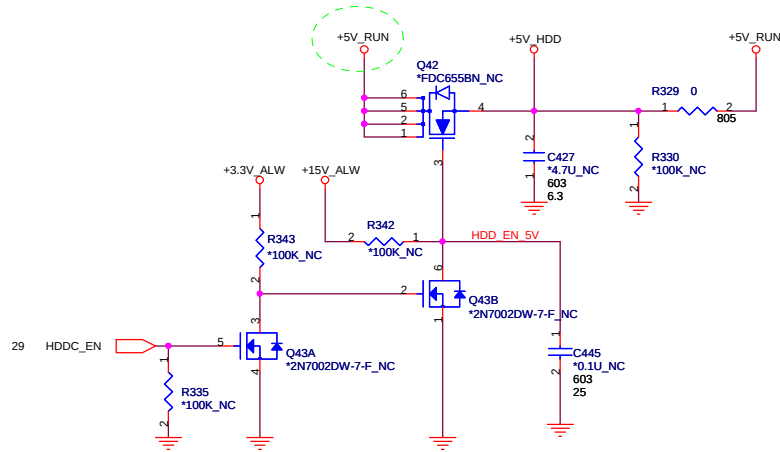
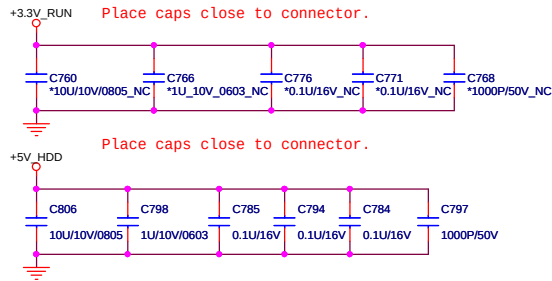
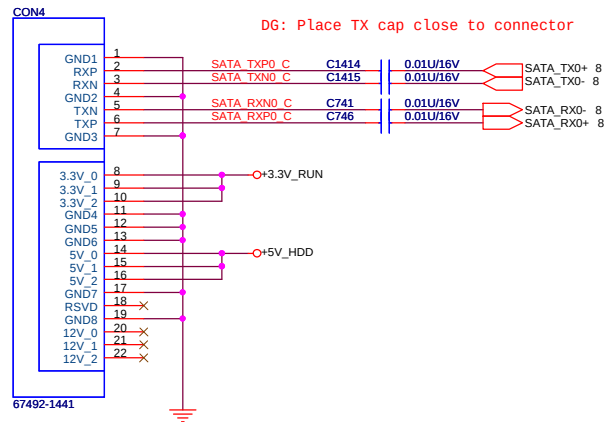


EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

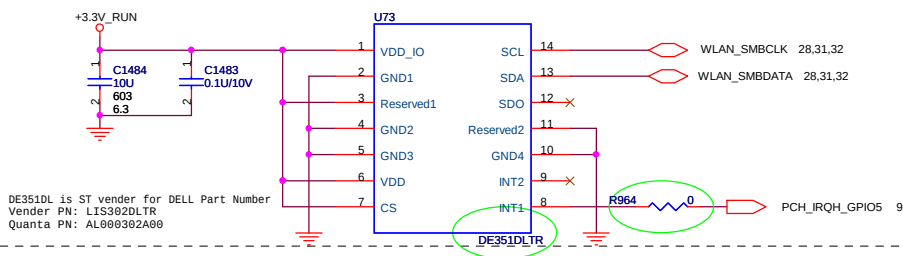




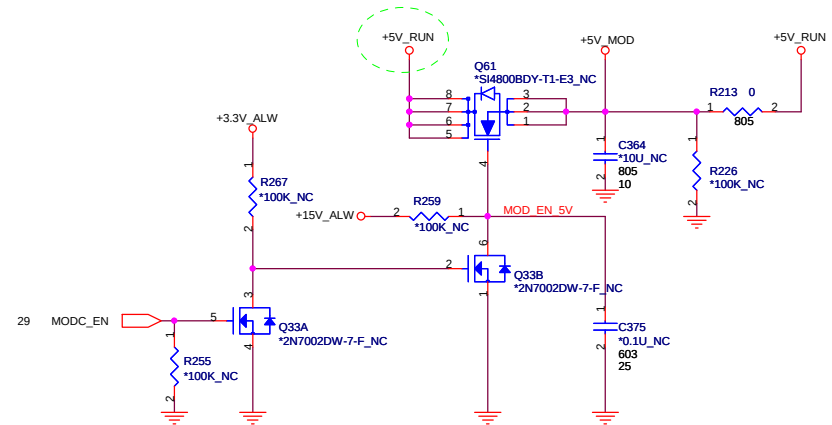
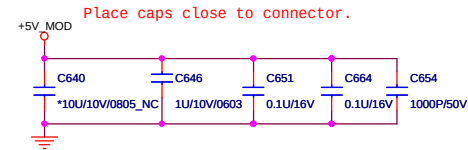
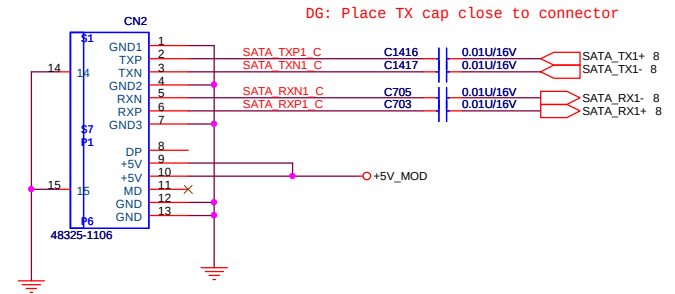
SATA Connector.



3-axis Fall Sensor (HDD data protector)

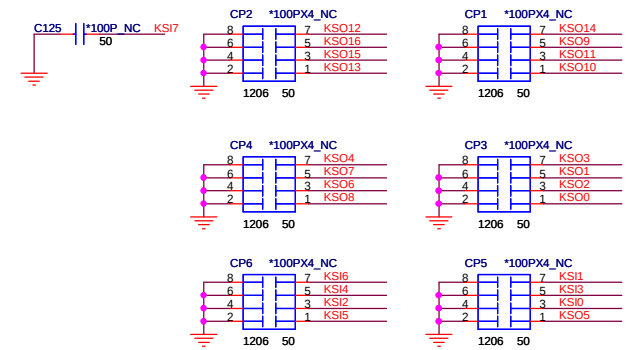
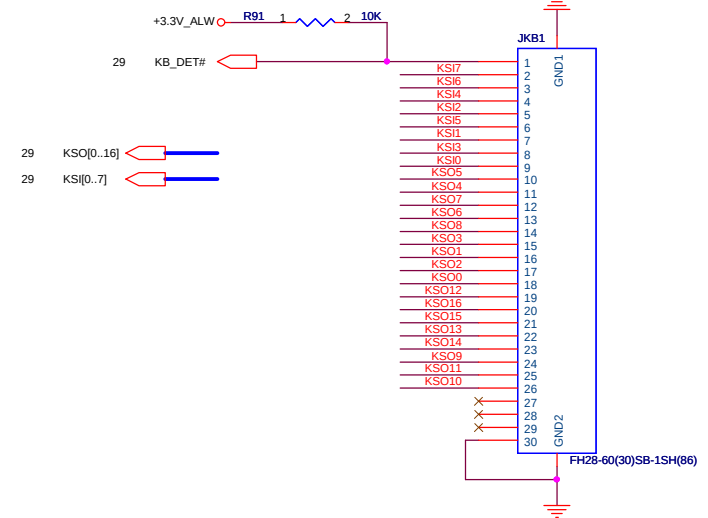


ODD Connector



Title			SATA (HDD&CD_ROM)
Size	Document Number	Rev	
	FMR	1A	
Date:	Thursday, February 26, 2009	Sheet	35 of 64

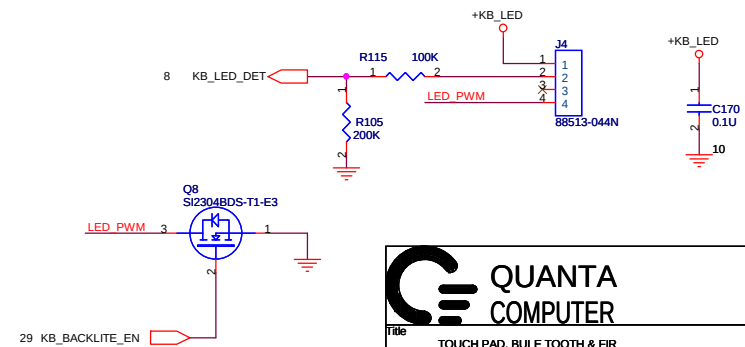
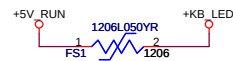
KEYBOARD CONNECTOR



100P CAPS CLOSE TO JKB1

Key board illumination

+KB_LED power trace width >10 mil



Title TOUCH PAD, BULE TOOTH & FIR

Size Document Number FM9

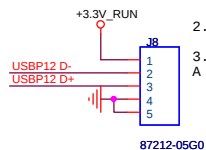
Rev 1A

Date: Thursday, February 26, 2009

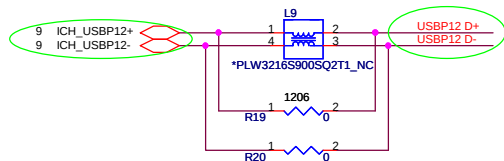
Sheet 36 of 64

Touch Screen Module

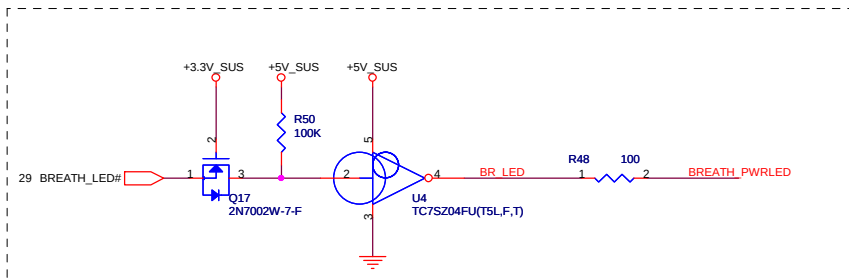
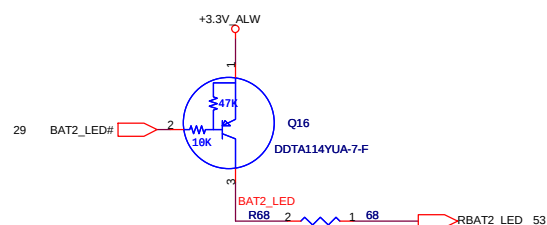
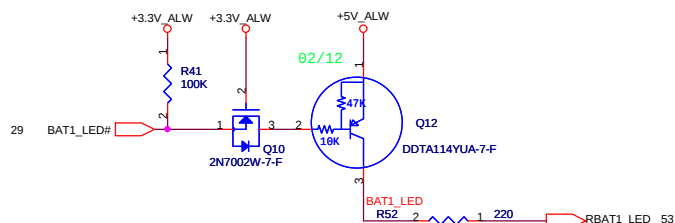
- Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
 2. Maximum cable resistance on VCC, GND should be 150m ohm.
 3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.



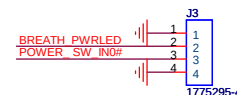
Need check the connector footprint and symbol.



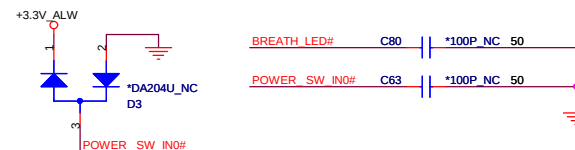
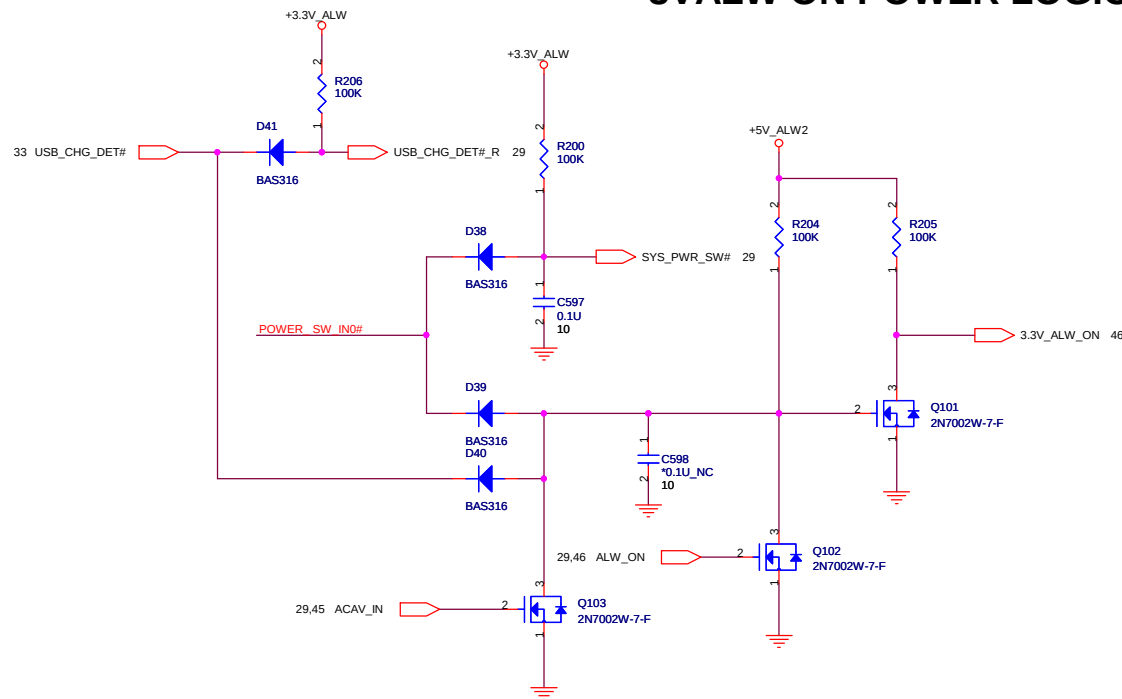
Battery status.



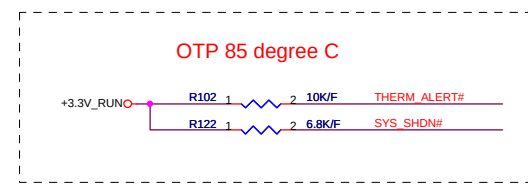
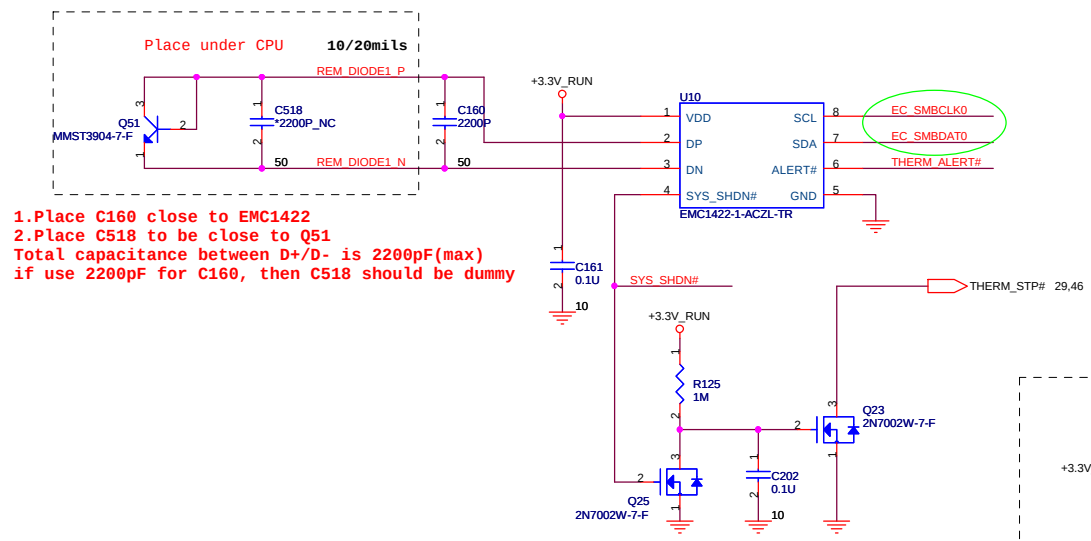
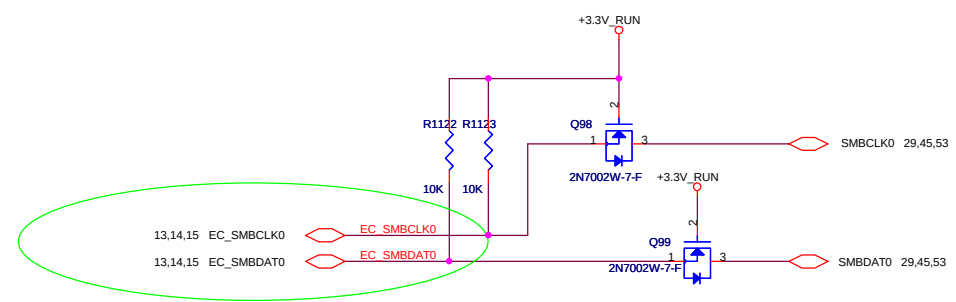
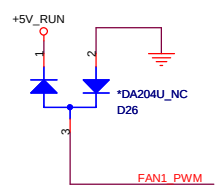
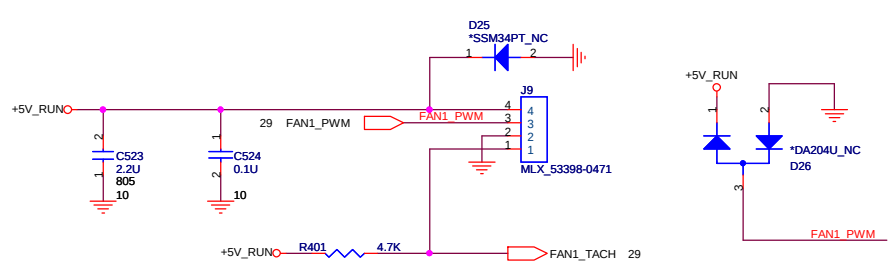
Power button Cable

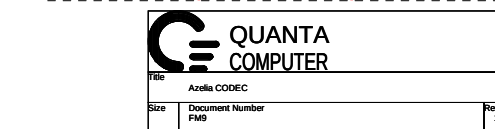
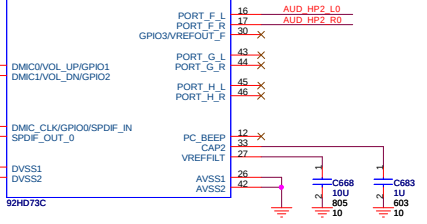
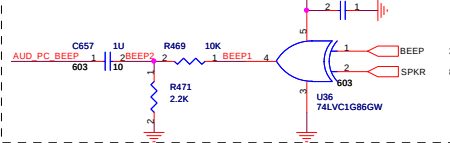
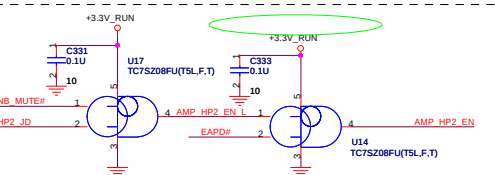
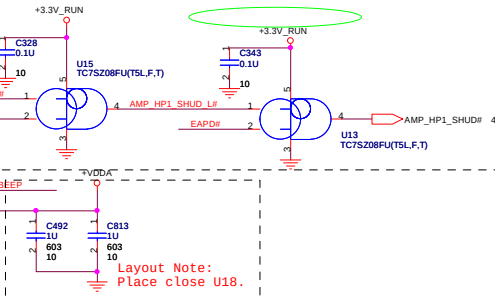
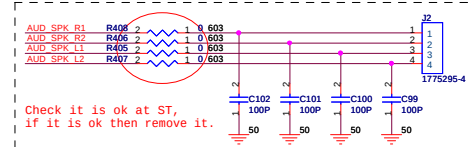


3VALW ON POWER LOGIC

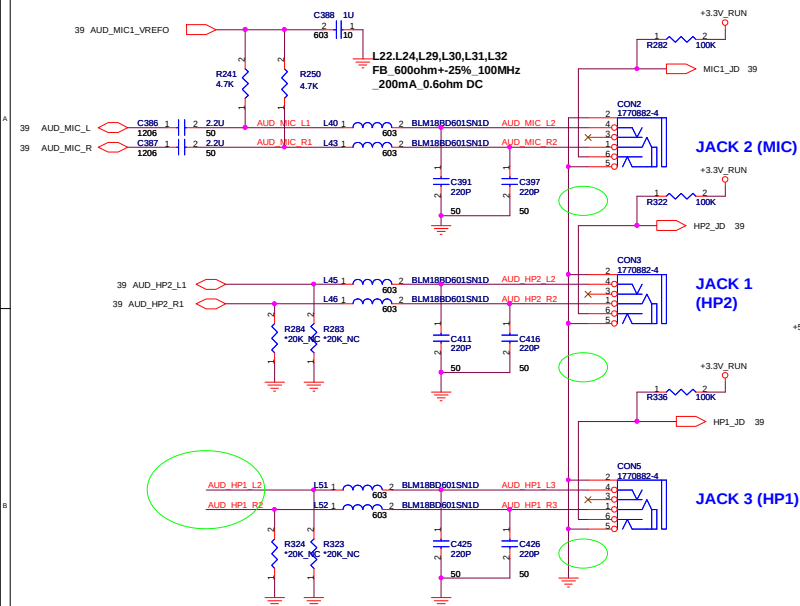


QUANTA COMPUTER		
Title SWITCH, KEYBOARD & LED&Touch Screen Module		
Size	Document Number FM9	Rev 1A
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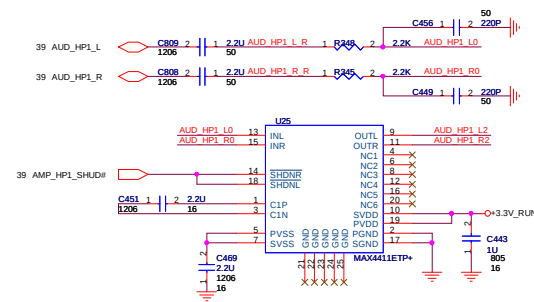
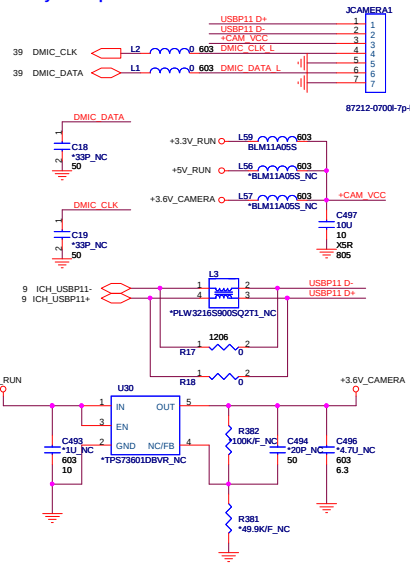




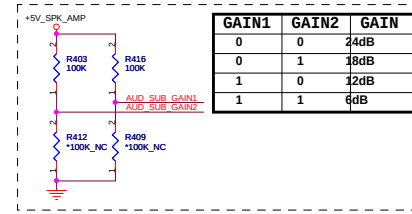
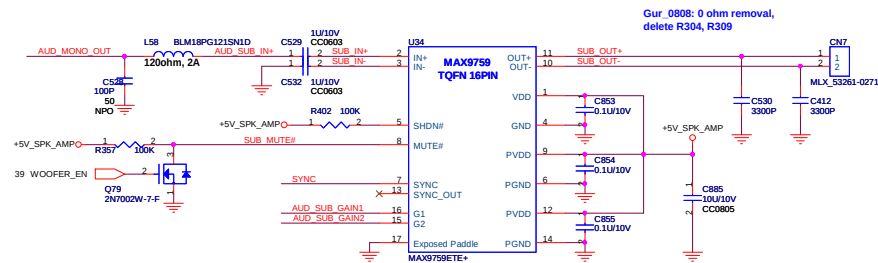
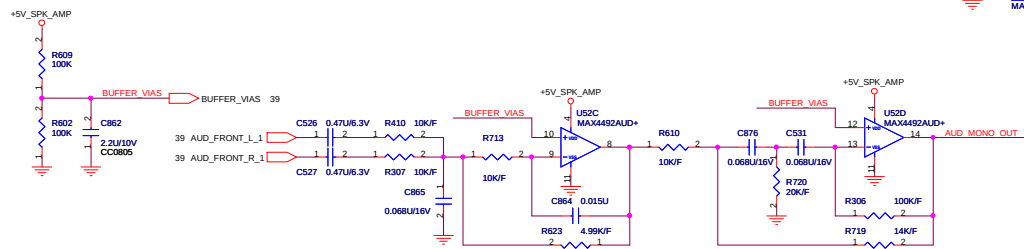
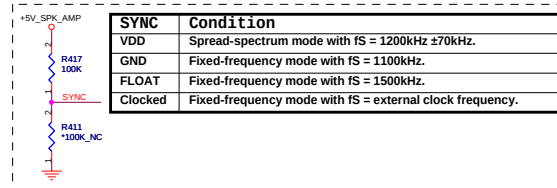
Headphone Jack
Stereo MIC Jack

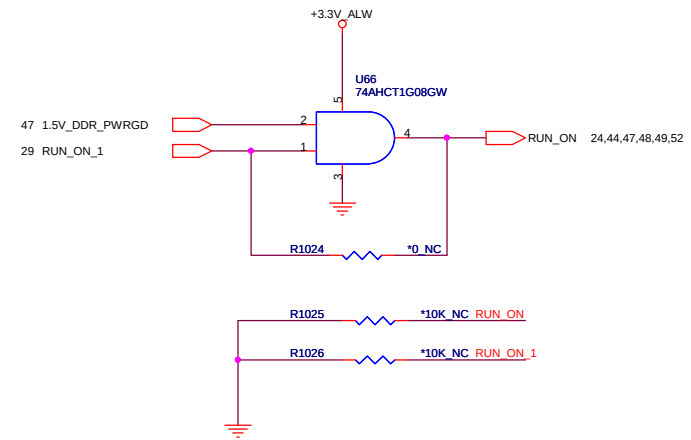
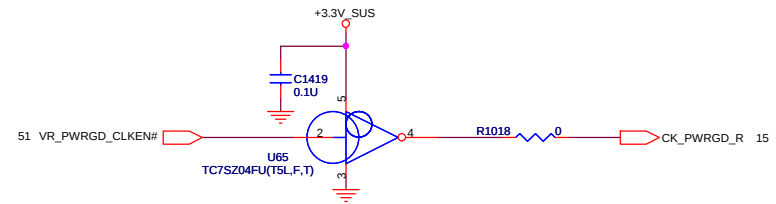


Array Microphone & Camera



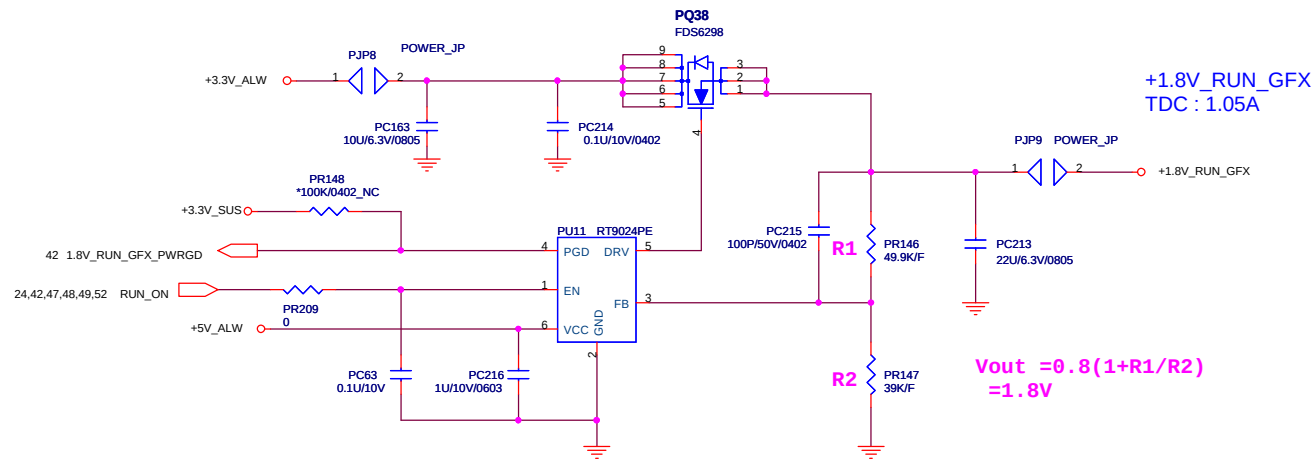
INTERNAL SUBWOOFER AMP



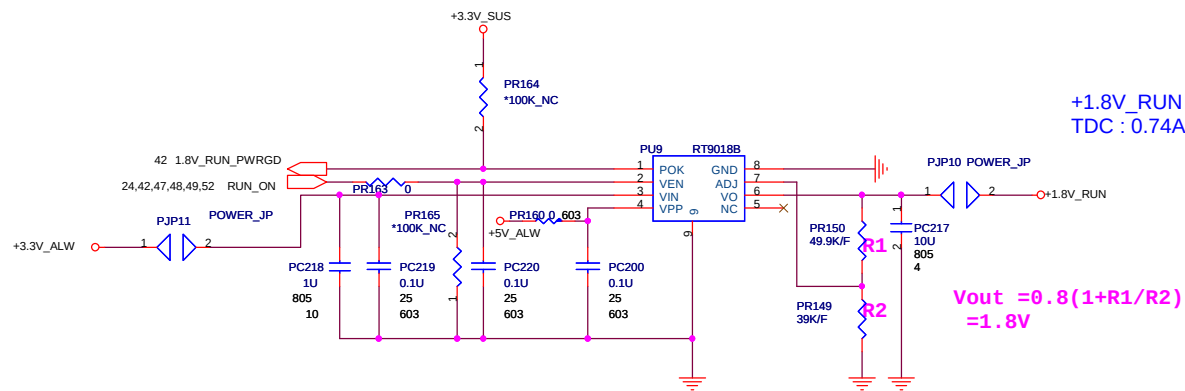


	1	2	3	4	5
A					
B					
C					
D					

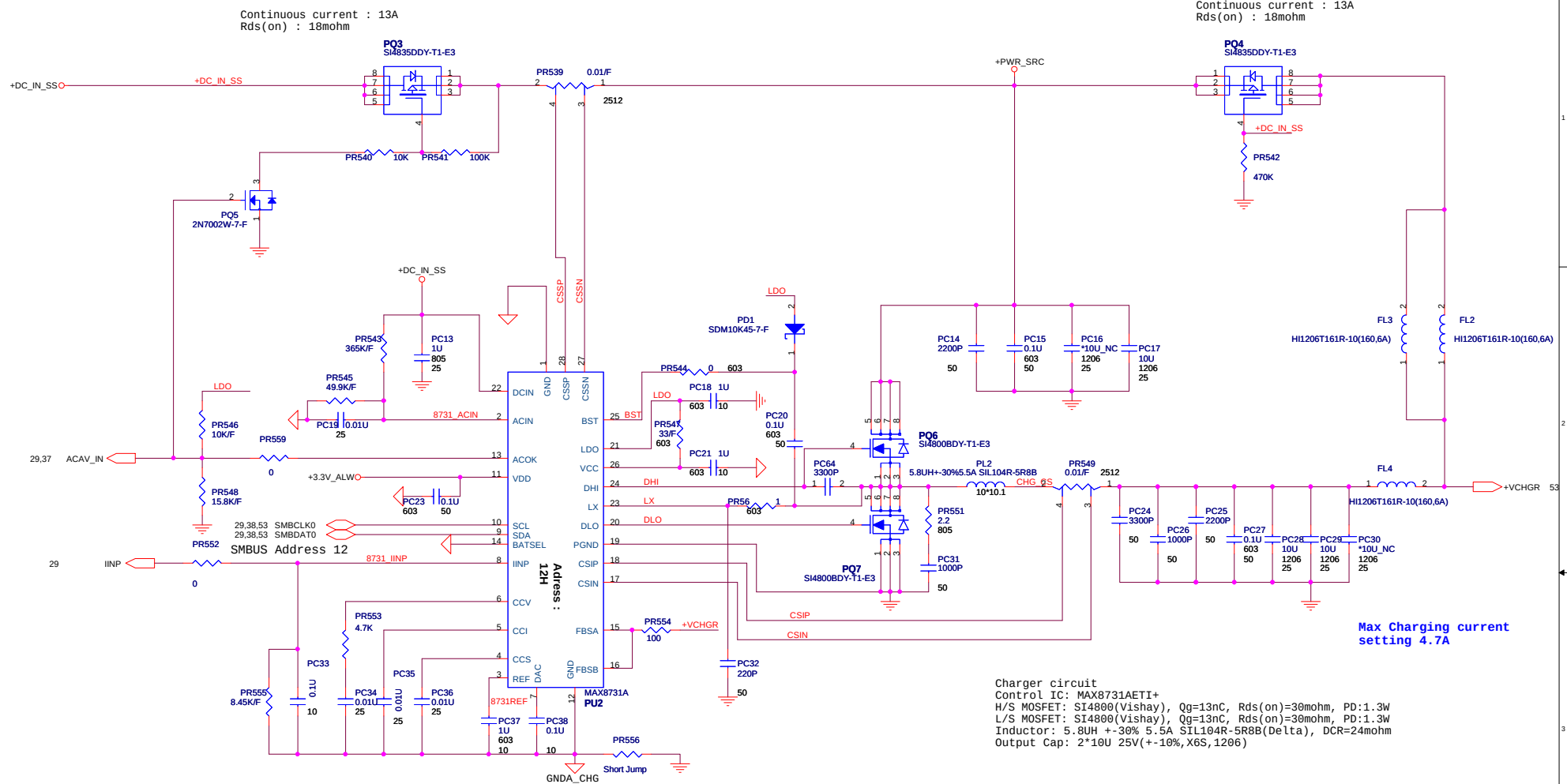
 QUANTA COMPUTER			
Title Battery Selector			
Size	Document Number FM9		Rev 1A
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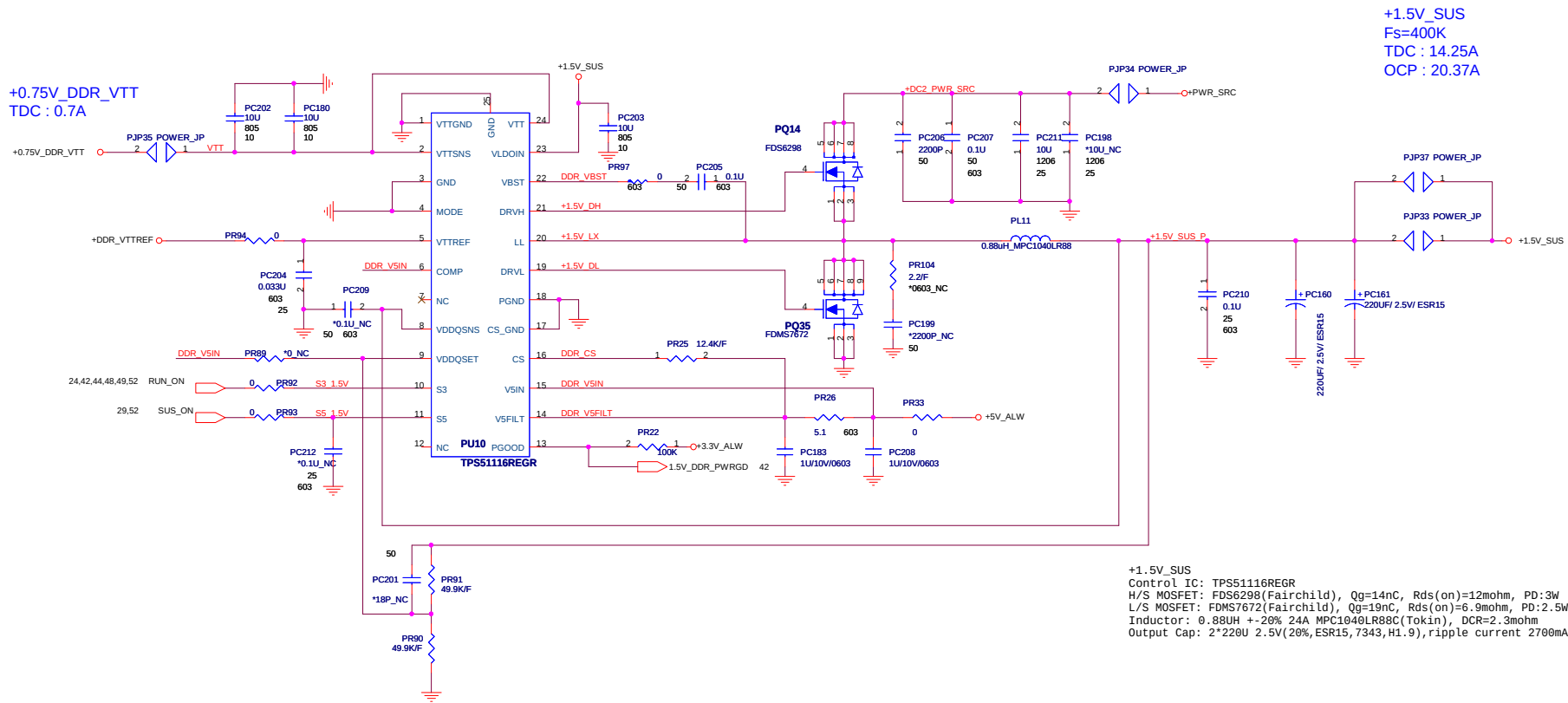


+1.8V_RUN_GFX for VGA 1.8V
+1.8V_RUN for CPU and PCH 1.8V



Title		
+1.8V_RUN_GFX (RT9024PE) & +1.8V_RUN(RT9018B)		
Size	Document Number	Rev
FM9		1A
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VDDQ and VTT discharge control

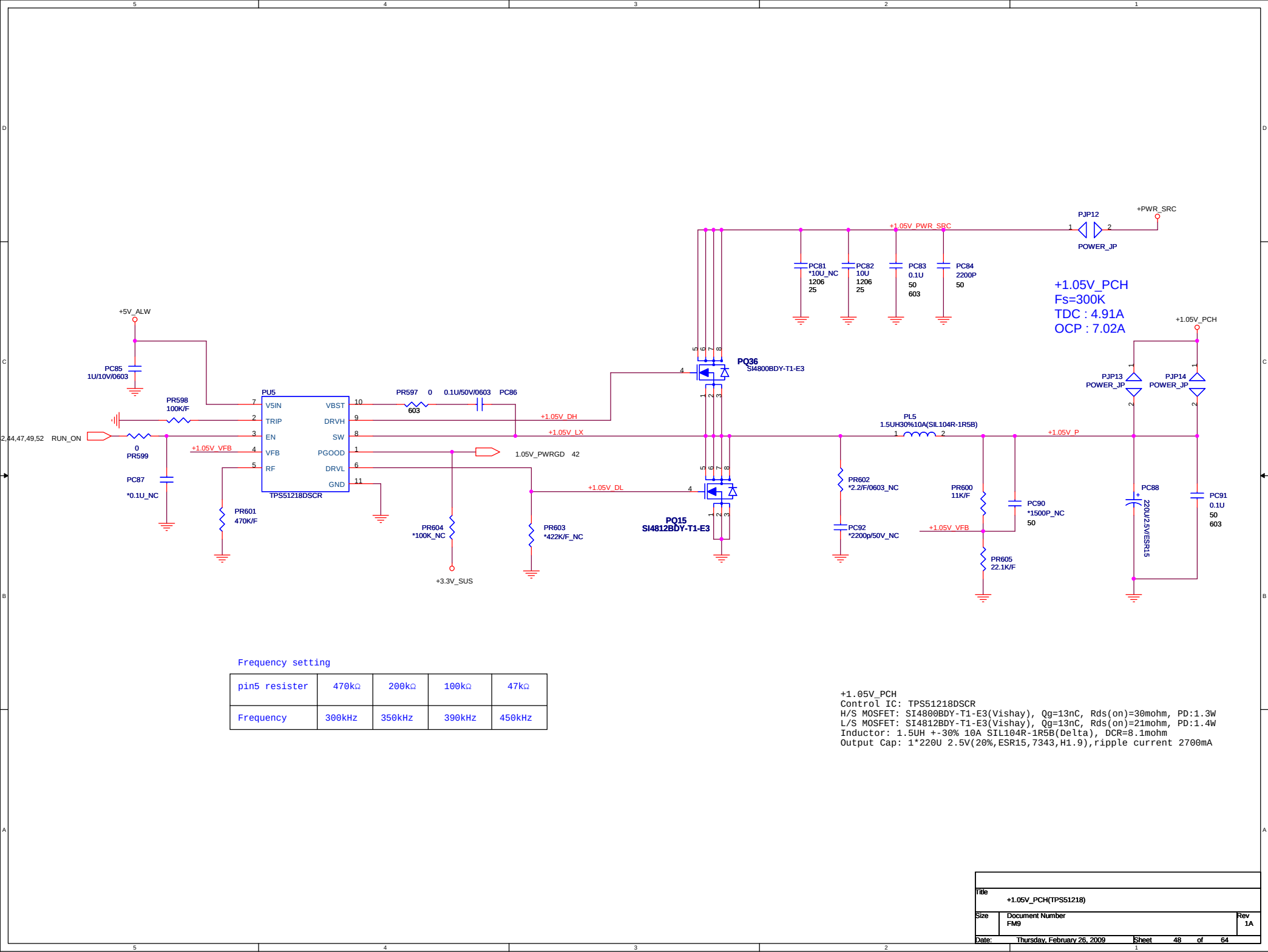
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

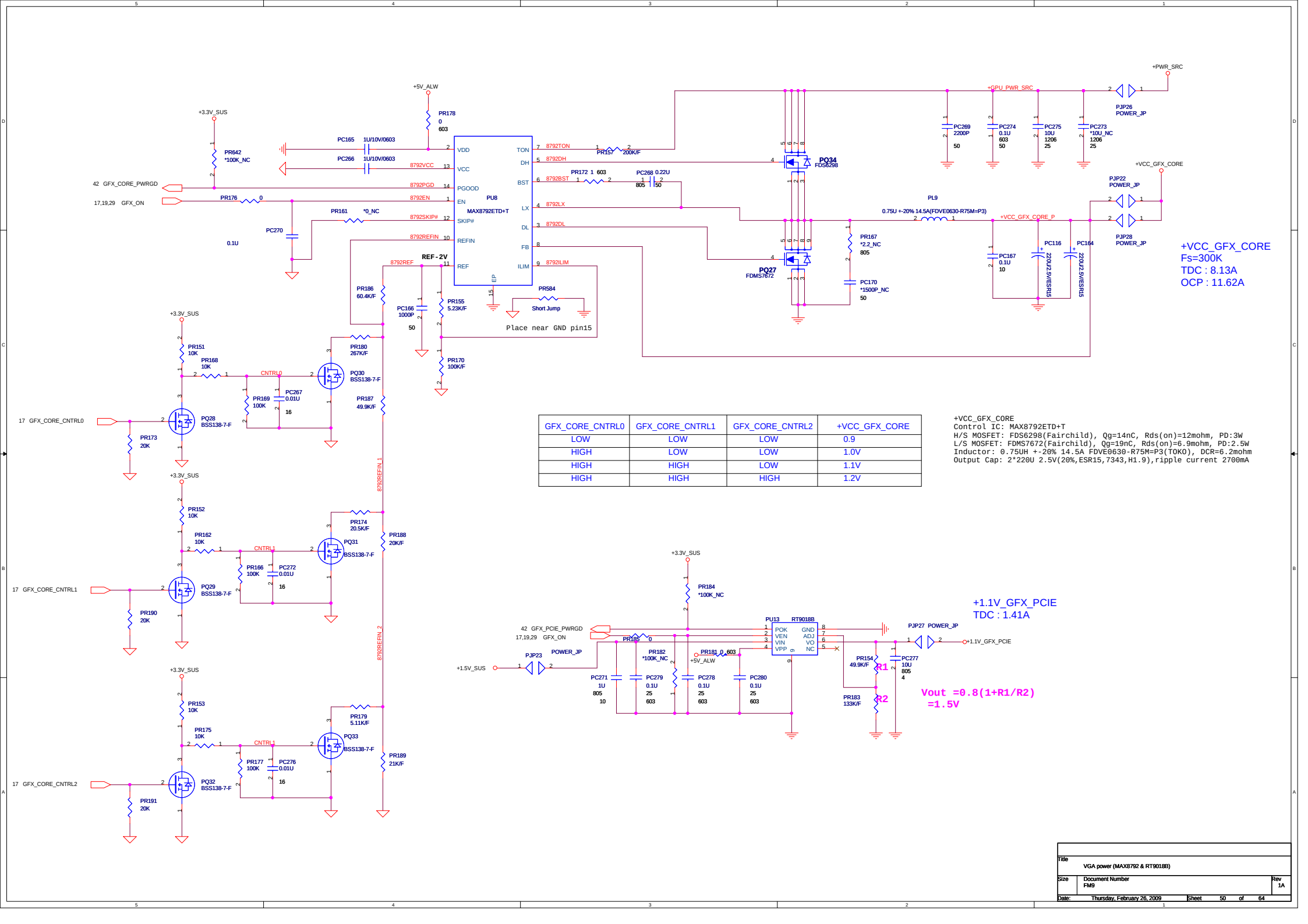
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	2.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	L0	HI	On	On	Off (Hi-Z)
S4/S5	L0	L0	On (discharge)	Off (discharge)	Off (discharge)



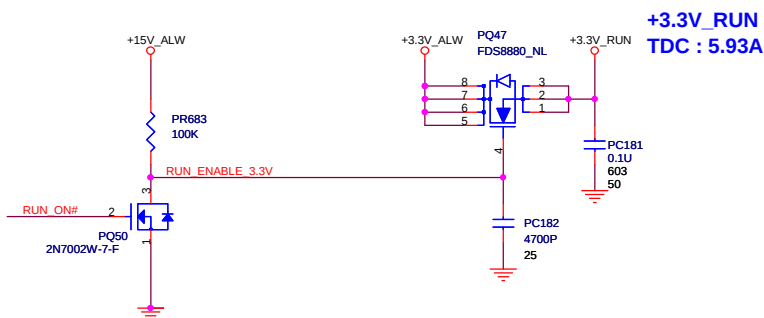
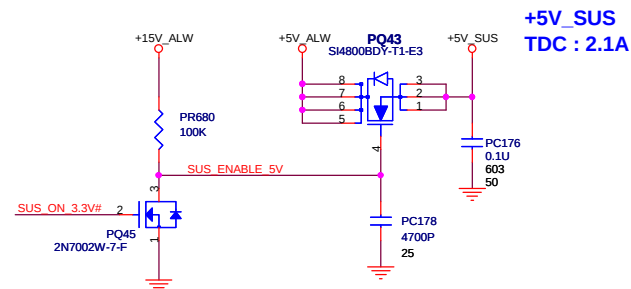
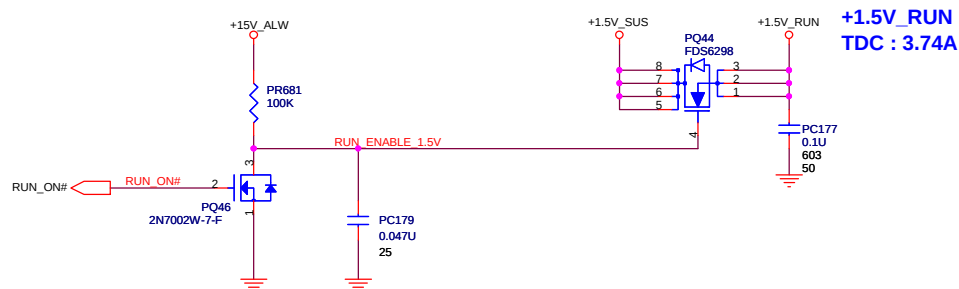
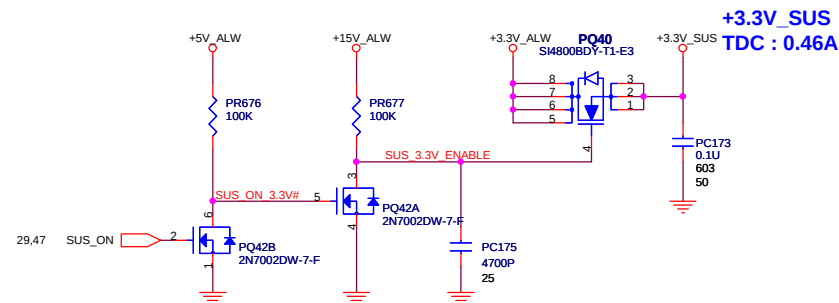
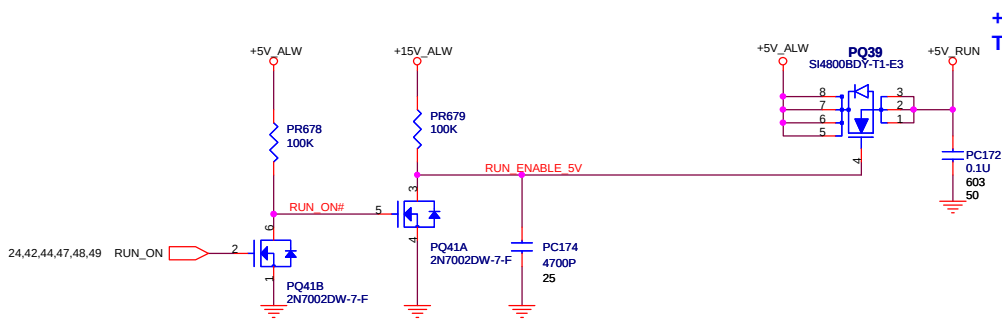


GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	GFX_CORE_CNTRL2	+VCC_GFX_CORE
LOW	LOW	LOW	0.9
HIGH	LOW	LOW	1.0V
HIGH	HIGH	LOW	1.1V
HIGH	HIGH	HIGH	1.2V

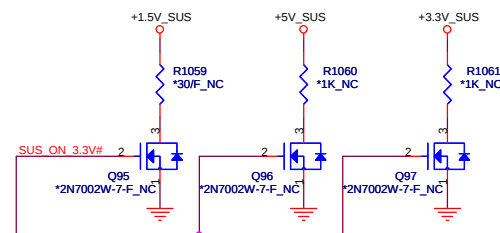
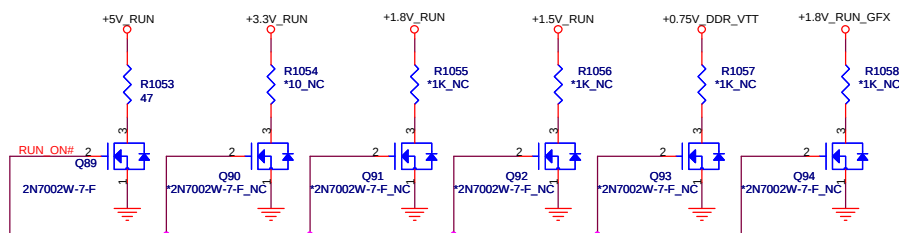
+VCC_GFX_CORE
Control IC: MAX8792ETD+T
H/S MOSFET: FDS6298(Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
L/S MOSFET: FDS7672(Fairchild), Qg=19nC, Rds(on)=6.9mohm, PD:2.5W
Inductor: 0.75uH +20% 14.5A(FDVE0630-R75M=P3(TOKO), DCR=6.2mohm
Output Cap: 2*220u 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

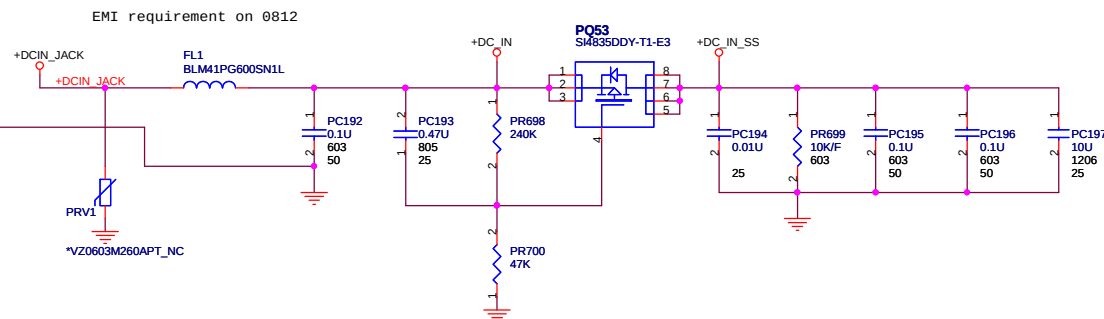
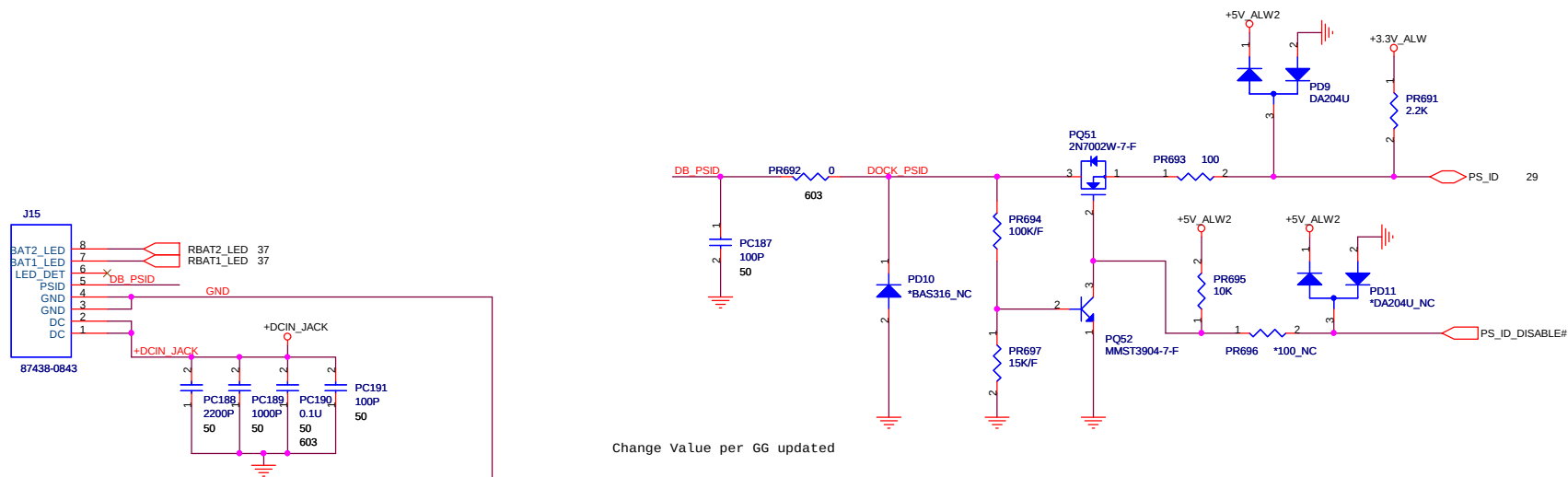
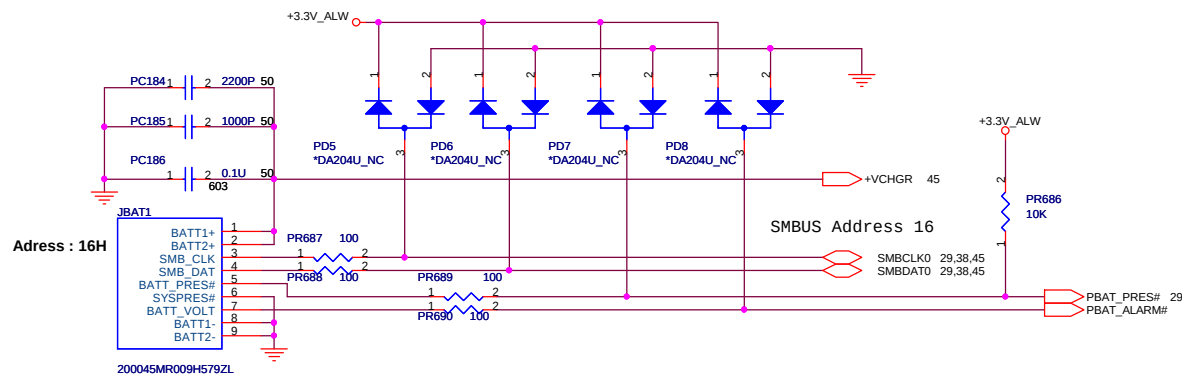
+1.1V_GFX_PCIE
TDC : 1.41A

$$V_{out} = 0.8(1 + R1/R2) = 1.5V$$



Reserve discharge path





Title
DCIN,BATT CONNECTOR

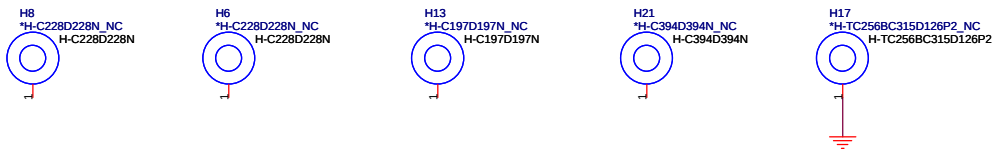
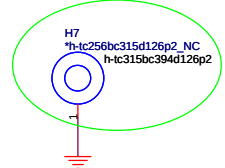
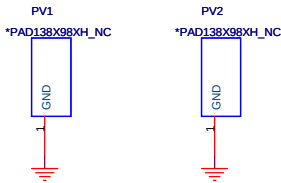
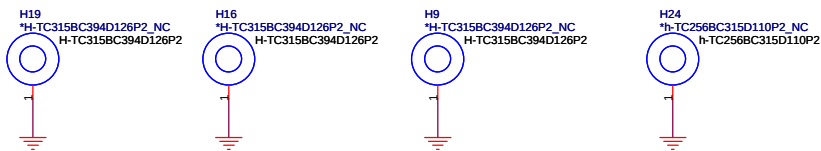
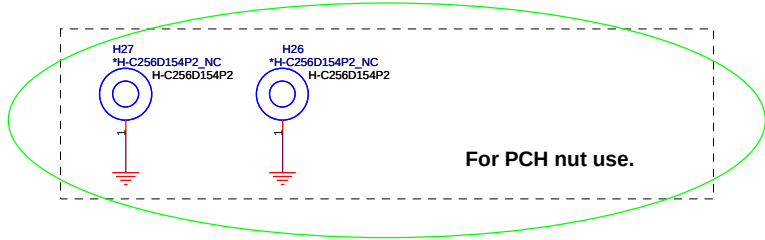
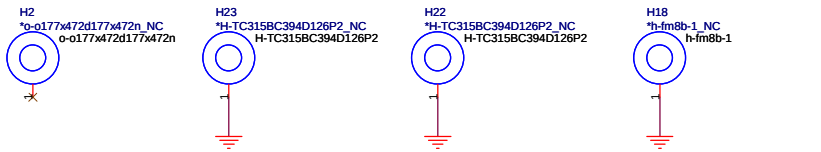
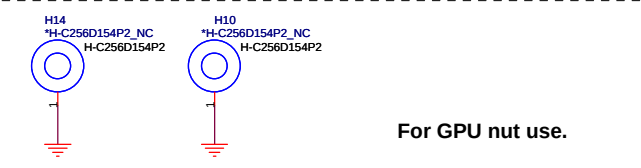
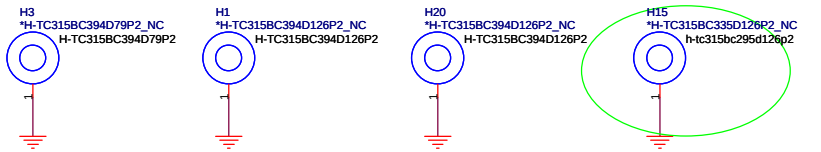
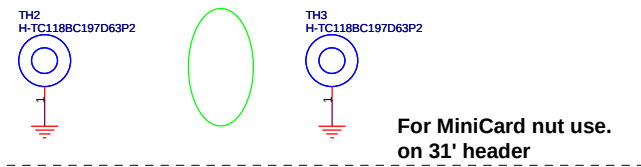
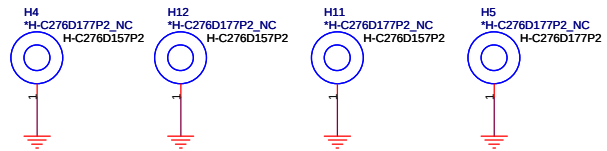
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FOR CPU use

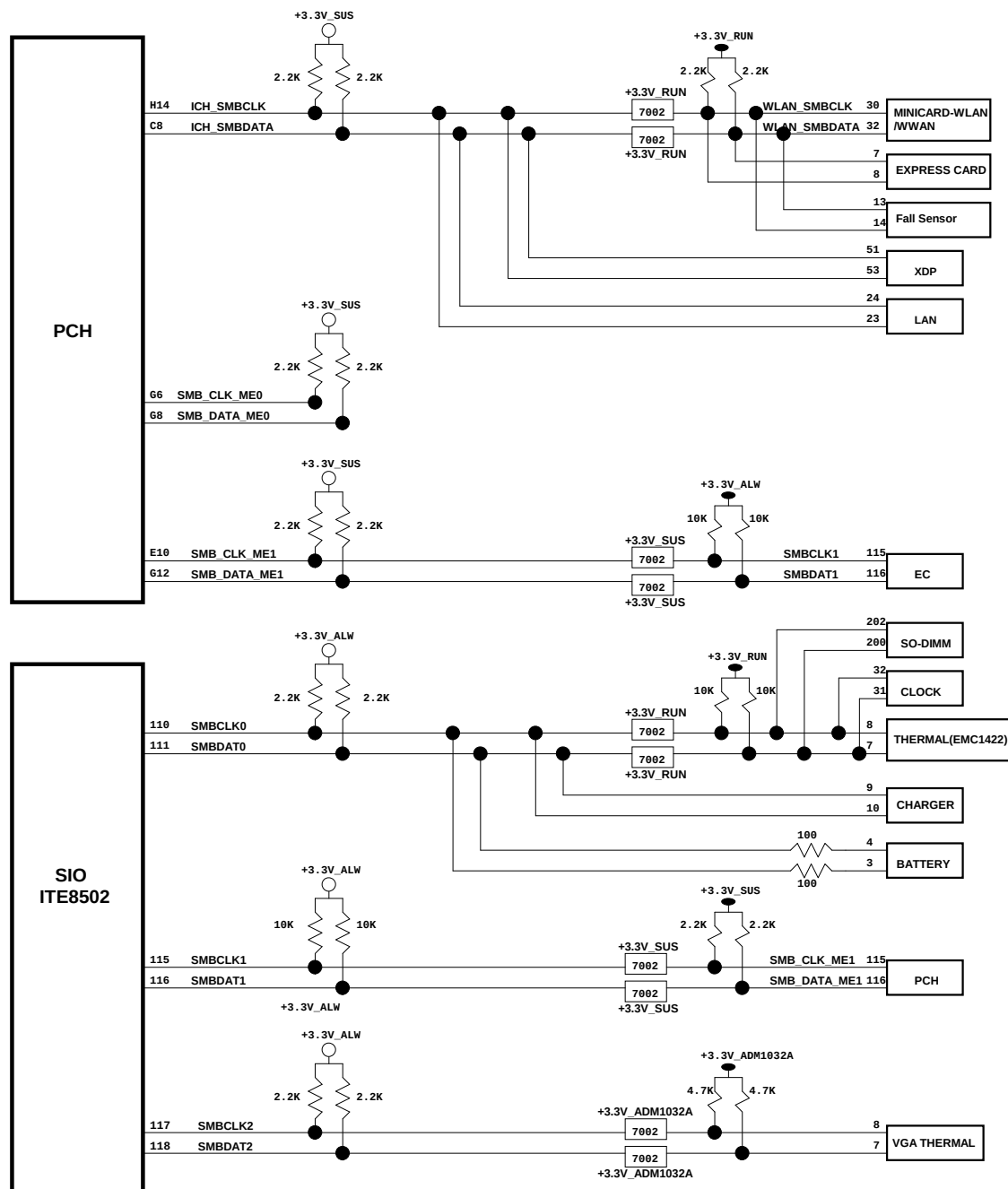


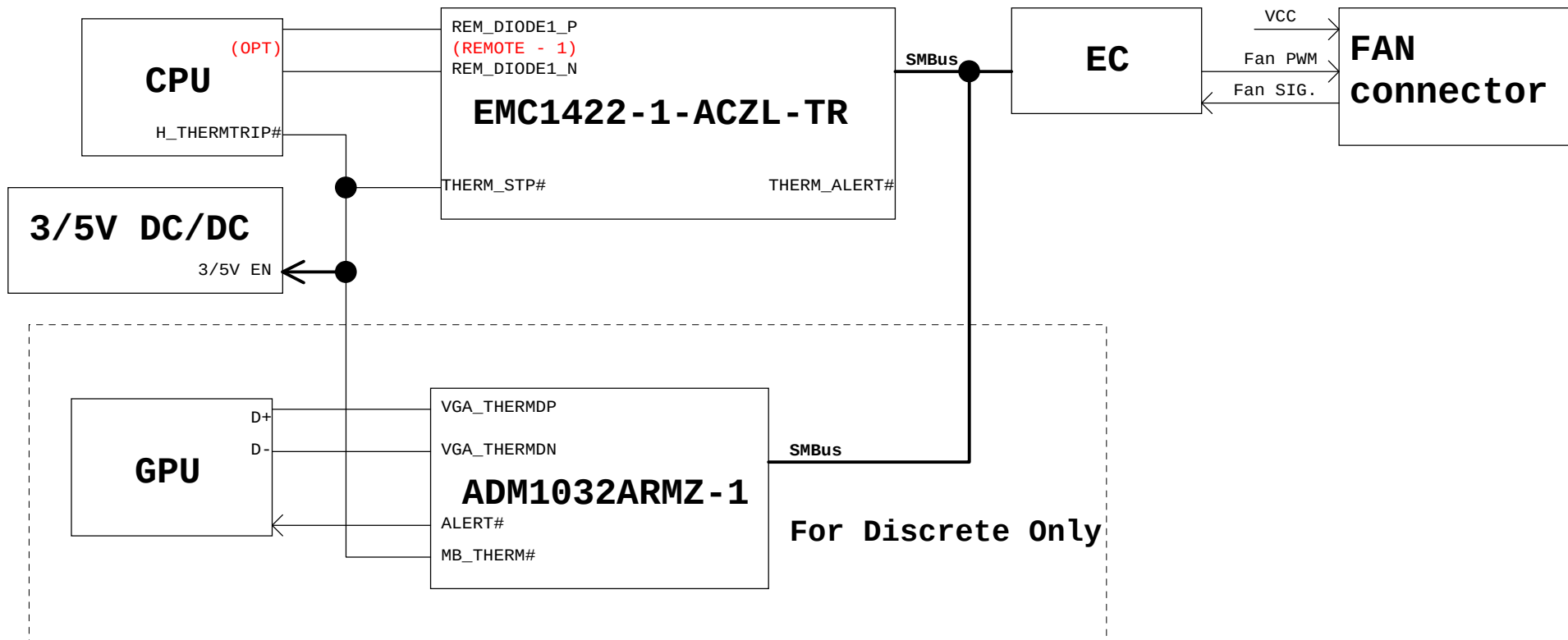
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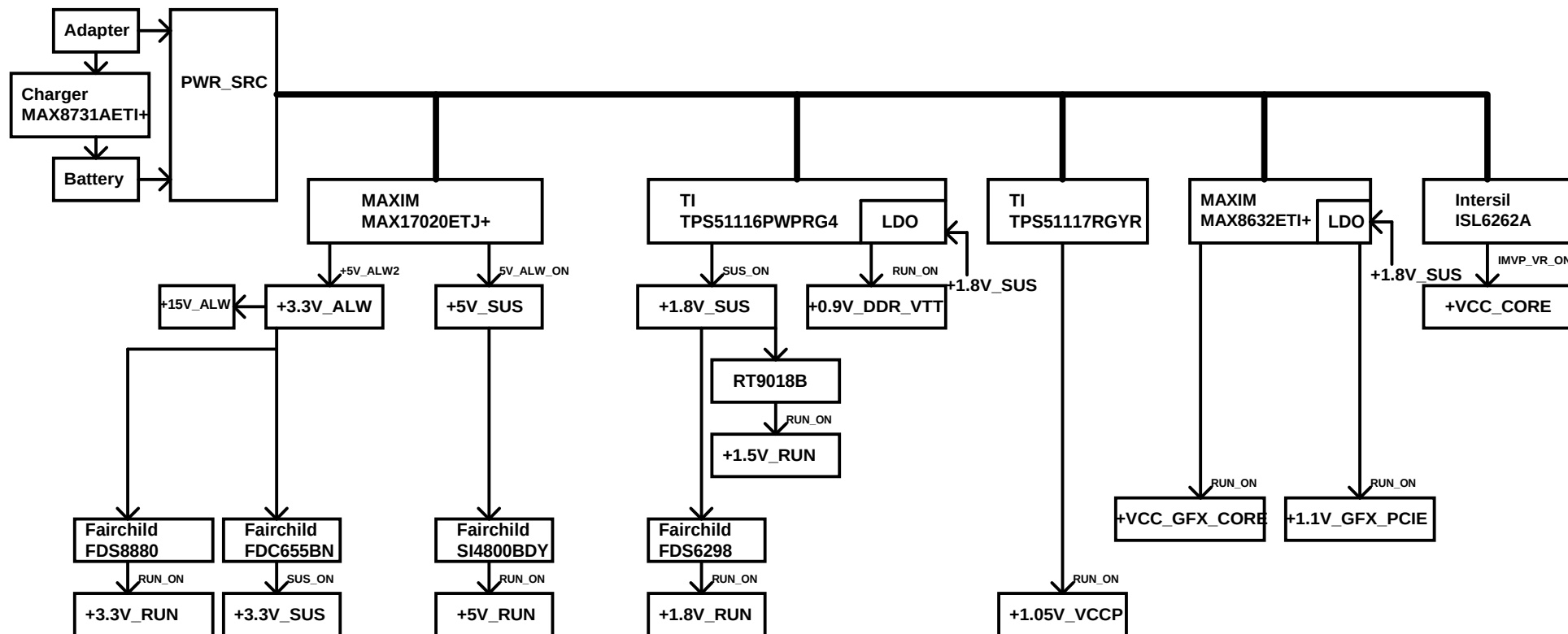


QUANTA
COMPUTER

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EMI CAP		
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FM9 Power Design Block Diagram 2009/02/25

