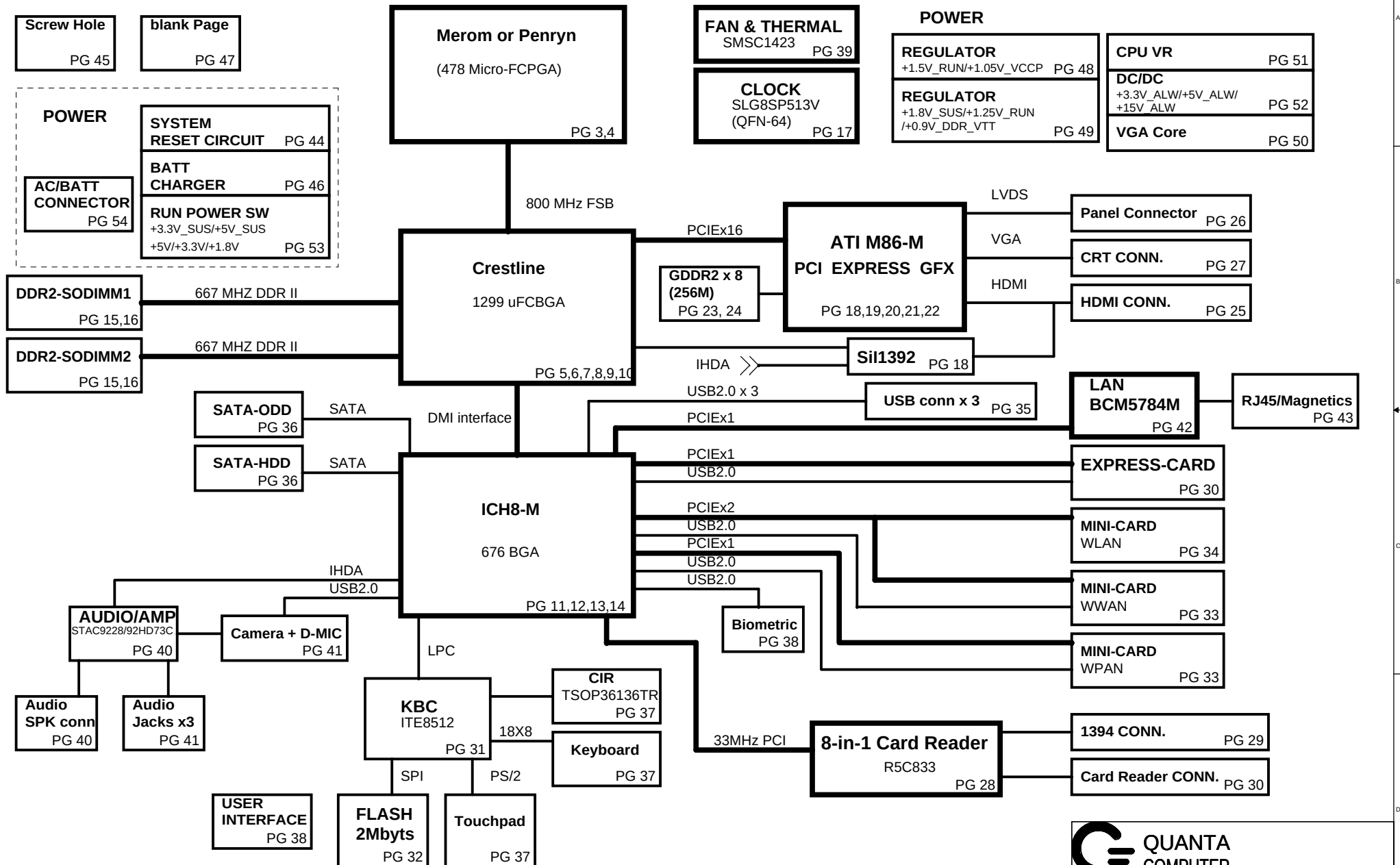


GM3(B) Pacino Intel Discrete & UMA Block Diagram

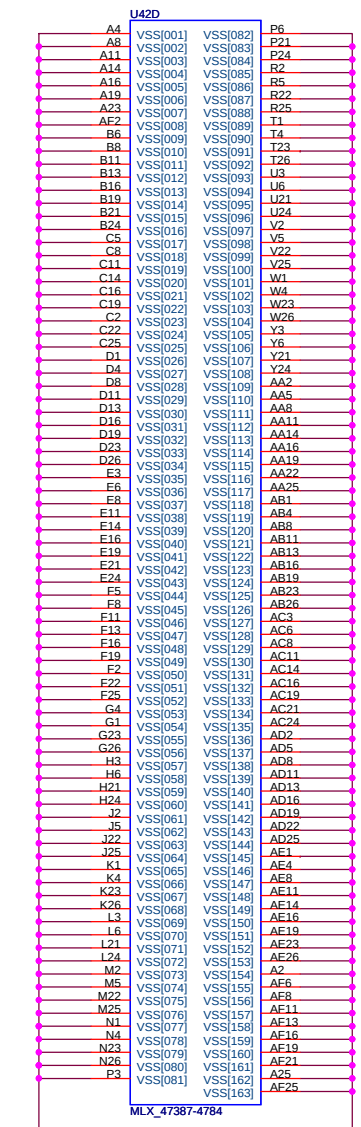
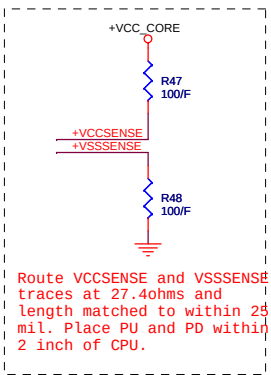
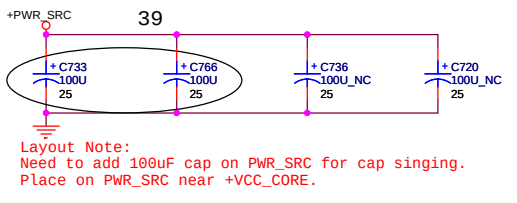
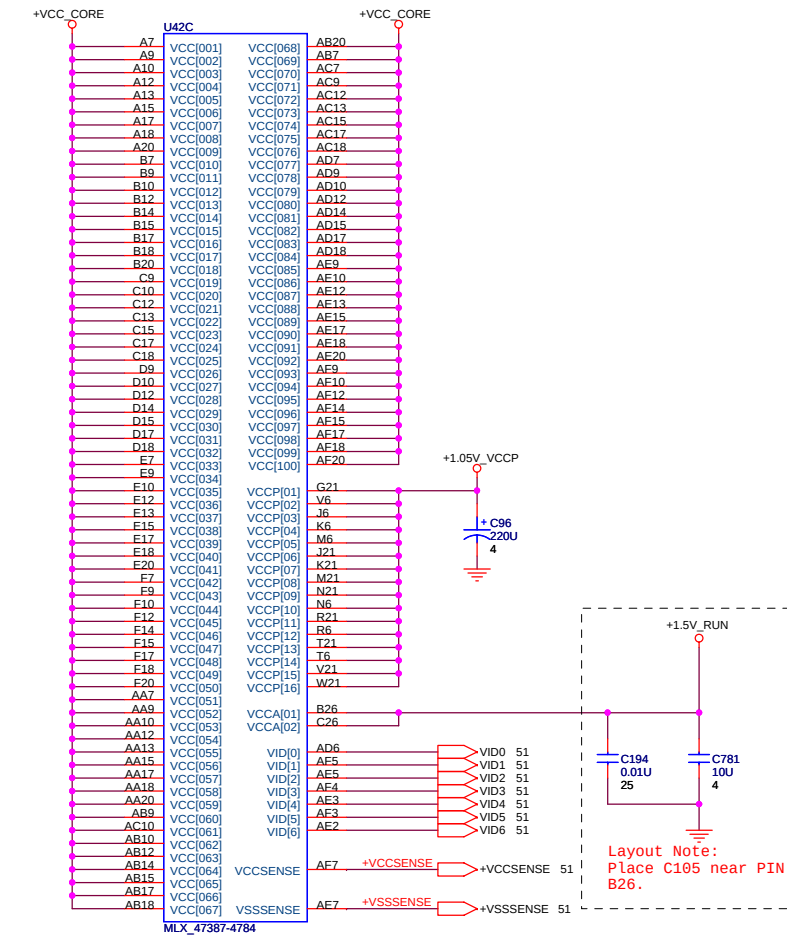
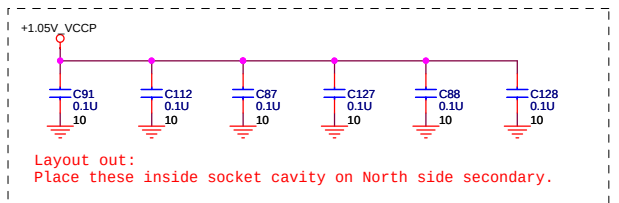
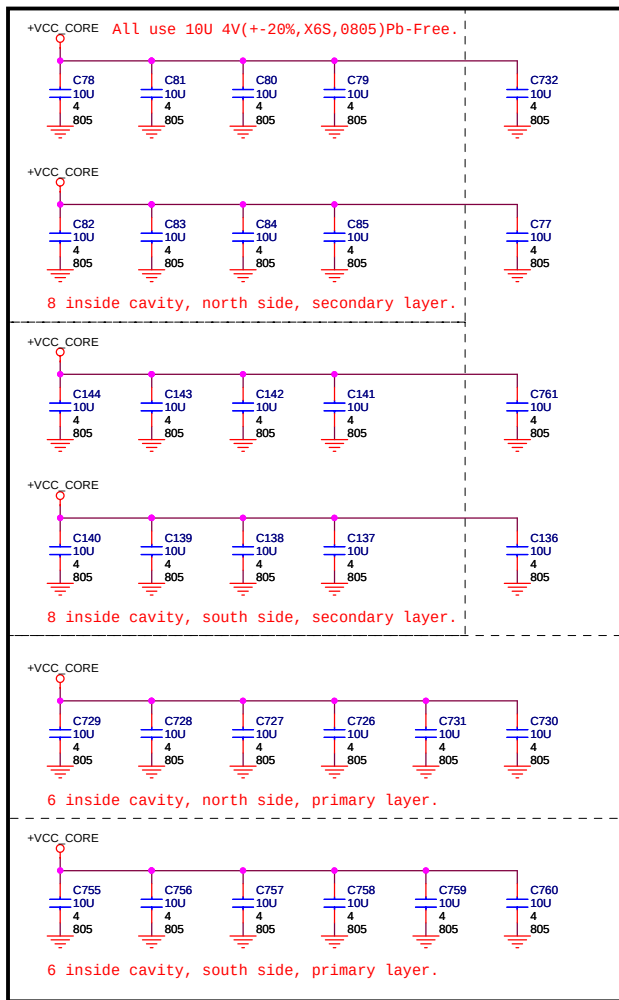
VER : 2A

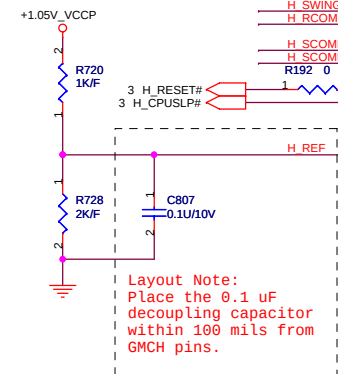
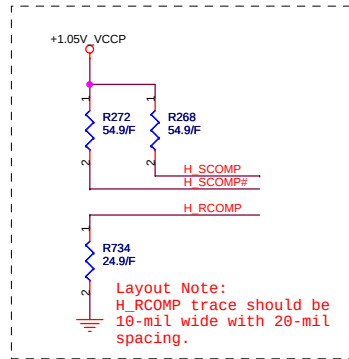
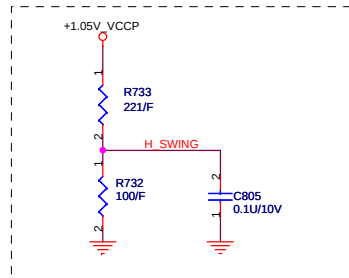
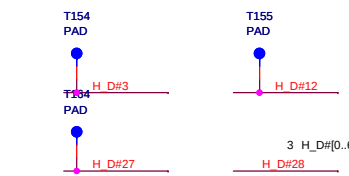


PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	Merom
5-10	Crestline
11-14	ICH8M
15-16	DDRII SO-DIMM(200P)
17	Clock Generator
18-24	VGA
25	HDMI
26	LCD connector
27	CRT
28	Card reader PCI interface
29	Card reader & 1394
30	Express card & card reader conn.
31	SIO
32	Flash/RTC
33	WWAN/WPAN
34	WLAN
35	USB port
36	SATA HDD & ODD
37	TP/KB/MB/CIR
38	switch/LED
39	FAN/Thermal
40-41	Audio/CONN.
42-43	Docking Conn/Q-Switch
44	System Reset Circuit
45-46	Screw hole & Charger
47	Blank page
48	1.05VCCP & 1.5VRUN
49	1.8VSUS & 0.9VTT
50	VGA power circuit
51	CPU_ISL6266 (2phase)
52	D/D ISL6237 3.3V/5V
53	RUN Power Switch
54	DCIN,Batt
55	EMI CAP
56	SMBUS BLOCK
57	Power statu & Block diagram

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,48,49,50,51,52,55	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,26,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,30,37,38,43,48,49,50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53,55	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,25,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,25,26,27,28,30,33,34,36,38,39,40,41,42,53,55	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,24,25,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,,53,55	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.25V_RUN	+1.25V	6,9,14,49,53	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,37,48,55	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.5V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	37,38,52,53	LED power source	LDO output	

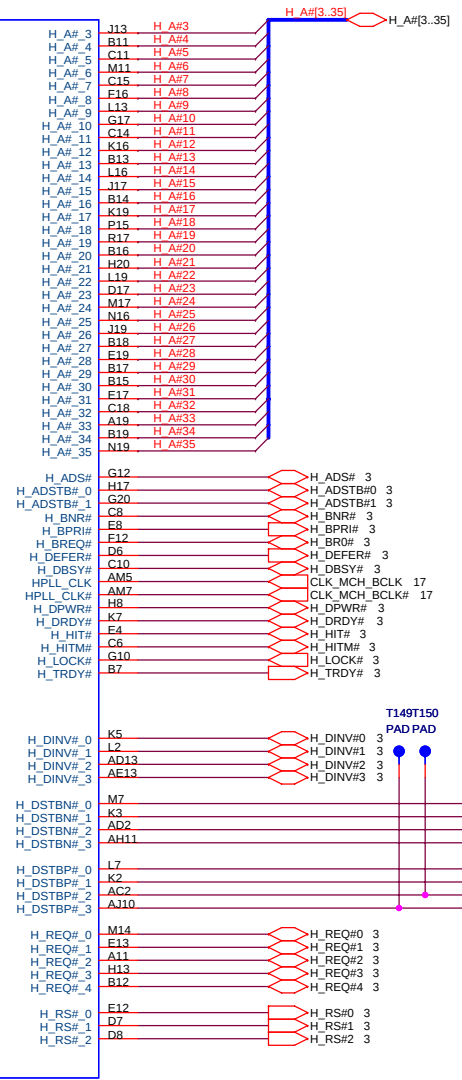
GND PLANE	PAGE	DESCRIPTION
⏏ 8731AGND	46	
⏏ AGND_0.9V	49	
⏏ AGND_DC/DC	52	
⏏ AGND_DC2	48	
⏏ AGND_DDR	49	
⏏ AGND_ISL6260	51	
≡ GND	ALL	





H_D#0	E2	H_D#_0
H_D#1	G2	H_D#_1
H_D#2	G7	H_D#_2
H_D#3	M6	H_D#_3
H_D#4	H7	H_D#_4
H_D#5	H3	H_D#_5
H_D#6	G4	H_D#_6
H_D#7	F3	H_D#_7
H_D#8	N8	H_D#_8
H_D#9	H2	H_D#_9
H_D#10	M10	H_D#_10
H_D#11	N12	H_D#_11
H_D#12	N9	H_D#_12
H_D#13	H5	H_D#_13
H_D#14	P13	H_D#_14
H_D#15	K9	H_D#_15
H_D#16	M2	H_D#_16
H_D#17	W10	H_D#_17
H_D#18	Y8	H_D#_18
H_D#19	V4	H_D#_19
H_D#20	M3	H_D#_20
H_D#21	J1	H_D#_21
H_D#22	N5	H_D#_22
H_D#23	N3	H_D#_23
H_D#24	W6	H_D#_24
H_D#25	W9	H_D#_25
H_D#26	N2	H_D#_26
H_D#27	Y7	H_D#_27
H_D#28	Y9	H_D#_28
H_D#29	P4	H_D#_29
H_D#30	W3	H_D#_30
H_D#31	N1	H_D#_31
H_D#32	AD12	H_D#_32
H_D#33	AE3	H_D#_33
H_D#34	AD8	H_D#_34
H_D#35	AC9	H_D#_35
H_D#36	AC7	H_D#_36
H_D#37	AC14	H_D#_37
H_D#38	AD11	H_D#_38
H_D#39	AC11	H_D#_39
H_D#40	AB2	H_D#_40
H_D#41	AD7	H_D#_41
H_D#42	AB1	H_D#_42
H_D#43	Y3	H_D#_43
H_D#44	AC6	H_D#_44
H_D#45	AE2	H_D#_45
H_D#46	AC5	H_D#_46
H_D#47	AG3	H_D#_47
H_D#48	AJ9	H_D#_48
H_D#49	AH8	H_D#_49
H_D#50	AJ14	H_D#_50
H_D#51	AE9	H_D#_51
H_D#52	AE11	H_D#_52
H_D#53	AH12	H_D#_53
H_D#54	AJ5	H_D#_54
H_D#55	AH5	H_D#_55
H_D#56	AJ6	H_D#_56
H_D#57	AE7	H_D#_57
H_D#58	AJ7	H_D#_58
H_D#59	AJ2	H_D#_59
H_D#60	AE5	H_D#_60
H_D#61	AJ3	H_D#_61
H_D#62	AH2	H_D#_62
H_D#63	AH13	H_D#_63

HOST



U45 QCI PN
DIS
AJSLA5U0T11
UMA
AJSLA5T0T13

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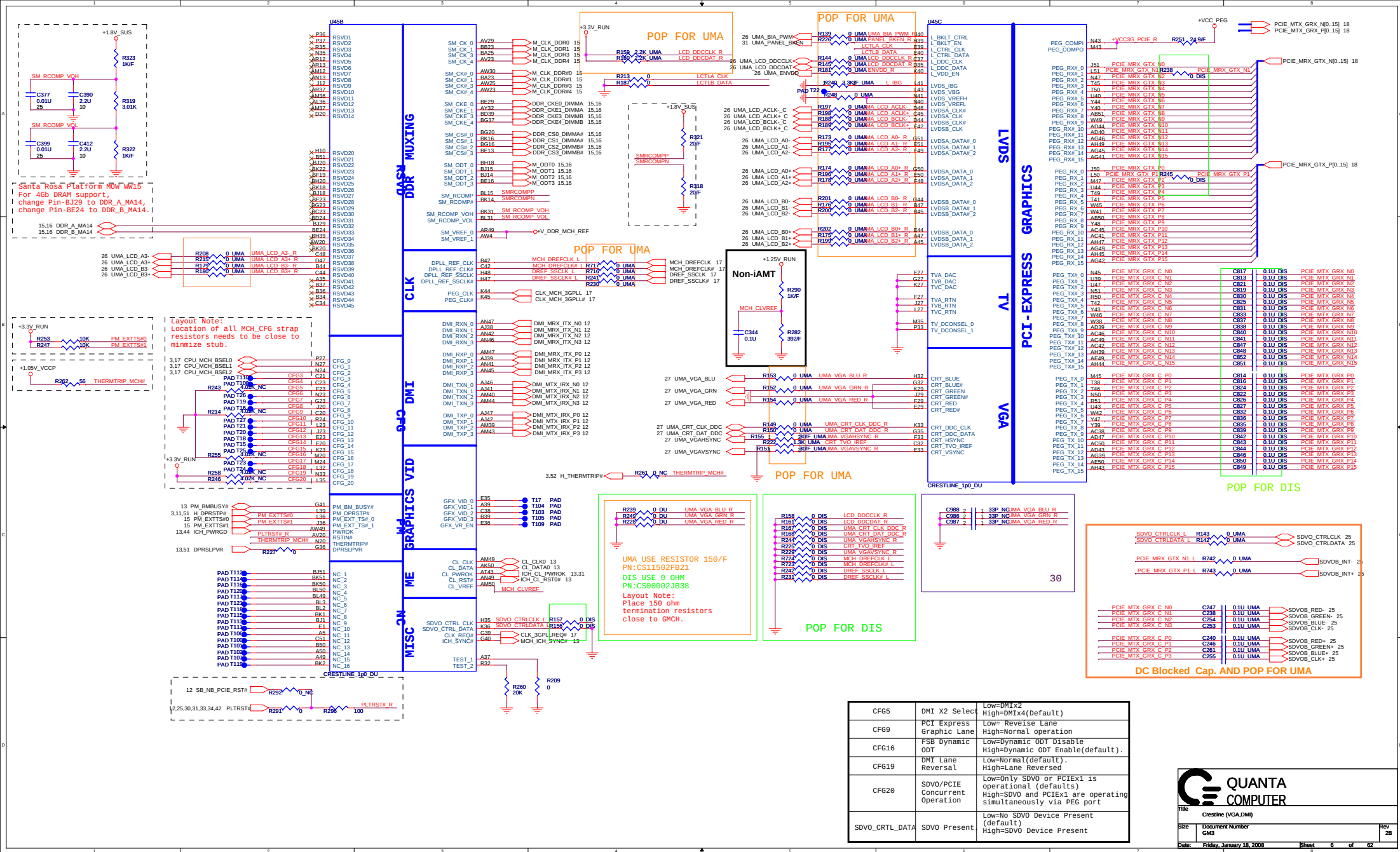
Title
Crestline (HOST)

Size
Document Number
GM3

Date
Friday, January 18, 2008

Rev
2B

Sheet
5 of 62



CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB dynamic ODT	Low=dynamic ODT Disable High=dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(Default). High=Lane Reversed
CFG28	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present



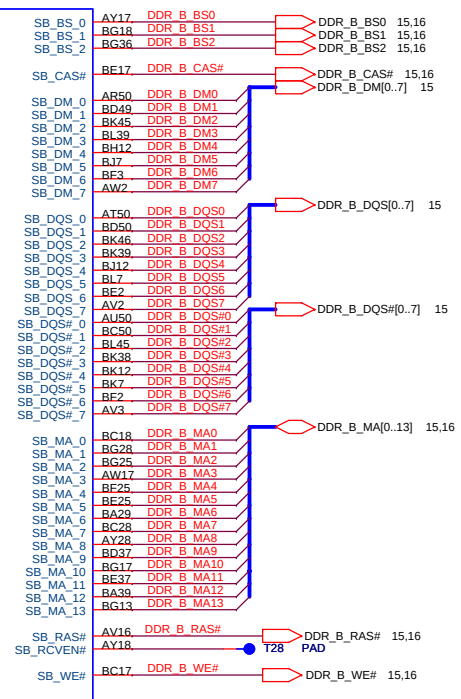
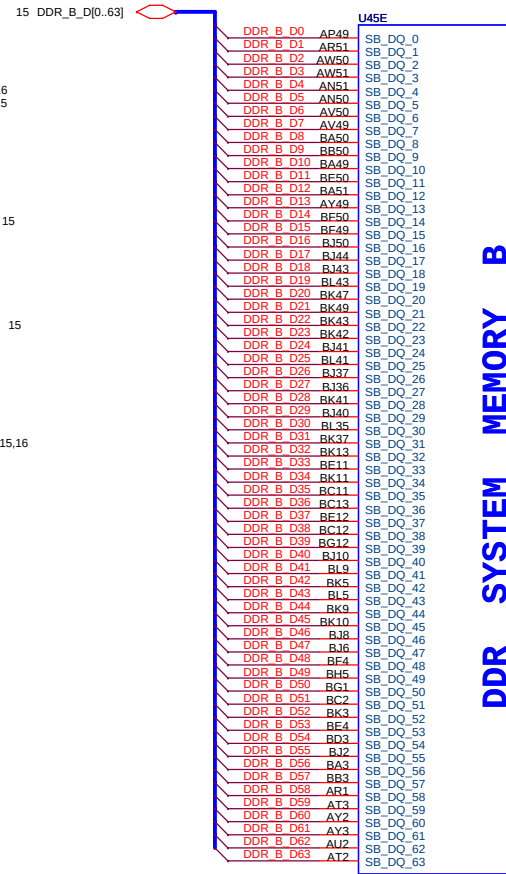
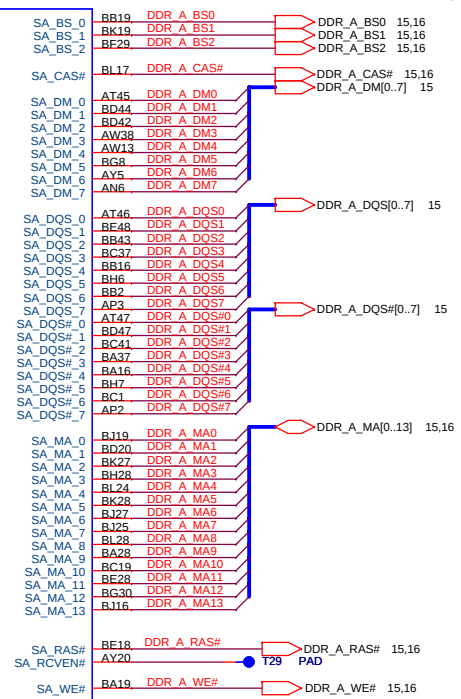
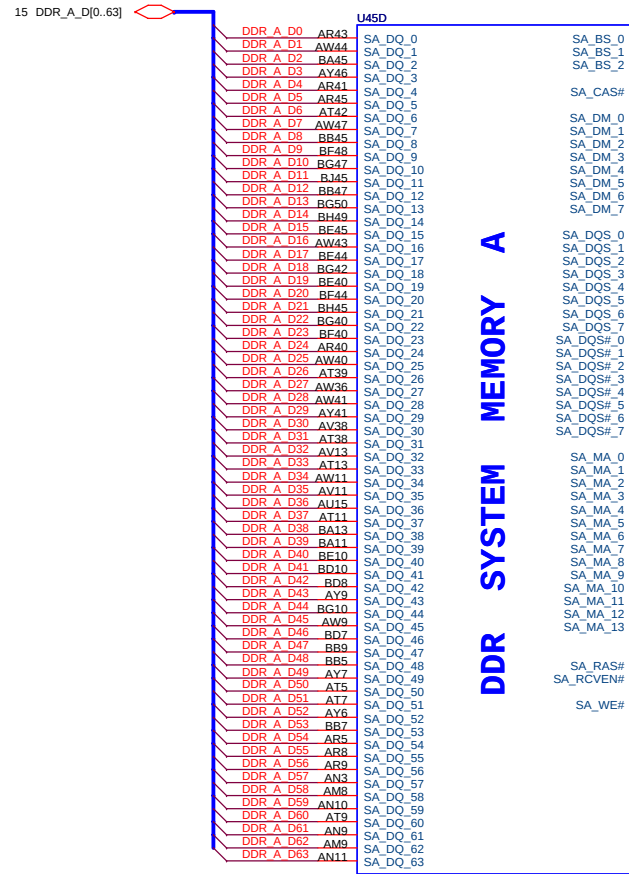
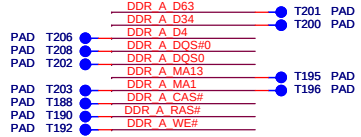
Title	Crestline (VGA-DMI)
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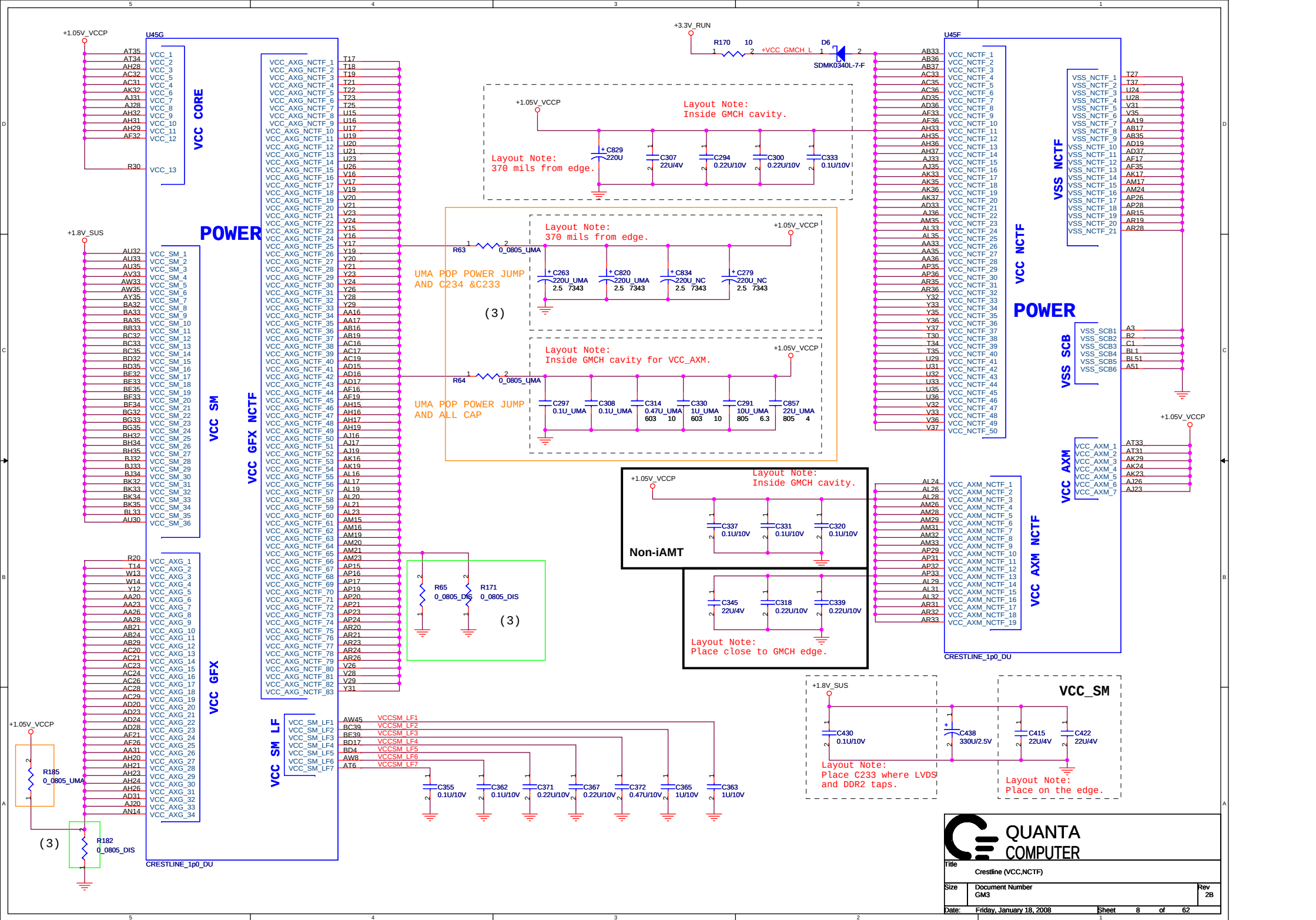
210	Document Number
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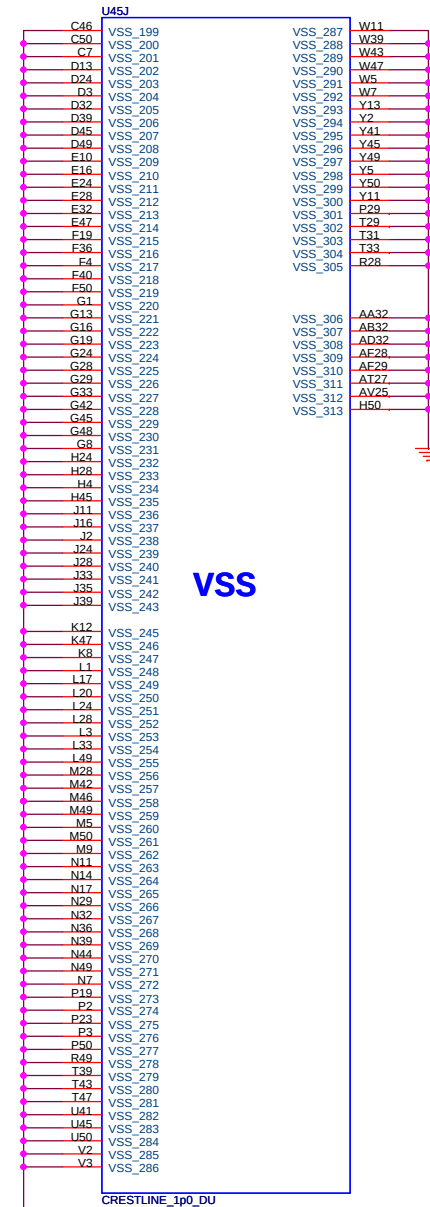
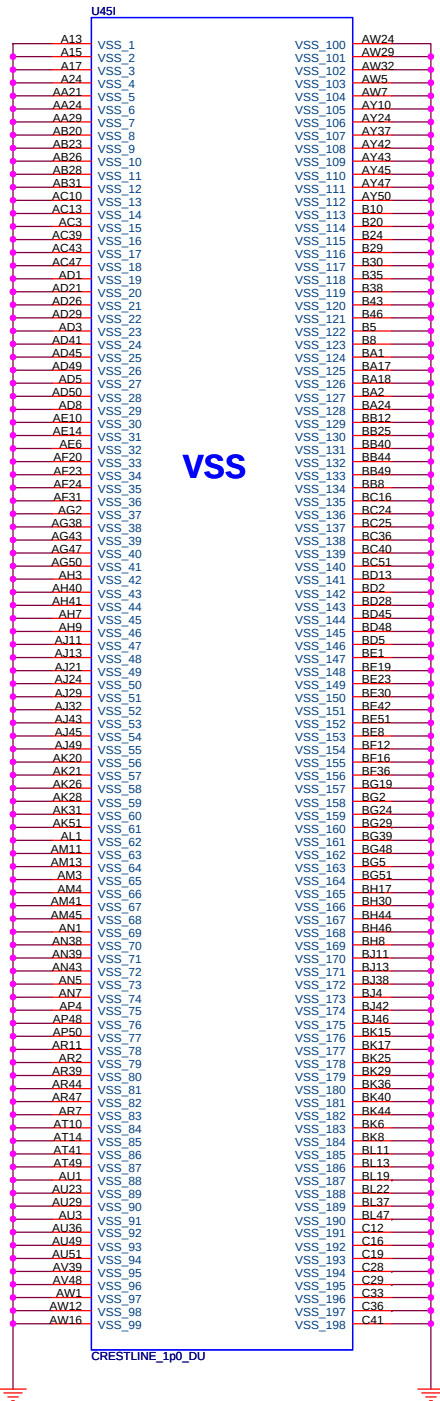
Size	Document Number
	GM3

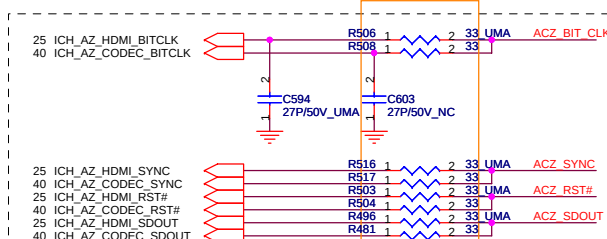
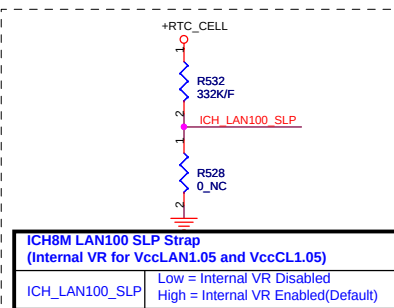
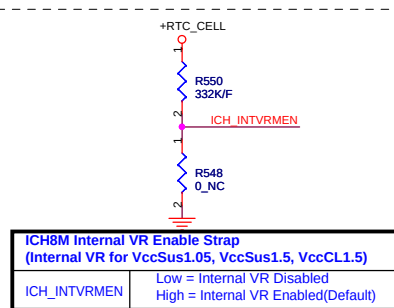
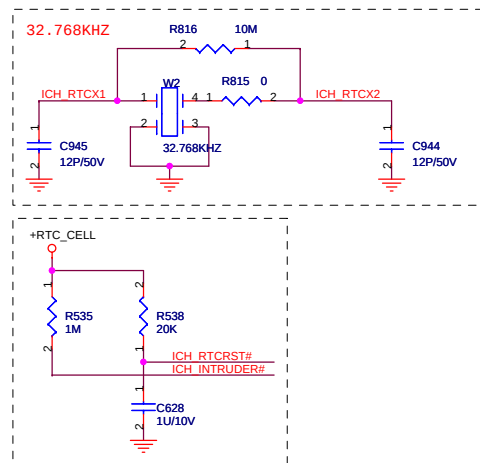
Date: Friday, January 18, 2019

[illegible]

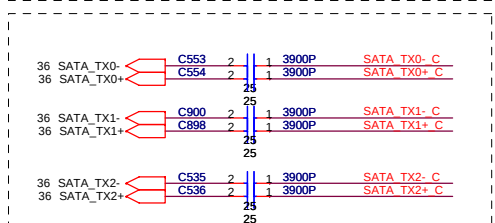




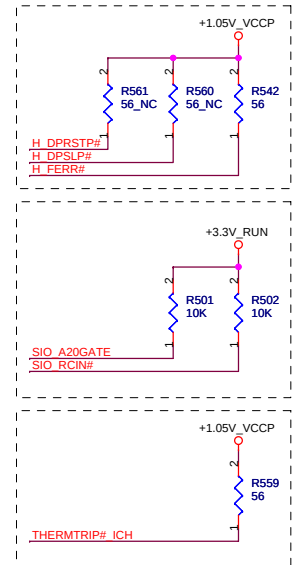
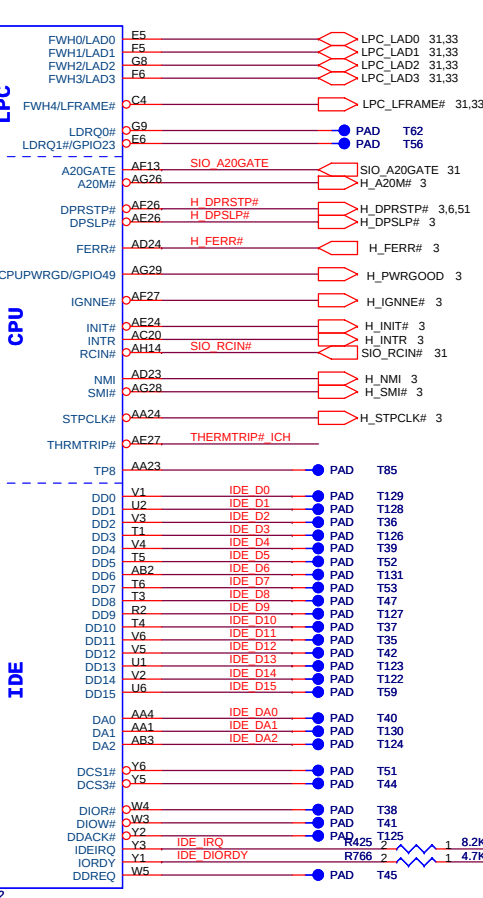
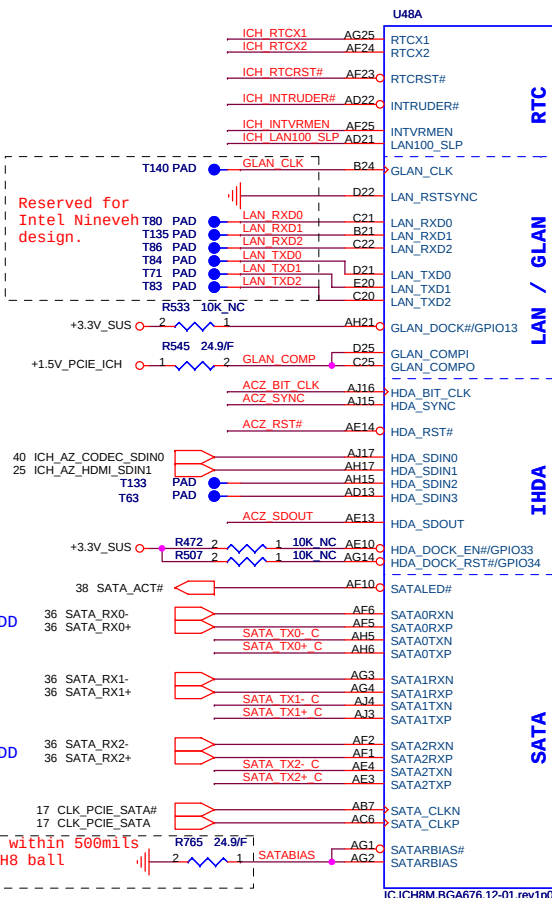




Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respectively. Basically, keep the same distance from T for all series termination resistors.

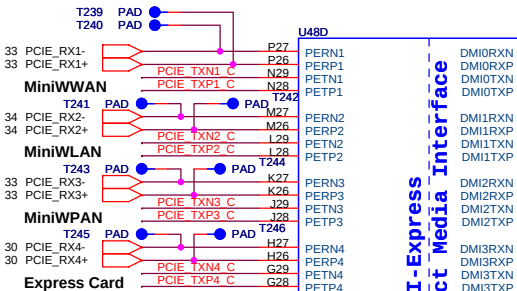
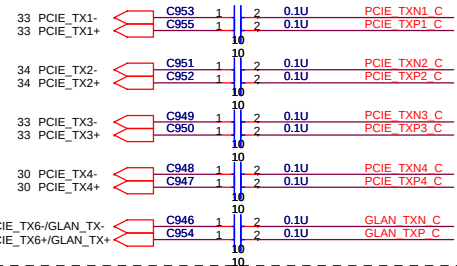


Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.

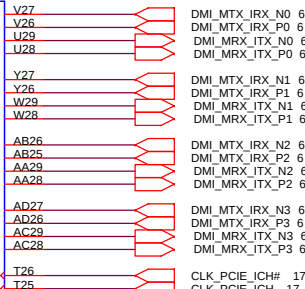


XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

Place TX DC blocking caps close ICH8.



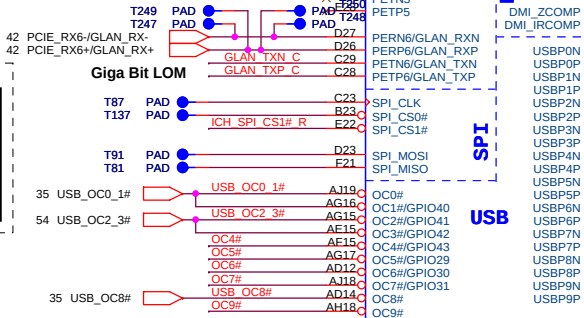
PCI-Express
Direct Media Interface

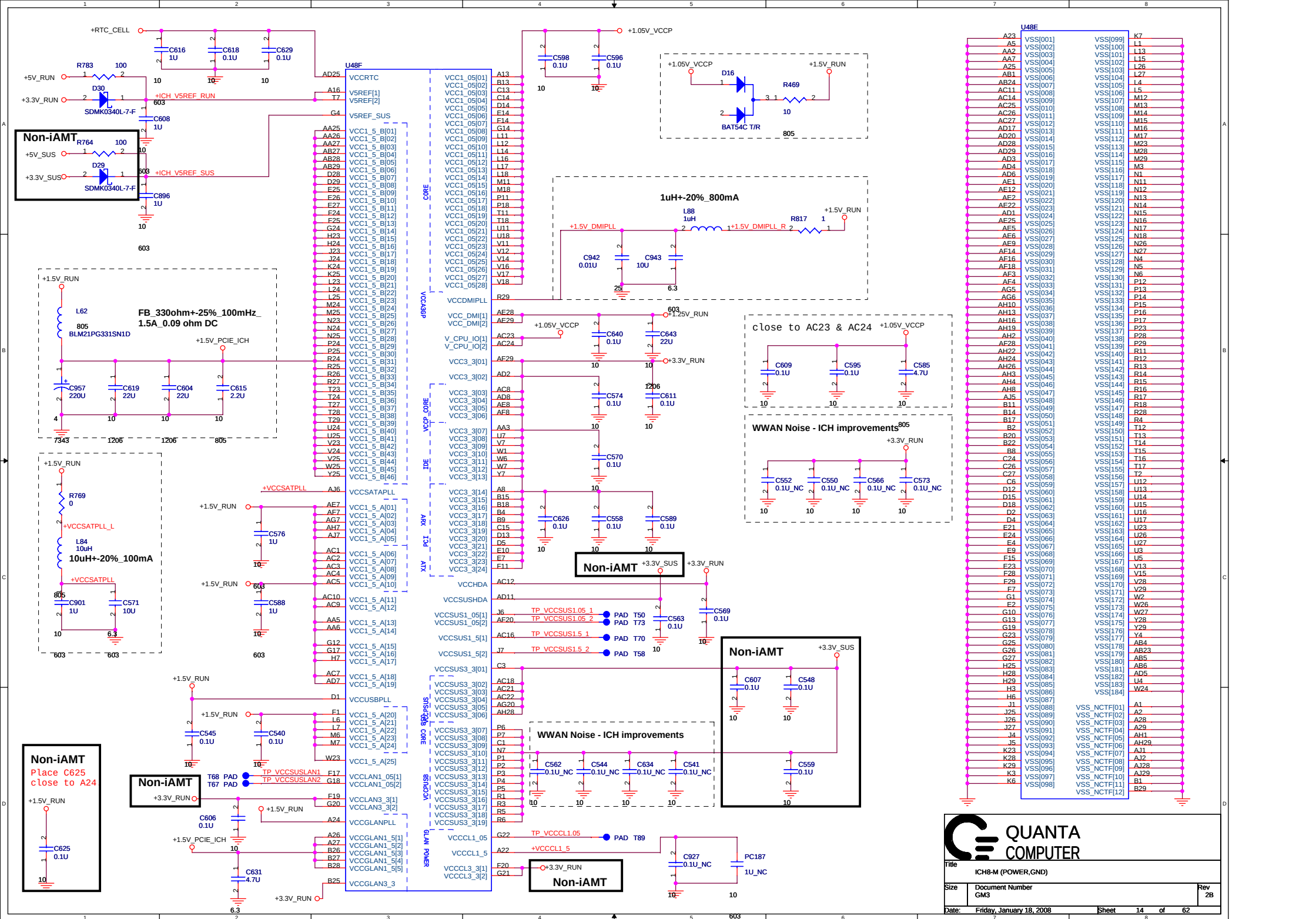


DM1_MTX_IRX_N0 6
DM1_MTX_IRX_P0 6
DM1_MRX_ITX_N0 6
DM1_MRX_ITX_P0 6
DM1_MTX_IRX_N1 6
DM1_MTX_IRX_P1 6
DM1_MRX_ITX_N1 6
DM1_MRX_ITX_P1 6
DM1_MTX_IRX_N2 6
DM1_MTX_IRX_P2 6
DM1_MRX_ITX_N2 6
DM1_MRX_ITX_P2 6
DM1_MTX_IRX_N3 6
DM1_MTX_IRX_P3 6
DM1_MRX_ITX_N3 6
DM1_MRX_ITX_P3 6
CLK_PCIE_ICH# 17
CLK_PCIE_ICH# 17

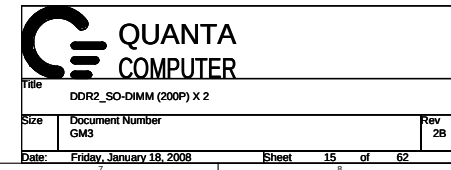
Place within 500mils of ICH8

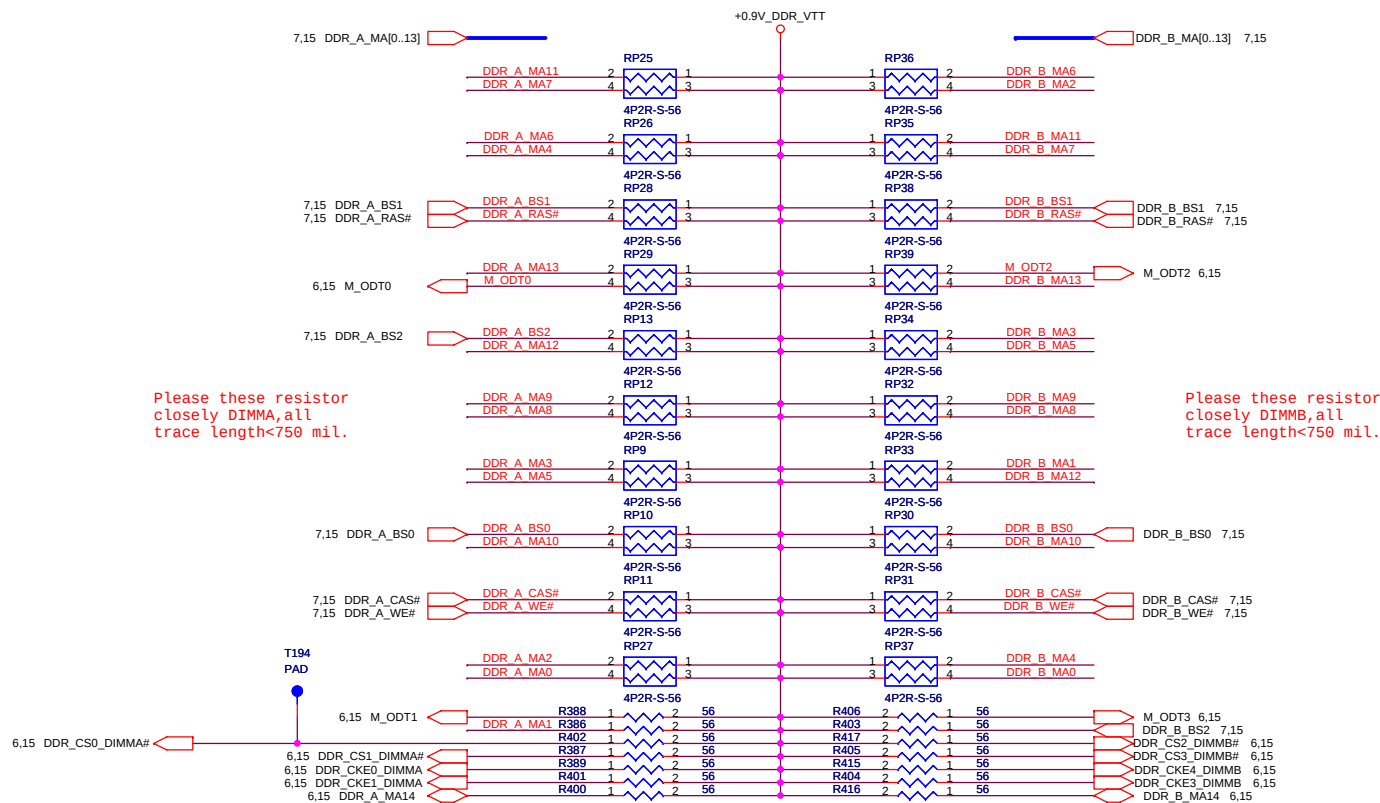
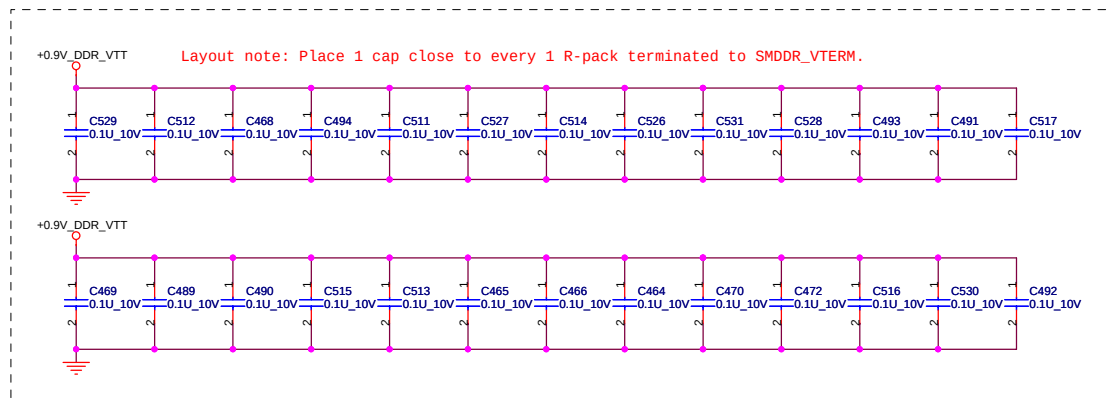
		Boot BIOS Strap		
		GNT0#	SPI_CS1#	
LPC	11	No stuff	No stuff	
PCI	10	No stuff	Stuff	
SPI	01	Stuff	No stuff	



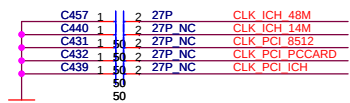


SLAVE

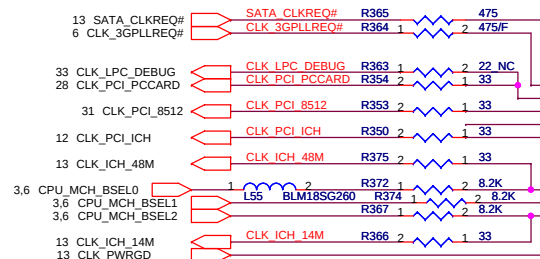




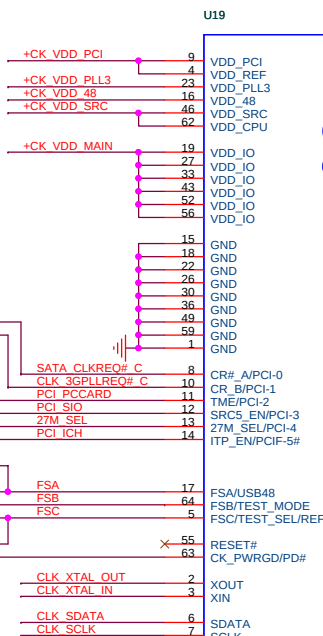
Add capacitor pads for improving WWAN.



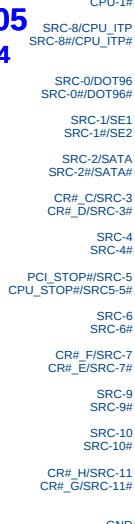
14.318MHz



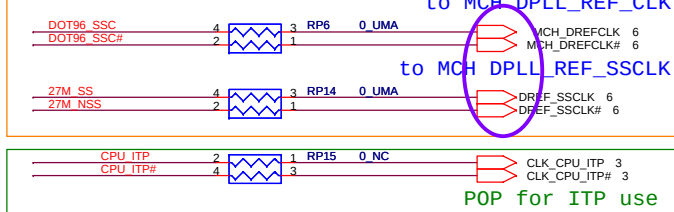
CLK_LPC_DEBUG FOR DEBUG
NEED POP RESISTOR



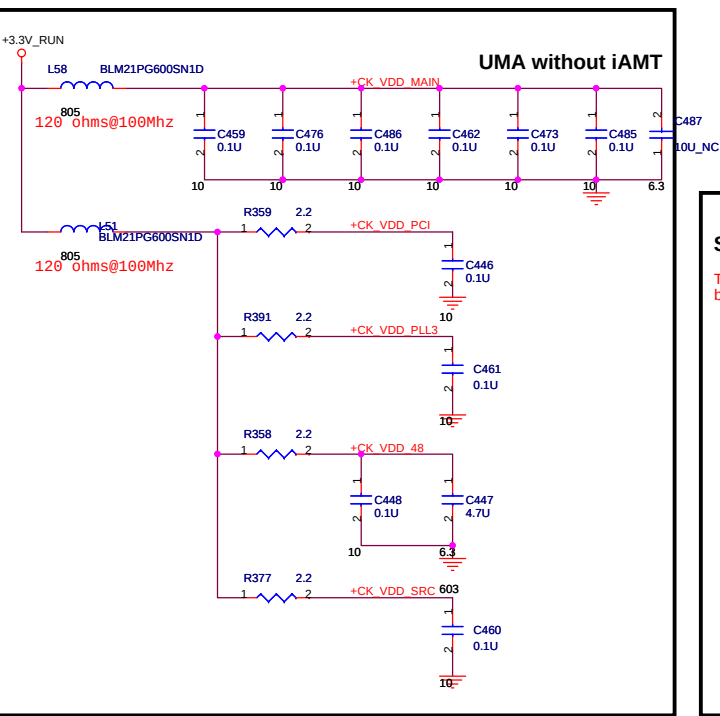
CK505
QFN64



POP RESISTOR FOR UMA

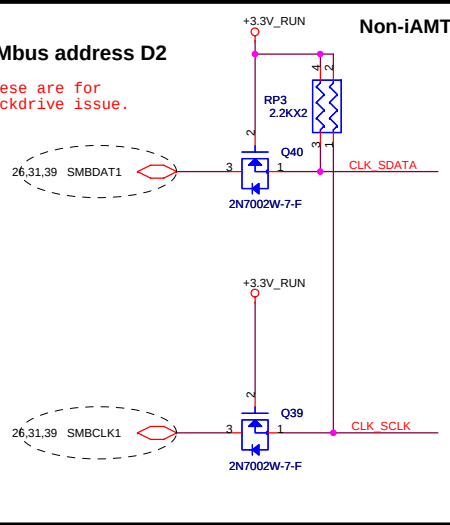


POP for ITP use

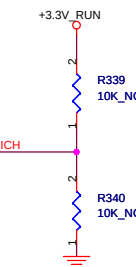


SMbus address D2

These are for
backDrive issue.



Non-iAMT



27M_SEL

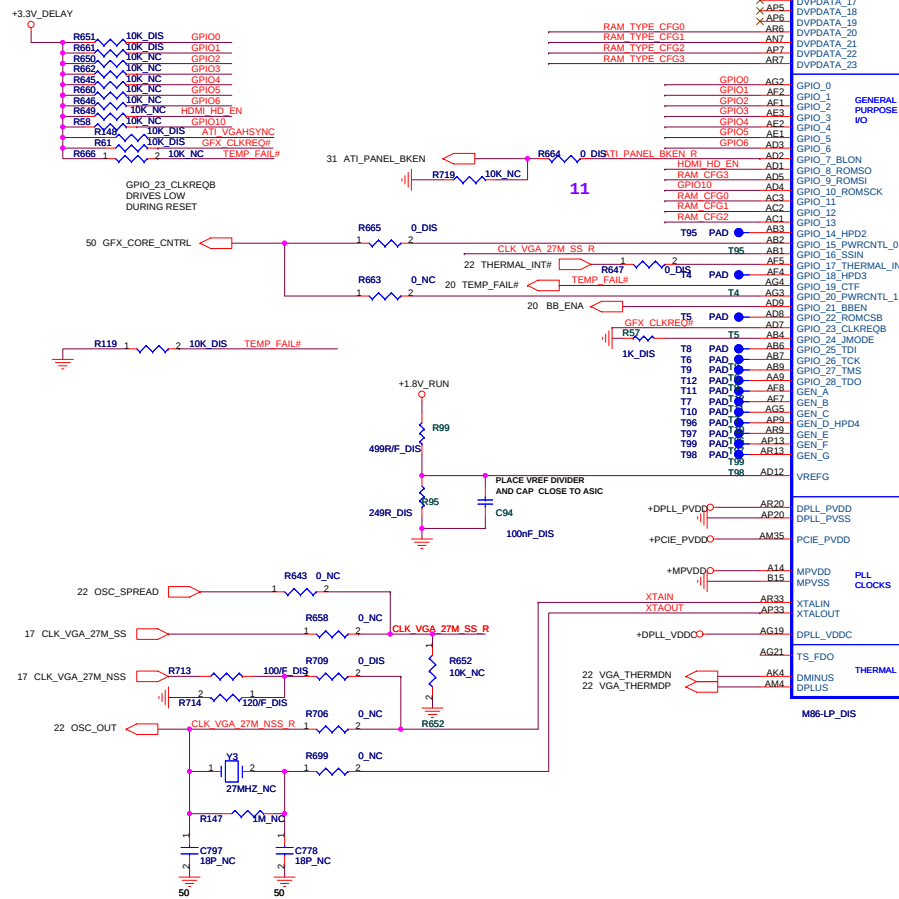
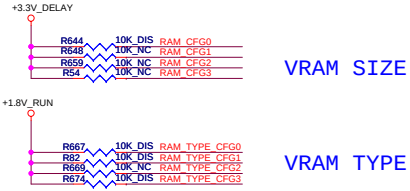
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

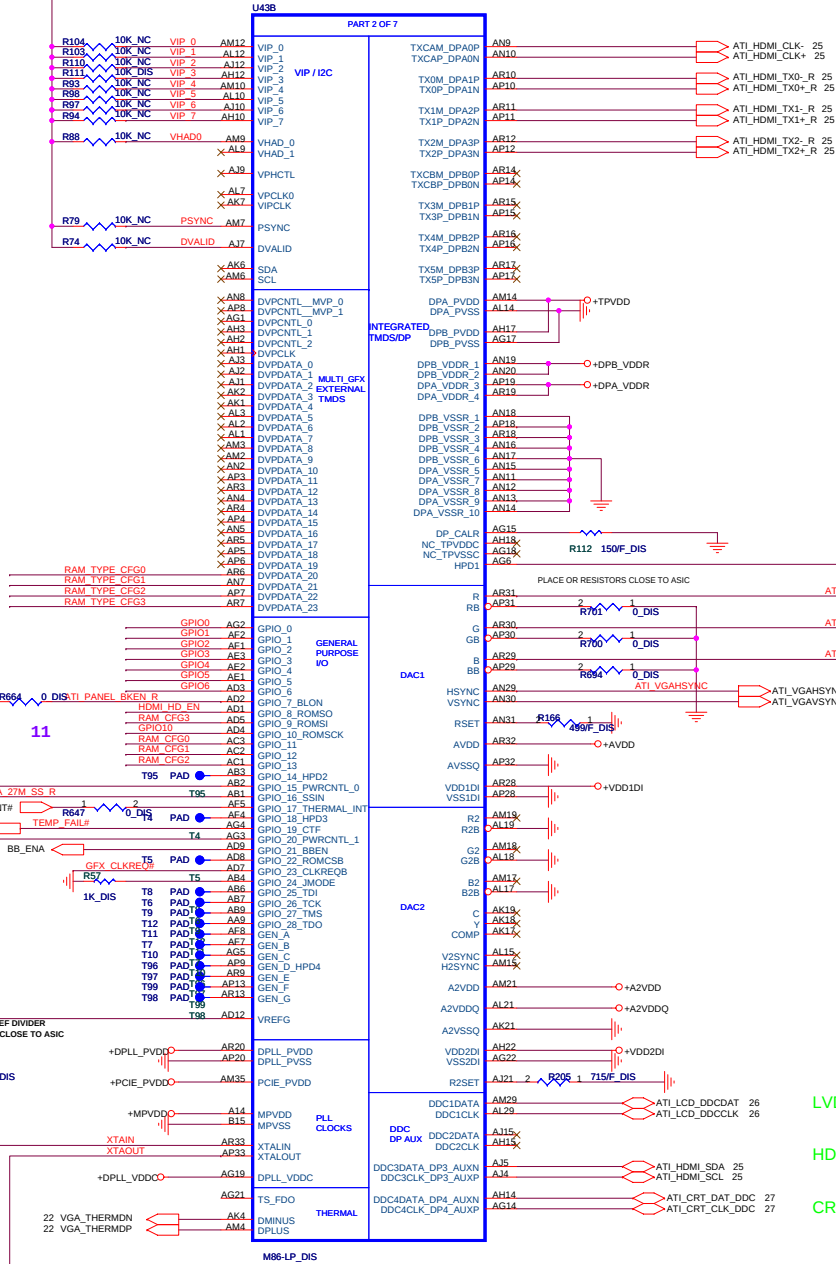
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MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	X	0	0	0
256MB	X	0	0	1
64MB	X	0	1	0
512MB	X	1	0	0

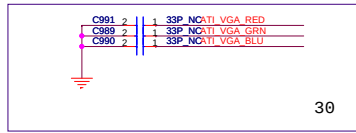
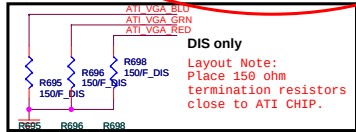
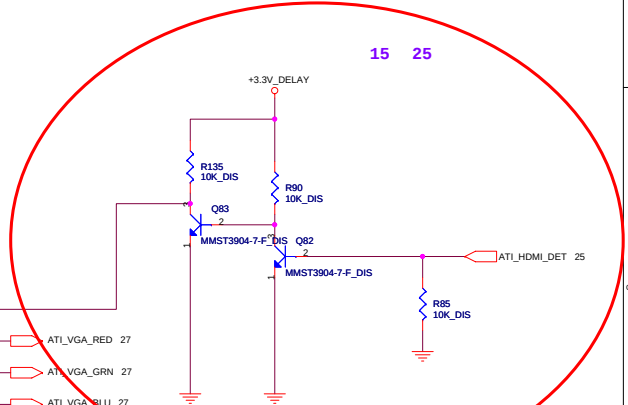
Memory Straps	RAM TYPE_CFG3	RAM TYPE_CFG2	RAM TYPE_CFG1	RAM TYPE_CFG0
400 MHz 256MB(16M*16) Hynix	1	1	1	1
400 MHz 256MB(16M*16) Qimonda	1	1	1	0
500 MHz 256MB(16M*16) Hynix	1	1	0	1
500 MHz 256MB(16M*16) Qimonda	1	1	0	0
500 MHz 256MB(16M*16) Samsung	1	0	1	1



8/15: The strap on VIP[3] is for enabling HD Audio on M86.



HDMI CONN



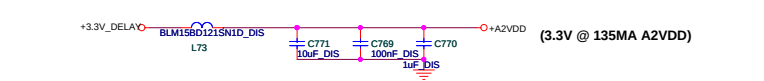
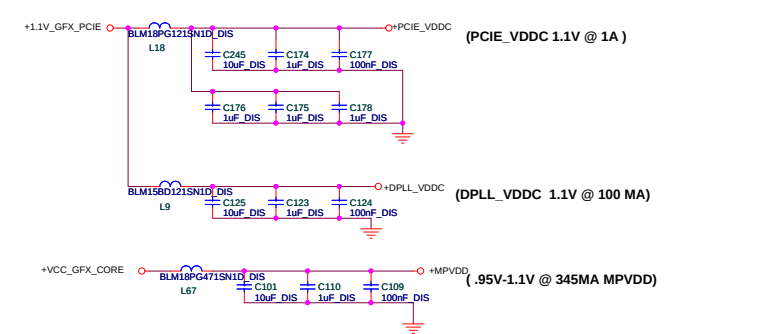
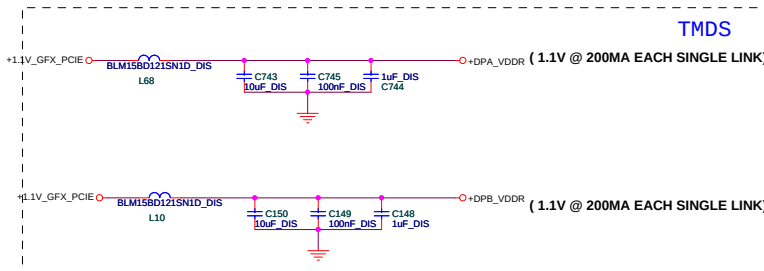
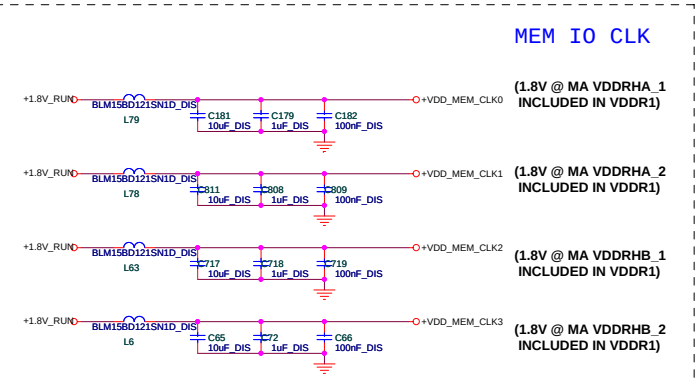
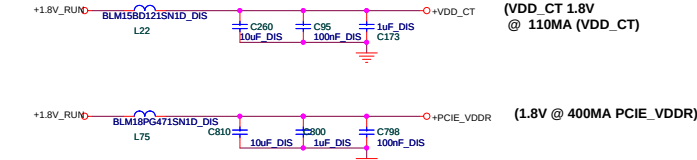
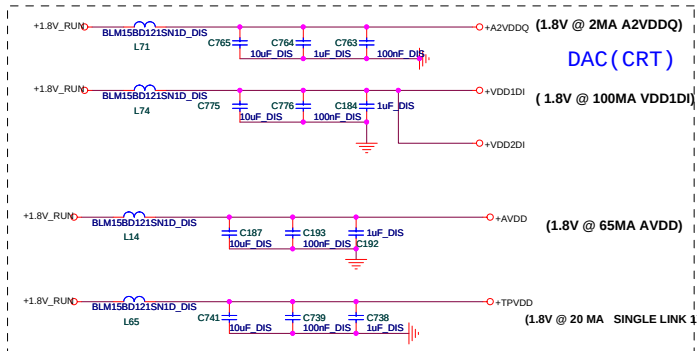
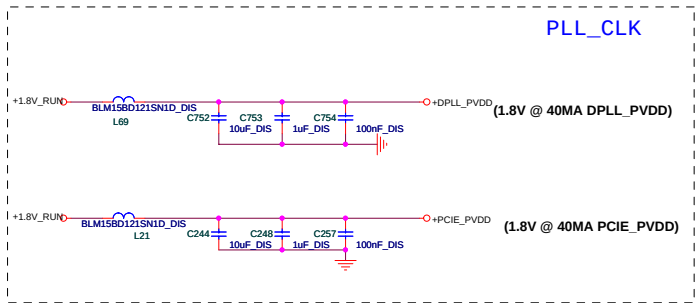
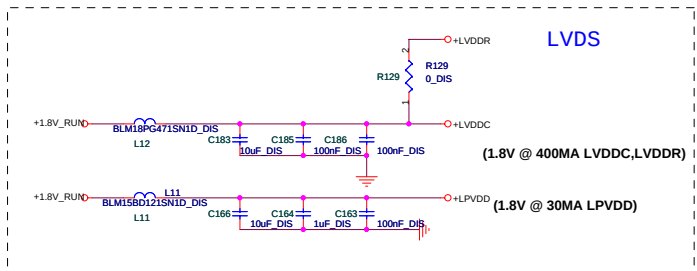
ATI VGA RED, ATI VGA GRN, ATI VGA BLU

LVDS

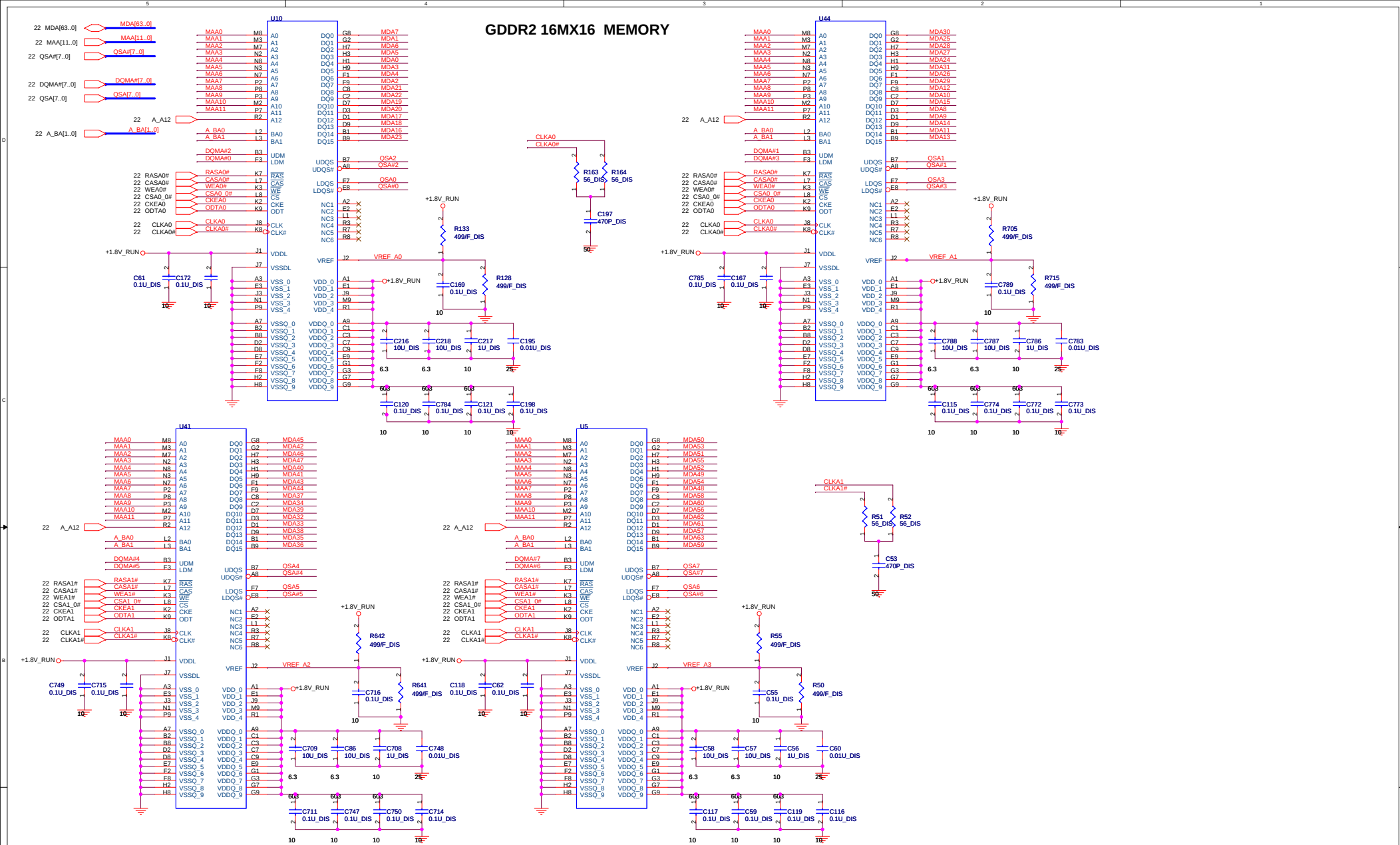
HDMI

CRT





PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE

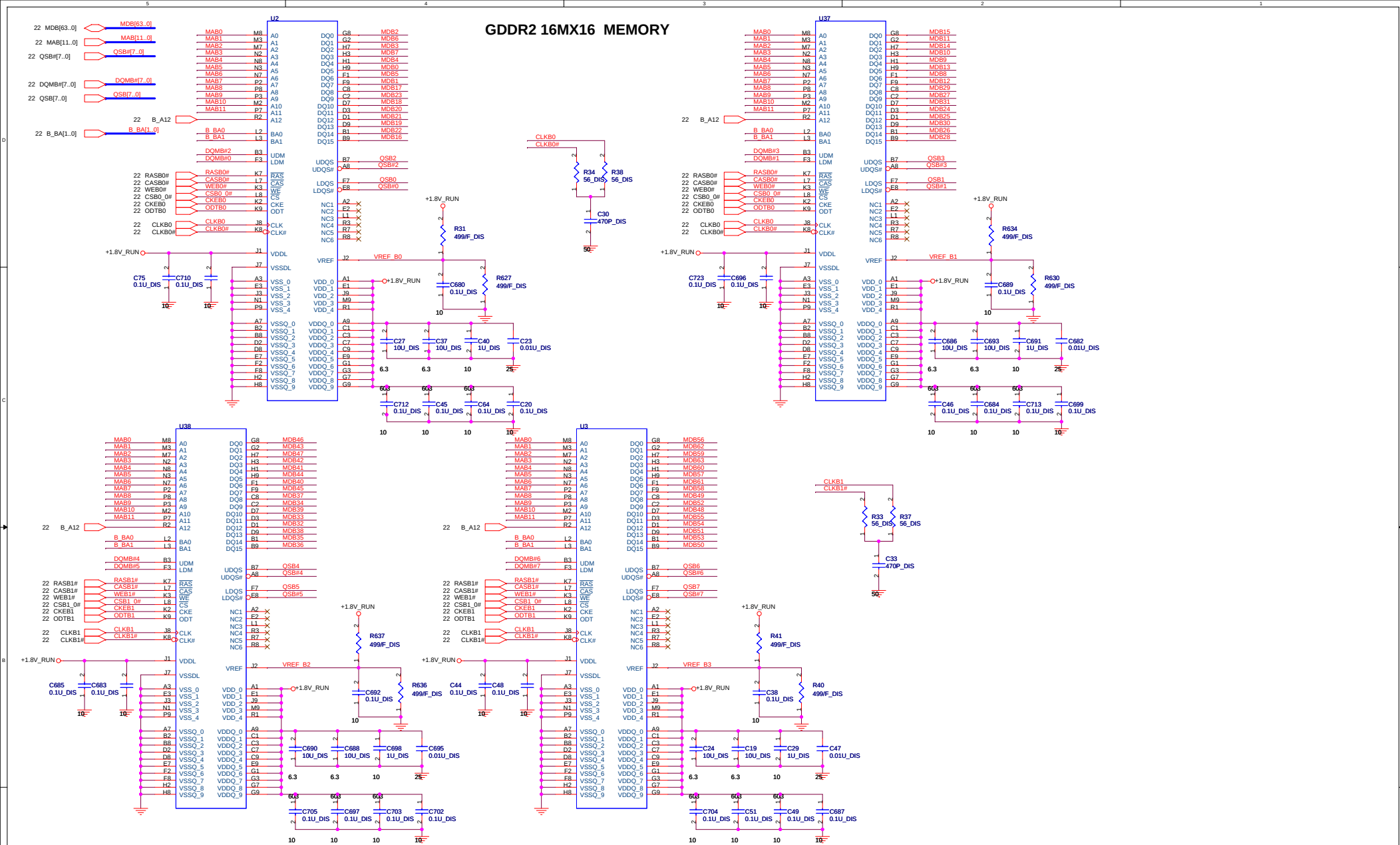
GDDR2 16MX16 MEMORY

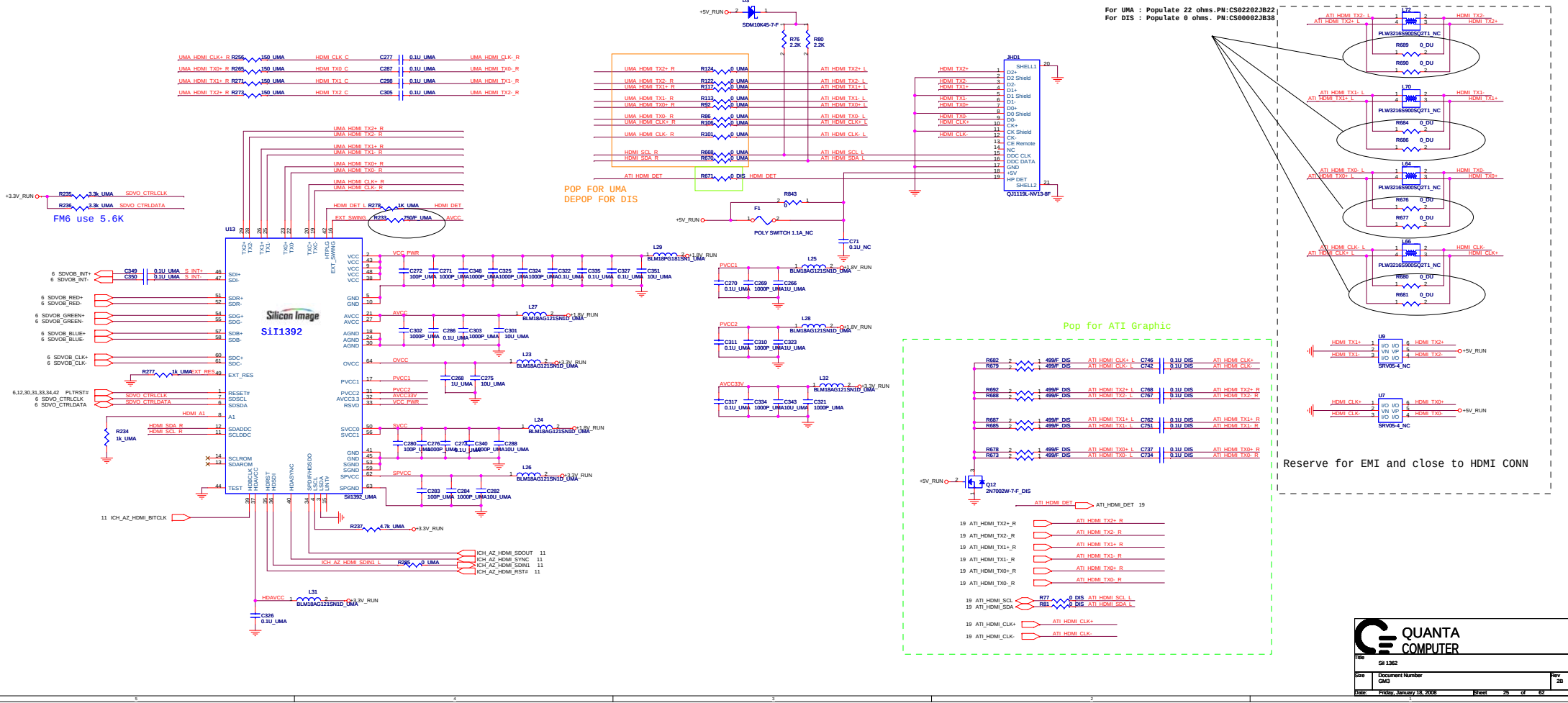
Title	VGA-M82-S (VRAM
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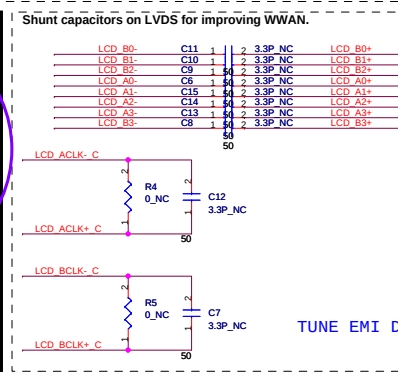
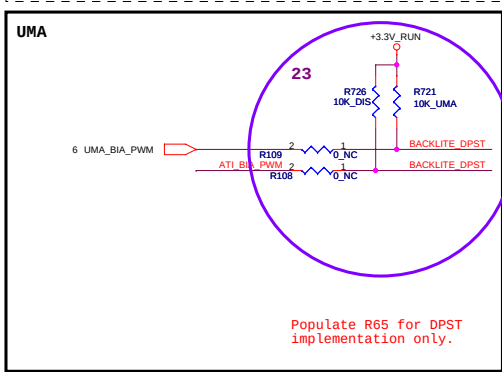
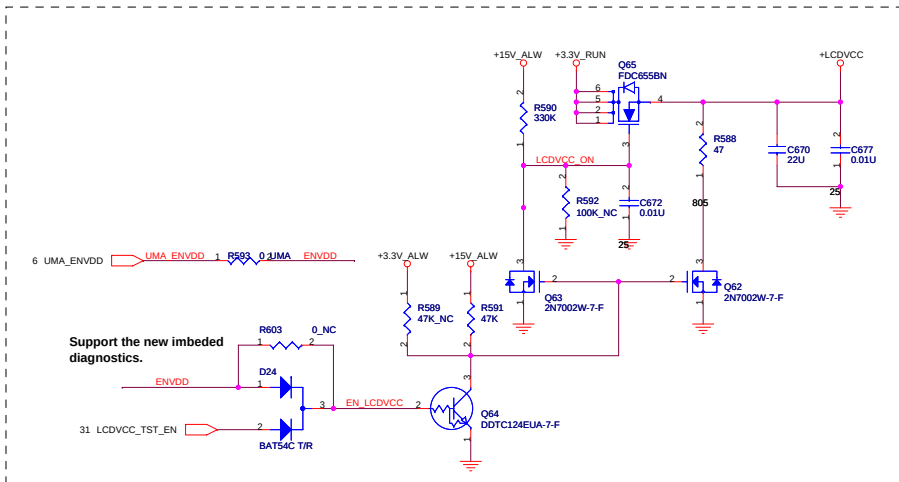
Size	Document Number
	GM3

Date: Friday, January 18, 2008

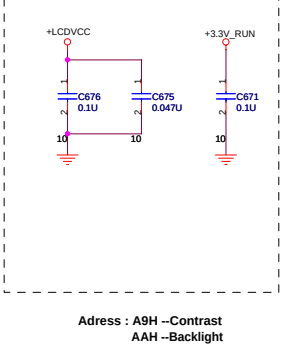
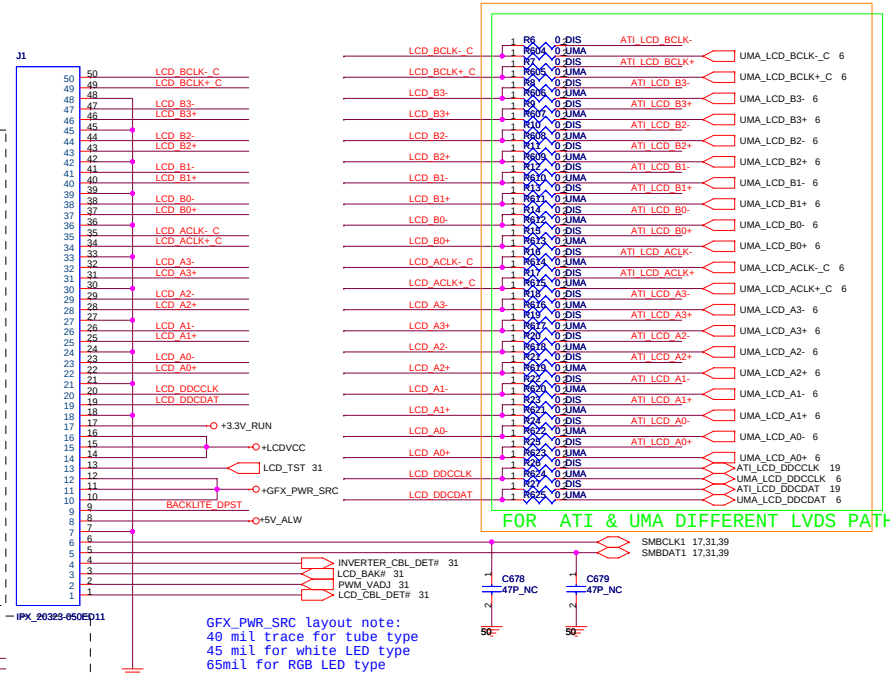
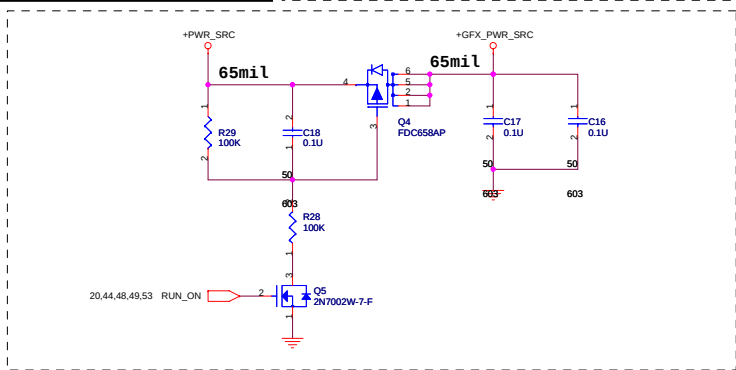
Sheet 23 of 62

GDDR2 16MX16 MEMORY

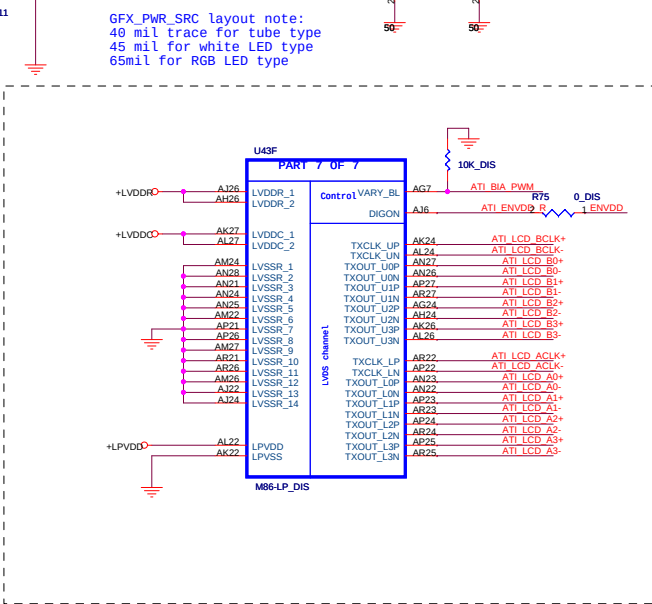


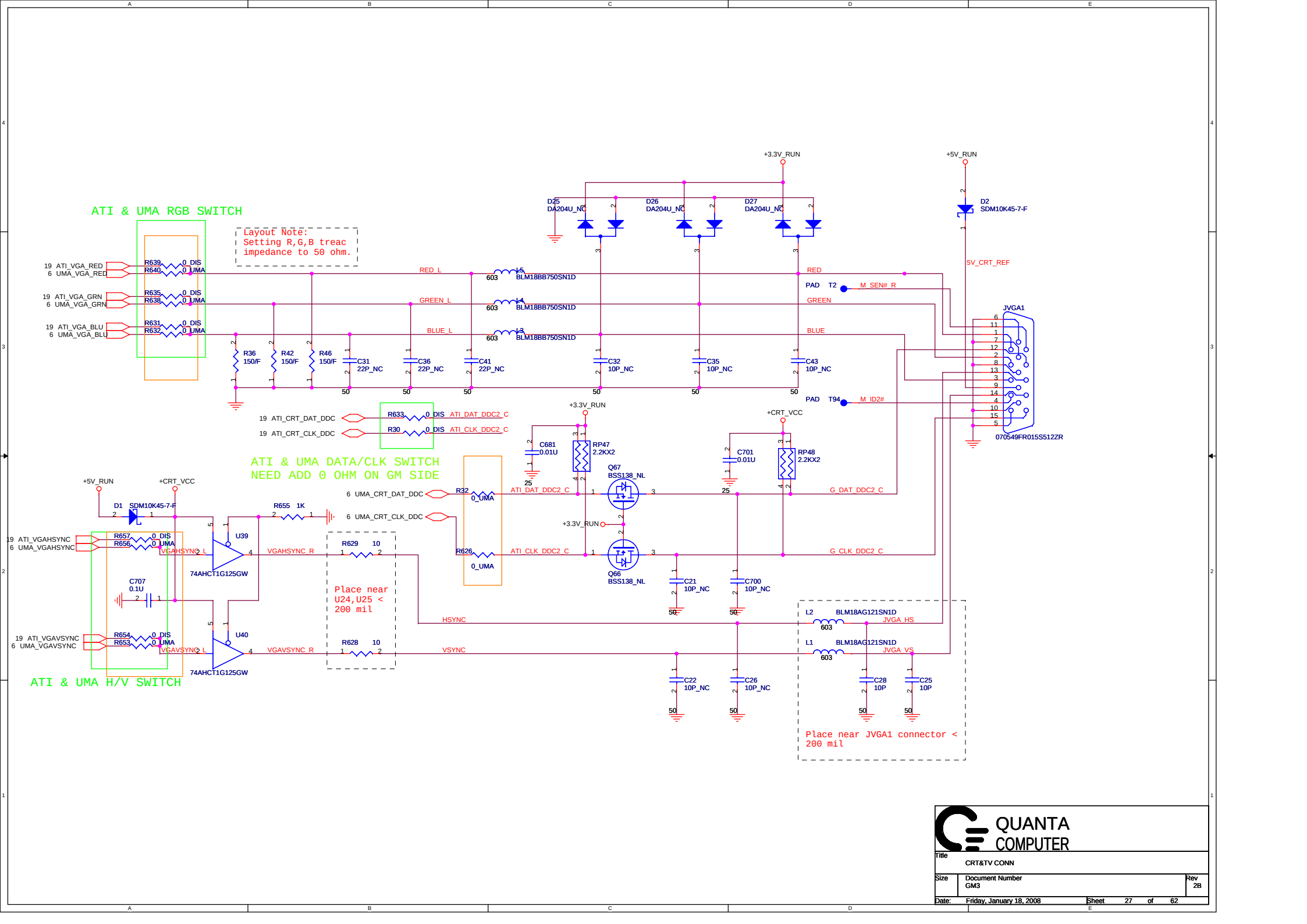


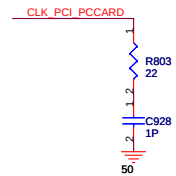
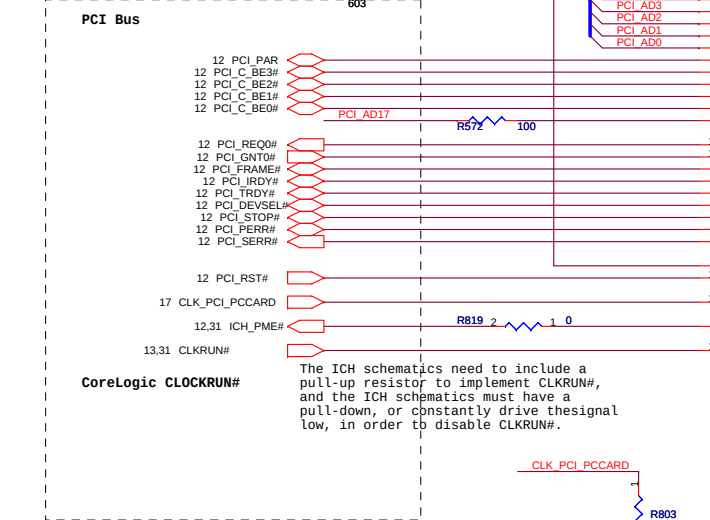
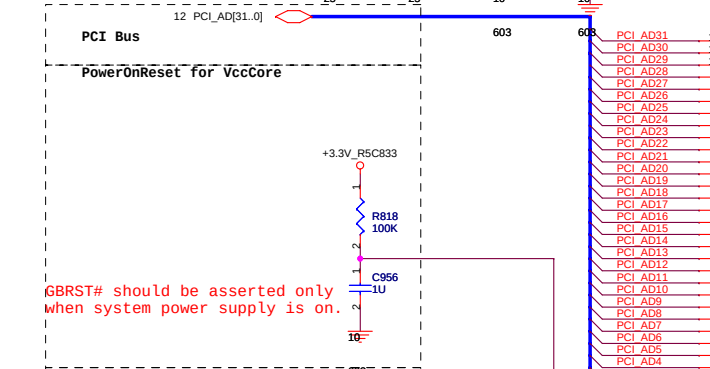
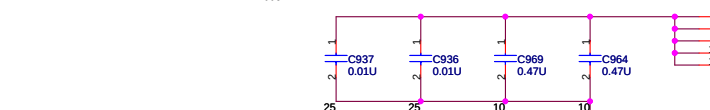
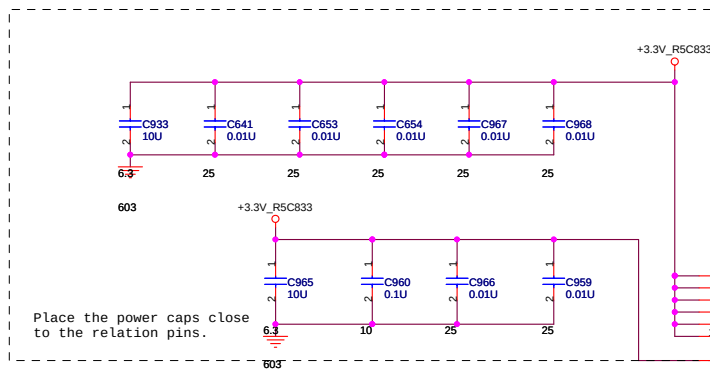
Populate R341 for platform without DPST support. No Stuff for Discrete DPST support due to back up plan.



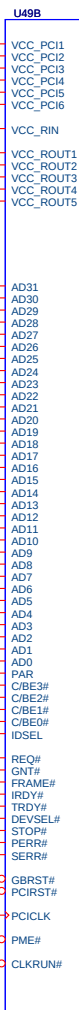
Address : A9H -Contrast
AAH -Backlight



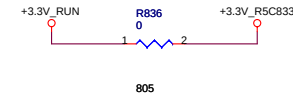
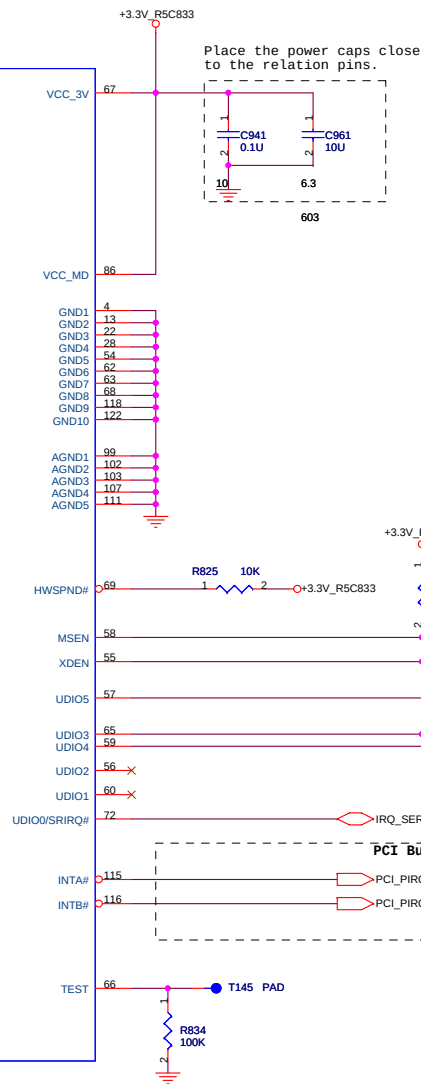




Refer to DELL
M07 schematic
X06



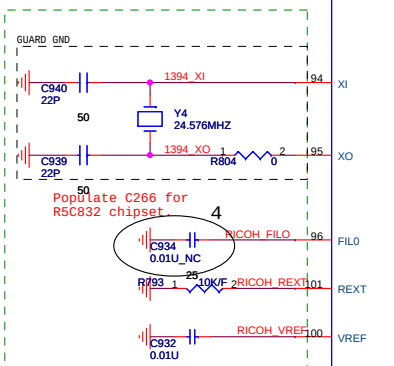
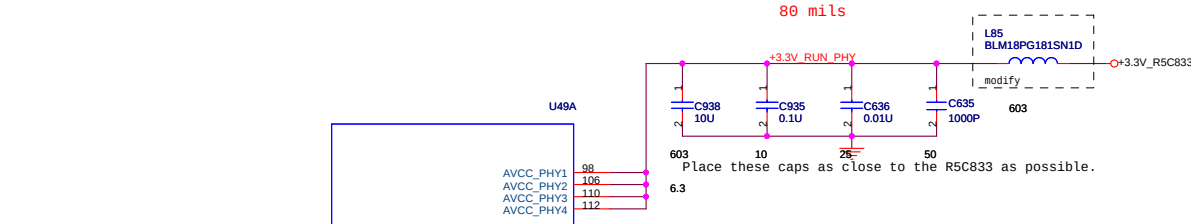
PCI / OTHER



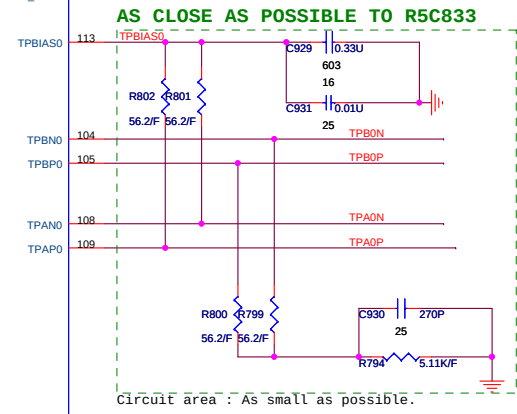
Memory Stick Enable
XD Card Enable
Serial ROM disable
SD Card Enable
MMC Card Enable

1394 Interrupt
Media card Interrupt

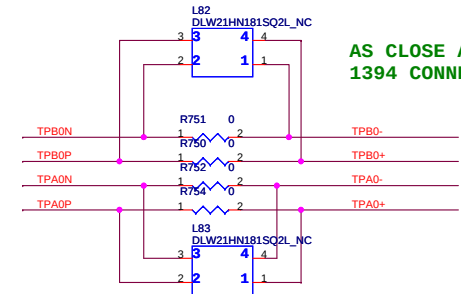
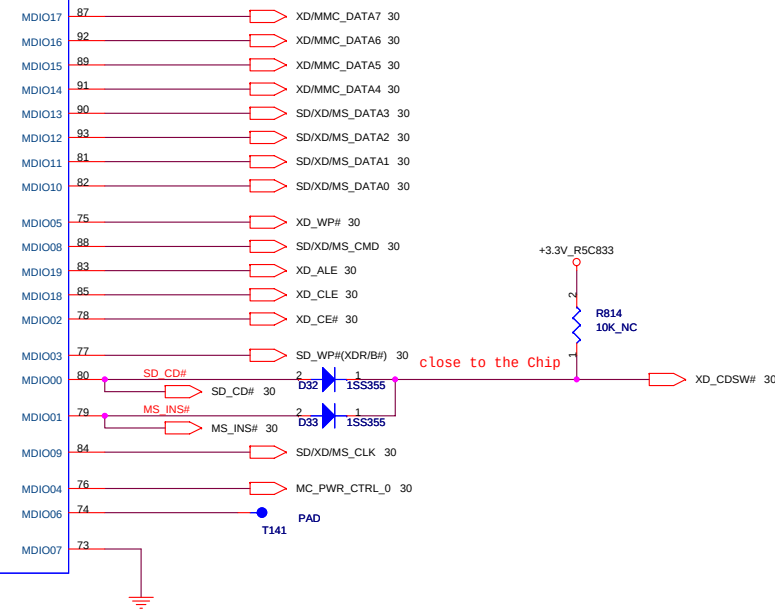




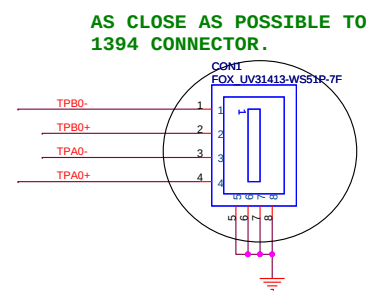
5/14:FAE review report say RC533 don't need FILO item, so NC it
Place these caps are close to the IC as possible.



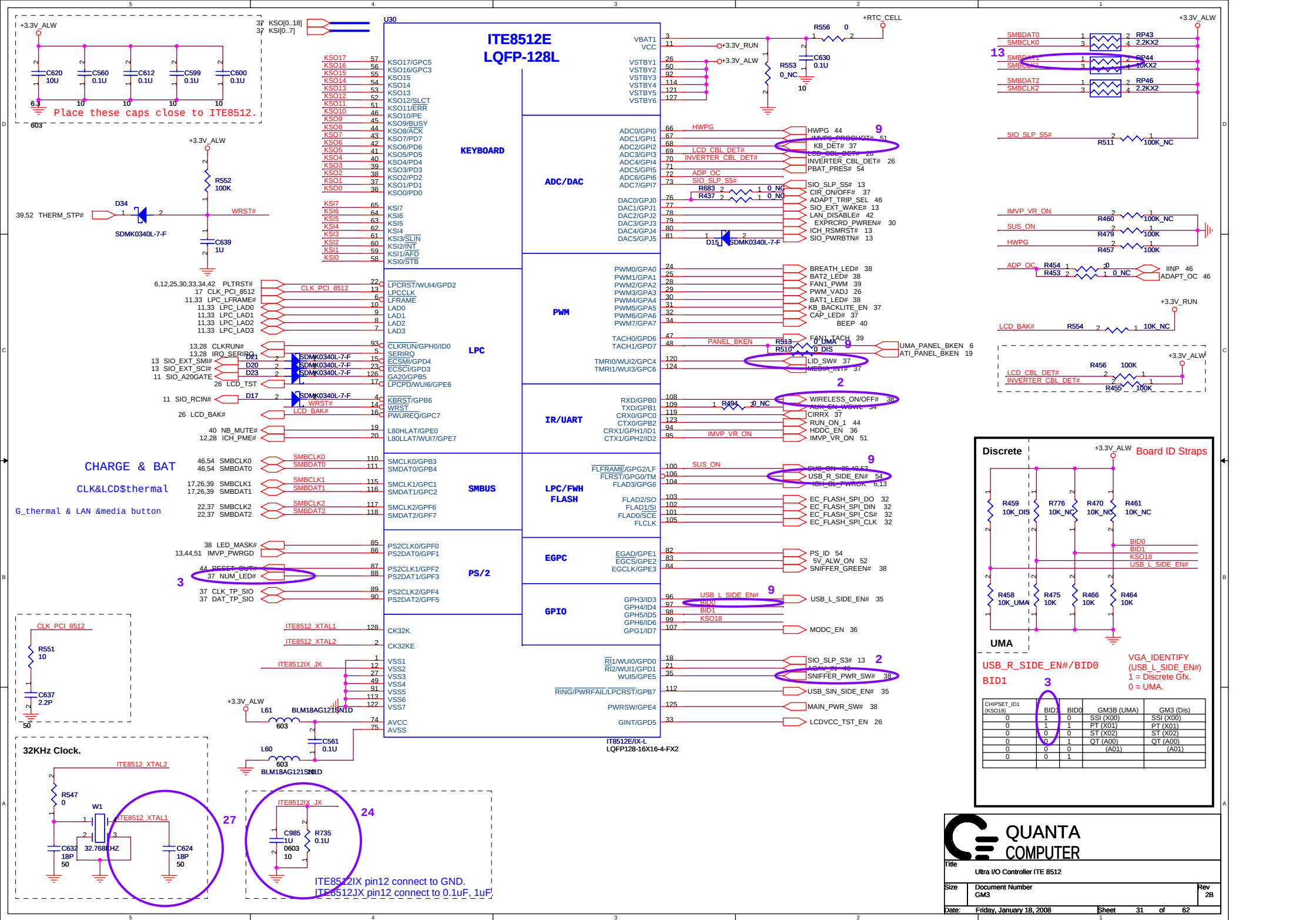
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).



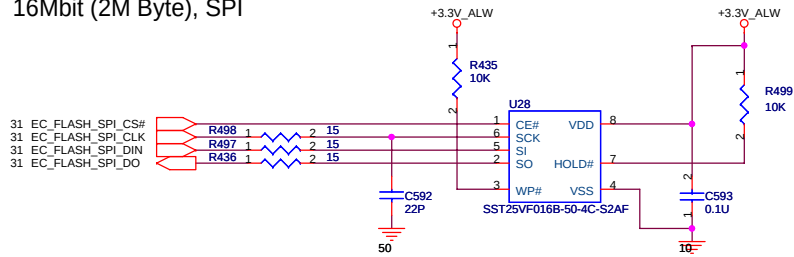
AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.



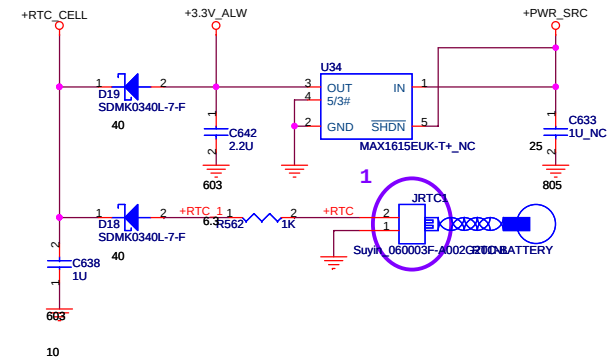
AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.



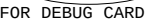
16Mbit (2M Byte), SPI



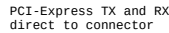
RTC BATTERY



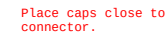
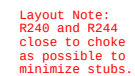
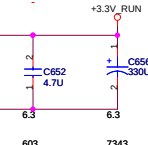
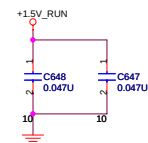
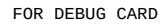
+3.3V RUN +3.3V RUN +1.5V_RUN



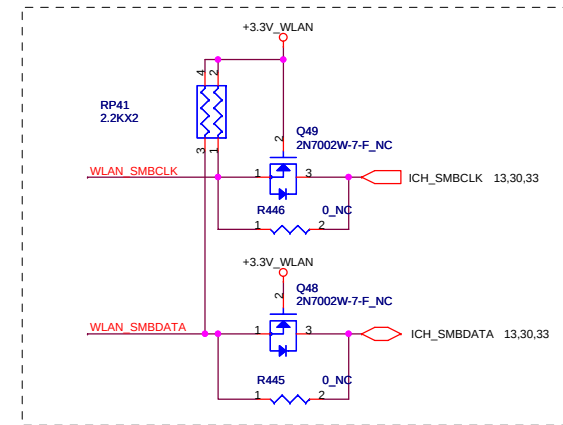
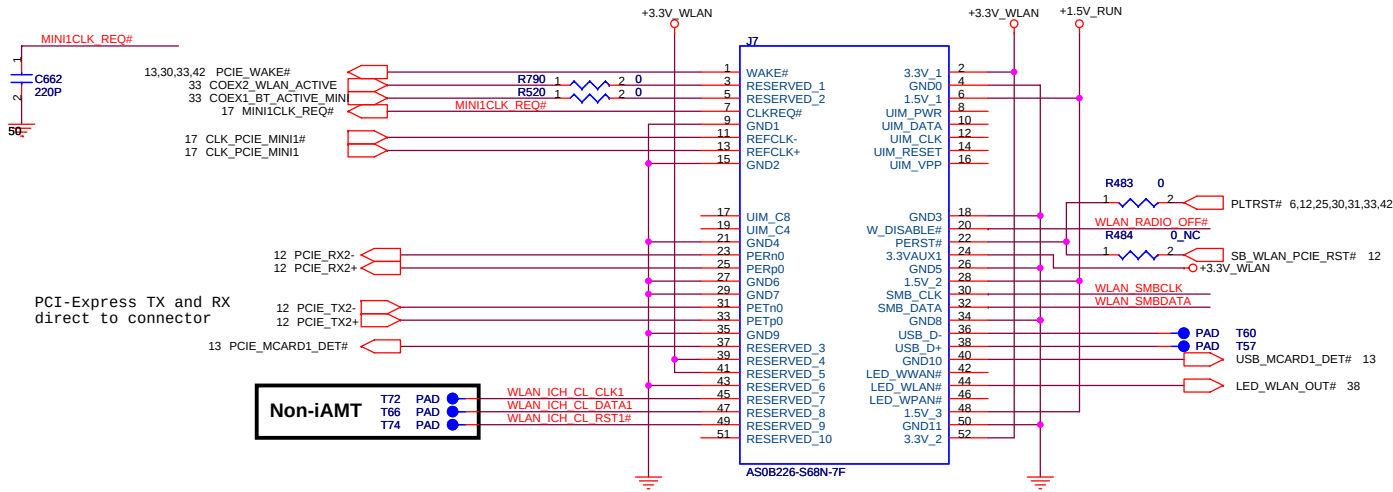
MiniCard WWAN connector



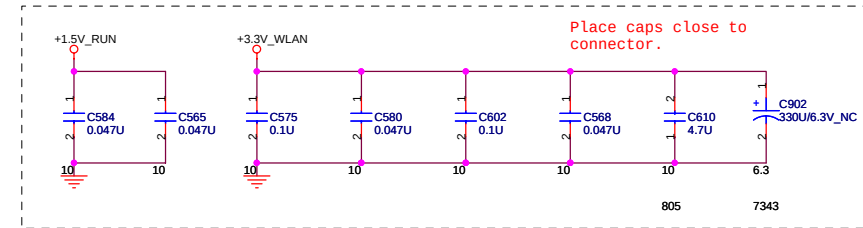
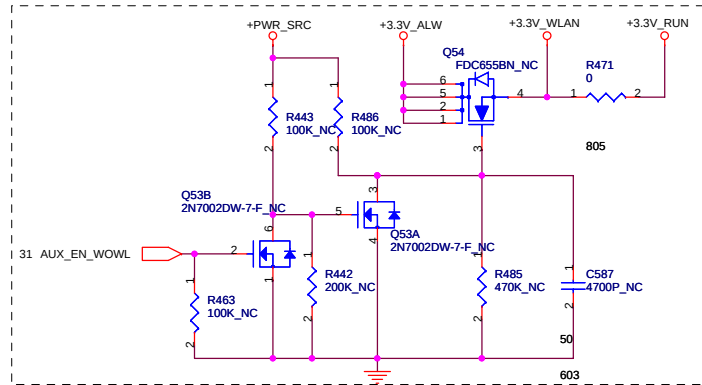
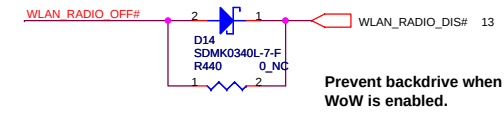
Place as close as possible to WWAN connector



MiniCard WLAN connector



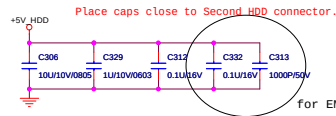
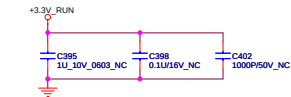
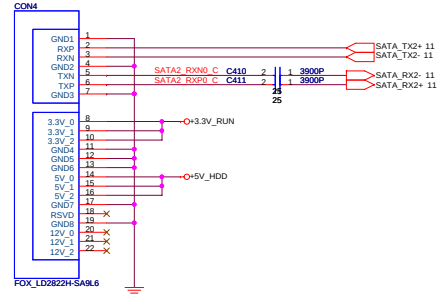
Support for WoW



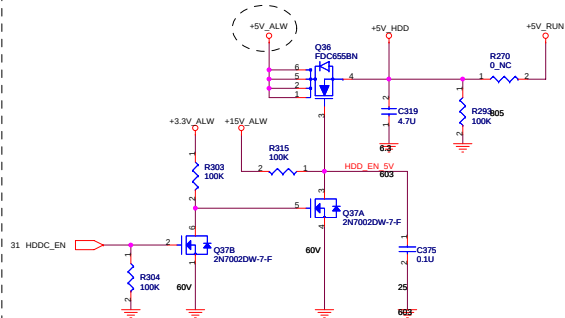
Title		
WLAN		
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SATA Connector.

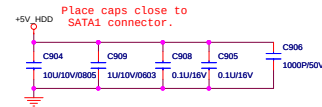
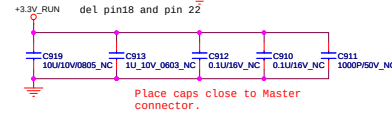
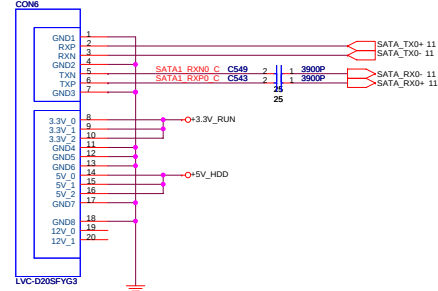
Second HDD



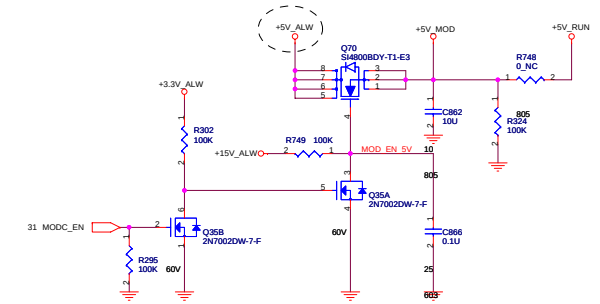
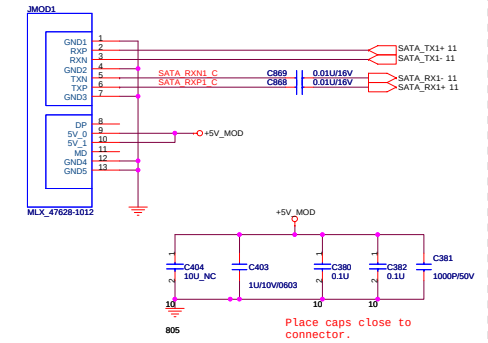
for EMI



Master

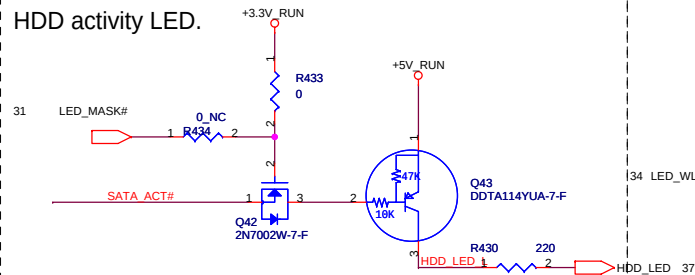


ODD Connector

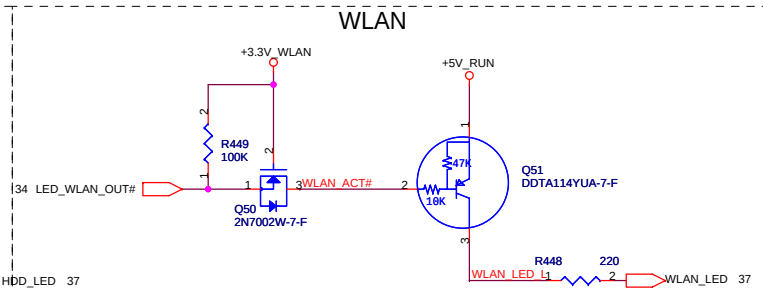


File	SATA (HDD&CD_ROM)	Rev	2B
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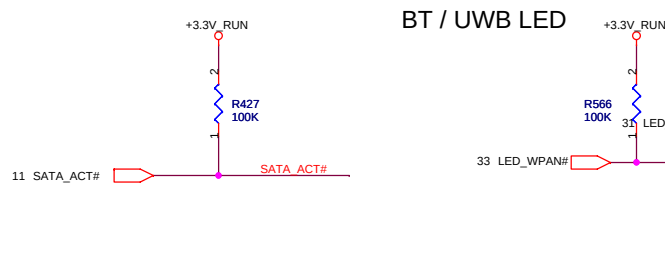
HDD activity LED.



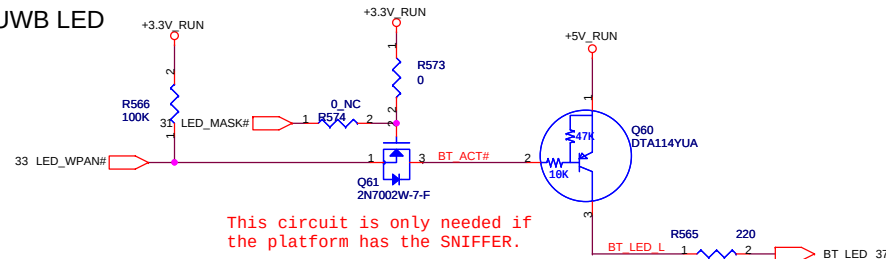
WLAN



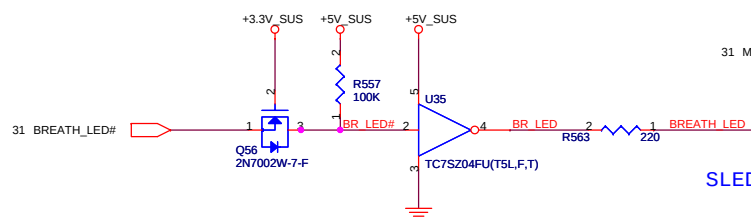
BT / UWB LED



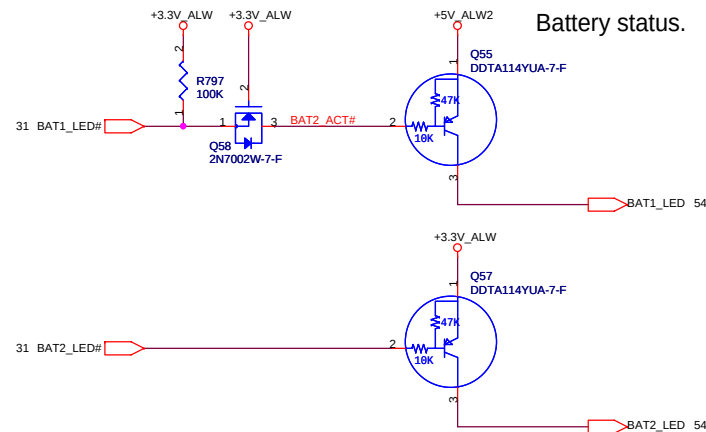
This circuit is only needed if the platform has the SNIFFER.



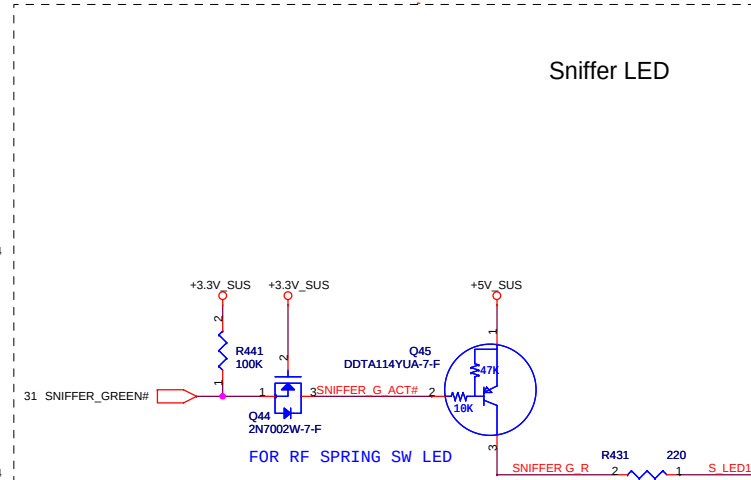
Power & Suspend.



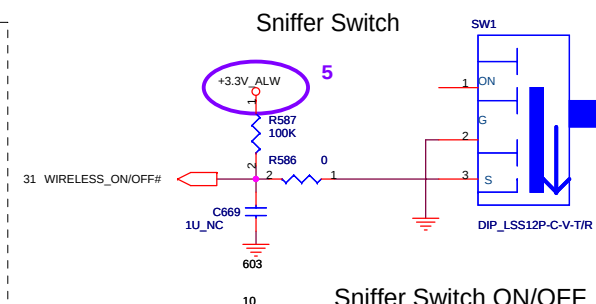
Battery status.



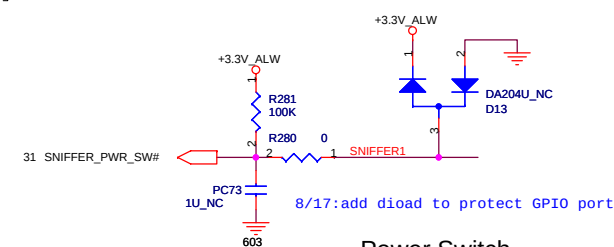
Sniffer LED



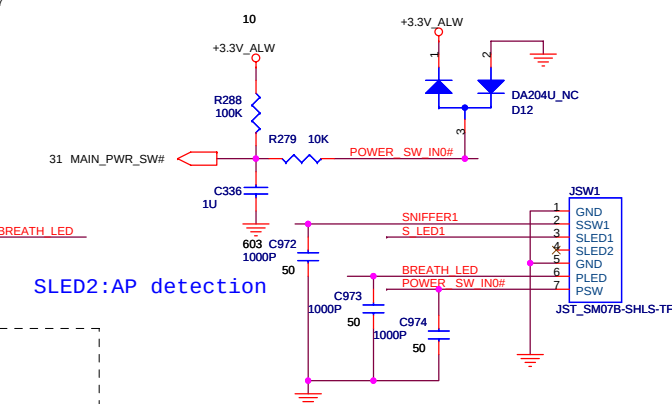
Sniffer Switch



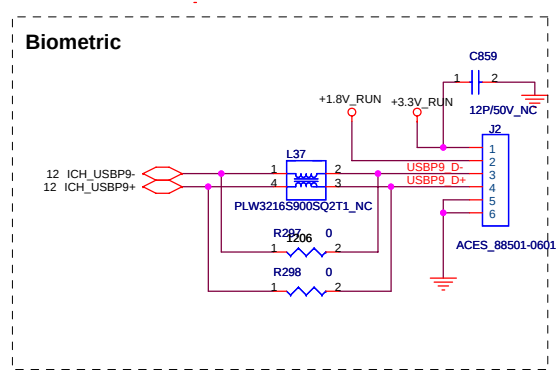
Sniffer Switch ON/OFF



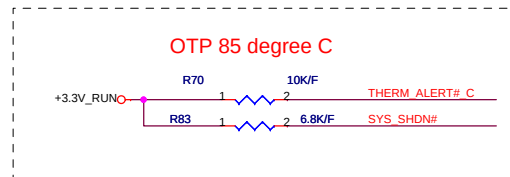
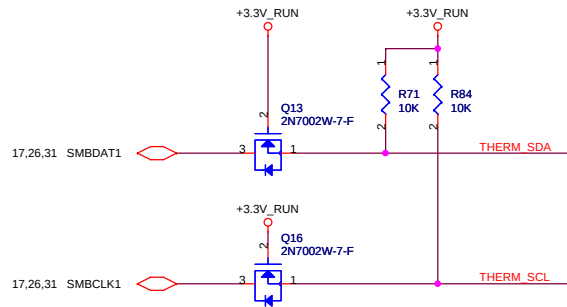
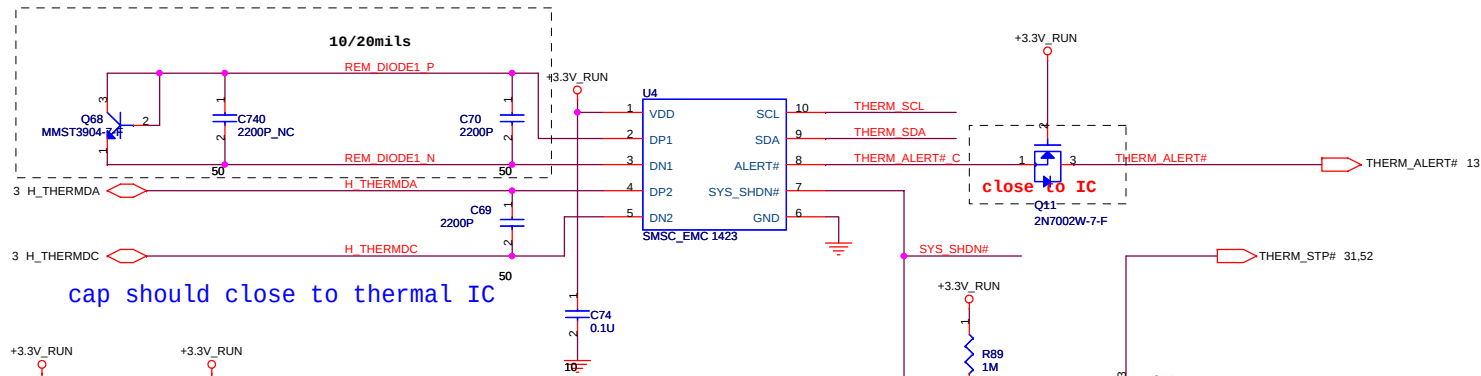
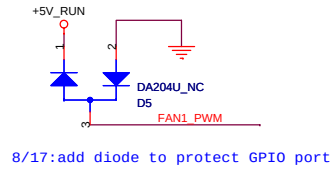
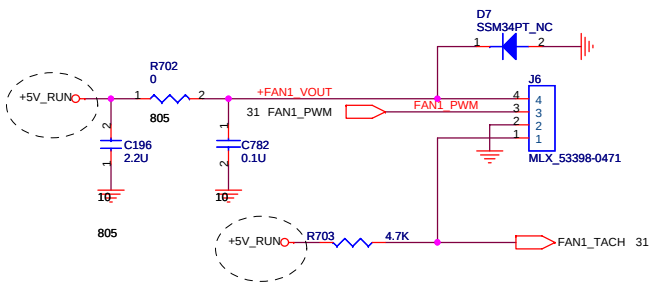
Power Switch



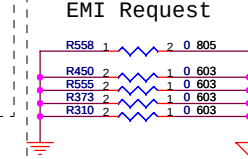
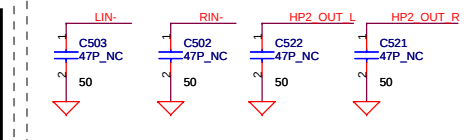
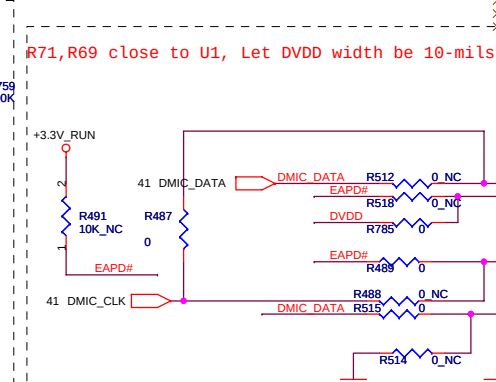
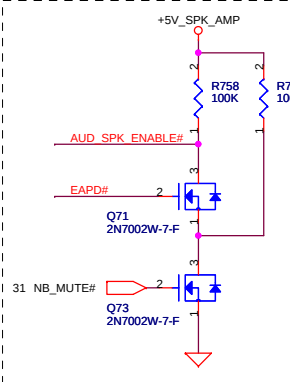
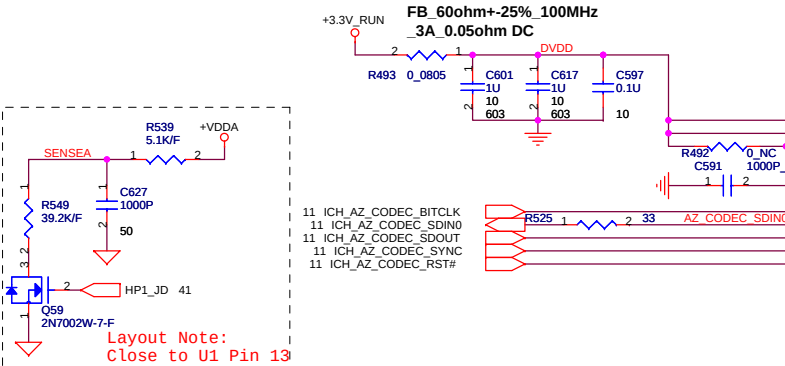
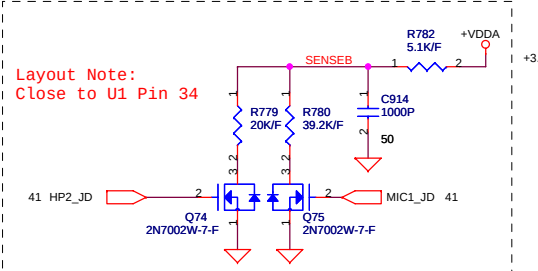
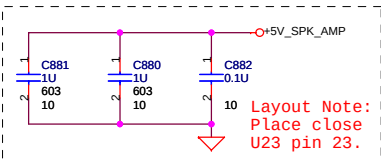
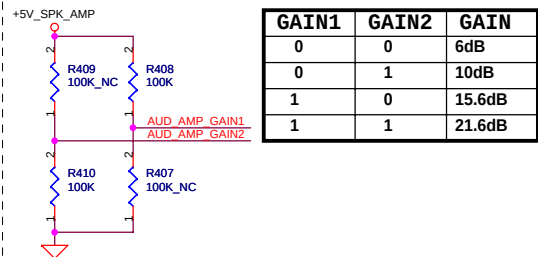
Biometric



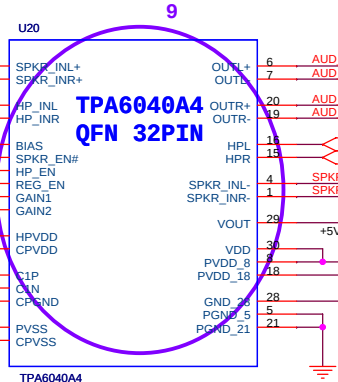
Title			
SWITCH, KEYBOARD & LED			
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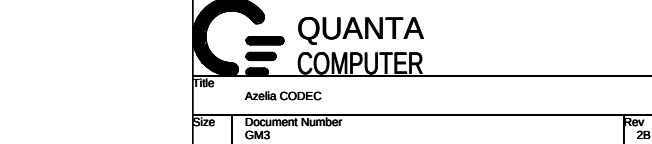
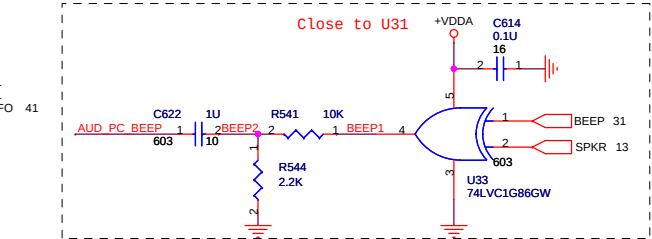
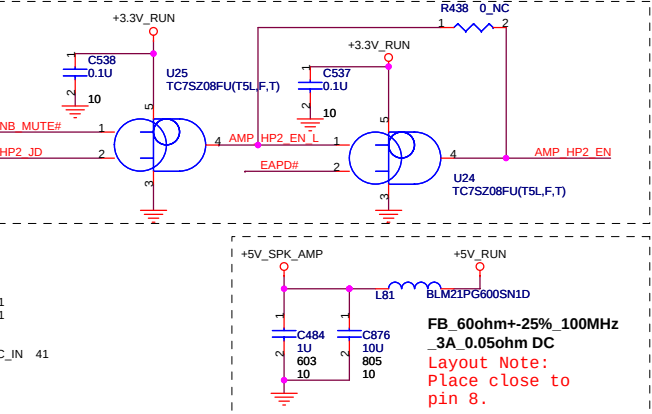
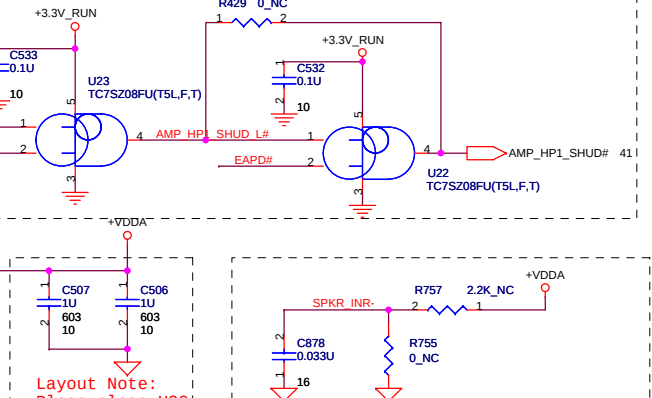
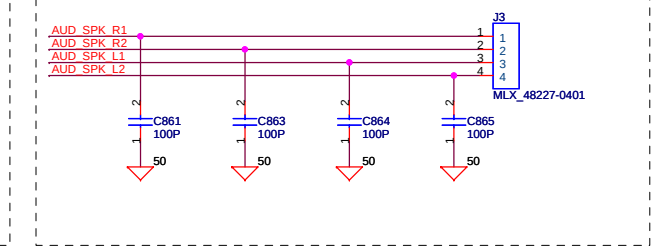
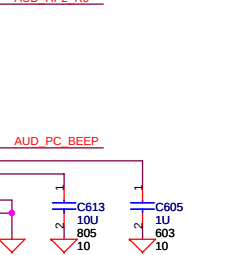
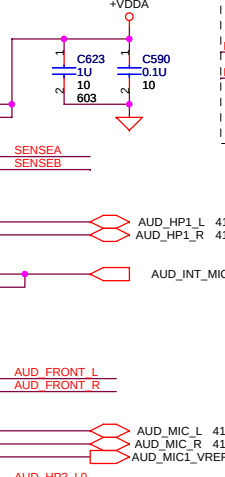
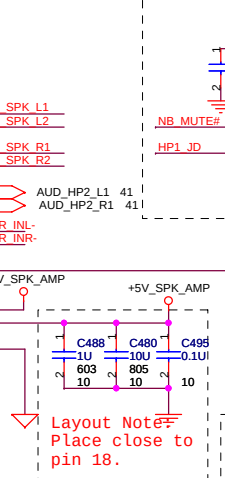
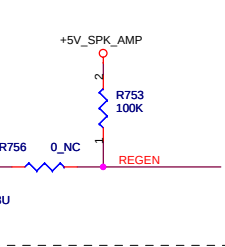
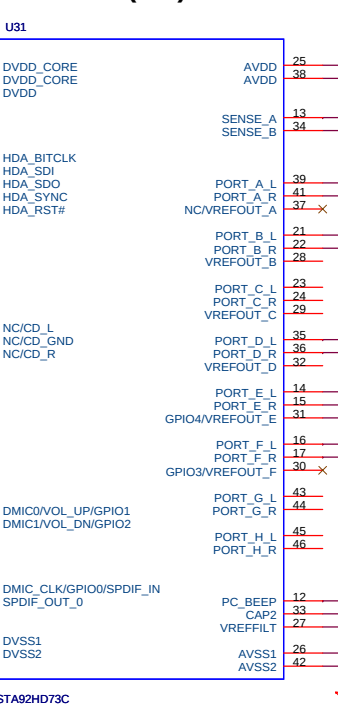
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



INTERNAL SPEAKER AMP



AZALIA (HD) CODEC

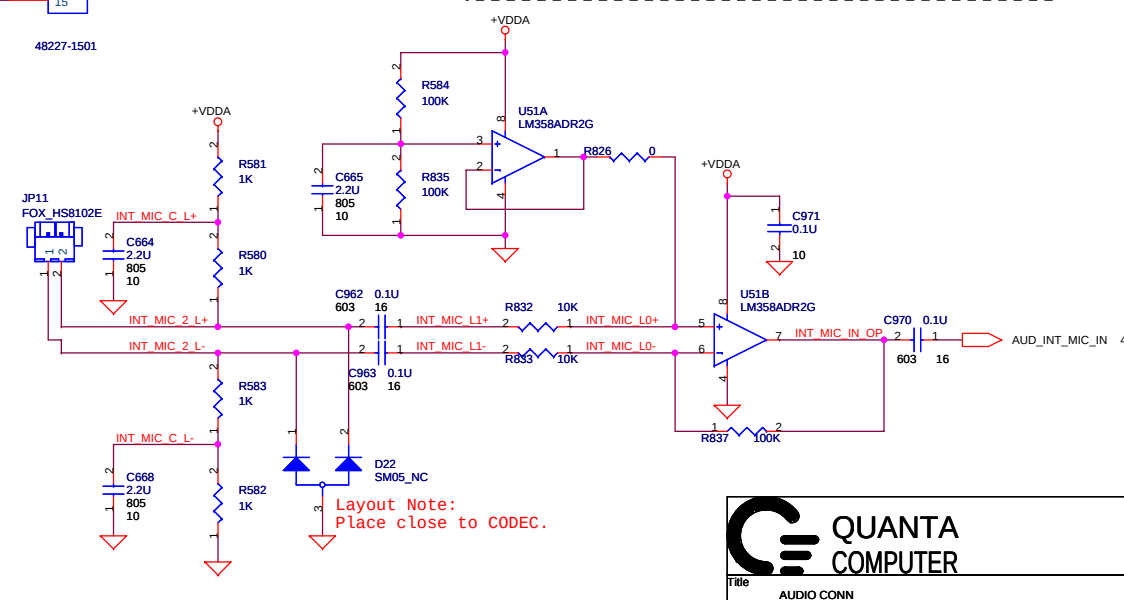
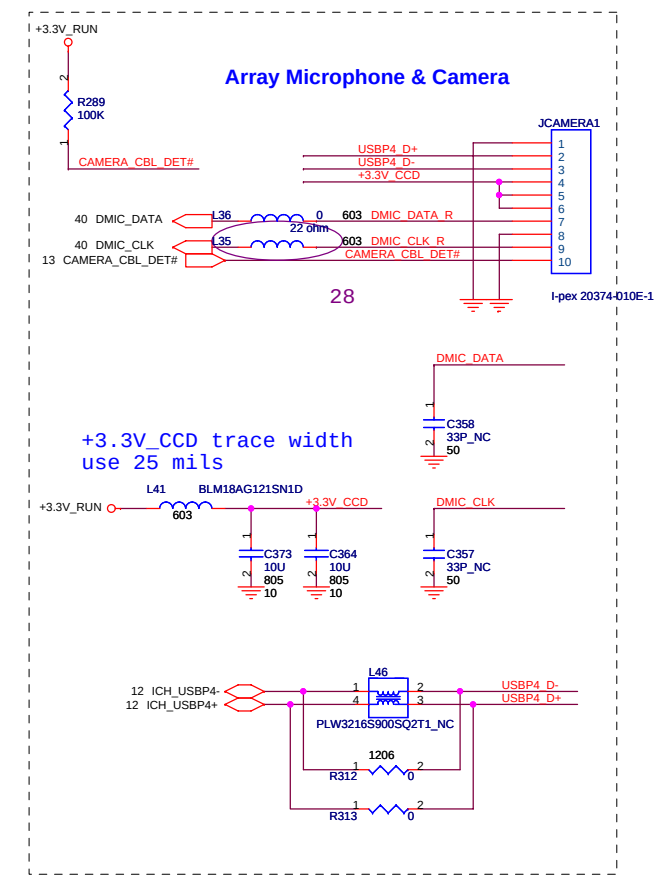
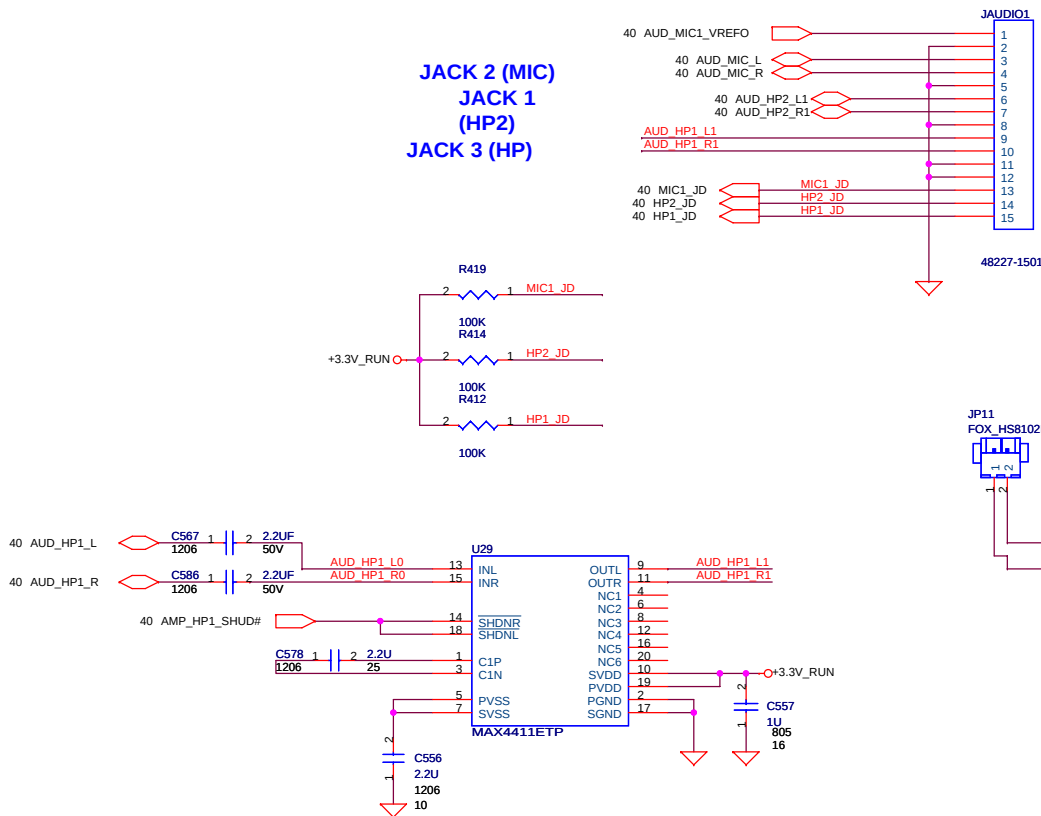


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Title Azalia CODEC		Rev 2B
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Headphone Jack Stereo MIC Jack

JACK 2 (MIC)
JACK 1
(HP2)
JACK 3 (HP)

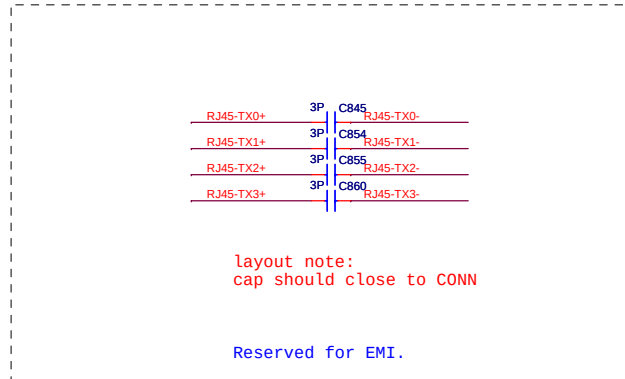
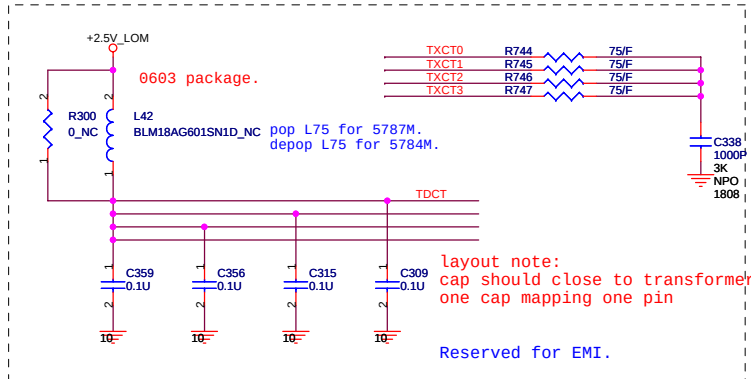
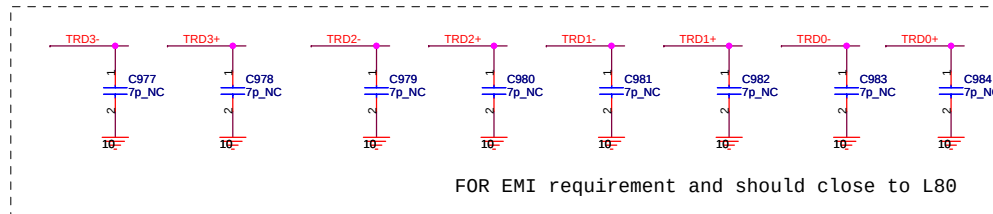
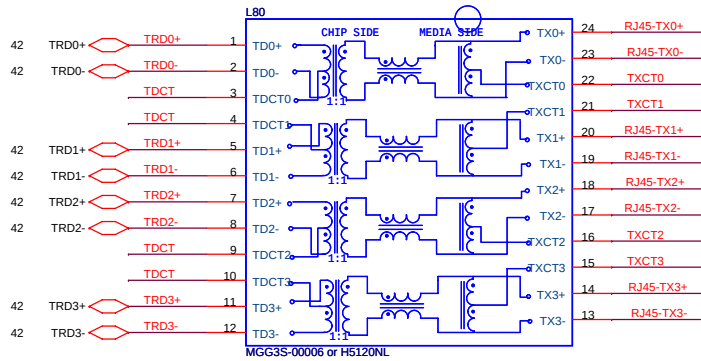


Layout Note:
Place close to CODEC.

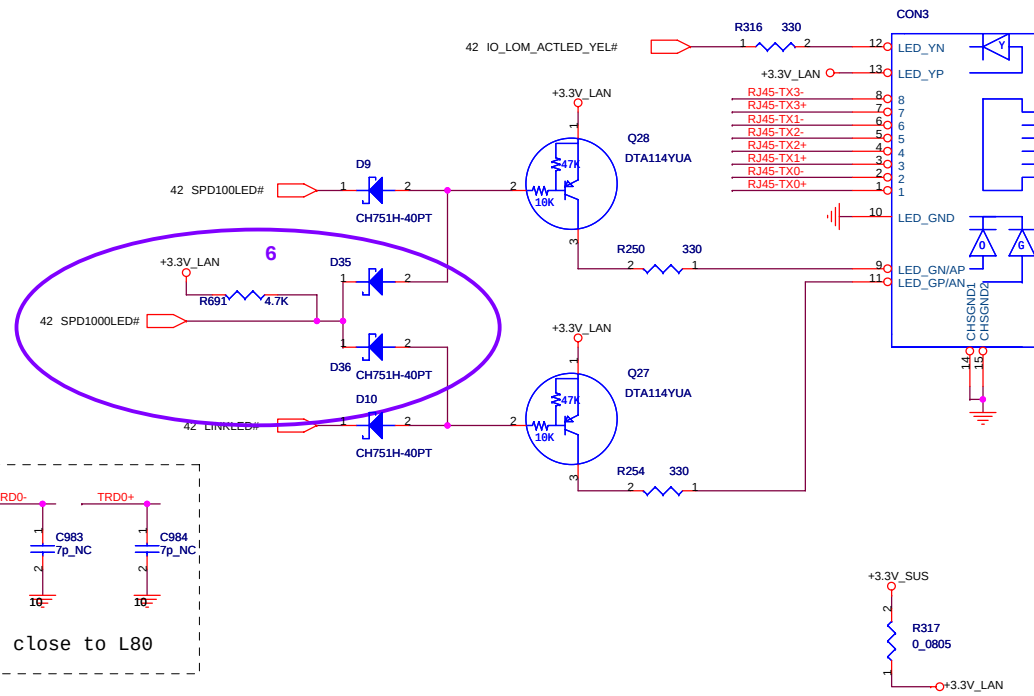
QUANTA
COMPUTER

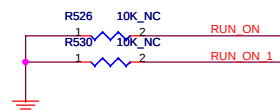
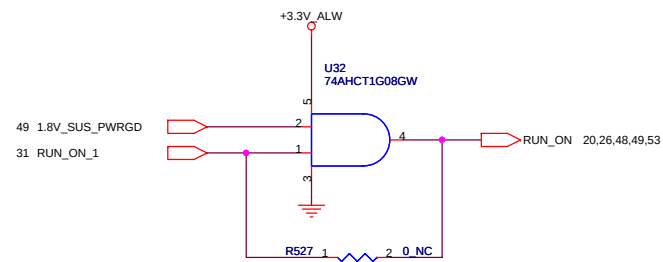
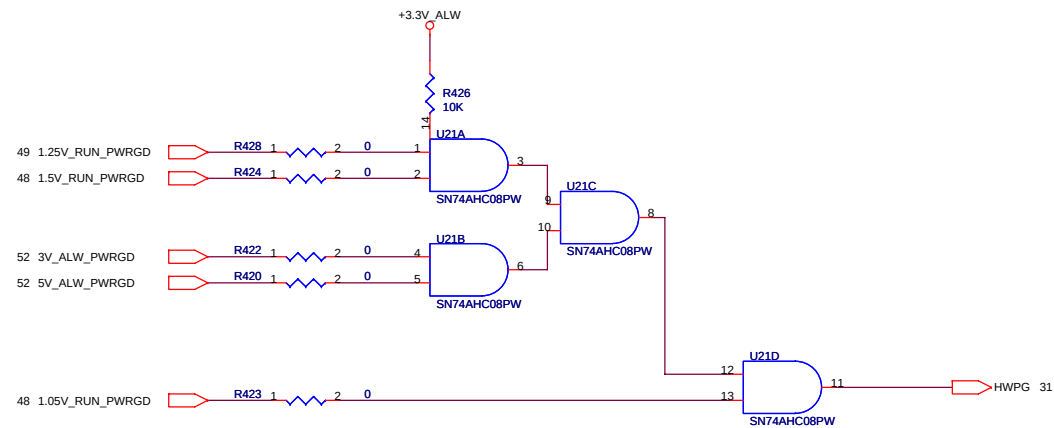
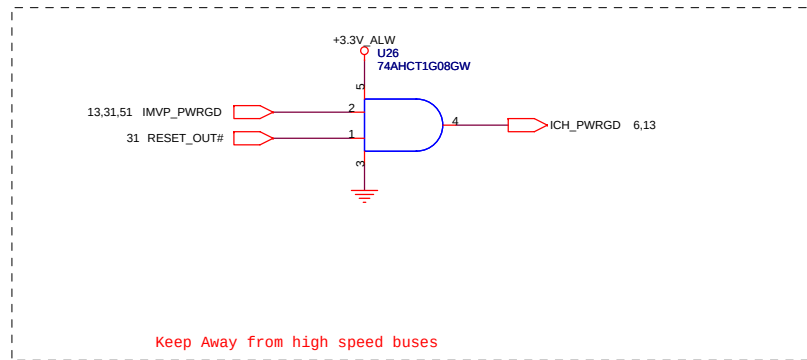
Title		
AUDIO CONN		
Size	Document Number	Rev
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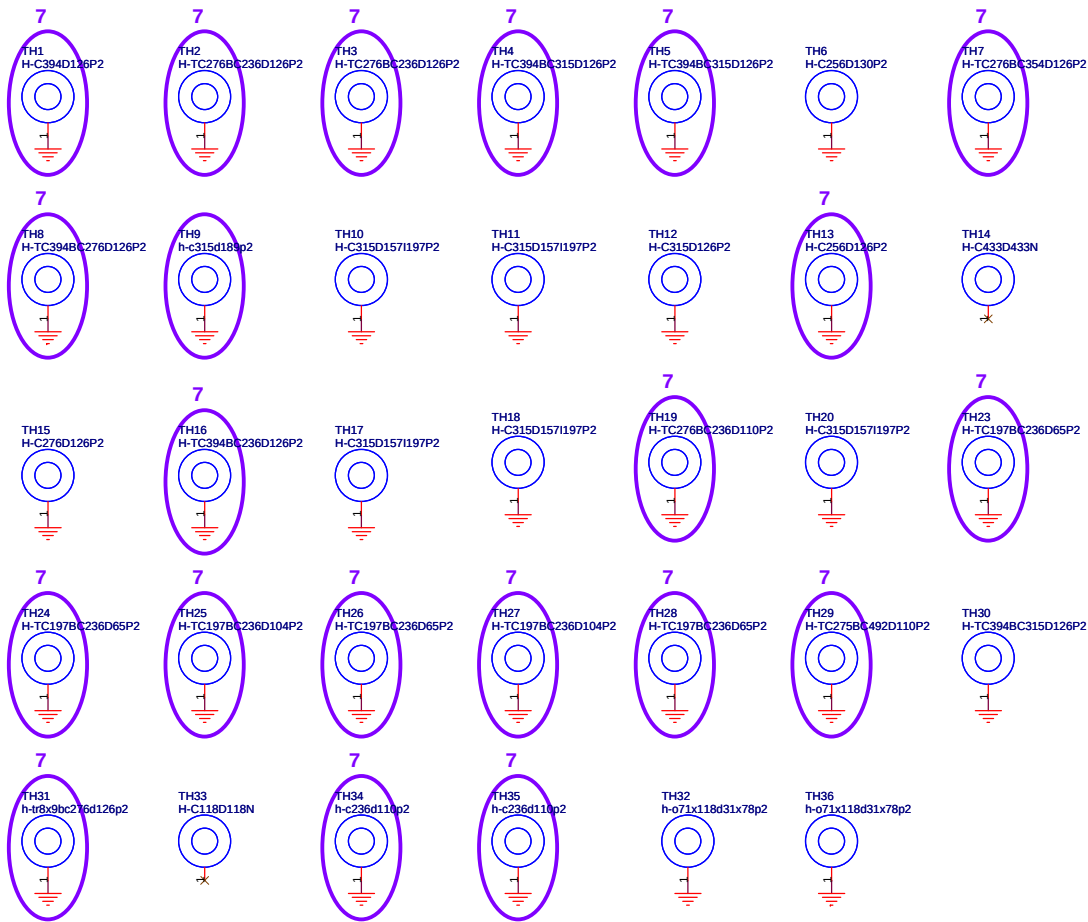
TRANSFORM



RJ-45 Connector







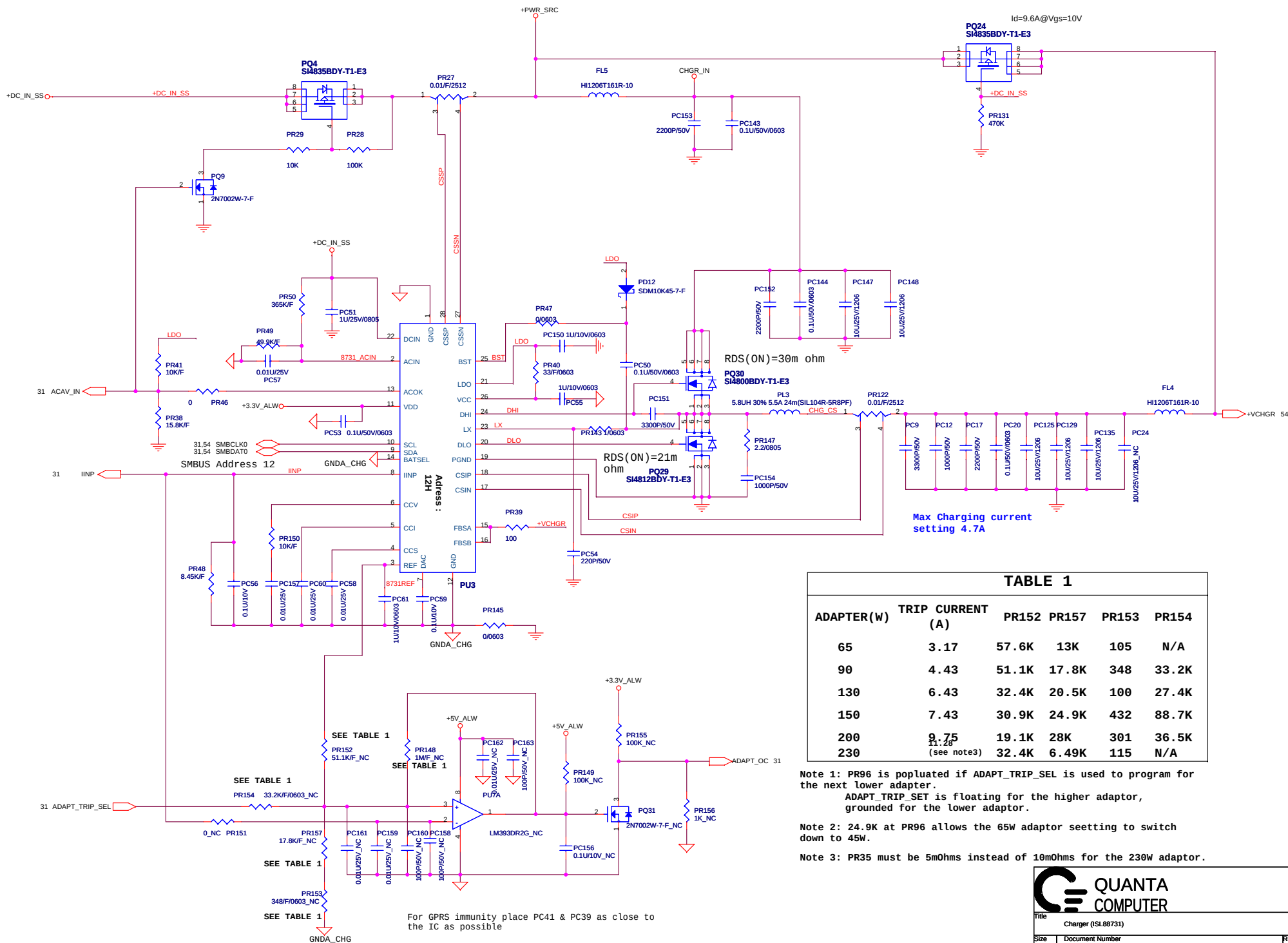


TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	PR152	PR157	PR153	PR154
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28 (see note3)	32.4K	6.49K	115	N/A

Note 1: PR96 is populated if ADAPT_TRIP_SEL is used to program for the next lower adaptor.

ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR96 allows the 65W adaptor setting to switch down to 45W.

Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.



Title
Charger (SL88731)

Size
Document Number
GM3

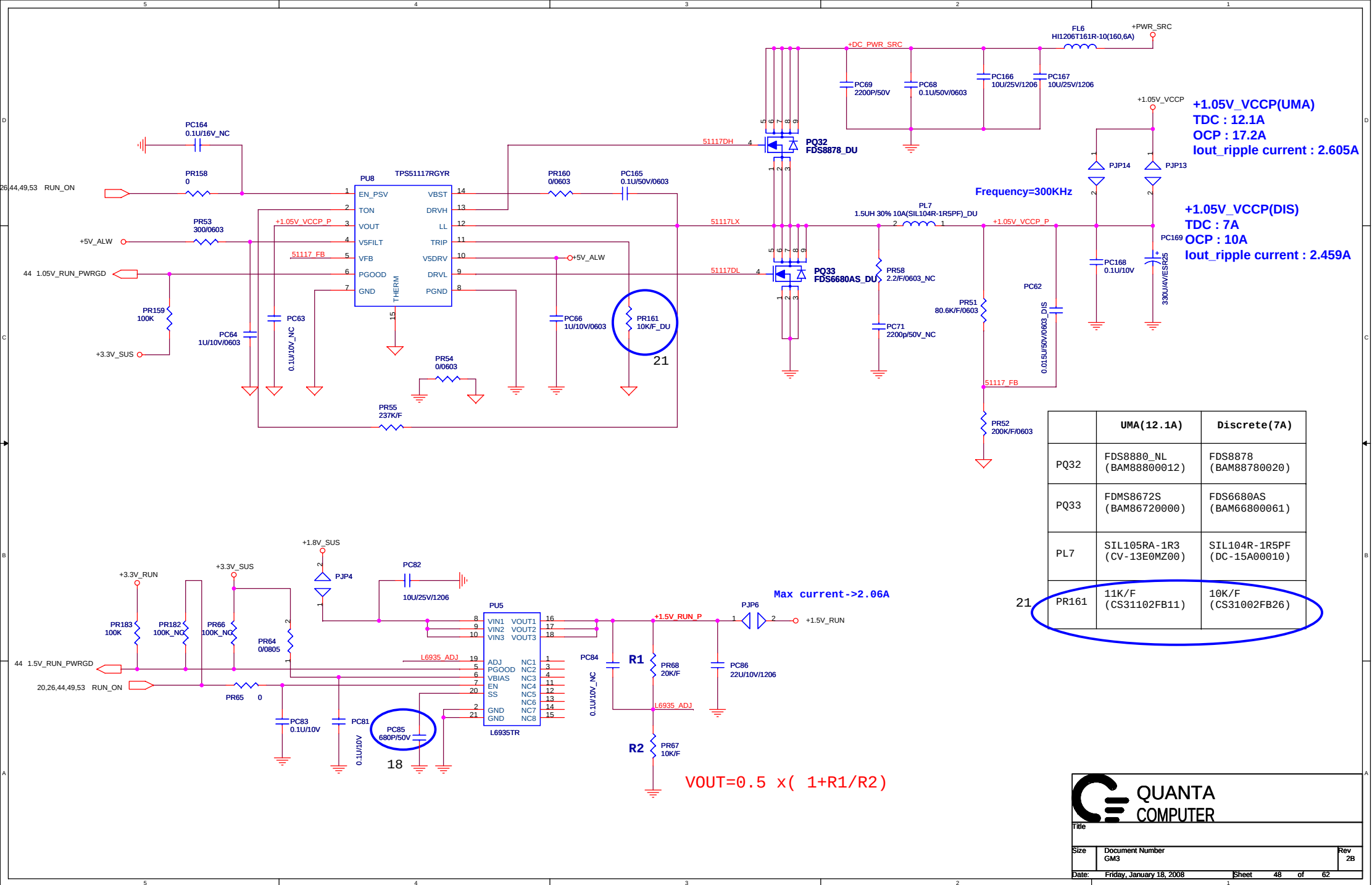
Date: Friday, January 18, 2008

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Rev 2B

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NUMBER SAME AS DISCRETE**

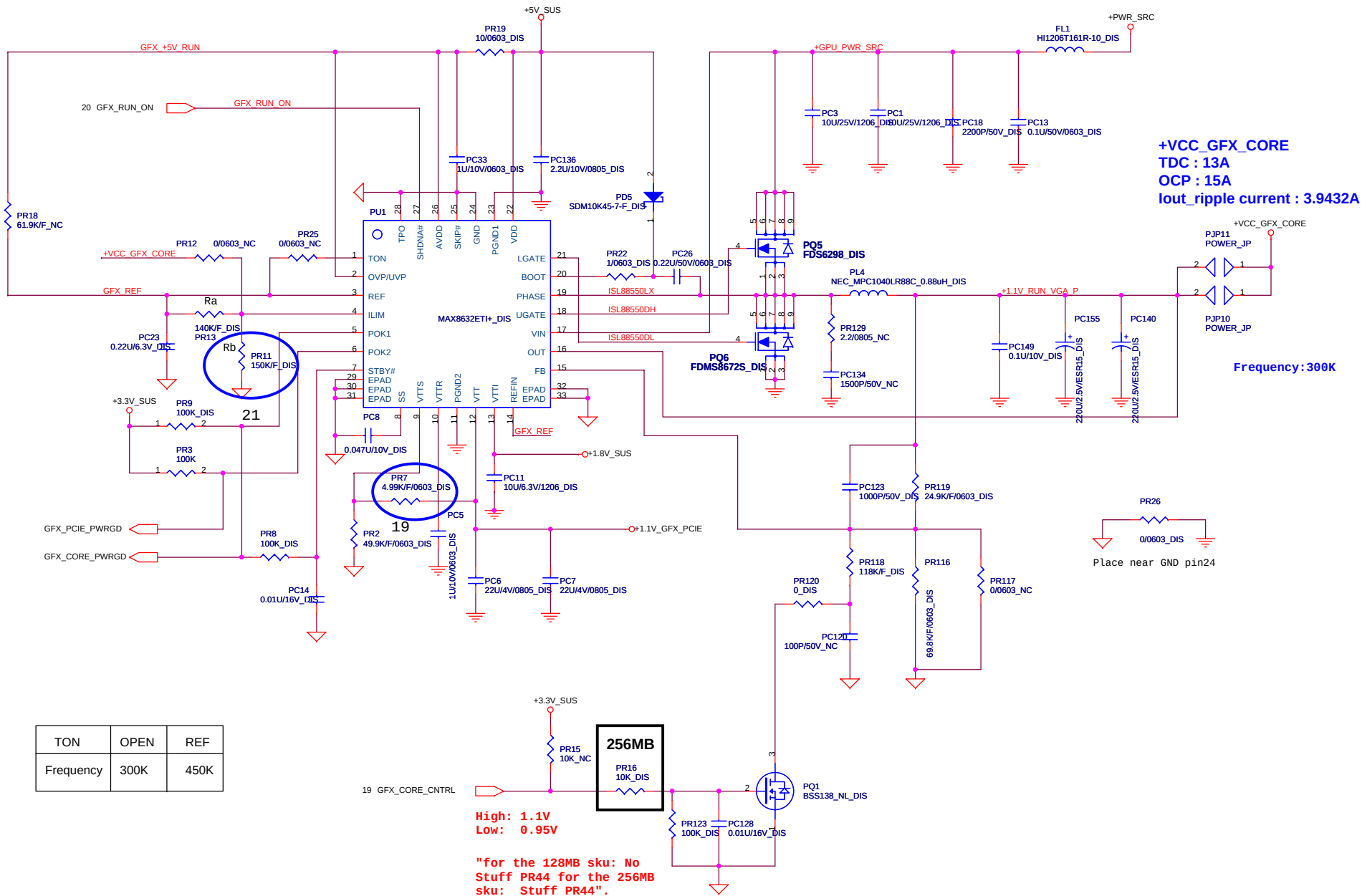
 QUANTA COMPUTER		
Title		
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PR172	10.5K/F/0603 (CS31053F909)	13.3K/F/0603 (CS31333F919)
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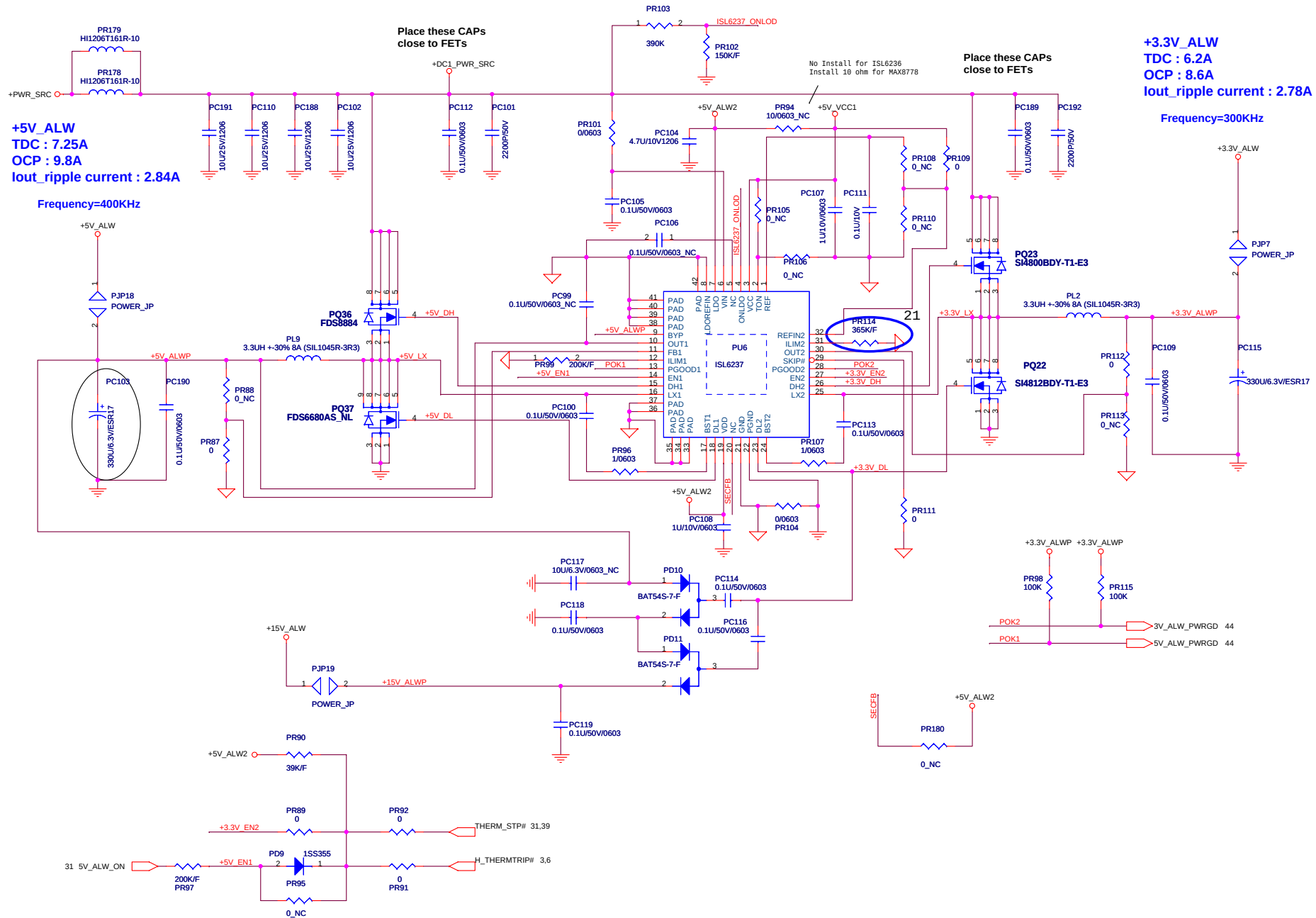
+1.8V_SUS(UMA)
TDC : 10.25A
OCP : 14.9A
Iout_ripple current : 4.868A

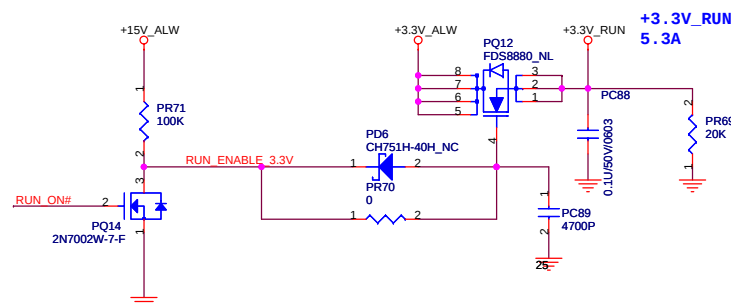
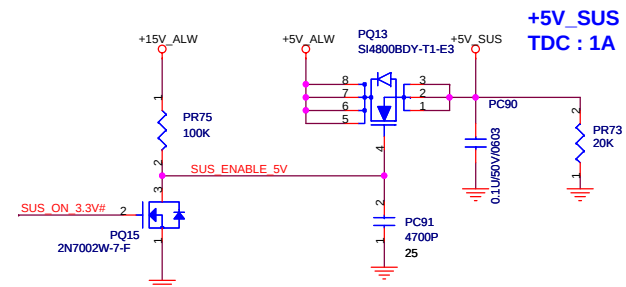
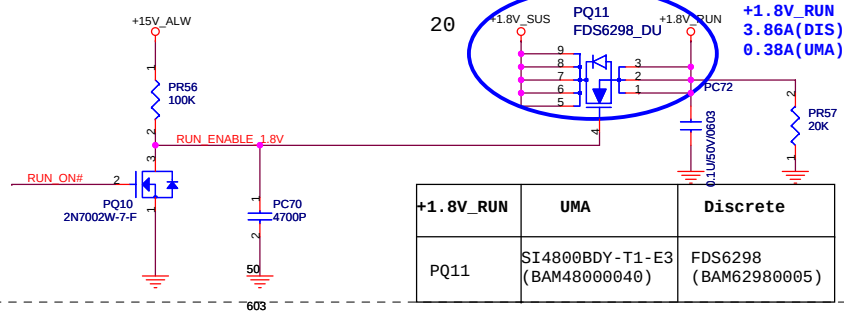
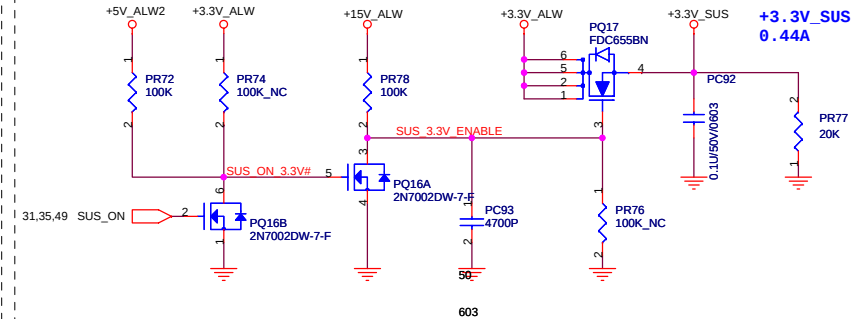
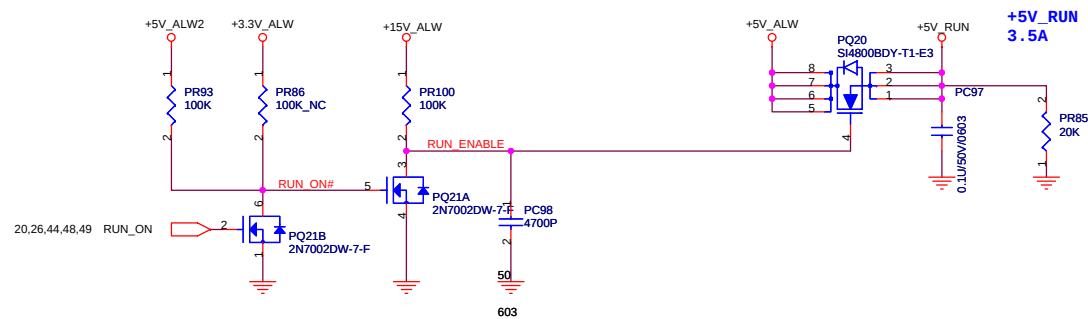




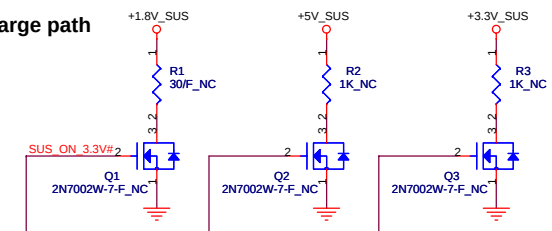
ILIM	$I_{ovp} = (2 * (R_b / (R_a + R_b)) * 0.1 * (1 / R_{DS(on)}) + (I_{\Delta} / 2)$
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVF	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.

DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW

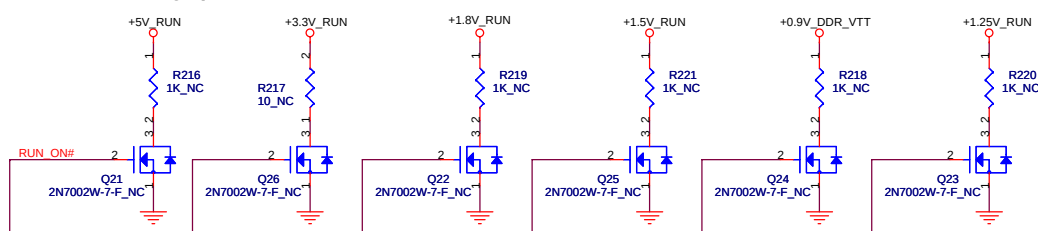


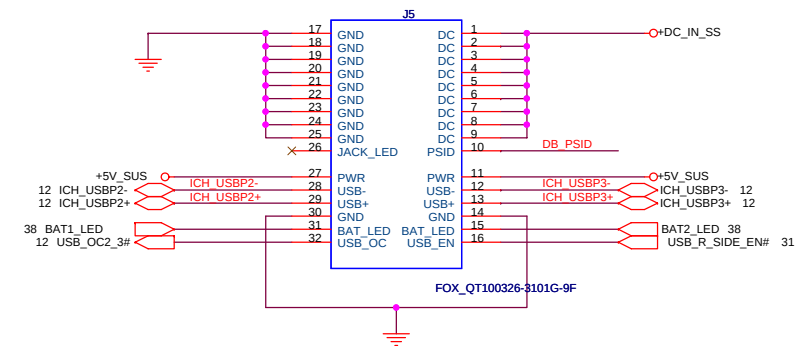
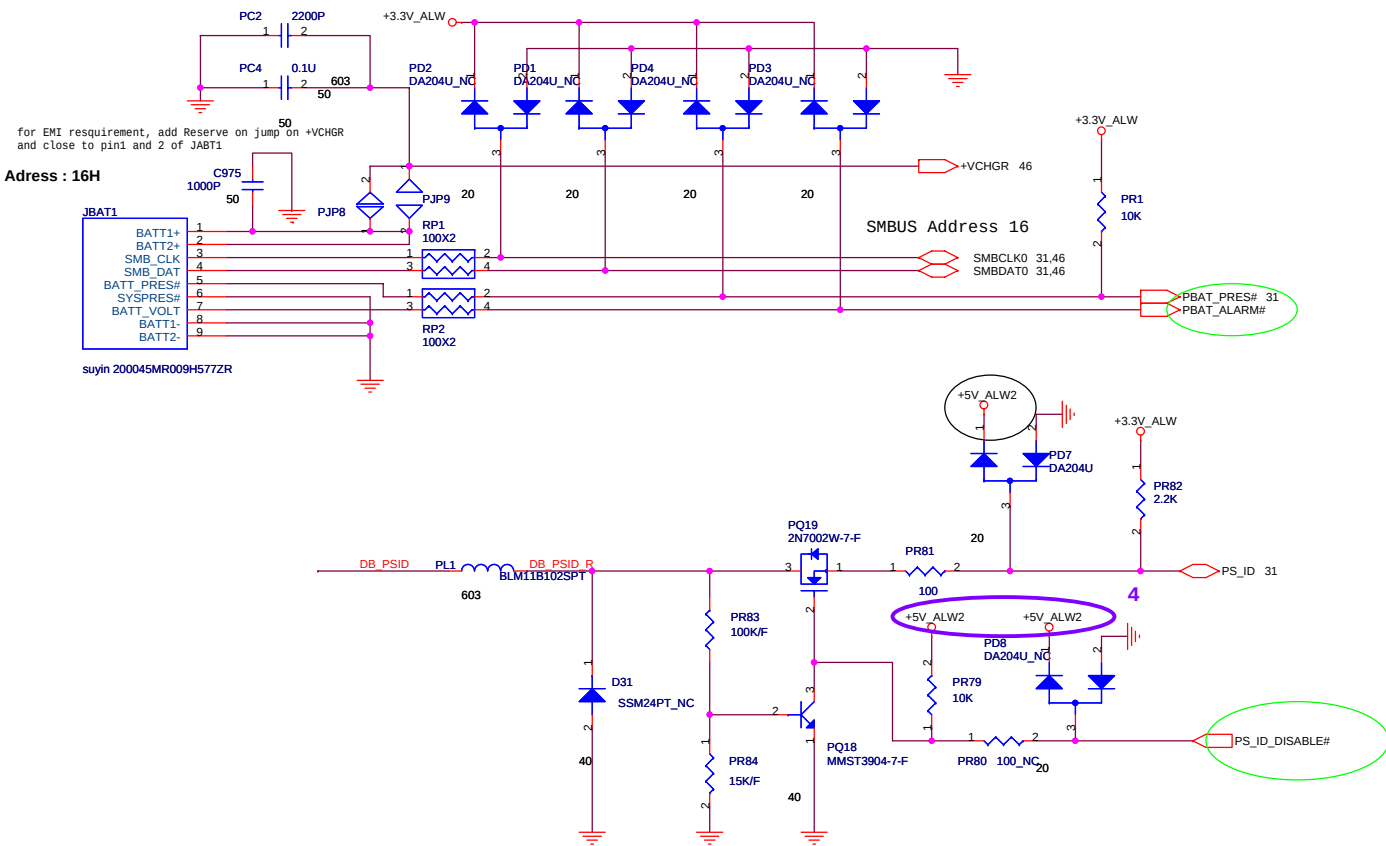


Reserve discharge path



Reserve discharge path





8/15: move the right side USB and DC-in connector schematic to DB.
so change BTB(J14) CONN to 32pin



Title
DCIN,BATT CONNECTOR

Size
Document Number
GM3

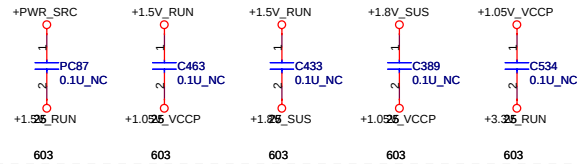
Rev
2B

Date: Friday, January 18, 2008

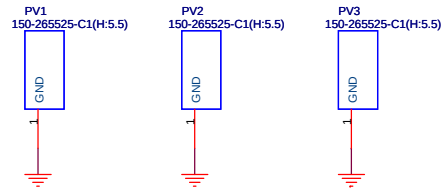
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Reserved for EMI.

Stitching caps



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Page 26
SATA (HDD&CD_ROM)

Page 27
PCCARD /CONN

Page 31
SIO(MEC5025)

Page 38
Azelia CODEC

Page 40
LAN(BCM5755M)

Page 48
1.5VRUN,1.05V(VTT)

Place C860,C216,C1426 close to PQ33.
Place C862,C222,C1427 close to PQ73.

Page 49
1.25V,1.8V,0.9V

Place C867,C254,C1428 close to PQ91.
Place C863,C253,C1429 close to PQ92.

Page 51
CPU_MAX8786(3phase)

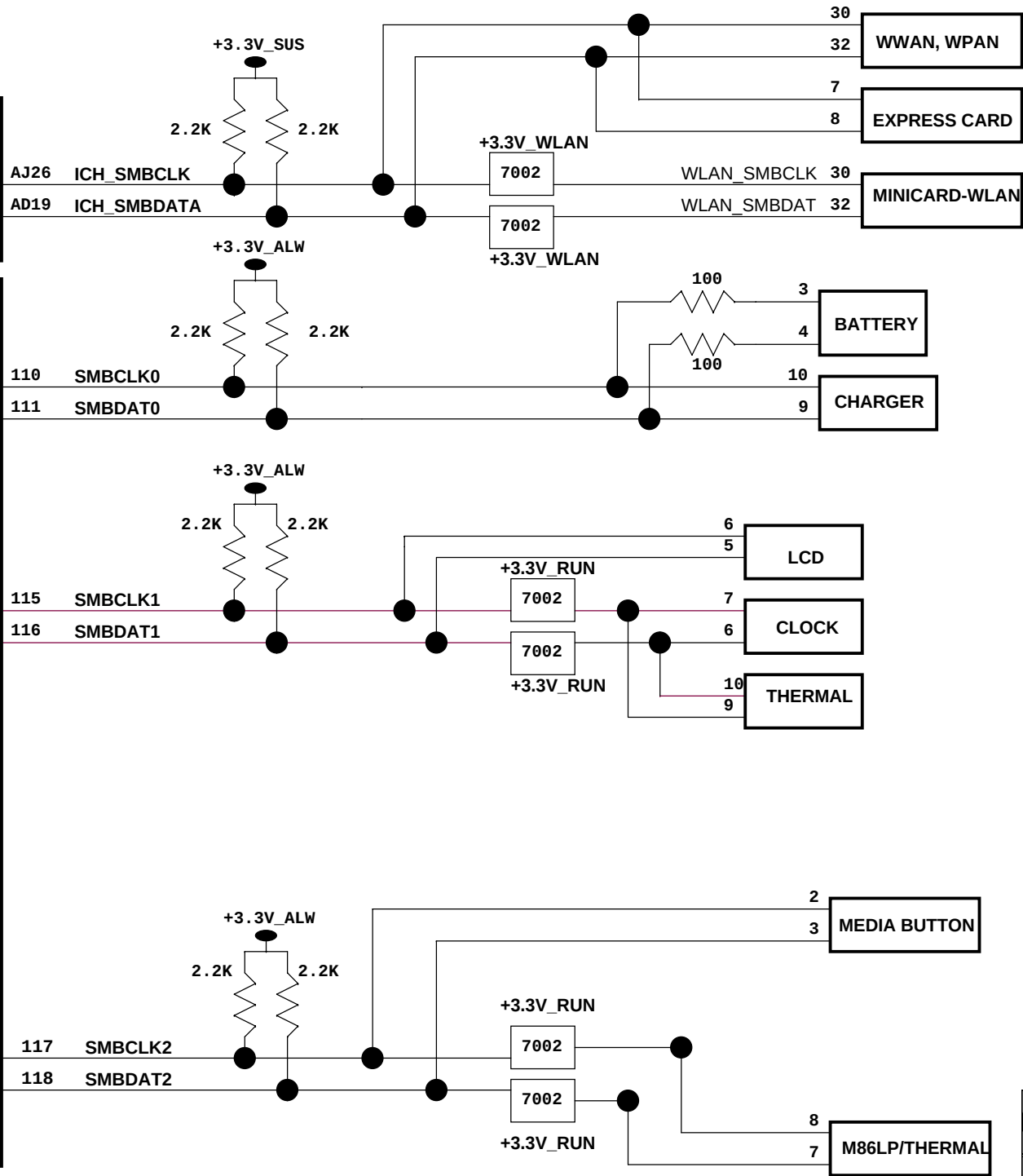
Page 52
D/D Power



Title EMI CAP		
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ICH8-M

SIO
ITE8512



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH					
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH					
S5 (SOFT OFF) / M1	LOW	HIGH	LOW					
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH					
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW					

PM TABLE

power plane State	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON		ON
S3	ON	ON	OFF		ON
S5 S4/AC	ON	OFF	OFF		ON
S5 S4/AC don't exist	OFF	OFF	OFF		ON

PCI TABLE

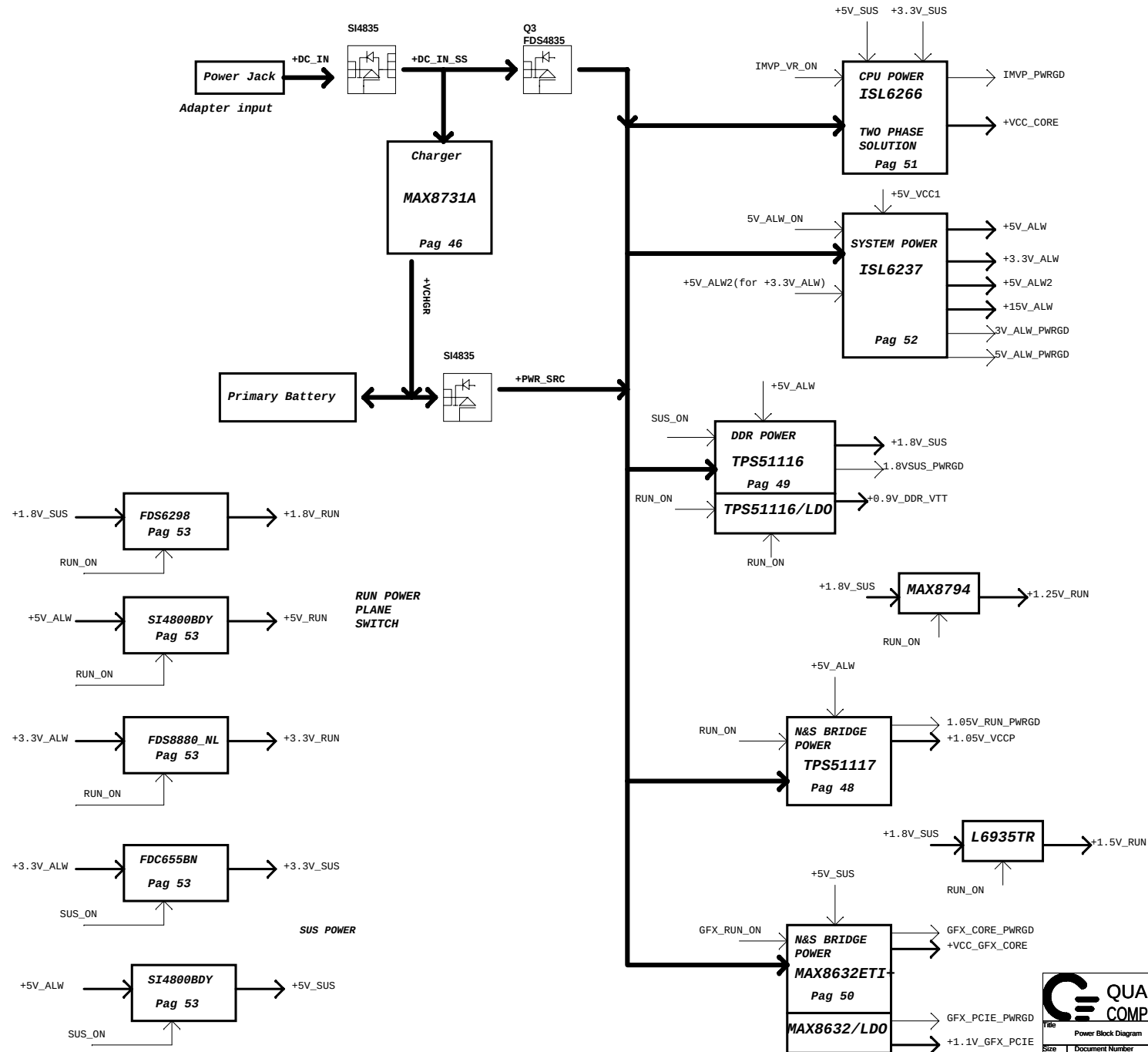
PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
BCM4401B	AD16	REQ#0 / GNT#0	PIRQB
R5C833	AD17	REQ#1 / GNT#1	PIRQC: Card reader PIEQD: 1394

ICH8-M	USB PORT#	DESTINATION
	0	Right Top
	1	Right Bottom
	2	Side TOP
	3	Side Bottom
	4	Ext. USB TOP
	5	Digital Camera
	6	Express Card
	7	WPAN/Bluetooth
	8	Ext. USB Bottom
ECE 5011	9	WWAN
	1	None
	2	None
	3	None
	4	None

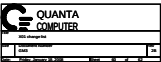
PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	None

GM3 Power Design Block Diagram

2007/09/06



Model	Item	Page	Date	Rev.	Description
Paco of Intel	1	12, 13, 17, 20, 69	9/27	2A	modify SST design issue: 1. delete unnecessary 8 ohm resistor 2. select correct frequency for DIS/UMA(R051AR342) 3. CARD_CLK_REQ# pull high 4. F10E5_DELAY pull down to avoid floating. 5. MC_R451 to set Boot BIOS Strap for LPC Interface
	2	52, 56	10/2	2A	For second source concern, change below item. 1. Change P09 from R48316 to 152305 2. Change P05 from C06534-00T to S04J46-7-F 3. Change PQ1 from B55138-7-F to B55138_NL
	3	8	10/3	2A	use 0005 0 ohm to instead of jump(1/0W, 1.6A per resistor)
	4	10	10/3	2A	pull high the GPIO 0 & GPIO 1 to enable PCIe Full TX OUTPUT 0x40 and PCIe TRANSMITTER DE-EMPHASIS function to solve no display problem.
	5	41	10/15	2A	The camera pin assignment changed : 2 pin camera power pin and they are 3.3 V ..
	6	40	10/15	2A	change resistor setting for STA629073C chip
	7	46, 52	10/15	2A	Due to SI4818BDV-TL-E3 will be EOL., change PQ29 and PQ22 from SI4810 to SI4812.
	8	10	10/16	2A	Due to V00R4 and V00R5(option reference source voltage) use 1.8V_RUN, FAE suggest DVPDATA use 1.8V pull high
	9	33	10/17	2A	remove external SIM card CONN that on MB side
	10	13	10/17	2A	It is multi function pin(SMBALERT#/OPT011). Before bios programming, the PTN function is SMBALERT.If it is pull high to 3.3V_RUN, the ICH6 will be alert by this pin. It caused the S3 can't normally sleep when system cold boot first time. so change to SUS power
	11	38	10/18	2A	Sniffer behavior is reverse, so modify design at PT stage
	12	42	10/18	2A	change to S784 design
	13	40	10/22	2A	change TP46040A4 symbol design to meet SPEC definition
	14	19	10/23	2A	FAE suggest: Ground R28/S28/R28 and implement R2SET to GND even if DAC2 is unused.
	15	43	10/23	2A	For factory requirement---increase pad length for SMT yield rate
	16	41	10/24	2A	for DELL SPEC---change camera conn pin definition
	17	31, 37	10/25	2A	modify LED Key board Illumination schematic and remove EC pin 68
reserve	18	44	10/29	2A	HMPG monitor change: change 3V/5V_ALN_PWRGD to GFX_PCIE/CORE_PWRGD
reserve	19	12, 13, 14, 31	10/29	2A	create +3.3V_SS and +5V_SS power at ICH part to fix ITE chip SUS resume problem, and move L10_S0W to pin1 68 and pin 120 for SUS_ON using
	20	35	10/30	2A	add F500R314X0 to control USB signal can be passed above SUS, and USB_S10E_EN# can control whether USB can supply power for external device at S0 mode
reserve	21	53	10/30	2A	For EE request , add two power rail "+3.3V_SS" and "+5V_SS" for south-bridge battery mode.
	22	48	10/30	2A	1.5V_RUN_PWRGD pull-high to RUN_ON for solve glitch issue.
	23	36, 54	10/30	2A	add 1000pF cap and close to connector for EN1
	24	35	10/30	2A	change LCD connector pin definition for LED panel: 1. change pin 8 from GND to +5V_ALN 2. change pin 56 from GND to LCD_VCC
	25	31	11/1	2A	change GPIO design 1. delete pin 63 SNIFFER_YELLOW# 2. move S1_ALN_EN# SNIFFER to pin 83 3. swap pin 188 WIRELESS_ON/OFF# and pin 35 SNIFFER_PWR_SW
	26	38	11/1	2A	change GPIO design 1. swap WIRELESS_ON/OFF# and SNIFFER_PWR_SW 2. remove SNIFFER_CIRCUITEN_YELLOW#
	27	31	11/5	2A	change GPIO design for fix thermal no function issue 1. MC ADAPT_OC and ADAPT_TRIP_SEL 2. add PV_ALN_ON function at pin 76
	28	3	11/5	2A	Modify H_THERTRIP# Voltage Level shift circuit.
	29	41	11/6	2A	add one GND pin for Audio precision dB value
reserve	30	37	11/8	2A	add circuit to control CIR power
	31	40	11/12	2A	Add PR181 for reserve +5V_ALN2.
	32	43	11/12	2A	For EN1 requirement, add 7pF cap close to LAN switch
	33	37	11/13	2A	for DELL requirement, add fuse between +5V_RUN and +48_LED
	34	31	11/13	2A	use pin 14(WST#) to monitor THERM_STPW function
	35	25	11/13	2A	for Silicon image FAE suggestion: 1. ESD may come from the impedance mismatch, that'll get distorted waveform . Try to replace the common choke with (1.0 22 ohm) resistor 2. Try to remove the source termination resistor (1.0 300 ohm -> 350 ohm) to get cleaner eye 3. change ANCE23P to 3.3V_RUN
	36	25	11/13	2A	per FAE suggestion:change C523 and C524 to 2.2uF for better Audio precision
	37	50	11/13	2A	Change PR11 to 100Kohm for set correct O.C.P.
	38	50	11/13	2A	For EE request, set VGA voltage to 0.90V/1.1V. Change PR116 to 60.8K and PR118 to 118K.
	39	4	11/13	2A	Base on acoustic team test ,add two EC-cap for noise issue. Stuff C733 and C766.
	40	52	11/13	2A	Base on test result, change PR114 to 204K for set OCP.
	41	48	11/13	2A	Change PR161 to 11K for set correct OCP.
	42	48	11/13	2A	For 1.05V jitter issue, change below item. DMA: Change output CAP from 3300/2.5V/ESR10 to 3300/4V/ESR25 Discrete: 1. Change output CAP from 3300/2.0V/ESR10 to 3300/4V/ESR25 2. Add PC62 1500pF
	43	48	11/13	2A	Change 1.05V UMA PQ33 from F056676A5 to F0M566725 for improve efficiency.
	44	40	11/13	2A	Base on EA report test , stuff PR171 and PC108 for reduce high side V05 ring.
	45	48	11/13	2A	Due to software support UL function via "IIMP", no stuff UL circuit.
	46	13	11/14	2A	add 4.7k on PCIE_MCARD1_DET# trace to solve WLAN card detect issue
	47	10	11/15	2A	change GPIO pin from 3.3V_RUN to 3.3V_delay to solve leakage problem between 3.3V_Run and 3.3V_delay(4ms) when boot.



Model	Item	Page	Date	Rev.	Description
Pacino of Intel	1	32	11/26	2B	Change RTC connector because ME modifyr.
	2	31	11/26	2B	Exchange 'SNIFFER_PWR_SW#' AND 'WIRELESS_ON/OFF#. per EC limitation.
	3	31	11/26	2B	Change NUM_LED# from SIO pin98 to pin 88 and used Pin 98 for BID only per EC limitation.
	4	54	11/26	2B	Change PSID relation parts to +5V_ALW2 for power saving in S5.
	5	38	11/26	2B	Change Sniffer Switch power rail from RUN plane to ALW plane.
	6	43	11/26	2B	Added LINK1000# for BCM cann't support GLAN LED driven by LINKLED#/SPD100LED#.
	7	45	11/27	2B	Modify Screw hole base on ME update.
	8	17	11/29	2B	Link to MCH DPLL clock is wrong. Change to correct link.
	9	31	11/30	2B	Fine tune GPIO define for EC.
	10	37	12/04	2B	Change MMB LED power source from 5V_ALW2 plane to 5V_ALW for power saving and avoid LED flash when AC in.
	11	22	12/04	2B	Check AMD +3.3V_DELAY power plane connection component for AMD new update REF133-7 file.
	12	40	12/19	2B	Change Audio AMP thermal PAD leave to NC.
	13	31	12/26	2B	Change SMBus pull hihg resistor form 2.2k to 10k for LED panel flash.
	14	37	12/26	2B	since we will use WLAN and BT LED to show function at factory side. Change power supply of Cap and Num LED from 5V_ALW2, 3.3V_ALW to 5V_RUN and 3.3V_RUN.
	15	19	12/26	2B	Change HDMI detect circuit to solve external panel feed back voltage shortage then caude ATI chip can't switch to HMDI mode problem.
	16	37	12/26	2B	Change the Media board power from 3V_ALW to 5V_ALW2 to solve LED flash issue when AC/Bat plug in.
	17	37	12/26	2B	Change the lid switch IC power source from 3.3V_SUS to 3.3V_ALW to avoid system can enter S4 mode but wake up fail problem
	18	48	1/3	2B	Change PC85 to 680P for meet sequence.
	19	50	1/3	2B	Change PR7 to 4.99K for adjust +1.1V_GFX_PCIE rail.
	20	53	1/3	2B	Change PQ11 from S08 to power package footprint.
	21	48 49 50 52	1/3	2B	Change PR161 ,PR172 ,PR11 ,PR114 to correct resistance for reliability request.
	22	35	1/4	2B	remove USB charge circuit
	23	26	1/7	2B	pull DPST signal to high for setting 100% duty cycle
	24	31	1/7	2B	pin12 should reserve 1u cap for ITE8512JX using
	25	19	1/7	2B	modify HDMI detect circuit to fix the monitor detection problem..
	26	55	1/7	2B	create EMI spring
	27	31	1/11	2B	per TXC report, we should change W1 cap to 18p
	28	41	1/11	2B	per IDT FAE suggestion, serial 22 ohm on DMIC_CLK can help DMIC performance
	29	37	1/11	2B	add 10u cap at JMB1, let 3.3V_ALE get lower drop voltage on MMB side.
	30	6, 19	1/11	2B	EMI demand add 33p cap on RGB signal.



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Model	Item	Page	Date	Rev.	Description
Pacino of Intel	1	45	10/08	B	Change screw holes define to meet ME request.



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Title

A00 change list

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