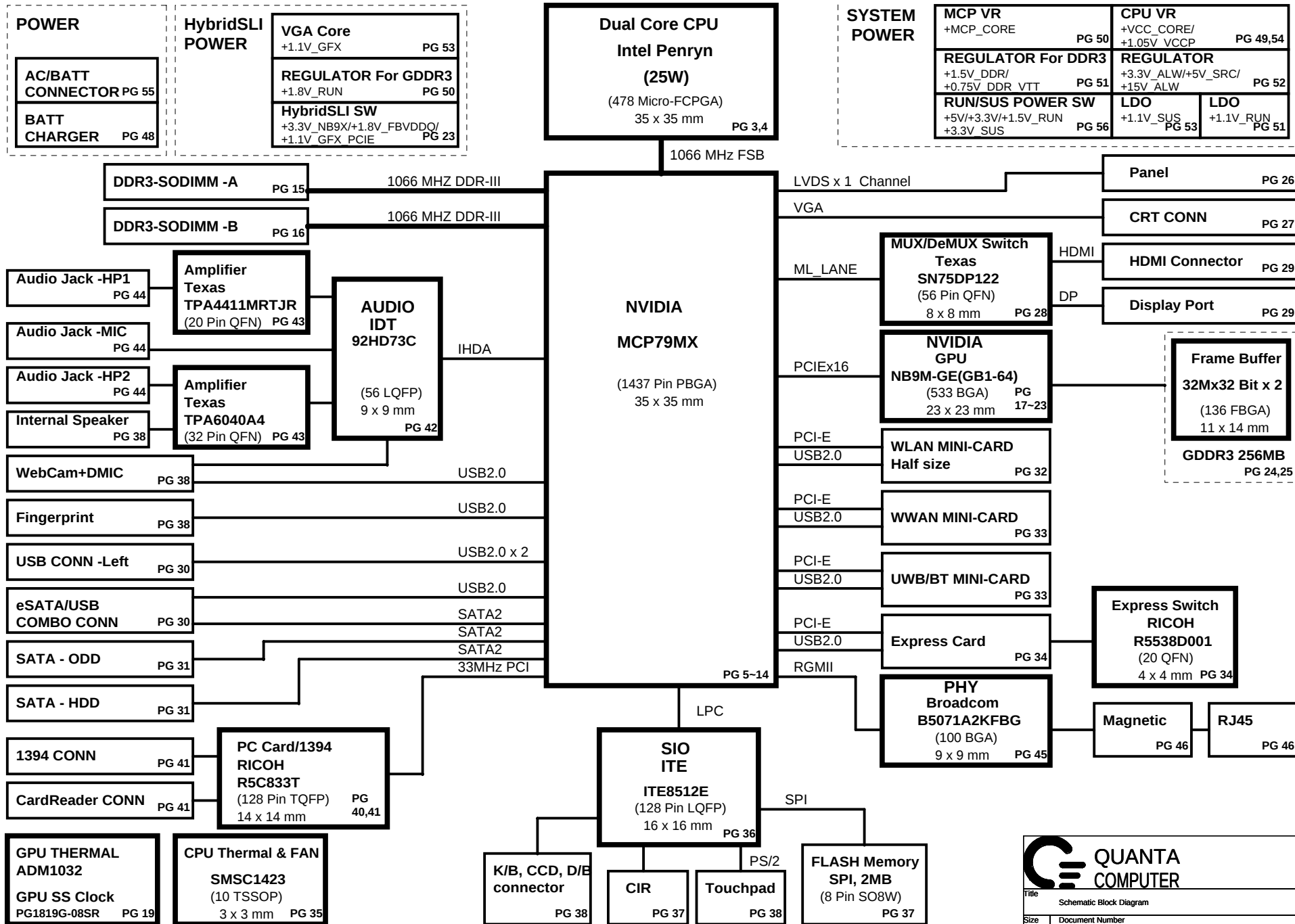


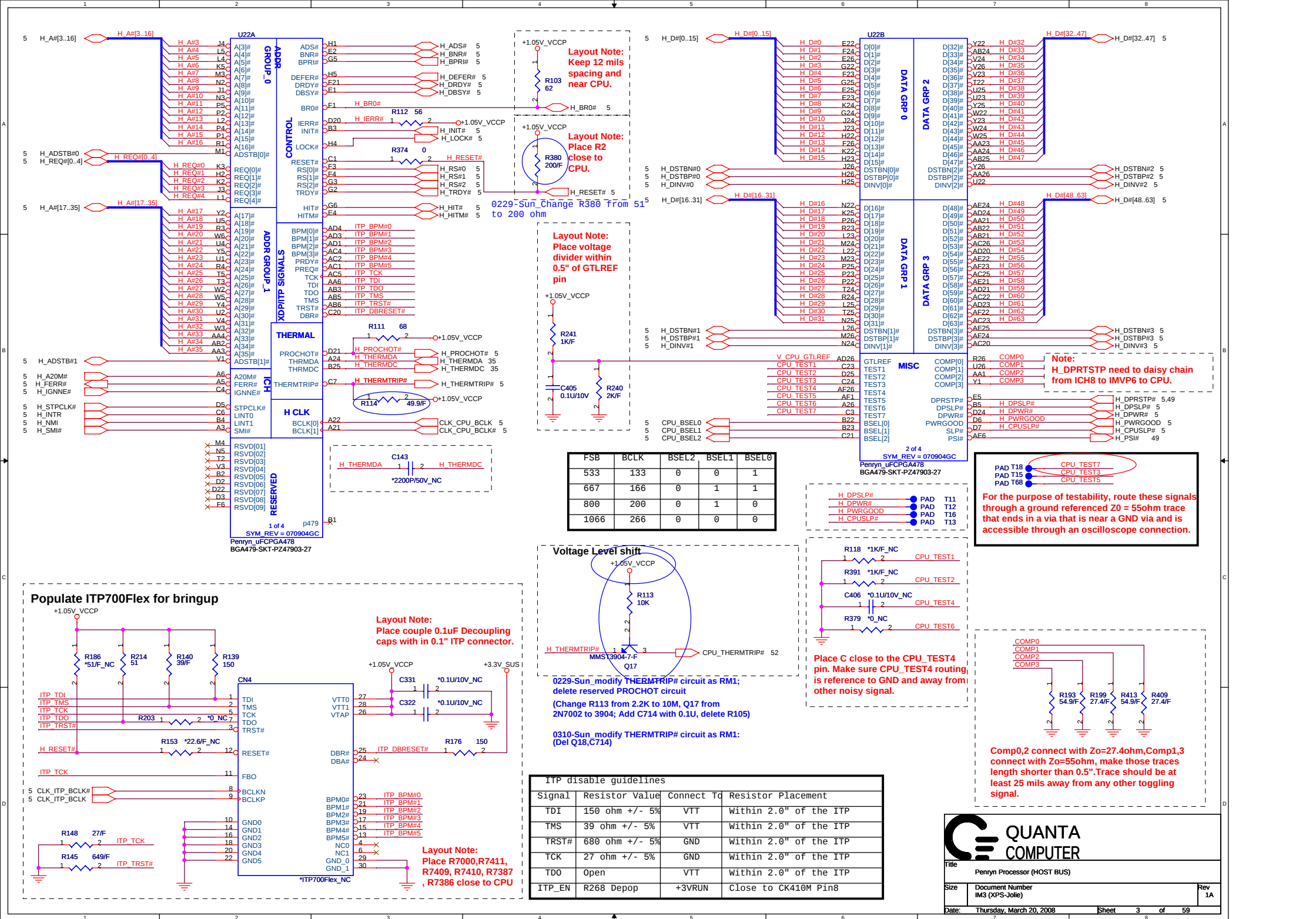
IM3 (Jolie) Discrete 256M

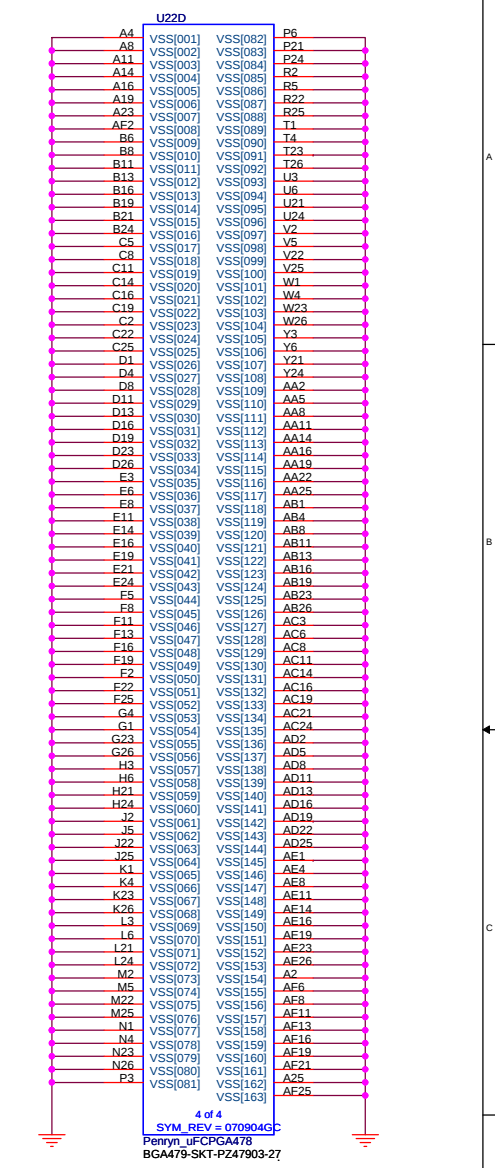
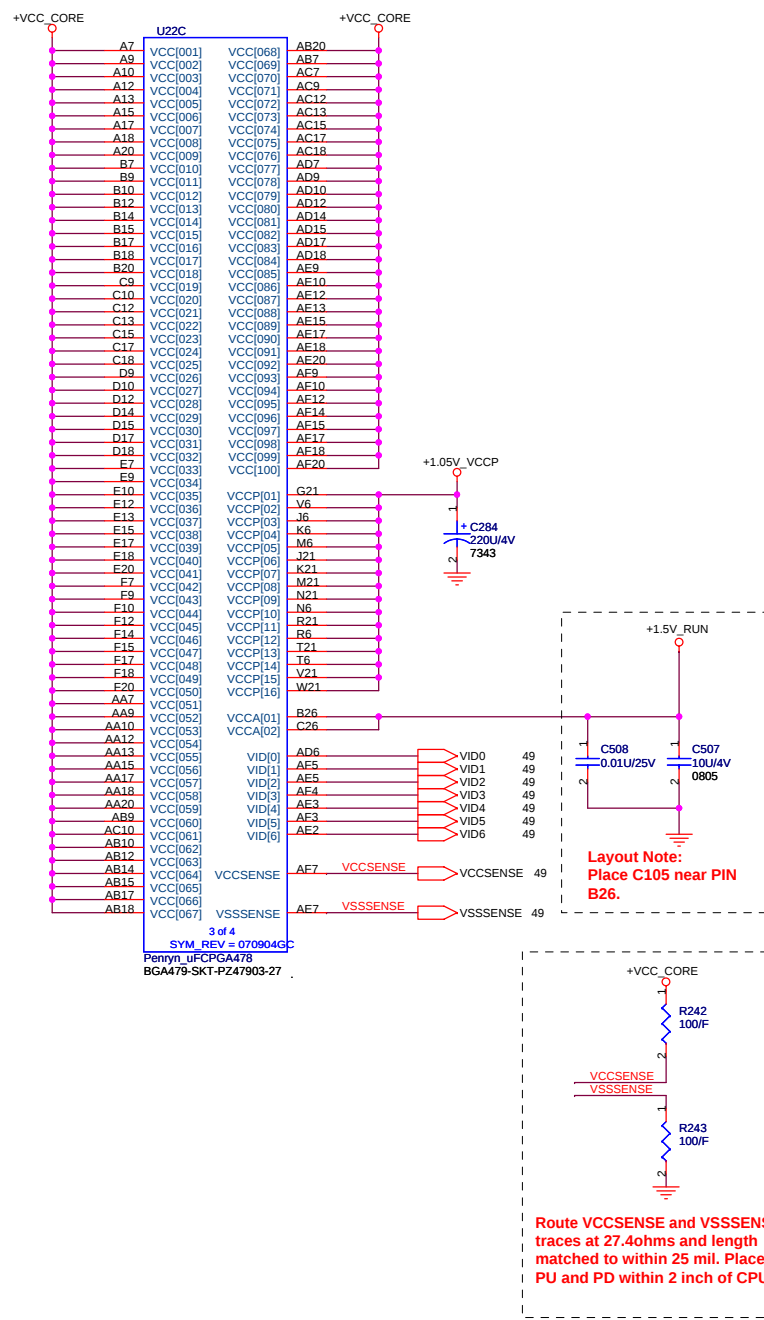
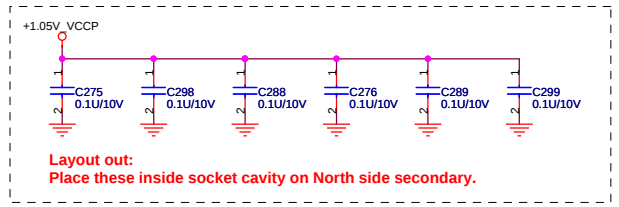
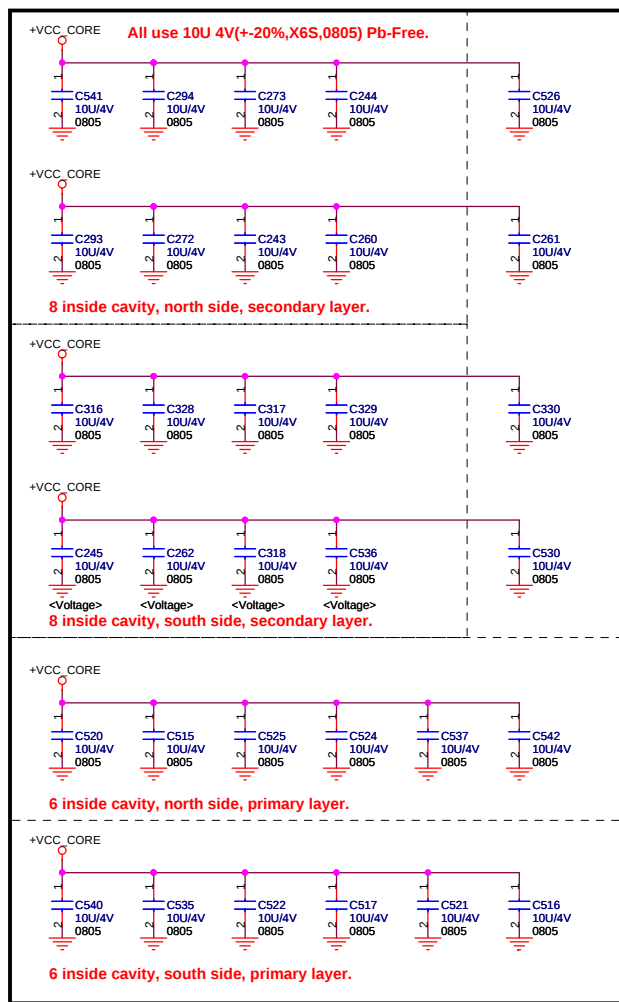
VER : 1B

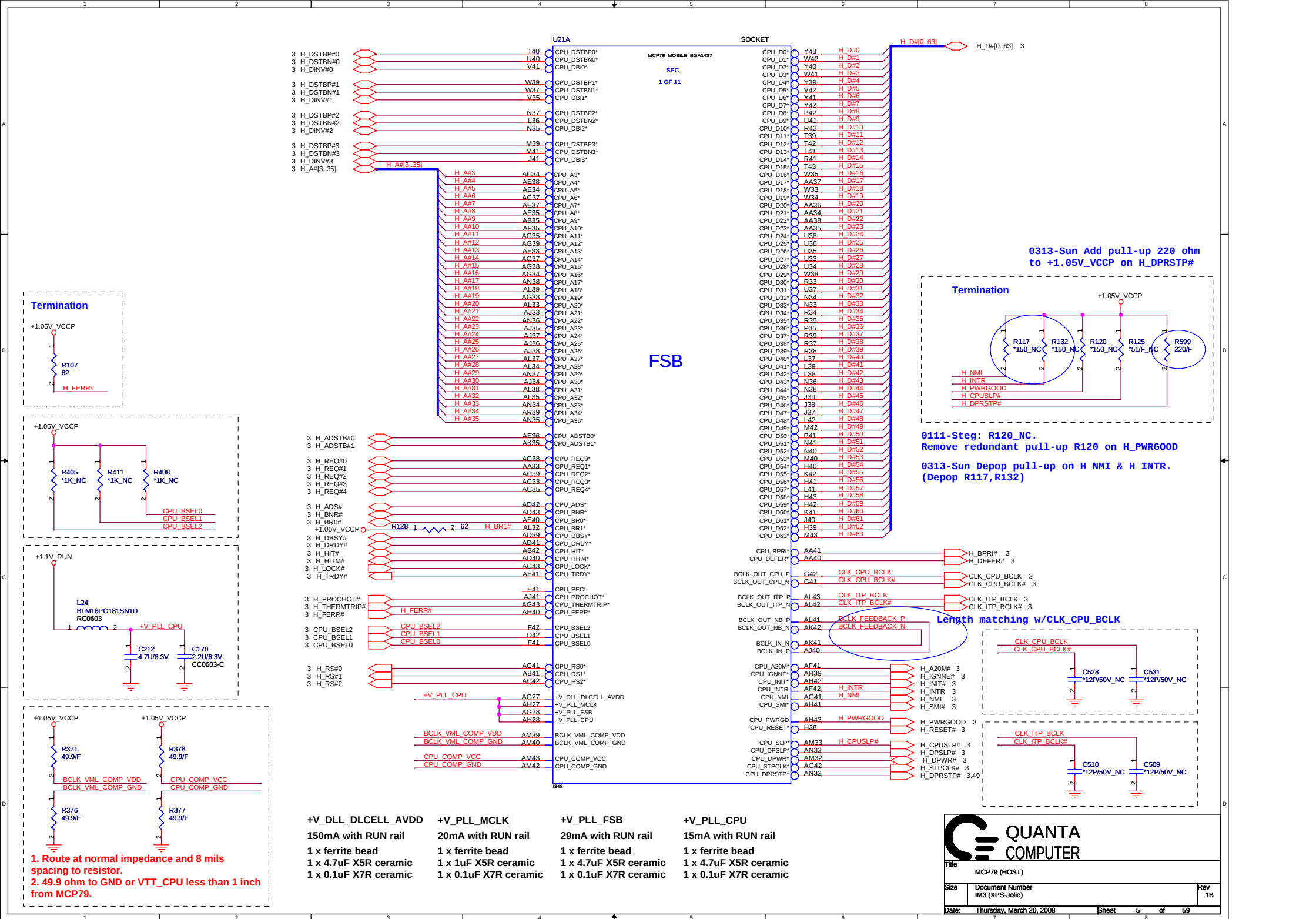


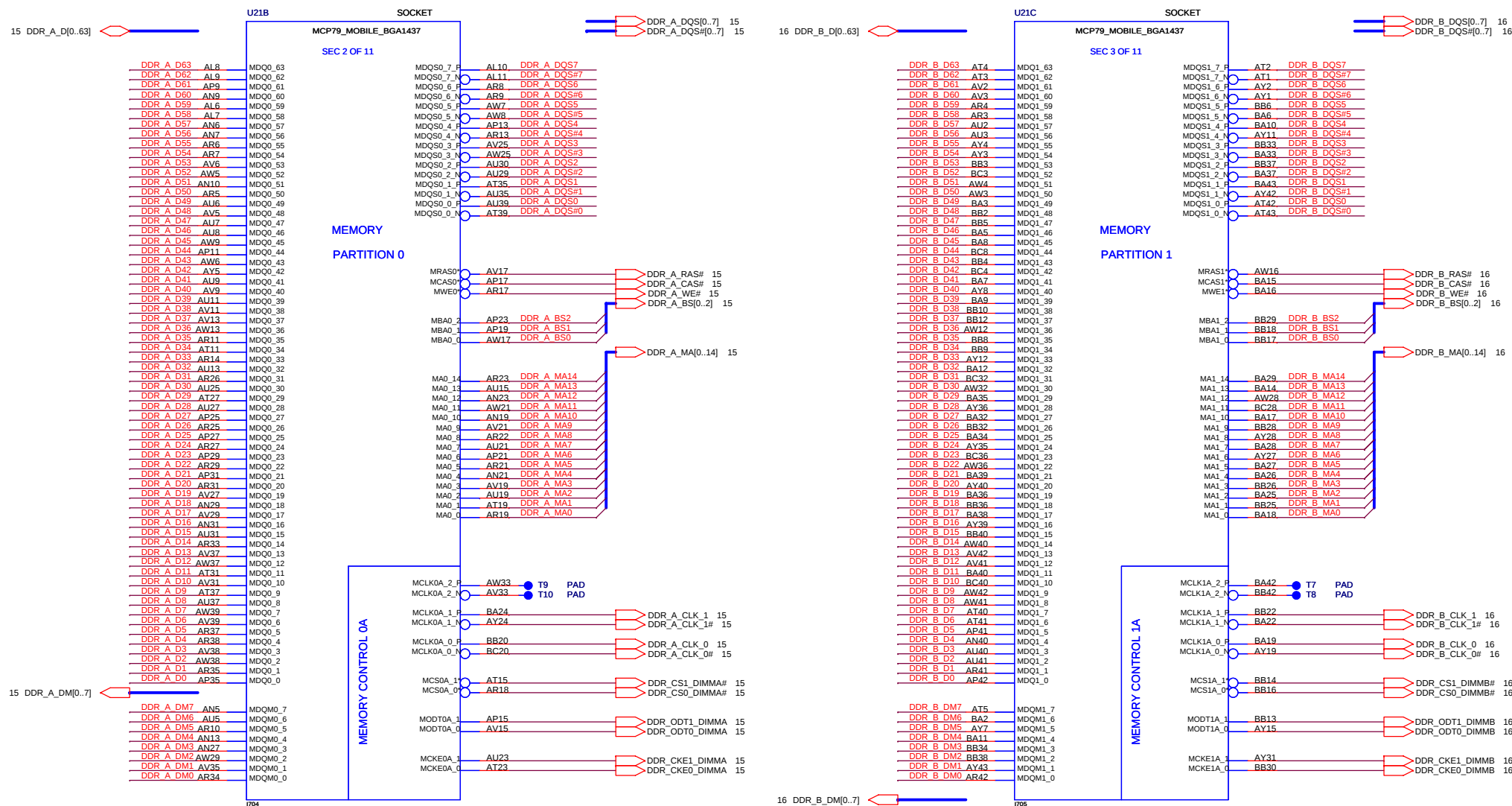
INDEX	
Page#	Description
1	Block Diagram
2	Front Page
3-4	Penryn (CPU)
5-14	MCP79 (NB+SB+CKG)
15-16	DDRIII SO-DIMM(204P)
17-25	VGA (NB9M)
26	LCD CONN
27	CRT CONN
28	DeMux SW (SN75DP122)
29	HDMI & DP CONN
30	USB & eSATA & TV
31	HDD & ODD (SATA)
32	MINI-CARD (WLAN)
33	MINI-CARD (WPAN,WWAN)
34	Express Card
35	FAN & Thermal
36	SIO (ITE8512)
37	Flash ROM/ RTC/ CIR
38	KB/ CCD/ User Interface
39	LED
40-41	Card Reader & 1394
42-43	Audio CODEC(92HD73C)/ AMP/ Jack/ Subwoofer
45-46	LAN PHY (B5071)/ RJ45/ Transformer
47	System Reset Circuit
48	CHARGER (MAX8731)
49	CPU Core (ISL6266)
50	MCP79 CORE/ 1.05V (MAX17007)
51	DDR 1.5V/ 1.1V (TPS51116)
52	SYS 5V/ 3V(MAX17020)
53	NB9 Core (MAX8632)
54	GRAM_1.8V (TPS51117)
55	DCIN,Batt
56	RUN POWER SW
57	Debug Port (Mini PCI)
58	PAD & SCREW

Power States						
Power Rail	Control Signal	S0	S3	S4	S5	G3
+PWR_SRC	N/A	V	V	V	V	
+0.75V_DDR_VTT	RUN_ON	V				
+1.05V_VCCP	CPUVDD_EN	V				
+1.1V_GFX	+3.3V_NB9X	V				
+1.1V_GFX_PCIE	MXM_PWR_EN	V				
+1.1V_RMGT	SLP_RMGT#	V	V			
+1.1V_RUN	RUN_ON	V				
+1.1V_SUS	+3.3V_SUS	V	V			
+1.5V_RUN	RUN_ON	V				
+1.5V_DDR	SIO_SLP_S5#	V	V			
+1.8V_FBVDDQ	NB9_CORE_PWRGD	V				
+1.8V_RUN	RUN_ON	V				
+15V_ALW	+5V_ALW	V	V			
+3.3V_ALW	+5V_ALW2	V	V	V	V	
+3.3V_NB9X	MXM_PWR_EN	V				
+3.3V_RMGT	SLP_RMGT#	V	V			
+3.3V_RUN	RUN_ON	V				
+3.3V_SUS	SUS_ON	V	V			
+5V_ALW	5V_ALW_ON	V	V			
+5V_ALW2	+PWR_SRC	V	V	V	V	
+5V_HDD	HDDC_EN	V				
+5V_MOD	MODC_EN	V				
+5V_RUN	RUN_ON	V				
+GFX_PWR_SRC	RUN_ON	V				
+LCDVCC	EN_LCDVCC	V				
+MCP_CORE	RUN_ON	V				
+NB9_CORE	+3.3V_NB9X	V				
+RTC_CELL	N/A	V	V	V	V	V
+VCC_CORE	1.05V_VCCP_PWRGD	V				
+USB_RIGHT_PWR	USB_SIDE_EN#	V	V			
+USB_LEFT_PWR	USB_BACK_EN#	V	V			









Layout Notice:

Memory Data Signal Group

MCP79 BGA Breakout (<175ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.

After Breakout: Route at 40 ohm impedance and 4x(Microstrip) or 3x(Stripline) dielectric spacing.

DIMM Fan-in (<90ps):

Route at 40 ohm impedance and 1.5x dielectric height spacing.

Memory Data Strobes

Route strobes differentially at 66 ohm impedance (42 ohm SE) and 5x dielectric height spacing to other signals.

Memory Clock Signal Group

MCP79 BGA Breakout (<90ps): Route at 50 ohm SE / 100 ohm differential impedance.

After Breakout: Route at 40 ohm SE / 66 ohm differential impedance and 5x dielectric height spacing to other signals.

Memory Address/Command/Control Signal Group

MCP79 BGA Breakout (<90ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.

After Breakout: Route at 40 ohm impedance and 2x dielectric height to other signals and 3x dielectric spacing to other non-associated signals.

DIMM Fan-in (<90ps):

Route at 40 ohm impedance and 1.5x dielectric height spacing.



Title MCP79 (DDR3)		
Size	Document Number IM3 (XPS-Jolie)	Rev 1A
Date:	Thursday, March 20, 2008	Sheet 6 of 59

17 PCIE_MRX_GTX_P[0..15]
17 PCIE_MRX_GTX_N[0..15]

PCIe Layout Notice:
MCP79 BGA Breakout (<27ps):
Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout:
Route at 50 Signal end and 90 ohm differential.
Inter-pair spacing 4x (Microstrip) dielectric height spacing 3x (Stripline) dielectric height spacing.

PCIE MRX GTX P0 E7 PE0_RX0_P
PCIE MRX GTX N0 E7 PE0_RX0_N
PCIE MRX GTX P1 D7 PE0_RX1_P
PCIE MRX GTX N1 C7 PE0_RX1_N
PCIE MRX GTX P2 E6 PE0_RX2_P
PCIE MRX GTX N2 E6 PE0_RX2_N
PCIE MRX GTX P3 E5 PE0_RX3_P
PCIE MRX GTX N3 E5 PE0_RX3_N
PCIE MRX GTX P4 E4 PE0_RX4_P
PCIE MRX GTX N4 E3 PE0_RX4_N
PCIE MRX GTX P5 C3 PE0_RX5_P
PCIE MRX GTX N5 D3 PE0_RX5_N
PCIE MRX GTX P6 C5 PE0_RX6_P
PCIE MRX GTX N6 H5 PE0_RX6_N
PCIE MRX GTX P7 J7 PE0_RX7_P
PCIE MRX GTX N7 J6 PE0_RX7_N
PCIE MRX GTX P8 J5 PE0_RX8_P
PCIE MRX GTX N8 J4 PE0_RX8_N
PCIE MRX GTX P9 L11 PE0_RX9_P
PCIE MRX GTX N9 L10 PE0_RX9_N
PCIE MRX GTX P10 L9 PE0_RX10_P
PCIE MRX GTX N10 L8 PE0_RX10_N
PCIE MRX GTX P11 L7 PE0_RX11_P
PCIE MRX GTX N11 L6 PE0_RX11_N
PCIE MRX GTX P12 N11 PE0_RX12_P
PCIE MRX GTX N12 N10 PE0_RX12_N
PCIE MRX GTX P13 N9 PE0_RX13_P
PCIE MRX GTX N13 N9 PE0_RX13_N
PCIE MRX GTX P14 P9 PE0_RX14_P
PCIE MRX GTX N14 N7 PE0_RX14_N
PCIE MRX GTX P15 N5 PE0_RX15_P
PCIE MRX GTX N15 N4 PE0_RX15_N

PCIE

SOCKET

PCIE MTX GRX C P0 C347 1 2 0.1U/10V PCIE MTX GRX P0
PCIE MTX GRX C N0 C340 1 2 0.1U/10V PCIE MTX GRX N0
PCIE MTX GRX C P1 C373 1 2 0.1U/10V PCIE MTX GRX P1
PCIE MTX GRX C N1 C384 1 2 0.1U/10V PCIE MTX GRX N1
PCIE MTX GRX C P2 C556 1 2 0.1U/10V PCIE MTX GRX P2
PCIE MTX GRX C N2 C565 1 2 0.1U/10V PCIE MTX GRX N2
PCIE MTX GRX C P3 C552 1 2 0.1U/10V PCIE MTX GRX P3
PCIE MTX GRX C N3 C548 1 2 0.1U/10V PCIE MTX GRX N3
PCIE MTX GRX C P4 C358 1 2 0.1U/10V PCIE MTX GRX P4
PCIE MTX GRX C N4 C367 1 2 0.1U/10V PCIE MTX GRX N4
PCIE MTX GRX C P5 C333 1 2 0.1U/10V PCIE MTX GRX P5
PCIE MTX GRX C N5 C323 1 2 0.1U/10V PCIE MTX GRX N5
PCIE MTX GRX C P6 C547 1 2 0.1U/10V PCIE MTX GRX P6
PCIE MTX GRX C N6 C544 1 2 0.1U/10V PCIE MTX GRX N6
PCIE MTX GRX C P7 C543 1 2 0.1U/10V PCIE MTX GRX P7
PCIE MTX GRX C N7 C539 1 2 0.1U/10V PCIE MTX GRX N7
PCIE MTX GRX C P8 C311 1 2 0.1U/10V PCIE MTX GRX P8
PCIE MTX GRX C N8 C319 1 2 0.1U/10V PCIE MTX GRX N8
PCIE MTX GRX C P9 C534 1 2 0.1U/10V PCIE MTX GRX P9
PCIE MTX GRX C N9 C538 1 2 0.1U/10V PCIE MTX GRX N9
PCIE MTX GRX C P10 C297 1 2 0.1U/10V PCIE MTX GRX P10
PCIE MTX GRX C N10 C307 1 2 0.1U/10V PCIE MTX GRX N10
PCIE MTX GRX C P11 C291 1 2 0.1U/10V PCIE MTX GRX P11
PCIE MTX GRX C N11 C280 1 2 0.1U/10V PCIE MTX GRX N11
PCIE MTX GRX C P12 C532 1 2 0.1U/10V PCIE MTX GRX P12
PCIE MTX GRX C N12 C529 1 2 0.1U/10V PCIE MTX GRX N12
PCIE MTX GRX C P13 C523 1 2 0.1U/10V PCIE MTX GRX P13
PCIE MTX GRX C N13 C527 1 2 0.1U/10V PCIE MTX GRX N13
PCIE MTX GRX C P14 C263 1 2 0.1U/10V PCIE MTX GRX P14
PCIE MTX GRX C N14 C267 1 2 0.1U/10V PCIE MTX GRX N14
PCIE MTX GRX C P15 C519 1 2 0.1U/10V PCIE MTX GRX P15
PCIE MTX GRX C N15 C518 1 2 0.1U/10V PCIE MTX GRX N15

PCIE_MTX_GRX_P[0..15] 17
PCIE_MTX_GRX_N[0..15] 17

10 MXM_ON#

Express Card

WLAN

UWB/BT

WWAN

0229 Pop R177 w/o ohm

12,17 PE_RESET_MXM#

12,36,47 MXM_RUNPWROK

32,33,34 PCIE_WAKE#

Express Card

WLAN

UWB/BT

WWAN

34 PCIE_RX0_P

34 PCIE_RX0_N

32 PCIE_RX1_P

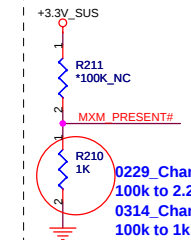
32 PCIE_RX1_N

33 PCIE_RX2_P

33 PCIE_RX2_N

33 PCIE_RX3_P

33 PCIE_RX3_N



0229 Change R210 from 100k to 2.2k ohm
0314 Change R210 from 100k to 1k ohm base on NV suggestion

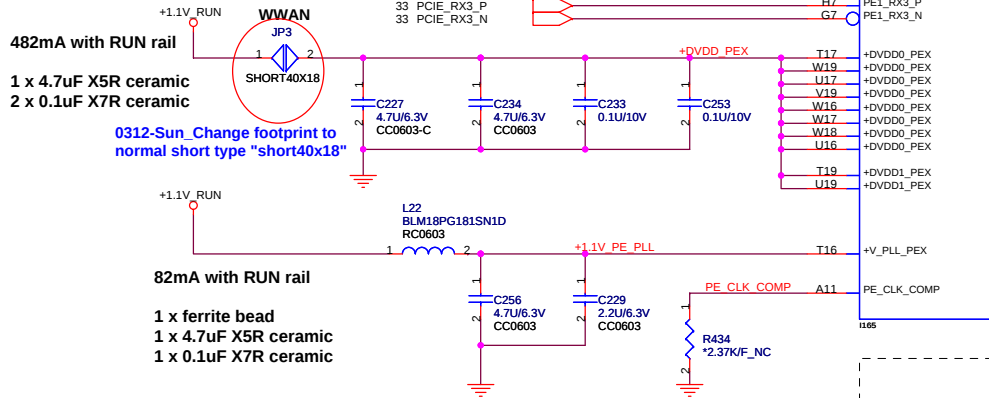
482mA with RUN rail

1 x 4.7uF X5R ceramic
2 x 0.1uF X7R ceramic

0312-Sun_Change footprint to normal short type "short40x18"

82mA with RUN rail

1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic

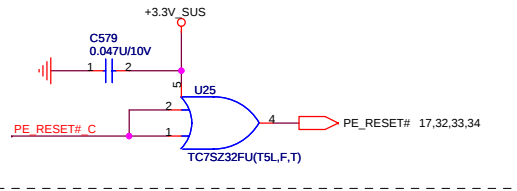
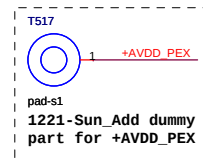
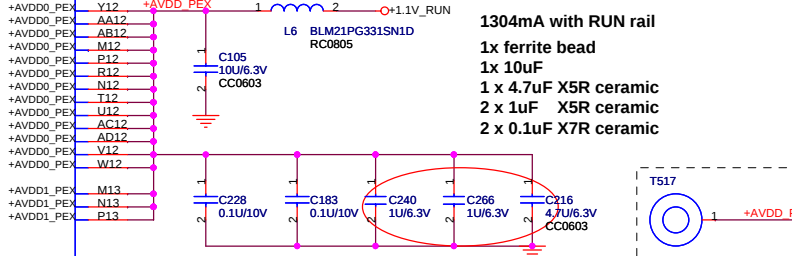


PE0_REFCLK_P E11 CLK_PCIE_VGA 17
PE0_REFCLK_N D11 CLK_PCIE_VGA# 17
PE1_REFCLK_P G11 CLK_PCIE_EXPCARD 34
PE1_REFCLK_N F11 CLK_PCIE_EXPCARD# 34
PE2_REFCLK_P J11 CLK_PCIE_MINI1 32
PE2_REFCLK_N I10 CLK_PCIE_MINI1# 32
PE3_REFCLK_P G13 CLK_PCIE_MINI2 33
PE3_REFCLK_N F13 CLK_PCIE_MINI2# 33
PE4_REFCLK_P J13 CLK_PCIE_MINI3 33
PE4_REFCLK_N H13 CLK_PCIE_MINI3# 33
PE5_REFCLK_P L14 PAD T28
PE5_REFCLK_N K14 PAD T30
PE6_REFCLK_P N14 PAD T22
PE6_REFCLK_N M14 PAD T21
PE_RST0# K11 PE_RESET# C

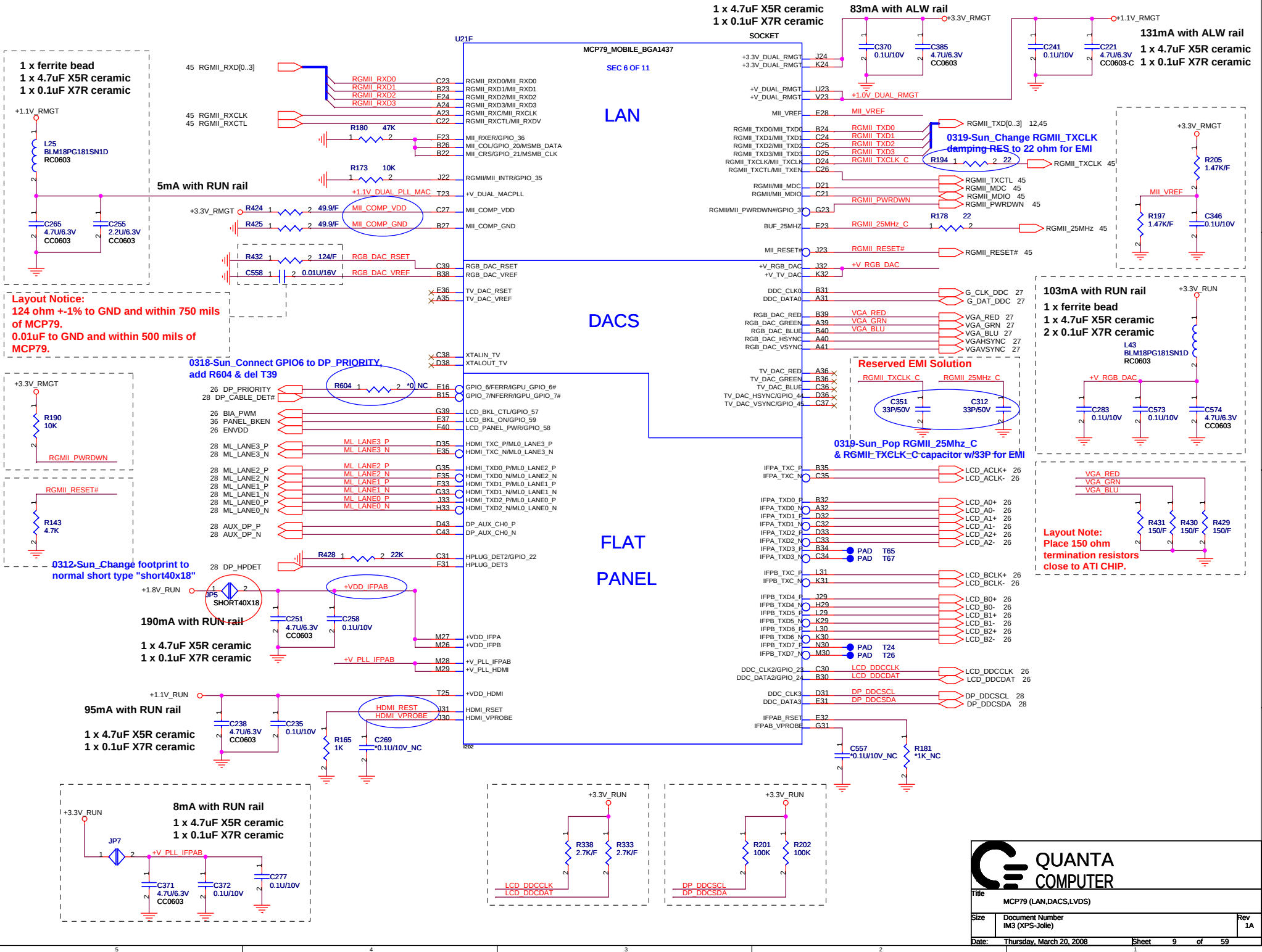
PCIE_TX0_P D8 PCIE_TX0_P_C C564 1 2 0.1U/10V PCIE_TX0_P 34
PCIE_TX0_N C8 PCIE_TX0_N_C C563 1 2 0.1U/10V PCIE_TX0_N 34
PCIE_TX1_P B8 PCIE_TX1_P_C C576 1 2 0.1U/10V PCIE_TX1_P 32
PCIE_TX1_N A8 PCIE_TX1_N_C C575 1 2 0.1U/10V PCIE_TX1_N 32
PCIE_TX2_P A7 PCIE_TX2_P_C C561 1 2 0.1U/10V PCIE_TX2_P 33
PCIE_TX2_N B7 PCIE_TX2_N_C C562 1 2 0.1U/10V PCIE_TX2_N 33
PCIE_TX3_P B6 PCIE_TX3_P_C C559 1 2 0.1U/10V PCIE_TX3_P 33
PCIE_TX3_N C6 PCIE_TX3_N_C C560 1 2 0.1U/10V PCIE_TX3_N 33

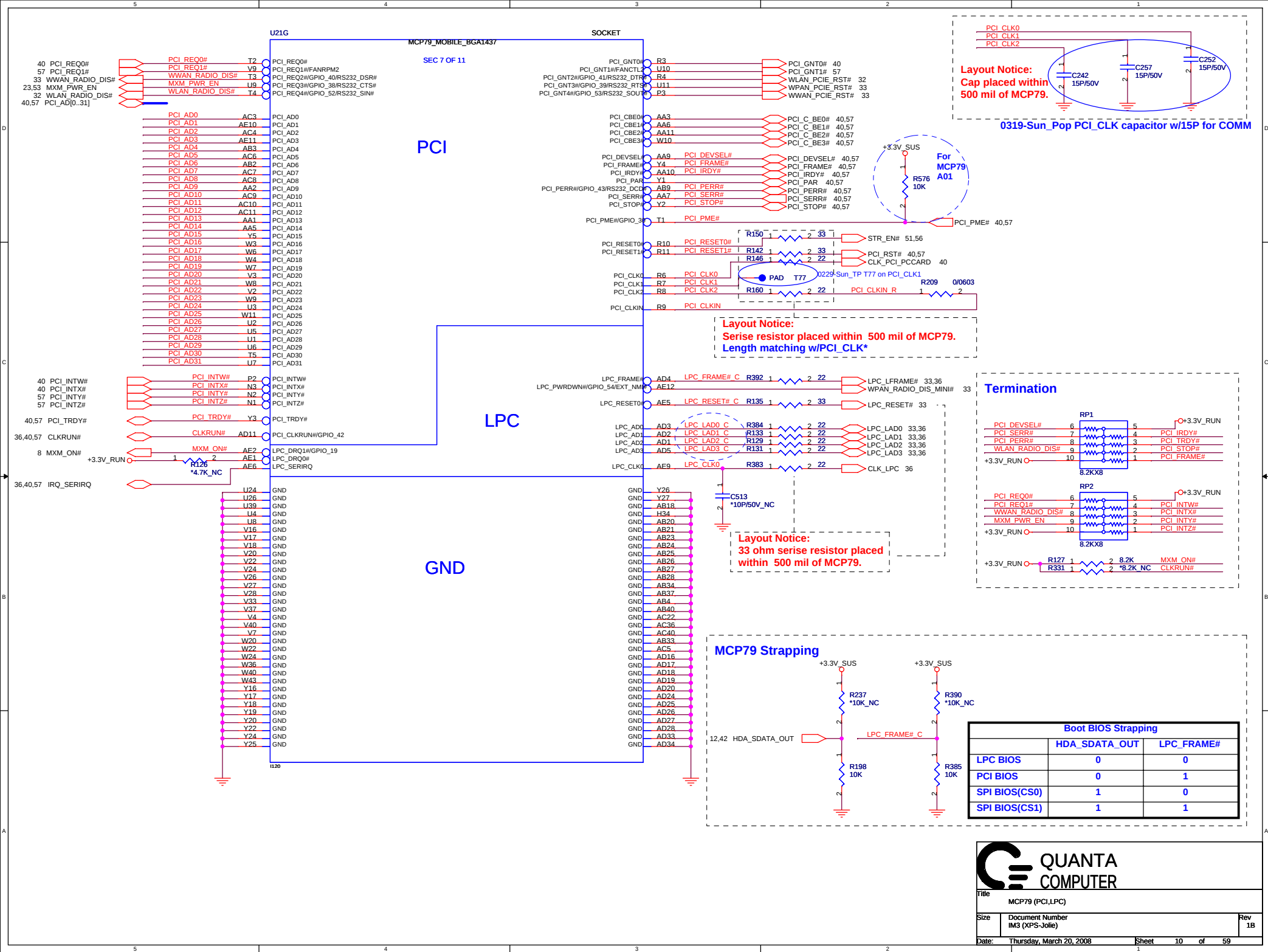
1304mA with RUN rail

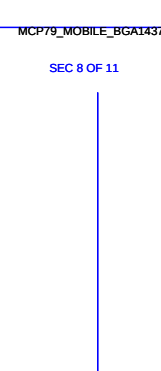
1x ferrite bead
1x 10uF
1 x 4.7uF X5R ceramic
2 x 1uF X5R ceramic
2 x 0.1uF X7R ceramic



Title			MCP79 (PCIE)
Size			Document Number IM3 (XPS-Jolie)
Date:			Friday, March 21, 2008
Sheet			8 of 59
Rev			1A







SATA



USB

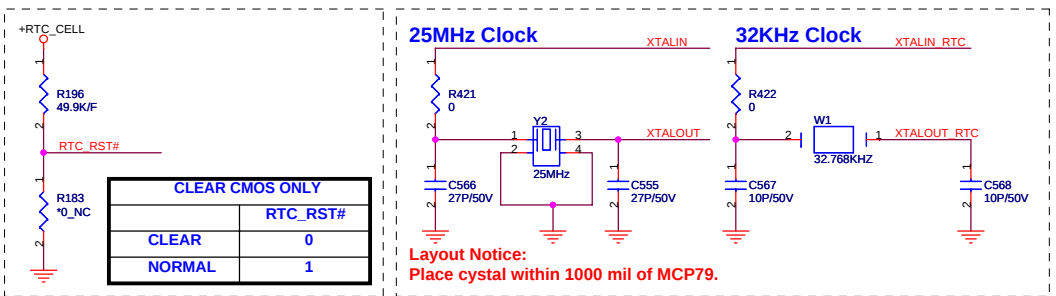
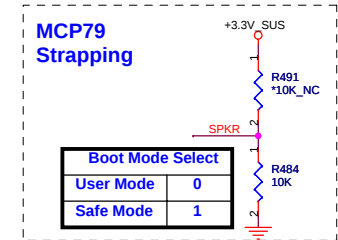
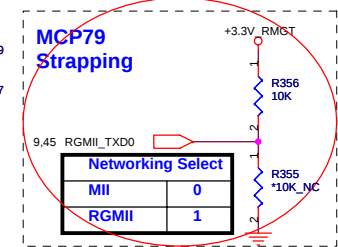
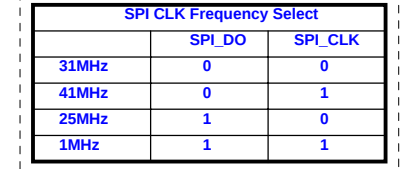
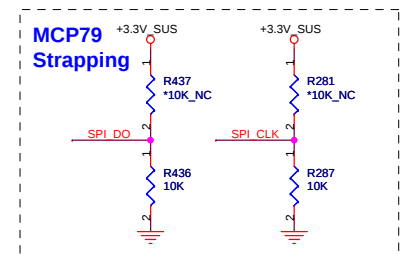
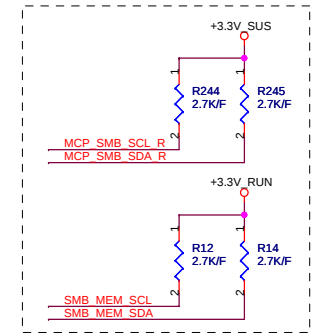
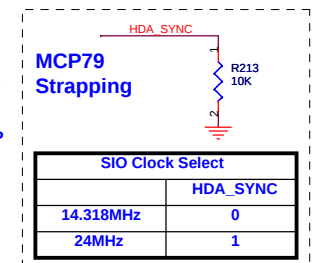
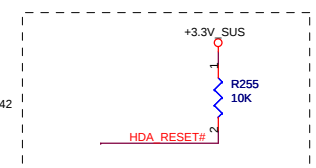
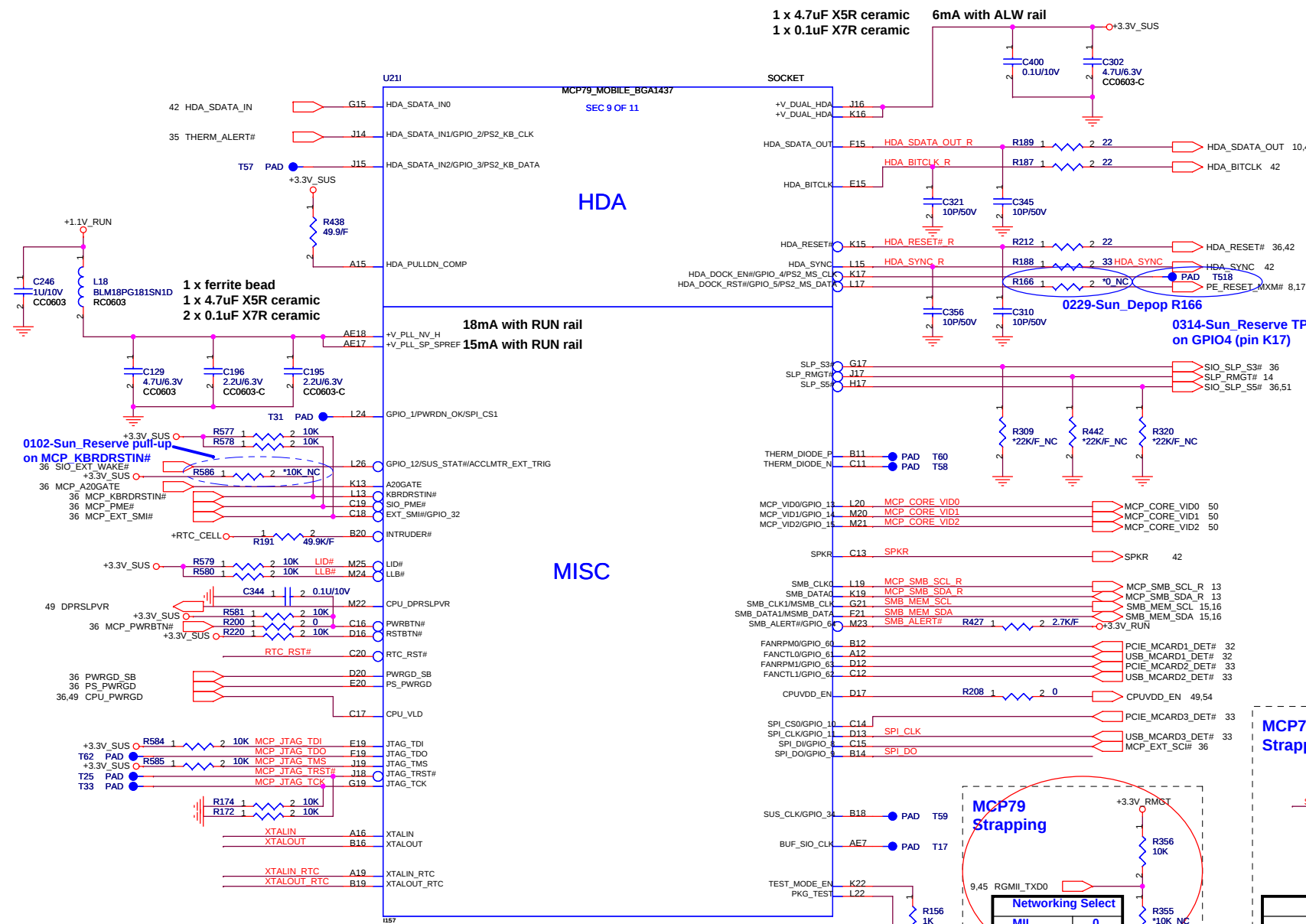
USB



USB



USB



CLEAR CMOS ONLY

CLEAR	RTC_RST#
CLEAR	0
NORMAL	1

Layout Notice:
Place crystal within 1000 mil of MCP79.

QUANTA
COMPUTER

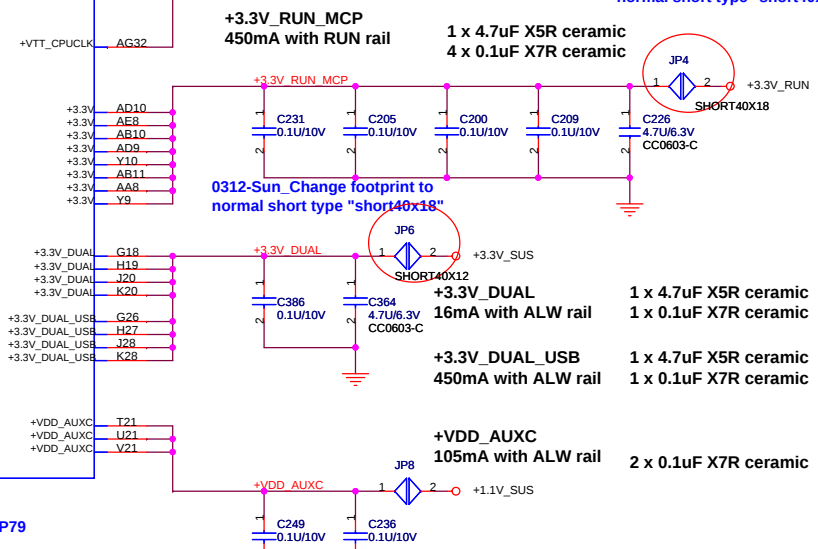
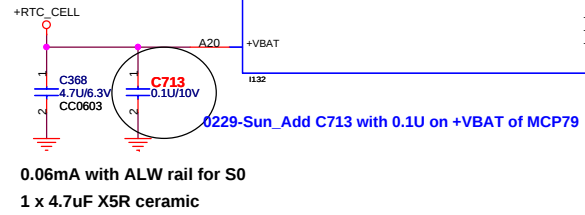
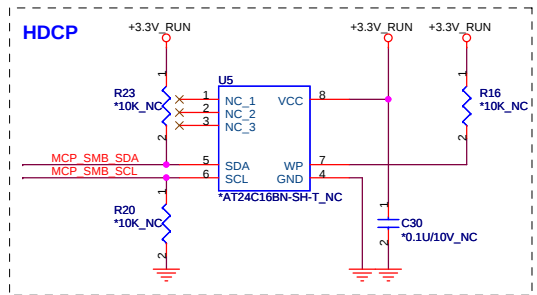
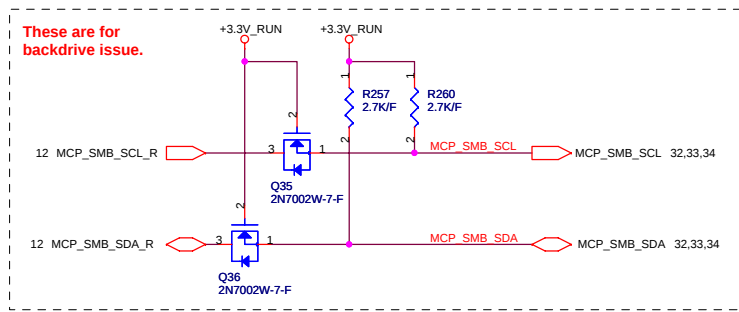
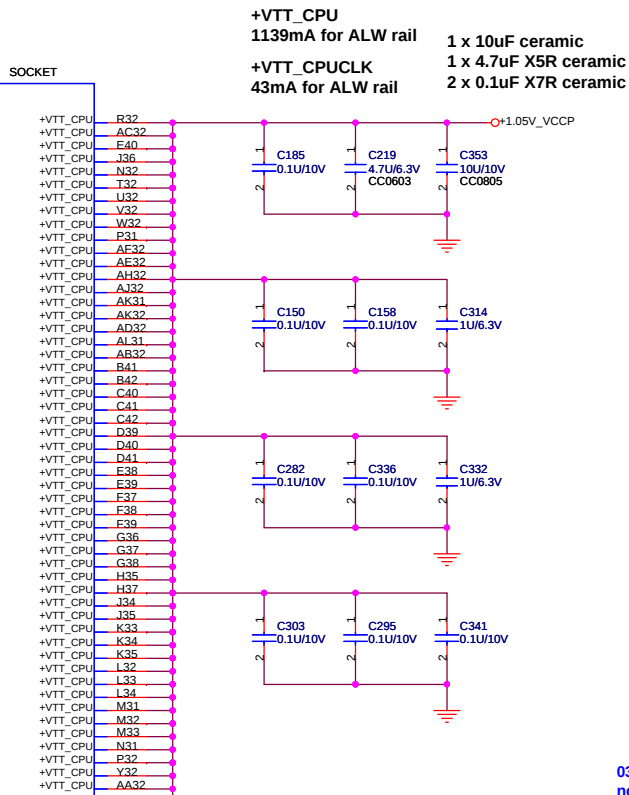
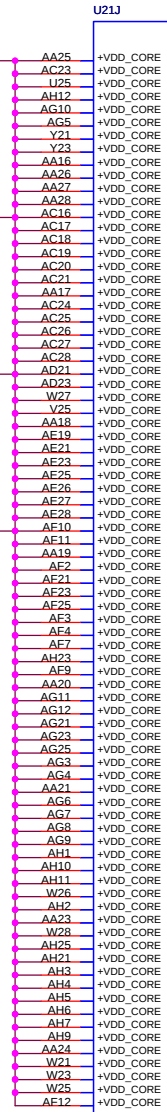
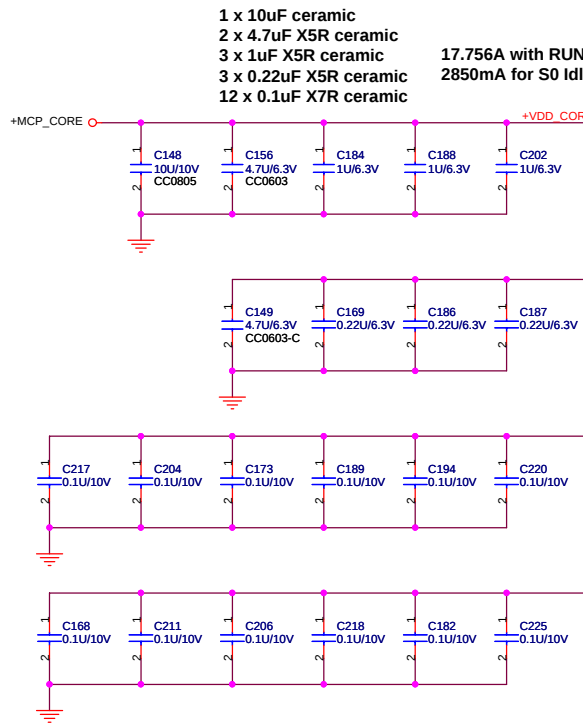
Title: MCP79 (HDA,MISC)

Size: Document Number IM3 (XPS-Jolie)

Date: Thursday, March 20, 2008

Sheet: 12 of 59

Rev: 1B



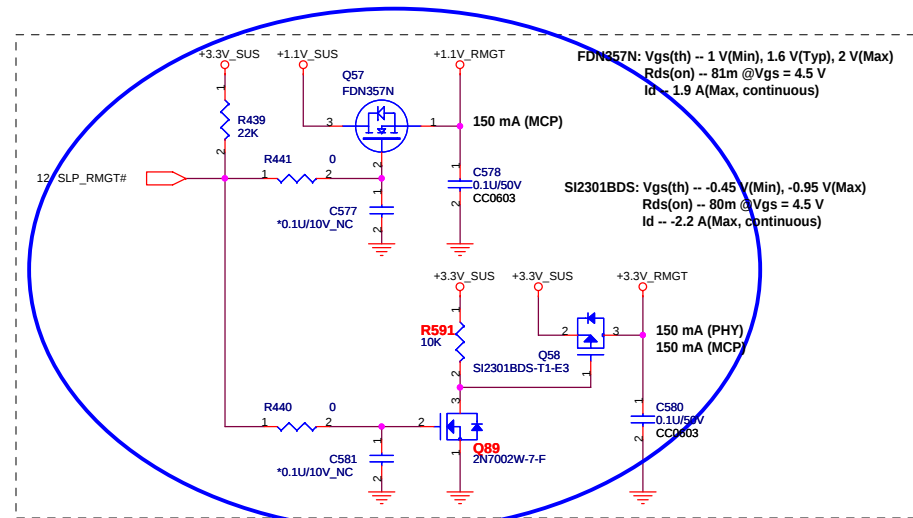
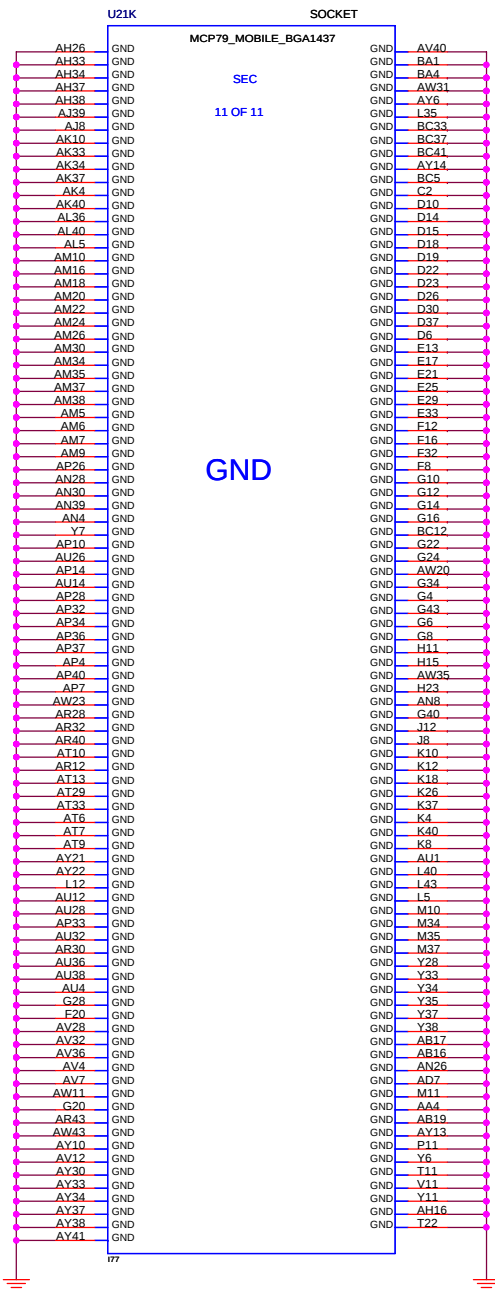
QUANTA COMPUTER

Title MCP79 (POWER)

Size Document Number IM3 (XPS-Jolie)

Rev 1A

Date: Thursday, March 20, 2008 Sheet 13 of 59



0229-Sun. 1.1V_RMGT & +3.3V_RMGT MOSFET Vgs aren't enough issue, modify circuit reference NV CRB

(Del JP11,JP12

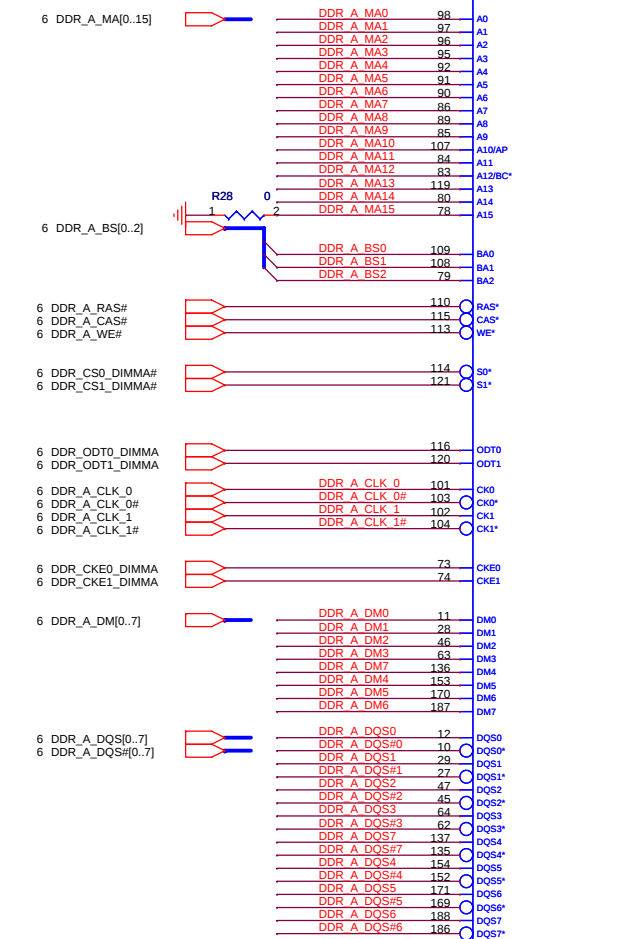
Change Q57 from SI2304BDS-T1-E3 to FDN357N, Q58 from SI2304BDS-T1-E3 to SI2301BDS-T1-E3

Add Q? with 2N7002,R? with 10K)



Title		
MCP79 (GND)		
Size	Document Number	Rev
	IM3 (XPS-Jolie)	1B
Date:	Thursday, March 20, 2008	Sheet 14 of 59

CN19A
DDR-AS0A62X-U2RN-204P
SO_DIMM204_DDR3

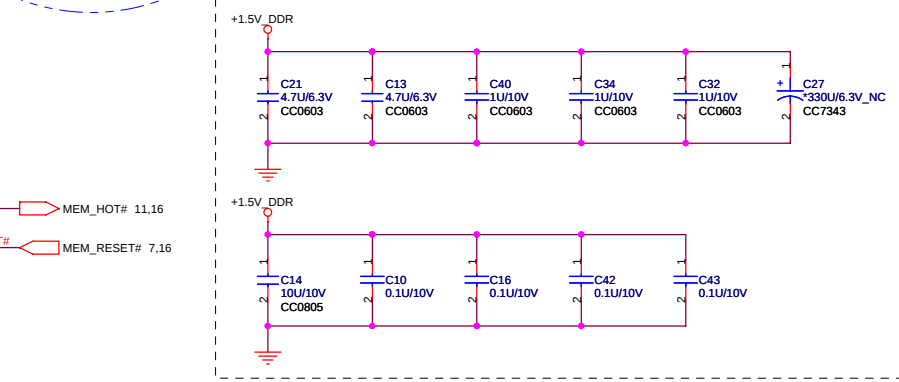
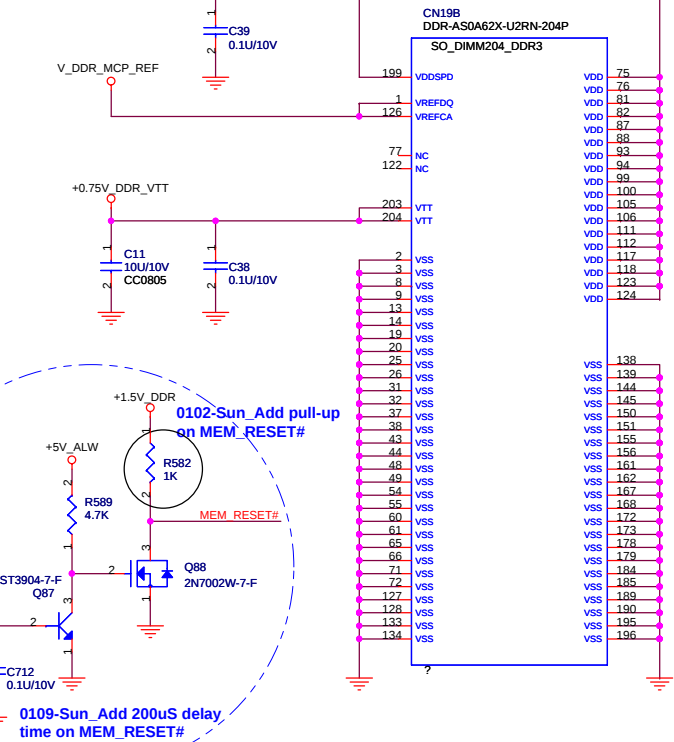
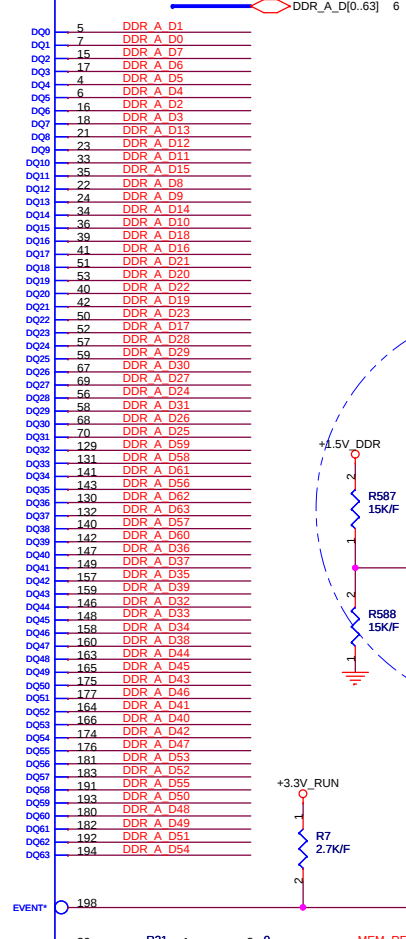
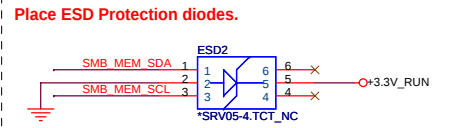


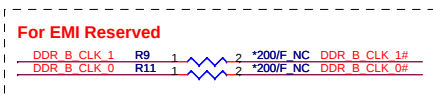
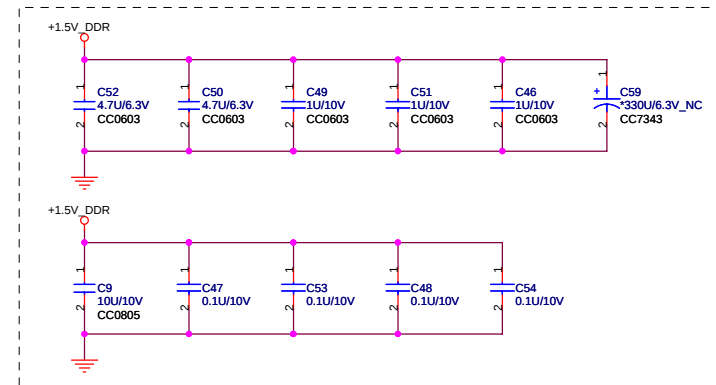
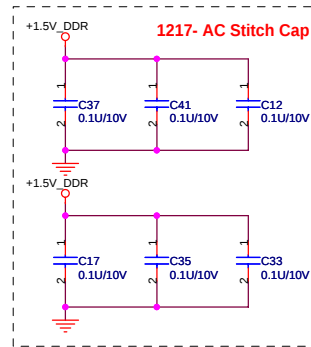
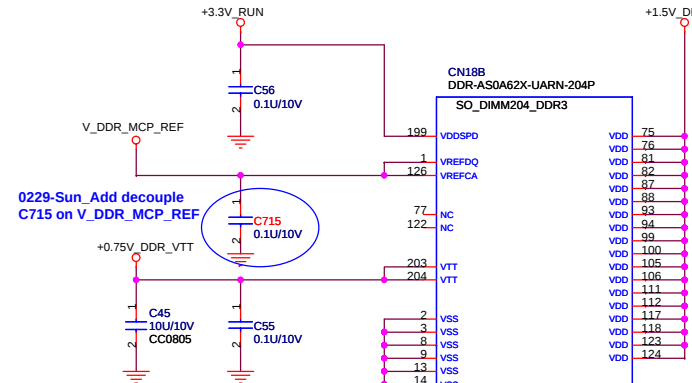
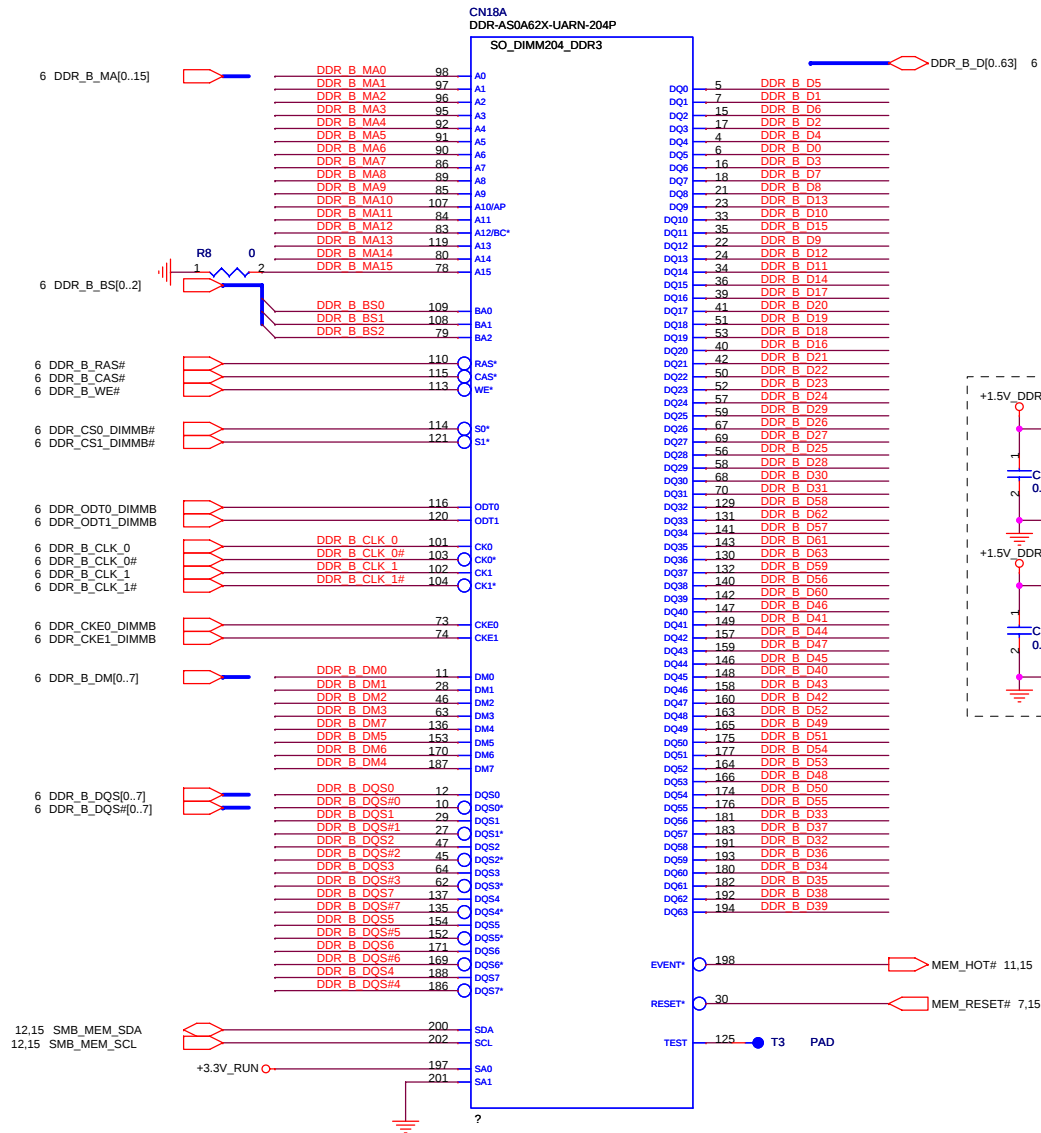
12.16 SMB_MEM_SDA
12.16 SMB_MEM_SCL

SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

For EMI Reserved

DDR_A_CLK_1 R19 1 2 *200/F NC DDR_A_CLK_1#
DDR_A_CLK_0 R30 1 2 *200/F NC DDR_A_CLK_0#





Title DDR3 SO-DIMM (204P)		
Size	Document Number IM3 (XPS-Jolie)	Rev 1A
Date:	Thursday, March 20, 2008	Sheet 16 of 59

8 PCIE_MTX_GRX_P[0..15]
8 PCIE_MTX_GRX_N[0..15]

1113-Sun_Swap PEG for routing smooth.

1115-Sun_Follow NV's command to swap PEG for routing

8 CLK_PCIE_VGA#
8 CLK_PCIE_VGA#
8,32,33,34 PE_RESET#
8,12 PE_RESET_MXM#

?_To GFX PWM
53 GFX_CORE_CNTRL0
53 GFX_CORE_CNTRL1
19 GFX_THERM_ALERT#
20,21 GDDR3_VREF_SW

+3.3V_NB9X
R108 43K/F
R102 10K
R116 5.1K/F
R119 39K/F
R104 29K/F
R167 10K
GPU JTAG TCLK
GPU JTAG TMS
GPU JTAG TDI
GPU JTAG TDO
GPU JTAG TRST#

Place together.

JTAG I/F

T54 PAD

U20A
PART 1 OF 5

PCI - EXPRESS INTERFACE

GPIO

JTAG

NB9M
PBG533-NVIDIA-GEFORCE6250
Footprint: BGA533-NVIDIA-NB9M-GS

Voltage Level shift

0311-Sun_Reserve GFX_THERM# to shutdown power.
(Add Q18, R540)

AD10 PCIE_MRX_GTX_C_P15 C142 1 2 0.1U/10V PCIE_MRX_GTX_P15
AD11 PCIE_MRX_GTX_C_N15 C155 1 2 0.1U/10V PCIE_MRX_GTX_N15
AD12 PCIE_MRX_GTX_C_P14 C163 1 2 0.1U/10V PCIE_MRX_GTX_P14
AD12 PCIE_MRX_GTX_C_N14 C171 1 2 0.1U/10V PCIE_MRX_GTX_N14
AD13 PCIE_MRX_GTX_C_P13 C139 1 2 0.1U/10V PCIE_MRX_GTX_P13
AD12 PCIE_MRX_GTX_C_N13 C128 1 2 0.1U/10V PCIE_MRX_GTX_N13
AD13 PCIE_MRX_GTX_C_P12 C181 1 2 0.1U/10V PCIE_MRX_GTX_P12
AD14 PCIE_MRX_GTX_C_N12 C190 1 2 0.1U/10V PCIE_MRX_GTX_N12
AD15 PCIE_MRX_GTX_C_P11 C191 1 2 0.1U/10V PCIE_MRX_GTX_P11
AC15 PCIE_MRX_GTX_C_N11 C201 1 2 0.1U/10V PCIE_MRX_GTX_N11
AD14 PCIE_MRX_GTX_C_P10 C172 1 2 0.1U/10V PCIE_MRX_GTX_P10
AD15 PCIE_MRX_GTX_C_N10 C179 1 2 0.1U/10V PCIE_MRX_GTX_N10
AC16 PCIE_MRX_GTX_C_P9 C222 1 2 0.1U/10V PCIE_MRX_GTX_P9
AD16 PCIE_MRX_GTX_C_N9 C215 1 2 0.1U/10V PCIE_MRX_GTX_N9
AD17 PCIE_MRX_GTX_C_P8 C224 1 2 0.1U/10V PCIE_MRX_GTX_P8
AD18 PCIE_MRX_GTX_C_N8 C230 1 2 0.1U/10V PCIE_MRX_GTX_N8
AC18 PCIE_MRX_GTX_C_P7 C213 1 2 0.1U/10V PCIE_MRX_GTX_P7
AD18 PCIE_MRX_GTX_C_N7 C203 1 2 0.1U/10V PCIE_MRX_GTX_N7
AD19 PCIE_MRX_GTX_C_P6 C247 1 2 0.1U/10V PCIE_MRX_GTX_P6
AD20 PCIE_MRX_GTX_C_N6 C239 1 2 0.1U/10V PCIE_MRX_GTX_N6
AD19 PCIE_MRX_GTX_C_P5 C232 1 2 0.1U/10V PCIE_MRX_GTX_P5
AD20 PCIE_MRX_GTX_C_N5 C237 1 2 0.1U/10V PCIE_MRX_GTX_N5
AD21 PCIE_MRX_GTX_C_P4 C290 1 2 0.1U/10V PCIE_MRX_GTX_P4
AC21 PCIE_MRX_GTX_C_N4 C296 1 2 0.1U/10V PCIE_MRX_GTX_N4
AD21 PCIE_MRX_GTX_C_P3 C301 1 2 0.1U/10V PCIE_MRX_GTX_P3
AD22 PCIE_MRX_GTX_C_N3 C309 1 2 0.1U/10V PCIE_MRX_GTX_N3
AC22 PCIE_MRX_GTX_C_P2 C248 1 2 0.1U/10V PCIE_MRX_GTX_P2
AD22 PCIE_MRX_GTX_C_N2 C259 1 2 0.1U/10V PCIE_MRX_GTX_N2
AD23 PCIE_MRX_GTX_C_P1 C271 1 2 0.1U/10V PCIE_MRX_GTX_P1
AD24 PCIE_MRX_GTX_C_N1 C286 1 2 0.1U/10V PCIE_MRX_GTX_N1
AE25 PCIE_MRX_GTX_C_P0 C264 1 2 0.1U/10V PCIE_MRX_GTX_P0
AE26 PCIE_MRX_GTX_C_N0 C268 1 2 0.1U/10V PCIE_MRX_GTX_N0

AE10 PEX_TSTCLK_OUT# R381 2 200/F
AE10 PEX_TSTCLK_OUT#
AG10 PEX_TERM R362 1 2.49K/F

1115-Sun_Follow NV's command to swap PEG for routing smooth

0321-Stege Change Resistor Value from 20K to 10K

B10 R110 2 10K
A10 R115 1 5.1K/F
C10 R106 1 15K/F
+3.3V_NB9X

VRAM Strap:ROM_SI

ID	ROM_SI	Memory part
01	Pull down 20K	Samsung
02	Pull down 10K	Infineon
03		
04		

GPIO USAGE

GPIO	I/O	ACTIVE	USAGE	Used
0	IN	N/A	NVGEM HOTPLUG DETECT	
1	IN	N/A	DVI/HDMI LINKC HOTPLUG DETECT	
2	OUT	HIGH	PANEL BACKLIGHT PWM	
3	OUT	HIGH	PANEL POWER ENABLE	
4	OUT	HIGH	PANEL BACKLIGHT ENABLE	
5	OUT	HIGH	NVDD ALTV0	
6	OUT	HIGH	NVDD ALTV1	
7	OUT	HIGH	FBVDD VID0	
8	IN	LOW	OVERTEMP ALERT	
9	OUT	LOW	THERMAL ALERT	
10	OUT	HIGH	DYNAMIC FB VREF GDDR3 (not used for DDR2)	
11	OUT	HIGH	SLI SYNC0 (not used for GB1-64)	
12	IN	N/A	AC DETECT	
13	OUT	LOW	POWER SUPPLY CONTROL0	
14	OUT	HIGH	POWER SUPPLY CONTROL1	
15	IN	N/A	HPD_E	
16	IN	N/A	DVI_E	No
17	IN	N/A	HDMI_E	No
18	IN	N/A	DVI_F (not used)	No
19	IN	N/A	HDMI_F (not used)	No

QUANTA
COMPUTER

Title
VGA-NB9X GB1-64 (PCIE,PCIE POWER)

Size

Document Number
IM3 (XPS-Jolie)

Rev
1A

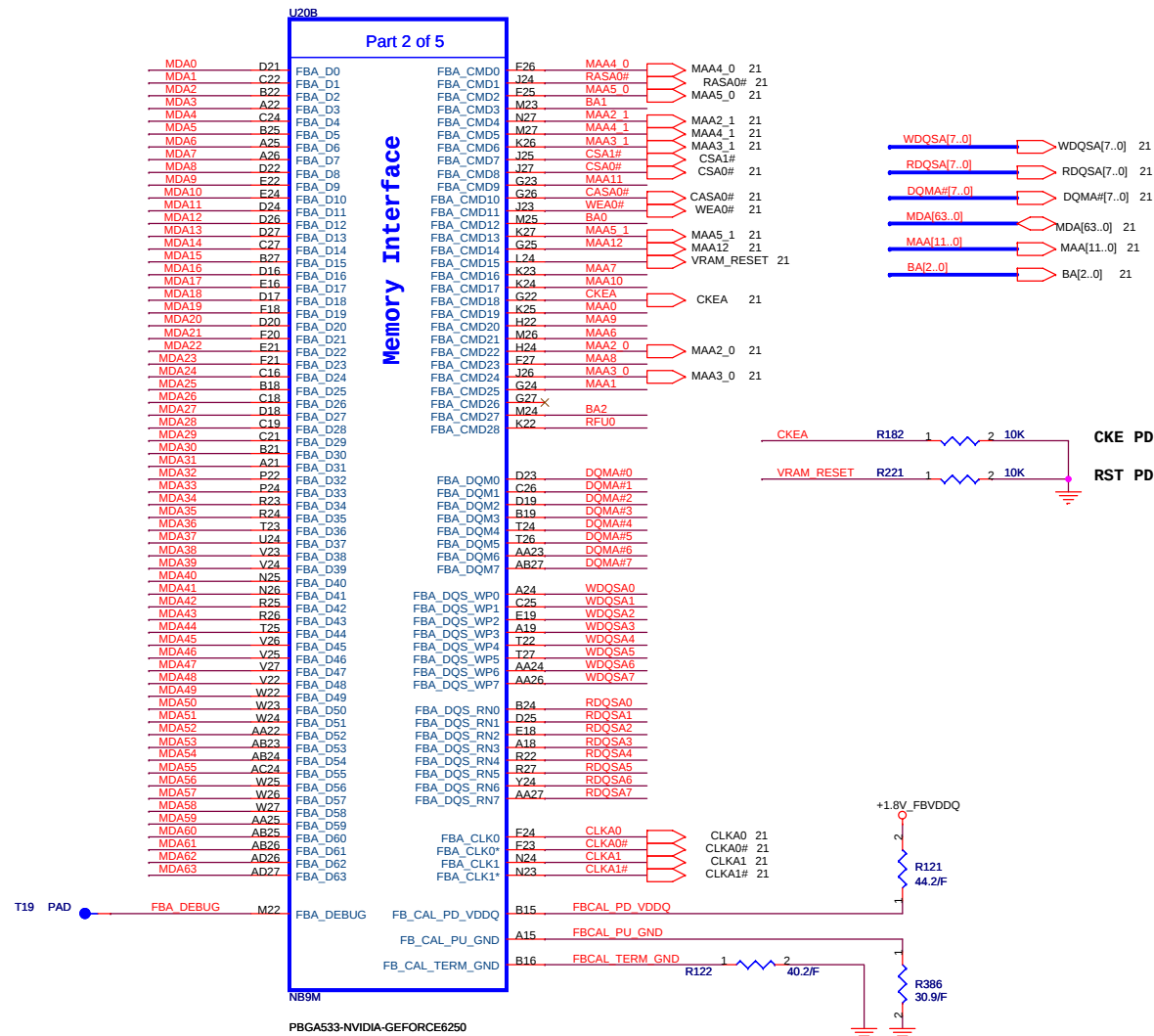
Date: Friday, March 21, 2008

Sheet

17

of

59



Update as "PUN-03303-001_V01".

GPU Driver Calibration			
Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ
DDR2	1.8V	30.1	30.1
GDDR3	1.8V	30.9	44.2
GDDR3 DVS	1.8V/1.5V	30.9	44.2

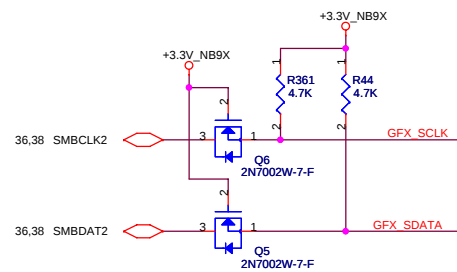
Note: Use only 1% resistors for driver calibration



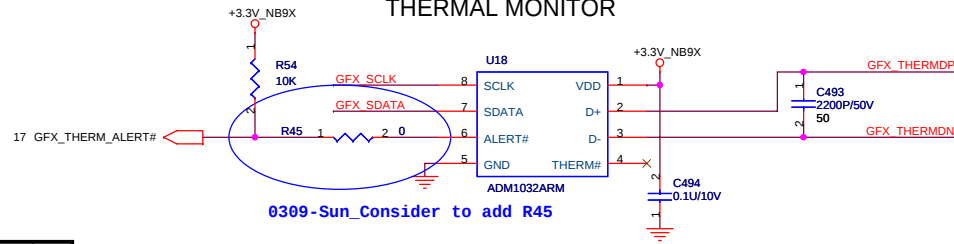
Title VGA-NB9X GB1-128 (Frame Buffer Channel A)

Size Document Number IM3 (XPS-Jolie) Rev 1A

Date: Thursday, March 20, 2008 Sheet 18 of 59



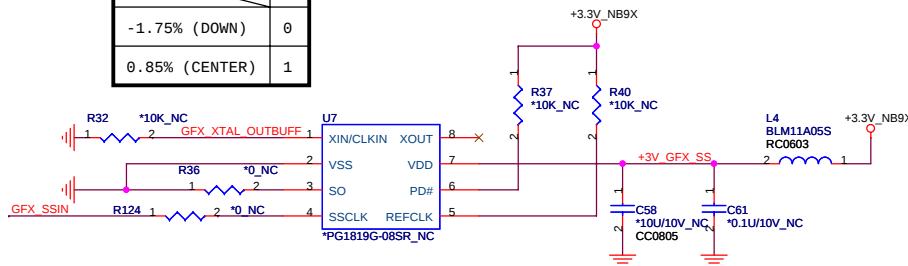
THERMAL MONITOR



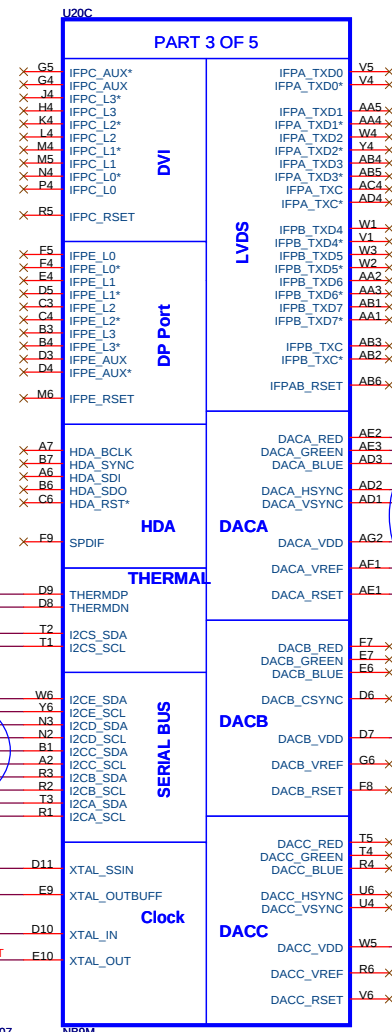
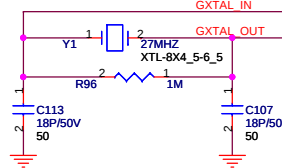
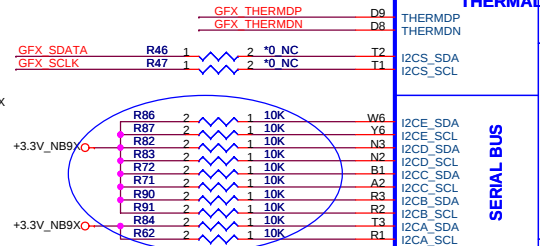
0309-Sun_Consider to add R45

	S0
-1.75% (DOWN)	0
0.85% (CENTER)	1

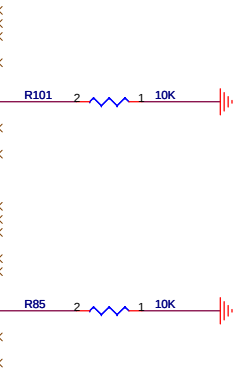
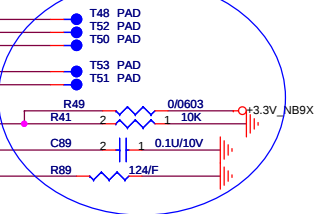
SPREAD SPECTRUM

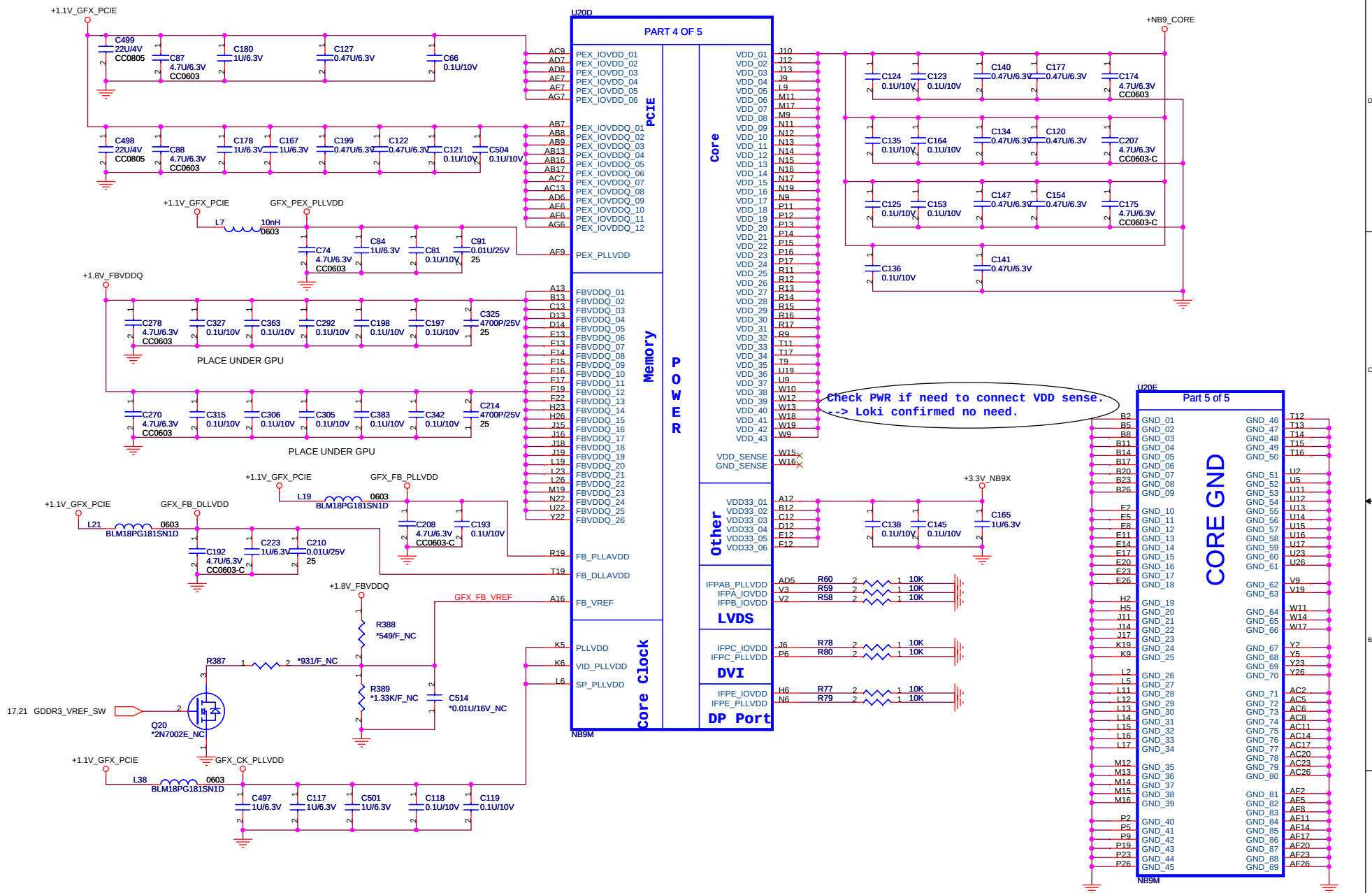


0309-Sun_Consider to change to R-pack ?

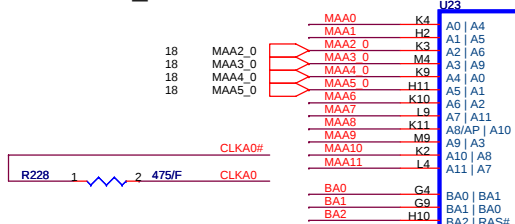


Reserve CRT for debug on first build.
Remove all of parts except DACA_VDD supply before QT.

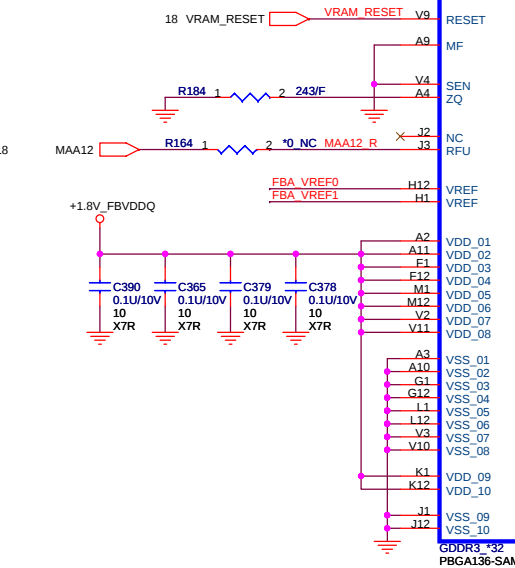




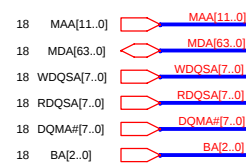
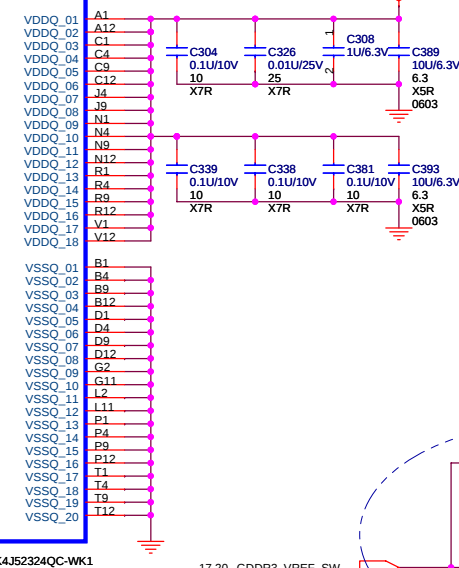
GDDR3 _M*32



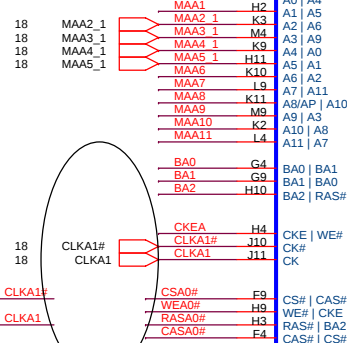
1114-Sun_Swap GDDR3
Data for routing smooth.



GDDR3 _M*32

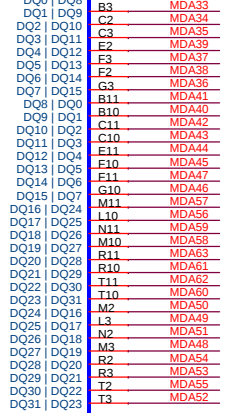


1114-Sun_Swap GDDR3
Data for routing smooth.

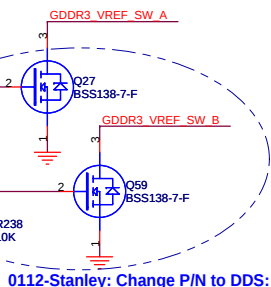
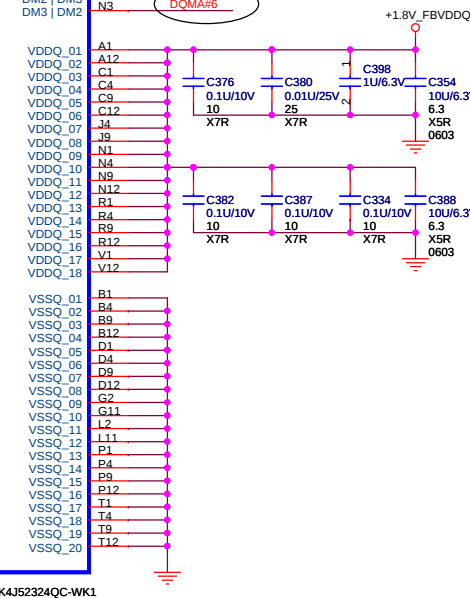


1114-Sun_Swap GDDR3
Data for routing smooth.

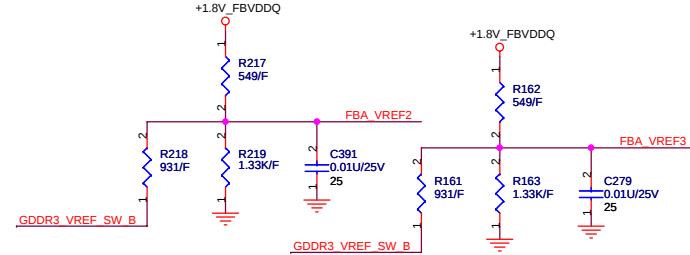
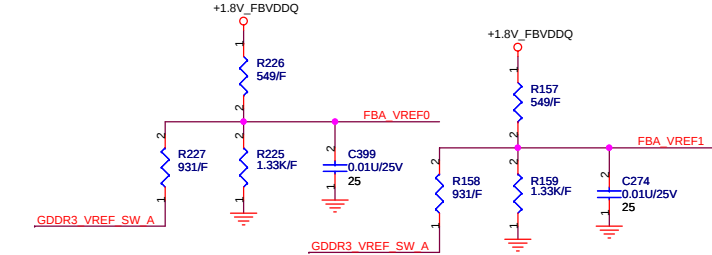
GDDR3 _M*32



1114-Sun_Swap GDDR3
Data for routing smooth.



0112-Stanley: Change P/N to DDS: BSS138-7-F.

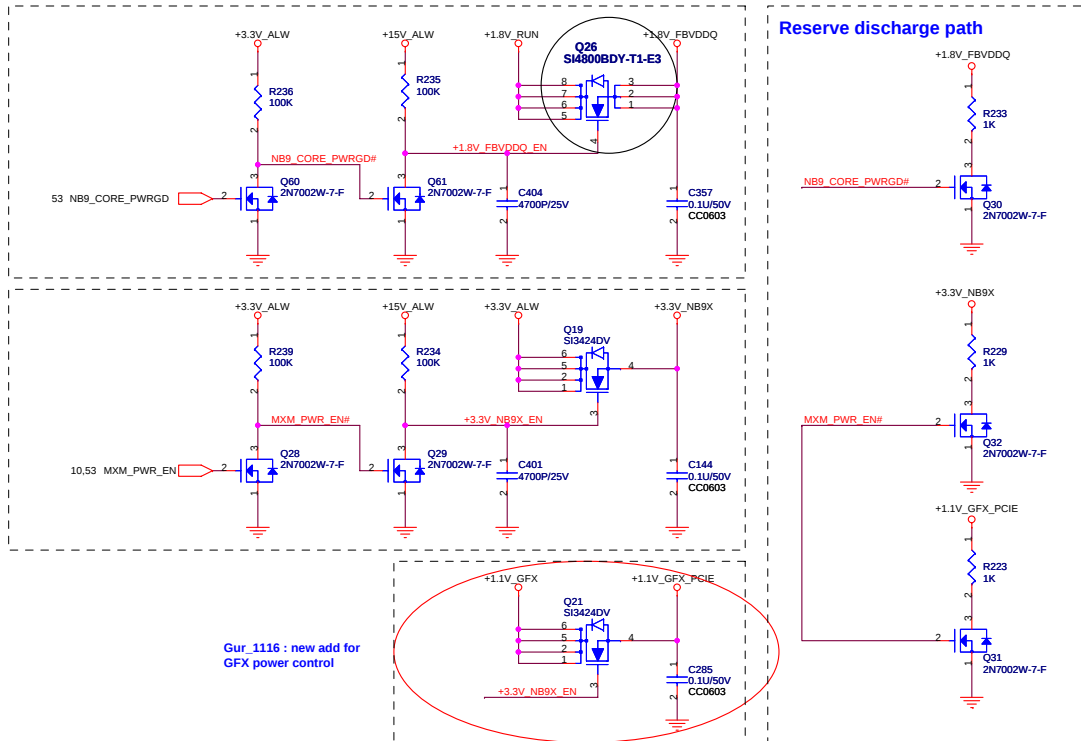


QUANTA
COMPUTER

Title VGA-NB9X GB1-64 (HybridSLI SWITCH)		
Size IM3 (XPS-Jolie)	Document Number IM3 (XPS-Jolie)	Rev 1B
Date Thursday, March 20, 2008	Sheet 21	of 59

**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

1225-Sun_Chenge Q26 from
SI4812BDY to SI4800BDY-T1-E3.

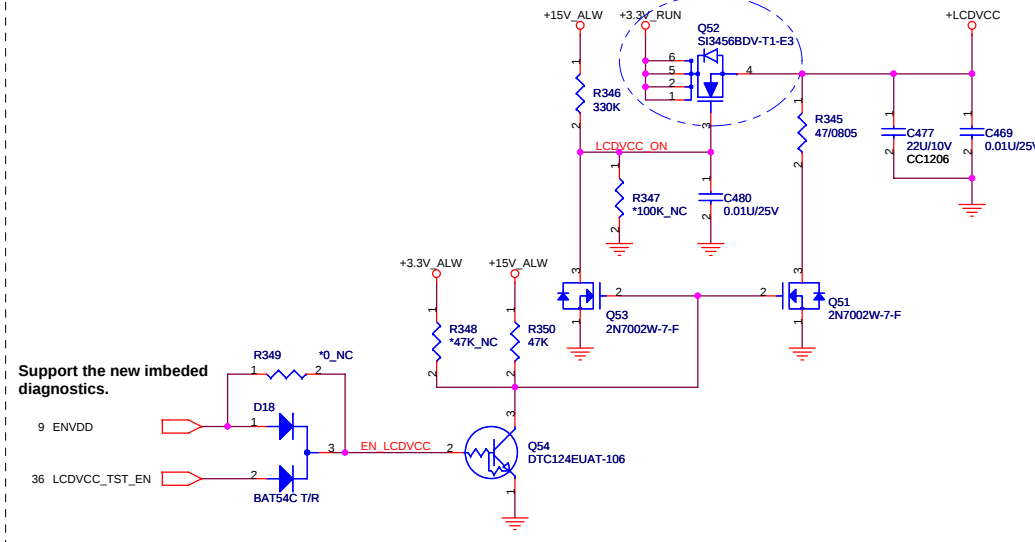


Gur_1116 : new add for
GFX power control

**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

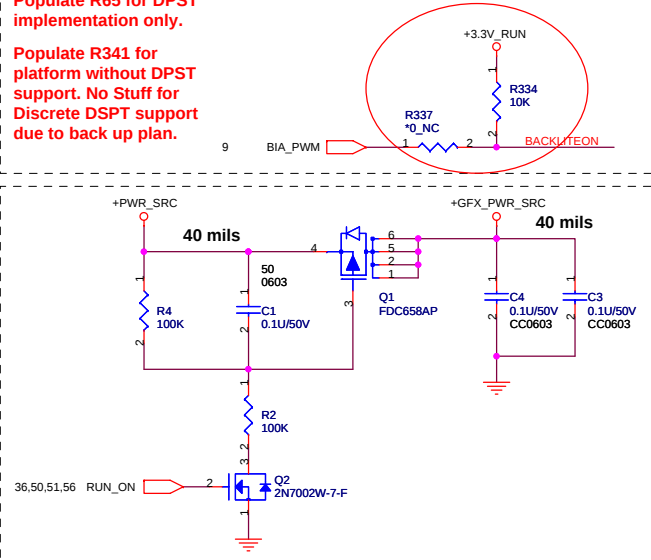
**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

0112-Stanley: Change BOM for EOL issue (SI3456BDV).

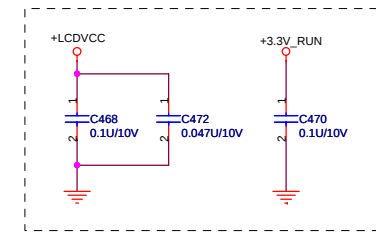
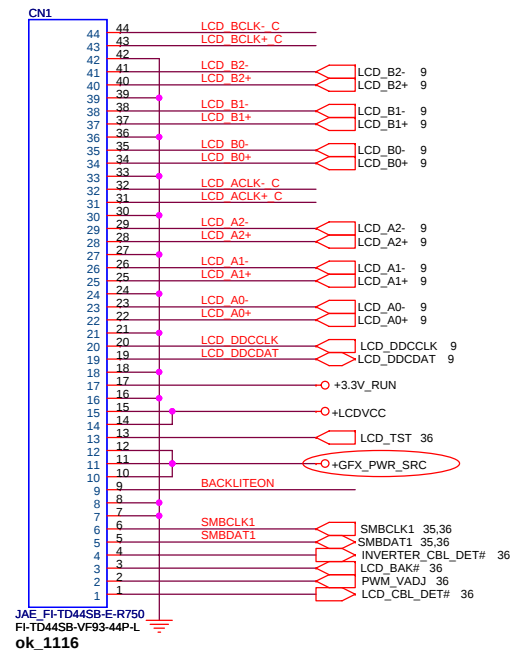


Populate R65 for DPST implementation only.

Populate R341 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.



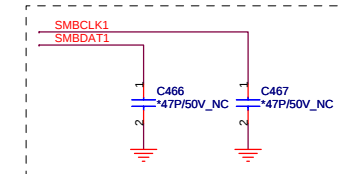
GND,VCC要用最粗的電子線



WXGA 1280*800=>70 MHz
WXGA+ 1440*900=>108 MHz
WSXGA+ 1680*1050=>120MHz
WUXGA 1920*1200=>166 MHz

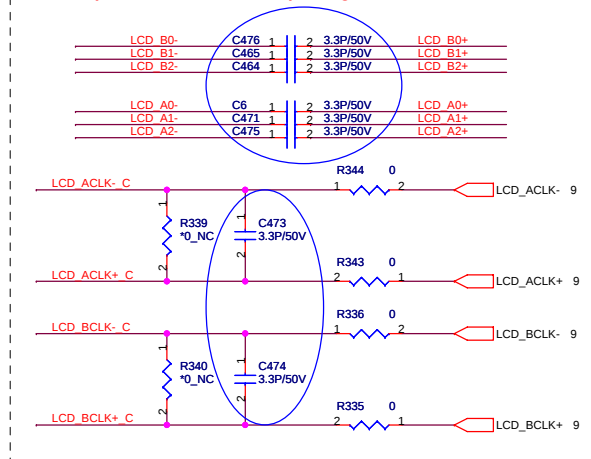
Address : A9H --Contrast
AAH --Backlight

MBRAI specification of antenna gain is 10dBi@474MHz, -7dBi@698MHz, -5dBi@858MHz.



0319-Sun_Pop 3.3P on LVDS bus for COMM team demand

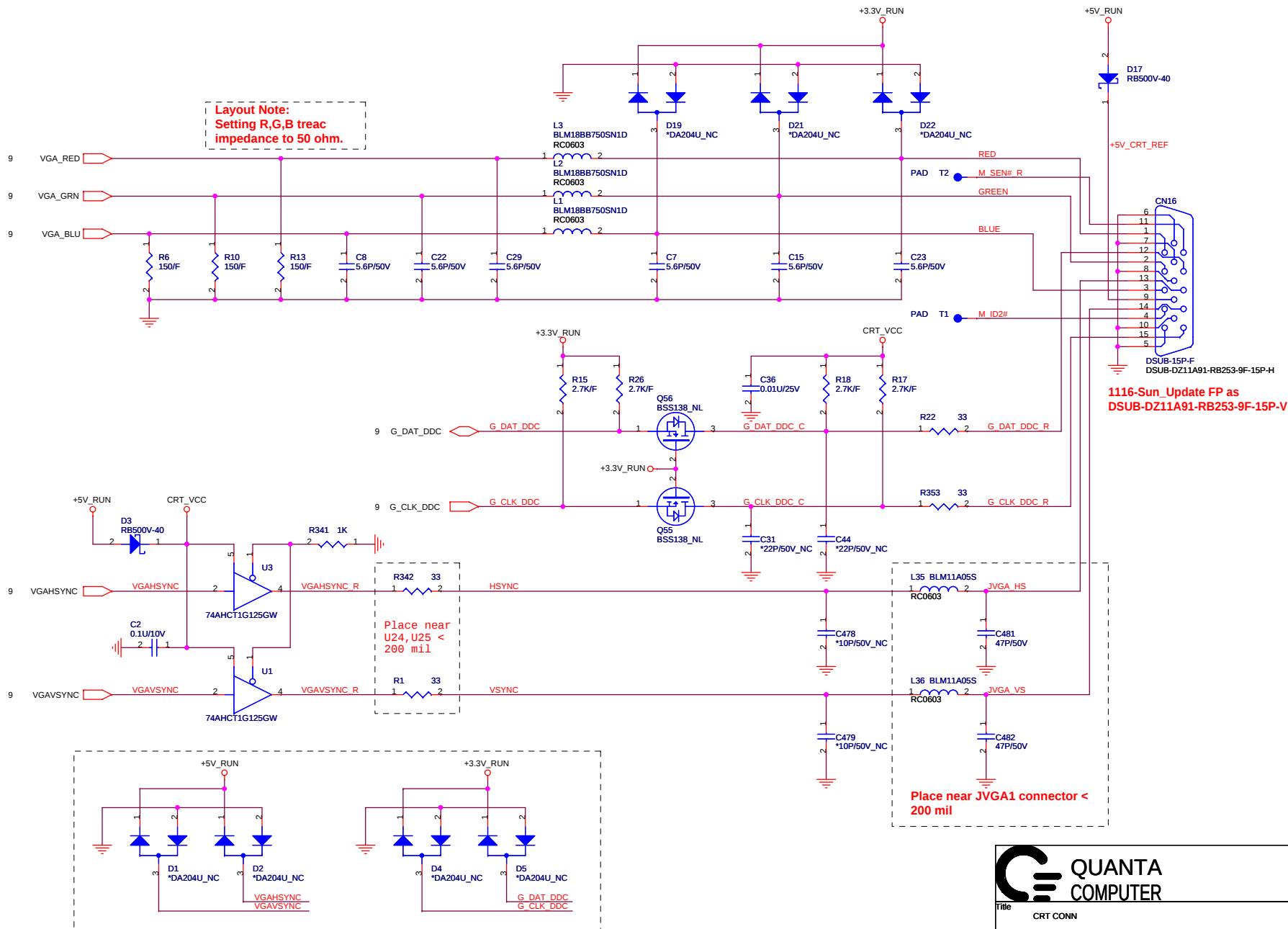
Shunt capacitors on LVDS for improving WWAN.

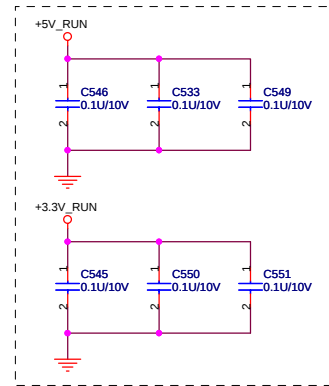
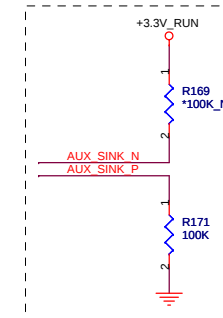
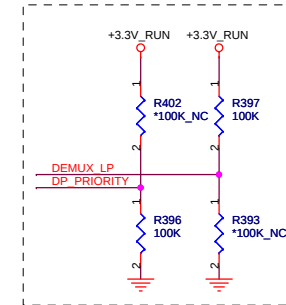
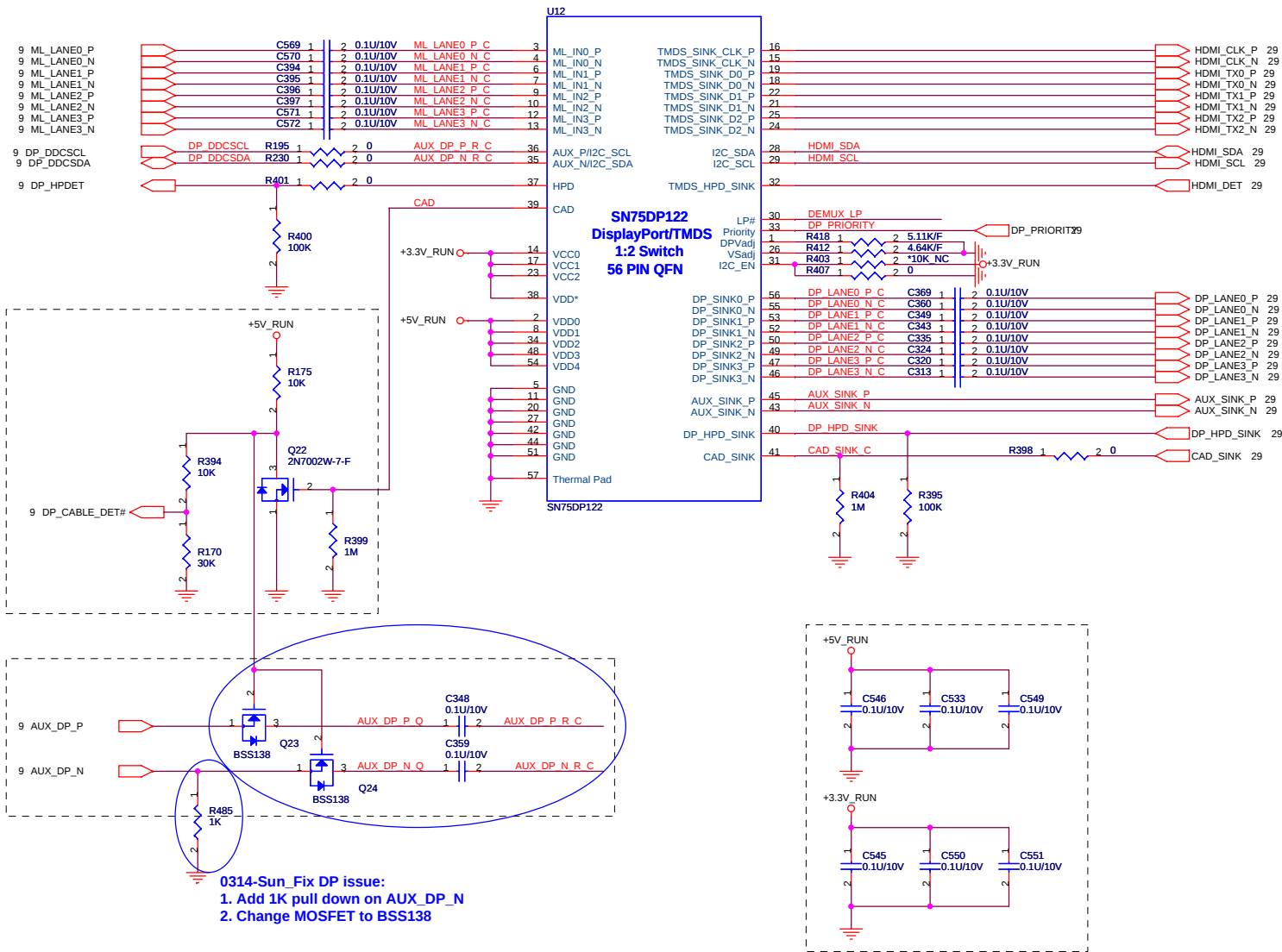


Title LCD CONN

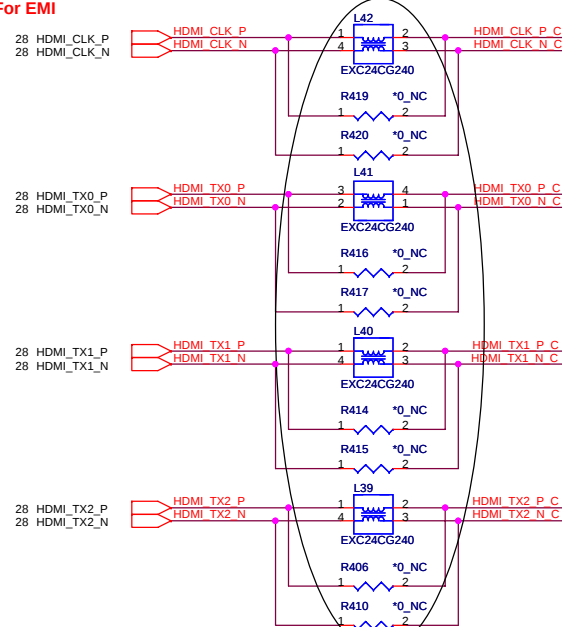
Size	Document Number IM3 (XPS-Jolie)
------	------------------------------------

Date: Thursday, March 20, 2008 Sheet 26 of 59

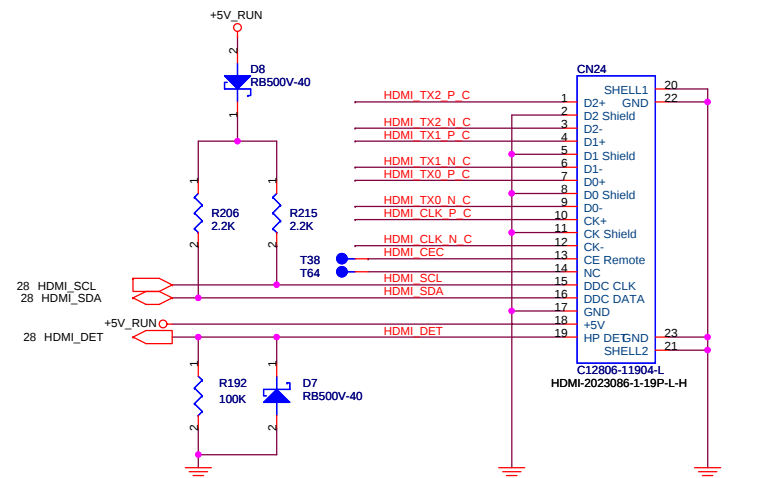




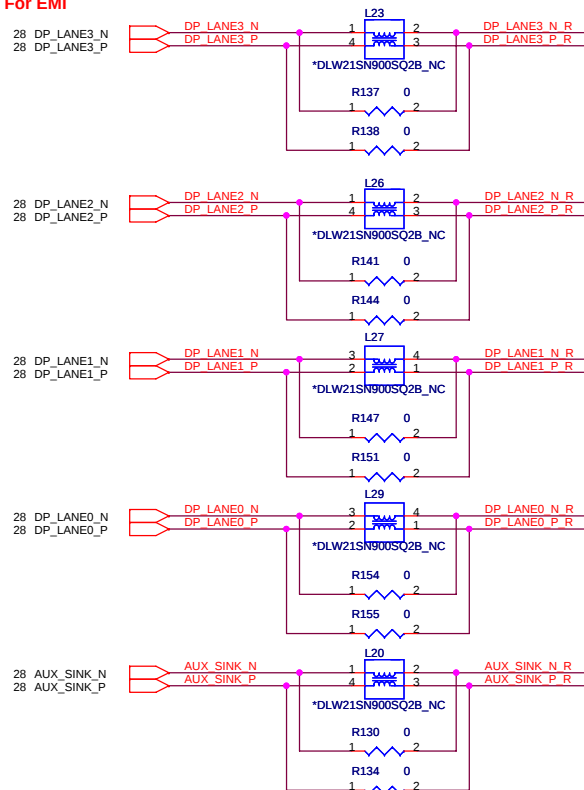
Reserve For EMI



HDMI CONNECTOR

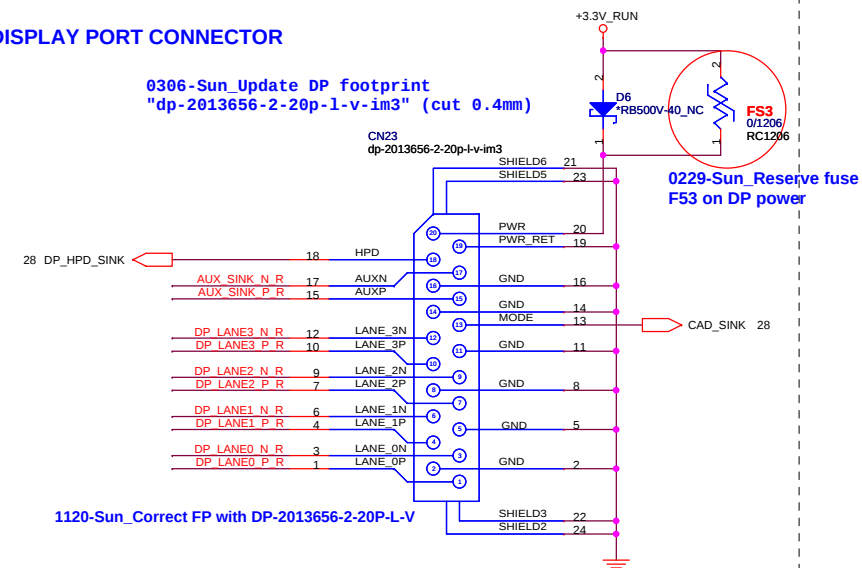


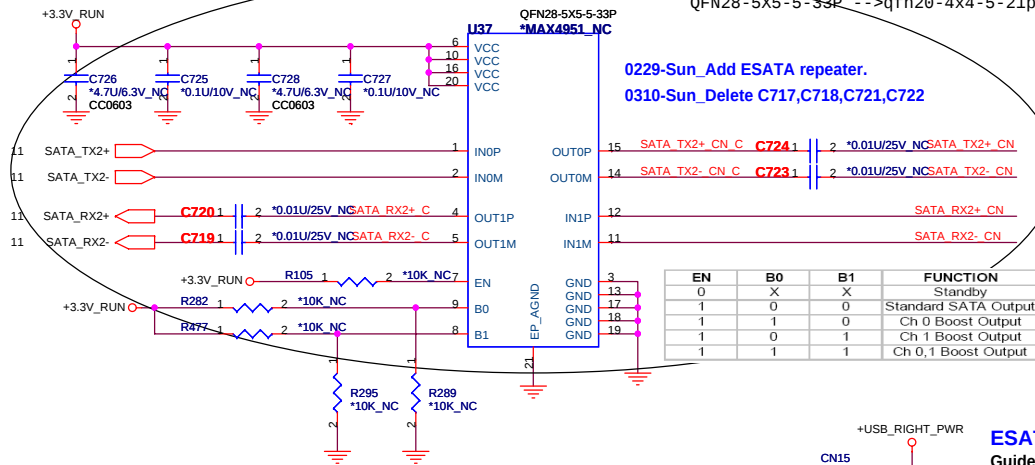
Reserve For EMI



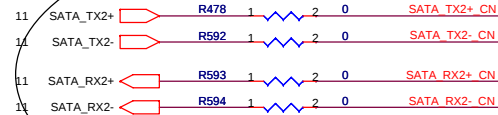
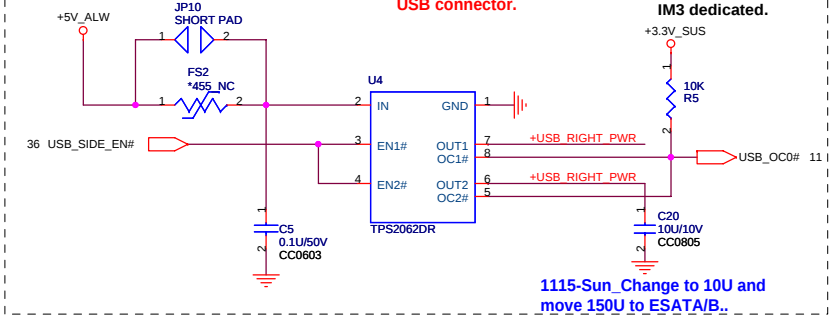
DISPLAY PORT CONNECTOR

0306-Sun_Update DP footprint
"dp-2013656-2-20p-1-v-im3" (cut 0.4mm)





USB POWER SW



0306-Sun_Add ESATA jump RES.

ESATA/B CONN

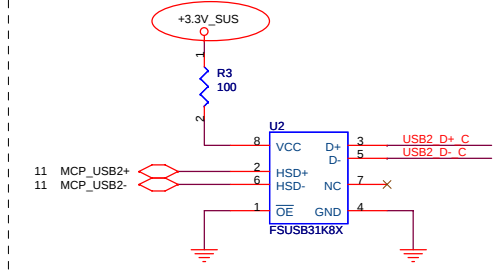
Guide pin type.
 Need to stagger power & GND if not guide pin type.

0229-Sun_Add detect pin for ESATA.

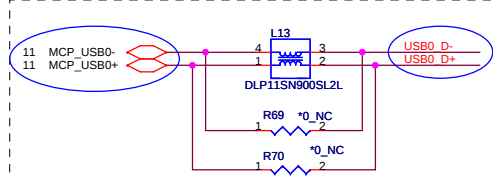
0306-Sun_Swap pin to align ESATA/B.

GND,VCC要用最粗的电子线

USB BUS SW

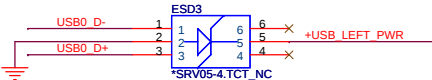


0318-Sun_change left USB port from port1 to port0

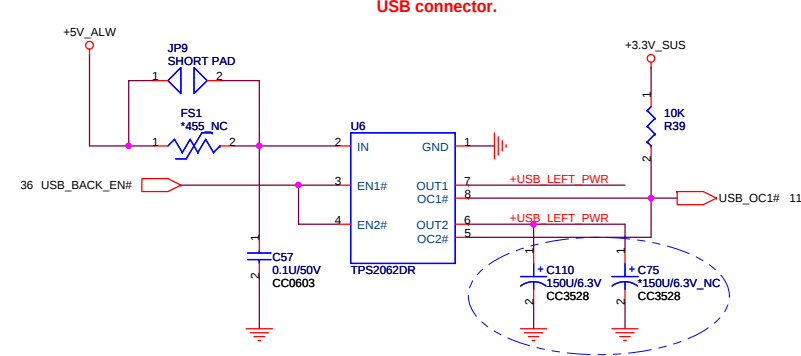


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.

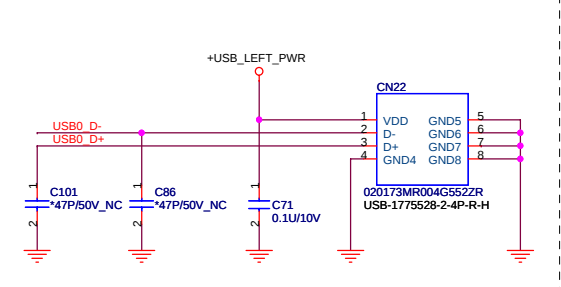


USB POWER SW

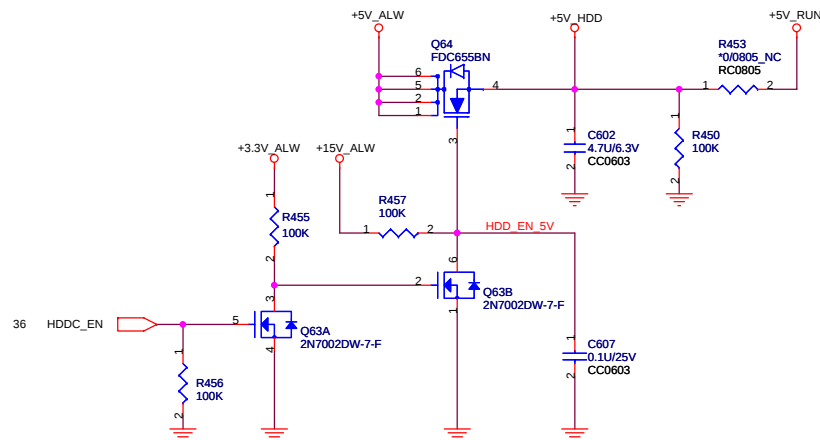
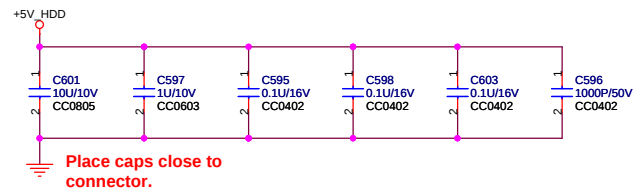
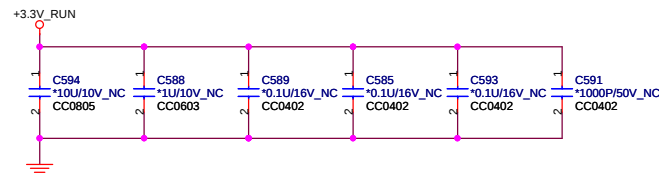
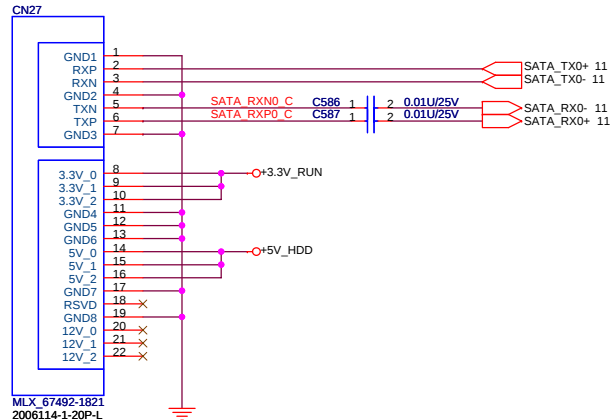


0111-Stanley: Change BOM from to 6.3V_3528.

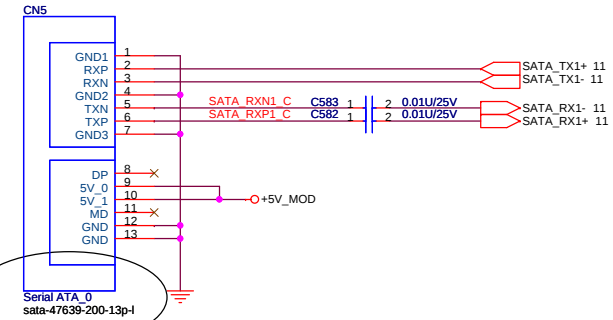
USB CONN



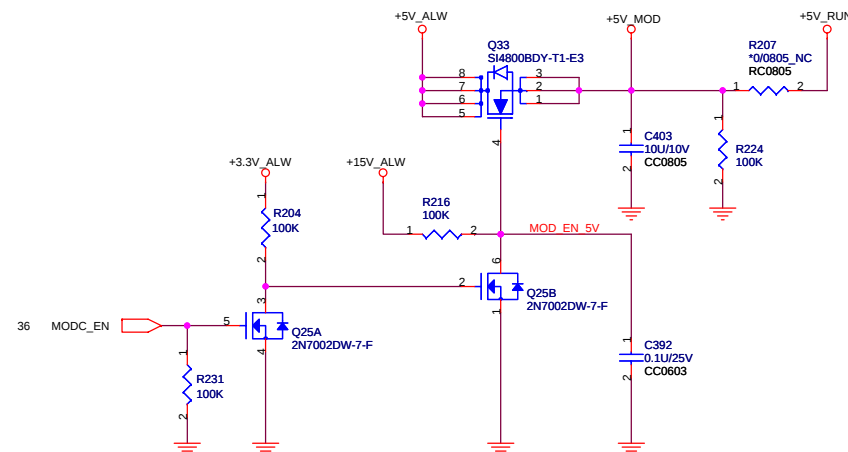
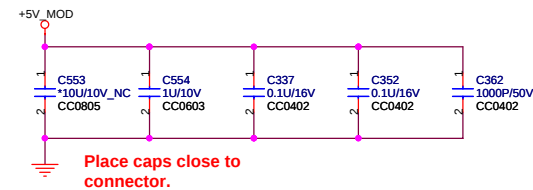
SATA HDD Connector



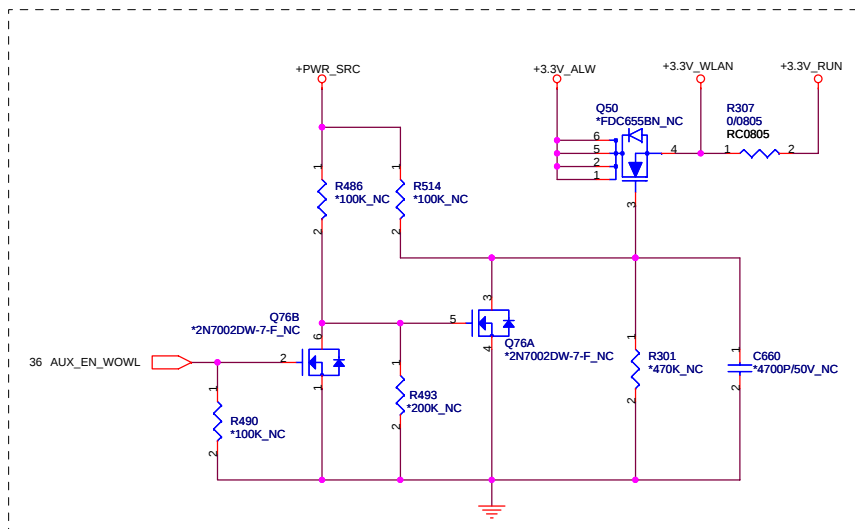
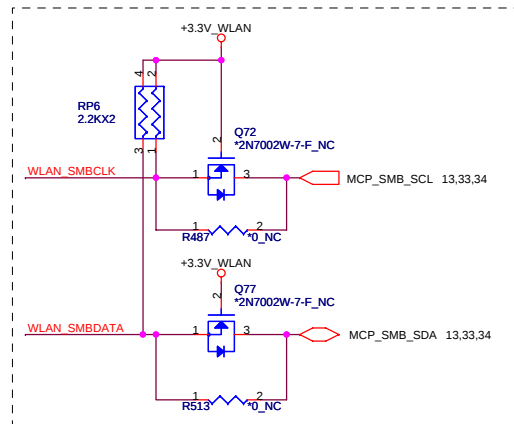
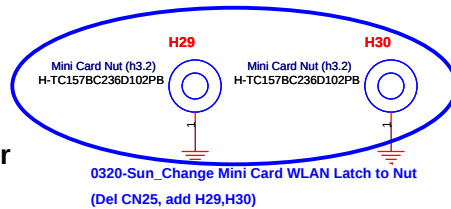
SATA ODD Connector

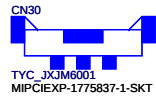


0306-Sun_Change to new footprint_sata-47639-200-13p-l

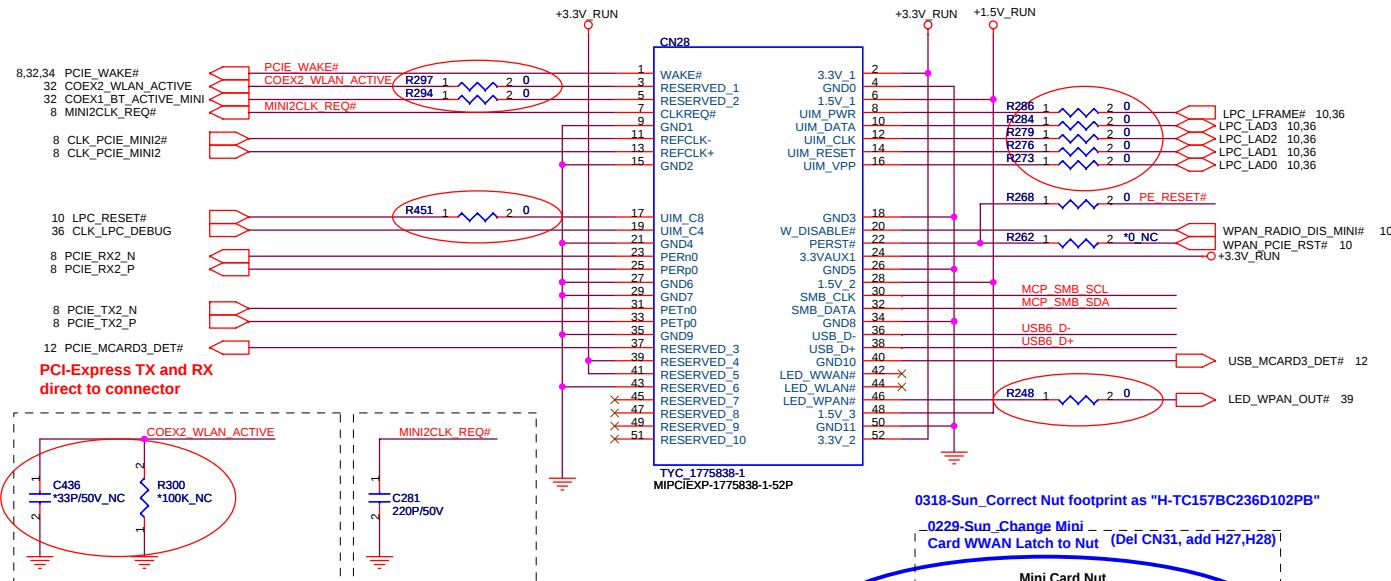


Title		
SATA (HDD&CD ROM)		
Size	Document Number	Rev
	IM3 (XPS-Jolie)	1A
Date:	Friday, March 21, 2008	Sheet 31 of 59

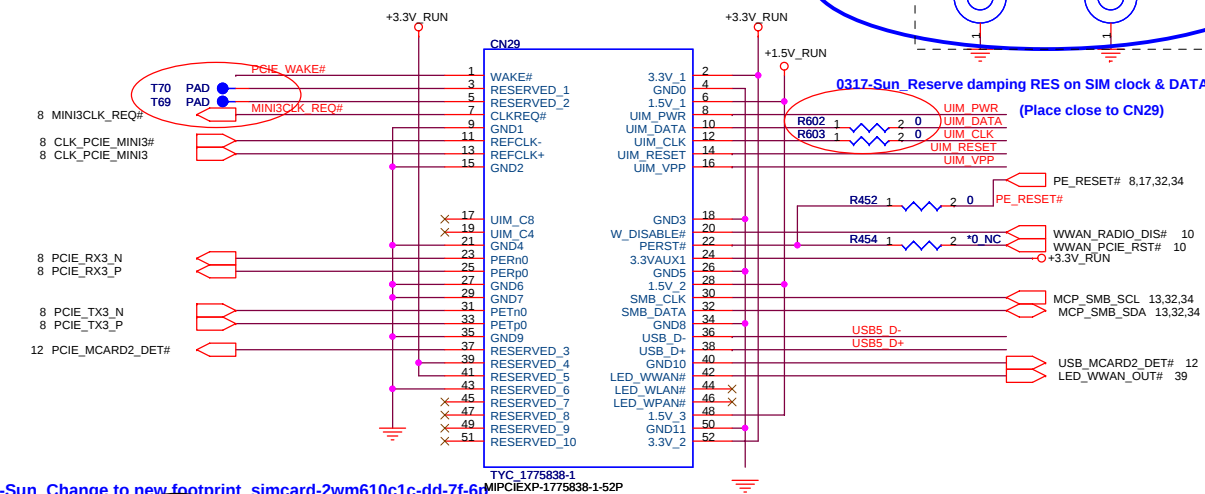
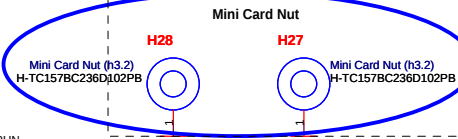




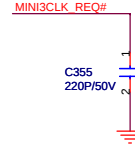
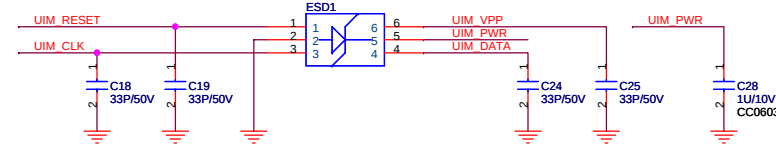
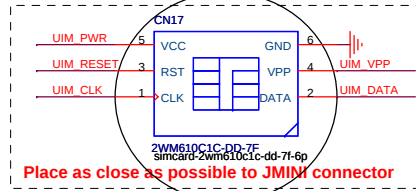
MiniCard Robson, BT. UWB Connector



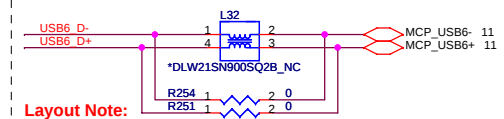
MiniCard WWAN Connector



0306-Sun_Change to new footprint_simcard-2wm610c1c-dd-7f-6p



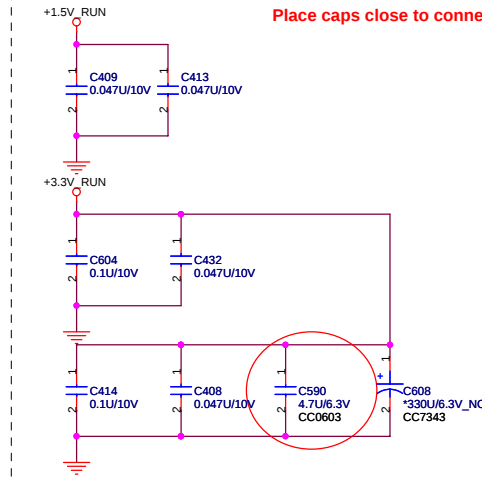
Reserve For EMI



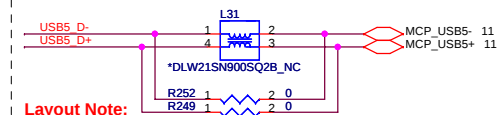
Layout Note:

R240 and R244 close to choke as possible to minimize stubs.

Place caps close to connector.



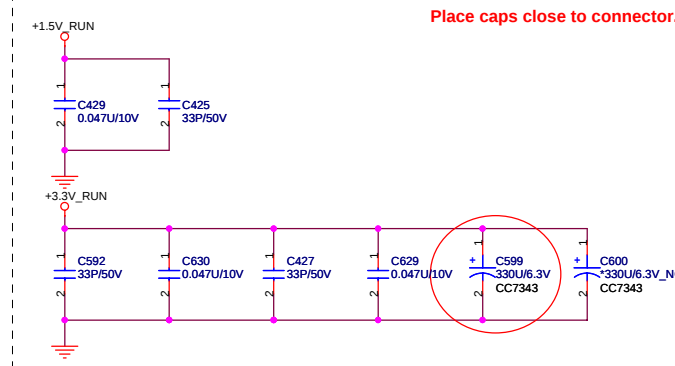
Reserve For EMI



Layout Note:

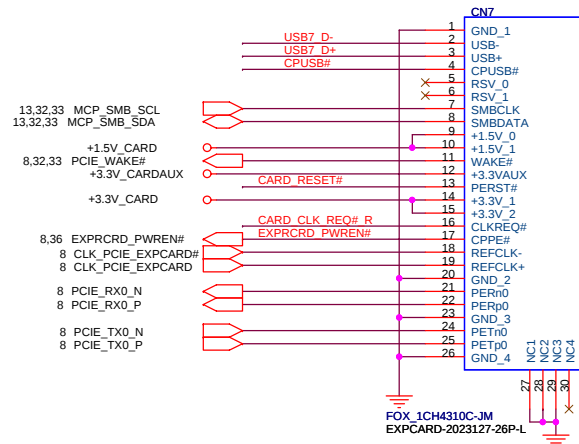
R240 and R244 close to choke as possible to minimize stubs.

Place caps close to connector.

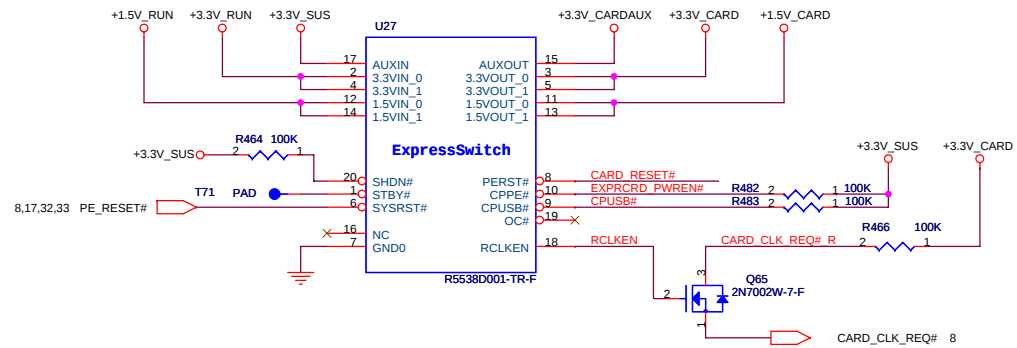


Title			
MINI-CARD (WWAN,WPAN)			
Size	Document Number		Rev
	IM3 (XPS-Jolie)		1A
Date:	Friday, March 21, 2008	Sheet	33 of 59

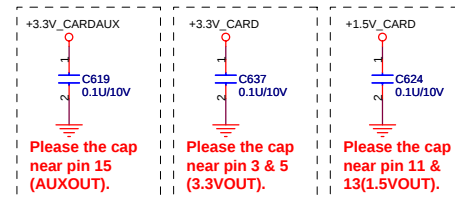
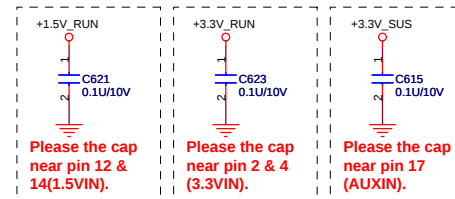
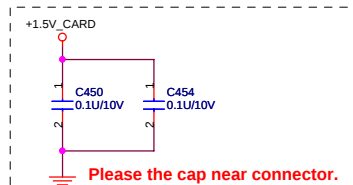
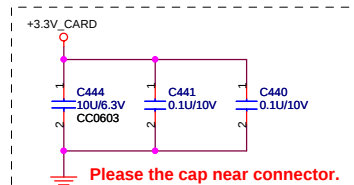
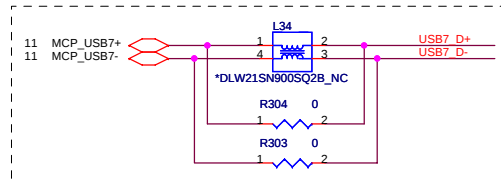
Express Card



+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



PCI-Express TX and RX direct to connector.



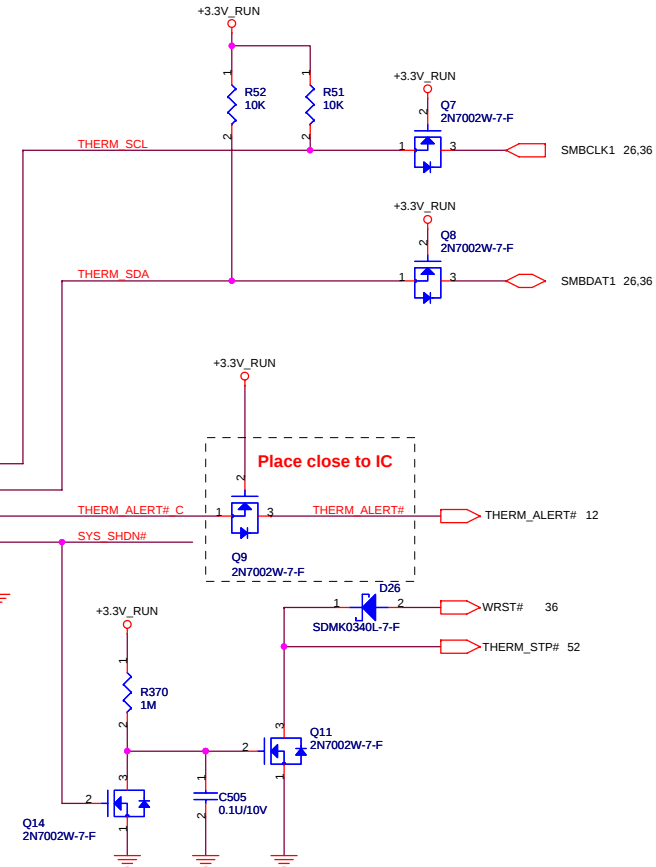
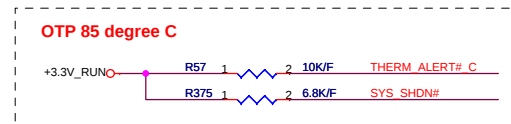
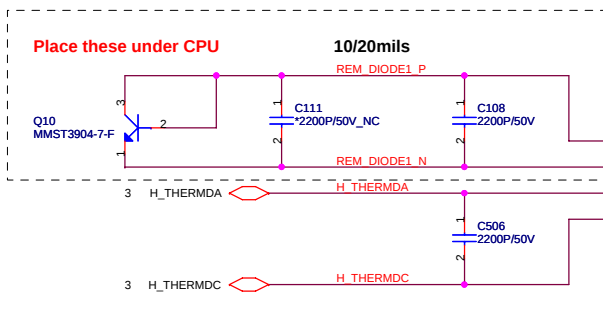
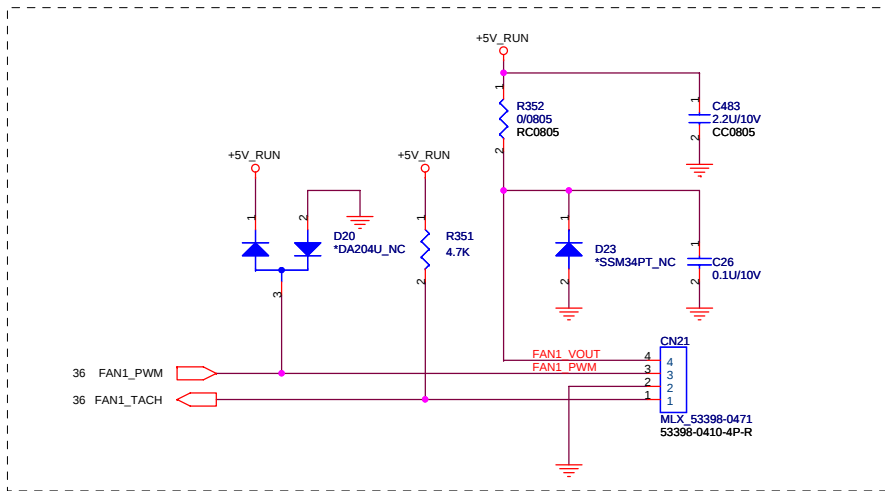
Title ExpressCard

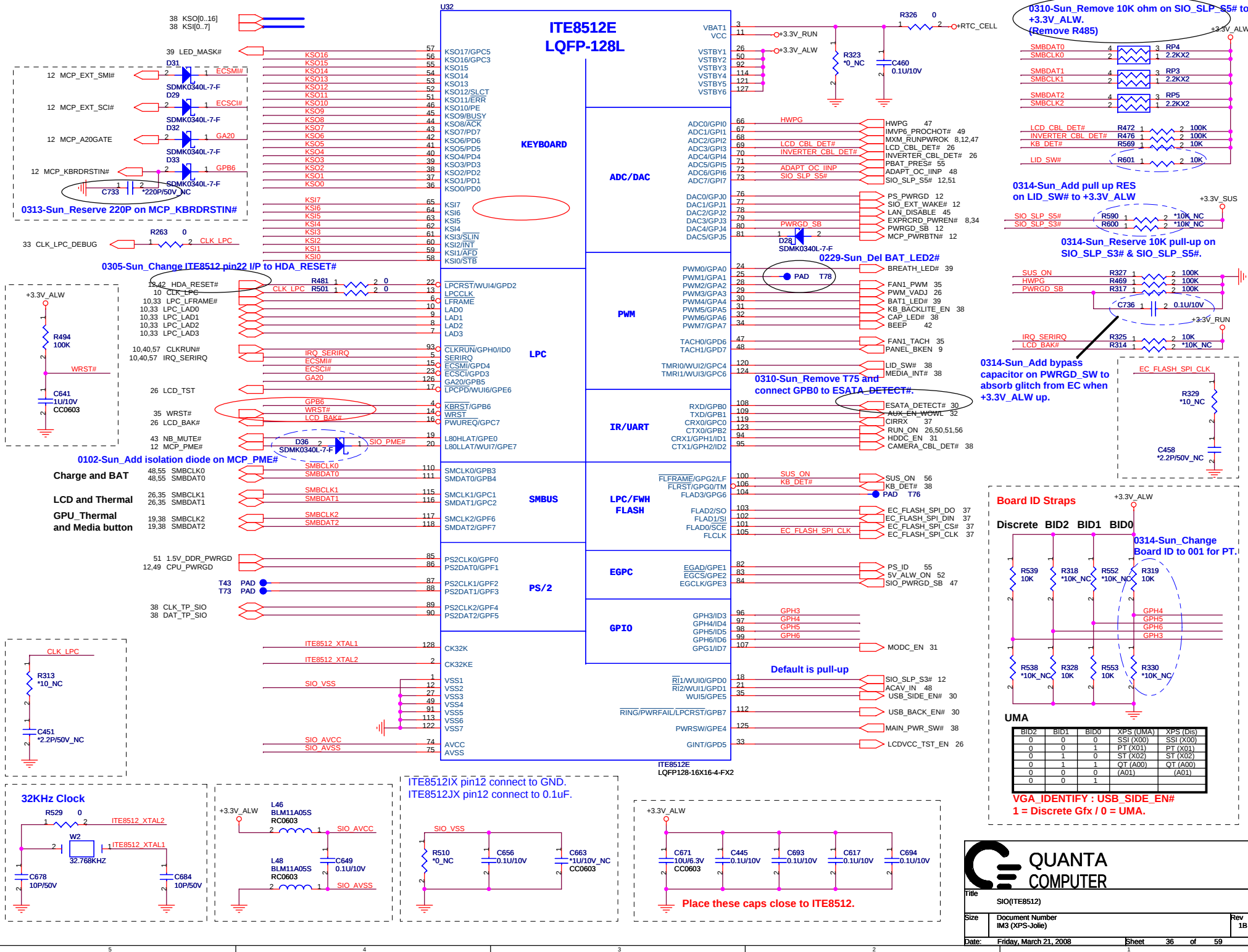
Size	Document Number IM3 (XPS-Jolie)
------	------------------------------------

Rev
1A

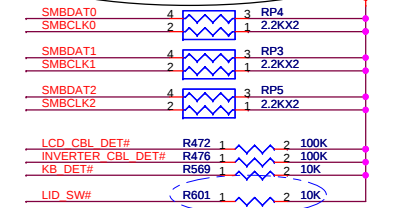
Date: Thursday, March 20, 2008

Sheet 34 of 59

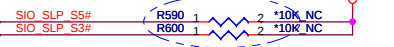




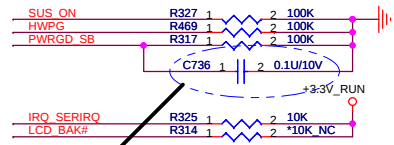
0310-Sun_Remove 10K ohm on SIO_SLP_S5# to +3.3V_ALW.
(Remove R485)



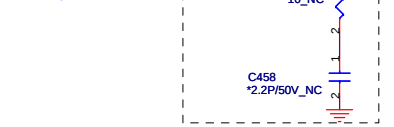
0314-Sun_Add pull up RES on LID_SW# to +3.3V_ALW



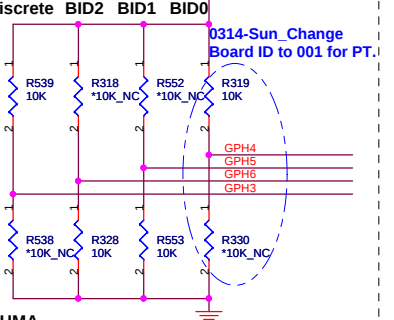
0314-Sun_Reserve 10K pull-up on SIO_SLP_S3# and SIO_SLP_S5#.



0314-Sun_Remove T75 and connect GPB0 to ESATA_DETECT#.



Board ID Straps

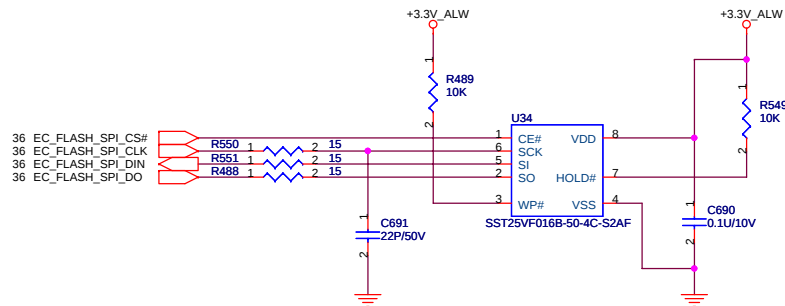


UMA

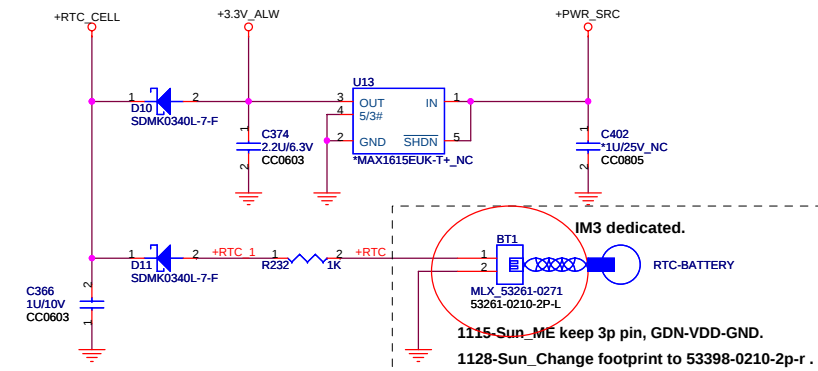
BID2	BID1	BID0	XPS (UMA)	XPS (D1S)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	QT (A00)	QT (A00)
0	0	0	(A01)	(A01)
0	0	1		

VGA_IDENTIFY : USB_SIDE_EN#
1 = Discrete Gfx / 0 = UMA.

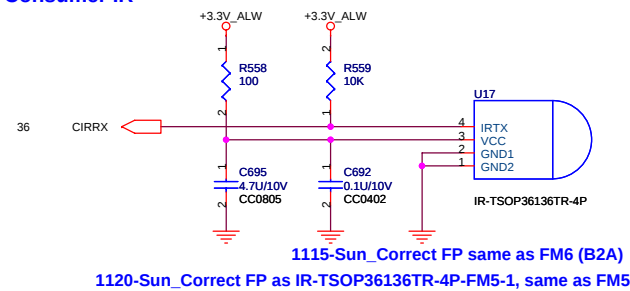
16Mbit (2M Byte), SPI



RTC BATTERY



Consumer IR



Title **FLASH & RTC**

Size	Document Number IM3 (XPS-Jolie)
------	------------------------------------

Date: Monday, March 24, 2008

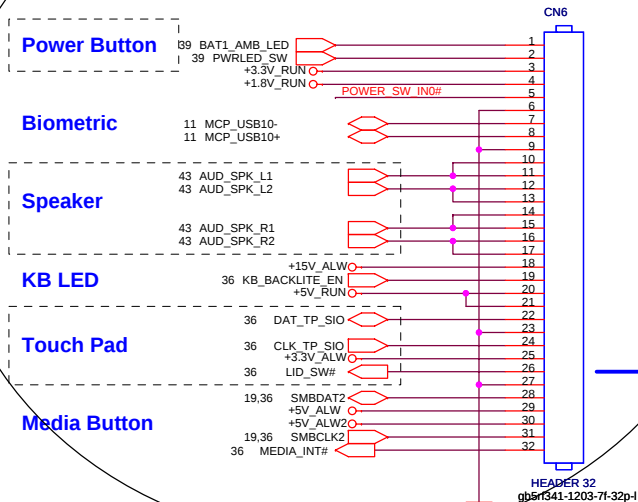
Sheet 37 of 59

Rev
1A

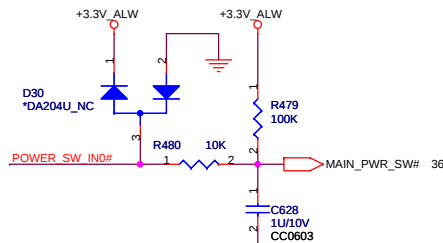
0306-Sun_Change CN6 to 34pin "gb5rf341-1203-7f-34p-I" 0314-Sun_Change CN6 to 32pin "gb5rf341-1203-7f-32p-I"

BREATH_PWRLED_BOT:

Solid = System On, Normal Activity; "Breathing" = System in Standby; Off = System Off (or in Hibernete)



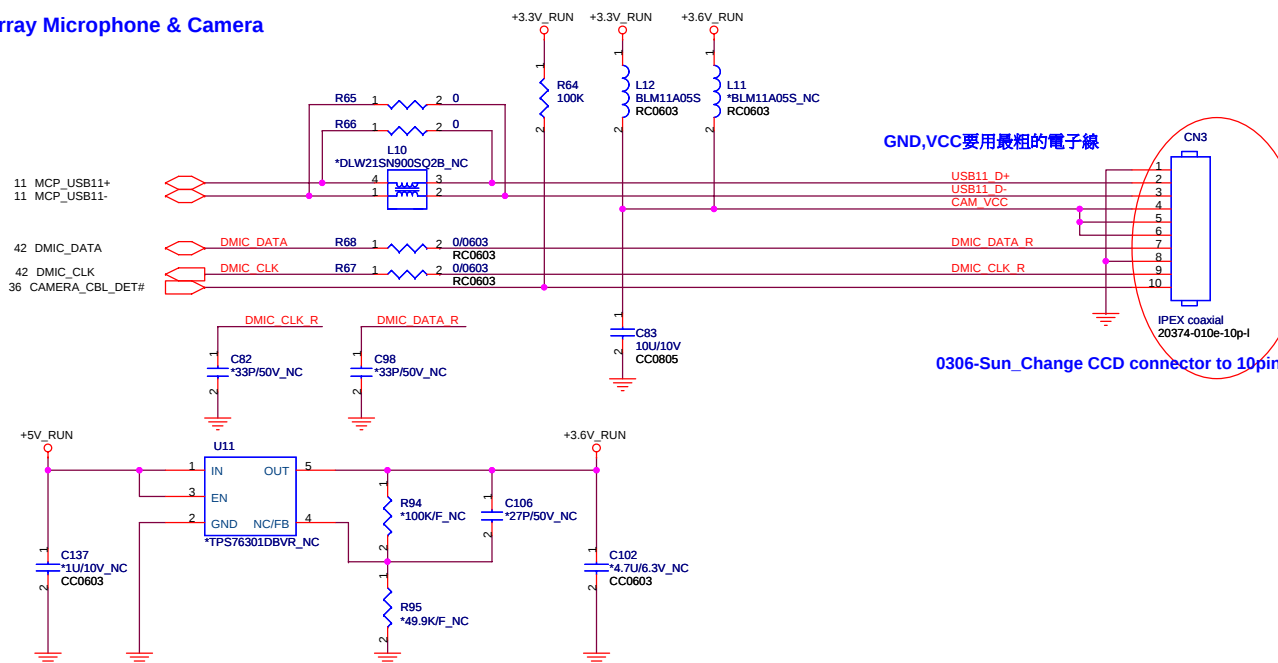
Power Button



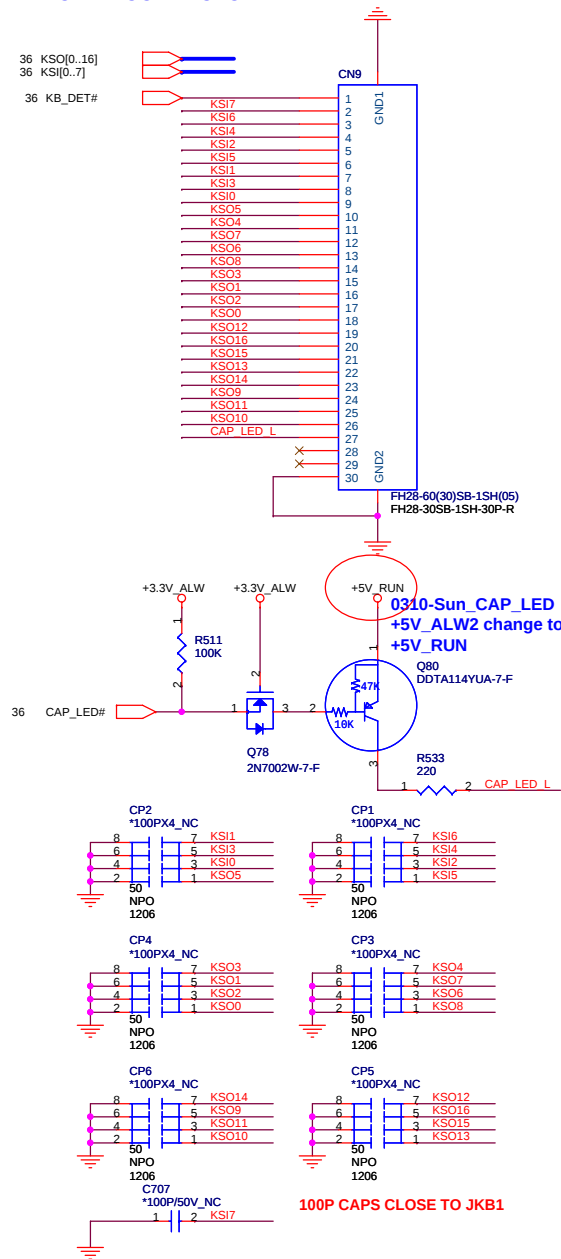
0311-Touch Pad:

1. Connect +3.3V_ALW to TP connector on D/B.
2. Inform TP vendor to change design.

Array Microphone & Camera

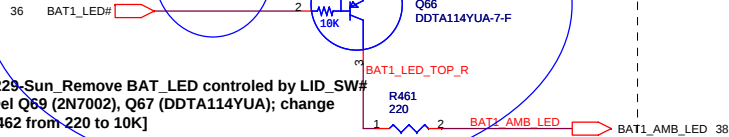


KEYBOARD CONNECTOR



Battery status

0313-Sun_Change battery LED to Amber (3.3V/drive)
(Remove Q68, R462, R460)

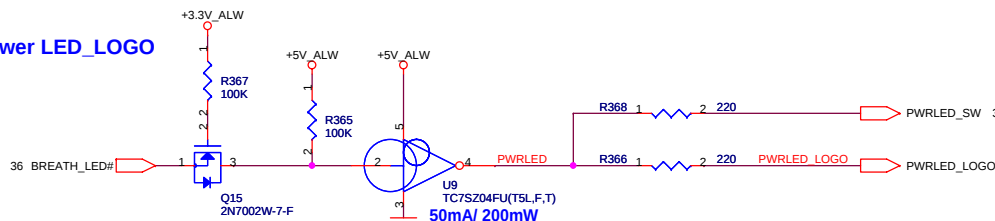


0229-Sun_Remove BAT_LED controlled by LID_SW#
[Del Q69 (2N7002), Q67 (DDTA114YUA); change R462 from 220 to 10K]

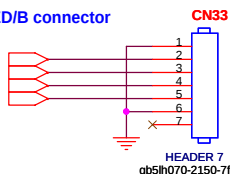
0229-Sun_Del BAT_LED2
[Del R295,Q48,Q43 (2N7002) and Q46,Q47 (DDTA114YUA)]

0229-Sun_Change PWRLED_SW control same as PWRLED_LOGO
[Del U10 (TC7SZ04F), Q16 (2N7002)]

Power LED_LOGO

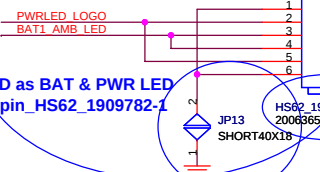


0306-Sun_Add status LED/B connector



0229-Sun_Remove LED control by LID_SW#
(Del R478,R477,Q75)

Logo LED/B connector

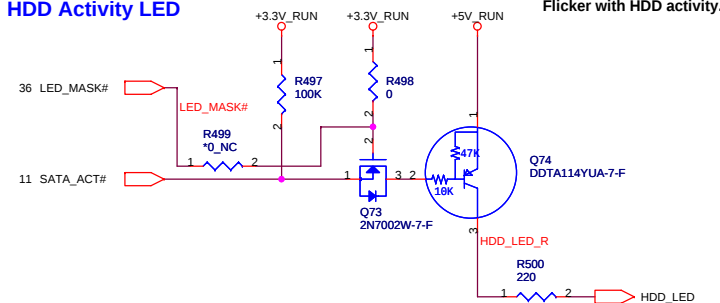


0306-Sun_Change Logo LED as BAT & PWR LED
and change connector to 6pin_HS62_1909782-1

0319-Sun_Update Footprint of
Logo LED/B connector

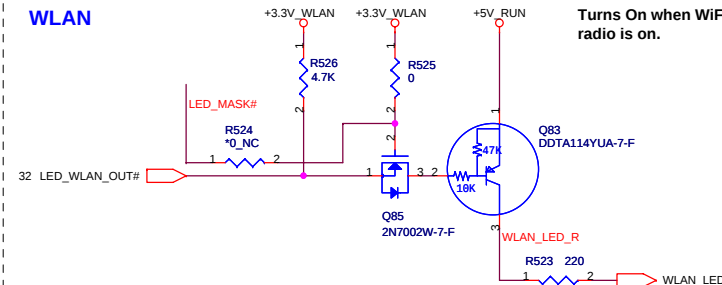
0314-Sun_Add short pad on GND of
Logo LED/B connector for EMI request.

HDD Activity LED



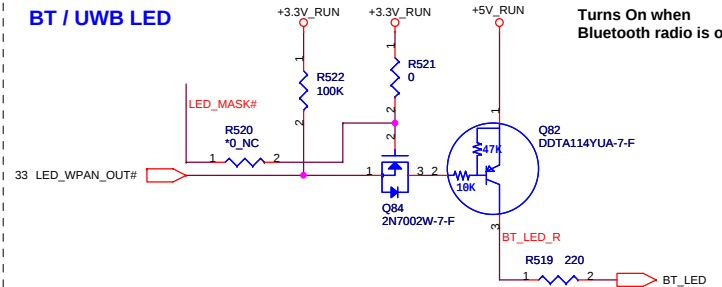
Flicker with HDD activity.

WLAN



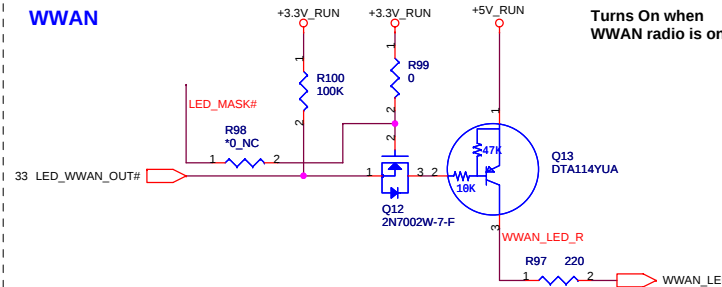
Turns On when WiFi
radio is on.

BT / UWB LED



Turns On when
Bluetooth radio is on.

WWAN

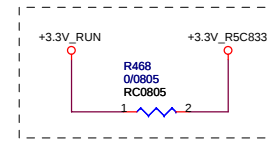
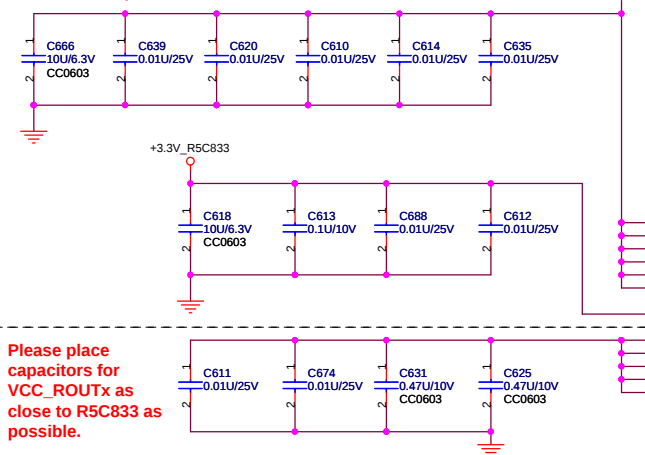


Turns On when
WWAN radio is on.

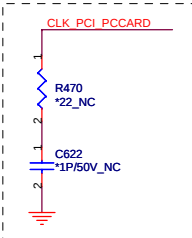
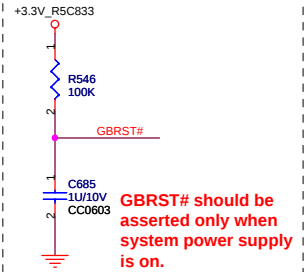
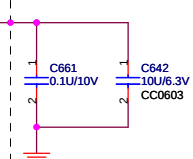


Title LED		
Size	Document Number IM3 (XPS-Jolie)	Rev 1A
Date:	Thursday, March 20, 2008	Sheet 39 of 59

Place the power caps close to the relation pins.



Place the power caps close to the relation pins.



10,57 PCI_PAR
10,57 PCI_C_BE3#
10,57 PCI_C_BE2#
10,57 PCI_C_BE1#
10,57 PCI_C_BE0#

10 PCI_REQ0#
10 PCI_GNT0#
10,57 PCI_FRAME#
10,57 PCI_IRDY#
10,57 PCI_TRDY#
10,57 PCI_DEVSEL#
10,57 PCI_STOP#
10,57 PCI_PERR#
10,57 PCI_SERR#

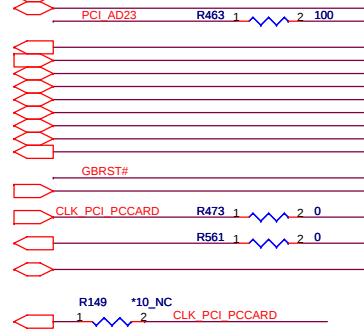
10,57 PCI_RST#

10 CLK_PCI_PCCARD

10,57 PCI_PME#

10,36,57 CLKRUN#

57 CLK_PCI_DEBUG

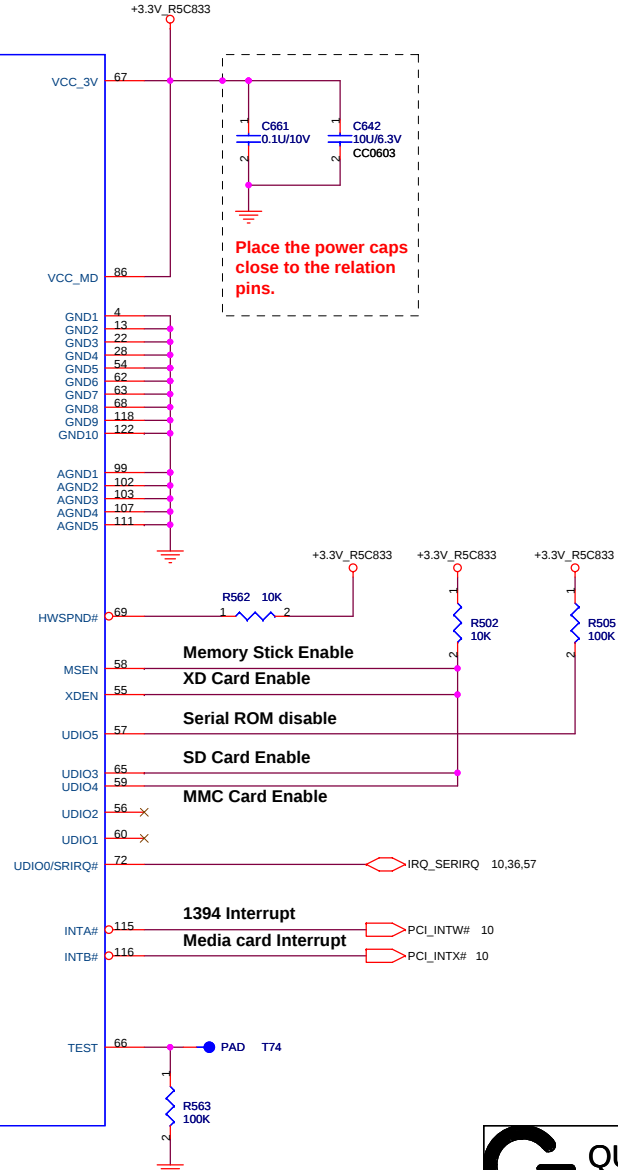


PCI AD31
PCI AD30
PCI AD29
PCI AD28
PCI AD27
PCI AD26
PCI AD25
PCI AD24
PCI AD23
PCI AD22
PCI AD21
PCI AD20
PCI AD19
PCI AD18
PCI AD17
PCI AD16
PCI AD15
PCI AD14
PCI AD13
PCI AD12
PCI AD11
PCI AD10
PCI AD9
PCI AD8
PCI AD7
PCI AD6
PCI AD5
PCI AD4
PCI AD3
PCI AD2
PCI AD1
PCI AD0

125 AD31
126 AD30
127 AD29
1 AD28
2 AD27
3 AD26
5 AD25
6 AD24
9 AD23
11 AD22
12 AD21
14 AD20
15 AD19
17 AD18
18 AD17
19 AD16
36 AD15
37 AD14
38 AD13
39 AD12
40 AD11
42 AD10
43 AD9
44 AD8
46 AD7
47 AD6
48 AD5
49 AD4
50 AD3
51 AD2
52 AD1
53 AD0

7 PAR
21 C/BE3#
35 C/BE2#
45 C/BE1#
8 C/BE0#
124 REQ#
123 GNT#
23 FRAME#
24 IRDY#
26 TRDY#
29 DEVSEL#
30 STOP#
31 PERR#
71 SERR#
119 GBRST#
121 PCIRST#
70 PCICLK
117 PME#
117 CLKRUN#

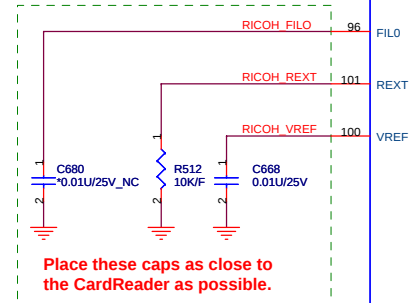
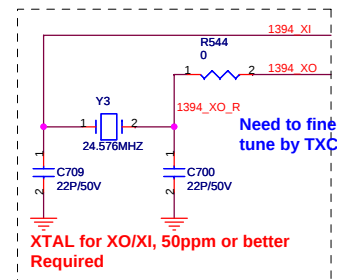
PCI / OTHER



Memory Stick Enable
XD Card Enable
Serial ROM disable
SD Card Enable
MMC Card Enable

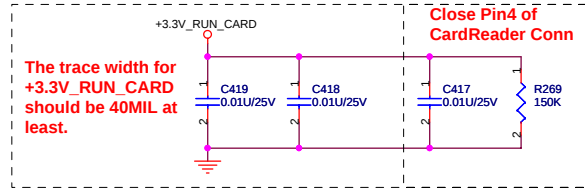
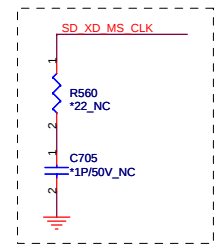
1394 Interrupt
Media card Interrupt





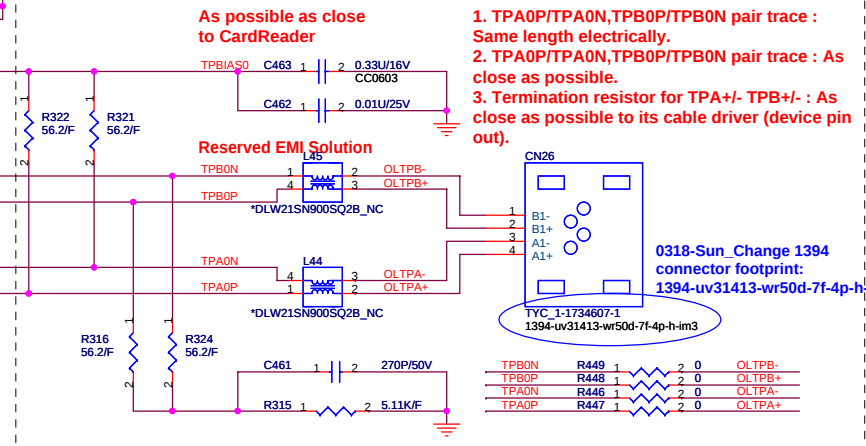
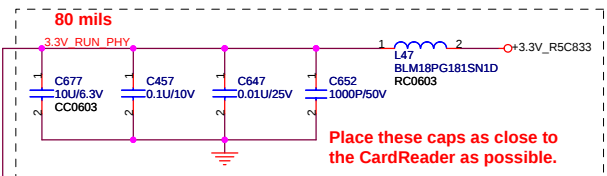
Card Reader interface signal mapping

PIN	SD	MMC	MS	XD
MDIO00	SD_CD#	MMC_CD#	MS_CD#	XD_CD#
MDIO01				XD_CD1#
MDIO02	SD_WP#	MMC_PWR	MS_PWR	XD_R/B#
MDIO03	SD_PWR#	MMC_PWR	MS_PWR	XD_PWR
MDIO04	SD_PWR1	MMC_PWR	MS_PWR	XD_PWR1
MDIO05	SD_LED#	MMC_LED#	MS_LED#	XD_LED#
MDIO06	MYEST			
MDIO07	SD_CMD	MMC_CMD	MS_BS	XD_WE#
MDIO08	SD_CLK	MMC_CLK	MS_CLK	XD_RE#
MDIO09	SD_D0	MMC_D0	MS_D0	XD_D0
MDIO10	SD_D1	MMC_D1	MS_D1	XD_D1
MDIO11	SD_D2	MMC_D2	MS_D2	XD_D2
MDIO12	SD_D3	MMC_D3	MS_D3	XD_D3
MDIO13				XD_D4
MDIO14				XD_D5
MDIO15				XD_D6
MDIO16				XD_D7
MDIO17				XD_CLE
MDIO18				XD_ALE
MDIO19				



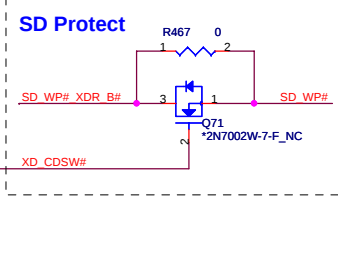
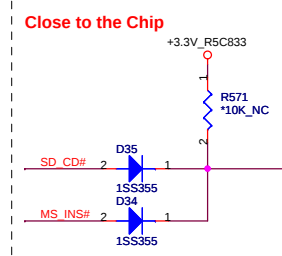
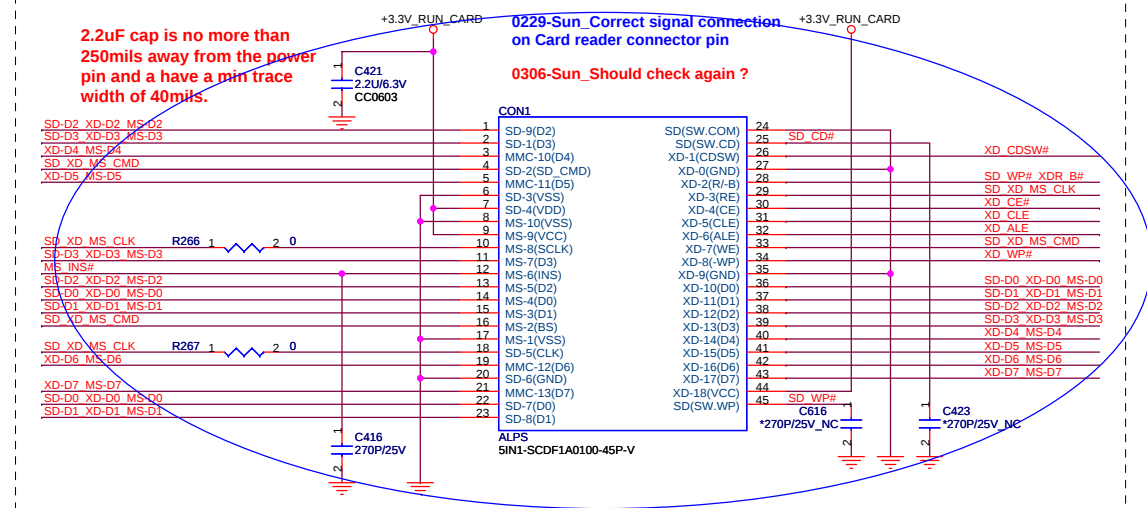
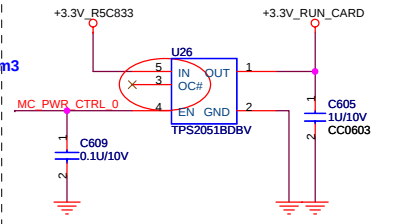
IEEE1394/SD

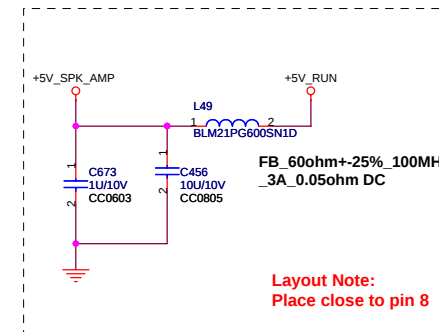
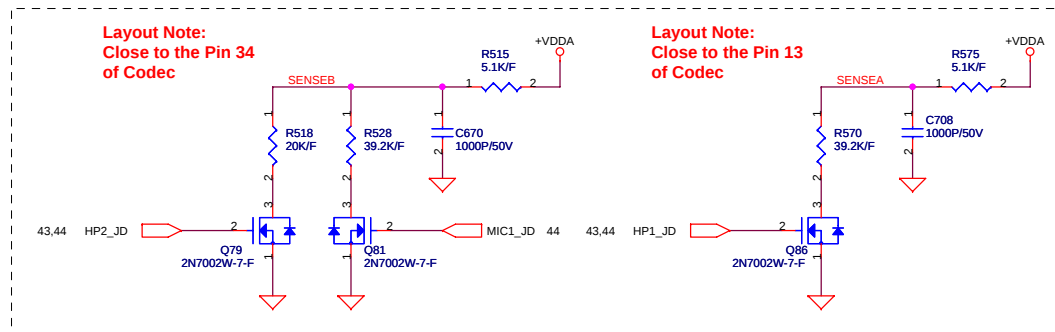
- MDIO17 XD-D7 MS-D7
- MDIO16 XD-D6 MS-D6
- MDIO15 XD-D5 MS-D5
- MDIO14 XD-D4 MS-D4
- MDIO13 XD-D3 XD-D3 MS-D3
- MDIO12 XD-D2 XD-D2 MS-D2
- MDIO11 XD-D1 XD-D1 MS-D1
- MDIO10 XD-D0 XD-D0 MS-D0
- MDIO05 XD_WP#
- MDIO08 SD_XD_MS_CMD
- MDIO19 XD_ALE
- MDIO18 XD_CLE
- MDIO02 XD_CE#
- MDIO03 SD_WP# XDR_B#
- MDIO00 SD_CD#
- MDIO01 MS_INS#
- MDIO09 SD_XD_MS_CLK
- MDIO04 MC_PWR_CTRL_0
- MDIO06 T44 PAD
- MDIO07



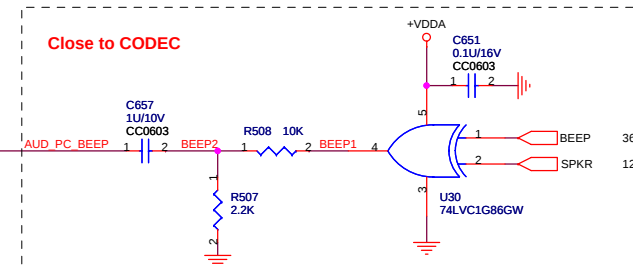
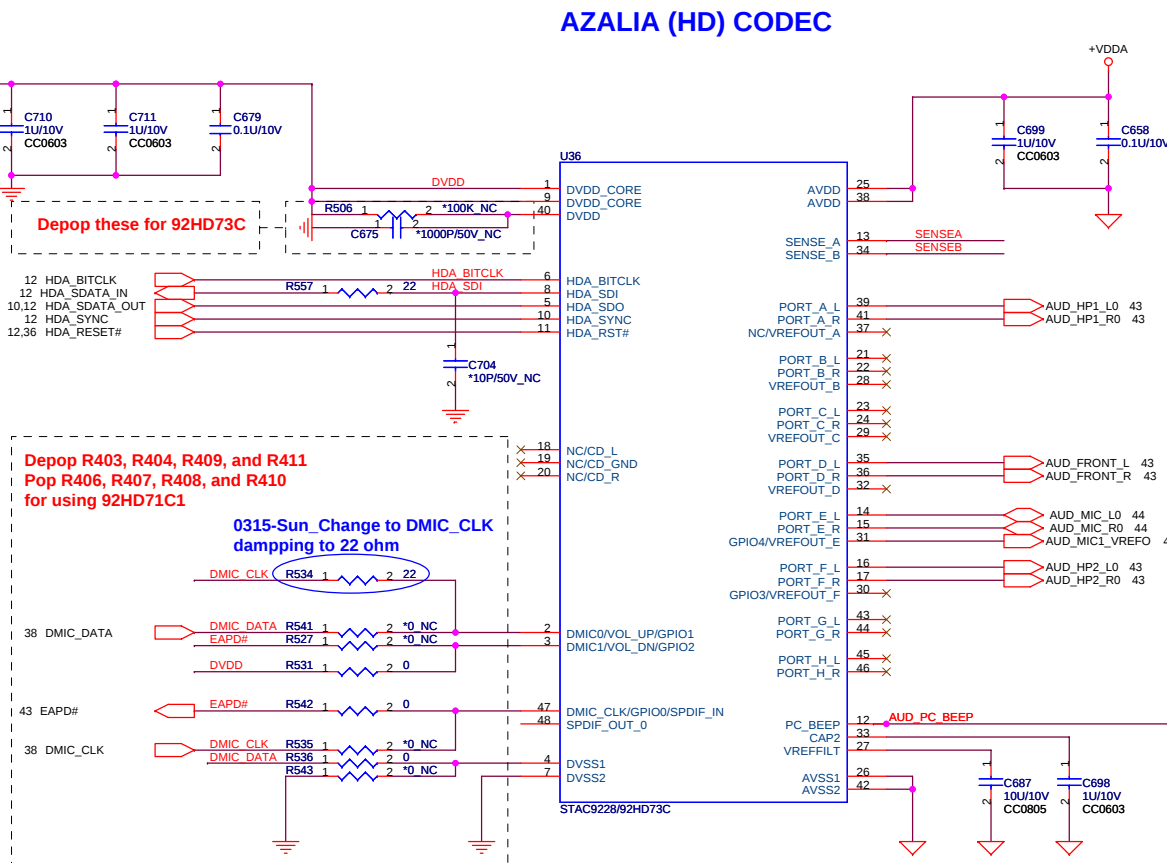
Layout Note:

- 1). The distance between Media Card Power Switch and Media Socket should be less than 2-inches.
- 2). The trace width for +3.3V_RUN_CARD should be 40MIL at least.
- 3). The GND trace for Media Card Socket should be 40MIL at least.





AZALIA (HD) CODEC



Title			Azella CODEC
Size	Document Number	Rev	
	IM3 (XPS-Jolie)	1A	
Date:	Friday, March 21, 2008	Sheet	42 of 59

INTERNAL SPEAKER AMP

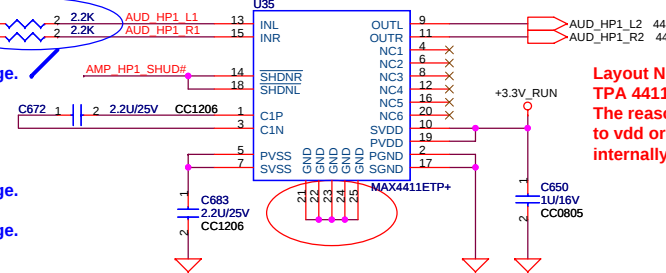
0315-Sun_Improve Dynamic Range.
0320-StegChange AC coupling to 10U/10V



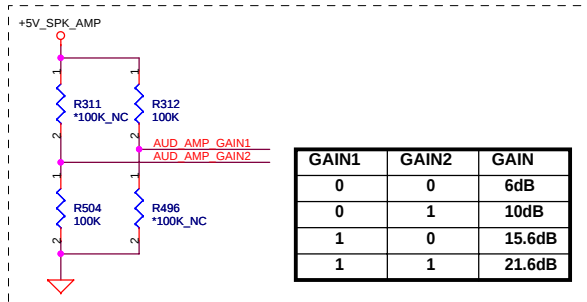
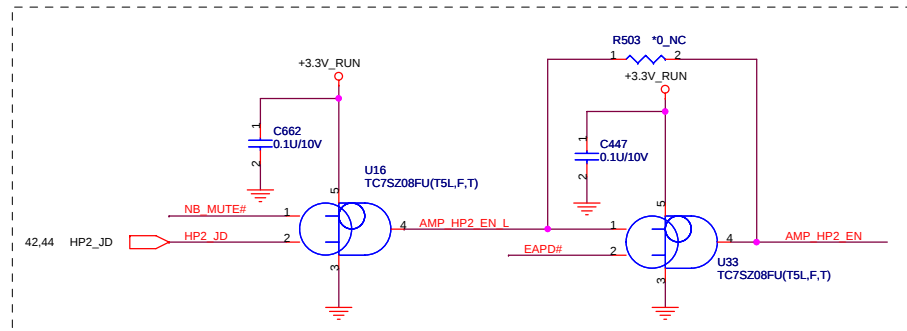
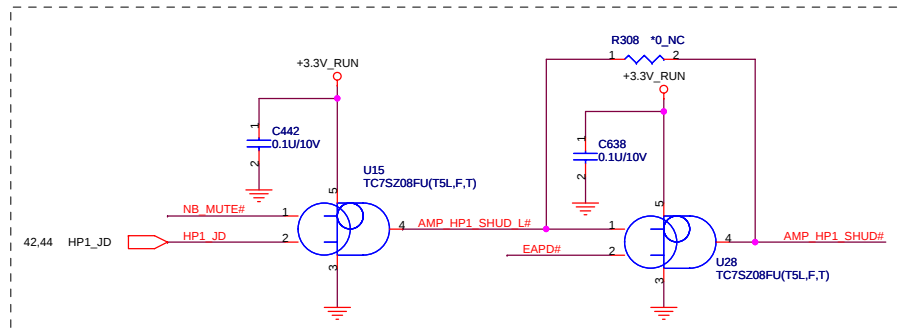
0310-Sun_Improve Dynamic Range.
Add R597,R598 w/2.2K



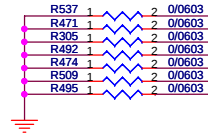
0310-Sun_Improve Dynamic Range.
Pop C452,C455 w/220P
0315-Sun_Improve Dynamic Range.
Change C452,C455 to 330P



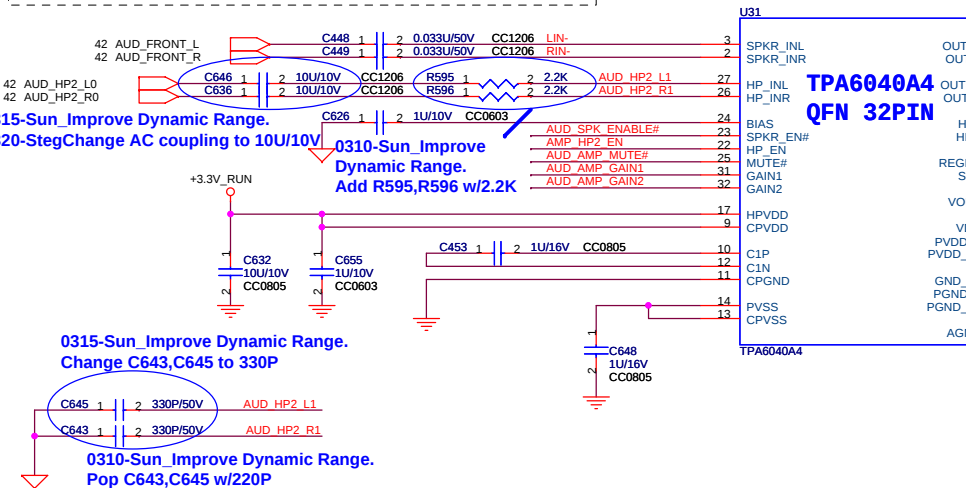
Layout Note:
TPA 4411 : cannot connect EP to GND.
The reason that we can't solder the pad to vdd or ground is because it is internally connected to VSS.



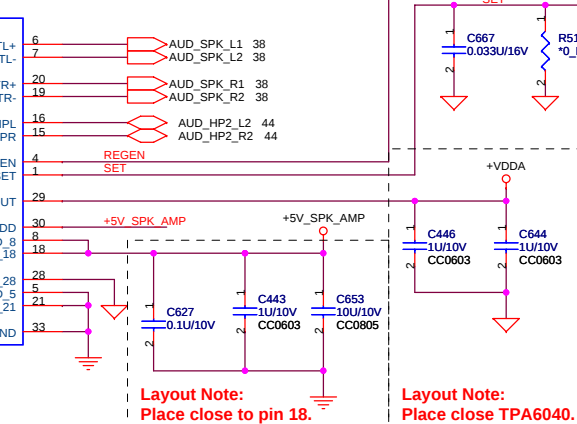
EMI Reserved



Layout Note:
MAX9789A/TPA6040A : need to connect EP (exposed paddle) to GND.
TPA 4411 : cannot connect EP to GND.
MAX 4411: can connect EP to GND.

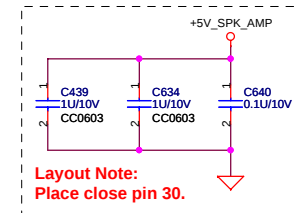


TPA6040A4
QFN 32PIN



Layout Note:
Place close to pin 18.

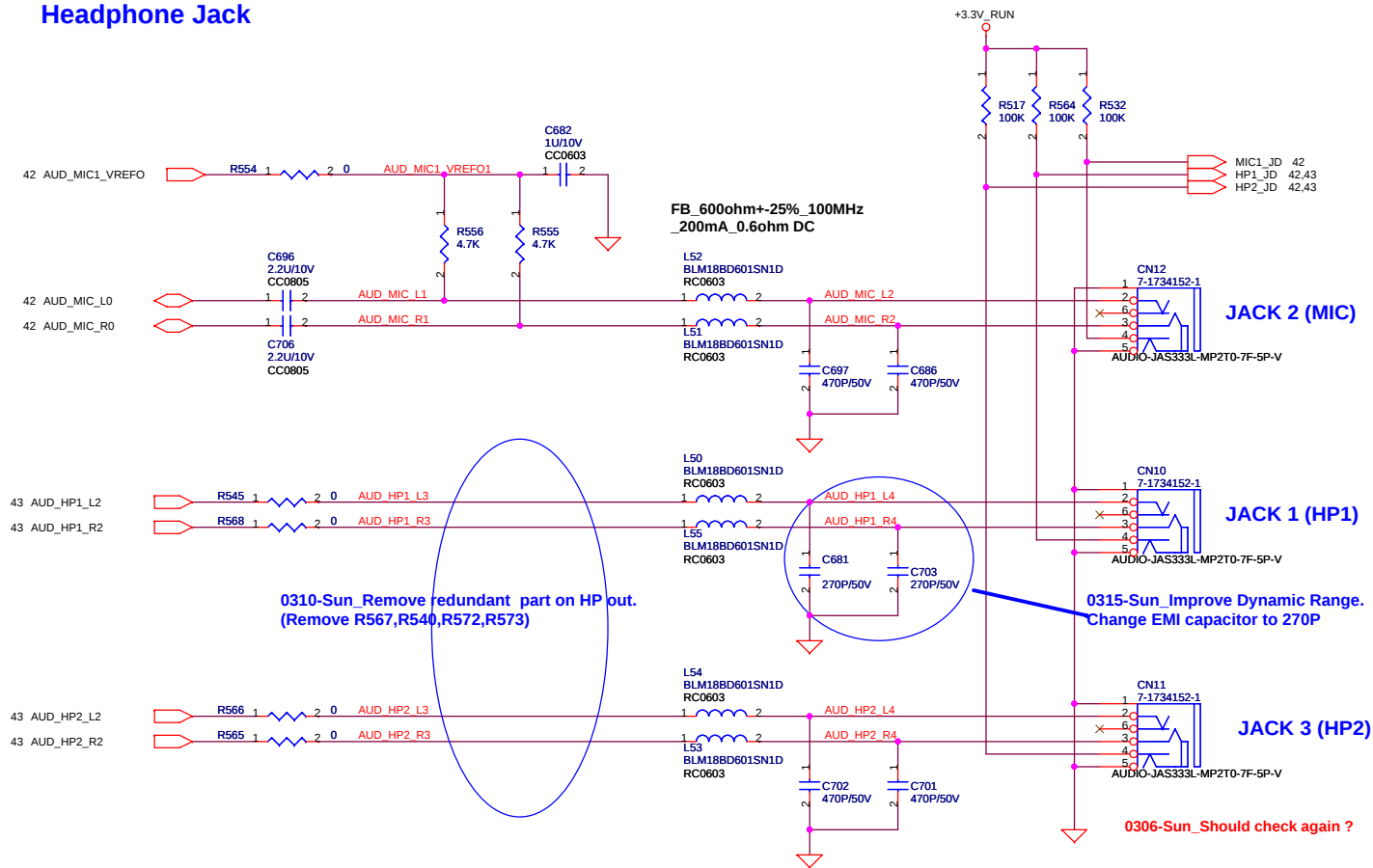
Layout Note:
Place close TPA6040.



Layout Note:
Place close pin 30.

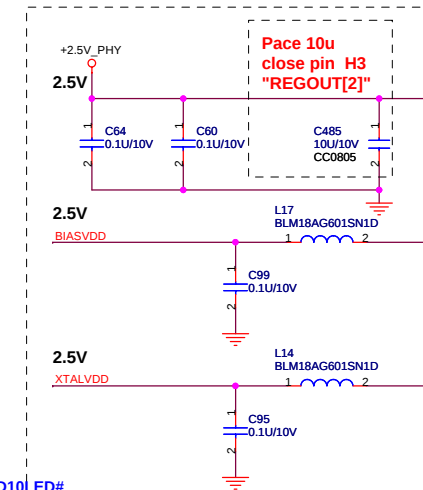
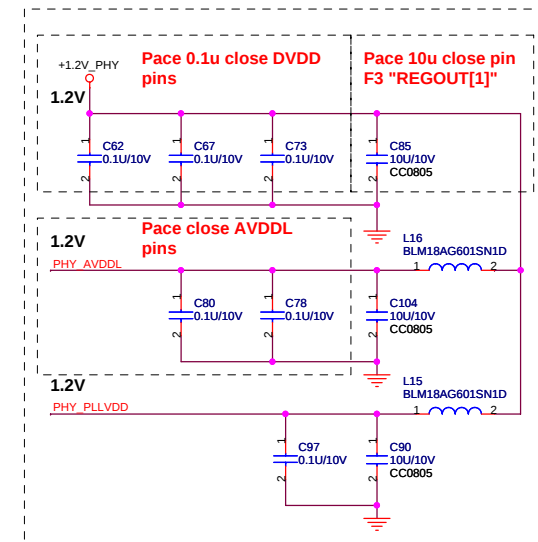
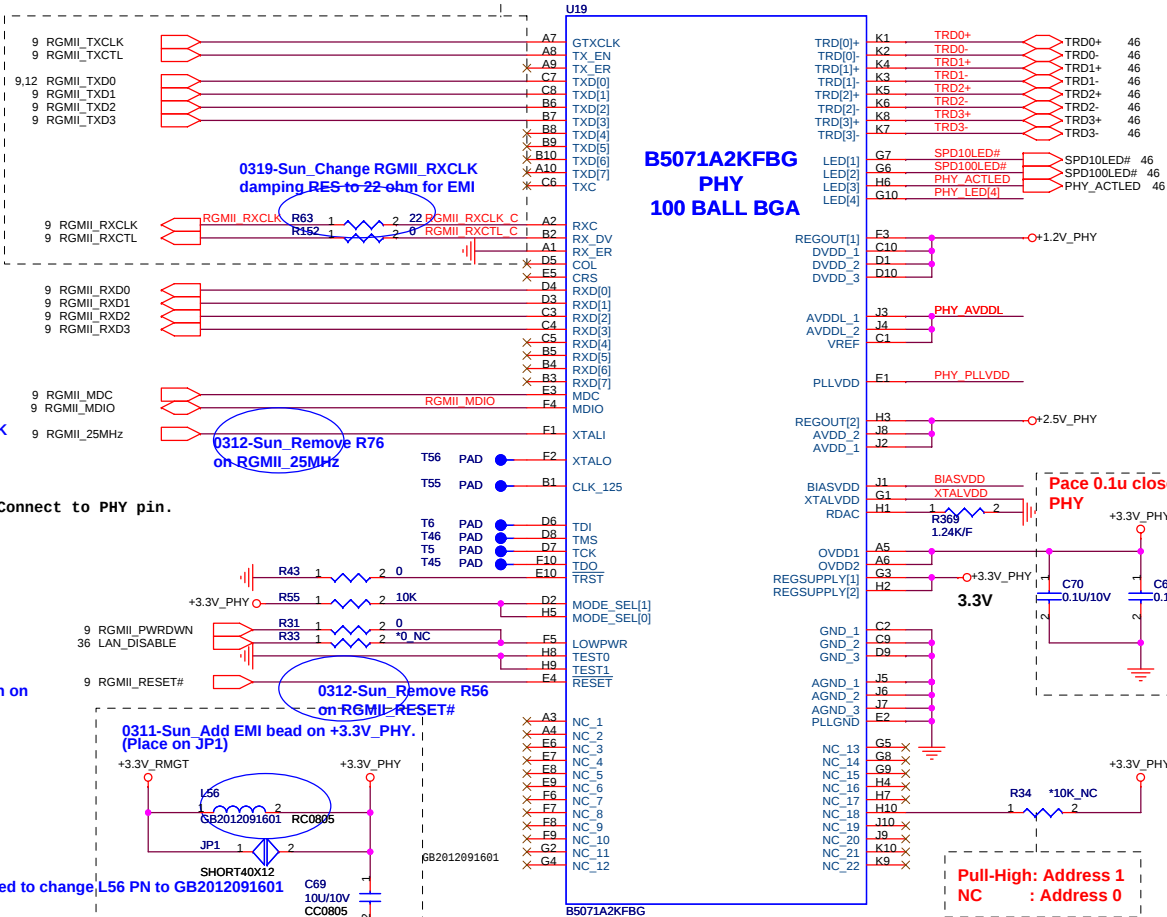
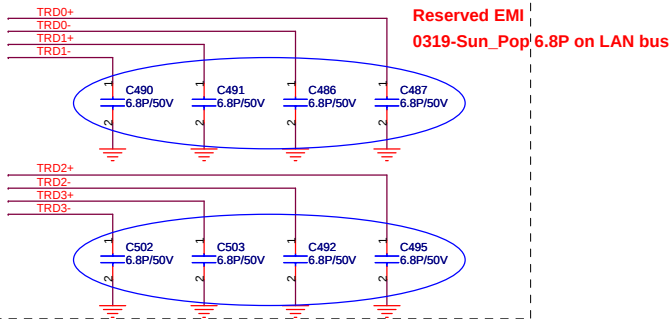


Headphone Jack



Layout Note:

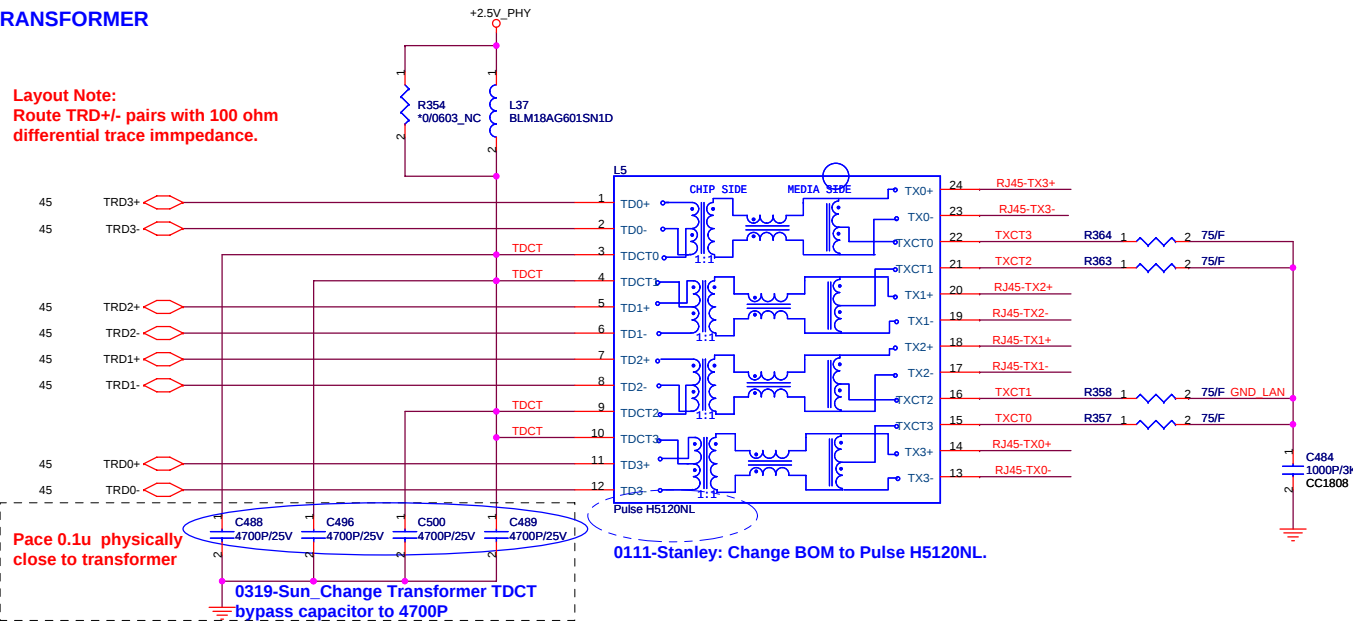
1. Use 50 ohm impedance for all trace.
2. Trace length matched to a tolerance of 9.8mm in order to keep the skew between signals less than 0.07ns.
3. The receive and transmit signals kept away from each other and other analog and clock signals to reduce crosstalk.



Title			LAN Broadcom PHY B5071
Size	Document Number	Rev	
	IM3 (XPS-Jolie)	1A	
Date:	Thursday, March 20, 2008	Sheet	45 of 59

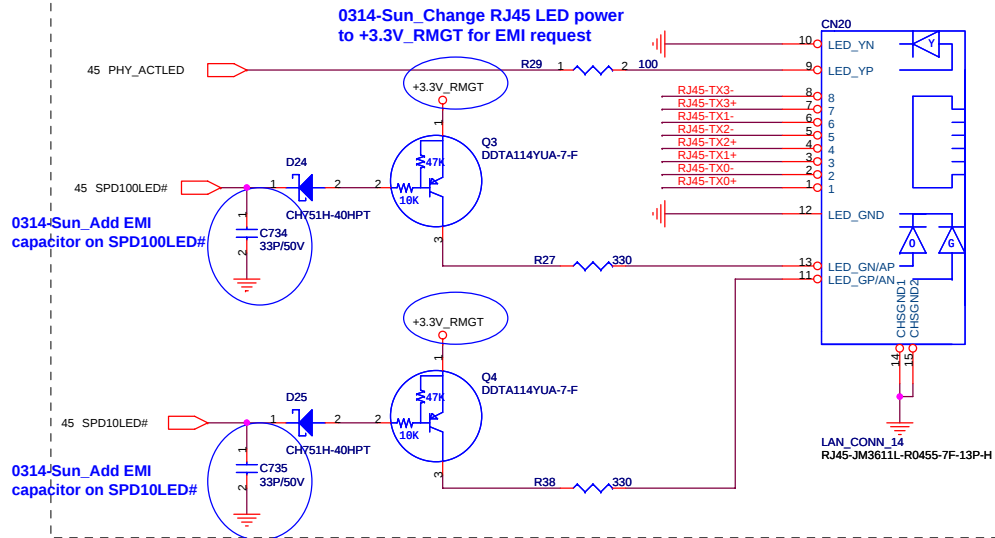
TRANSFORMER

Layout Note:
Route TRD+/- pairs with 100 ohm differential trace impedance.

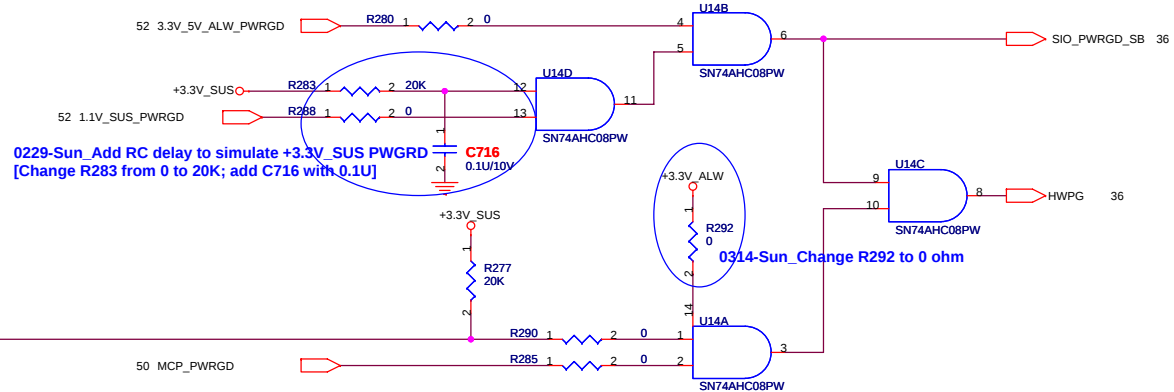
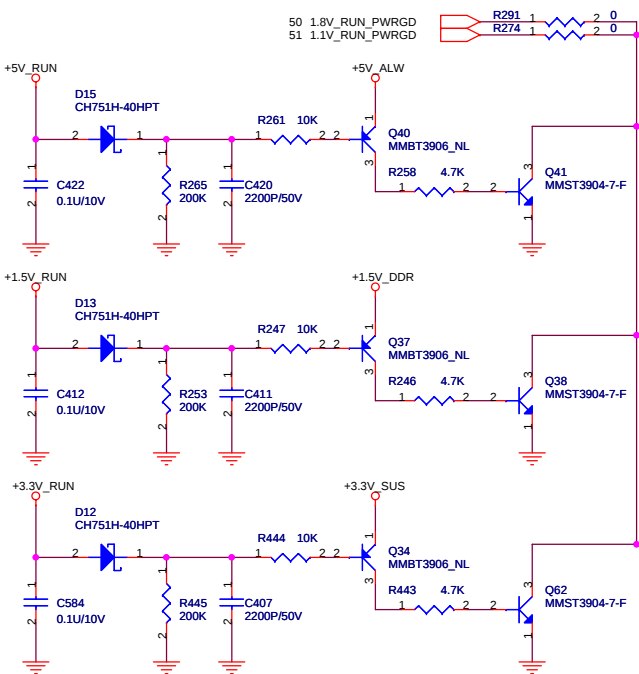
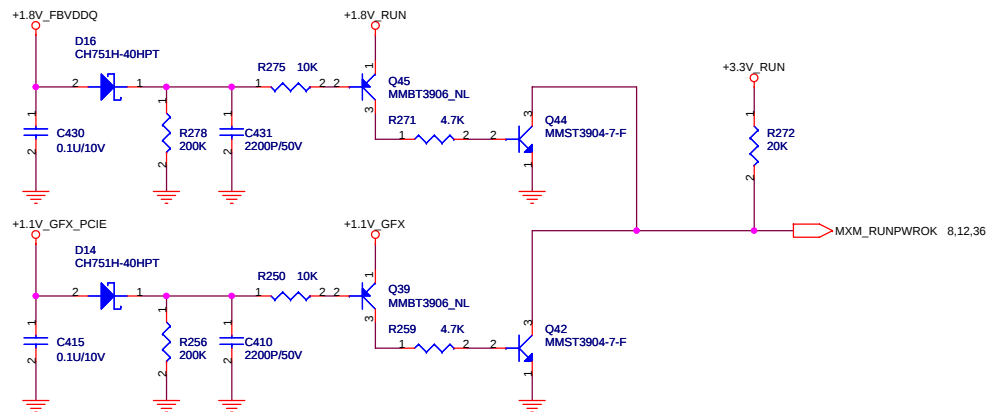


RJ-45 Connector

0314-Sun_Change RJ45 LED power to +3.3V_RMGT for EMI request



Title		
LAN SWITCH		
Size	Document Number	Rev
	IM3 (XPS-Jolie)	1B
Date:	Friday, March 21, 2008	Sheet 46 of 59

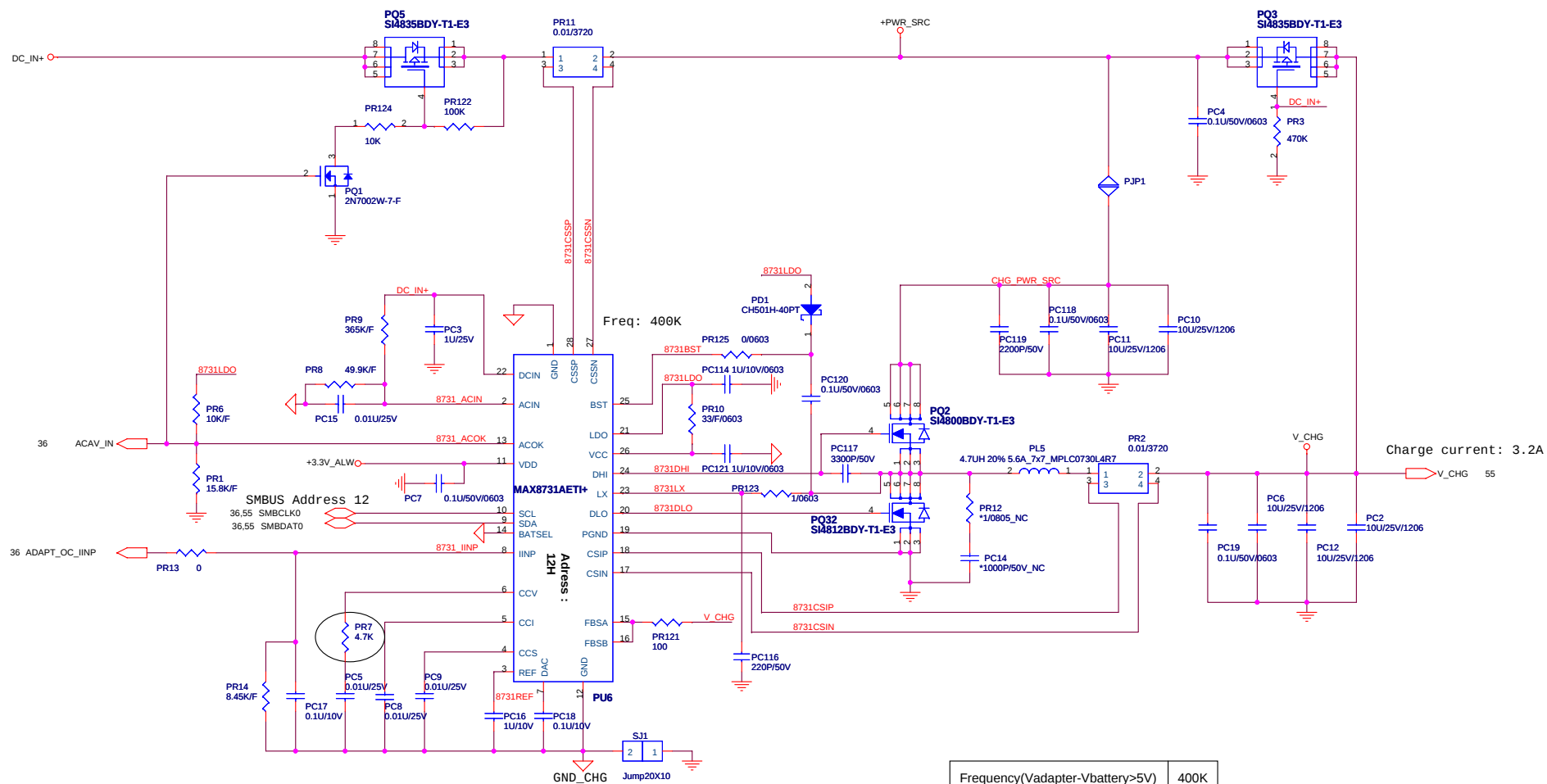


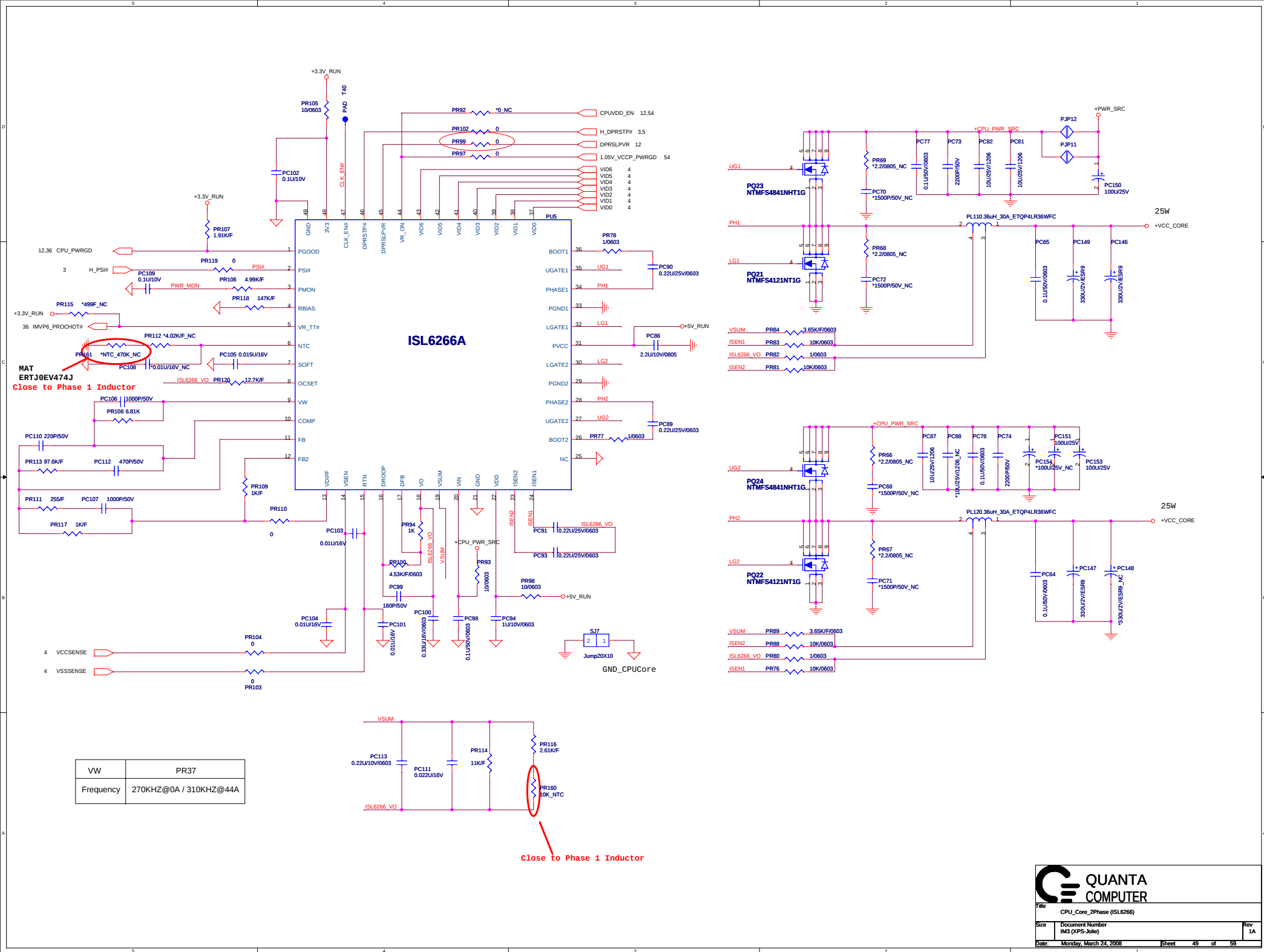
0229-Sun_Add RC delay to simulate +3.3V_SUS PWGRD
[Change R283 from 0 to 20K; add C716 with 0.1U]

0314-Sun_Change R292 to 0 ohm



Title			System Reset Circuit
Size	Document Number		Rev
	IM3 (XPS-Jolie)		1A
Date:	Friday, March 21, 2008	Sheet	47 of 59





VID2	VID1	VID0	+MCP_Core
L	L	L	+1.303V
L	L	H	+1.245V
L	H	L	+1.189V
L	H	H	+1.141V
H	L	L	+1.085V
H	L	H	+1.045V
H	H	L	+1.005V
H	H	H	+0.970V

0111-Rick: Change Votage table.

0314-Rick: Add PR202, PR203

0111-Rick: Change PR142, PR46.

0304- Change TDC , OCP.

TDC: 12.429A
OCP: 17.756A

TDC: 1.785A
OCP: 2.55A

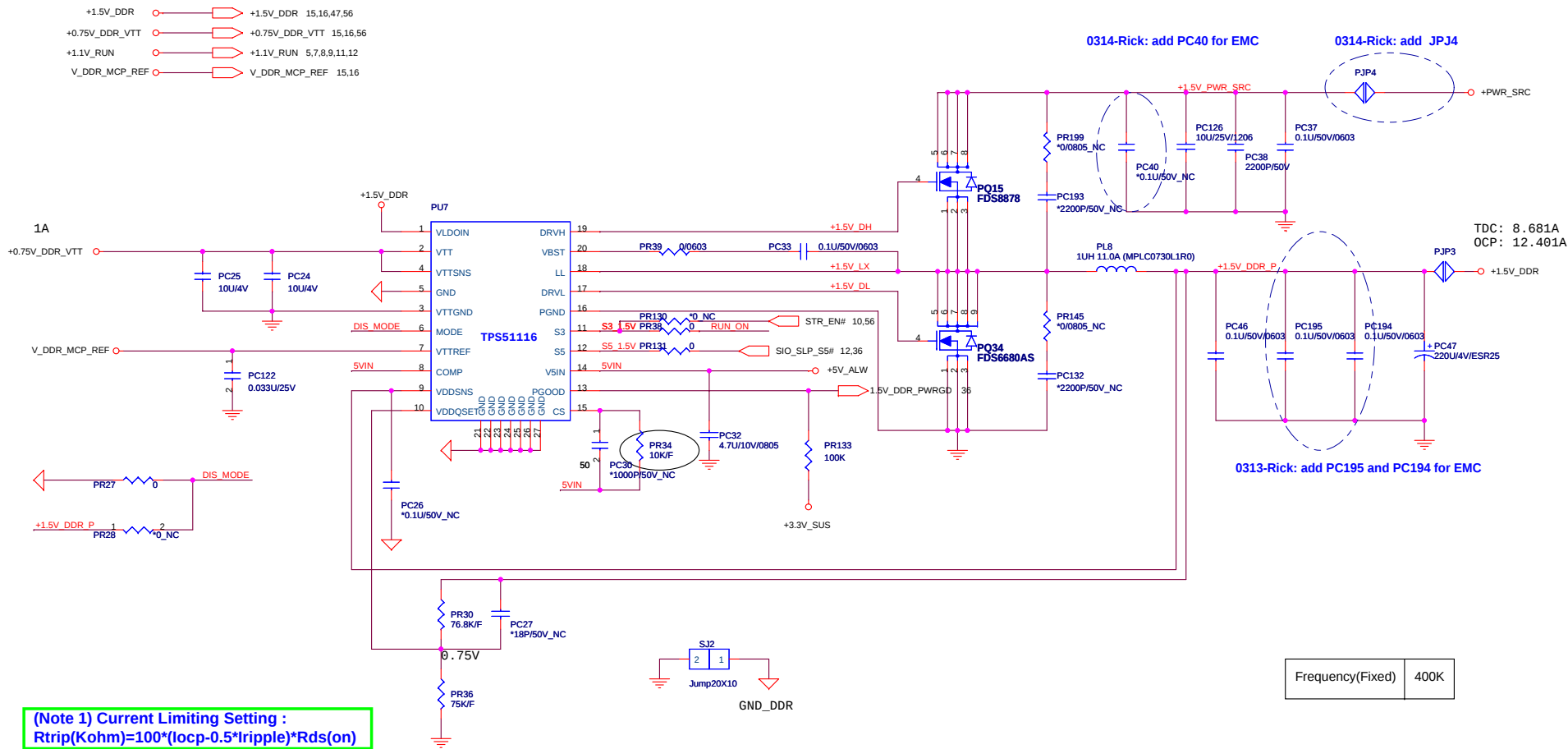
TON1	PR73 = 200K
Frequency	297K

TON2	PR75 = 200K
Frequency	297K

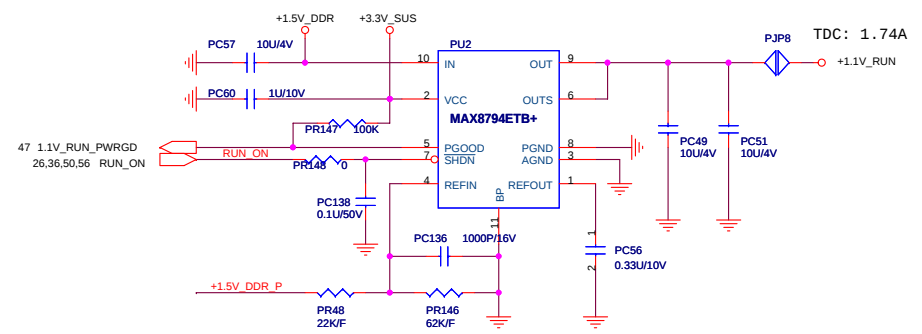


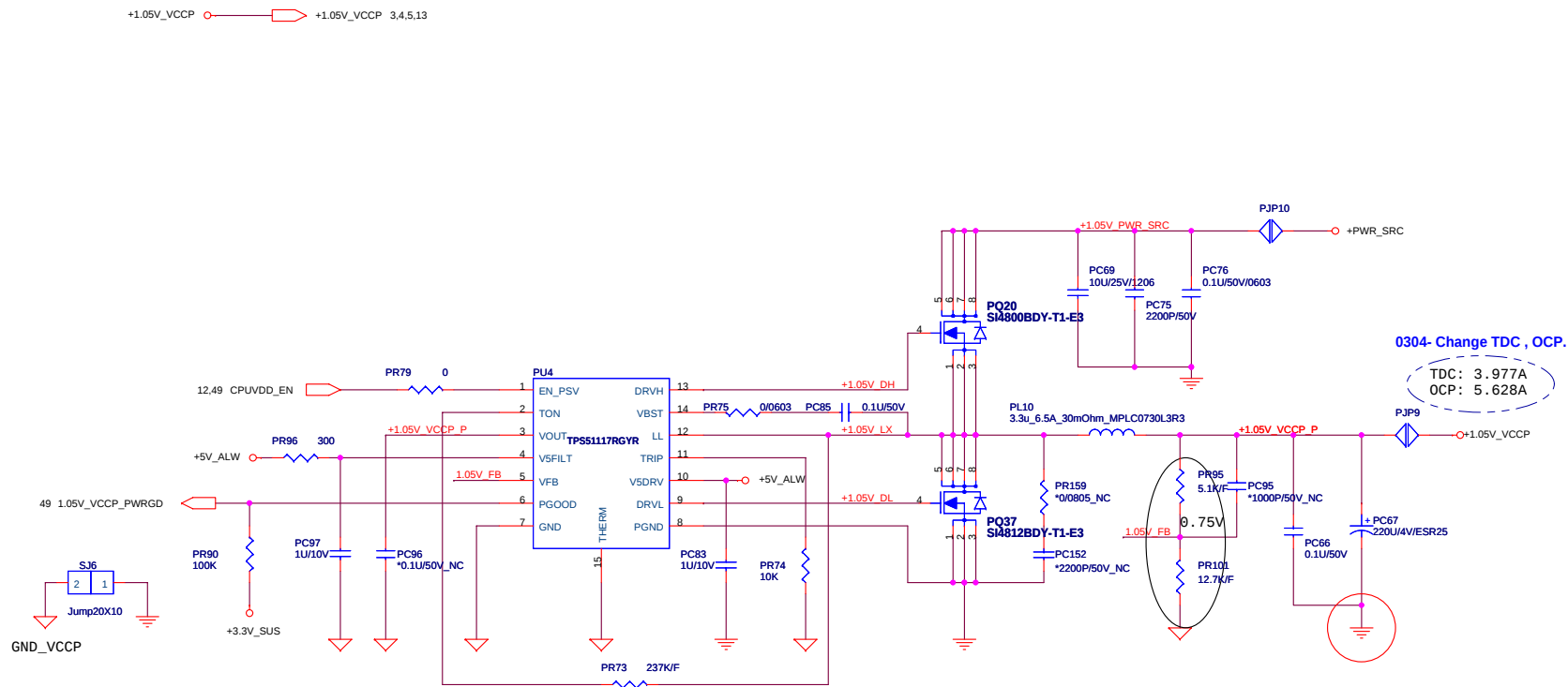
QUANTA
COMPUTER

Title			MCP1.8V (MAX17007)		
Size	Document Number		Rev		1B
IM3 (XPS-Jolie)					
Date:	Monday, March 24, 2008	Sheet	50	of	59

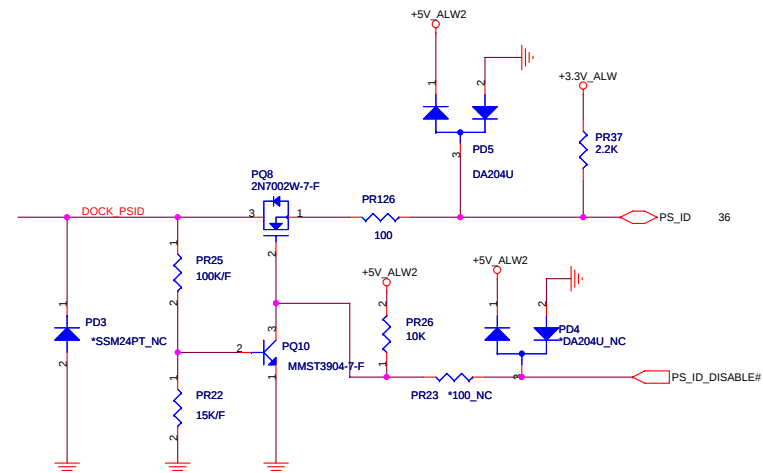
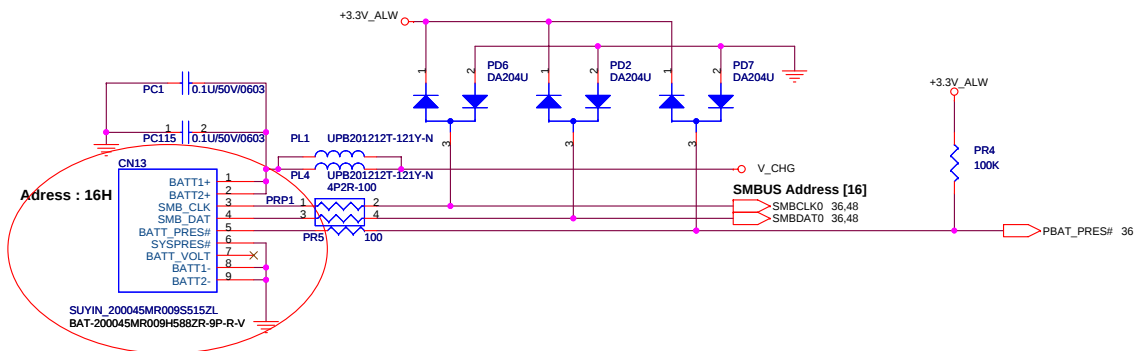


Frequency(Fixed)	400K
------------------	------

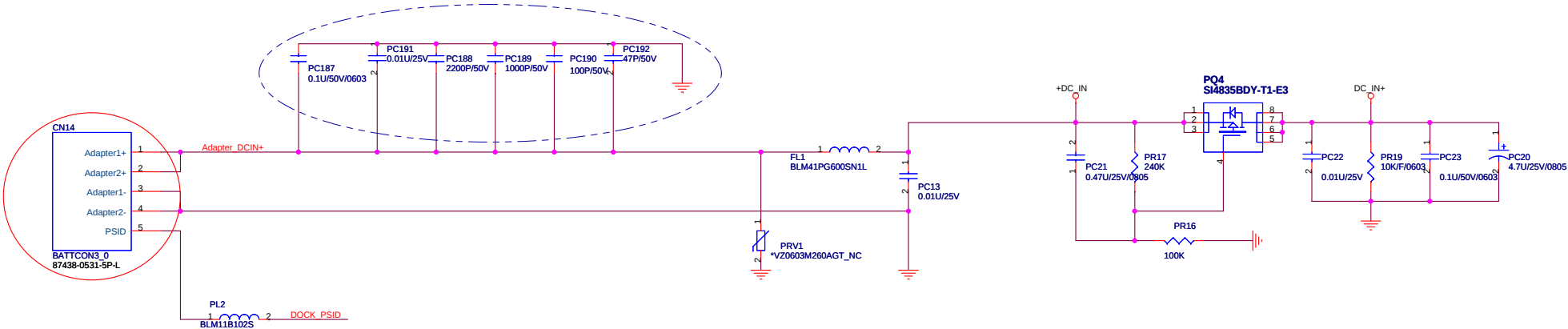




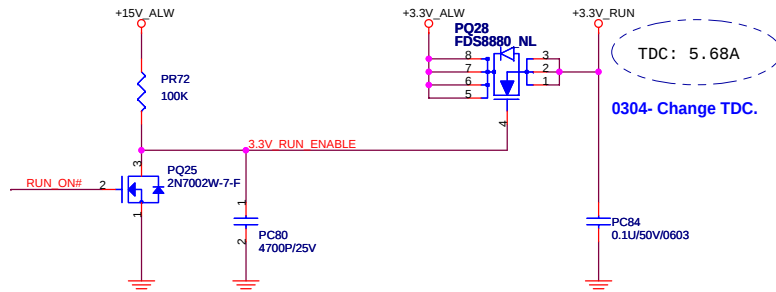
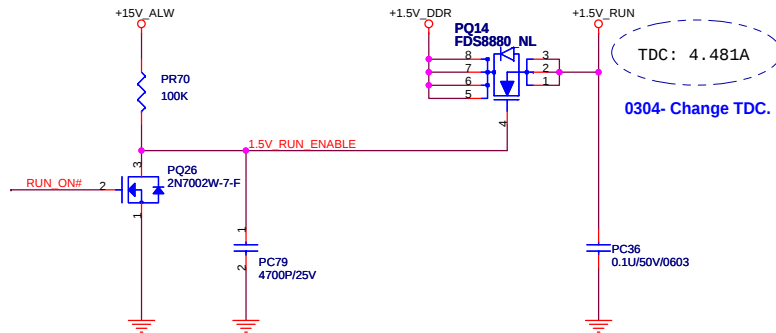
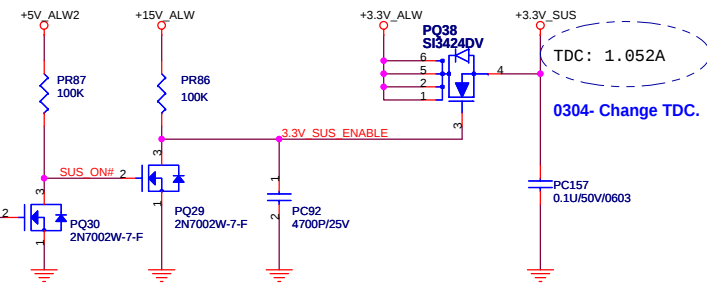
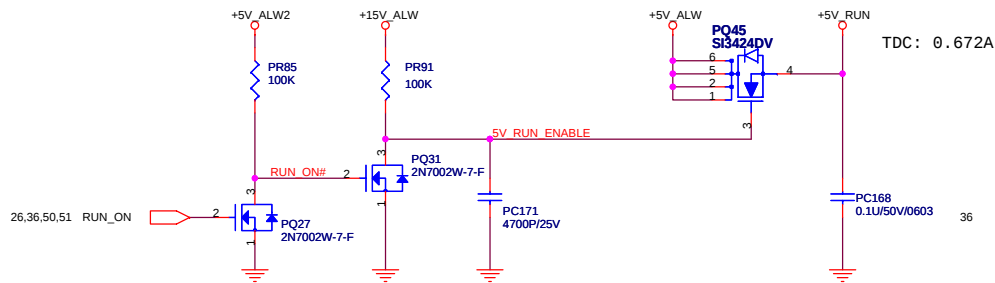
TON	PR185=237K
Frequency	300K



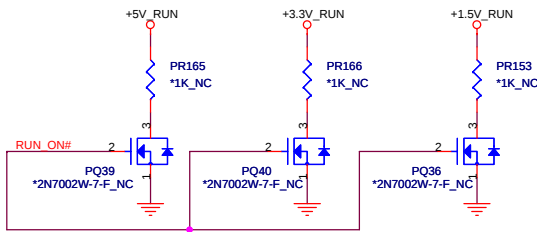
0311-Rick: Add PC187-PC192 for EMC



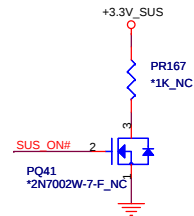
Title			DCIN,Batt
Size	Document Number	Rev	
	IM3 (XPS-Jolie)	1A	
Date:	Thursday, March 20, 2008	Sheet	55 of 59



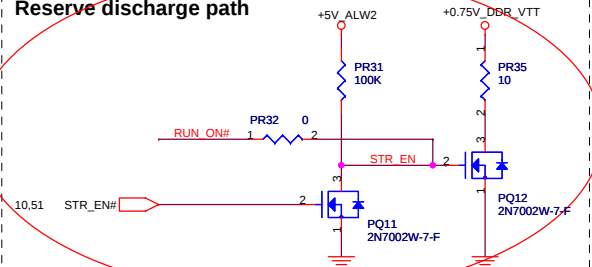
Reserve discharge path



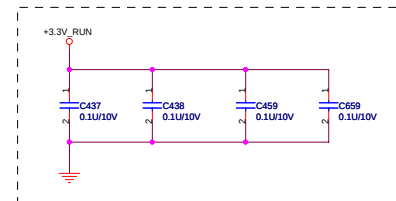
Reserve discharge path



Reserve discharge path



Title			RUN POWER SW
Size	Document Number		Rev
	IM3 (XPS-Jolie)		1A
Date:	Thursday, March 20, 2008	Sheet	56 of 59



 QUANTA COMPUTER	
File	
Debug Port (Mini PCI)	
Size	Document Number IM3 (XPS-Jolie)
Date:	Thursday, March 20, 2008
Sheet	57 of 58

