

VM8M Block Diagram Intel UMA

VER :E3B

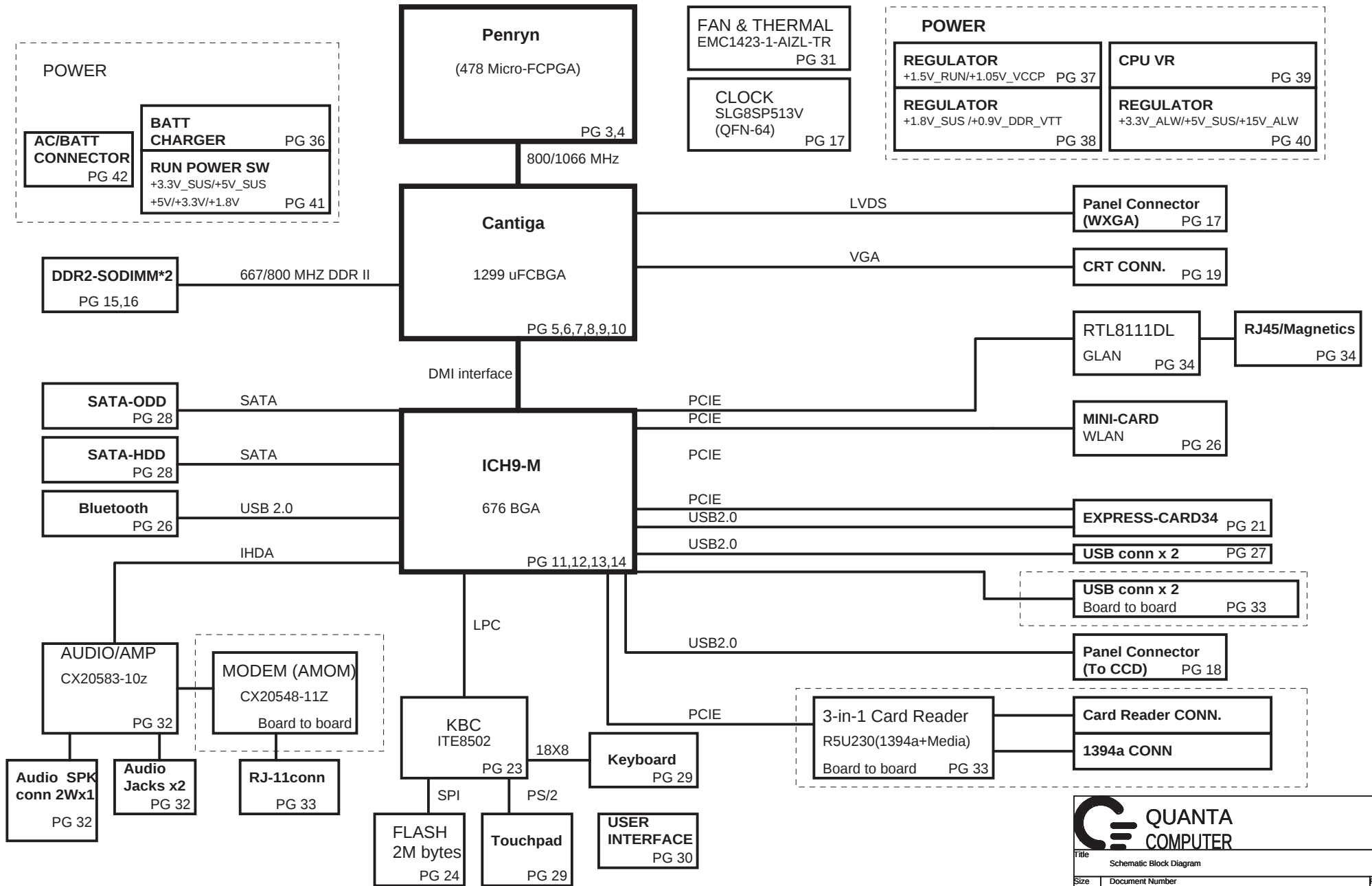
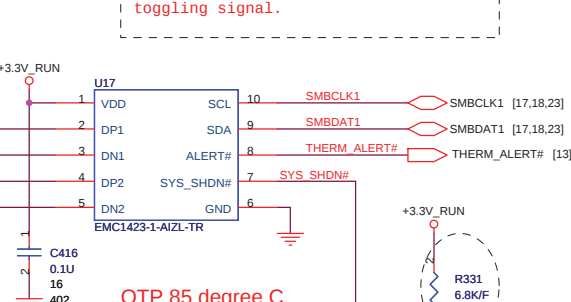
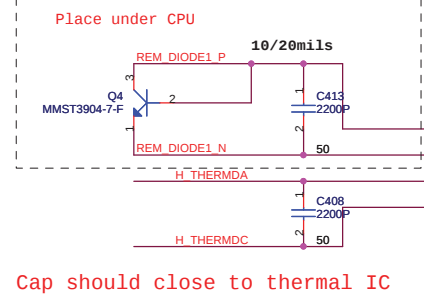
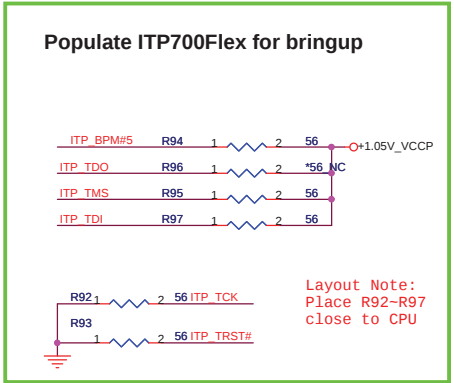
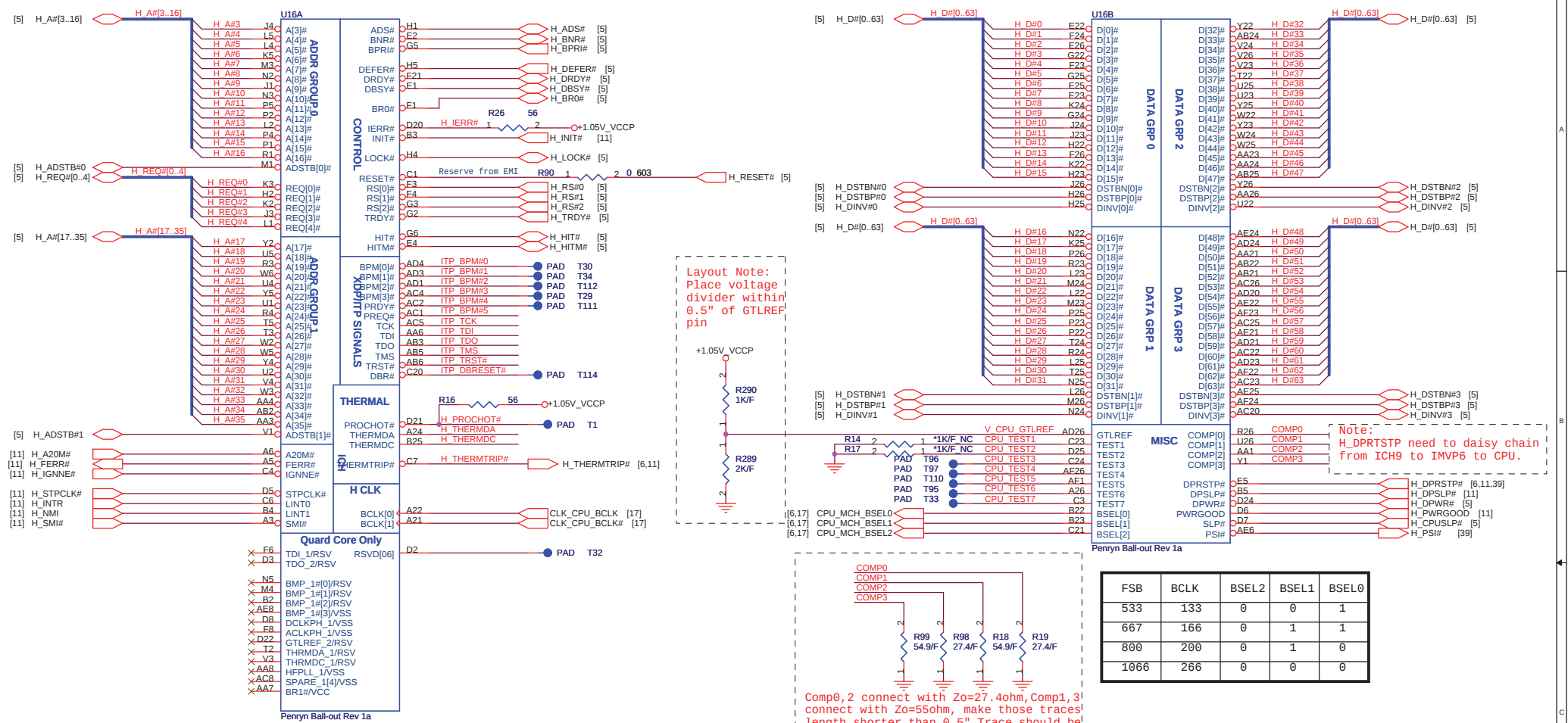


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Power States						
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN	
+PWR_SRC	10V~+19V	4,18,24,36,37,3,8,39,40,44	MAIN POWER		S0-S5	
+RTC_CELL	+3.0V~+3.3V	11,14,23,24	RTC		S0-S5	
+3.3V_ALW	+3.3V	3,23,24,30,35,36,38,40,41,42,45	8051 POWER	ALWON	S0-S5	
+5V_ALW2	+5V	37,38,40,41,42	LCD/CHARGE POWER	ALWON	S0-S5	
+15V_ALW	+15V	11,18,40,41	LARGE POWER	+5V_ALW	S0-S5	
+3.3V_LAN	+3.3V	34	LAN POWER			
+5V_SUS	+5V	14,27,30,39,40,41,44	SLP_S5# CTRLD POWER	SUS_ON		
+3.3V_SUS	+3.3V	3,11,12,13,14,18,25,30,37,39,41,45	SLP_S5# CTRLD POWER	3.3V_SUS_ON		
+1.8V_SUS	+1.8V	6,8,9,15,37,38,41	SODIMM POWER	DDR_ON		
+0.9V_DDR_VTT	+0.9V	16,38,41	SODIMM POWER	0.9V_DDR_VTT_ON		
+5V_RUN	+5V	14,18,19,21,25,28,29,30,31,32,41,44	SLP_S3# CTRLD POWER	RUN_ON		
+3.3V_RUN	+3.3V	3,6,8,9,11,12,13,14,15,17,30,31,32,34,18,19,20,21,23,25,26,28,41,44,45	SLP_S3# CTRLD POWER	3.3V_RUN_ON		
+1.5V_RUN	+1.5V	4,9,14,26,37,41,44	CALISTOGA/ICH8 POWER	1.5V_RUN_ON		
+1.05V_VCCP	+1.05V	3,4,6,8,9,11,14,37,44	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON		
+VCC_CORE	+0.7V~+1.77V	4,39	CPU CORE POWER	IMVP_VR_ON		
+LCDVCC	+3.3V	18	LCD Power	LCDVCC_TST_EN & ENVDD		
+5V_MOD	+5V	28	Module Power			
+5V_HDD	+5V	28	HDD Power			
+PBATT	+10V~+17V	42	MAIN BATTERY	CHG_PBATT		

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	

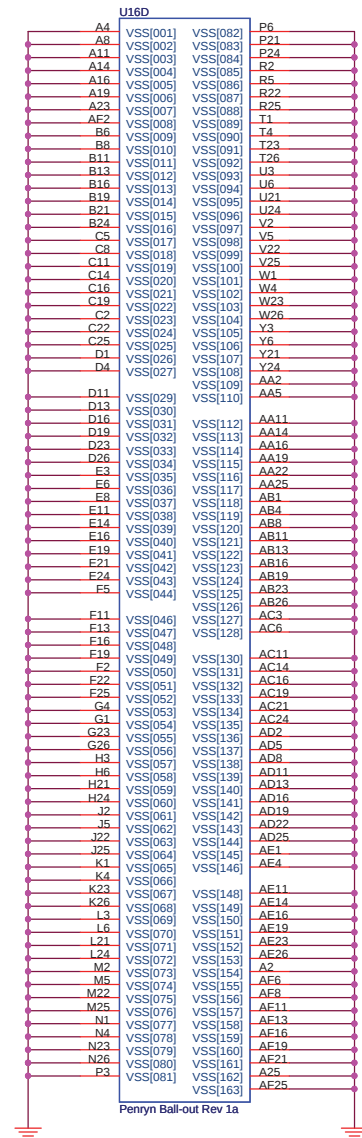
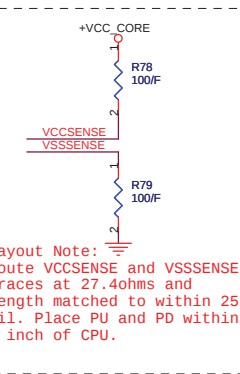
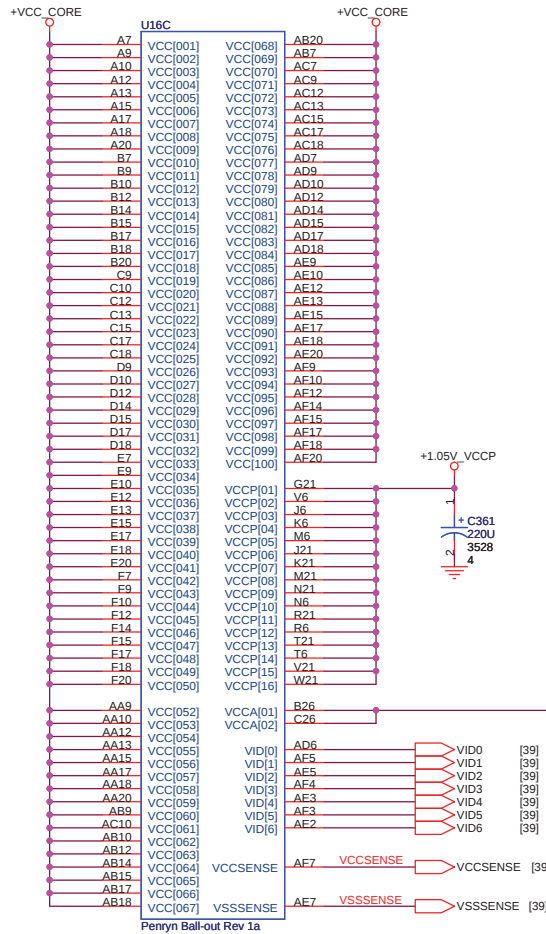
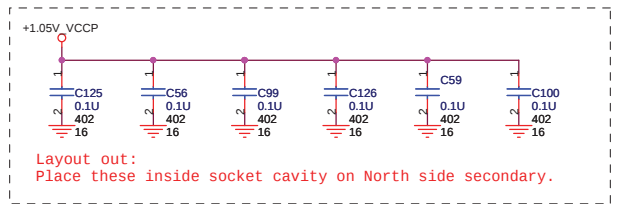
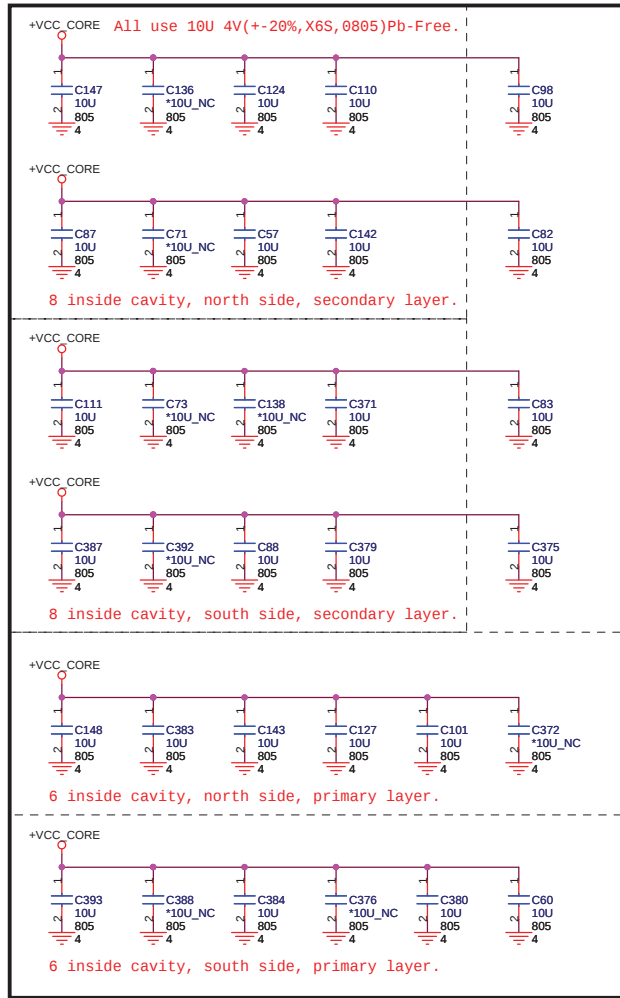


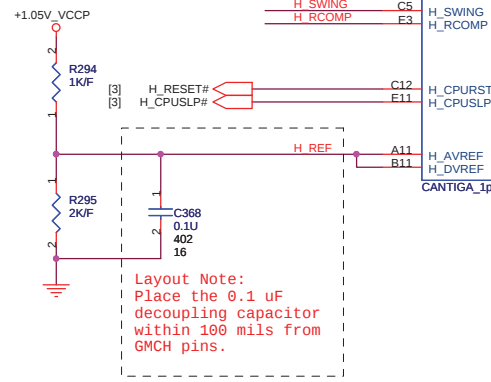
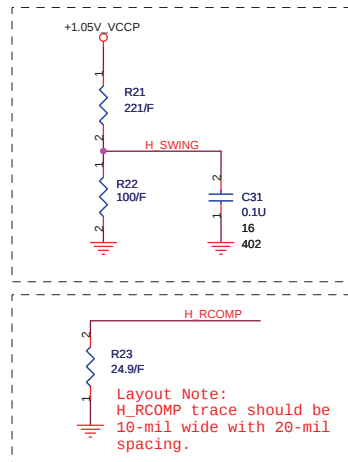
to EC



QUANTA
COMPUTER

File Penryn Processor (HOST BUS)		
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H D#0	F2	H D# 0
H D#1	G8	H D# 1
H D#2	F8	H D# 2
H D#3	E6	H D# 3
H D#4	G2	H D# 4
H D#5	H6	H D# 5
H D#6	H2	H D# 6
H D#7	F6	H D# 7
H D#8	D4	H D# 8
H D#9	H3	H D# 9
H D#10	M9	H D# 10
H D#11	J1	H D# 11
H D#12	J2	H D# 12
H D#13	N12	H D# 13
H D#14	J6	H D# 14
H D#15	P2	H D# 15
H D#16	L2	H D# 16
H D#17	R2	H D# 17
H D#18	N9	H D# 18
H D#19	L6	H D# 19
H D#20	M5	H D# 20
H D#21	J3	H D# 21
H D#22	N2	H D# 22
H D#23	R1	H D# 23
H D#24	N5	H D# 24
H D#25	N6	H D# 25
H D#26	P13	H D# 26
H D#27	N8	H D# 27
H D#28	L7	H D# 28
H D#29	N10	H D# 29
H D#30	M3	H D# 30
H D#31	Y2	H D# 31
H D#32	AD14	H D# 32
H D#33	Y6	H D# 33
H D#34	Y10	H D# 34
H D#35	Y12	H D# 35
H D#36	Y14	H D# 36
H D#37	Y7	H D# 37
H D#38	W2	H D# 38
H D#39	AA8	H D# 39
H D#40	Y9	H D# 40
H D#41	AA13	H D# 41
H D#42	AA9	H D# 42
H D#43	AA11	H D# 43
H D#44	AD11	H D# 44
H D#45	AD10	H D# 45
H D#46	AD13	H D# 46
H D#47	AE9	H D# 47
H D#48	AE3	H D# 48
H D#49	AC3	H D# 49
H D#50	AE11	H D# 50
H D#51	AE8	H D# 51
H D#52	AG2	H D# 52
H D#53	AD6	H D# 53

HOST

H_A#_3	A14	H_A#3
H_A#_4	C15	H_A#4
H_A#_5	F16	H_A#5
H_A#_6	H13	H_A#6
H_A#_7	C18	H_A#7
H_A#_8	M16	H_A#8
H_A#_9	J13	H_A#9
H_A#_10	P16	H_A#10
H_A#_11	R16	H_A#11
H_A#_12	N17	H_A#12
H_A#_13	M13	H_A#13
H_A#_14	E17	H_A#14
H_A#_15	P17	H_A#15
H_A#_16	E17	H_A#16
H_A#_17	G20	H_A#17
H_A#_18	B19	H_A#18
H_A#_19	J16	H_A#19
H_A#_20	E20	H_A#20
H_A#_21	H16	H_A#21
H_A#_22	J20	H_A#22
H_A#_23	L17	H_A#23
H_A#_24	A17	H_A#24
H_A#_25	B17	H_A#25
H_A#_26	L16	H_A#26
H_A#_27	C21	H_A#27
H_A#_28	J17	H_A#28
H_A#_29	H20	H_A#29
H_A#_30	B18	H_A#30
H_A#_31	K17	H_A#31
H_A#_32	B20	H_A#32
H_A#_33	F21	H_A#33
H_A#_34	K21	H_A#34
H_A#_35	L20	H_A#35

H_DIN#_0	J8	H_DIN#0
H_DIN#_1	L3	H_DIN#1
H_DIN#_2	Y13	H_DIN#2
H_DIN#_3	Y1	H_DIN#3

H_DSTBN#_0	L10	H_DSTBN#0
H_DSTBN#_1	M7	H_DSTBN#1
H_DSTBN#_2	AA5	H_DSTBN#2
H_DSTBN#_3	AE6	H_DSTBN#3

H_DSTBP#_0	L9	H_DSTBP#0
H_DSTBP#_1	M8	H_DSTBP#1
H_DSTBP#_2	AA6	H_DSTBP#2
H_DSTBP#_3	AE5	H_DSTBP#3

H_REQ#_0	B15	H_REQ#0
H_REQ#_1	K13	H_REQ#1
H_REQ#_2	E13	H_REQ#2
H_REQ#_3	B13	H_REQ#3
H_REQ#_4	B14	H_REQ#4

H_RS#_0	B6	H_RS#0
H_RS#_1	E12	H_RS#1
H_RS#_2	C8	H_RS#2

For EA test use

ET10	1	H_DSTBP#0
ET2	1	H_D#7
ET14	1	H_D#12
ET9	1	H_DSTBN#1
ET8	1	H_DSTBP#1
ET13	1	H_D#9
ET3	1	H_D#21
ET18	1	H_D#32



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[15] DDR_A_D[0..63]

DDR A D0	A138	SA_DQ_0
DDR A D1	A141	SA_DQ_1
DDR A D2	AN38	SA_DQ_2
DDR A D3	AM38	SA_DQ_3
DDR A D4	A136	SA_DQ_4
DDR A D5	A140	SA_DQ_5
DDR A D6	AM44	SA_DQ_6
DDR A D7	AM42	SA_DQ_7
DDR A D8	AN43	SA_DQ_8
DDR A D9	AN44	SA_DQ_9
DDR A D10	AU40	SA_DQ_10
DDR A D11	AT36	SA_DQ_11
DDR A D12	AN41	SA_DQ_12
DDR A D13	AN39	SA_DQ_13
DDR A D14	AU44	SA_DQ_14
DDR A D15	AU42	SA_DQ_15
DDR A D16	AV39	SA_DQ_16
DDR A D17	AY44	SA_DQ_17
DDR A D18	BA40	SA_DQ_18
DDR A D19	BD43	SA_DQ_19
DDR A D20	AV41	SA_DQ_20
DDR A D21	AY43	SA_DQ_21
DDR A D22	BA41	SA_DQ_22
DDR A D23	BC40	SA_DQ_23
DDR A D24	AY37	SA_DQ_24
DDR A D25	BD38	SA_DQ_25
DDR A D26	AV37	SA_DQ_26
DDR A D27	AT36	SA_DQ_27
DDR A D28	AY38	SA_DQ_28
DDR A D29	BB38	SA_DQ_29
DDR A D30	AV36	SA_DQ_30
DDR A D31	AW36	SA_DQ_31
DDR A D32	BD13	SA_DQ_32
DDR A D33	AU11	SA_DQ_33
DDR A D34	BC11	SA_DQ_34
DDR A D35	BA12	SA_DQ_35
DDR A D36	AU13	SA_DQ_36
DDR A D37	AV13	SA_DQ_37
DDR A D38	BD12	SA_DQ_38
DDR A D39	BC12	SA_DQ_39
DDR A D40	BB9	SA_DQ_40
DDR A D41	BA9	SA_DQ_41
DDR A D42	AU10	SA_DQ_42
DDR A D43	AV9	SA_DQ_43
DDR A D44	BA11	SA_DQ_44
DDR A D45	BD9	SA_DQ_45
DDR A D46	AY8	SA_DQ_46
DDR A D47	BA6	SA_DQ_47
DDR A D48	AV5	SA_DQ_48
DDR A D49	AV7	SA_DQ_49
DDR A D50	AT9	SA_DQ_50
DDR A D51	AN8	SA_DQ_51
DDR A D52	AU5	SA_DQ_52
DDR A D53	AT5	SA_DQ_53
DDR A D54	AU6	SA_DQ_54
DDR A D55	AN10	SA_DQ_55
DDR A D56	AM11	SA_DQ_56
DDR A D57	AM5	SA_DQ_57
DDR A D58	A19	SA_DQ_58
DDR A D59	A18	SA_DQ_59
DDR A D60	AM12	SA_DQ_60
DDR A D61	AM13	SA_DQ_61
DDR A D62	AJ11	SA_DQ_62
DDR A D63	AJ12	SA_DQ_63

CANTIGA_tp0

DDR SYSTEM MEMORY A

SA_BS_0	BD21	DDR A BS0
SA_BS_1	RG18	DDR A BS1
SA_BS_2	AT25	DDR A BS2
SA_RAS#	BB20	DDR A RAS#
SA_CAS#	BD20	DDR A CAS#
SA_WE#	AY20	DDR A WE#
SA_DM_0	AM37	DDR A DM0
SA_DM_1	AT41	DDR A DM1
SA_DM_2	AY41	DDR A DM2
SA_DM_3	AU39	DDR A DM3
SA_DM_4	BB12	DDR A DM4
SA_DM_5	AY6	DDR A DM5
SA_DM_6	AT7	DDR A DM6
SA_DM_7	AJ5	DDR A DM7
SA_DQS_0	AJ44	DDR A DQS0
SA_DQS_1	AT44	DDR A DQS1
SA_DQS_2	BA43	DDR A DQS2
SA_DQS_3	BC37	DDR A DQS3
SA_DQS_4	AW12	DDR A DQS4
SA_DQS_5	BC8	DDR A DQS5
SA_DQS_6	AU8	DDR A DQS6
SA_DQS_7	AM7	DDR A DQS7
SA_DQS#_0	AJ43	DDR A DQS#0
SA_DQS#_1	AT43	DDR A DQS#1
SA_DQS#_2	BA44	DDR A DQS#2
SA_DQS#_3	BD37	DDR A DQS#3
SA_DQS#_4	AY12	DDR A DQS#4
SA_DQS#_5	BD8	DDR A DQS#5
SA_DQS#_6	AU9	DDR A DQS#6
SA_DQS#_7	AM8	DDR A DQS#7
SA_MA_0	BA21	DDR A MA0
SA_MA_1	BG24	DDR A MA1
SA_MA_2	BH24	DDR A MA2
SA_MA_3	BG25	DDR A MA3
SA_MA_4	BA24	DDR A MA4
SA_MA_5	BD24	DDR A MA5
SA_MA_6	BG27	DDR A MA6
SA_MA_7	BF25	DDR A MA7
SA_MA_8	AW24	DDR A MA8
SA_MA_9	RC21	DDR A MA9
SA_MA_10	BG26	DDR A MA10
SA_MA_11	BH26	DDR A MA11
SA_MA_12	BH17	DDR A MA13
SA_MA_13	AY25	DDR A MA14
SA_MA_14		

DDR_A_BS0	[15,16]
DDR_A_BS1	[15,16]
DDR_A_BS2	[15,16]
DDR_A_RAS#	[15,16]
DDR_A_CAS#	[15,16]
DDR_A_WE#	[15,16]
DDR_A_DM[0..7]	[15]
DDR_A_DQS[0..7]	[15]
DDR_A_DQS#[0..7]	[15]
DDR_A_MA[0..14]	[15,16]

[15] DDR_B_D[0..63]

DDR B D0	AK47	SB_DQ_0
DDR B D1	AH46	SB_DQ_1
DDR B D2	AP47	SB_DQ_2
DDR B D3	AP46	SB_DQ_3
DDR B D4	AJ46	SB_DQ_4
DDR B D5	A148	SB_DQ_5
DDR B D6	AM48	SB_DQ_6
DDR B D7	AP48	SB_DQ_7
DDR B D8	AU47	SB_DQ_8
DDR B D9	AU46	SB_DQ_9
DDR B D10	BA48	SB_DQ_10
DDR B D11	AY48	SB_DQ_11
DDR B D12	AT47	SB_DQ_12
DDR B D13	AR47	SB_DQ_13
DDR B D14	RA47	SB_DQ_14
DDR B D15	BC47	SB_DQ_15
DDR B D16	RC46	SB_DQ_16
DDR B D17	RC44	SB_DQ_17
DDR B D18	RG43	SB_DQ_18
DDR B D19	BE43	SB_DQ_19
DDR B D20	BE45	SB_DQ_20
DDR B D21	BC41	SB_DQ_21
DDR B D22	BE40	SB_DQ_22
DDR B D23	BE41	SB_DQ_23
DDR B D24	BG38	SB_DQ_24
DDR B D25	BE38	SB_DQ_25
DDR B D26	BH35	SB_DQ_26
DDR B D27	BG35	SB_DQ_27
DDR B D28	BH40	SB_DQ_28
DDR B D29	BG39	SB_DQ_29
DDR B D30	BG34	SB_DQ_30
DDR B D31	BH34	SB_DQ_31
DDR B D32	BH14	SB_DQ_32
DDR B D33	BG12	SB_DQ_33
DDR B D34	BH11	SB_DQ_34
DDR B D35	BG8	SB_DQ_35
DDR B D36	BH12	SB_DQ_36
DDR B D37	BE11	SB_DQ_37
DDR B D38	BE8	SB_DQ_38
DDR B D39	BG7	SB_DQ_39
DDR B D40	BC5	SB_DQ_40
DDR B D41	BC6	SB_DQ_41
DDR B D42	AY3	SB_DQ_42
DDR B D43	AY1	SB_DQ_43
DDR B D44	BE6	SB_DQ_44
DDR B D45	BE5	SB_DQ_45
DDR B D46	BA1	SB_DQ_46
DDR B D47	BD3	SB_DQ_47
DDR B D48	AV2	SB_DQ_48
DDR B D49	AU3	SB_DQ_49
DDR B D50	AR3	SB_DQ_50
DDR B D51	AN2	SB_DQ_51
DDR B D52	AY2	SB_DQ_52
DDR B D53	AV1	SB_DQ_53
DDR B D54	AP3	SB_DQ_54
DDR B D55	AR1	SB_DQ_55
DDR B D56	AL1	SB_DQ_56
DDR B D57	AL2	SB_DQ_57
DDR B D58	A11	SB_DQ_58
DDR B D59	AM2	SB_DQ_59
DDR B D60	AM1	SB_DQ_60
DDR B D61	AM3	SB_DQ_61
DDR B D62	AH3	SB_DQ_62
DDR B D63	A13	SB_DQ_63

U15E

DDR SYSTEM MEMORY B

SB_BS_0	BC16	DDR B BS0
SB_BS_1	RB17	DDR B BS1
SB_BS_2	BB33	DDR B BS2
SB_RAS#	AU17	DDR B RAS#
SB_CAS#	BG16	DDR B CAS#
SB_WE#	BF14	DDR B WE#
SB_DM_0	AM47	DDR B DM0
SB_DM_1	AY47	DDR B DM1
SB_DM_2	BD40	DDR B DM2
SB_DM_3	BE35	DDR B DM3
SB_DM_4	RG11	DDR B DM4
SB_DM_5	BA3	DDR B DM5
SB_DM_6	AP1	DDR B DM6
SB_DM_7	AK2	DDR B DM7
SB_DQS_0	AL47	DDR B DQS0
SB_DQS_1	AV48	DDR B DQS1
SB_DQS_2	BG41	DDR B DQS2
SB_DQS_3	BG37	DDR B DQS3
SB_DQS_4	BH9	DDR B DQS4
SB_DQS_5	BB2	DDR B DQS5
SB_DQS_6	AU1	DDR B DQS6
SB_DQS_7	AN6	DDR B DQS7
SB_DQS#_0	AL46	DDR B DQS#0
SB_DQS#_1	AV47	DDR B DQS#1
SB_DQS#_2	BH41	DDR B DQS#2
SB_DQS#_3	BH37	DDR B DQS#3
SB_DQS#_4	BC2	DDR B DQS#4
SB_DQS#_5	AT2	DDR B DQS#5
SB_DQS#_6	AN5	DDR B DQS#6
SB_DQS#_7		
SB_MA_0	AV17	DDR B MA0
SB_MA_1	BA25	DDR B MA1
SB_MA_2	BC25	DDR B MA2
SB_MA_3	AU25	DDR B MA3
SB_MA_4	AW25	DDR B MA4
SB_MA_5	BB28	DDR B MA5
SB_MA_6	AU28	DDR B MA6
SB_MA_7	AW28	DDR B MA7
SB_MA_8	AT33	DDR B MA8
SB_MA_9	BD33	DDR B MA9
SB_MA_10	BB16	DDR B MA10
SB_MA_11	AW33	DDR B MA11
SB_MA_12	AY33	DDR B MA12
SB_MA_13	BH15	DDR B MA13
SB_MA_14	AU33	DDR B MA14

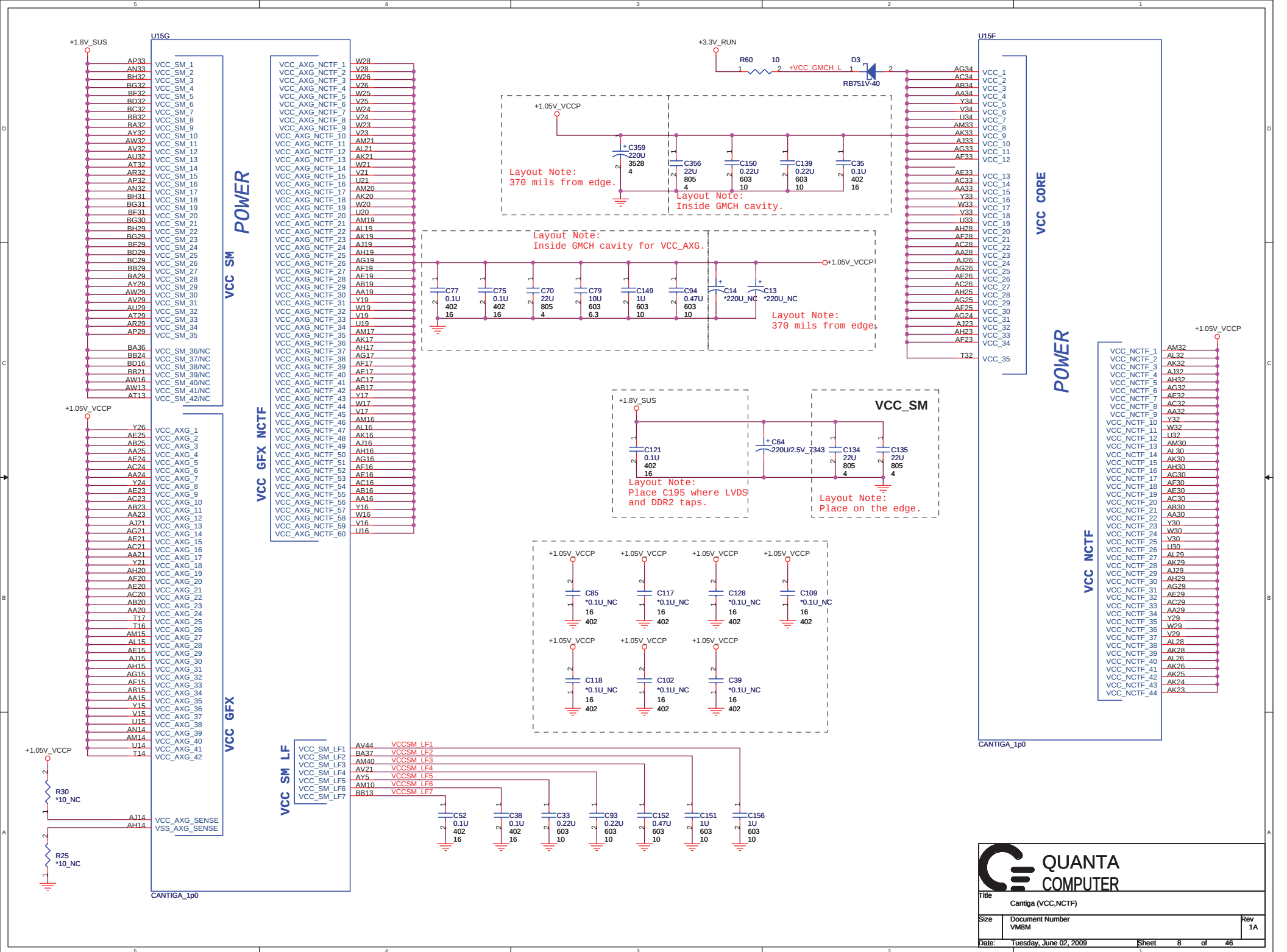
DDR_B_BS0	[15,16]
DDR_B_BS1	[15,16]
DDR_B_BS2	[15,16]
DDR_B_RAS#	[15,16]
DDR_B_CAS#	[15,16]
DDR_B_WE#	[15,16]
DDR_B_DM[0..7]	[15]
DDR_B_DQS[0..7]	[15]
DDR_B_DQS#[0..7]	[15]
DDR_B_MA[0..14]	[15,16]

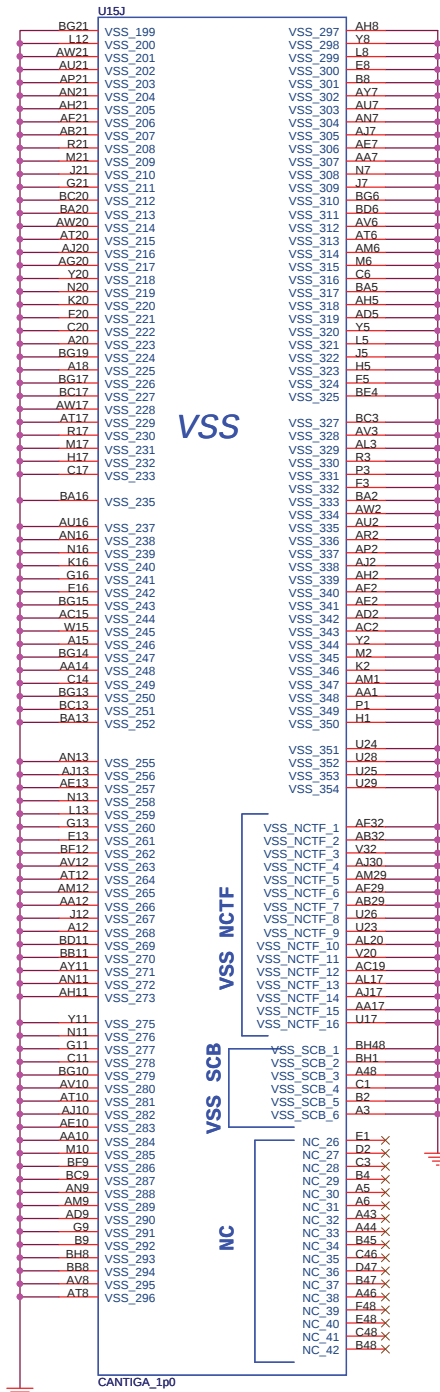
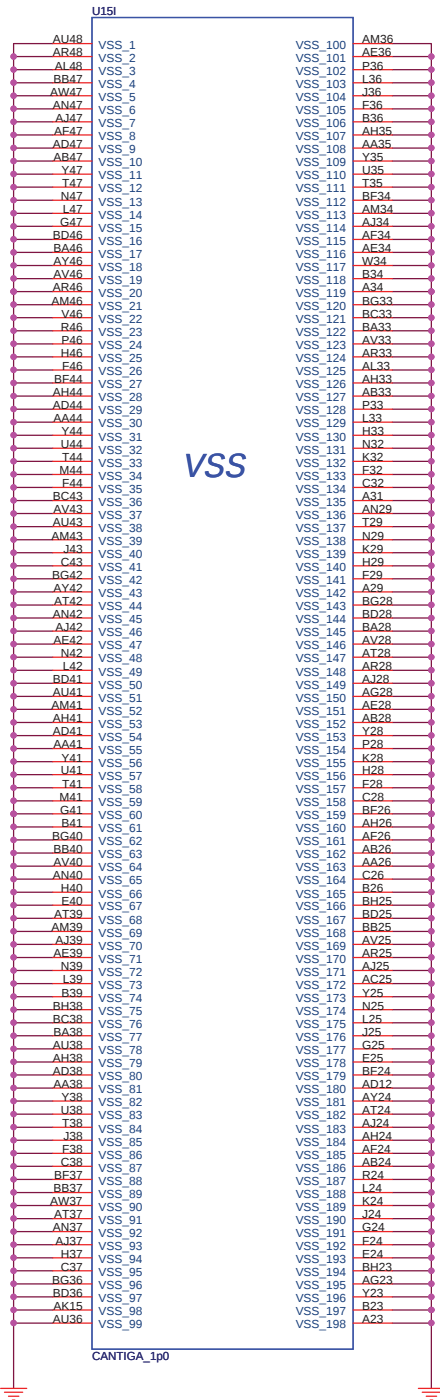
CANTIGA_tp0



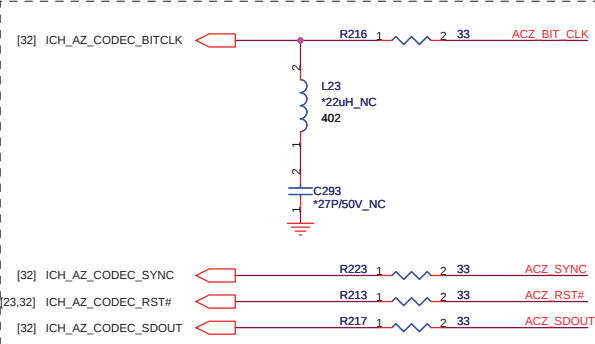
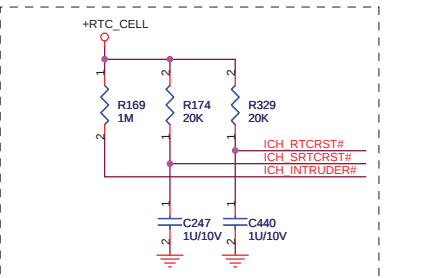
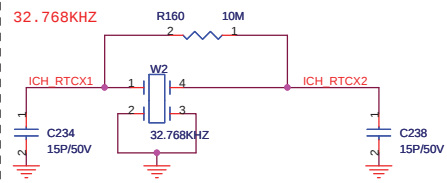
QUANTA
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Title			
Cantiga (DDR2)			
Size	Document Number		Rev
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Date:	Tuesday, June 02, 2009	Sheet	7 of 46

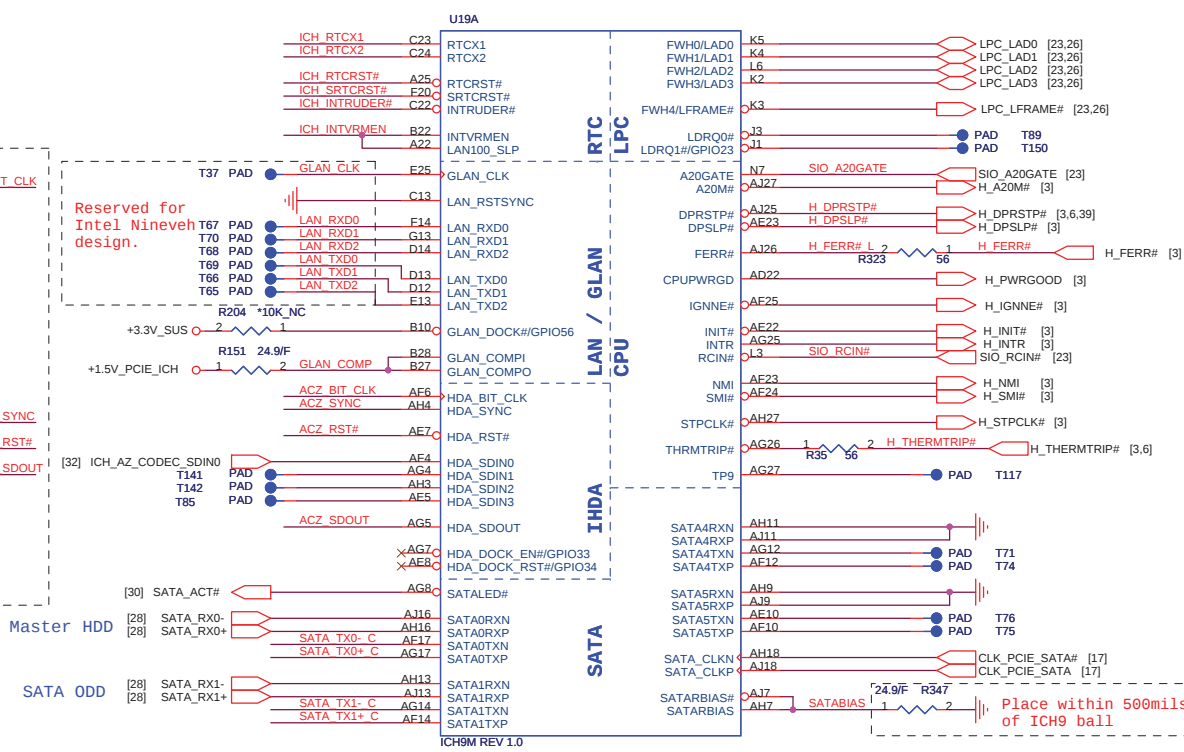
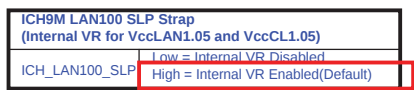
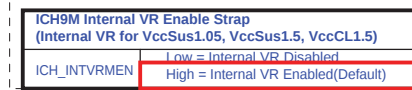
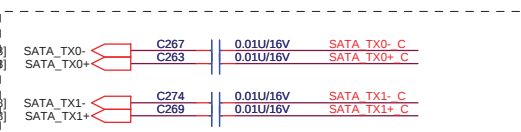




 QUANTA COMPUTER		
Title Cantiga (VSS)		
Size VMBM	Document Number	Rev 1A
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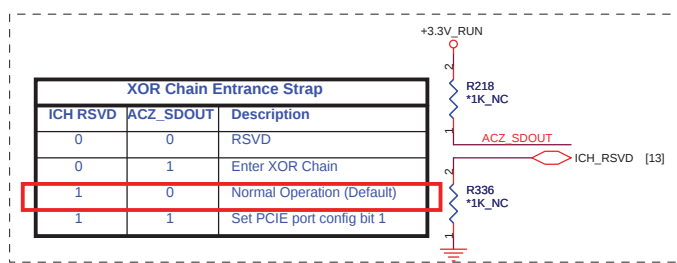


Place all series terms close to ICH9 except for SDIN input lines, which should be close to source.

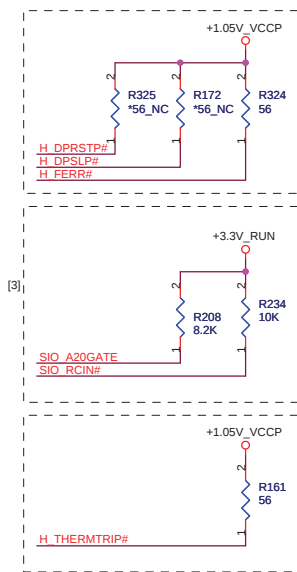


Master HDD

SATA ODD

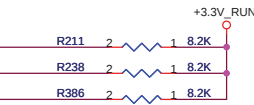
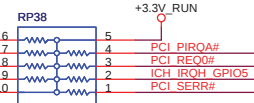
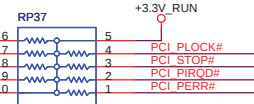
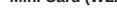
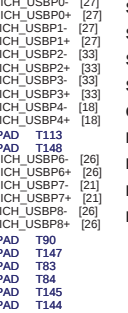
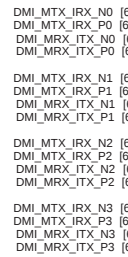
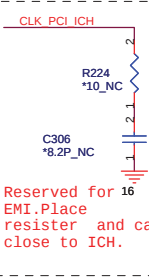
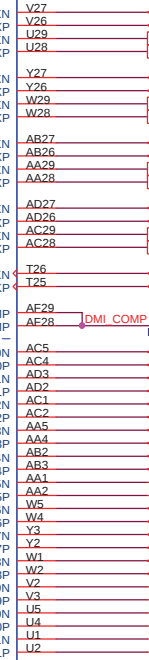
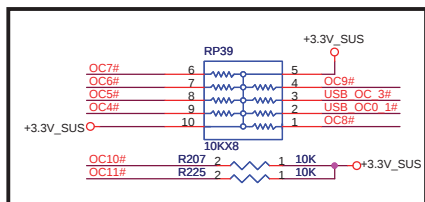


XOR Chain Entrance Strap		
ICH_RSVD	ACZ_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIe port config bit 1

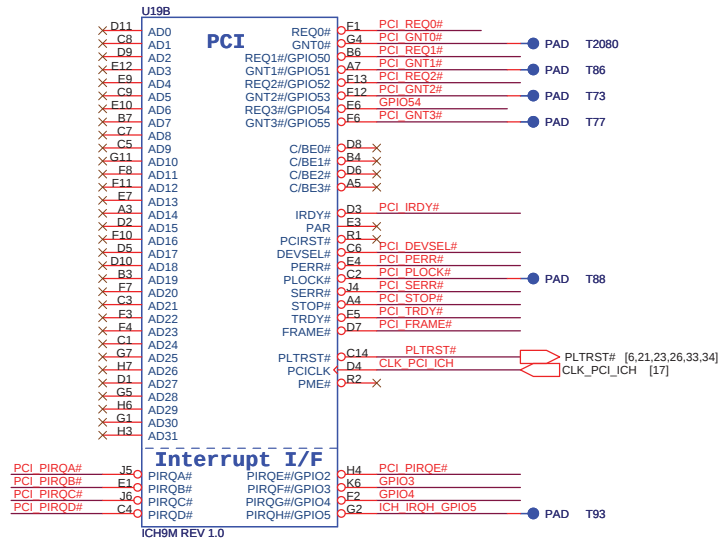


CIE_TX6-/GLAN_TX-	C229	1	2	0.1U	16	GLAN TXN C
CIE_TX6+/GLAN_TX+	C230	1	2	0.1U	16	GLAN TXP C

Boot BIOS Strap			
		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

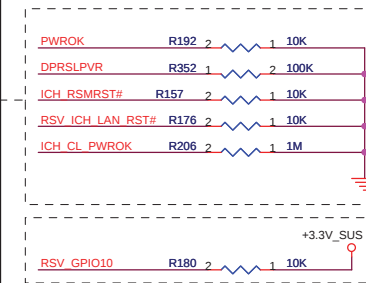


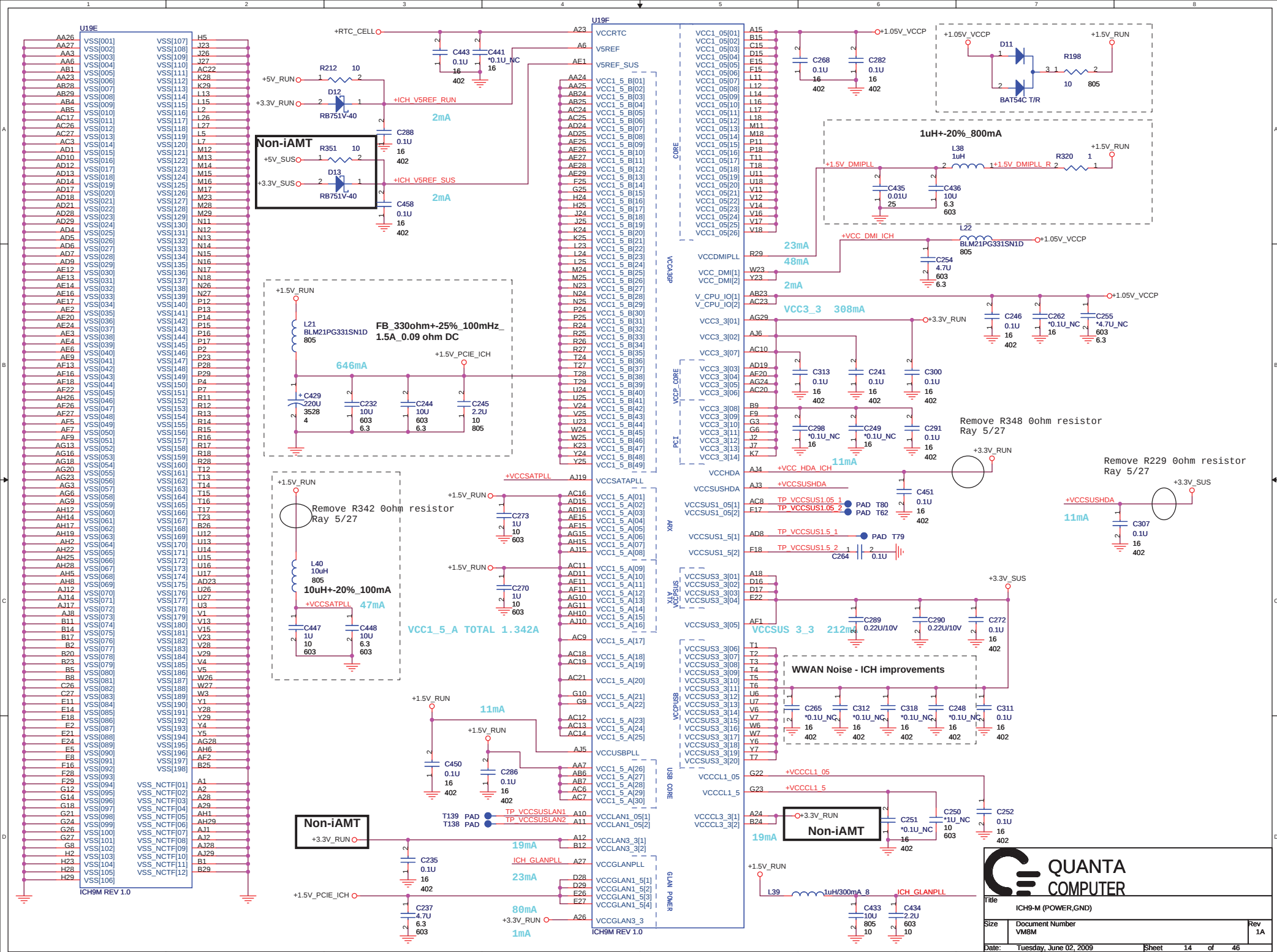
BIOS should not enable the internal GPIO pull up resistor



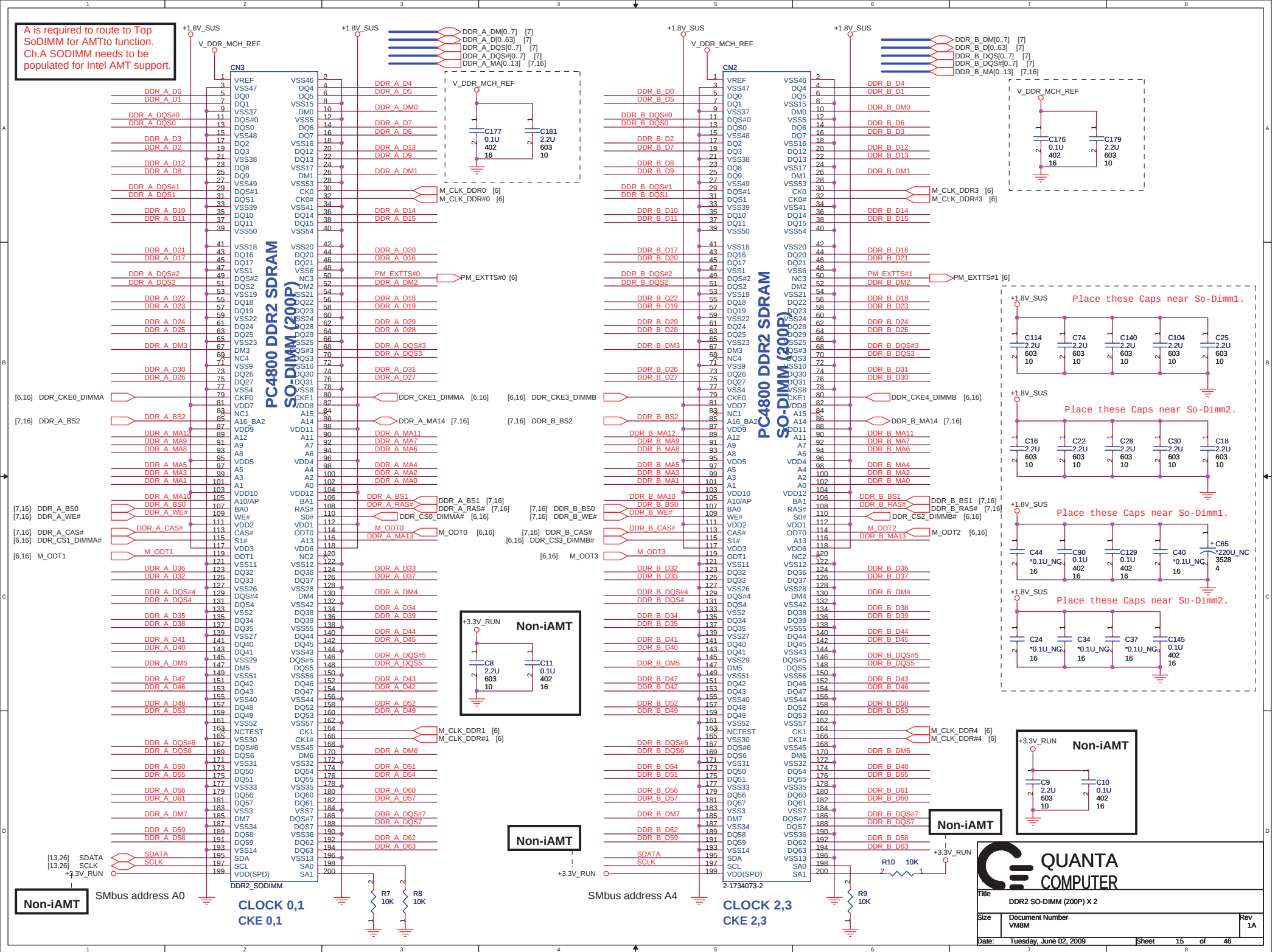
QUANTA
COMPUTER

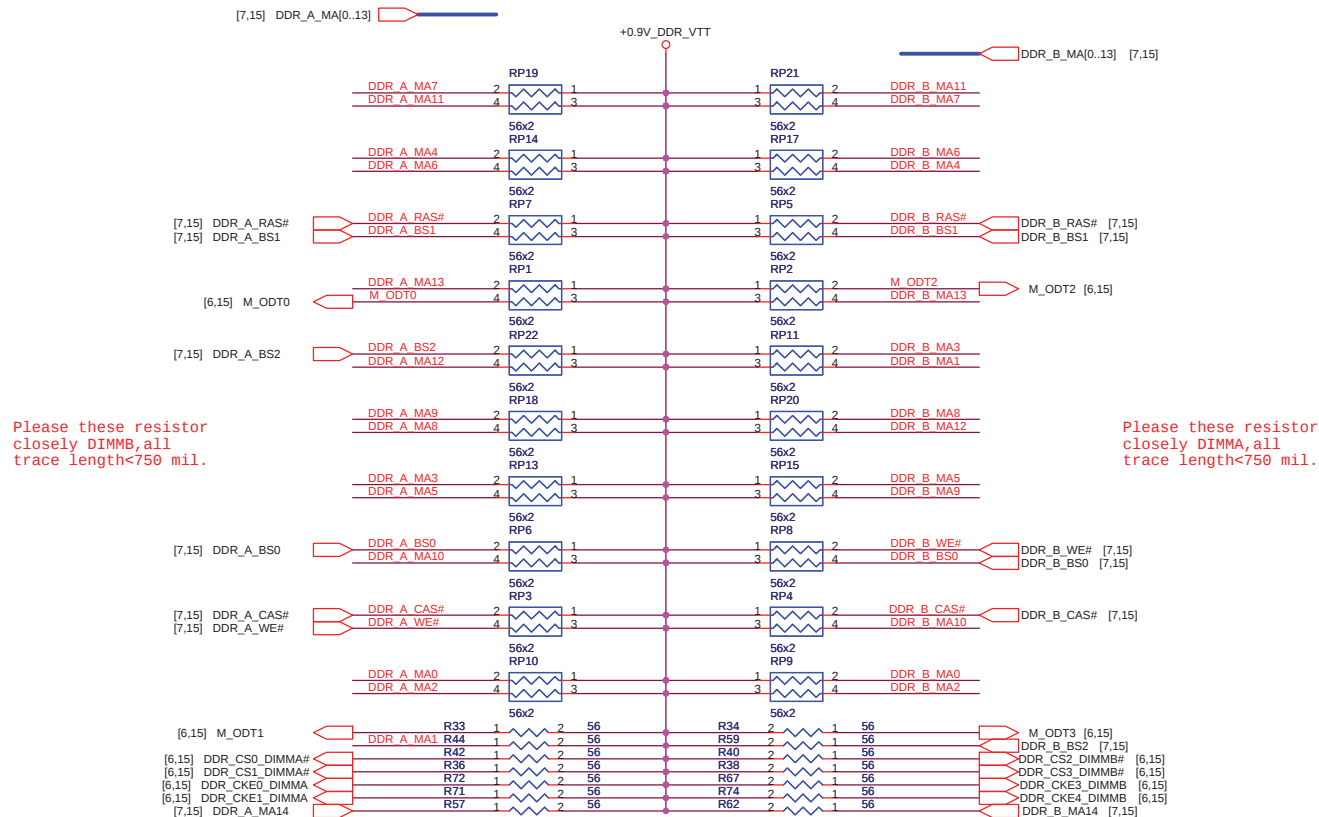
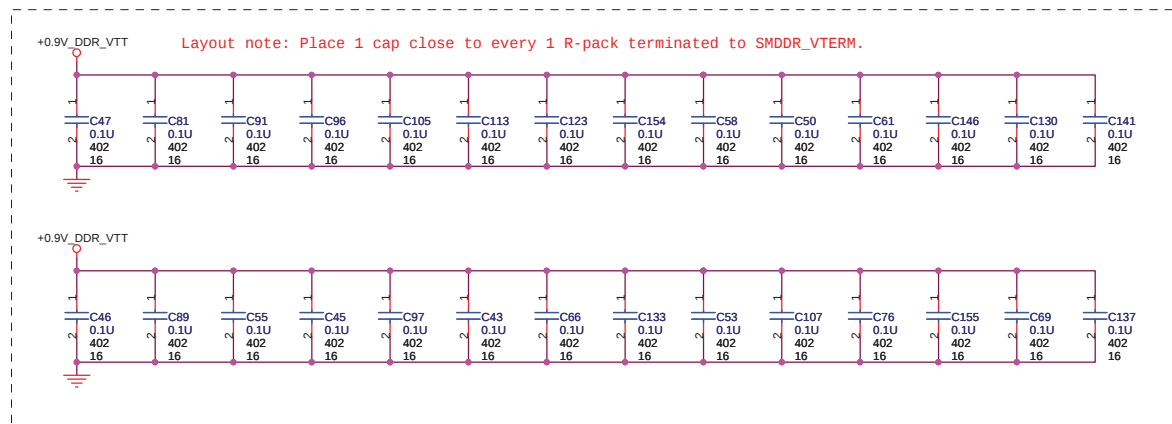
Title		
ICH9-M (USB,DMI,PCI,PCI)		
Size	Document Number	Rev
	VM8M	1A
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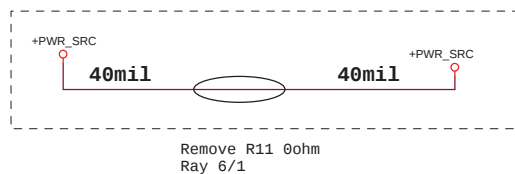
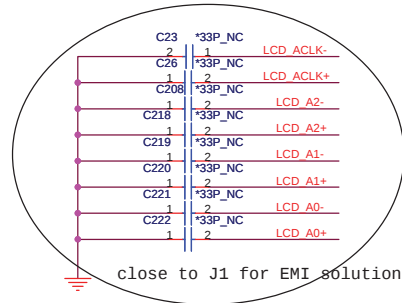
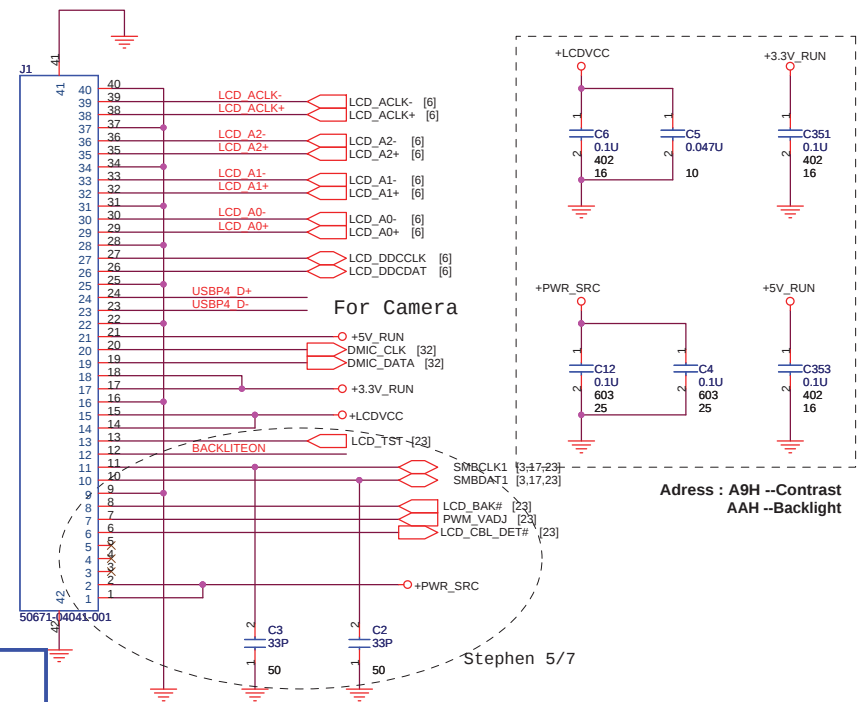


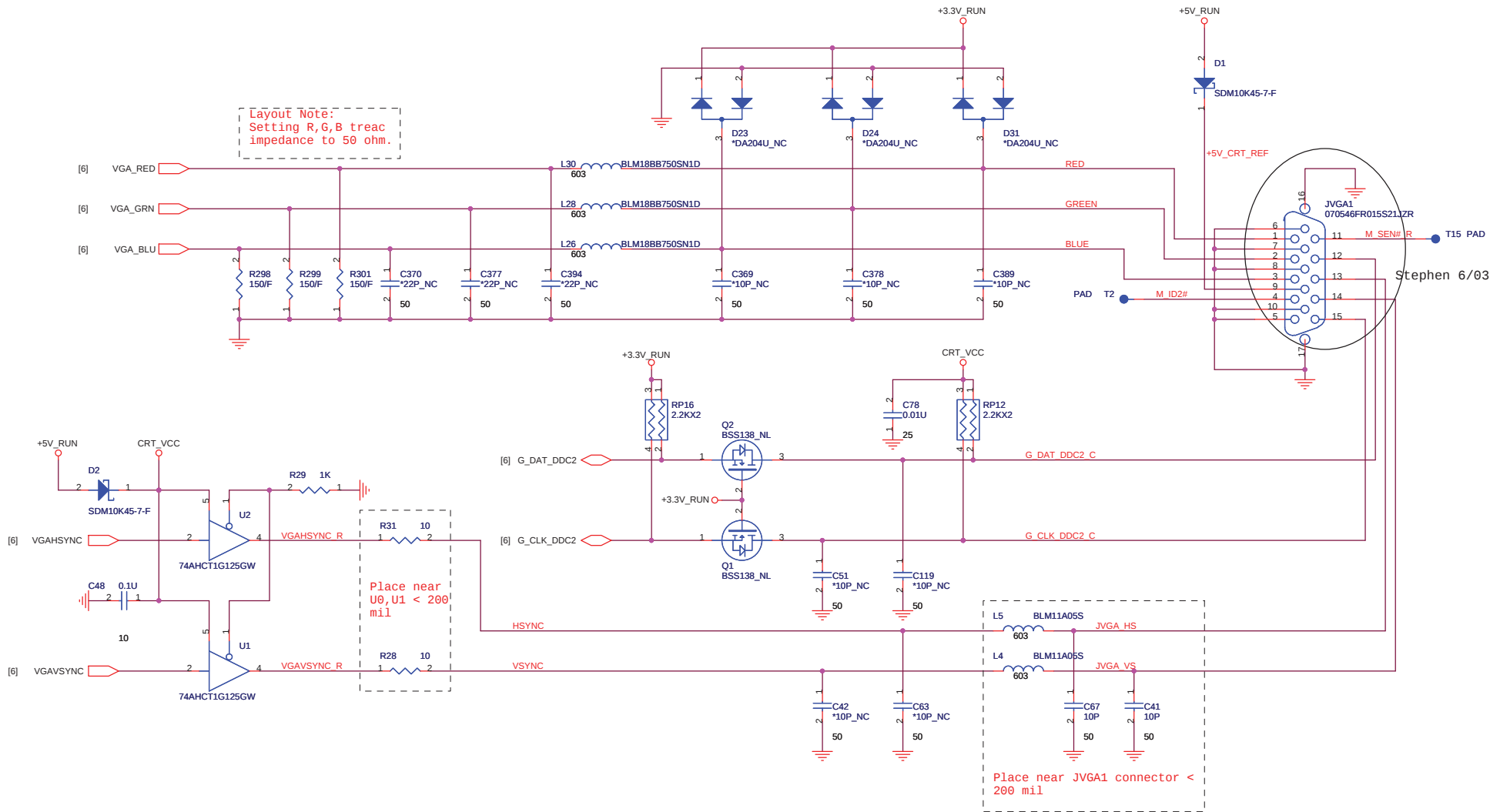


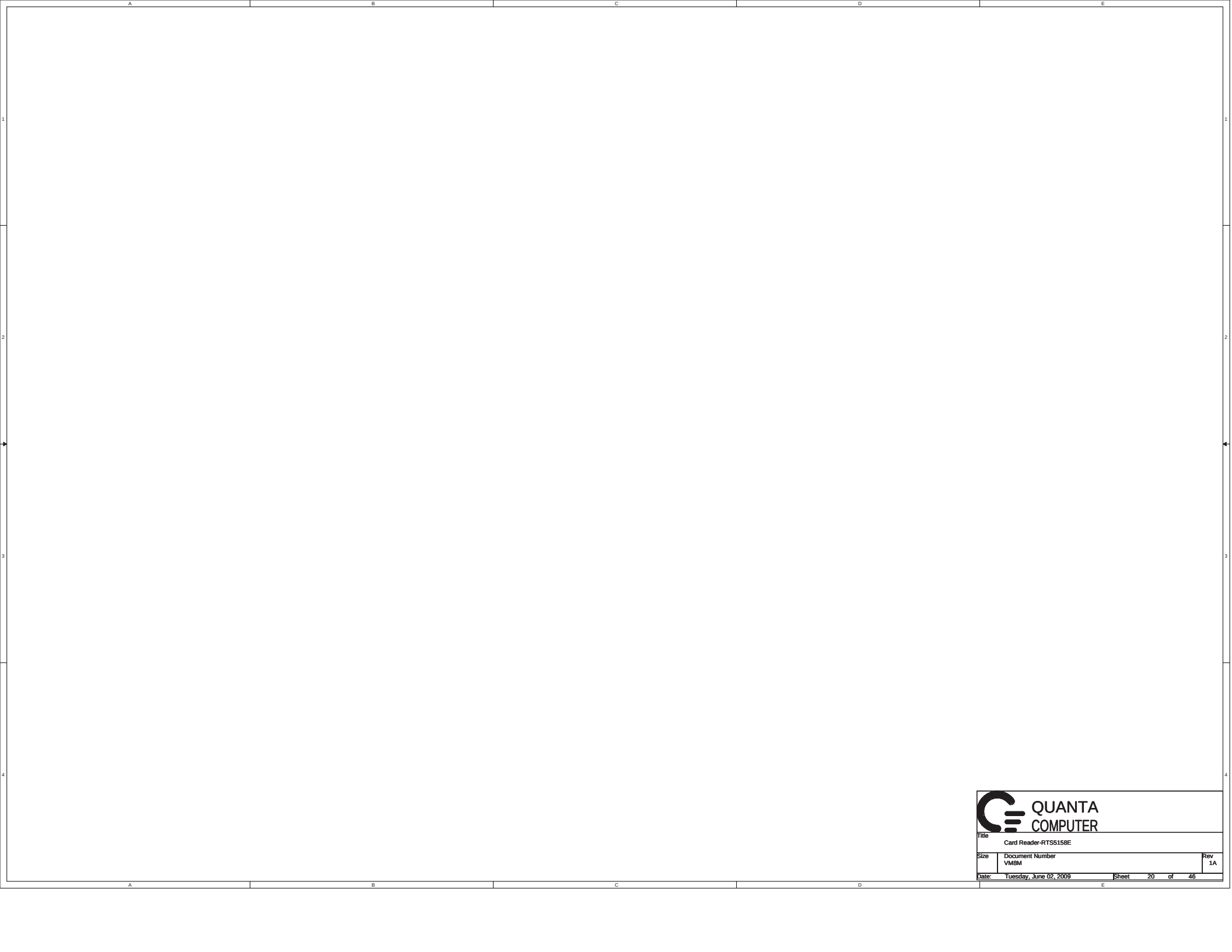
A is required to route to Top SoDIMM for AMT to function. Ch.A SODIMM needs to be populated for Intel AMT support.



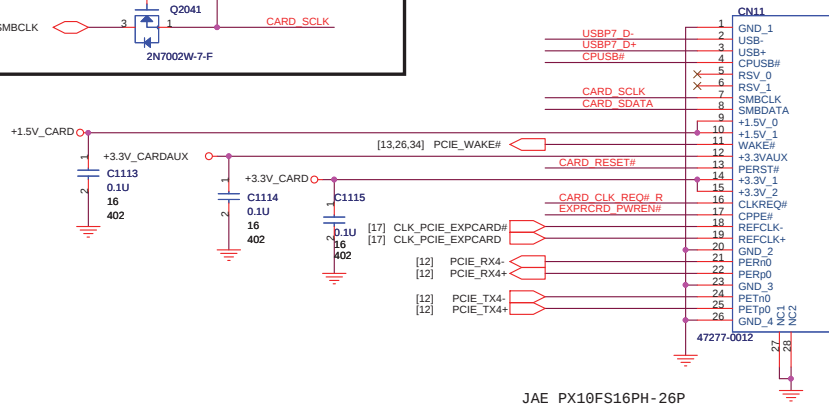
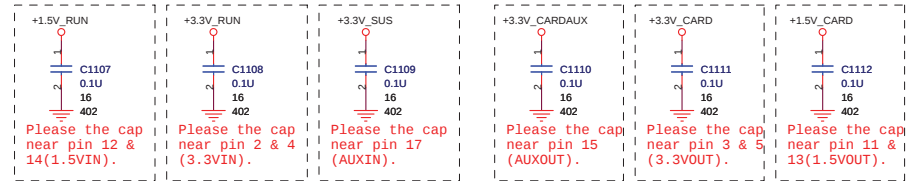
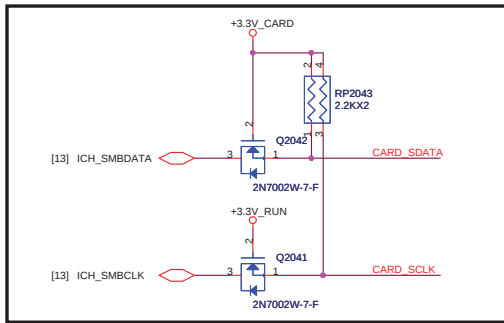
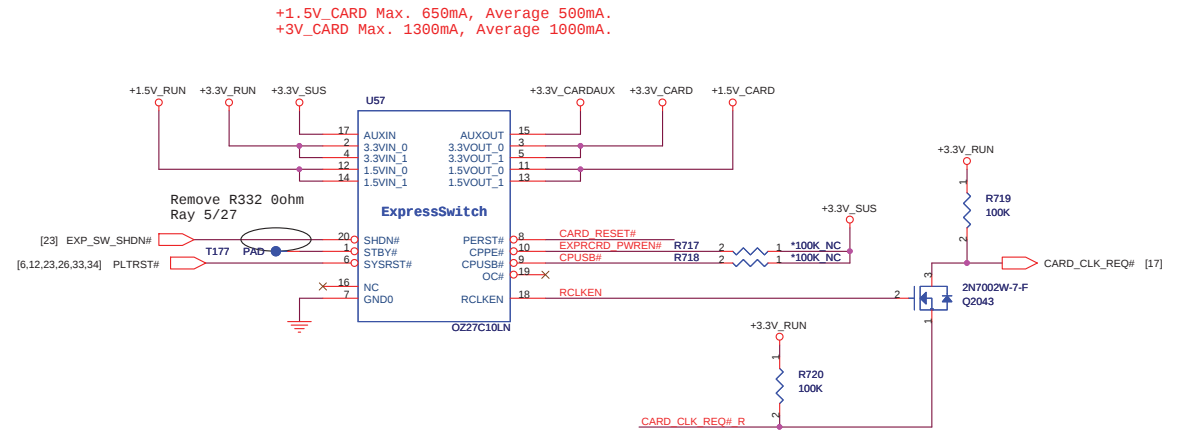
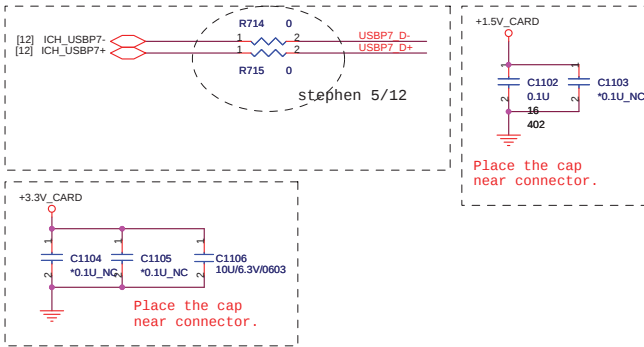








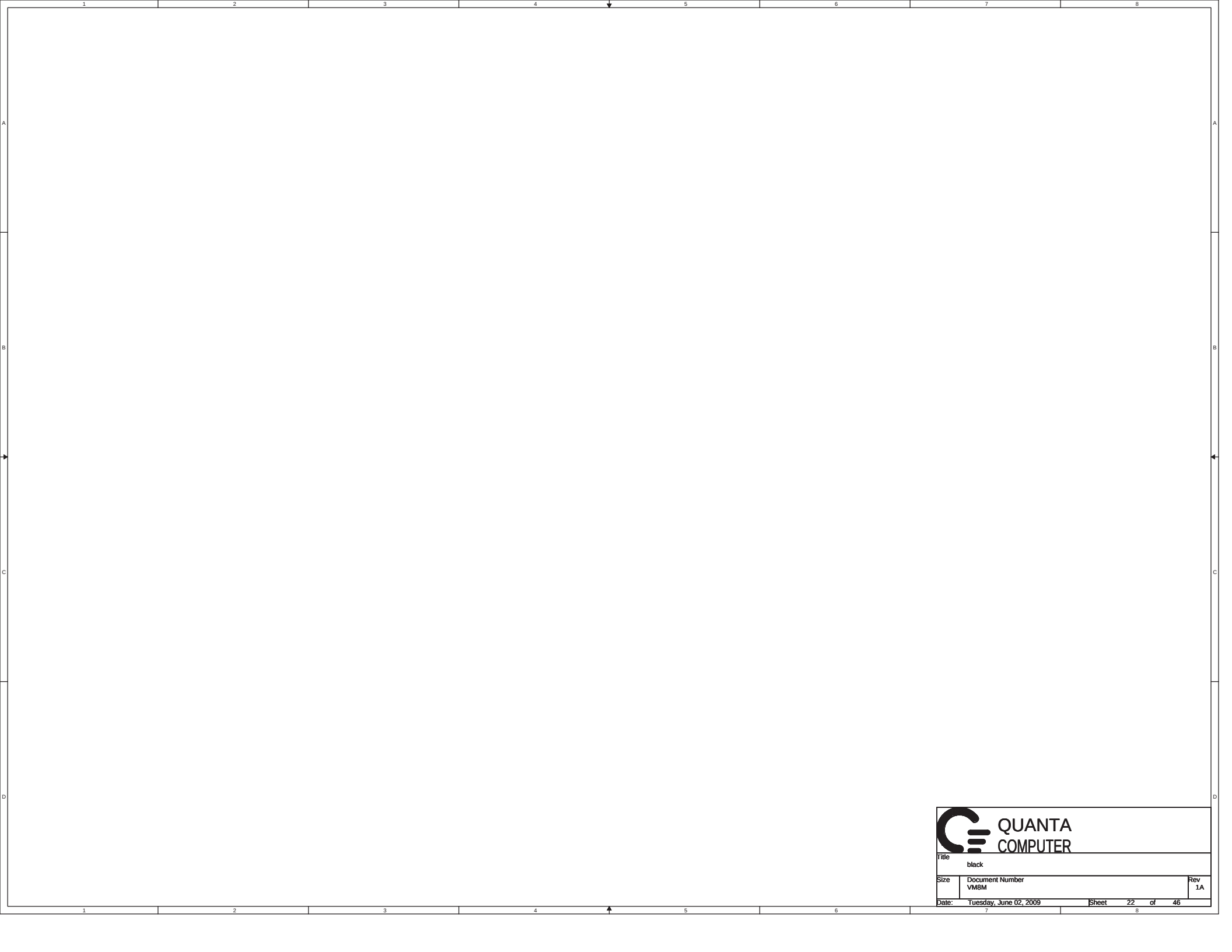
 QUANTA COMPUTER			
Title Card Reader-RTSS158E			
Size	Document Number VM8M		Rev 1A
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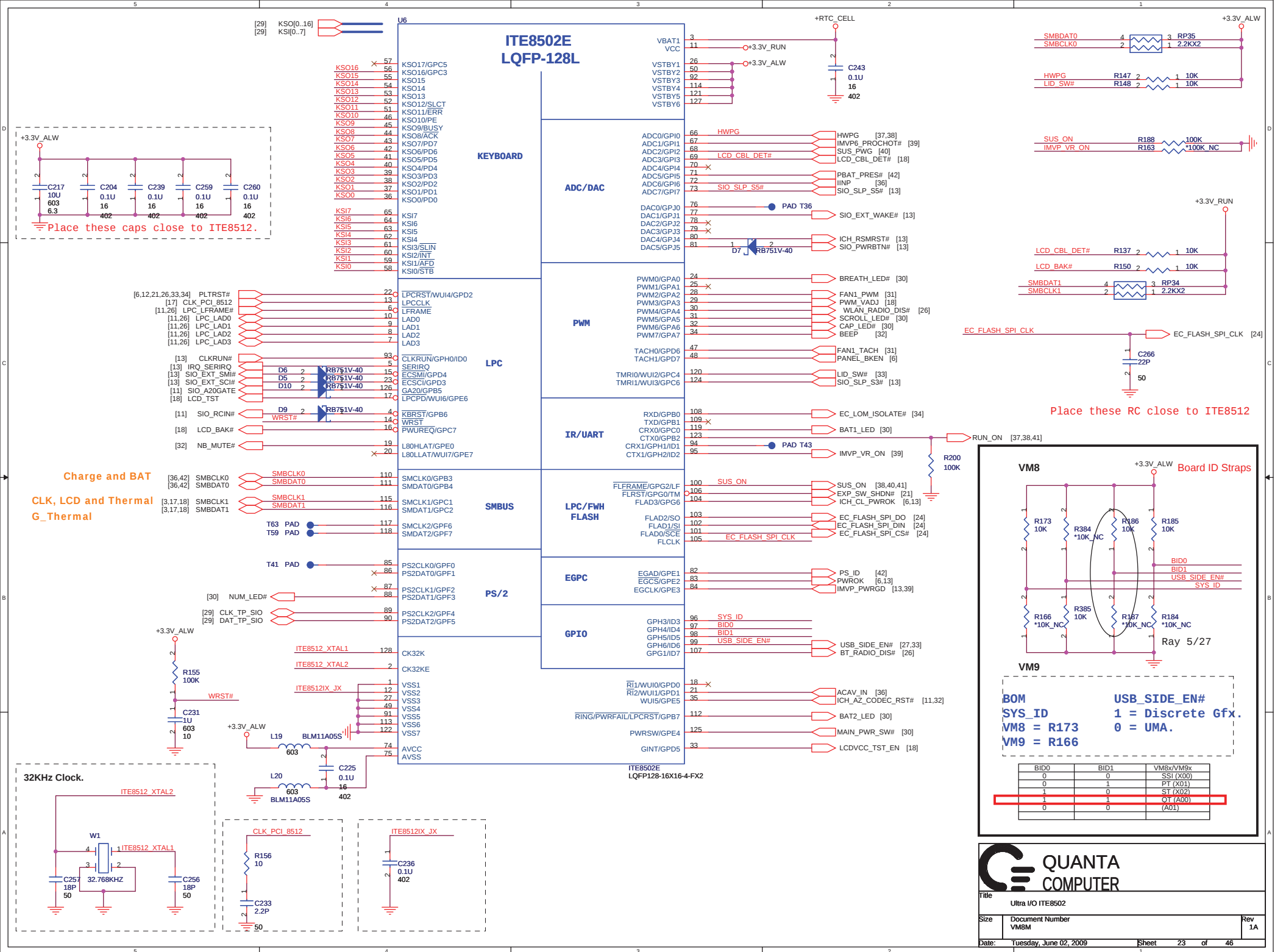
Express Card



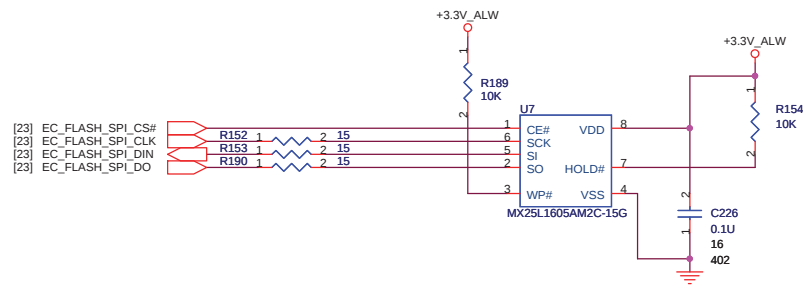
Express Card cage



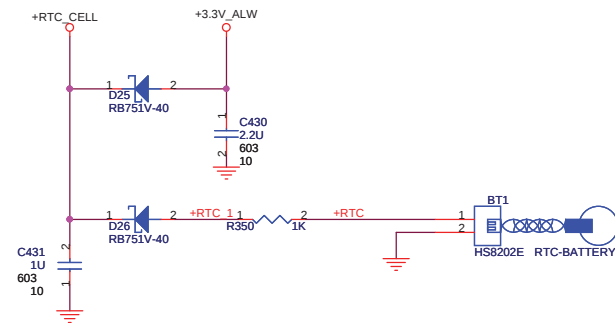
		QUANTA COMPUTER	
Title		black	
Size	Document Number VMBM		Rev 1A
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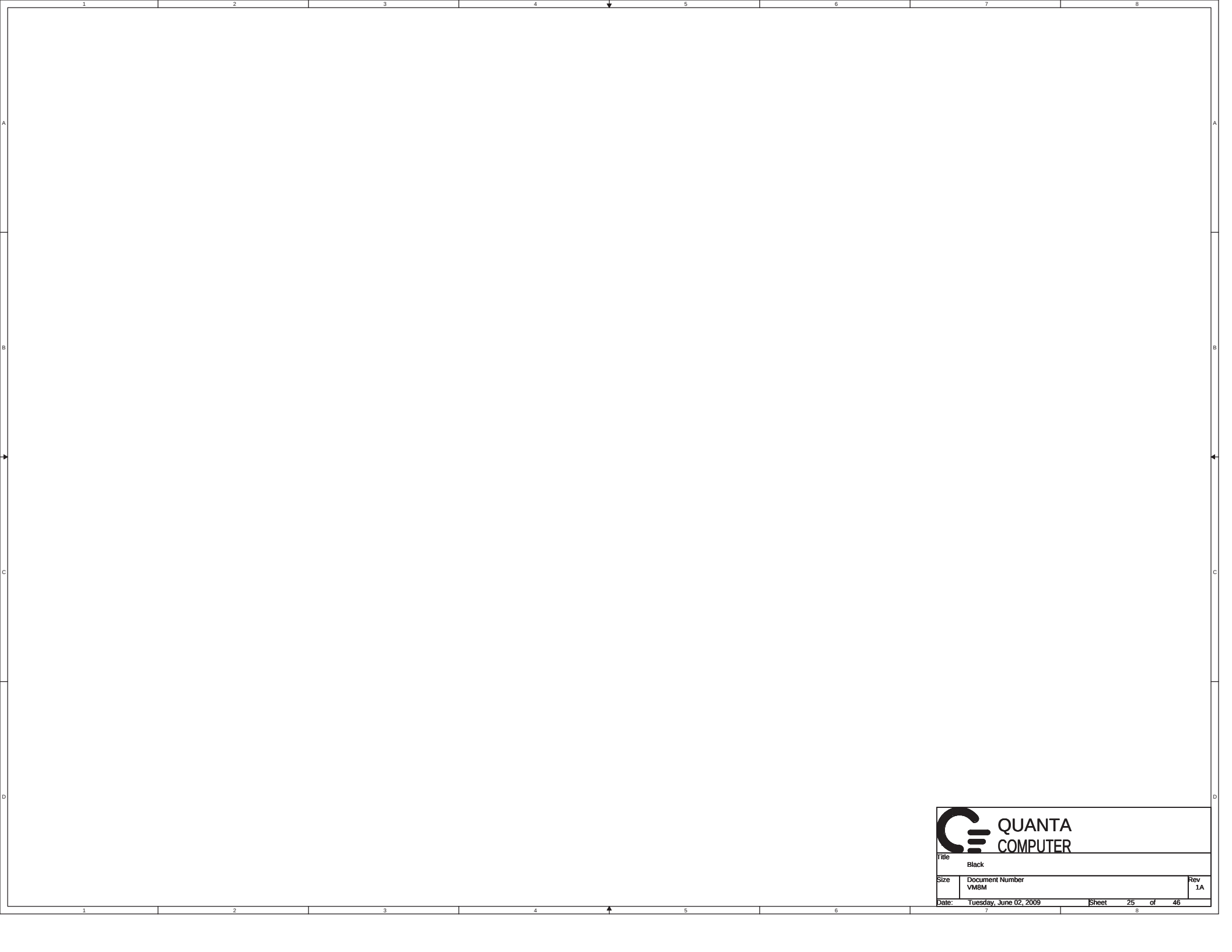


16Mbit (2M Byte), SPI



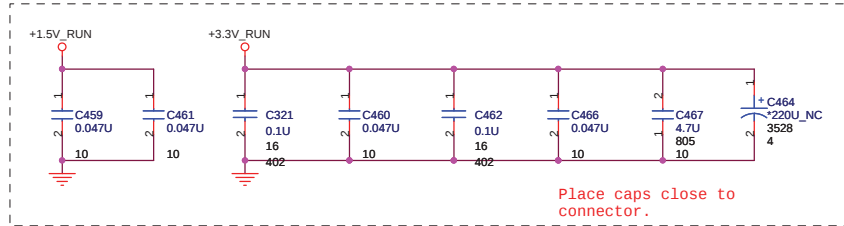
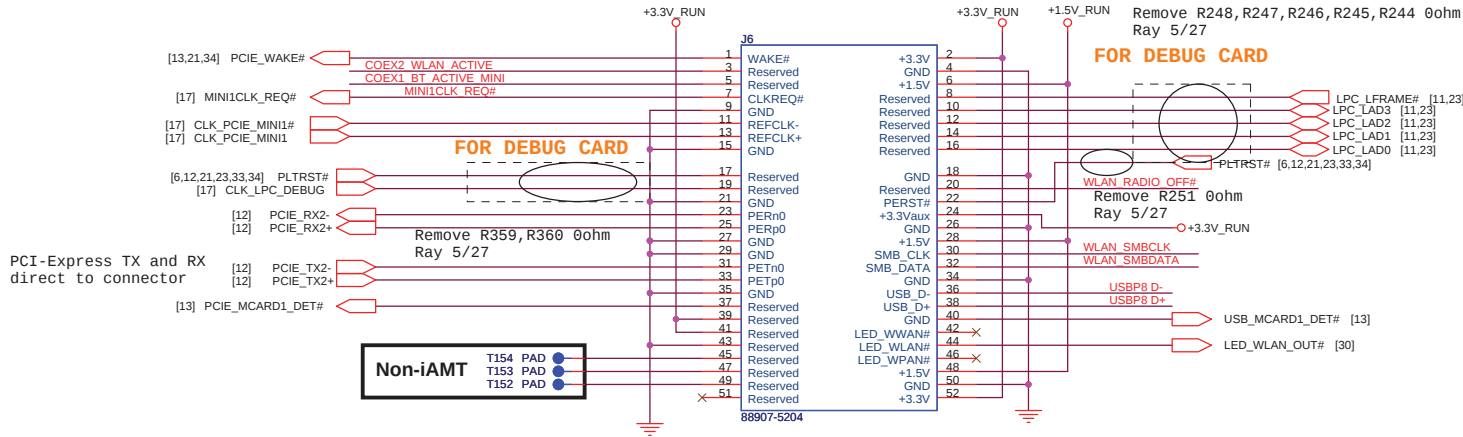
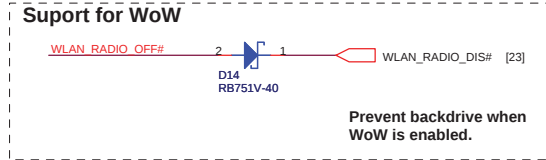
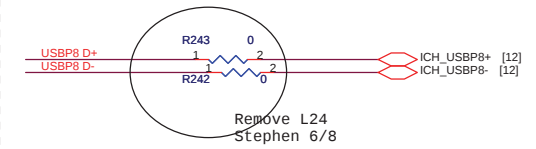
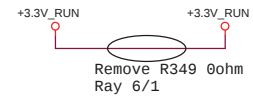
RTC BATTERY



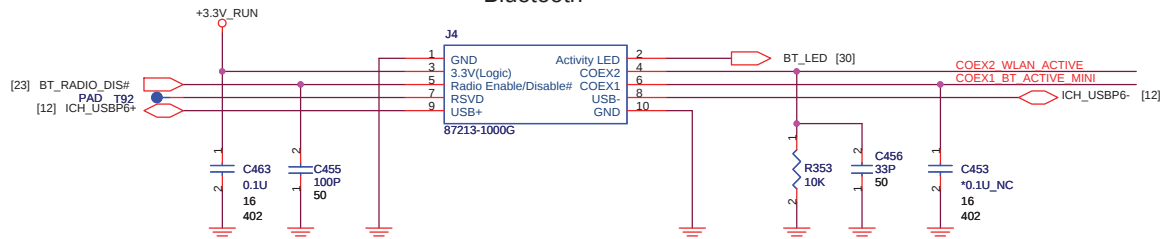


		QUANTA COMPUTER	
Title		Black	
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MiniCard WLAN connector

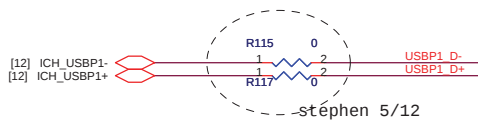
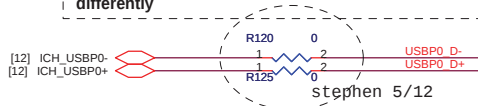


Bluetooth

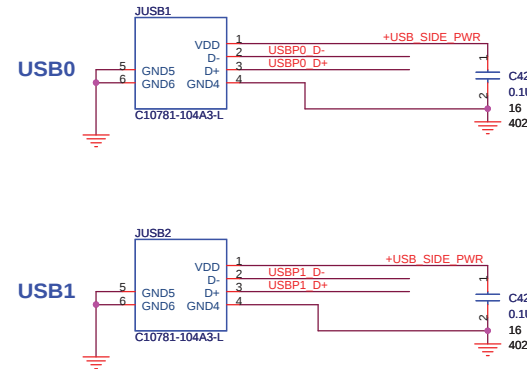
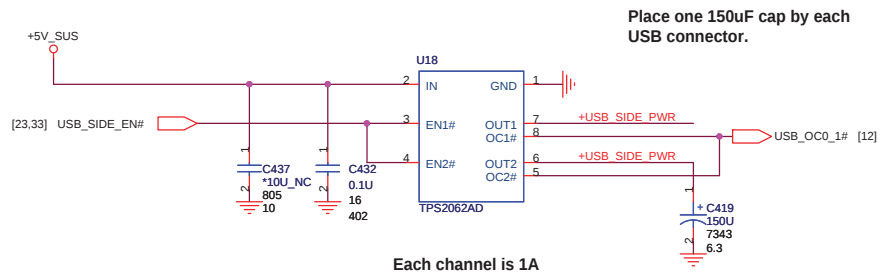


Title			
MDC CONN.			
Size	Document Number	Rev	
	VMSM	1A	
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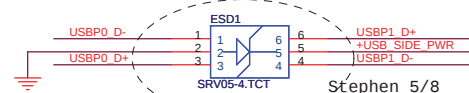
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



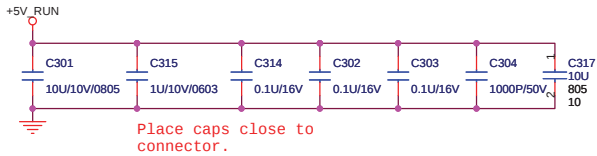
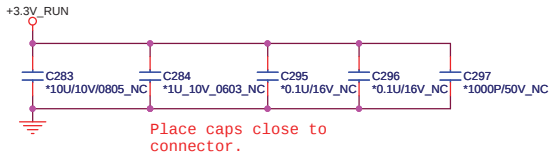
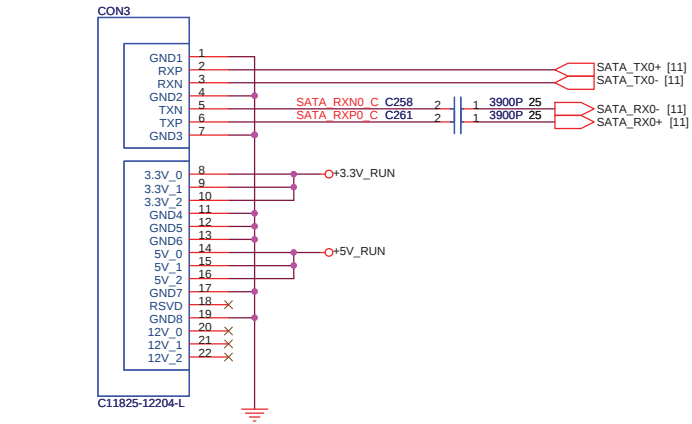
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



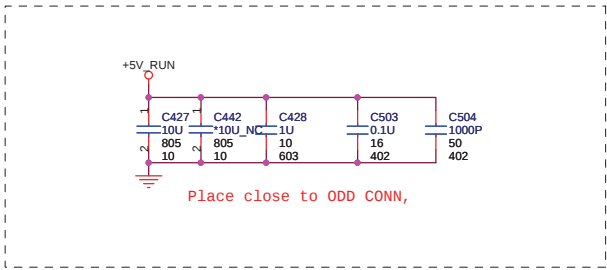
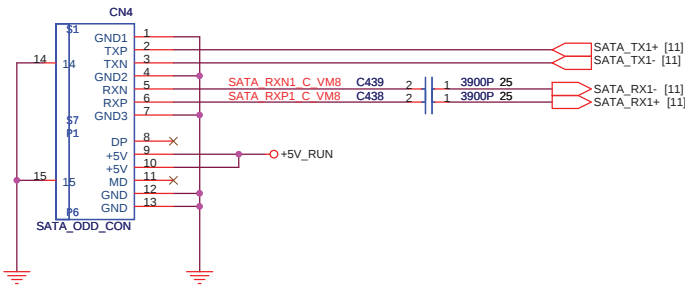
Place ESD diodes as close as USB connector.



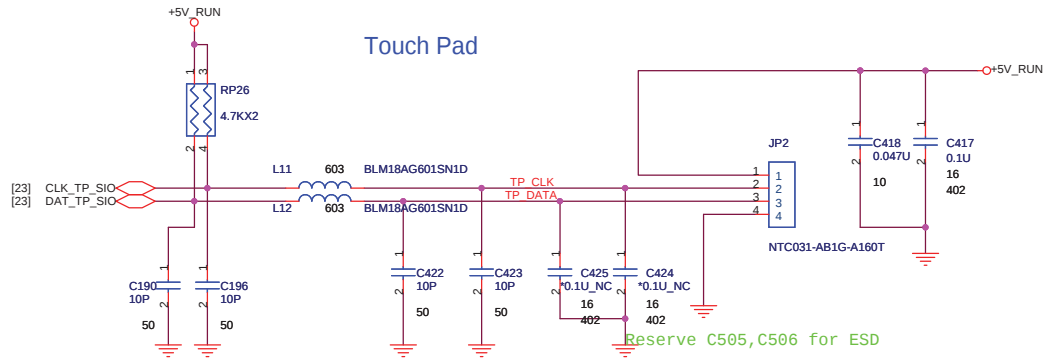
SATA HDD Connector.



SATA ODD Connector.

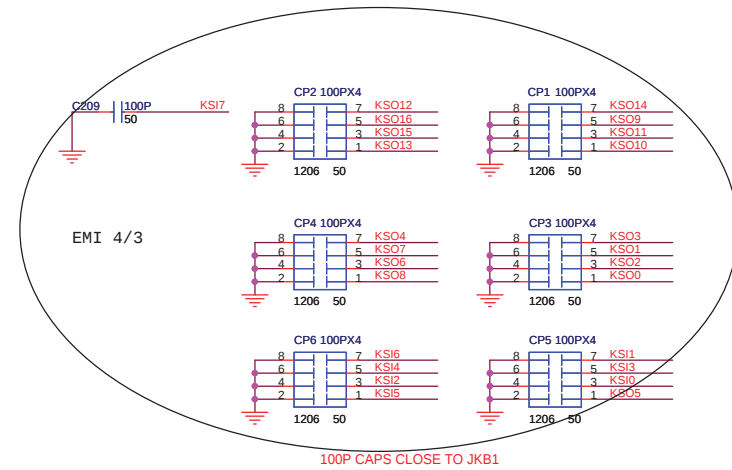
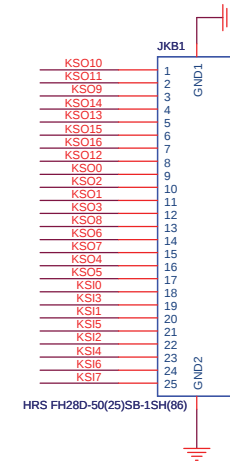


Touch Pad



KEYBOARD CONNECTOR

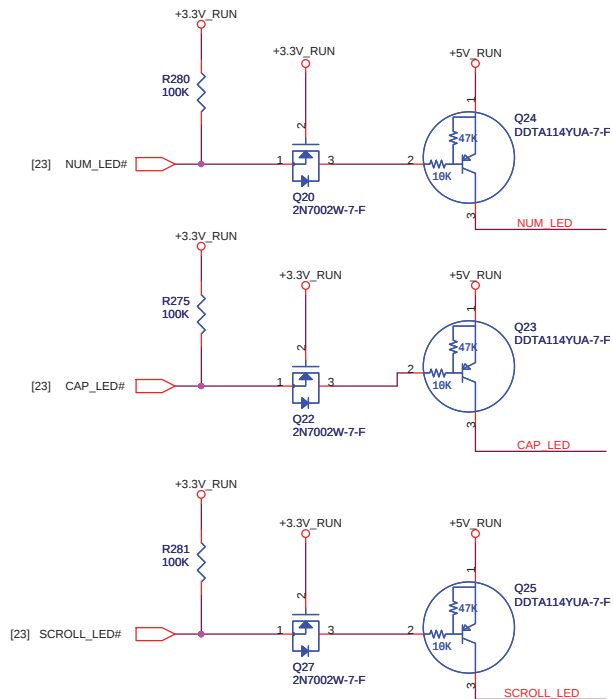
[23] KSO[0..16]
[23] KSI[0..7]



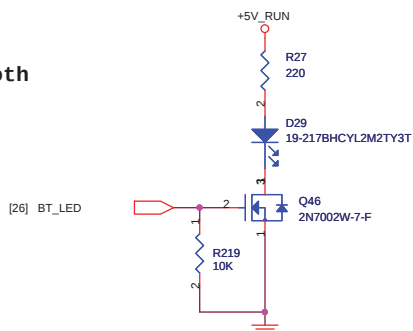
QUANTA
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Title		TOUCH PAD, BULE TOOTH & FIR
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Keyboard LED

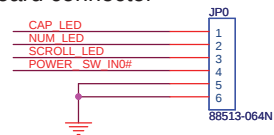


Bluetooth

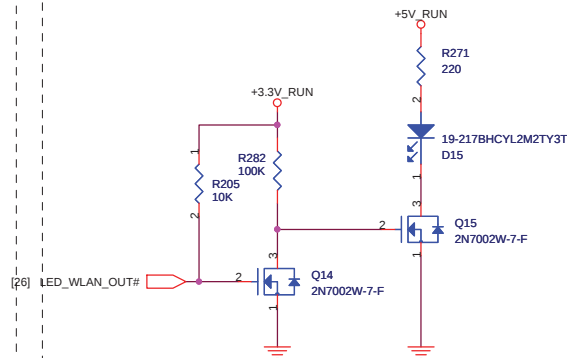


Dash board connector

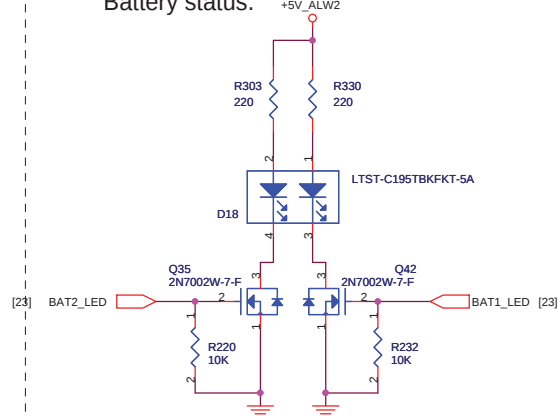
Keyboard LED



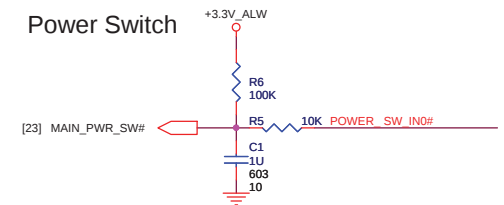
WLAN



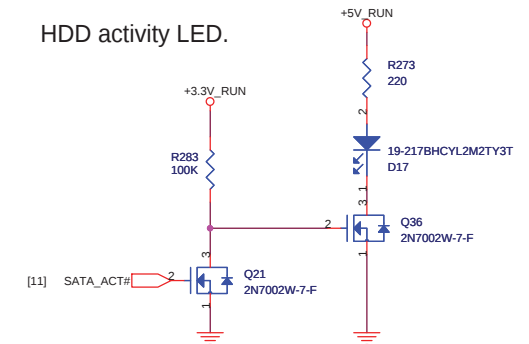
Battery status.



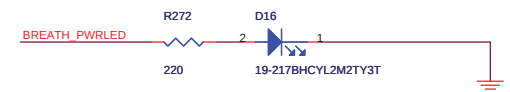
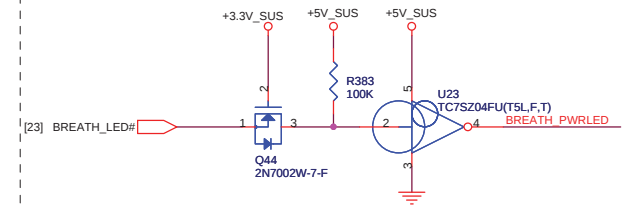
Power Switch



HDD activity LED.



Power & Suspend.



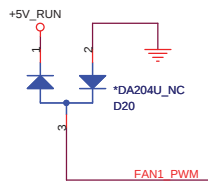
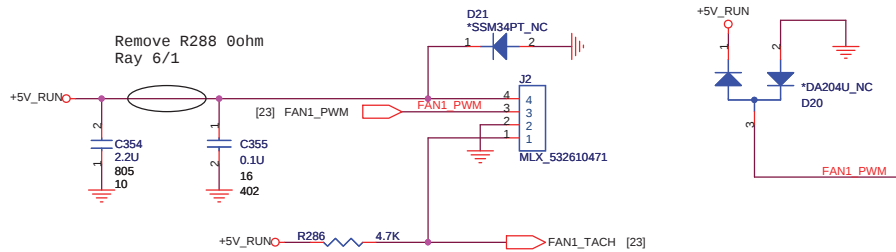
File
SWITCH, KEYBOARD & LED

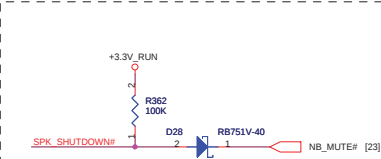
Size
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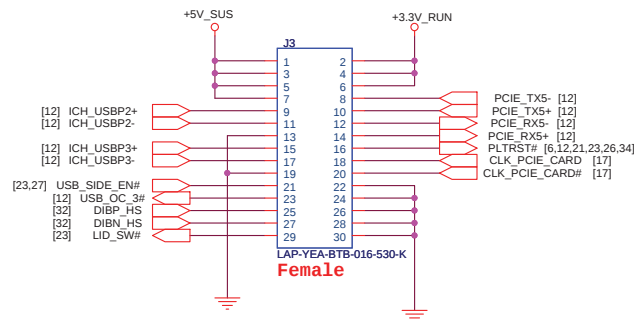
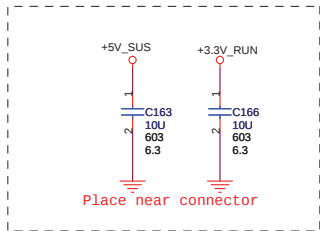


Schematic diagram of the HP_JD output stage. It shows a differential pair of NMOS transistors Q10 and Q11, both 2N7002W-7-F. The gates are tied together and driven by a common gate voltage. The sources are connected to ground. The drains are connected to a common drain voltage through resistors R268 (20K/F) and R267 (39.2K/F). The output of Q11 is HP_JD. A sense resistor R374 (5.1K/F) is connected between SENSEA and +3.3V_RUN.

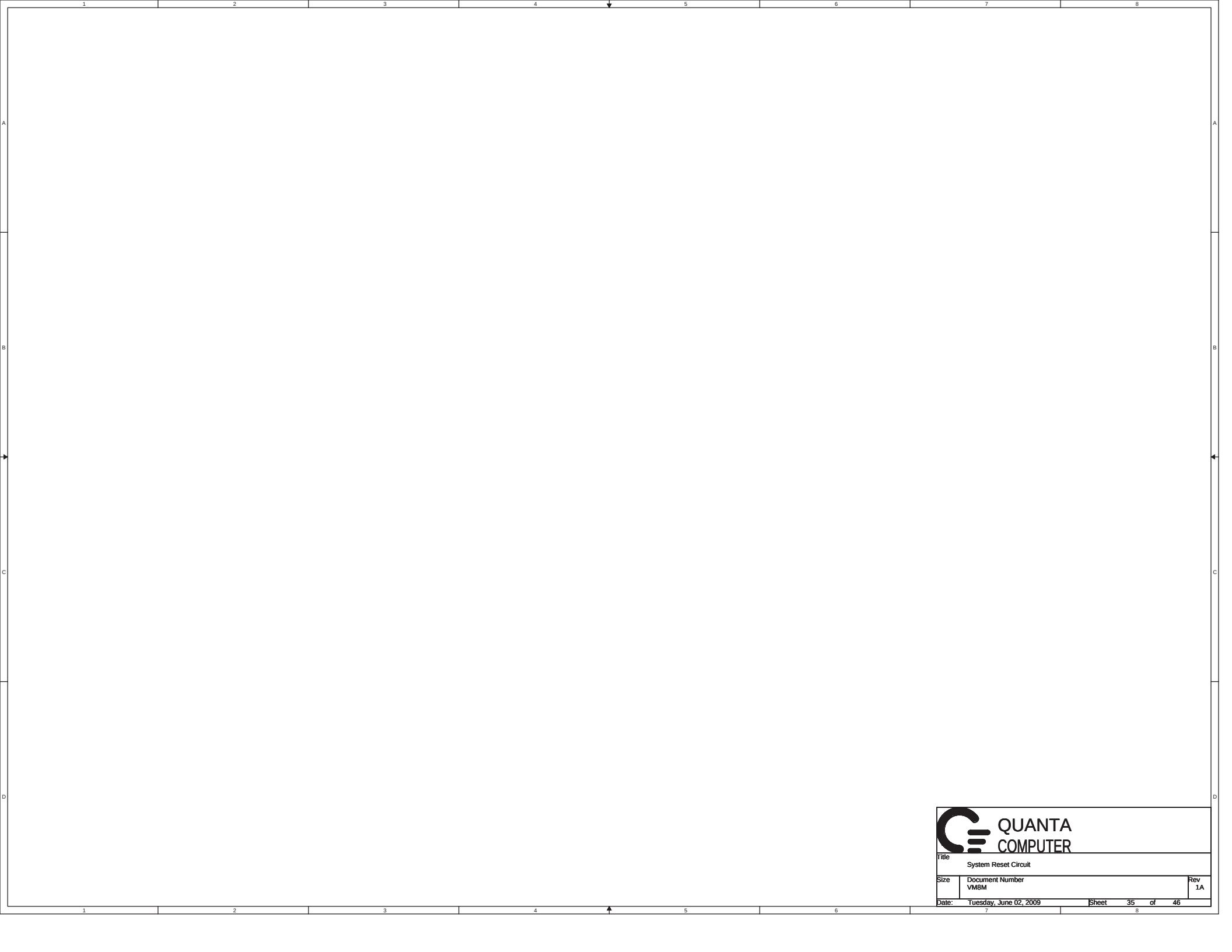
Circuit diagram for the speaker output. It shows two parallel paths. The top path consists of a 1uF capacitor (C483) in series with a 10K resistor (R338), connected to a speaker terminal labeled BEEP. The bottom path consists of a 1uF capacitor (C502) in series with a 10K resistor (R339), connected to a speaker terminal labeled SPKR. Both paths are driven by the AUD_PC_BEEP signal.



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Board to board connector (Modem Card + Cardreader+1394a+ 2 USB Port)



		QUANTA COMPUTER	
Title System Reset Circuit			
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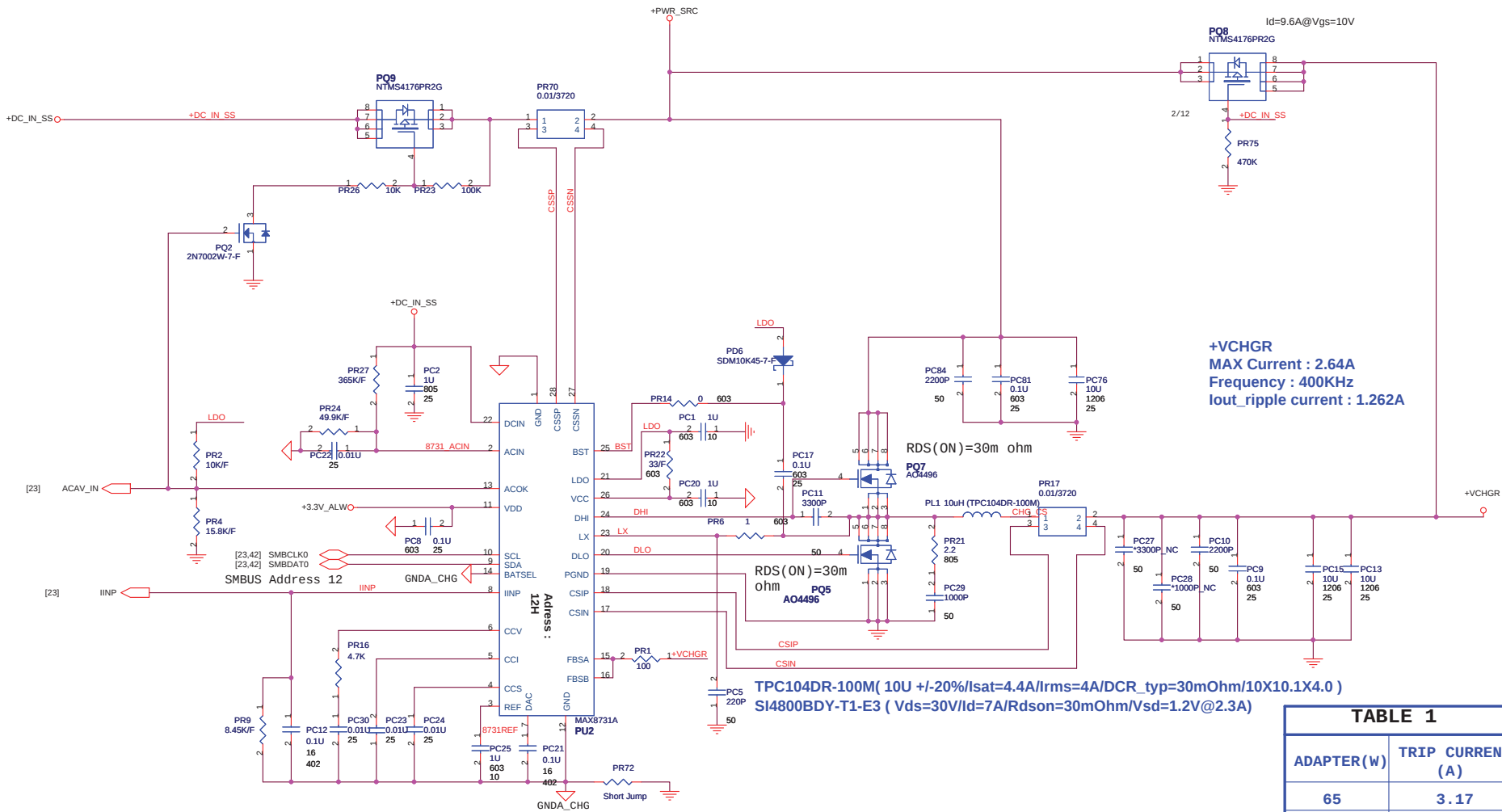
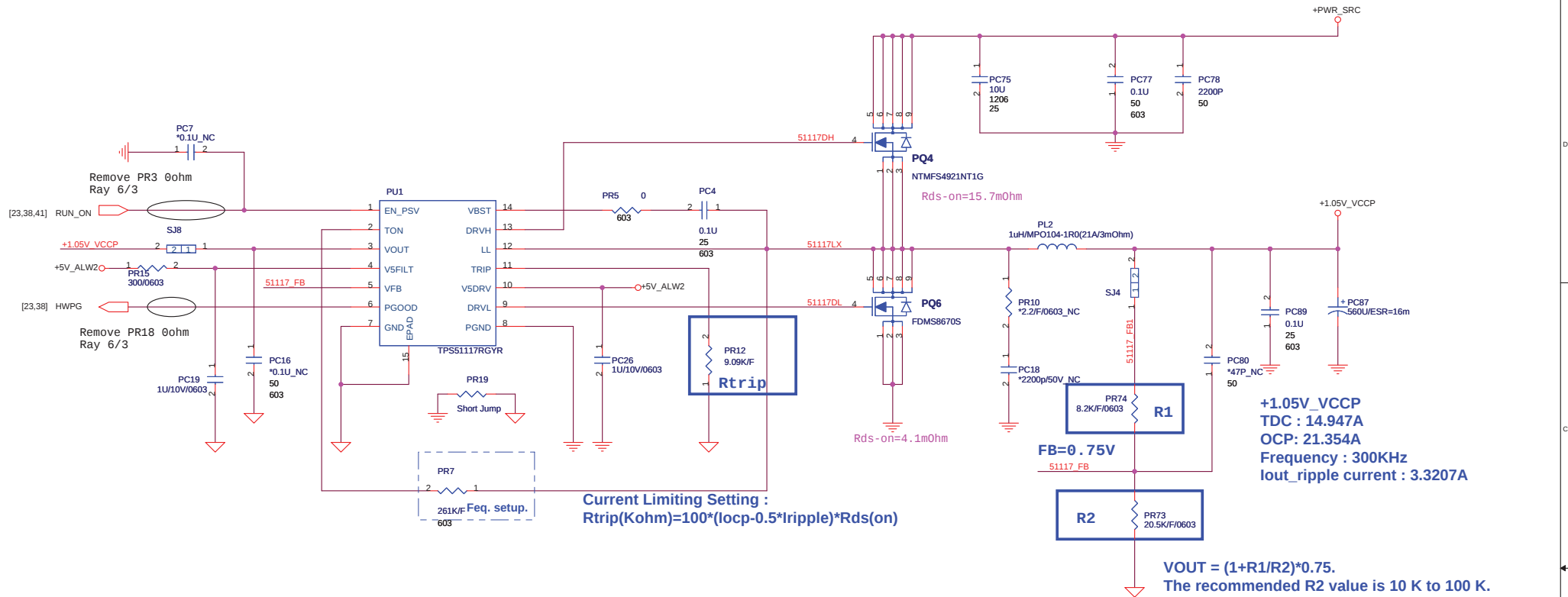


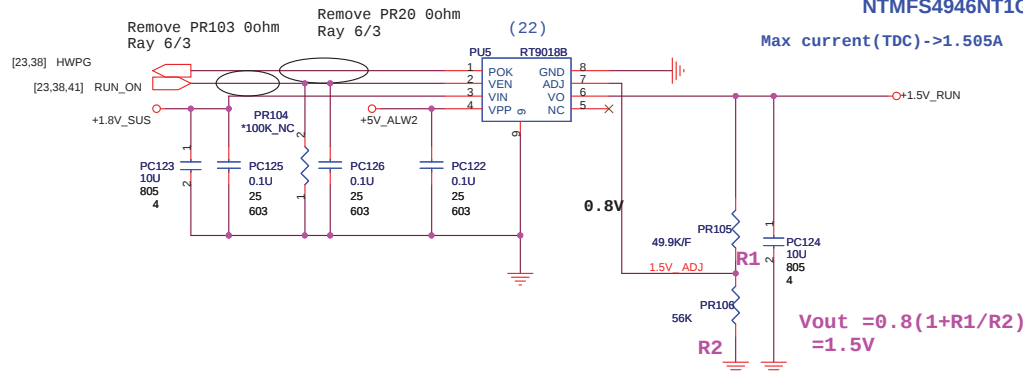
TABLE 1	
ADAPTER(W)	TRIP CURRENT (A)
65	3.17
90	4.43
130	6.43
150	7.43
200	9.75
230	11.28

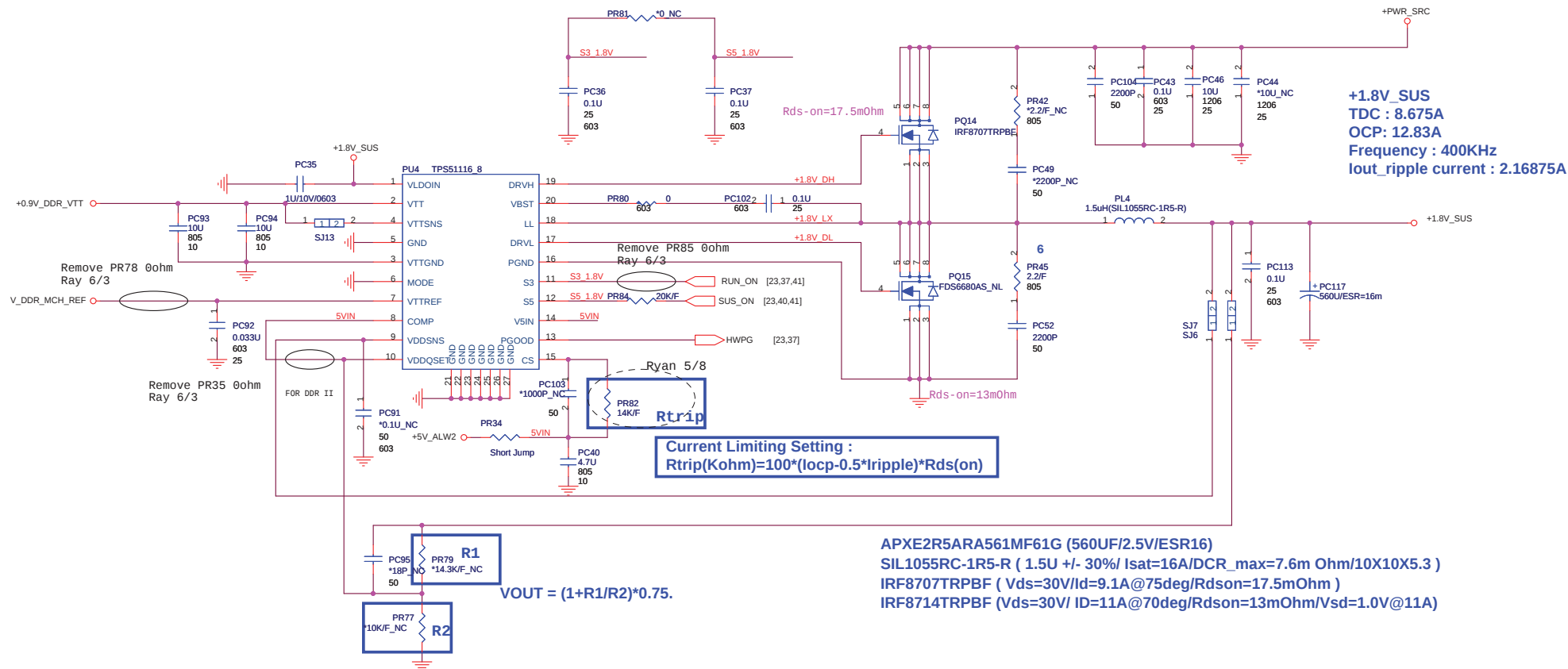


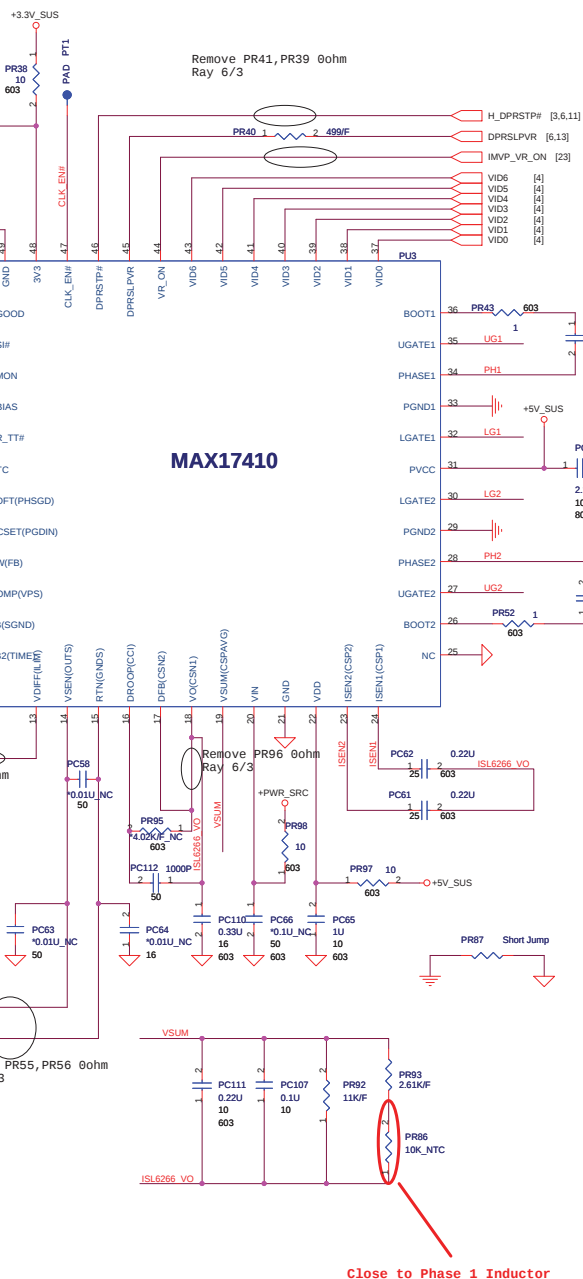
APXE2R5ARA561MF61G (560UF/2.5V/ESR16)
MPO104-1R0 (1.0U +/- 20% Isat=30A/DCR_max=3m Ohm/11.5X10X4)

NTMFS4921NT1G (Vds=30V/Id=10.2A@85deg/Rdson=10.5mOhm)
NTMFS4946NT1G (Vds=30V/ ID=14.6A@85deg/Rdson=5.1mOhm/Vsd=1.0V@30A)

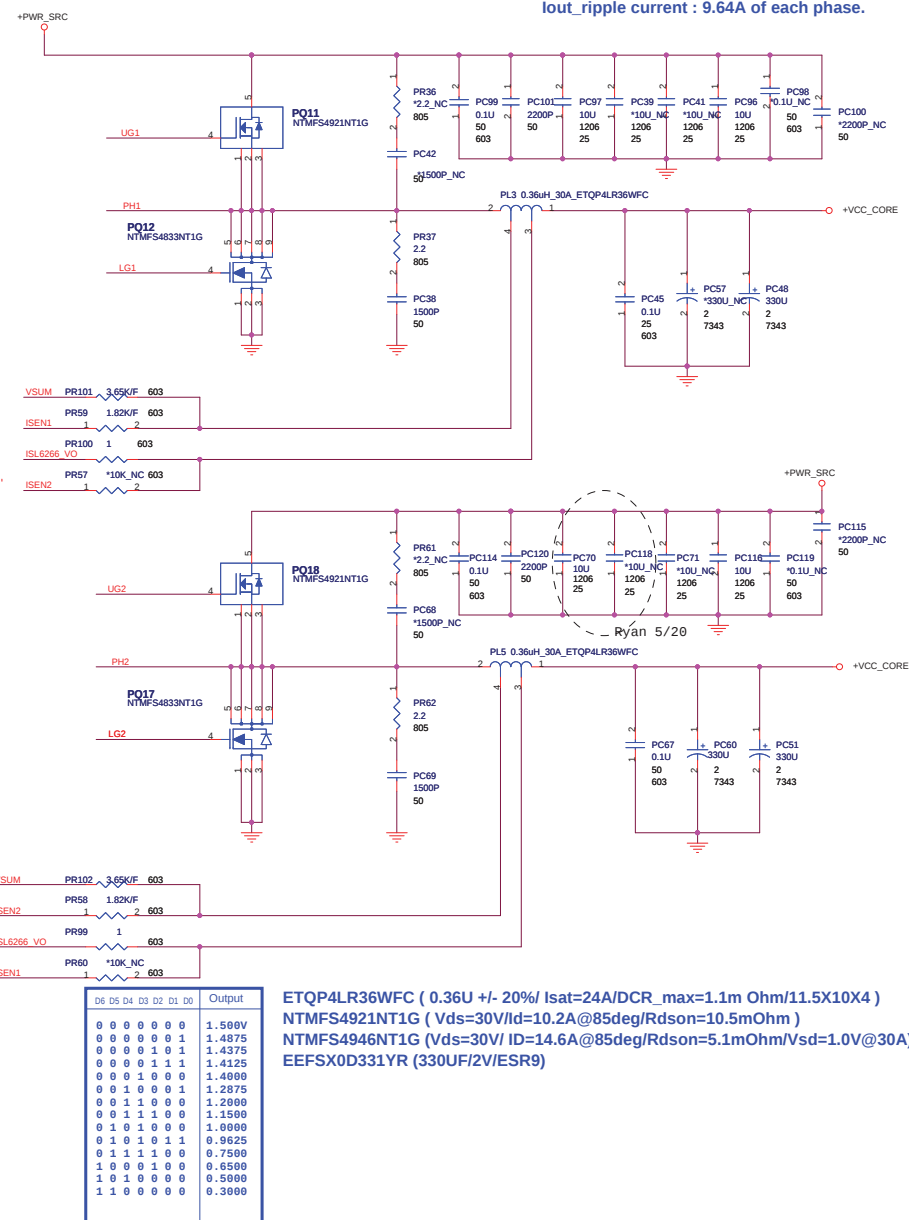
Max current (TDC) -> 1.505A







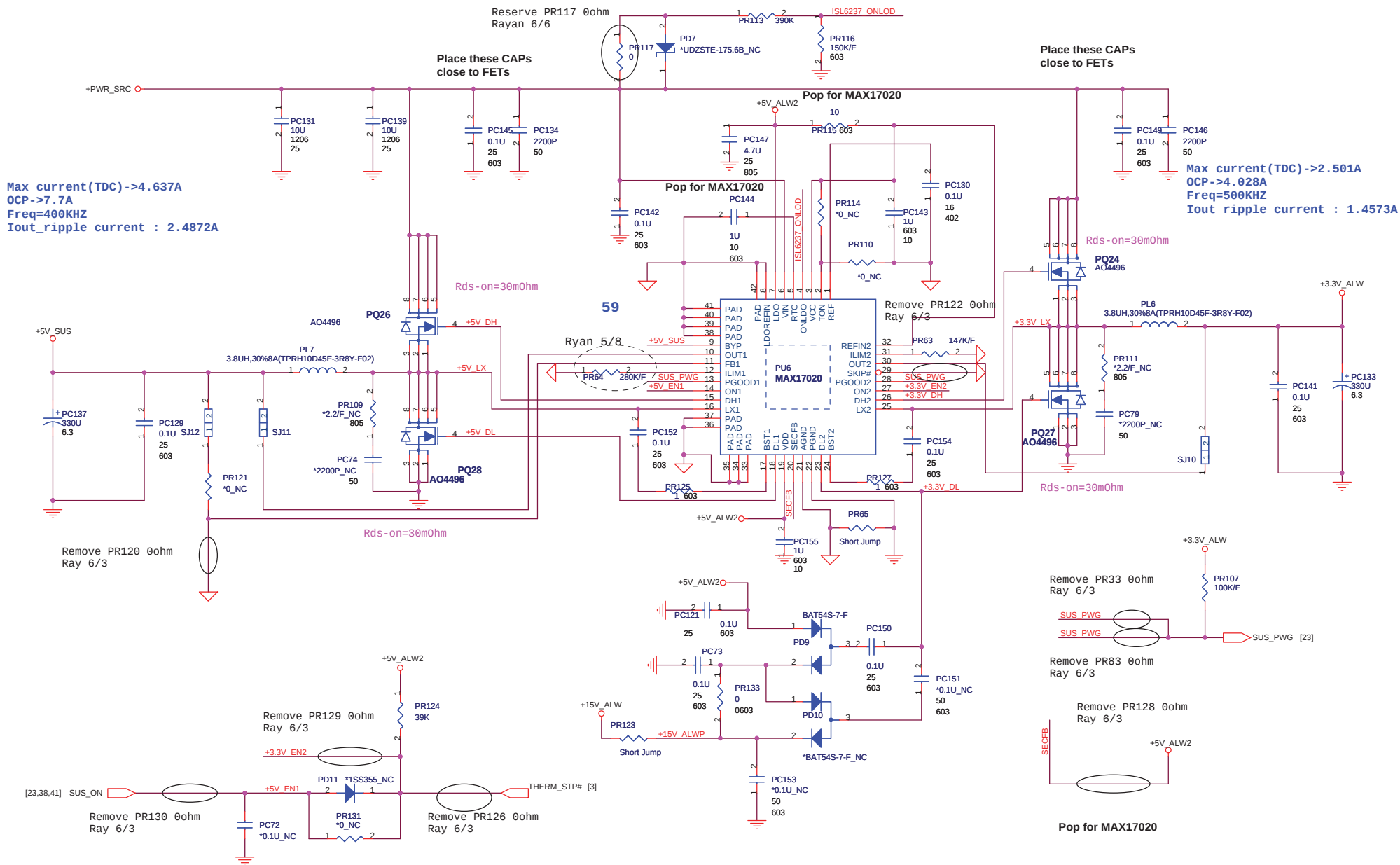
+VCC_CORE
TDC : 35A
MAX:47A
Frequency : 300KHz
Iout ripple current : 9.64A of each phase.



D6	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	0	1.500V
0	0	0	0	0	0	1	1.4875
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	1	0	0	0	1	1.2875
0	0	1	1	0	0	0	1.2000
0	0	1	1	1	0	0	1.1500
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	1	1	0.9625
0	1	1	1	1	0	0	0.7500
1	0	0	0	1	0	0	0.6500
1	0	1	0	0	0	0	0.5000
1	1	0	0	0	0	0	0.3000

ETQP4LR36WFC (0.36U +/- 20%/ Isat=24A/DCR_max=1.1m Ohm/11.5X10X4)
NTMF54921NT1G (Vds=30V/Id=10.2A@85deg/Rdson=10.5mOhm)
NTMF54946NT1G (Vds=30V/ ID=14.6A@85deg/Rdson=5.1mOhm/Vsd=1.0V@30A)
EEFSX0D331YR (330UF/2V/ESR9)

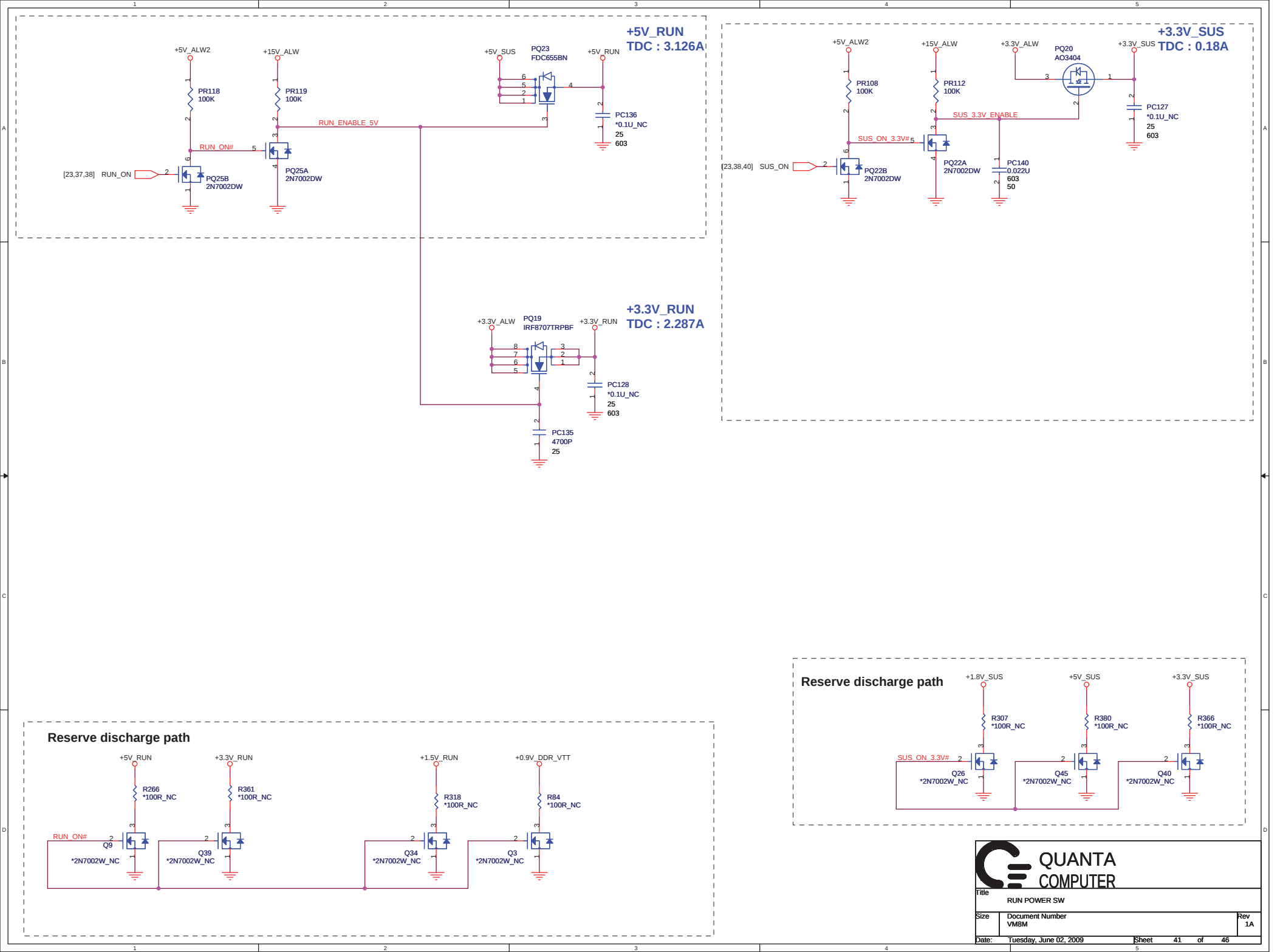
DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW

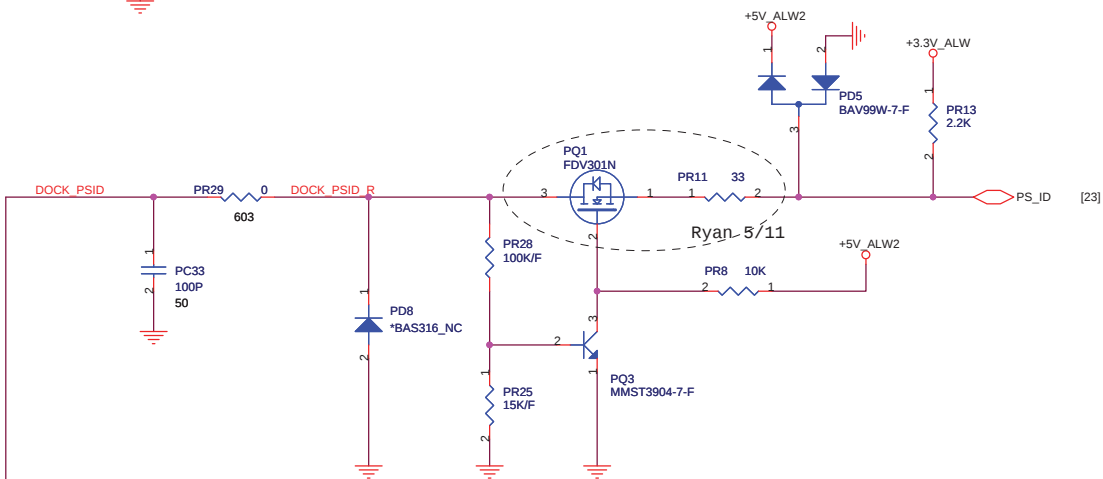
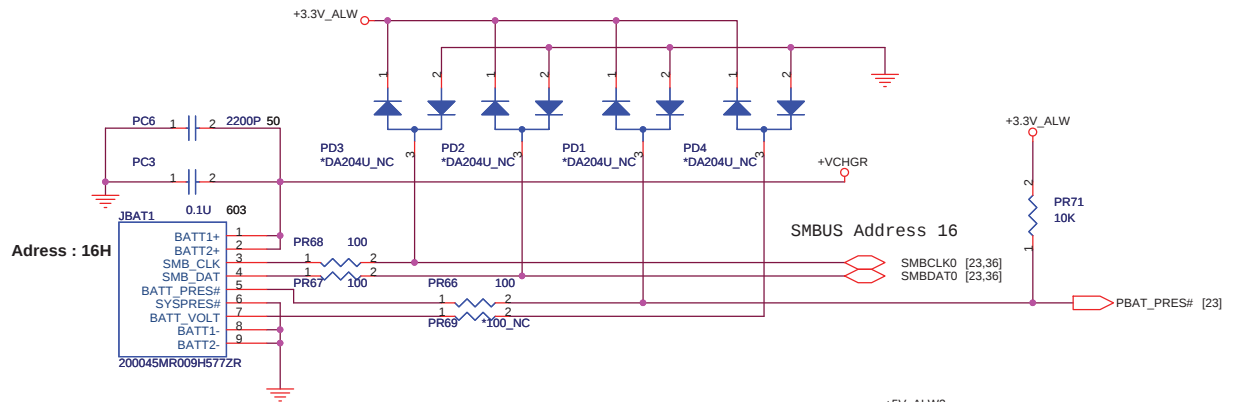


APXE6R3ARA331MF61G (330UF/6.3V/ESR17)
TPC104DR-3R8Y(3.8U +/- 30%/ Isat=6A/DCR_max=12m Ohm/10X10X4)
SI4800BDY-T1-E3 (Vds=30V/Id=7A/Rdson=30mOhm/Vsd=1.2V@2.3A)

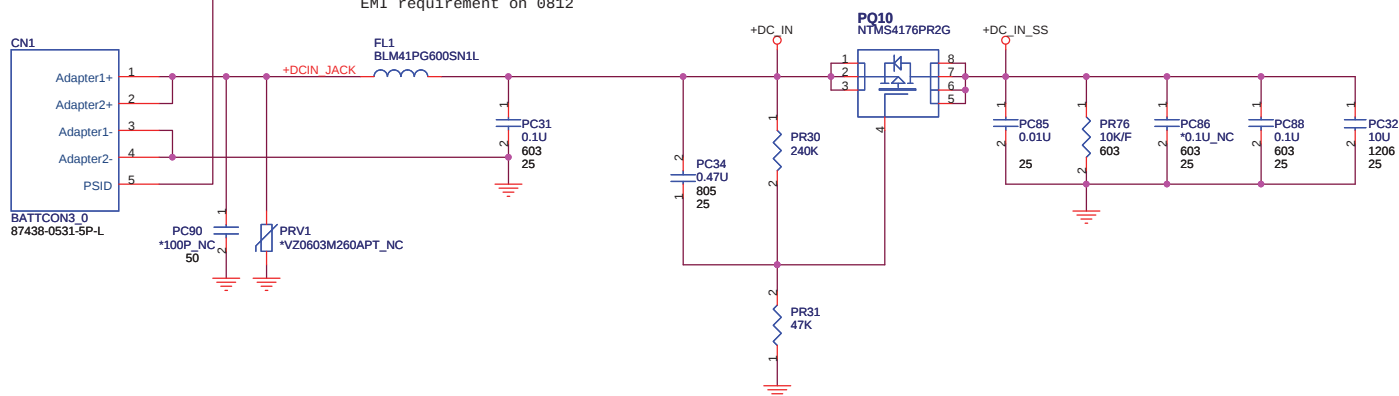


Title			
3VALW,5V,3V,(MAX17020)			
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	VMBM		1A
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Change Value per GG updated
EMI requirement on 0812



Title
DCIN,BATT CONNECTOR

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VM8M

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1A

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Reserved for EMI.

