

MODEL NAME : VBW00
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WK000 LA-9981P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

Dell / Compal Confidential

Schematic Document

Intel Shark Bay ULT
OAK Value2
UMA/DIS AMD Sun XT

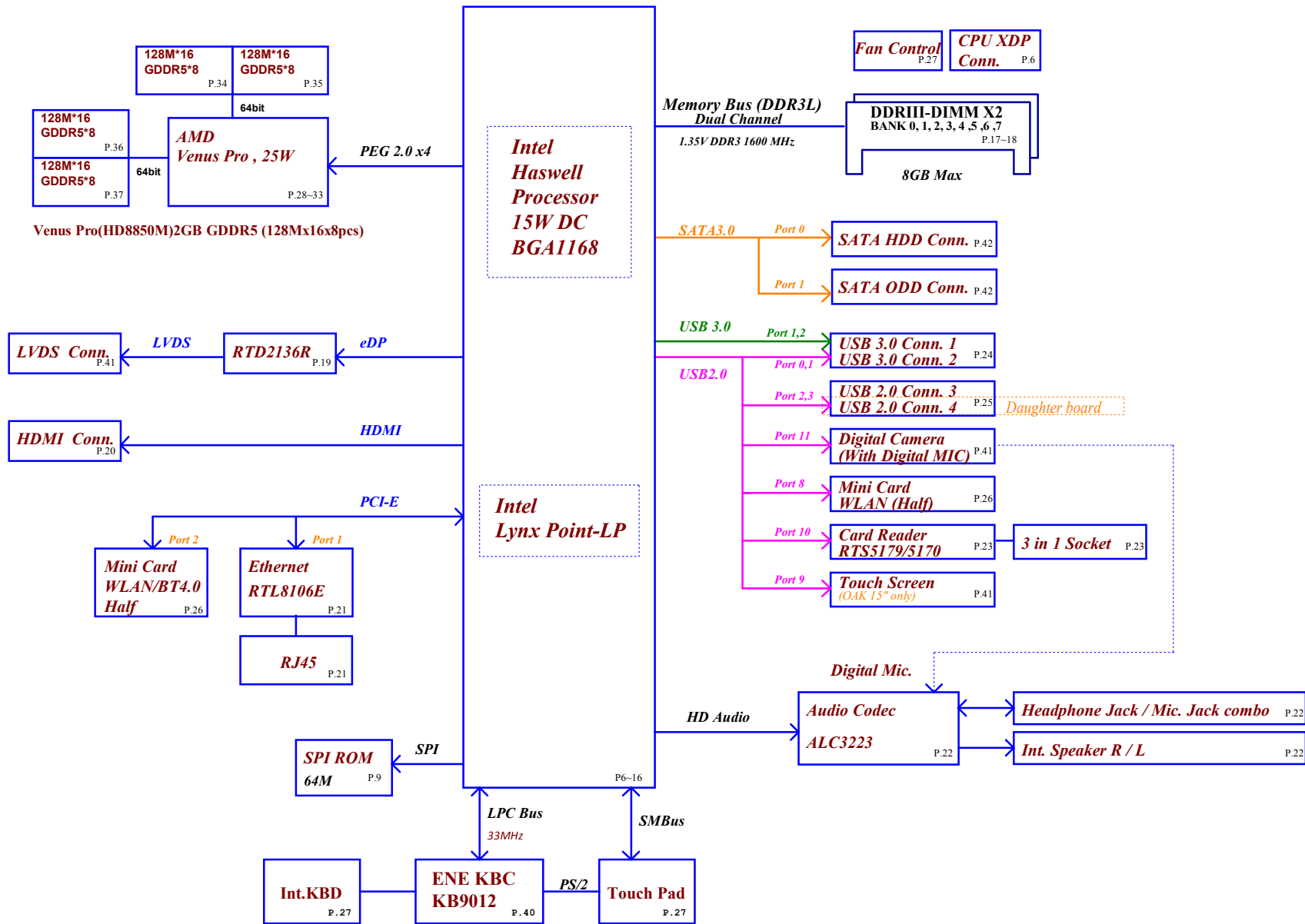
2013-03-09 Rev: 0.2

X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
SUN@ : SUN XT
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts

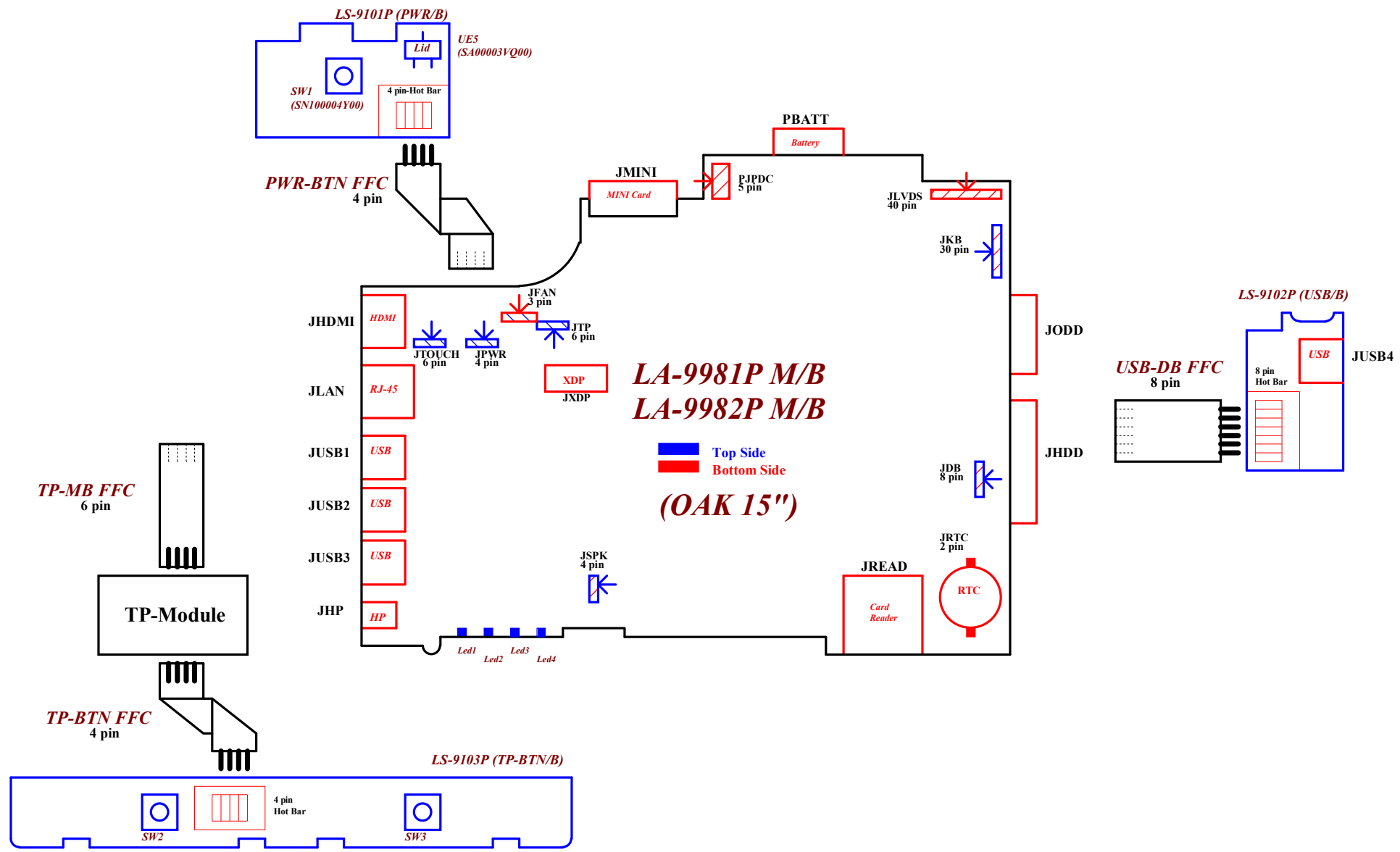
BOM config
UMA : UMA@,EMI@,ESD@,RF@,XDP@
DIS SUN : SUN@,DIS@,EMI@,ESD@,RF@,XDP@



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Project Code : VAW00 / VAW01
File Name : LA-9981P / LA-9982P



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								Size	Document Number			Rev		
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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SMLCLK SMLDATA	ULT								
SML1CLK SML1DATA	ULT								

Link

BOARD ID Table

ID	PCB Revision			
	UMA	Sun XT	Venus Pro	Venus XT
0	0.1			
1		0.1		
2			0.1	
3				0.1
4	0.2			
5		0.2		
6			0.2	
7				0.2
8	0.3			
9		0.3		
10			0.3	
11				0.3
12	1.0			
13		1.0		
14			1.0	
15				1.0

Symbol Note :



: means Digital Ground



: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU (N14P)
CLKOUT_PCIE5	

USB3.0	
Port1	USB connector 2
Port2	USB connector 1
Port3	
Port4	
USB2.0	
Port0	USB connector 2
Port1	USB connector 1
Port2	USB connector 3
Port3	USB connector 4 (DB)
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (N14P)
Lane 6	PEG (N14P)
SATA	
SATA0	HDD
SATA1	ODD
SATA2	
SATA3	

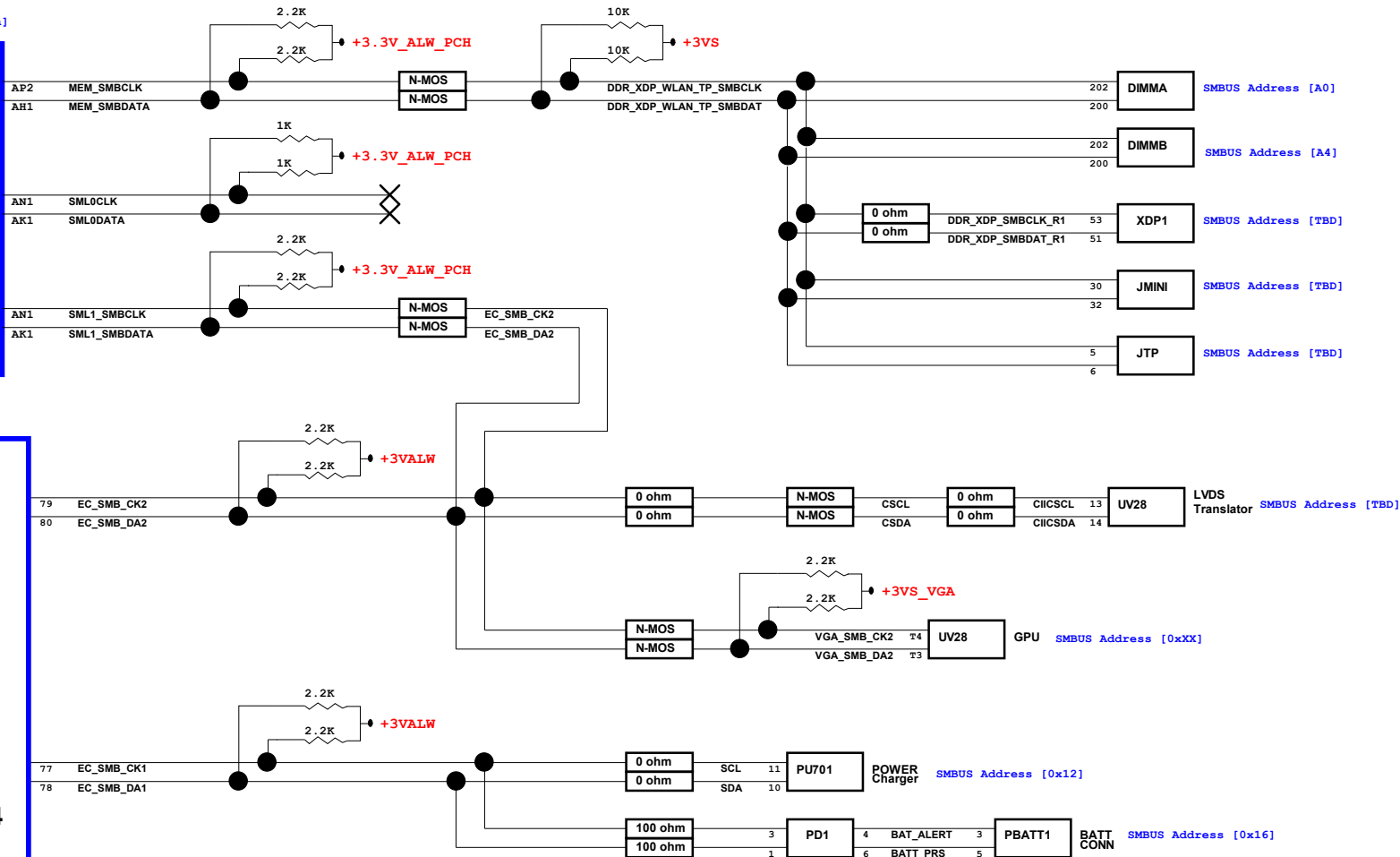
ULT

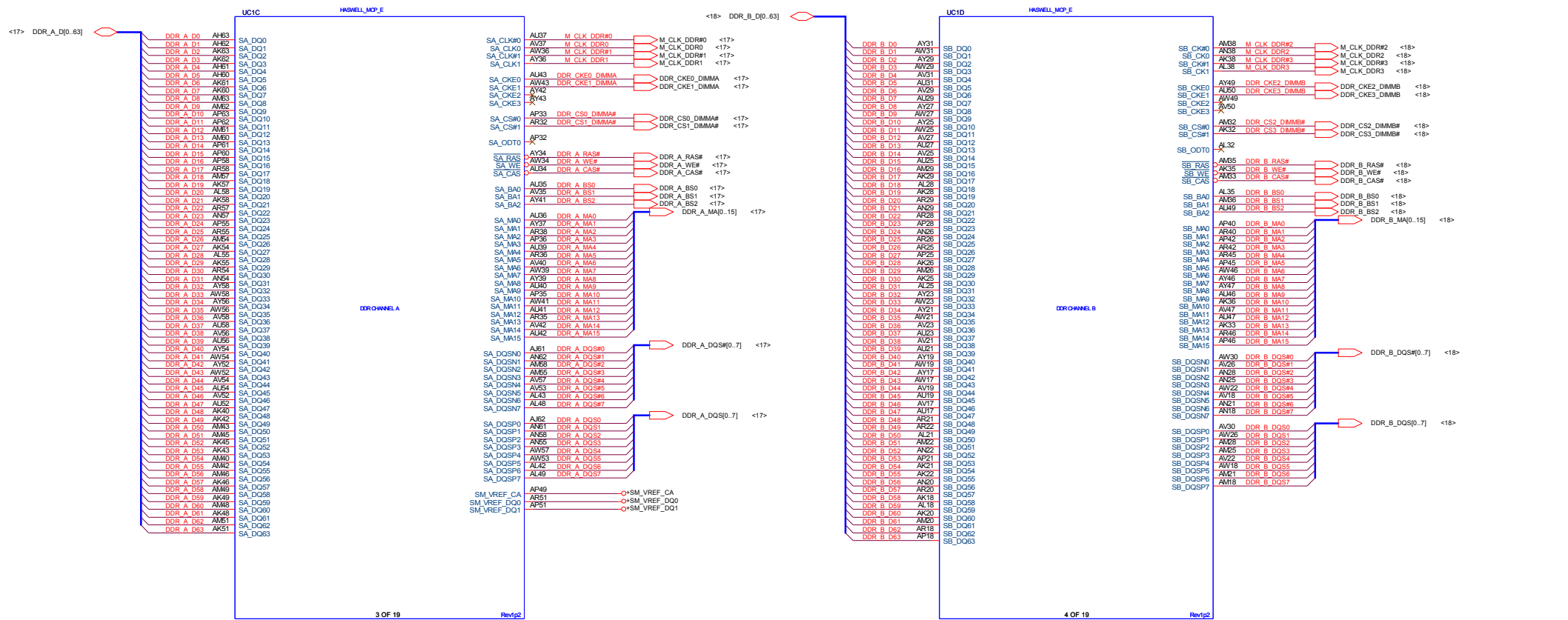
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SMBUS Address [0x9a]

MCH
Shark bay

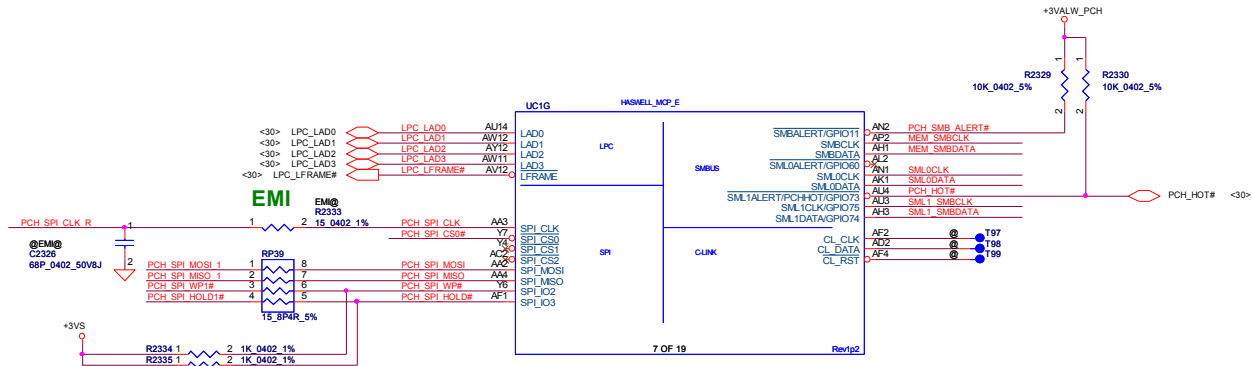
KBC
KB9012A4



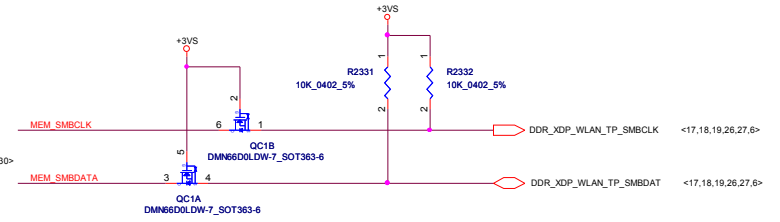


confirm by intel request PDG P141

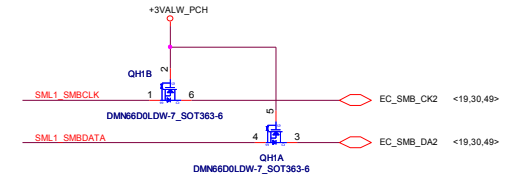
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Issued Date	2013/03/09	Deciphered Date	2014/04/01	MCP(3,4/19) DDR3	
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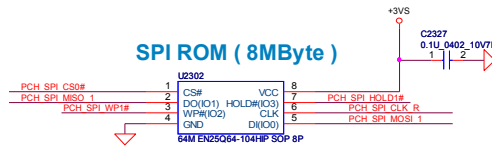
MEM Bus : DDR/XDP/WLAN/TP



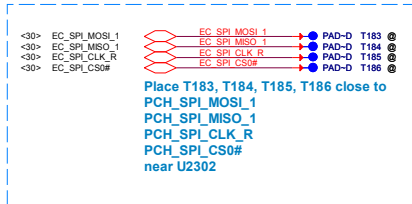
SML1 Bus : EC/Sensors



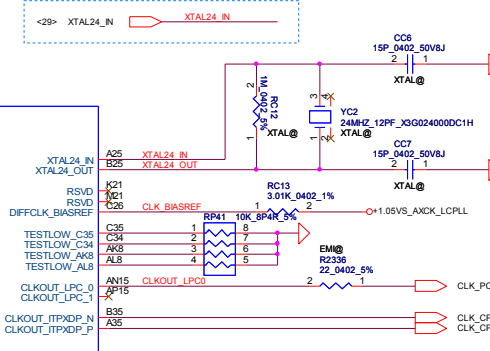
SPI ROM (8MByte)



PN : SA000046400 ,64M,EN25Q64-104HIP



For GCLK



10/100 LAN ----->

WLAN (Mini Card) ---->

dGPU ---->

<21> CLK_PCIE_LAN#

<21> CLK_PCIE_LAN

<21> LAN_CLKREQ#

<26> CLK_PCIE_WLAN#

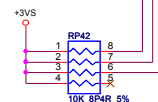
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<26> WLAN_CLKREQ#

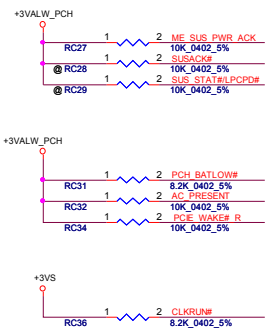
<48> CLK_PEG_VGA#

<48> CLK_PEG_VGA

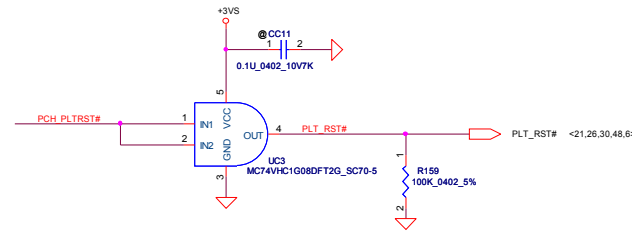
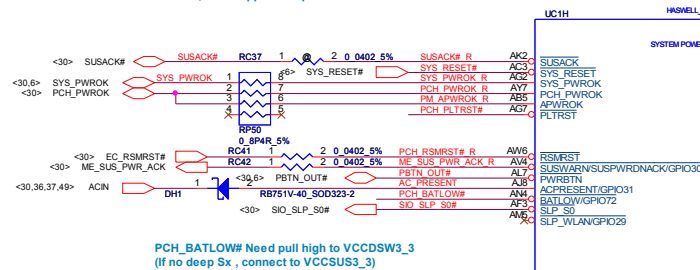
<49> CLK_PEG_VGA



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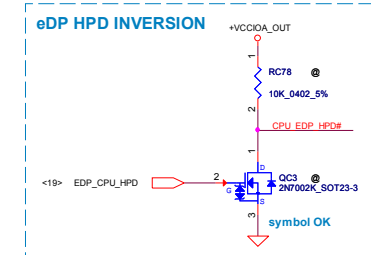
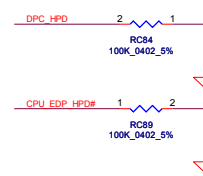
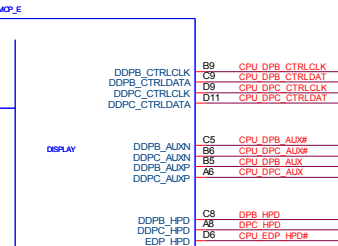
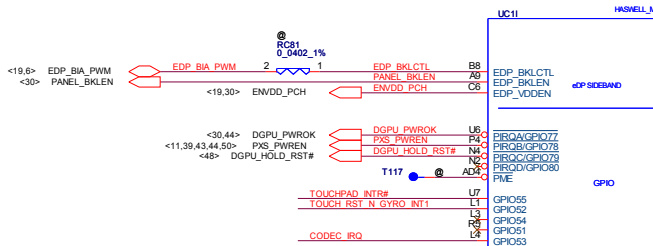
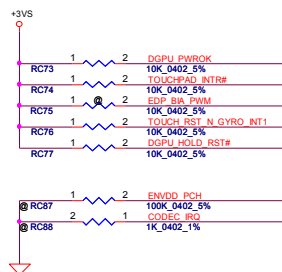
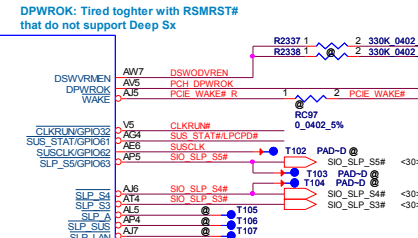
Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit CAN be NC ,if not support Deep Sx



DSWODVREN - On Die DSW VR Enable
* H : Enable(DEFAULT)
L : Disable

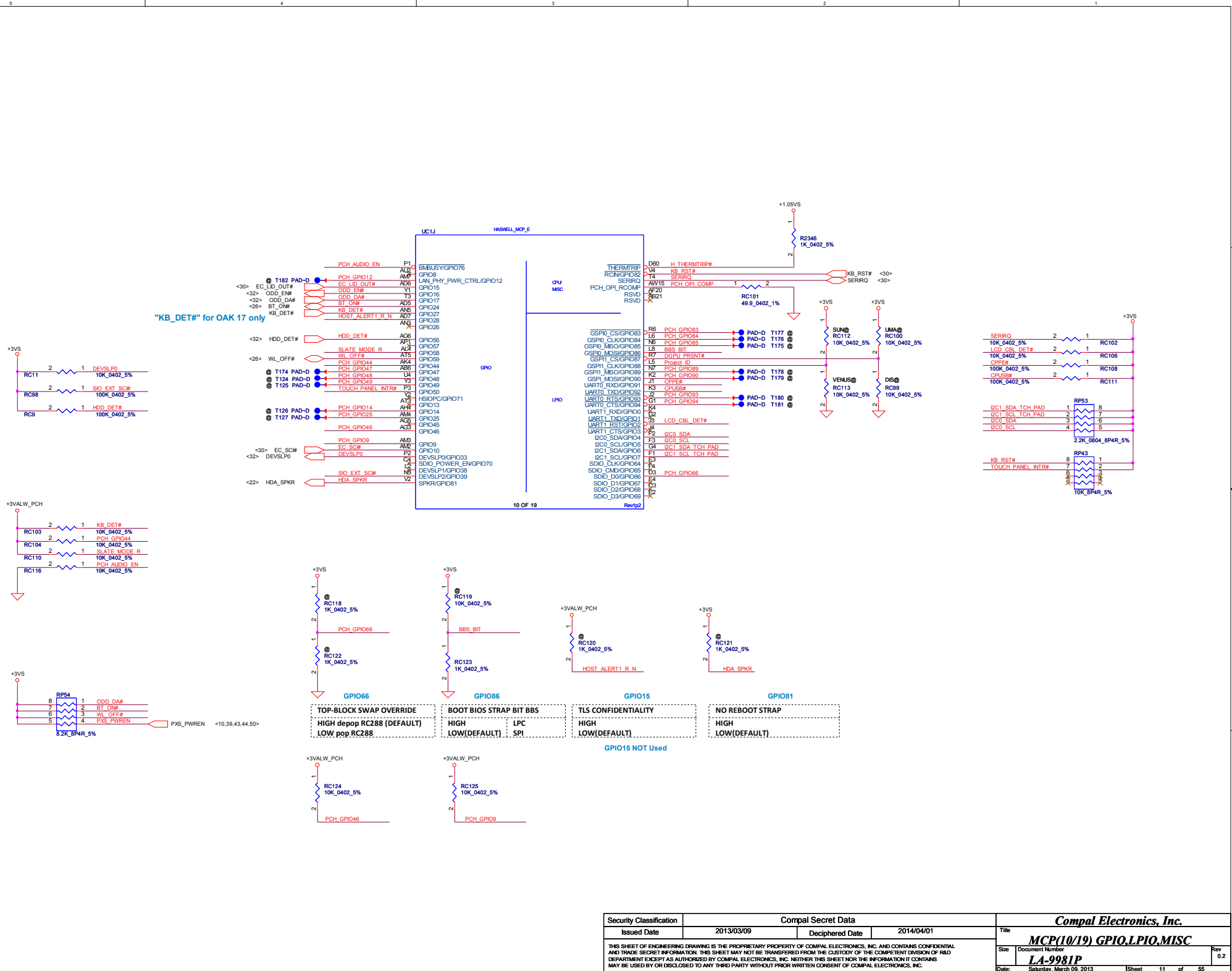
DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED

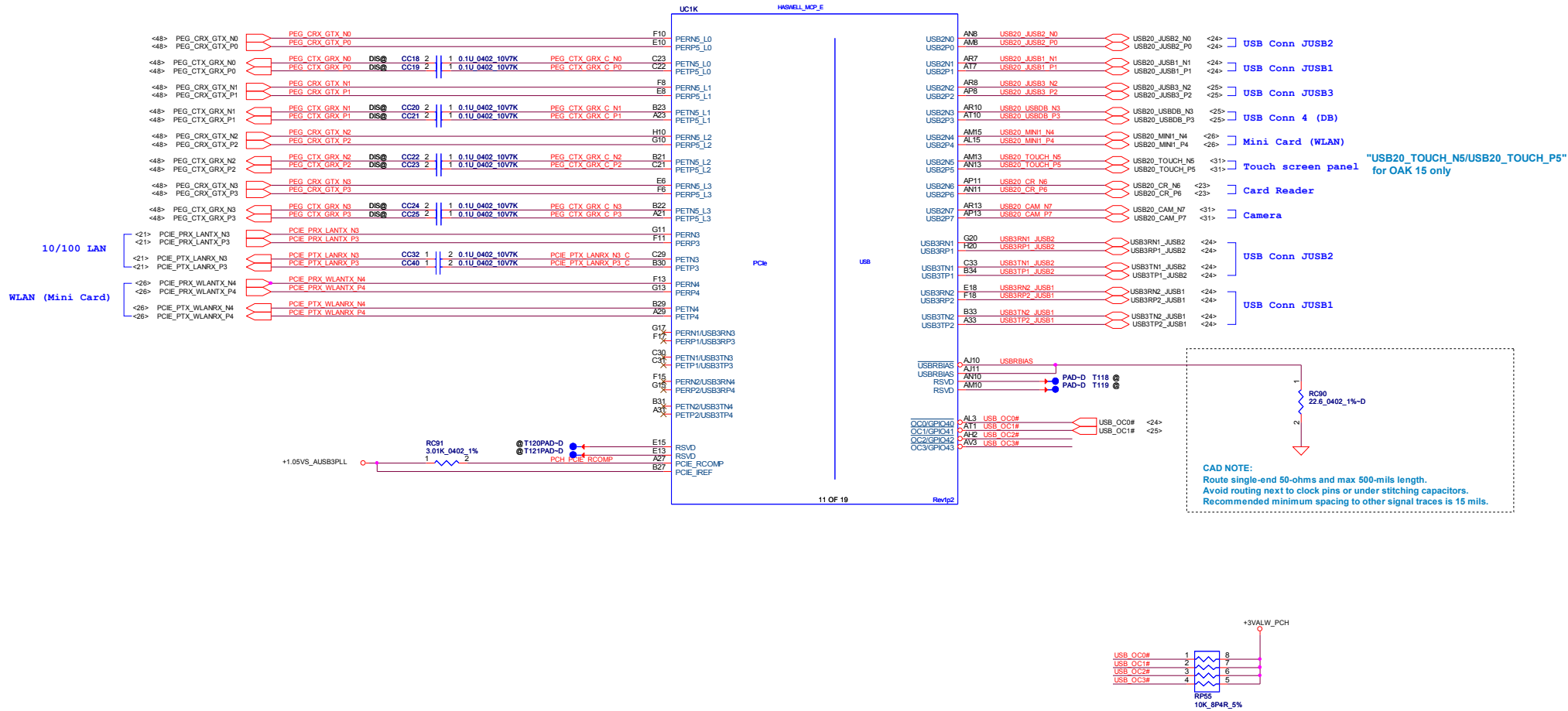
DPWROK: Tired together with RSMRST# that do not support Deep Sx



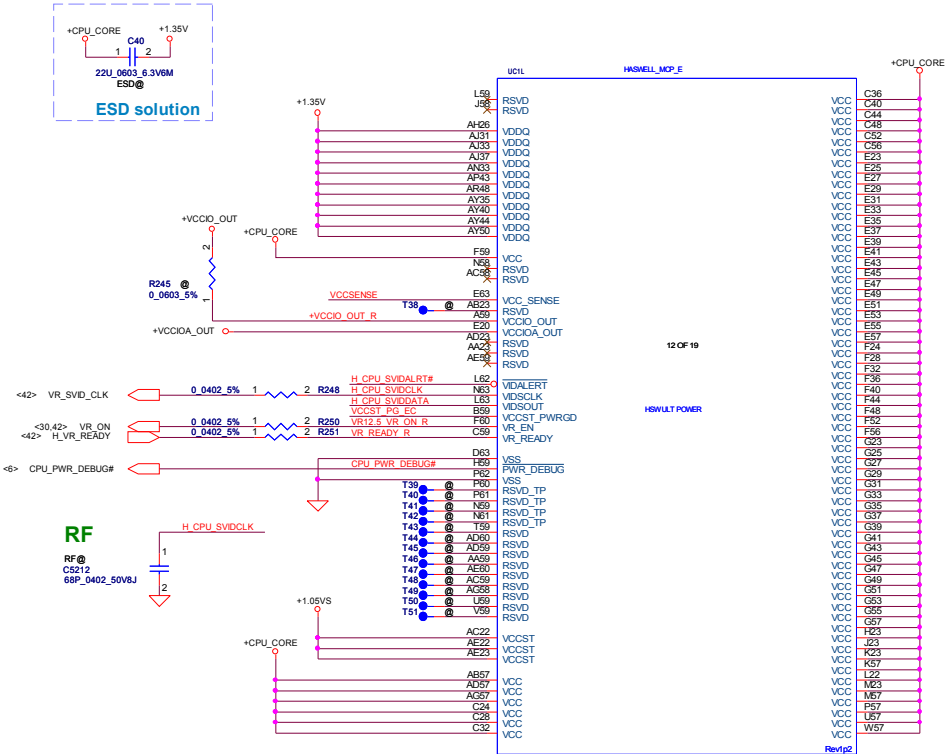
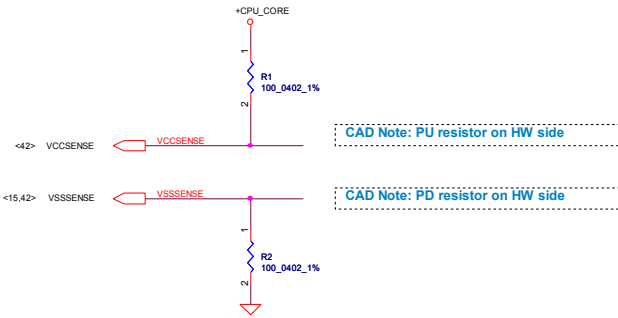
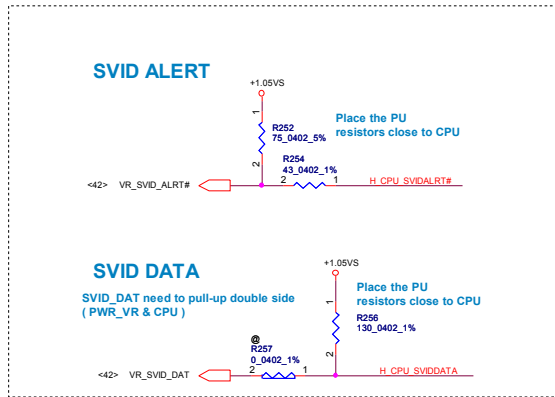
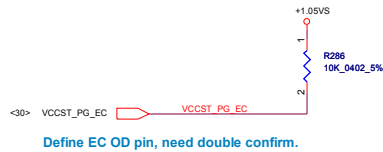
EDP_CPU_HPDI 1 2 CPU_EDP_HPDI# 0_0402_5% Reserve for debug

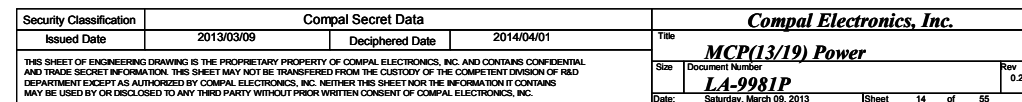
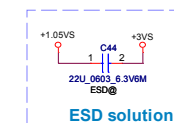
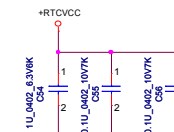
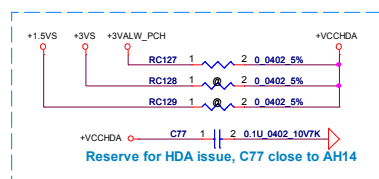
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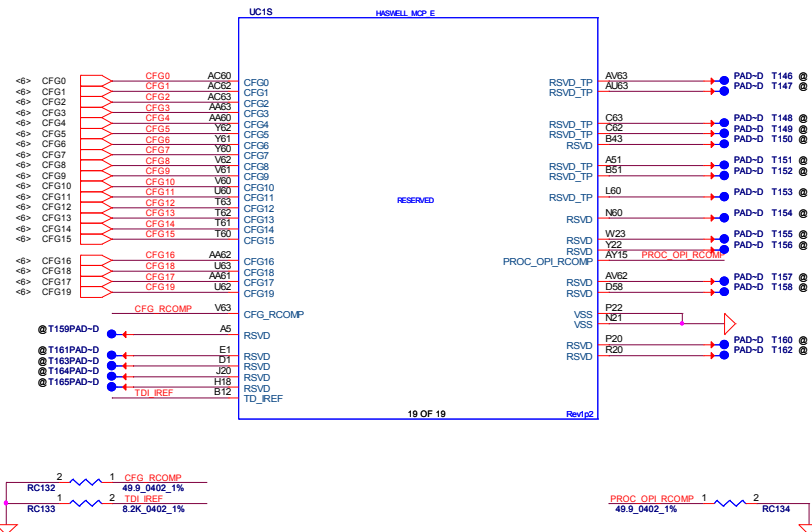
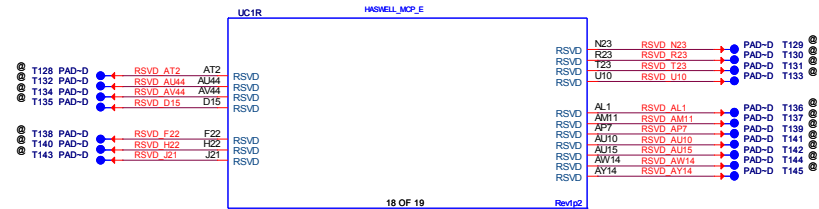
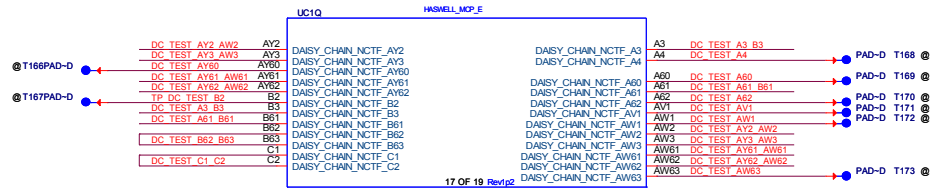




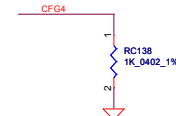
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CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port

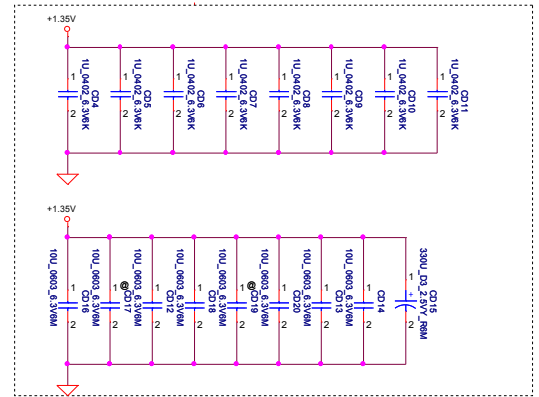
Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

<7> DDR_A_DQS[0..7]
<7> DDR_A_DQ[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_MA[0..15]

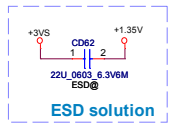
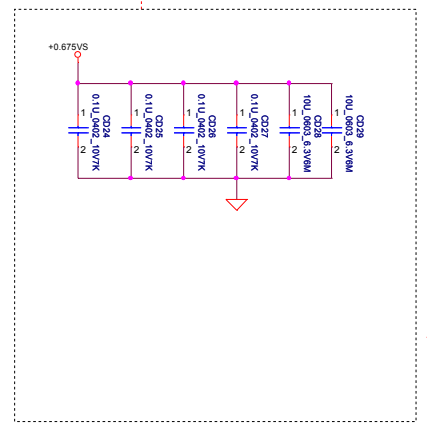
All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

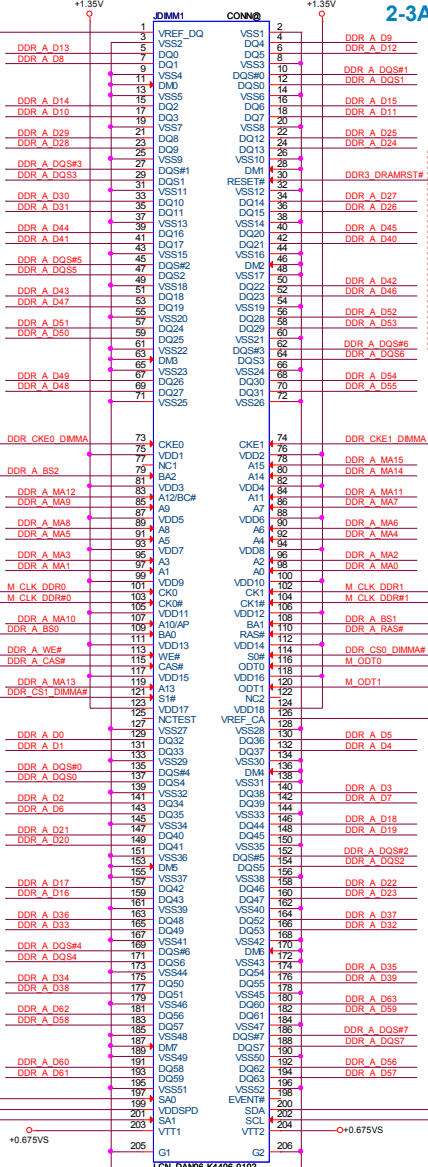


Layout Note:
Place near JDIMM1.203,204

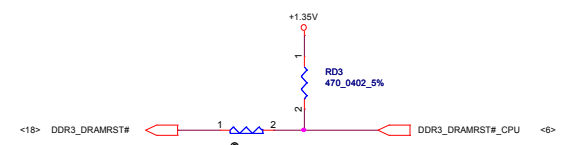


H=4mm

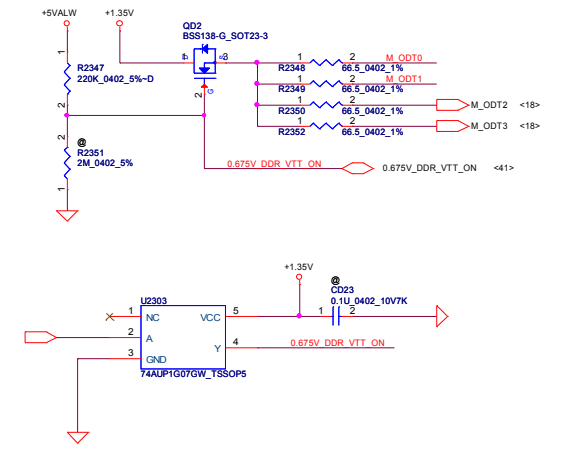
2-3A to 1 DIMMs/channel



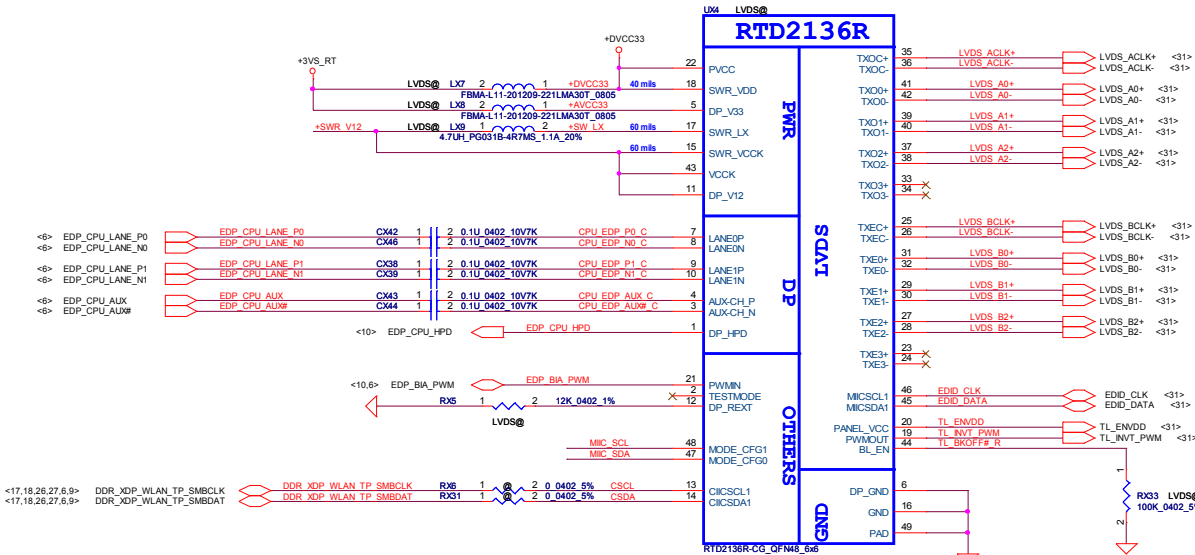
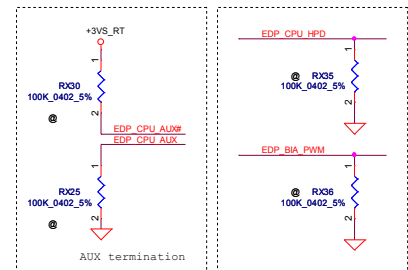
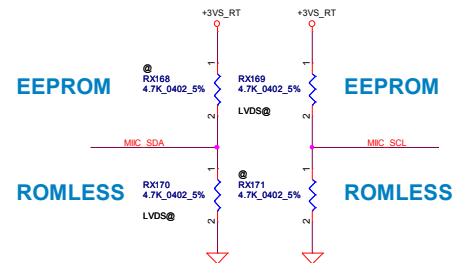
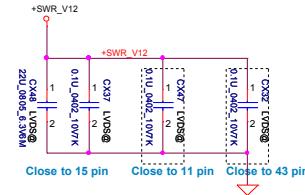
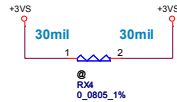
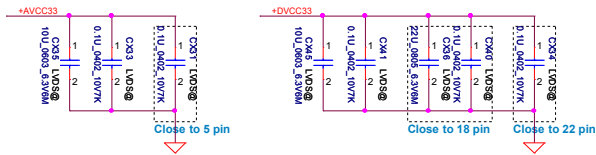
CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN



DDR3L SODIMM ODT GENERATION

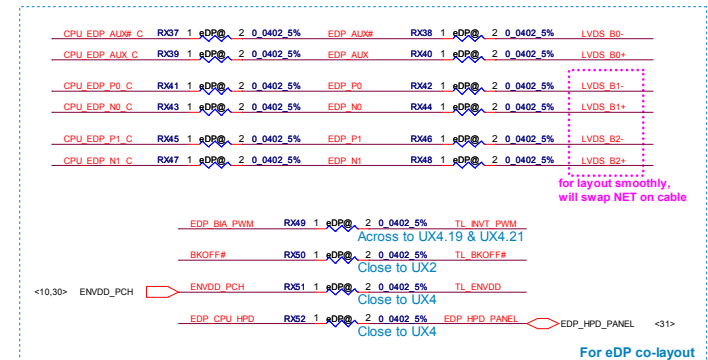
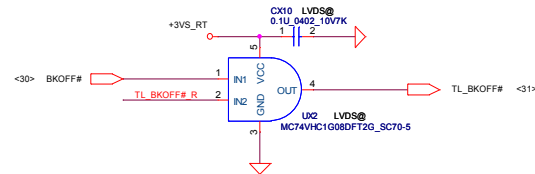


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Issued Date	2013/03/09	Deciphered Date	2014/04/01	DDR3L DIMM	
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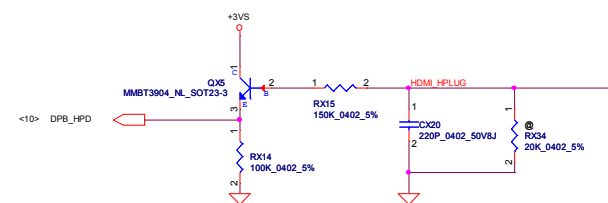
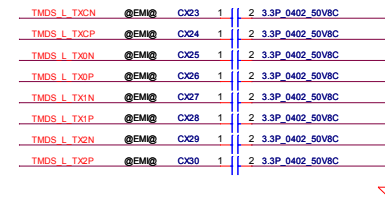
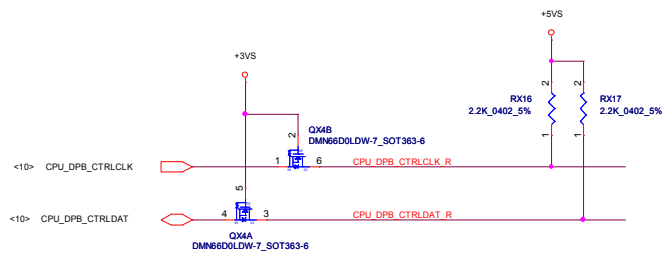
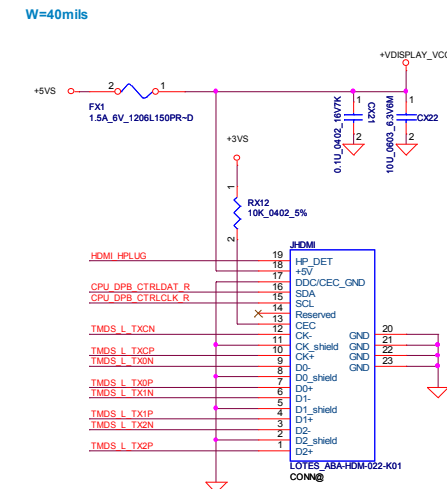
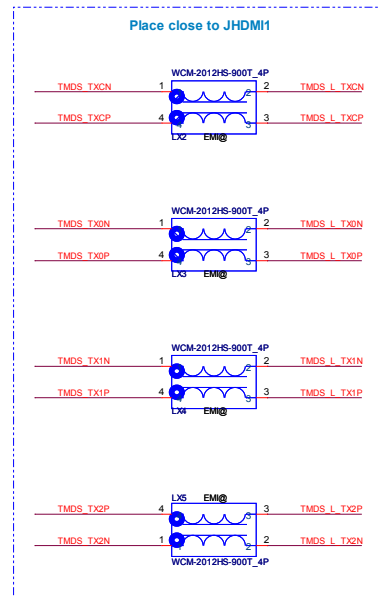
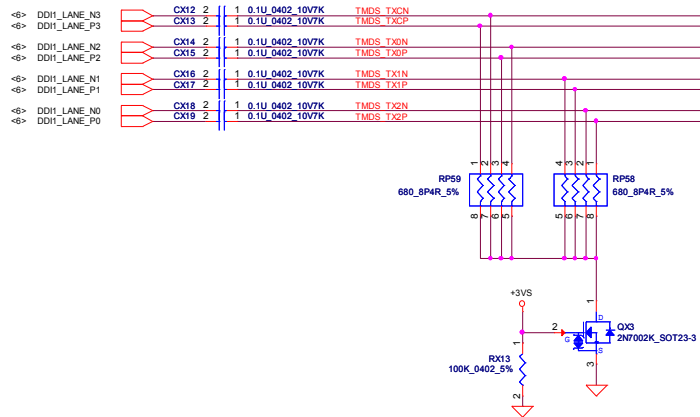


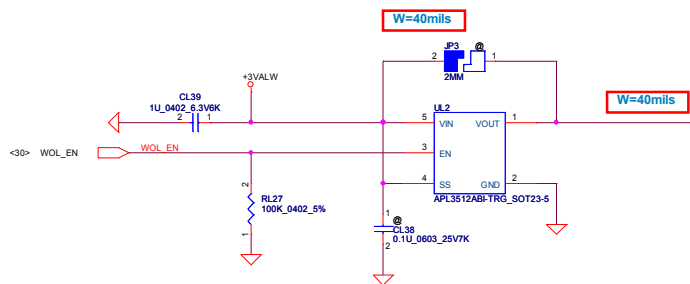
RTD2136S : SA00004NW10
RTD2136R : SA000067100

Vendor advise reserve it



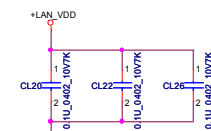
Security Classification		Compal Secret Data		Title	
Issued Date	2013/03/09	Deciphered Date	2014/04/01	Compal Electronics, Inc.	
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				Size	Document Number
				LA-9981P	
				Date	Rev
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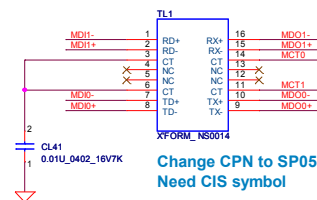
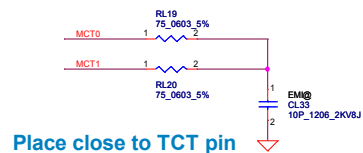


W=40mils +LAN_IO rising time : >1ms and <100ms

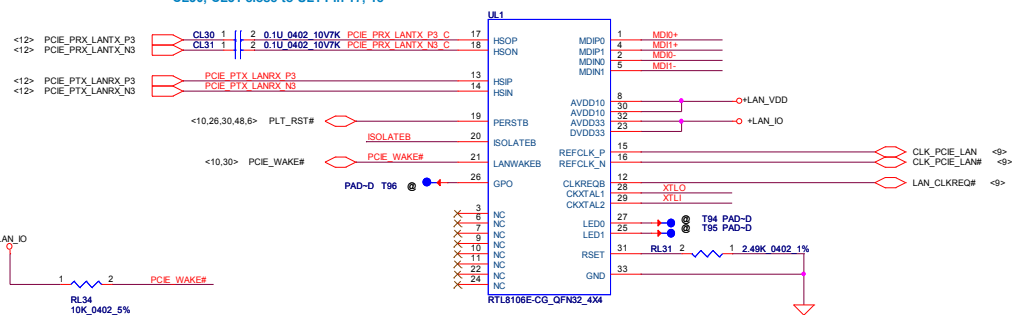
These caps close to Pin 23,32
For 8106E pop the capacitor close pin 23,32



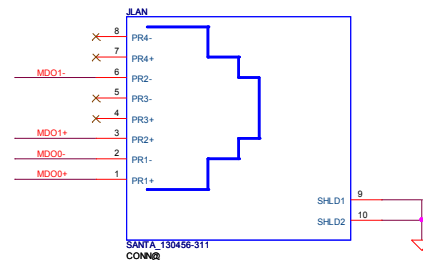
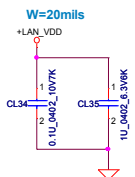
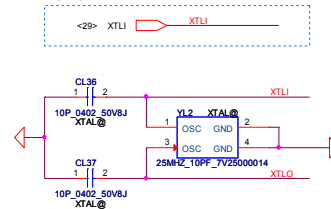
These caps close to Pin 8,30
For 8106E pop capacitor close to pin 8,30



CL30, CL31 close to UL1 Pin 17, 18



For GCLK



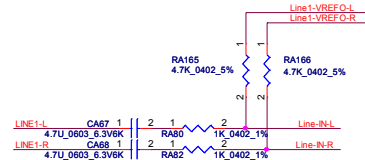
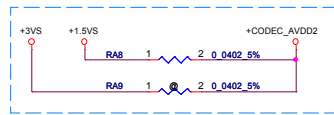
Reserve 10K pull LAN_IO

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				Date	Sheet
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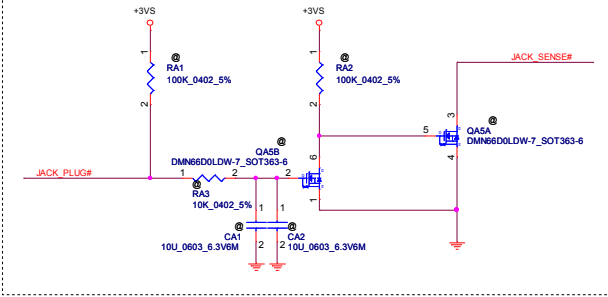
CA71, CA51 place close to Pin 26

CA53, CA55 change Value
from 10U_0603_6.3V6M~D to
4.7U_0603_6.3V6K

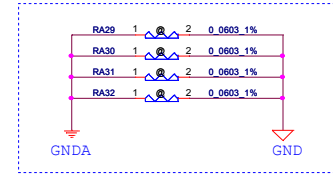
Reserve for HDA issue



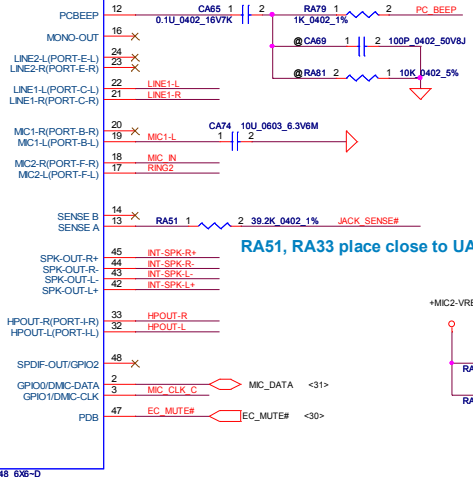
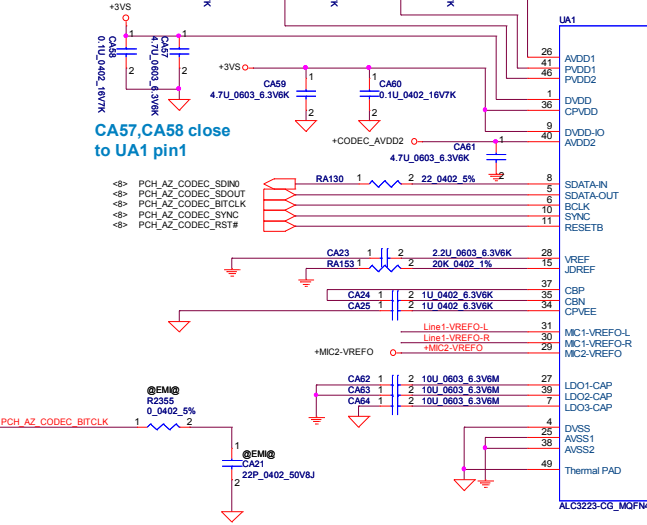
JACK_PLUG Delay circuitis



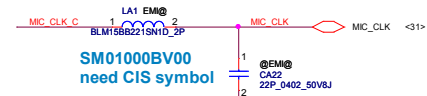
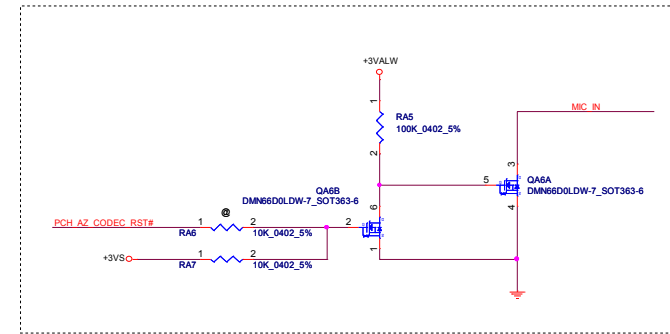
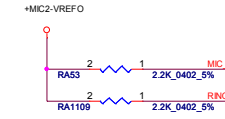
Reserve for cancel Delay circuitis



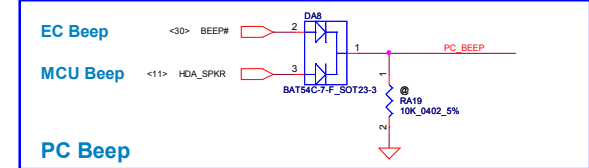
Place on the moat between GND & GNDA.



RA51, RA33 place close to UA1



SM01000BV00
need CIS symbol

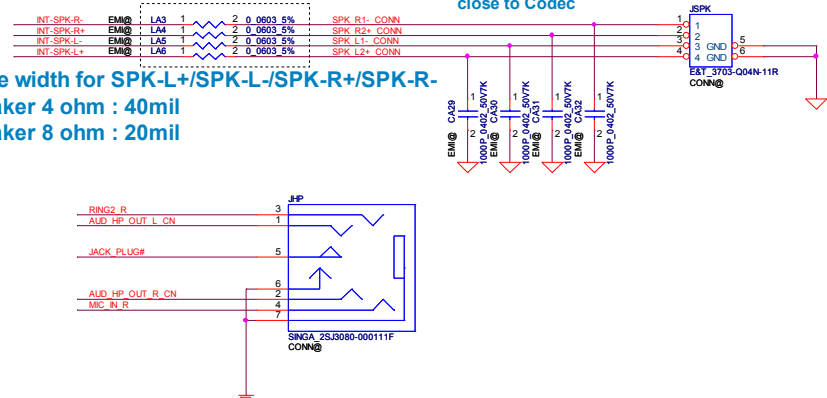
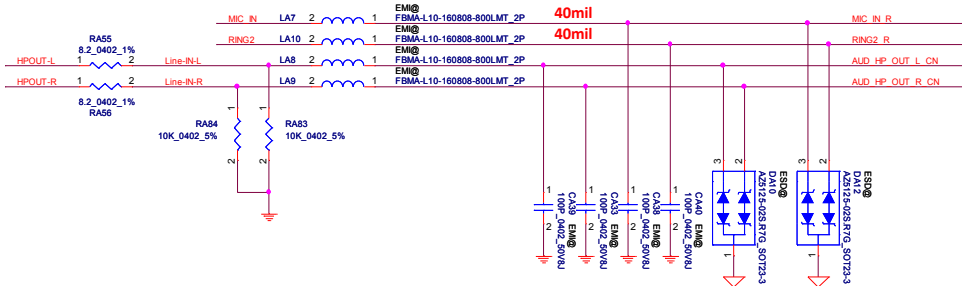


Close to UA1
Pin11,13,14,16

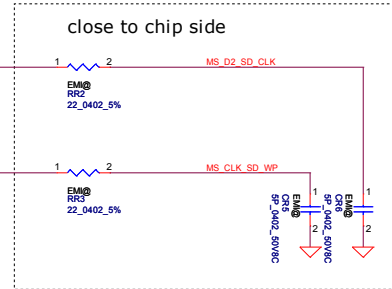
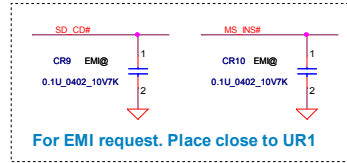
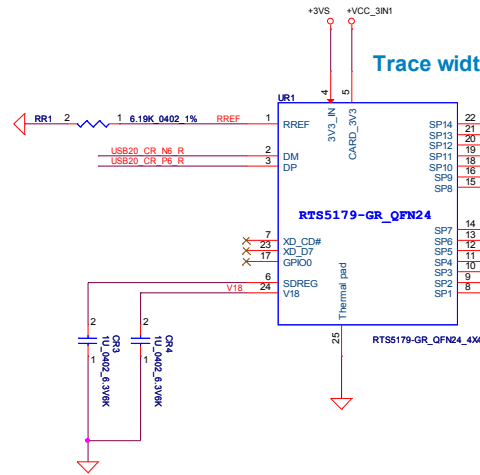
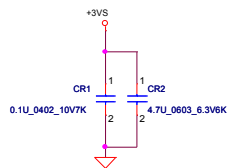
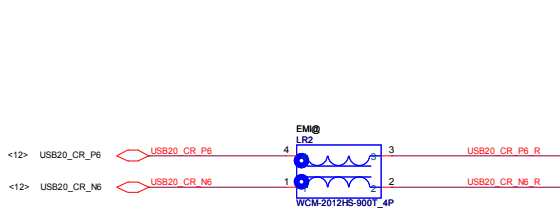
close to Codec

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

iPhone and Nokia type Combo Jack

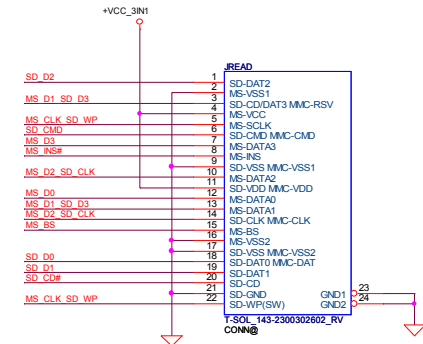
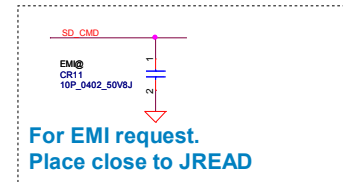
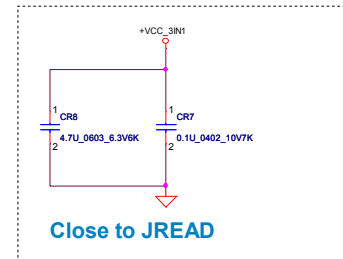


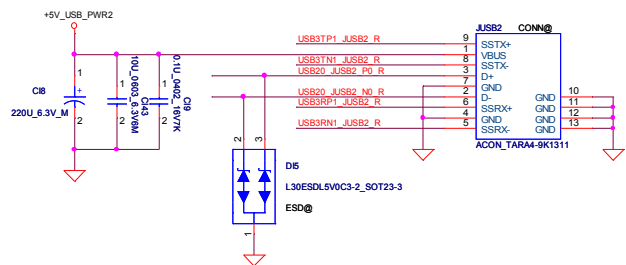
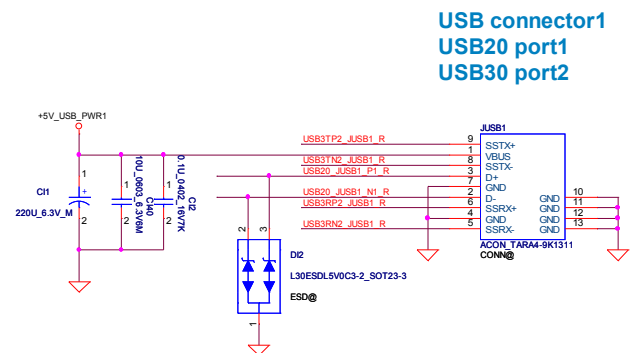
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		2014/04/01	
2013/03/09		2014/04/01		Compal Electronics, Inc.	
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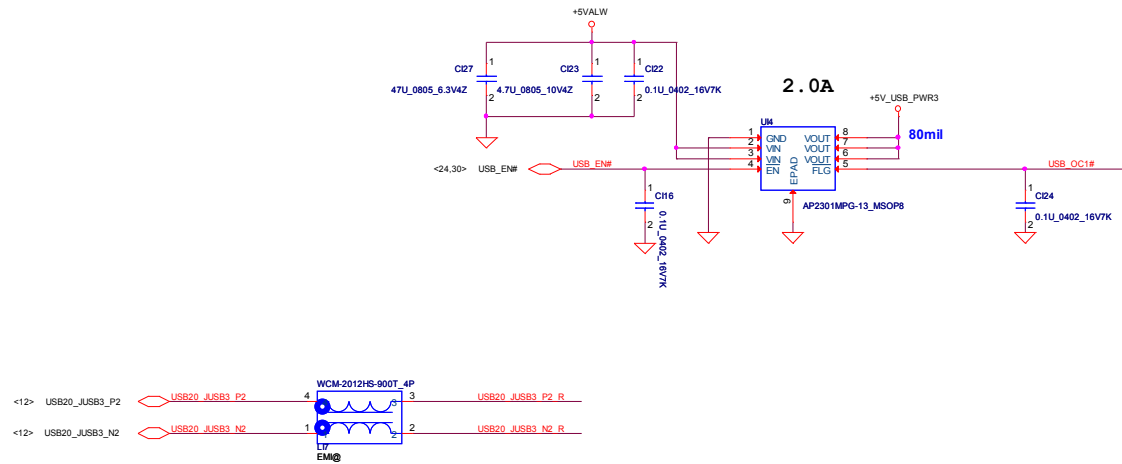
拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W

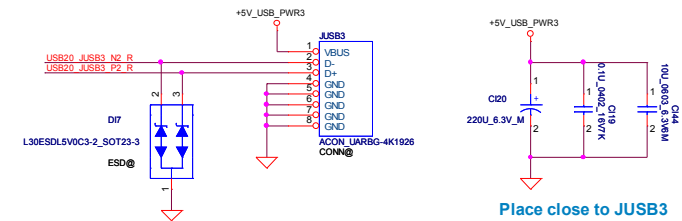




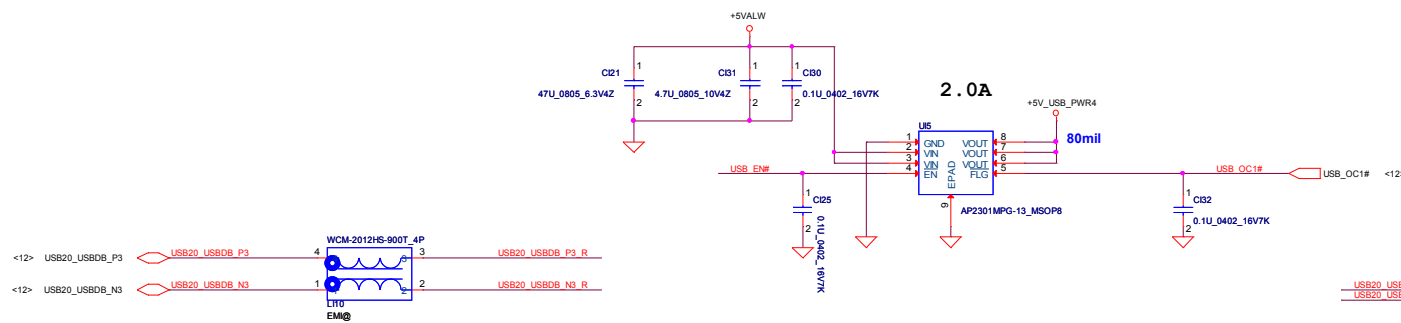
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Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title	USB3.0	
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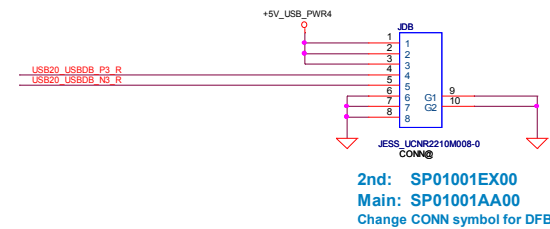
USB connector3
USB20 port2



Place close to USB3



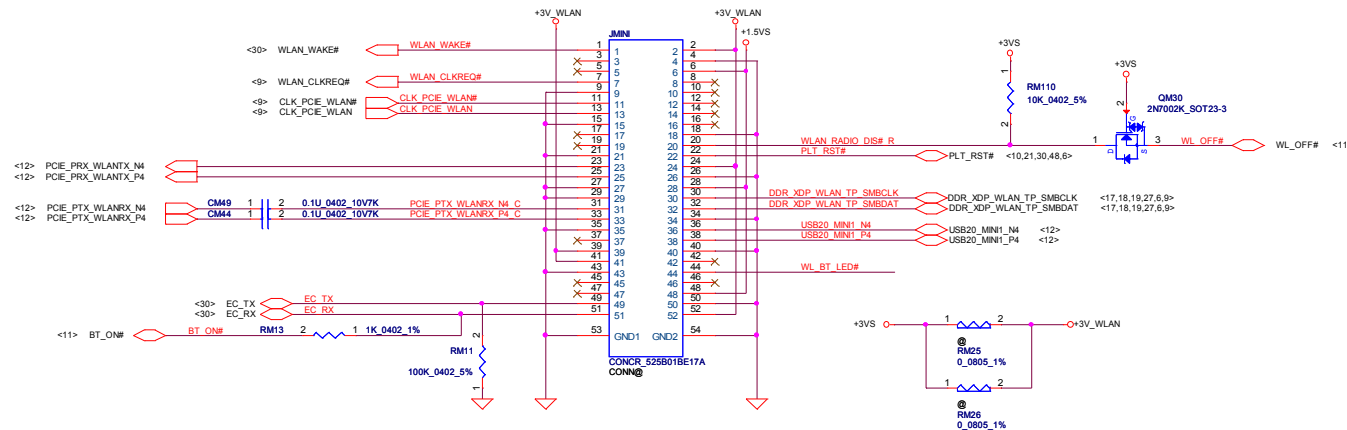
USB connector4
USB20 port3



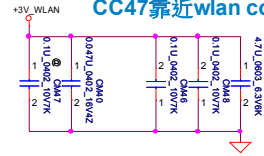
2nd: SP01001EX00
Main: SP01001AA00
Change CONN symbol for DFB

Security Classification		Compal Secret Data		Title	
Issued Date	2013/03/09	Deciphered Date	2014/04/01	MB to USB2.0 DB	
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				Saturday, March 09, 2013	0.2
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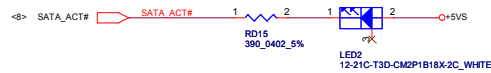
Mini WLAN/WIMAX H=6.7



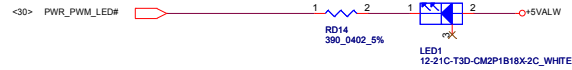
CC47靠近wlan connector



HDD LED

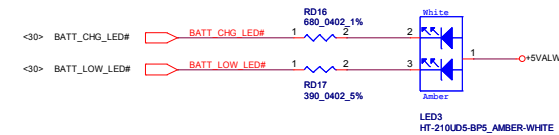


Power LED

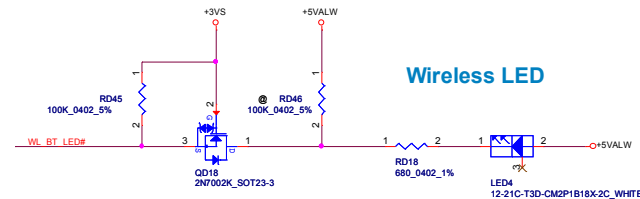


10mils, All pins

Battery LED

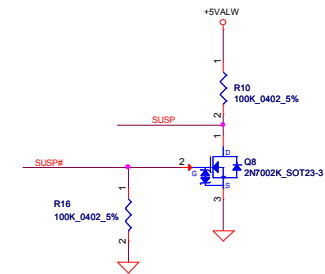
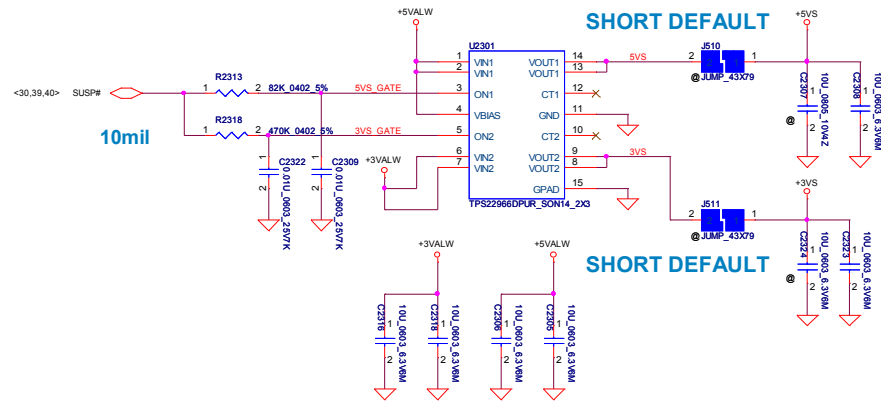


Wireless LED

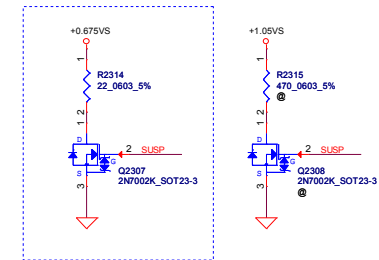
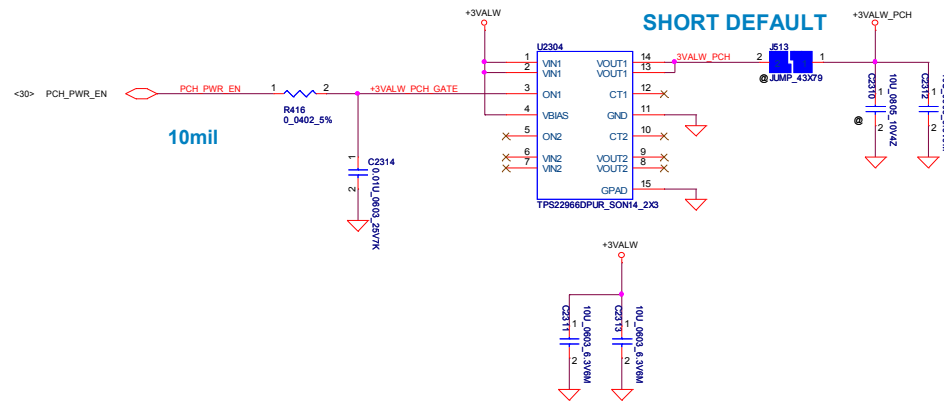


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+5VS and +3VS switch

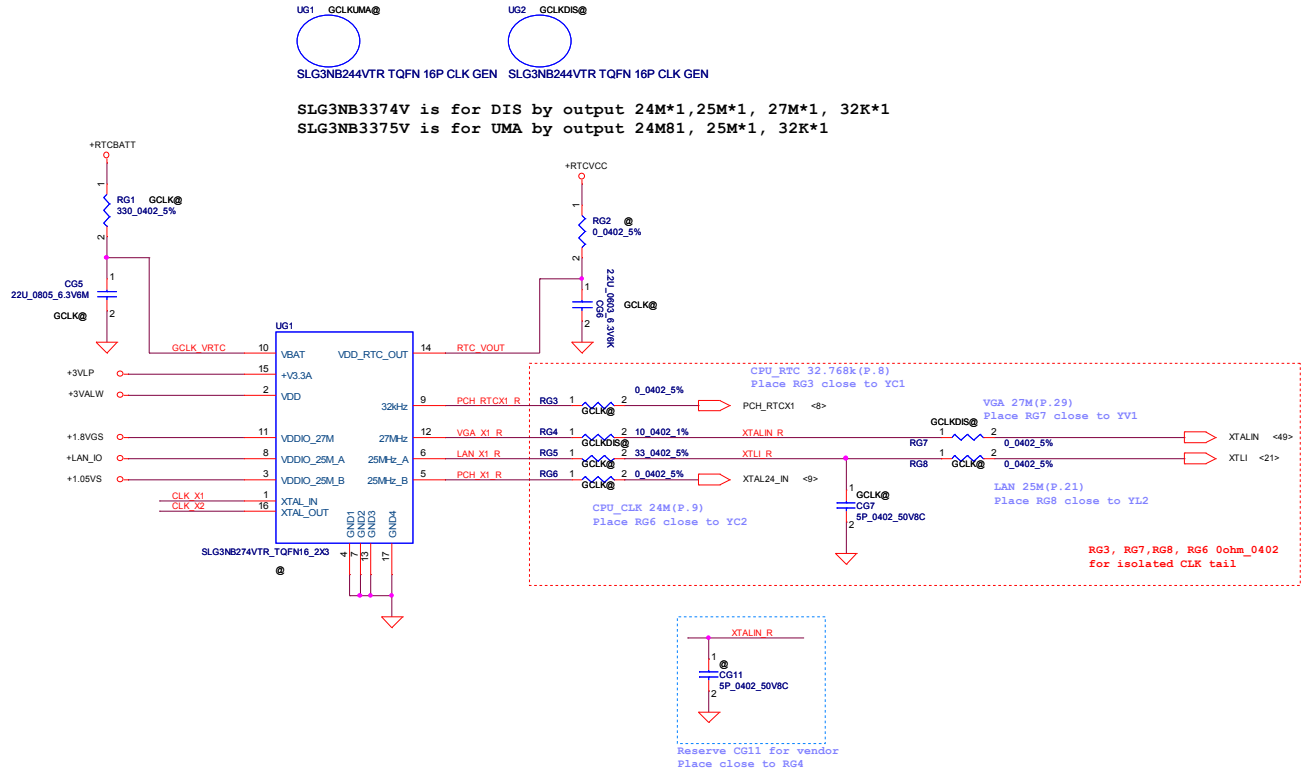
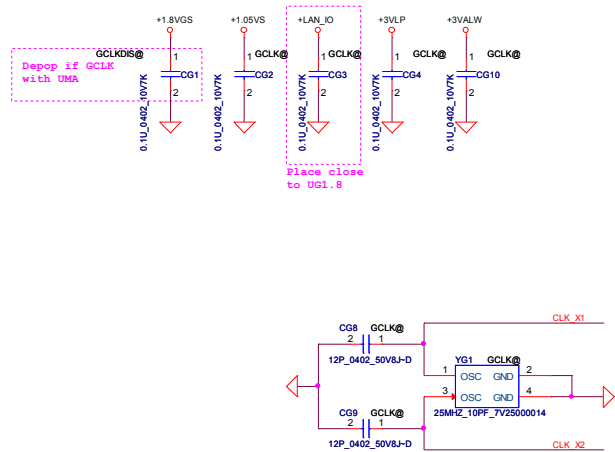


+3VALW_PCH switch

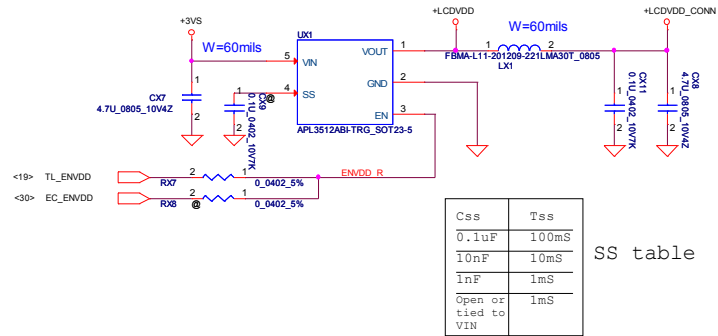


For Intel S3 Power Reduction

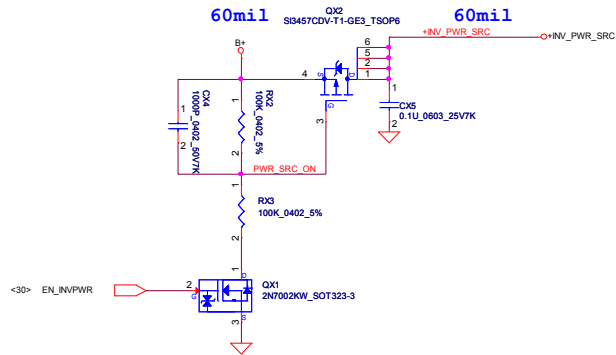
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Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title	DC/DC Interface
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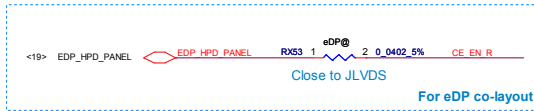
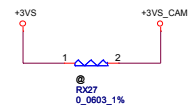
LCD PWR CTRL



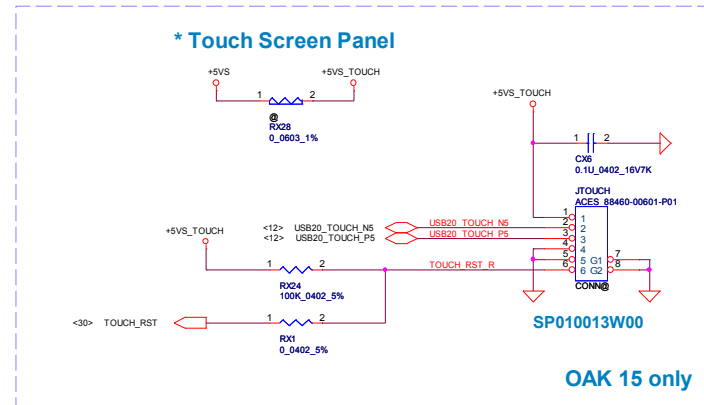
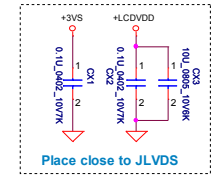
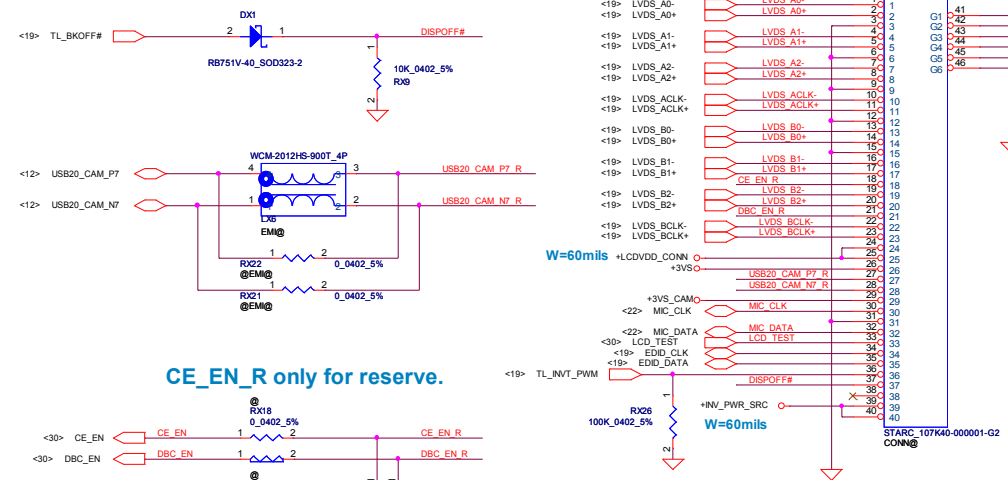
LCD backlight PWR CTRL



Webcam PWR CTRL

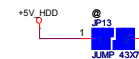


LVDS Connector

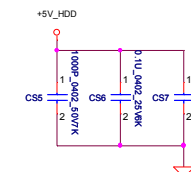
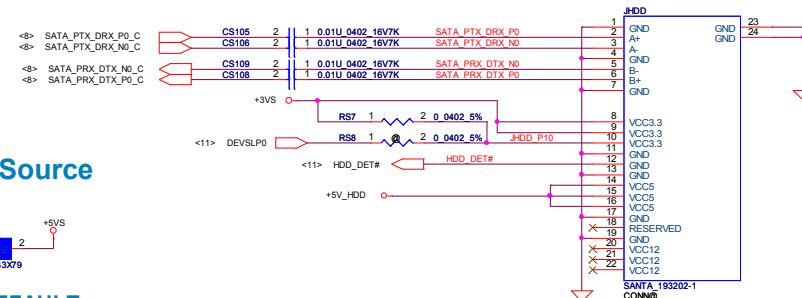


SATA HDD Connector

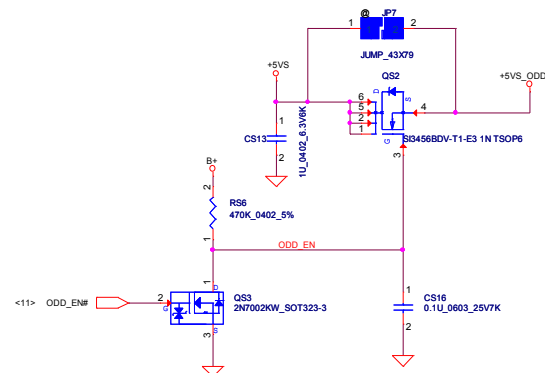
+5V_HDD Source



SHORT DEFAULT

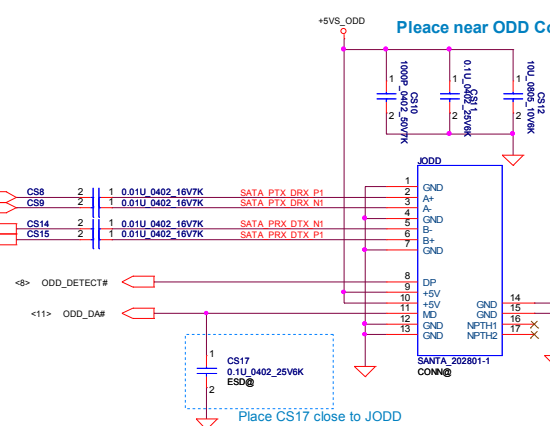


ODD Power Control



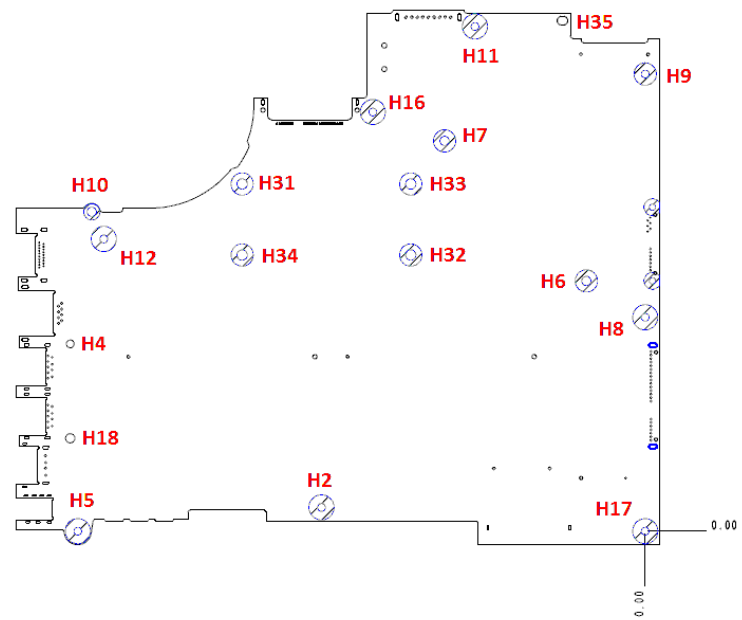
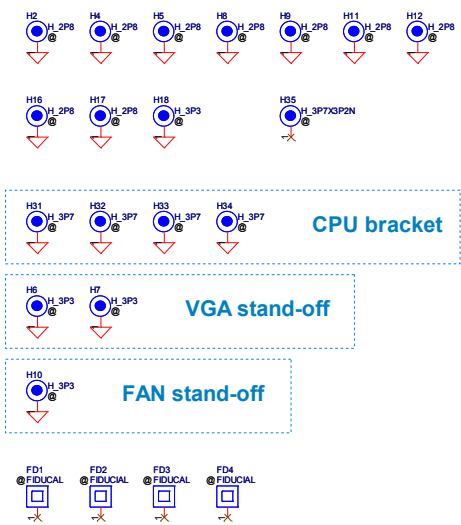
SATA ODD Connector

Please near ODD Connector



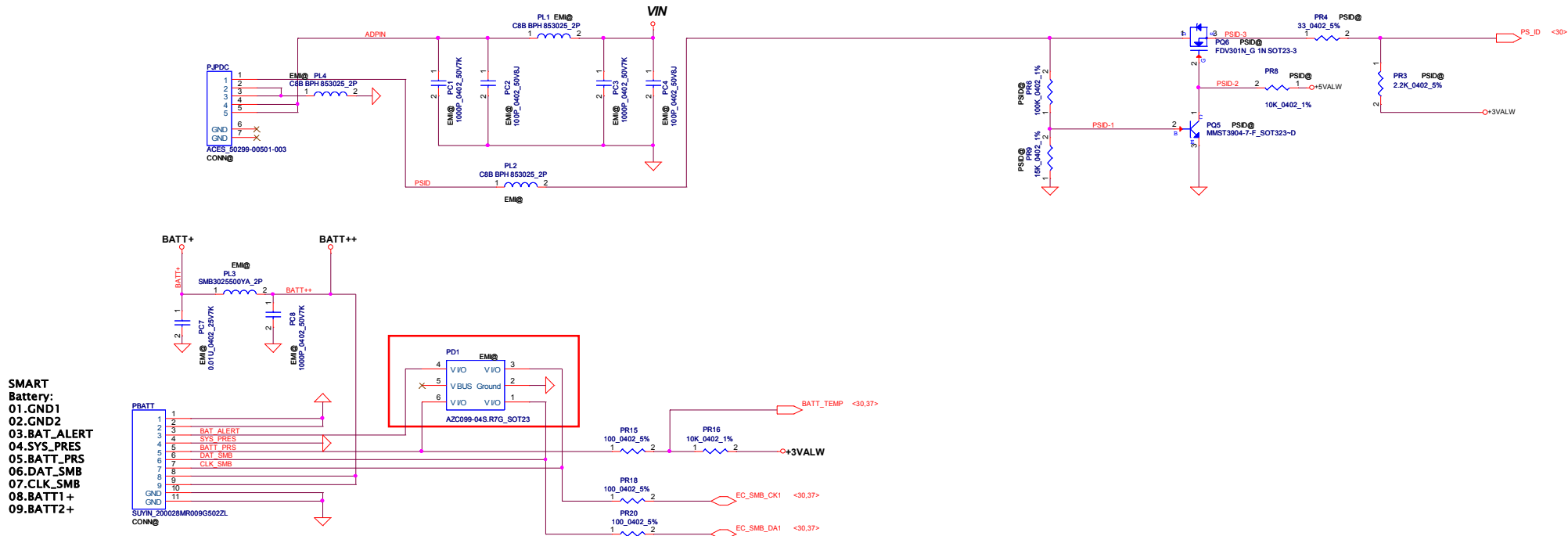
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Screw Hole

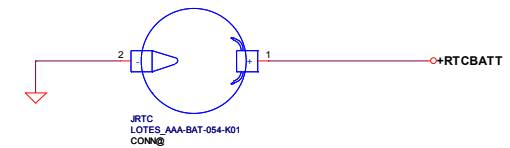
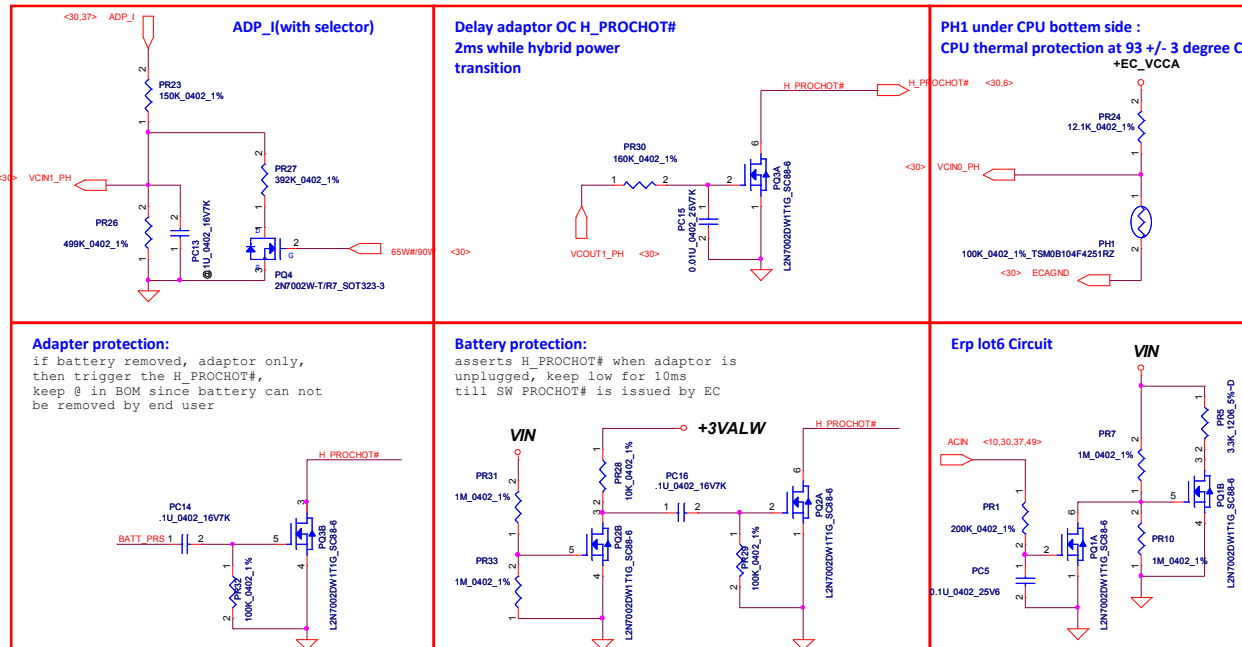


Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP URL USB signal P/N	0.2
2							
3							
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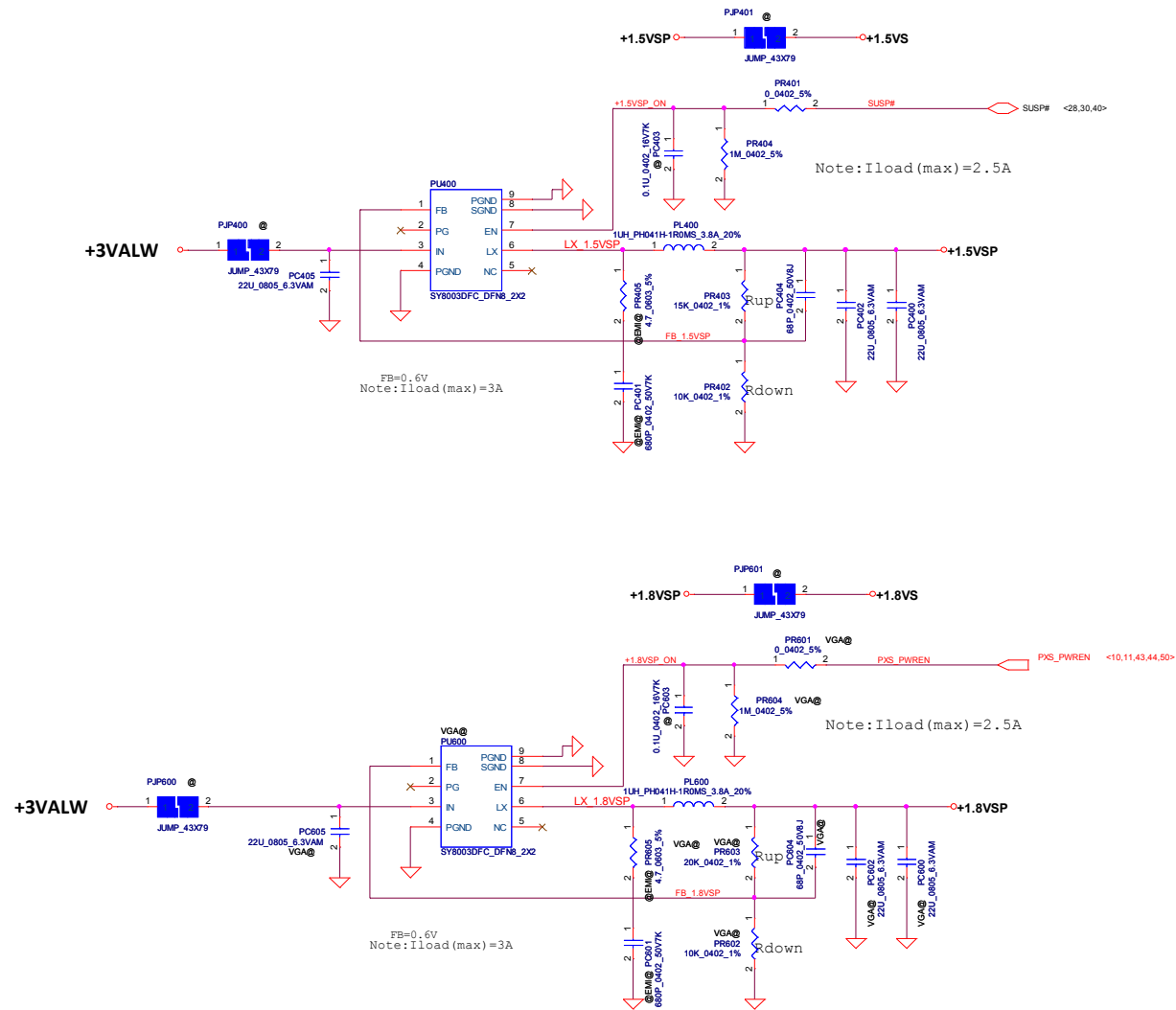
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40							
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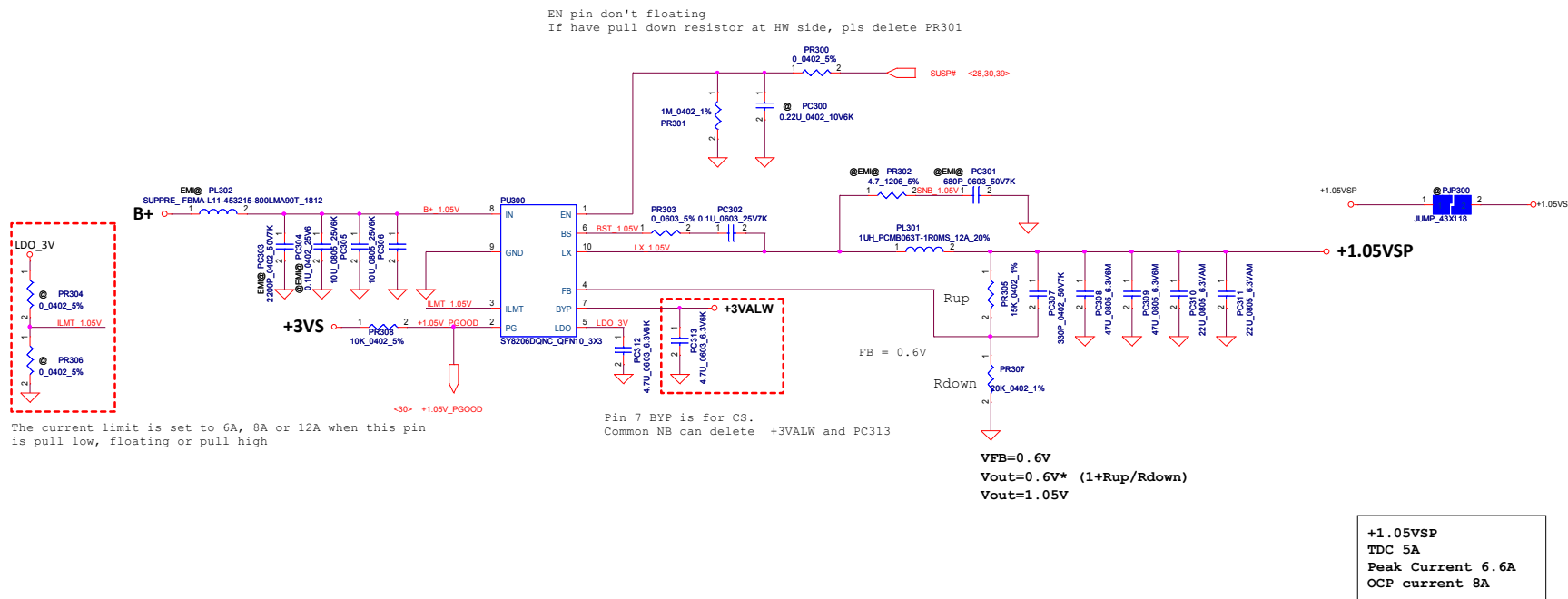


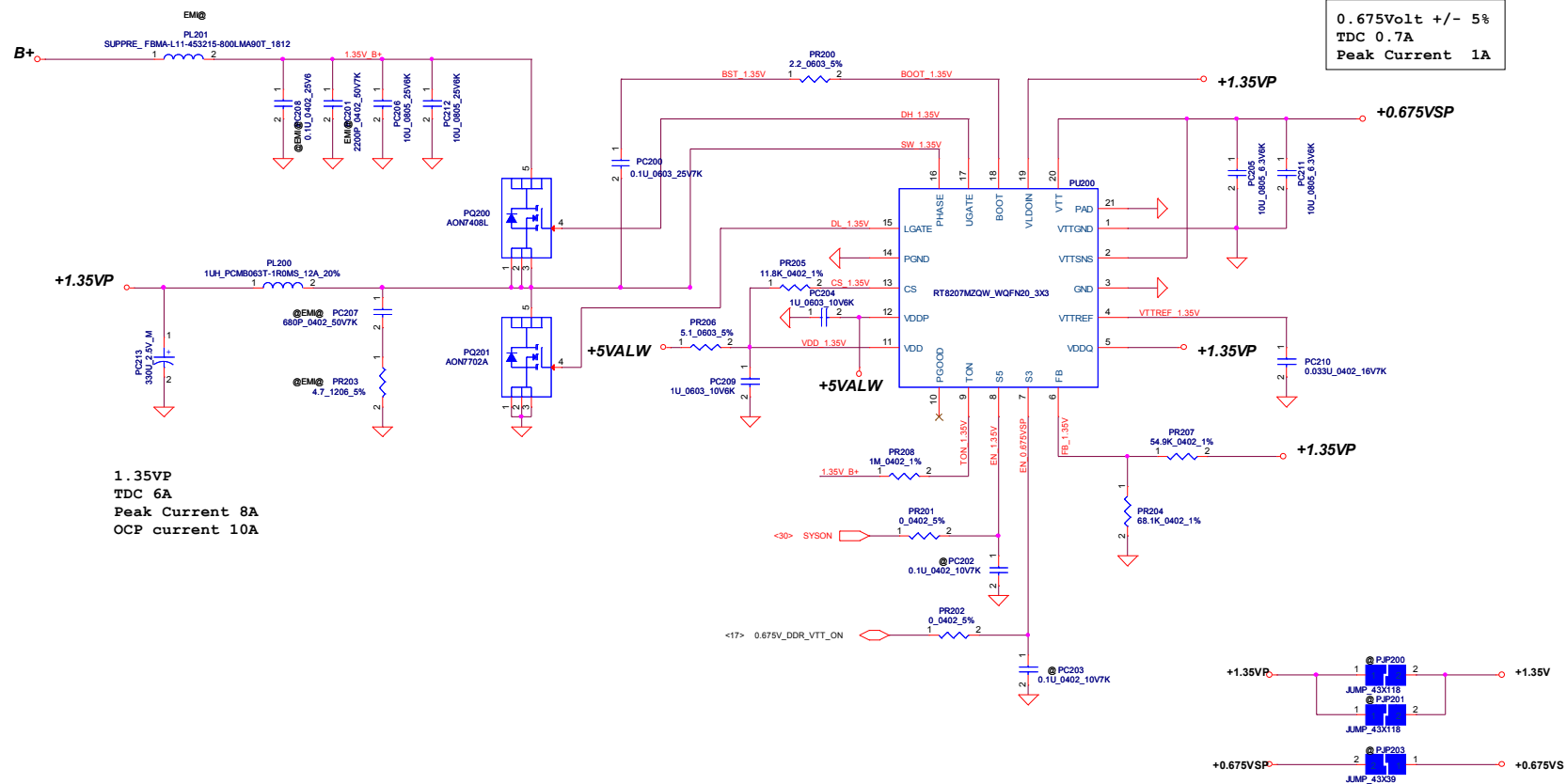
Other component (37.1)



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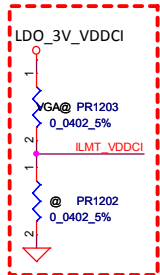




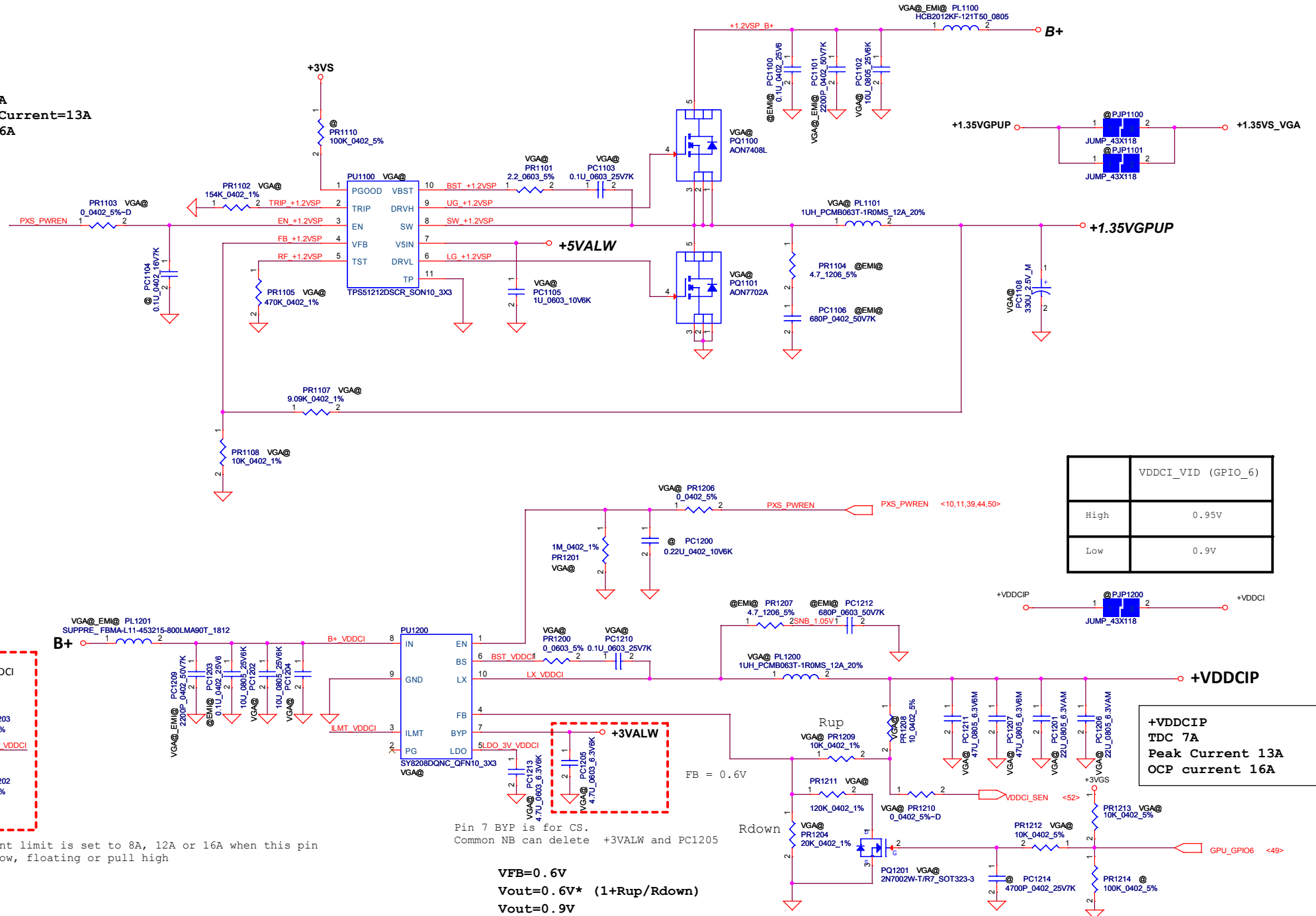


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TDC=9A
Peak Current=13A
OCP=16A



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high



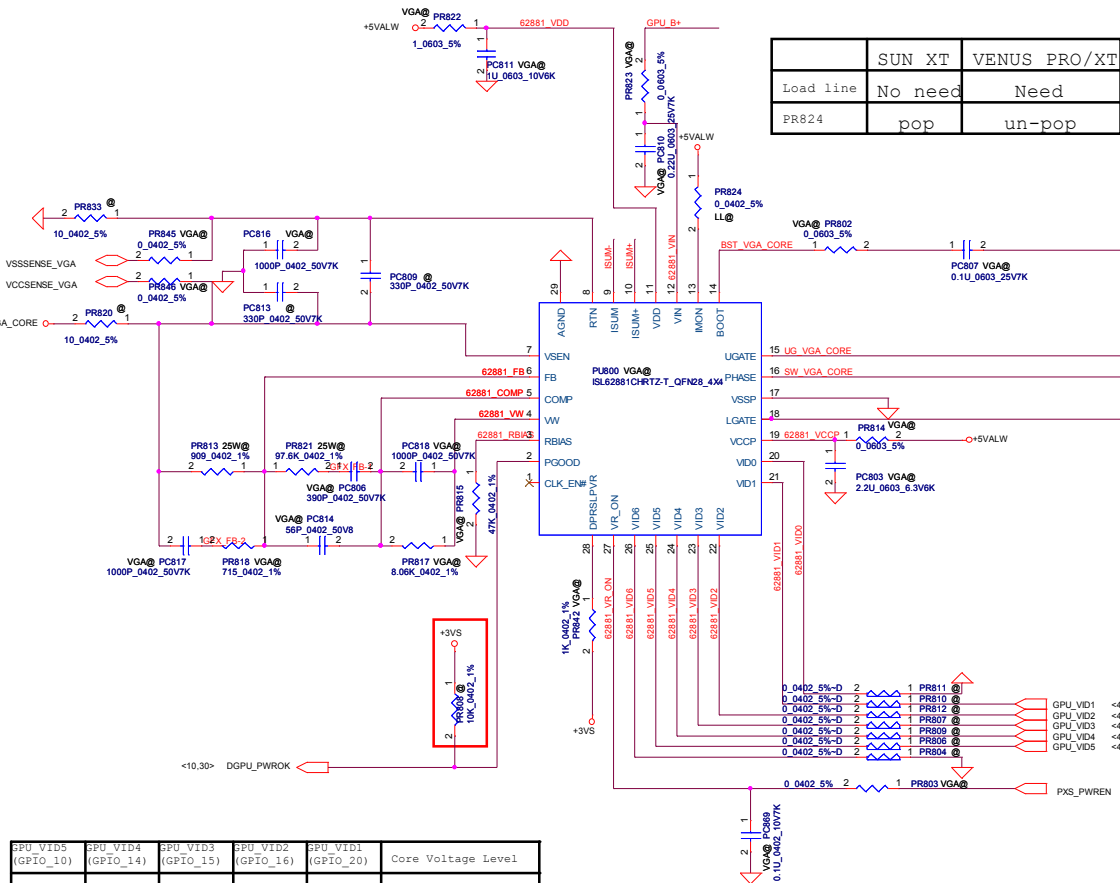
	VDDCI_VID (GPIO_6)
High	0.95V
Low	0.9V

+VDDCIP
TDC 7A
Peak Current 13A
OCP current 16A

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC1205

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=0.9V

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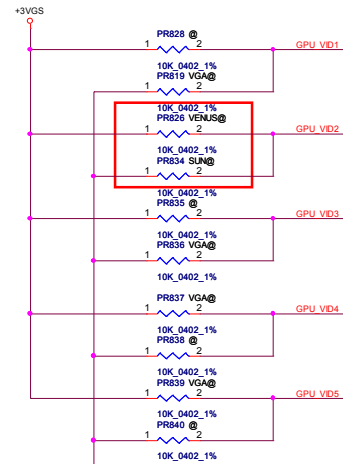


VGA_CORE
Frequency 300kHz
TDC 23A (25W) / 33A (32W)
Peak Current 30A (25W) / 47A (32W)
OCF current 36A (25W) / 56A (32W)
TYP MAX
H/S Rds(on) : 12.2mohm , 15mohm
L/S Rds(on) : 2.75mohm , 3.5mohm
Choke DCR 1.1mohm (Typ) / 1.3mohm (Max)
Load line : -1.5mV/A

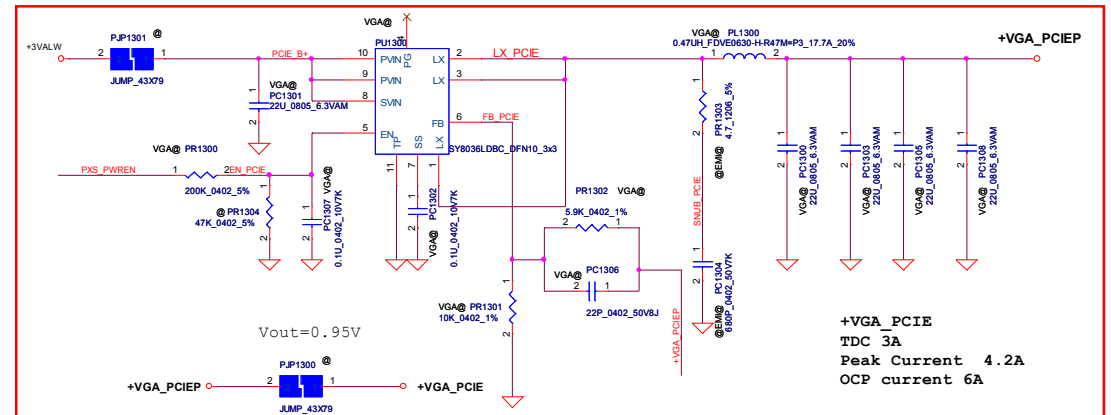


	25W	32W
PR813	909	1.4K
PR821	97.6K	143K
PR825	976	1.5K

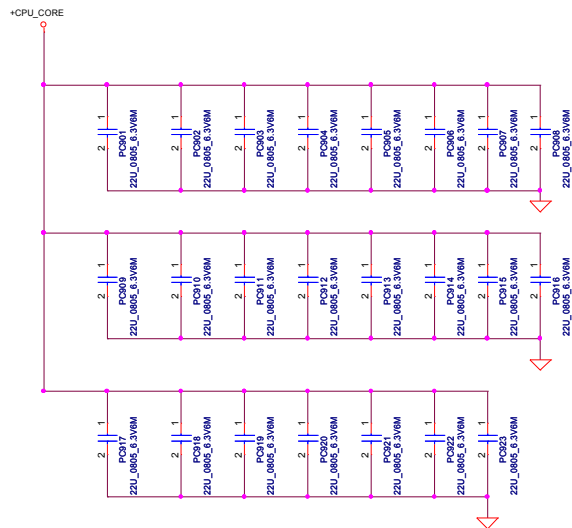
SPU_VID5 (GPIO_10)	SPU_VID4 (GPIO_14)	SPU_VID3 (GPIO_15)	SPU_VID2 (GPIO_16)	SPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	0	0	1.2V
0	1	1	0	1	1.175V
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	1	1	0.775V



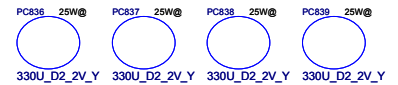
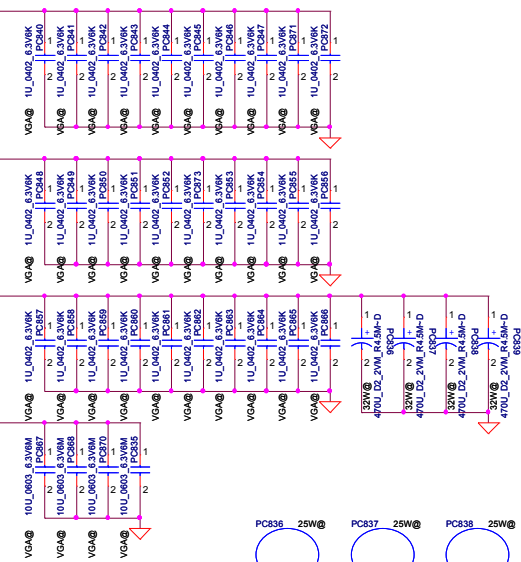
Initial voltage: 0.85V (Venus)
0.9V (Sun)



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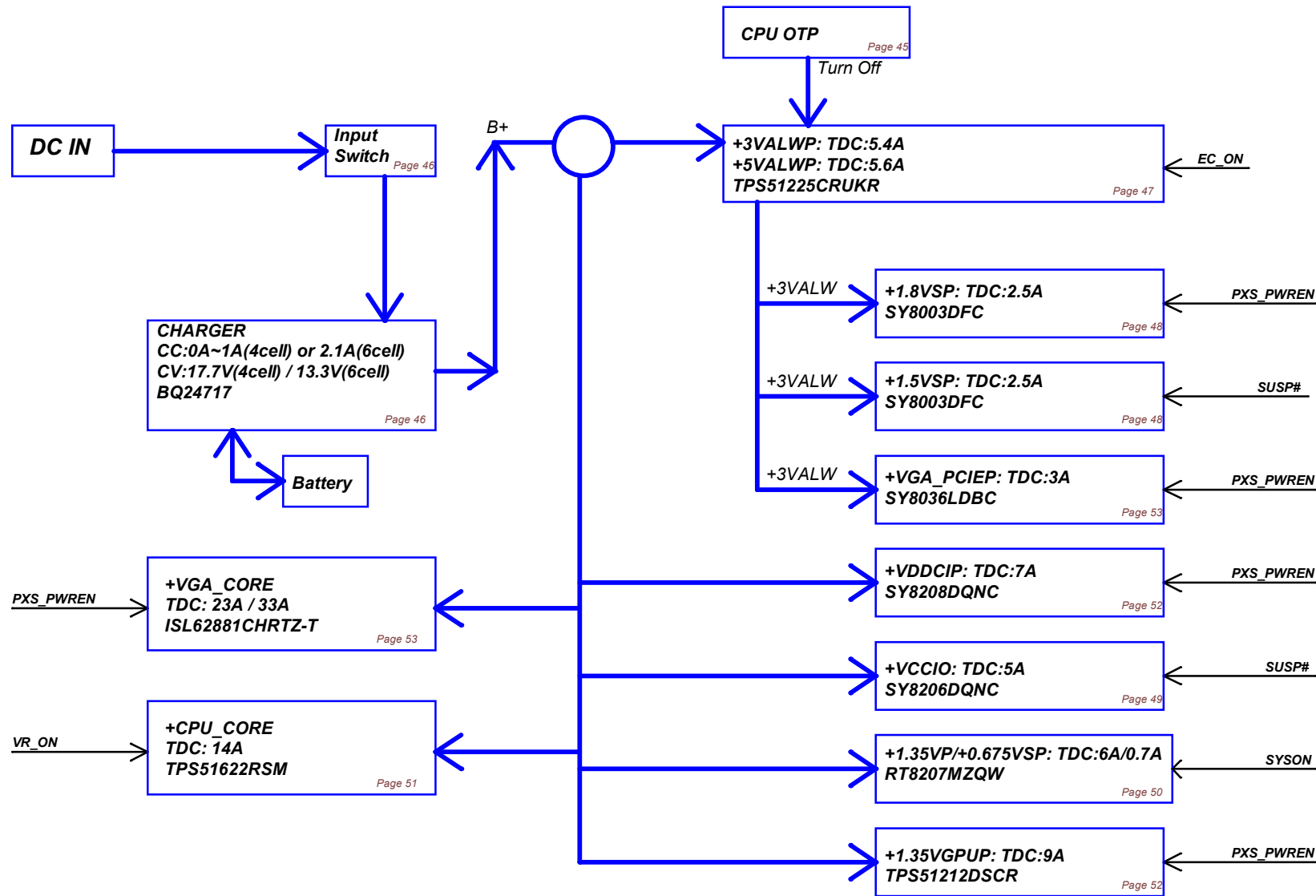


+VGA_CORE



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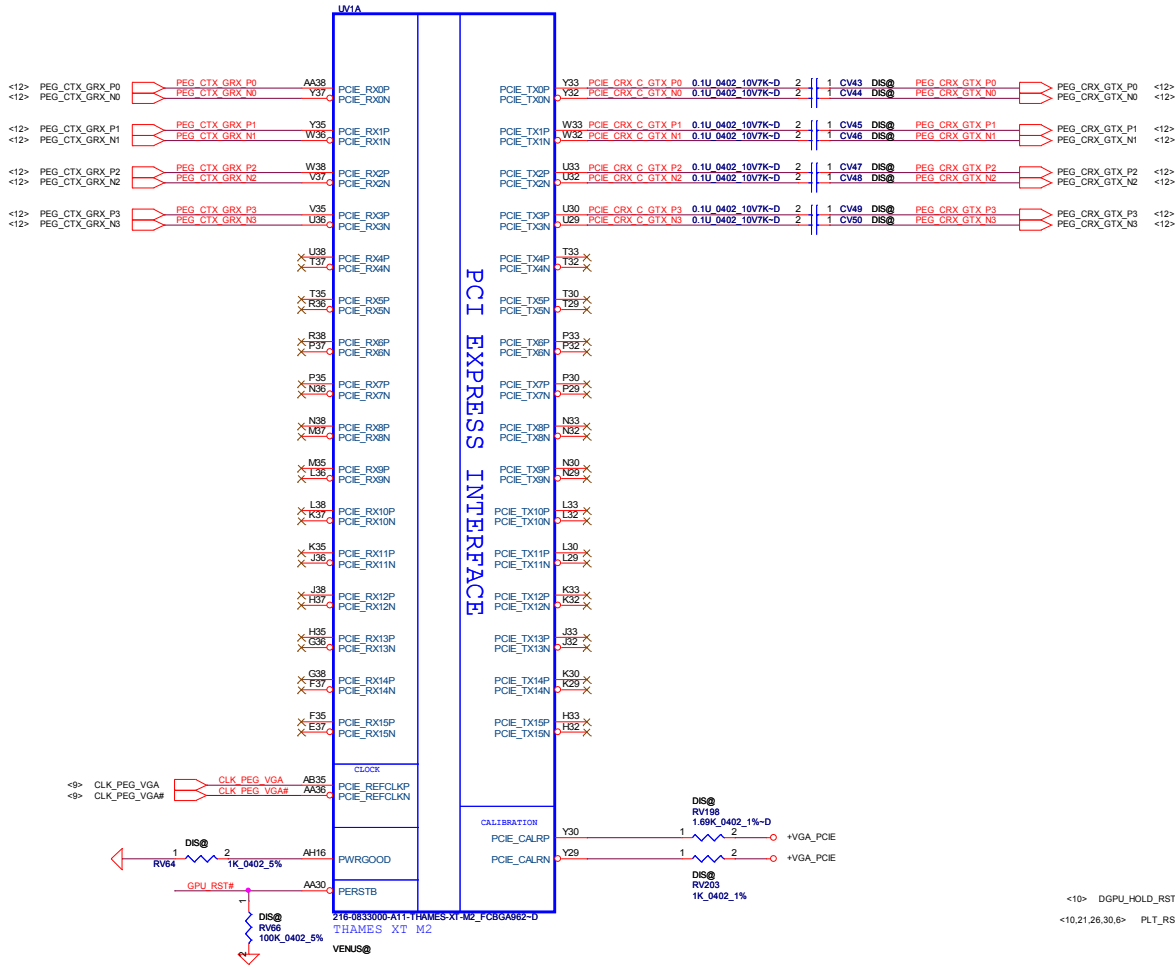
Power block



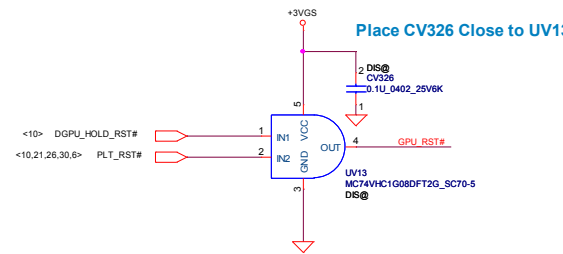
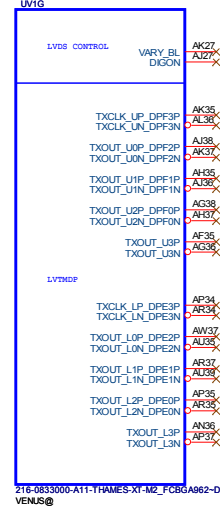
Page 1

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GFX PCIE LANE REVERSAL

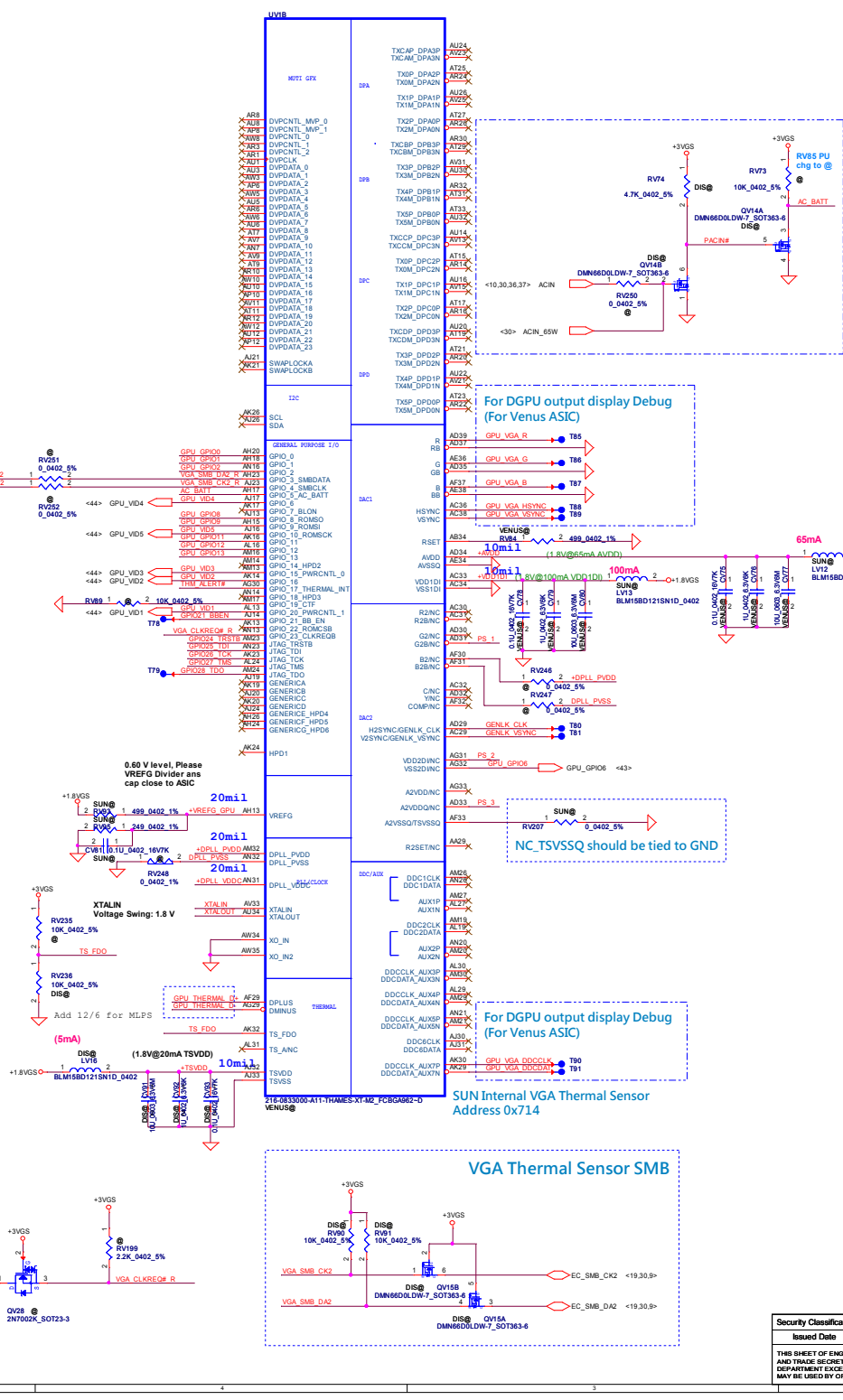
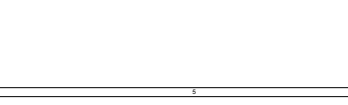
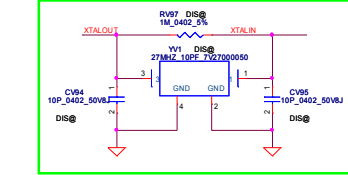
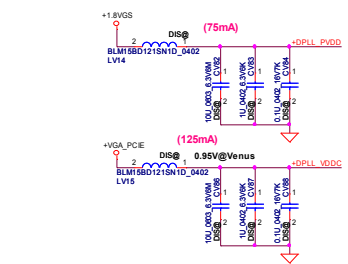
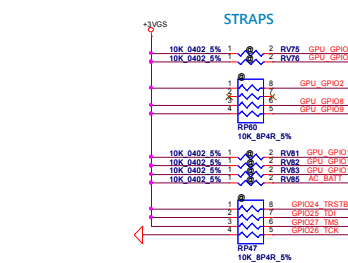


LVDS Interface



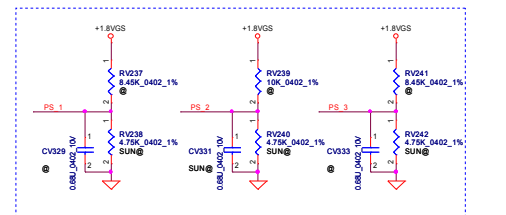
SUN GPIO N.C. PIN

- GPIO1 GPU_GPIO1
- GPIO2 GPU_GPIO2
- GPIO7 N.C
- GPIO11 GPU_GPIO11
- GPIO12 GPU_GPIO12
- GPIO13 GPU_GPIO13
- GPIO14 N.C
- GPIO18 N.C



CONFIGURATION STRAPS				RECOMMENDED SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEPENDANT NA= NOT APPLICABLE	
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS		RECOMMENDED SETTINGS	
TX_PWRs_ENB	GPIO0	PCIE FULL TX OUTPUT SWING		0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS		0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIe speed when compliance test		0: 2.50t/s 1: 5.0t/s	0
RSVD	GPIO8	RESERVED			0
BF_VGA_DIS	GPIO9	VGA ENABLED			0
RSVD	GPIO21	RESERVED			0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM		0: disable 1: enable	X
ROMCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT			XXX
WP_DEVICE_STRAP_ENA	V2SYNC	IGNORE WP DEVICE STRAPS			0
RSVD	H2SYNC				0
RSVD	GENERICC				0
AUD[1]	HSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI			11
AUD[0]	VSYNC				
AMD RESERVED CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET					
GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8	

TX_PWRs_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)



Vendor	RV241	RV242	Bits [3:1]
1280X16 (1GB) DDR3	Hynix 2Gb SA00006H40L(R1) SA00006H41L(R3)	NC	4.75K
1280X16 (1GB) DDR3	Samsung 2Gb SA00005SH0L(R1) SA00005SH1L(R3)	8.45K	2K
1280X16 (1GB) DDR3	Micron 2Gb SA00005XB0L(R1) SA00005XB1L(R3)	4.75K	NC

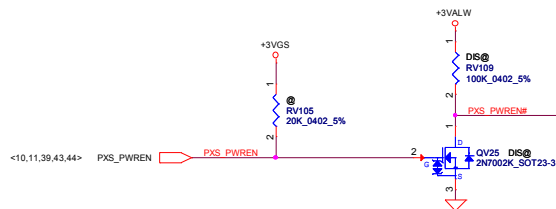


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PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails except VDDR3, PCIE_VDDC and 1.8V rail

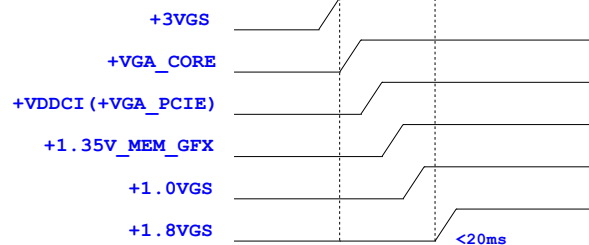
Note:

PX4.0 +VGA_CORE, VDDCI, +1.5VGS ON
PX4.0 +3VGS, +1.0VGS, +1.8VGS OFF
PX5.0 +3VGS, +VGA_CORE, VDDCI, +1.5VGV, +1.0VGS, +1.8VGS OFF

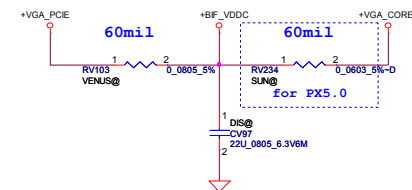


for PX4.0 and PX5.0

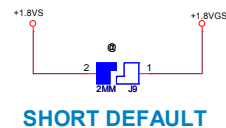
Power sequence of Sun XT, Venus Pro, Venus XT



Switch circuits in BACO desings for Thames/Seymour only
55mA@1.0V, in BACO mode

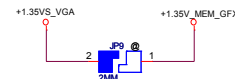


+1.8VS TO +1.8VGS



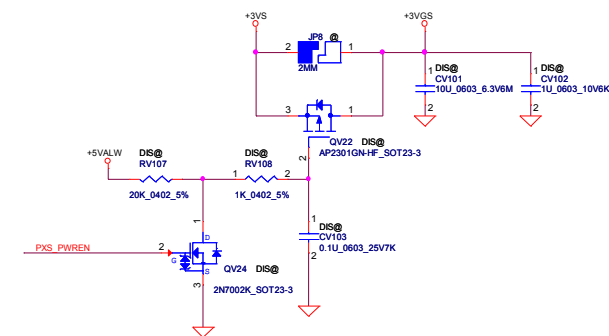
SHORT DEFAULT

+1.35VS_VGA TO +1.35V_MEM_GFX

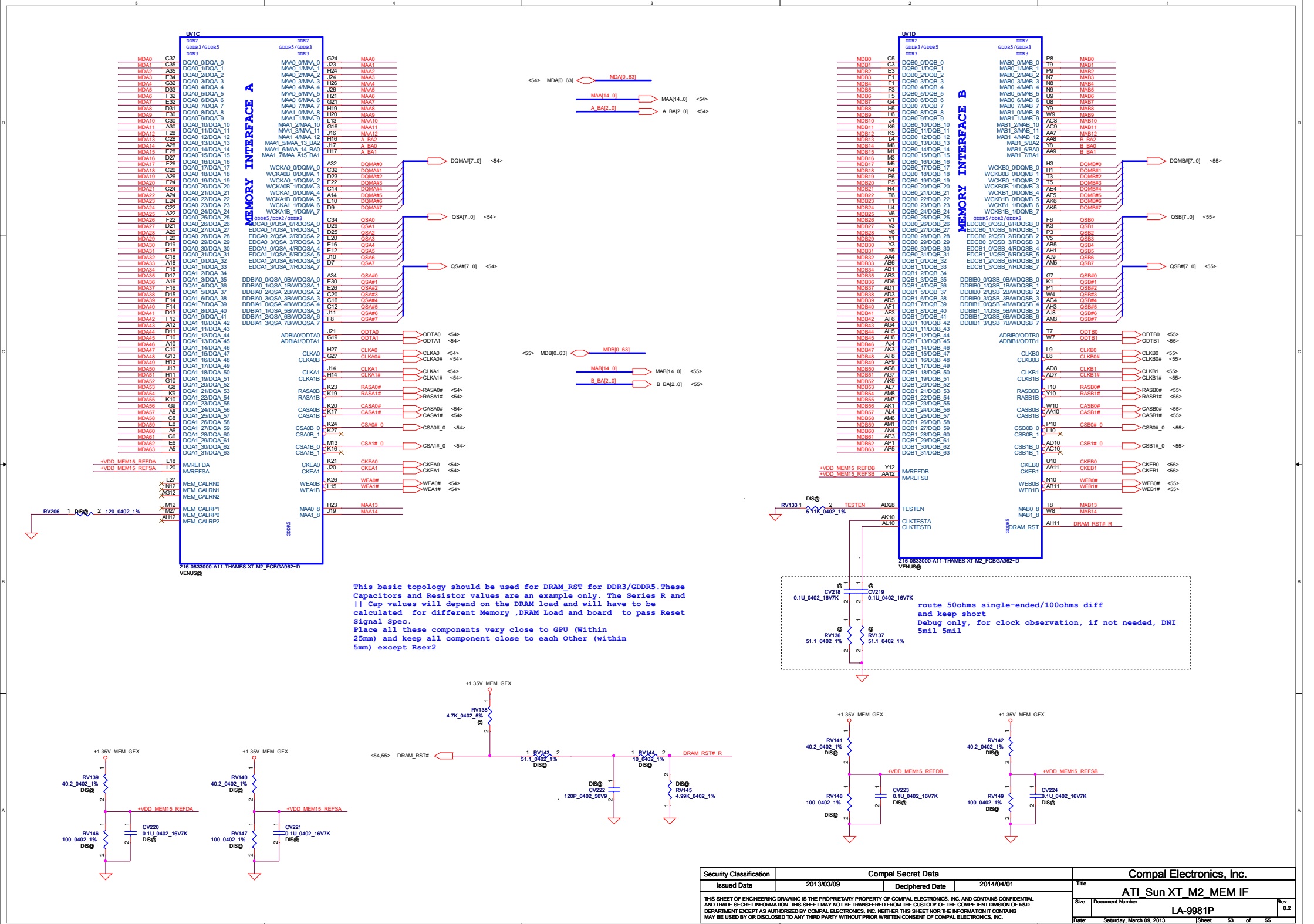


SHORT DEFAULT

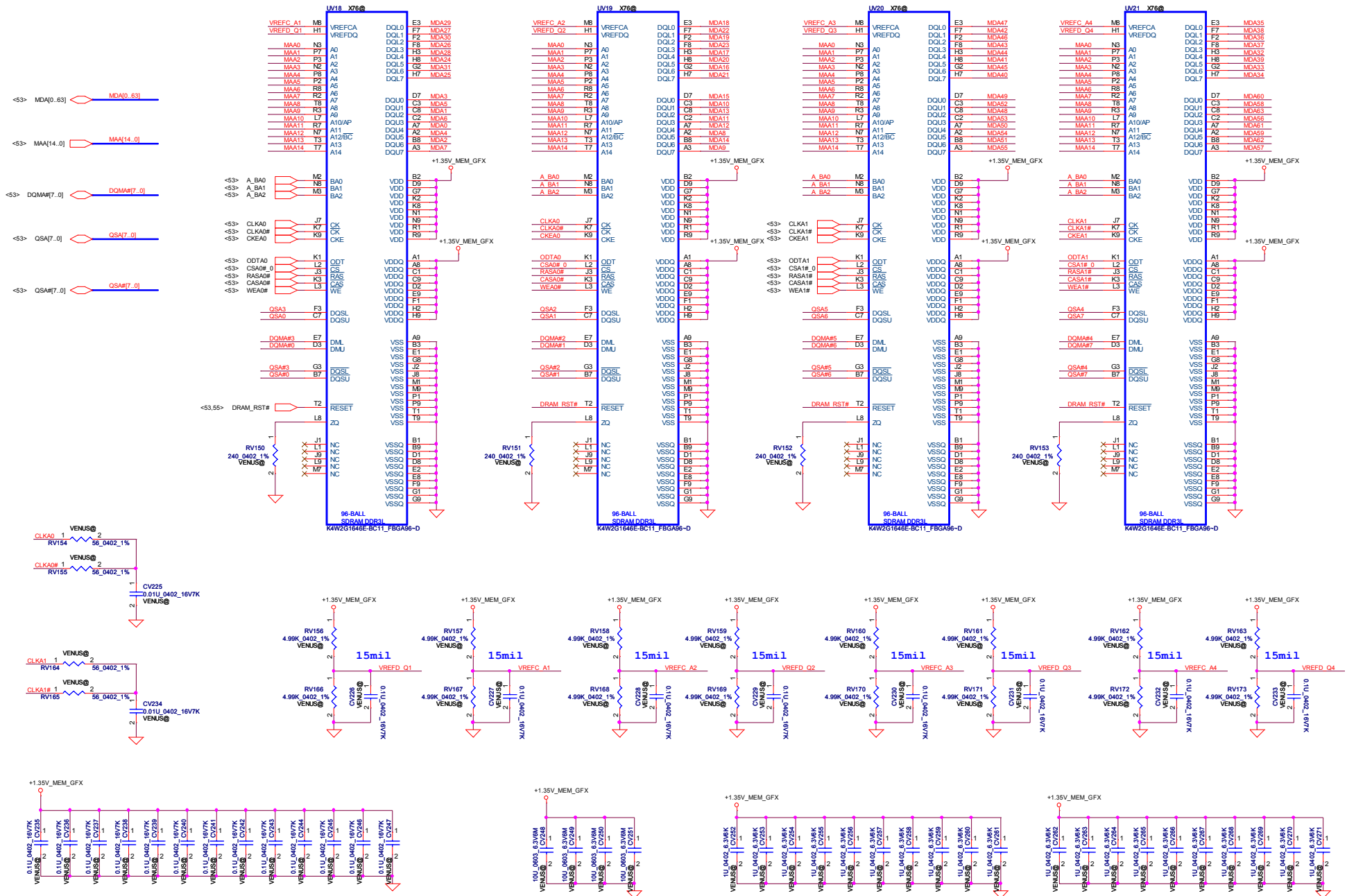
+3VS TO +3VGS



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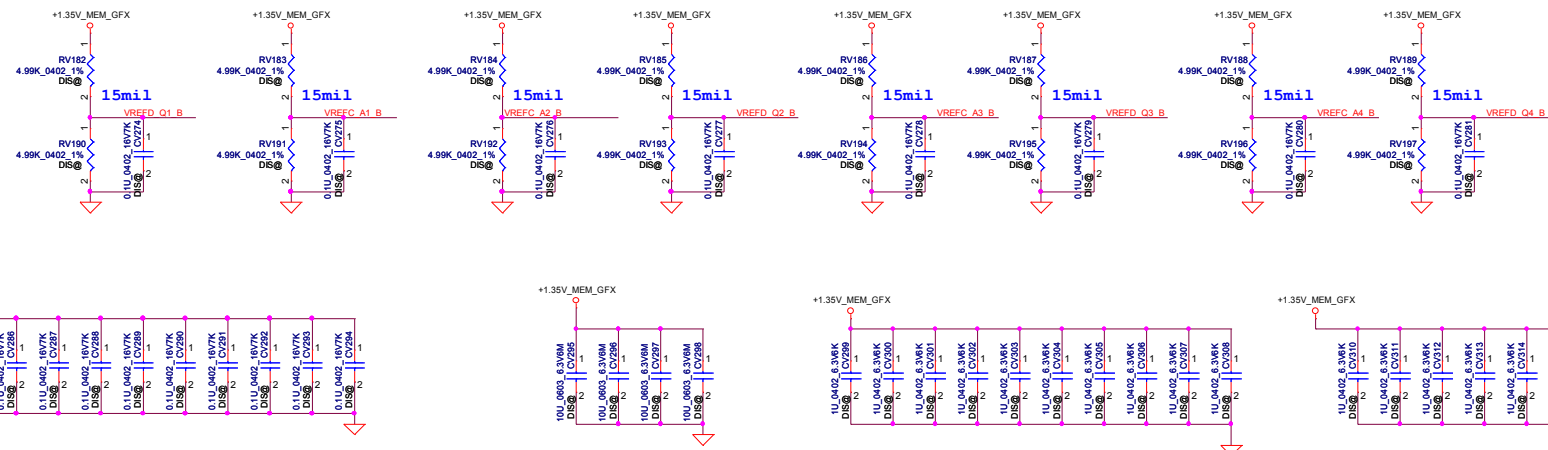
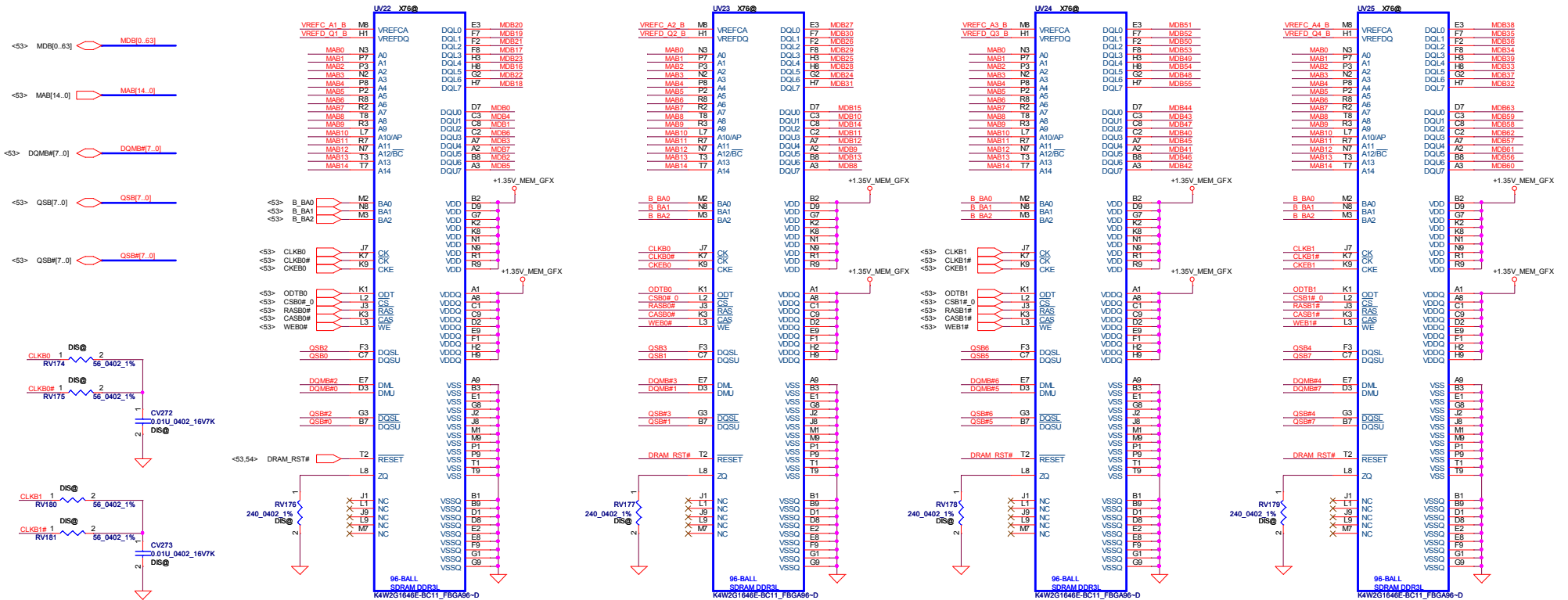


CHANNEL A: 256MB DDR3



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CHANNEL B: 256MB DDR3



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