

Compal Confidential

ZAMB0/ZAMC0 M/B Schematics Document

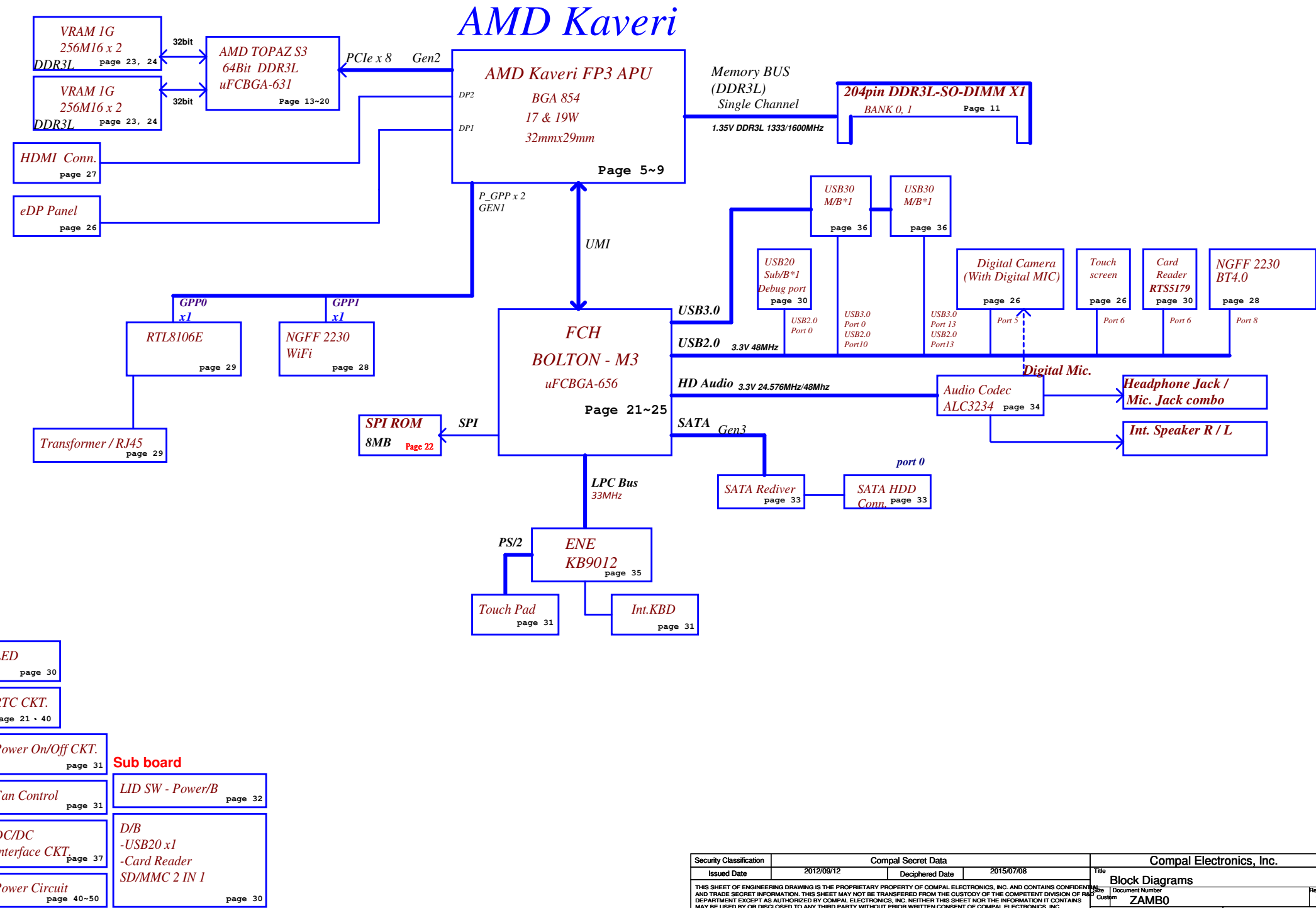
AMD Kaveri(FP3) + Bolton(M3)

AMD TOPAZ S3

2014-2-24

REV : 0.2

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/12	Deciphered Date	2015/07/08	Title	Cover Page
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Voltage Rails

Power Plane	Description	S0	S3	S4	S5
VIN	Adapter power supply (19V)	ON	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF	OFF
+APU_CORE_NB	Voltage for VDDNB	ON	OFF	OFF	OFF
+VGA_CORE	0.95-1.0V switched power rail	PX5	OFF	OFF	OFF
+VDDCI	0.95-1.0V switched power rail	PX5	OFF	OFF	OFF
+0.675VS	0.675V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+VGA_PCIE	0.95V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	AC/DC	AC/DC
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF	OFF
+1.05VS	1.05VS switched power rail for APU	ON	OFF	OFF	OFF
+1.35V	1.35V power rail for CPU VDDIO and DDR	ON	ON	OFF	OFF
+1.5VS	1.5VS switched power rail	ON	OFF	OFF	OFF
+3VGS	3.3V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.8VS	1.8V for CPU_VDDA	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	ON
+3VALW	3.3V power rail for FCH	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	WOL	WOL
+3VS_WLAN_NGFF	3.3V power rail for WLAN	ON	IOAC	IOAC	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64

BOARD ID Table

Board ID	UMA	DIS(Topaz)
0	SSI	
1		SSI
2	PT	
3		PT
4	ST	
5		ST
6	1.0	
7		1.0

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	Fintek thermal sensor	1001 101X b	9AH
Charger IC	0001 001X b	09H	SB-TSI (APU)	1001 100X b	98H
			VGA Internal Thermal	1000 001X b	82H

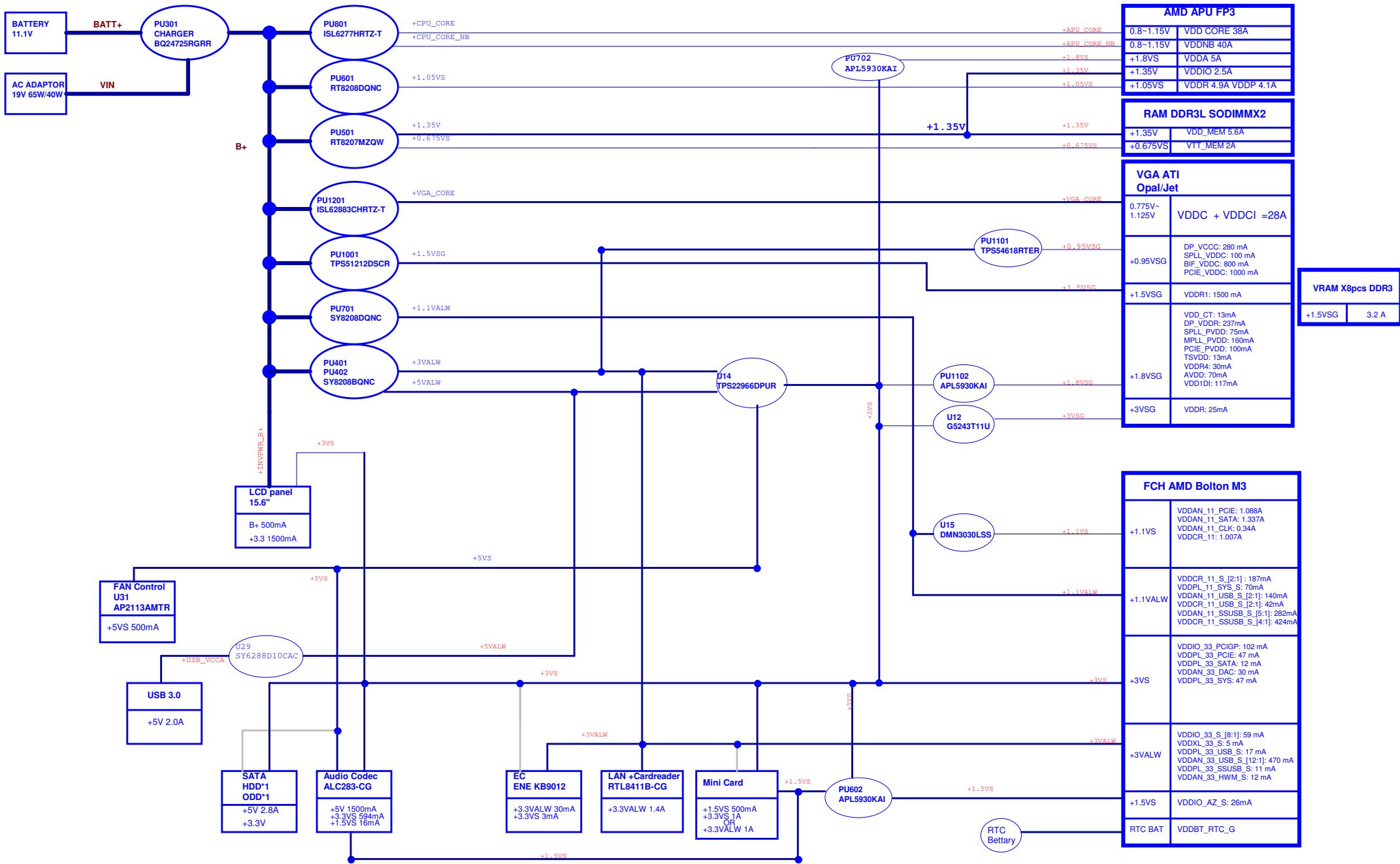
FCH SM Bus 0 address			FCH SM Bus 1 address		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	90			
MINI CARD					

BOM Option Table

BOM Structure	Description	UMA 43XX	OPAL 43XX	JET 43XX										
9022@	Use EC 9022													
9012@	Use EC 9012	V	V											
UMA@	Display output from APU (UMA only)	V	V											
VGA@	Use VGA (PX or DIS only)		V											
EDP@	Use eDP Panel		V											
AL@	Use Auto load EC code function													
AC@	Support AC Function													
NOAC@	No Support AC Function													
		V	V											
CONN@	Connector (Control by ME)	V	V											
HDT@	Debug Connector													
EMC@	EMC Component													
XEMC@	Reserve for EMC													
X76@	VRAM ID Table (Load By X76J)													
128@	VRAM x 8pcs													
OPAL@	ATI OPAL VGA CONTROLLER													
JET@	ATI JET VGA CONTROLLER													
BL@	ATI JET VGA CONTROLLER													
@	Unpop													
TS@	Touch Screen													
NEMI@	Unpop EMI													
NESD@	Unpop ESD													
AOAC@	AOAC Function													
NAOAC@	Non AOAC Function													

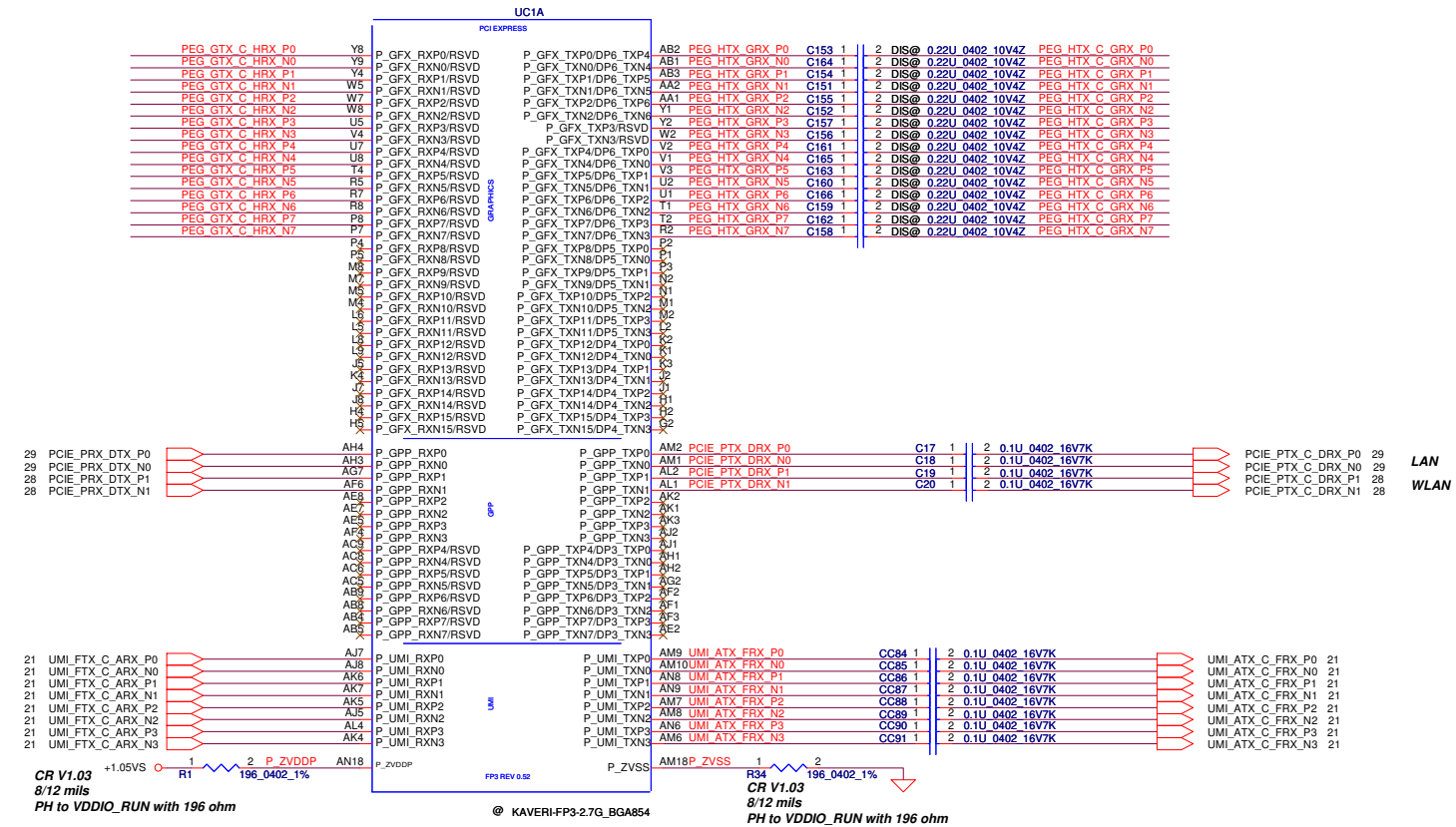
BOM Config

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13 PEG_GTX_C_HRX_P[7..0] PEG_GTX_C_HRX_P[7..0]
13 PEG_GTX_C_HRX_N[7..0] PEG_GTX_C_HRX_N[7..0]

PEG_HTX_C_GRX_P[7..0] PEG_HTX_C_GRX_P[7..0] 13
PEG_HTX_C_GRX_N[7..0] PEG_HTX_C_GRX_N[7..0] 13



A8-7100 AM7100ECH44JA 1.8G BGA 854P APU A10-7300 AM7300ECH44JA 2G BGA 854P APU FX-7500 FM7500ECH44JA 2.1G BGA 854P APU

SA00007S20L



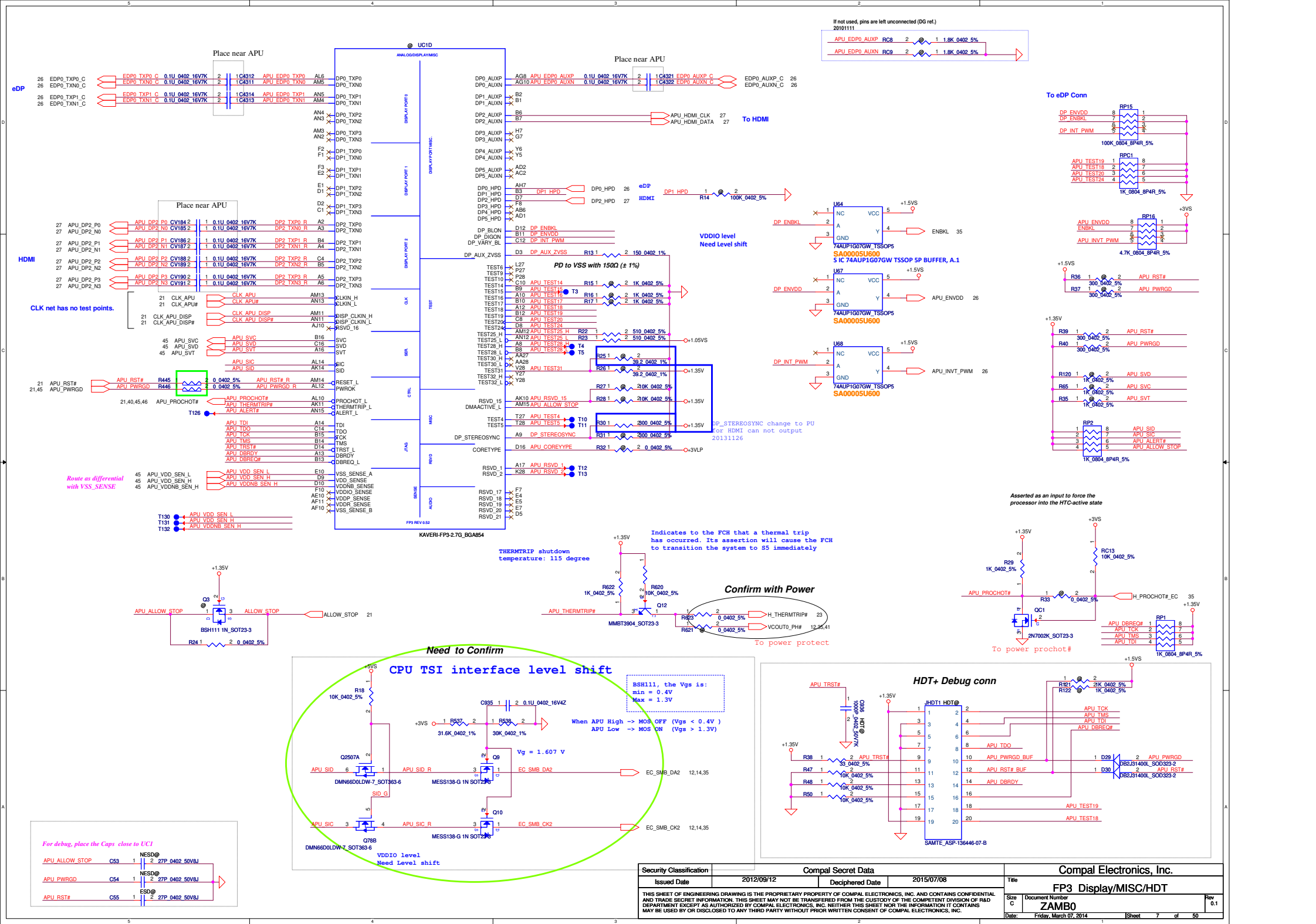
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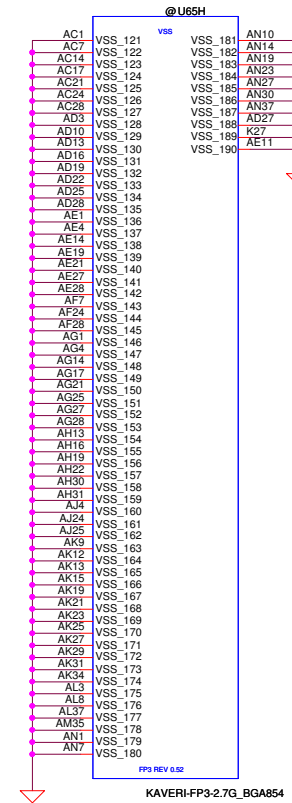
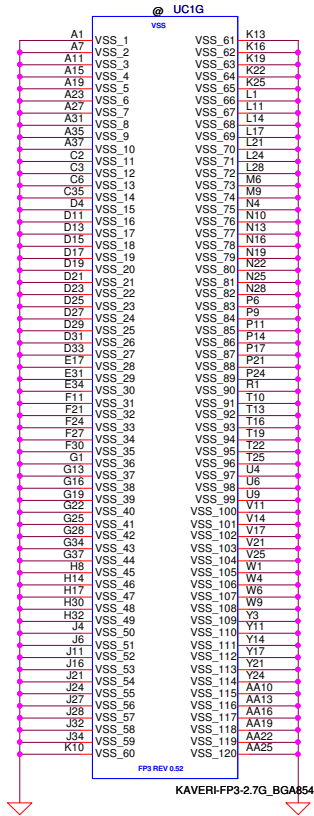
SA00007TT0L

AMD, FX-7500, KAVERI, PR	SA00007TT0L	S IC FX-7500 FM7500ECH44JA 2.1G BGA 854P APU
AMD,A10-7300, KAVERI, PR	SA00007S30L	S IC A10-7300 AM7300ECH44JA 2G BGA 854P APU
AMD A8-7100, KAVERI, PR	SA00007S20L	S IC A8-7100 AM7100ECH44JA 1.8G BGA 854P APU

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5

4

3

2

1

D

C

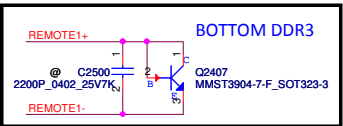
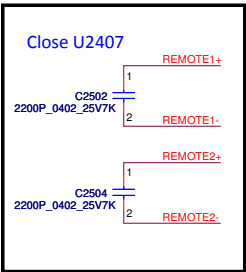
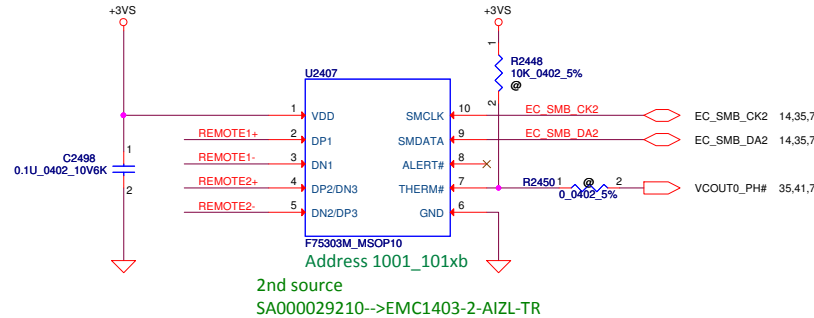
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A

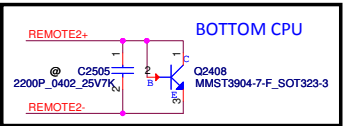
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Issued Date	2011/07/08	Deciphered Date	2015/07/08	AMD FS1R2 Singal Level Shifter	
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Fintek thermal sensor
placed near by DDR3

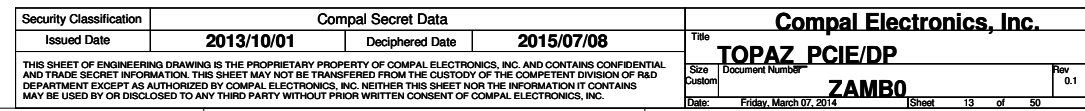
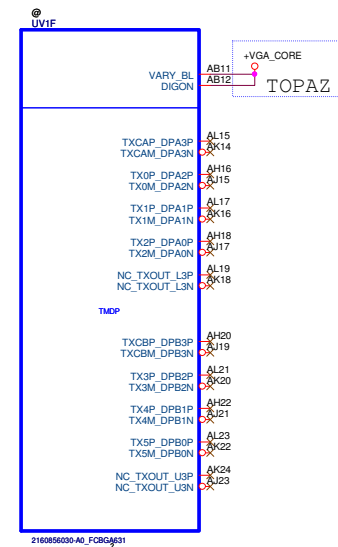
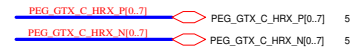
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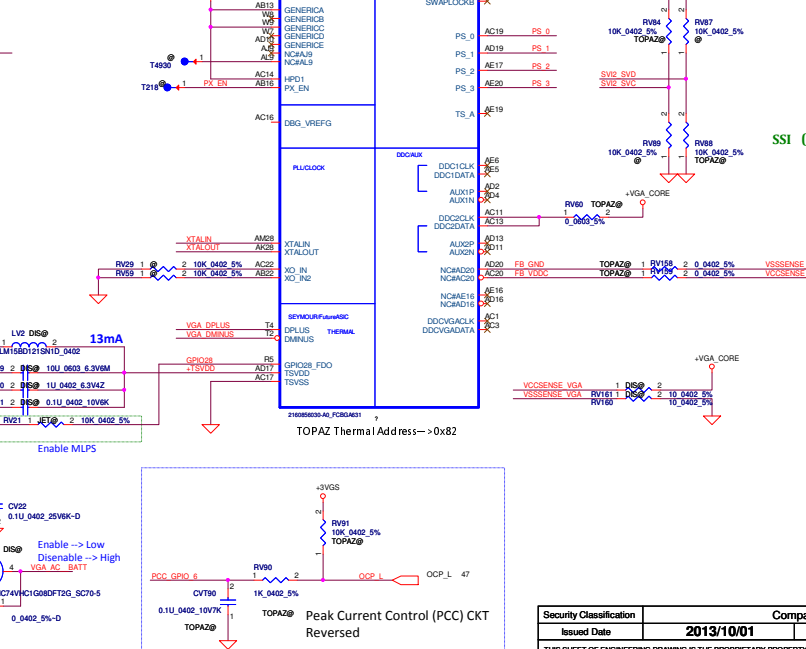
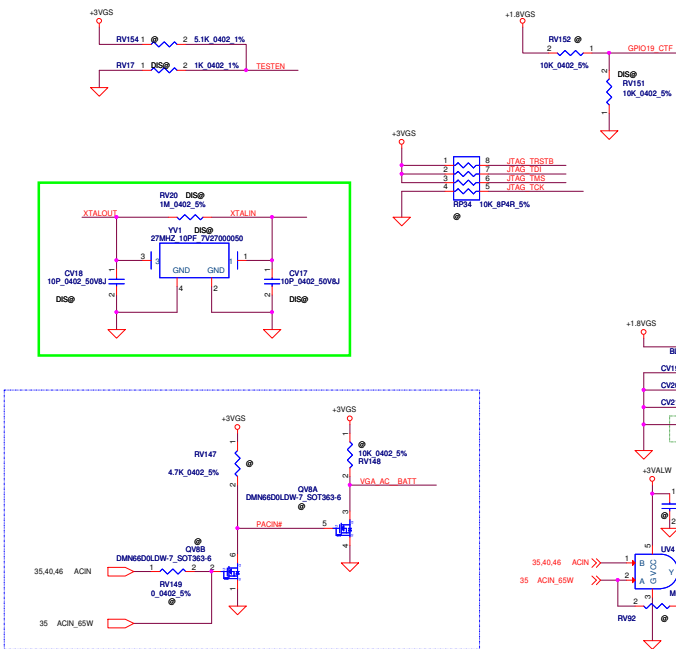


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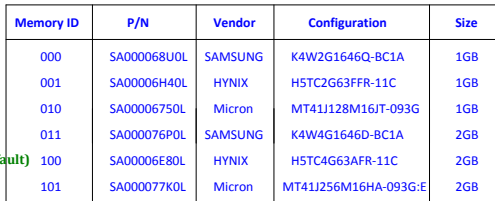


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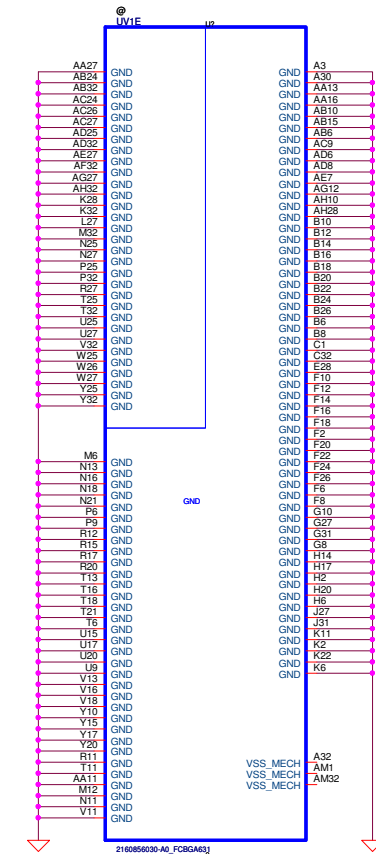


Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



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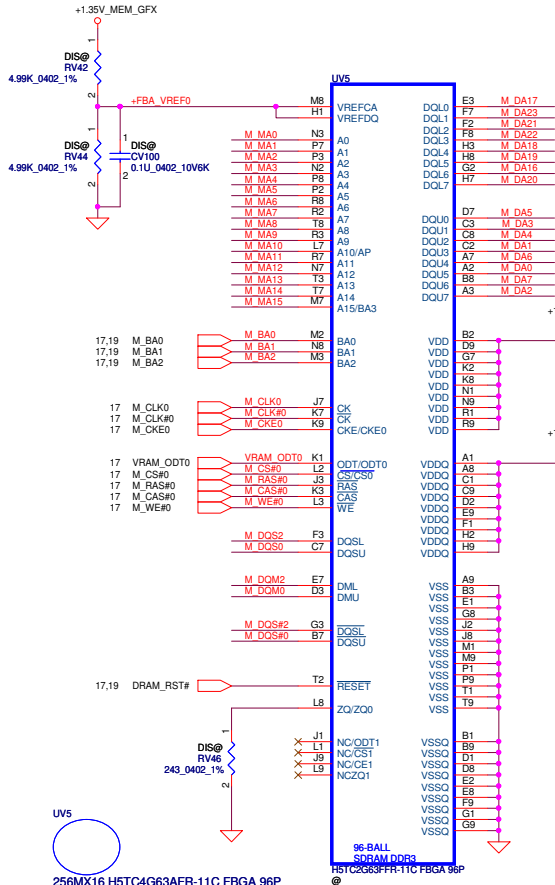
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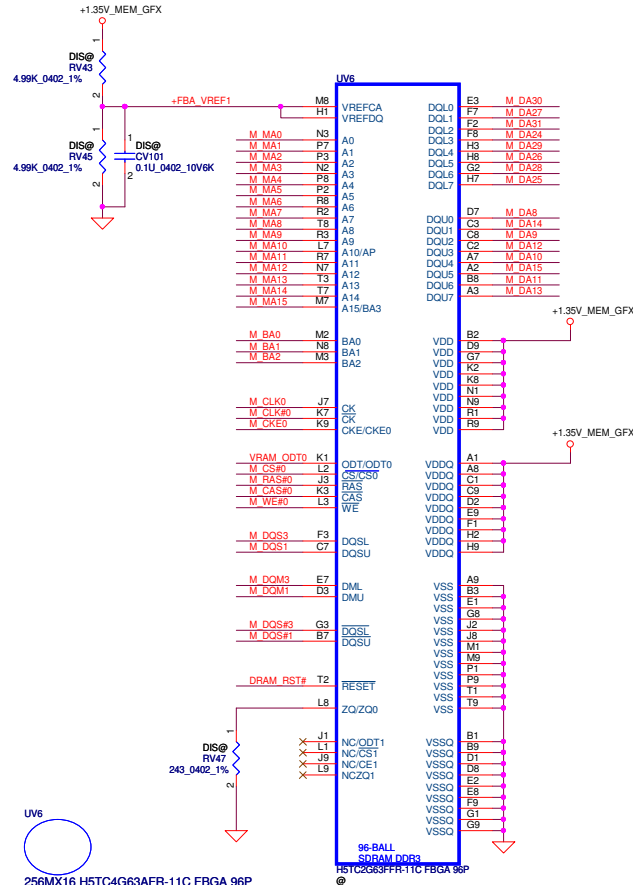
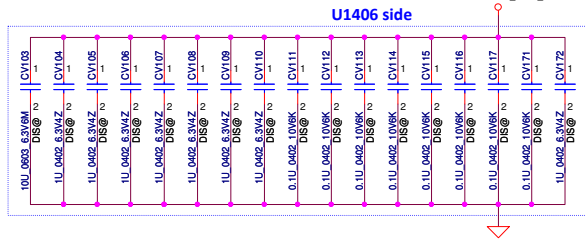
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Memory Partition A - Lower 32 bits

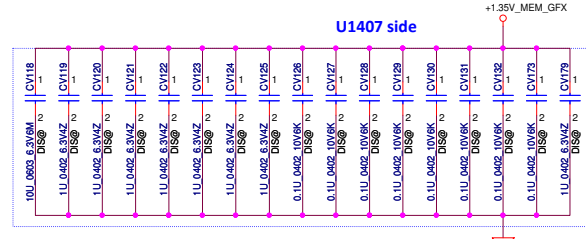
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 17,19 M_MA[15..0] M_MA[15..0]
 17,19 M_DQM[7..0] M_DQM[7..0]
 17,19 M_DQS[7..0] M_DQS[7..0]
 17,19 M_DQS#[7..0] M_DQS#[7..0]



U1406 side
 256MX16 H5TC4G63AFR-11C FBGA 96P
 SA00006E80L
 X76@



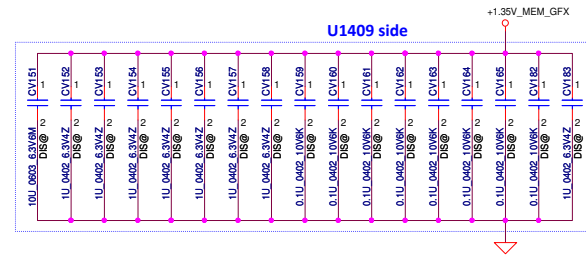
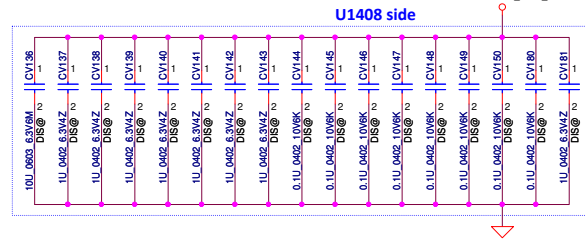
U1407 side
 256MX16 H5TC4G63AFR-11C FBGA 96P
 SA00006E80L
 X76@



X7655131104, ALT. GROUP PARTS VRAM 2G HYNIX ZAVC0, A.2 (Design)
SA00006E80L, S IC D3 256MX16 H5TC4G63AFR-11C FBGA 96P, A.1 (Design)
SD034453180, S RES 1/16W 4.53K +/-1% 0402, A.1 (Design)
SD034499180, S RES 1/16W 4.99K +/-1% 0402, A.2 (Design)
X7655131105, ALT. GROUP PARTS VRAM 2G SAMSUNG ZAVC0, A.2 (Design)
SA000076P0L, S IC D3 256MX16 K4W4G1646D-BC1A FBGA 96P, A.2 (Design)
SD000002680, S RES 1/16W 6.98K +/-1% 0402, A.1 (Design)
SD034499180, S RES 1/16W 4.99K +/-1% 0402, A.2 (Design)
X7655131106, ALT. GROUP PARTS VRAM 2G MICRON ZAVC0, A.2 (Design)
SA000077K0L, S IC D3 256MX16 MT41J256M16HA-093G:E FBGA, A.4 (Design)
SD034324180, S RES 1/16W 3.24K +/-1% 0402, A.1 (Design)
SD034562180, S RES 1/16W 5.62K +/-1% 0402, A.1 (Design)

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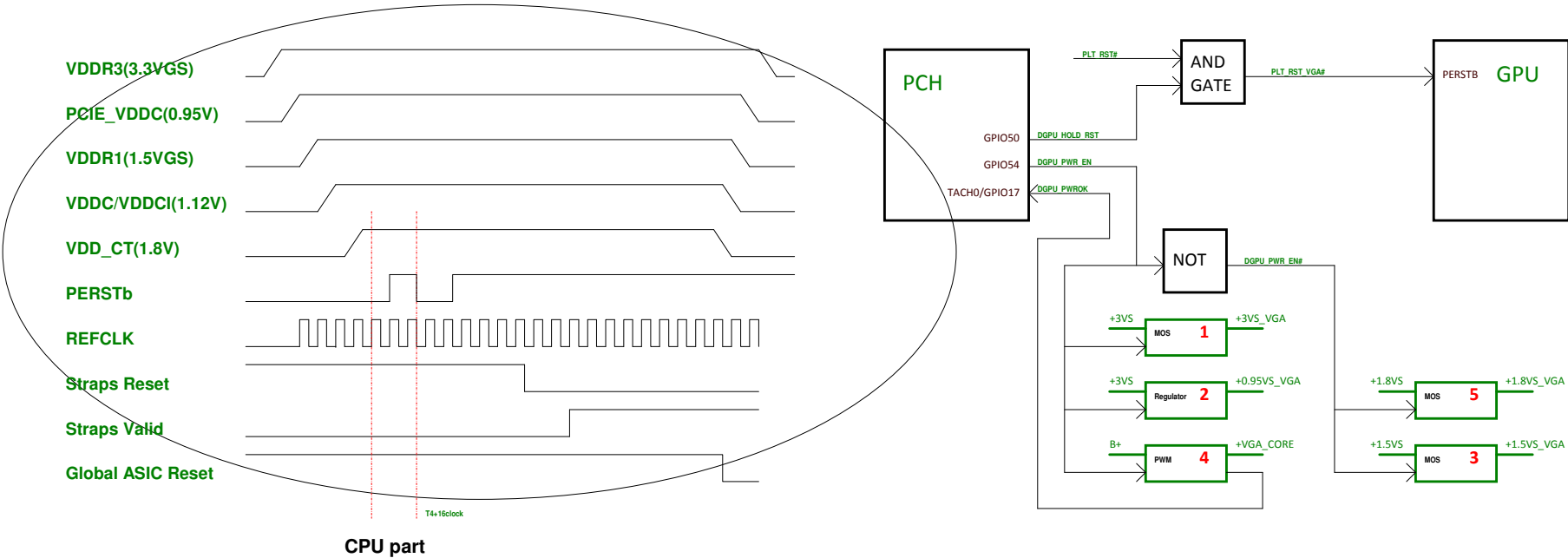
17,18	M_DA[63..0]		M_DA[63..0]
17,18	M_MA[15..0]		M_MA[15..0]
17,18	M_DQM[7..0]		M_DQM[7..0]
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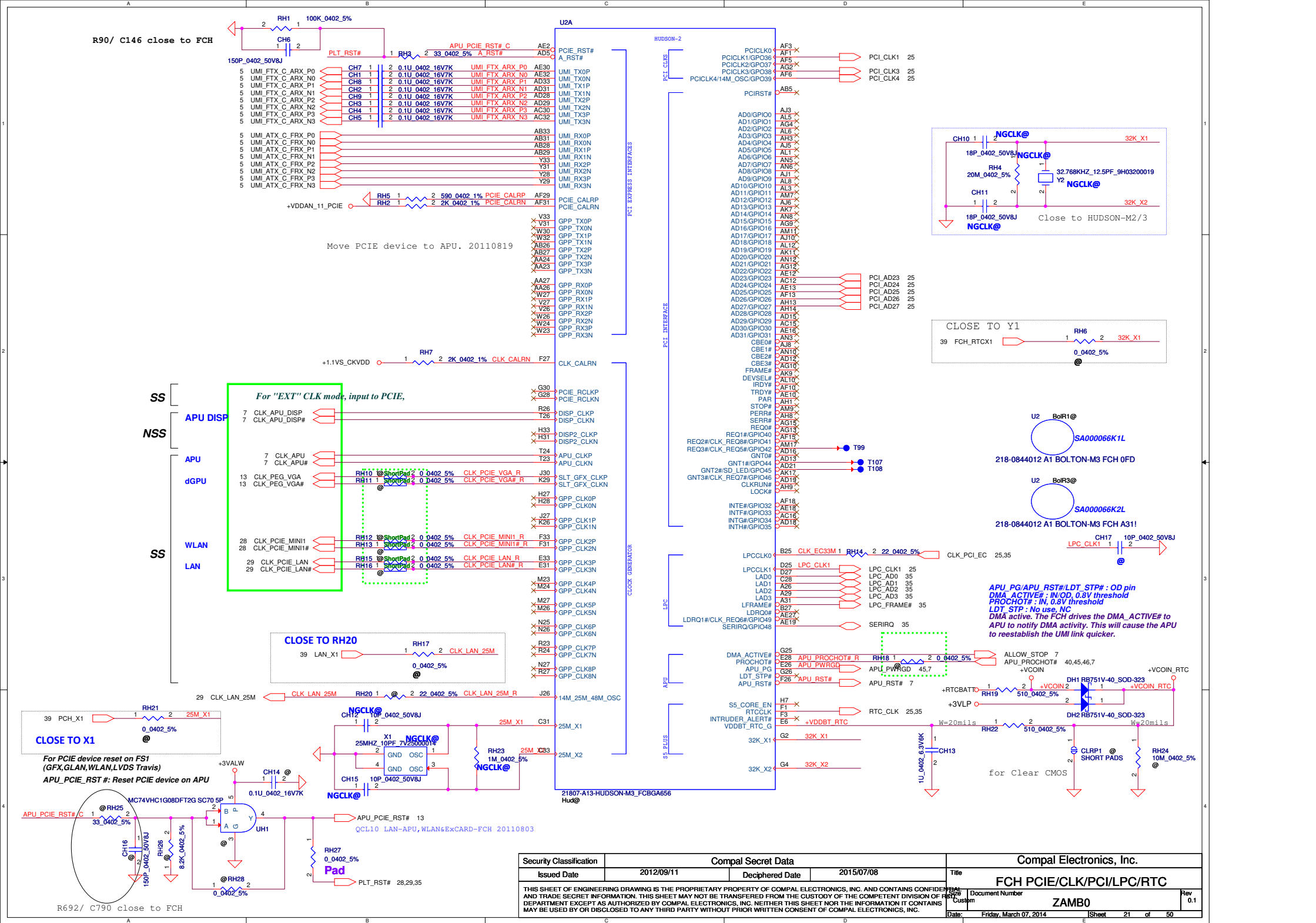


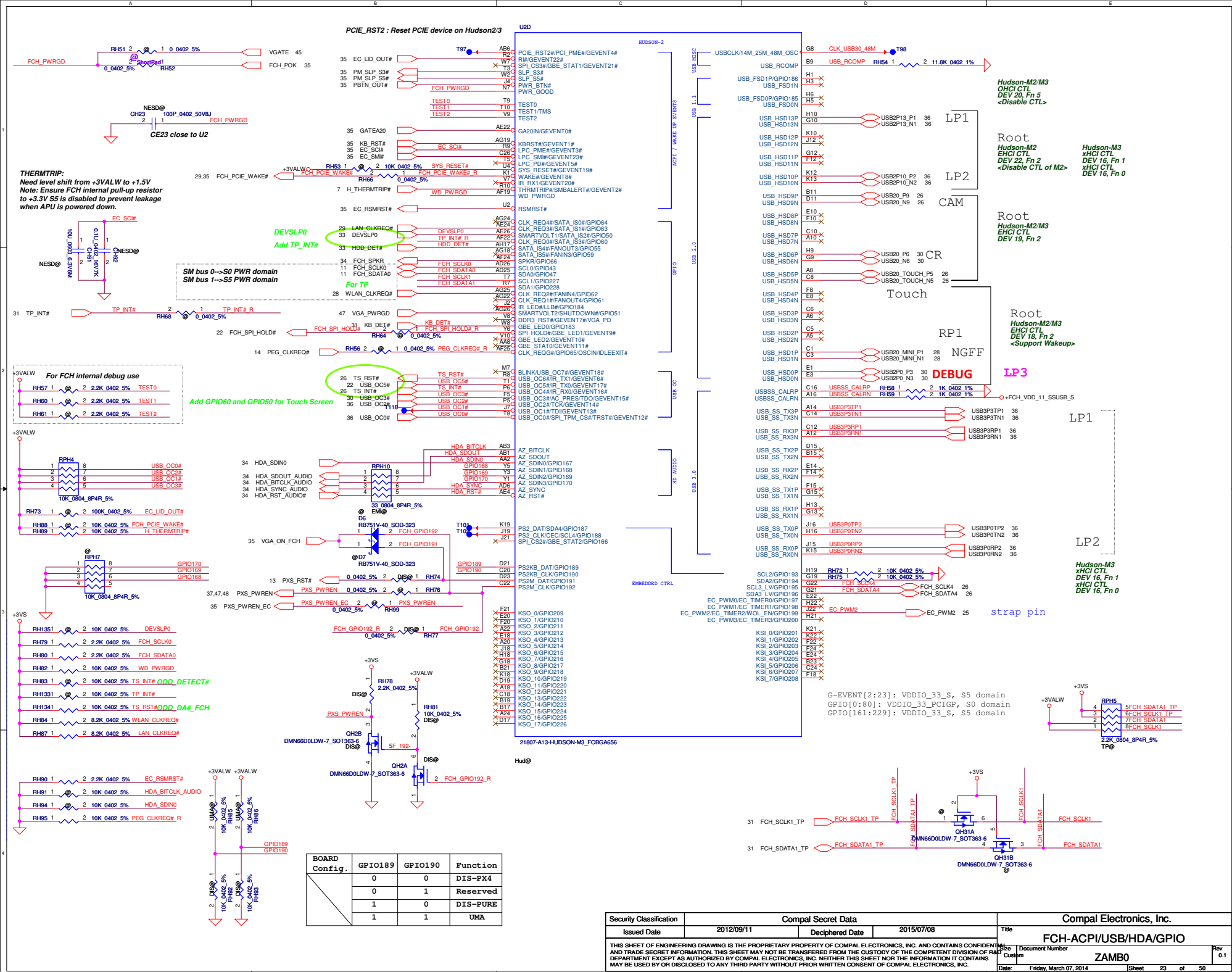
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Power-Up/Down Sequence

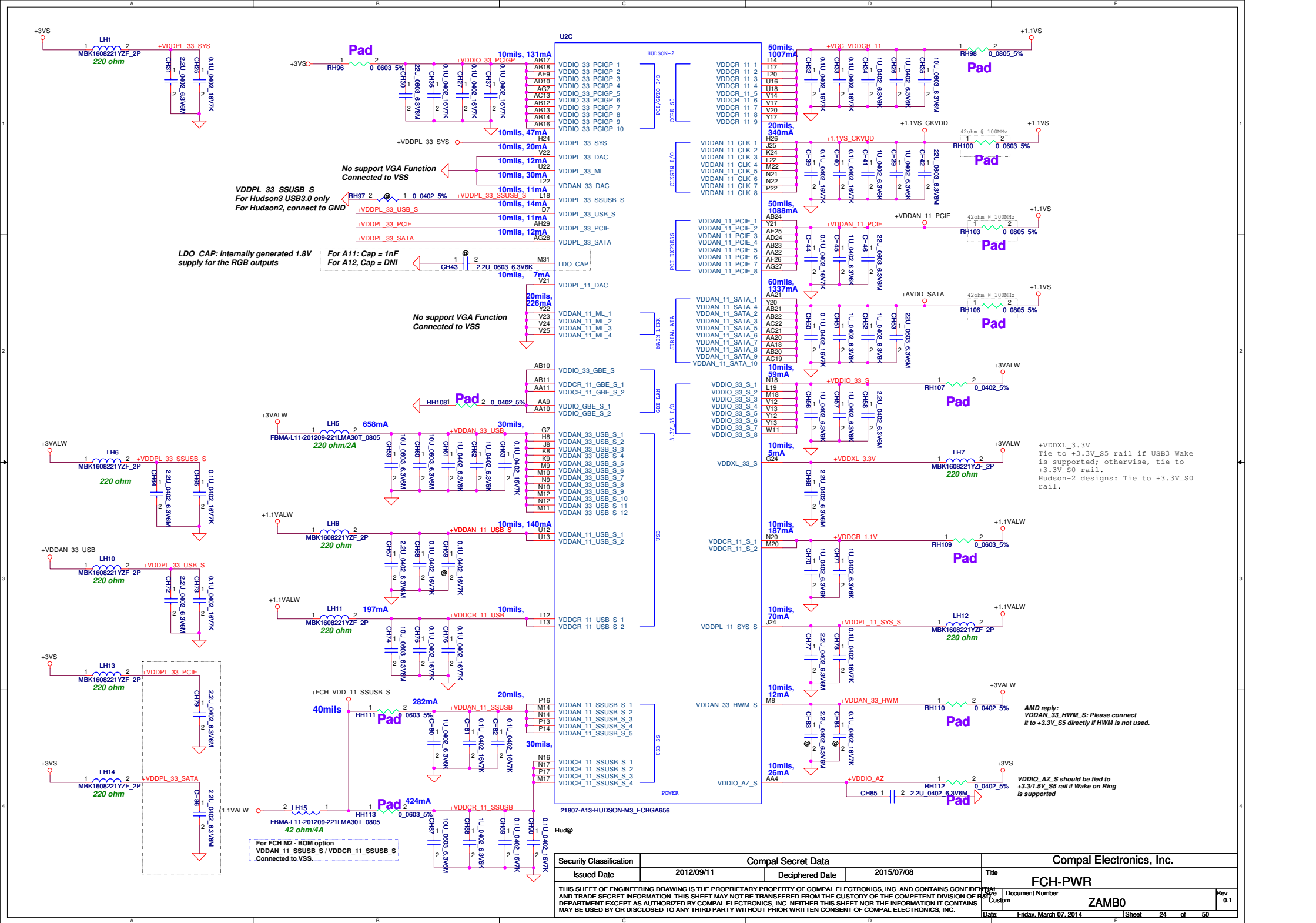
1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
4. For power down, reversing the ramp-up sequence is recommended.

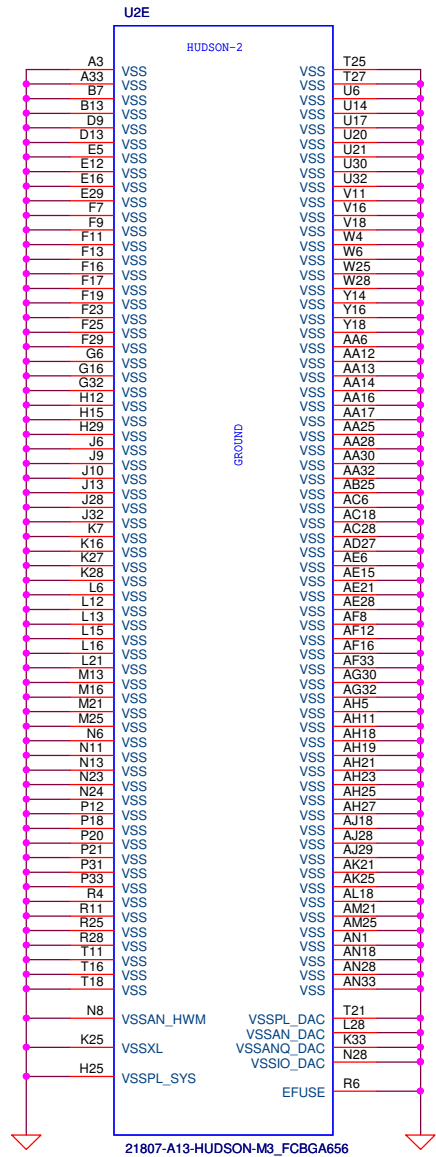






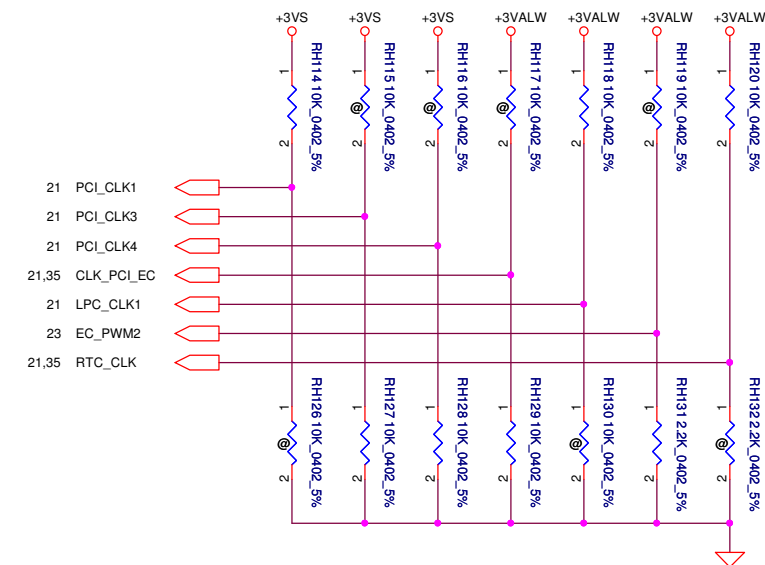
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STRAP PINS

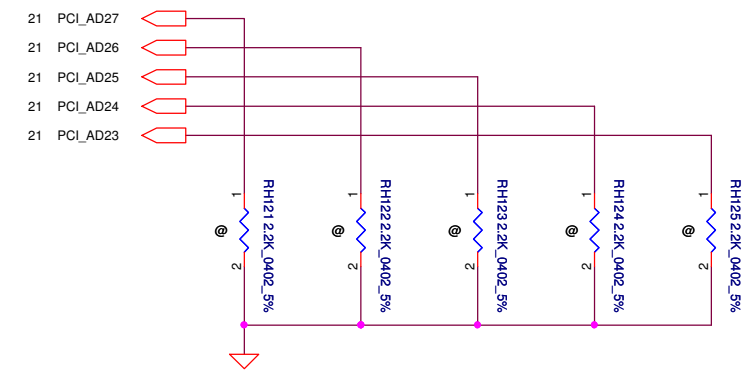
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



DEBUG STRAPS

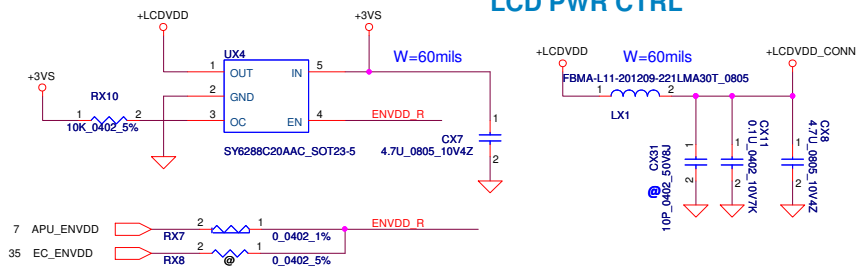
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

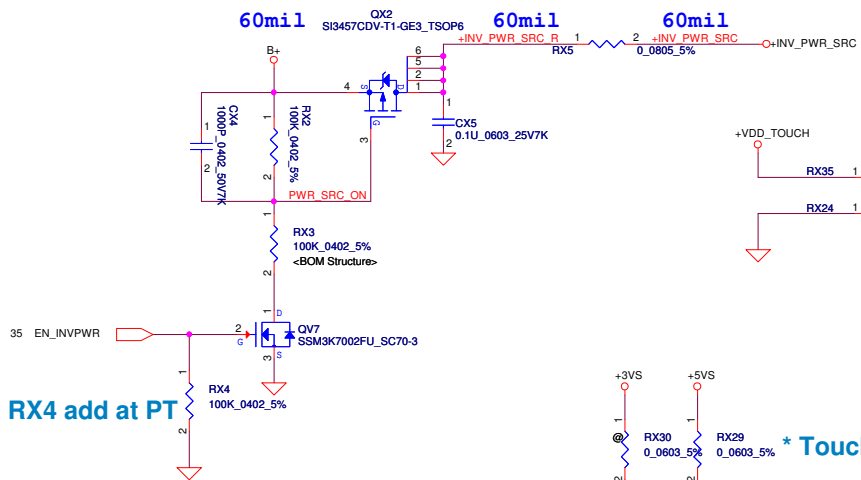


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								Size	Document Number	Rev
								B	ZAMBO	0.1
								Date:	Friday, March 07, 2014	Sheet

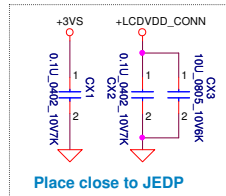
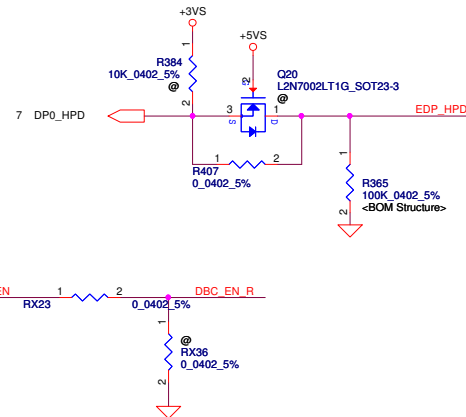
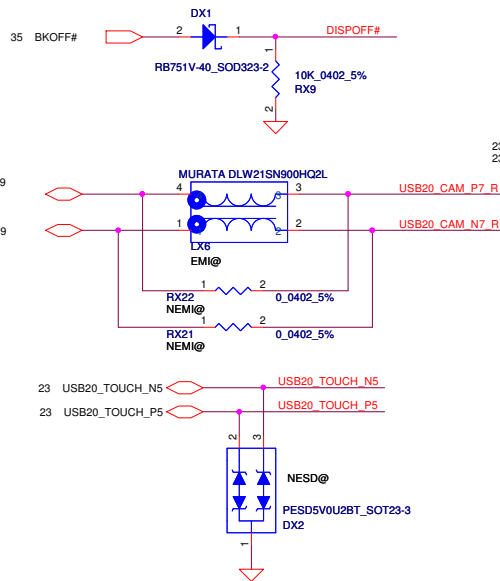
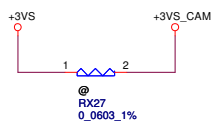
LCD PWR CTRL

SS table

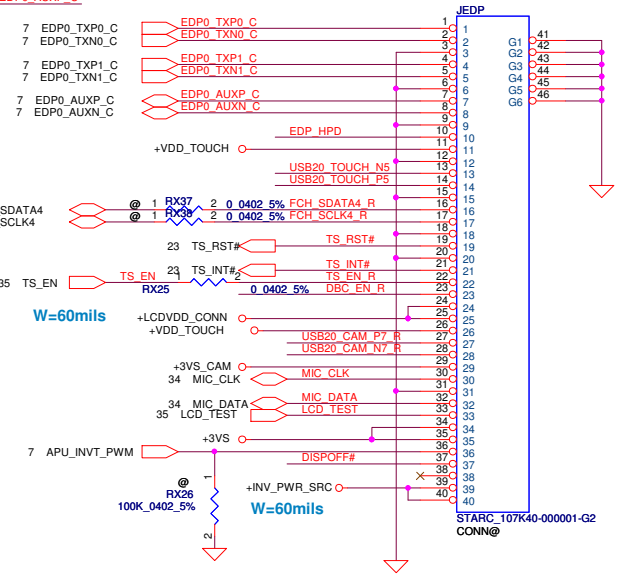
LCD backlight PWR CTRL



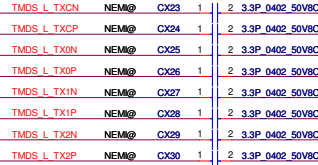
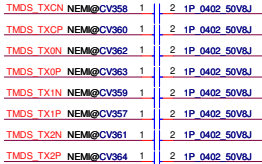
Webcam PWR CTRL



eDP Connector



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				Document Number		Rev	
				ZAMBO		0.1	
				Date: Friday, March 07, 2014		Sheet 26 of 50	



Compal Electronics, Inc.

HDMI

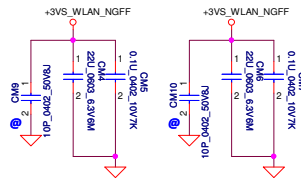
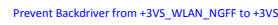
Document Number

ZAMBU

Rev

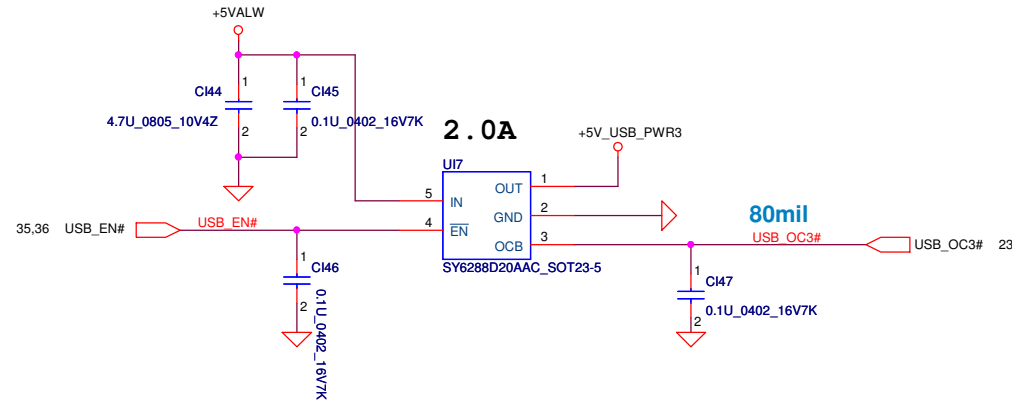
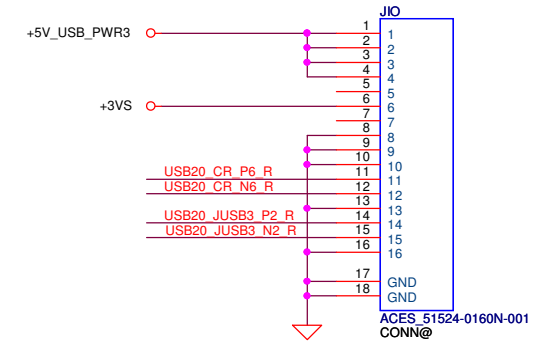
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closed to pin 64, 66

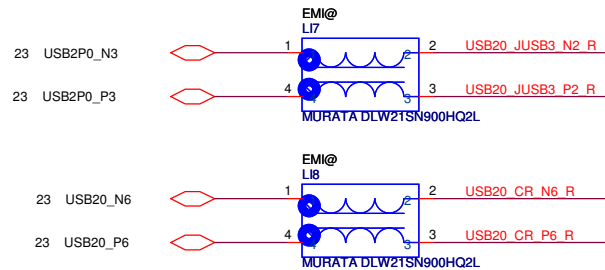
[illegible]

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						Document Number	Rev
						ZAMBO	0.1
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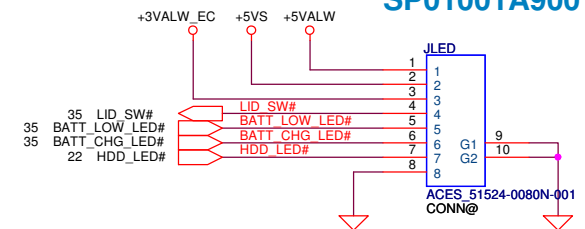
IO to MB CONN Substitute:SP01001FS00



USB Conn DEBUG Port



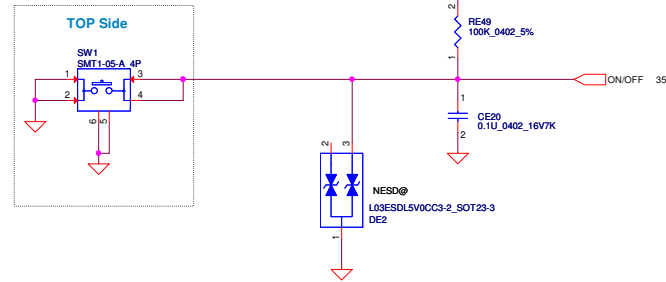
LED/B TO M/B SP01001A900



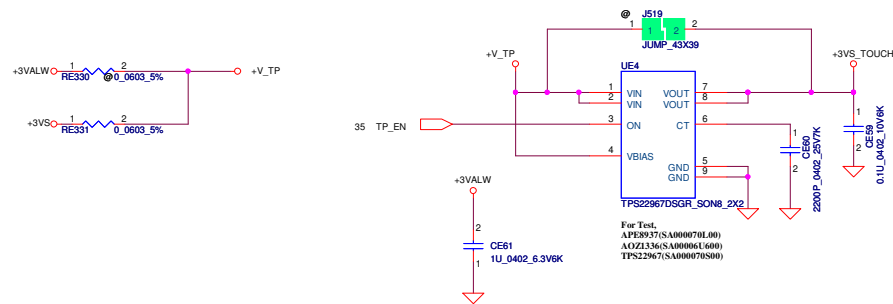
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Issued Date				2013/10/01		Deciphered Date		2015/07/08		Size	
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Power ON Circuit

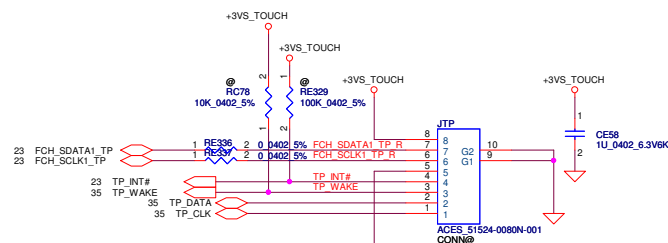
ON/OFF switch



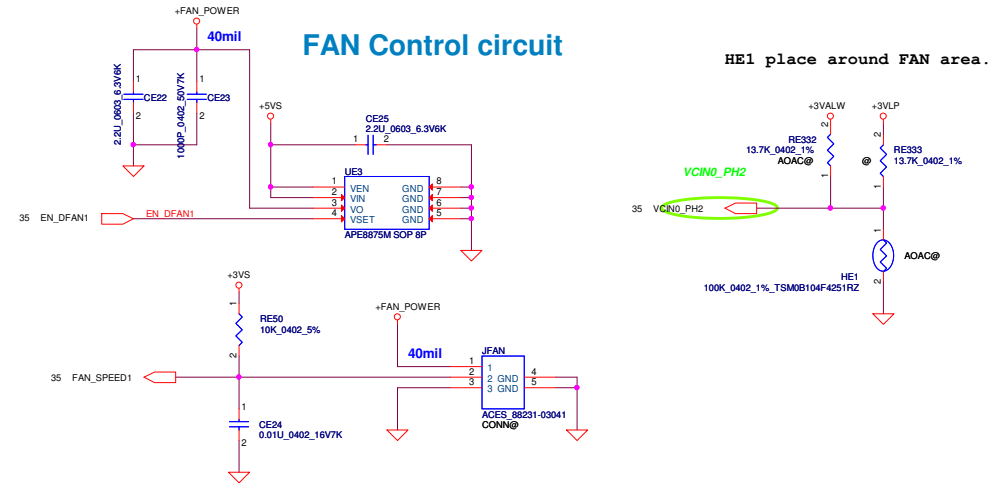
J519 short



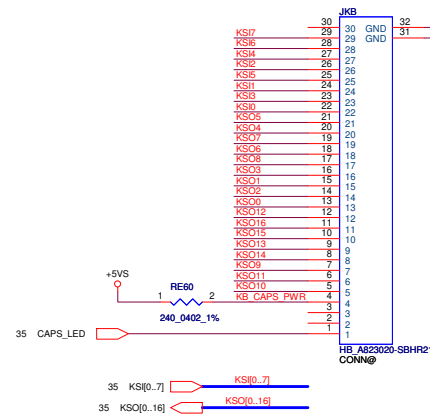
Touch pad PS/2 only



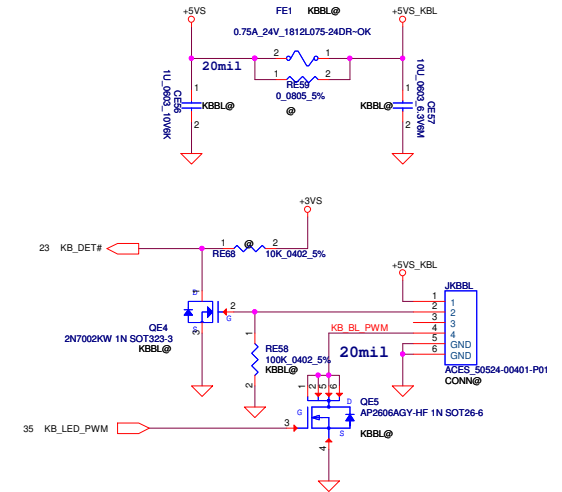
FAN Control circuit



INT_KBD Connector



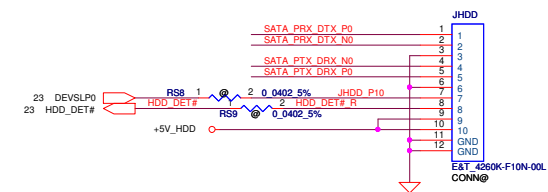
* Key Board Back Light



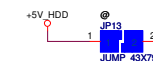
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Issued Date		Deciphered Date		FAN / TP / PWR SW / KBBL	
2013/10/01		2015/07/08		Document Number	
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				Custom	ZAMB0	0.1
				Date:	Friday, March 07, 2014	Sheet 32 of 50

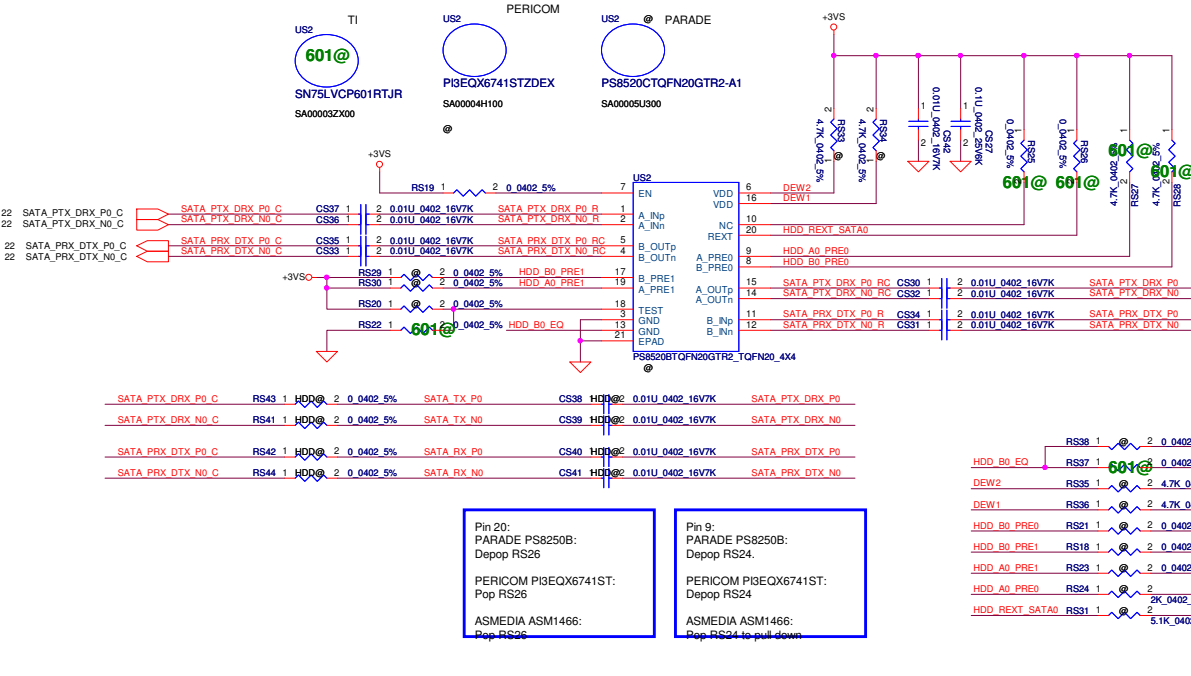
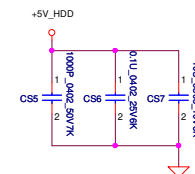
SATA HDD Connector



+5V_HDD Source



SHORT DEFAULT



Pin 20: PARADE PS8250B: Depop RS26	Pin 9: PARADE PS8250B: Depop RS24
PERICOM PI3EQX6741ST: Pop RS26	PERICOM PI3EQX6741ST: Depop RS24
ASMEIA ASM1466: Pop RS26	ASMEIA ASM1466: Pop RS24 to pull down

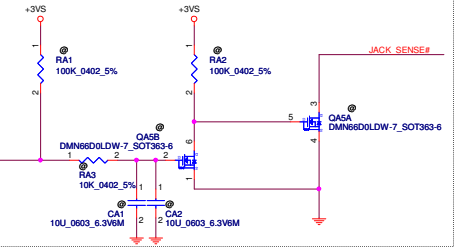
CA71, CA51 place close to Pin 26

CA53, CA55 change Value from 10U_0603_6.3V6M to 4.7U_0603_6.3V6K

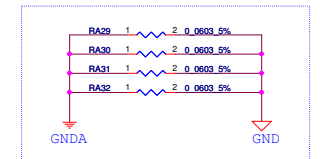
CA57, CA58 close to UA1 pin1

CA59 CA60 close to UA1 pin9

JACK_PLUG Delay circuitis

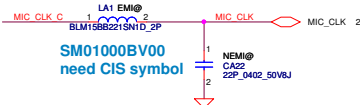
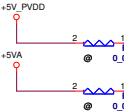
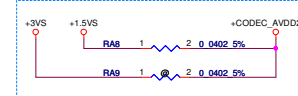


Reserve for cancel Delay circuitis

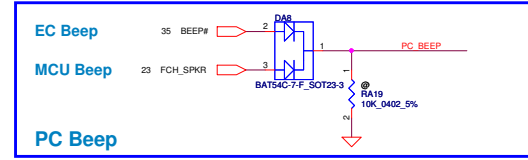


Place on the moat between GND & GNDA.

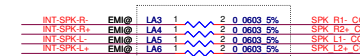
Reserve for HDA issue



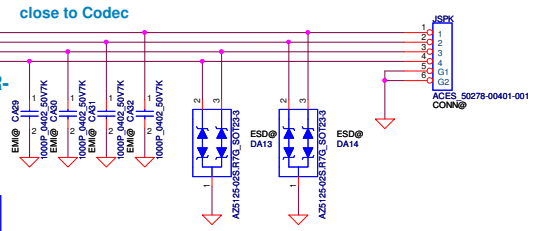
SM01000BV00 need CIS symbol



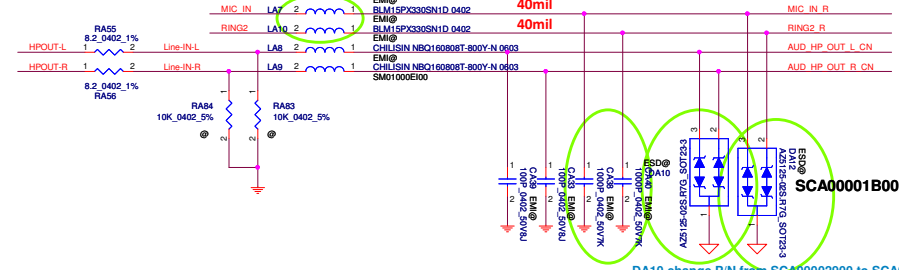
Close to UA1 Pin11,13,14,16



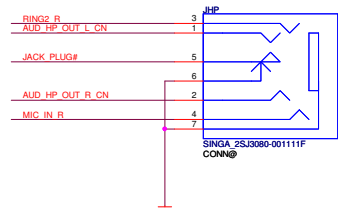
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil



iPhone and Nokia type Combo Jack

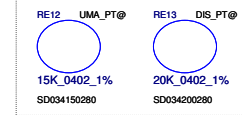


DA10 change P/N from SCA00002900 to SCA00001A00

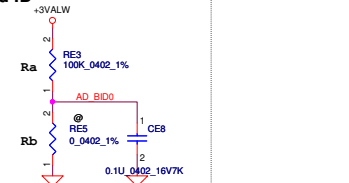


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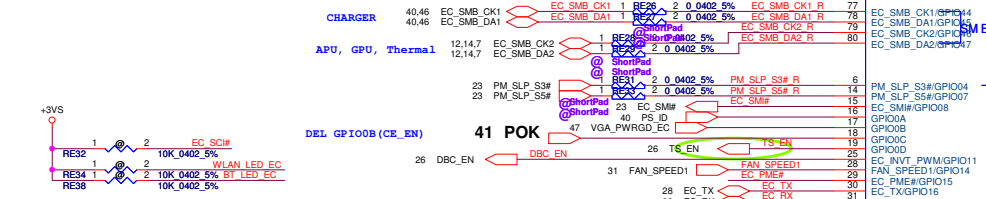
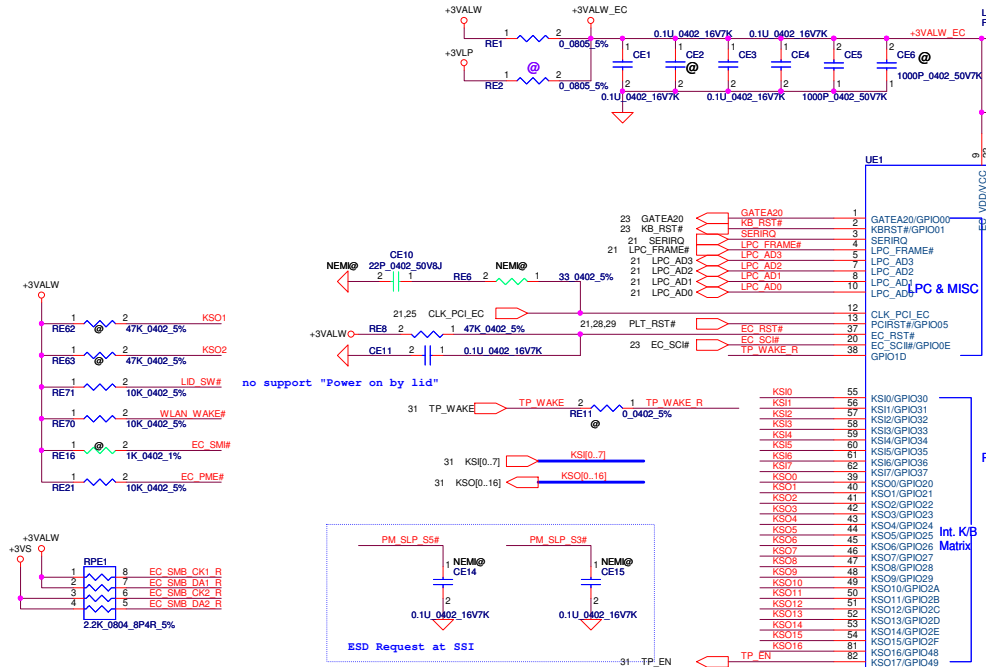
DVT- Build



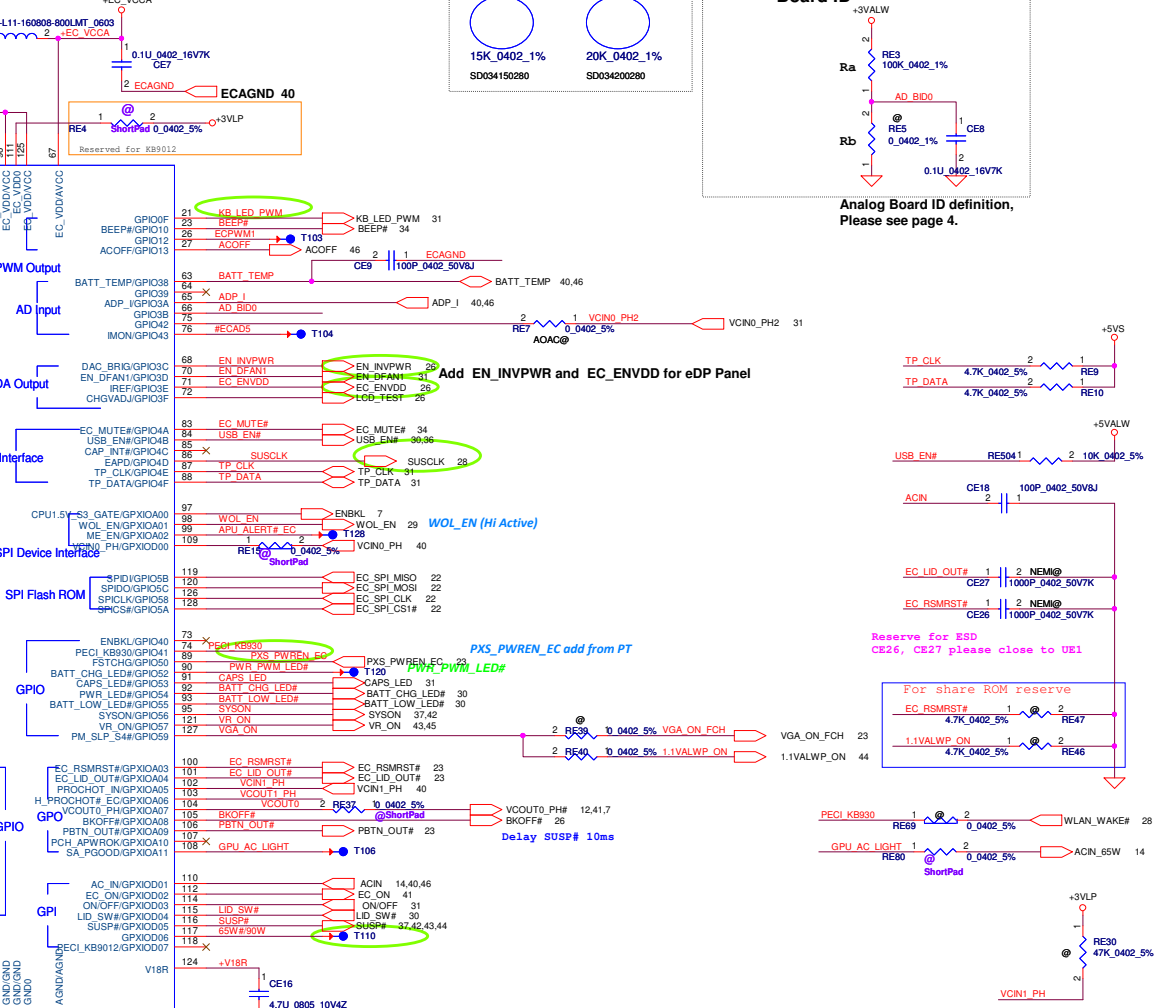
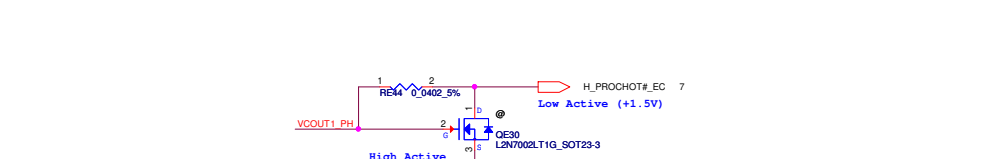
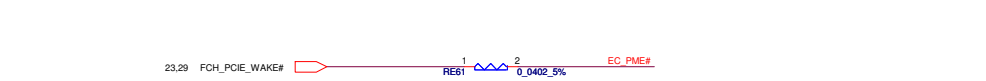
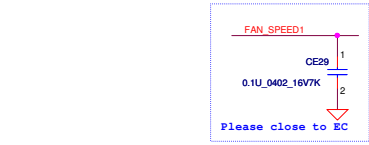
Board ID



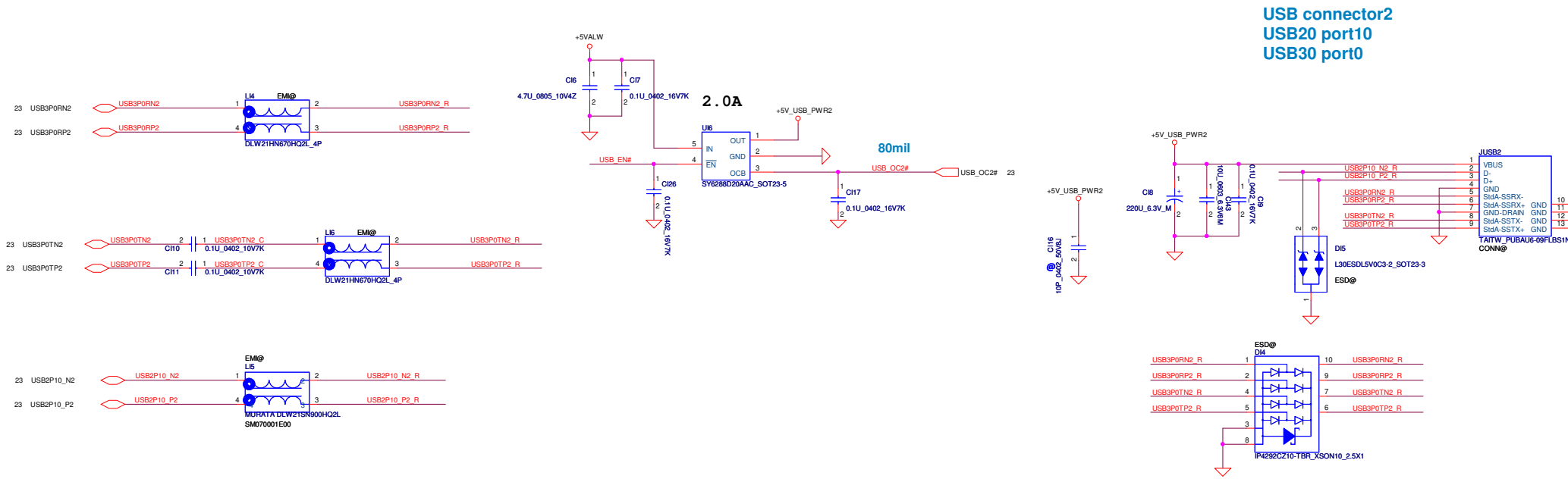
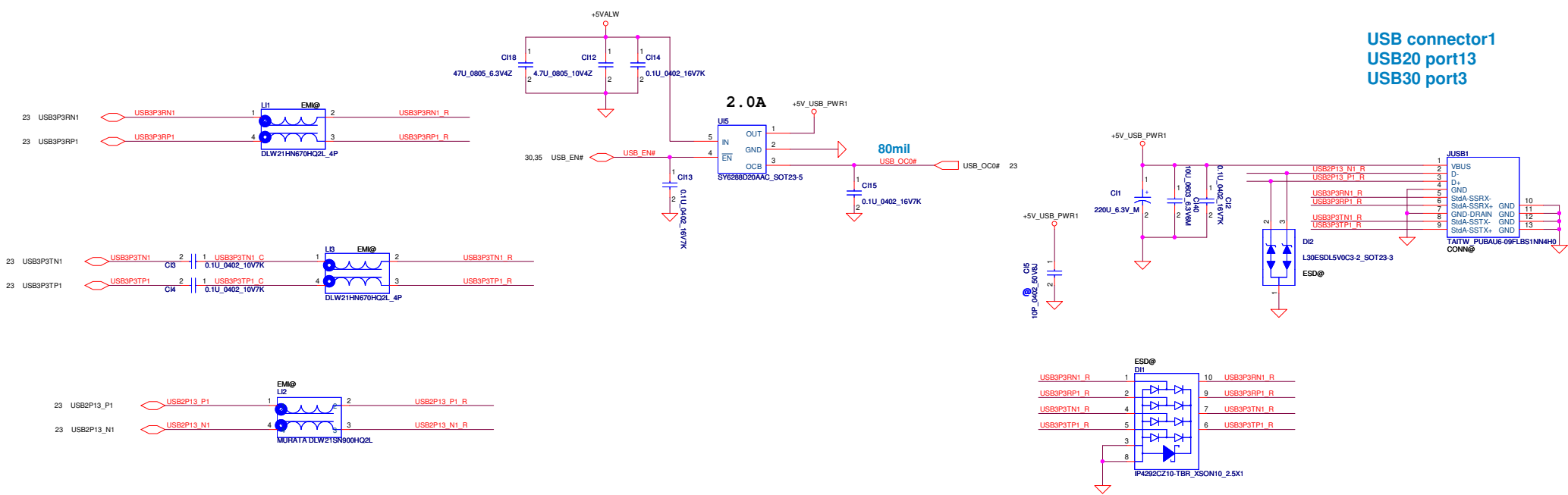
Analog Board ID definition,
Please see page 4.



RE34, RE38
Please Close to UE1

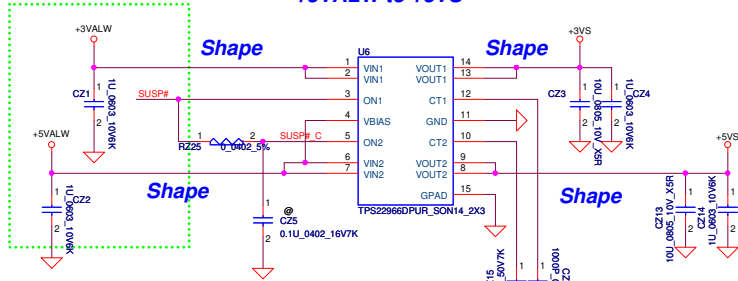


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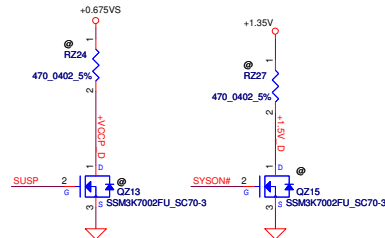
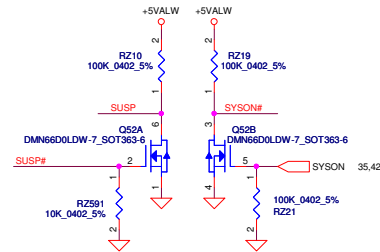


+5VALW to +5VS
+3VALW to +3VS

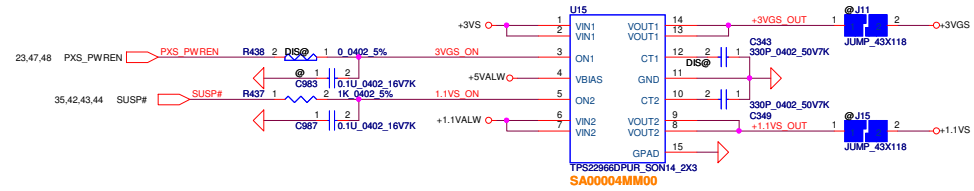
CZ3, CZ13 Change to H=0.85mm



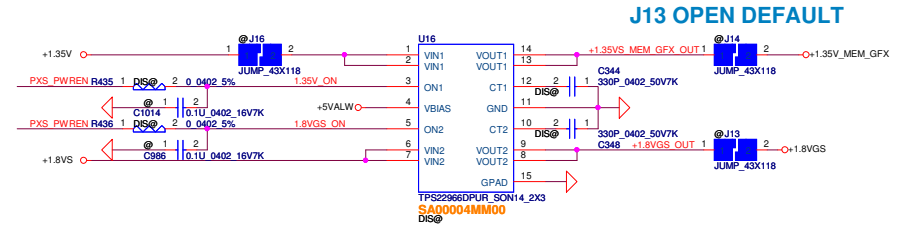
CTx (pF)	RISE TIME (µs)	
	5V	3.3V
0	124	88
220	481	323
470	855	603
1000	1724	1185
2200	3328	2240
4700	7459	4950
10000	16059	10835



+1.1VALW to +1.1VS
+3VS to +3VGS

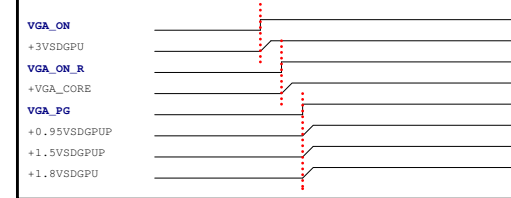


+1.35V to +1.35VS_MEM_GFX_OUT
+1.8VS to +1.8VSDGPU

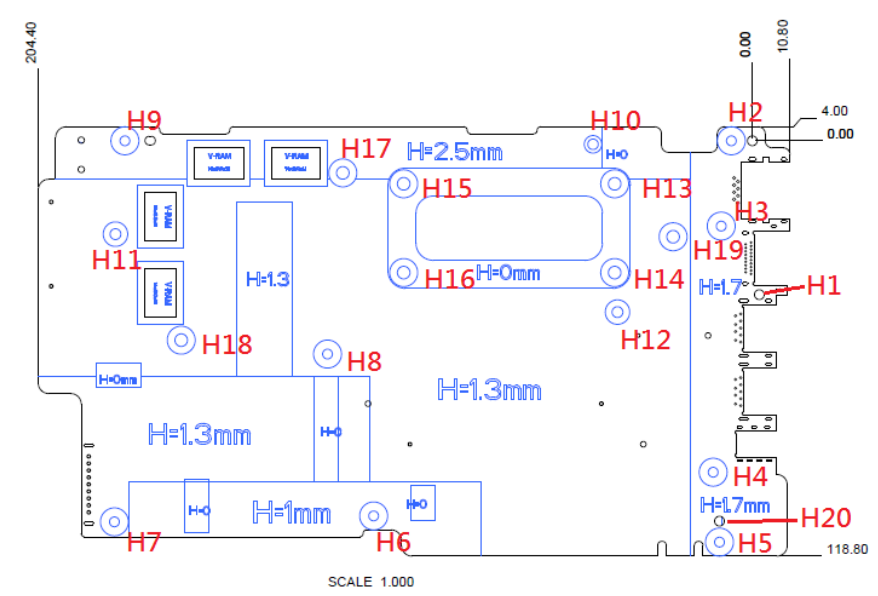
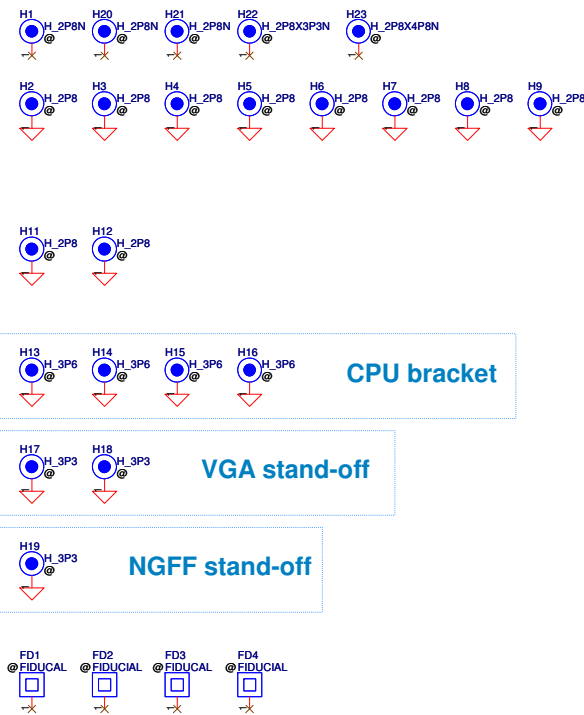


J13 OPEN DEFAULT

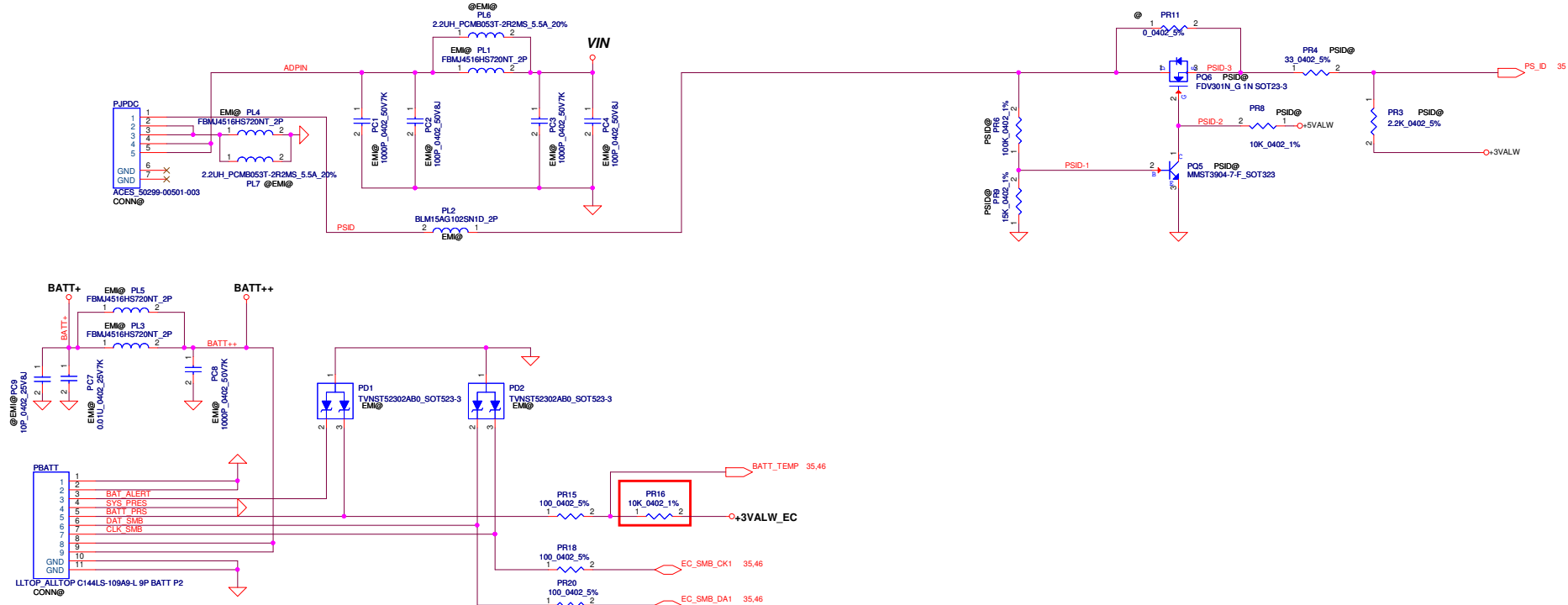
VGA sequence : default same as V5WE2
(0.95V can be option before VGA CORE)



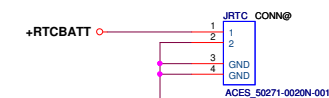
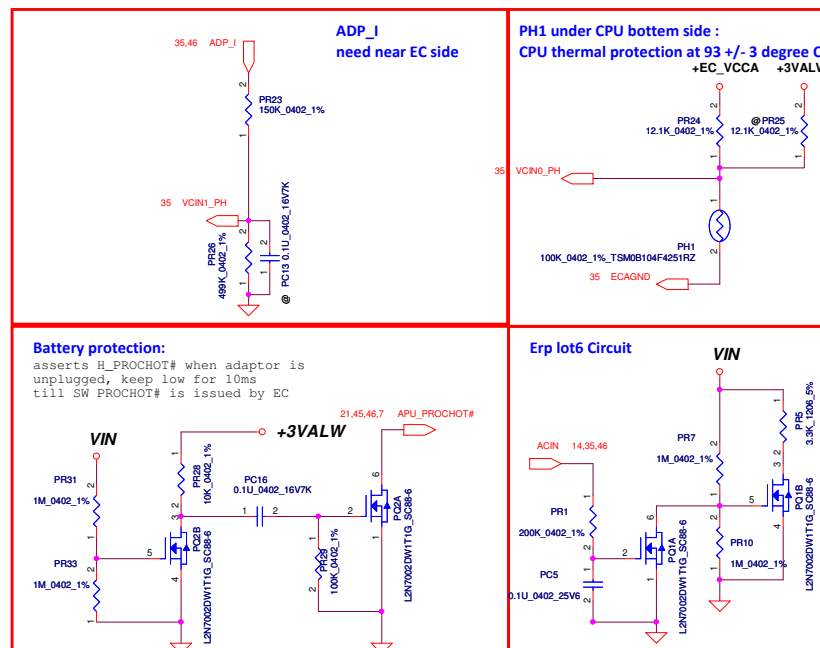
Screw Hole



**SMART
Battery:**
01.GND1
02.GND2
03.BAT_ALERT
04.SYS_PRES
05.BATT_PRS
06.DAT_SMB
07.CLK_SMB
08.BATT1 +
09.BATT2 +



Other component (37.1)

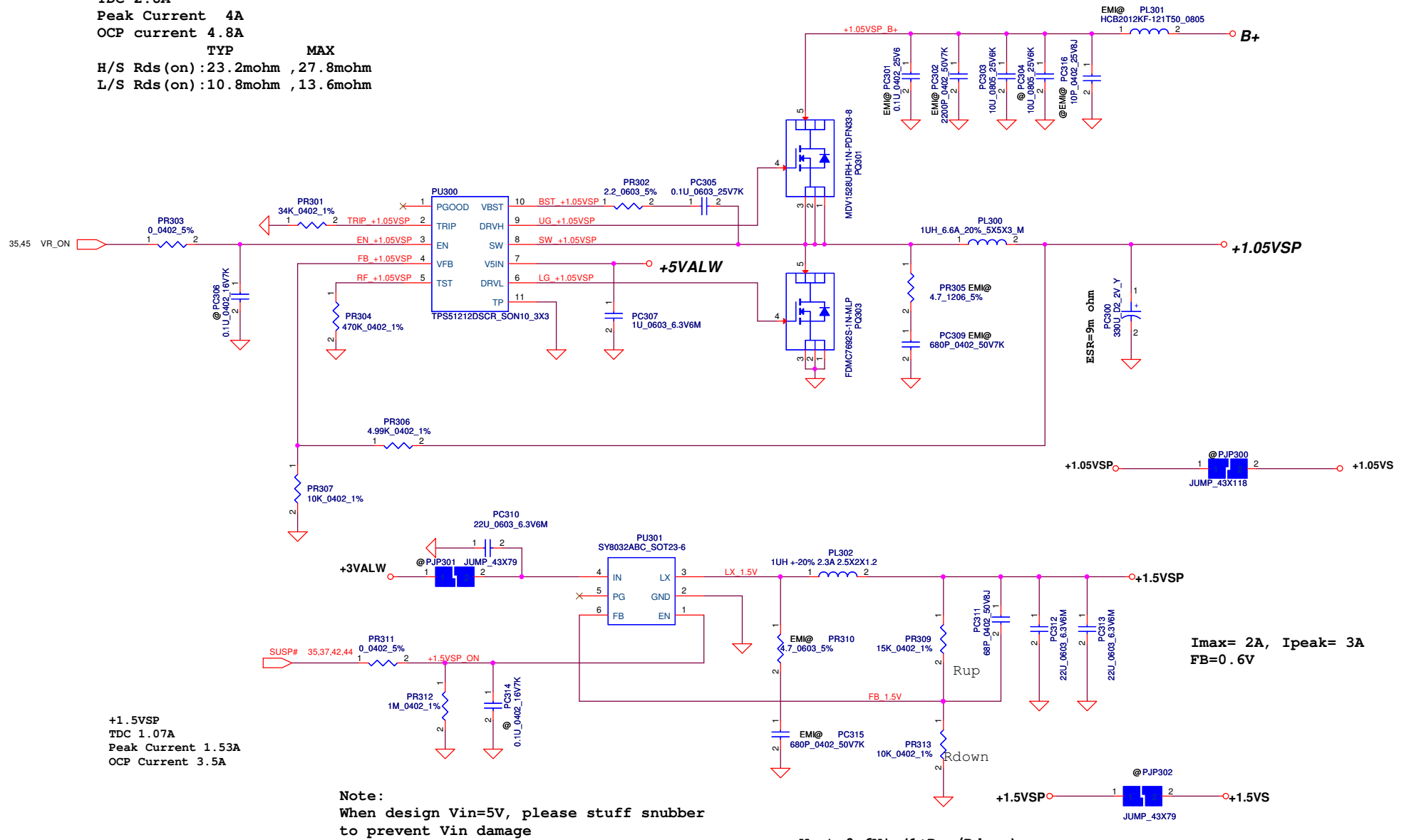


DELL CONFIDENTIAL/PROPRIETARY

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1.05VSP
TDC 2.8A
Peak Current 4A
OCP current 4.8A

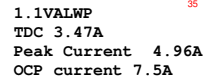
TYP MAX
H/S Rds (on) : 23.2mohm , 27.8mohm
L/S Rds (on) : 10.8mohm , 13.6mohm



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Issued Date	2011/07/29	Deciphered Date		PWR +1.05VSP +1.5VSP	
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				ZAMBO	
				Date:	Friday, March 07, 2014
				Sheet	43 of 50
				Rev	0.1

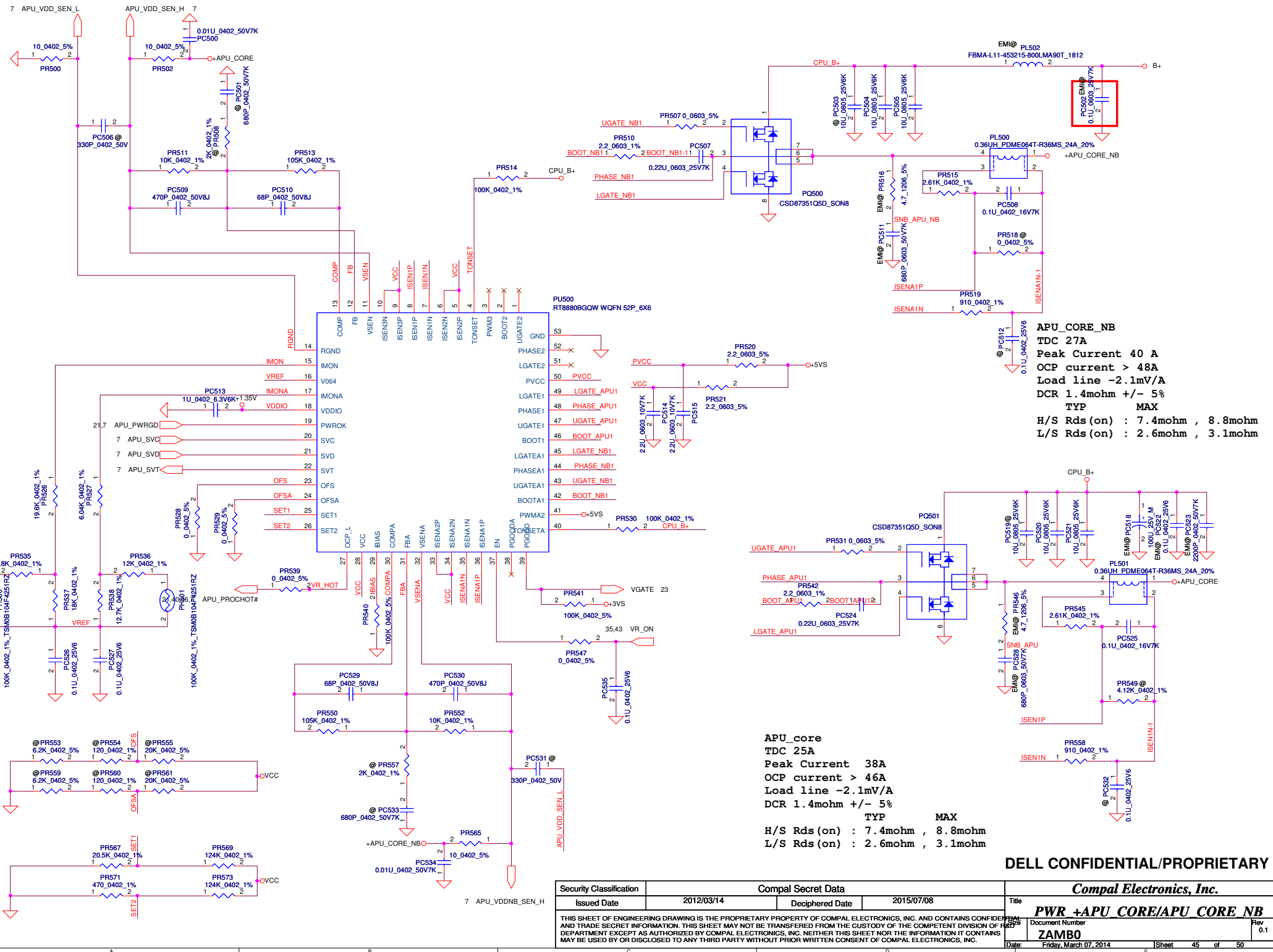
4*4 DCR 14~15.5mΩ
Heat Rating Current=6A
Saturation Current=11.5A

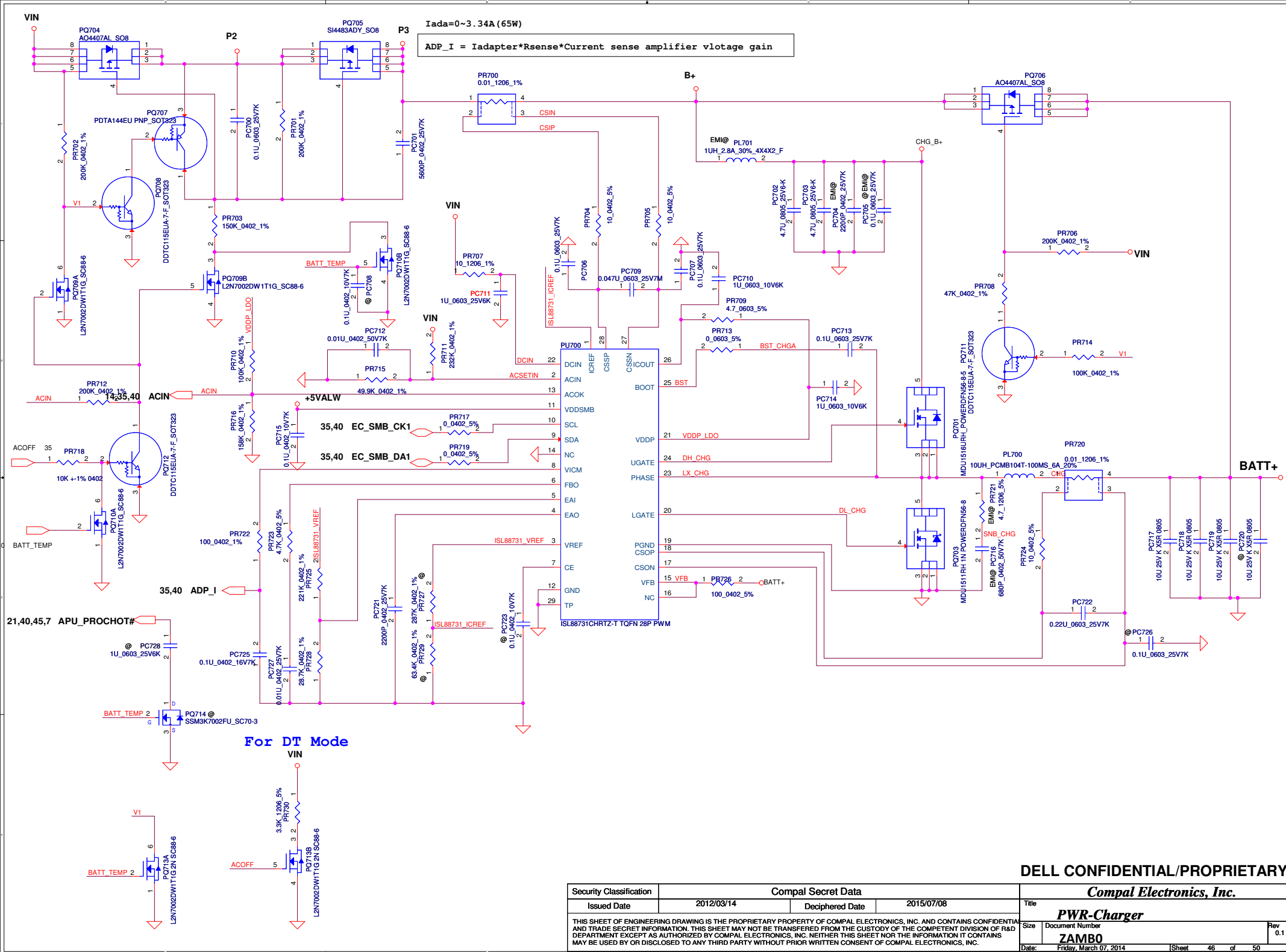


```
Over voltage IC latch off protection threshold
min=115%      type=120%      max=125 %
Delay time 10us
```

Diagram illustrating the JUMP_43X79 component. The component is represented by a blue square symbol with two pins. Pin 1 is connected to +1.8VSP and Pin 2 is connected to +1.8VS. The component is labeled JUMP_43X79 and has a reference designator @PJP403.

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					Docuement Number	Rev
					ZAMBO	0.1
					Date:	Friday, March 07, 2014





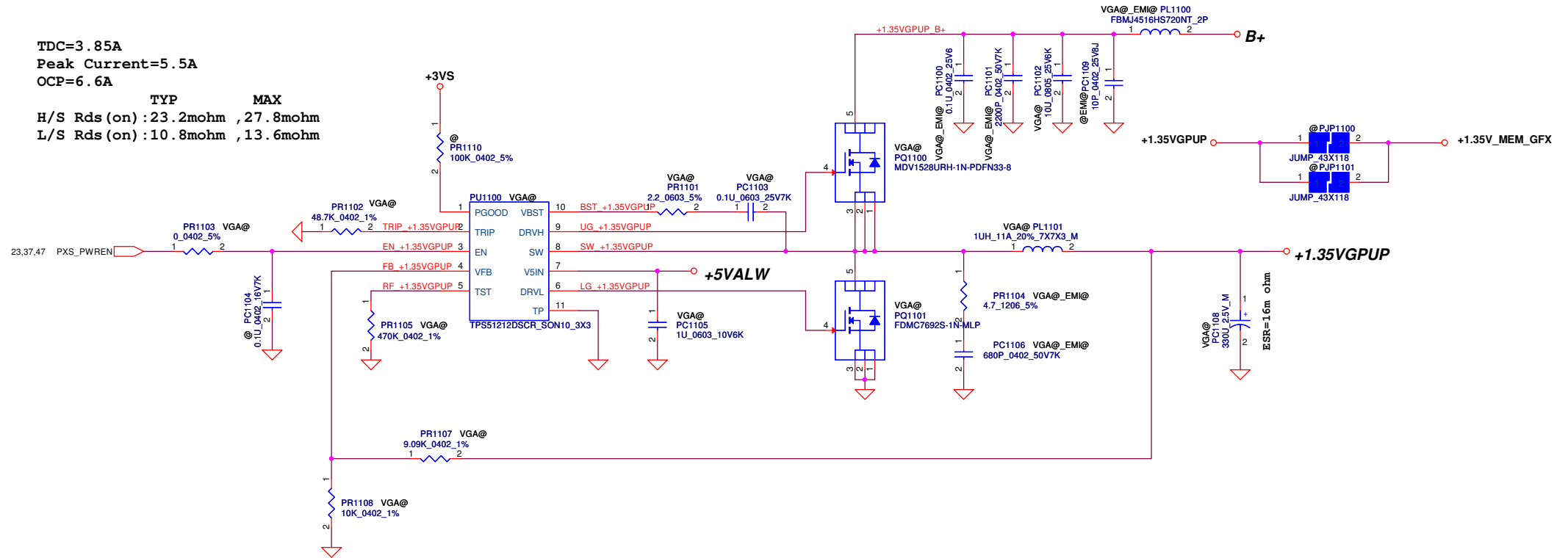
Iada=0~3.34A (65W)
ADP_I = Iadapter*Rsense*Current sense amplifier voltage gain

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TDC=3.85A
Peak Current=5.5A
OCP=6.6A

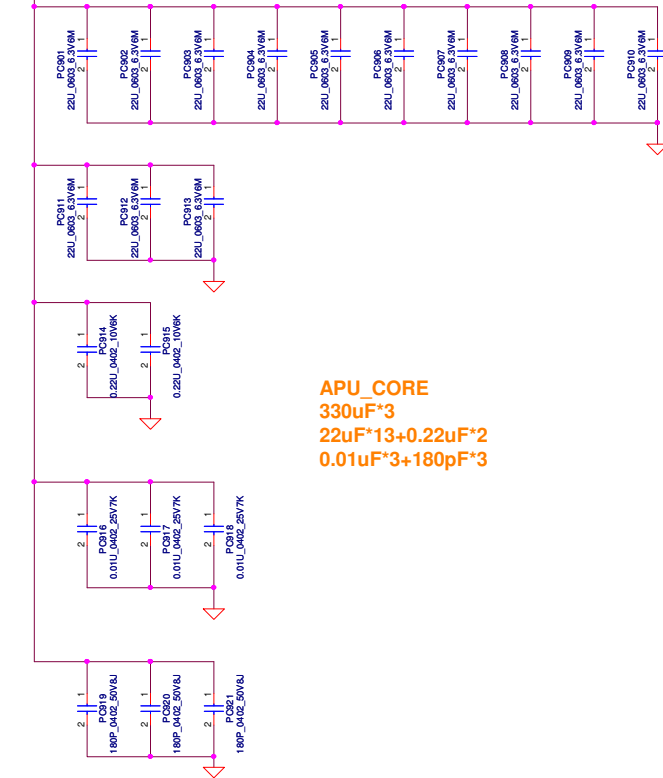
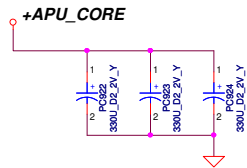
TYP MAX
H/S Rds (on) : 23.2mohm , 27.8mohm
L/S Rds (on) : 10.8mohm , 13.6mohm



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Size		Document Number		Rev	
		ZAMBO		0.1	
Date:		Friday, March 07, 2014		Sheet 48 of 50	

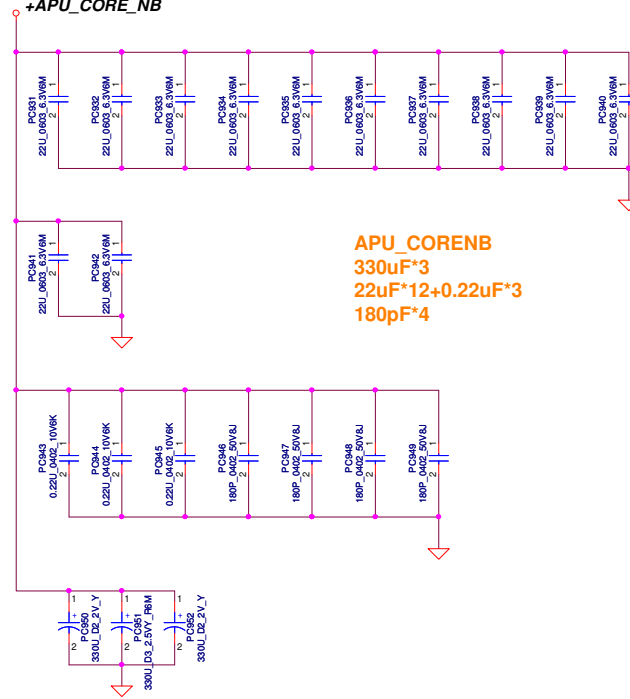
+APU_CORE

APU_CORE
330uF*3
22uF*13+0.22uF*2
0.01uF*3+180pF*3

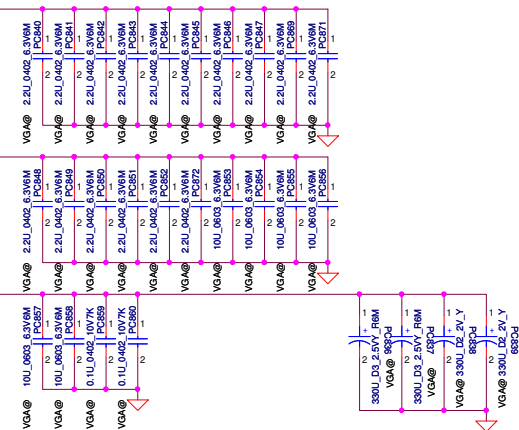


+APU_CORE_NB

APU_CORENB
330uF*3
22uF*12+0.22uF*3
180pF*4



+VGA_CORE



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Date:		Friday, March 07 2014		ISheet	50	of 50