Compal Confidential

QCL10 Schematics Document

AMD APU Trinity FS1r2 + FCH Hudson-M3 + GPU Seymour/Thames XT

2012-07-13

REV:1.0(A00)

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Issued Date	2011/08/01	Deciphered Date	2013/01/01	Title: Cover Page
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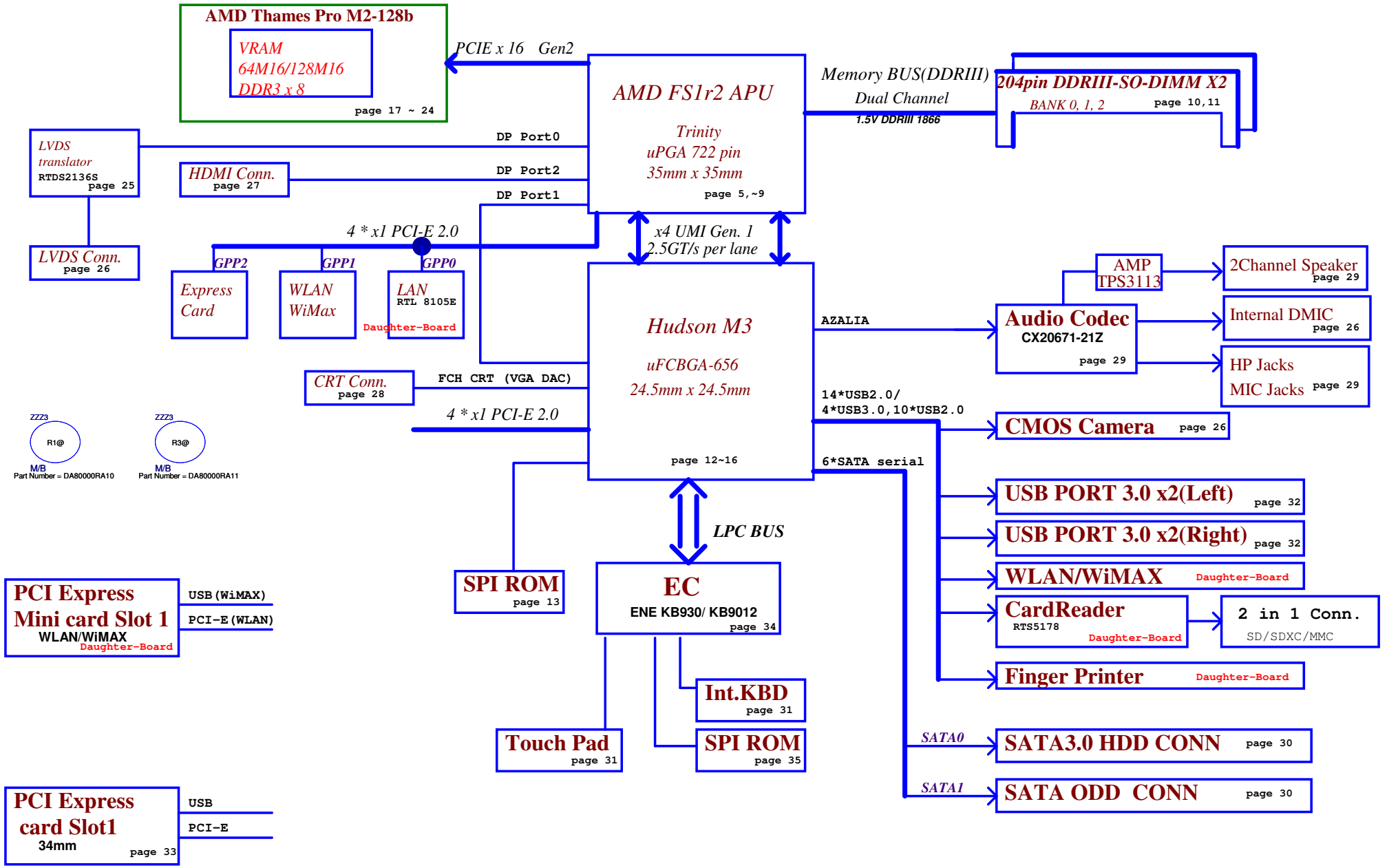
File Name : QCL10



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+1.5V	1.5V power rail for APU VDDIO and DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.2VS	1.2V (VDDR, VDDP) switched power rail for APU	ON	OFF	OFF
+2.5VS	2.5V for APU VDDA	ON	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VGS	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+1.0VGS	1.0V switched power rail for VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

FCH Hudson-M3 SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

Comal PCIE Port List

APU	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	ExCARD
	PCIE3	NC
FCH	PCIE0	NC
	PCIE1	NC
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M3 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	DEBUG PORT
Port1	WLAN
Port2	NC
Port3	FingerPrint
Port4	NC
Port5	NC
Port6	NC
Port7	CardReader
Port8	ExCARD
Port9	CAM
Port10	LP1
Port11	LP2
Port12	RP1
Port13	RP2

FCH Hudson-M3 USB Port List

Port0	LP1
Port1	LP2
Port2	RP1
Port3	RP2

EC SM Bus1 address

Device	Address	HEX
Smart Battery	000 1011	11h 0x16
Charger IC	000 1001	09h 0x12

EC SM Bus2 address

Device	Address	HEX
ADM1032ARMZ	100 1101	4Dh 0x9A
SB-TSI	100 1100	4Ch 0x98
RTD2136	100 1010	4Ah 0x94
GPU	100 0001	41h 0x82

SM Bus Controller 0

(FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		

SM Bus Controller 1

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

BOM Structure

```
UMA@  : UMA only
DIS@  : DIS muxluss
45@   : 45 Level
9012@:  EC9012
930@:   EC930
INS@:  Inspiron
VOS@:  Vostro
M2@:  FCH M2
M3@:  FCH M3
FFS@:  FreeFallSensor
EXP@:  Express Card
FP@:  FingerPrint
EMC@: EMI&ESD part
SE@:  SEYMOUS GPU
CH@:  Chelsea GPU
X76@: VRAM
H2G@: Hynix 2G
S2G@: Samsung 2G
R1@:   R1 P/N for FCH,PCB
TMSR1@: R1 P/N for GPU,VRAM
R3@:   R3 P/N for FCH,PCB
TMSR3@: R3 P/N for GPU,VRAM
```


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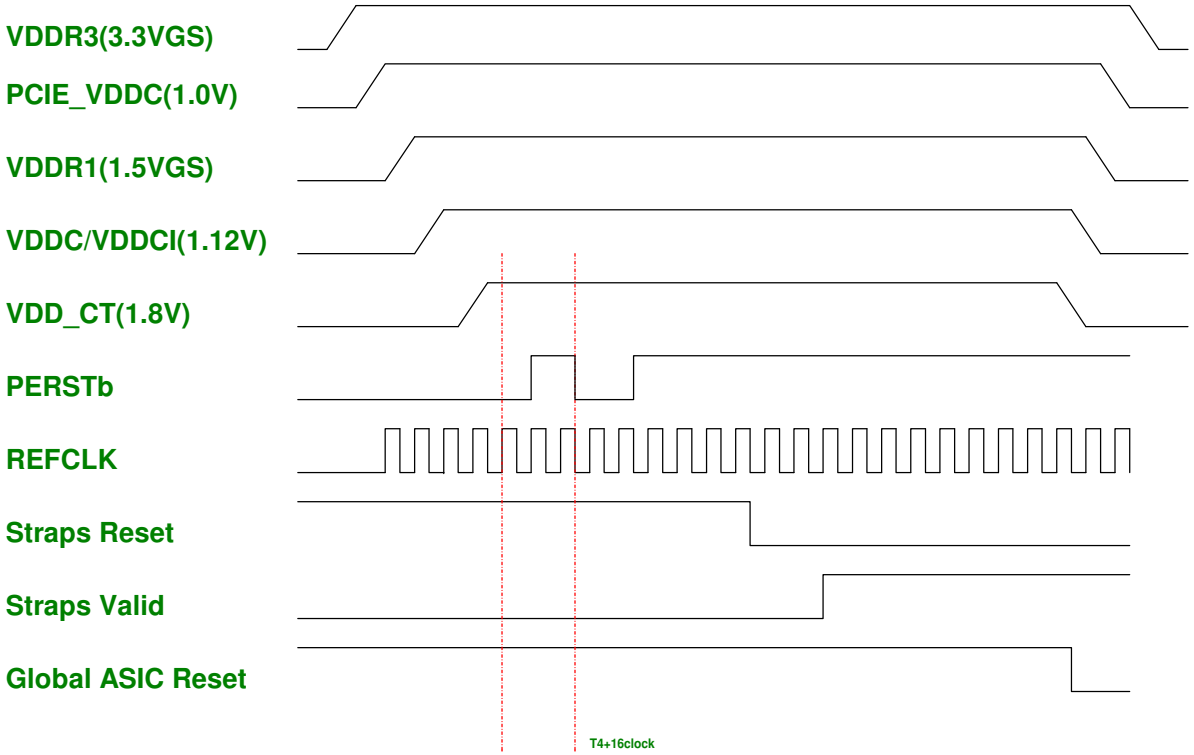
Power-Up/Down Sequence

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



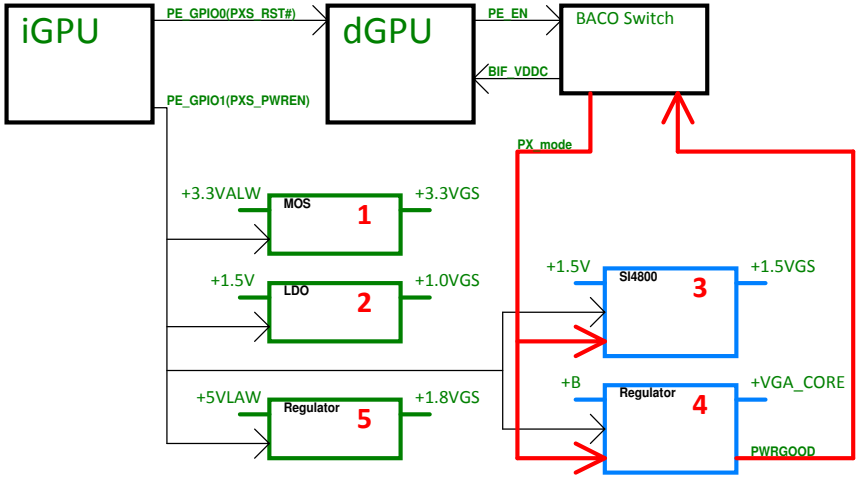
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	775mA
PCIE_VDDC	1.0V	OFF	ON	1.1A
VDDR3	3.3V	OFF	ON	60mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	1.2A
VDDC/VDDCI	TBD	OFF	OFF	28



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Title: dGPU Block Diagram

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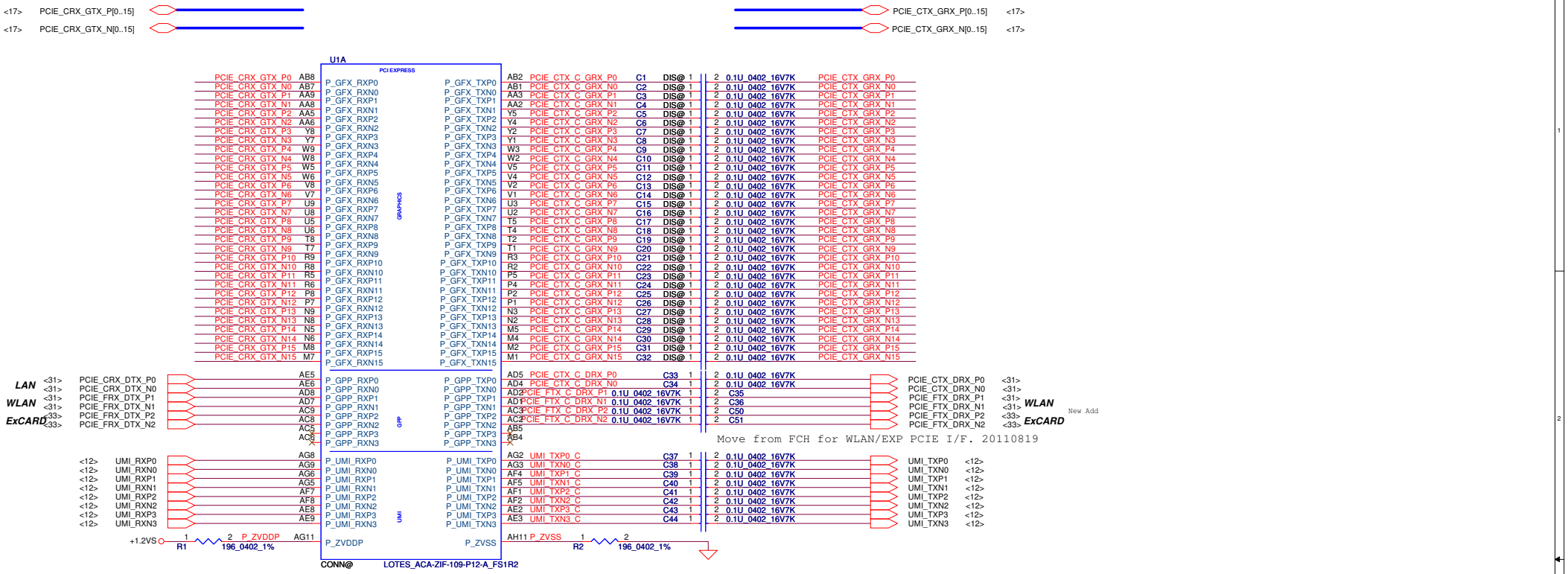
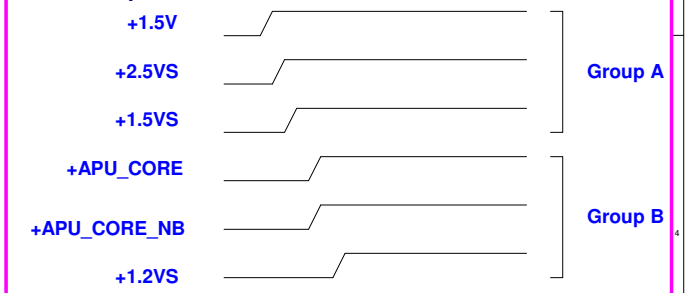


Power Sequence of APU



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Size: Custom	Document Number: LA8251P		Rev: 1.0
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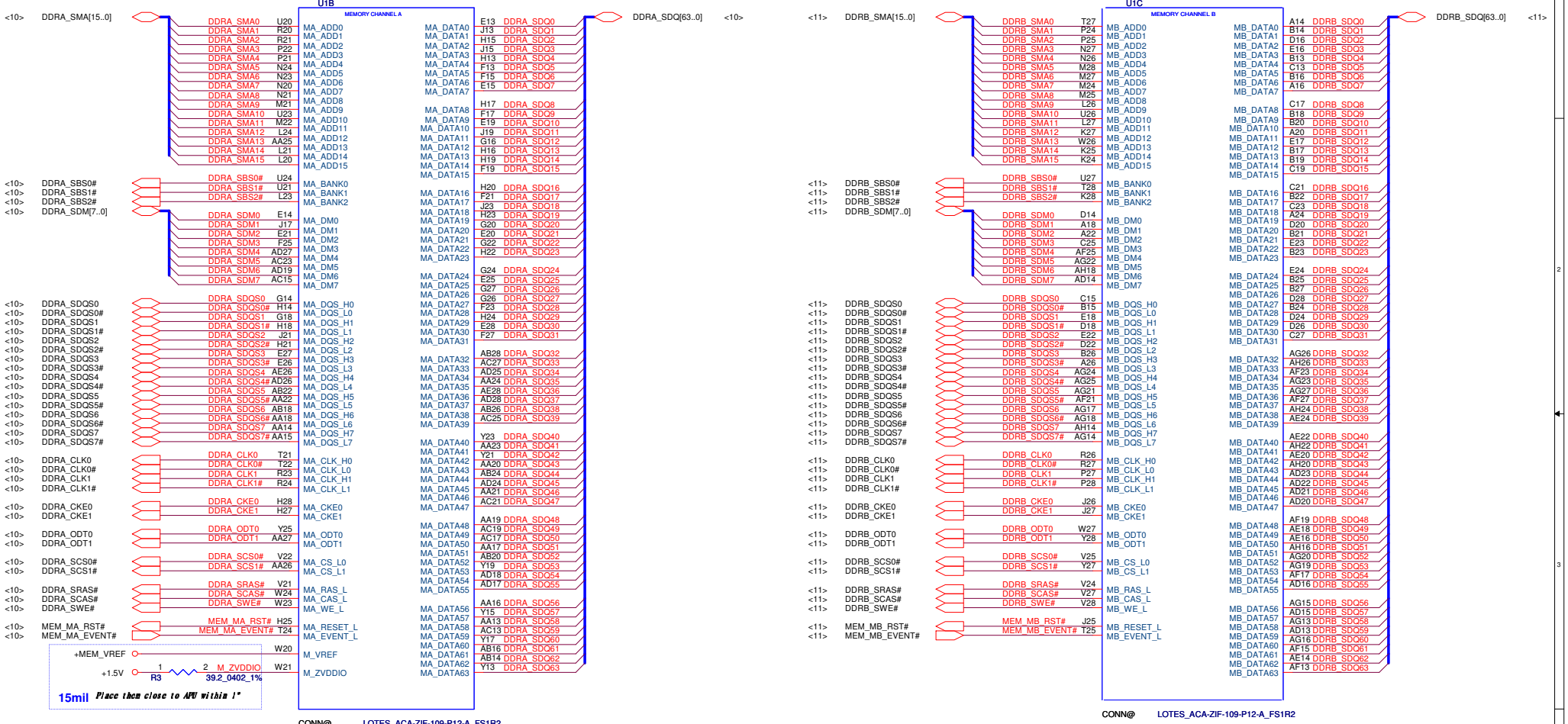

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Title: FS1r2 DDRIII Memory I/F			
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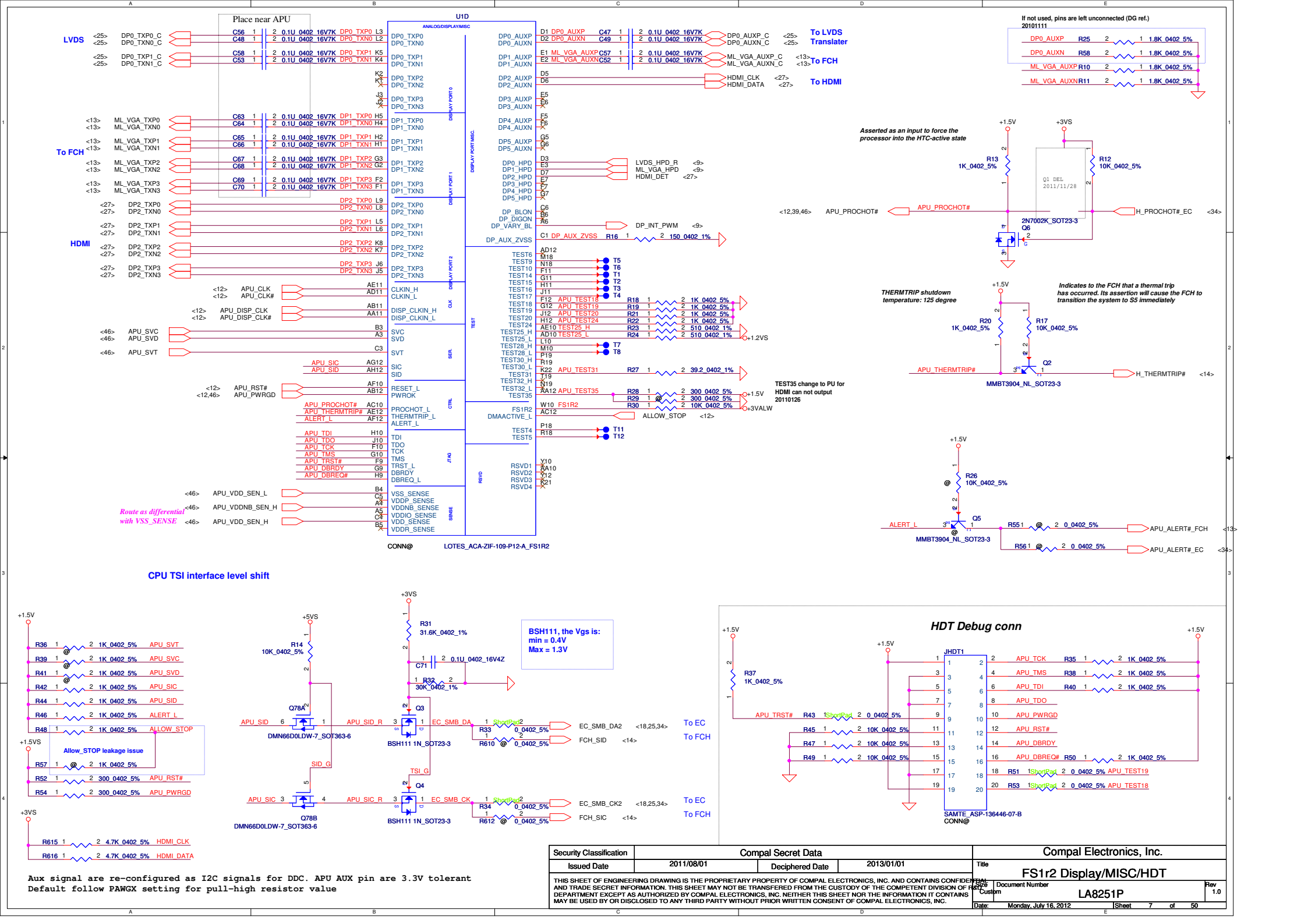

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Title: FS1r2 Display/MISC/HDT			
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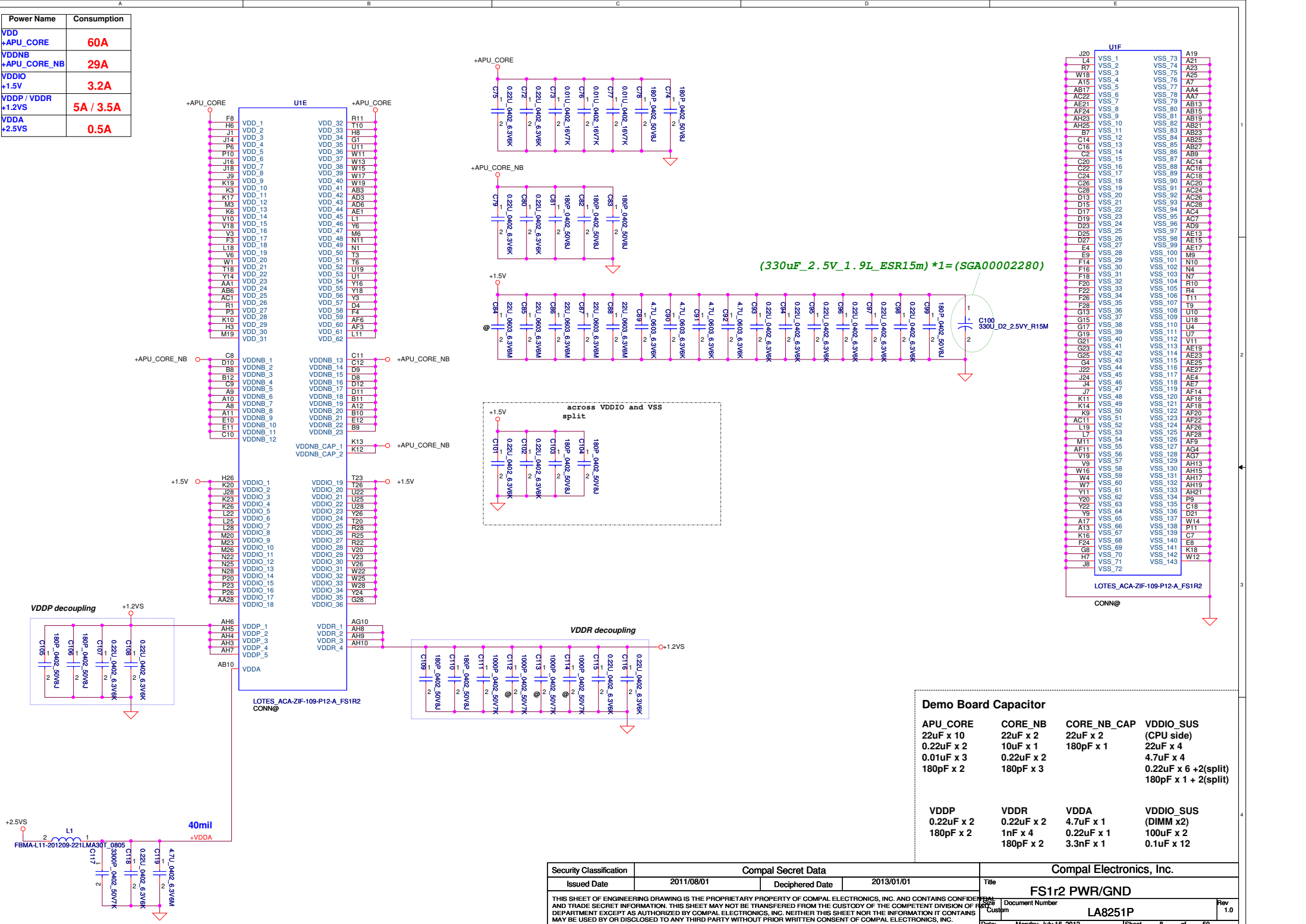
Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	29A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)

VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

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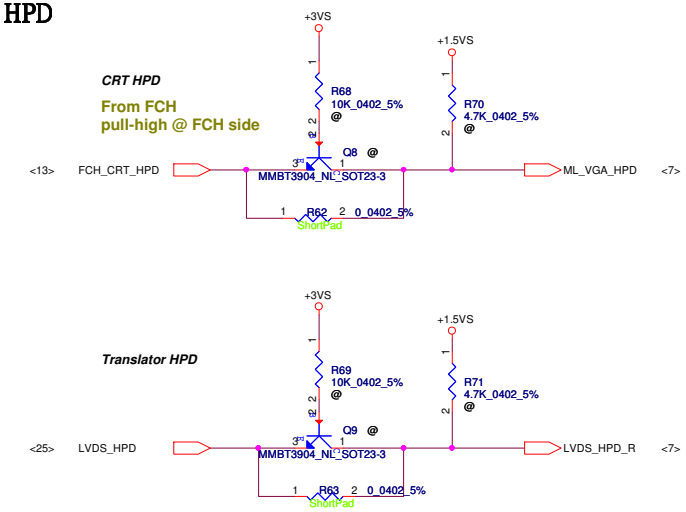
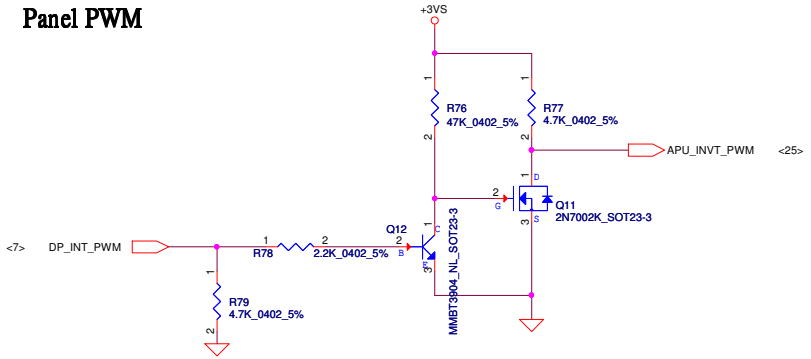
HPD



Panel PWM



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Title: FS1r2 Signal Level Shifter

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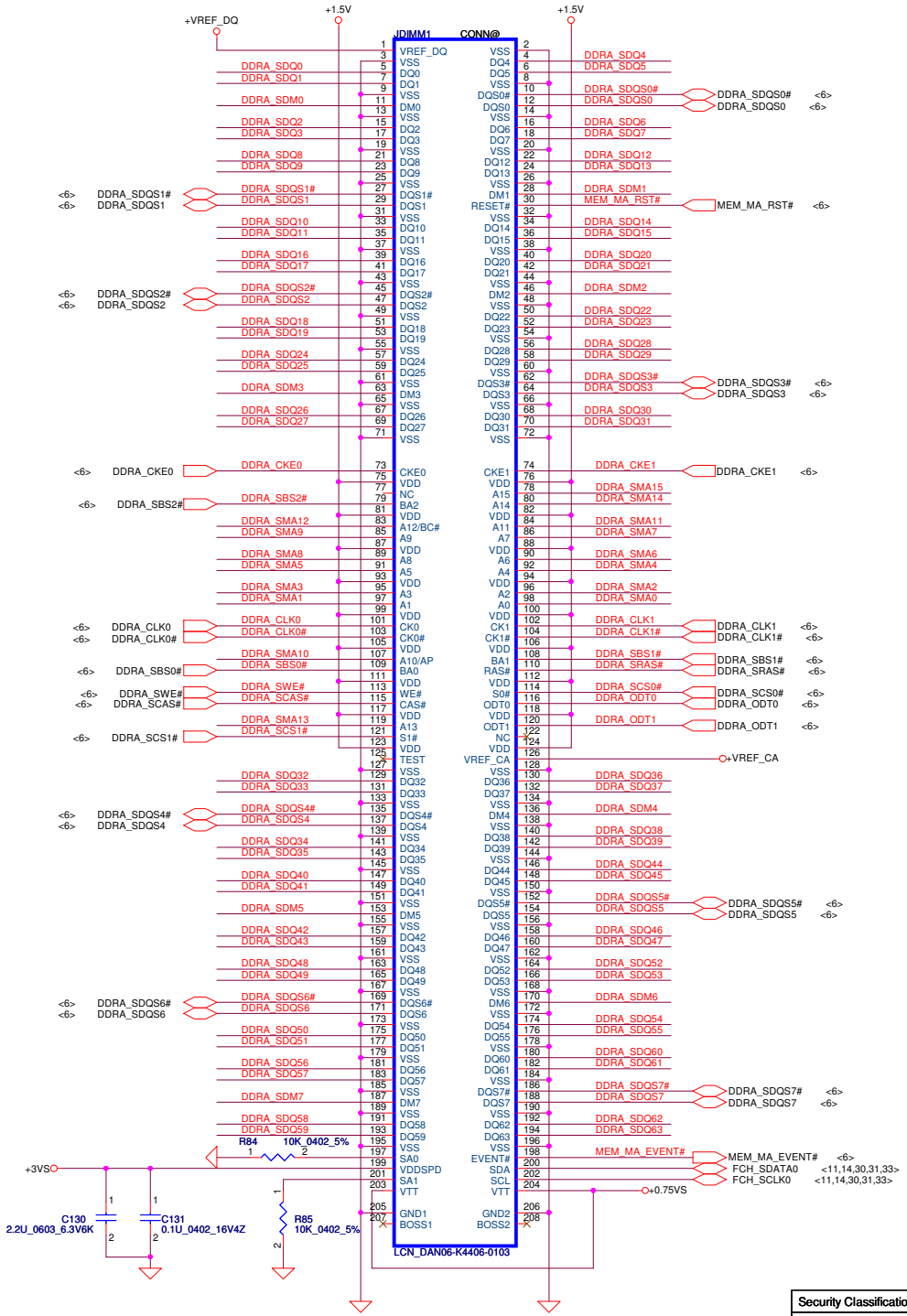

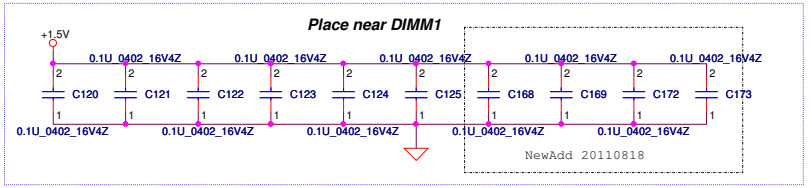

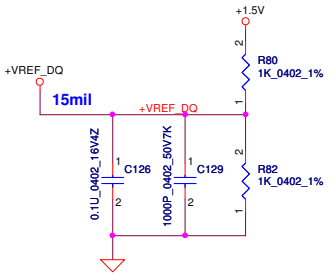

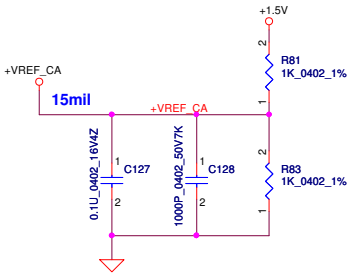

Reverse H:4mm

<Address: 00>

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Title: DDRIII SO-DIMM 1			
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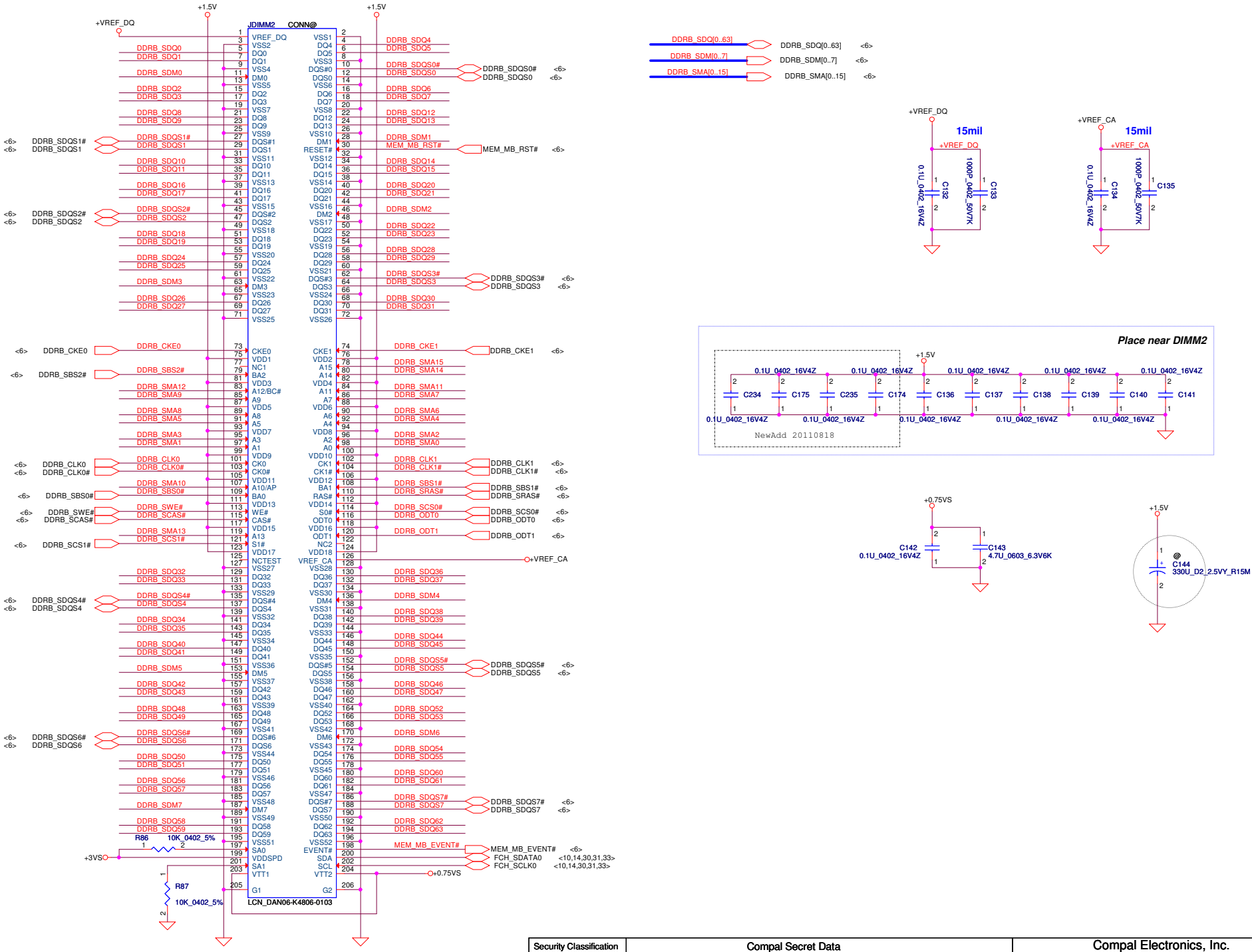

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Title: DDRIII SO-DIMM 2

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R90/ C146 close to FCH

U2
R3@
FCH-M3
Part Number = SA000043I3L

R90 100K_0402_5%
C146 150P_0402_50V8J
PLT_RST#
R89 33_0402_5% APU_PCIE_RST#_C A_RST#

U2A

UMI_RXP0 C147 0.1U_0402_16V7K UMI_RXP0_C
UMI_RXN0 C148 0.1U_0402_16V7K UMI_RXN0_C
UMI_RXP1 C149 0.1U_0402_16V7K UMI_RXP1_C
UMI_RXN1 C150 0.1U_0402_16V7K UMI_RXN1_C
UMI_RXP2 C151 0.1U_0402_16V7K UMI_RXP2_C
UMI_RXN2 C152 0.1U_0402_16V7K UMI_RXN2_C
UMI_RXP3 C153 0.1U_0402_16V7K UMI_RXP3_C
UMI_RXN3 C154 0.1U_0402_16V7K UMI_RXN3_C

UMI_TXP0 UMI_TXN0 UMI_TXP1 UMI_TXN1 UMI_TXP2 UMI_TXN2 UMI_TXP3 UMI_TXN3

R94 590_0402_1% PCIE_CALRP
R88 2K_0402_1% PCIE_CALRN
+VDDAN_11_PCIE

Move PCIE device to APU. 20110819

R95 2K_0402_1% CLK_CALRN
+1.1VS_CKVDD

SS
For "EXT" CLK mode, input to PCIE,
NSS
APU DISP APU_DISP_CLK APU_DISP_CLK#
APU APU_CLK APU_CLK#
VGA CLK_PCIE_VGA CLK_PCIE_VGA# R98 R99 CLK_PCIE_VGA_R CLK_PCIE_VGA#_R
SS
WLAN CLK_PCIE_WLAN CLK_PCIE_WLAN# R102 R103
GLAN CLK_PCIE_LAN CLK_PCIE_LAN# R100 R101
ExCARD CLK_PCIE_XCRD CLK_PCIE_XCRD# RX7 RX8 CLK_PCIE_XCRD_R CLK_PCIE_XCRD#_R
New Add

CLOSE TO R680
LAN_X1 R801 CLK_LAN_25M 0_0402_5%

CLOSE TO X1
PCH_X1 R800 25M_X1 0_0402_5%

CLK_LAN_25M R680 22_0402_5% CLK_LAN_25M_R 14M_25M_48M_OSC

CH27 10P_0402_50V8J~D
CH28 10P_0402_50V8J~D
YH2 25MHZ_10PF_7V25000014
R106 1M_0402_5%
25M_X1 25M_X2

For PCIE device reset on FS1
(GFX,GLAN,WLAN,LVDS Travis)
APU_PCIE_RST #: Reset PCIE device on APU

+3VALW
C789 @ 0.1U_0402_16V4Z
MC74VHC1G08DFT2G SC70 5P U43
APU_PCIE_RST# C R692 @ 33_0402_5%
C790 @ 150P_0402_50V8J
R693 @ 8.2K_0402_5%
R695 @ 0_0402_5%
R694 0_0402_5% ShortPad
APU_PCIE_RST# <17>
PLT_RST# <31,33,34>
QCL10 LAN-APU,WLAN&ExCARD-FCH 20110803

R692/ C790 close to FCH

U2A
HUDSON-2

PCIE_RST# A_RST#
PCI_CLKS
PCICLK0 PCICLK1/GPO36 PCICLK2/GPO37 PCICLK3/GPO38 PCICLK4/14M_OSC/GPO39
PCI_CLK1 <16>
PCI_CLK3 <16>
PCI_CLK4 <16>
PCIRST#
PCI EXPRESS INTERFACES
PCI INTERFACE
AD0/GPIO0 AD1/GPIO1 AD2/GPIO2 AD3/GPIO3 AD4/GPIO4 AD5/GPIO5 AD6/GPIO6 AD7/GPIO7 AD8/GPIO8 AD9/GPIO9 AD10/GPIO10 AD11/GPIO11 AD12/GPIO12 AD13/GPIO13 AD14/GPIO14 AD15/GPIO15 AD16/GPIO16 AD17/GPIO17 AD18/GPIO18 AD19/GPIO19 AD20/GPIO20 AD21/GPIO21 AD22/GPIO22 AD23/GPIO23 AD24/GPIO24 AD25/GPIO25 AD26/GPIO26 AD27/GPIO27 AD28/GPIO28 AD29/GPIO29 AD30/GPIO30 AD31/GPIO31
PCI_AD23 <16>
PCI_AD24 <16>
PCI_AD25 <16>
PCI_AD26 <16>
PCI_AD27 <16>
CBE0# CBE1# CBE2# CBE3# FRAME# DEVSEL# IRDY# TRDY# PAR STOP# PERR# SERR# REQ0# REQ1#/GPIO40 REQ2#/CLK_REQ8#/GPIO41 REQ3#/CLK_REQ5#/GPIO42 GNT0# GNT1#/GPO44 GNT2#/SD_LED/GPO45 GNT3#/CLK_REQ7#/GPIO46 CLKRUN# LOCK#
T14
XCRD_CLKREQ#
R223 @ 0_0402_5%
R224 @ 0_0402_5%
PXS_RST# <14,17>
PXS_PWREN <14,19,42,44>
XCRD_CLKREQ# <33>
INTE#/GPIO32 INTF#/GPIO33 INTG#/GPIO34 INTH#/GPIO35
HDD_FALL_INT
HDD_FALL_INT <30>

CLOCK GENERATOR
LPCCLK0 CLK_EC33M R222 22_0402_5%
CLK_PCI_EC <16,34>
LPC
LPCCLK1 LAD0 LAD1 LAD2 LAD3 LFRAME# LDRQ0# LDRQ1#/CLK_REQ6#/GPIO49 SERIRQ/GPIO48
LPC_CLK1 <16>
LPC_AD0 <34>
LPC_AD1 <34>
LPC_AD2 <34>
LPC_AD3 <34>
LPC_FRAME# <34>
SERIRQ <34>
APU
DMA_ACTIVE# PROCHOT# APU_PG LDT_STP# APU_RST#
APU_PROCHOT# R15 510_0402_5%
ALLOW_STOP <7>
APU_PROCHOT# <39,46,7>
APU_PWRGD <46,7>
APU_RST# <7>
S5 PLUS
S5_CORE_EN RTCCLK INTRUDER_ALERT# VDDBT_RTC_G
RTC_CLK <16,34>
+VDDBT_RTC
32K_X1 32K_X2

APU_PG/APU_RST#/LDT_STP# : OD pin
DMA_ACTIVE# : IN/OD, 0.8V threshold
PROCHOT# : IN, 0.8V threshold
LDT_STP : No use, NC
DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

C158 18P_0402_50V8J
R107 20M_0402_5%~D
32.768KHZ_12.5PF_9H03200019 Y1
C159 18P_0402_50V8J
Close to HUDSON-M2/3

CLOSE TO Y1
FCH_RTCX1 R803 32K_X1 0_0402_5%

+3VS
EXP@ 8.2K_0402_5% RX6

+RTCBATT R135 510_0402_5% +VCOIN
+3VLP
D8 RB751V40_SC76-2
D5 RB751V40_SC76-2
+VCOIN_RTC
R105 510_0402_5% W=20mils W=20mils
C156 1U_0402_6.3V6K
CLRP1 @ SHORT PADS
R109 10M_0402_5% @
for Clear CMOS

218-0755097 A14 HUDSON-M3_FCBGA656

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Issued Date	2011/08/01	Deciphered Date	2013/01/01

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Title: FCH PCIE/CLK/PCI/LPC/RTC

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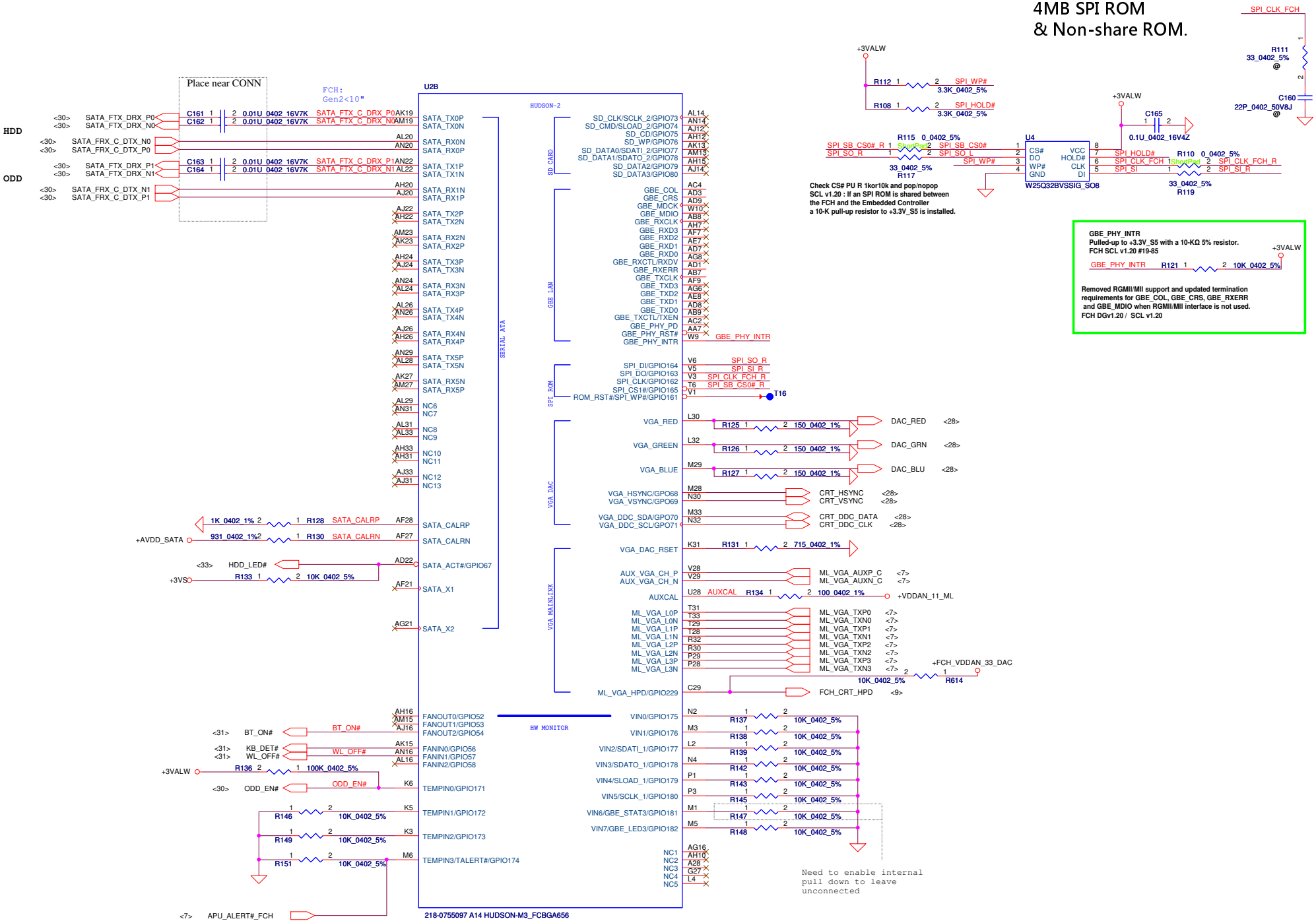
4MB SPI ROM & Non-share ROM.



Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.			
Title: FCH SATA/SPI/VGA/HWM/SD			
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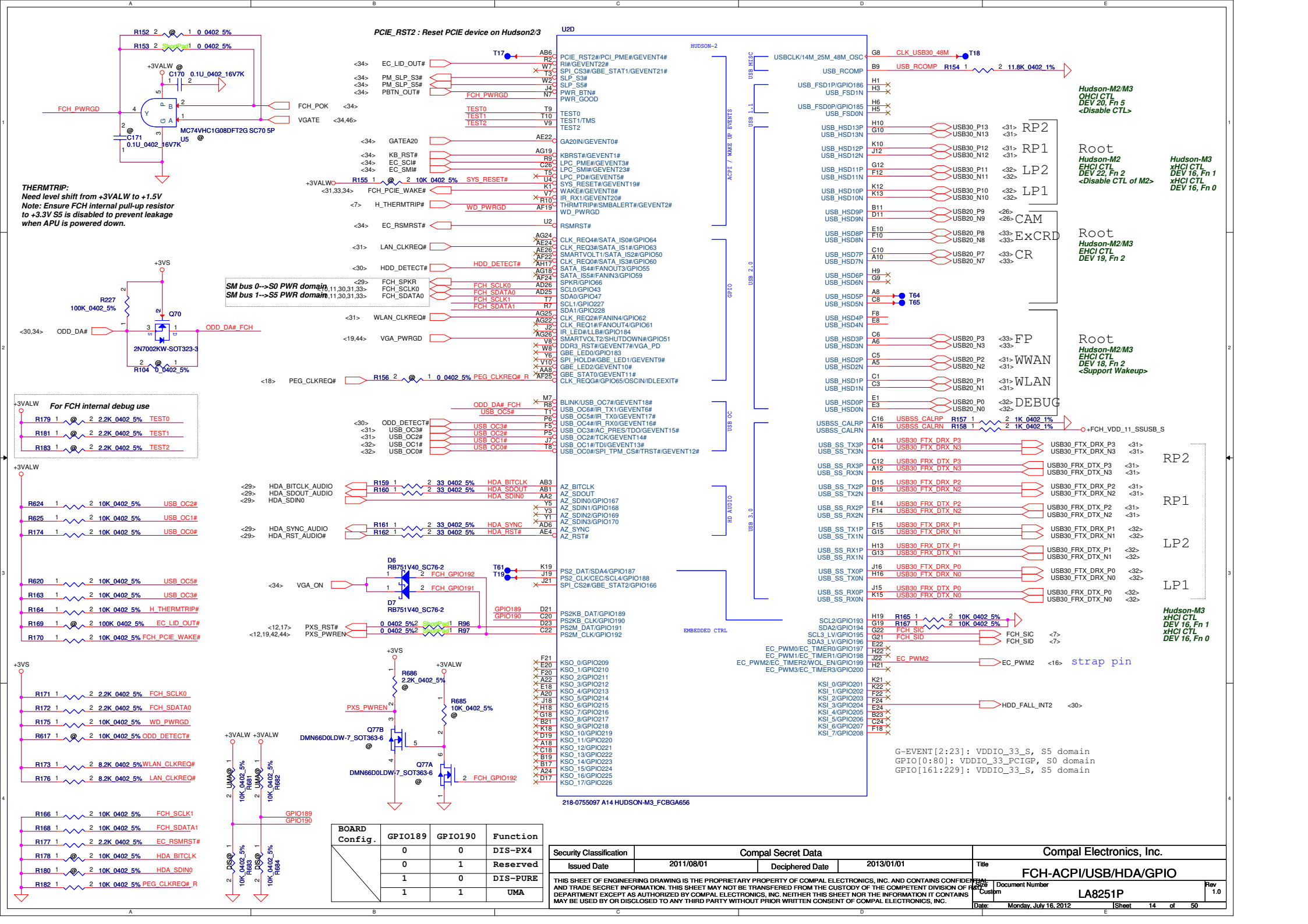

BOARD Config.	GPIO189	GPIO190	Function
	0	0	DIS-PX4
	0	1	Reserved
	1	0	DIS-PURE
	1	1	UMA

Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.

Title: FCH-ACPI/USB/HDA/GPIO

Size: B2S Custom | Document Number: LA8251P | Rev: 1.0

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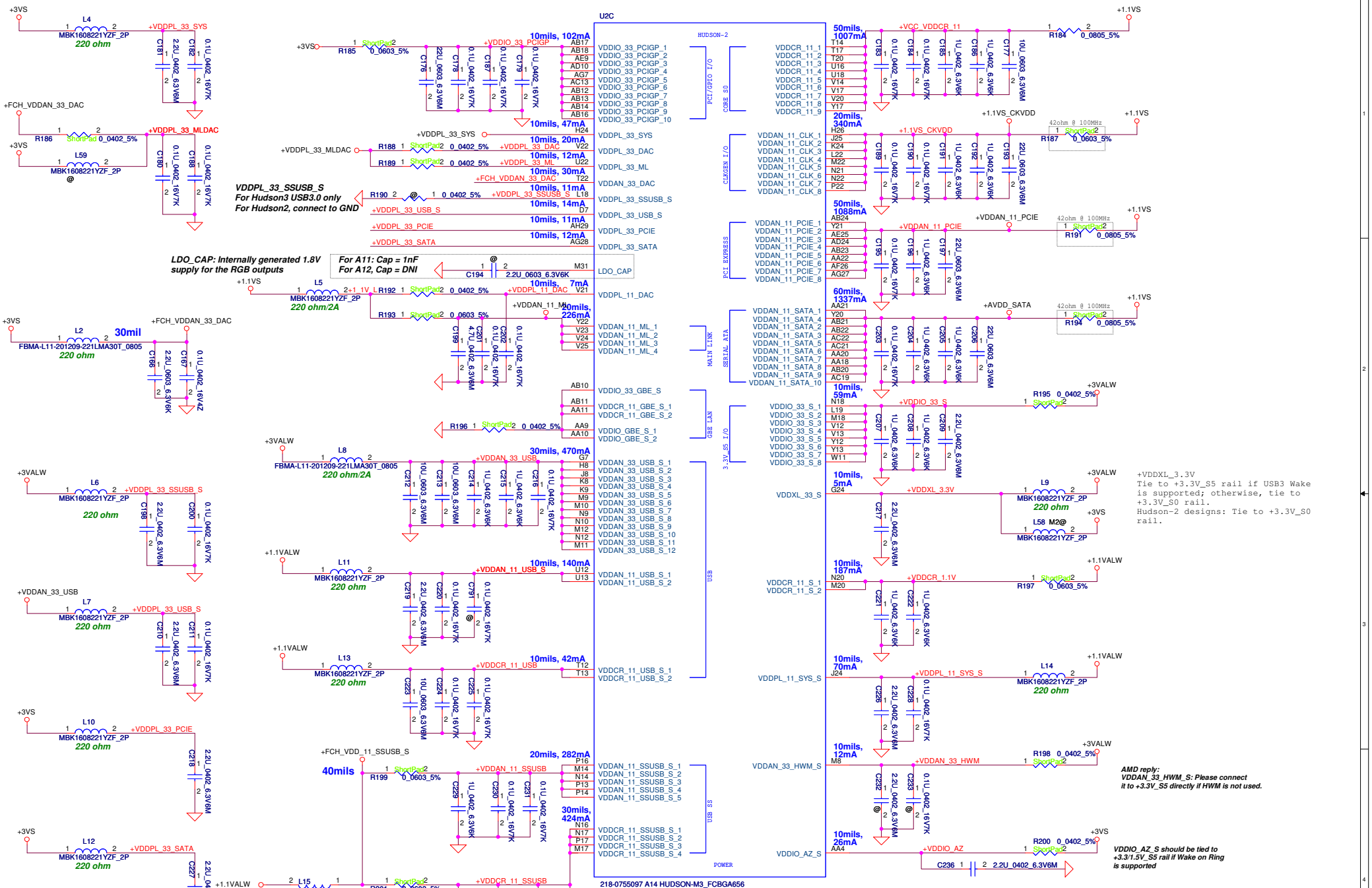

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Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.

Title: FCH-PWR

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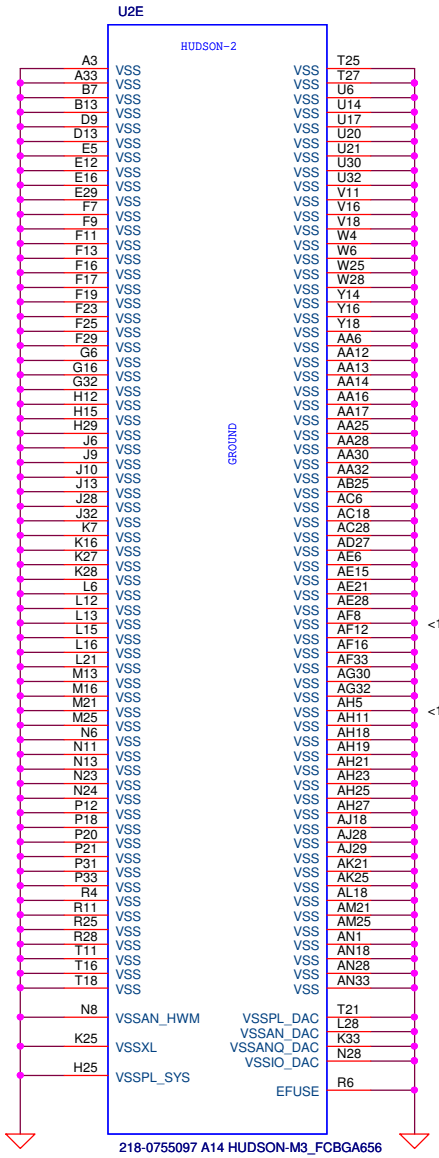
STRAP PINS

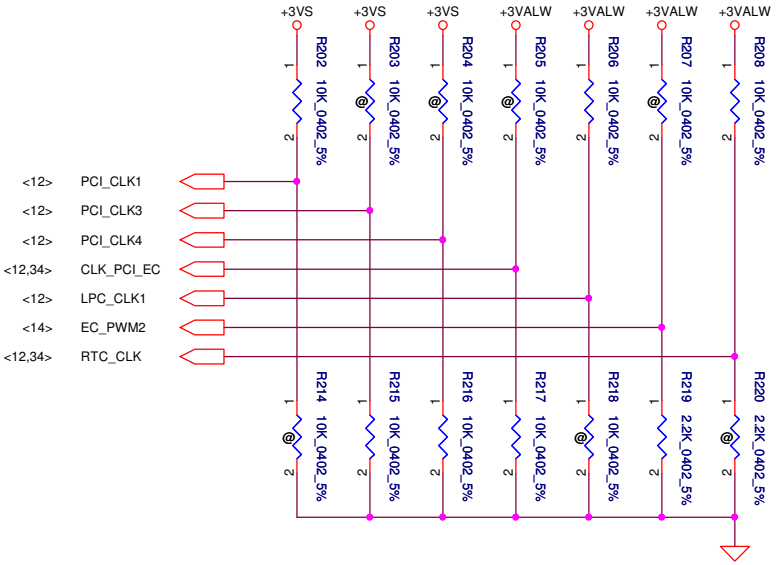
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

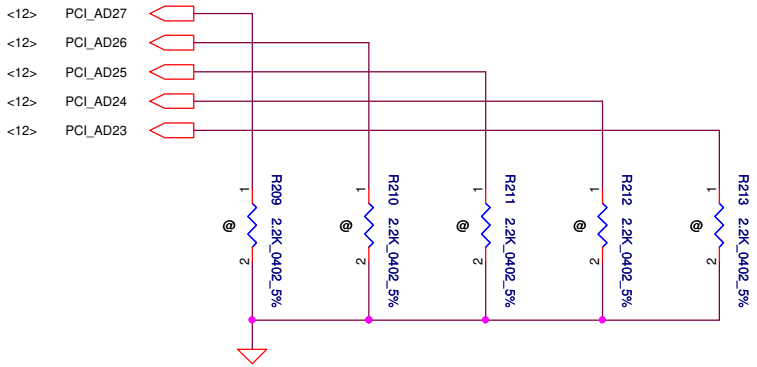
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT







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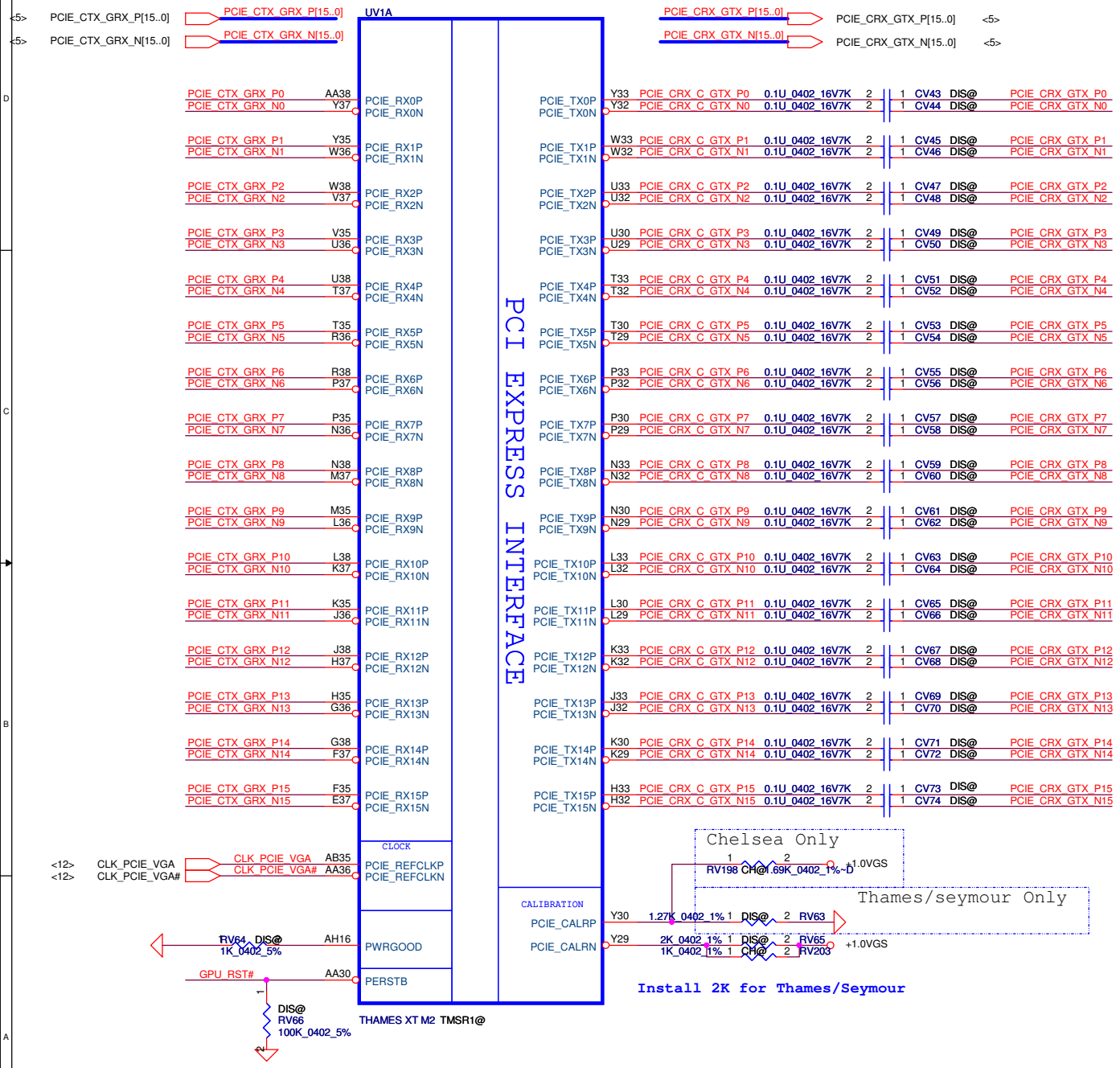
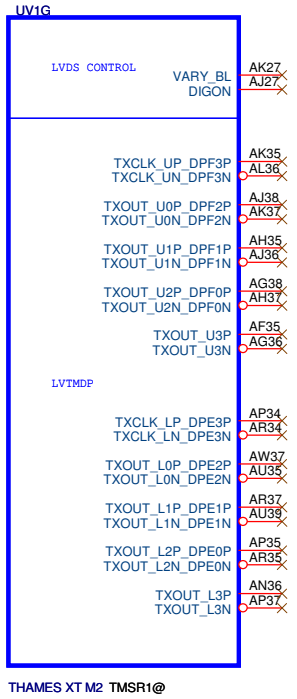
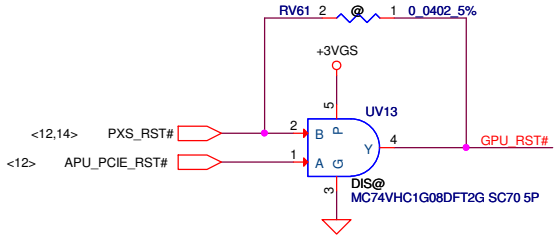
Issued Date	2011/08/01	Deciphered Date 2013/01/01	Title: FCH-VSS/Strap
			Size: B; Document Number: LA8251P; Rev: 1.0
			Date: Monday, July 16, 2012; Sheet 16 of 50

GFX PCIE LANE REVERSAL



LVDS Interface





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Title	ATI_SeymourXT_M2_PCIE/LVDS		
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CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS		RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS	0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test	0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED		0
BIF_VGA DIS	GPIO9	VGA ENABLED		0
RSVD	GPIO21	RESERVED		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS		0
RSVD	H2SYNC			0
RSVD	GENERICC			0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI		11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2	
★64MX16 (1G) Hynix 1GB PN:SA00004IS20	RV67 1	RV70 0	RV72 0	PT
★64MX16 (1G) Samsung 1GB PN:SA00004GS0L	RV68 0	RV69 1	RV72 0	PT
128MX16 (2G) Hynix 2GB PN:SA00003VO00	RV67 1	RV70 0	RV71 1	
128MX16 (2G) Samsung 2GB PN:SA00004TQ00	RV68 0	RV69 1	RV71 1	

Not Share via for other GND

Reserved test pad of CRT Signals for debug

Add 12/8

NC_TSVSSQ should be tied to GND on Thames/Seymour

Add 12/6 for MLPS

CLOSE TO YV1

Internal VGA Thermal Sensor

VGA Thermal Sensor ADM1032ARMZ

Closed to GPU

Address:100_1101

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Issued Date	2011/08/01	Deciphered Date	2013/01/01

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Title: ATI_SeymourXT_M2_Main_MSIC

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Circuits to support BACO

Switch circuits in BACO desingns for Thanes/Seymour only

55mA@1.0V, in BACO mode

for PX4.0

for PX4.0 and PX5.0

for PX5.0

PX_MODE=1 for Normal Operation

PX_MODE=0 for BACO mode to shut down power rails expcept VDDR3,PCIE_VDDC and 1.8V rail

+3.3VS TO +3.3VGS

+1.5V TO +1.5VGS

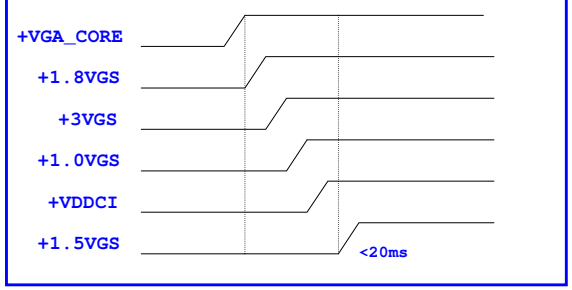
Note:

PX4.0 +VGA_CORE,VDDCI,+1.5VGS OFF

PX4.0 +3VGS, +1.0VGS,+1.8VGS ON

PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

Power Seguence of Thames and Chelsea



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Title	ATI_SeymourXT_M2_BACO POWER		
Size C	Document Number LA8251P		Rev 1.0
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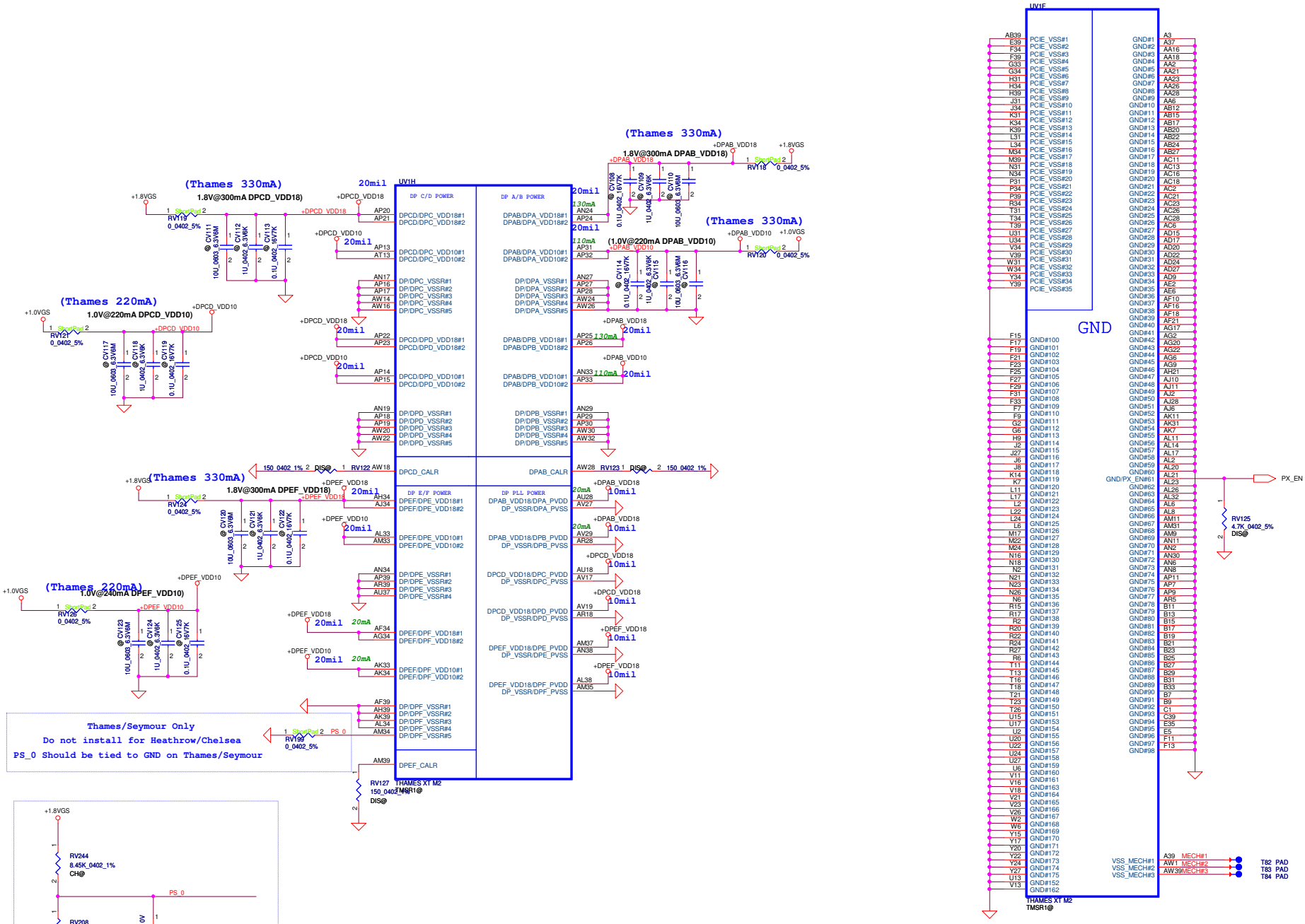

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Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.

Title: ATI_SetmourXT_M2_PWR_GND

Size	Document Number	Rev
C	LA8251P	1.0

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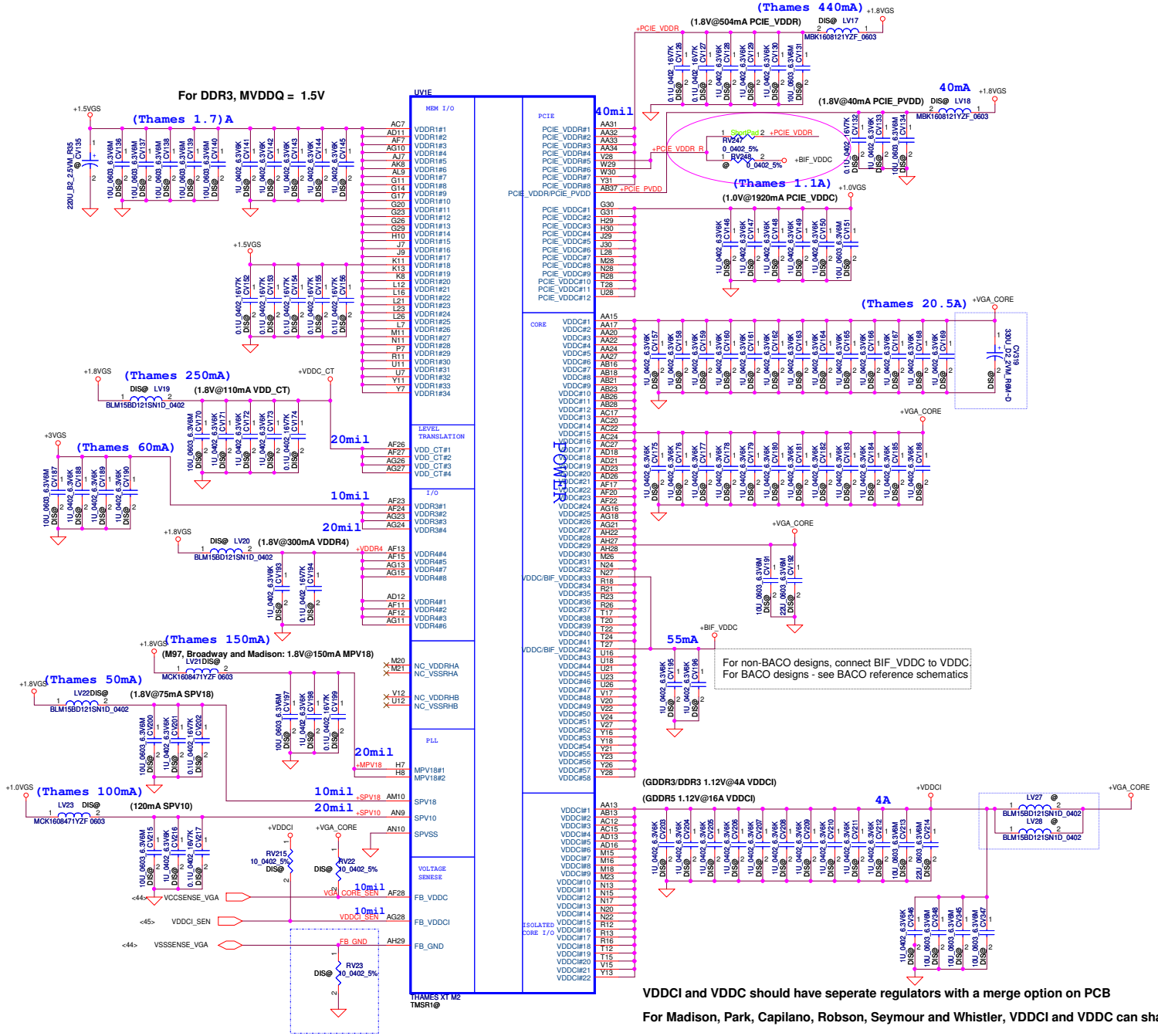

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Title	ATI_SeymourXT_M2_Power		
Size C	Document Number LA8251P		Rev 1.0
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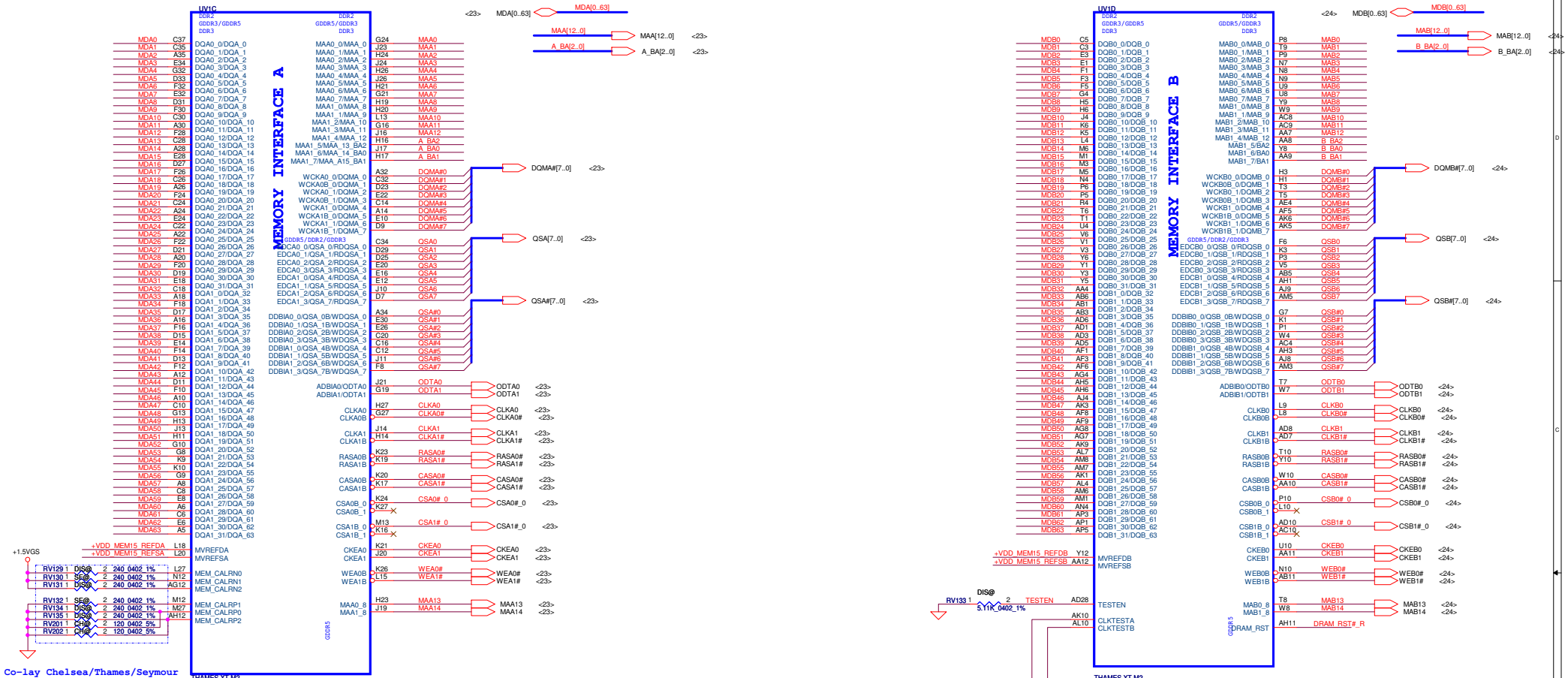

	Thames M2	Seymour M2	Chelsea M2
RV129	POP	@	@
RV130	@	POP	@
RV131	POP	@	@
RV132	@	POP	@
RV134	POP	@	@
RV135	POP	@	@
RV136	@	@	POP
RV137	@	@	POP

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

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Title: ATI_SeymourXT_M2_MEM IF

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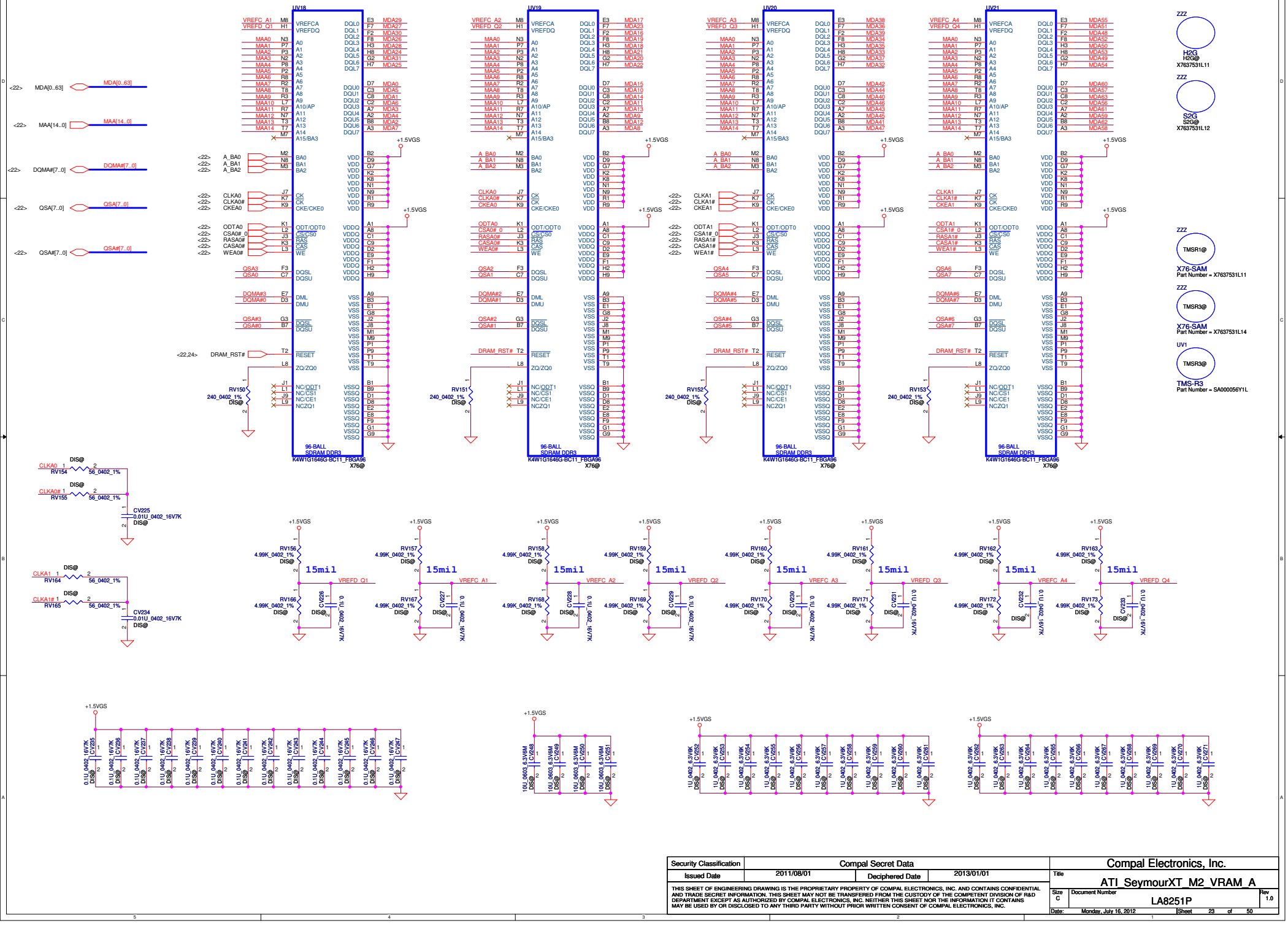
CHANNEL A: 256MB/512MB DDR3



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Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_A

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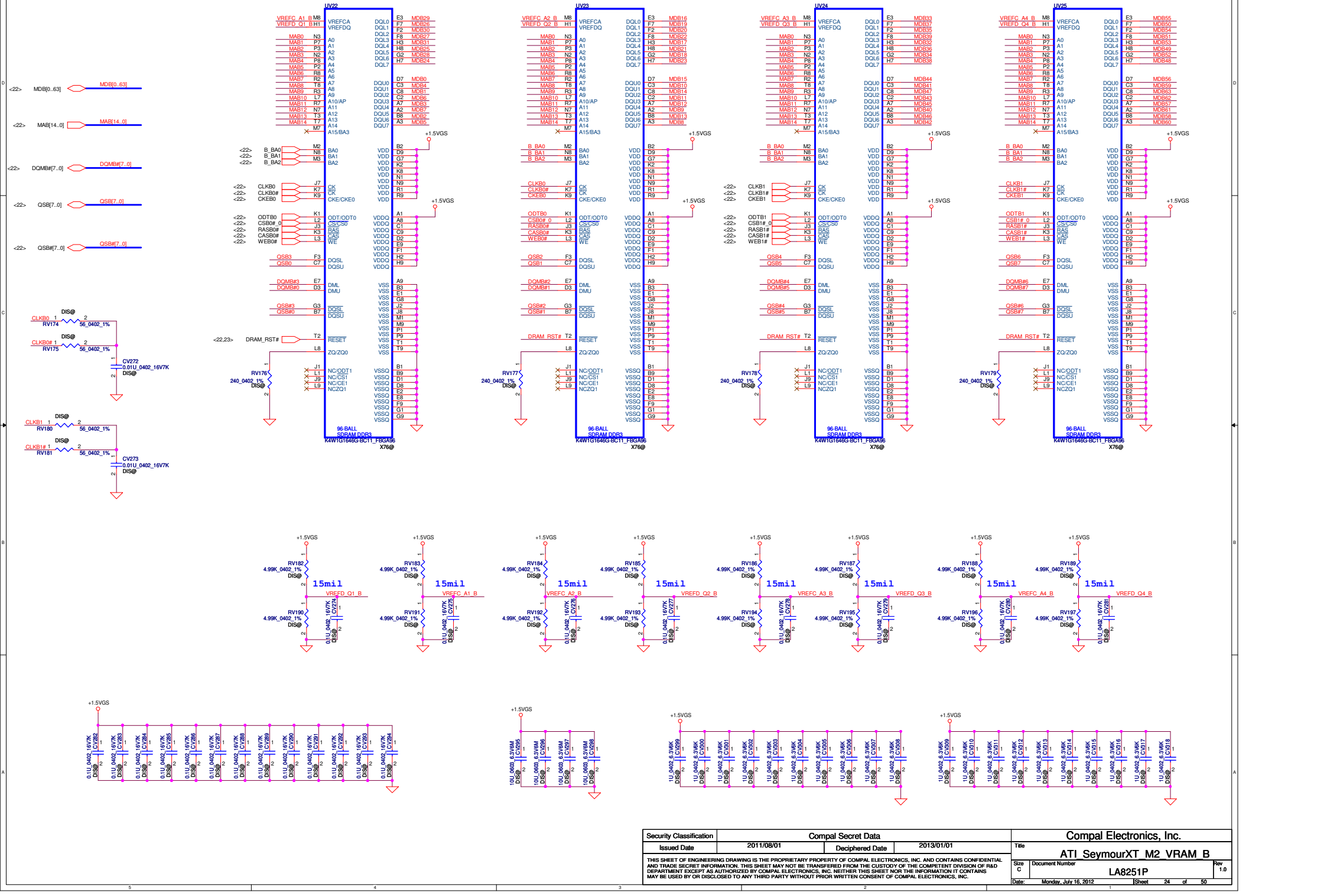
CHANNEL B: 256MB/512MB DDR3



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Title: ATI_SeymourXT_M2_VRAM_B

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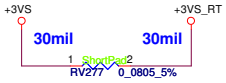
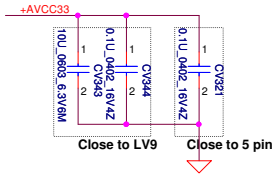
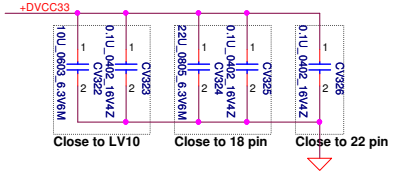
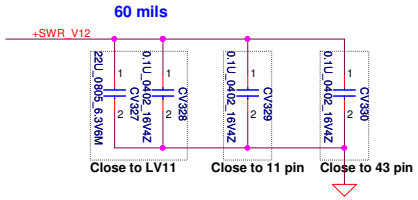
Power Consumption:

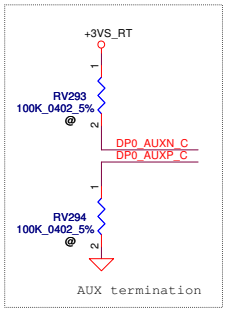
Pin5 (DPV33) < 20mA
Pin 11 (DPV12) < 100mA
Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
Pin 22 (PVCC) < 50 mA
Pin 43 (VCCK) < 50mA

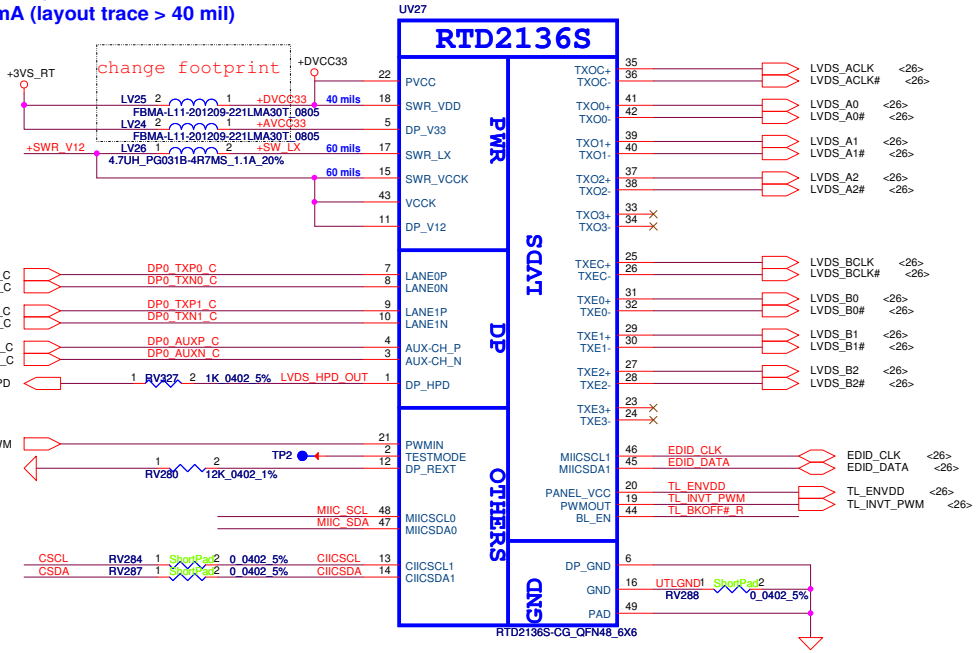


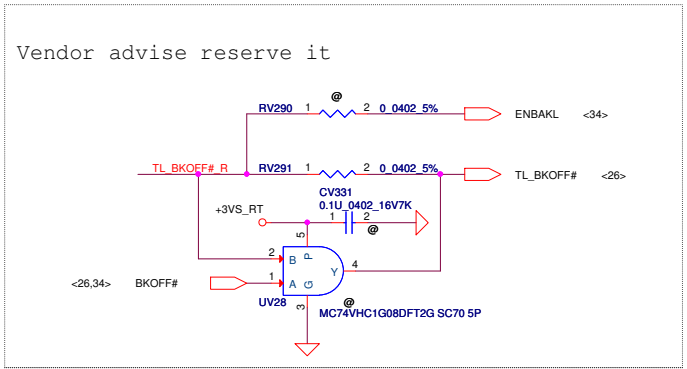


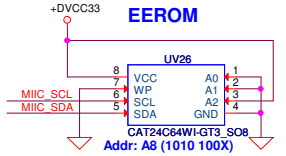


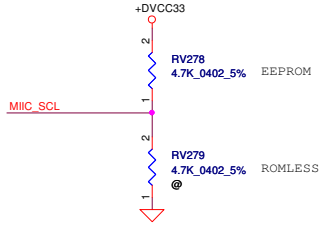


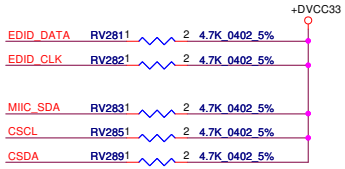


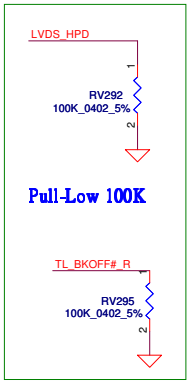












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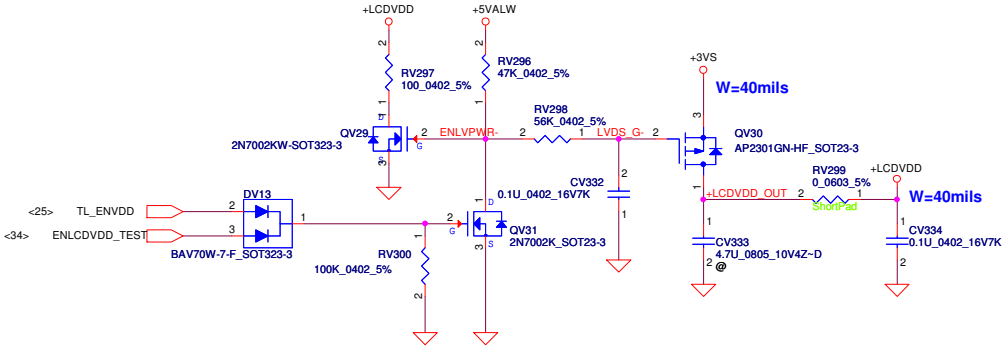
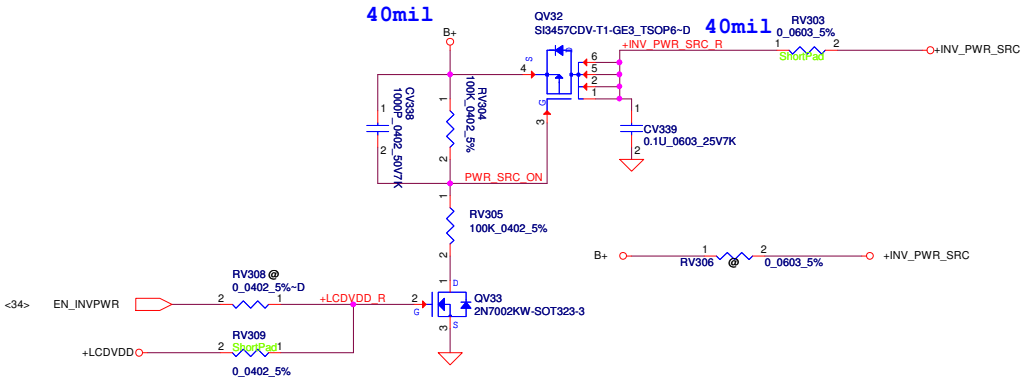
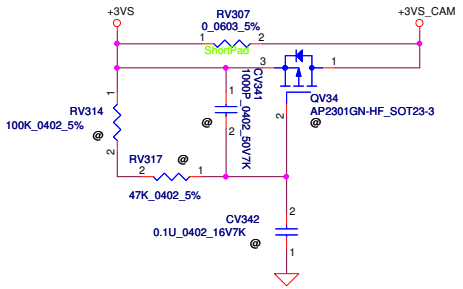
LCD PWR CTRL



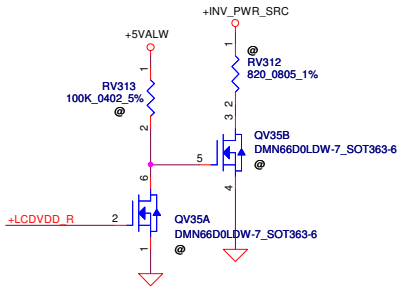
LCD backlight PWR CTRL



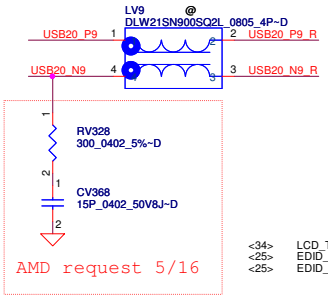
Wedcam PWR CTRL

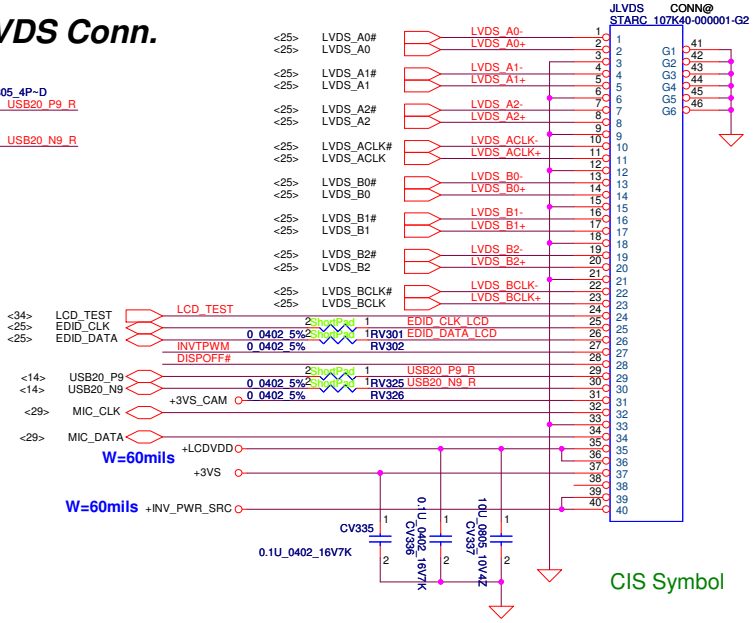


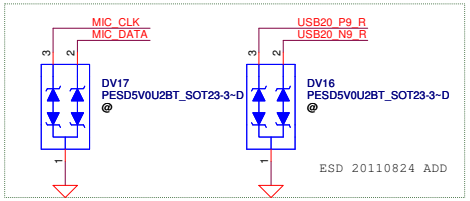
* Reserved for LCD sequence tuning

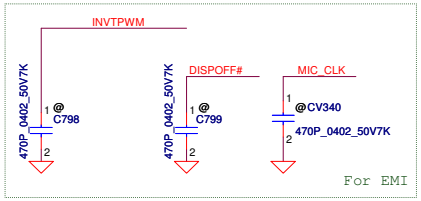


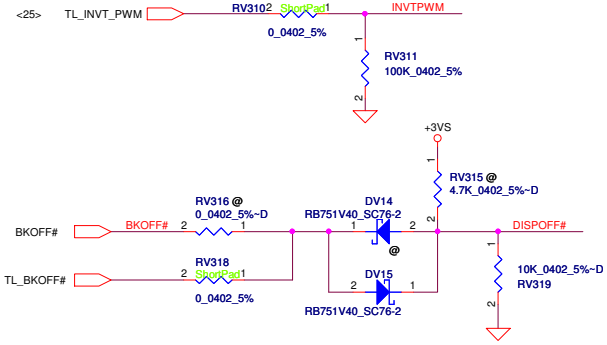
LVDS Conn.











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Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.			
Title	LVDS/CAMERA		
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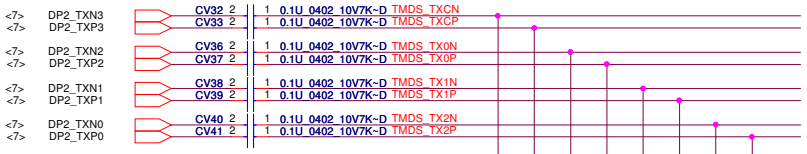
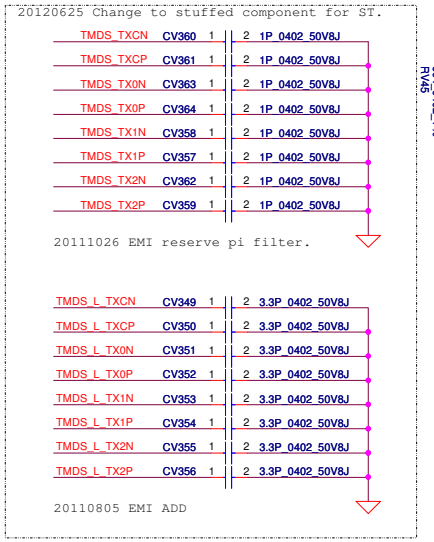
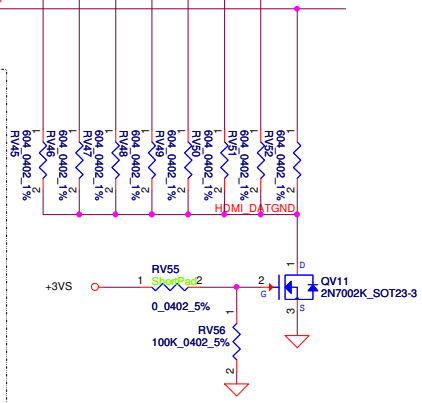
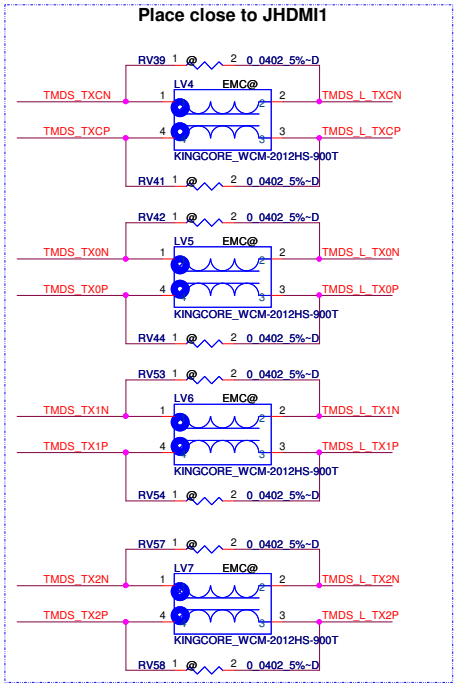
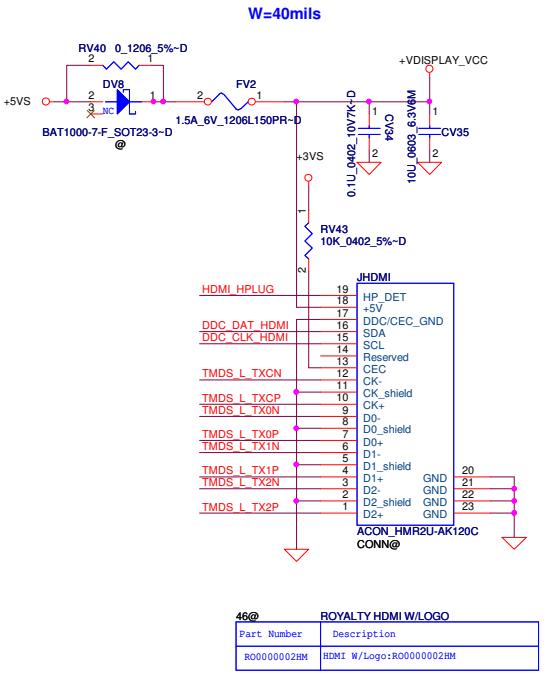




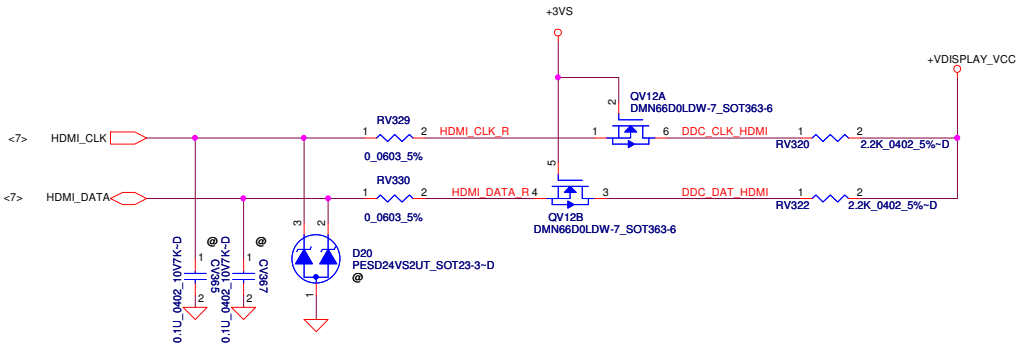


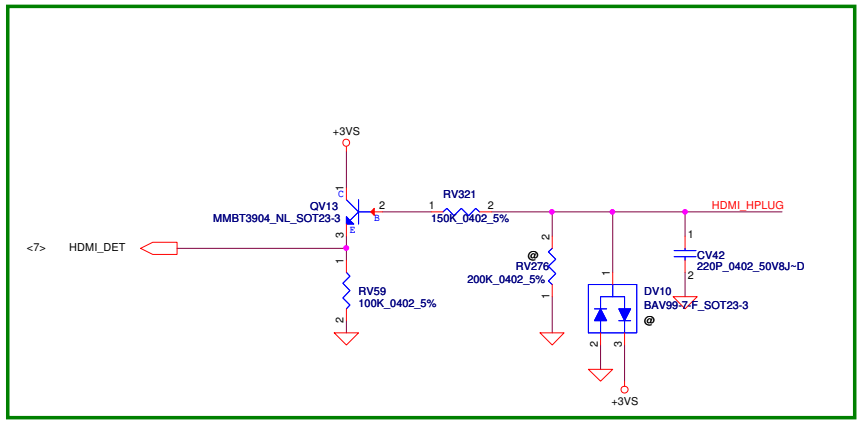




46@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM





Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.

Title: HDMI

Size	Document Number	Rev
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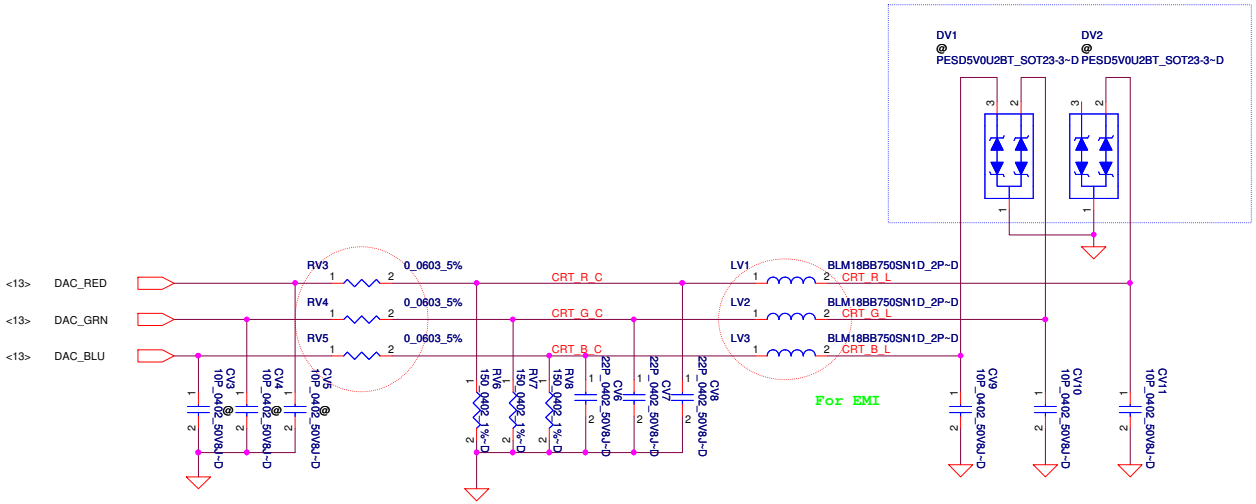
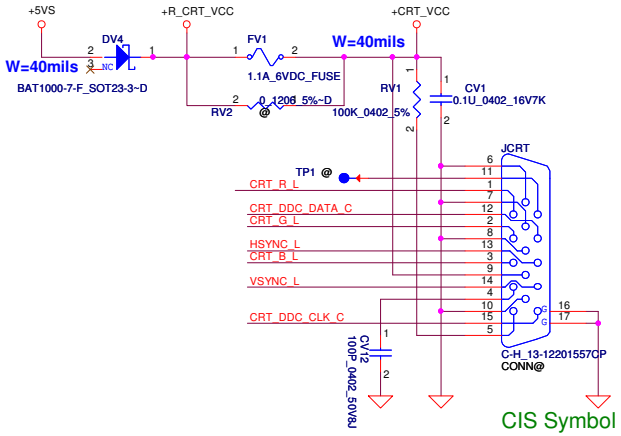
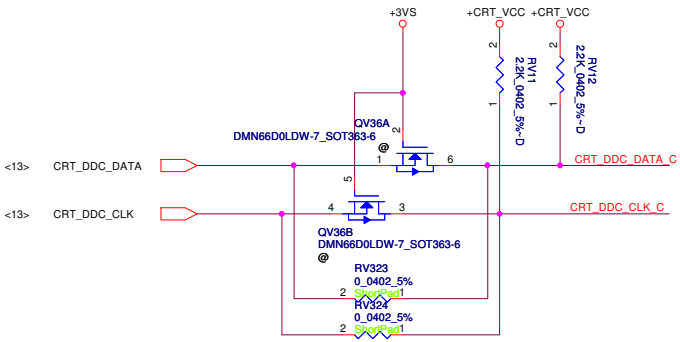
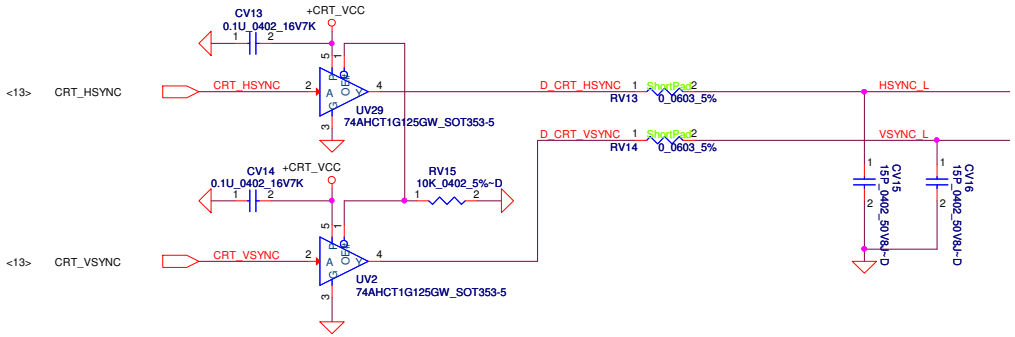
C R T

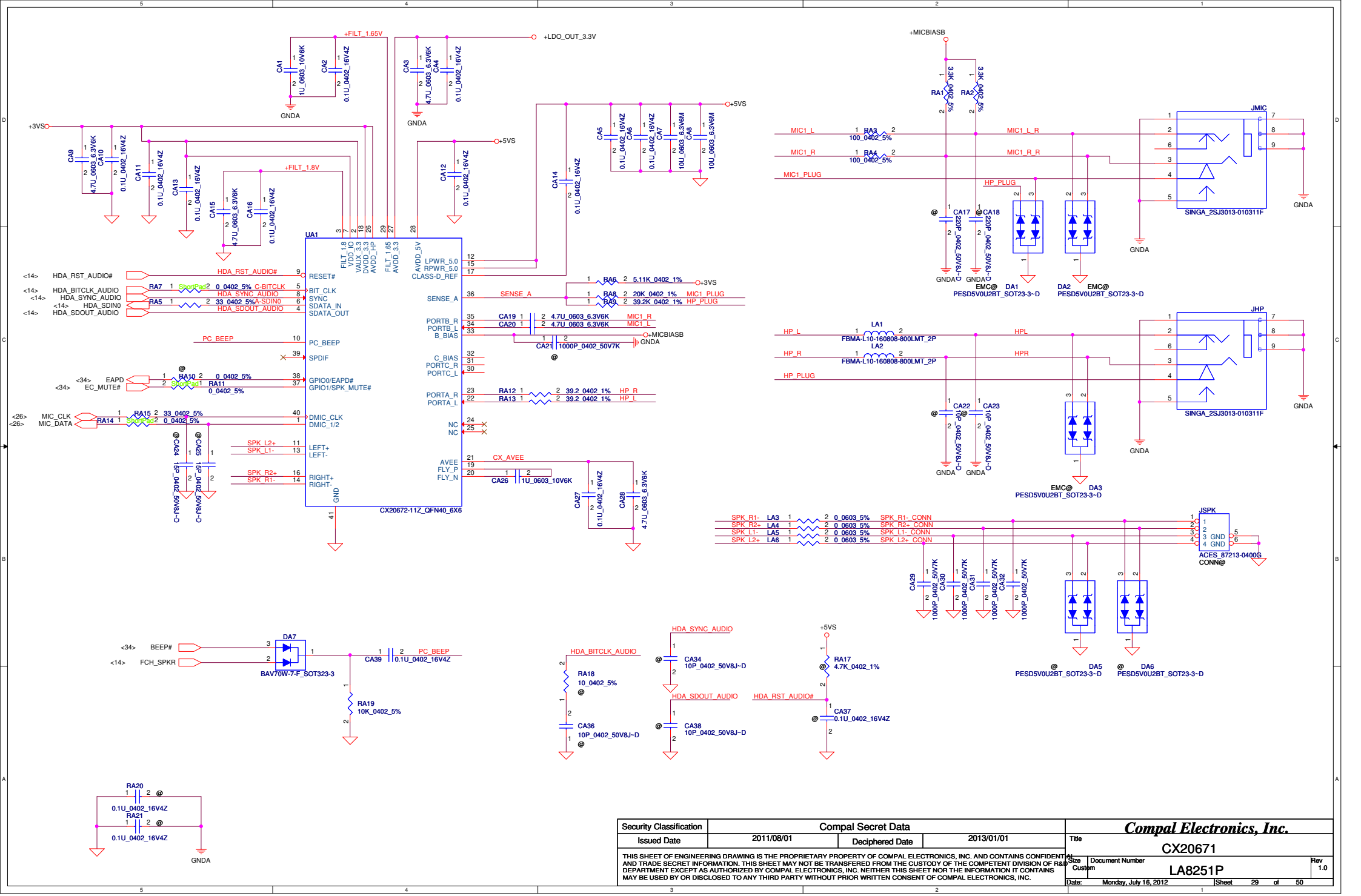








Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/01	Deciphered Date 2013/01/01	Title CRT Conn.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size Document Number LA8251P Rev 1.0
			Date: Monday, July 16, 2012 Sheet 28 of 50



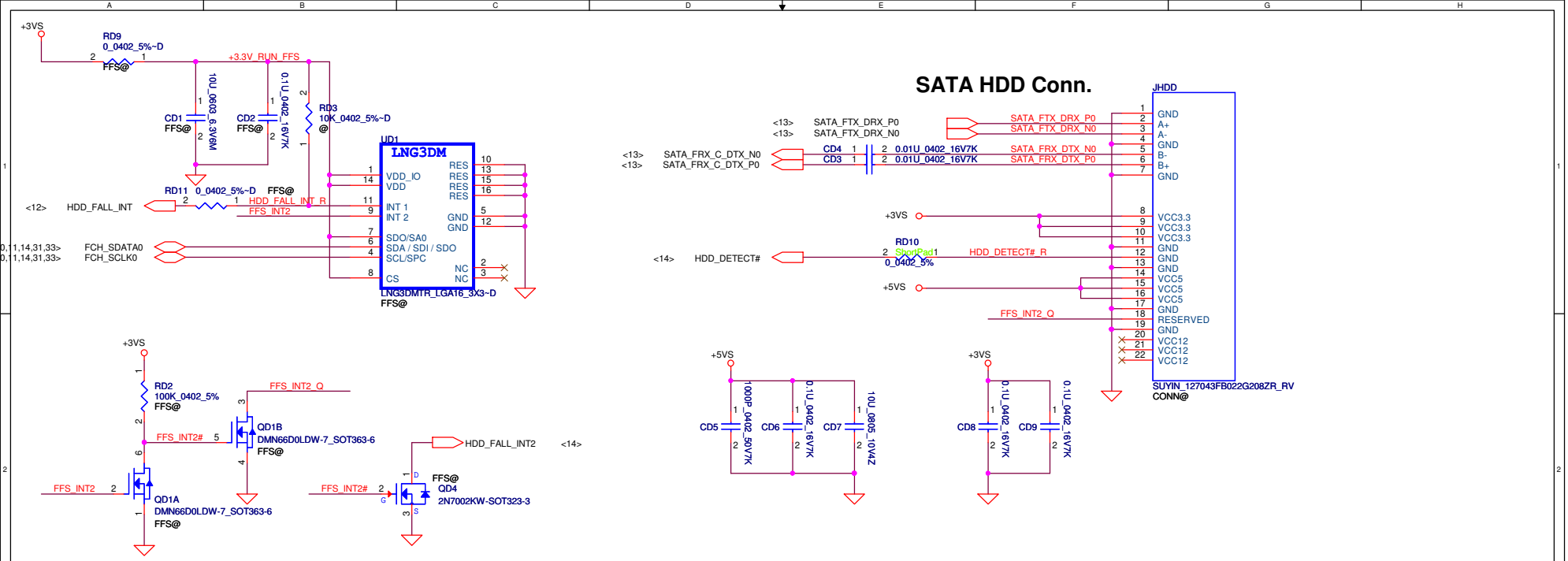
Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

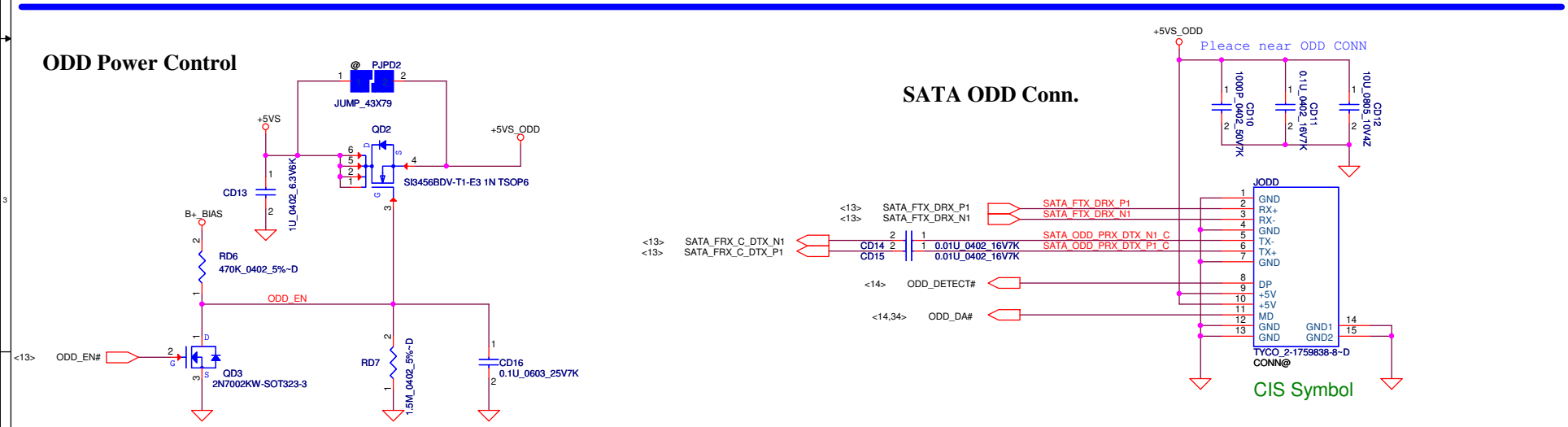
Compal Electronics, Inc.

Title: CX20671

Size: Custom | Document Number: LA8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 29 of 50

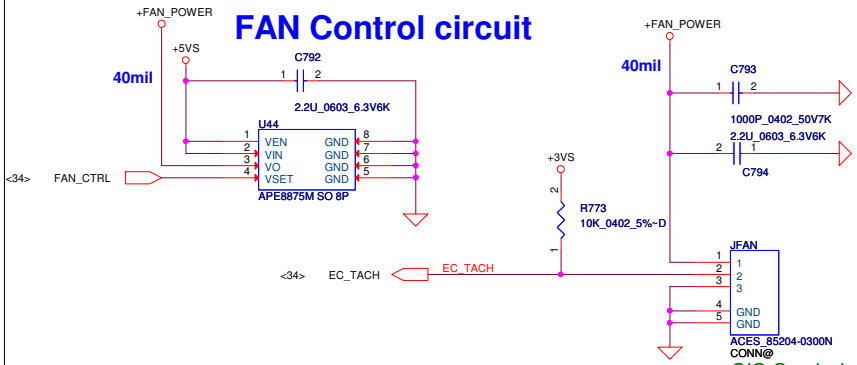




Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

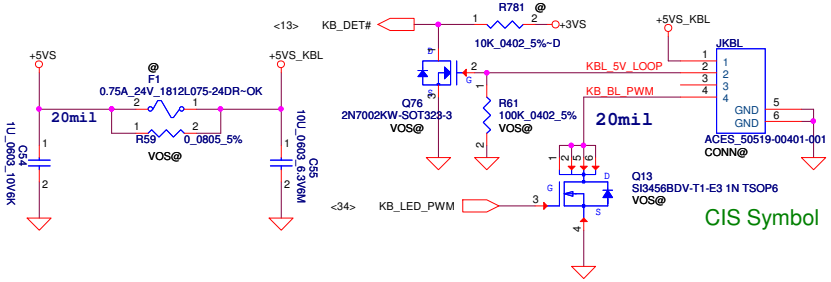
Compal Electronics, Inc.			
Title	HDD/ODD/FAN		
Size: Custom	Document Number: LA8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 30 of 50		

FAN Control circuit



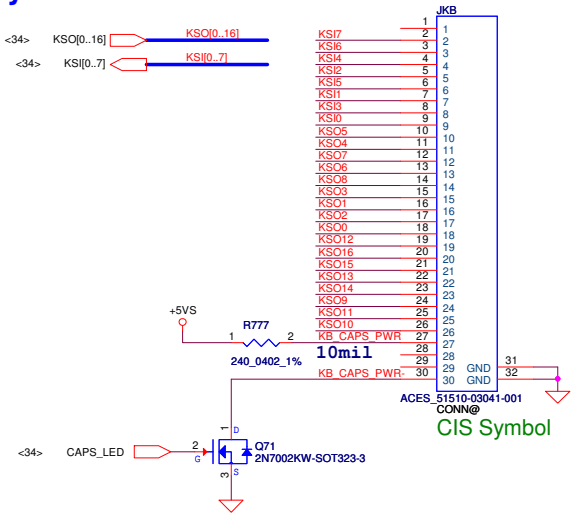
CIS Symbol

Keyboard back light



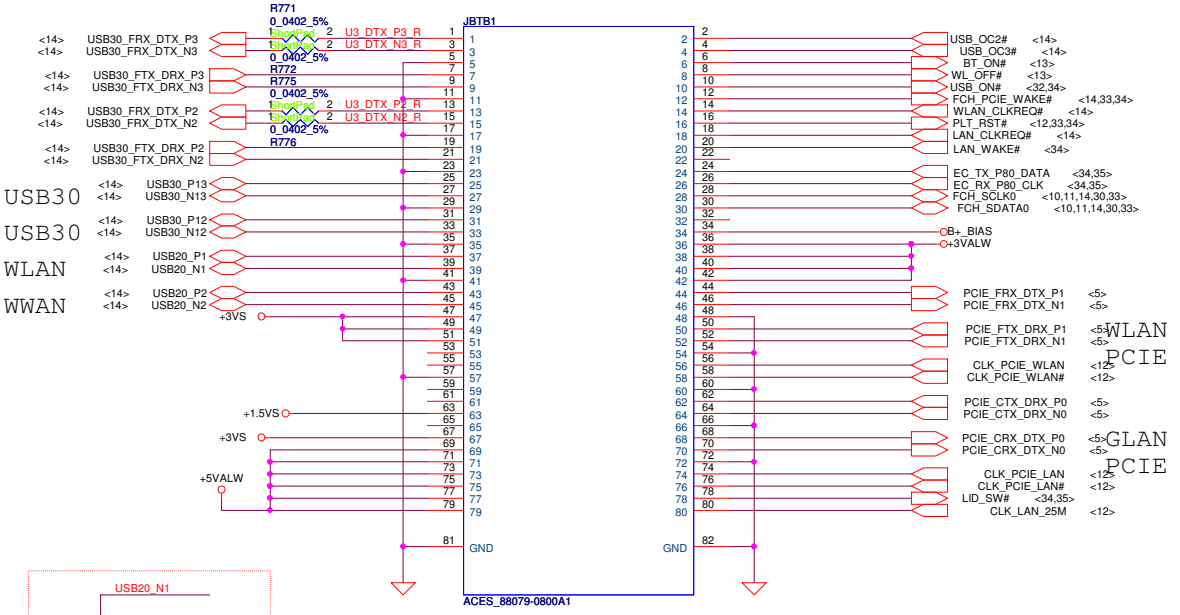
CIS Symbol

Keyboard Connector

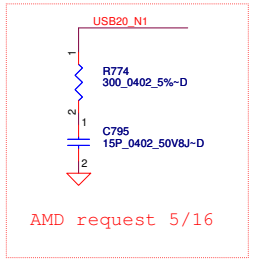


CIS Symbol

M/B to D/B BTB connector, LAN, FMC, HMC, USB3.0*2

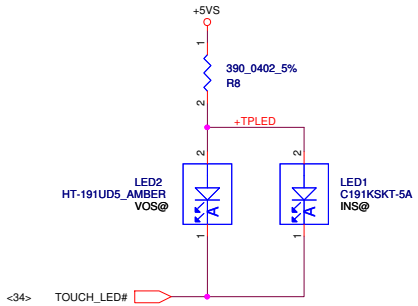


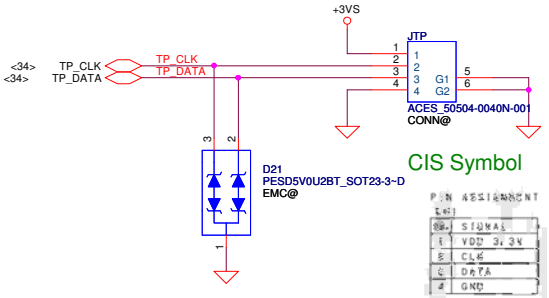
CIS Symbol, Receptacle.



AMD request 5/16

Touch pad





CIS Symbol

Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.

Title: IO brd Conn & FAN/KB/TP

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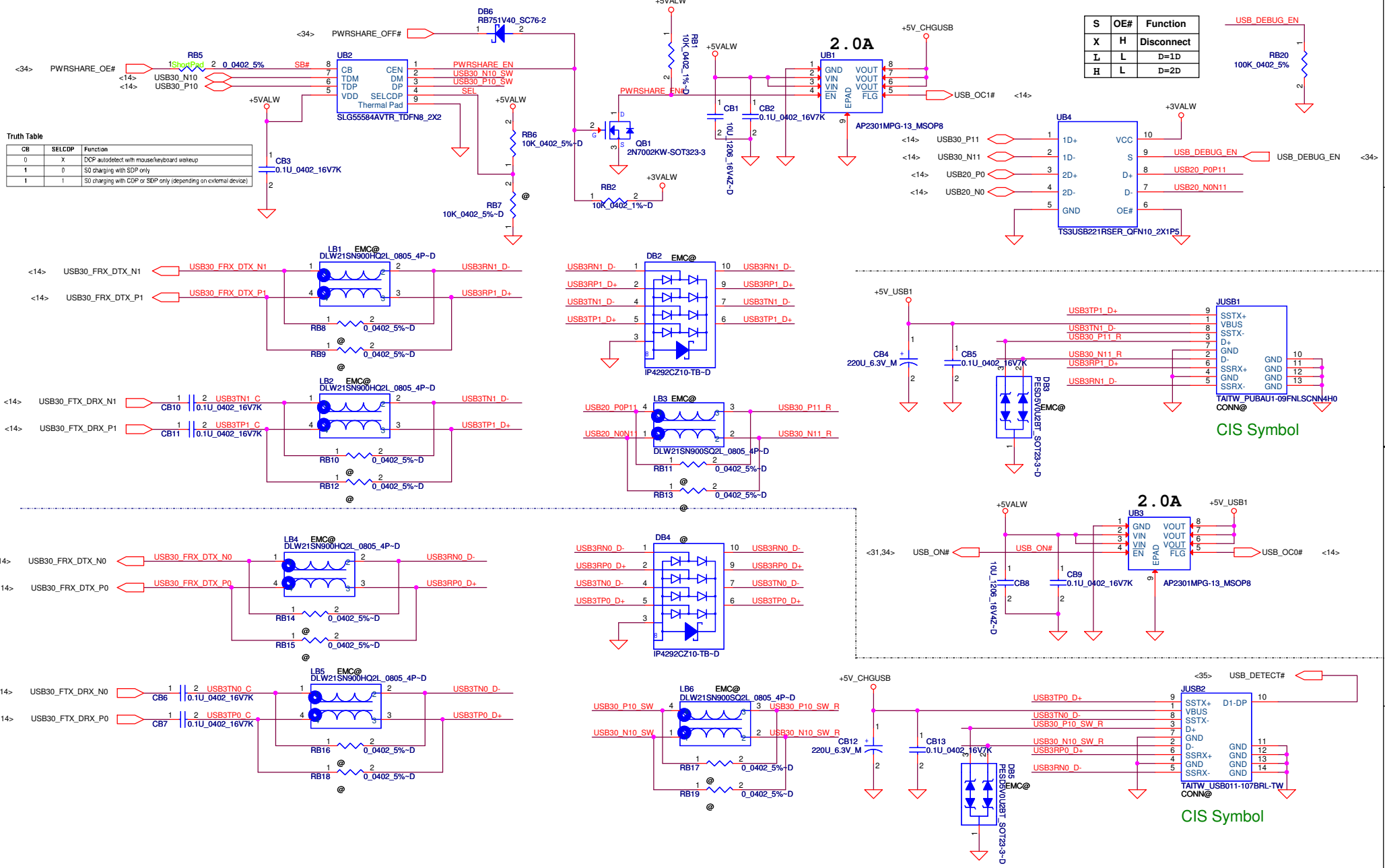
Power share

CB	Function
L	auto detection charger identification active
H	DP/DM=TDP/TDM

S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

Truth Table

CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)



Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.

Title: USB LP1/2

Size: Custom | Document Number: LA8251P | Rev: 1.0

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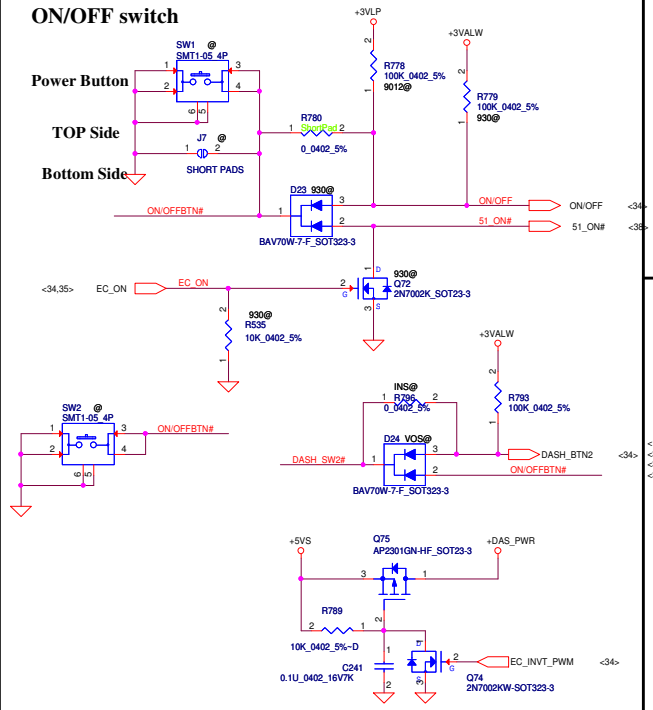
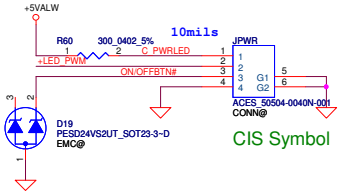
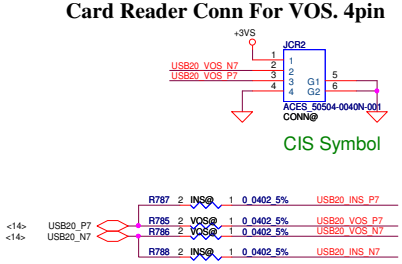
ON/OFF switch

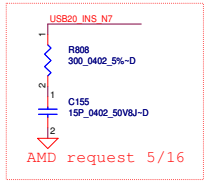


Power Button Board Conn. 4pin

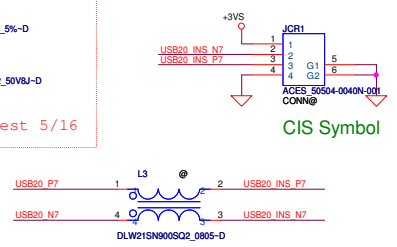


Card Reader Conn For VOS. 4pin

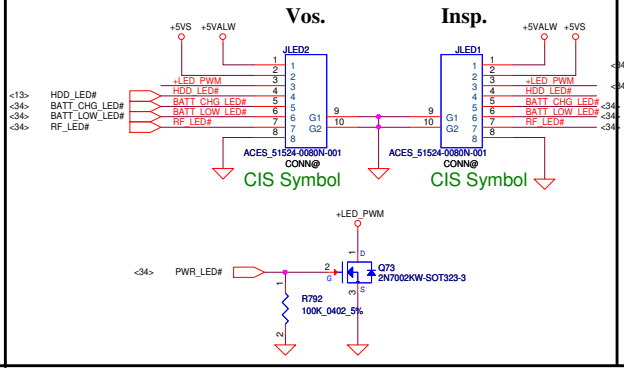




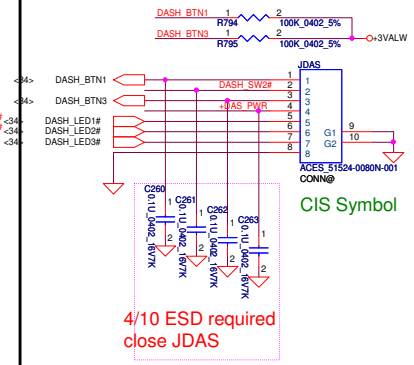
Card Reader Conn For INS.



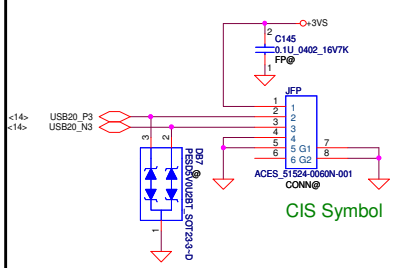
LED Board Conn, include LID SW. 10pin



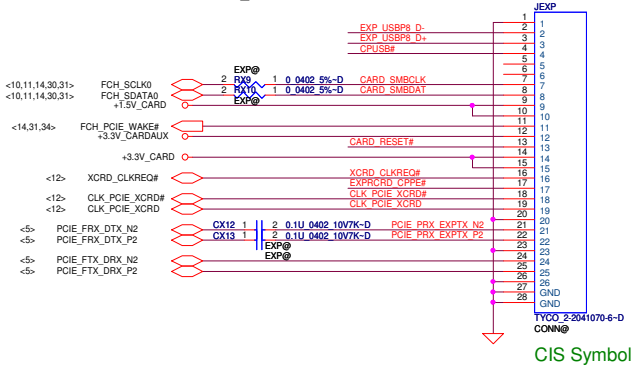
Dashboard Function Conn. 8pin

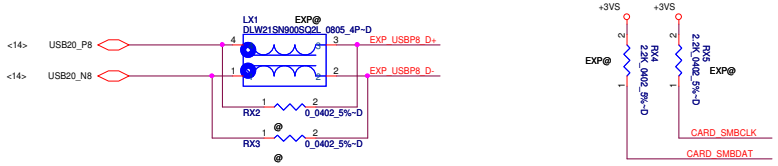


Finger Printer Conn. 6pin

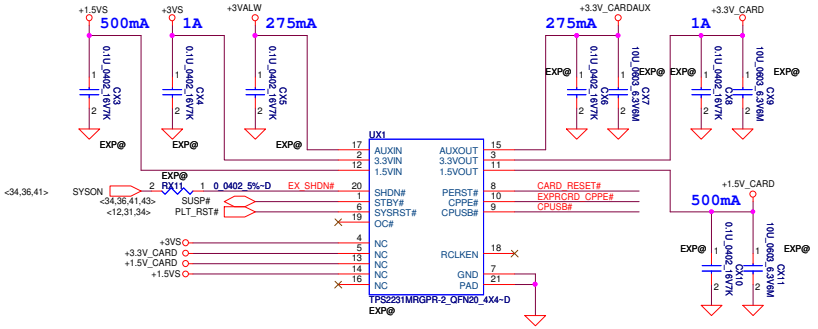


Express Card





Express Card PWR S/W



Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.	
Title	Other IO Conn. ExCARD
Size C	Document Number LA8251P
Rev	1.0
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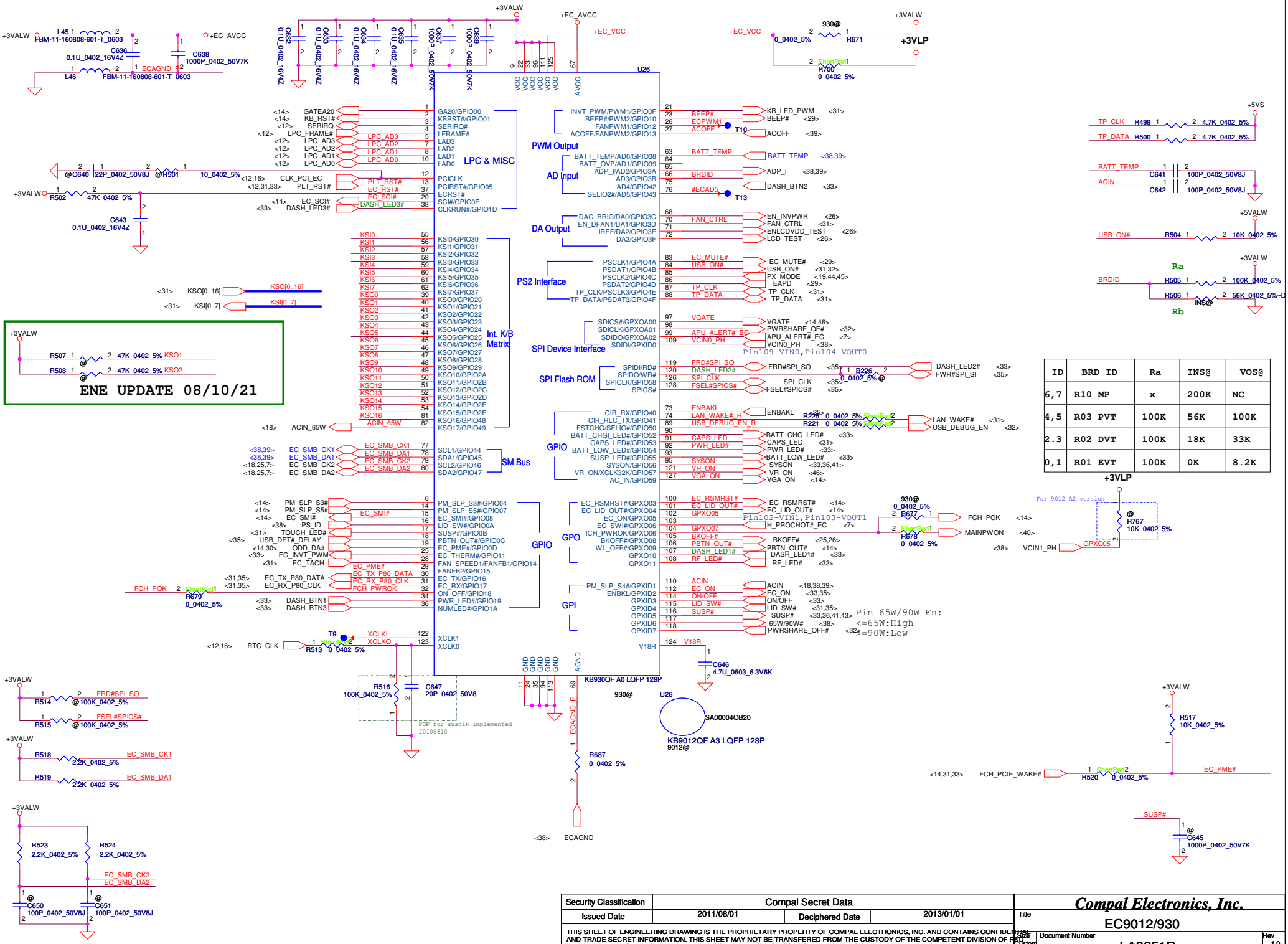


ID	BRD ID	Ra	INS@	VOS@
6,7	R10 MP	x	200K	NC
4,5	R03 PVT	100K	56K	100K
2,3	R02 DVT	100K	18K	33K
0,1	R01 EVT	100K	0K	8.2K

Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

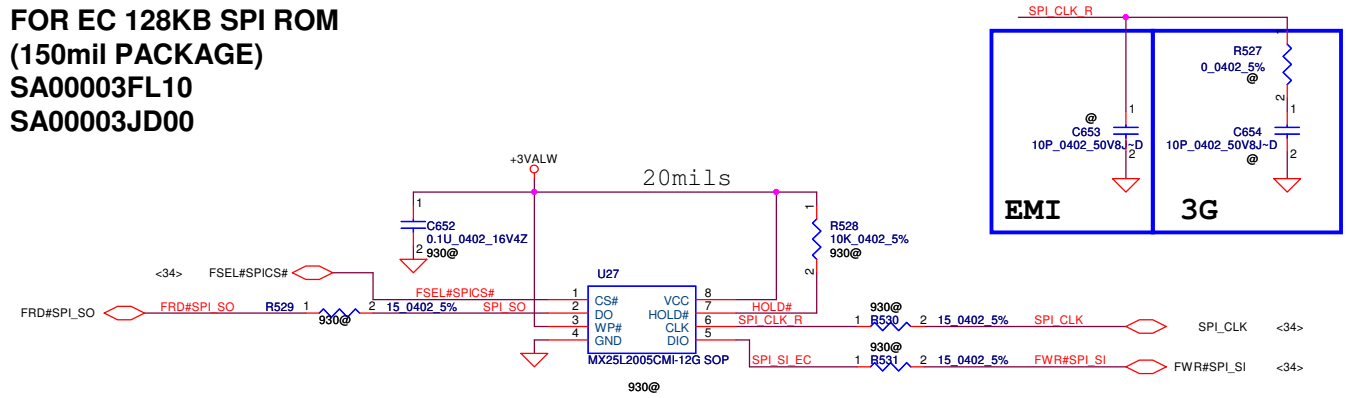
Compal Electronics, Inc.

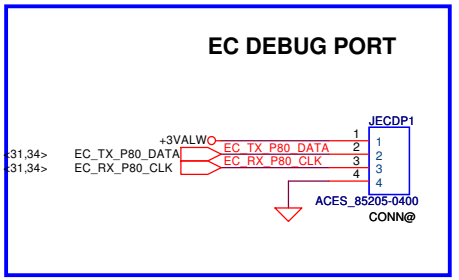
Title: EC9012/930

Size: Custom | Document Number: LA8251P | Rev: 1.0

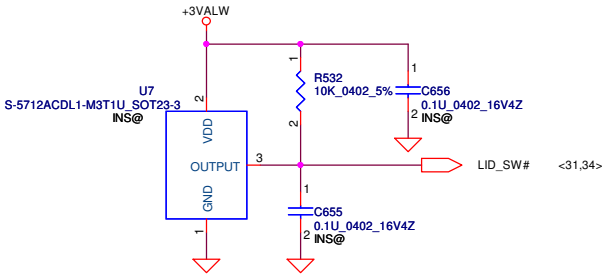
Date: Monday, July 16, 2012 | Sheet 34 of 50

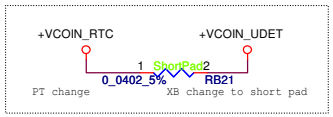
FOR EC 128KB SPI ROM
(150mil PACKAGE)
SA00003FL10
SA00003JD00



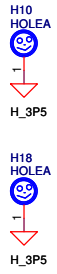


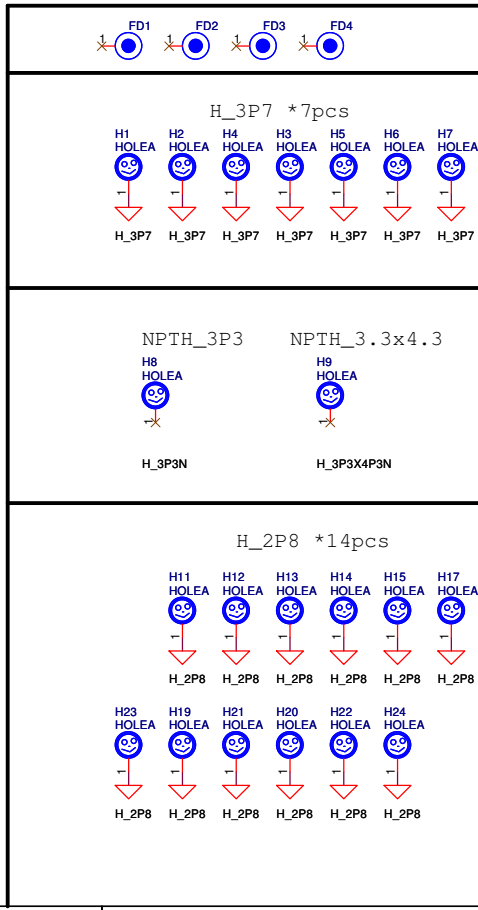
LID SWITCH FOR INS. ONLY





H_3P5 *2pcs





Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.

Title: EC ROM/Debug

Size: B | Document Number: LA8251P | Rev: 1.0

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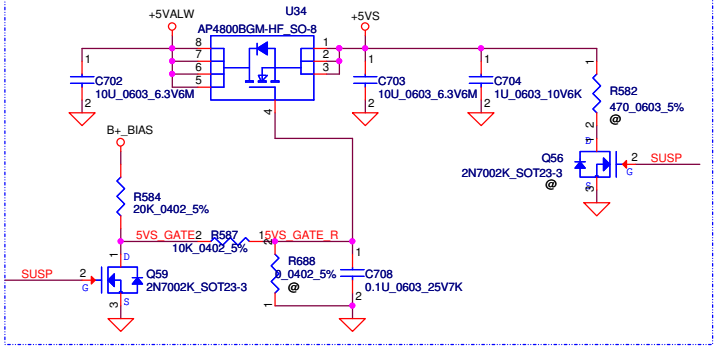
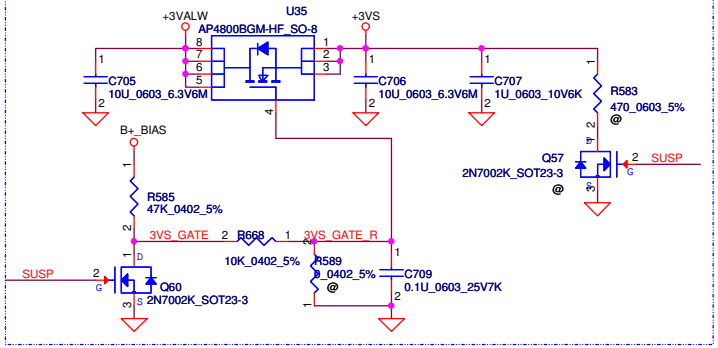
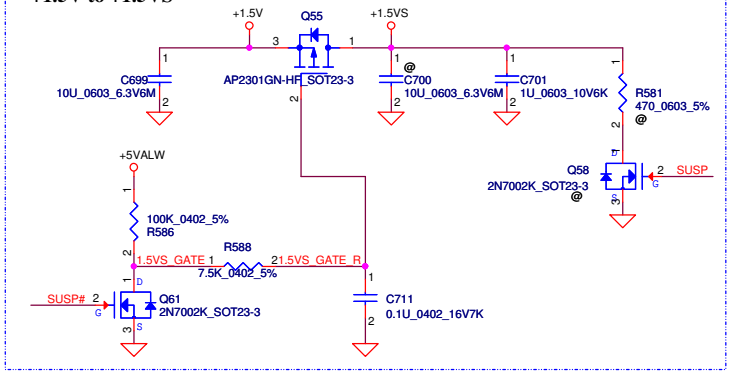
+5VALW TO +5VS



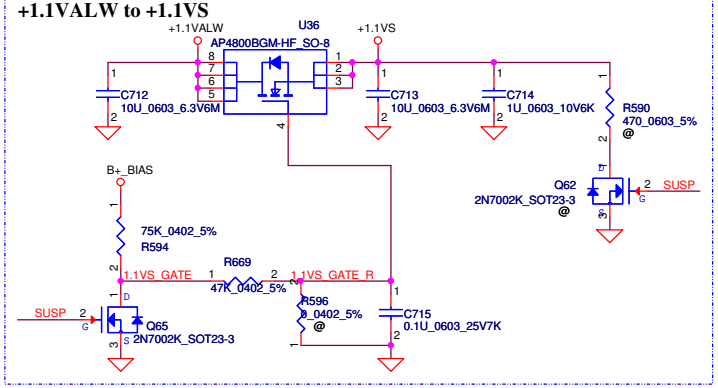
+3VALW TO +3VS

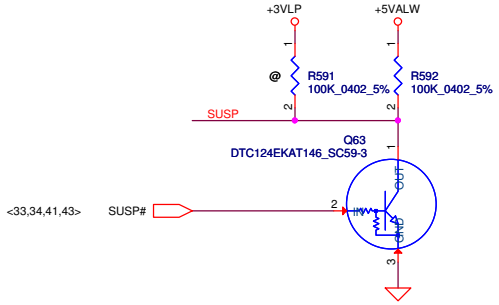


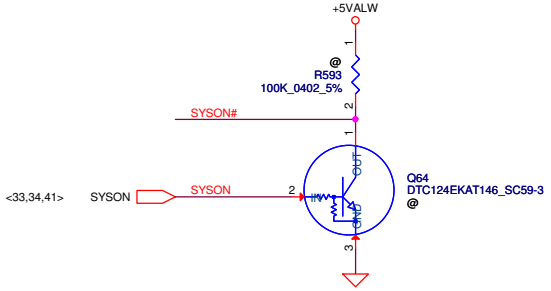
+1.5V to +1.5VS

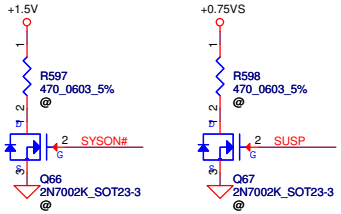


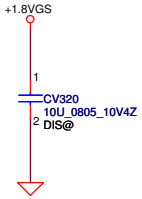
+1.1VALW to +1.1VS

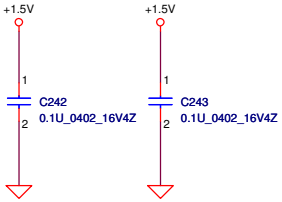




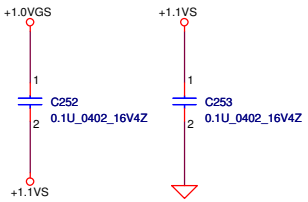




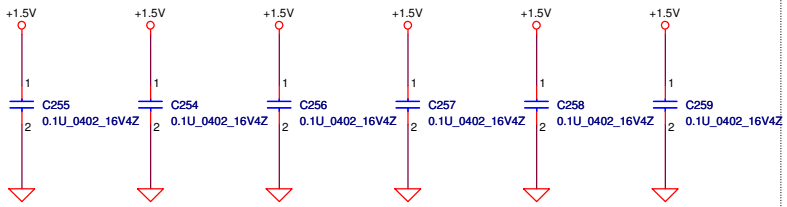




For USB3.0 Cross Moat On Bottom



ESD demand in PT



EMI Adding for PT, 2011/11/28

Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: LA8251P | Rev: 1.0

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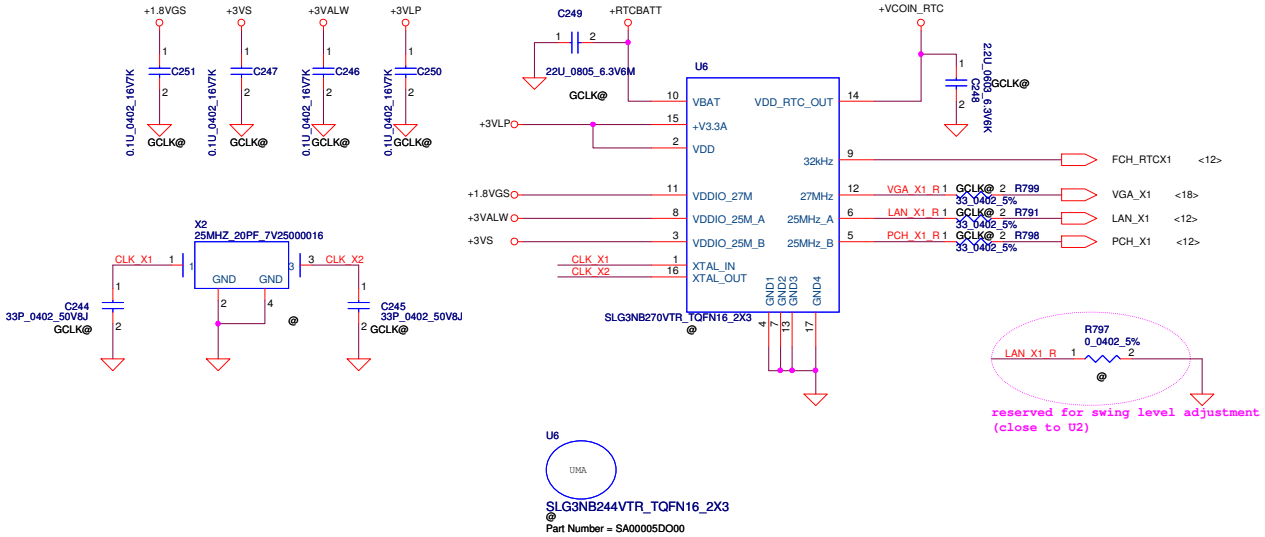

Compal Electronics, Inc.

Title: **AMP & GCLK**

Size	Document Number	Rev
Custom	LA8251P	1.0

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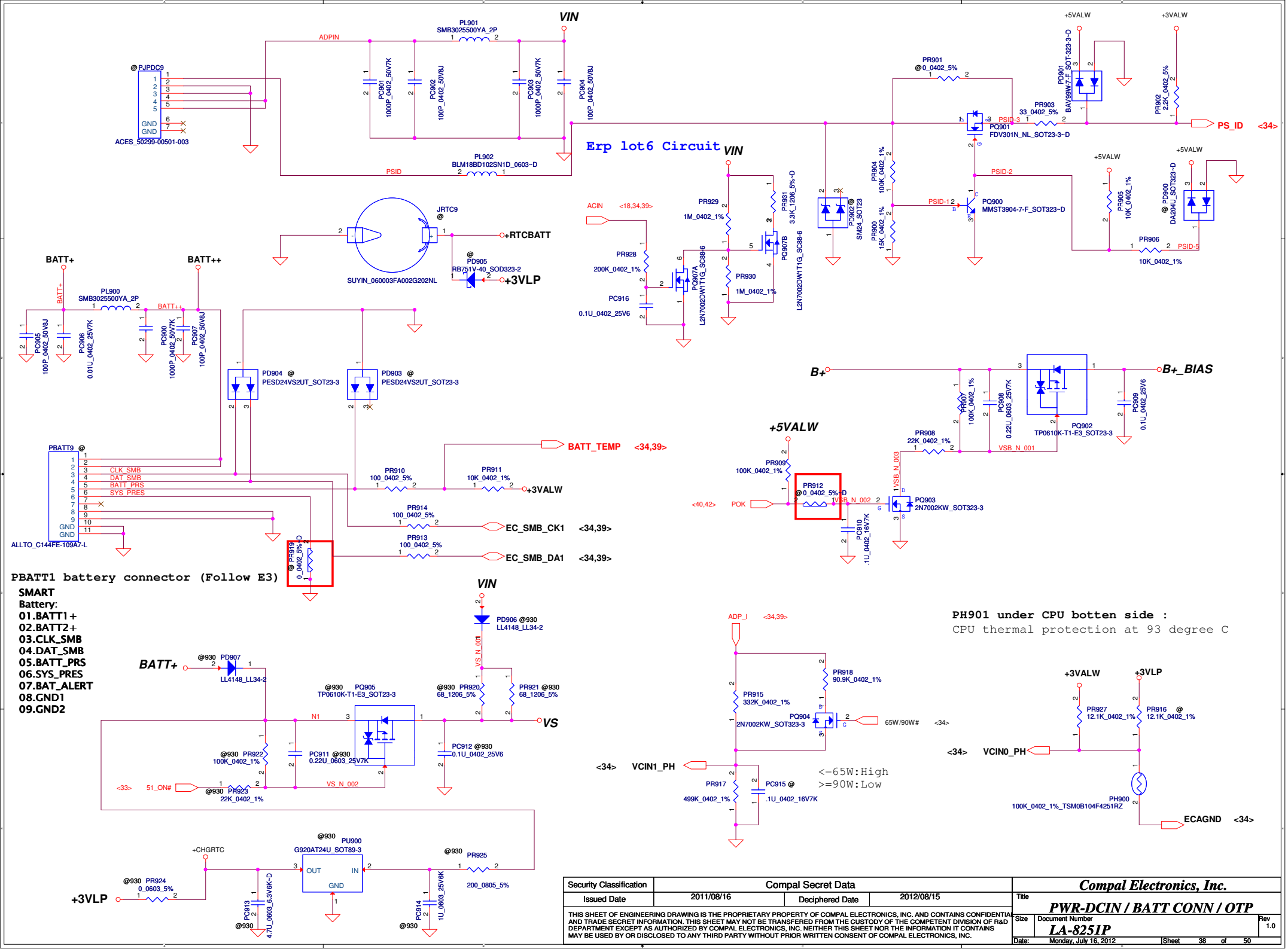
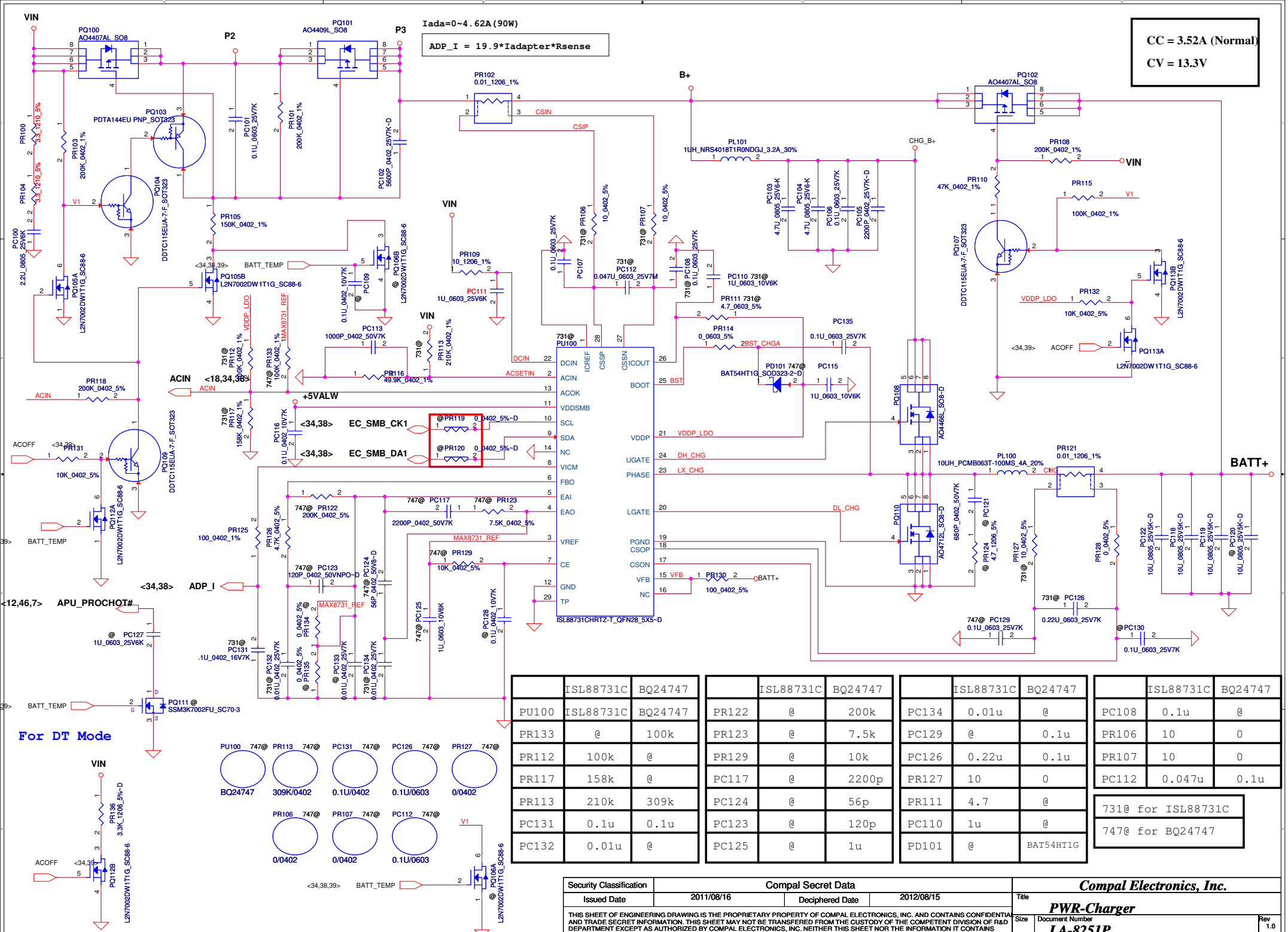


Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Compal Electronics, Inc.			
Title	PWR-DCIN / BATT CONN / OTP		
Size	Document Number LA-8251P		Rev 1.0
Date: Monday, July 16, 2012		Sheet 38 of 50	



	ISL88731C	BQ24747
PU100	ISL88731C	BQ24747
PR133	@	100k
PR112	100k	@
PR117	158k	@
PR113	210k	309k
PC131	0.1u	0.1u
PC132	0.01u	@

	ISL88731C	BQ24747
PR122	@	200k
PR123	@	7.5k
PR129	@	10k
PC117	@	2200p
PC124	@	56p
PC123	@	120p
PC125	@	1u

	ISL88731C	BQ24747
PC134	0.01u	@
PC129	@	0.1u
PC126	0.22u	0.1u
PR127	10	0
PC110	1u	@
PD101	@	BAT54HT1G

	ISL88731C	BQ24747
PC108	0.1u	@
PR106	10	0
PR107	10	0
PC112	0.047u	0.1u

731@ for ISL88731C
747@ for BQ24747

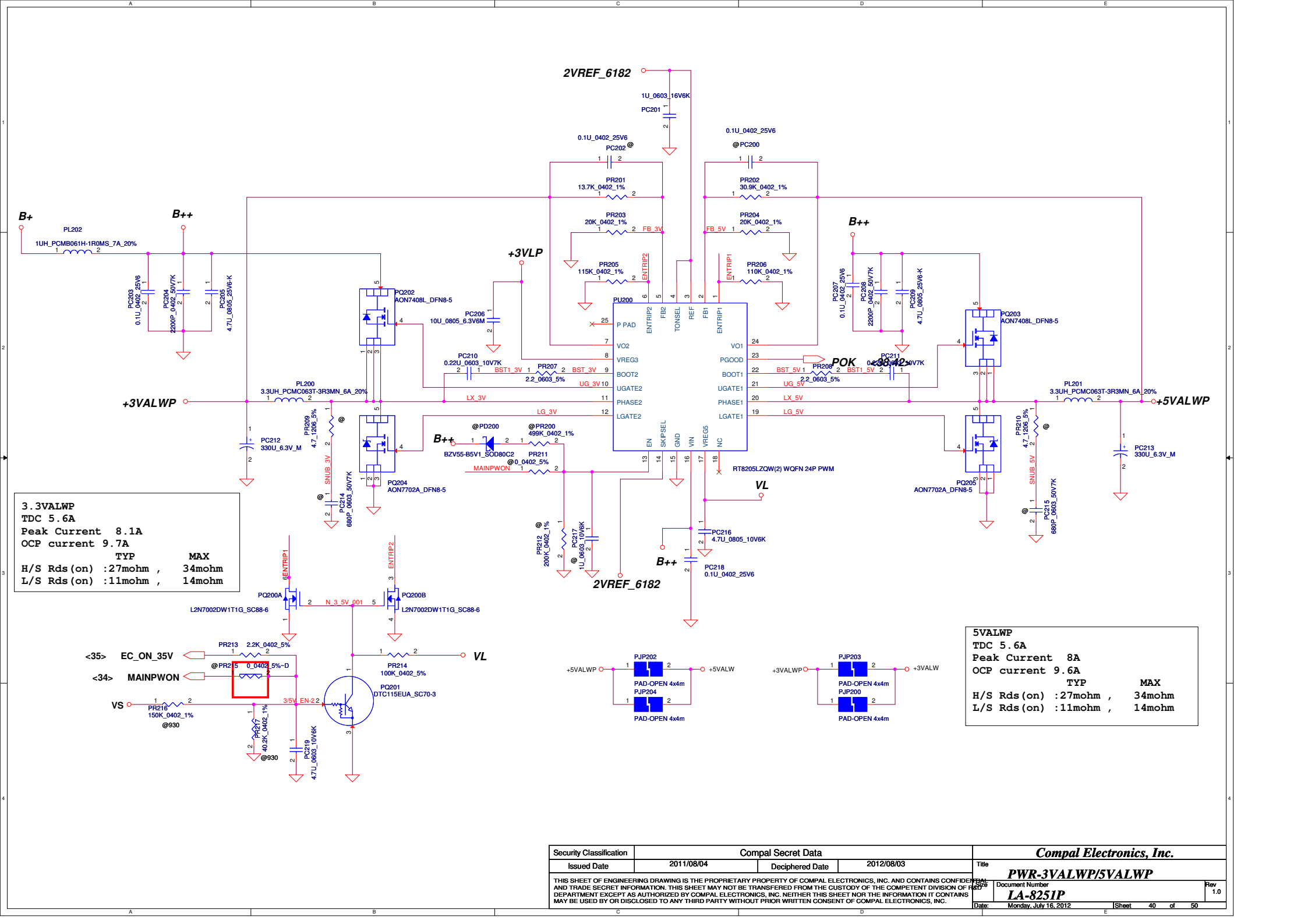
Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Compal Electronics, Inc.

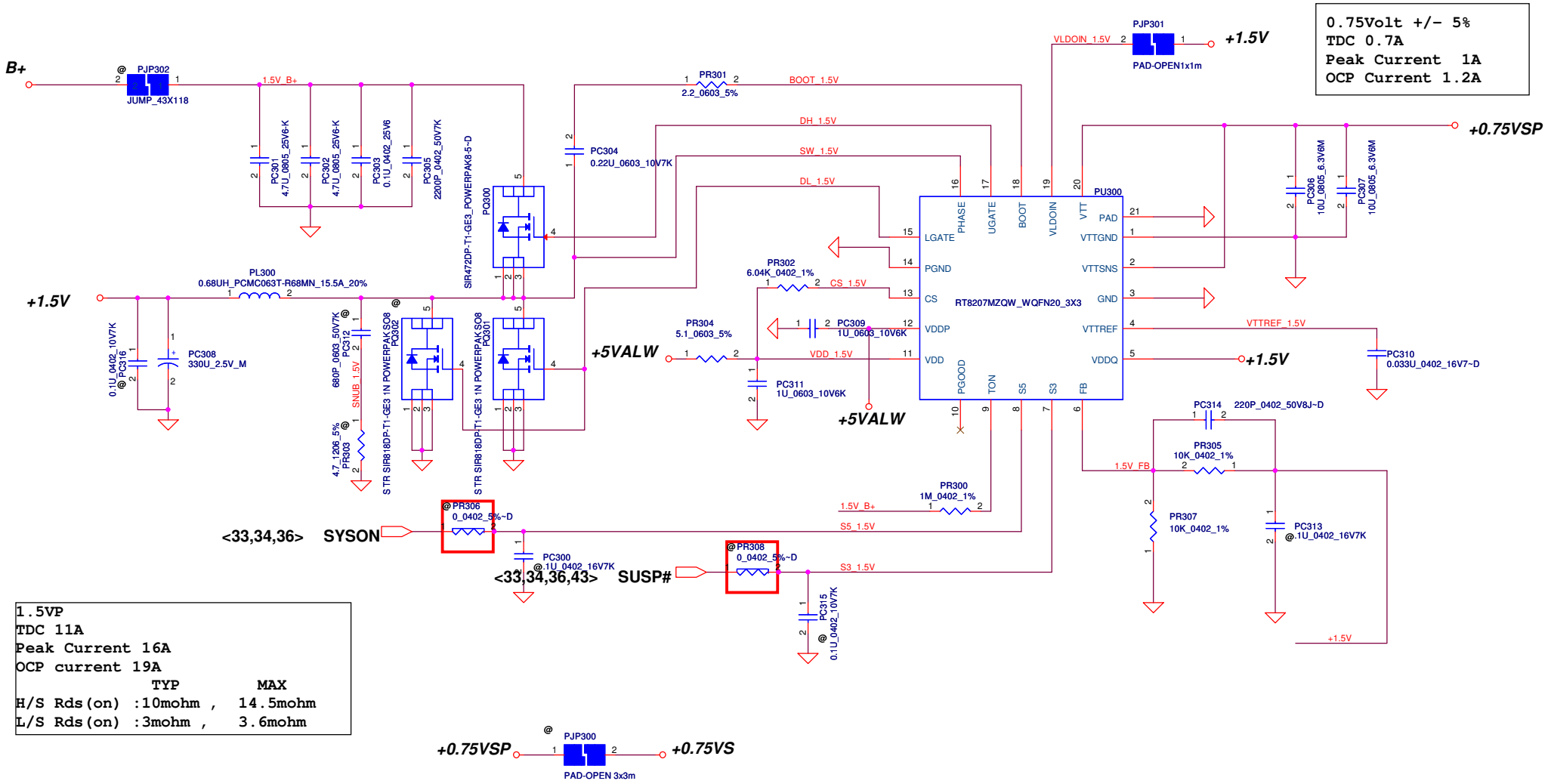
Title: PWR-Charger

Size | Document Number: LA-8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 39 of 50



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/04	Deciphered Date	2012/08/03
Title	PWR-3VALWP/5VALWP		
Size	Document Number		Rev
	LA-8251P		1.0
Date:	Monday, July 16, 2012	Sheet	40 of 50



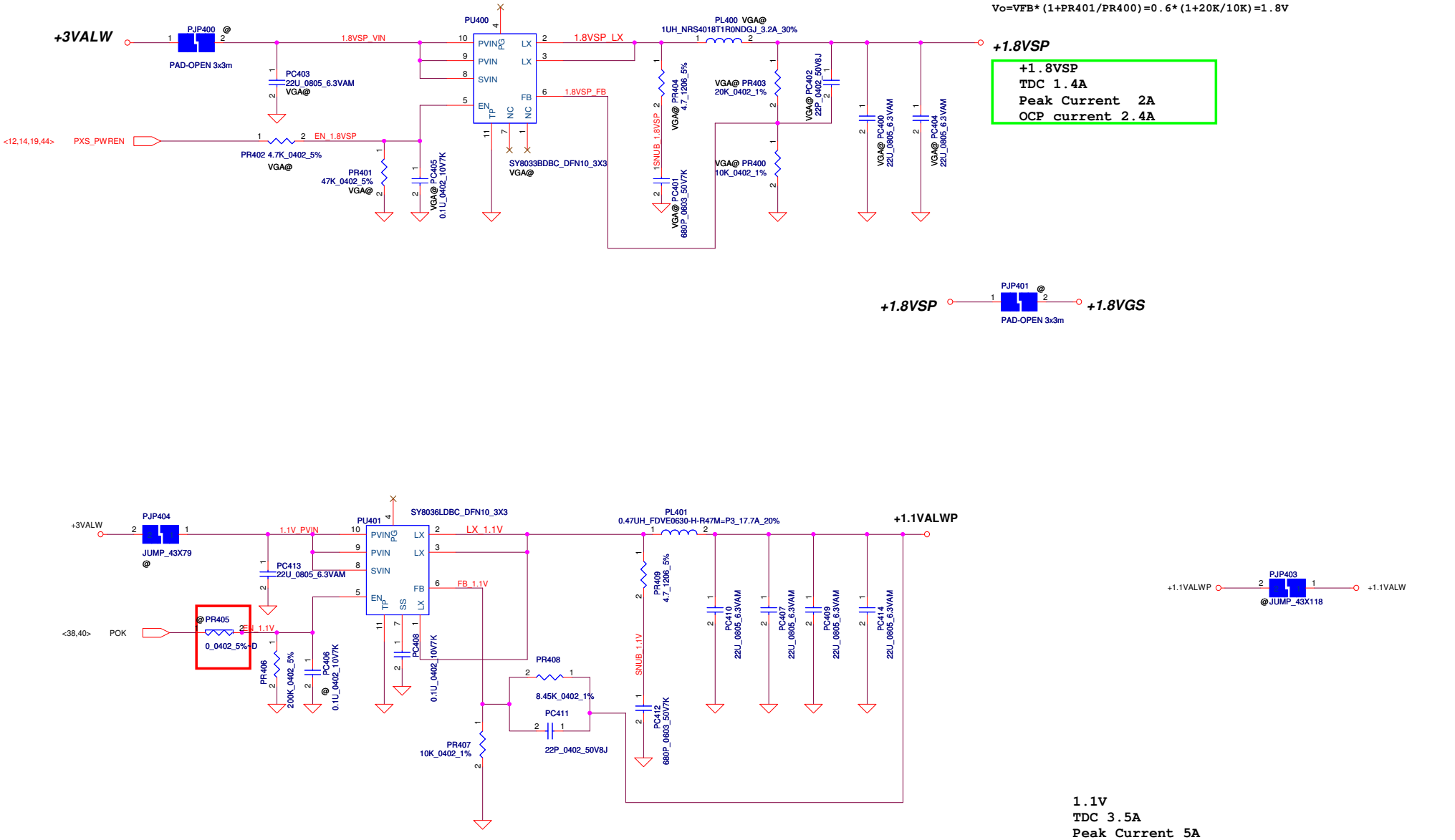
Security Classification	Compal Secret Data		
Issued Date	2011/08/04	Deciphered Date	2012/08/03

Compal Electronics, Inc.

Title: PWR-1.5V/0.75VSP

Size | Document Number: LA-8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 41 of 50



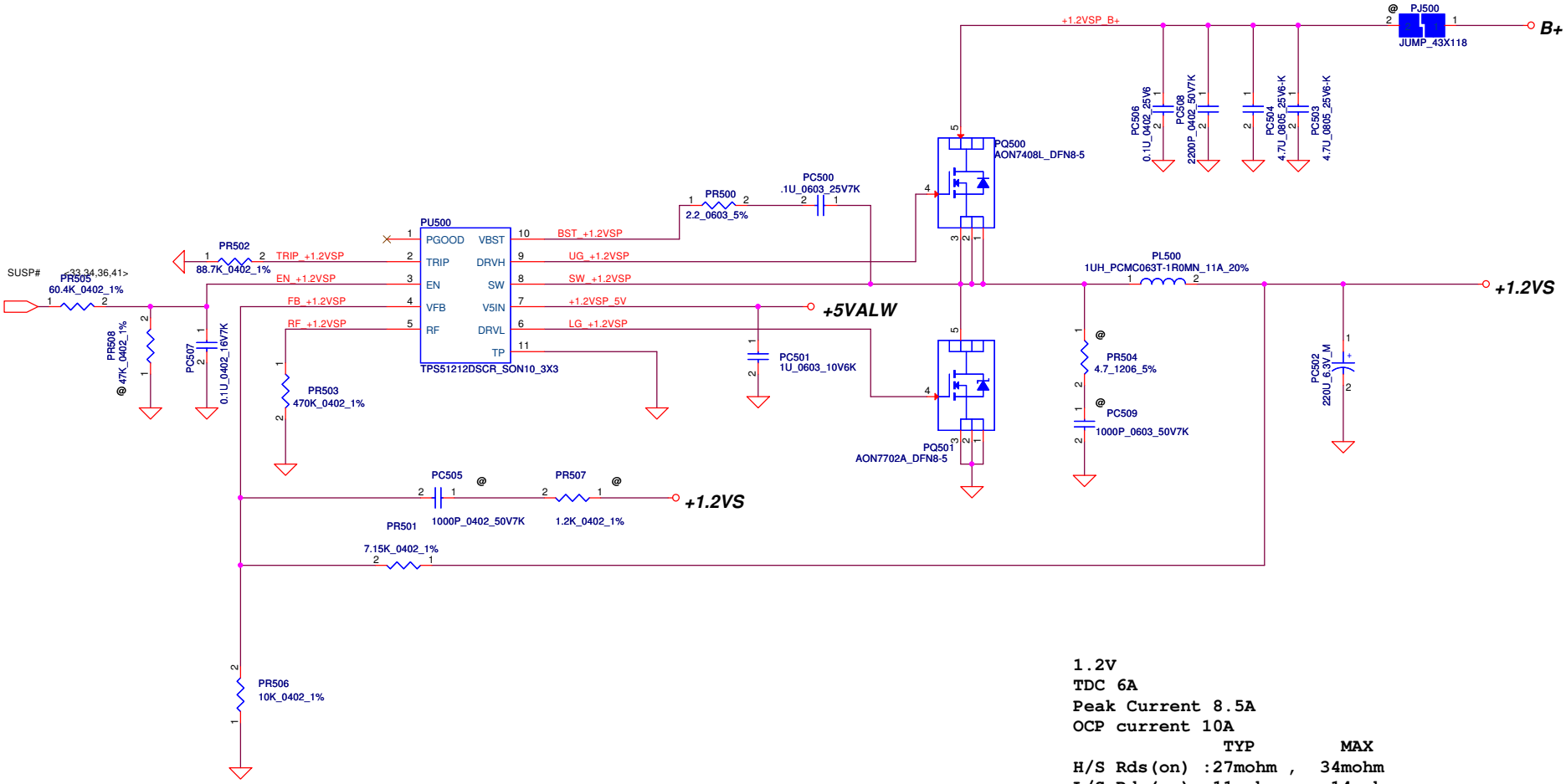
Security Classification	Compal Secret Data		
Issued Date	2011/08/04	Deciphered Date	2012/08/03

Compal Electronics, Inc.

Title: **PWR-1.8VSP/1.1VALWP**

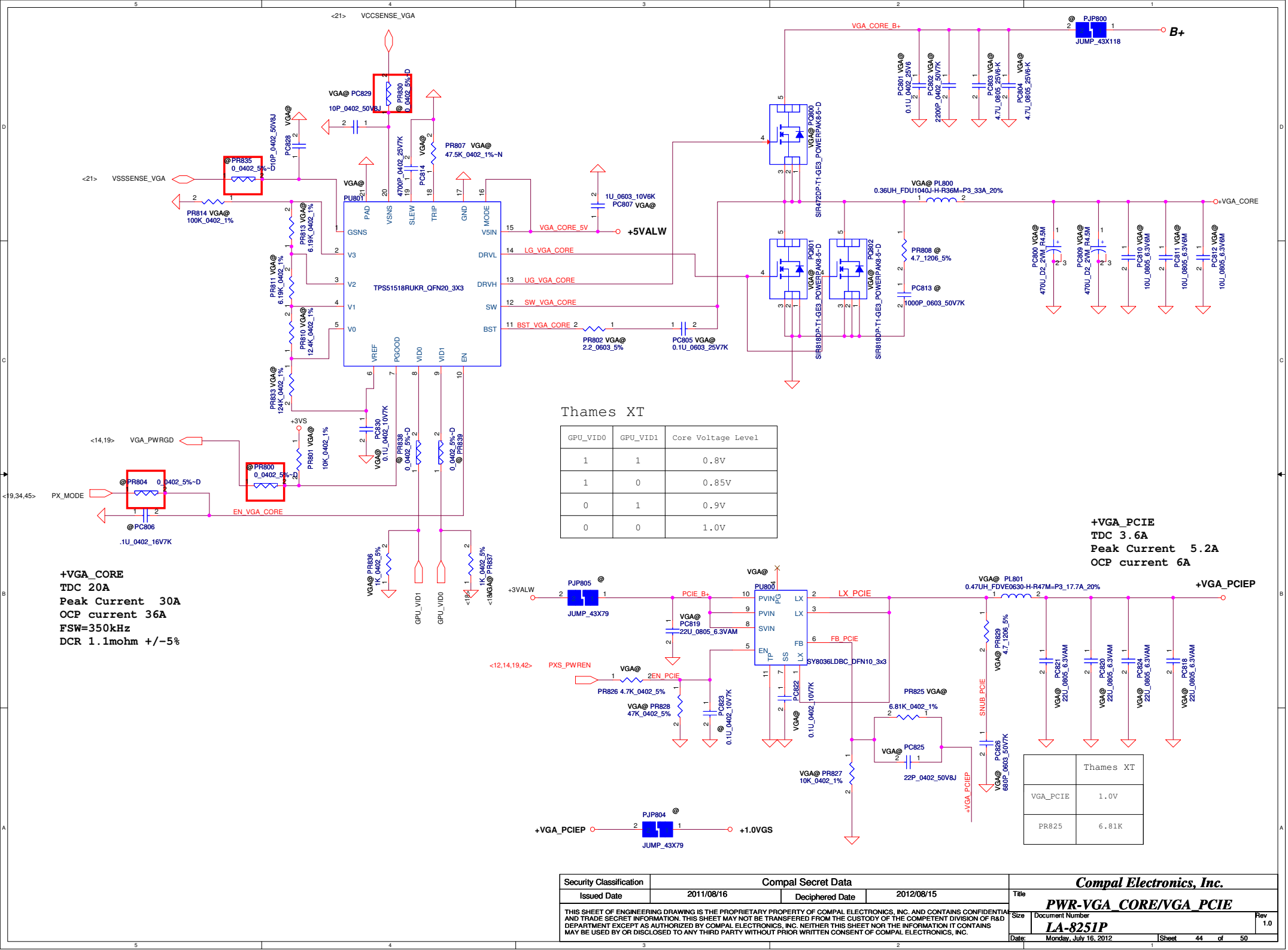
Size | Document Number: **LA-8251P** | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 42 of 50



Security Classification	Compal Secret Data		
Issued Date	2011/08/04	Deciphered Date	2012/08/03

Compal Electronics, Inc.			
Title: PWR-1.2VSP/2.5VSP			
Size	Document Number: LA-8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 43 of 50		



Thames XT

GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.8V
1	0	0.85V
0	1	0.9V
0	0	1.0V

	Thames XT
VGA_PCIE	1.0V
PR825	6.81K

Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Compal Electronics, Inc.	
Title	PWR-VGA_CORE/VGA_PCIE
Size	Document Number: LA-8251P
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Date:	Monday, July 16, 2012
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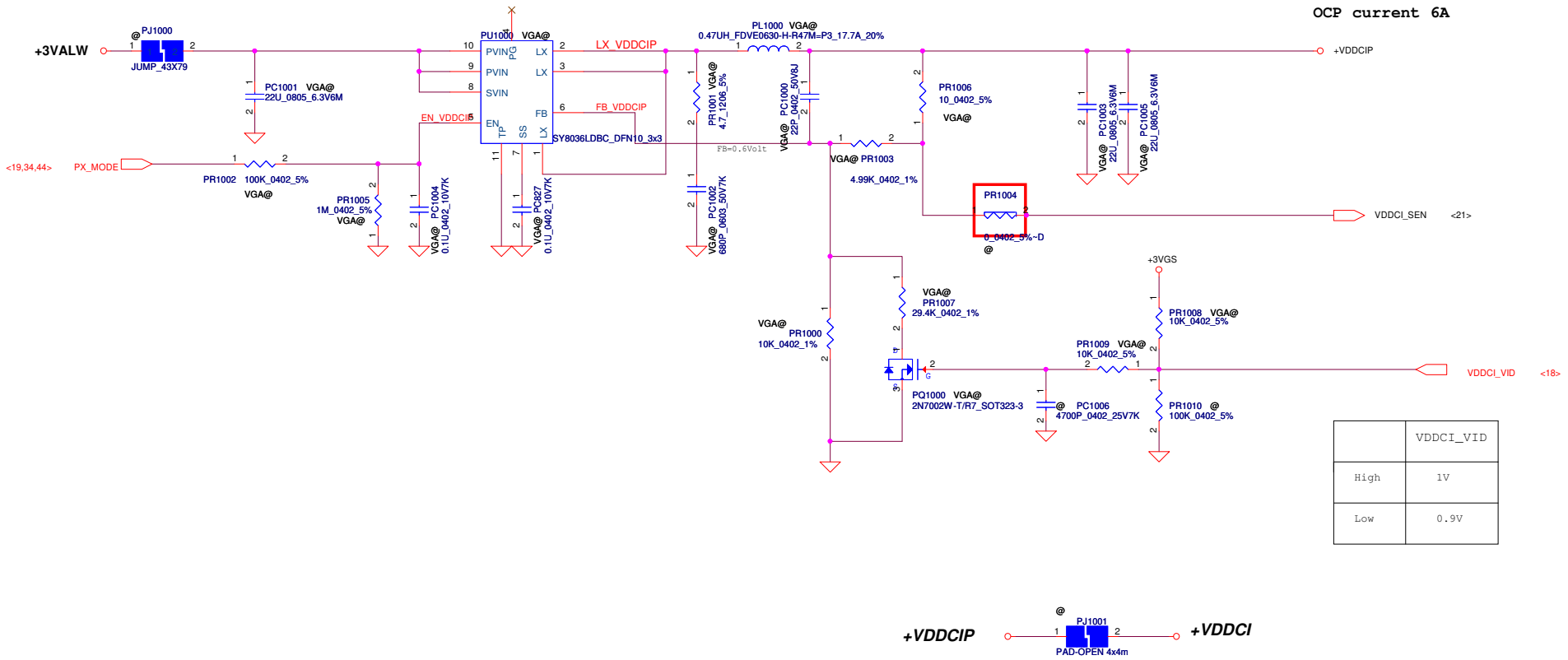
+VDDCI
TDC 2.8A
Peak Current 4A
OCP current 6A



	VDDCI_VID
High	1V
Low	0.9V

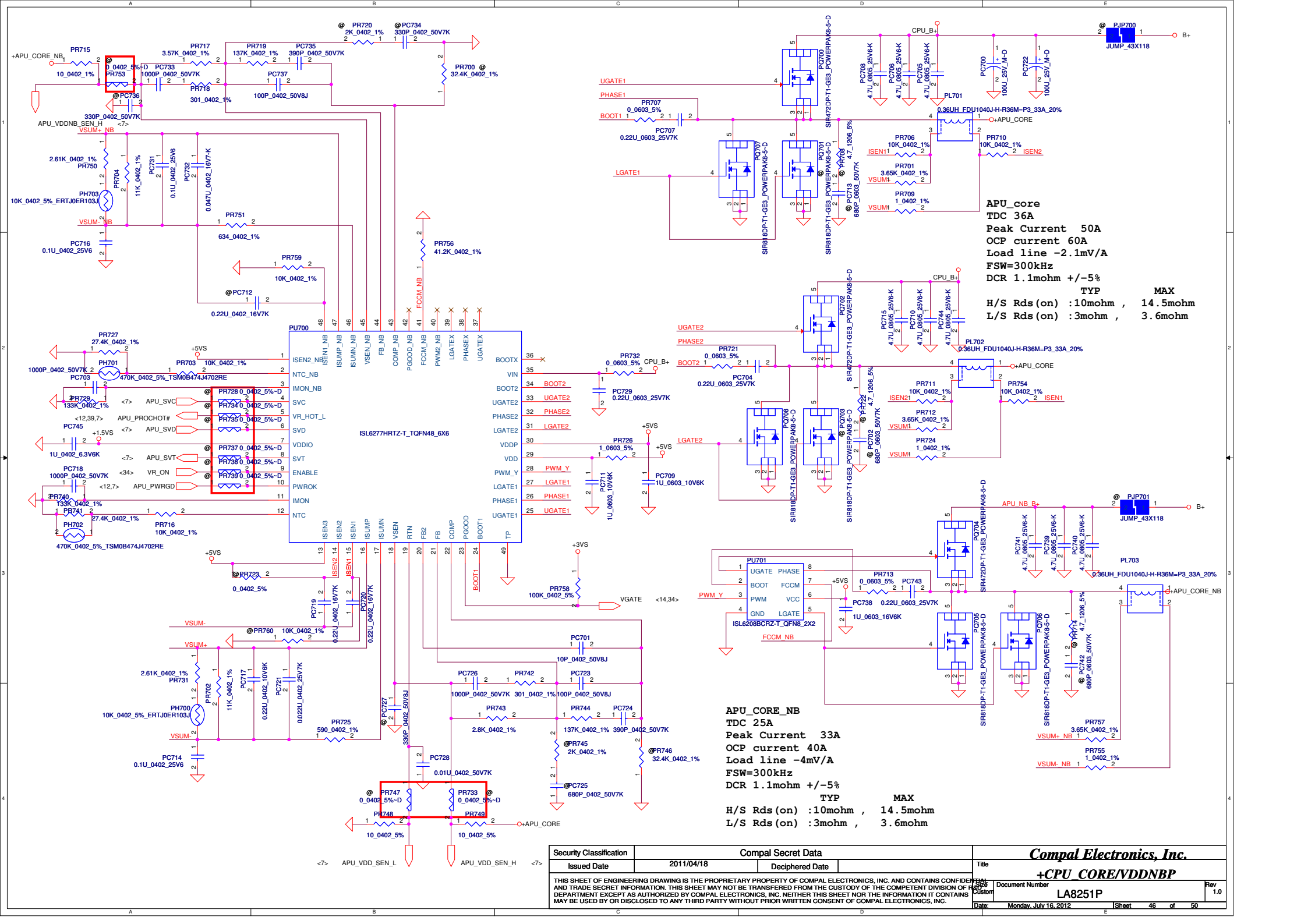
Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Compal Electronics, Inc.

Title: +VDDCIP

Size | Document Number: LA-8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 45 of 50


PU700
ISL6277HRTZ-T_TQFN48_6X6
PU701
ISL6208BCRZ-T_QFN8_2X2
APU_core
TDC 36A
Peak Current 50A
OCP current 60A
Load line -2.1mV/A
FSW=300kHz
DCR 1.1mohm +/-5%
TYP MAX
H/S Rds(on) :10mohm , 14.5mohm
L/S Rds(on) :3mohm , 3.6mohm
APU_CORE_NB
TDC 25A
Peak Current 33A
OCP current 40A
Load line -4mV/A
FSW=300kHz
DCR 1.1mohm +/-5%
TYP MAX
H/S Rds(on) :10mohm , 14.5mohm
L/S Rds(on) :3mohm , 3.6mohm
Security Classification
Compal Secret Data
Issued Date
2011/04/18
Deciphered Date
Compal Electronics, Inc.
Title
+CPU_CORE/VDDNBP
Size
Custom
Document Number
LA8251P
Rev
1.0
Date:
Monday, July 16, 2012
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50
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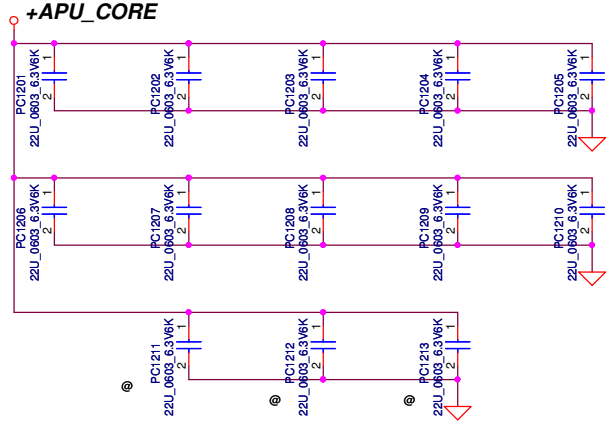
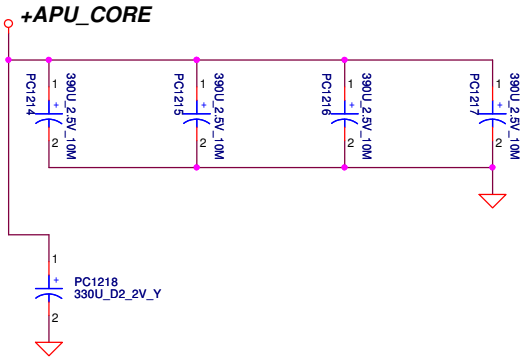
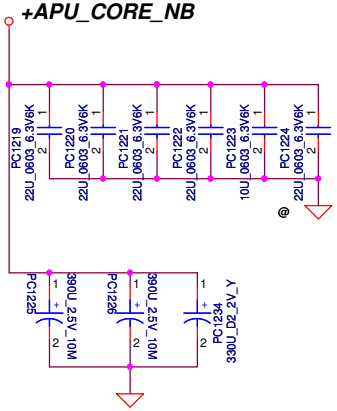
+APU_CORE

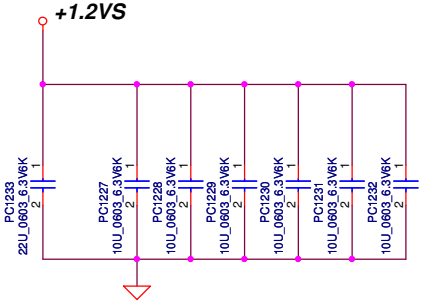




+APU_CORE_NB



+1.2VS



+1.2VS

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size	Document Number	Rev
Custom	LA8251P	1.0

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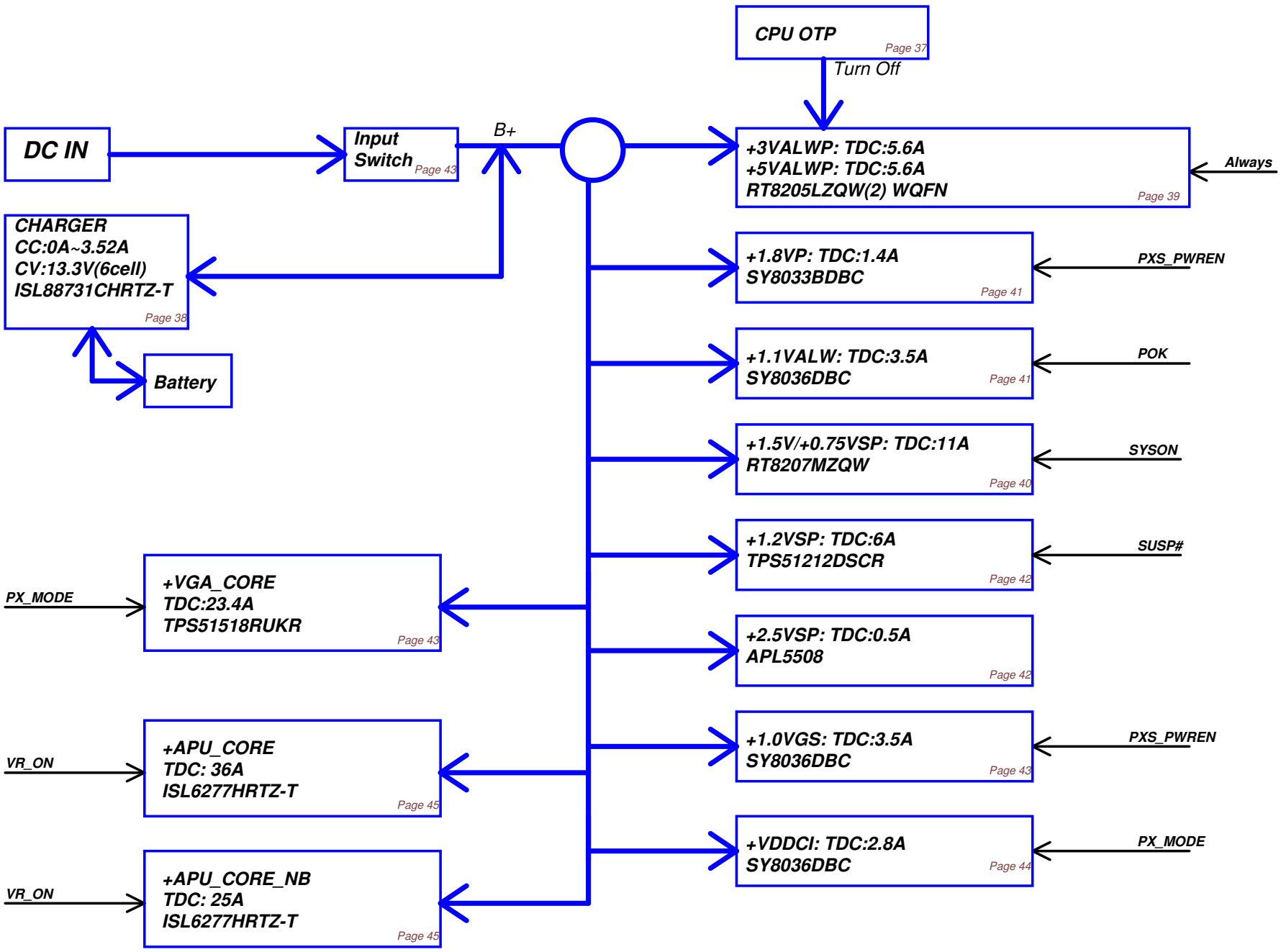
Power block



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/04/18	Deciphered Date	Title: PWR-POWER BLOCK DIAGRAM

Size: Custom	Document Number: LA8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 48 of 50		

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1							

Compal Electronics, Inc.

Title: PWR-PIR

Size: C Custom | Document Number: LA8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 49 of 50

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	9	XXX	XX'XX/XX	Compal_XX	XXXXX	Change PRXX from Xohm to XXKohm.	X01

Design Change

Date	Page	Part reference	change description	Reason
10/17/2011	33	JLED2	Add JLED2 for Inspiron use only.	ME change drawing.
10/17/2011	30	UD1	Swap nets FCH_SDATA0/FCH_SCLK0	correct connection
10/17/2011	25	UV27.1	ADD RV327 for HPD	Vendor review
10/17/2011	25	RV268	DEL RV268	No need 1.2V from system.
10/17/2011	14	D6.D7	Change D6. D7 to Schottky for VGA PWR control	Original Diode. Vf too high.
10/17/2011	12	C159.C158	Change C159.C158 to 10pF	Vendor review
10/17/2011	12	D5.D8	Change D5. D8 to Schottky	Original Diode. Vf too high. Vendor review.
10/17/2011	27	DV8	Reserve DV8. use RV40 short.	HDMI Voltage issue.
10/17/2011	26	JLVDS	JLVDS Reverse Pin	LVDS connector location change.
10/17/2011	21	RV215	RV215 connect to net:+VDDCI	FB_VDDCI Should connect to +VDDCI
10/17/2011	37	AMP	Add an Audio AMP Circuit in page37	customer requires.
10/19/2011	33	DB7	Reserve DB7 for ESD	ESD request
10/19/2011	36	RB21	Adding RB21. change USB charge circuit power rail to +VC	USB charge sequence fine tune
10/19/2011	34	U26	Dashboard button change to U26 pin34.36.75	to meet customer spec.
10/19/2011	13	U2	KB_DET# Change to FCH GPIO56. add Q76	EC pin saving.
10/20/2011	34	R503	R503 DEL	Leakage form 3VALW to VS
10/20/2011	30	QD4	Add QD4	Leakage form 3VALW to VS
10/21/2011	33	R793.R794.R795.R796.D24	add R793.R794.R795 100K*3.R796 0ohm.D24 BAT54C	For Dashboard support 3 second boot up.
10/21/2011	37	U6	Reserve U6. C244~C251. R797~R799	Reserve GreenCLK
10/21/2011	31	JBTB1	change pin67 to +3VS. pin36.38.40.42 to +3VALW	LAN D/B design changes.
10/21/2011	27.32	JUSB2.JHDMI	update JUSB2 Footprint. JHDMI Footprint	ME change drawing.
10/25/2011	29	CA19.CA20	From 2.2UF to 4.7UF	Vendor review
10/25/2011	28	CV6.CV7.CV8	From 22pF to 10pF	CRT high resolution issue.
10/26/2011	33	R60.R8	Change to 300ohm	LED current need >5mA
10/26/2011	33	R792	Add 100Kohm to GND	Power LED issue.
10/26/2011	33	UX1	SYSON connect to UX1.20	Express Card not support S5 weakup.
10/28/2011	29	RA12.RA13	Change from 5.1ohm to 39.2ohm	Vendor review
11/21/2011	33	UX1	Connect pin4 to +3VS. pin14 to +1.5VS for 2nd GMT	2nd source required.
11/28/2011	7	Q6	Add Q6, Del Q1	ProcHot# change to High active. Common code for EC
11/28/2011	12	R109	10M reserved	Without RTC battery, system should not boot up issue
11/28/2011	36	EMI	Add C254,C255,C256,C257,C258,C259 0.1uF +1.5V	For EMI request
11/28/2011	32	UB4	AMD USB debug Port0 change to JUSB1	JUSB1 USB SI too margin. Due to switch serial resistor approx 10ohm

Design Change for PT

Date	Page	Part reference	change description	Reason
04/03/12	18	YV1	27MHz package change to small size	Sourcer's recommend for cost down
04/03/12	26	JLVDS	pin assignment change for 31,32,33,34,35,37	Sourcer's recommend for cost down
04/03/12	35	C657	add 0.1u_0402 on USB_DETECT#	ESD required
04/03/12	35	C658	add 0.1u_0402 on USB_DET#_DELAY	ESD required
04/03/12	18	RV205,RV206	add 10K_0402 reserved only.	AMD Chelsea required
04/03/12	18	R804,R805	add 0_0402 reserved only.	AMD Chelsea required
04/03/12	20	RV244,CV366,RV208	add 2K_0402 ,10P_0402, 0_0402, reserved	AMD Chelsea required
04/03/12	21	RV247,RV248	add 0_0402 reserved, RV247 stuffed.	AMD Chelsea required
04/03/12	18	RV250	add 0_0402 to GND for Thames, stuffed.	AMD Chelsea required
04/03/12	28	JCRT	footprint changed	DFB required
04/03/12	30	JHDD	footprint changed	DFB required
04/03/12	12	C158,C159,Y1	18p,18p,small size, 10P→18P	Sourcer's recommend for cost down
04/03/12	12	C155,C157,X1	12p,12p,small size, 27P→12P	Sourcer's recommend for cost down
04/12/12	19	RV104,RV101,QV21,CV96,RV103,RV109,QV25,RV99,RV100,QV18,QV19,QV20	Remove from BOM	These parts are PX4.0 supports. We support PX5.0 only.
04/12/12	19	RV112,RV113	RV113 Change 150K→240K, RV112 change 20K→240K.	Power rail +1.5VGS Timing fine tune.
04/12/12	18	R807,R806	Reserve 0ohm, R807 stuffed.	Reserve adaptor choice for dGPU GPIO5(net:AC_BATT)
04/12/12	29	R14, Q78	R14 10K, Q78 NMOS dual.	AMD recommend.
04/12/12	32	LB6, RB17, RB19	LB6 add to BOM.	EMI required.
04/12/12	13	R136	100K ohm stuffed.	Add PU for FCH GPIO171. (net:ODD_EN#)
04/12/12	14	R104	Reserve 0ohm.	Reserve for ODD_DA#
04/12/12	33	C260, C261, C262, C263	0.1uF stuffed.	ESD required
04/10/12	8	C100	Change to SGA00002280	ME Height limit. 4mm.
04/11/12	27	CV365,CV367	add 0.1U_0402_10V7K~D, reserve only.	EMI required, add caps in HDMI DDC
04/12/12	33	L3	add DLW21SN900SQ2_0805~D, reserve only.	EMI required, add CC in Cardreader
05/02/12	7	C71	pop 0.1U_0402_16V4Z	EE required, Shutdown issue, Leason learn from CGs

Design Change for ST

Date	Page	Part reference	change description	Reason
05/31/12	26,33,31	RV328,R808,R774	add 300_0402_5%~D	AMD required, USB20 D- add RC for device lose
05/31/12	26,33,31	CV368,C155,C795	add 15P_0402_50V8J~D	AMD required, USB20 D- add RC for device lose
05/31/12	18,28	RV220,RV223,RV217,RV226,RV222,RV225,RV221,RV224,RV216,RV227,RV218,RV228,RV219,RV229	delete CRT debug	AMD required, for VGA layout concern.
05/31/12	7	Q6	reverse Q6	EE required
05/31/12	27	RV329,RV330	add 0_0603_5%~D	EMI required, DDC EMI issue.
05/31/12	27	D20	add PESD24VS2UT_SOT23-3~D, reserve only.	ESD required, HDMI plug issue, Leason learn from CGs
06/22/12	18	R806	pop R806 0ohm	Fast Power reduce function
06/23/12	27	RV39, RV41, RV42, RV44, RV53, RV54, RV57, RV58	Remove these part	change to common mode chock
06/24/12	27	LV4, LV5, LV6,LV7	add these KINGCORE WCM-2012HS-900T common mode chock	EMI required for HDMI noise
06/25/12	27	CV351, CV352, CV349, CV350, CV353, CV354, CV355, CV356	add these 3.3pF 50V 0402	EMI required for HDMI noise
06/26/12	27	CV364, CV363, CV360, CV361, CV358, CV357, CV362, CV359	add these 1pF 50V 0402	EMI required for HDMI noise
06/22/12	32	DB4	Remove	USB detect issue