

MODEL NAME : VBW01
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WL000 LA-9982P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

Dell / Compal Confidential

Schematic Document

Intel Shark Bay ULT
OAK Mainstream2
UMA/DIS AMD Venus Pro

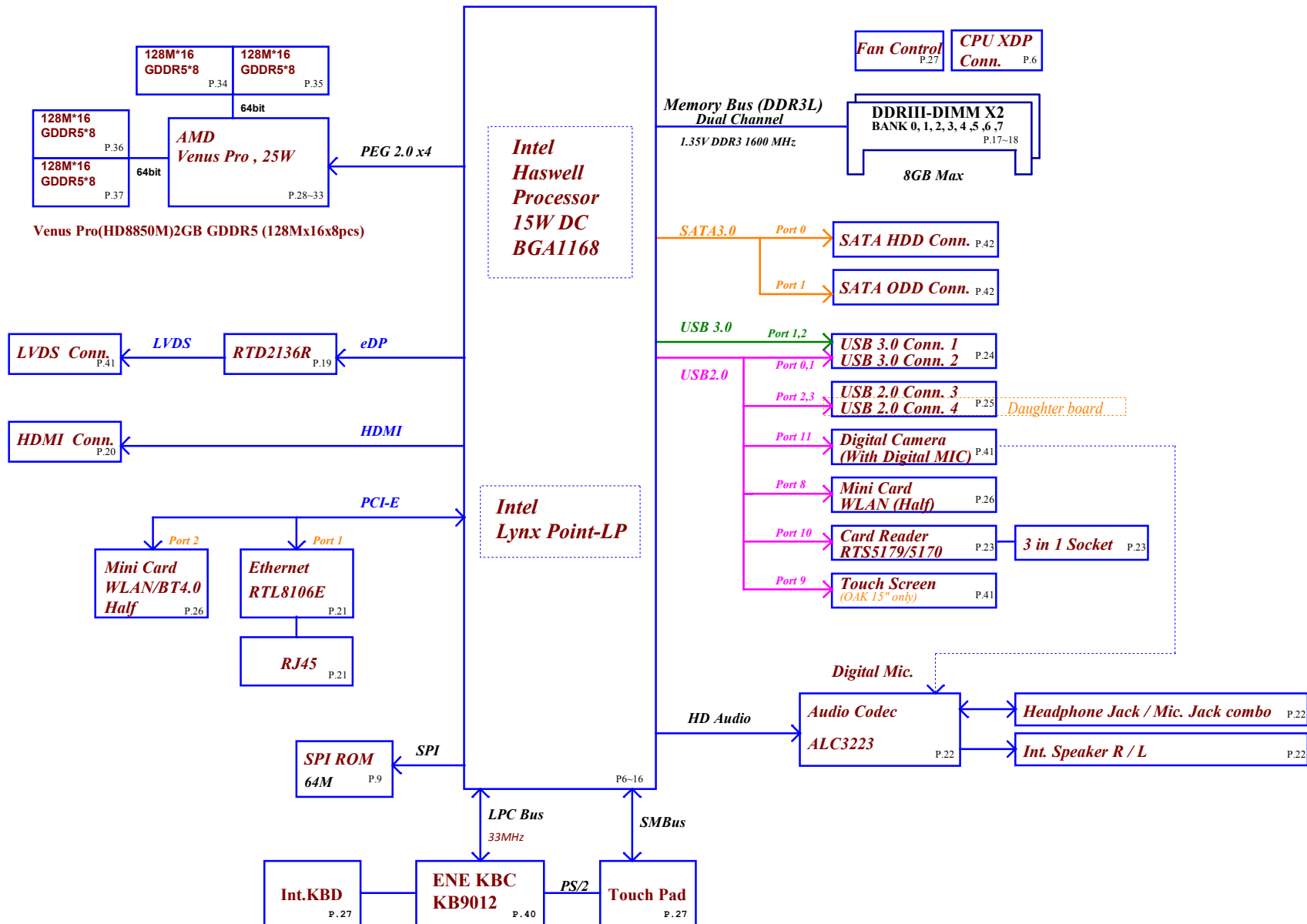
2013-05-29 Rev: 3.0

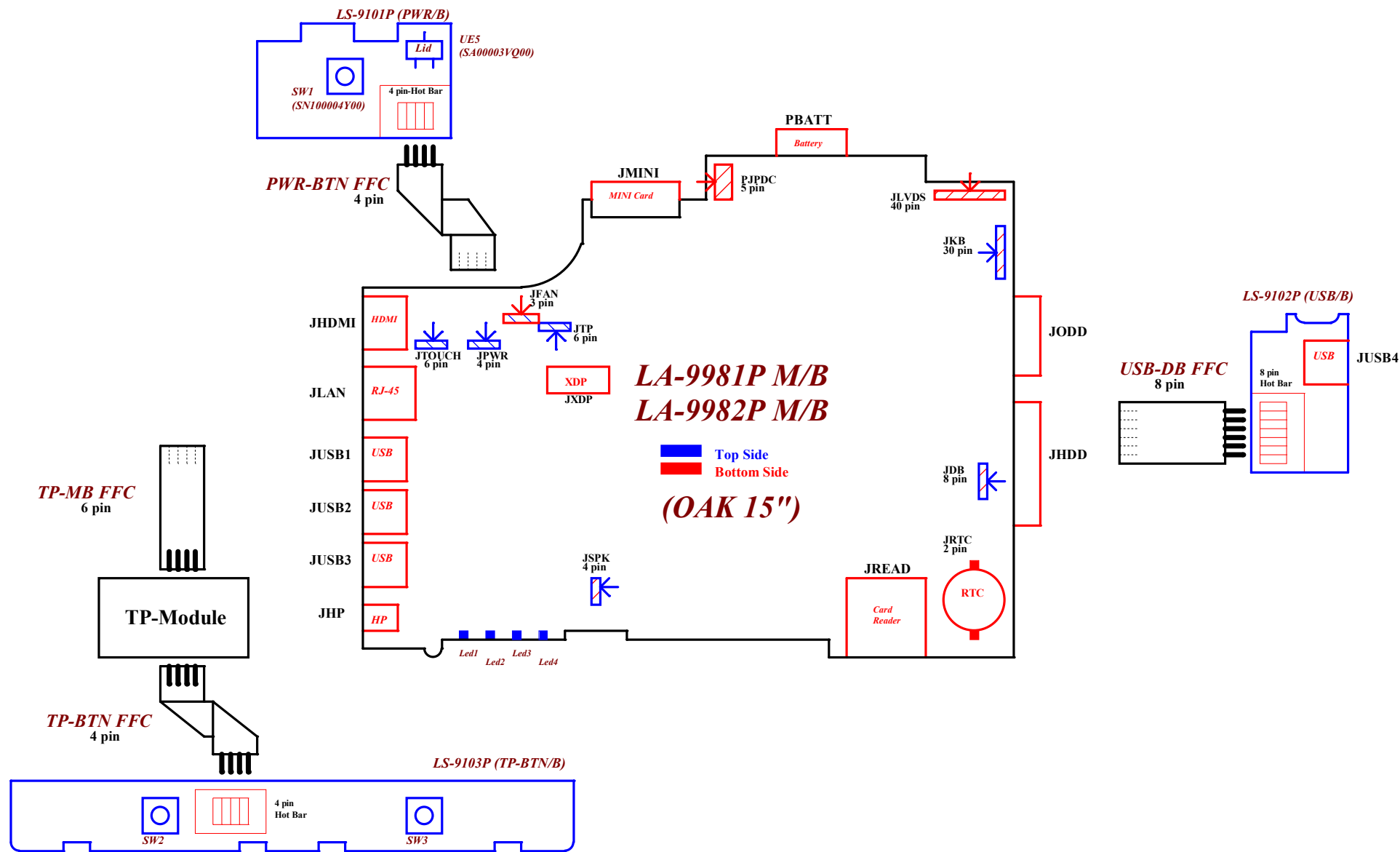
X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
VENUS@ : VENUS Pro,VENUS XT
VENUSXT@ : VENUS XT
VENUSPRO@ : VENUS Pro
@VENUS@ : VENUS nopop component
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts

BOM config
UMA : UMA@,EMI@,ESD@,RF@
DIS VENUS : VENUS@,VENUSPRO@,DIS@,EMI@,ESD@,RF

ZZZ R1@
PCB VBW01 LA9982P/LS9101P/LS9102P/LS9103P
DA20ZG00120

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				Date: Wednesday, May 29, 2013	Rev 3.0
				Sheet 1 of 57	





Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

Link

Board ID TABLE

ID	PCB Revision			
	UMA	Sun XT	VenusPro	VenusXT
0	SSI&A02			
1		SSI&A02		
2			SSI&A02	
3				SSI&A02
4	PT			
5		PT		
6			PT	
7				PT
8	ST			
9		ST		
10			ST	
11				ST
12	XB			
13		XB		
14			XB	
15				XB
16	A01			
17		A01		
18			A01	
19				A01

Symbol Note :



: means Digital Ground



: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

ULT

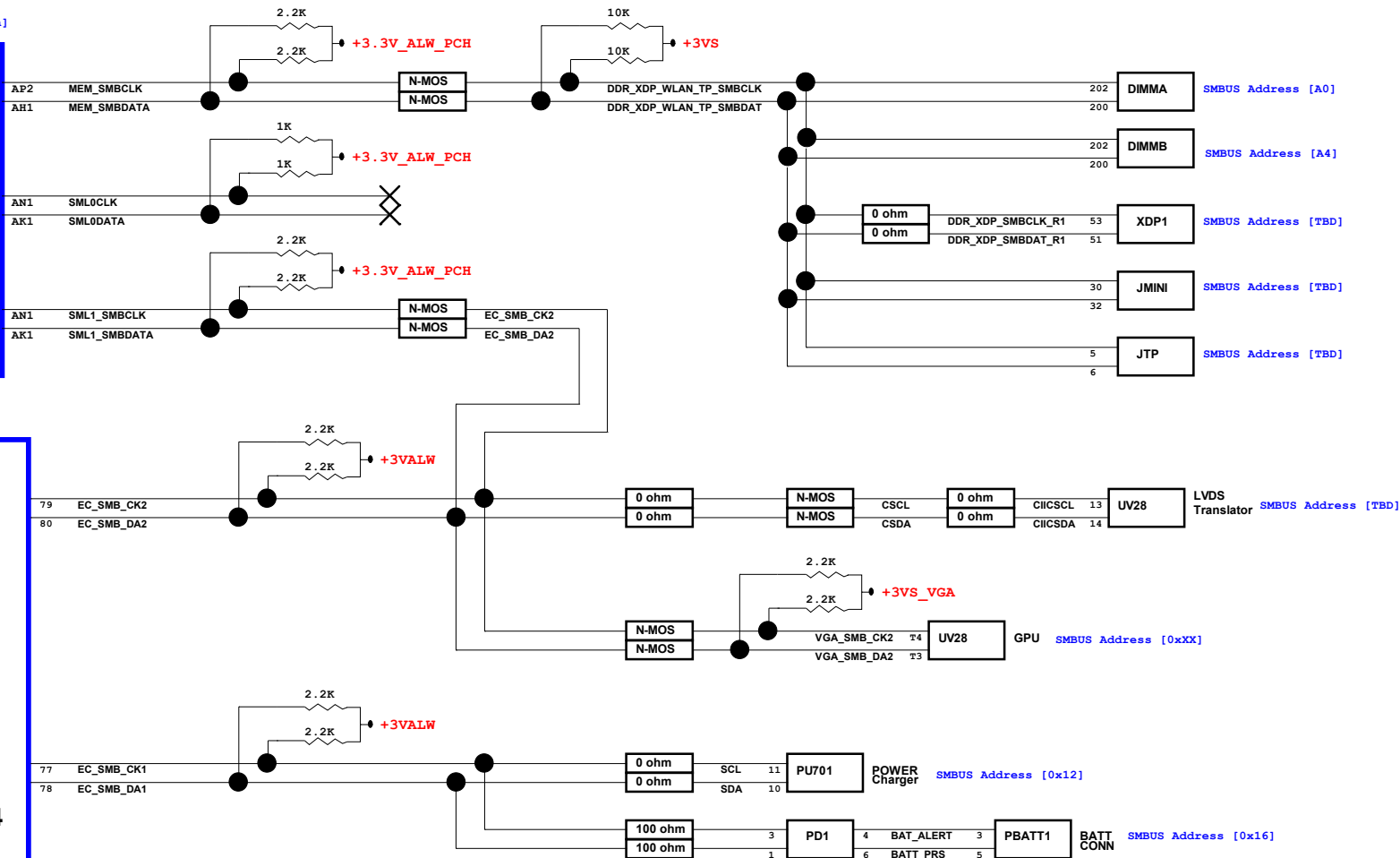
USB3.0	
Port1	USB connector 2
Port2	USB connector 1
Port3	
Port4	
USB2.0	
Port0	USB connector 2
Port1	USB connector 1
Port2	USB connector 3
Port3	USB connector 4 (DB)
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (N14P)
Lane 6	PEG (N14P)
SATA	
SATA0	HDD
SATA1	ODD
SATA2	
SATA3	

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				Sheet	4 of 57

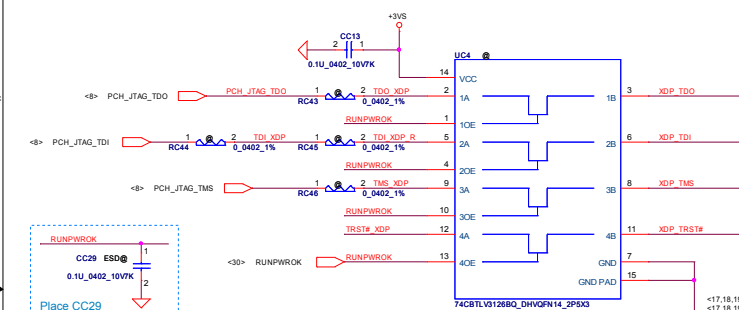
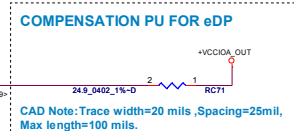
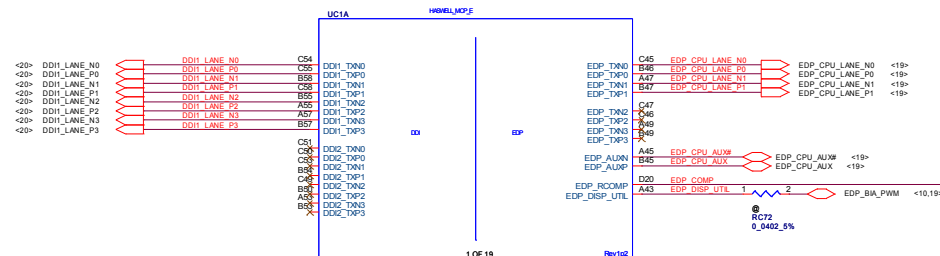
SMBUS Address [0x9a]

MCH
Shark bay

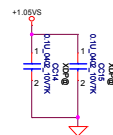
KBC
KB9012A4



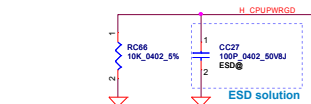
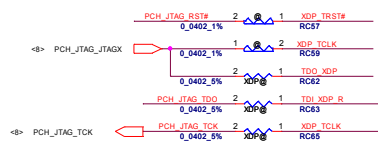
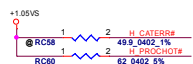
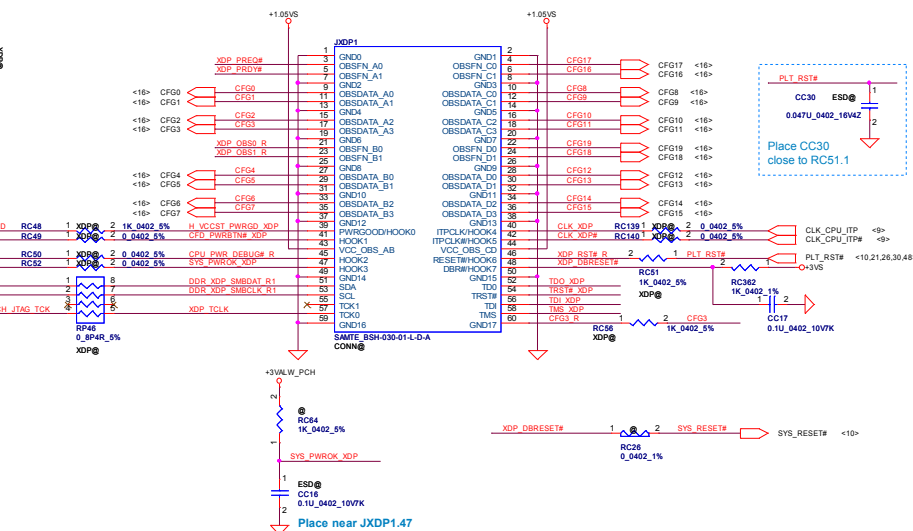
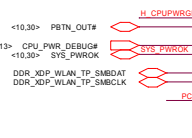
UC1 4010UI3G2R1Ⓢ CL8064701478202 SR16Q C1 1.7G BGA SA00006SX1L	UC1 4010UI3G2R3Ⓢ CL8064701478202 SR16Q C1 1.7G A315 SA00006SX2L
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reference Shark Bay ULT Validation Customer Debug Port
Implementation Requirement Rev 1.0



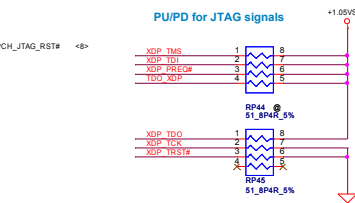
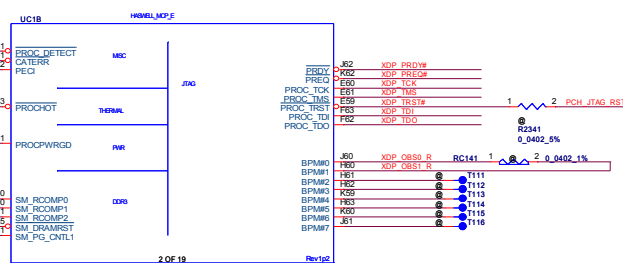
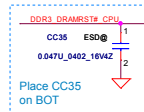
Place near JXDP1



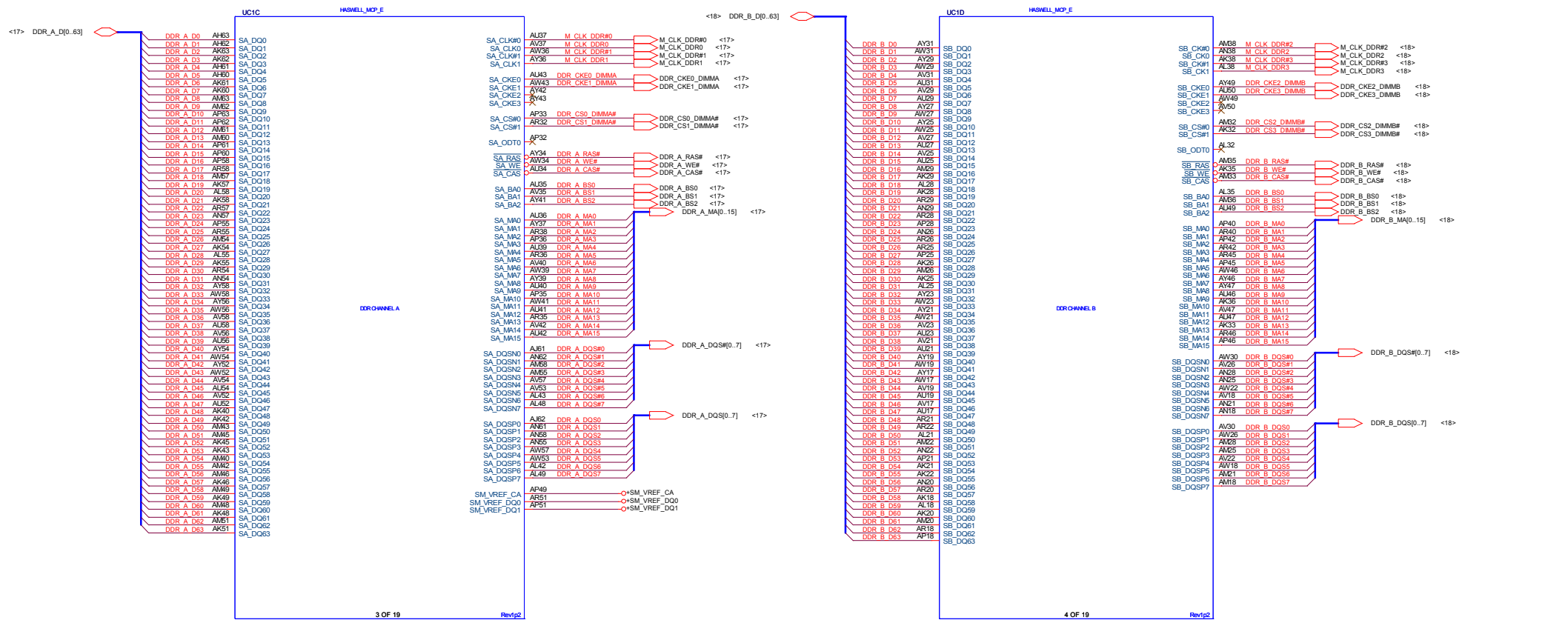
CAD Note:
Avoid stub in the PWRGD path while placing resistors RC115

200_0402_1% 2 1 RC68 SM RCOMP0

CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Min. to max. length=500 mil

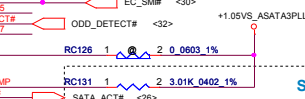
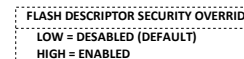
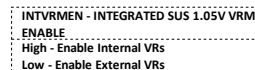
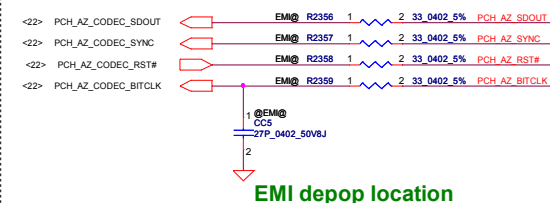
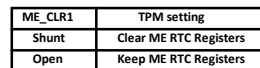


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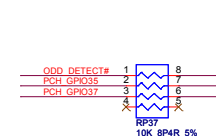


confirm by intel request PDG P141

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				Date	Wednesday, May 29, 2013
				Sheet	7 of 57

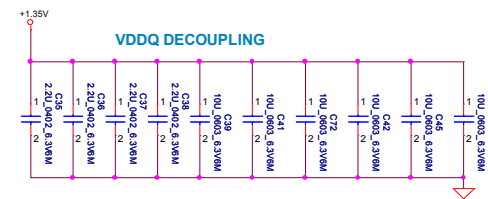
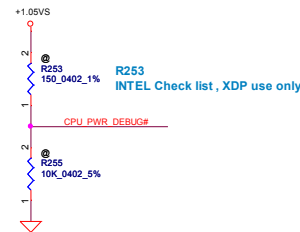
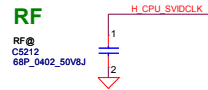
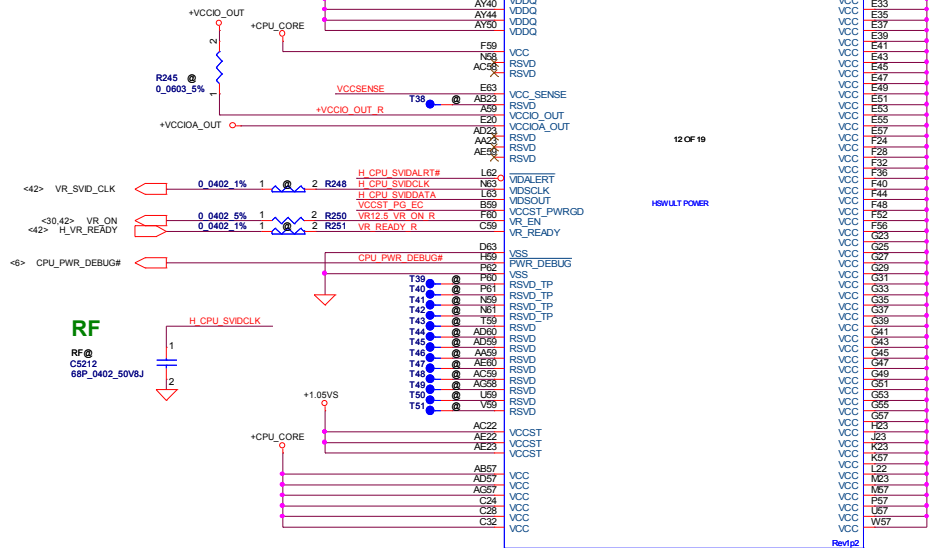
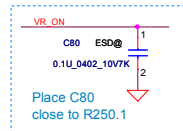
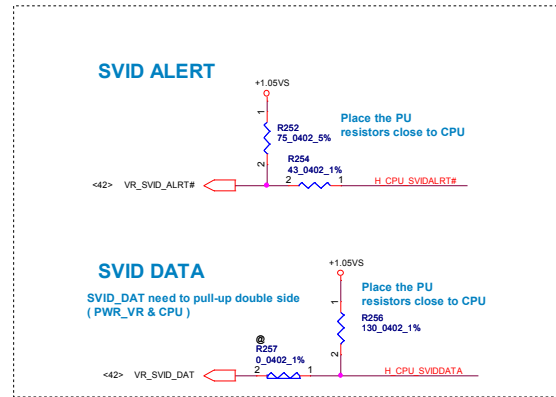
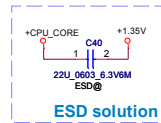
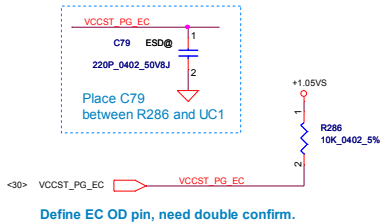


CAD note:
Place the resistor within 500 mils of the PCH. Avoid
routing next to clock pins.
reference FFRD sch 0.5



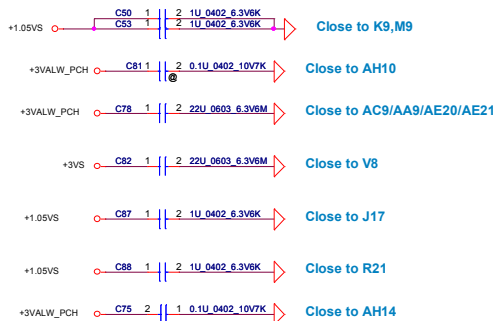
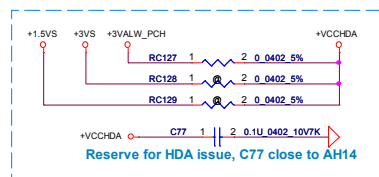
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					LA-9982P		3.0
					Date	Wednesday May 29, 2013	Sheet

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Date:				Wednesday, May 29, 2013	Sheet 10 of 57

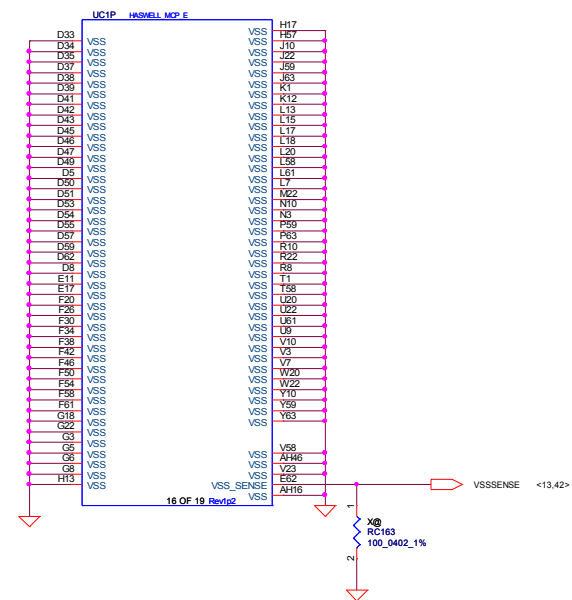
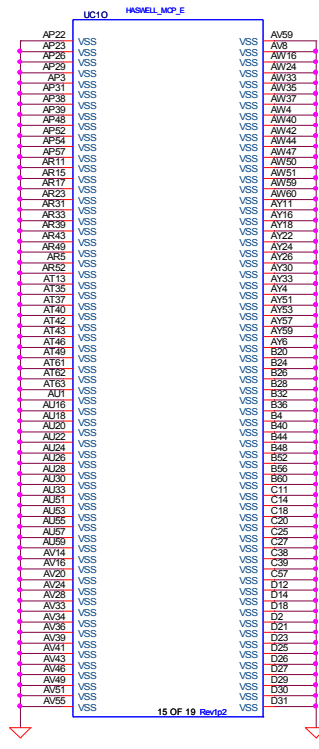
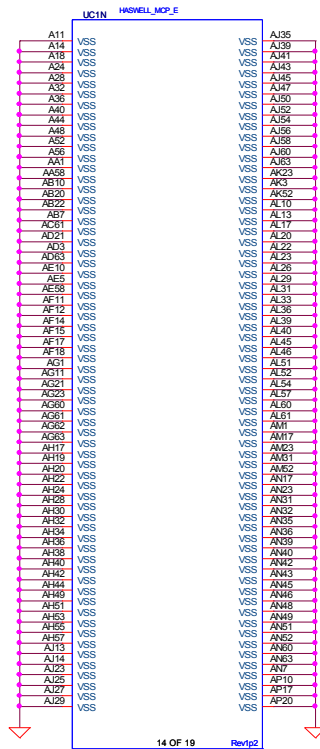


+1.35V : 470UF/2V/7343 *2 (PWR)
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

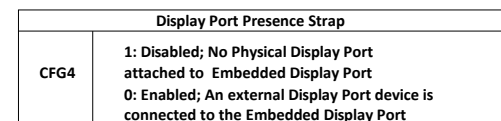
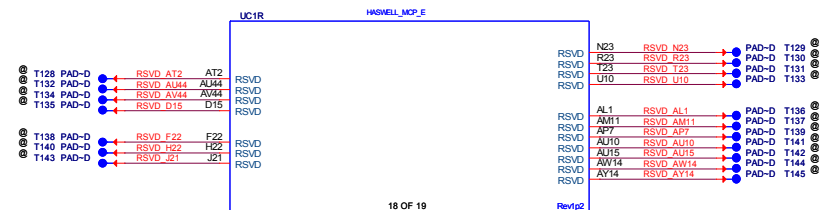
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				Date	Wednesday, May 29, 2013
				Sheet	13 of 57
				Rev	3.0



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				Date	Wednesday, May 29, 2013
				Sheet	15 of 57
				Rev	3.0



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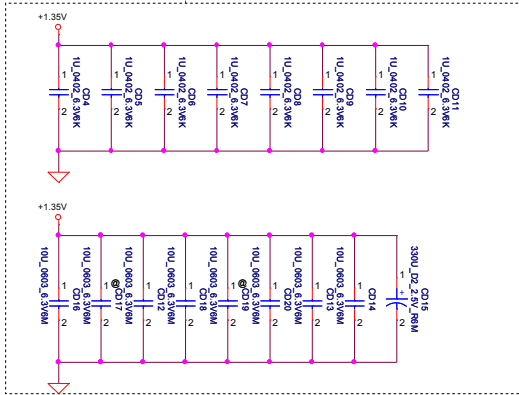
Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

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<7> DDR_A_DQ[0..63]
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<7> DDR_A_MA[0..15]

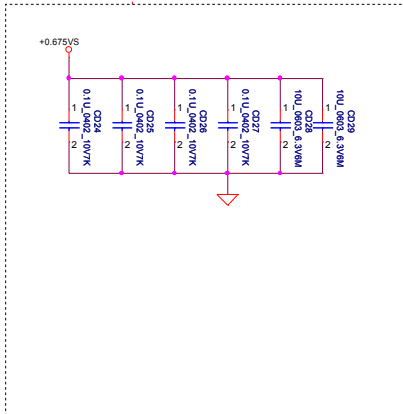
All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

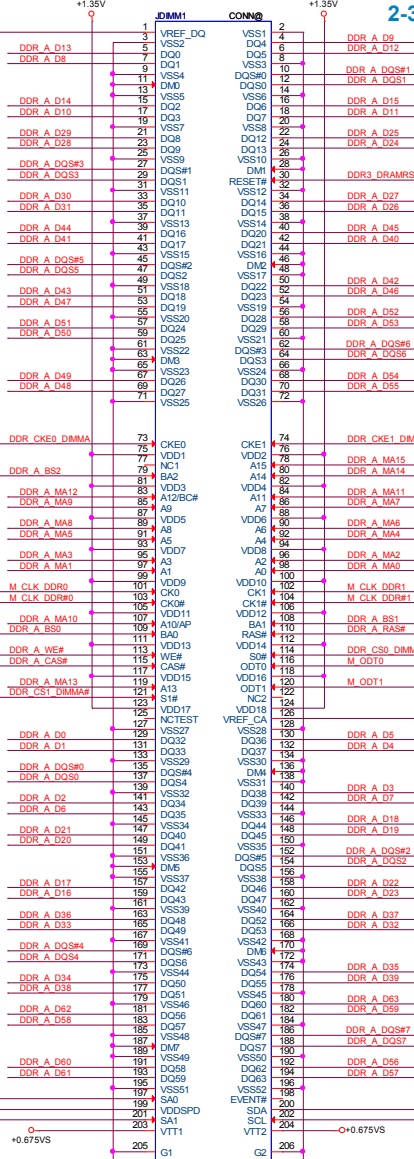


Layout Note:
Place near JDIMM1.203,204

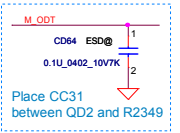
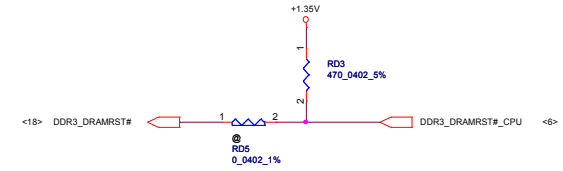


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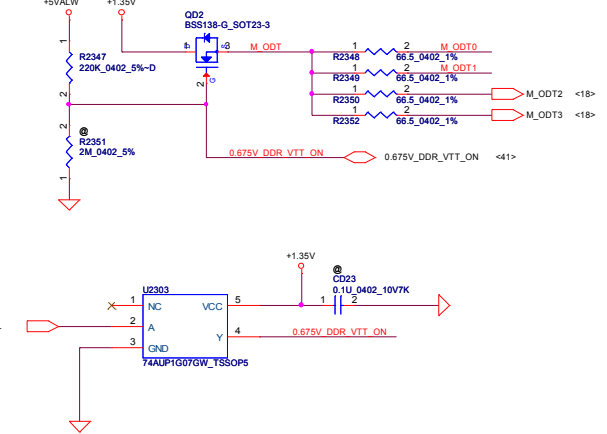
2-3A to 1 DIMMs/channel



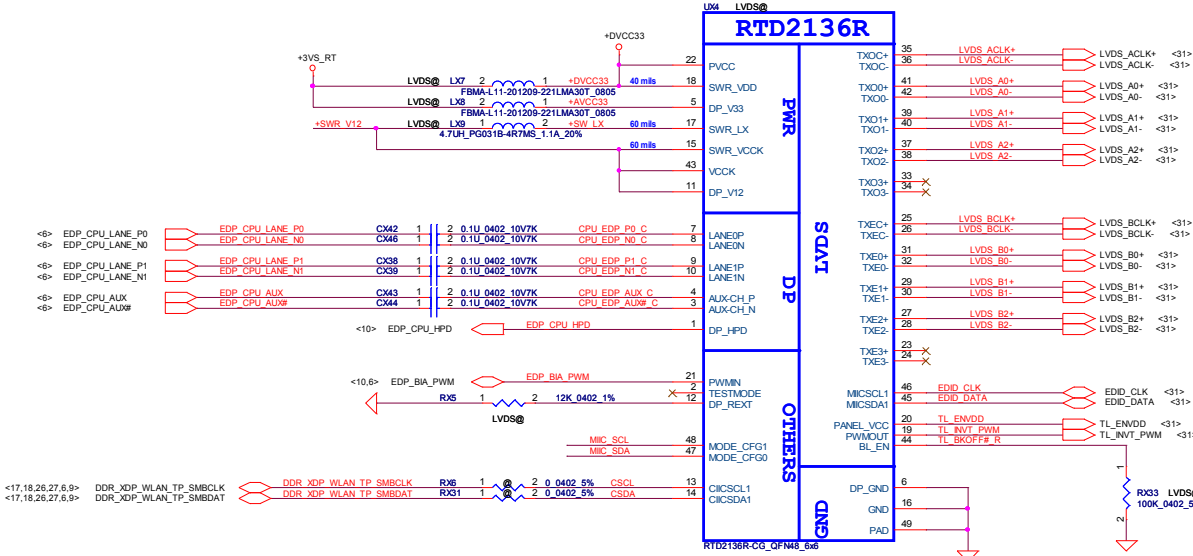
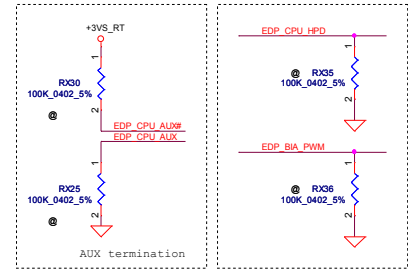
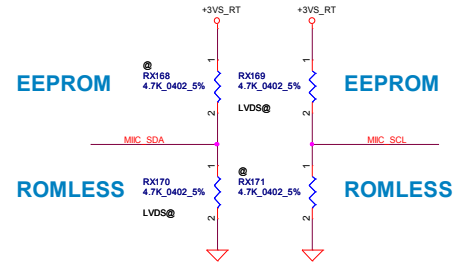
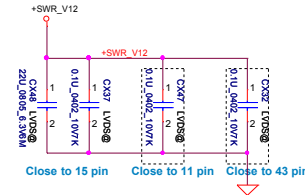
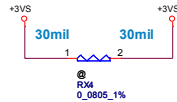
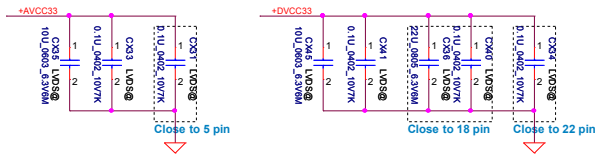
CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN



DDR3L SODIMM ODT GENERATION

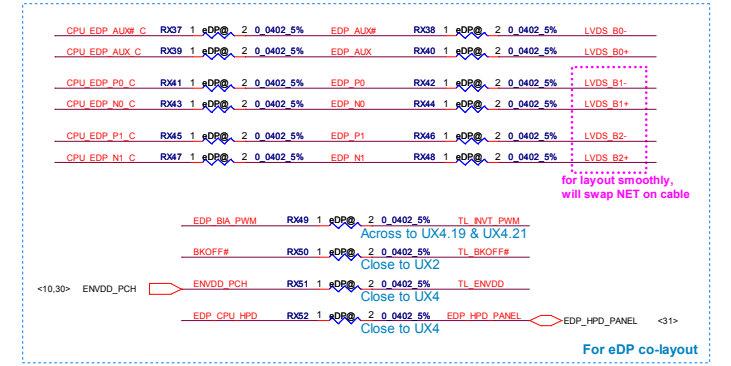
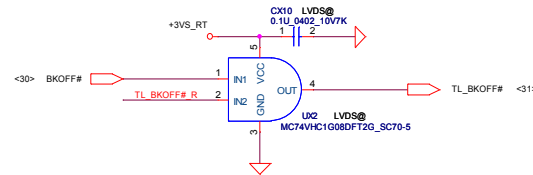


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				LA-9982P	Rev 3.0
				Date:	Wednesday, May 29, 2013
				Sheet	17 of 57

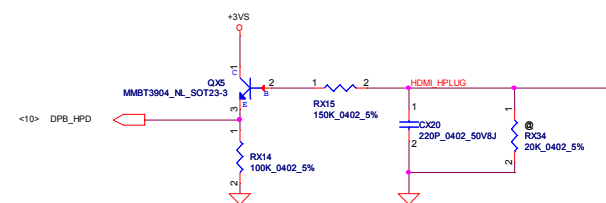
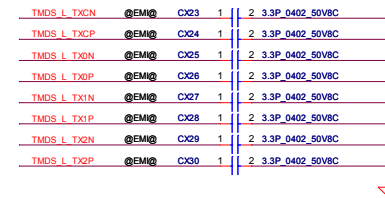
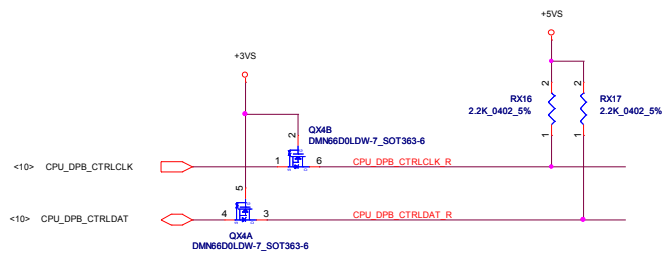
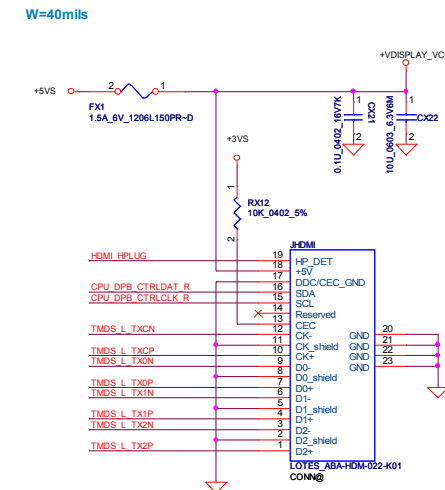
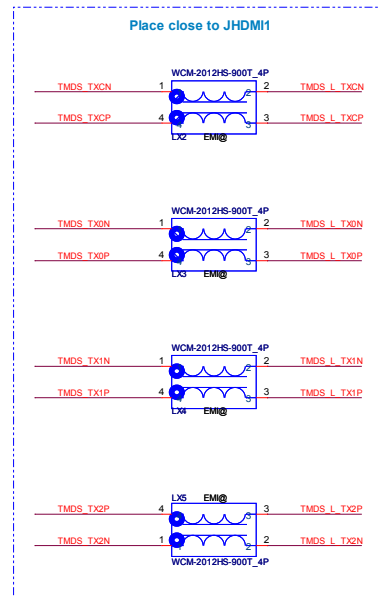
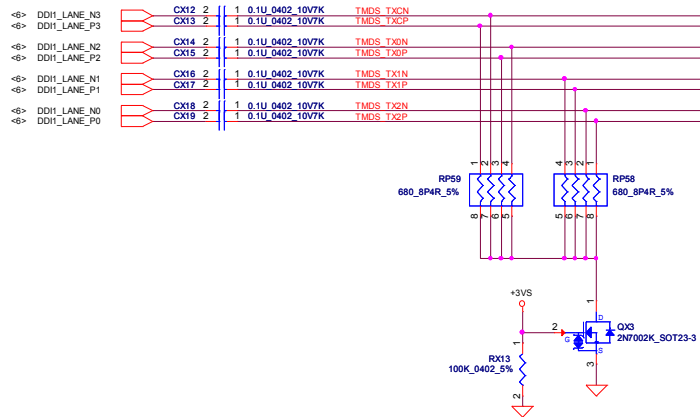


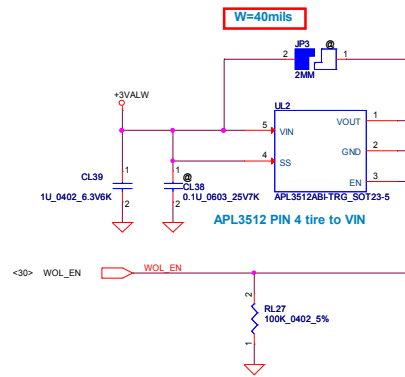
RTD2136S : SA00004NW10
RTD2136R : SA000067100

Vendor advise reserve it



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				Size	Document Number
				LA-9982P	
				Date	Wednesday, May 29, 2013
				Sheet	19 of 57

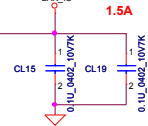




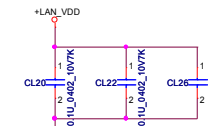
SS table

Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

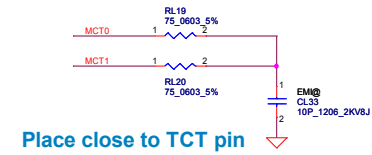
W=40mils +LAN_IO rising time : >1ms and <100ms



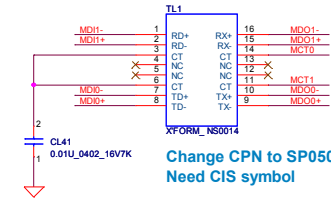
These caps close to Pin 23,32
For 8106E pop the capacitor close pin 23,32



These caps close to Pin 8,30
For 8106E pop capacitor close to pin 8,30

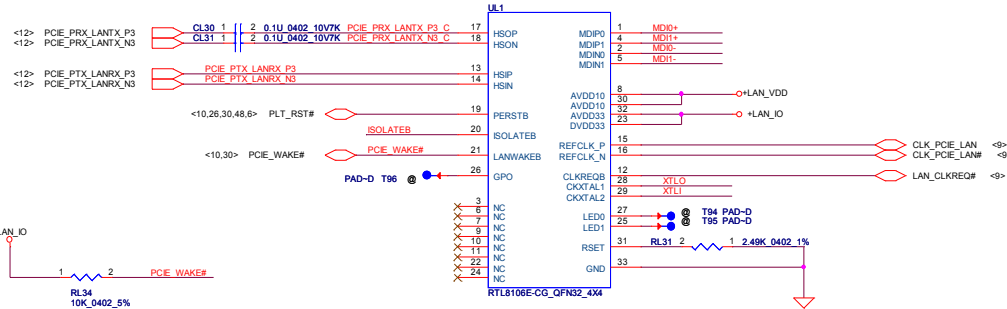


Place close to TCT pin

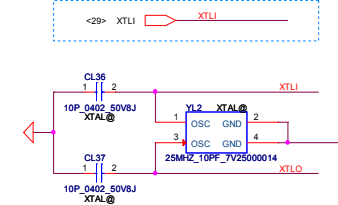


Change CPN to SP050007J00 only
Need CIS symbol

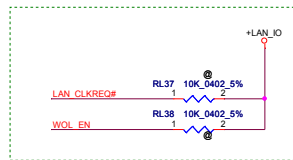
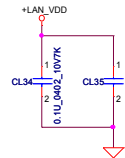
CL30, CL31 close to UL1 Pin 17, 18



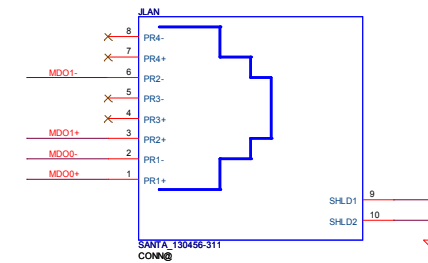
For GCLK



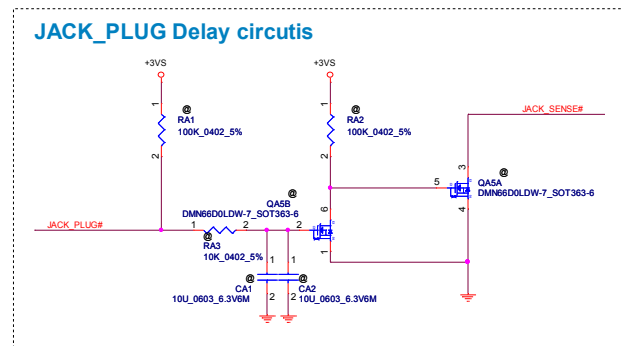
W=20mils



Reserve 10K pull LAN_IO



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Date:	Wednesday, May 29, 2013	Sheet	21	of 57



The diagram shows a 4-wire RTD bridge circuit. It consists of four resistors: RA29, RA30, RA31, and RA32. RA29 and RA30 are 0.0603 1% resistors. RA31 and RA32 are 0.0603 1% resistors. The bridge is connected to a GND and a GND+ source. The output is measured across the bridge.

LA1 EMI@

MIC_CLK C

1 2

BLM56B22 1SMD_2P

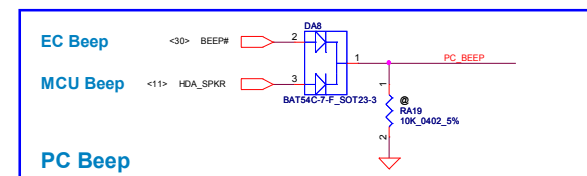
MIC_CLK

MIC_CLK <3>

SM01000BV00
need CIS symbol

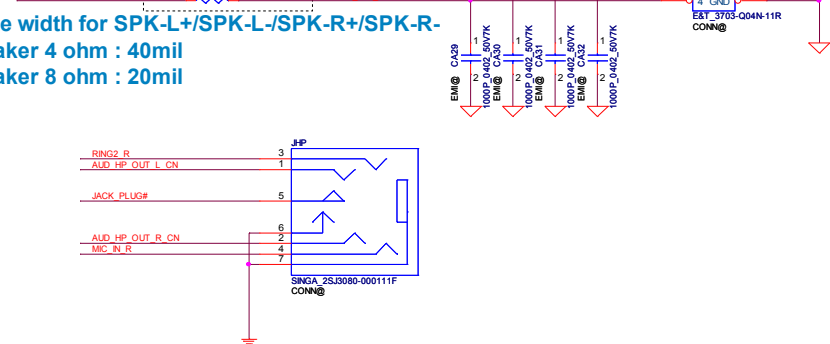
1 2

@EMI@
CA22
22P_0402_50V8J

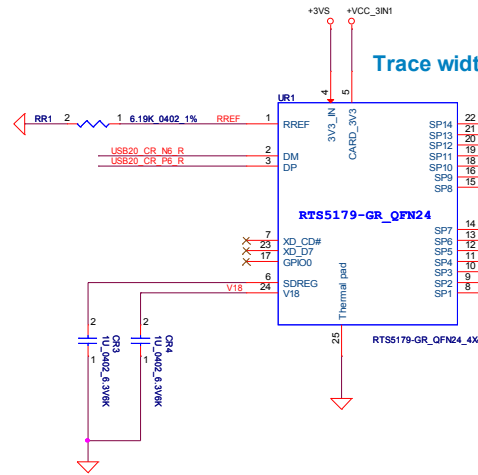
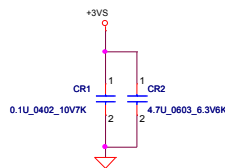
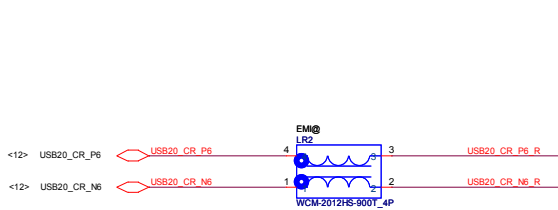


INT-SPK-R-	EMG	LA3	1	2	0	0603	5%	SPK R1- CONN
INT-SPK-R+	EMG	LA4	1	2	0 <td>0603 <td>5%</td> <td>SPK R2+ CONN</td> </td>	0603 <td>5%</td> <td>SPK R2+ CONN</td>	5%	SPK R2+ CONN
INT-SPK-L-	EMG	LA5	1	2	0 <td>0603 <td>5%</td> <td>SPK L1- CONN</td> </td>	0603 <td>5%</td> <td>SPK L1- CONN</td>	5%	SPK L1- CONN
INT-SPK-L+	EMG	LA6	1	2	0 <td>0603 <td>5%</td> <td>SPK L2+ CONN</td> </td>	0603 <td>5%</td> <td>SPK L2+ CONN</td>	5%	SPK L2+ CONN

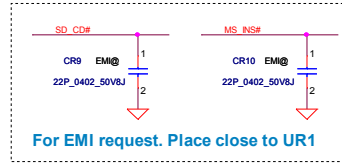
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil



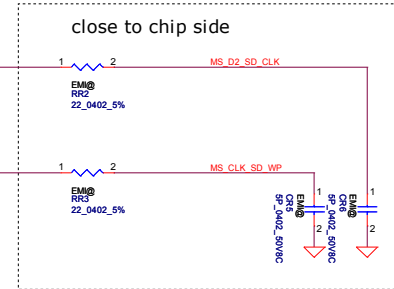
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						Audio Codec ALC3223						
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							Size	Document Number				Rev
							LA-9982P					3.0
Date:		Wednesday May 29 2013			Sheet	22 of 57						



Trace width:40mil



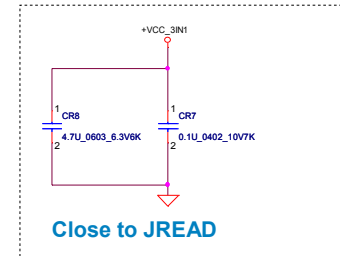
For EMI request. Place close to UR1



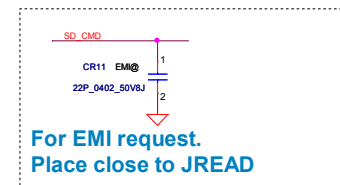
close to chip side

拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

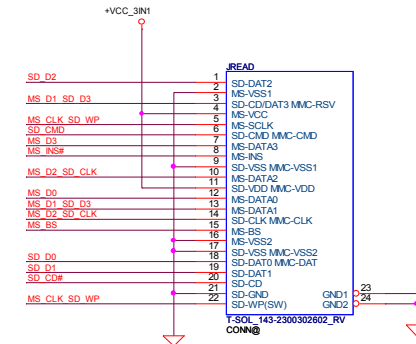
拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W



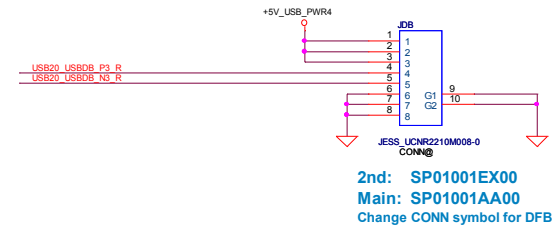
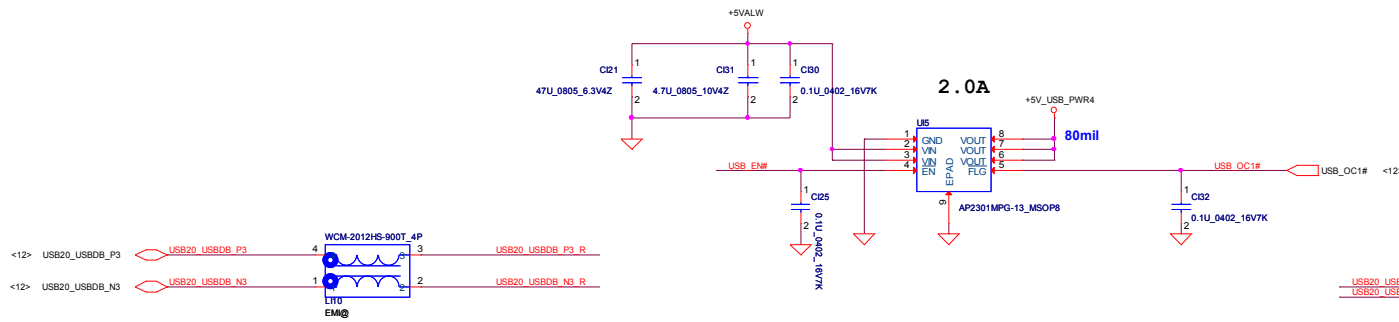
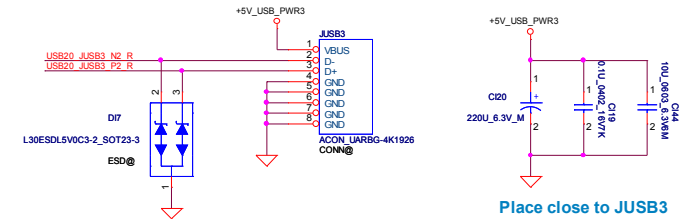
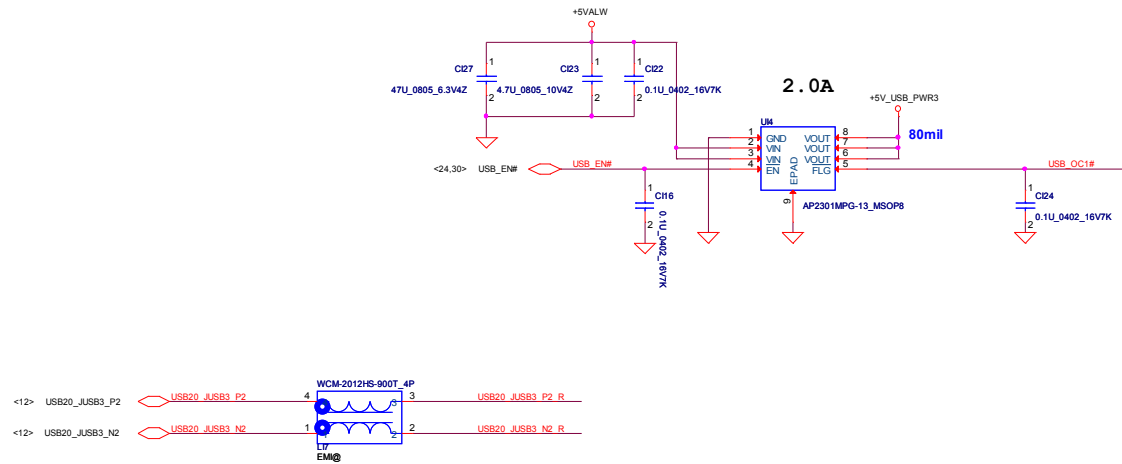
Close to JREAD



For EMI request.
Place close to JREAD

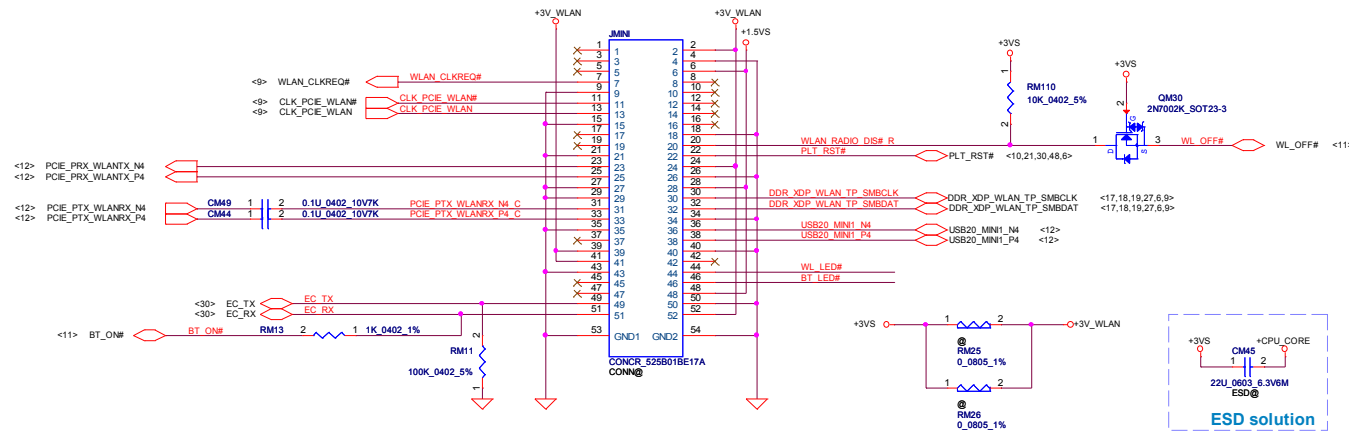


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				Date	Wednesday, May 29, 2013
				Sheet	23 of 57
				Rev	3.0

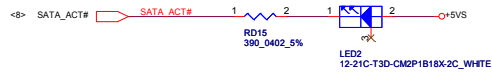


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				LA-9982P	Rev 3.0
				Date: Wednesday, May 29, 2013	Sheet 25 of 57

Mini WLAN/WIMAX H=6.7



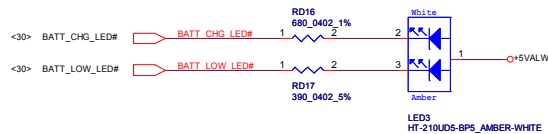
HDD LED



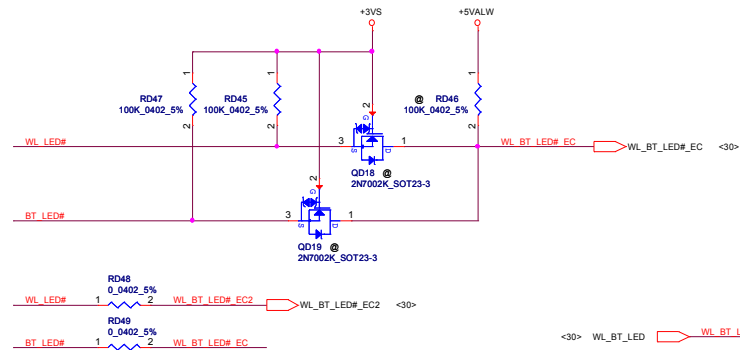
Power LED



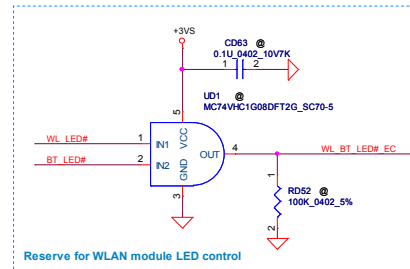
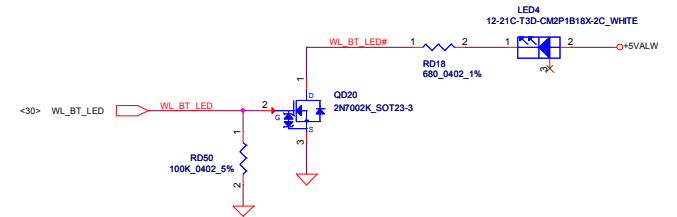
Battery LED



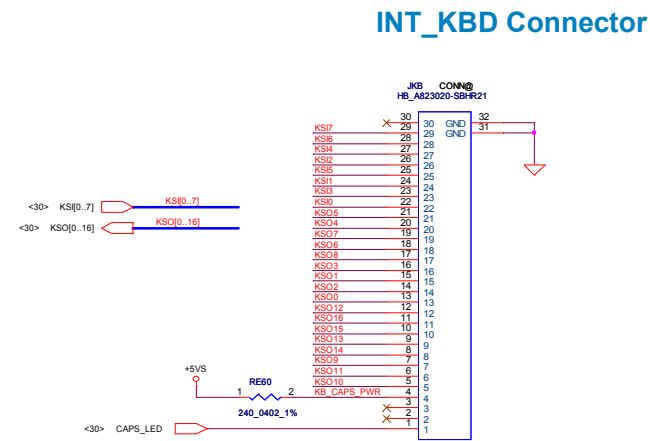
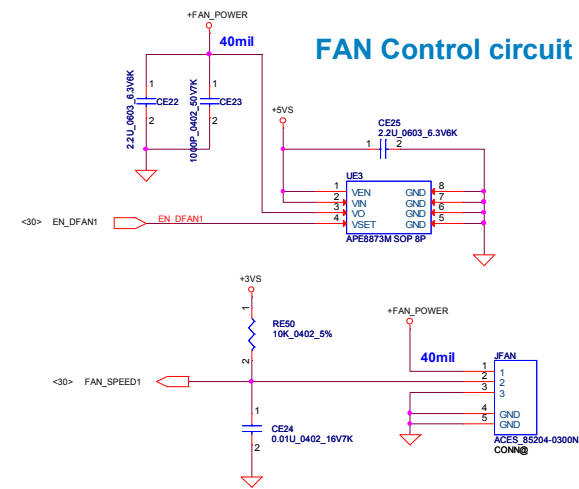
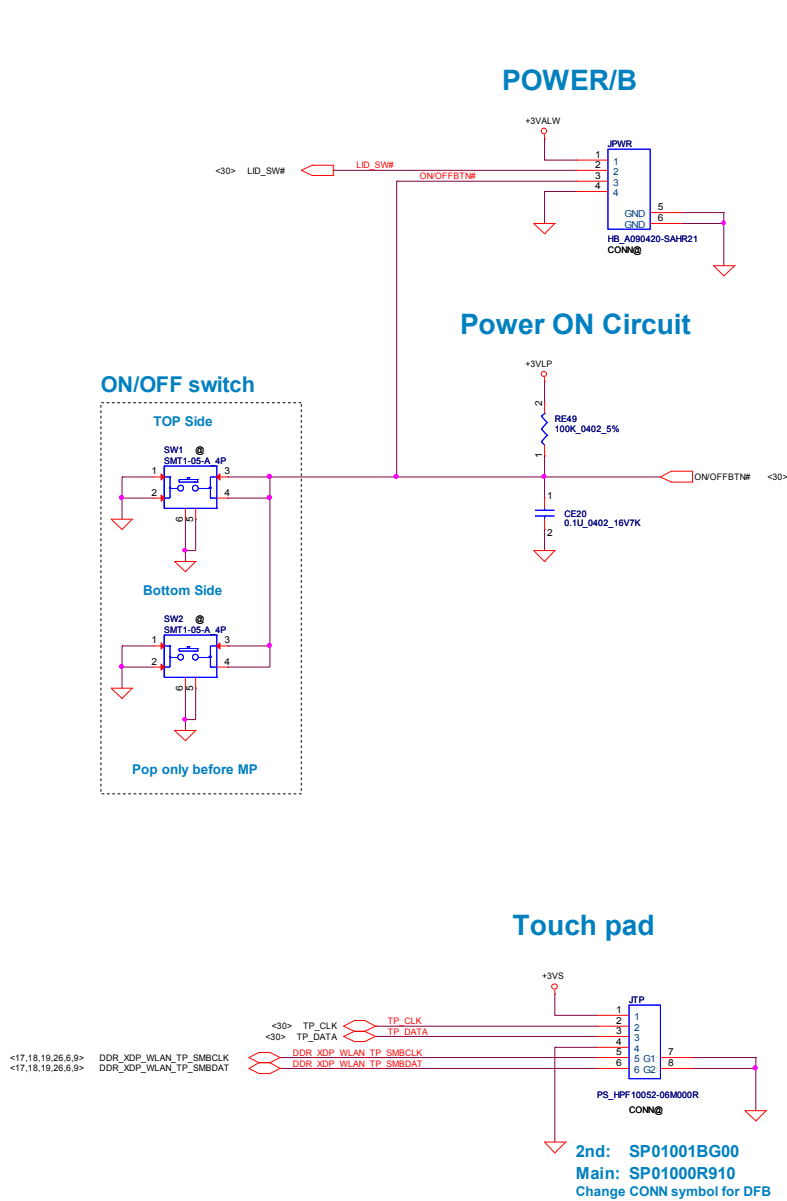
10mils, All pins



Wireless LED

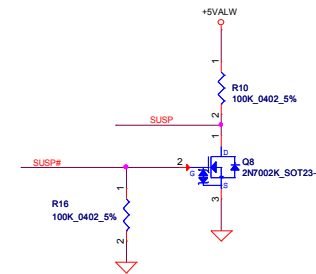
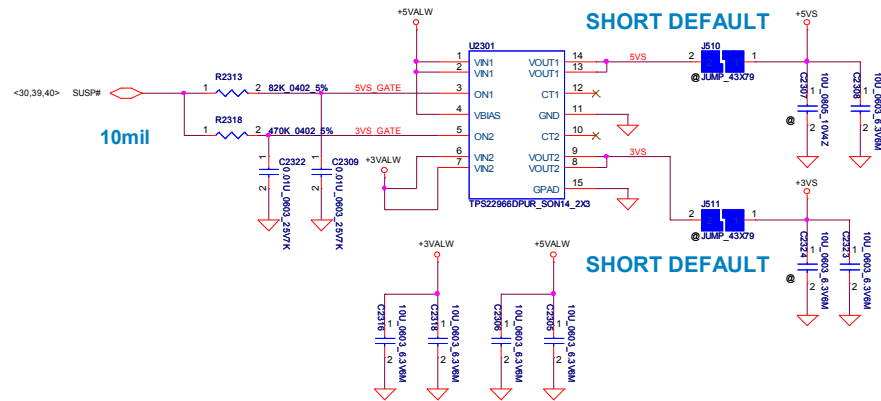


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				LA-9982P		
Date:				Wednesday, May 29, 2013	Sheet 26 of 57	

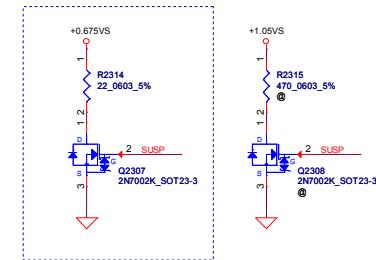
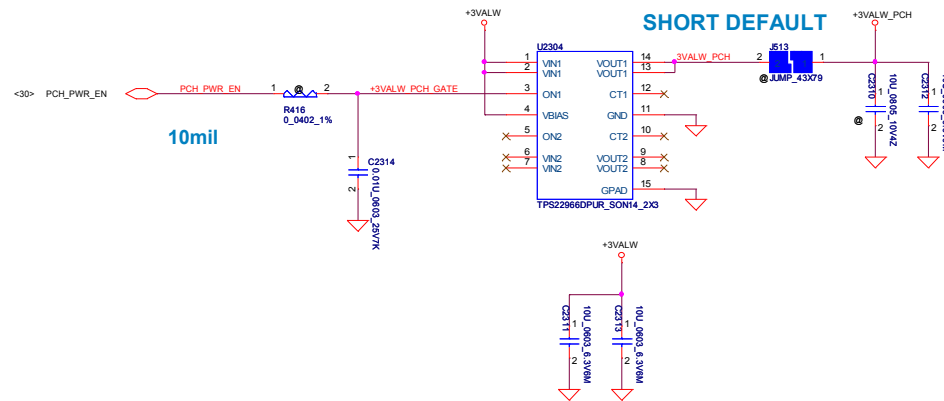


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					LA-9982P
				Date:	Wednesday, May 29, 2013
				Sheet	27 of 57
				Rev	3.0

+5VS and +3VS switch

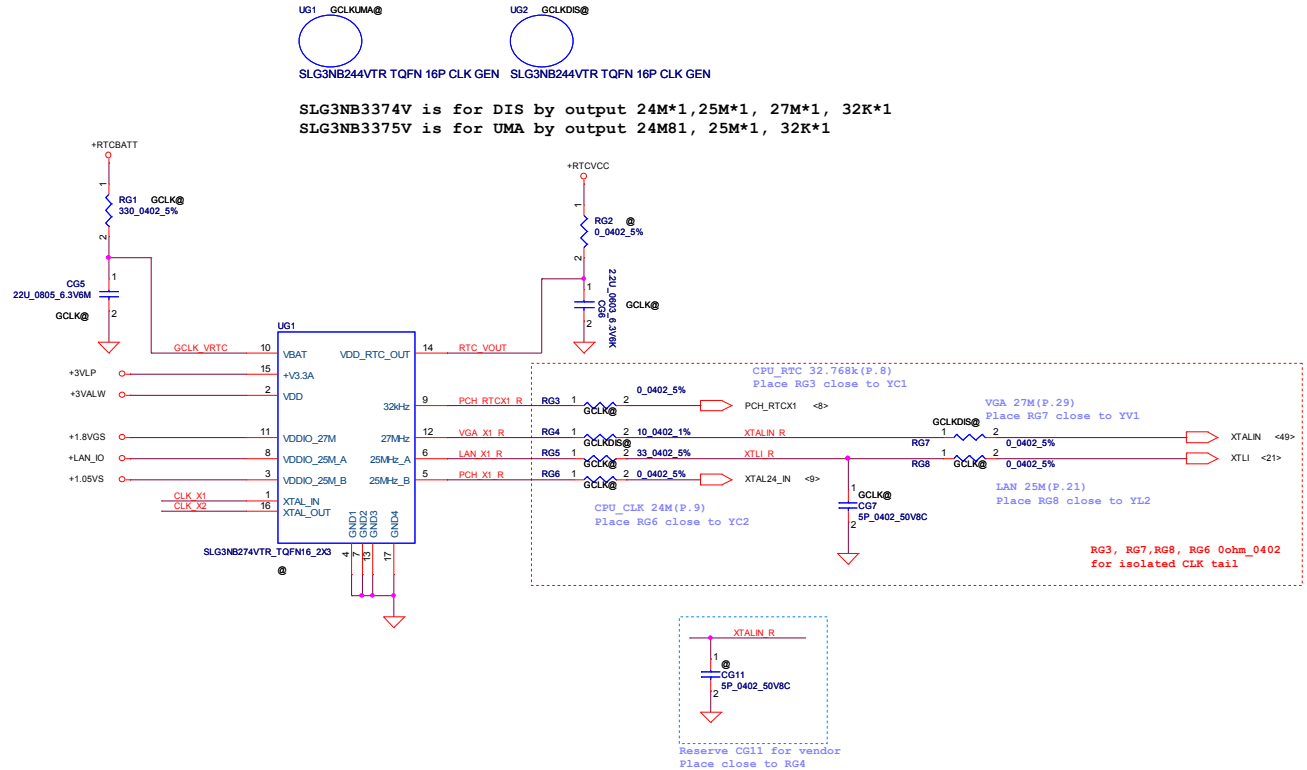
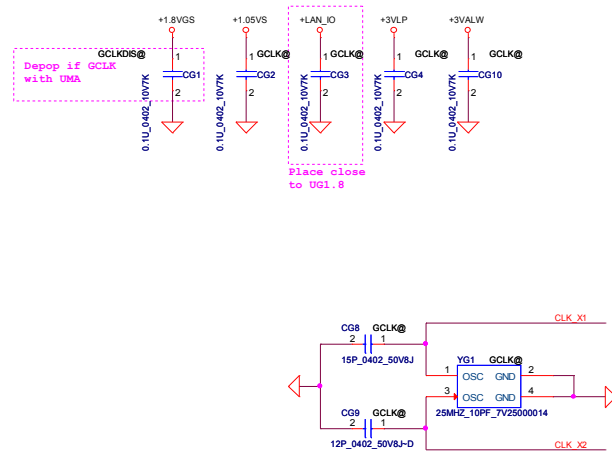


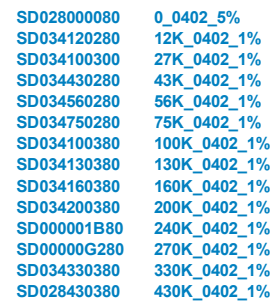
+3VALW_PCH switch



For Intel S3 Power Reduction

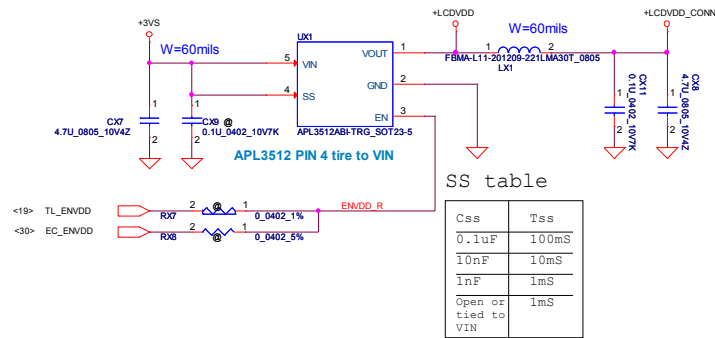
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					LA-9982P
				Rev	3.0
				Date:	Wednesday, May 29, 2013
				Sheet	28 of 57



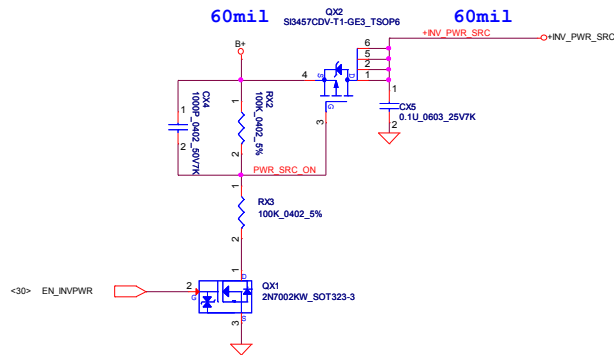


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						LA-9982P		3.0
						Date	Wednesday, May 29, 2013	Sheet

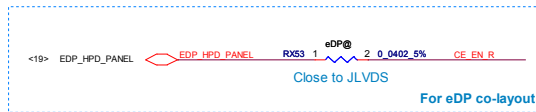
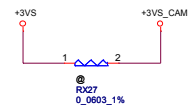
LCD PWR CTRL



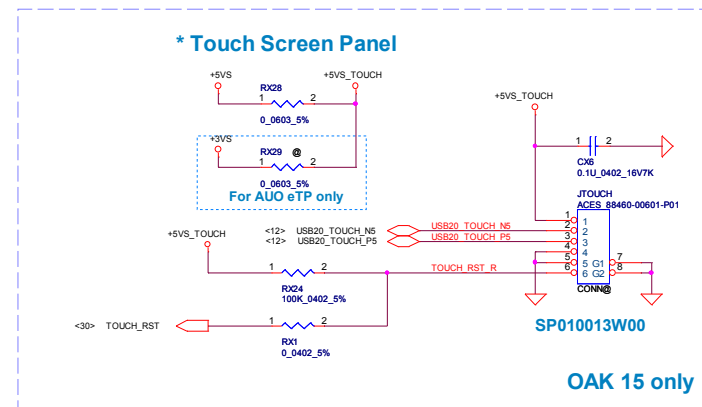
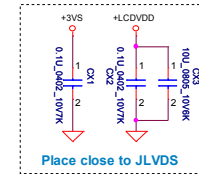
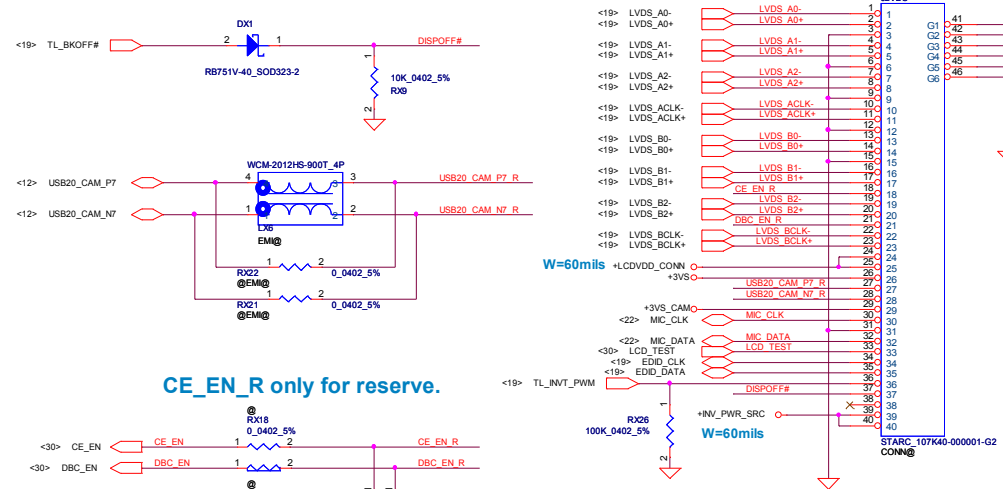
LCD backlight PWR CTRL



Webcam PWR CTRL

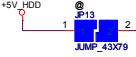


LVDS Connector

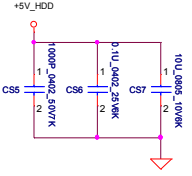
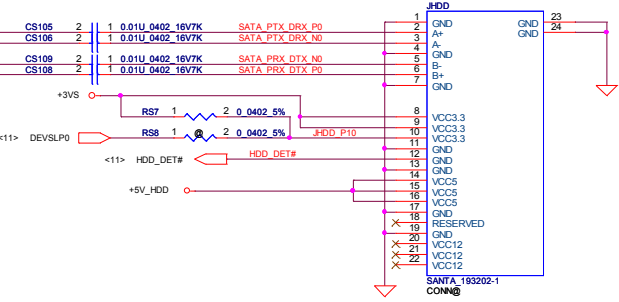


SATA HDD Connector

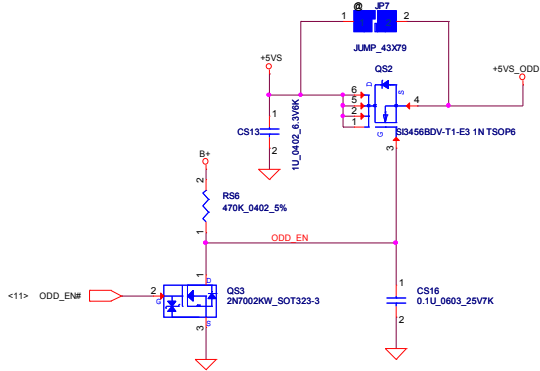
+5V_HDD Source



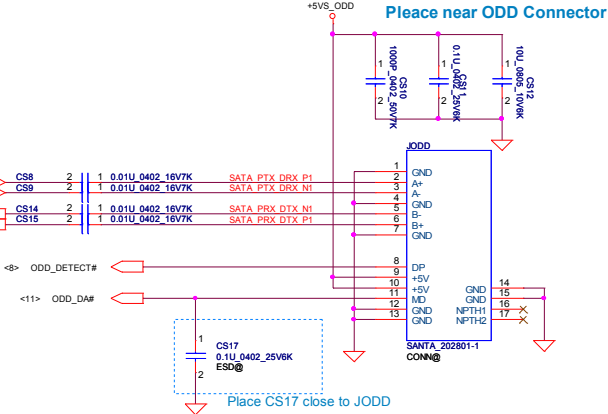
SHORT DEFAULT



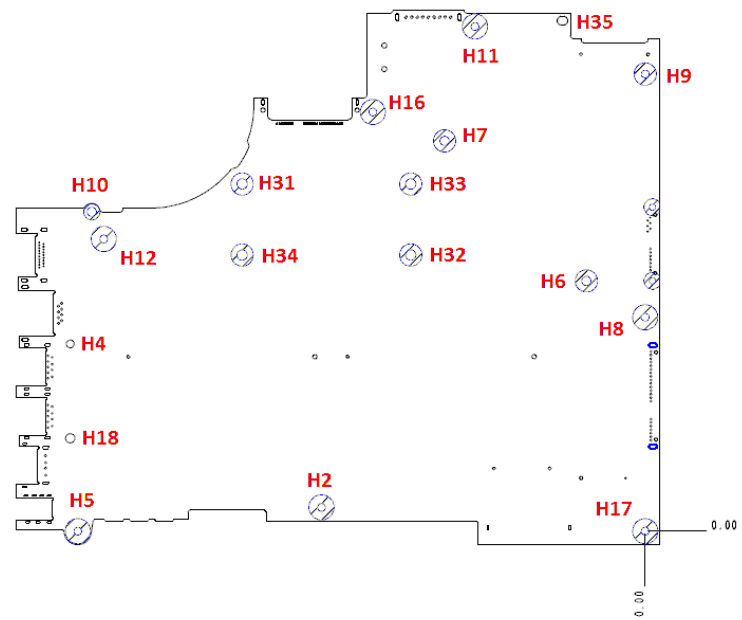
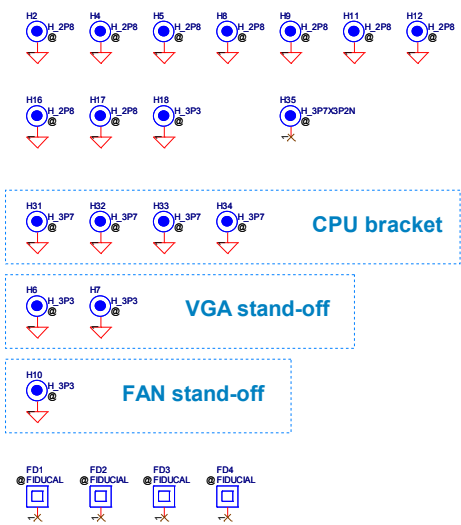
ODD Power Control



SATA ODD Connector



Screw Hole



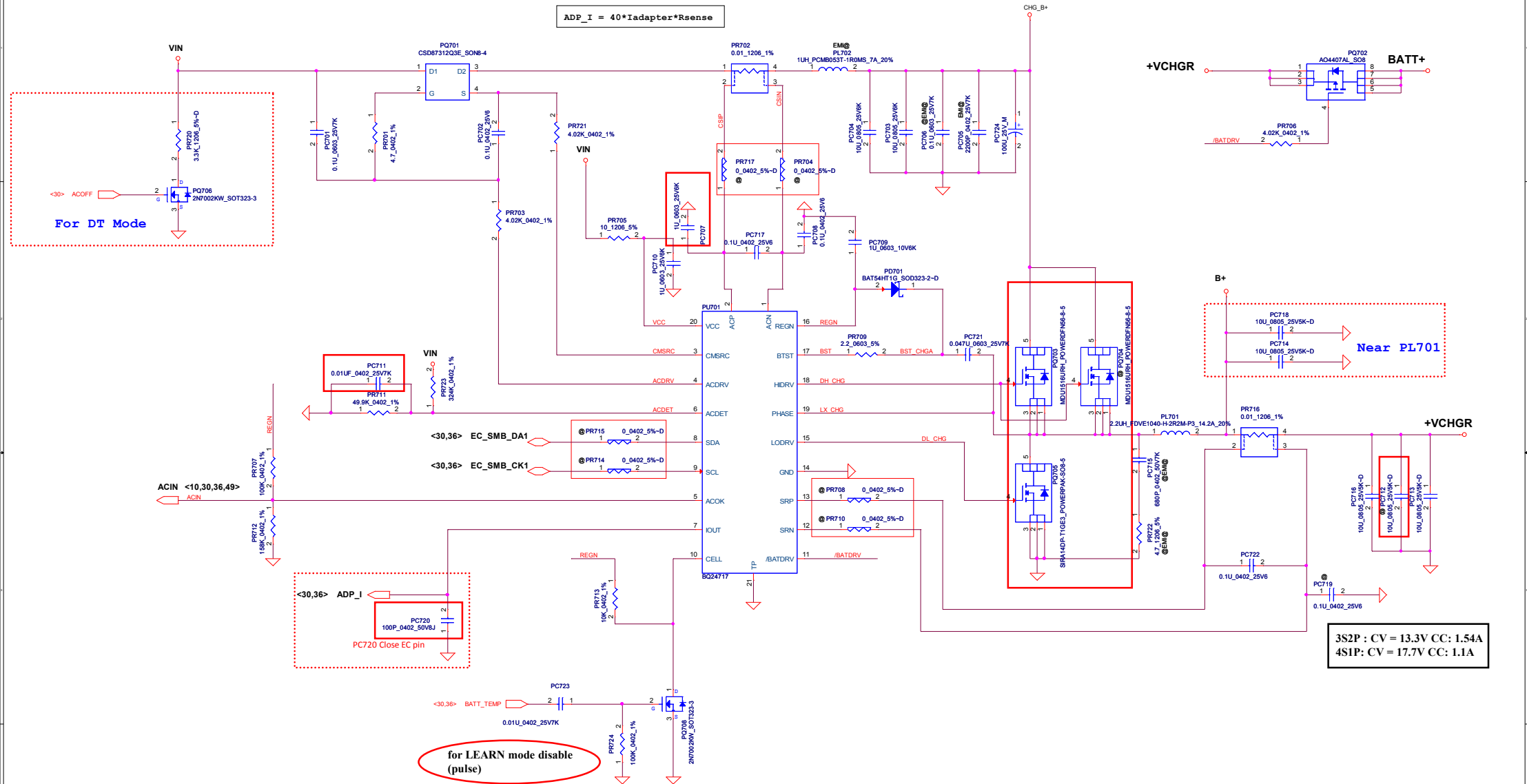
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1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP URL USB signal P/N	0.2
2							
3							
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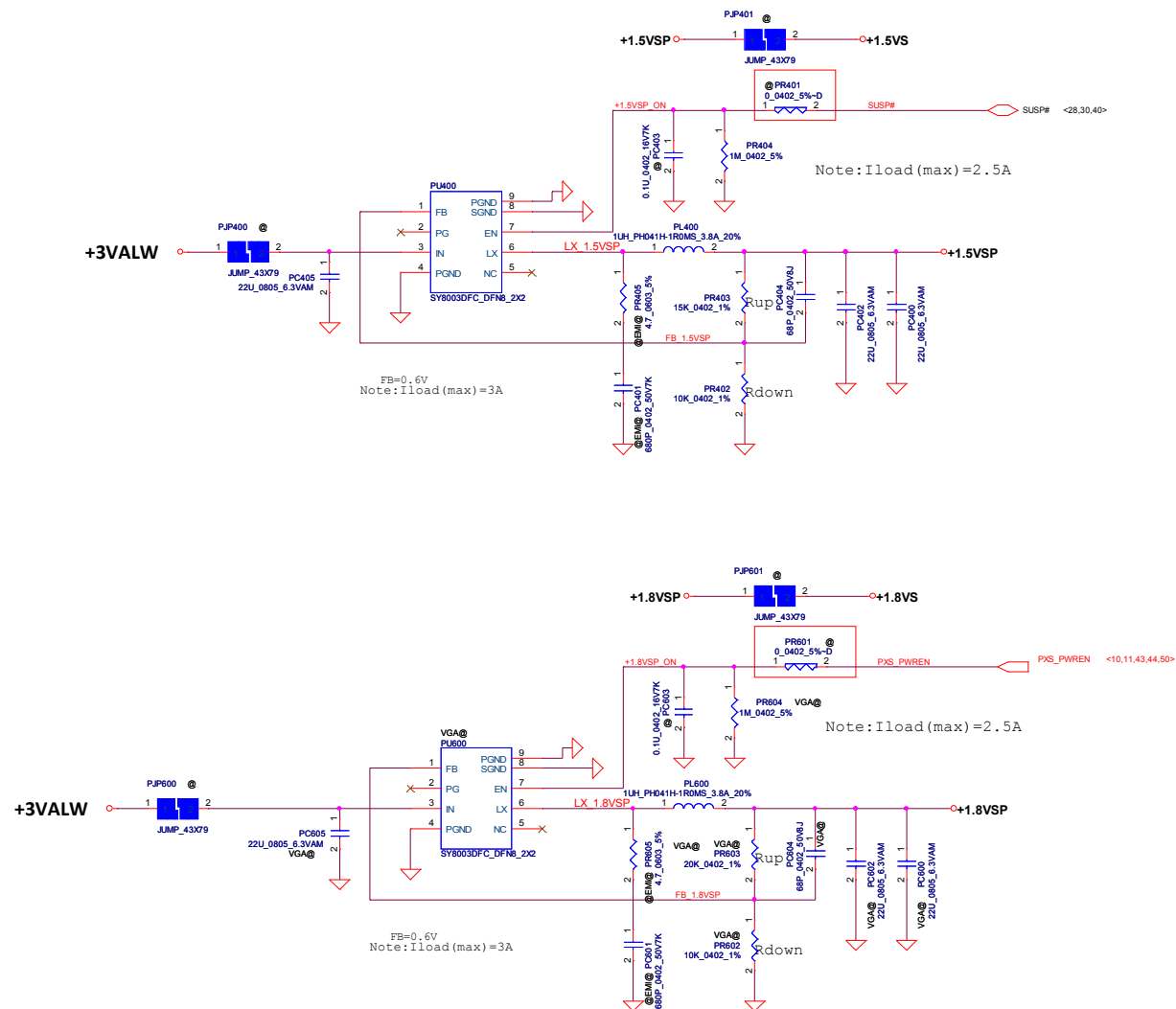
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40							
41							
42							
43							
44							
45							
46							
47							
48							
49							
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54							

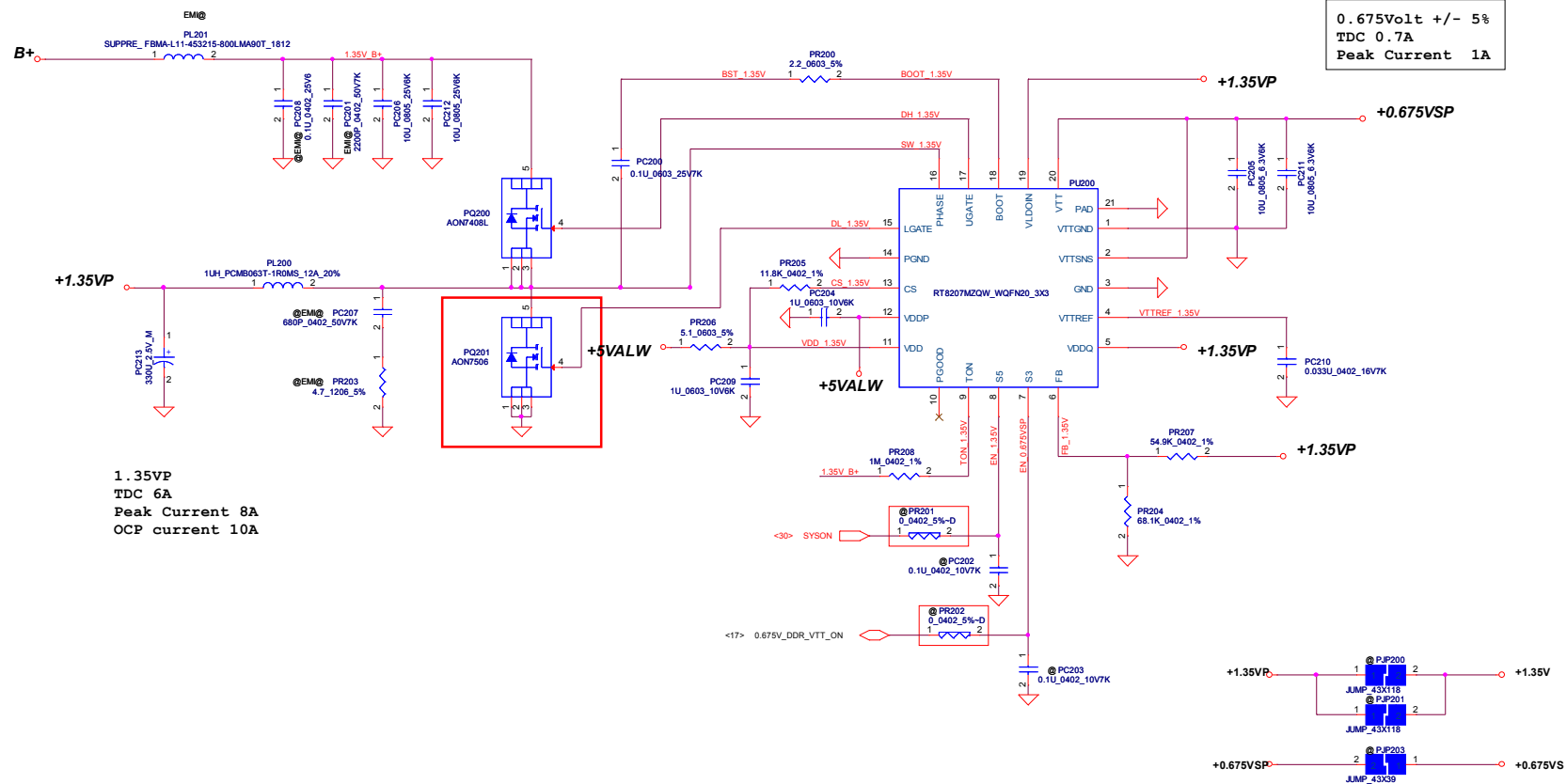
Iada=0~3.33A (65W)

Iada=0~4.62A (90W)

$$ADP_I = 40 \times I_{\text{adapter}} \times R_{\text{sense}}$$





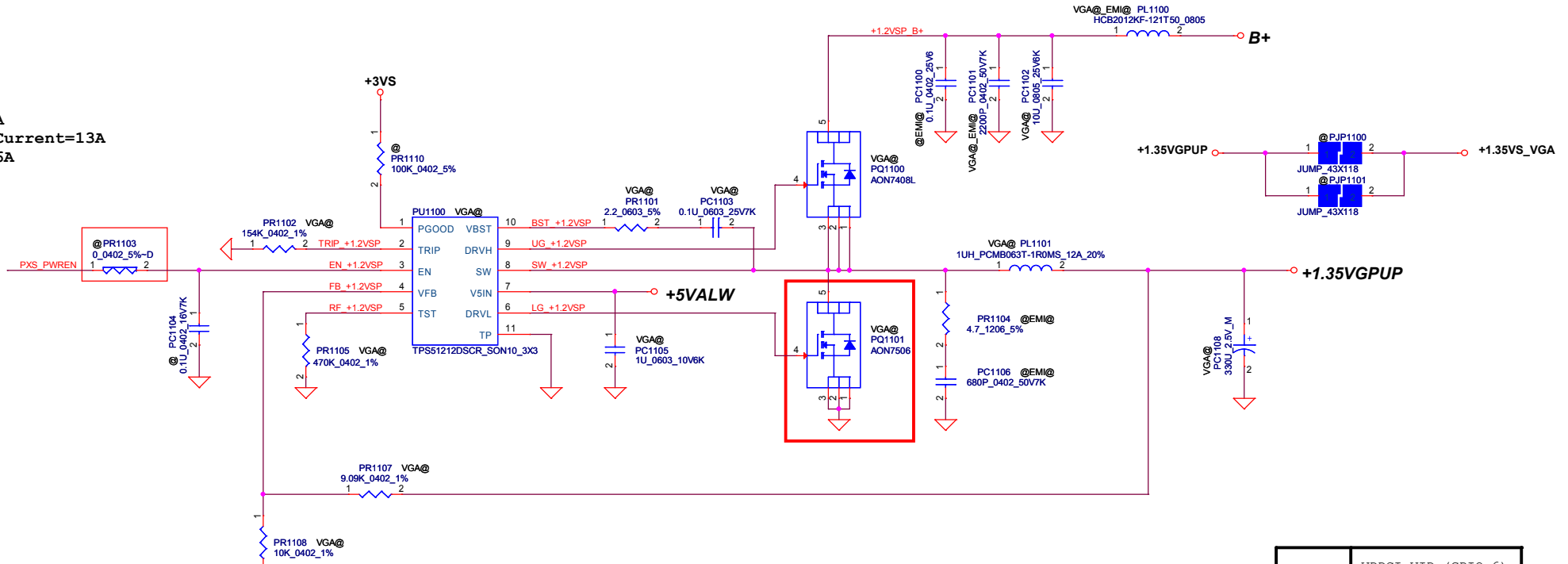


0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

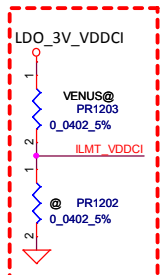
1.35VP
TDC 6A
Peak Current 8A
OCP current 10A

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	Title	PWR +1.35VP/0.675VSP
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				Date	Wednesday, May 29, 2013
				Sheet	41 of 57
				Rev	3.0

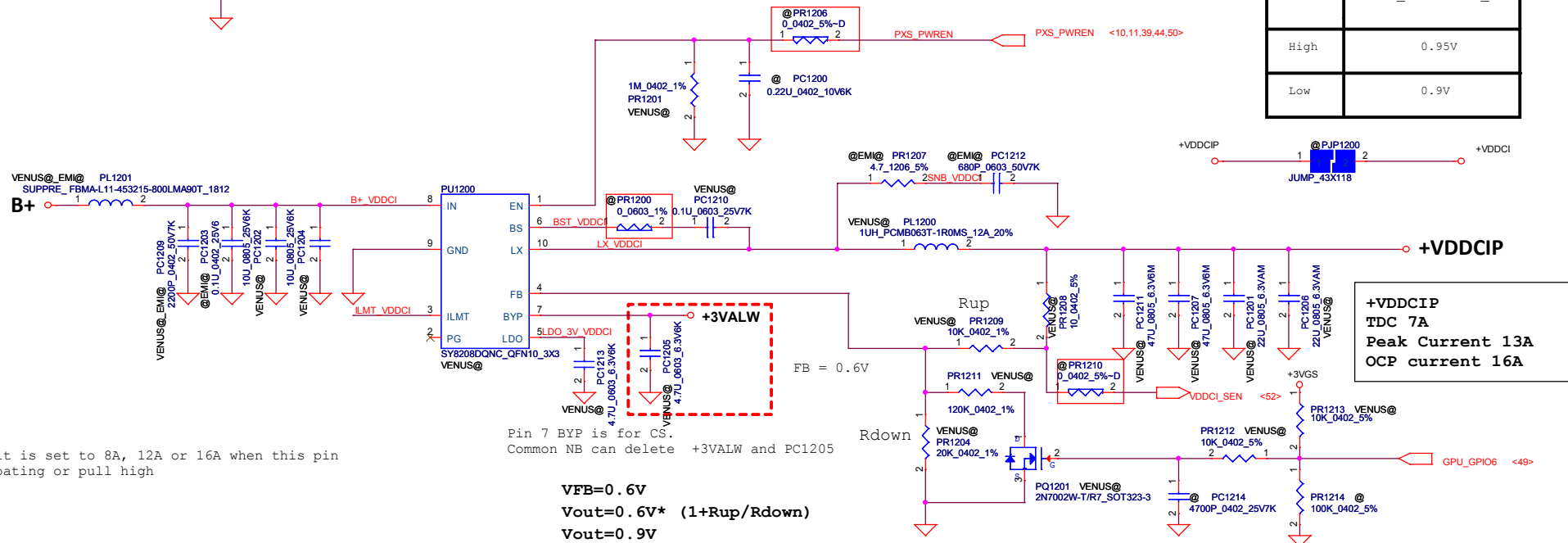
TDC=9A
Peak Current=13A
OCP=16A



	VDDCI_VID (GPIO_6)
High	0.95V
Low	0.9V



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high



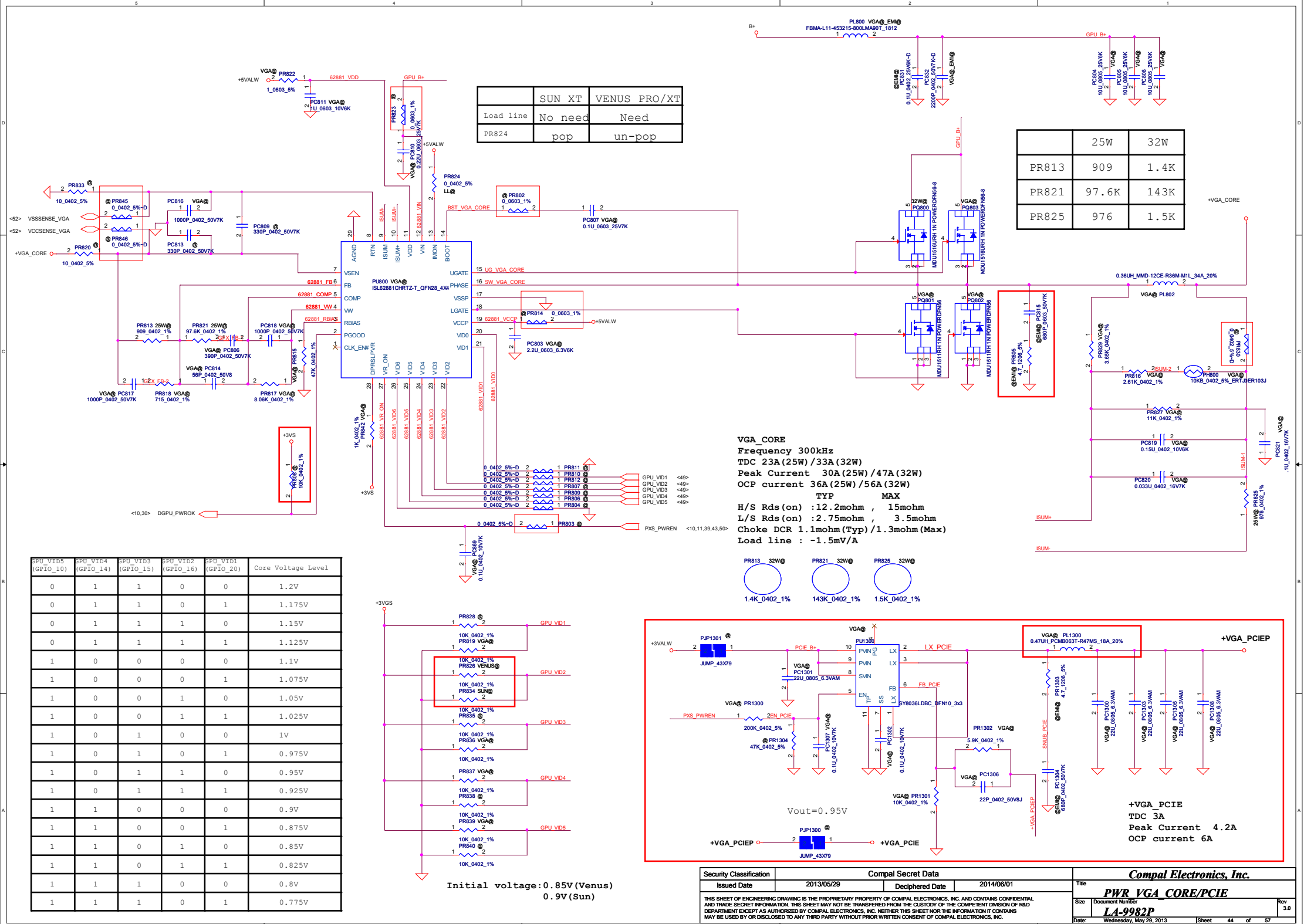
Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC1205

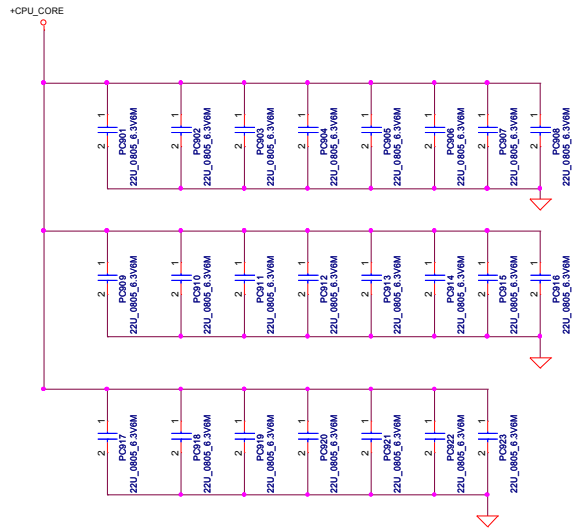
$$VFB=0.6V$$

$$Vout=0.6V \cdot (1+Rup/Rdown)$$

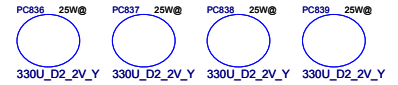
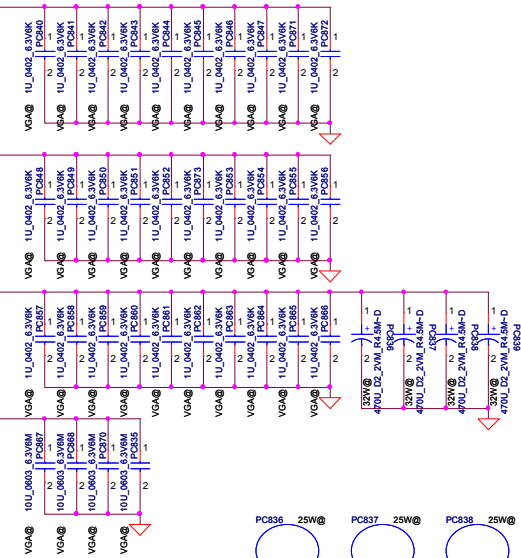
$$Vout=0.9V$$

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	Title	PWR +1.35VGPU/VDDCIP
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				LA-9982P	
				Date	Wednesday, May 29, 2013
				Sheet	43 of 57



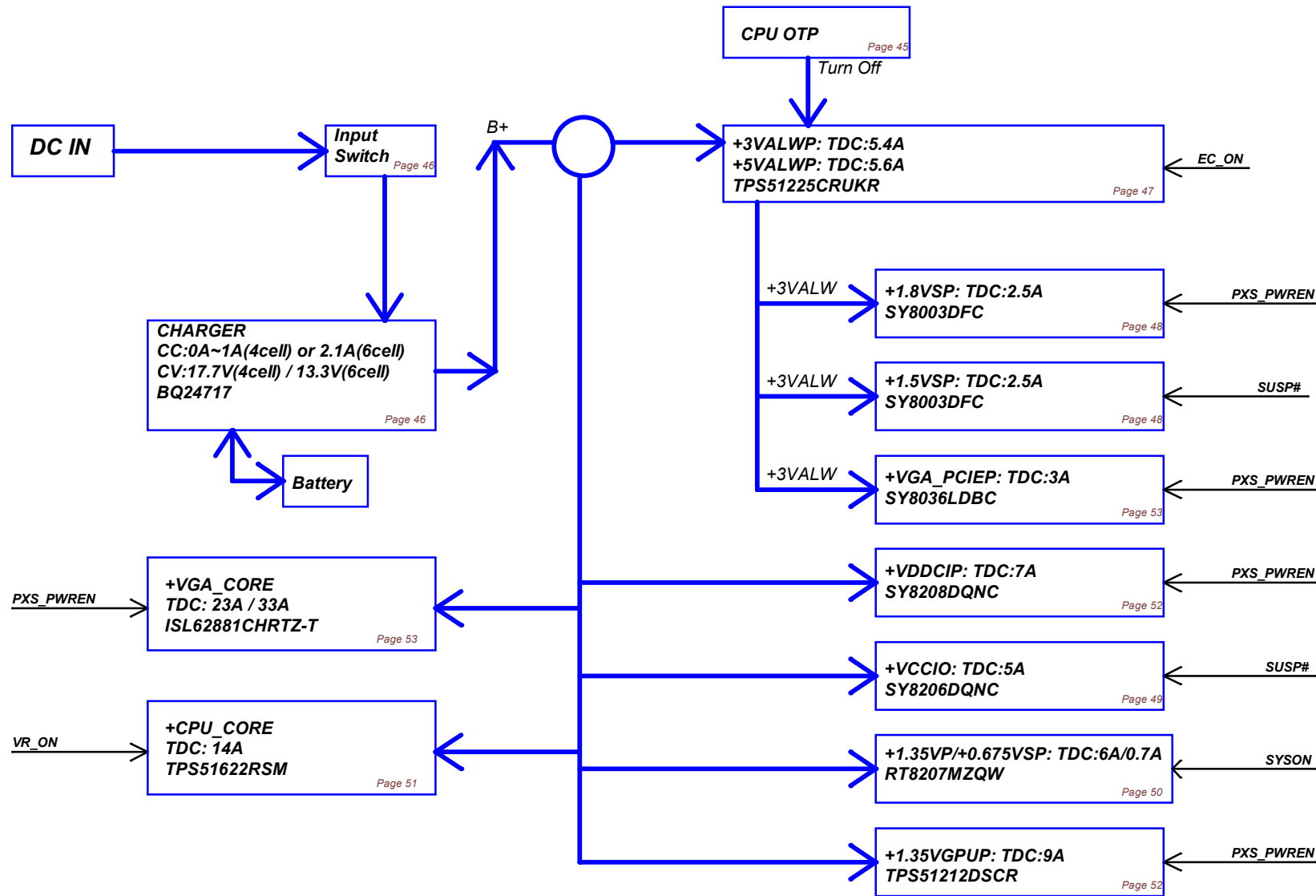


+VGA_CORE



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Issued Date		2013/05/29	Deciphered Date	2014/06/01	Title		
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					Size	Document Number	Rev
					LA-982P	3.0	
Date:		Wednesday, May 29, 2013		Sheet	45 of 57		

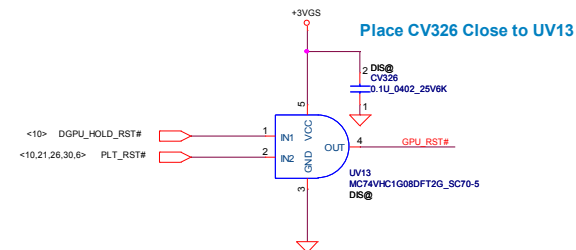
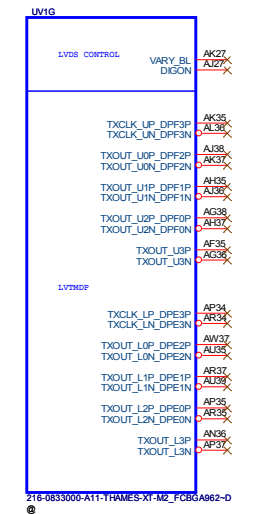
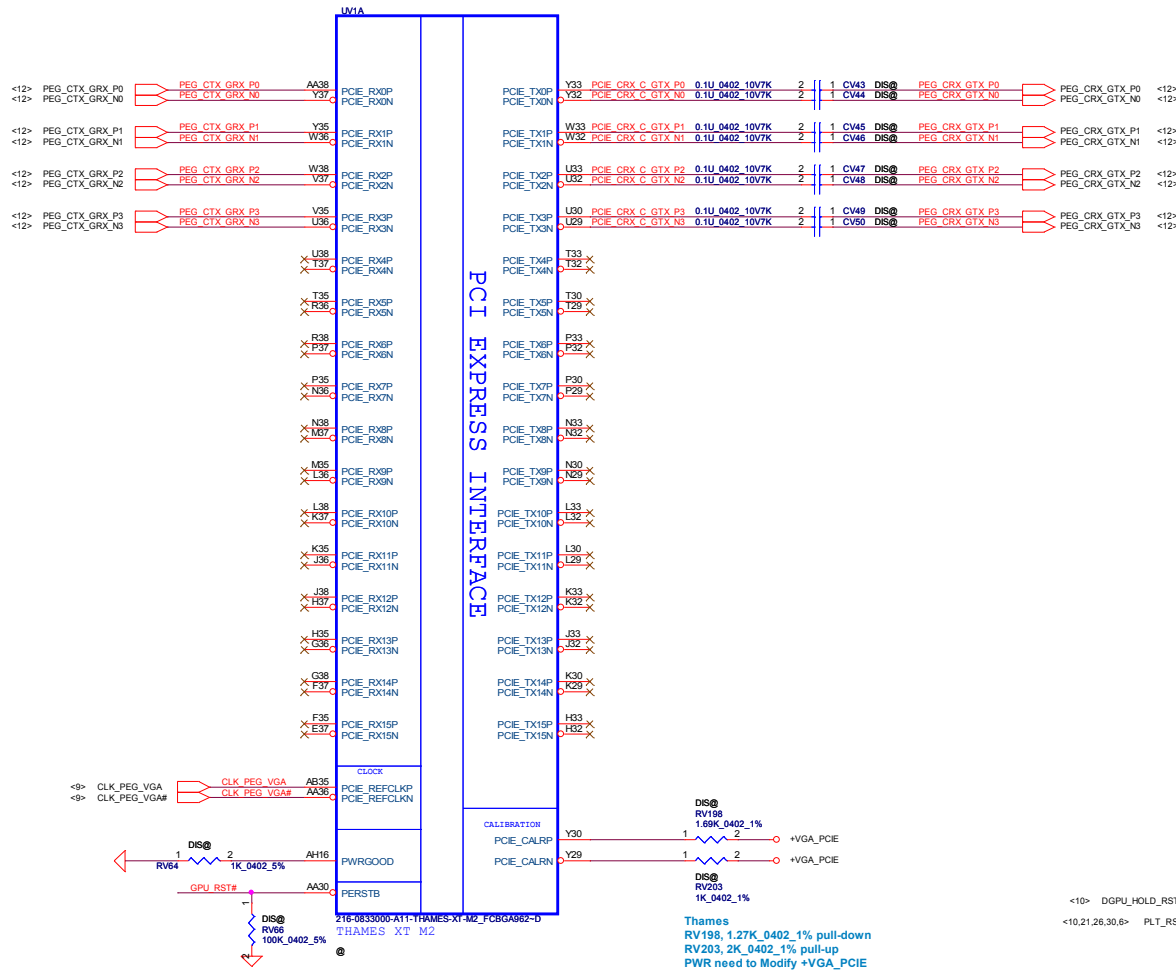
Power block



Page 1

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/05/29	Deciphered Date	2014/06/01	Title	PWR-PIR	
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					LA-9982P	3.0
Date:				Wednesday	May 28 2013	Sheet 47 of 57

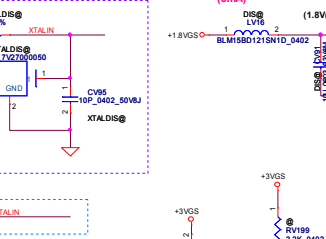
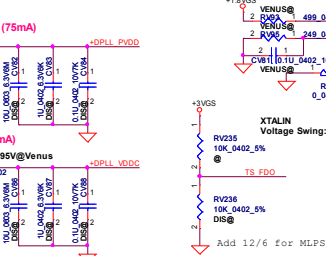
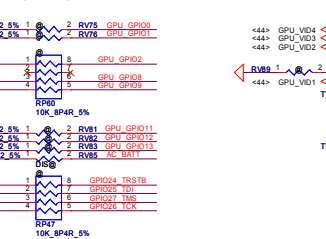
GFX PCIE LANE REVERSAL



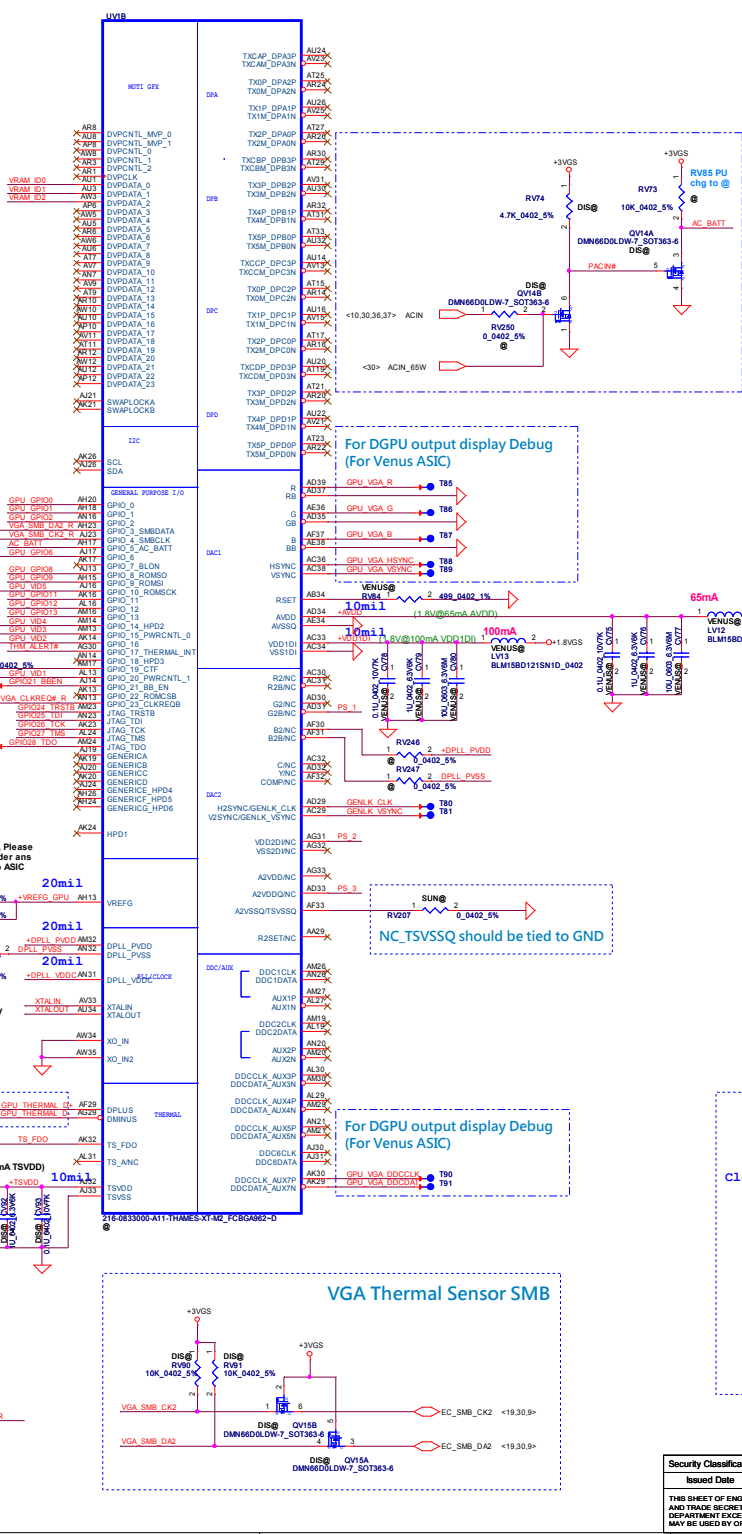
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2013/05/29	Deciphered Date	2014/06/01	Title ATI Venus Pro M2 PCIE/LVDS		
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				Date	Wednesday, May 29, 2013	Sheet 48 of 57

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix 2Gb SA00004GD1L(R1) SA00004GD2L(R3)	RV67	RV69	RV71
Samsung 2Gb SA00005B70L(R1) SA00005B71L(R3)	RV68	RV69	RV71
	RV67	RV70	RV71
Hynix 2Gb SA00006H40L(R1) SA00006H41L(R3)			
Samsung 2Gb SA00005SH0L(R1) SA00005SH1L(R3)			
Micron 2Gb SA00005XB0L(R1) SA00005XB1L(R3)			

STRAPS

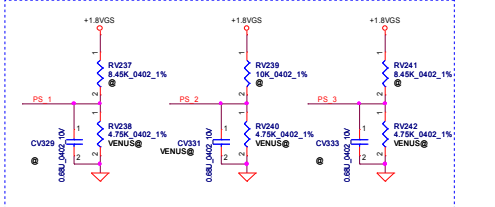


SUN internal VGA Thermal Sensor
Address 0x714



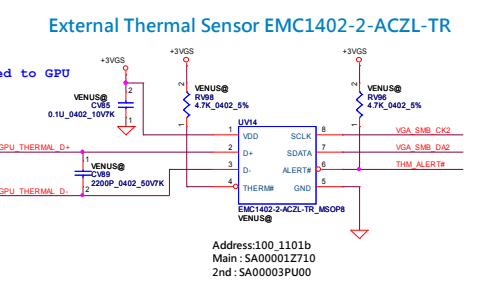
CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPI00	GPIO FULL TX OUTPUT SWING	0: 50% swing 1: full swing
TX_DEEMPH_EN	GPI01	PCI TRANSMITTER DE-EMPHASIS	0: disable 1: enable
RSVD	GPI02	Advertises PCIe speed when compliance test	0: 2.5Gt/s 1: 5.0Gt/s
RSVD	GPI08	RESERVED	0
BF_VGA_DIS	GPI09	VGA ENABLED	0
RSVD	GPI021	RESERVED	0
BIOS_ROM_EN	GPI0_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable
ROMCFG(2:0)	GPI0(13:1)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
WP_DEVICE_STRAP_ENA	V2SYNC	IGNORE WP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0] 0: No audio function 1: Audio for DisplayPort and HDMI if dongle is detected	11
AUD[0]	VSNC	1: Audio for DisplayPort only 1: Audio for both DisplayPort and HDMI	

AMD RESERVED CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET			
GPI021	H2SYNC	GENERICC	GPI02



SUN MLPs PS_3			
Vendor	MLP	NC	Bits [3:1]
Hynix	NC	4.75k	000
Samsung	8.45k	2k	001
Micron	4.75k	NC	111

VENUS MLPs
PS_3 used default

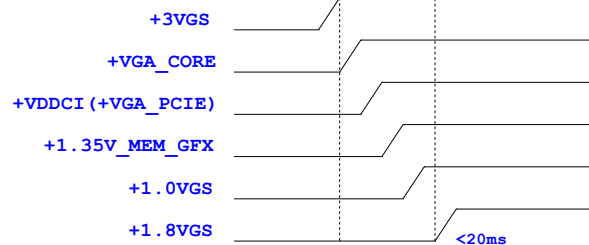


Address: 100_1101b
Main: SA00001Z710
2nd: SA00003PU00

Security Classification		Compel Secret Data		Compel Electronics, Inc.	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	Title	ATI Venus Pro M2 Main MSIC
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				LA-9982P	Rev 3.0
				Date	Wednesday, May 29, 2013
				Sheet	49 of 57

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Note:

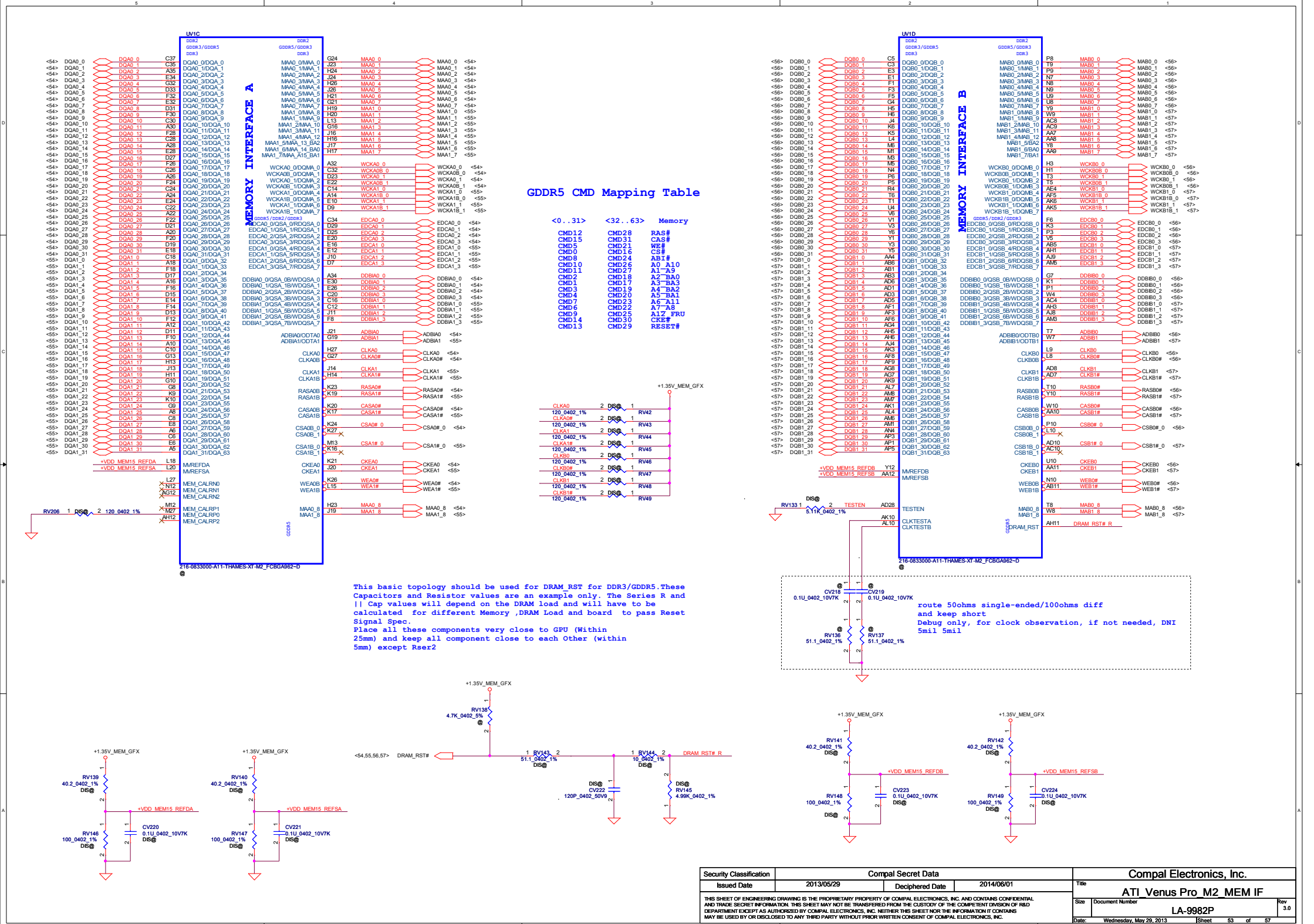
Power sequence of Sun XT,Venus Pro,Venus XT



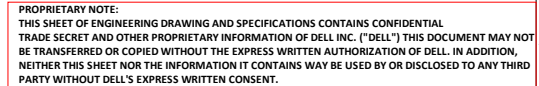
A schematic diagram showing a short circuit. Two red wires, each labeled +1.8V, are connected to a blue component labeled 2MM J0. The component has two pins, labeled 2 and 1, which are connected to the two +1.8V sources. A circled 'X' is placed above the component, indicating a fault or error.

A diagram of a 2-pin jumper labeled JP9. The pins are numbered 1 and 2. A blue line connects pin 1 to pin 2, indicating a short circuit. The text "2MM" is written below the pins. Above pin 2 is the label "+1.35VS_VGA" and above pin 1 is the label "+1.35V_MEM_GFX".

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Issued Date	2013/05/29	Deciphered Date	2014/06/01	Title	ATI Venus Pro M2 BACO POWER	
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					LA-9982P	3.0
				Date	Wednesday, May 29, 2013	Sheet

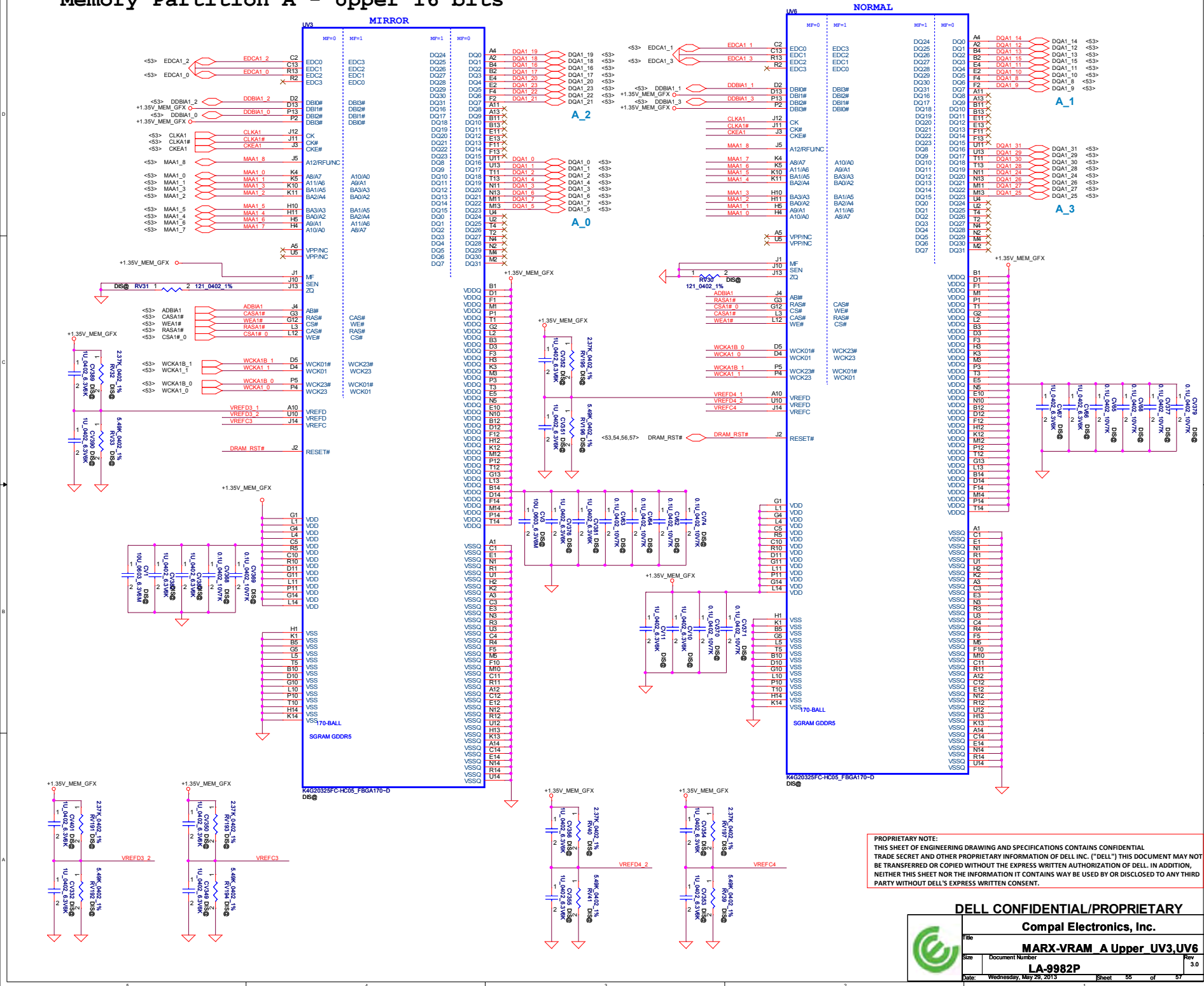


64X32 GDDR5

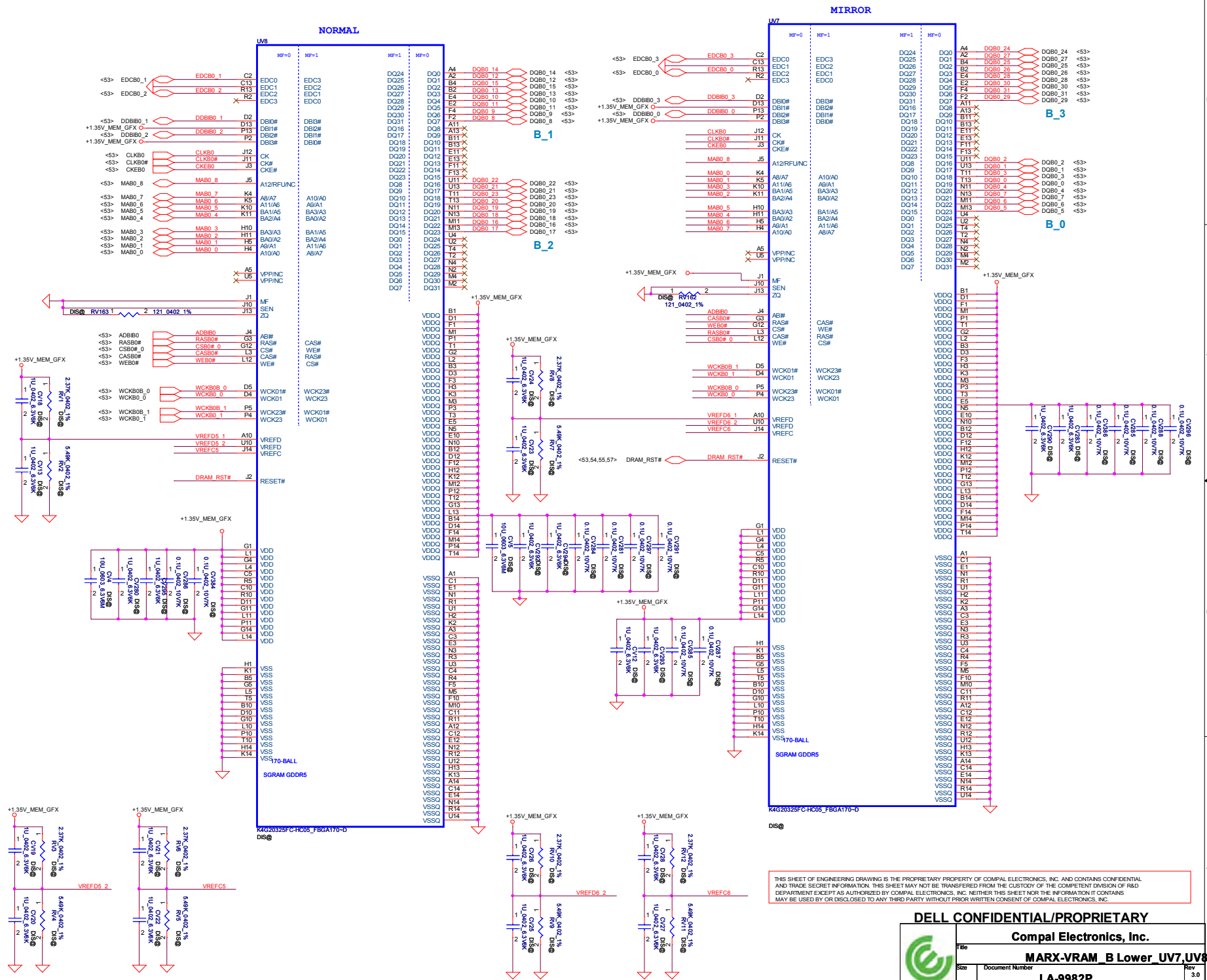


Title			
VRAM A Lower UV4,UV5			
Size	Document Number		Rev
	LA-9982P		3.0
Date:	Wednesday, May 29, 2013	Sheet	54 of 57

5	4
Memory Partition A - Upper 16 bits	



Memory Partition B - Lower 16 bits



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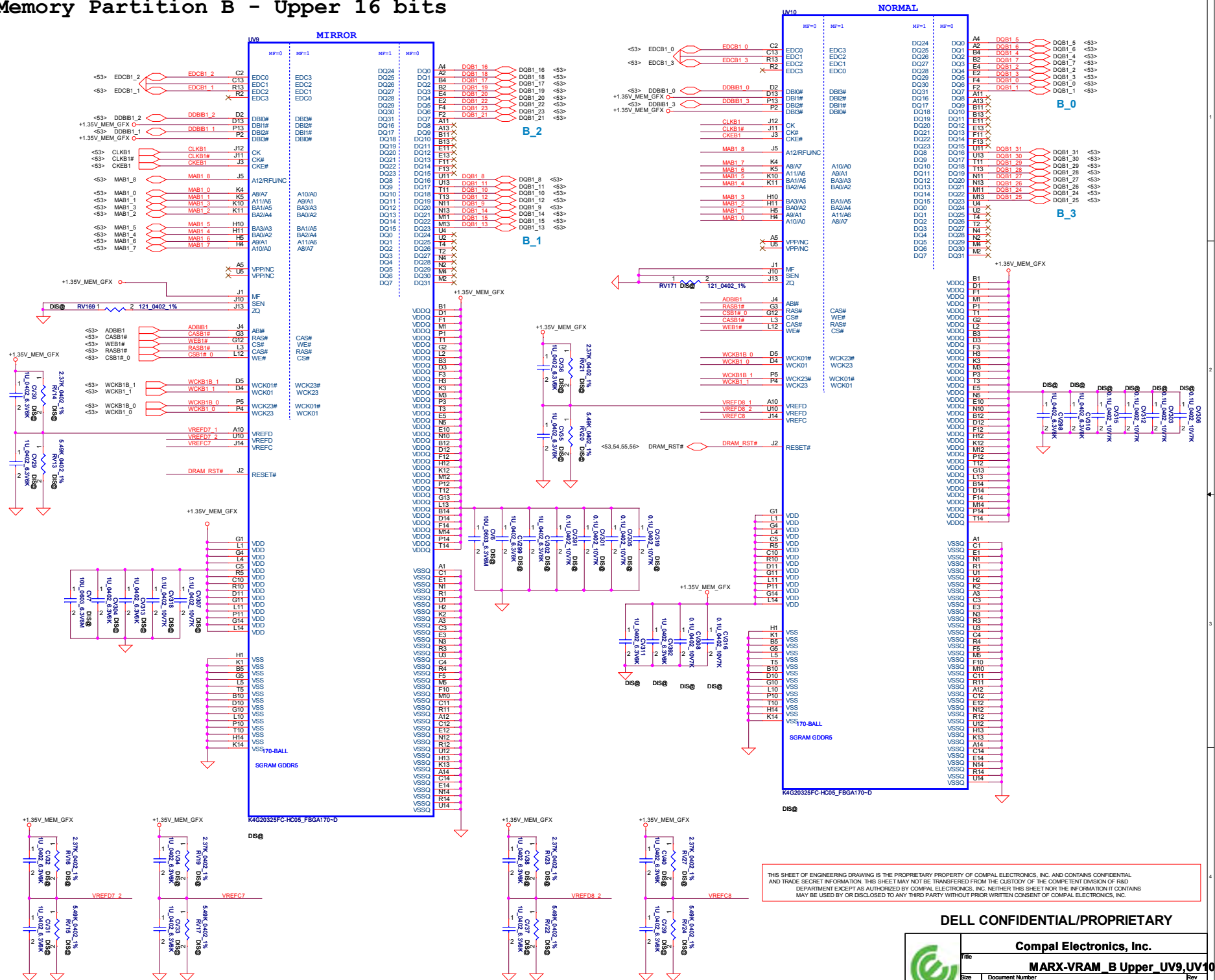
MARX-VRAM_B Lower UV7,UV8

LA-9982P

Rev
3.0

Date: Wednesday, May 29, 2013 Sheet 56 of 57

Memory Partition B - Upper 16 bits



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MARX-VRAM_B Upper_UV9,UV10

LA-9982P

Rev
3.0

Date: Wednesday, May 29, 2013 Sheet 57 of 57