

MODEL NAME :ZAW12
PCB NO : LA-A691P
BOM P/N : DA60012B000 LA-A691P M/B
DA40001G410 LS-9105P POWER BUTTON/B
DA40001FP10 LS-9102P USB/B
DA40001FQ10 LS-9103P TP BUTTON/B
DA40001FR10 LS-9104P ODD/B

Dell / Compal Confidential

Schematic Document

AMD FP2 Richland Processor with DDRIII + Bolton M3 FCH

AMD VGA Sun XT

2013-05-23

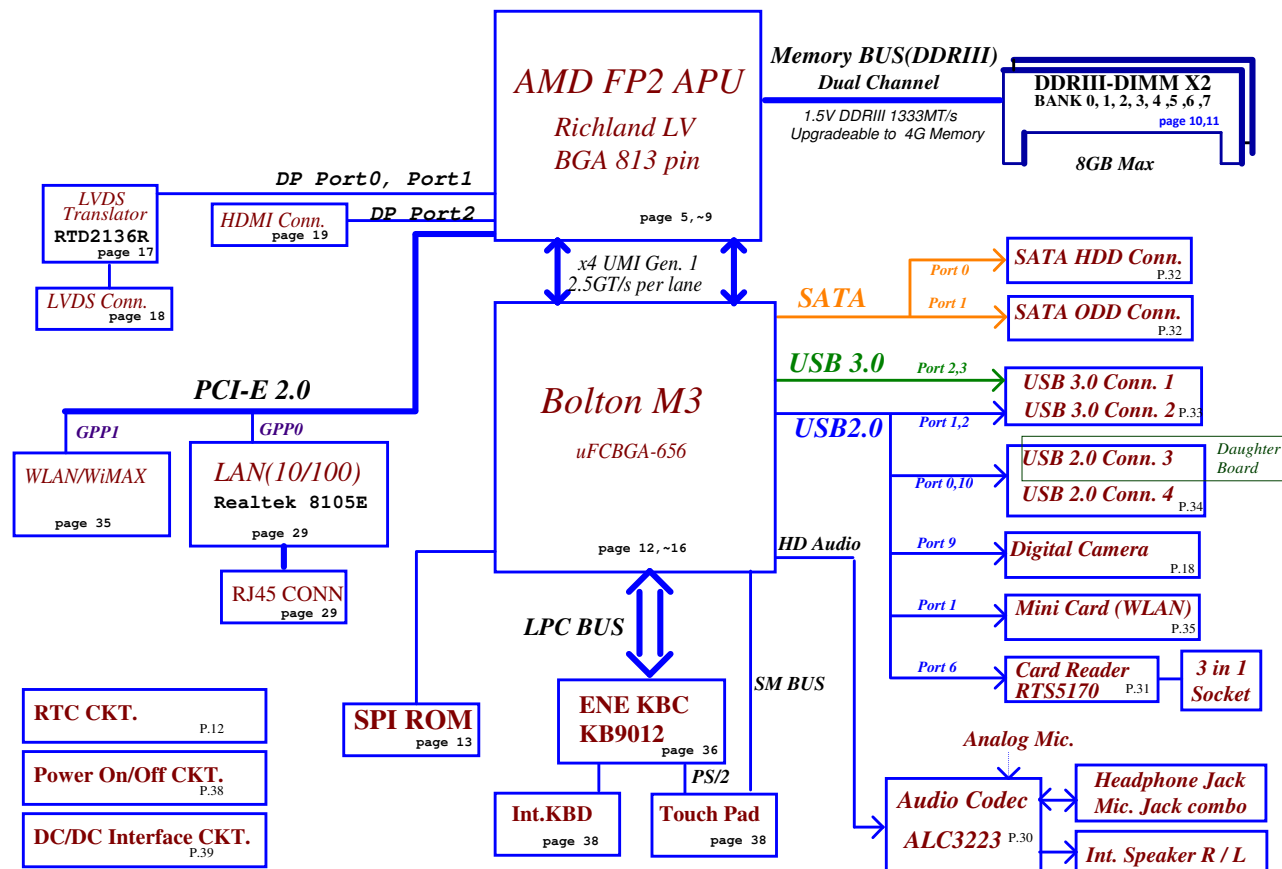
Rev: 1.0

46@ : for 46 level
@ : Nopop Component
CONN@ : Connector Component
UMA@ : Only for UMA
DIS@ : Only for Discrete
GCLK@ : Green CLK implemented
NGCLK@ : Non Green CLK implemented
@3221: ALC 3221
@3223 : ALC 3223
EMC@ : EMC Parts
NEMC@ : EMC不上件

R1@ : R1 P/N for PCB
R3@ : R3 P/N for PCB
THR1@ : Thames-XT R1 P/N
THR3@ : Thames-XT R3 P/N
CHR1@ : Chelsea-Pro R1 P/N
CHR3@ : Chelsea-Pro R3 P/N
R@ : RTD2132-R
S@ : RTD2132-S
KBBL@ : KeyBoard Backlight

X76@ : VRAM Group
CH@ : Chelsea M2
SE@ : Seymour M2
TH@ : Thames-XT
Mars@ : Mars Pro M2
A4R1@ : A4 APU-R1
A6R1@ : A6 APU-R1
A8R1@ : A8 APU-R1
A8@ : A8 APU Symbol
Hud@ : HUDSON-M3
Bol@ : BOLTON-M3

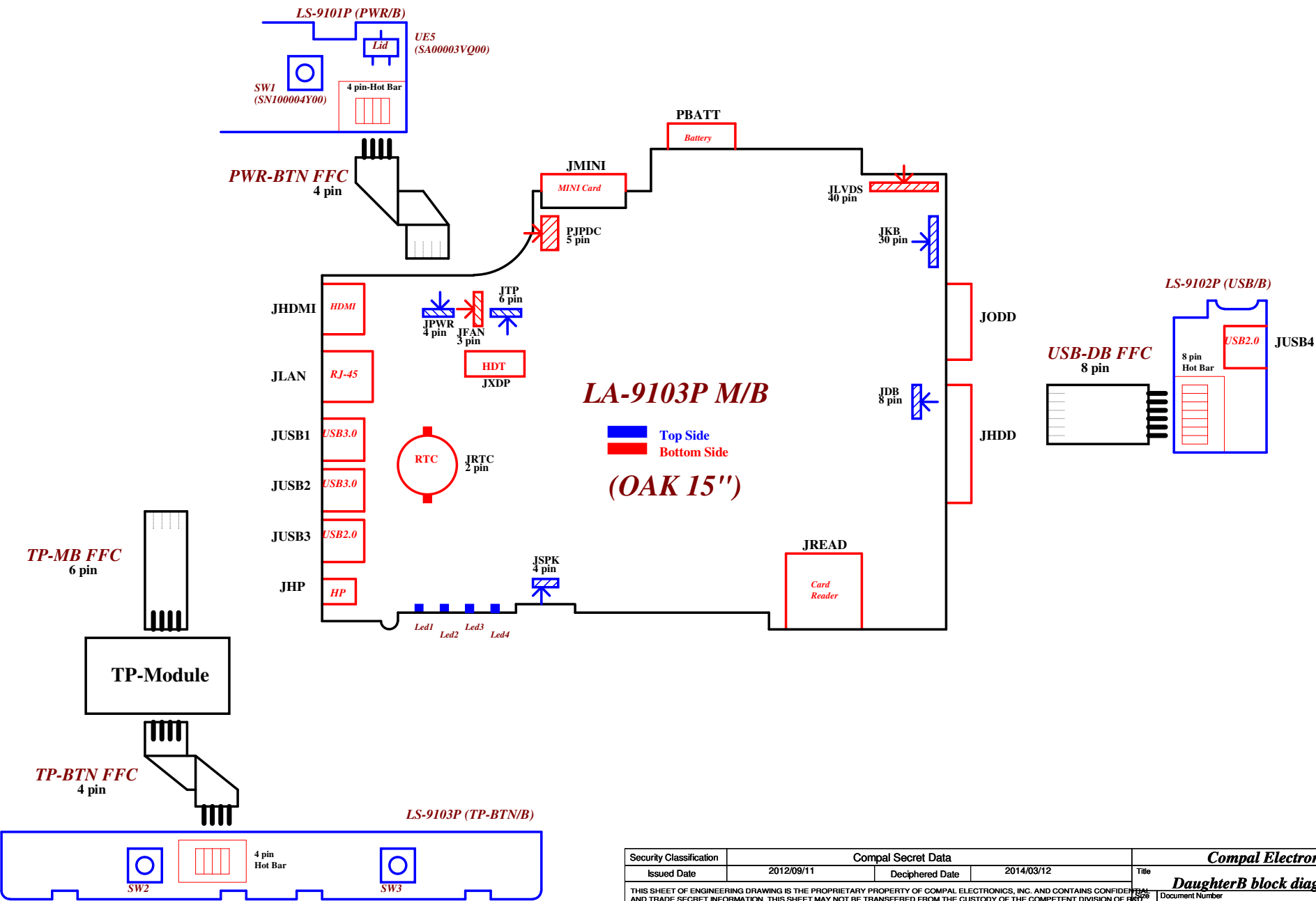
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Project Code : VAW03
File Name : LA-9103P



Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0 SD028330280
4	
5	
6	
7	

FCH

USB PORT#	DESTINATION
0	USB conn.3 DEBUG PORT
1	MINI CARD (WLAN)
2	USB conn.4
3	NC
4	NC
5	NC
6	Card Reader
7	NC
8	NC
9	Camera
10	USB conn.2
11	NC
12	NC
13	USB conn.1

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	000 1011	11h 0x16	ADM1032ARMZ	100 1101	4Dh 0x9A
Charger IC	000 1001	09h 0x12	SB-TSI	100 1100	4Ch 0x98
			RTD2132	100 1010	4Ah 0x94
			GPU	100 0001	41h 0x82

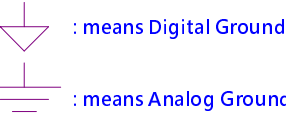
SM Bus Controller 0 (FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		

SM Bus Controller 1 (FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

Symbol Note :

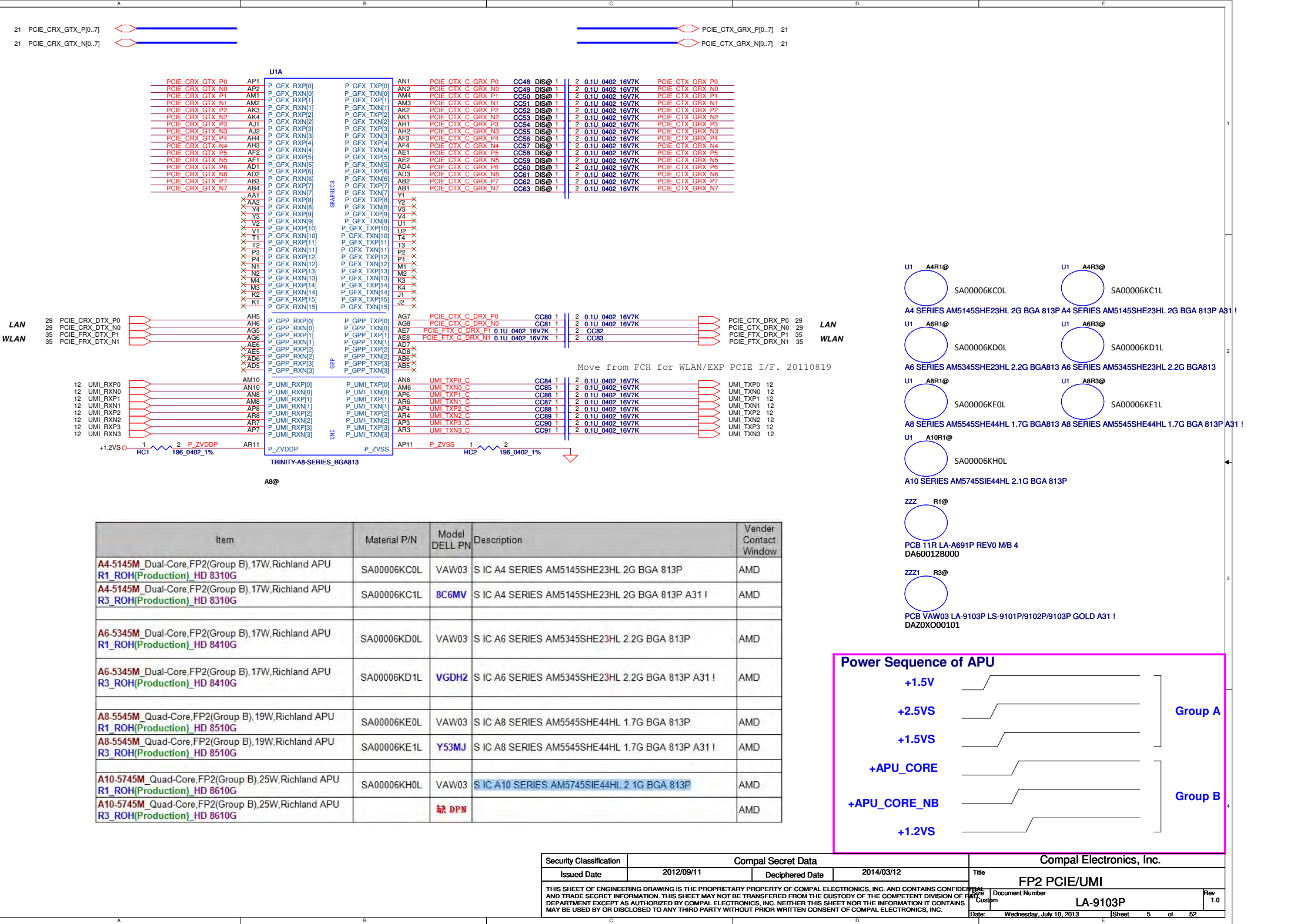


CLK

DIFFERENTIAL	DESTINATION
CLKOUT_PCIE0	None
CLKOUT_PCIE1	None
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI CARD WLAN
CLKOUT_PCIE4	None
CLKOUT_PCIE5	None
CLKOUT_PCIE6	None
CLKOUT_PCIE7	None
CLKOUT_PEG_B	None

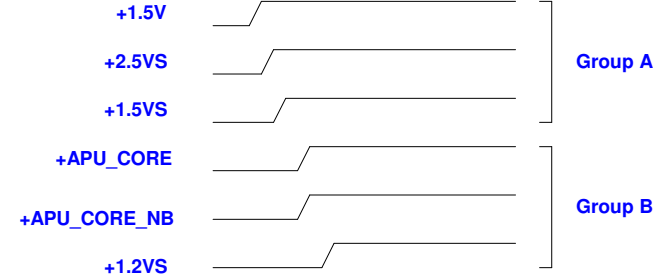
SATA	DESTINATION
SATA0	HDD
SATA1	ODD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

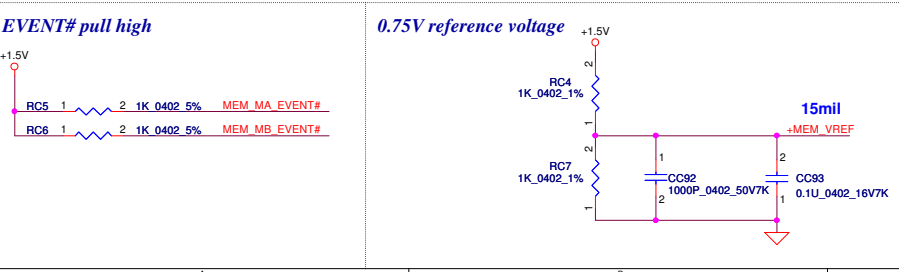
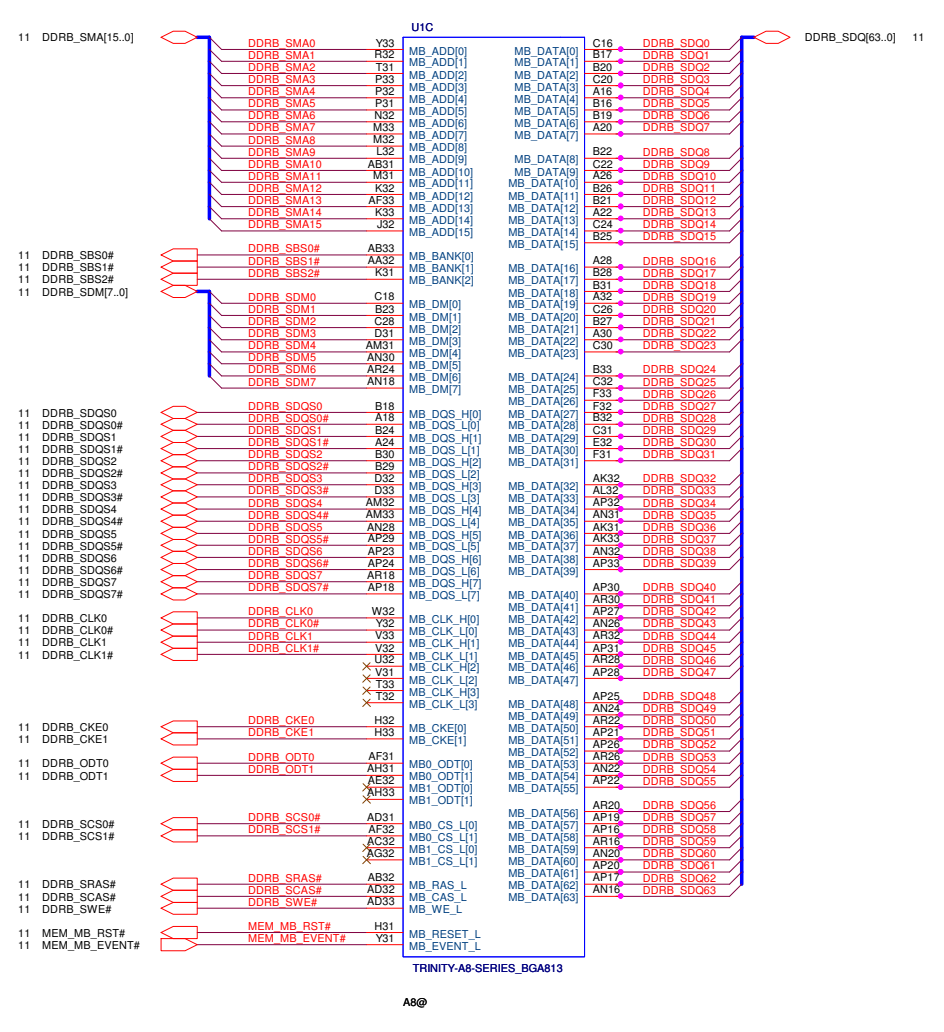
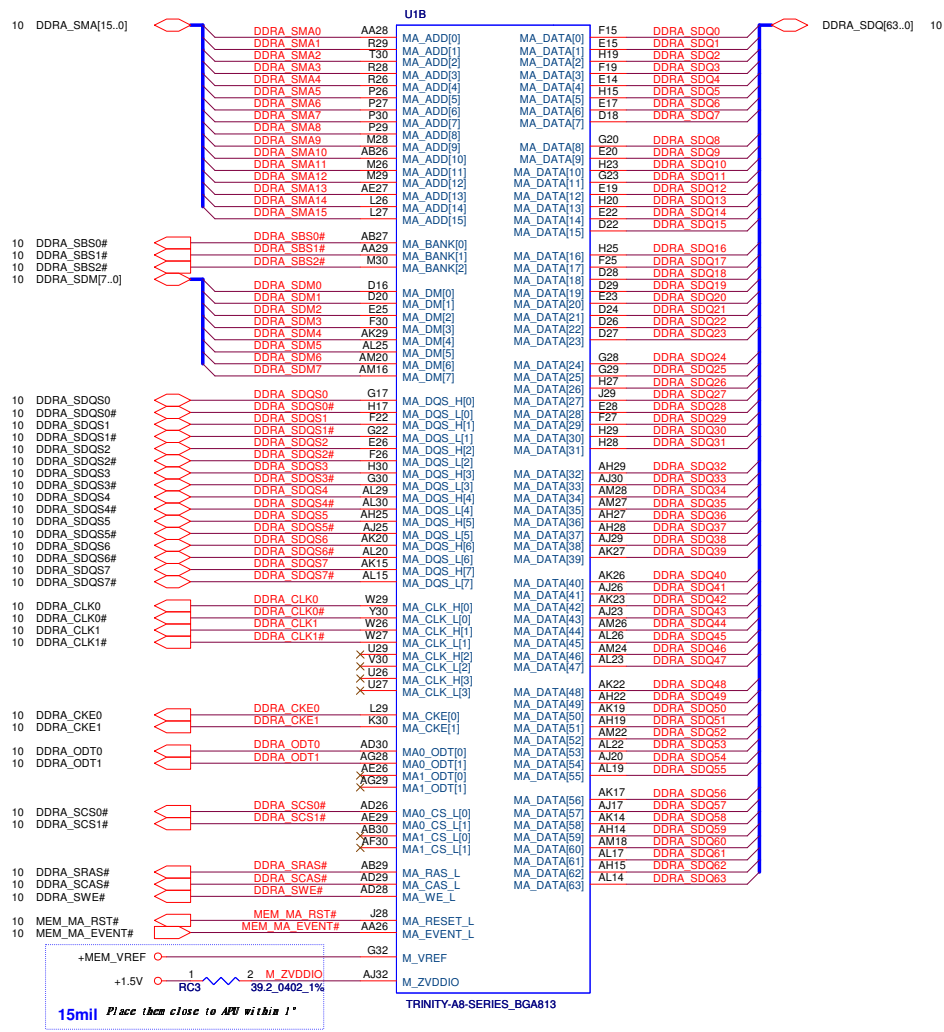


Item	Material P/N	Model DELL PN	Description	Vendor Contact Window
A4-5145M Dual-Core,FP2(Group B),17W,Richland APU R1_ROH(Production)_HD 8310G	SA00006KC0L	VAW03	S IC A4 SERIES AM5145SHE23HL 2G BGA 813P	AMD
A4-5145M Dual-Core,FP2(Group B),17W,Richland APU R3_ROH(Production)_HD 8310G	SA00006KC1L	8C6MV	S IC A4 SERIES AM5145SHE23HL 2G BGA 813P A31 !	AMD
A6-5345M Dual-Core,FP2(Group B),17W,Richland APU R1_ROH(Production)_HD 8410G	SA00006KD0L	VAW03	S IC A6 SERIES AM5345SHE23HL 2.2G BGA 813P	AMD
A6-5345M Dual-Core,FP2(Group B),17W,Richland APU R3_ROH(Production)_HD 8410G	SA00006KD1L	VGDH2	S IC A6 SERIES AM5345SHE23HL 2.2G BGA 813P A31 !	AMD
A8-5545M Quad-Core,FP2(Group B),19W,Richland APU R1_ROH(Production)_HD 8510G	SA00006KE0L	VAW03	S IC A8 SERIES AM5545SHE44HL 1.7G BGA 813P	AMD
A8-5545M Quad-Core,FP2(Group B),19W,Richland APU R3_ROH(Production)_HD 8510G	SA00006KE1L	Y53MJ	S IC A8 SERIES AM5545SHE44HL 1.7G BGA 813P A31 !	AMD
A10-5745M Quad-Core,FP2(Group B),25W,Richland APU R1_ROH(Production)_HD 8610G	SA00006KH0L	VAW03	S IC A10 SERIES AM5745SIE44HL 2.1G BGA 813P	AMD
A10-5745M Quad-Core,FP2(Group B),25W,Richland APU R3_ROH(Production)_HD 8610G		缺 DPN		AMD

Power Sequence of APU

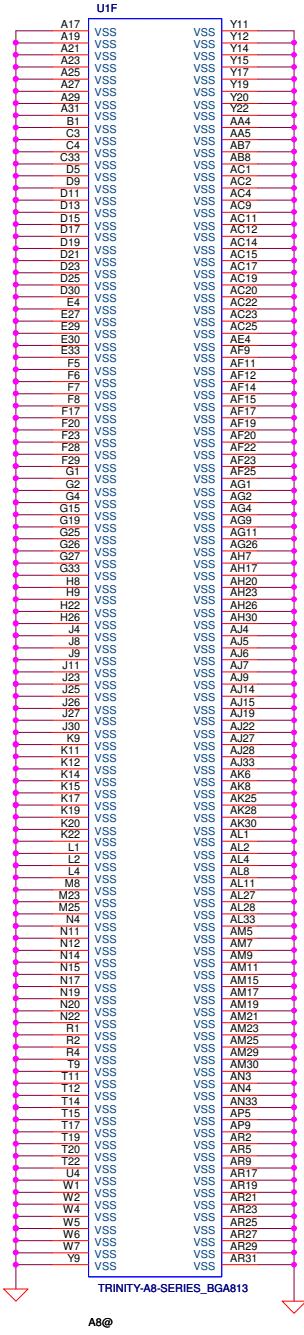
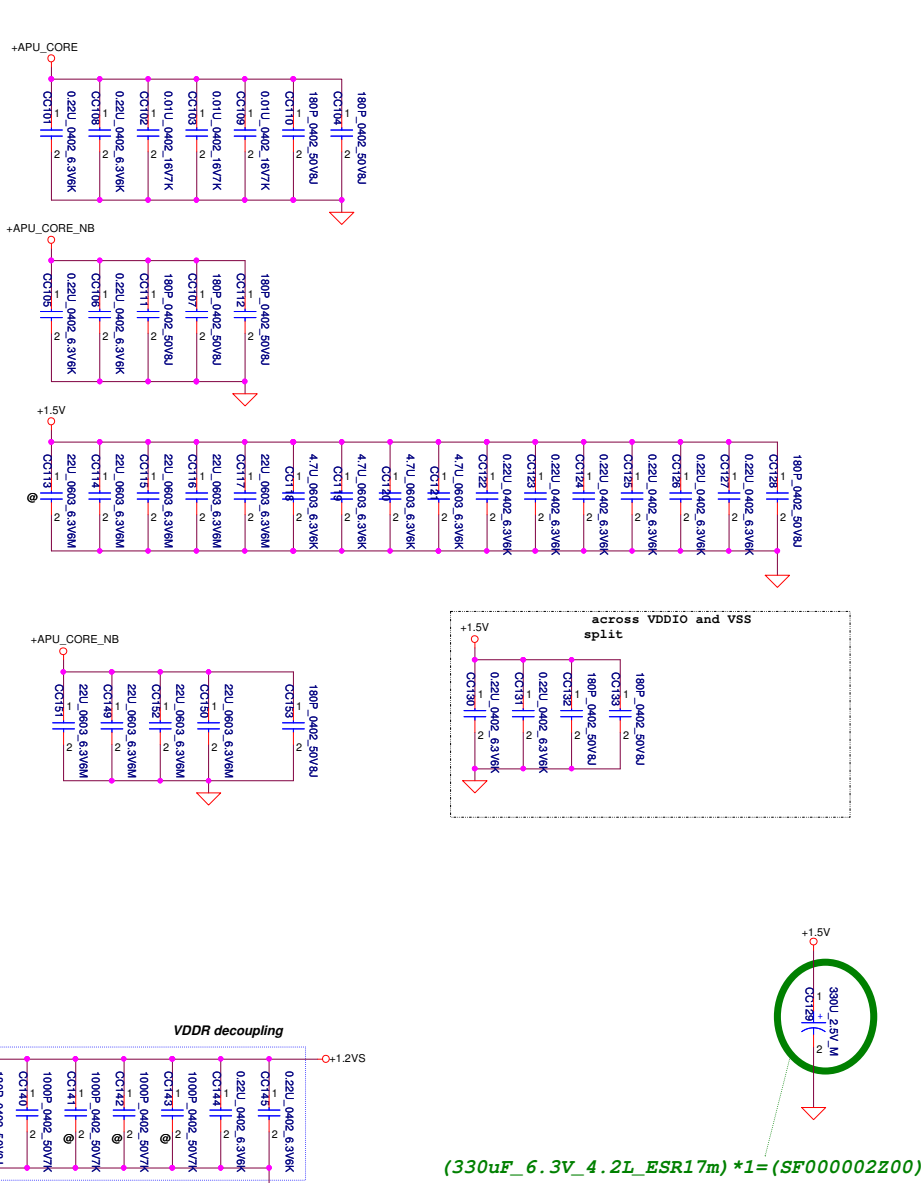
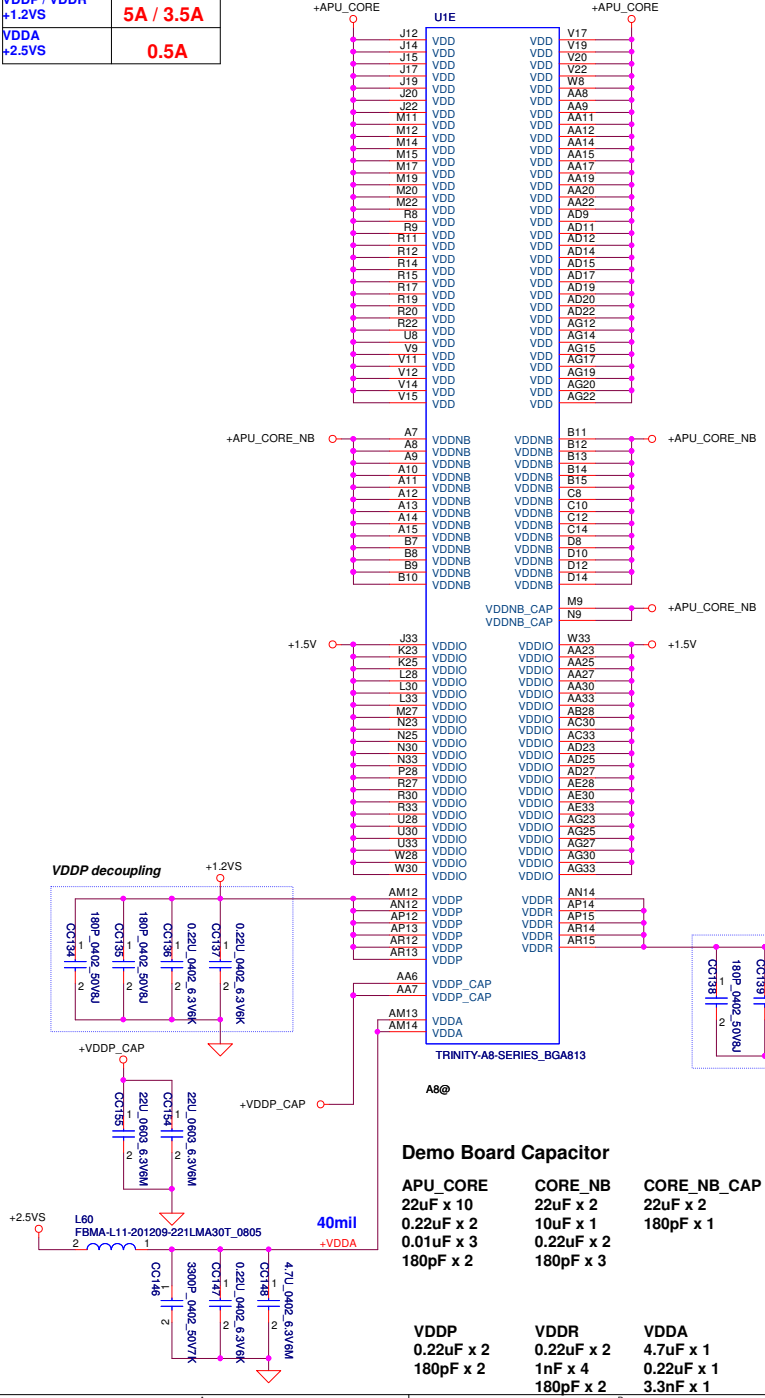


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						Document Number		LA-9103P		Rev	
						Custom				1.0	
						Date		Wednesday, July 10, 2013		Sheet 6 of 52	

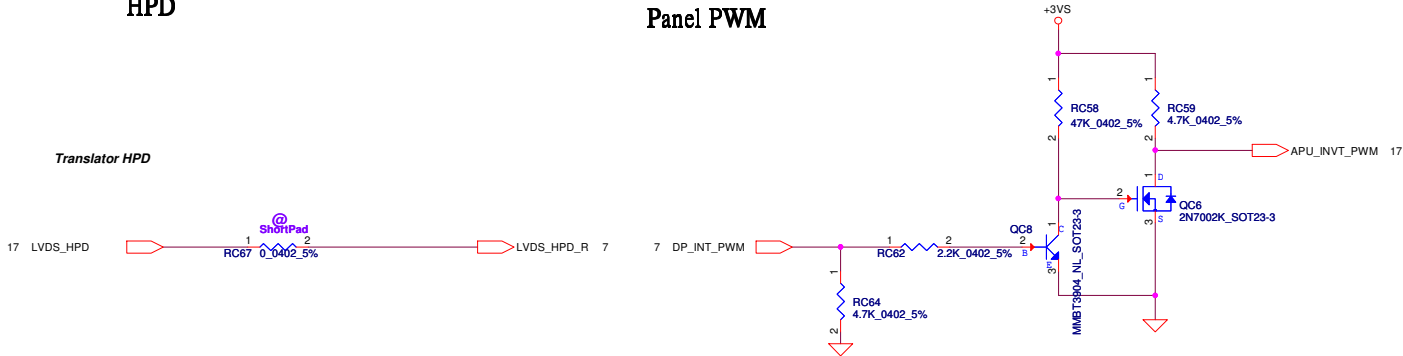
Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	29A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



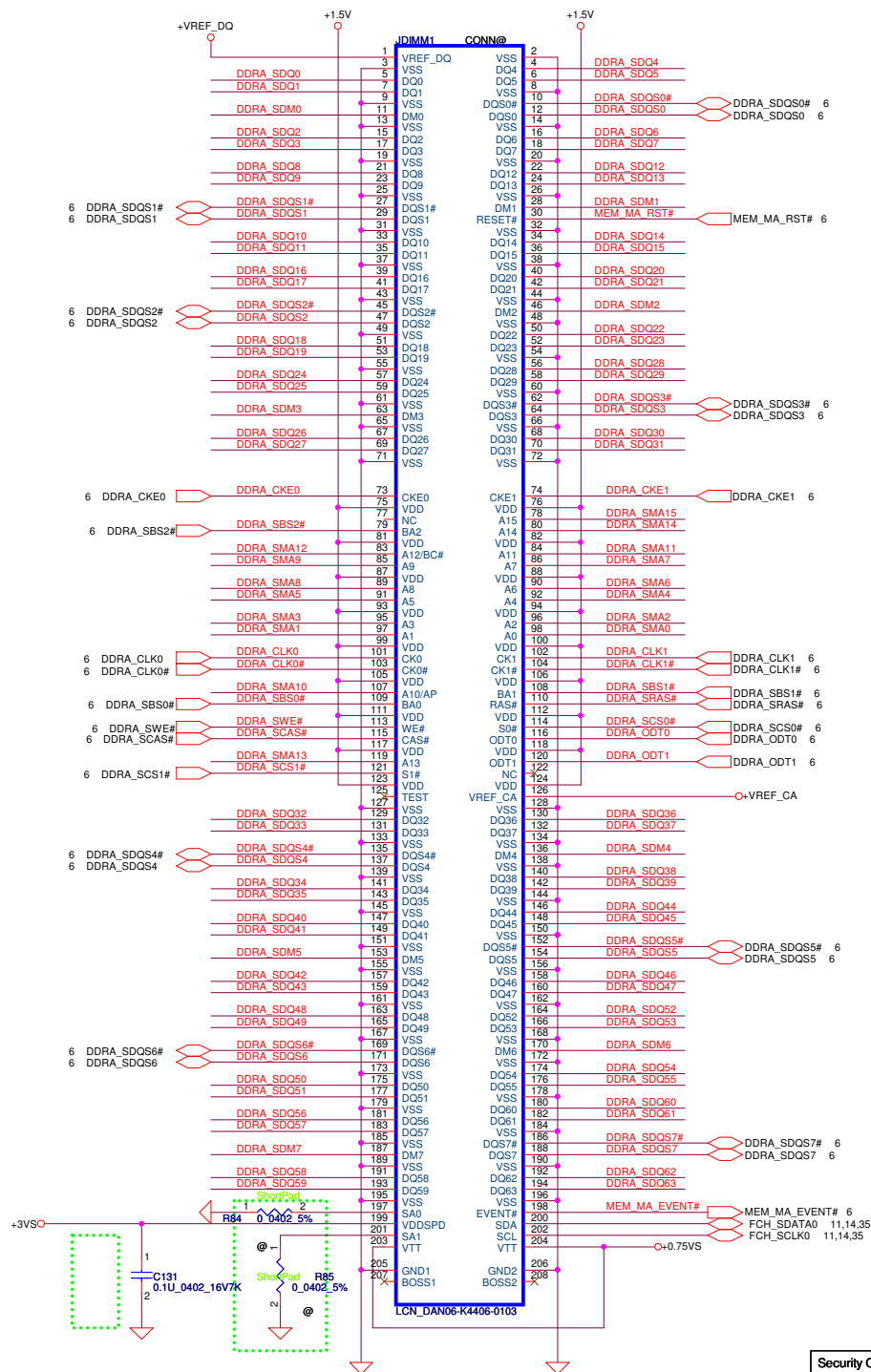
HPD

Panel PWM

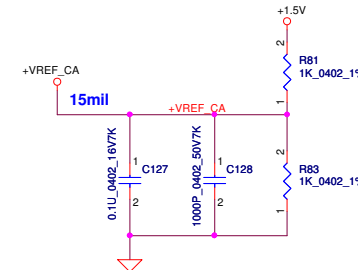
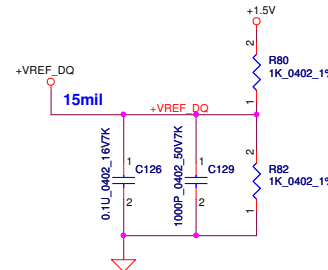
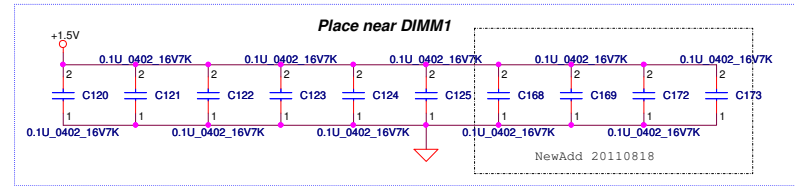
Translator HPD



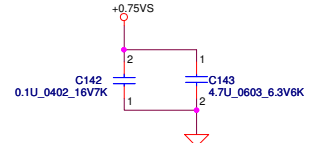
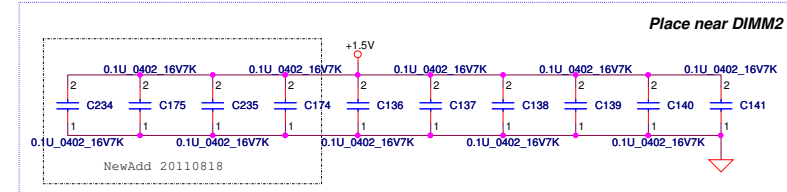
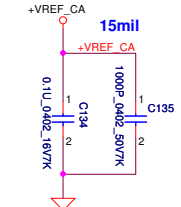
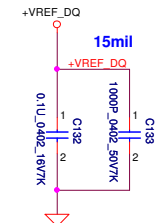
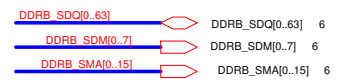
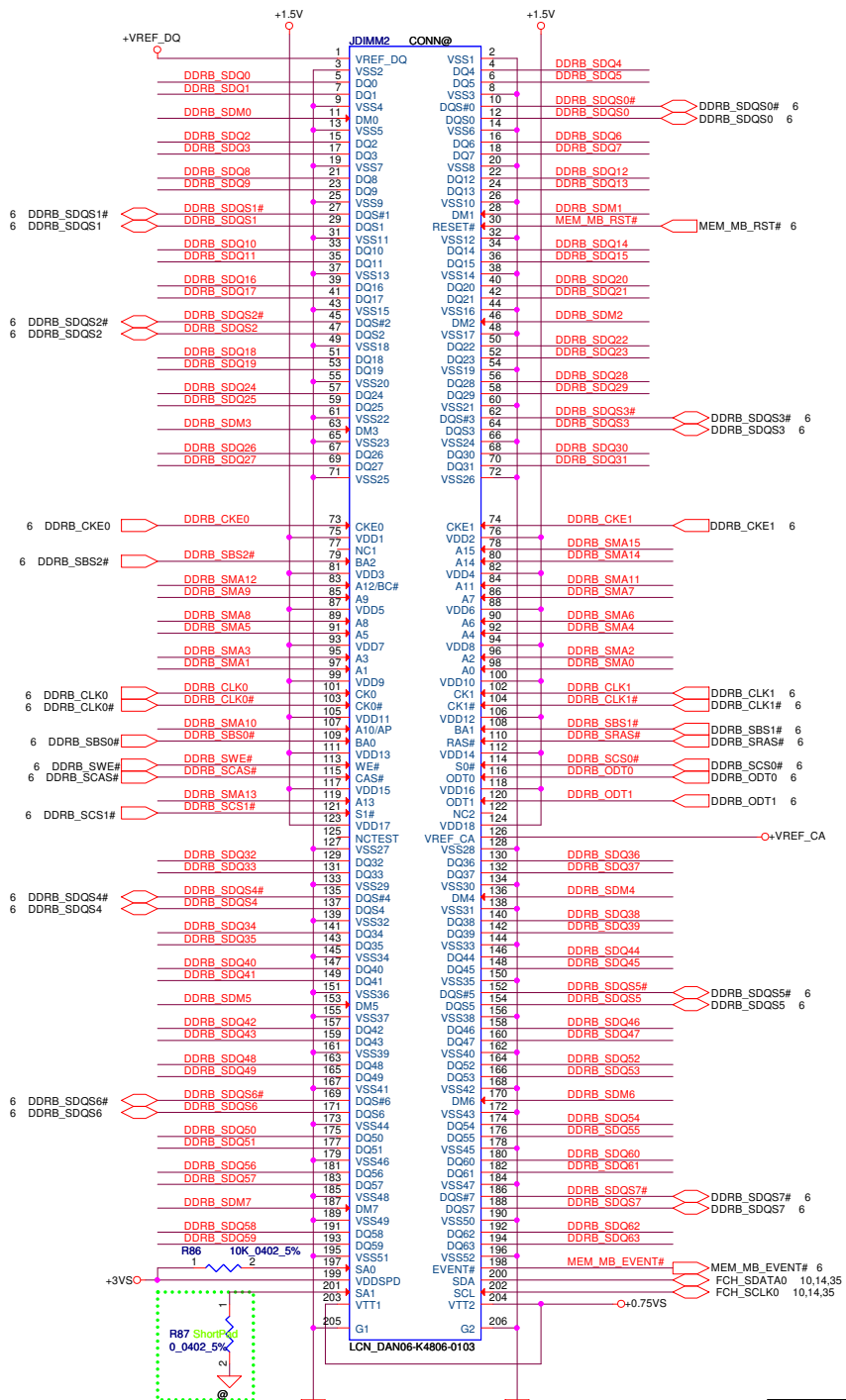
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DDR_A_SQ[0..63] 6
 DDR_A_SDM[0..7] 6
 DDR_A_SMA[0..15] 6



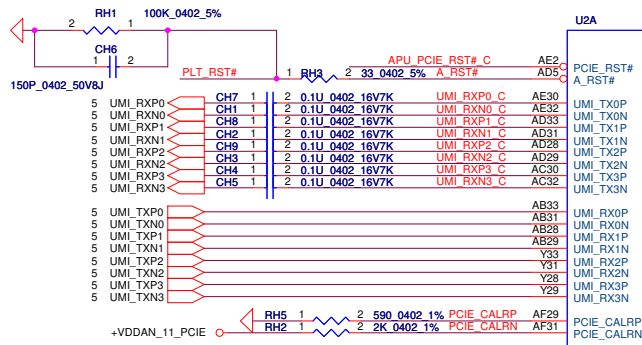
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								Document Number		LA-9103P		Rev		1.0	
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Reserve H:8mm
<Address: 01>

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R90/ C146 close to FCH



Move PCIe device to APU. 20110819

SS

NSS

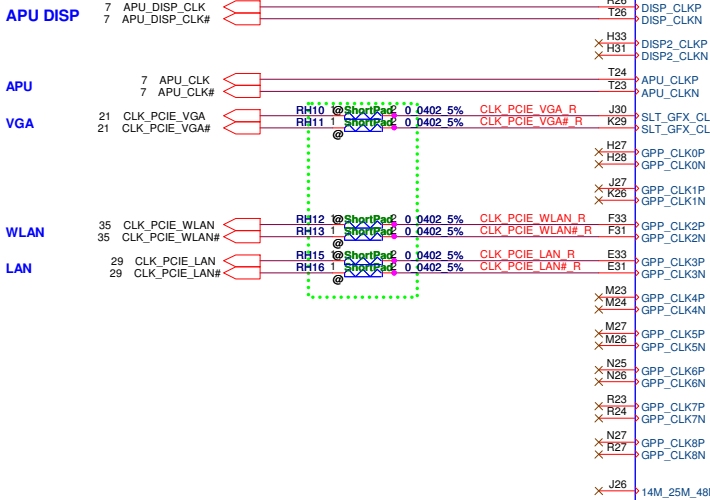
APU

VGA

WLAN

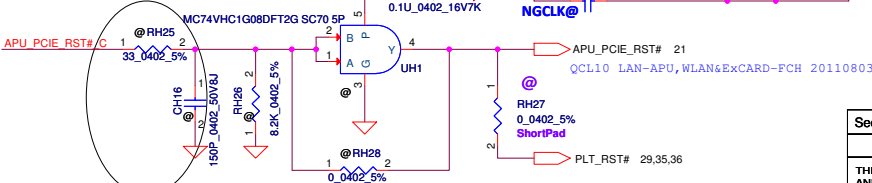
LAN

For "EXT" CLK mode, input to PCIe,



For PCIe device reset on FS1 (GFX,LAN,WLAN,LVDS Travis)

APU_PCIE_RST# : Reset PCIe device on APU



R692/ C790 close to FCH

U2A

HUDSON-2

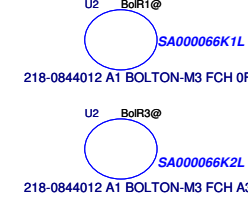
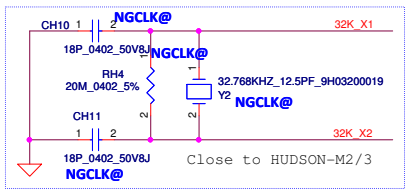
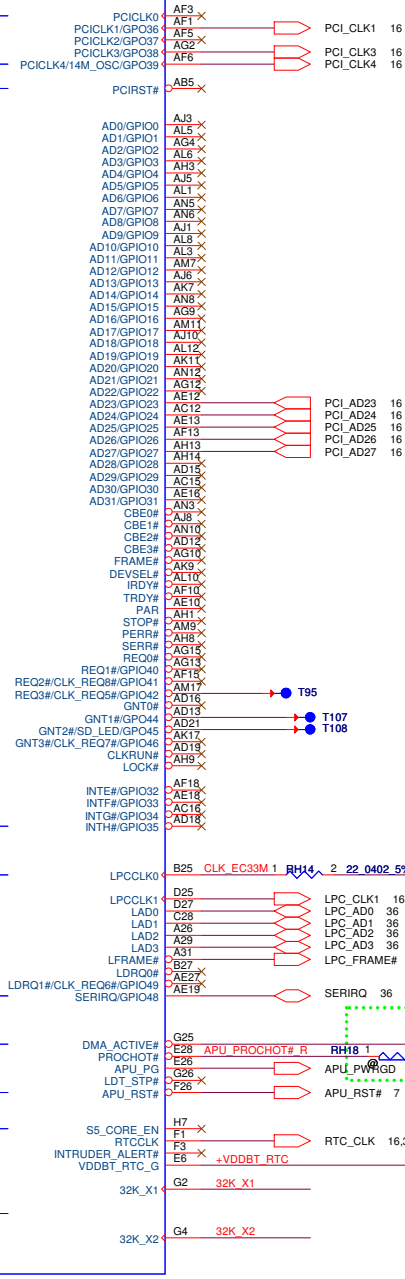
PCI EXPRESS INTERFACES

PCI INTERFACE

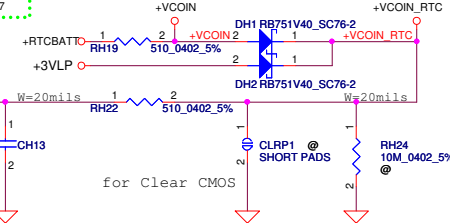
CLOCK GENERATOR

APU

SS PLUS

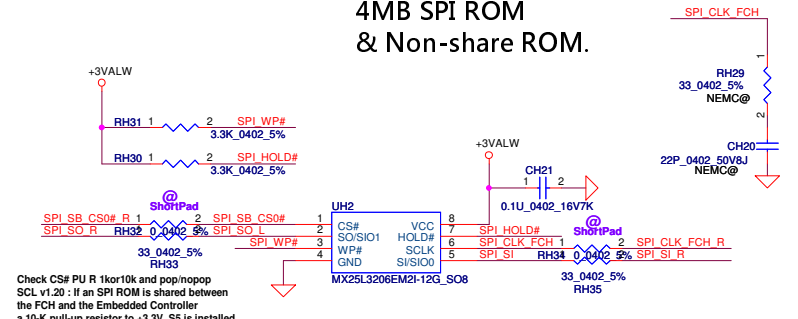
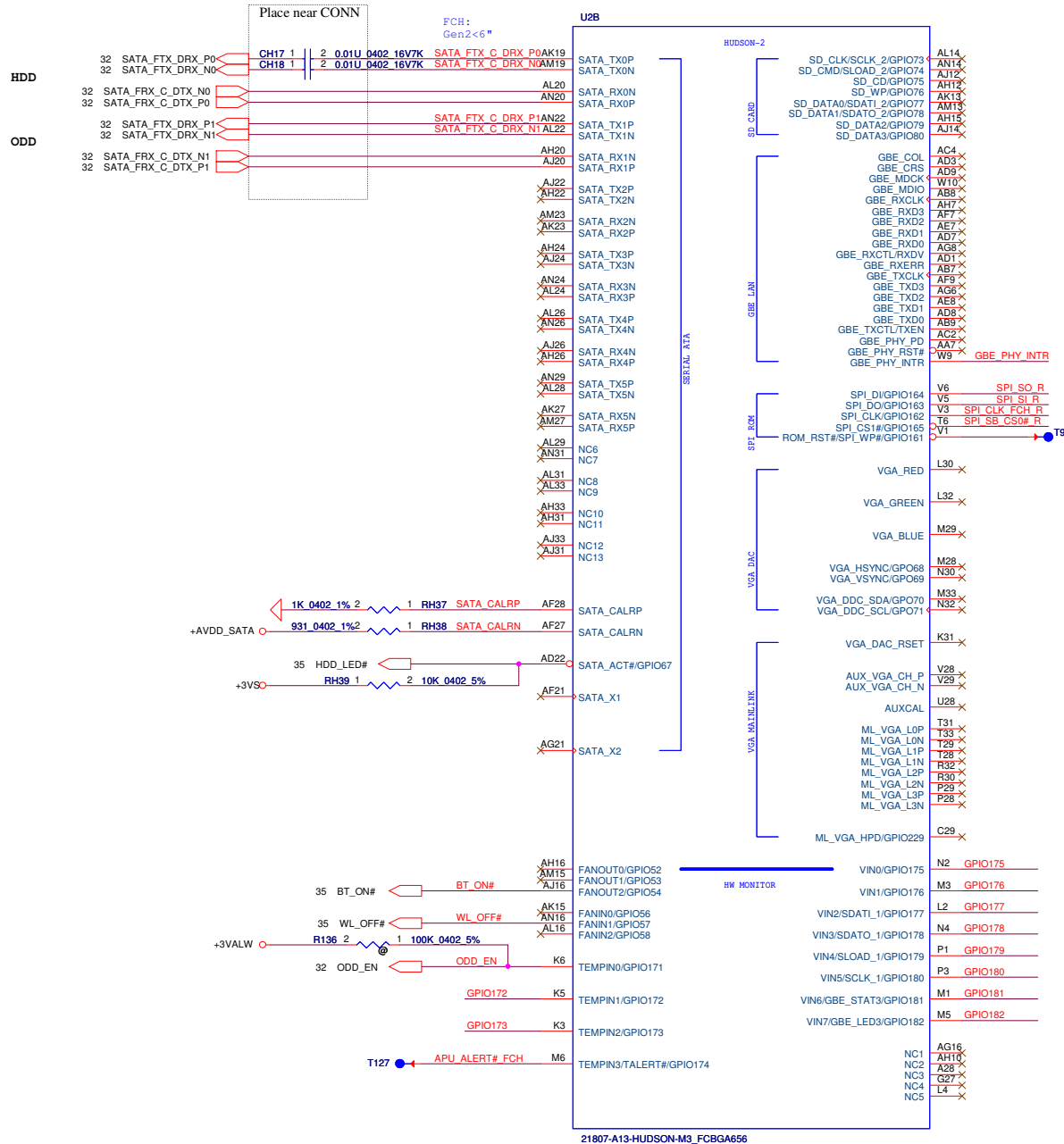


APU_PG/APU_RST#/LDT_STP# : OD pin DMA_ACTIVE# : IN/OD, 0.8V threshold PROCHOT# : IN, 0.8V threshold LDT_STP : No use, NC DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.



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4MB SPI ROM & Non-share ROM.

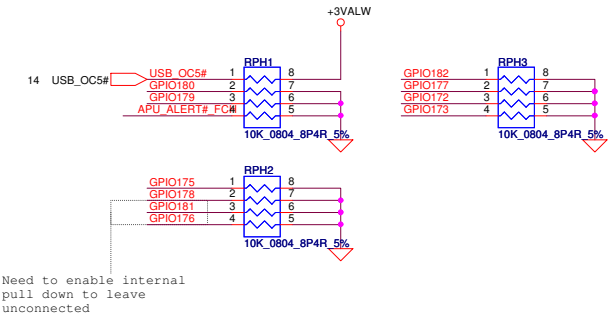


Check CS# PU R 1k or 10k and pop/nopop
SCL v1.20 : If an SPI ROM is shared between
the FCH and the Embedded Controller
a 10-K pull-up resistor to +3.3V_S5 is installed.

GBE_PHY_INTR
Pulled-up to +3.3V_S5 with a 10-K 5% resistor.
FCH SCL v1.20 #19-85

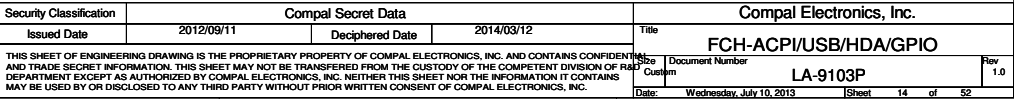
GBE_PHY_INTR RH36 1 2 10K 0402 5%

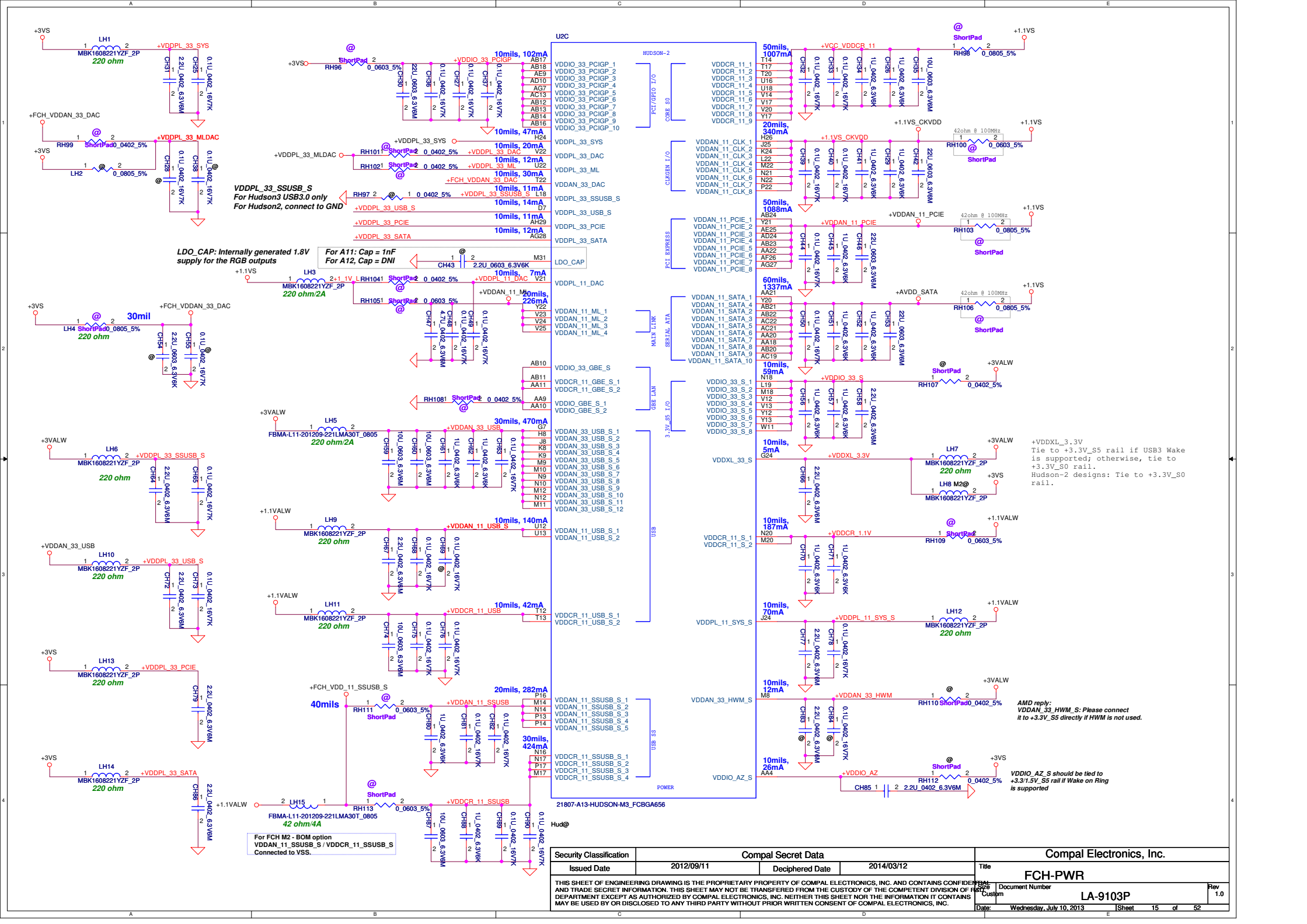
Removed RGMII/MII support and updated termination
requirements for GBE_COL, GBE_CRS, GBE_RXERR
and GBE_MDIO when RGMII/MII interface is not used.
FCH DGv1.20 / SCL v1.20



Need to enable internal
pull down to leave
unconnected

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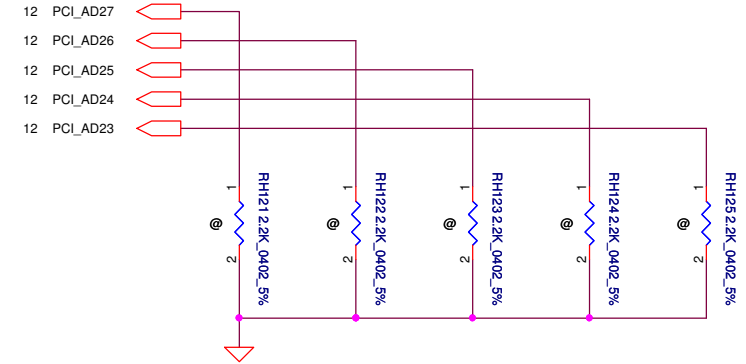
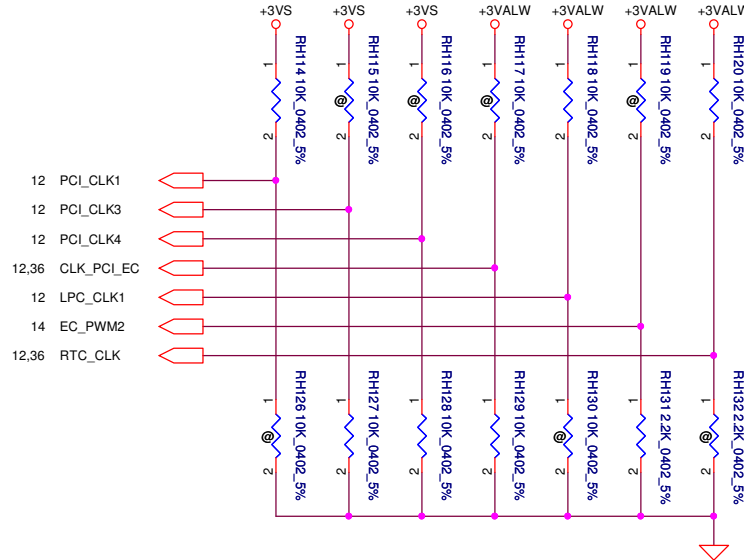
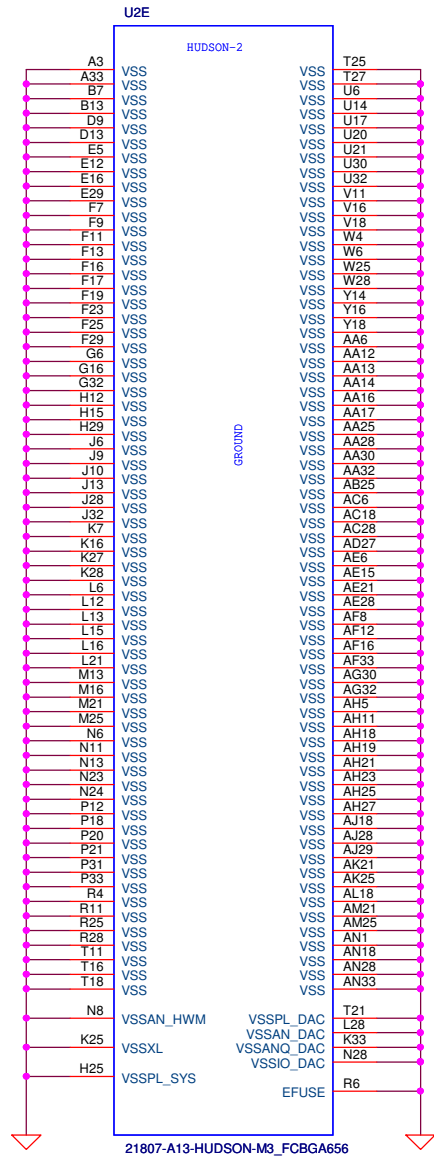
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

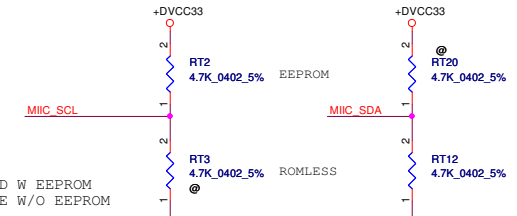
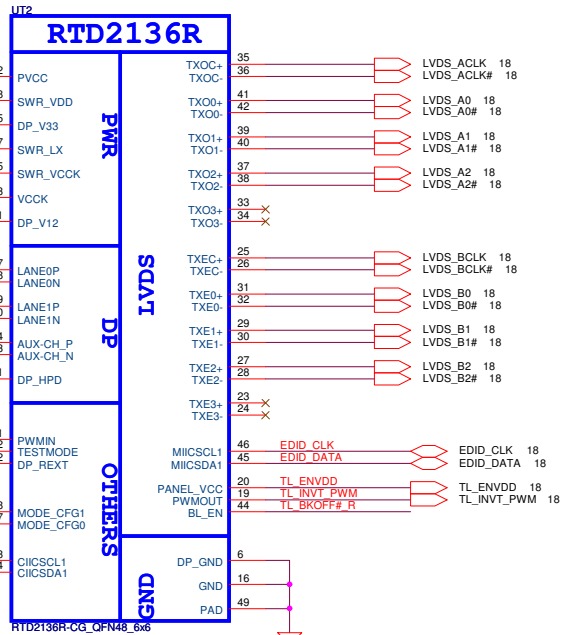
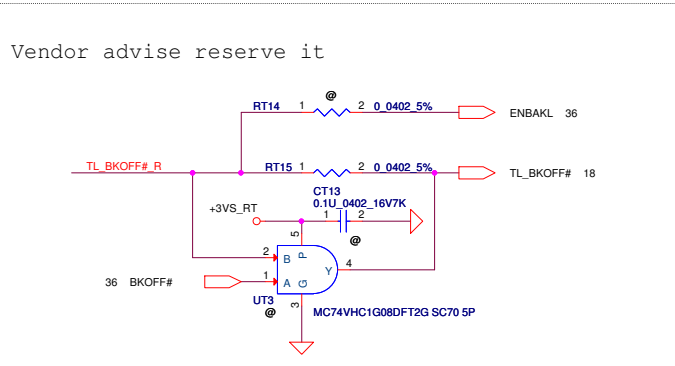
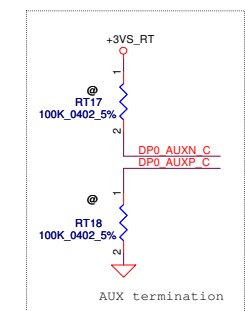
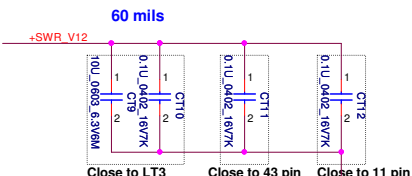
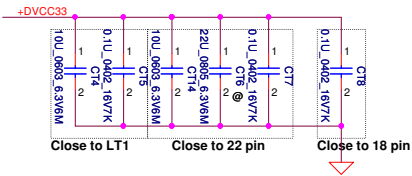
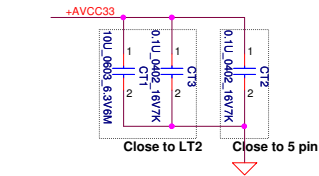
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PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



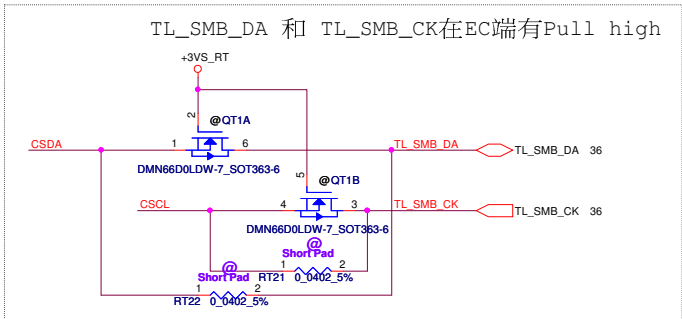
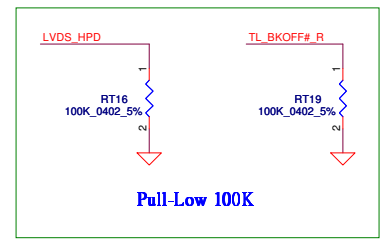
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					Date:	Wednesday, July 10, 2013	Sheet 16 of 52

Power Consumption:

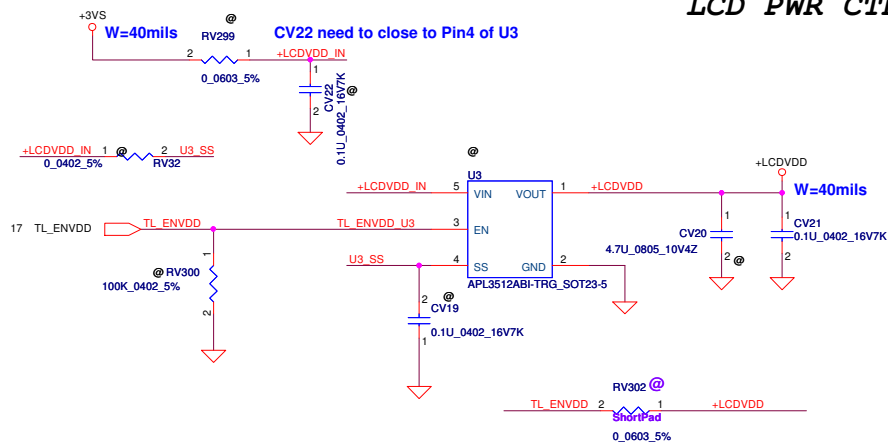
Pin22 (DPV33) < 20mA
 Pin 11 (DP_V12) < 100mA
 Pin 15 (SWR_VCKK) < 100mA (layout trace > 60 mil)
 Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
 Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
 Pin 22 (PVCC) < 50 mA
 Pin 43 (VCKK) < 50mA



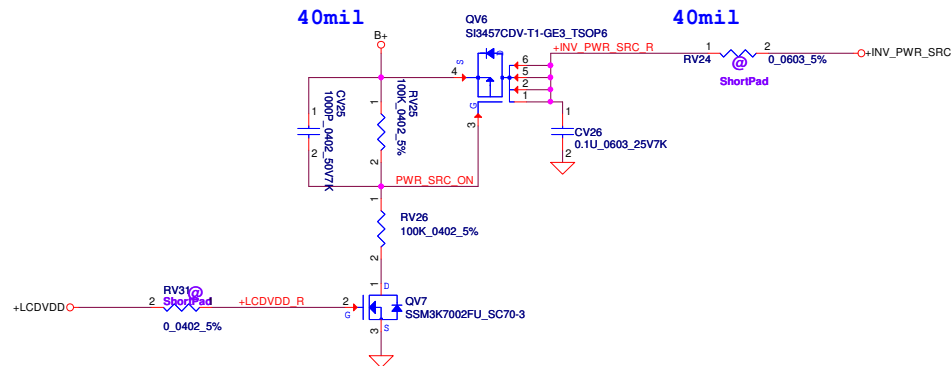
		Pin47 MIIC_SDA	
		0	1
Pin48 MIIC_SCL	0	x	EP MODE
	1	ROM	EEPROM



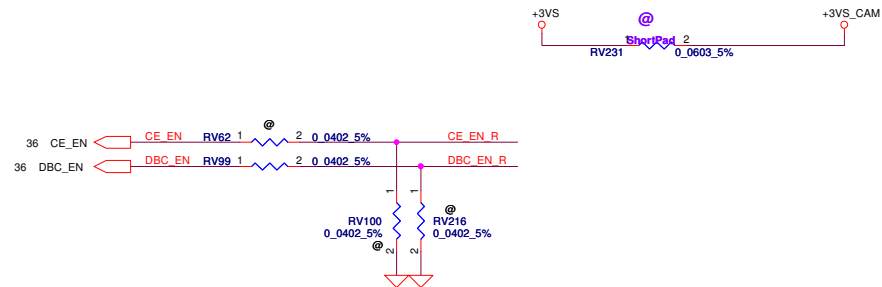
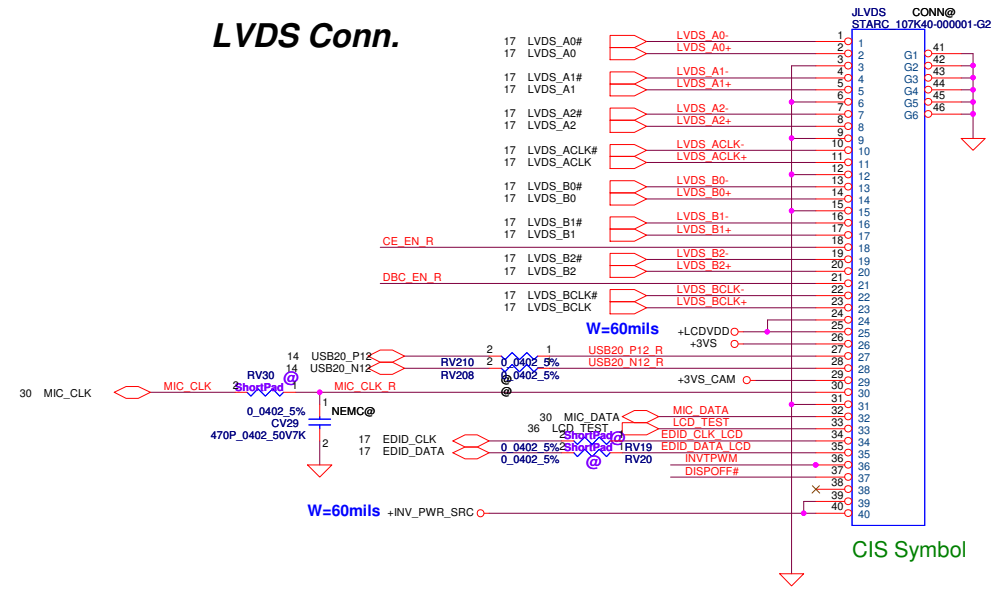
LCD PWR CTRL



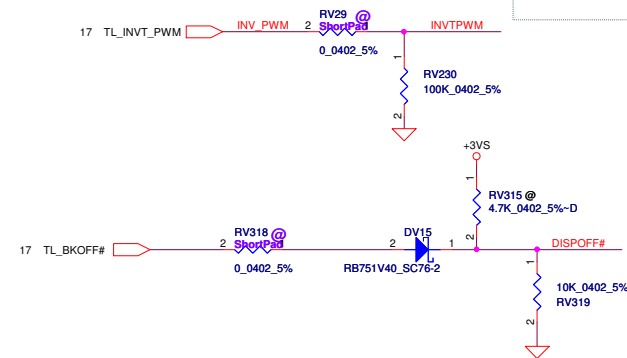
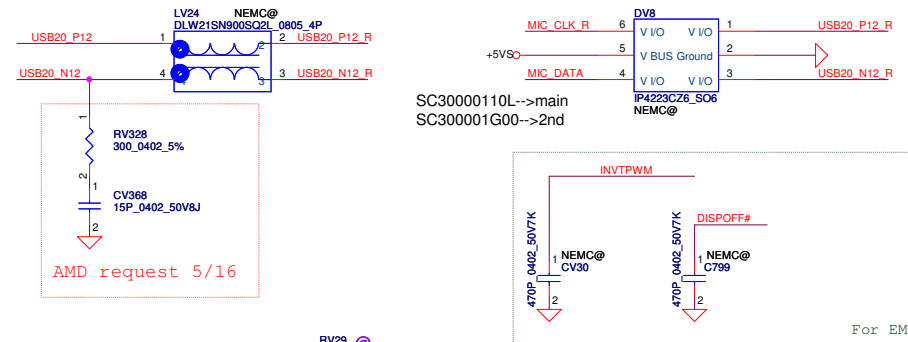
LCD backlight PWR CTRL



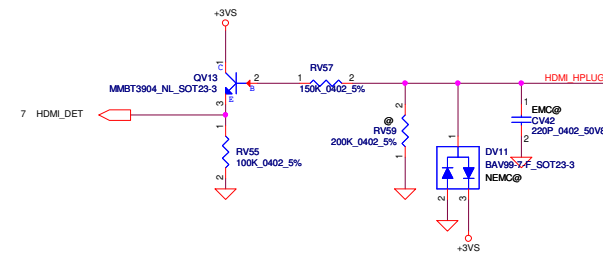
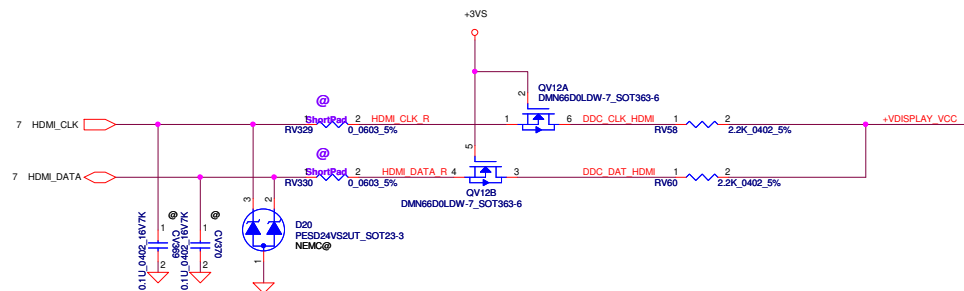
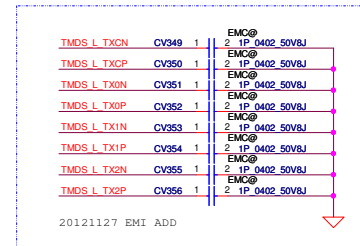
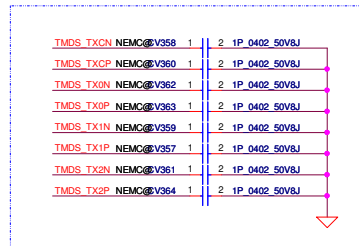
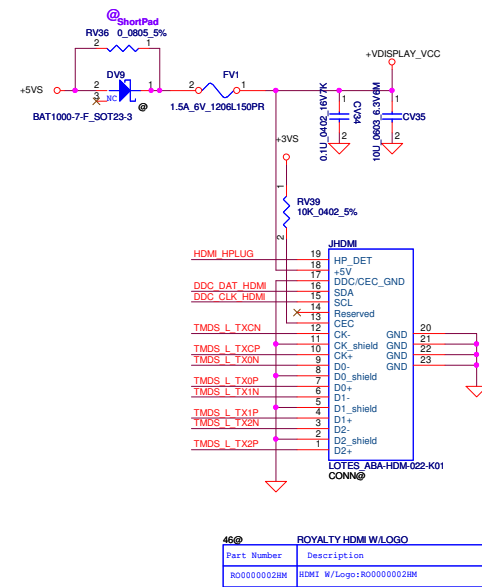
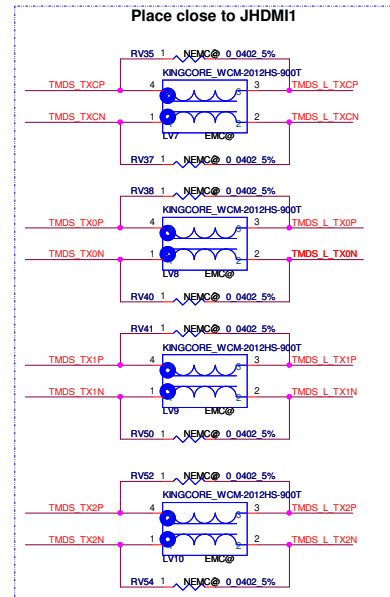
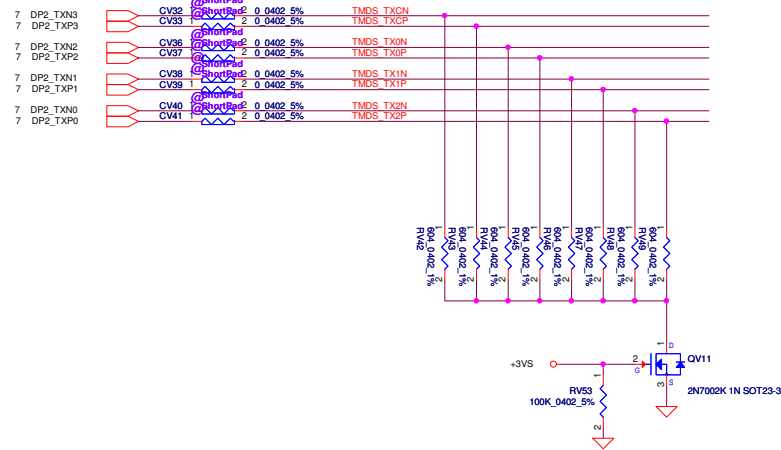
Wedcam PWR CTRL

**LVDS Conn.**

* Reserved for EMI/ESD/RF
need to close to JLVDS



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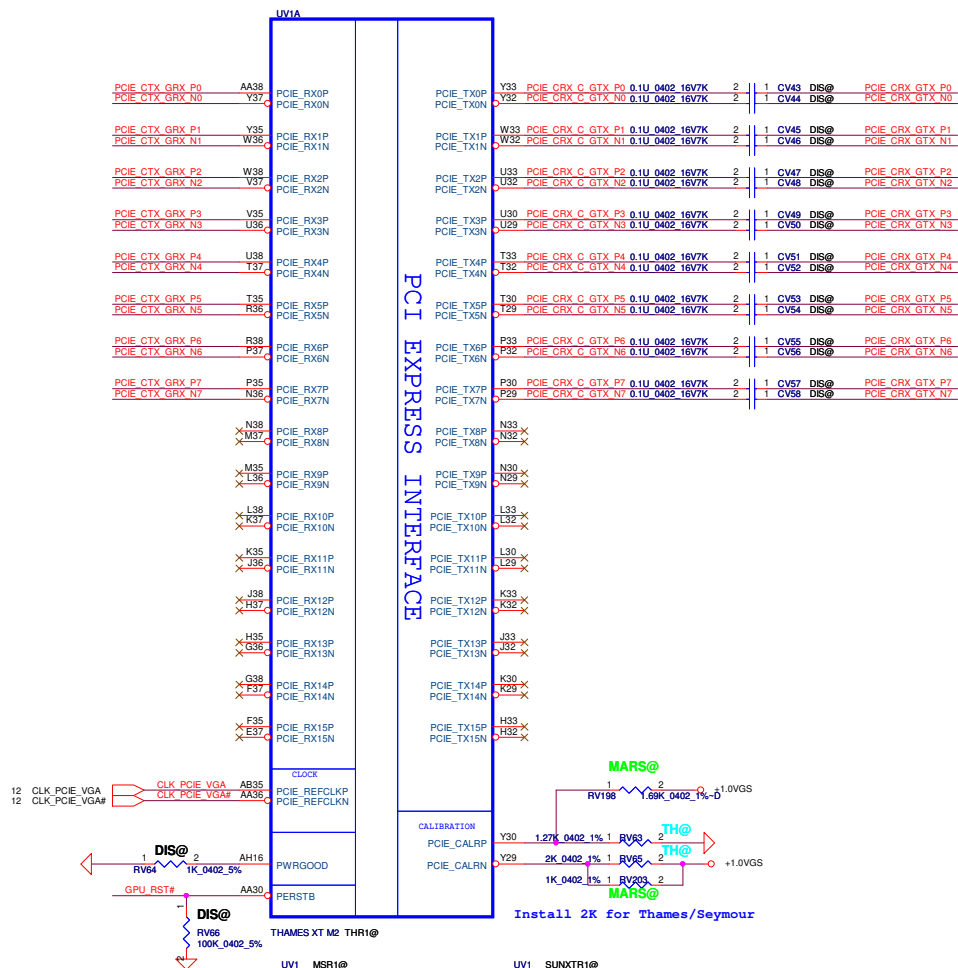


CV365, CV367
Please close APU side

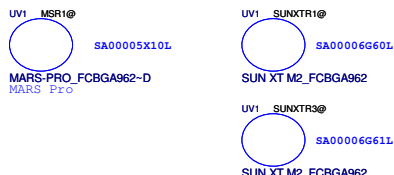
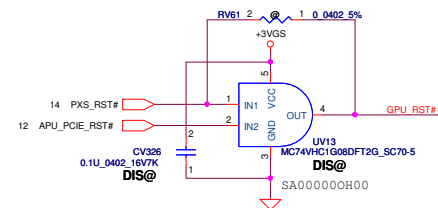
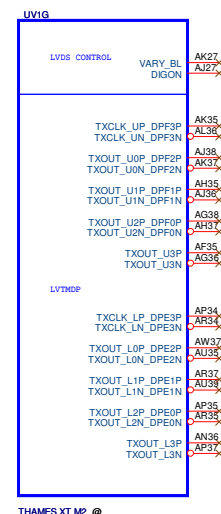
5 PCIE_CTX_GRX_P[7..0] PCIE_CTX_GRX_P[7..0]
5 PCIE_CTX_GRX_N[7..0] PCIE_CTX_GRX_N[7..0]

GFX PCIE LANE REVERSAL

PCIE_CRX_GTX_P[7..0] PCIE_CRX_GTX_P[7..0] 5
PCIE_CRX_GTX_N[7..0] PCIE_CRX_GTX_N[7..0] 5

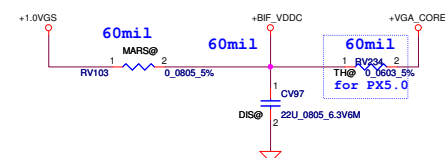
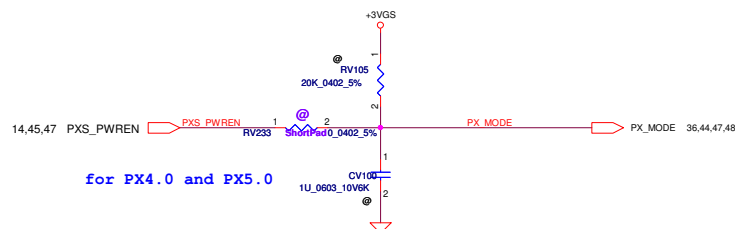


LVDS Interface

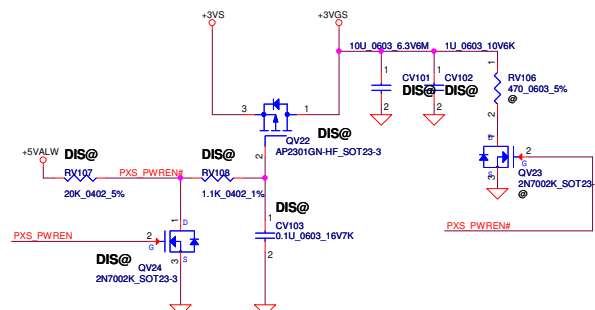


PX_MODE=0 for BACO mode to shut down power rails expcept VDDR3,PCIE_VDDC and 1.8V rail

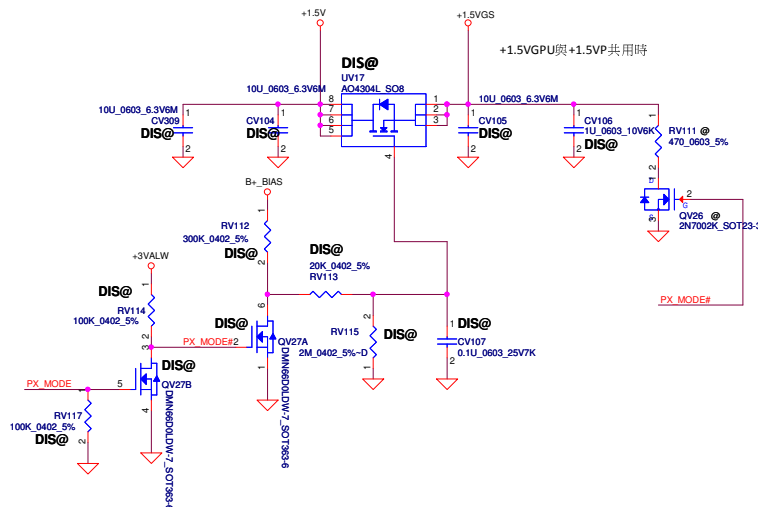
55mA@1.0V, in BACO mode



+3.3VS TO +3.3VGS

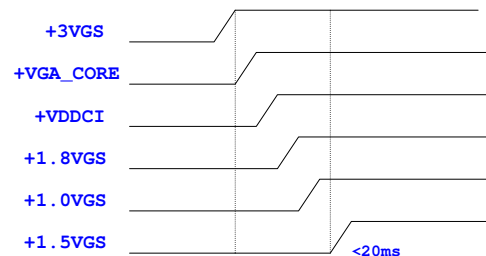


+1.5V TO +1.5VGS

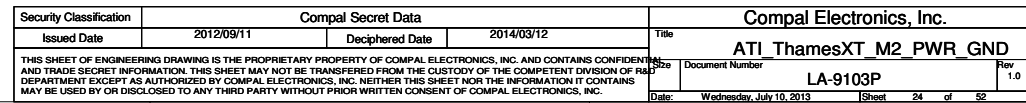


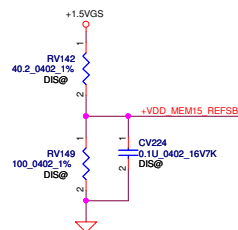
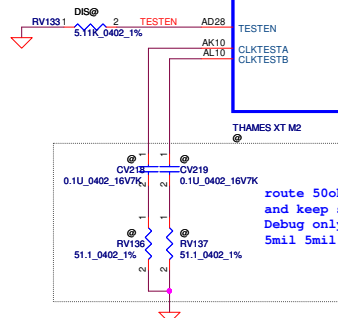
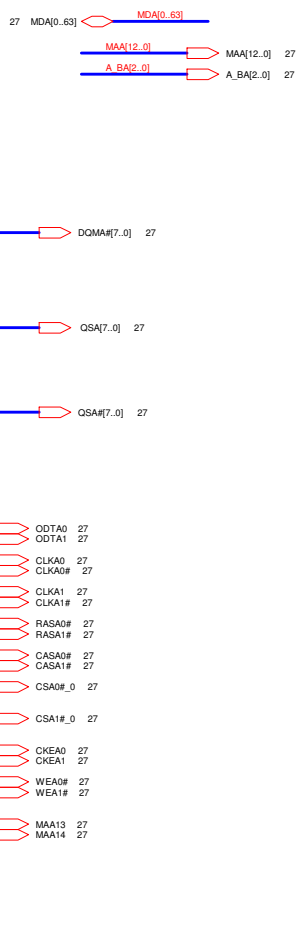
PX5.0 +3VGS,+VGA CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

Power Sequence of Thames and Chelsea



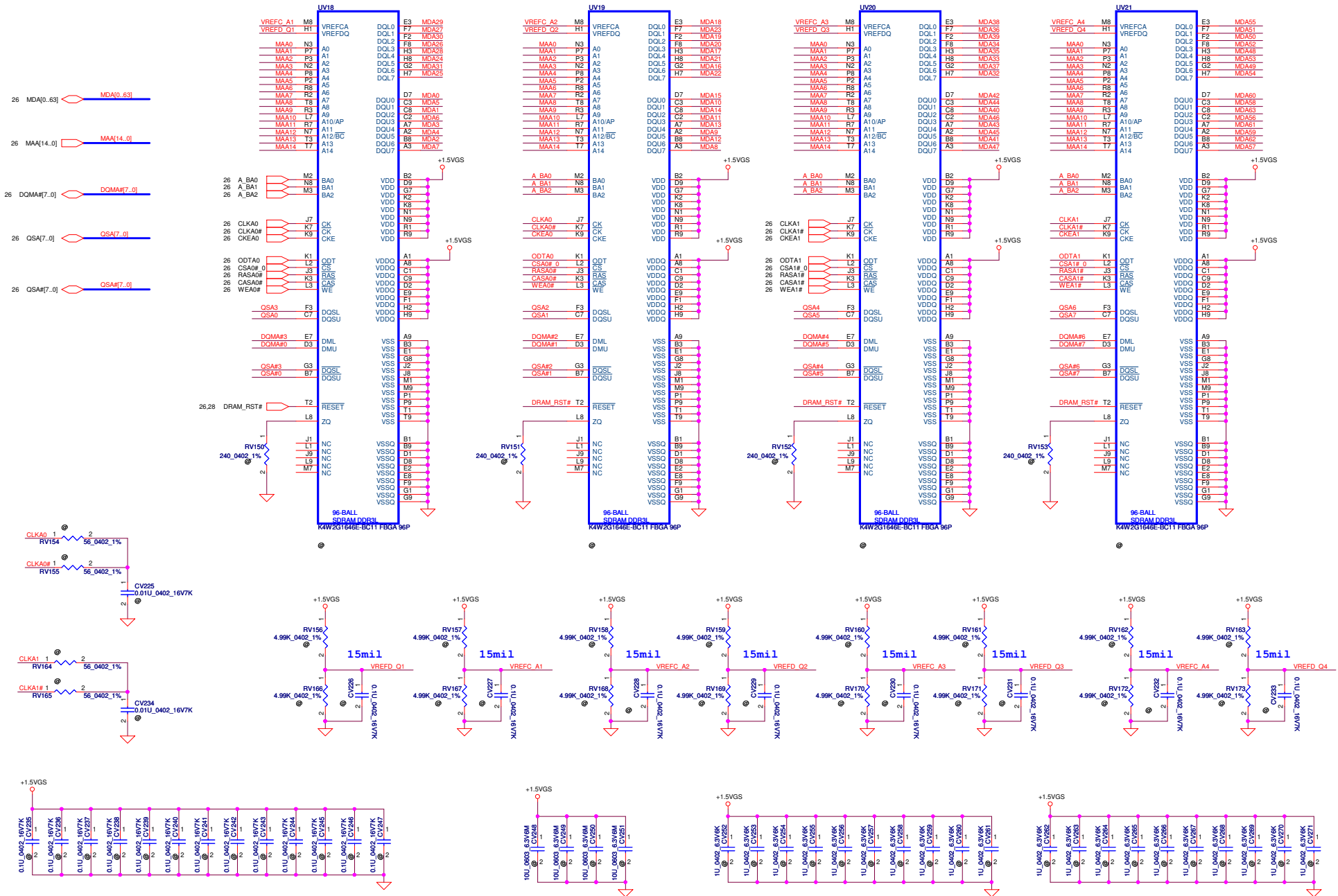
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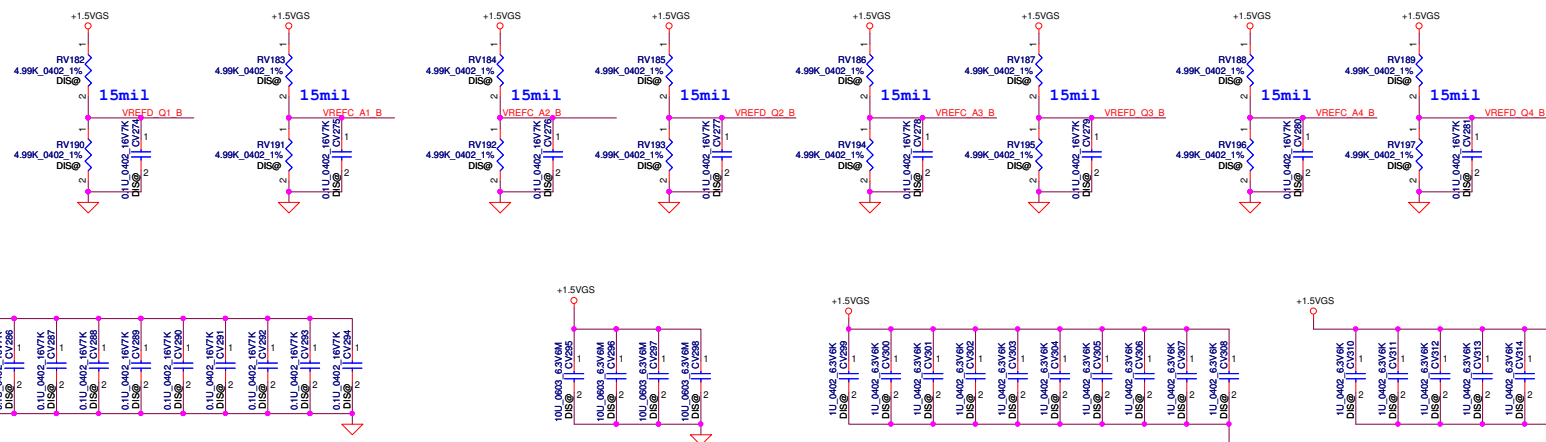
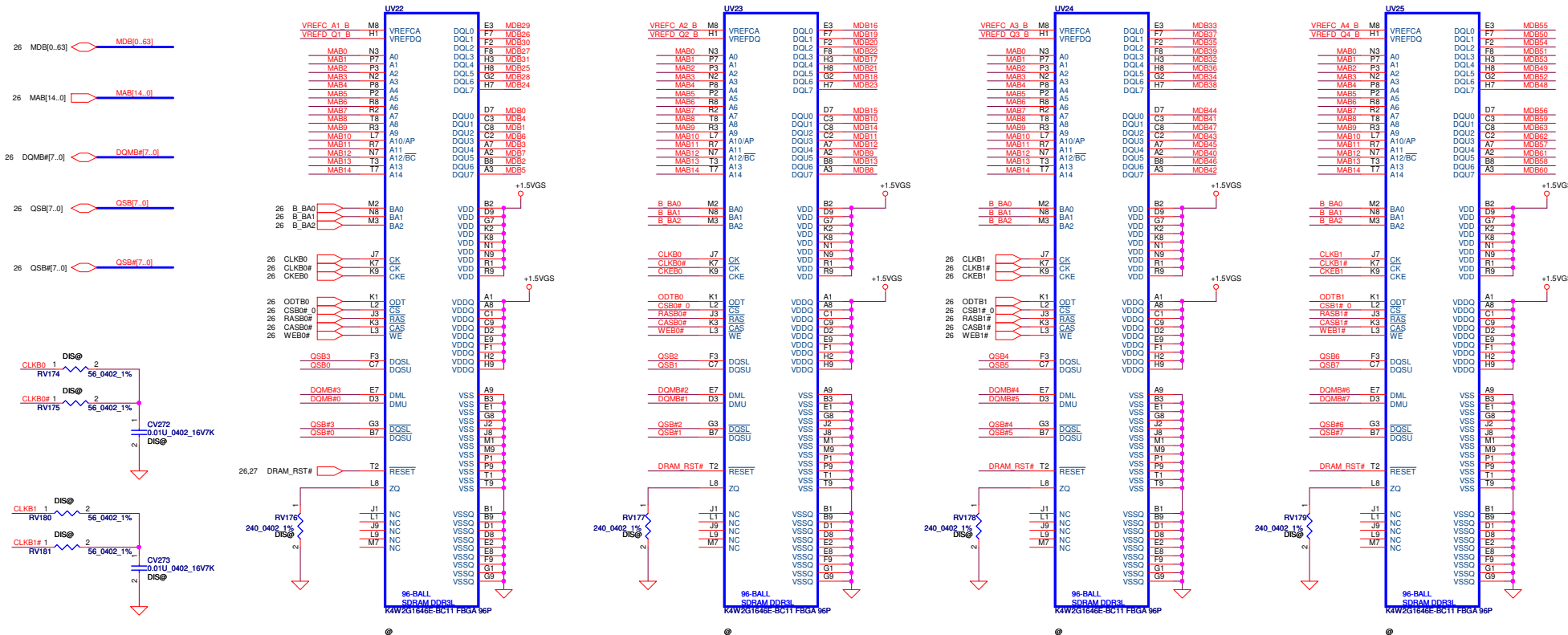
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				AT1 ThamesXT M2 MEM IF	
				Document Number LA-9103P	
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CHANNEL A: 256MB/512MB DDR3

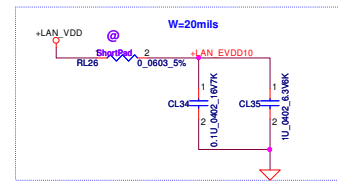
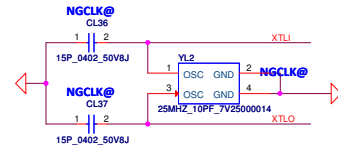
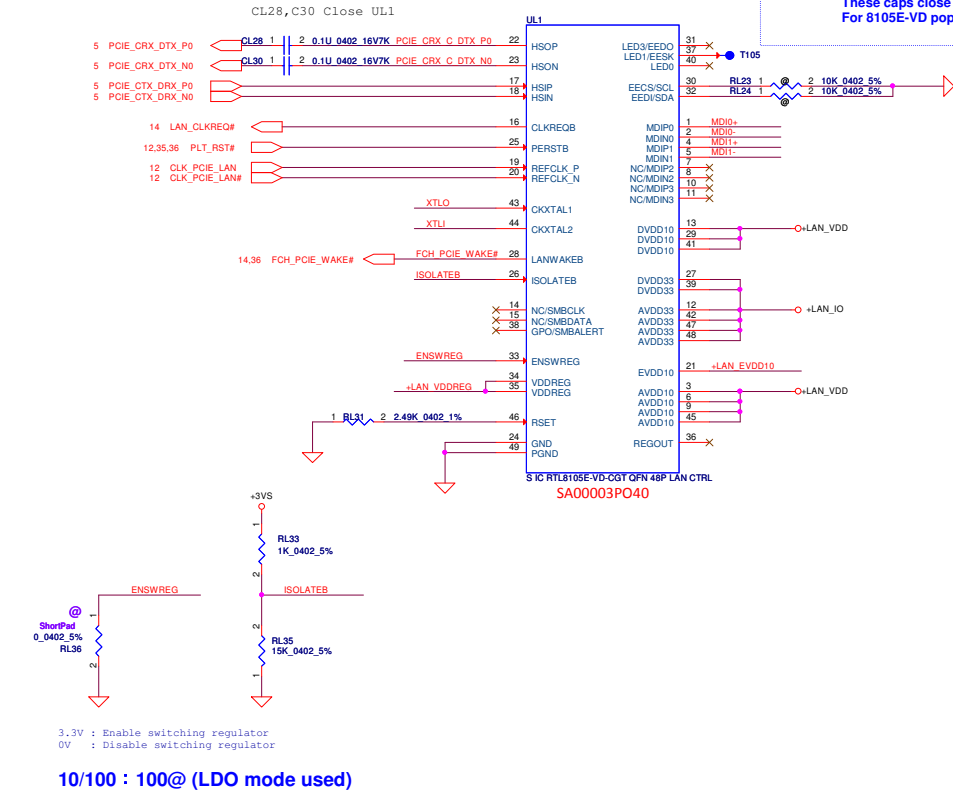
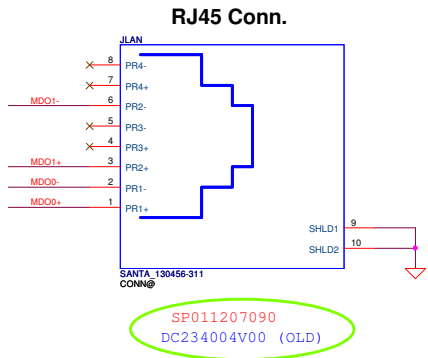
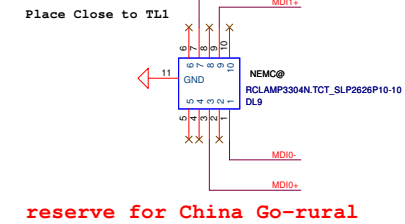
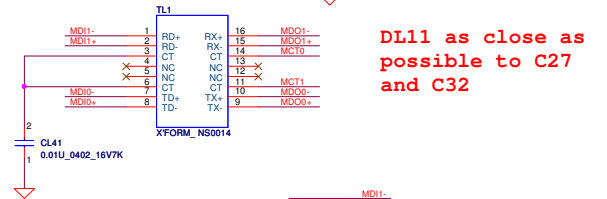
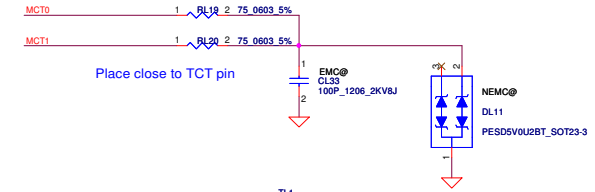
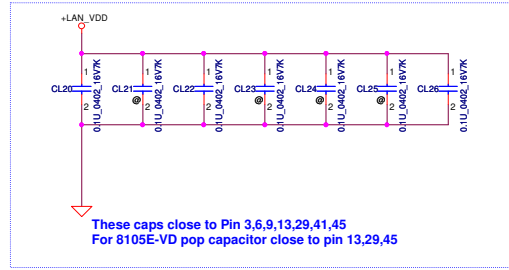
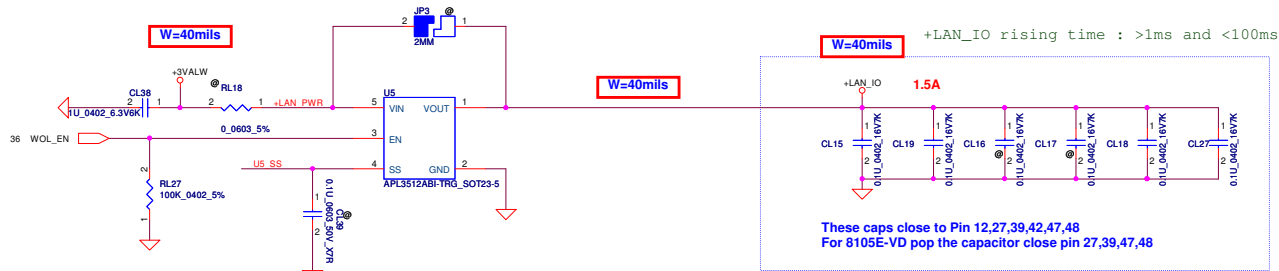


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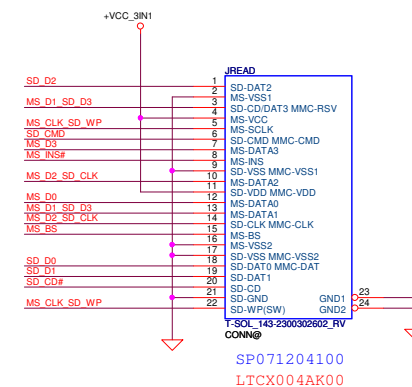
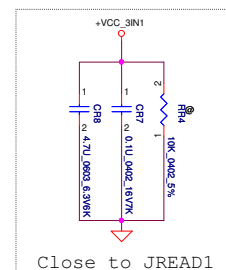
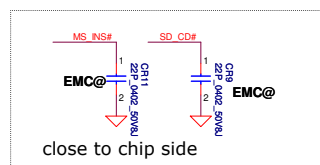
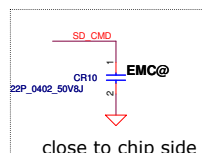
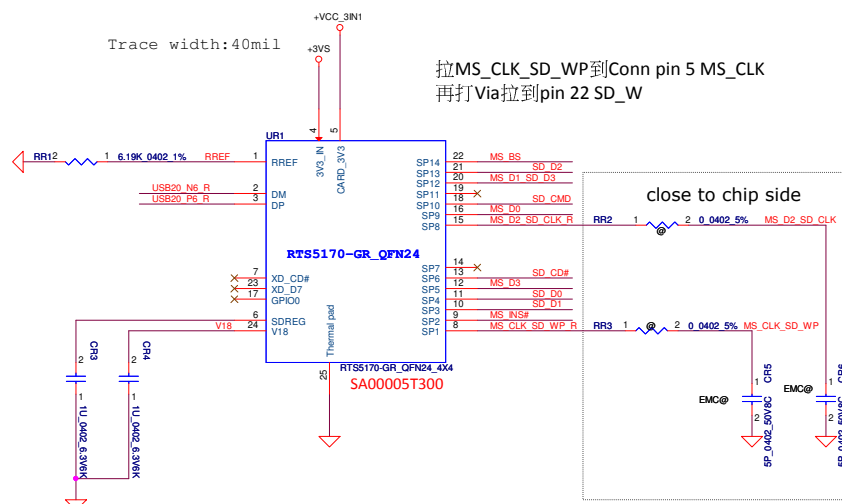
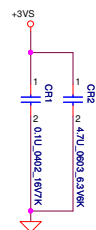
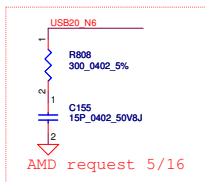
CHANNEL B: 256MB/512MB DDR3



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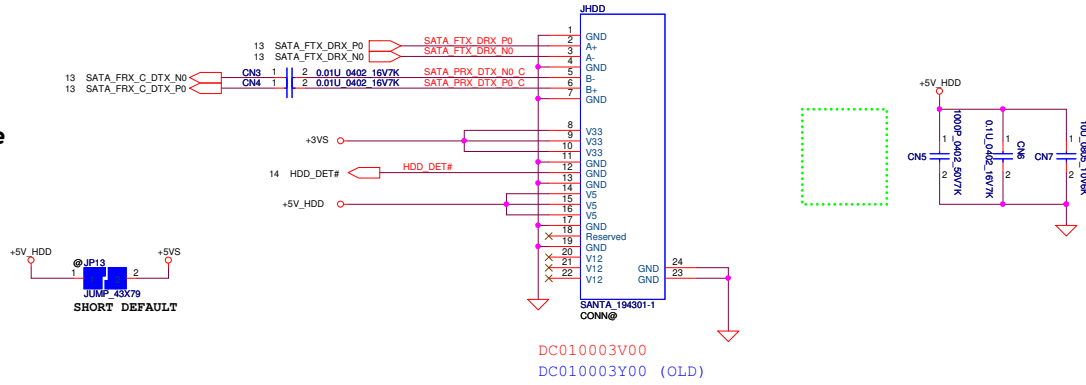


拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 22 SD_W

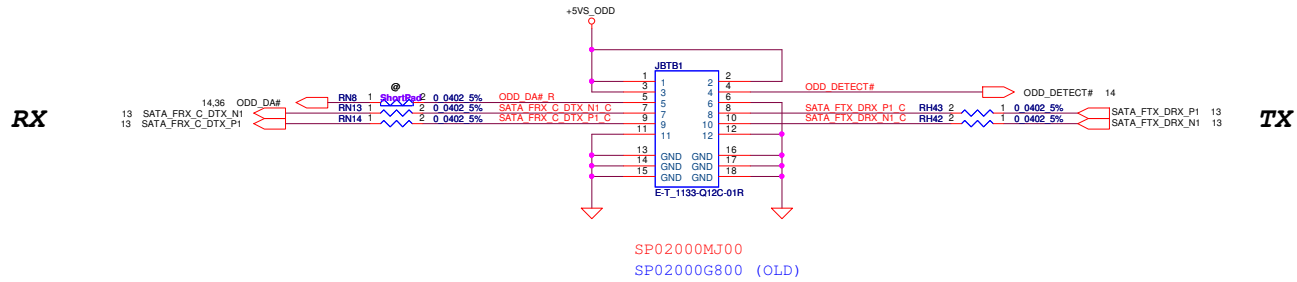
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SATA HDD Conn.

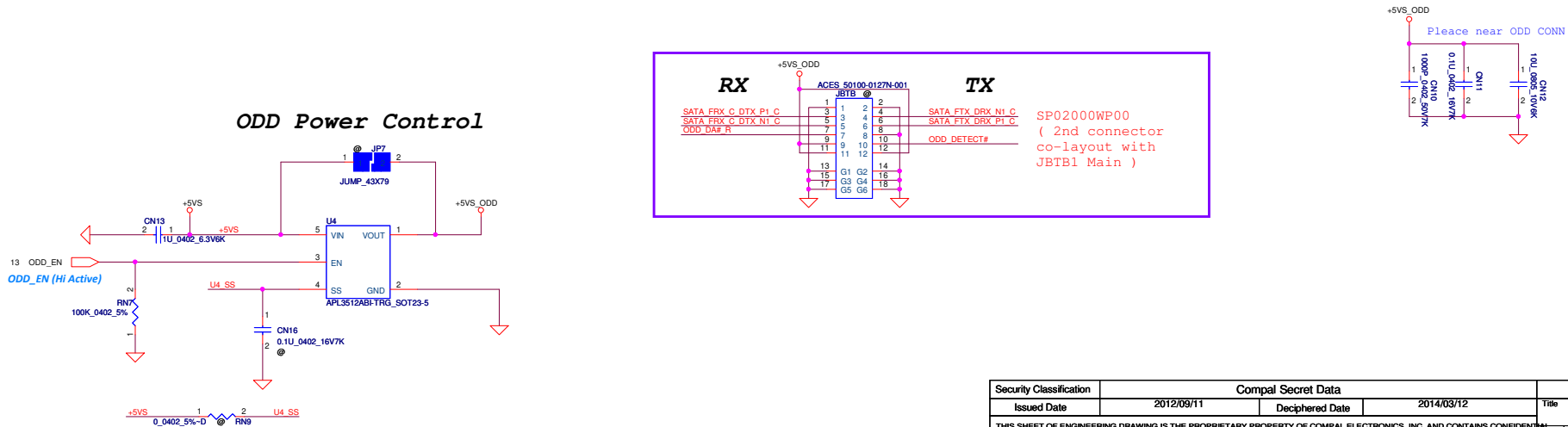
+5V_HDD Source



ODD BTB Conn.

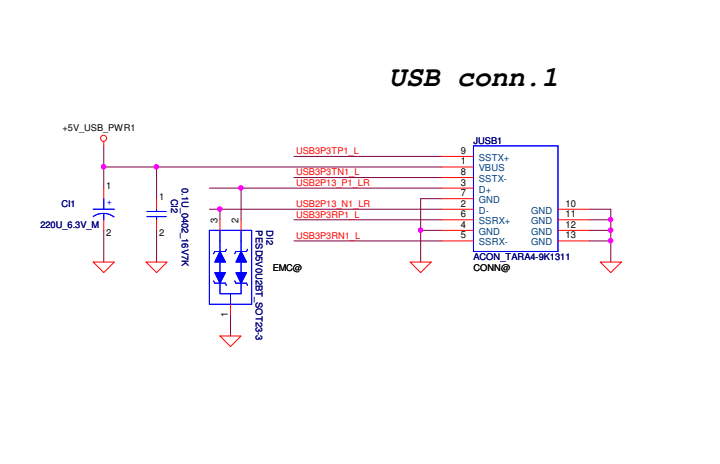
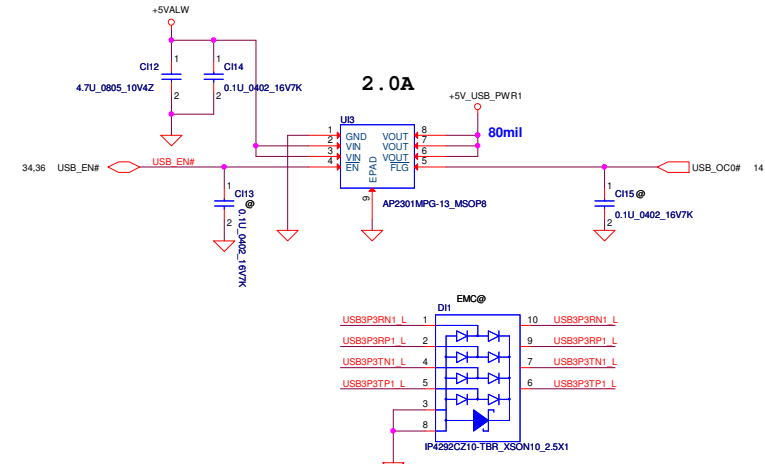
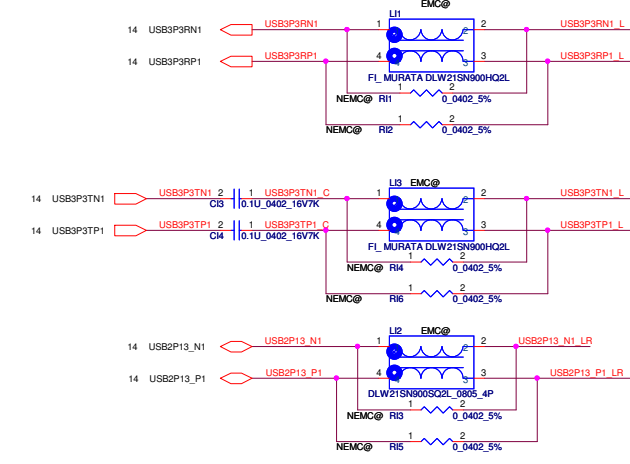


ODD Power Control

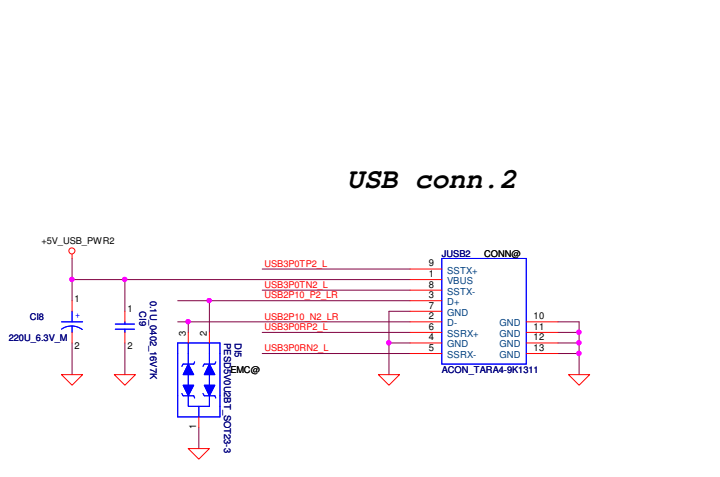
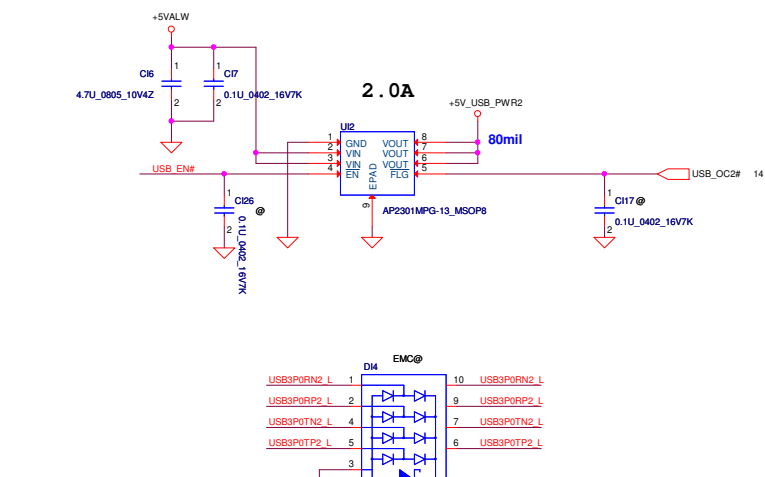
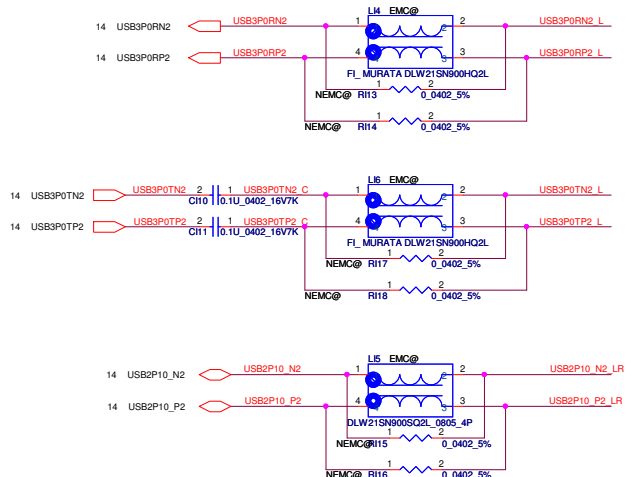


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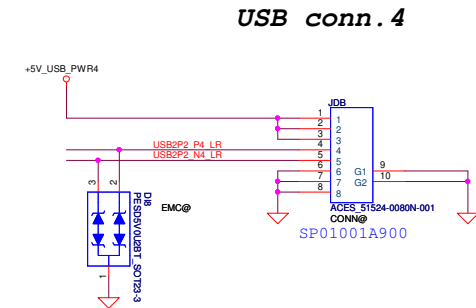
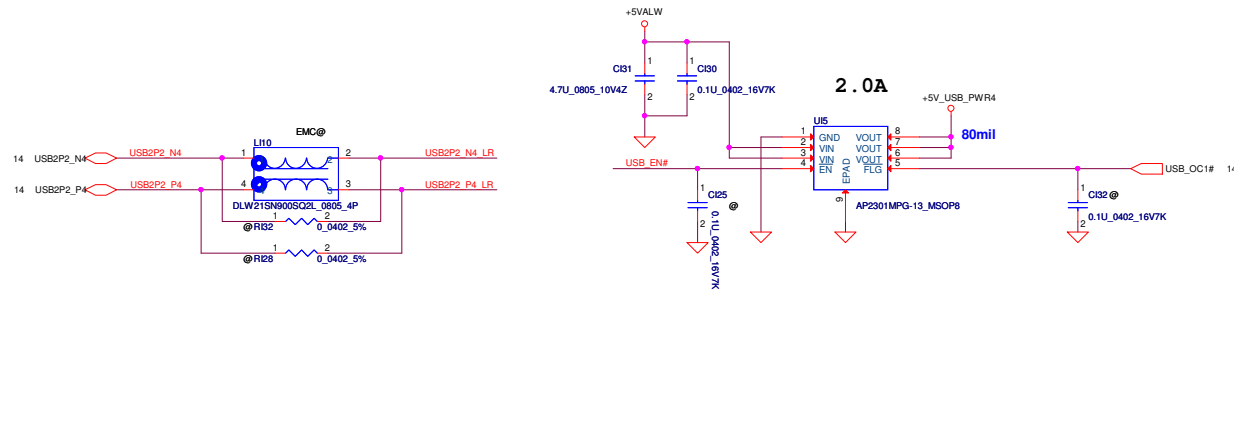
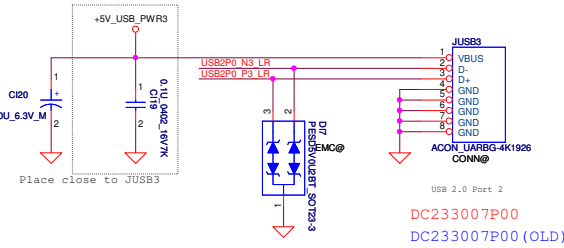
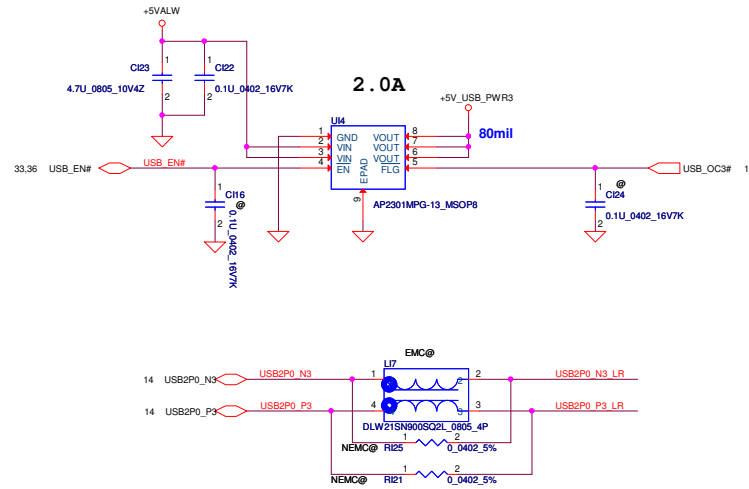
9/20 OAK Intel USB3.0 issue
Change LI1, LI3, LI4, LI6 Part
PN: from SM01002080L (S SUPPRE_MURATA DLW21SN900SQ2L 0805)
To SM070000S80 (S COM FL_CHENG HANN WCM2012F2SF-670T04)
1/22 Change LI1, LI3, LI4, LI6 Part
PN: from SM070000S80 (S COM FL_CHENG HANN WCM2012F2SF-670T04)
To SM070001E00 (S COM FL_MURATA DLW21SN900HQ2L)-Main
To SM070001S00 (S COM FL_KINGCORE WCM-2012HS-900T)-2nd



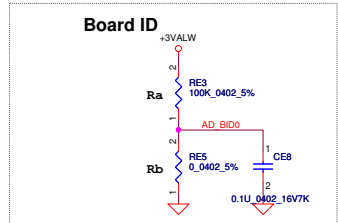
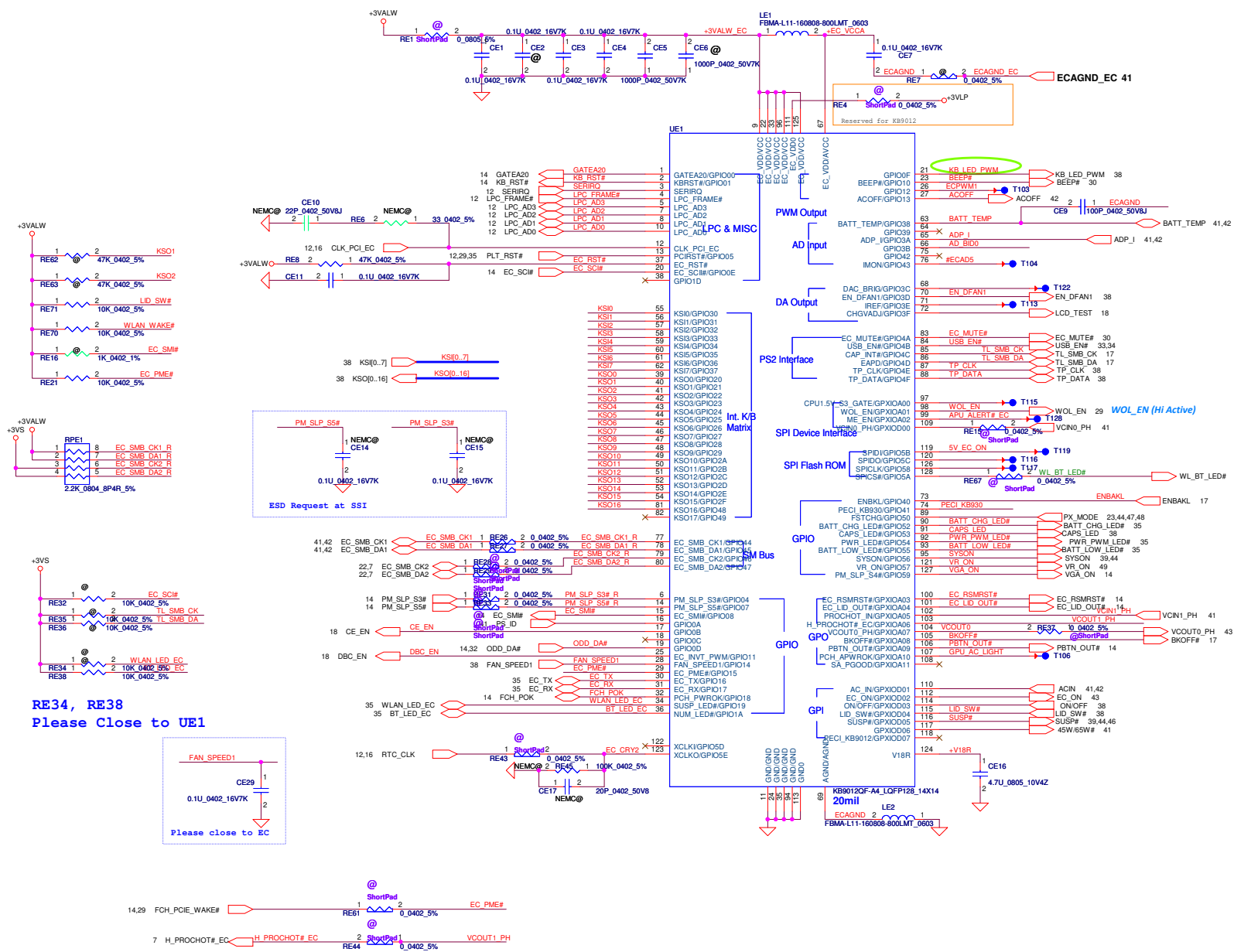
USB conn.1



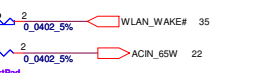
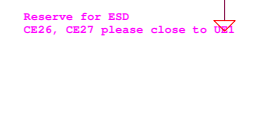
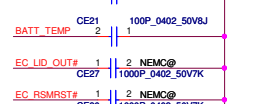
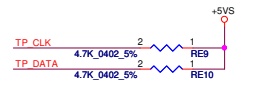
USB conn.2



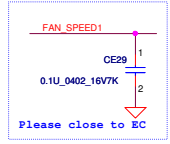
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Issued Date	2012/09/11	Deciphered Date	2014/03/12	MB to USB2.0 DB	
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Analog Board ID definition,
Please see page 4.

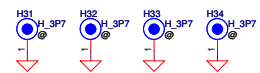
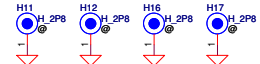
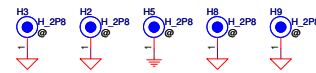


RE34, RE38
Please Close to UE1

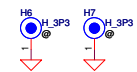


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Screw Hole



APU Screw Hole



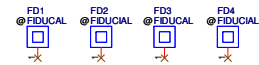
GPU Screw Hole



FAN Screw Hole

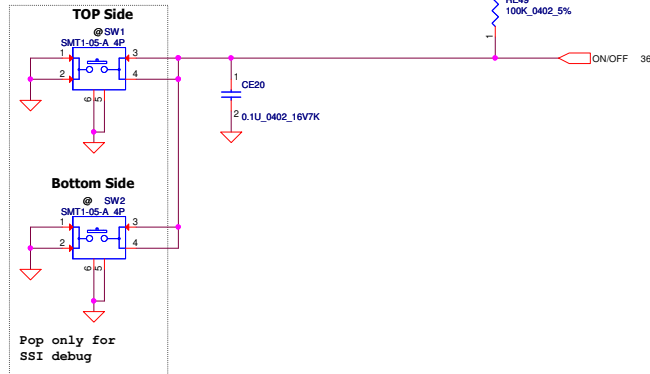


ODD Screw Hole

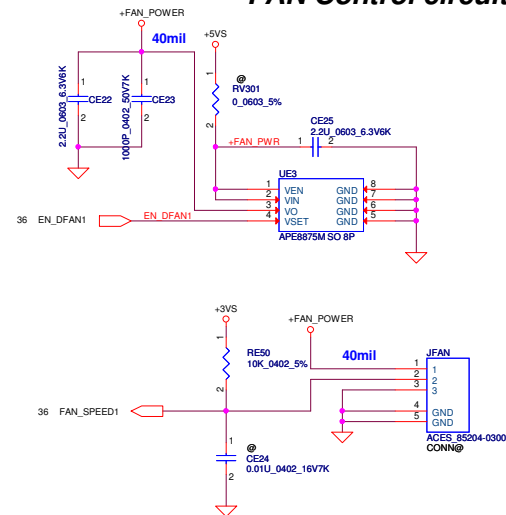


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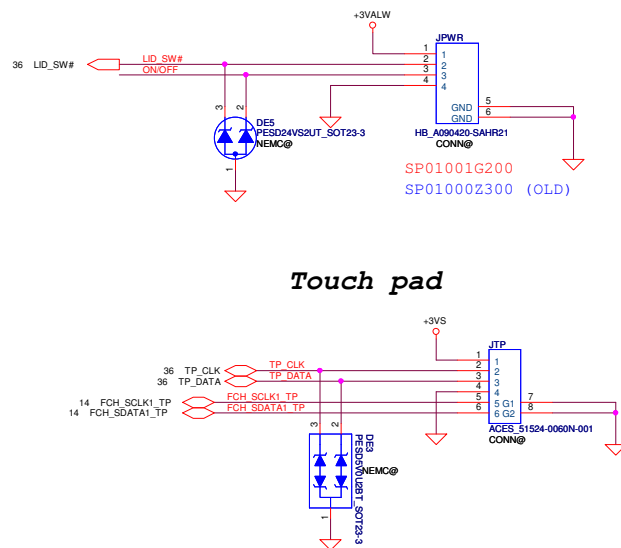
ON/OFF switch



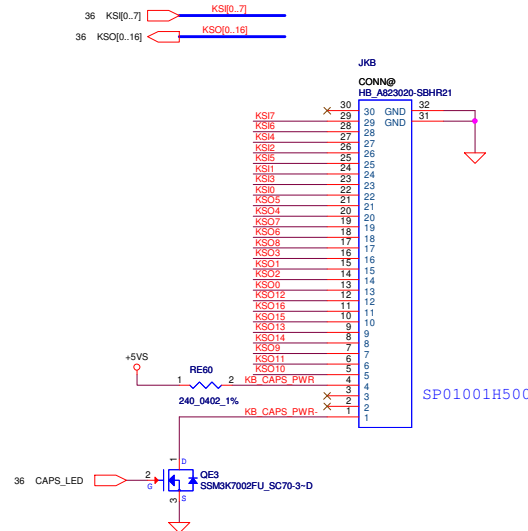
FAN Control circuit



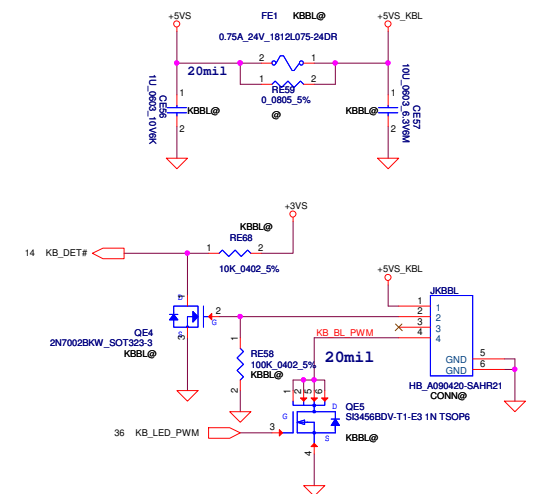
POWER/B



INT_KBD Conn.

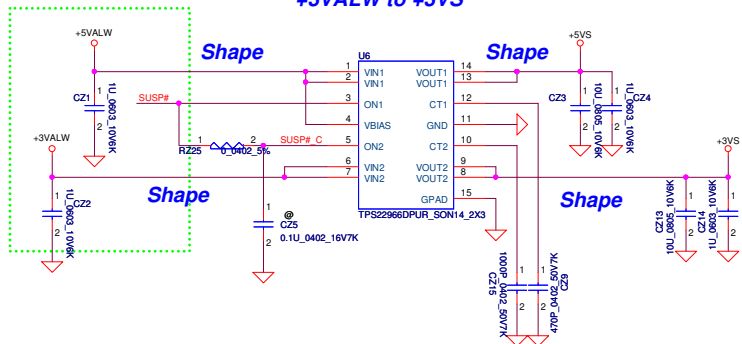


* Key Board Back Light

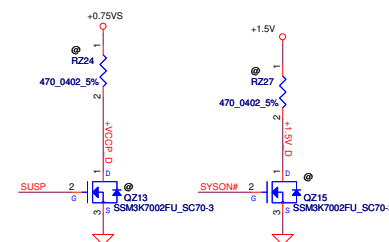
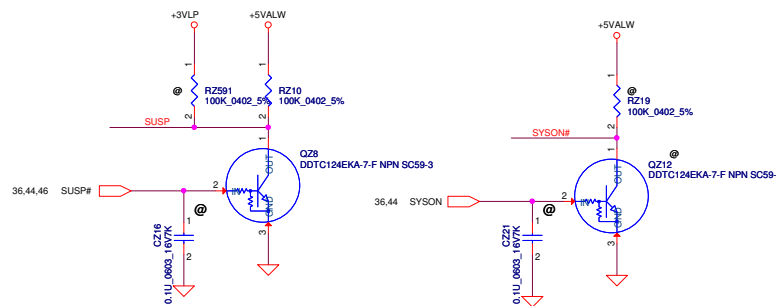
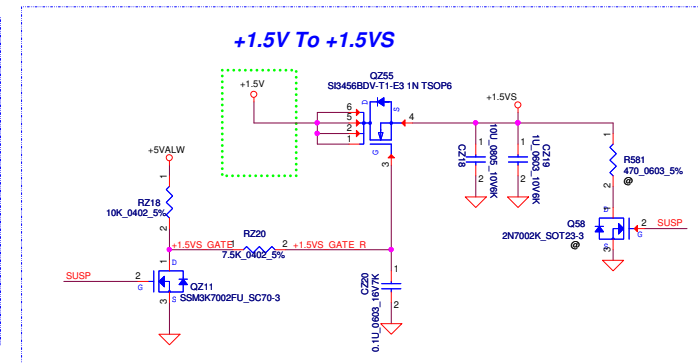
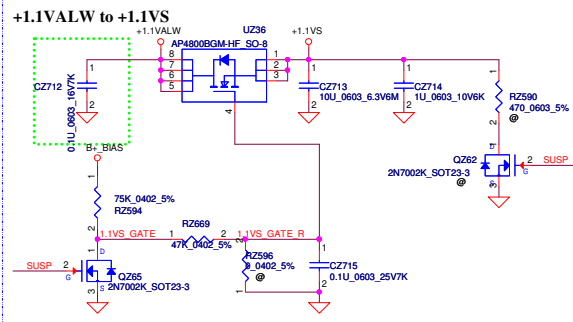


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+5VALW to +5VS
+3VALW to +3VS



CTx (pF)	RISE TIME (µs)	
	5V	3.3V
0	124	88
220	481	323
470	855	603
1000	1724	1185
2200	3328	2240
4700	7459	4950
10000	16059	10835



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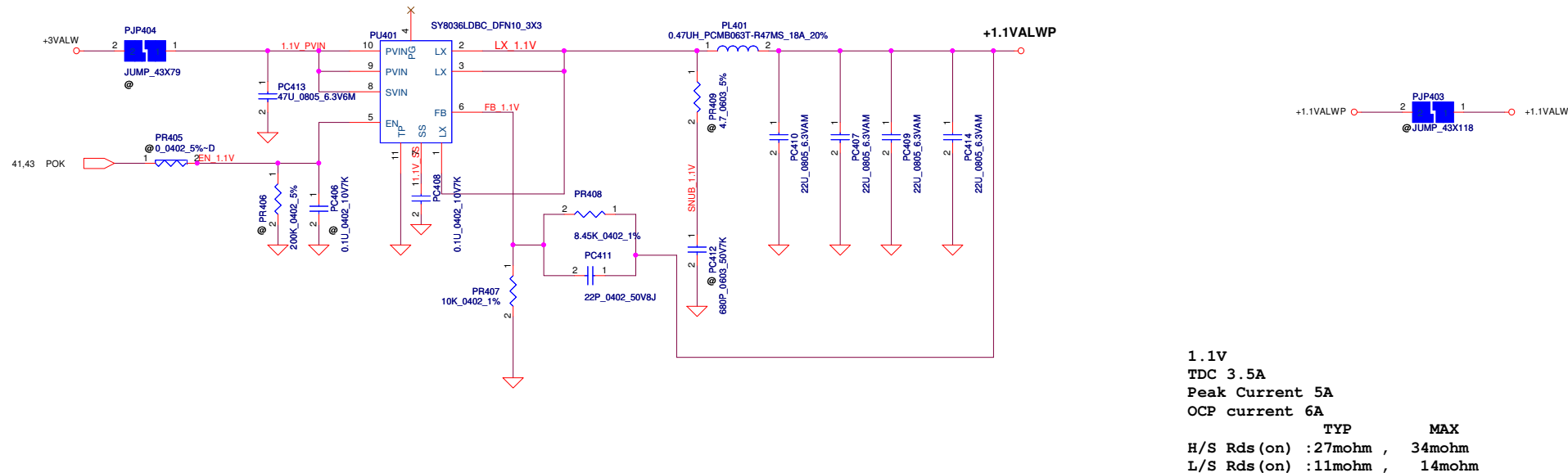
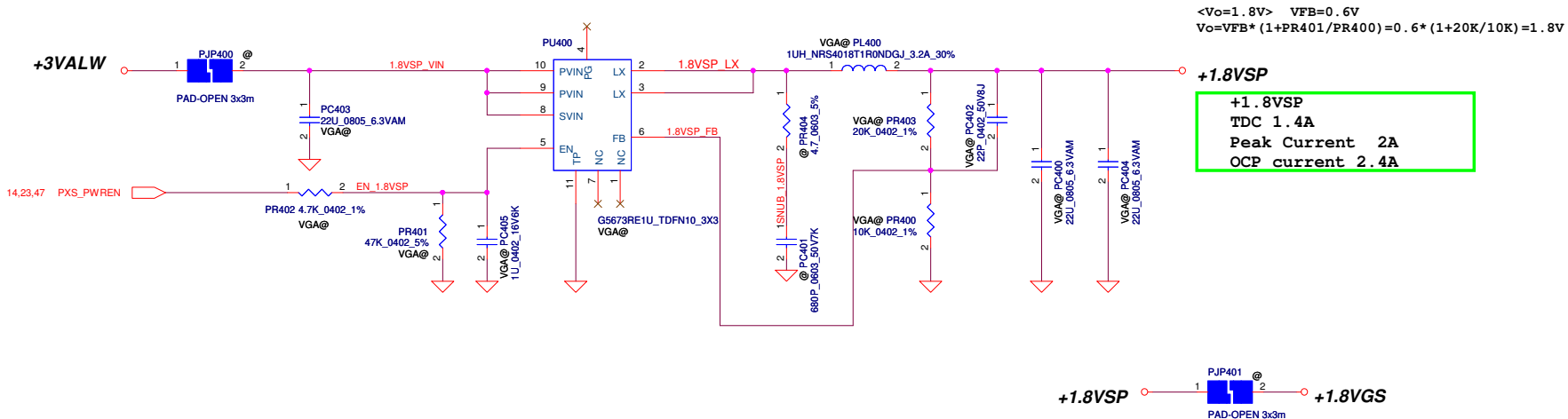
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Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	HW-PIR	
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1.5VP
TDC 11A
Peak Current 16A
OCP current 19A

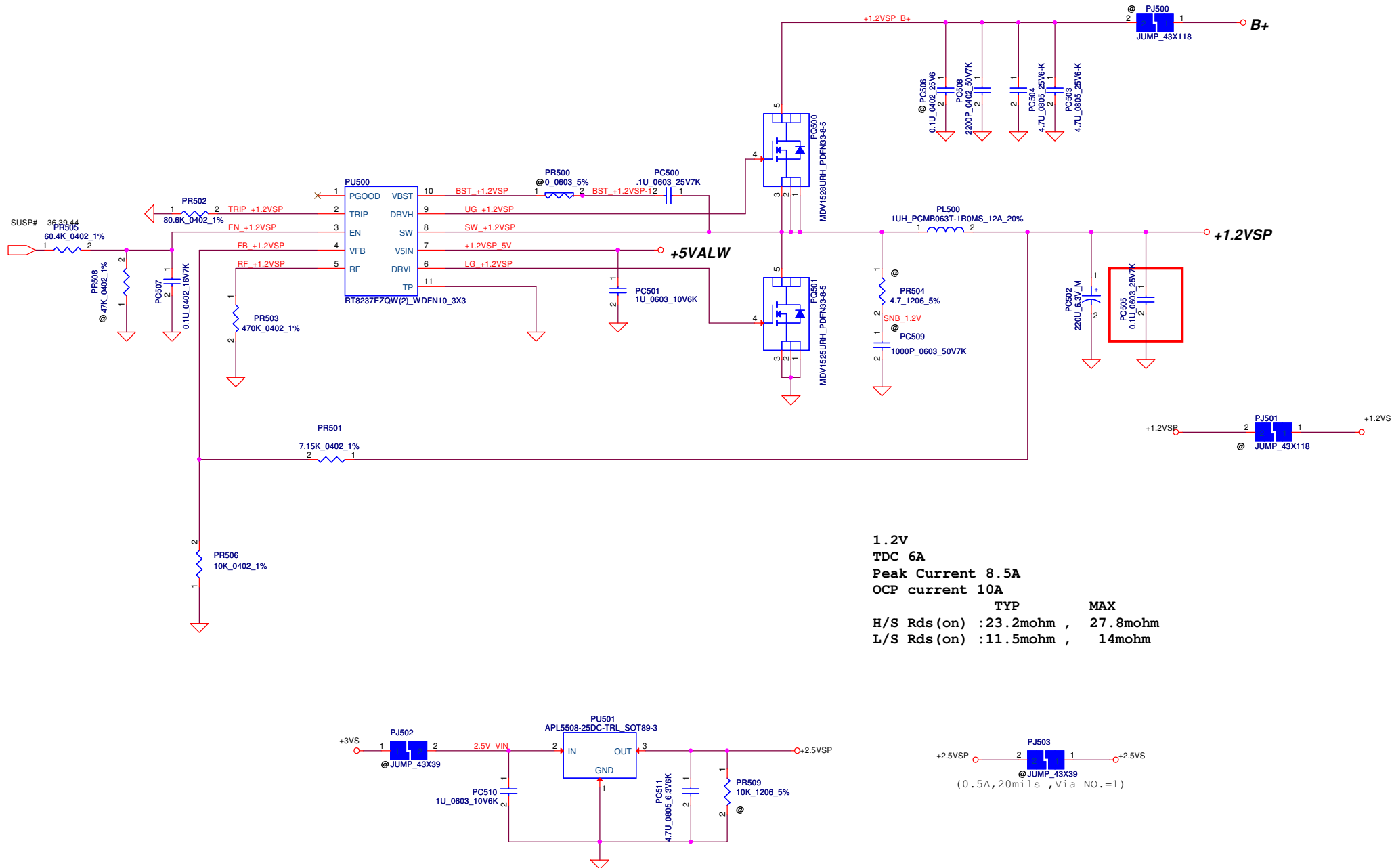
	TYP	MAX
H/S Rds(on)	: 23.2mohm	, 27.8mohm
L/S Rds(on)	: 7mohm	, 8.4mohm

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

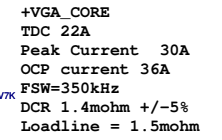
+1.5VGPU
TDC 5.6A
Peak Current 8A
OCP current 9.6A



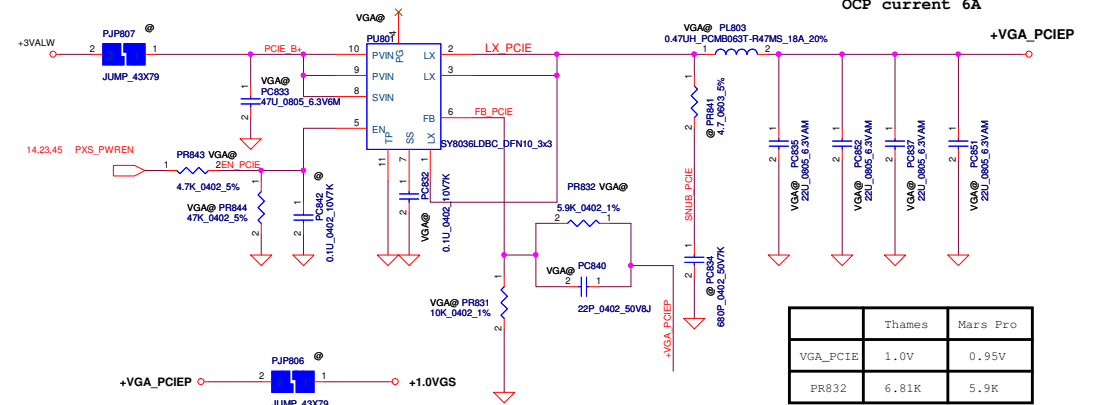
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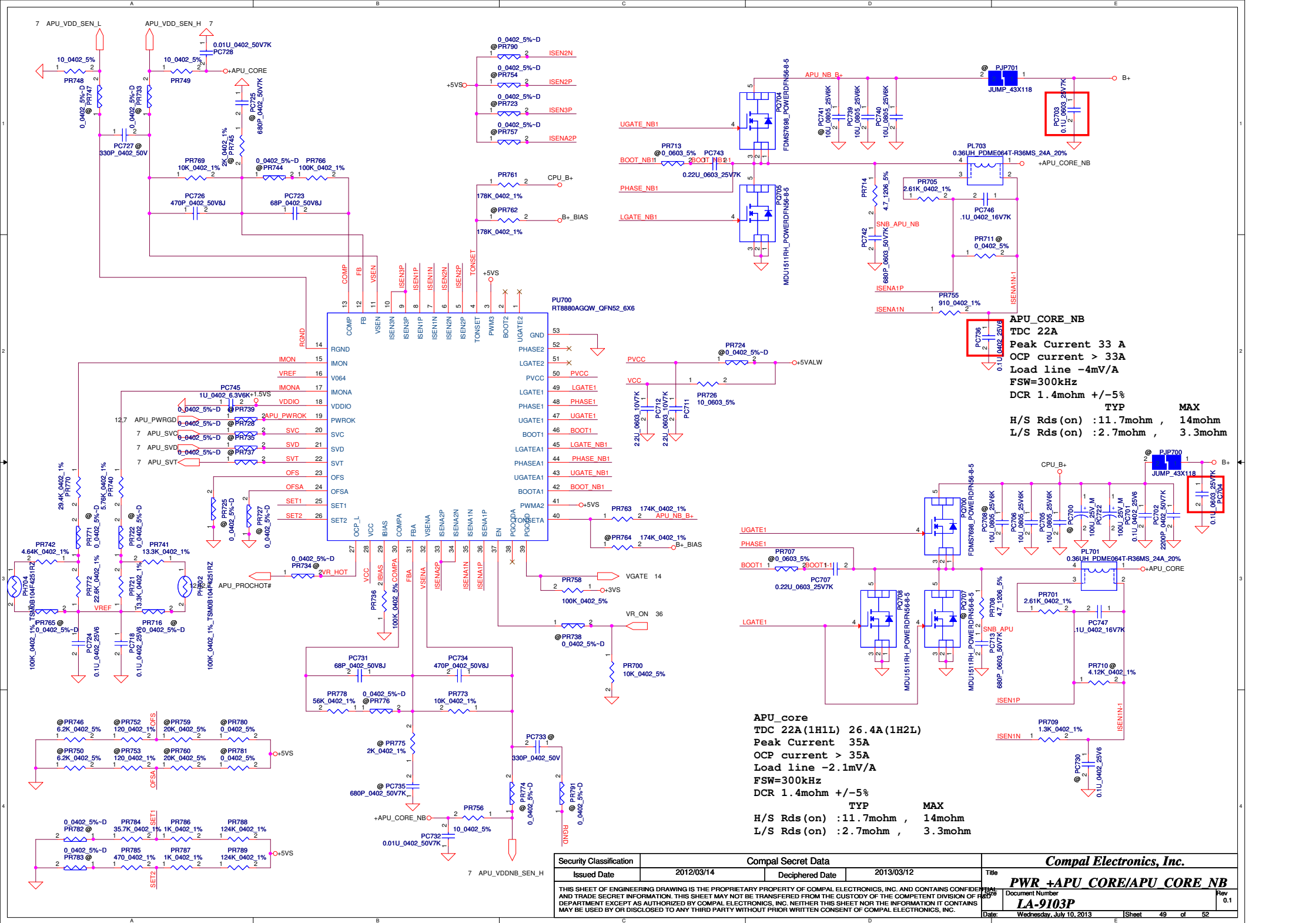


GPU_VID5 (GPU_10)	GPU_VID4 (GPU_14)	GPU_VID3 (GPU_15)	GPU_VID2 (GPU_16)	GPU_VID1 (GPU_20)	Core Voltage Level
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V



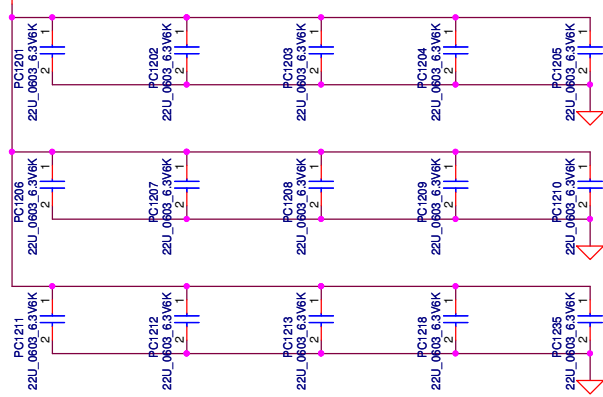
	Thames	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K

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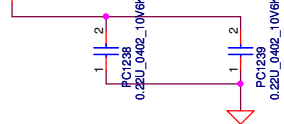


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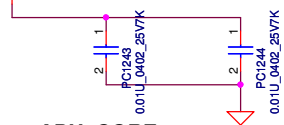
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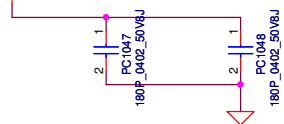
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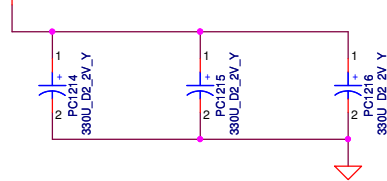
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+APU_CORE

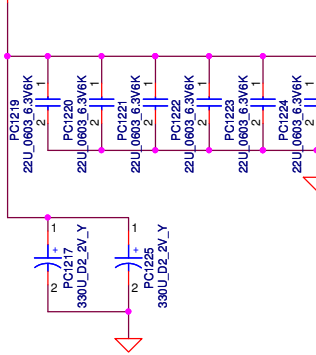


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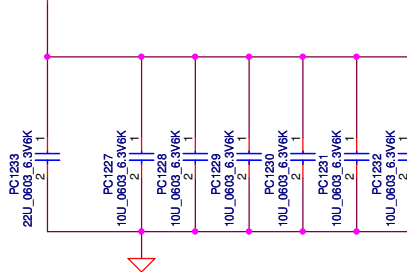
+APU_CORE_NB

+APU_CORE_NB



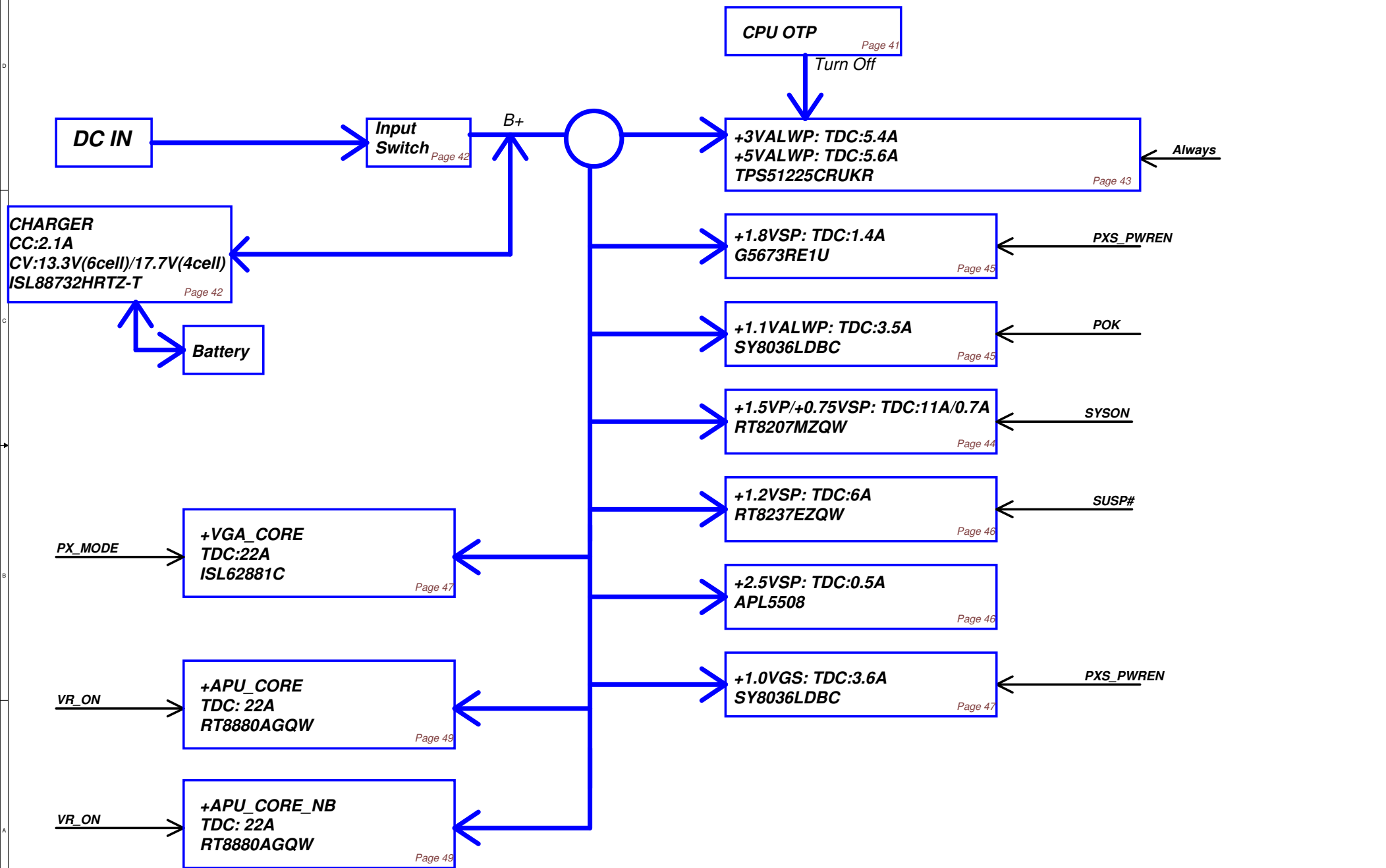
+1.2VS

+1.2VS



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Power block



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