

Thurman UMA Schematics Document

uFCPGA Mobile Merom

Intel Crestline-GM + ICH8M

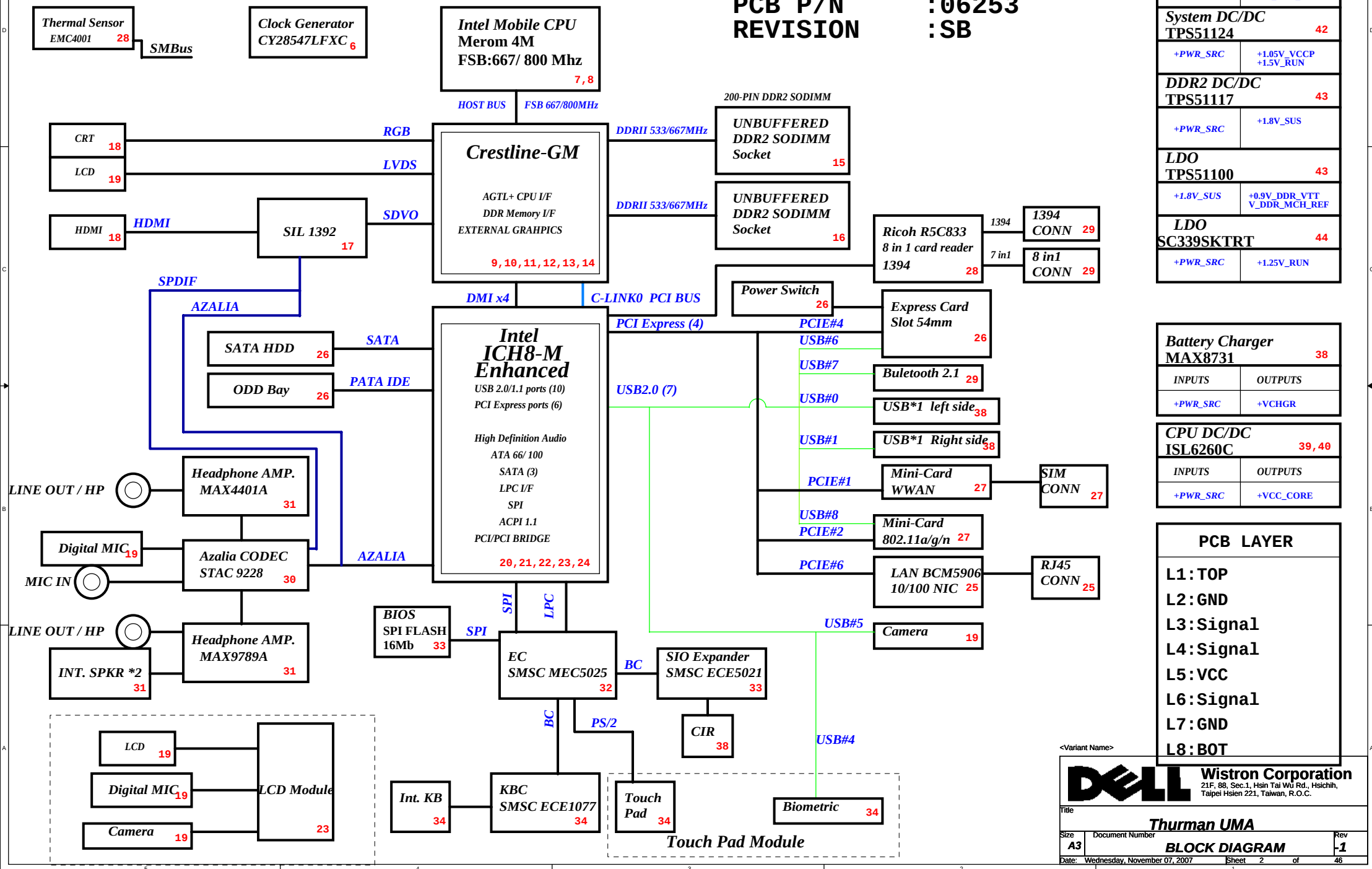
2007-11-19

REV : -1 (DELL:A00)

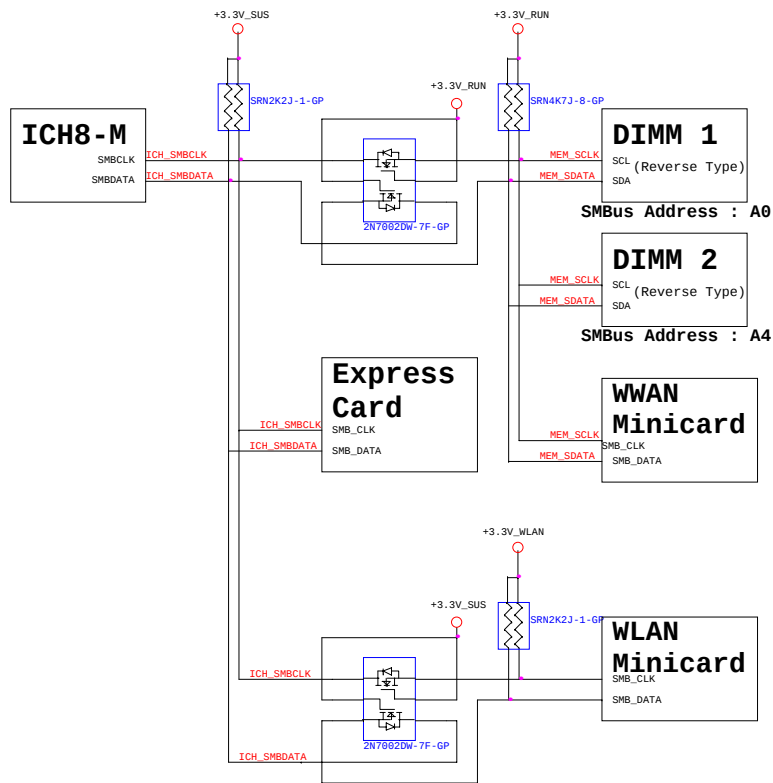
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		Thurman UMA	
Size	Document Number	Rev	
A3		COVER PAGE	-1
Date: Friday, January 18, 2008	Sheet 1	of 46	

Thurman UMA Block Diagram

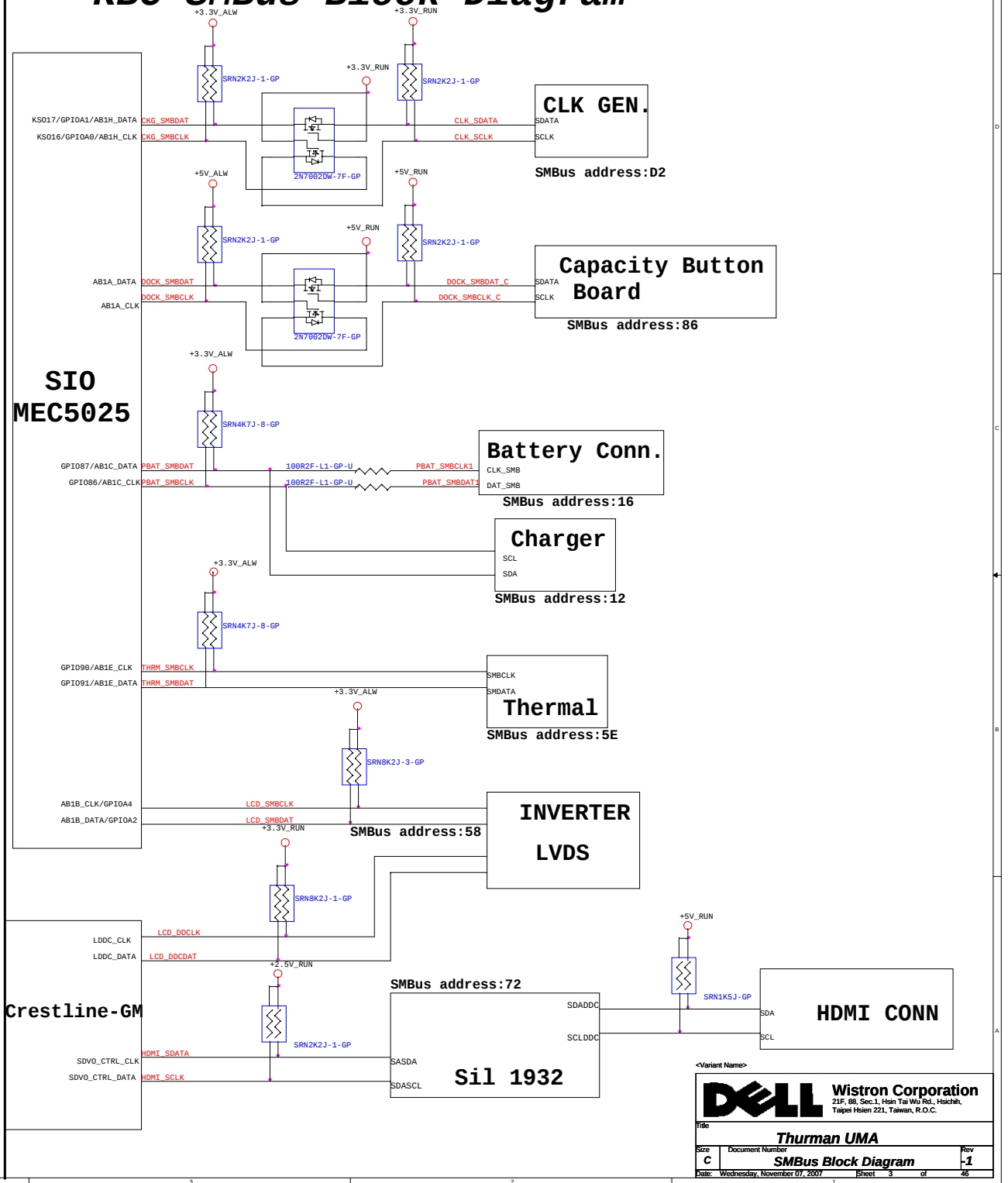
Project code: 91.4C301.001
PCB P/N : 06253
REVISION : SB



ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 15 IO_VOUT[2,1,0]			
Bit5 S1	Bit4 S8	Spread Spectrum S14:0	
0	0	-0.5%(Default)	
0	1	-1.0%	
1	0	-1.5%	
1	1	-2.0%	

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPI020	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSusi_05 VccSusi_15 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSusi_05,VccSusi_15 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPI033/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

INTEL CRESTLINE STRAP PIN

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation*	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

CFG[13:12]	
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation*

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	10/100 LOM

ICH USB TABLE

USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	
USB9	MINI Card WWAN

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPI0[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPI023	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

XOR Chain Entrance Strap			
ICH_RSVD	TP3	AZ_DOUT ICH	Description
0	0	0	RSVD
0	1	1	Enter XOR Chain
1	0	0	Normal Operation(default)
1	1	1	Set PCIE port config bit1

A16 swap override strap			
PCI_GNT#3	low	high	A16 swap override enable
0	0	0	high = default
1	0	1	high = default
1	1	1	high = default

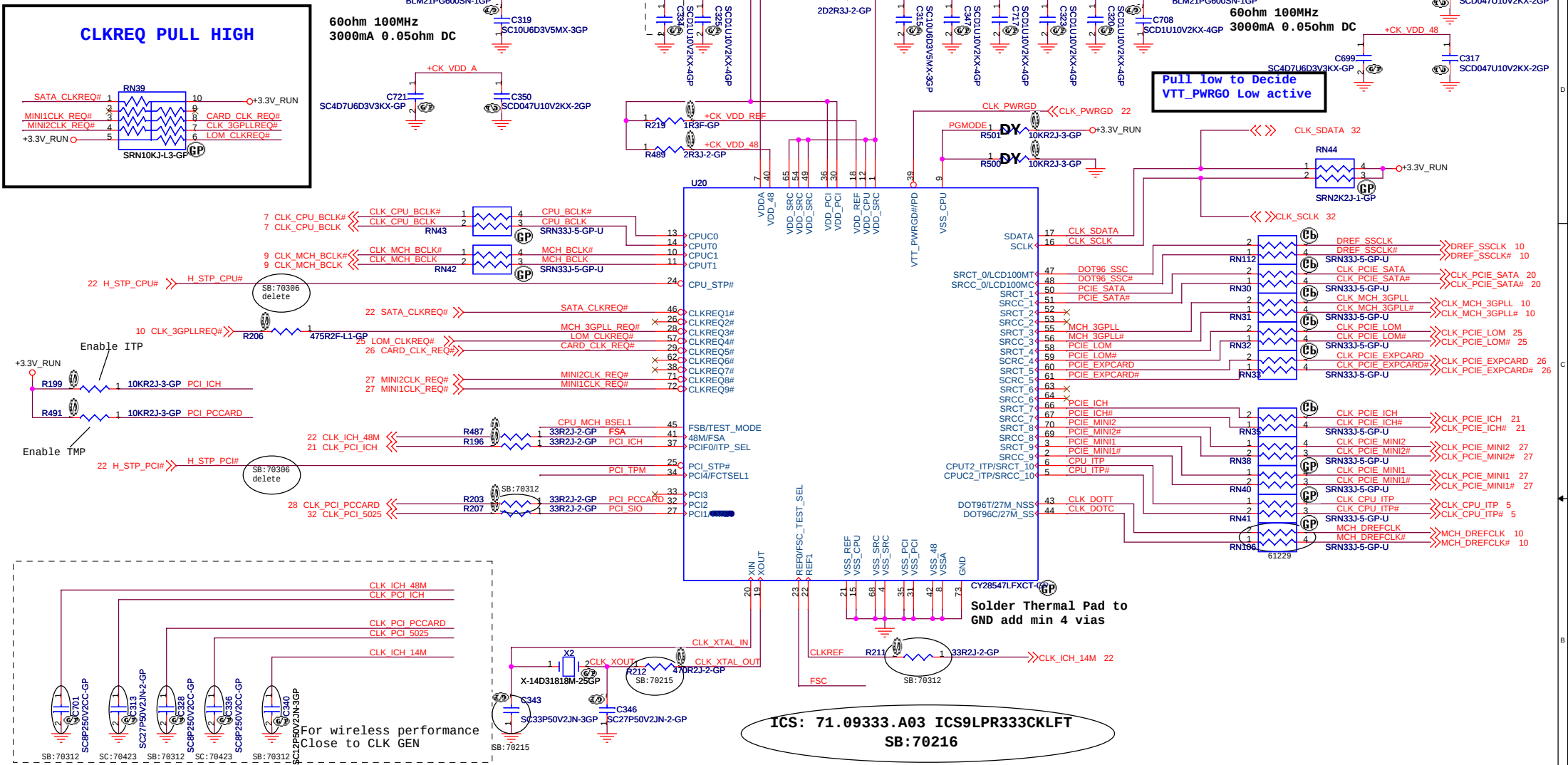
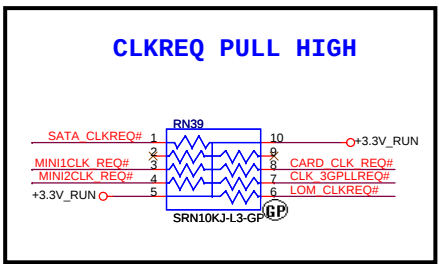
Boot BIOS Strap			
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location	
0	1	SPT	
1	0	PCI	
1	1	LPC(Default)	

Integrated VccSusi_05,VccSusi_15,VccCL1_5			
SM_INTVRMEN	High=Enable	Low=Disable	
0	0	0	
1	0	1	
1	1	1	

Integrated VccLAN1_05VccCL1_05			
LAN100_SLP	High=Enable	Low=Disable	
0	0	0	
1	0	1	
1	1	1	

No Reboot Strap	
SPKR	LOW = Default
0	LOW = Default
1	High=No Reboot

8.2K PULL HIGH

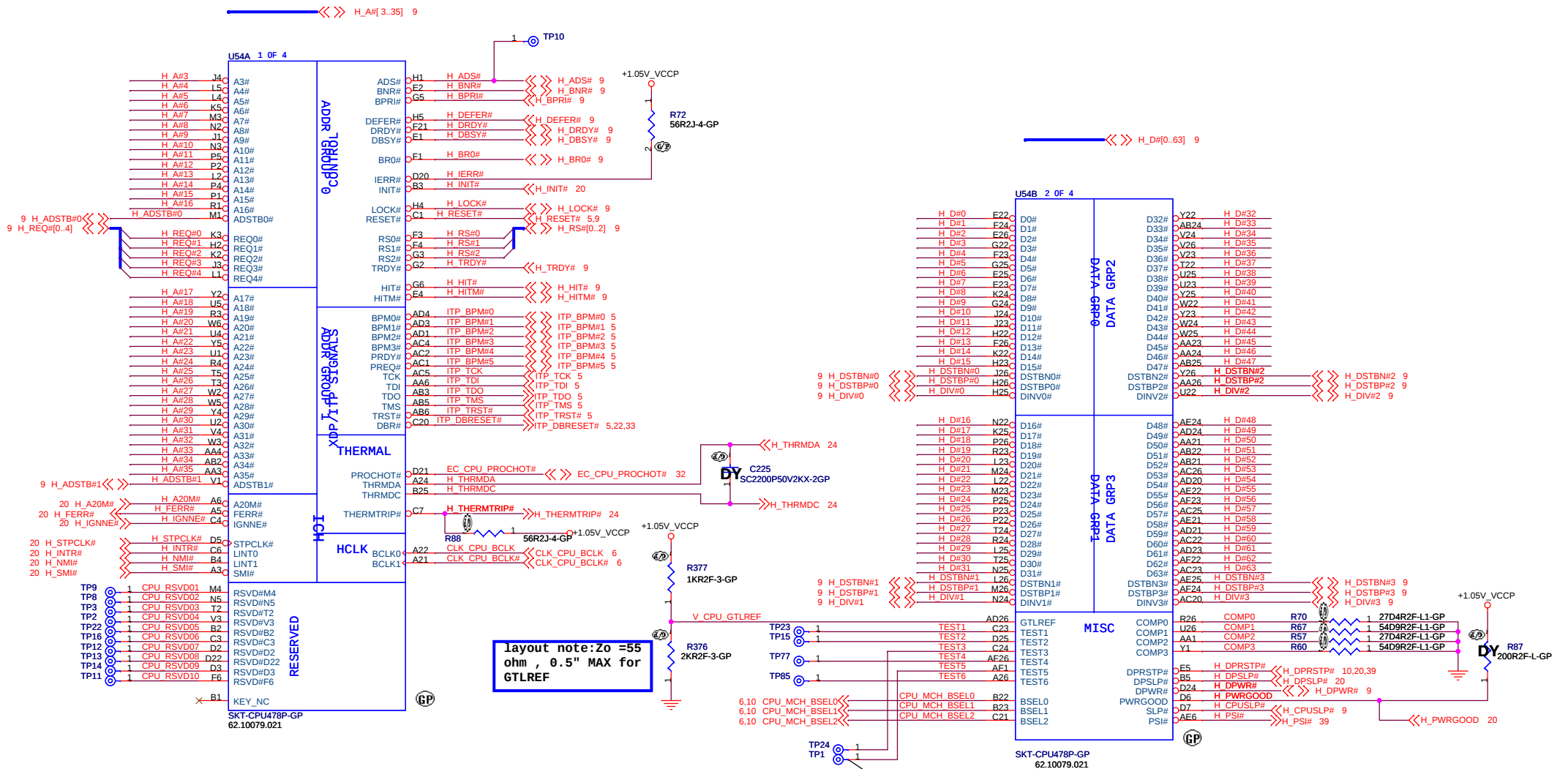


SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

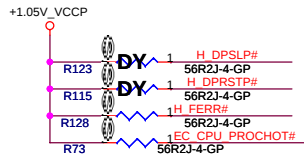
PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

PIN9 PGMODE	PIN39 DISCRIPTION
0	VTT_PWRGD#/PD
1	CKPWRGD/PD# (DEFAULT)

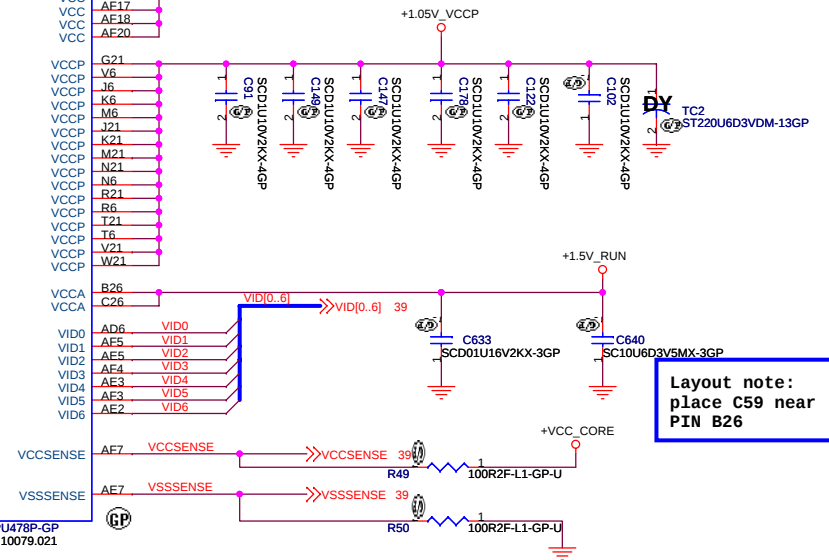
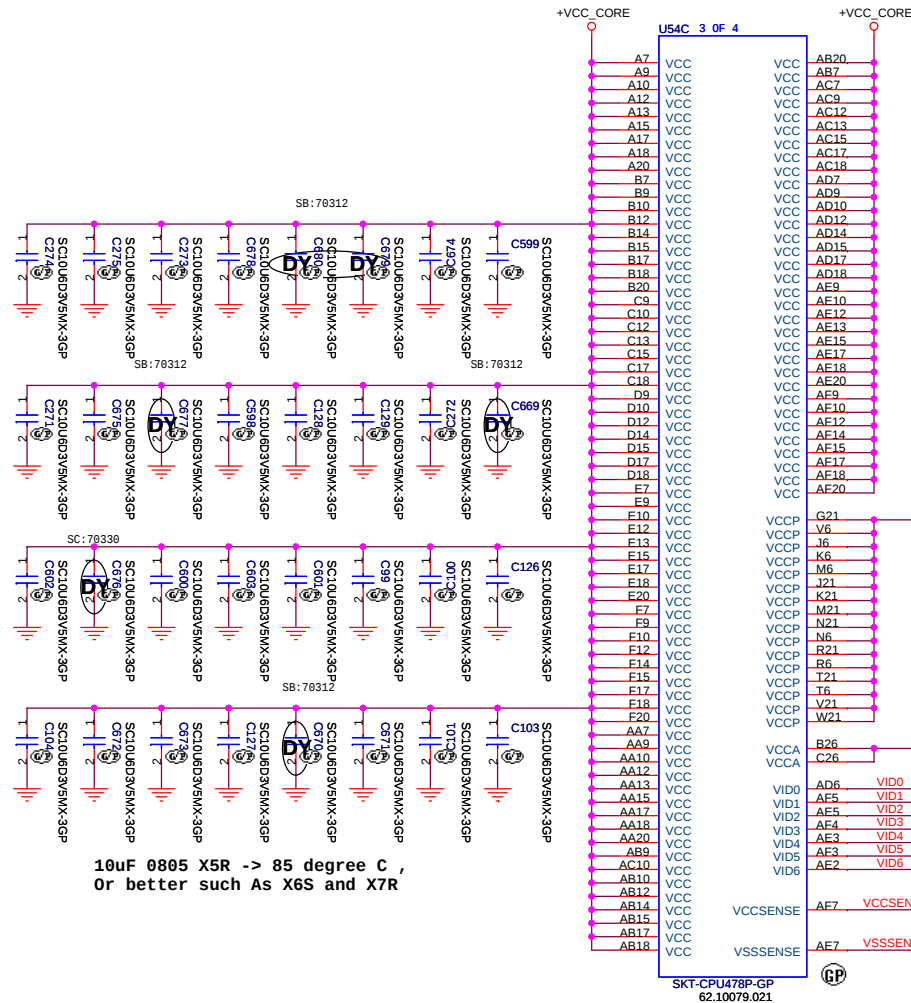
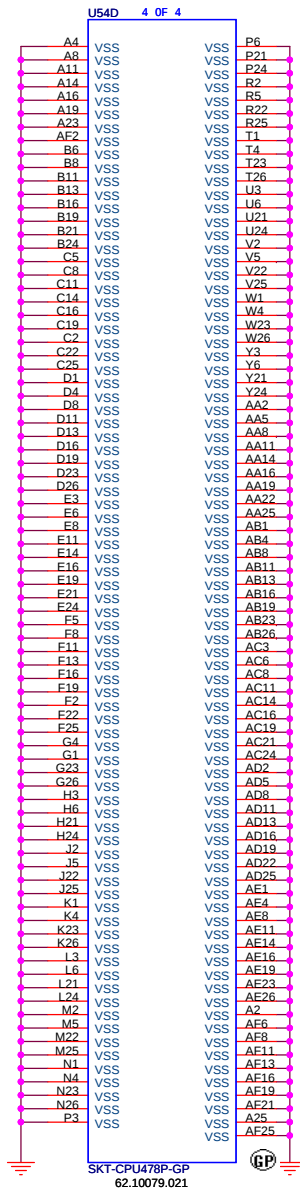
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Title			
		Thurman HSN	
Size	Document Number	Rev	
A3	CLK_GEN CY28547	-1	
Date:	Wednesday, November 07, 2007	Sheet	6 of 46



Use old Symbol replace New P/N
original value:SKT-CPU478P-GP



TEST3 and TEST5
For the purpose of testability,
route the signals through a ground
referenced Zo=55ohm trace that ends
in a via that is near a GND via
and is accessible through an
oscilloscope connection.



<Variant Name>

DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Thurman UMA

Size

Document Number

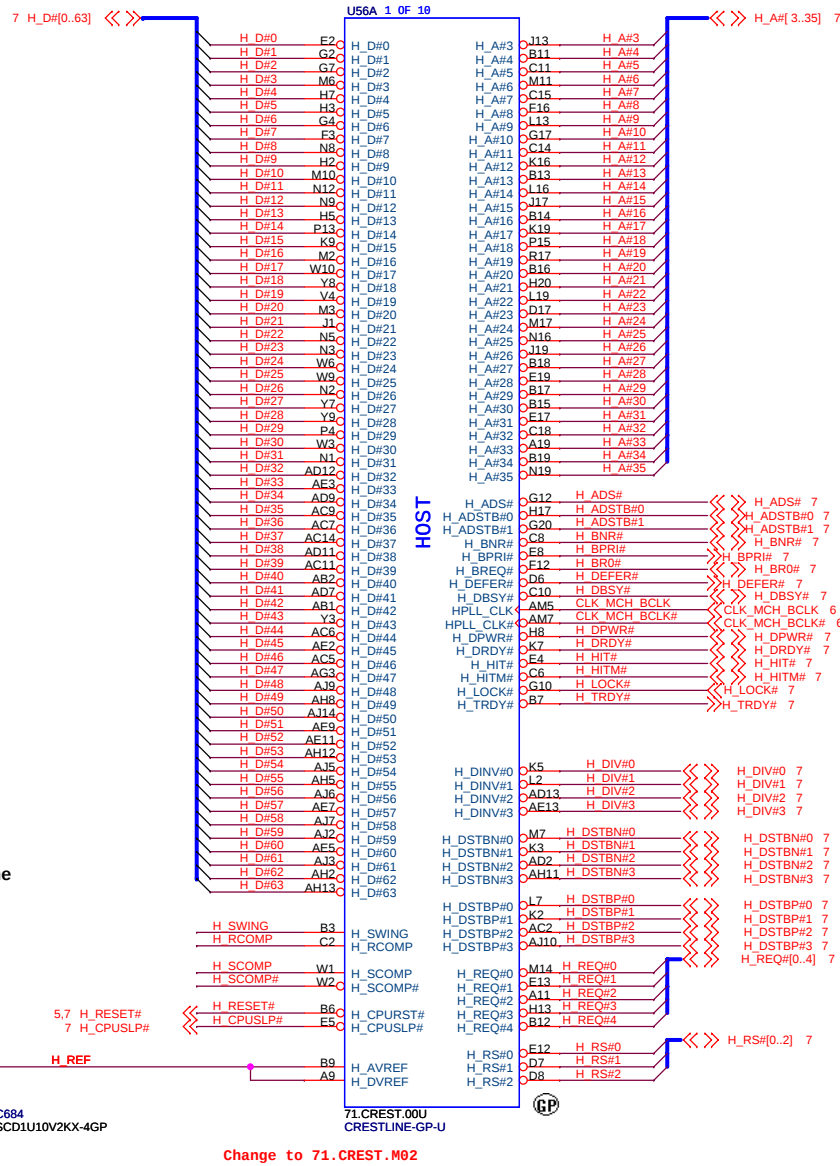
06.CPU-POWER (2/2)

Rev

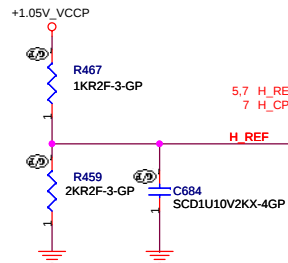
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Date: Wednesday, November 07, 2007

Sheet 8 of 46



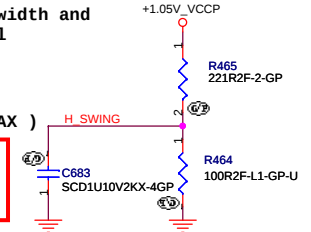
H_REF Decoupling Crestline
close Crestline 100 mil



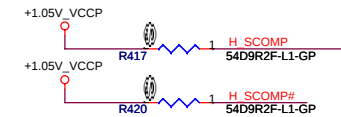
H_SWING routing Trace width and
Spacing use 10 / 20 mil

H_SWING Resistors and
Capacitors close
Caliistoga 500 mil (MAX)

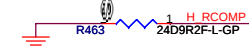
From Schematic Design
Checklit v.1201
221 1% pull high 100
1% pull low



H_SCOMP and H_SCOMP# Resistors
and Capacitors close Caliistoga
500 mil (MAX)
Zo=55ohms



H_RCOMP routing Trace width and
Spacing use 10 / 20 mil



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Thurman UMA

Size

Document Number

GMCH-FSB LIBC (1/6)

Rev

-1

Date: Wednesday, November 07, 2007

Sheet

9 of

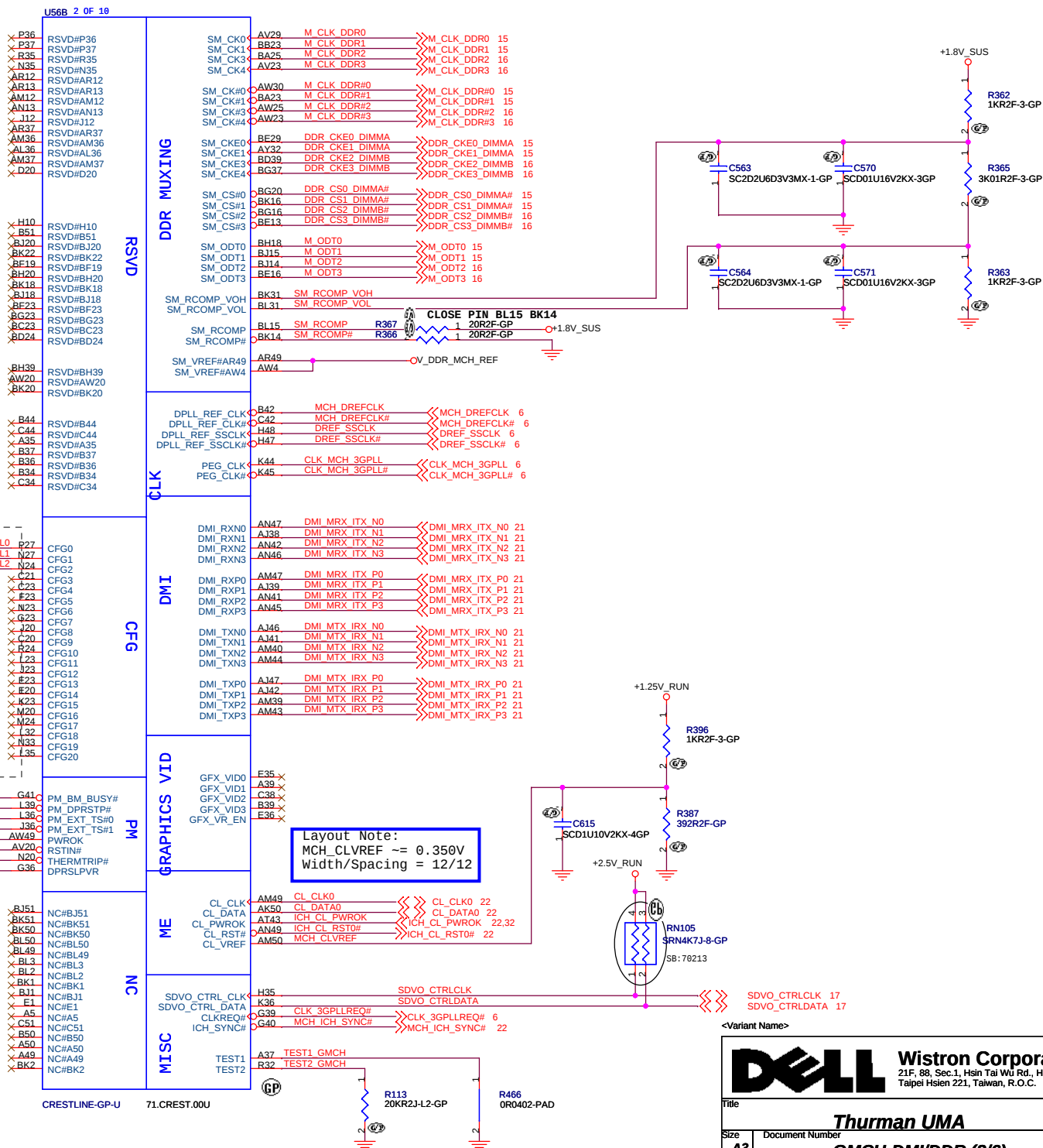
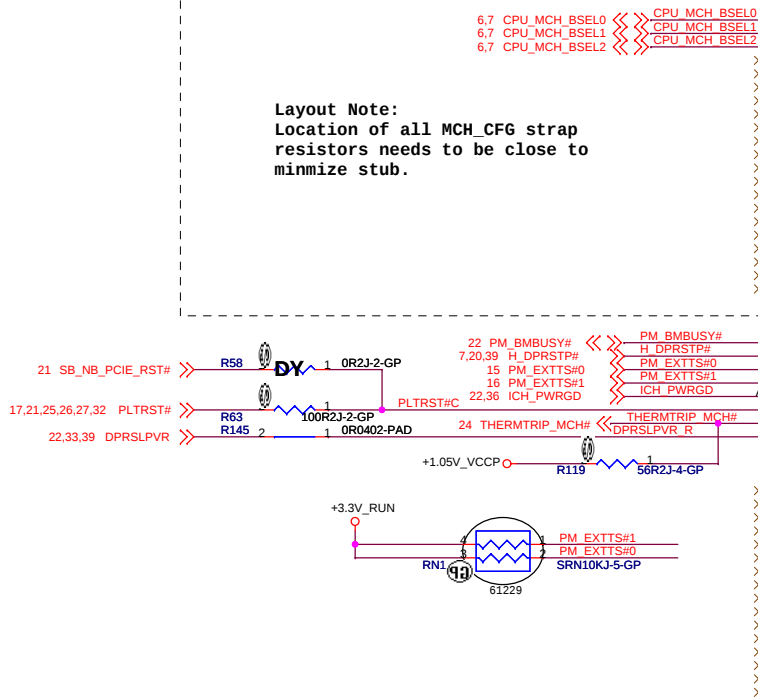
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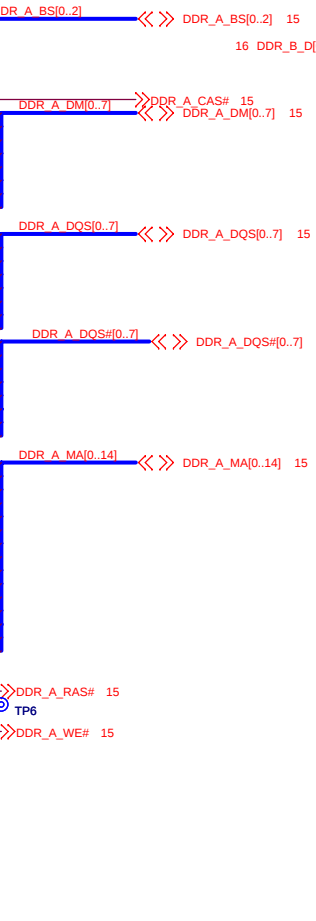
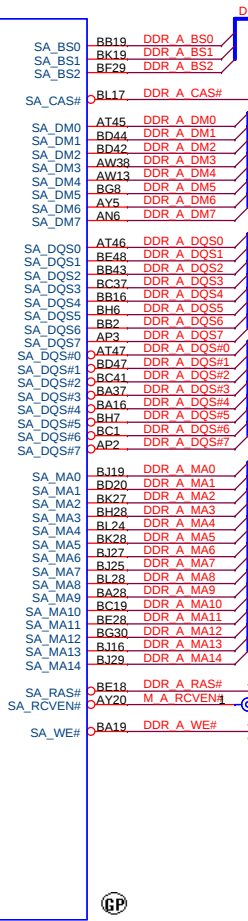
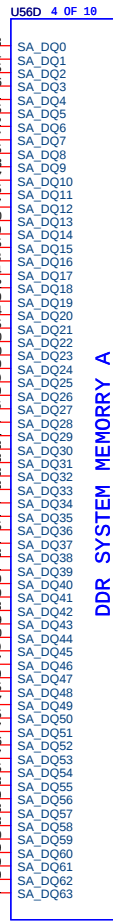
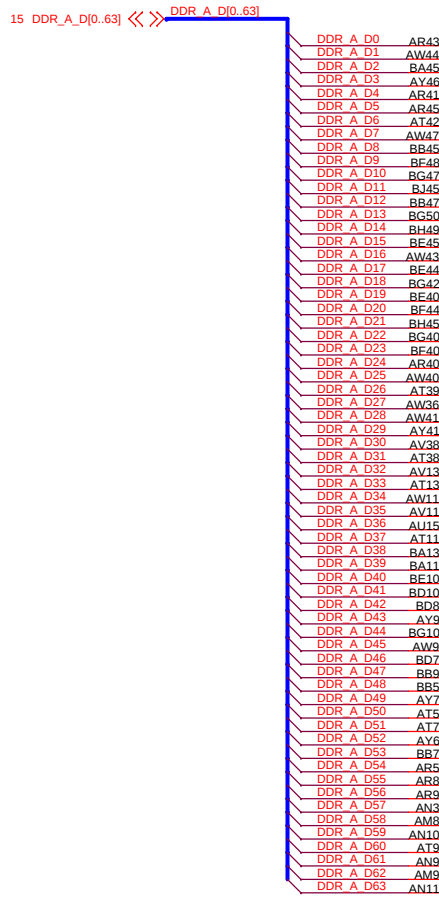
* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

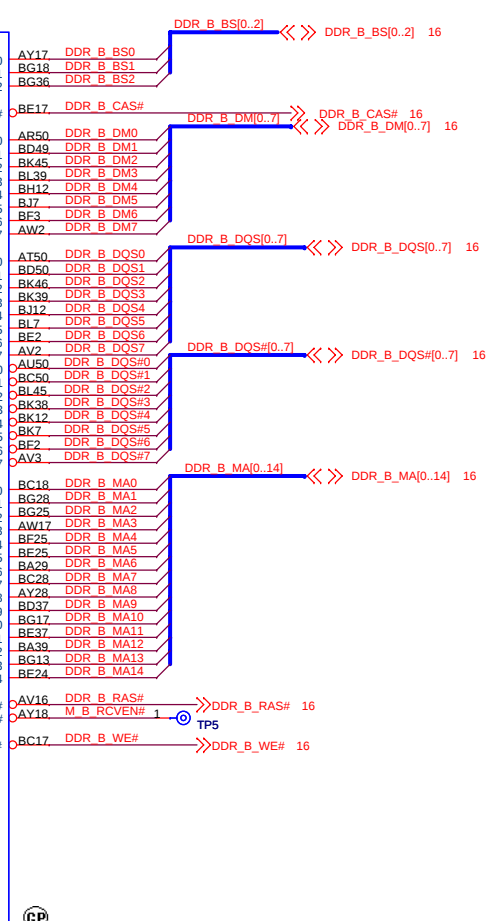
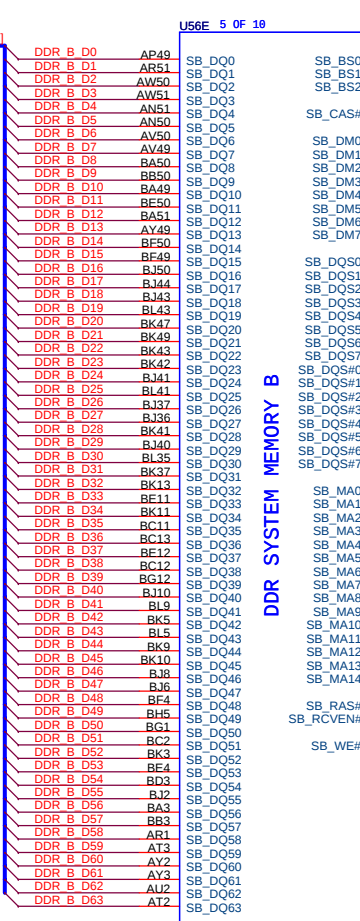
	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation*
	CFG[2..0] FSB Select
LHL	FSB 800
LHH	FSB 667
Other	Reserved

Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minimize stub.

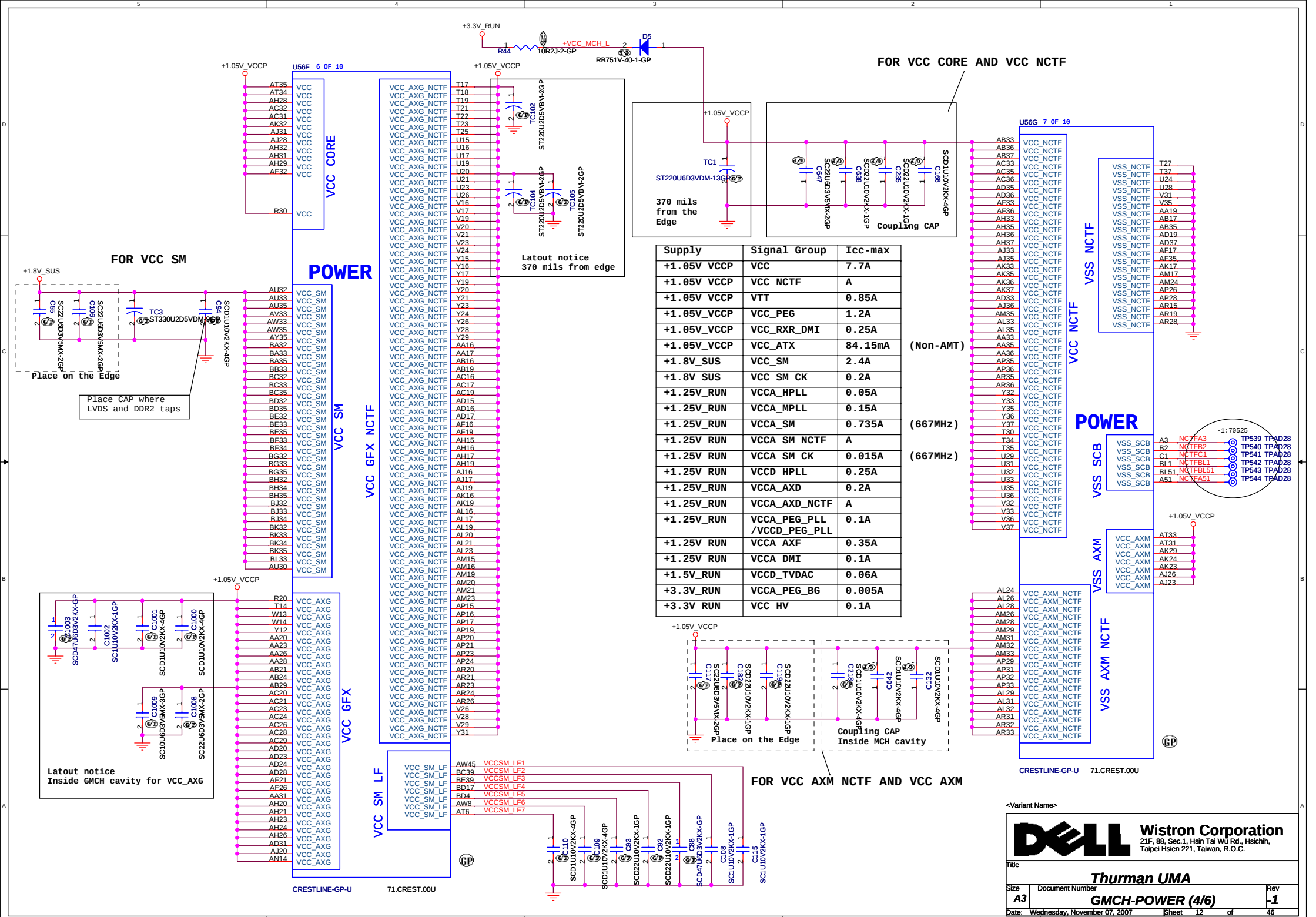


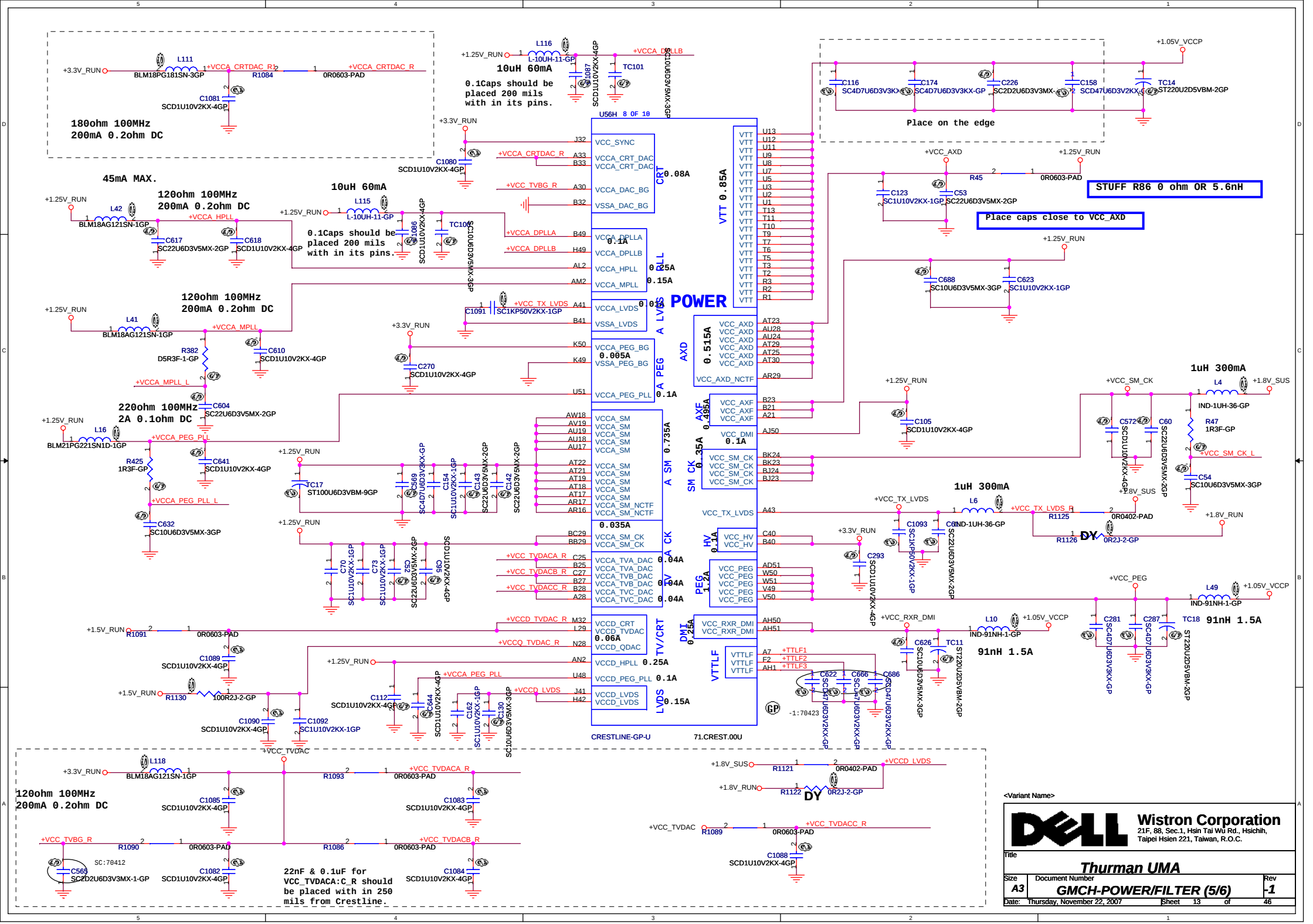


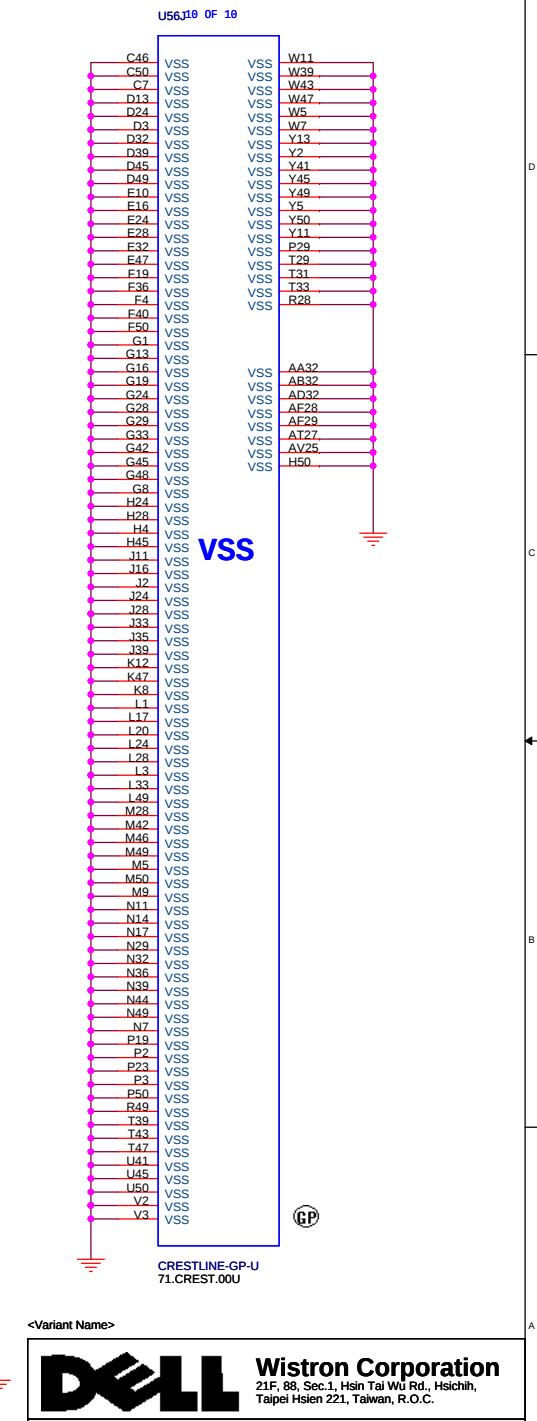
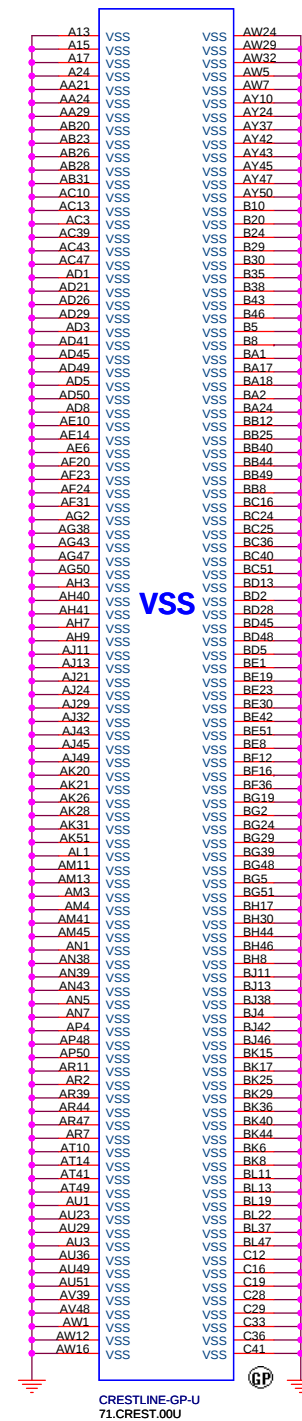
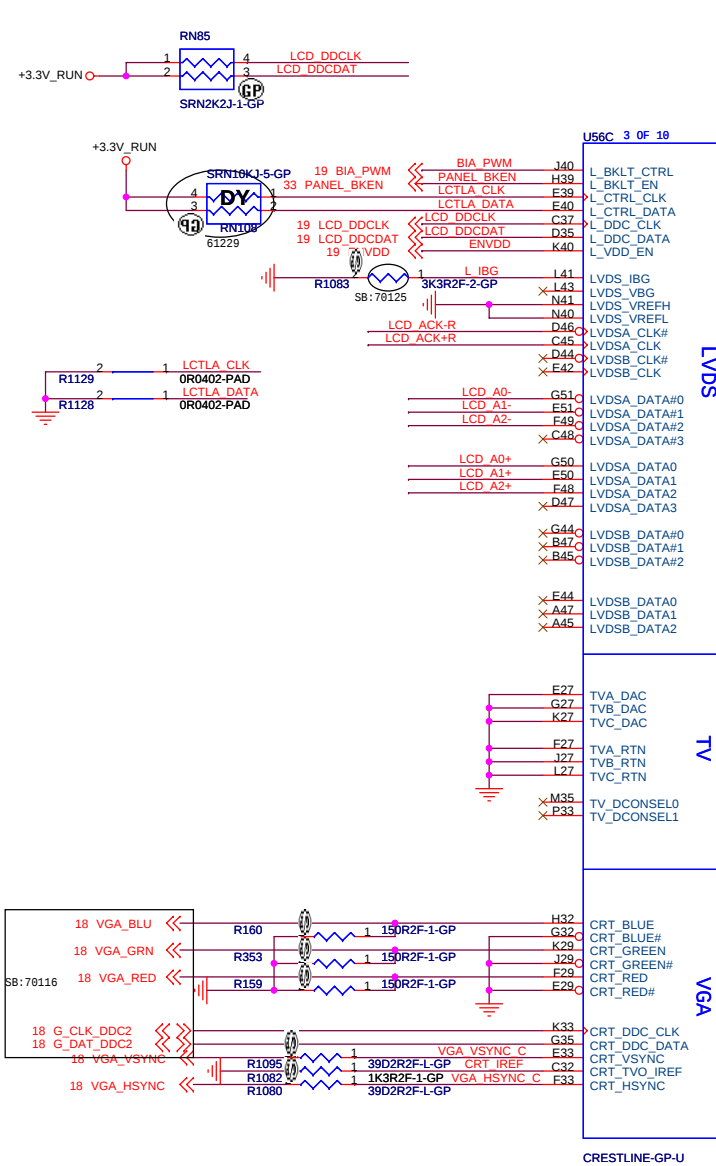
CRESTLINE-GP-U 71.CREST.00U

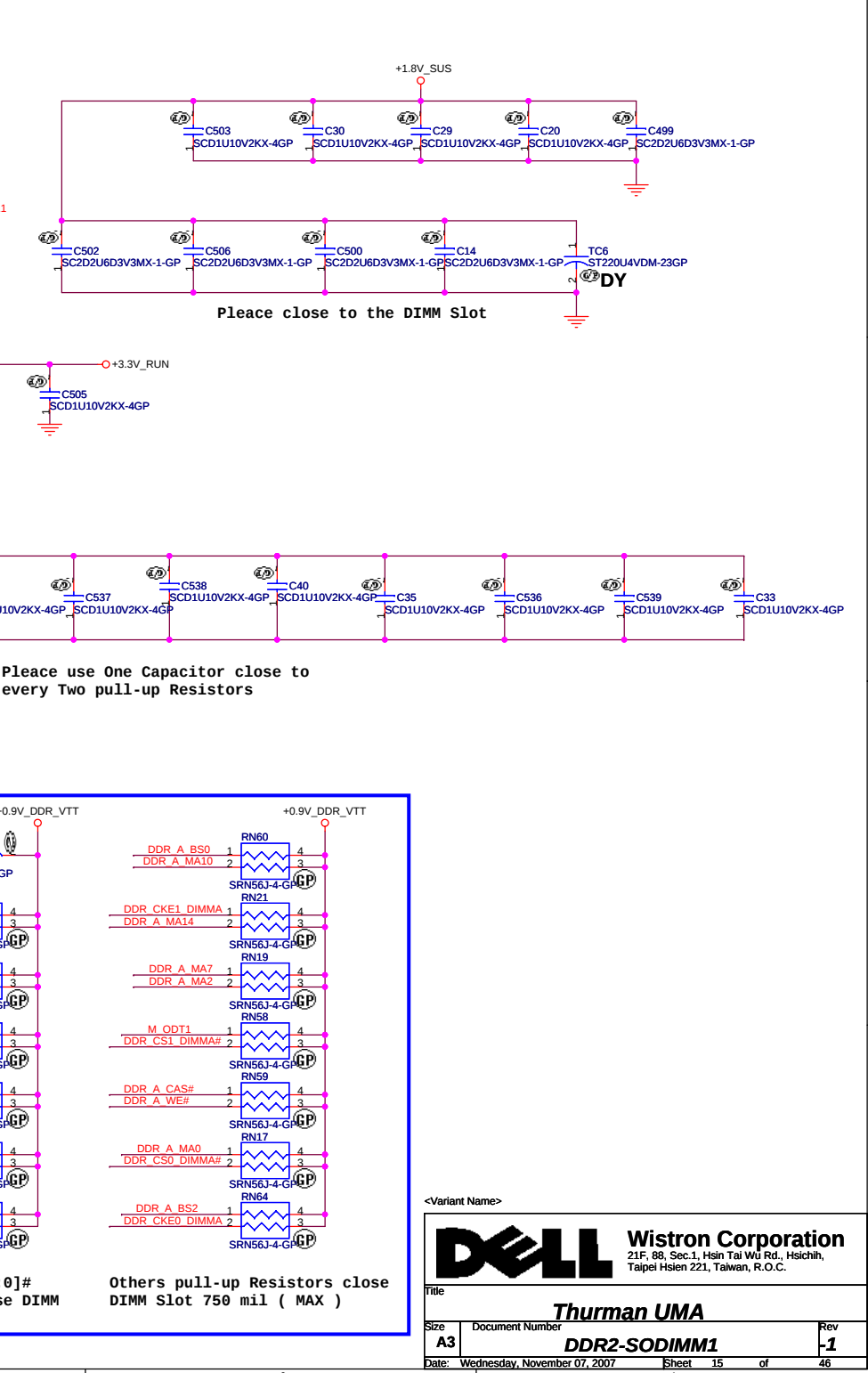
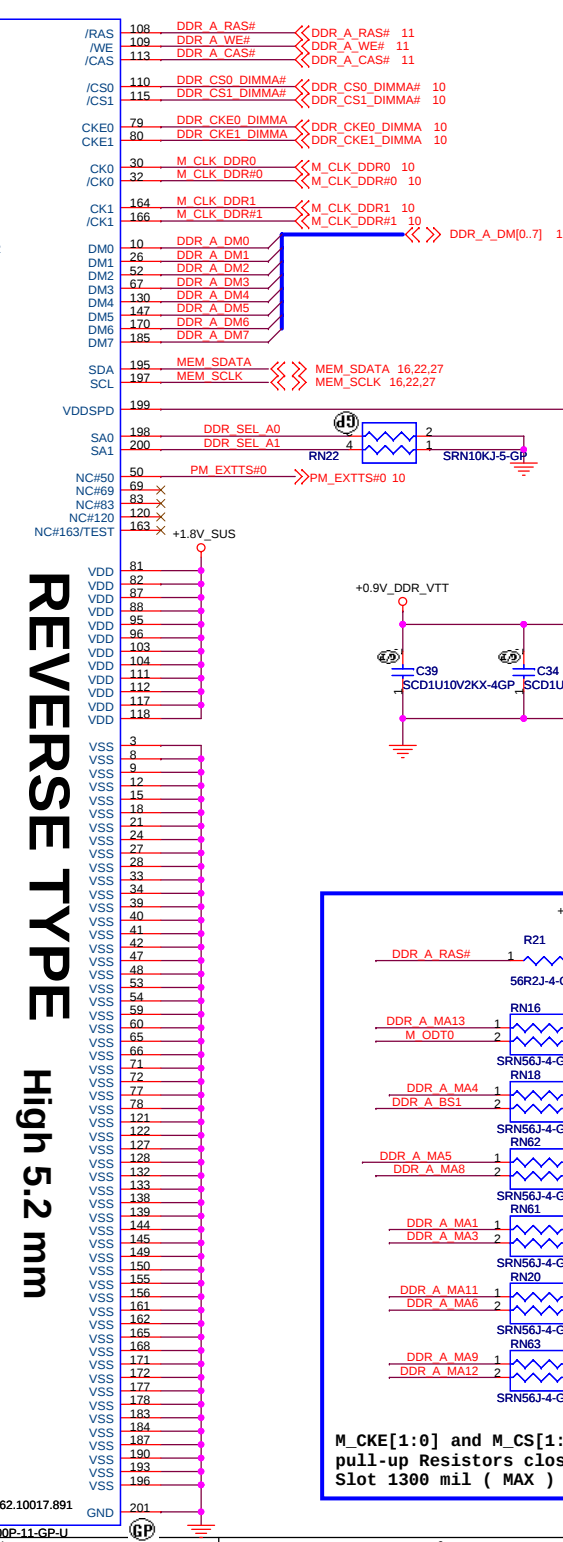
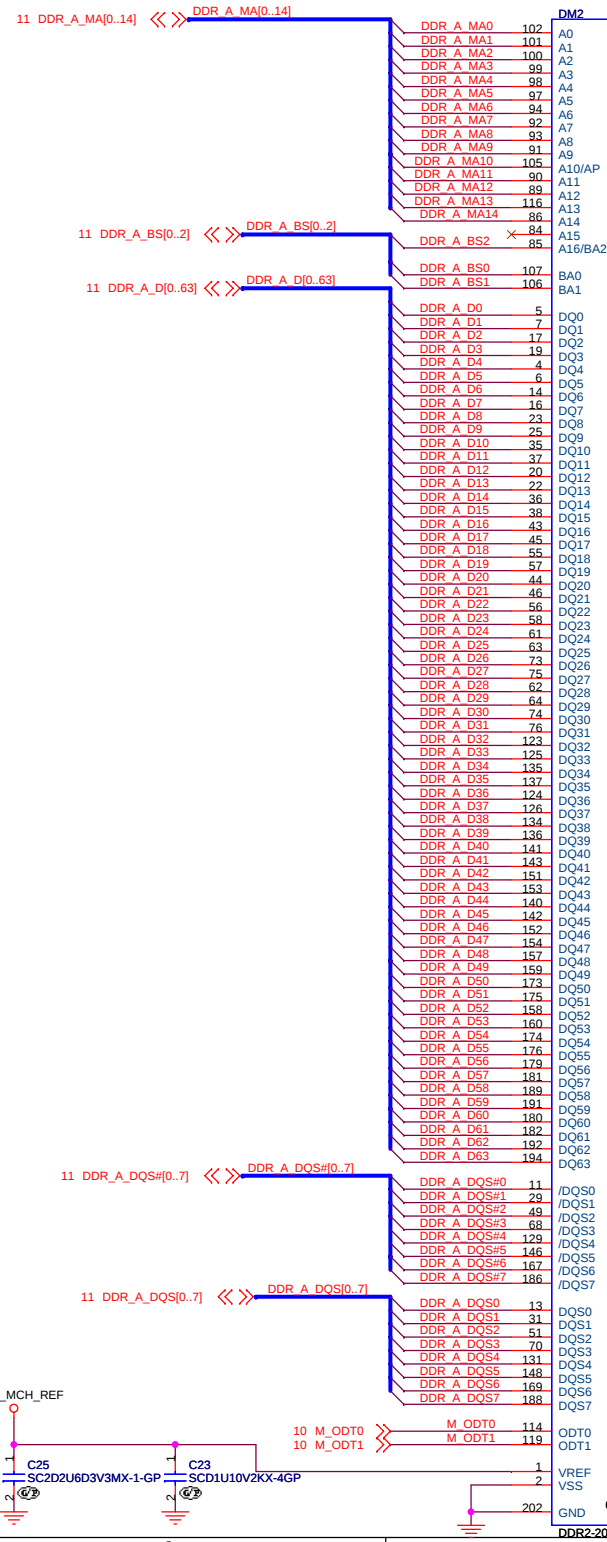


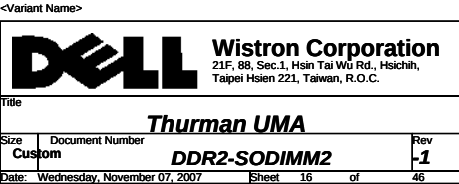
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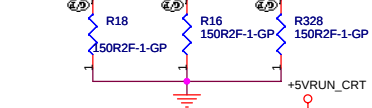






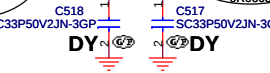
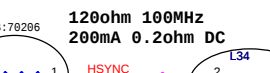
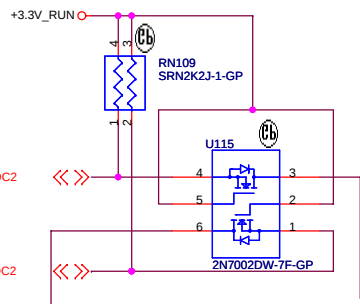
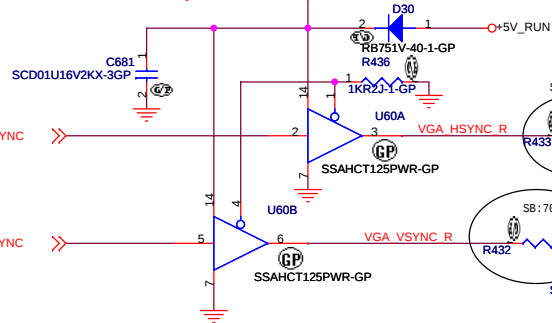
Setting R,G,B trace impedance to 50 ohm.

14 VGA_RED
14 VGA_GRN
14 VGA_BLU

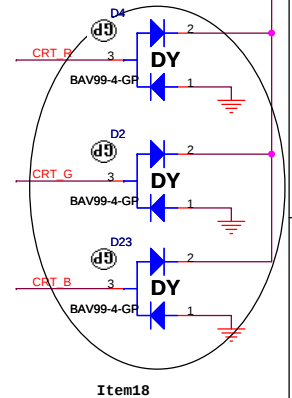
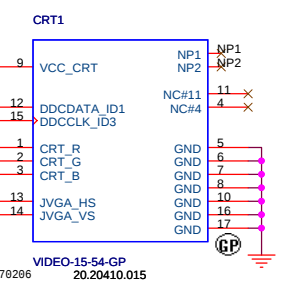


14 VGA_HSYNC

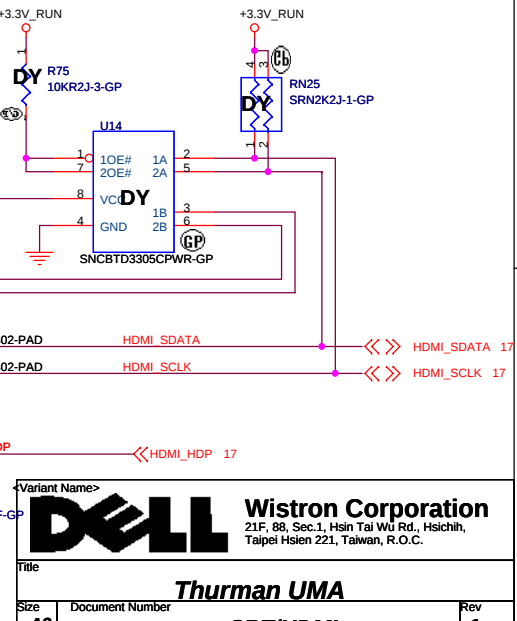
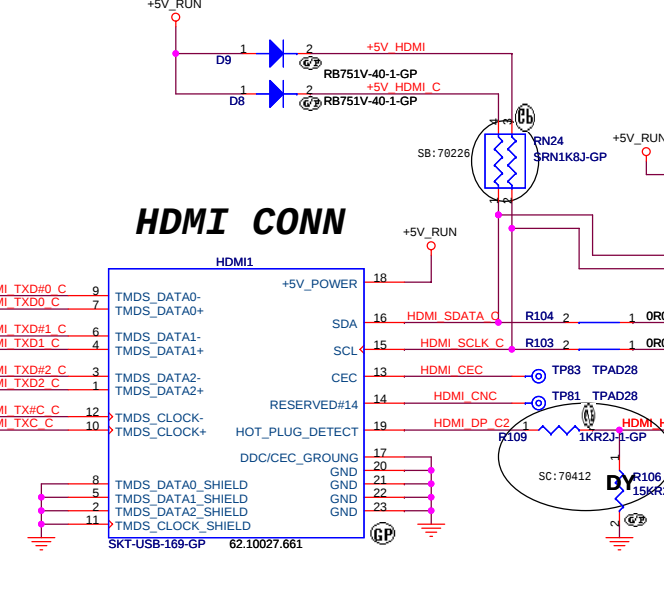
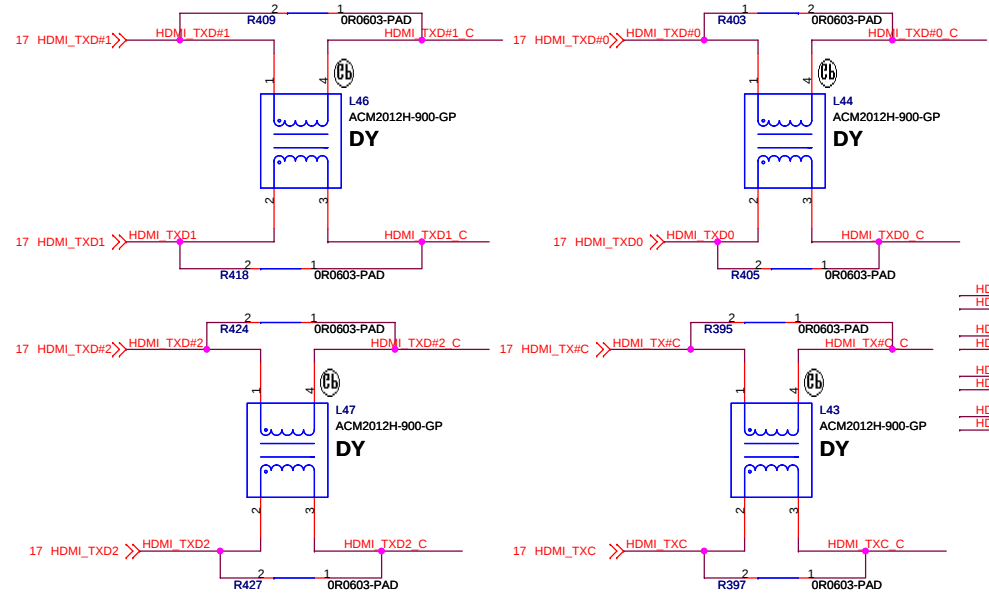
14 VGA_VSYNC



CRT conn.



Item18





Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Variant Name>

Thurman UMA

CRT/HDMI

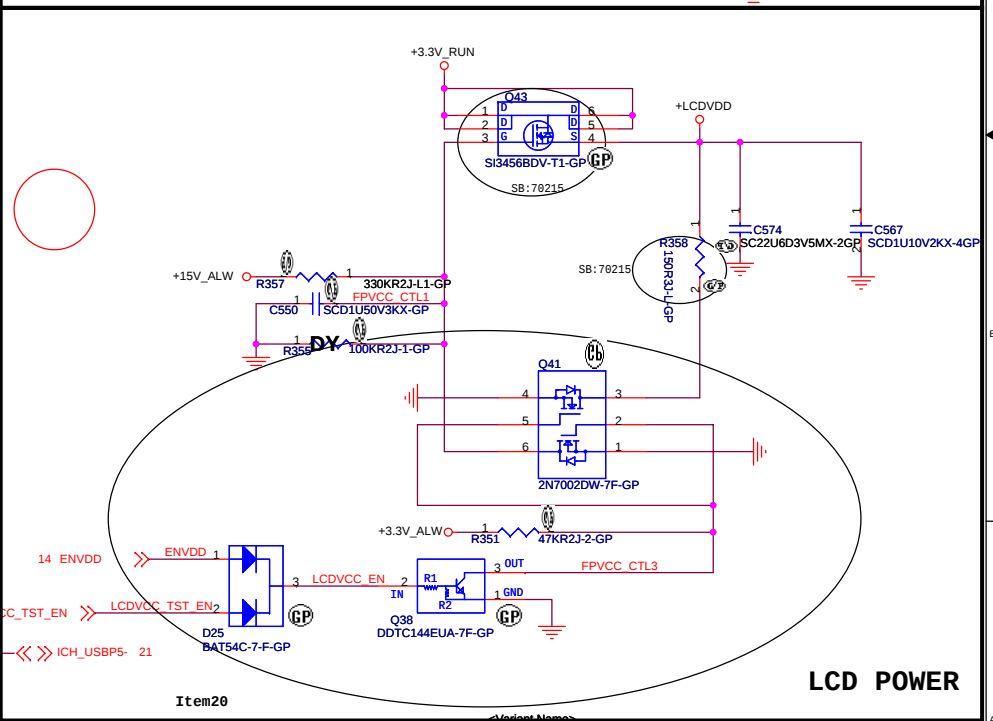
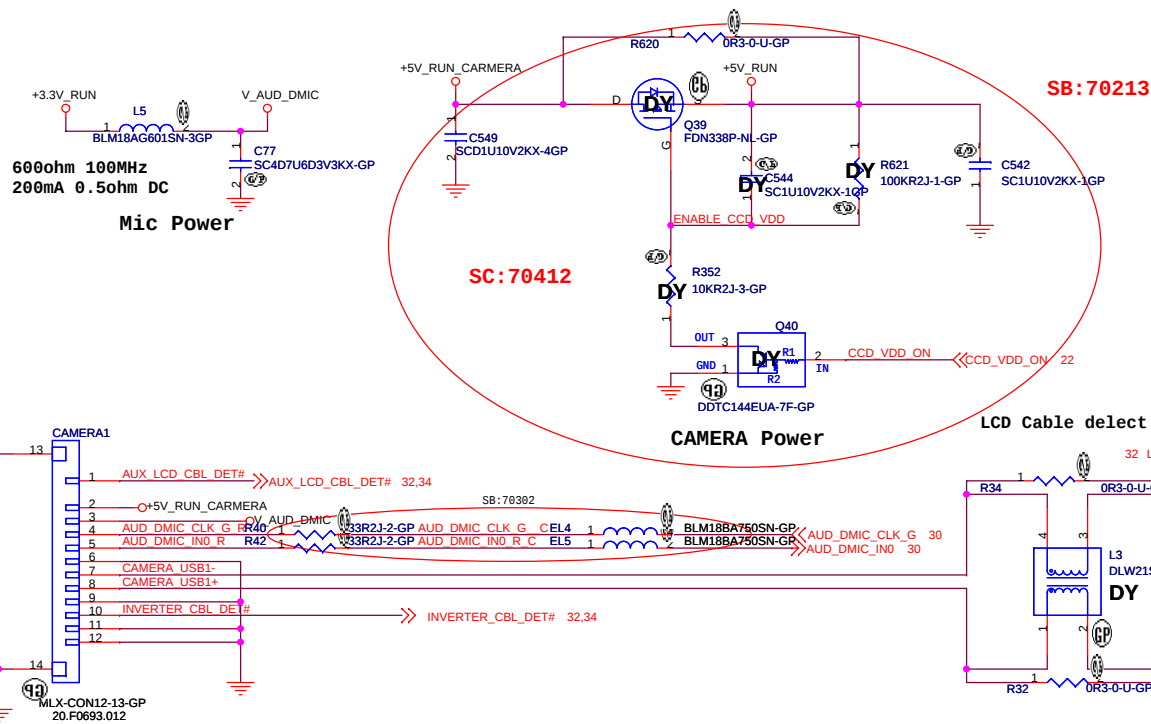
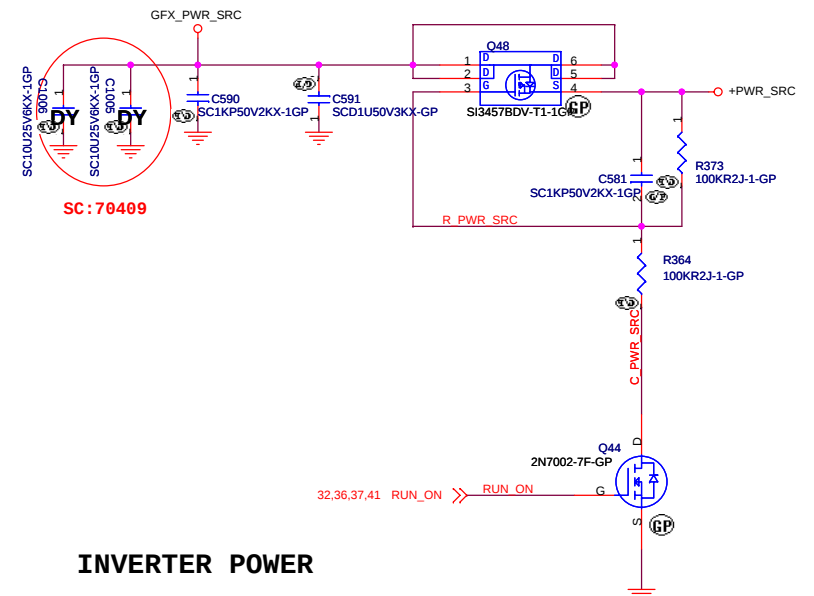
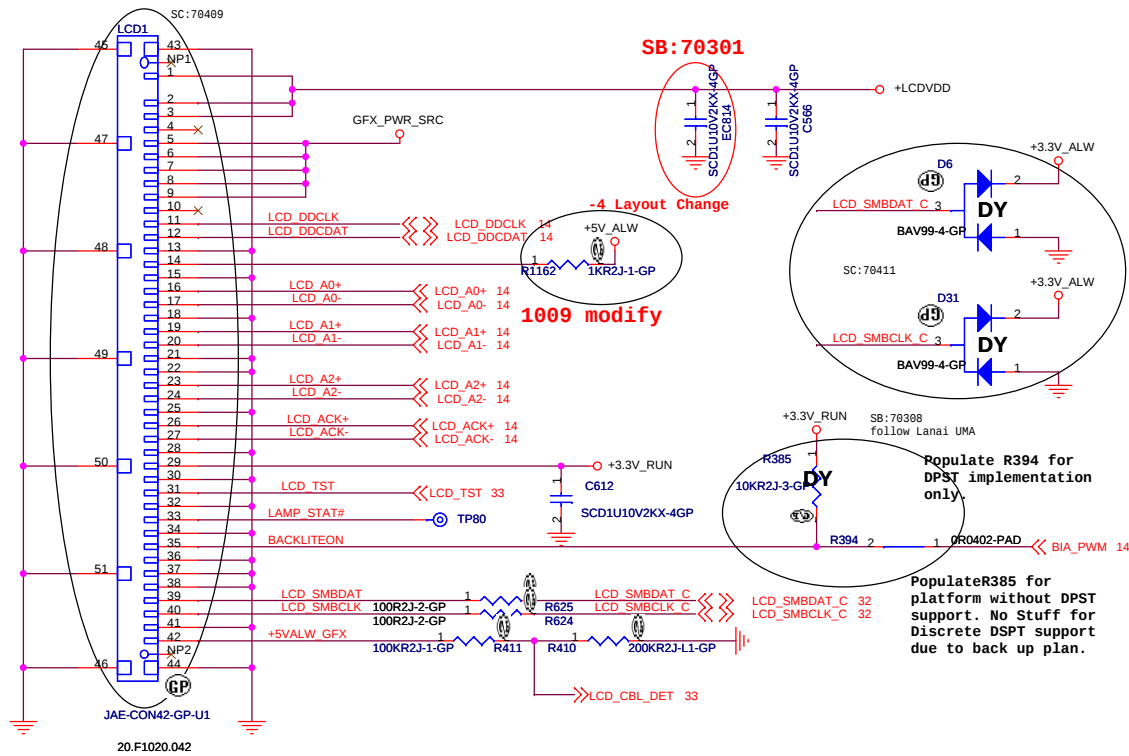
Size A3

Document Number

Date: Wednesday, November 07, 2007

Rev -1

Sheet 18 of 46



We would like to change X5 to 82.10026.021 and X3 to 82.30001.691.

ICH8-Strap PIN

integrated VccSus1_05,VccSus1_5,VccCl1_5		
ICH_INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCl1_05		
ICH_LAN100_SLP	High=Enable	Low=Disable

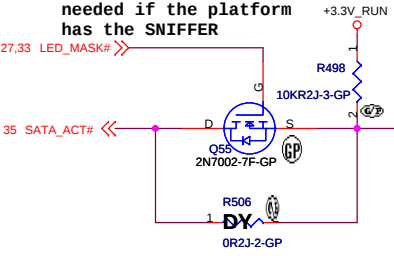
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17 ICH_AZ_S1392_BITCLK

30 ICH_AZ_CODEC_SYNC
17 ICH_AZ_S1392_SYNC

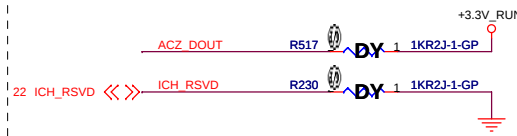
30 ICH_AZ_CODEC_RST#
17 ICH_AZ_S1392_RST#

30 ICH_AZ_CODEC_SDOUT
17 ICH_AZ_S1392_SDOUT

This circuit is only needed if the platform has the SNIFFER

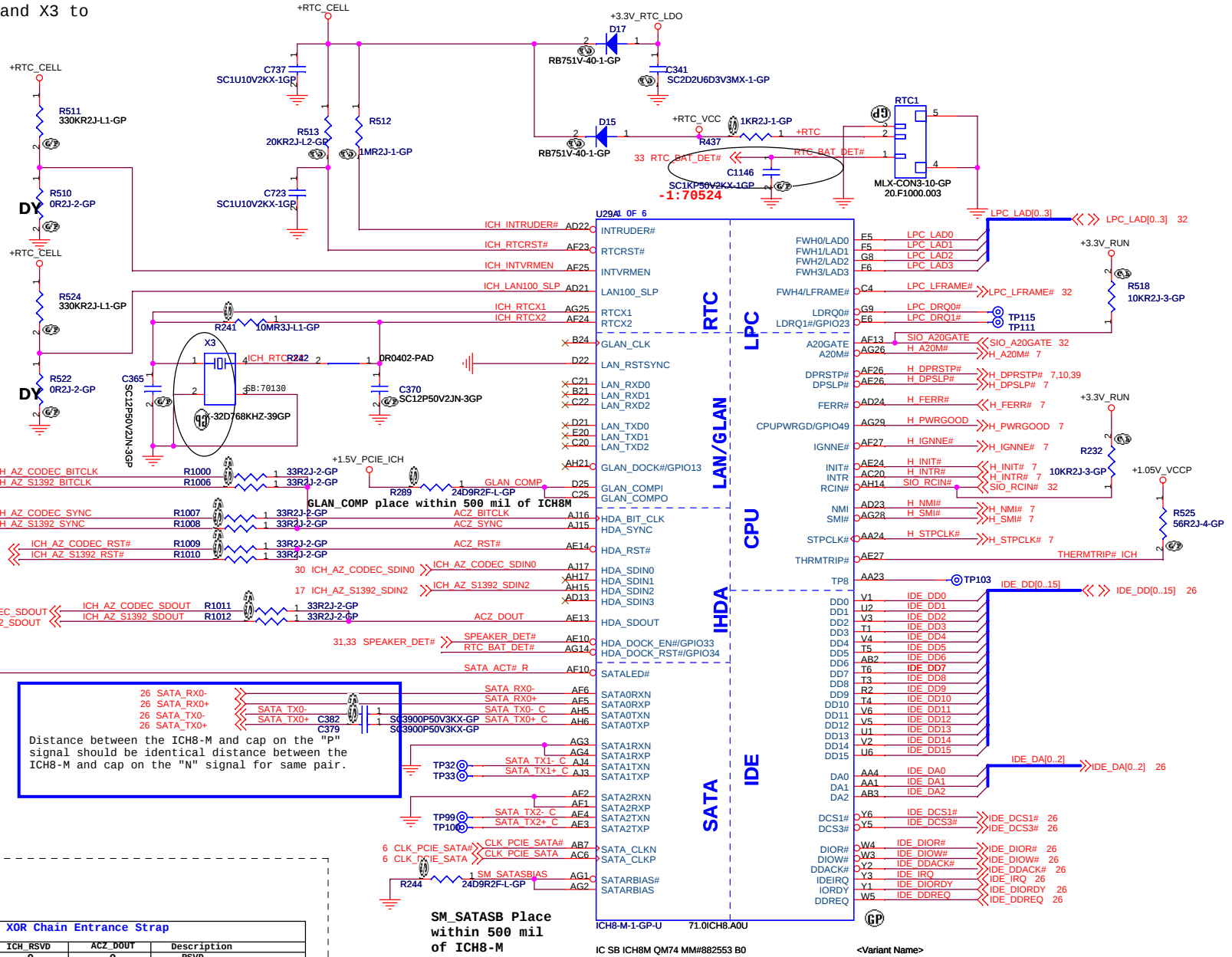


ICH8-Strap PIN



XOR Chain Entrance Strap		
ICH_RSVD	ACZ_DOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIe port cofig bit1

RTC circuitry



SM_SATASB Place within 500 mil of ICH8-M

Change to 71.0ICH8.M08

<Variant Name>



Title		
Thurman UMA		
Size	Document Number	Rev
A3	ICH8M-RTC/IDE/LPC/DHI (1/4)	-1
Date	Thursday, November 22, 2007	Sheet 20 of 46

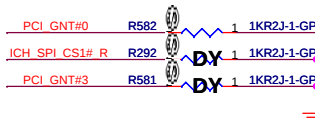
ICH8-Strap PIN

BOOT BIOS Strap

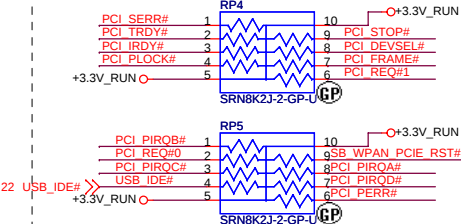
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

A16 swap override strap

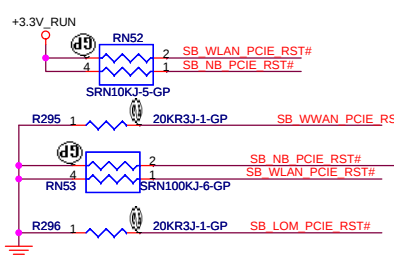
PCI_GNT#3 (R168)	low = A16 swap override enable high = default
------------------	--



PCI I/F PULL HIGH

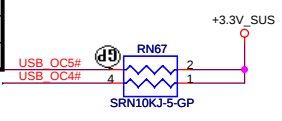


BIOS should not enable the internal GPIO pull up

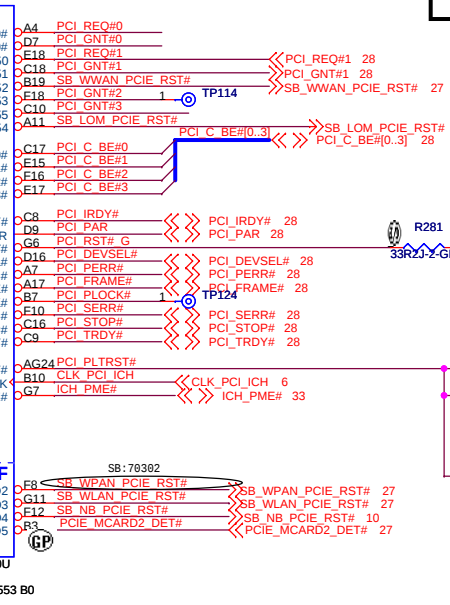
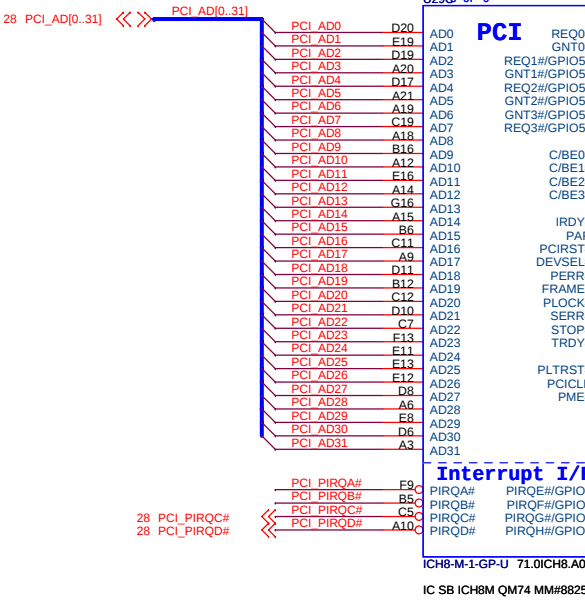
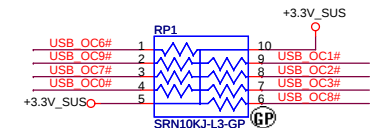


PCIE Interface Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	LAN



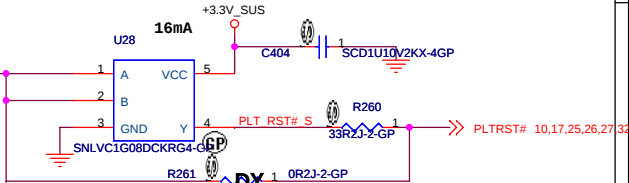
Layout Note:
Place R235, R237 and R234 within 500 mils from ICH.



	IDSEL	INT	REQ	GNT
1394/MediaCard	AD17	C D	1	1

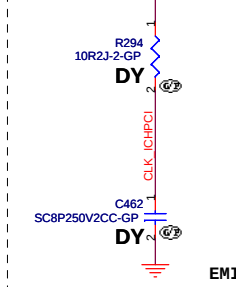
PCI Interface Routing

Add Buffers as need for Loading and Fanout concerns



CLK ICH_14M EMI Mode

Place close to ICH8-M



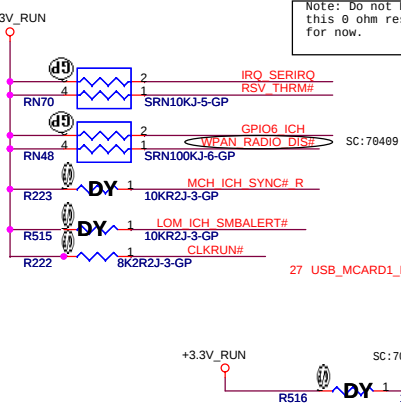
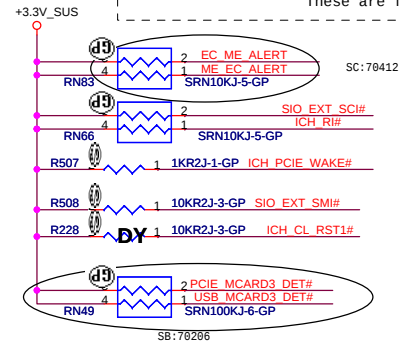
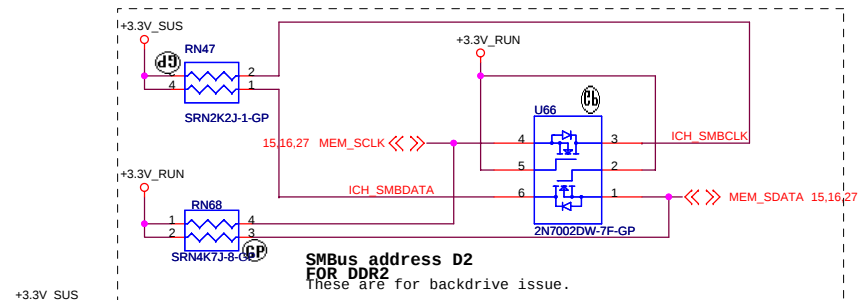
USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	MINI Card WLAN
USB9	

<Variant Name>



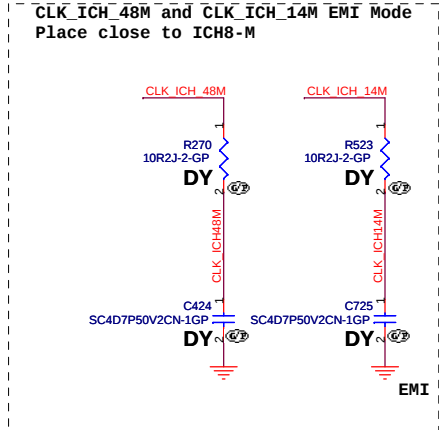
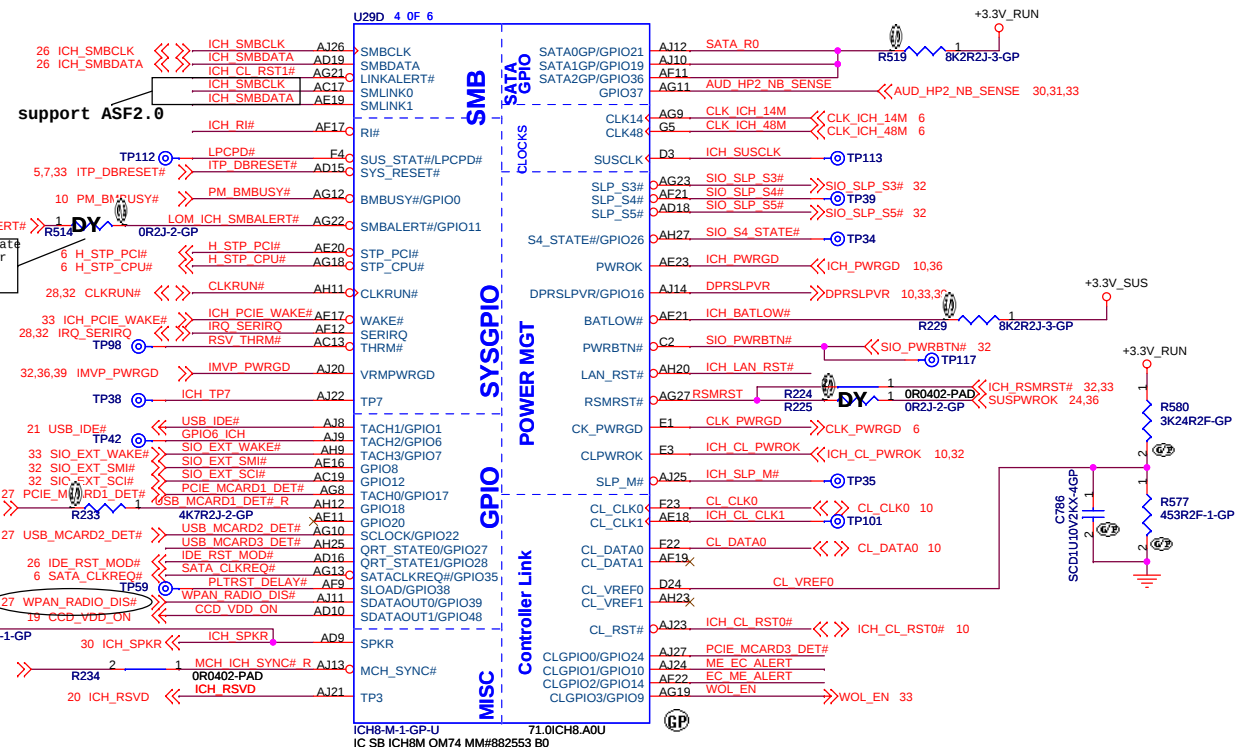
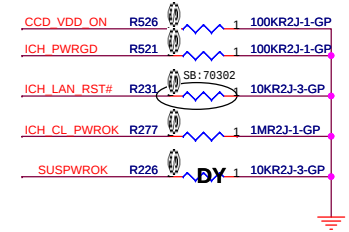
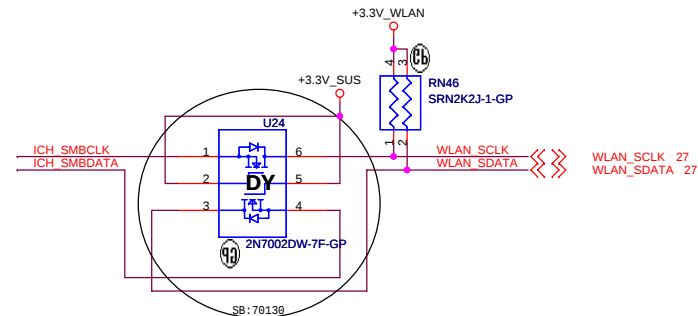
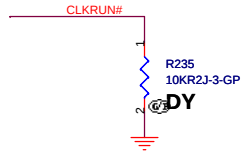
Size	Document Number	Rev
A3	ICH8M-PCIE/USB/SPI/DMI (2/4)	-1
Date:	Thursday, November 22, 2007	Sheet 21 of 46

USB8BIAS close to ICH8M 500 mils and Trace impedance should be 60 ohm +/- 15%



ICH8-Strap PIN

No Reboot Strap
ICH_SPKR LOW = Defaule
High=No Reboot



SSID = THERMAL

REM_DIODE1_N and REM_DIODE1_P
routing Trace width and Spacing
use 10 / 10 mil

Place inside CPU socket

C300 Please close to Guardian

Close to Pin5, Pin6

Close to Pin9

C276 Please Close to Guardian

Place near the bottom SODIMM CONN

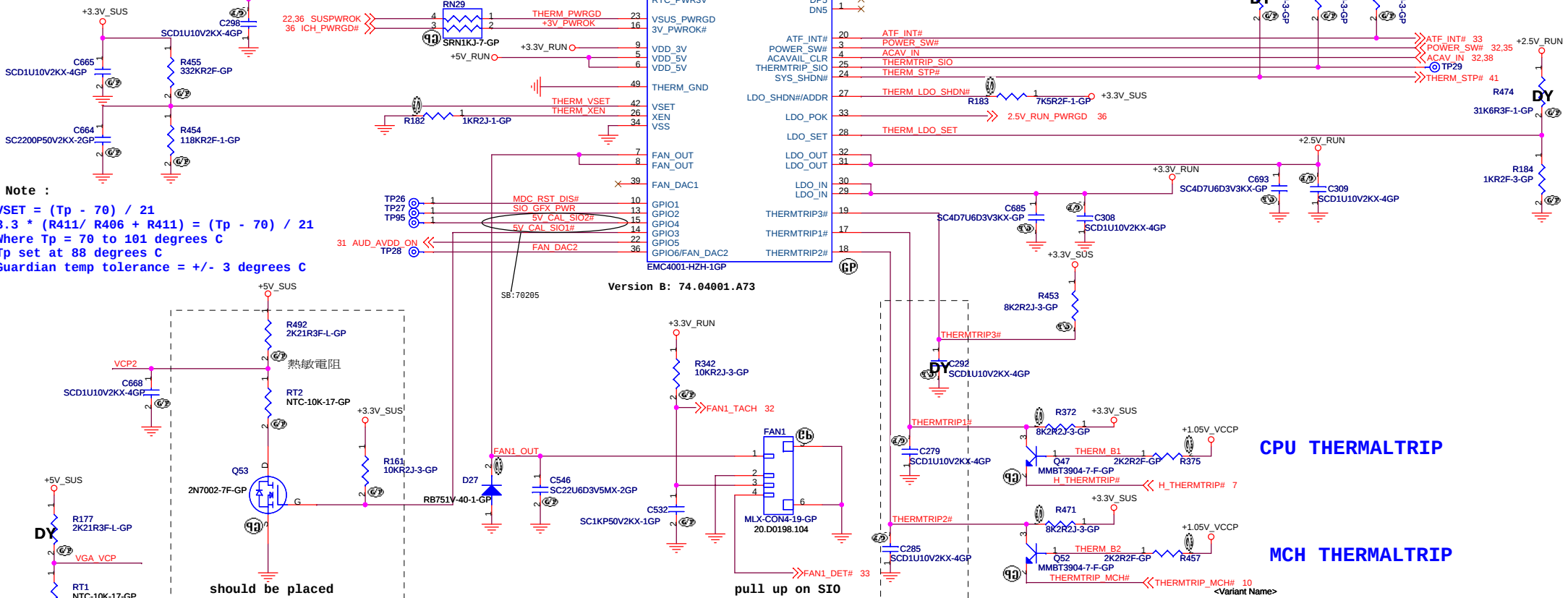
REM_DIODE4_N and REM_DIODE4_P
routing Trace width and Spacing
use 10 / 10 mil

Thermal sensor for Mini Card
should be placed TOP Side under WWAN CARD

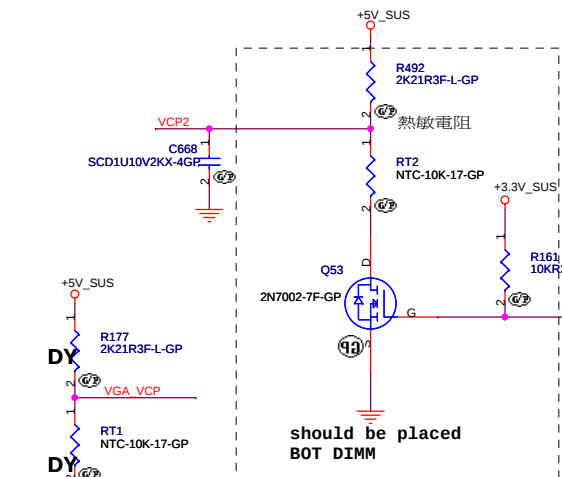
C260 Please Close to Guardian

H_THERMDA and H_THERMDC
routing Trace width and
Spacing use 10 / 10 mil

C295 Please close to Guardian



Note :
 $VSET = (T_p - 70) / 21$
 $3.3 * (R411 / R406 + R411) = (T_p - 70) / 21$
 Where $T_p = 70$ to 101 degrees C
 T_p set at 88 degrees C
 Guardian temp tolerance = ± 3 degrees C



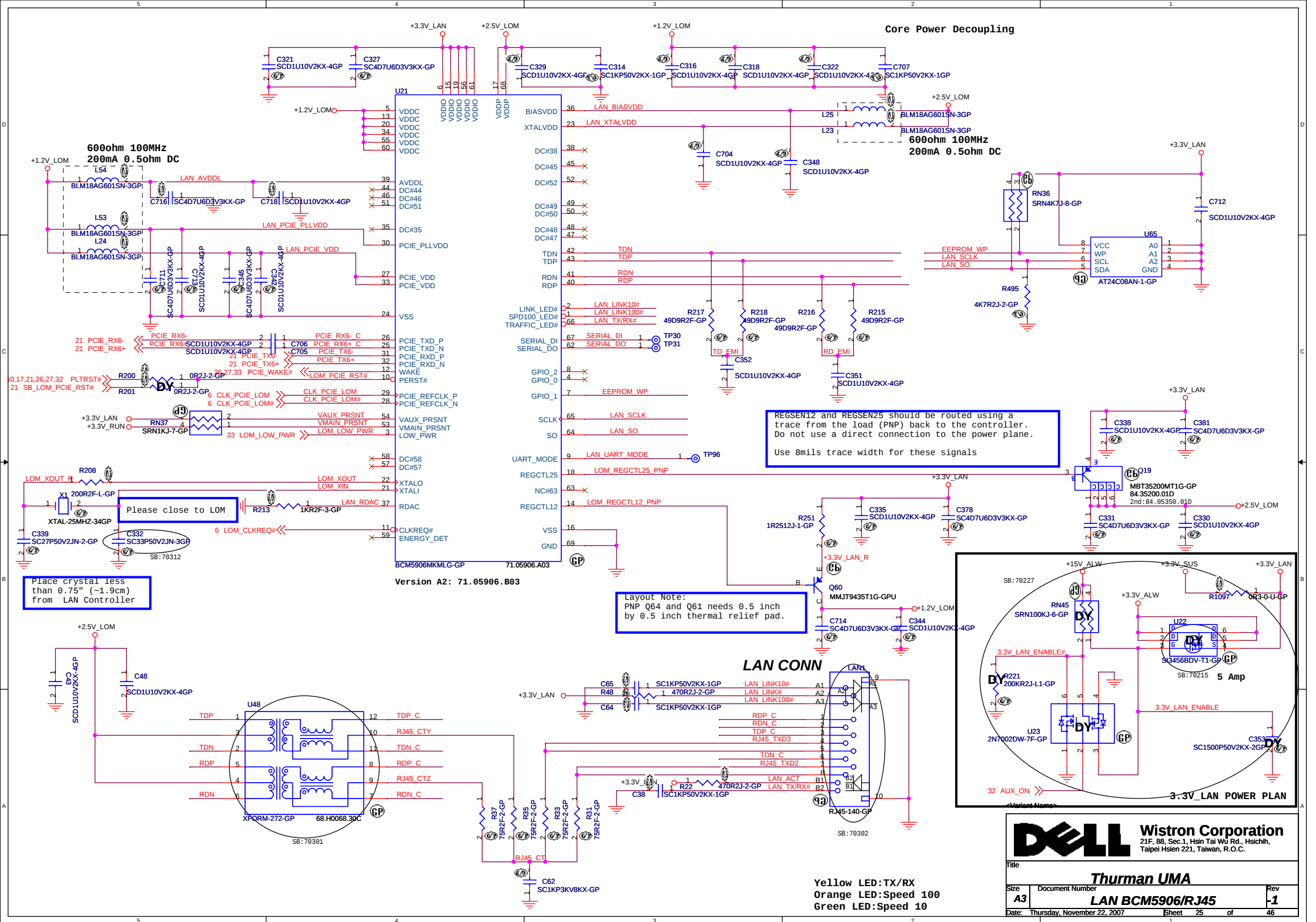
C916, C459, C472 Please Close to Guardian

CPU THERMALTRIP

MCH THERMALTRIP

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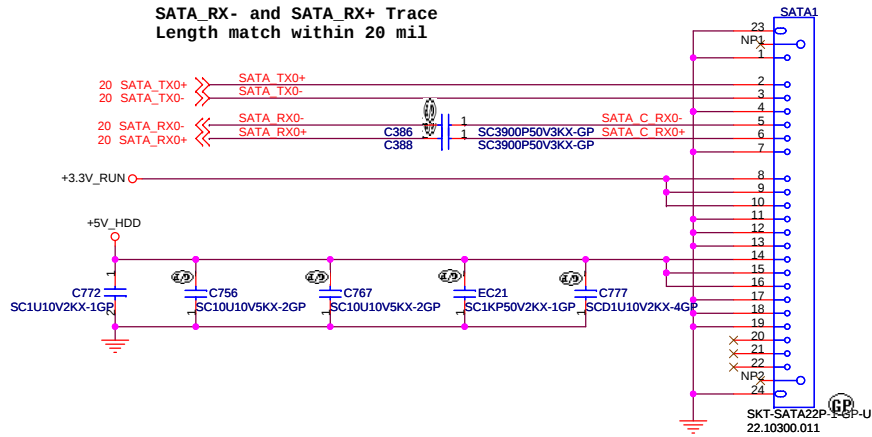
Title Thurman UMA		
Size A3	Document Number FAN/EMC4001	Rev -1
Date: Wednesday, November 07, 2007	Sheet 24	of 46



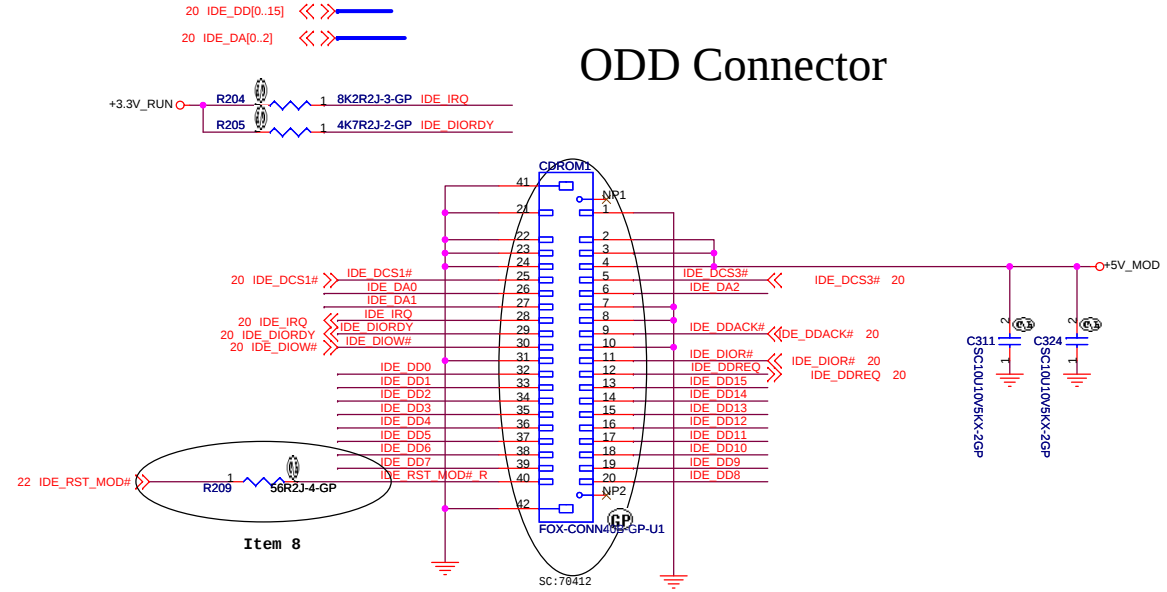
SSID = IDE & SATA

SATA HDD Connector

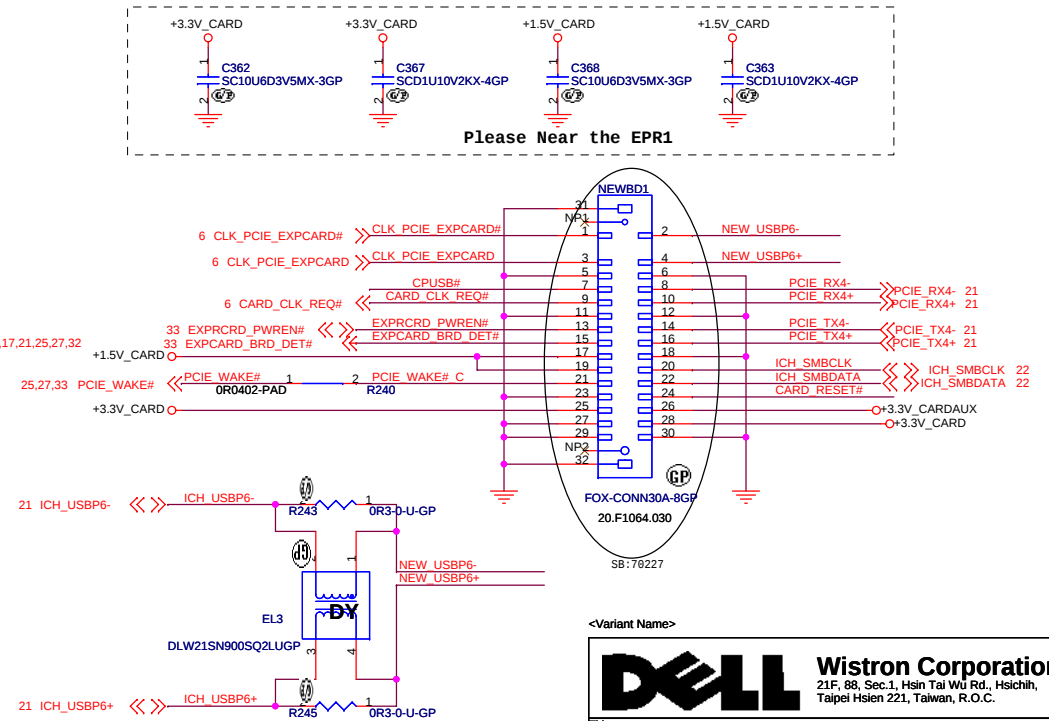
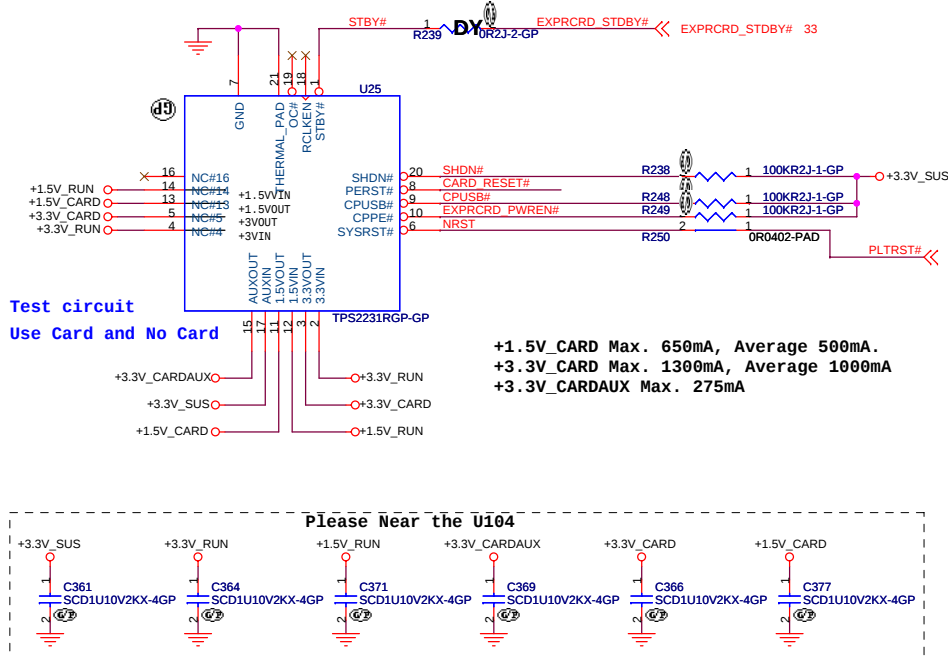
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil



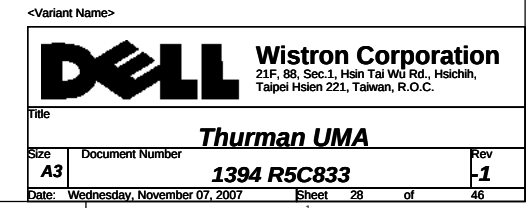
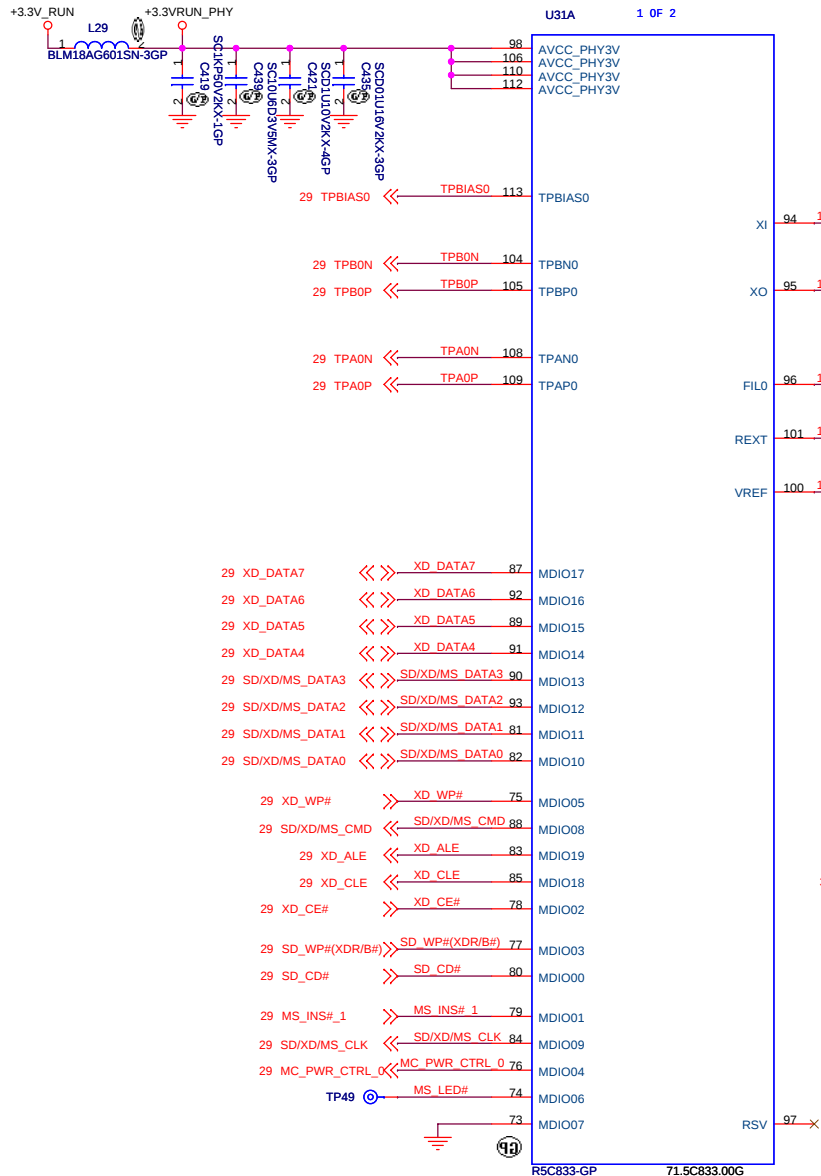
ODD Connector



Express Card

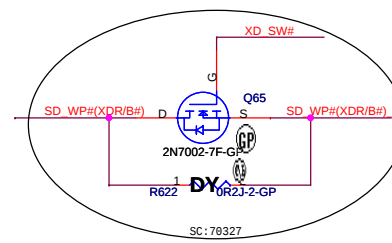
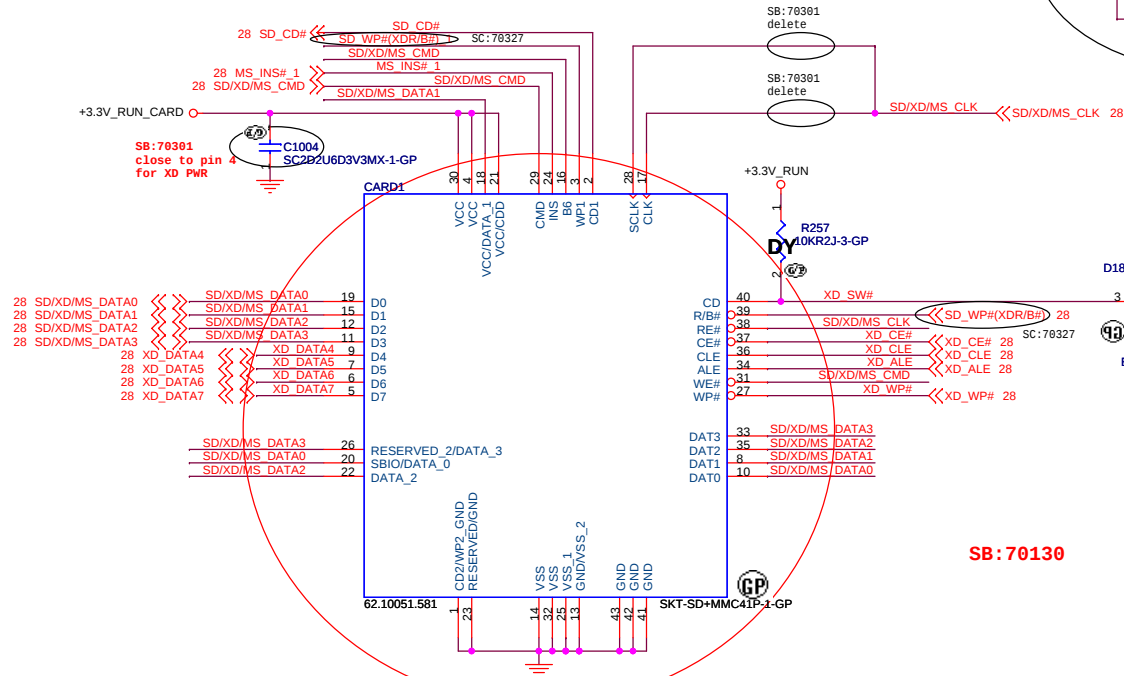


SSID = 1394

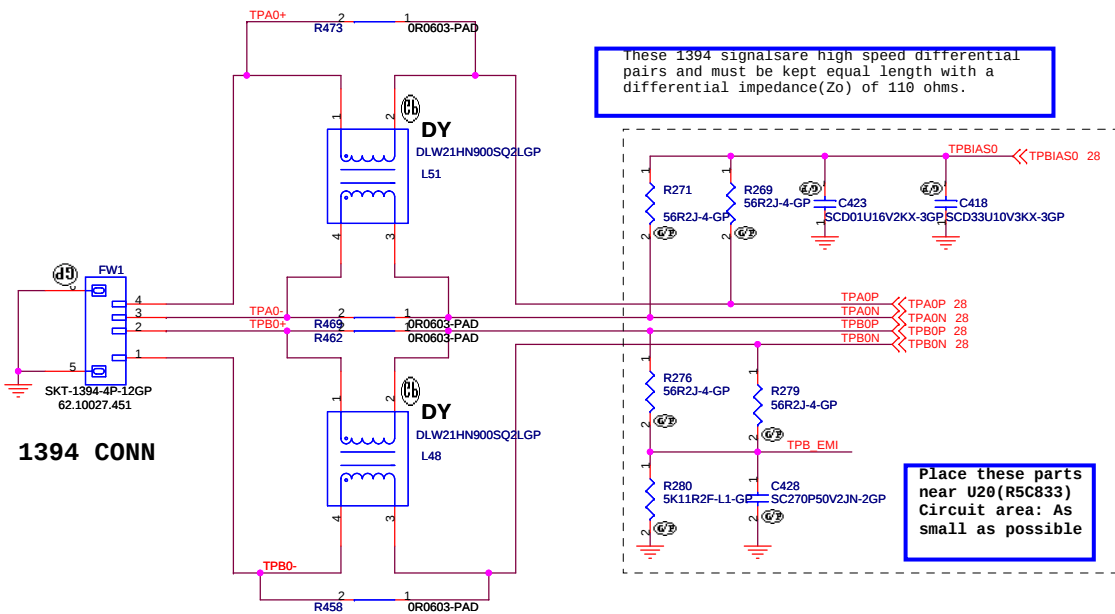
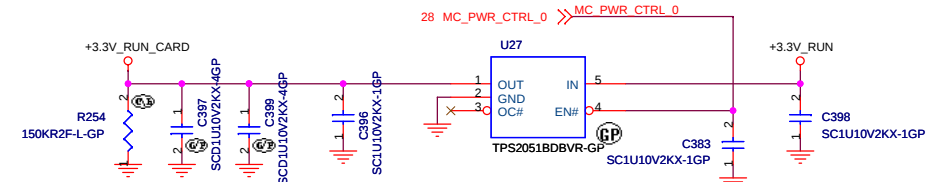


SSID = 1394

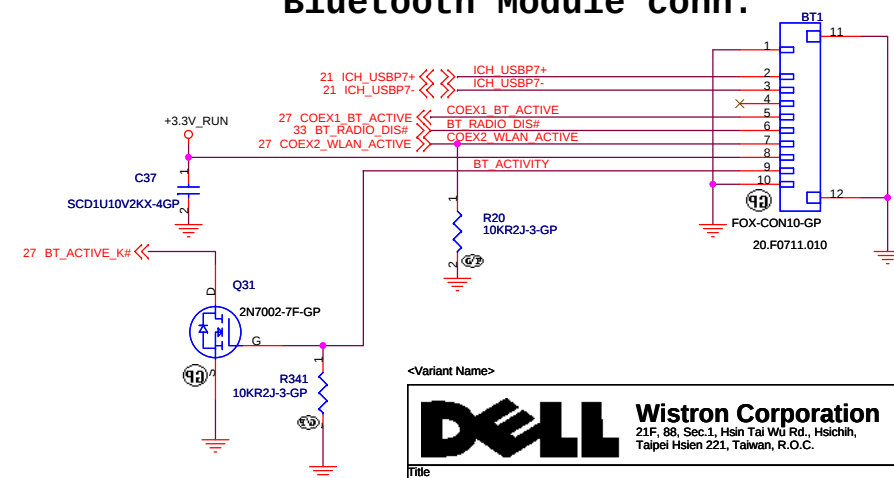
Card Reader CONN



SNIFFER BOARD CONN



Bluetooth Module conn.



<Variant Name>



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Title

Thurman UMA

Size

Document Number

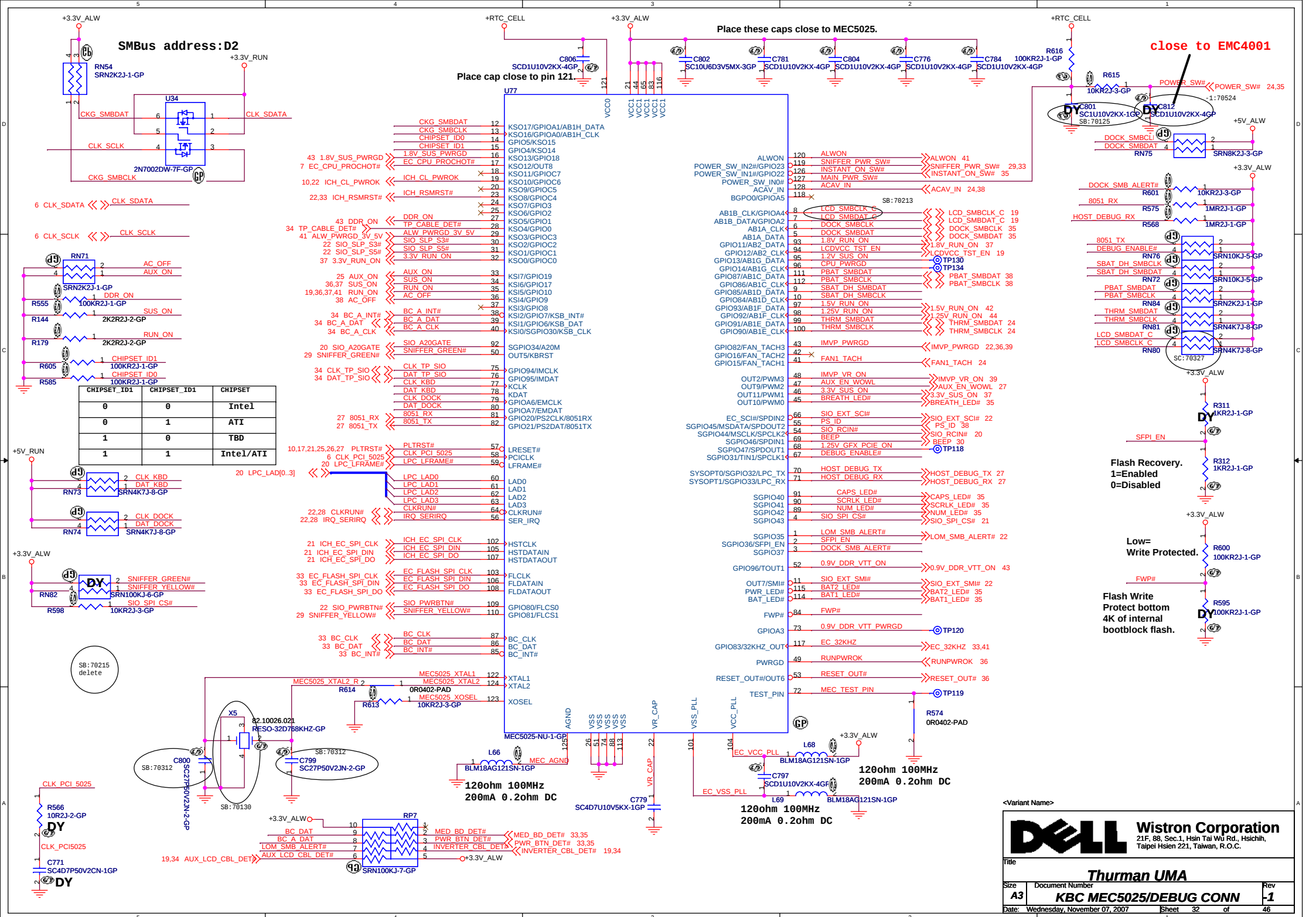
8in1 /1394/SNIFFER BD CON/BT

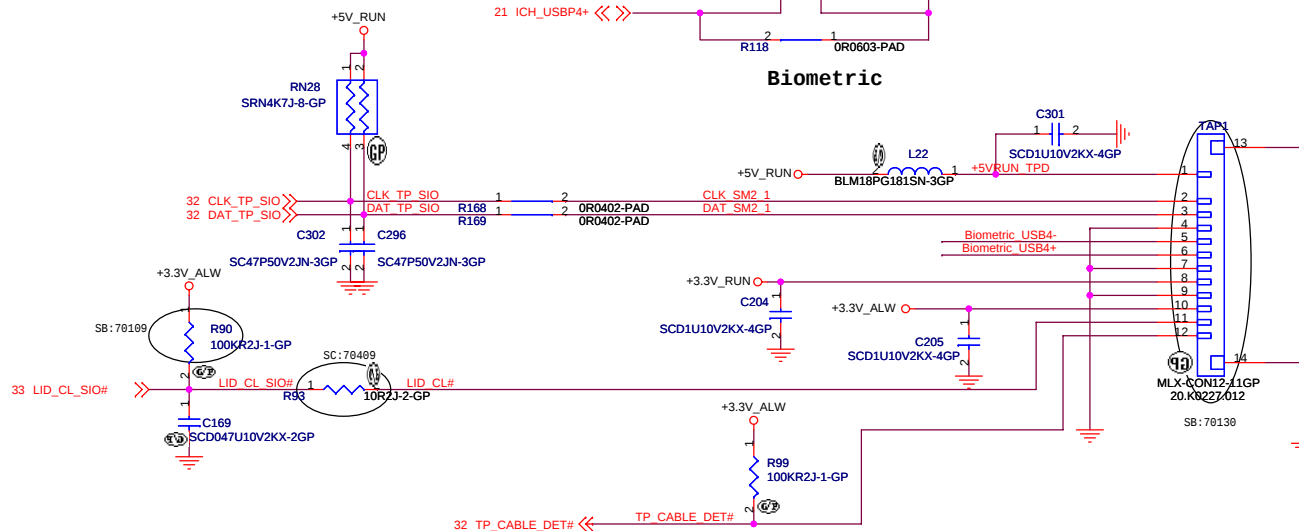
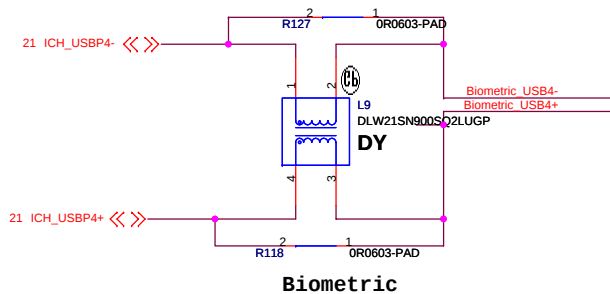
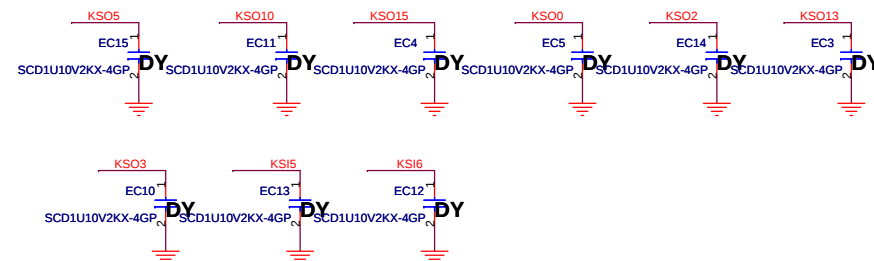
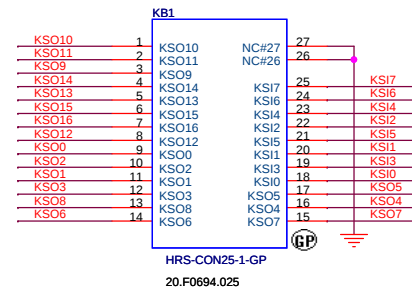
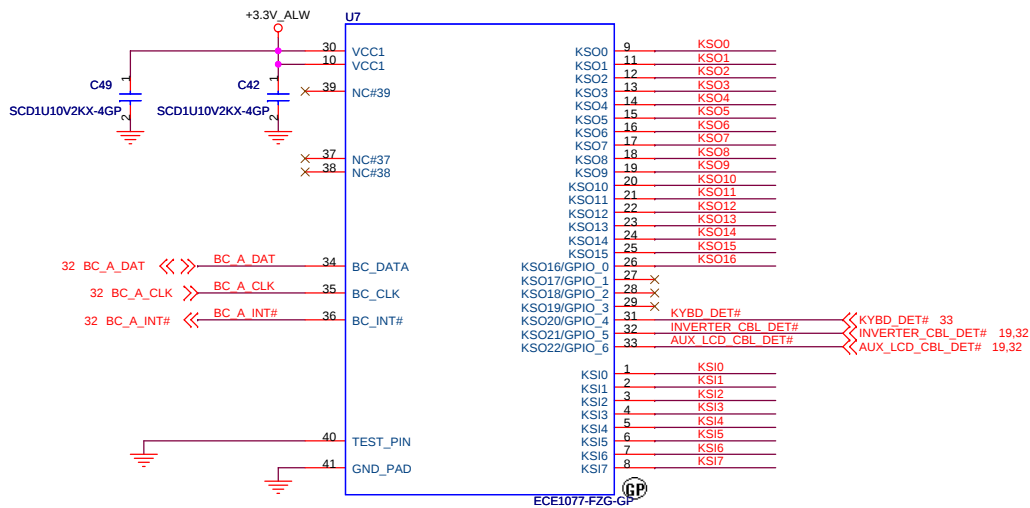
Rev

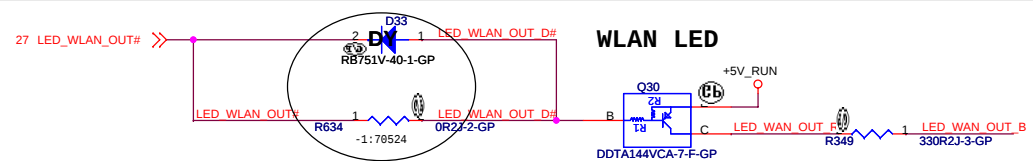
Date: Wednesday, November 07, 2007

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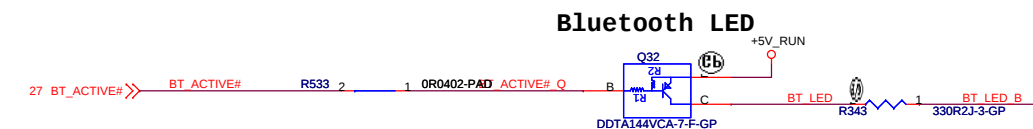
46



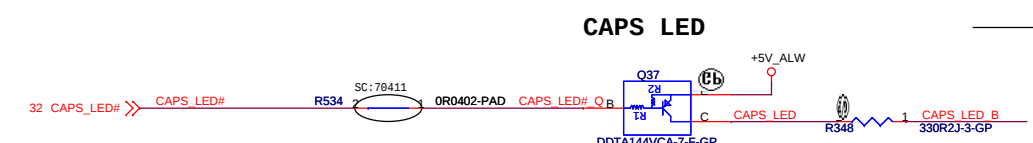




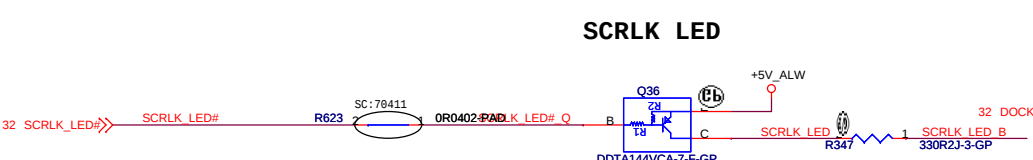
WLAN LED



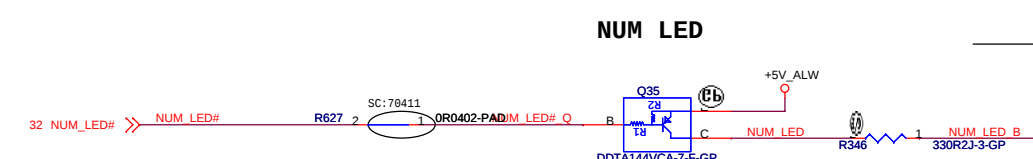
Bluetooth LED



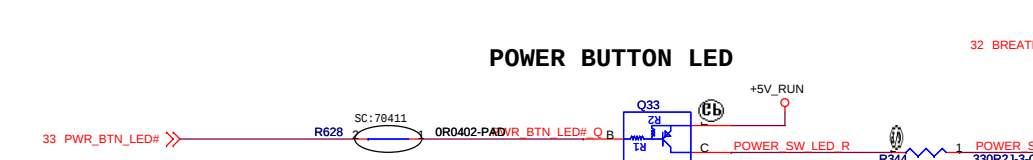
CAPS LED



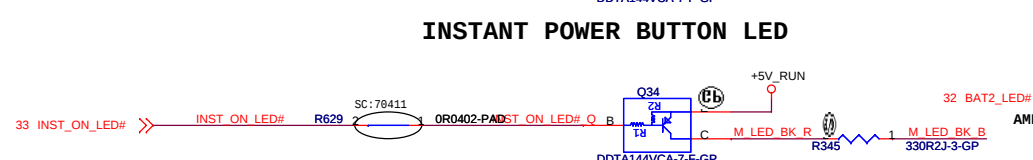
SCRLK LED



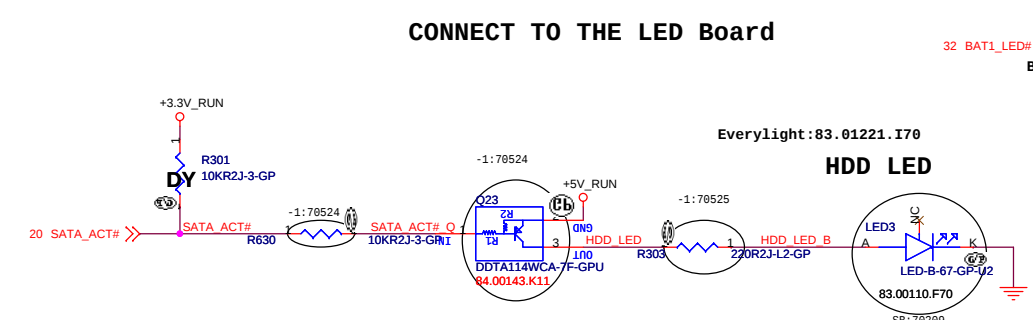
NUM LED



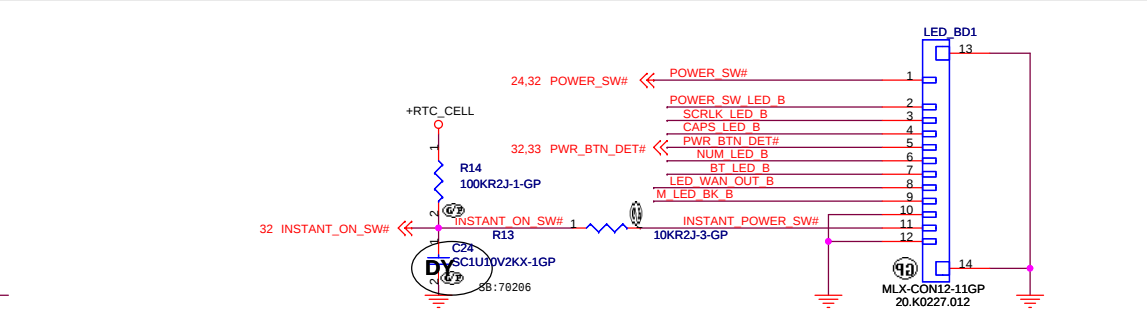
POWER BUTTON LED



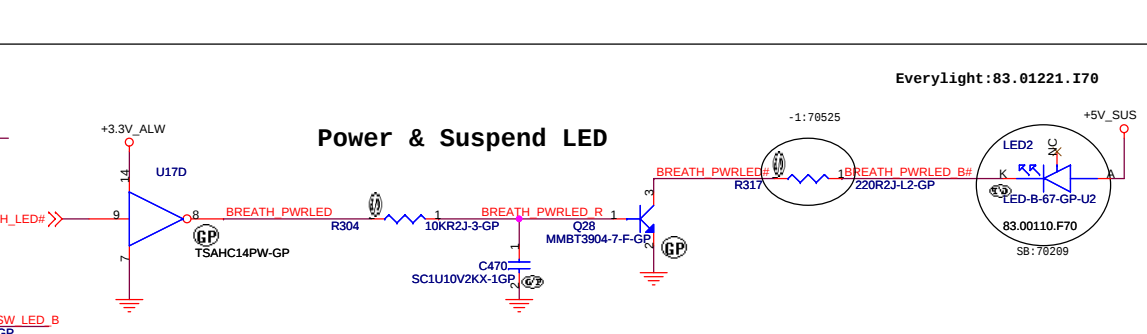
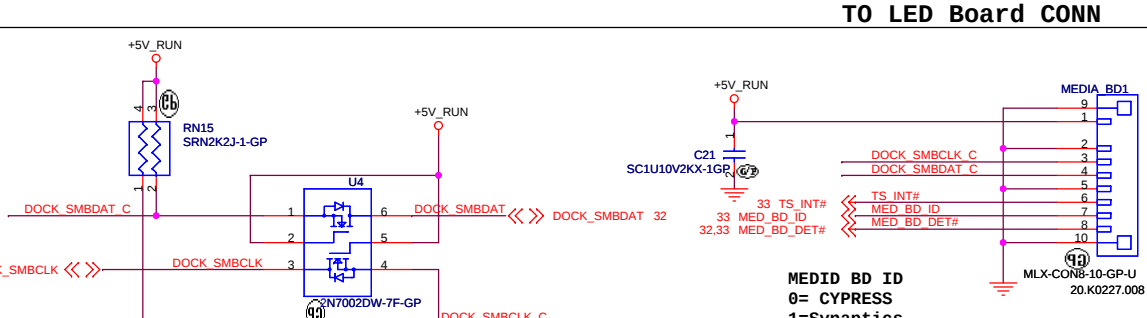
INSTANT POWER BUTTON LED



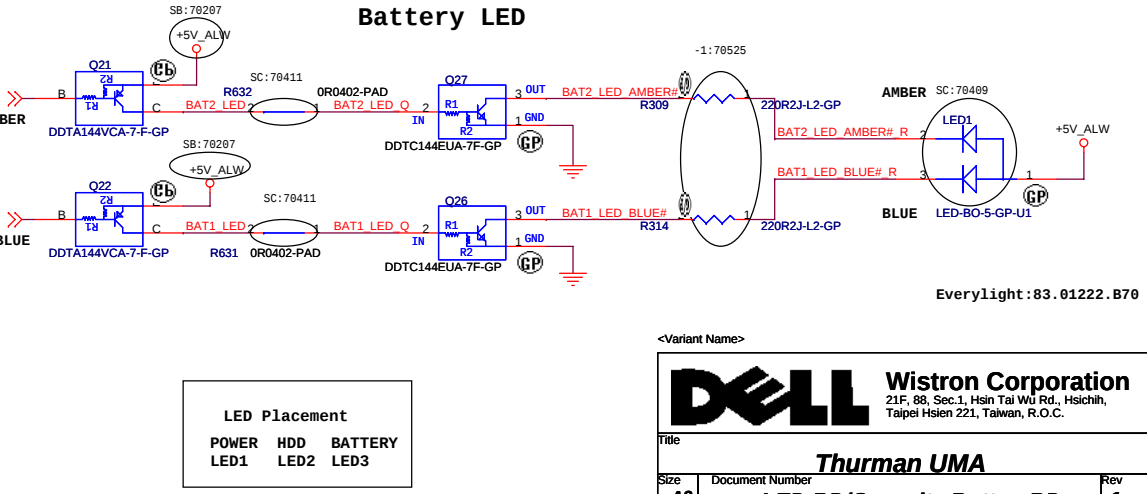
HDD LED



T0 LED Board CONN



Power & Suspend LED



Battery LED

LED Placement
POWER LED1
HDD LED2
BATTERY LED3

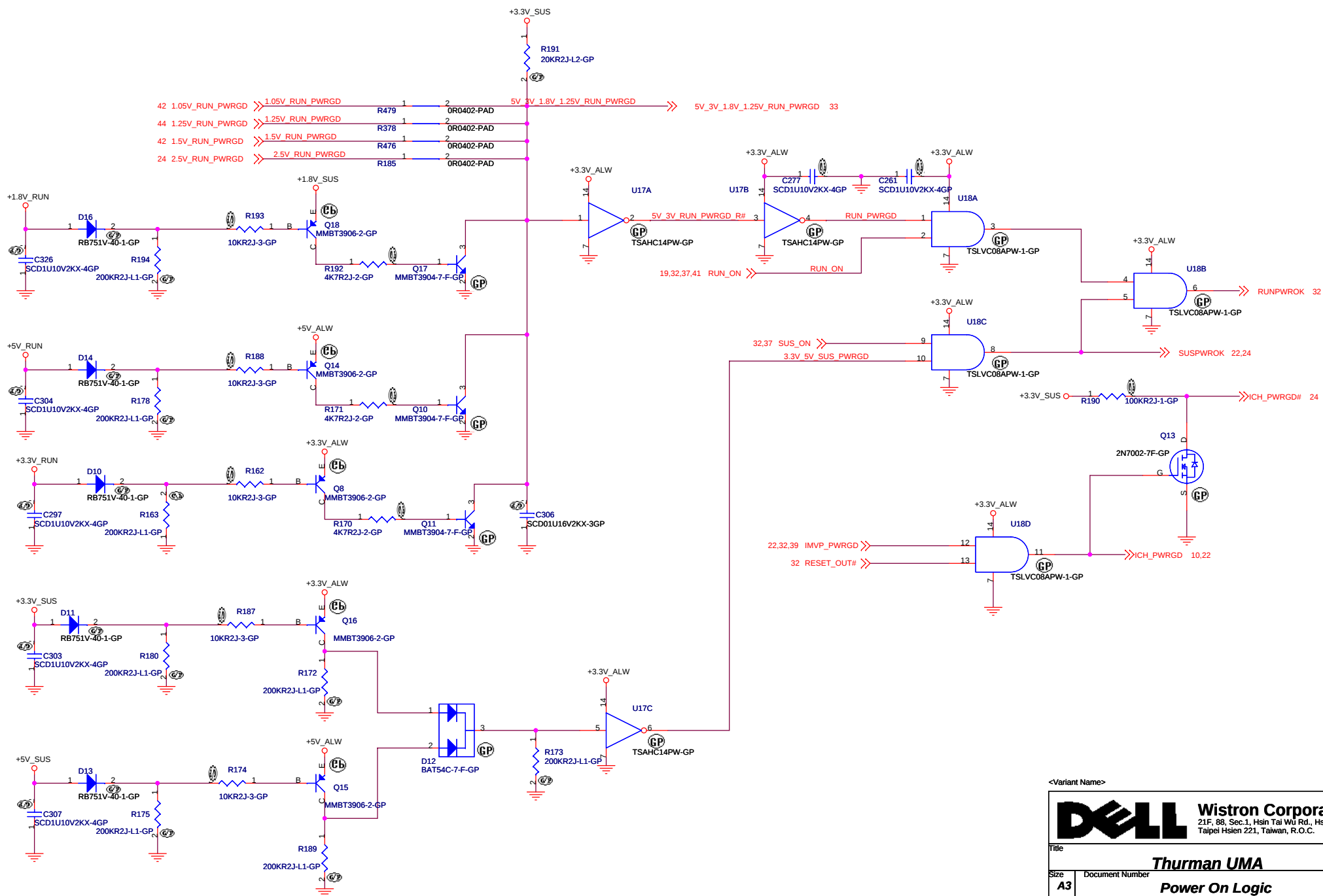
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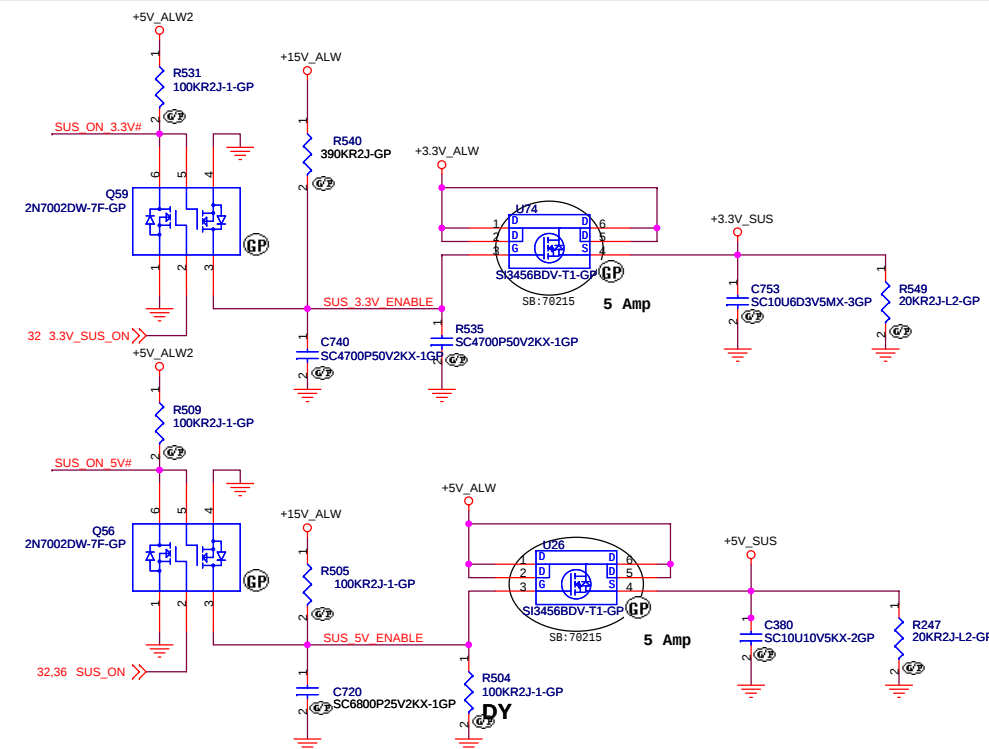
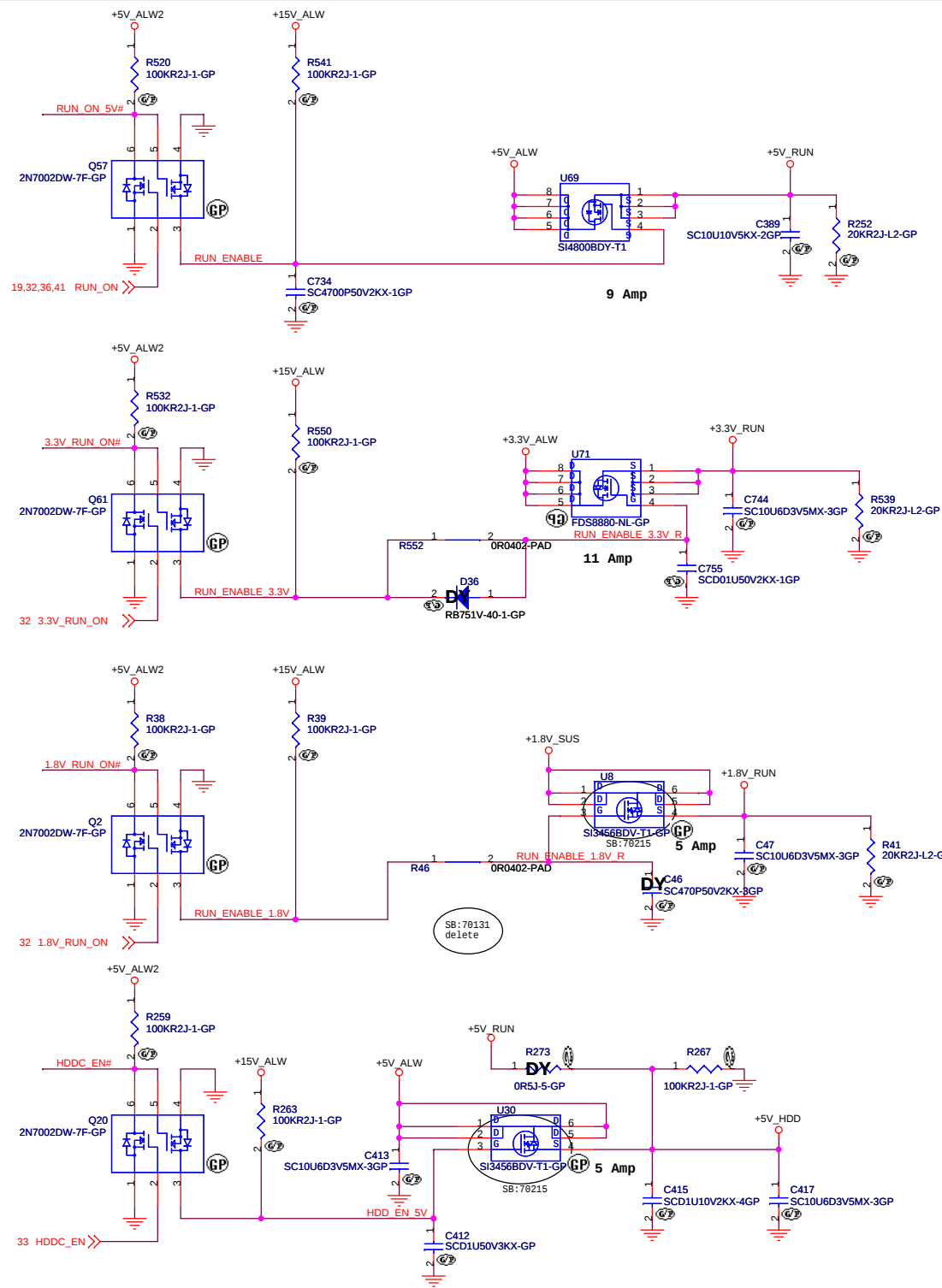
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thurman UMA**

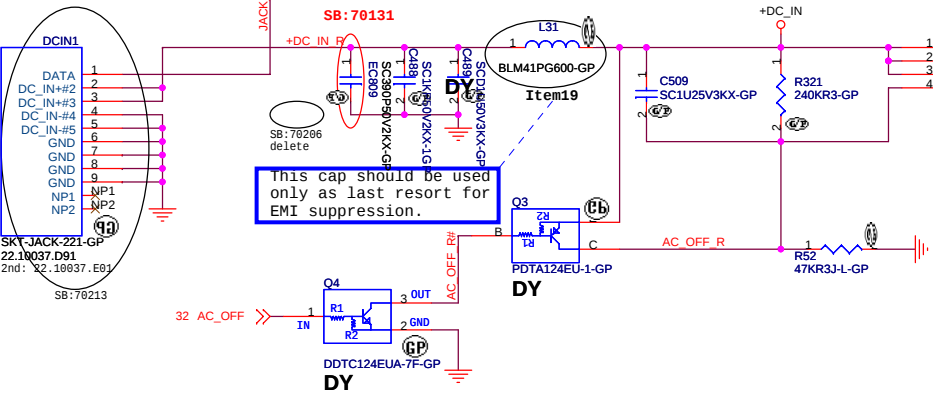
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Date: Wednesday, November 07, 2007 Sheet 35 of 46





Adapter In

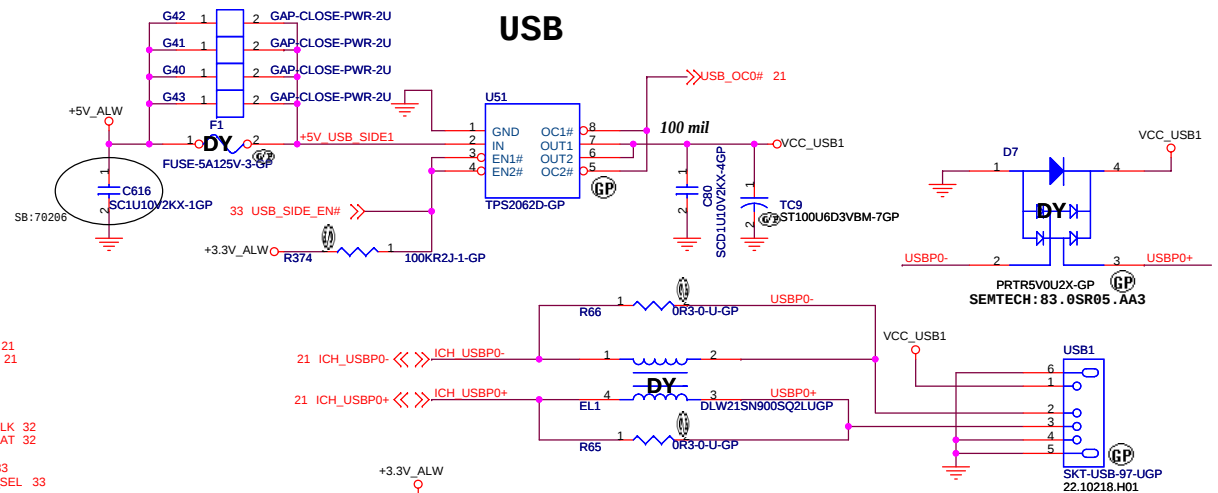


Reserved for EMI

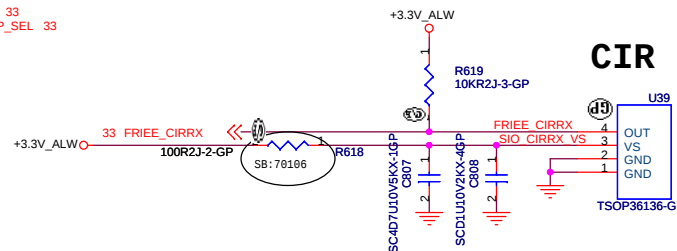
+DC IN

Place near DCIN1

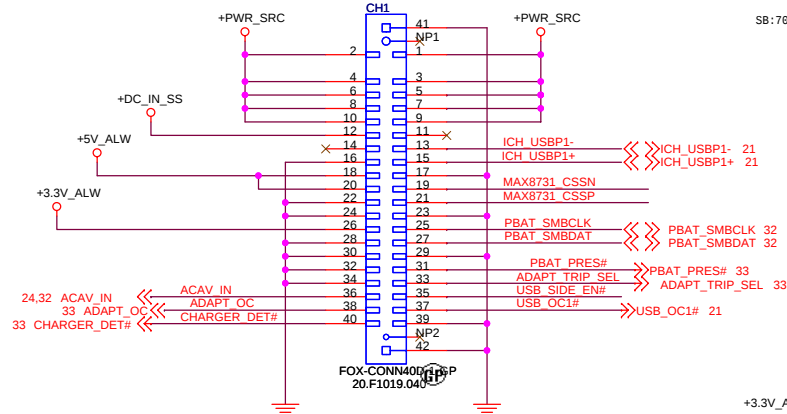
USB



CIR



CHARGER Board CONN



<Variant Name>

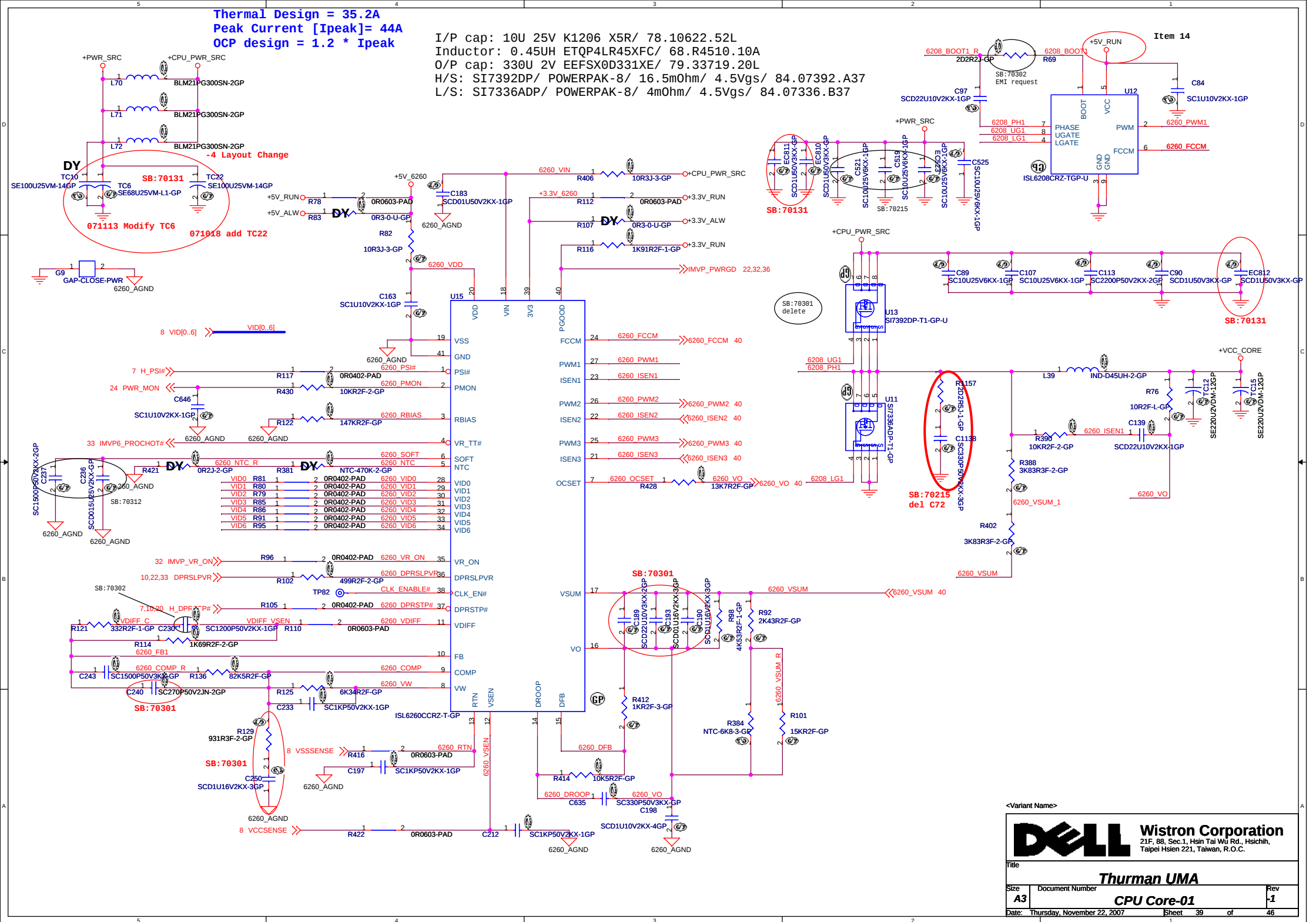


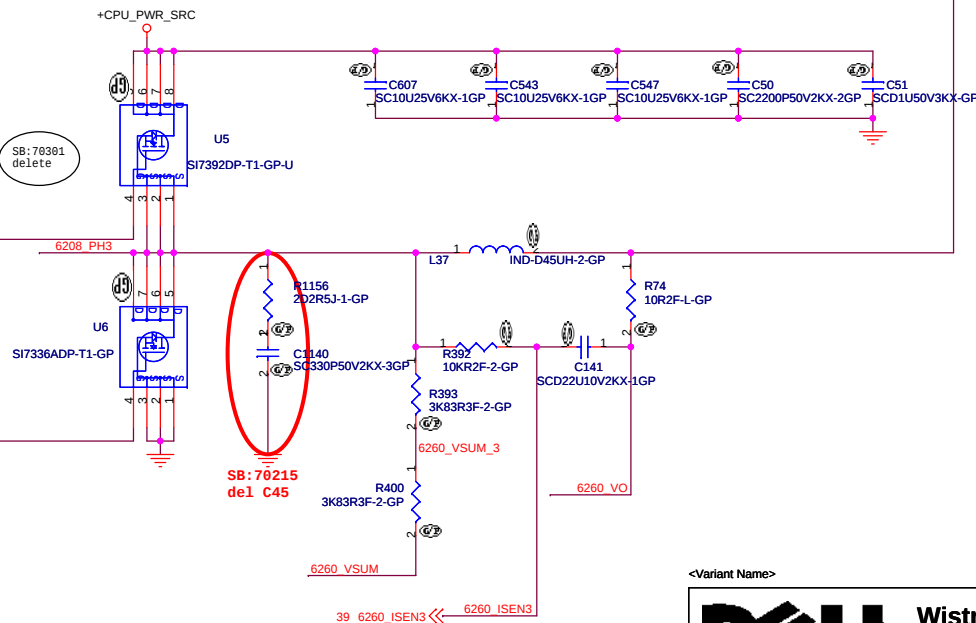
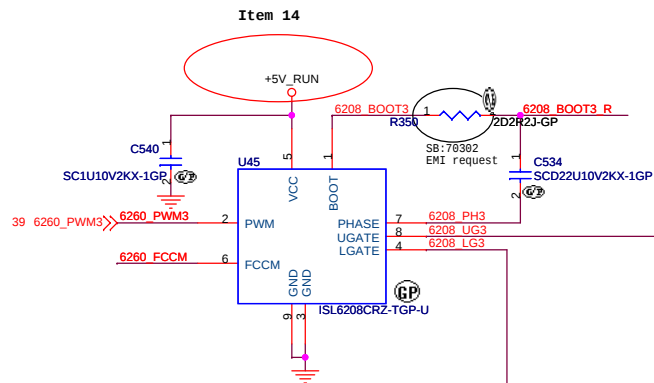
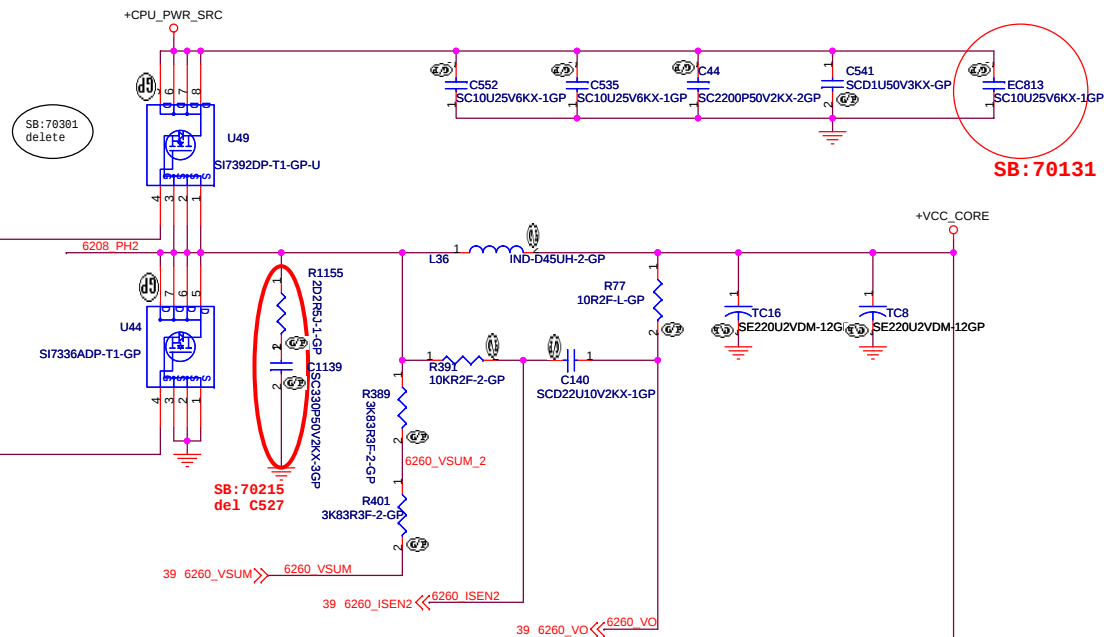
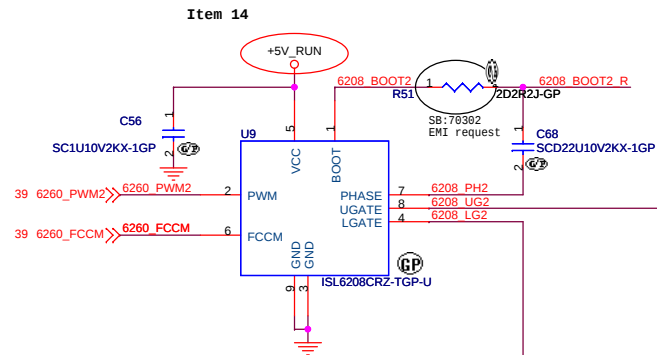
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

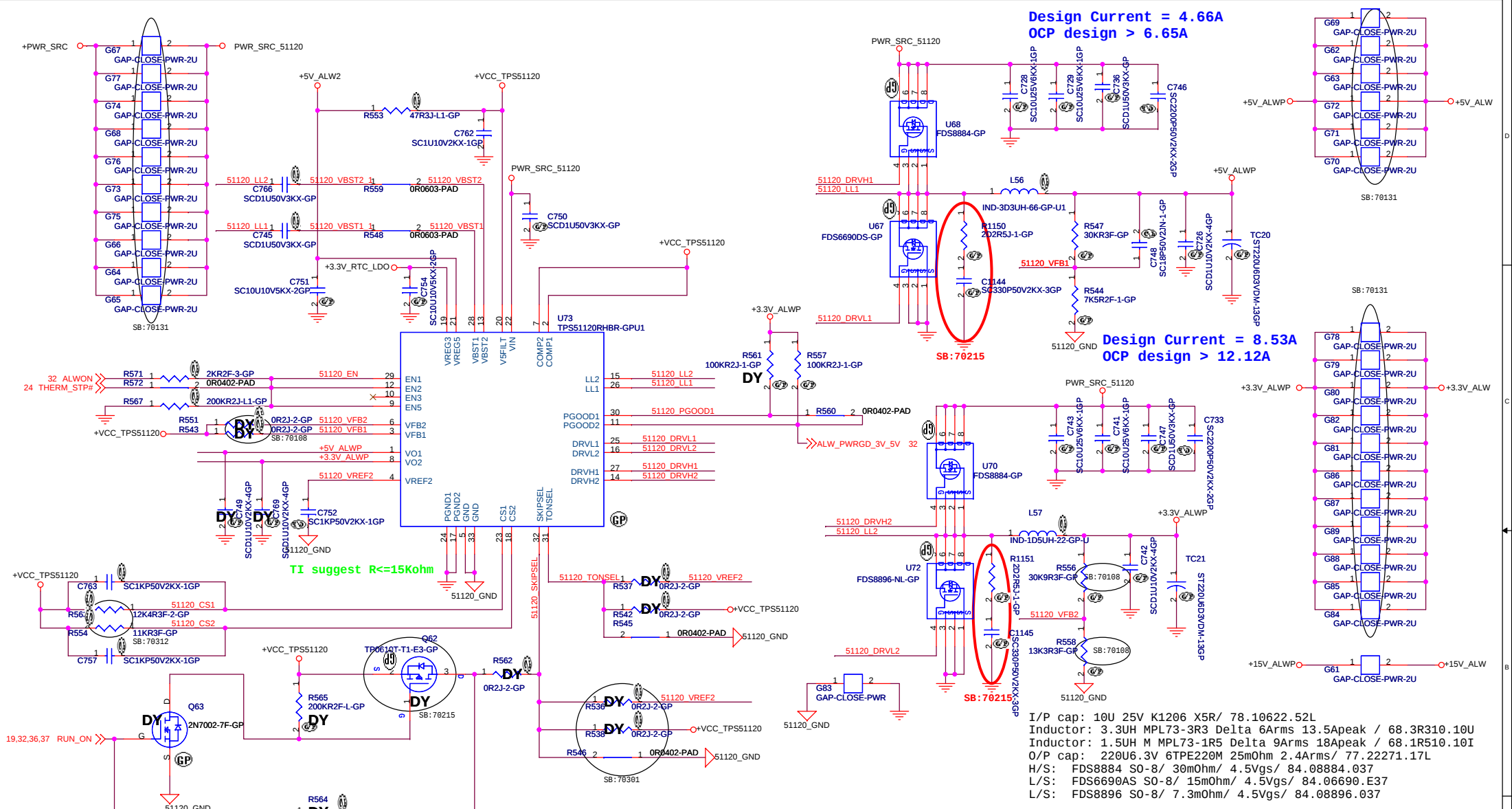
Title		Thurman UMA	
Size	Document Number	Rev	
A3	DCIN/USB/CIR/CHARGER CONN	-1	
Date:	Thursday, November 22, 2007	Sheet	38 of 46

Thermal Design = 25.5A
Peak Current [Ipeak]= 44A
OCP design = 1.2 * Ipeak

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.45UH ETQP4LR45XFC/ 68.R4510.10A
O/P cap: 330U 2V EEF5X0D331XE/ 79.33719.20L
H/S: SI7392DP/ POWERPAK-8/ 16.5mOhm/ 4.5Vgs/ 84.07392.A37
L/S: SI7336ADP/ POWERPAK-8/ 4mOhm/ 4.5Vgs/ 84.07336.B37







	GND	VREF2	FLOUT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 ON

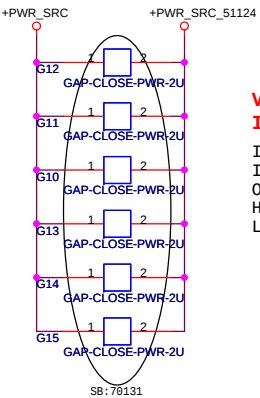
Variant Name>

DELL Wistron Corporation
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Title

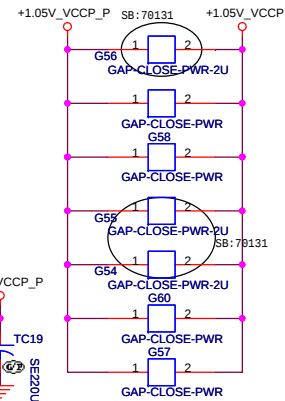
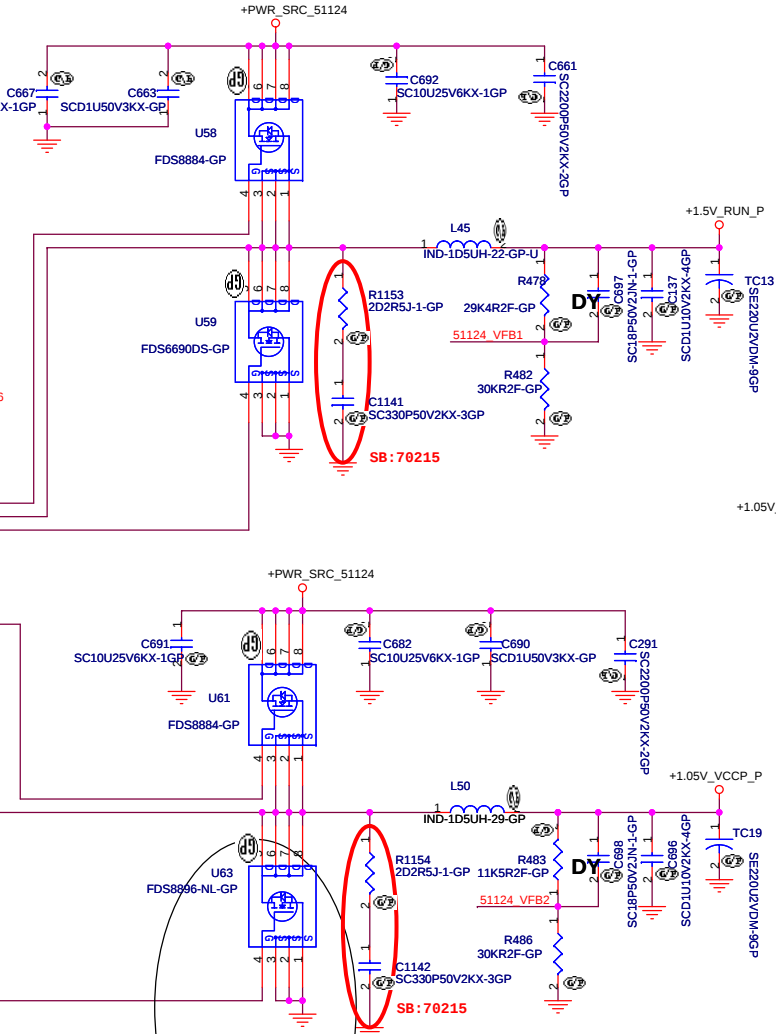
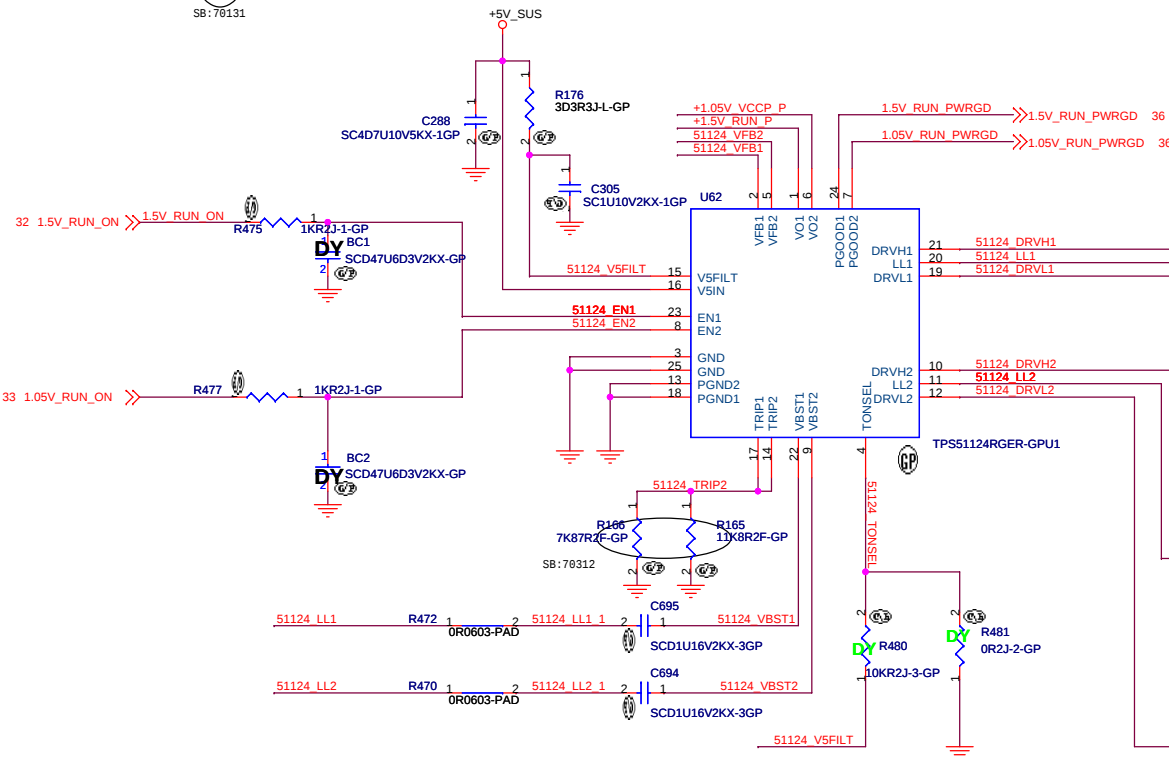
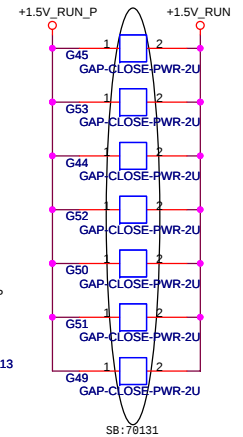
Size **A3** Document Number **DCDC 5V/3V** Rev **-1**

Date: Wednesday, November 07, 2007 Sheet 41 of 46



$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out})/V_{in}))$
 I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
 O/P cap: 220U 2V EEFSX0D221ER 9mOhm 3Arms Panasonic/ 79.22719.2PL
 H/S: FDS8884 S0-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
 L/S: FDS6690AS S0-8/ 15mOhm/ 4.5Vgs/ 84.06690.E37

Design Current = 6.0A
 OCP design > 6.8A
 Included 1.25V LDO(3.02A)



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1+R2)/R2$ --> PWM mode
 $V_{out} = 0.764V * (R1+R2)/R2$ --> Skip Mode

Design Current= 12.2A
 OCP design > 15A

<Variant Name>

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 Taipei Hsien 221, Taiwan, R.O.C.

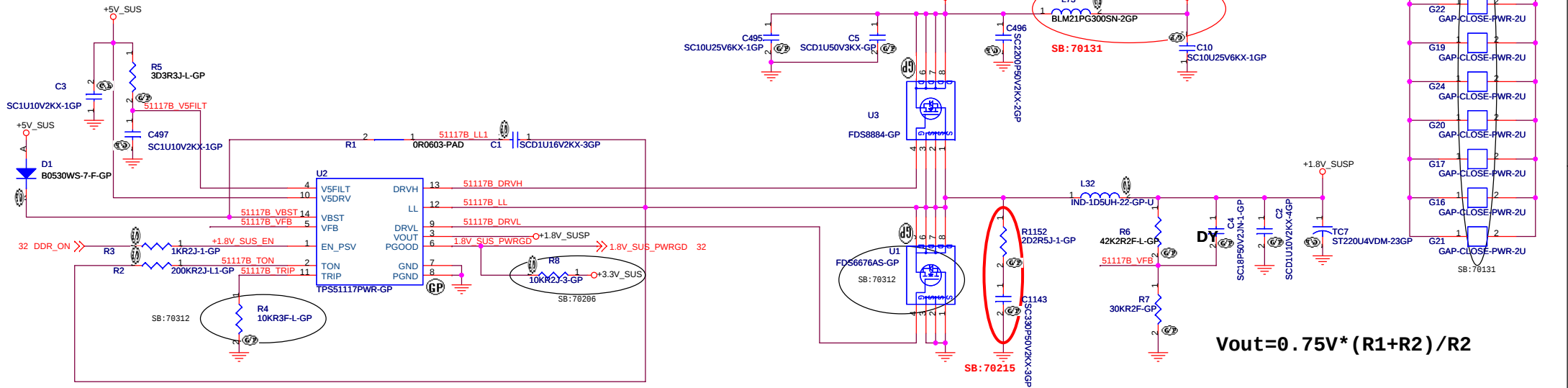
Title

Thurman UMA

Size **A3** Document Number **DCDC 1.5V/1.05V** Rev **-1**

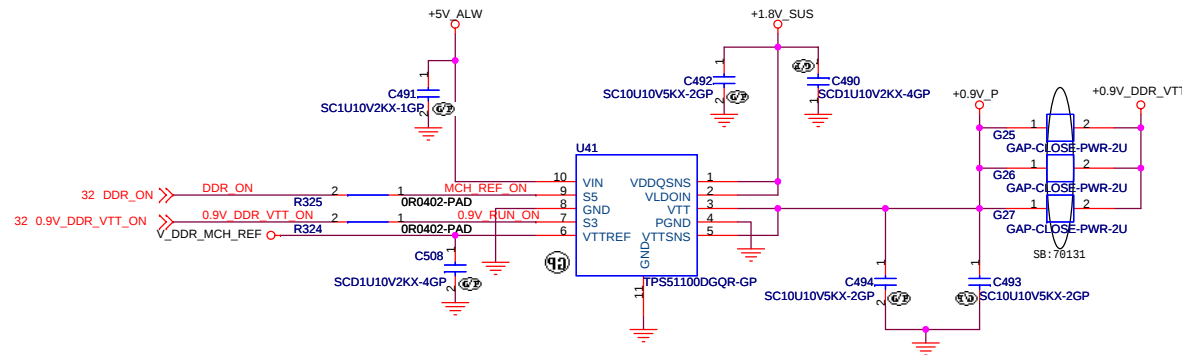
Date: Wednesday, November 07, 2007 Sheet 42 of 46

Design Current = 8.64A
 OCP design = 12.34A



$$V_{out} = 0.75V * (R1 + R2) / R2$$

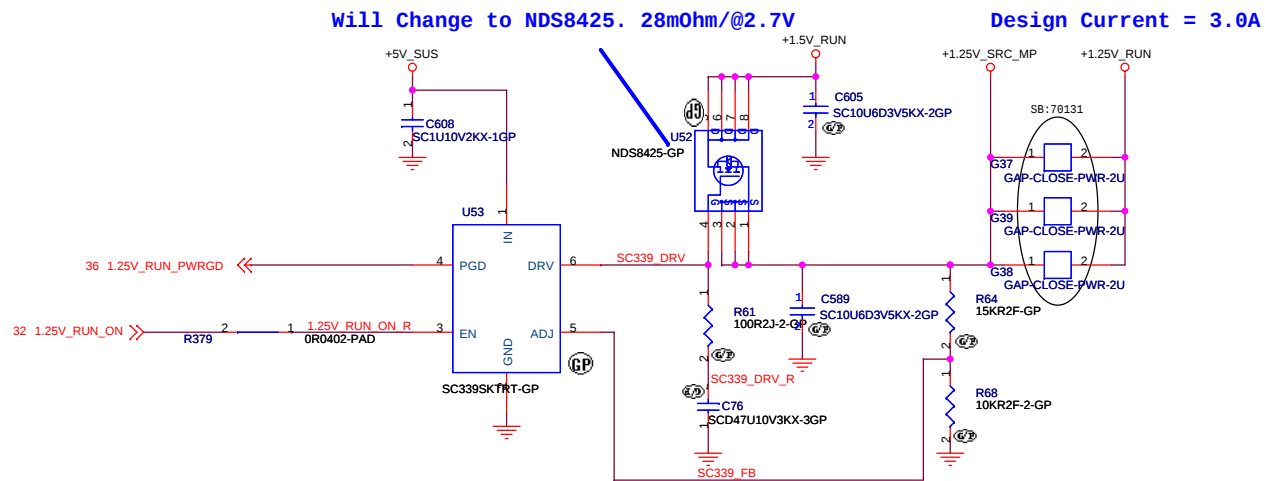
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
 O/P cap: 220U 4V 4TPE220MF 15mOhm 3.1Arms/ 77.22271.161
 H/S & L/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
 L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037
 Ton = 200KOhm --> 330KHz



<Variant Name>



Title		
Thurman UMA		
Size	Document Number	Rev
A3	DCDC 1.8V/0.9V	-1
Date:	Wednesday, November 07, 2007	Sheet 43 of 46

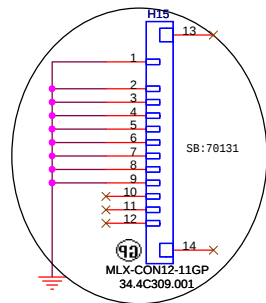
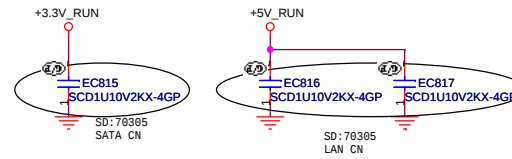
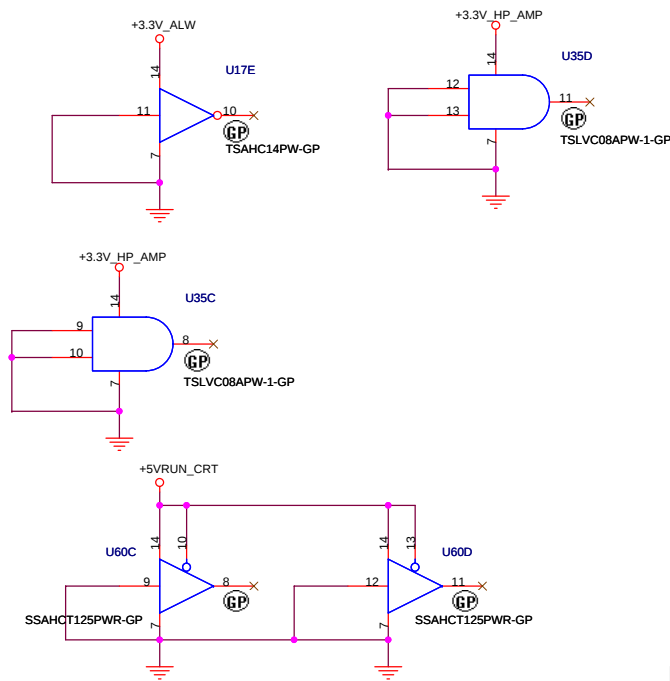


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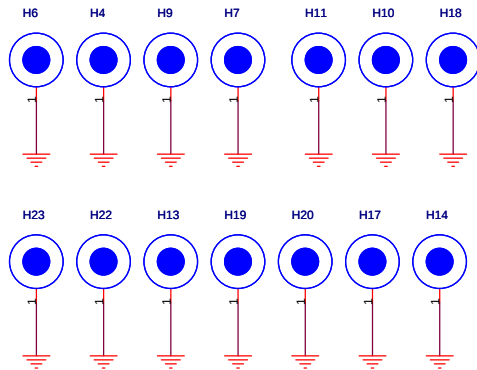
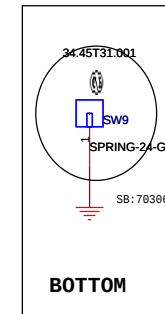
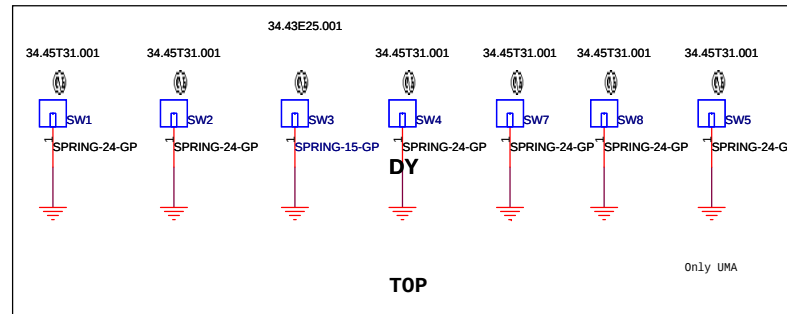


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Title			Thurman UMA	
Size	Document Number	DCDC 1.25V		Rev
A3				-1
Date:	Wednesday, November 07, 2007	Sheet	44	of 46



SW3 - 34.43E25.001
SW9 - 34.49002.001
SW5 - 34.34T31.001 (Only for UMA)
others-34.45T31.001



H12, H16: 34.45X06.001
H8: 34.4A908.001
H27: 34.47M04.001
H26: 34.4G901.001
H21: 34.4C401.001

