Hadley15" Schematics Document

Haswell ULT

2013-06-28
REV : A00

DY : None Installed
UMA: UMA only installed
OPS: Optimus solution installed.
eDP: Support eDP Panel installed.
LVDS: Support LVDS Panel installed.

<Core Design>

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Title: *Cover Page*		
Size: A3	Document Number: *Hadley 15"*	Rev: *X02*
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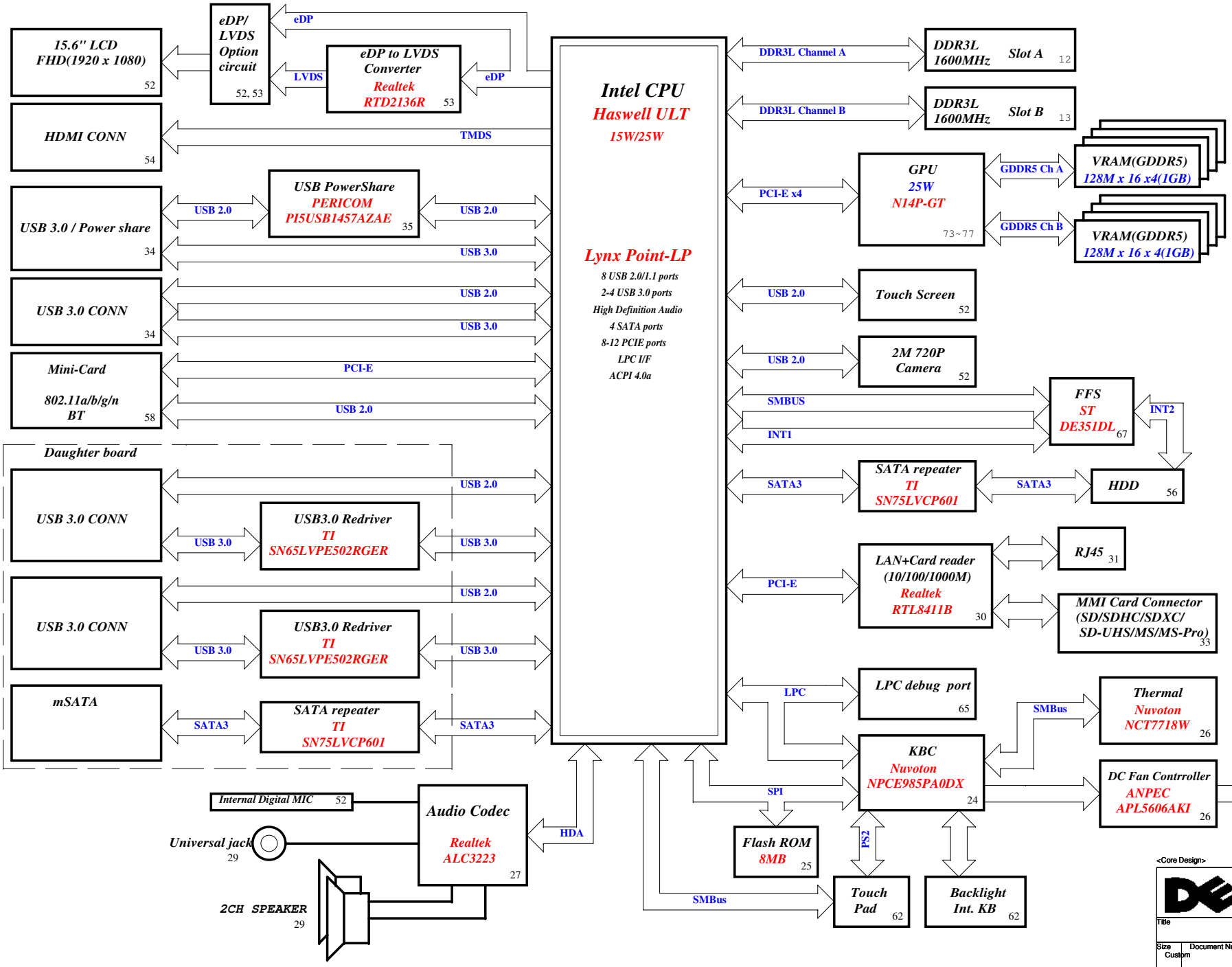
Hadly15 Block Diagram

Project code : 91.47L01.001
PCB P/N : 12311-1
Revision : A00



CHARGER BQ24717 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC TPS51225 45	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_CHARGER 3D3V_PWR

CPU DC/DC TPS51622 46~47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51363 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC TPS51216 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0

SYSTEM DC/DC NCP81172 82	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

Switches 36, 83	
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3D3V_S0
3D3V_S0	3D3V_VGA_S0
1D05V_S0	1D05V_VGA_S0
1D35V_S3	1D35V_VGA_S0

LDO TLV70215DBVR 51	
INPUTS	OUTPUTS
3D3V_S5	

PCB LAYER
L1 : TOP
L2 : GND
L3 : Signal
L4 : Signal
L5 : VCC
L6 : Signal
L7 : GND
L8 : Bottom

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Title: Block Diagram

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Title: *(Reserved)*

Size	Document Number	Rev
A3	*Hadley 15"*	*X02*

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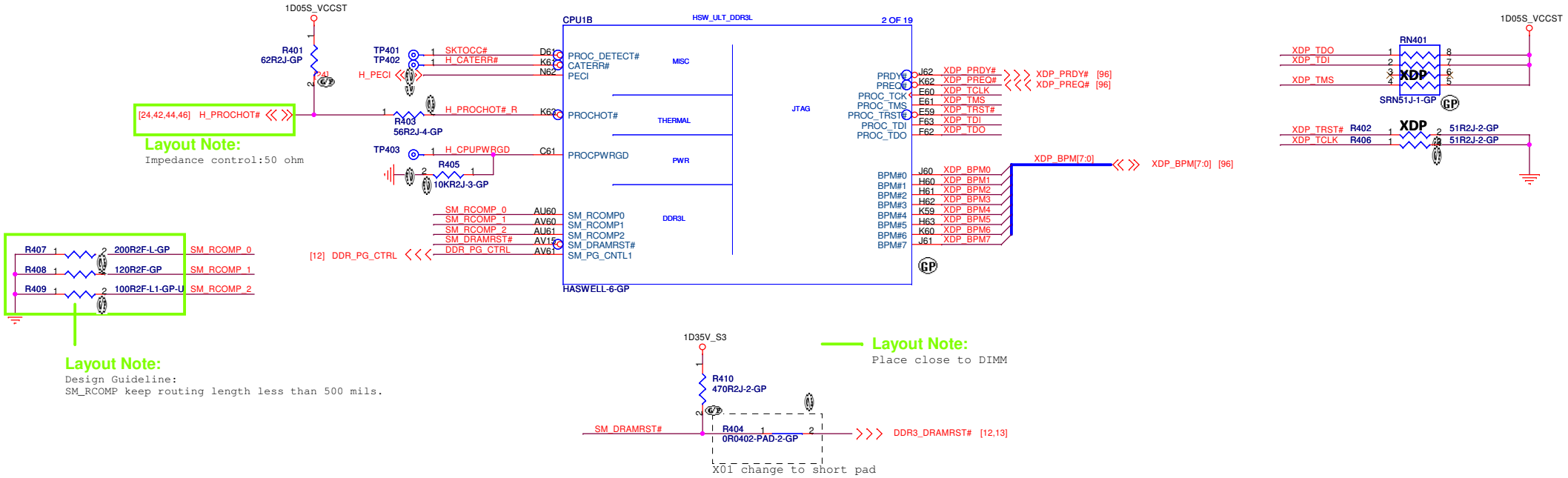
SSID = CPU



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Title: CPU (THERMAL/CLOCK)

Size	Document Number	Rev
A3	Hadley 15"	X02

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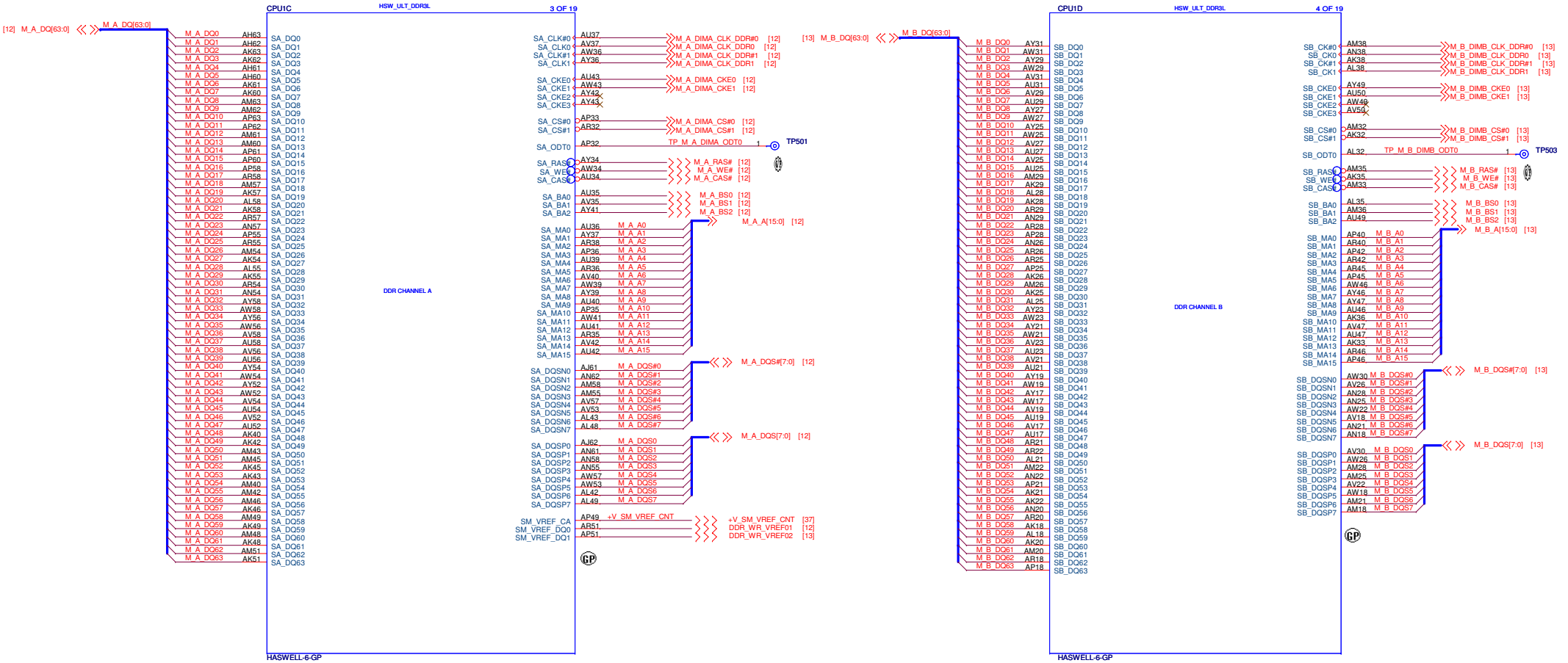
SSID = CPU



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Title: CPU (DDR)

Size	Document Number	Rev
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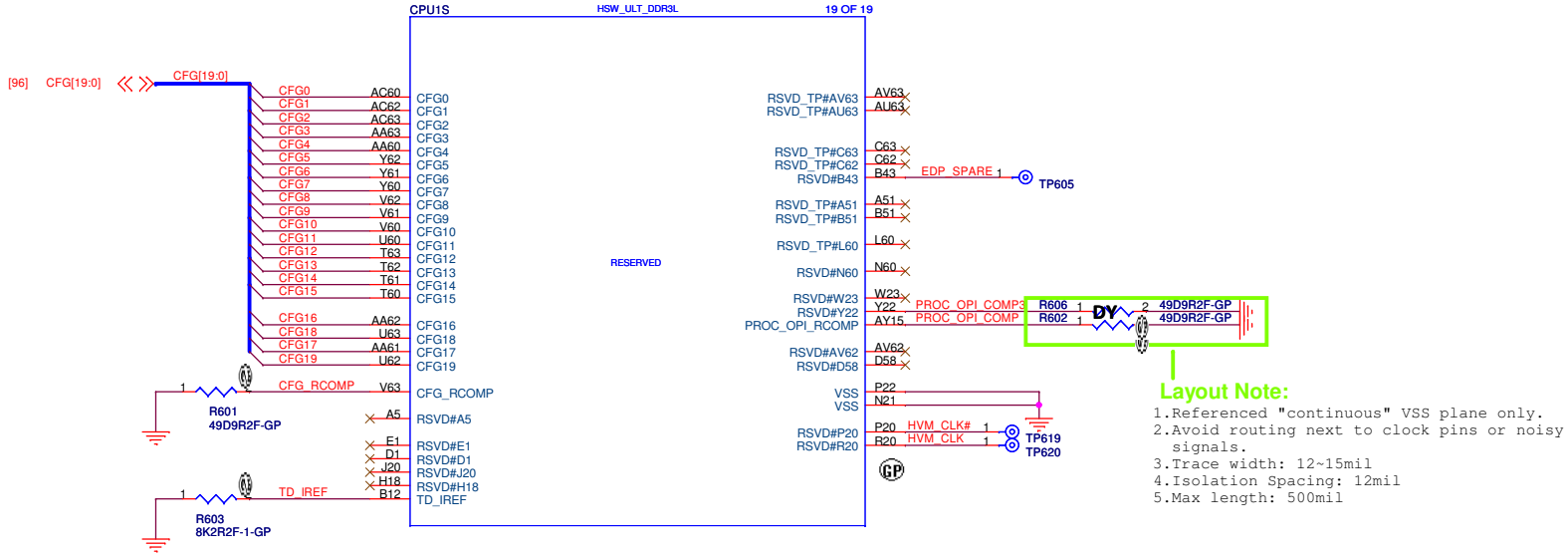
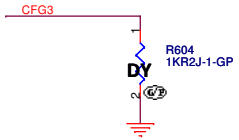
SSID = CPU

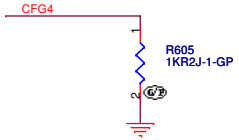


Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR **1 : DISABLED**



DISPLAY PORT PRESENCE STRAP	
CFG[4]	**0 : ENABLED** **AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT** 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

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Title: CPU (RESERVED)

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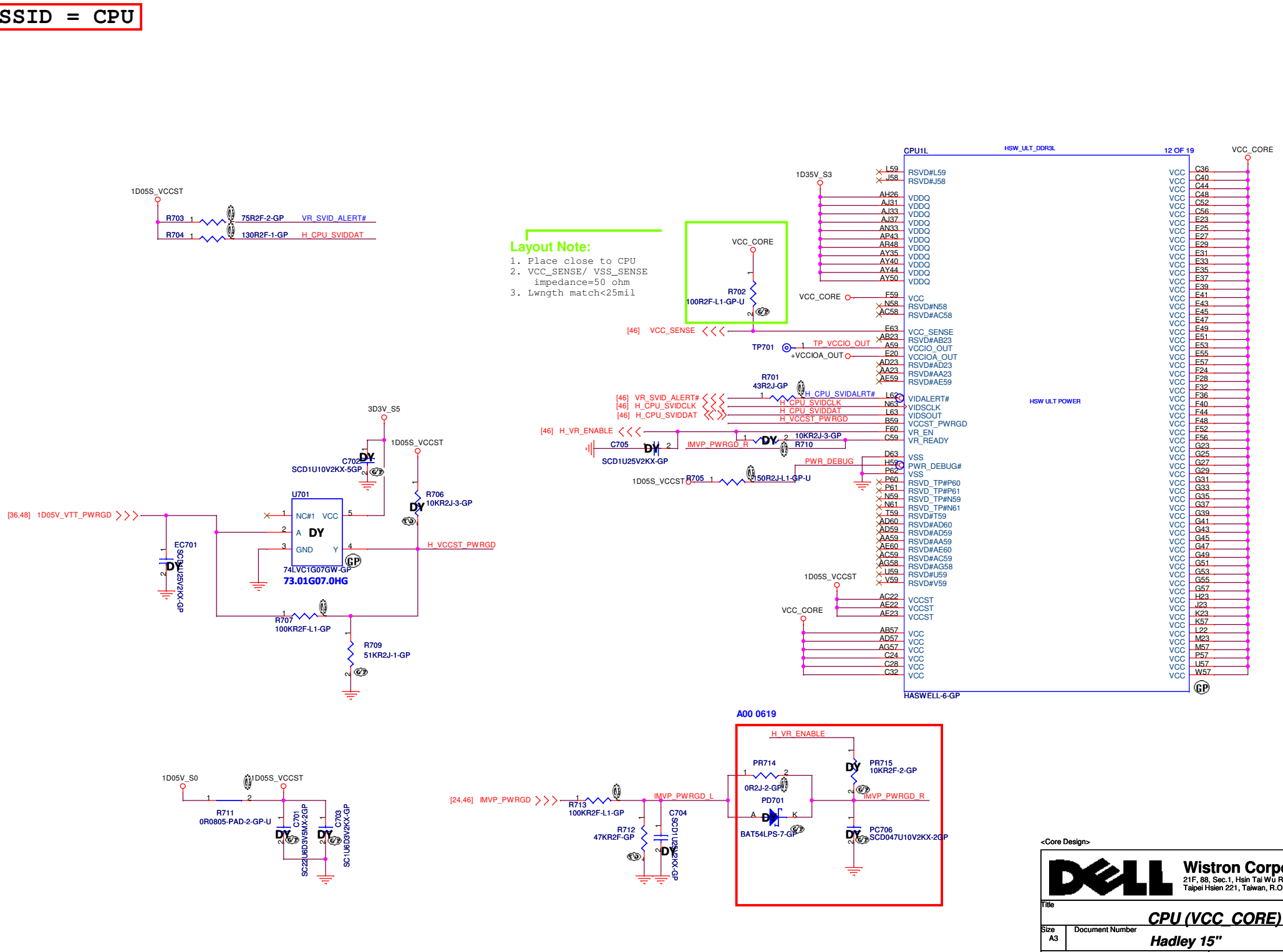
SSID = CPU



<Core Design>

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Title: CPU (VCC_CORE)

Size: A3 | Document Number: Hadley 15" | Rev: X02

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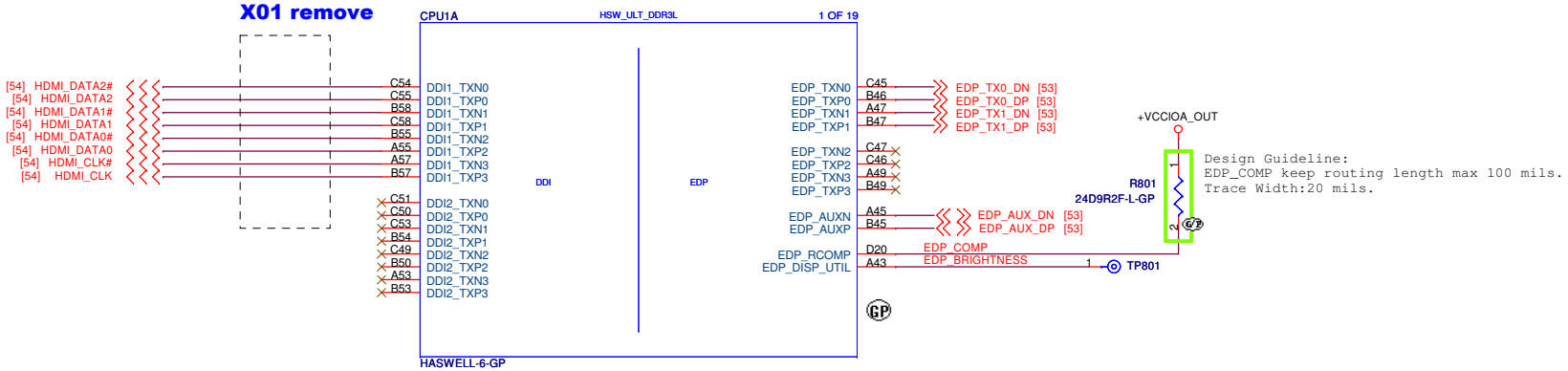
SSID = CPU

HDMI

X01 remove



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Title: CPU (DDI/EDP)

Size	Document Number	Rev
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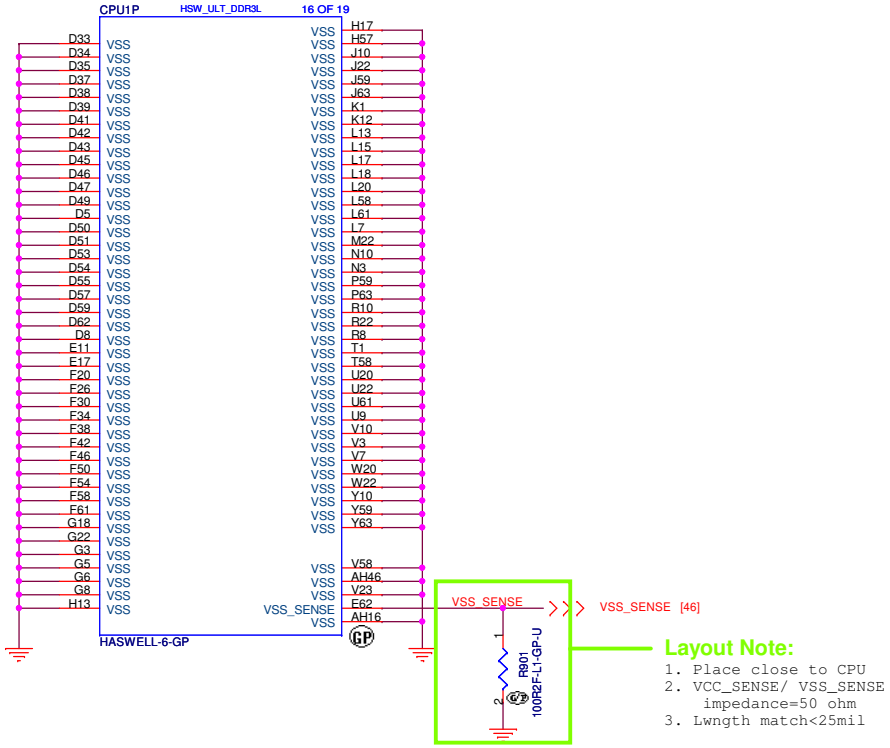
SSID = CPU



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Title: CPU (VSS)

Size: A3 | Document Number: Hadley 15" | Rev: X02

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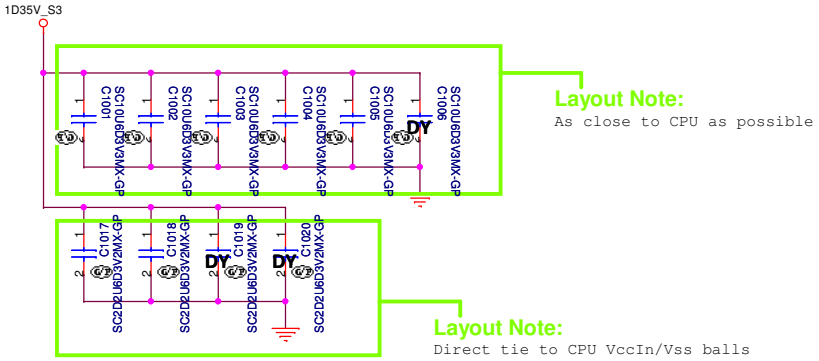
SSID = CPU



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Title	CPU(Power CAP1)	
Size: A3	Document Number: Hadley 15"	Rev: X02
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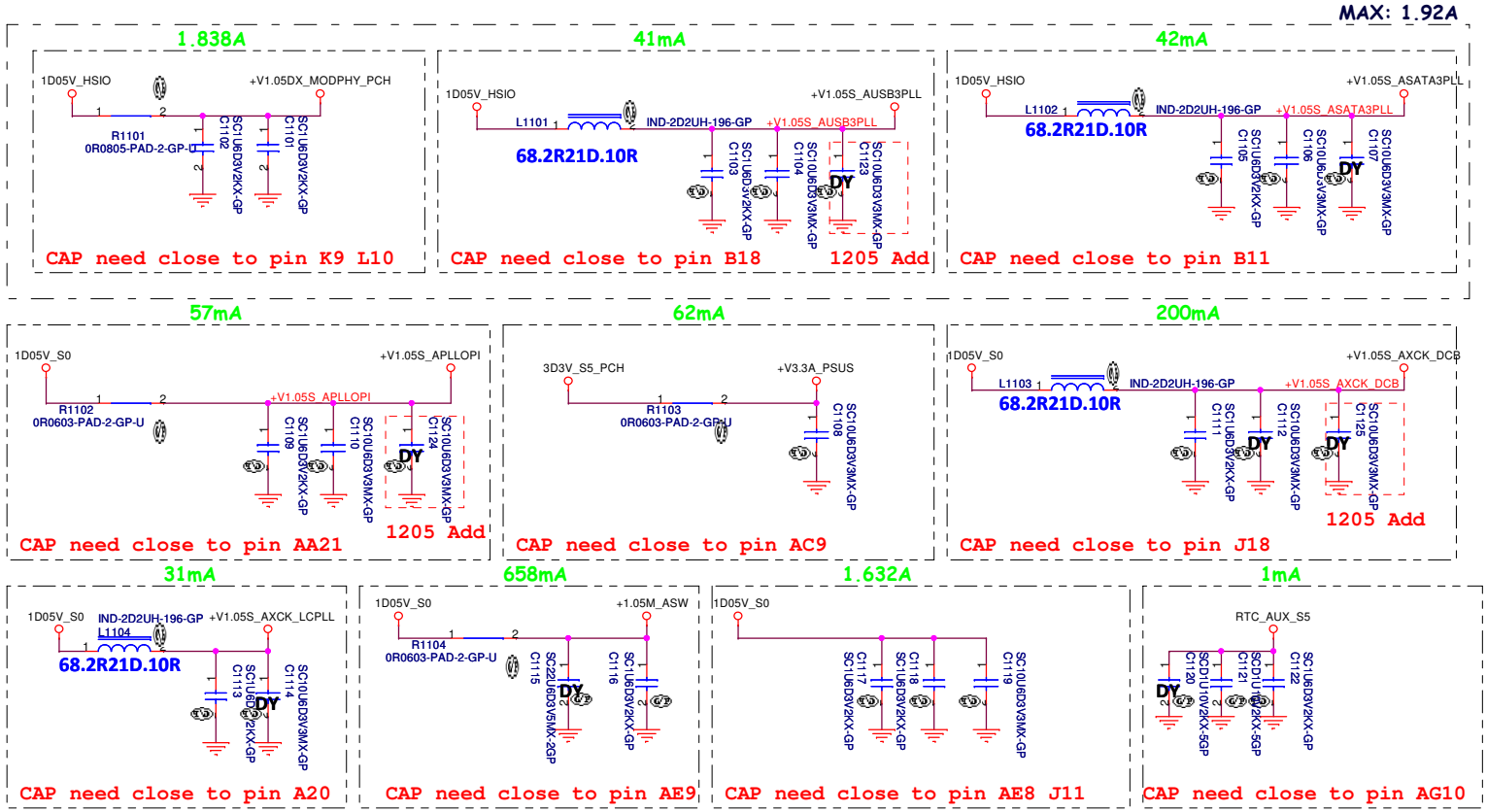
SSID = CPU



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Title	CPU(Power CAP2)	
Size: A3	Document Number: Hadley 15"	Rev: X02
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SSID = MEMORY

DM1

DDR3-204P-122-GP-U1

62.10017.Z51

Note:
SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

Layout Note:
Place these caps close to VREF_CA

Layout Note:
Place these caps close to VREF_DQ

Layout Note:
Place these caps close to VTT1 and VTT2.

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

close to dimm

Layout Note:
Place these Caps near SO-DIMMA.

Layout Note:
Place Close SO-DIMMA.

X01 change to short pad

Q1201 Need check Vth=1V

84.05067.031

Q1202
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031

Q1201
DMN5L06K-7-GP

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Title: DDR3L-SODIMM1

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SSID = MEMORY

DM2

M_B_A[15:0] [5]

M_B_BS2 [5]
M_B_BS0 [5]
M_B_BS1 [5]
M_B_DQ[63:0] [5]

M_B_DQS#[7:0] [5]
M_B_DQS[7:0] [5]

[12] M_B_DIMB_ODT0
[12] M_B_DIMB_ODT1

M_VREF_CA_DIMMB
M_VREF_DQ_DIMMB

[4,12] DDR3_DRAMRST#

M_B_RAS# [5]
M_B_WE# [5]
M_B_CAS# [5]
M_B_DIMB_CS#0 [5]
M_B_DIMB_CS#1 [5]
M_B_DIMB_CKE0 [5]
M_B_DIMB_CKE1 [5]
M_B_DIMB_CLK_DDR0 [5]
M_B_DIMB_CLK_DDR#0 [5]
M_B_DIMB_CLK_DDR1 [5]
M_B_DIMB_CLK_DDR#1 [5]
PCH_SMBDATA [12,18,58,62,67]
PCH_SMBCLK [12,18,58,62,67]
SA0_DIMB
SA1_DIMB

3D3V_S0
1D35V_S3
0D675V_S0

DDR3-204P-122-GP-U1
62.10017.Z51

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

Layout Note:
Place these caps close to VREF_CA

Layout Note:
Place these caps close to VREF_DQ

Layout Note:
Place these caps close to VTT1 and VTT2.

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

close to dimm

Layout Note:
Place these Caps near SO-DIMMA.

Layout Note:
Place Close SO-DIMMA.

[5] DDR_WR_VREF02

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Title: DDR3L-SODIMM2
Size: Custom
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Title: M1&M3

Size: A3 | Document Number: Hadley 15" | Rev: X02

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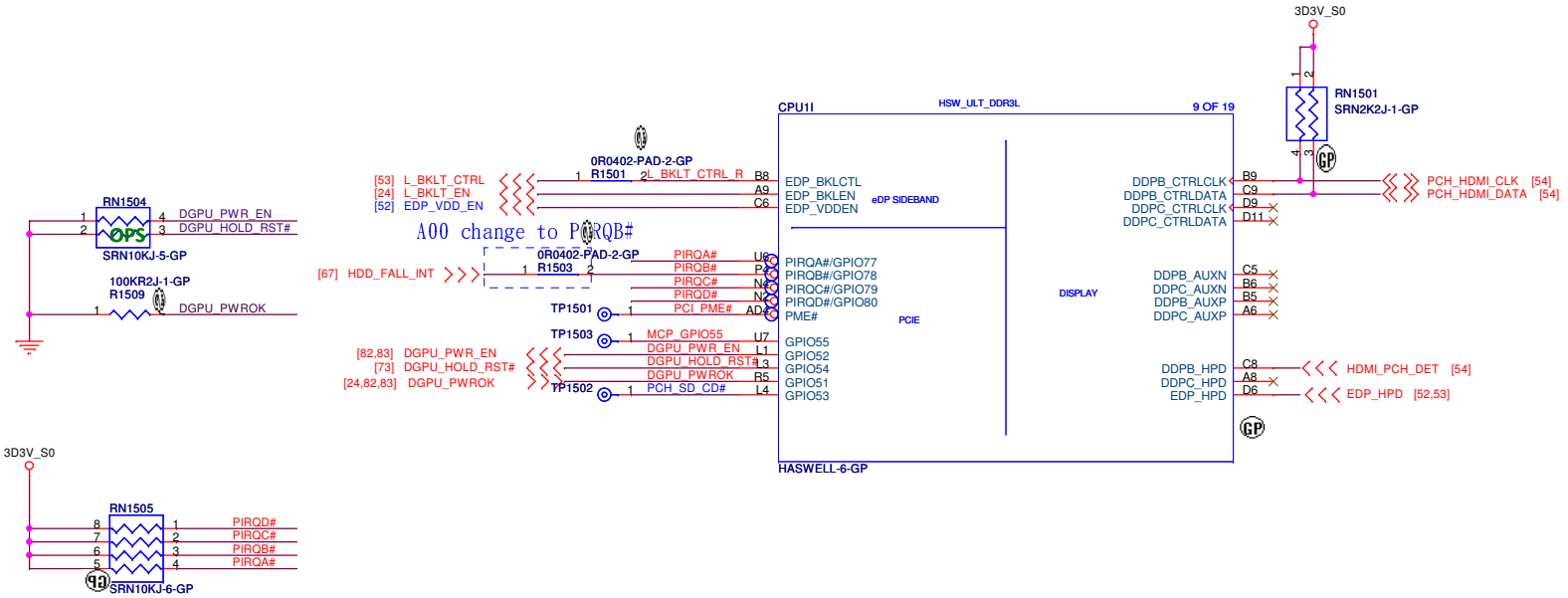
SSID = CPU



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Title		
CPU (EDP SIDEBAND/GPIO/DDI)		
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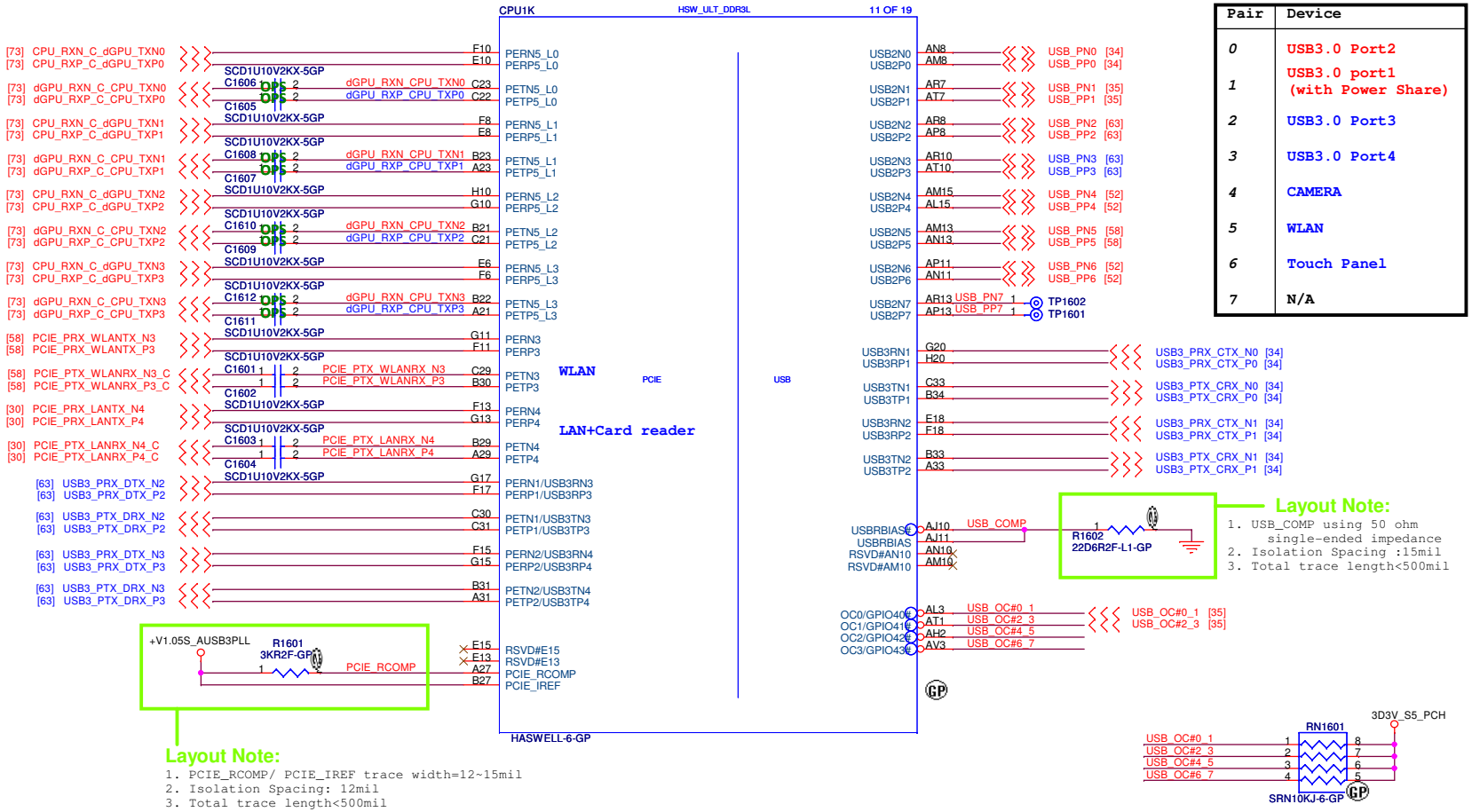
SSID = CPU

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN+ Card reader	
5(4lane)	GPU	
6(4lane)	N/A	SATA0~3

USB 2.0 Table

Pair	Device
0	USB3.0 Port2
1	USB3.0 port1 (with Power Share)
2	USB3.0 Port3
3	USB3.0 Port4
4	CAMERA
5	WLAN
6	Touch Panel
7	N/A



Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

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Title: CPU (PCIE/USB)

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SSID = CPU

On Die DSW VR Enable	
DSWODVREN	Low = Disable High = Enable (default)

DSWODVREN — R1720 330KR2J-L1-GP — RTC_AUX_S5; R1721 330KR2J-L1-GP (DY)

RN1703 SRN10KJ-5-GP: PM_RSMRST#, PM_PCH_PWROK, SYS_PWROK; R1717 10KR2J-3-GP (DY)

3D3V_S0

RN1704 SRN8K2J-3-GP: XDP_DBRESET#, PM_CLKRUN#

CPU1H — HSW_ULT_DDR3L — 8 OF 19 — SYSTEM POWER MANAGEMENT — HASWELL-6-GP

[24,96] SYS_PWROK
[24,26,36] PCH_PWROK
R1706 0R0402-PAD-2-GP
R1707 0R0402-PAD-2-GP
PM_SUSACK# AK2 → SUSACK#
XDP_DBRESET# AC2 → SYS_RESET#
SYS_PWROK AG2 → SYS_PWROK
PM_PCH_PWROK AY7 → PCH_PWROK
MPWROK AB5 → APWROK
PCI_PLTRST# AG7 → PLTRST#

PM_RSMRST# AW8 → RSMRST#
PM_SUSWARN# AV8 → SUSWARN#/SUSPWRDNACK#/GPIO30
PM_PWRBTN# AL → PWRBTN#
AC_PRESENT AJ8 → ACPRESENT/GPIO31
BATLOW# AN8 → BATLOW#/GPIO72
PCH_SLP_S0# AE2 → SLP_S0#
PCH_SLP_WLAN# AM2 → SLP_WLAN#/GPIO29

[24,96] PM_PWRBTN#
[24,76] AC_PRESENT
[48] PCH_SLP_S0#
TP1705 0R0402-PAD-2-GP

[24,30,58,65,73] PLT_RST# — R1713 — PCI_PLTRST#
R1715 100KR2J-1-GP (DY); C1701 SC220P50V2KX-3GP (DY)

DSWVRMEN AW7 → DSWODVREN
DPWROK AV5 → PCH_DPWROK
WAKE# AJ5 → PCH_WAKE# R1703 → PM_RSMRST#

NON DS3
0R2J-2-GP R1704
3D3V_S5
0311 PCH WAKE# pin PH 1K
0R0402-PAD-2-GP A00 0618

CLKRUN#/GPIO32 V5 → PM_CLKRUN# R1709 → PM_CLKRUN#_EC [24]
SUS_STAT#/GPIO61 AG4 → PM_SUS_STAT# TP1702
SUSCLK/GPIO62 AE6 → SUS_CLK R1710 → PCH_SUSCLK_KBC [24]
SLP_S5#/GPIO63 AP5 → PM_SLP_S5# TP1703 0R0402-PAD-2-GP

SLP_S4# AJ6 → PM_SLP_S4# [24,49]
SLP_S3# AT4 → PM_SLP_S3# [24,36,48,49,51]
SLP_A# AL5 → PM_SLP_A# TP1704
SLP_SUS# AP4 → PM_SLP_SUS# [24,38]
SLP_LAN# AJ7 → PM_SLP_LAN# TP1707

3D3V_S5 — RN1701 SRN10KJ-5-GP: BATLOW#, AC_PRESENT

[24] PM_SUSACK#
[24] PM_SUSWARN#
A00 0618 — 0R4P2R-PAD RN1702: PM_SUSACK#_R, PM_SUSWARN#_R

PCH_DPWROK — R1718 0R0402-PAD-2-GP — KBC_DPWROK [24]
A00 0618
R1725 100KR2F-L1-GP DS3

3D3V_AUX_S5
NON DS3
R1708 100KR2J-1-GP
R1726 10KR2J-3-GP

Q1701 2N7002KDW-GP
3V_5V_POK# → 3V_5V_POK
PM_RSMRST# → 1KR2J-1-GP R1702 → RSMRST#_KBC [24]
3V_5V_POK R1728 0R2J-2-GP → 3V_5V_POK [45]
NON DS3
PM_SLP_SUS# → R1729 0R0402-PAD-2-GP
A00 0618

3D3V_S5_PCH
R1724 10KR2J-3-GP (DY) — PM_SUS_STAT#
R1727 10KR2J-3-GP — PM_SUSWARN#

PCH_SUSCLK_KBC
EC1701 SC4D7P50V2CN-1GP (DY)

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Title		
CPU (PM)		
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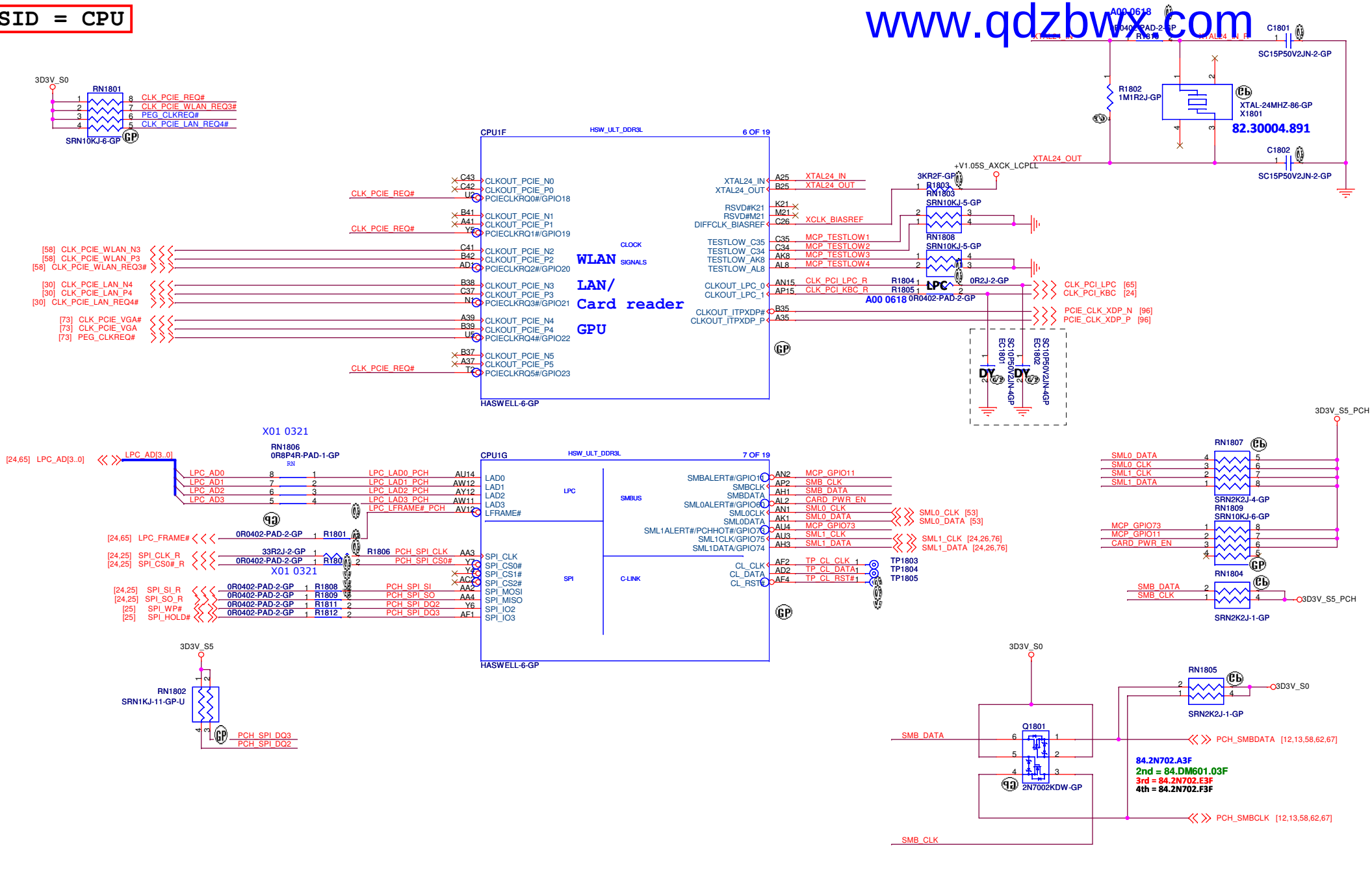
SSID = CPU



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Title: CPU (CLK/SMB/LPC/SPI)

Size	Document Number	Rev
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SSID = CPU

X02 0502 change C1903 C1904 from 18pF to 15 pF

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default ★ High = Enable

The internal pull-down is disabled after PLTRST# deasserts

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs★

Layout Note:
4mil trace at break-out and 3 12-15mil trace with <0.2 ohms and length total <= 500mils.

HDD1
mSATA

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Title: CPU (RTC/SATA/HDA/JTAG)
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SSID = CPU

GPIO[47:44]=[1,1,1,1] for SODIMM configuration

PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Disable (Default) High = Enable

The internal pull-down is disabled after PLTRST# deasserts

Top-Block Swap Override mode	
SDIO_D0 / GPIO66	High = Enable "Top-Block swap" mode (Default) * Low = Disable "Top-Block swap" mode

The internal pull-down is disabled after PLTRST# deasserts

TLS Confidentiality	
GPIO15	* Low = Disable Intel ME Crypto TLS High = Enable Intel ME Crypto TLS

The internal pull-down is disabled after RSMRST# deasserts.

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI High = LPC

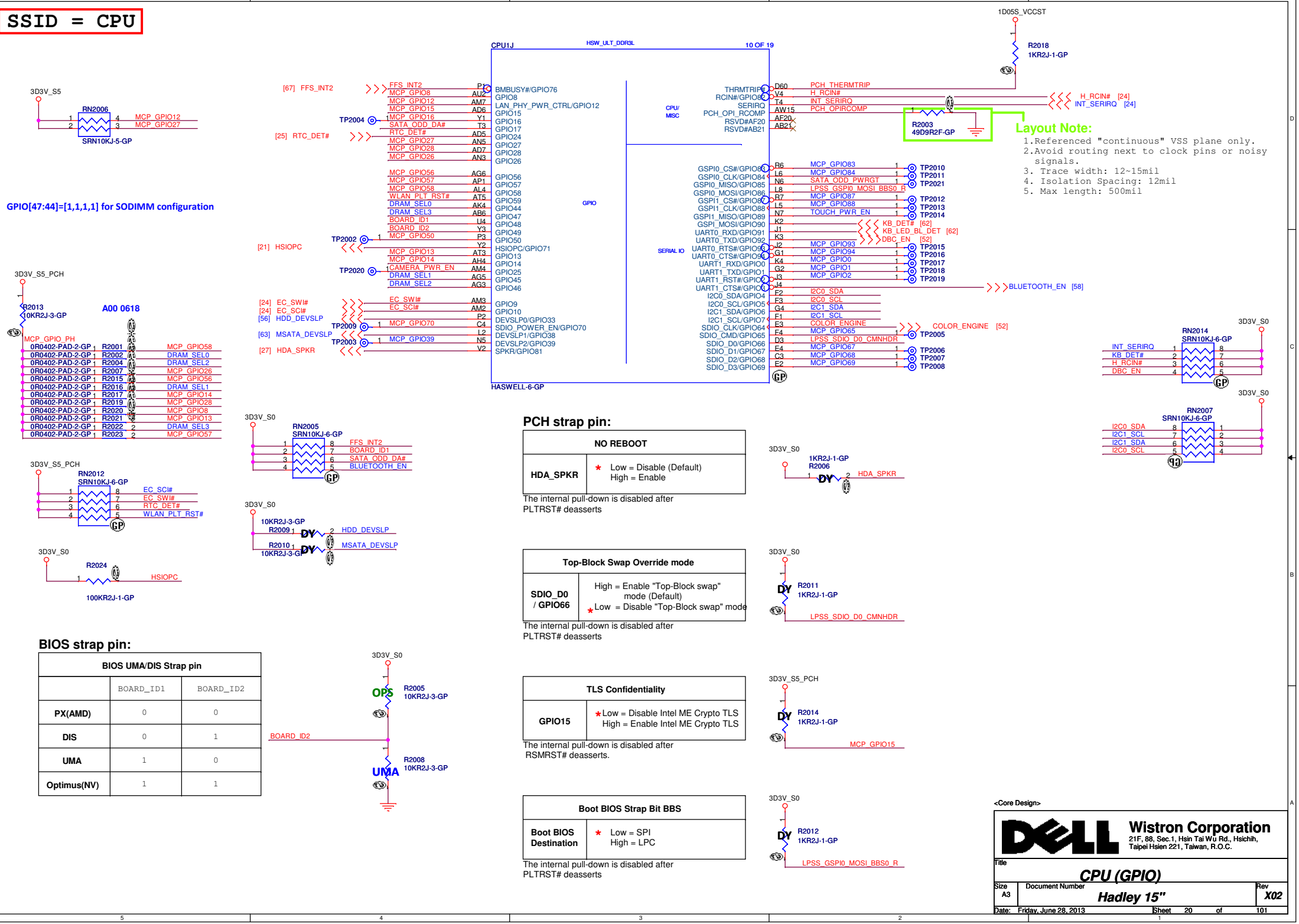
The internal pull-down is disabled after PLTRST# deasserts

BIOS strap pin:

BIOS UMA/DIS Strap pin		
	BOARD_ID1	BOARD_ID2
PX(AMD)	0	0
DIS	0	1
UMA	1	0
Optimus(NV)	1	1

Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



<Core Design>

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Title: CPU (GPIO)

Size: A3 | Document Number: Hadley 15" | Rev: X02

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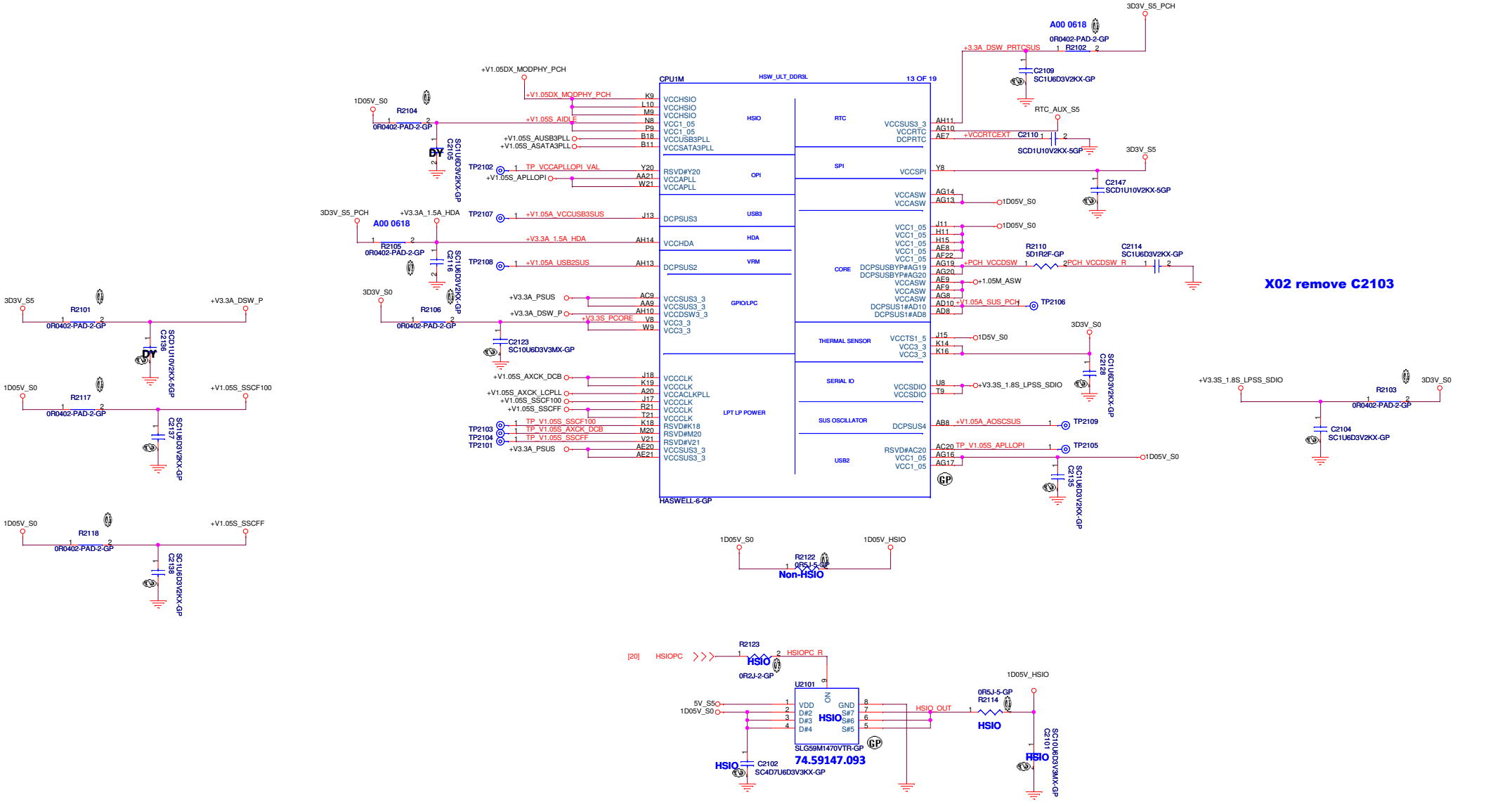
SSID = CPU


CPU1M
HSW_ULT_DDR3L
13 OF 19
HASWELL-6-GP
A00 0618
X02 remove C2103
Non-HSIO
HSIO
74.59147.093
SLG59M1470VTR-GP
<Core Design>
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Title
CPU (POWER2)
Size
Custom
Document Number
Hadley 15"
Rev
X02
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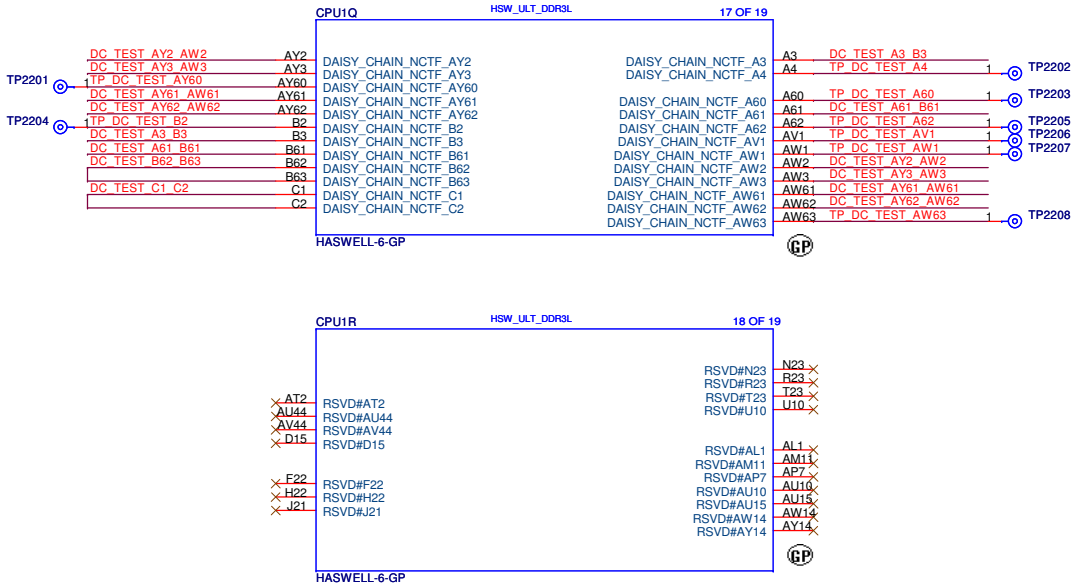
SSID = CPU



<Core Design>

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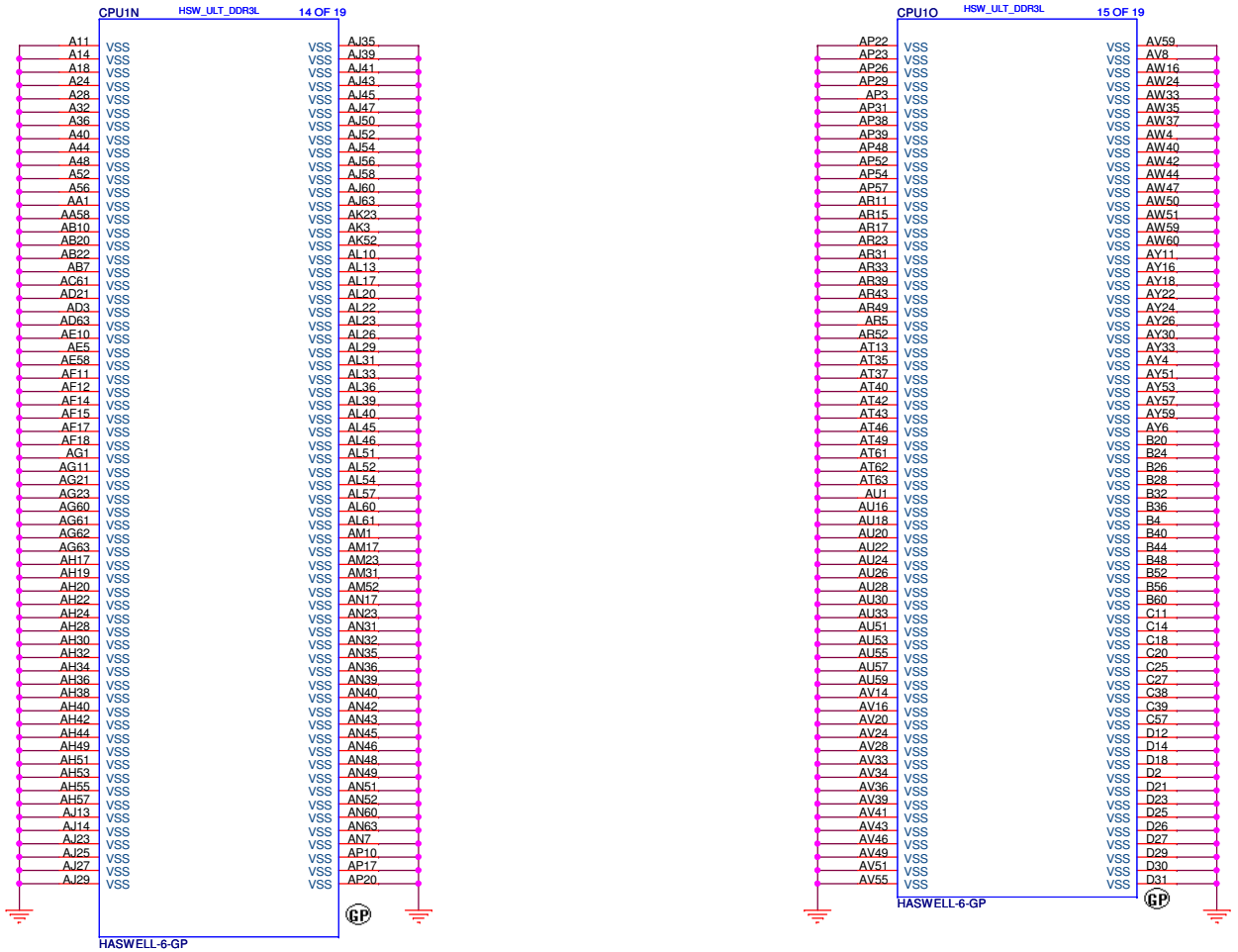
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RSVD

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 22 of 101

SSID = CPU



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: Hadley 15" | Rev: X02

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SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
(DOH70)UMA	100.0K	10.0K(64.10025.6DL)	3.0V
(DOH50)UMA/eDP	100.0K	13.7K(64.13725.6DL)	2.902V
TBD	100.0K	17.8K(64.17825.6DL)	2.801V
(DOH70)DIS	100.0K	22.1K(64.22125.6DL)	2.702V
TBD	100.0K	27.0K(64.27025.6DL)	2.598V
TBD	100.0K	32.4K(64.32425.6DL)	2.492V
TBD	100.0K	37.4K(64.37425.6DL)	2.402V
TBD	100.0K	43.2K(64.43225.6DL)	2.304V
(DOH50)UMA/LVDS	100.0K	49.9K(64.49925.6DL)	2.201V
(DOH50)DIS/eDP	100.0K	57.6K(64.57625.6DL)	2.093V
TBD	100.0K	64.9K(64.64925.6DL)	2.001V
TBD	100.0K	73.2K(64.73225.6DL)	1.905V
TBD	100.0K	82.5K(64.82525.6DL)	1.808V
TBD	100.0K	93.1K(64.93125.6DL)	1.709V
TBD	100.0K	107K(64.10735.6DL)	1.594V
TBD	100.0K	120K(64.12035.6DL)	1.499V
TBD	100.0K	137K(64.13735.6DL)	1.392V
TBD	100.0K	154K(64.15435.6DL)	1.299V
TBD	100.0K	200K(64.20035.6DL)	1.099V
TBD	100.0K	232K(64.23236.6DL)	0.994V

Layout Note:
Need very close to EC

Don't PD

ALL_SYS_PWRGD assert, delay 10ms;
PCH_PWROK assert.

ALL_SYS_PWRGD assert, delay 100ms;
SYS_PWROK assert.

LVDS backlight Control from PS8625

eDP backlight Control from PCH

Backlight Control from LVDS Converter

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC
C2422 PDG is 47p

Layout Note:
Connect GND and AGND planes via either
0R resistor or connect directly.

X01 0321

AOAC Ambient temperature detect

EC_GPIO47 High Active

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

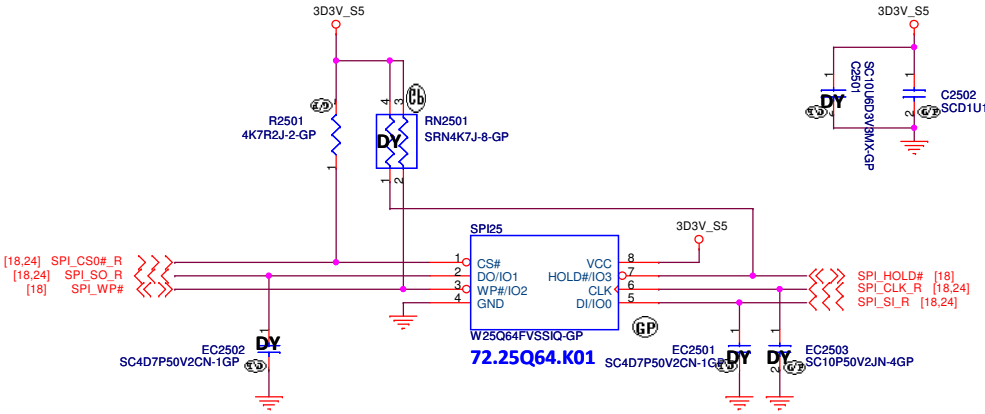
Title: KBC Nuvoton NPCE985

Size: A2 | Document Number: Hadley 15" | Rev: X02

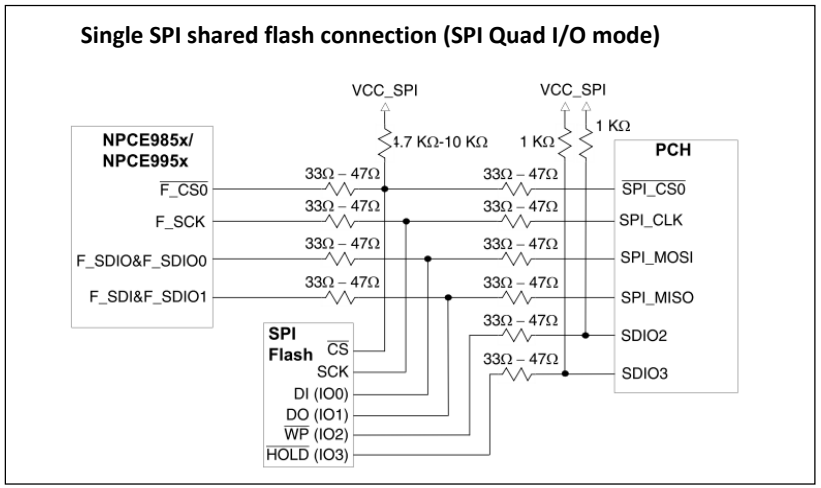
Date: Friday, June 28, 2013 | Sheet 24 of 101

SSID = Flash.ROM

SPI Flash ROM(8M) for PCH

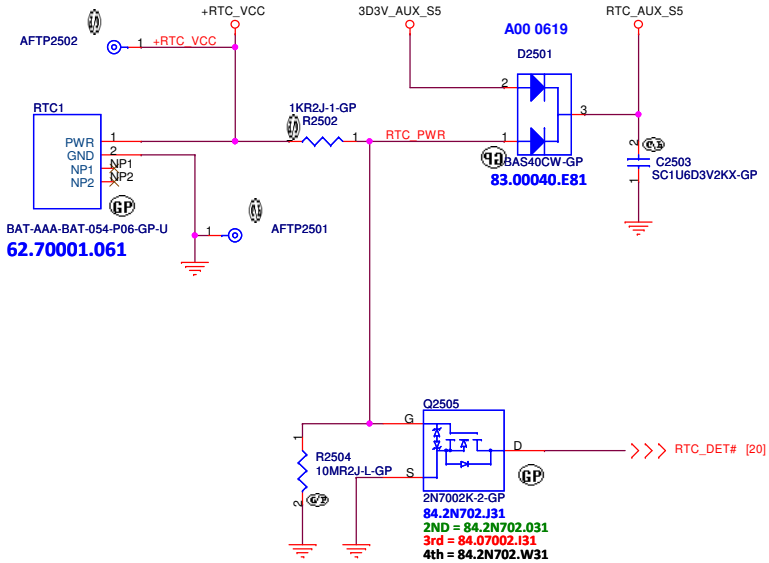


Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25647.00A	O	O



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT

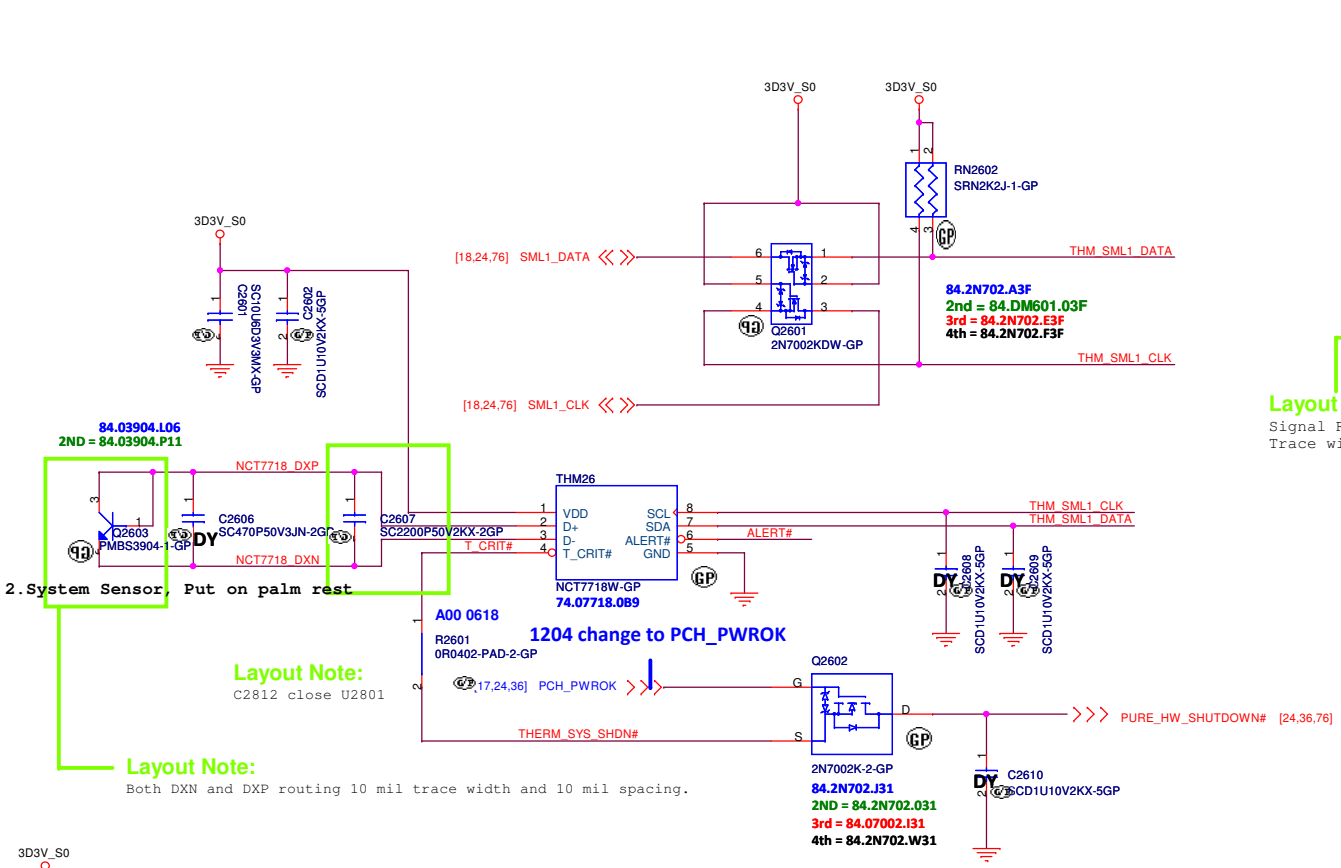


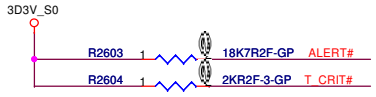
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC		
Size: A3	Document Number: Hadley 15"	Rev: X02
Date: Friday, June 28, 2013	Sheet 25 of 101	

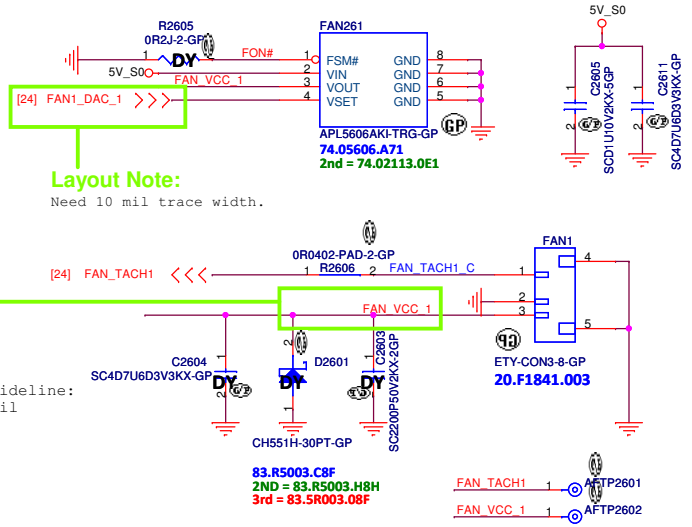
SSID = Thermal





TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Fan controller1



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal NCT7718W/Fan

Size: A3 | Document Number: Hadley 15" | Rev: X02

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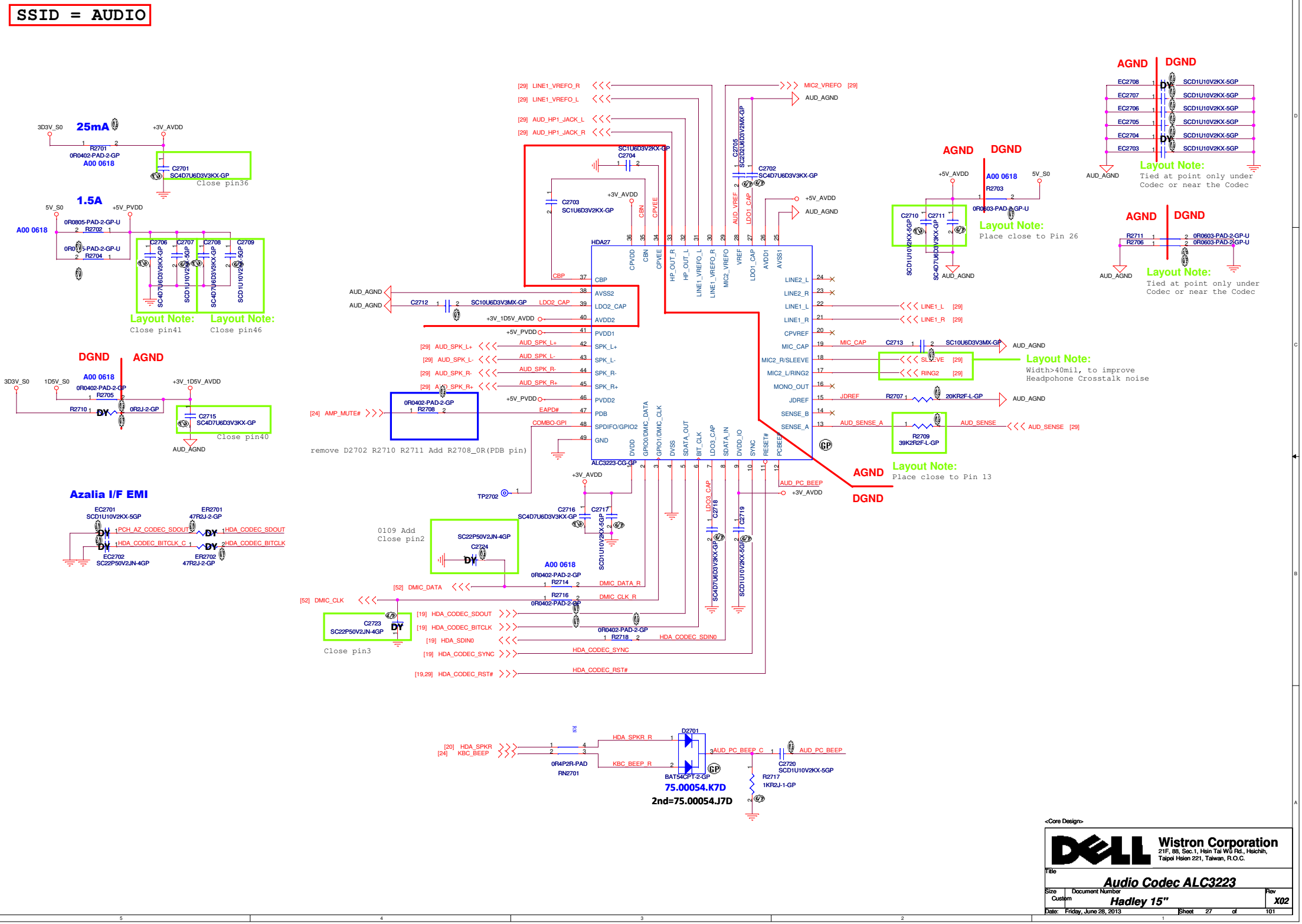
SSID = AUDIO



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Codec ALC3223**

Size	Document Number	Rev
Custom	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 27 of 101

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<Core Design>

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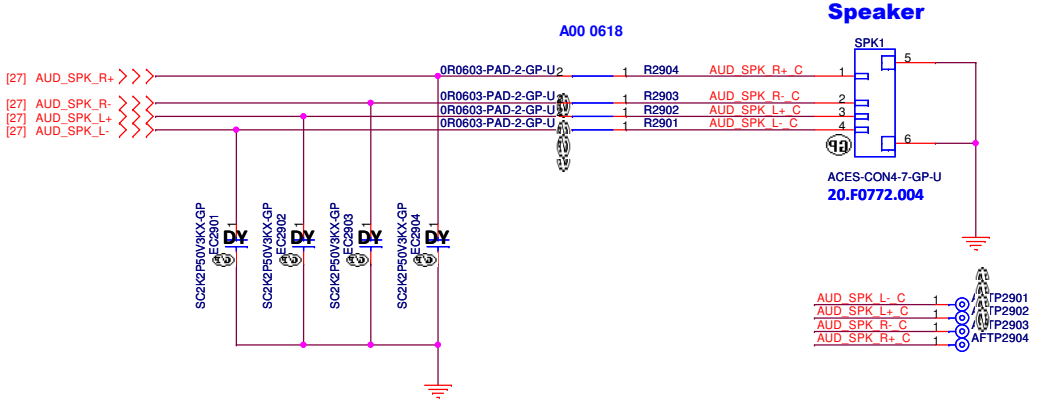
Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 28, 2013 | Sheet 28 of 101

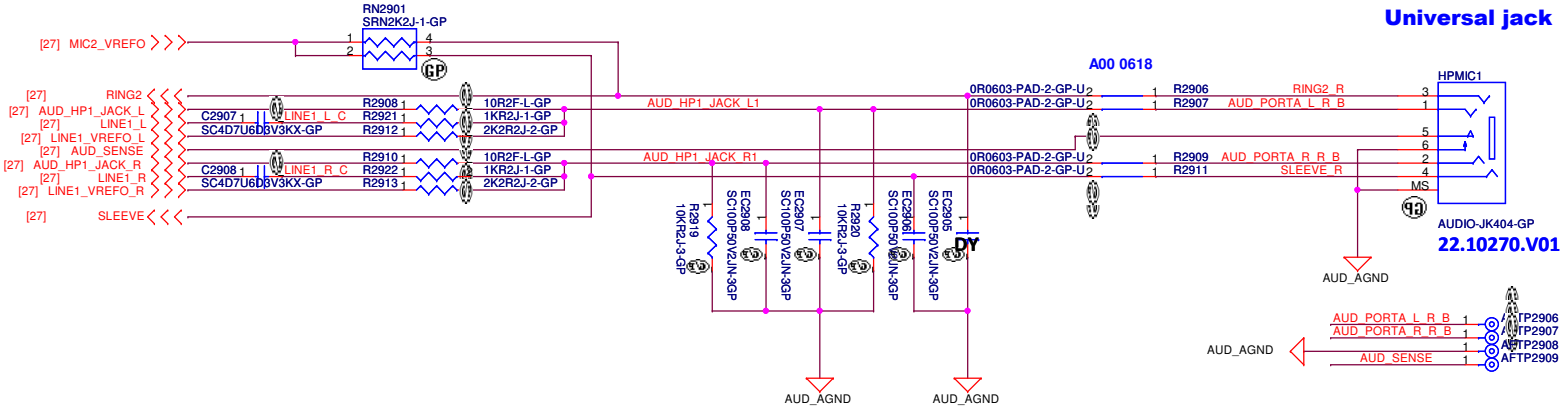
SSID = AUDIO

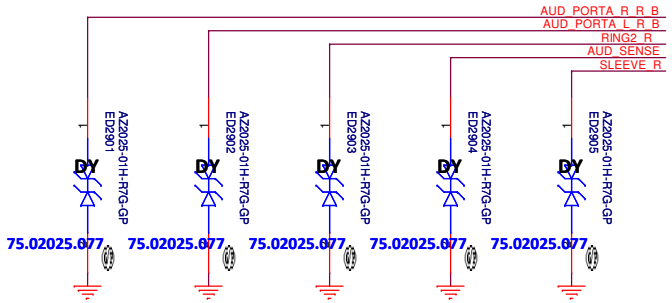
Speaker

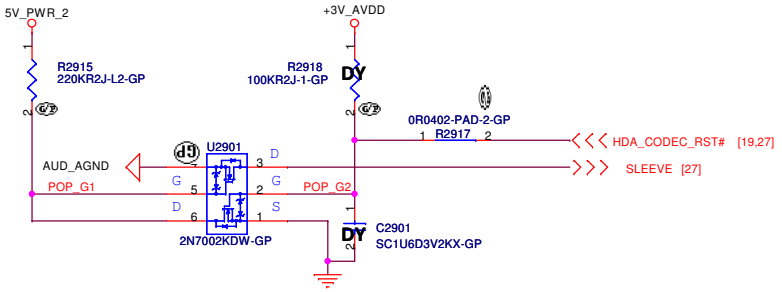


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L_

Universal jack







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/HPMIC CONN

Size	Document Number	Rev
A3	Hadley 15"	X02

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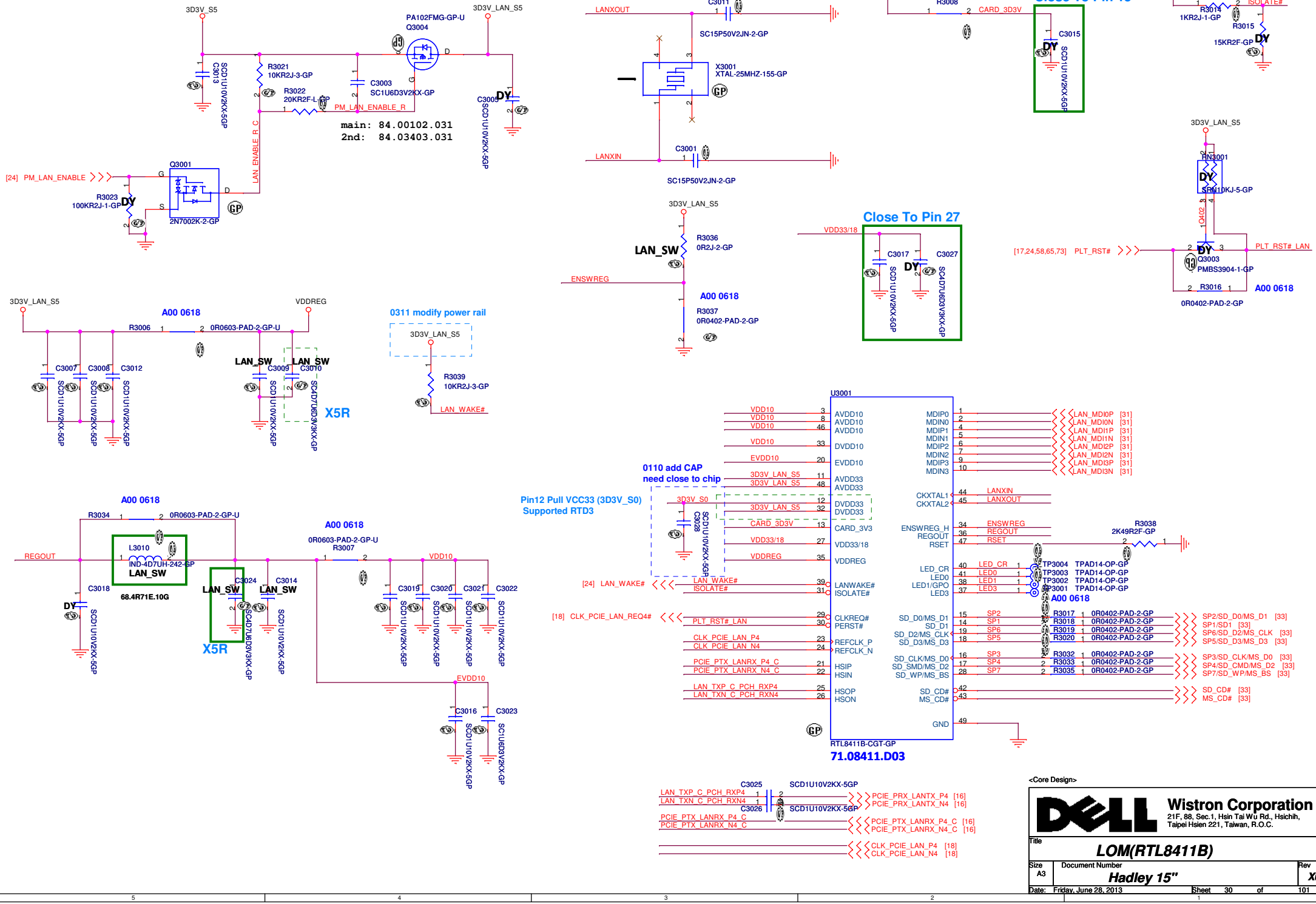
SSID = LOM



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

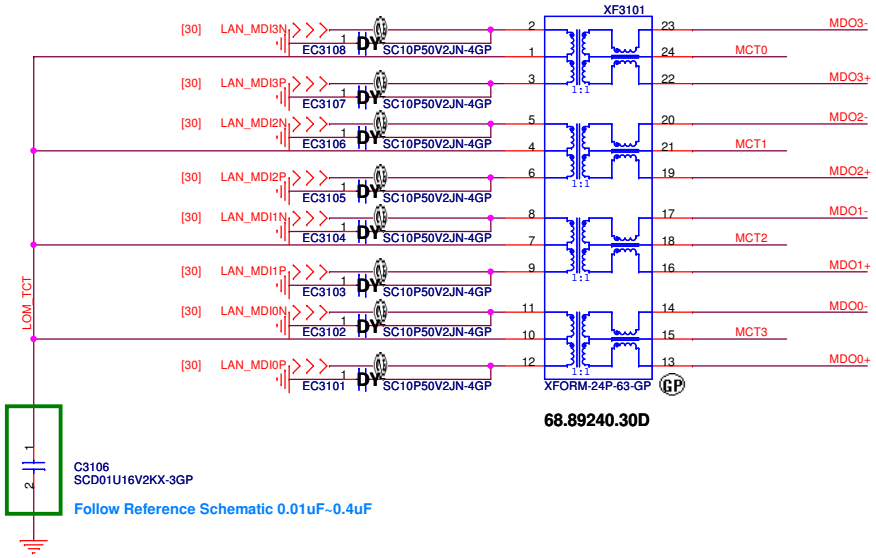
Title: LOM(RTL8411B)

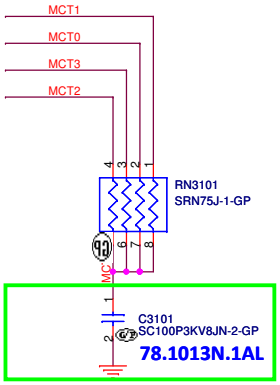
Size	Document Number	Rev
A3	Hadley 15"	X02

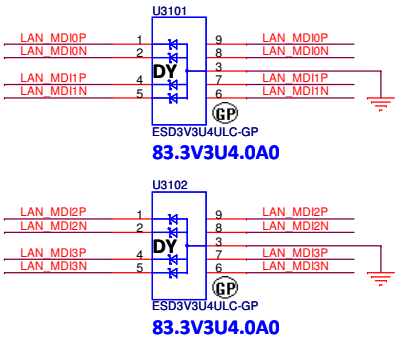
Date: Friday, June 28, 2013 Sheet 30 of 101

SSID = LOM

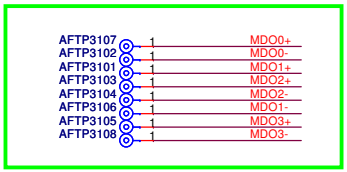
GIGA LAN TransFormer

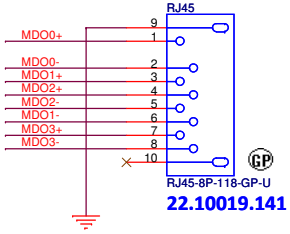






Layout:
Place near RJ45





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RJ45+Transformer

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 31 of 101

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

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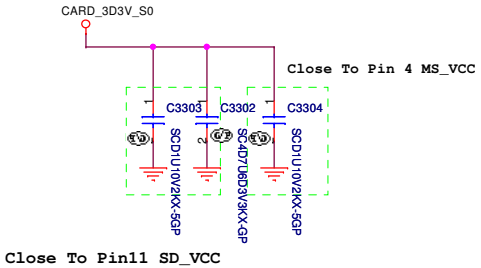
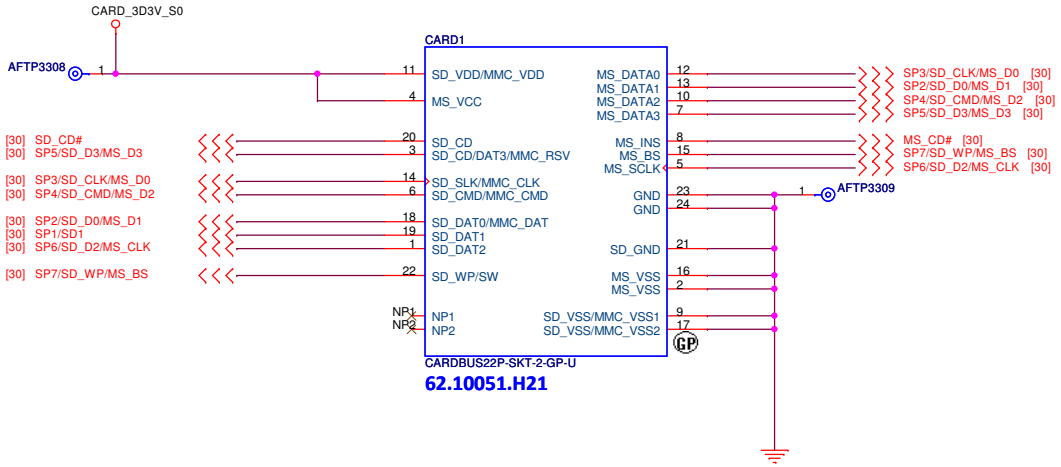
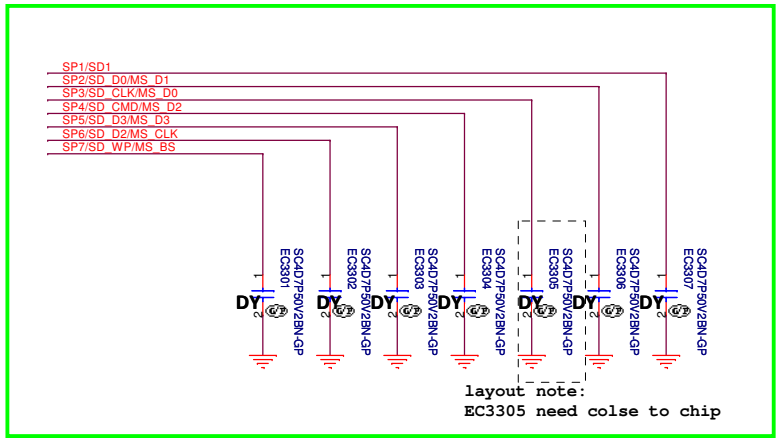
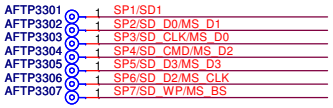
SSID = SDIO





Reserve EMI Cap, 0107 CLK Cap DY





<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	Card Reader CONN	
Size: A3	Document Number: Hadley 15"	Rev: X02
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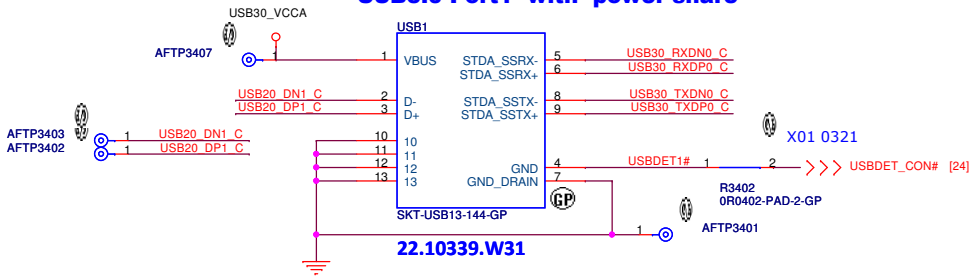
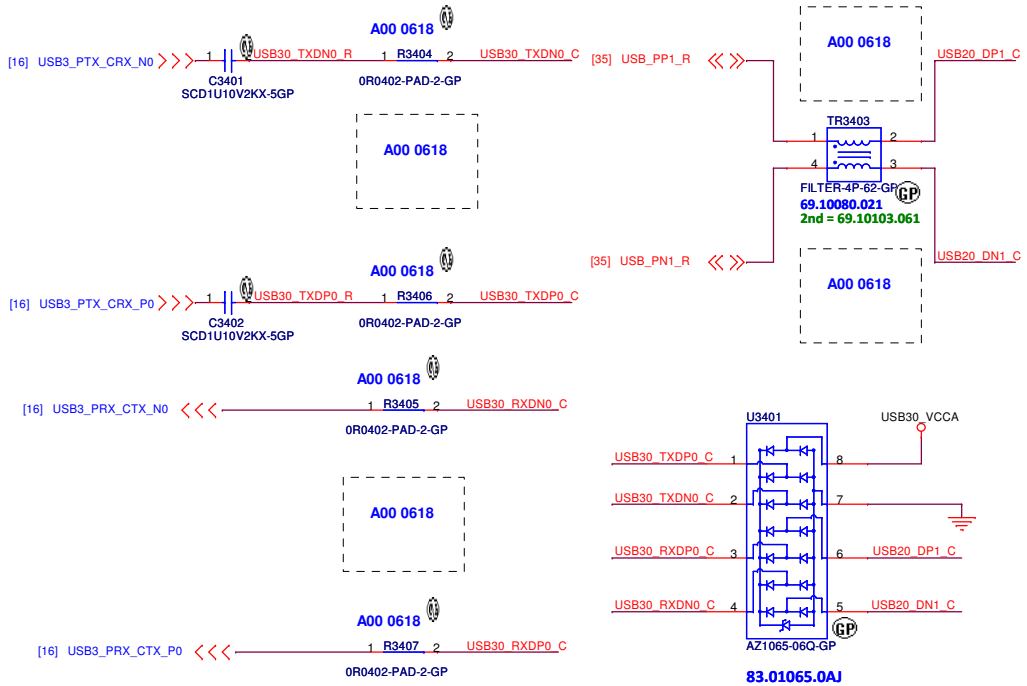
SSID = USB

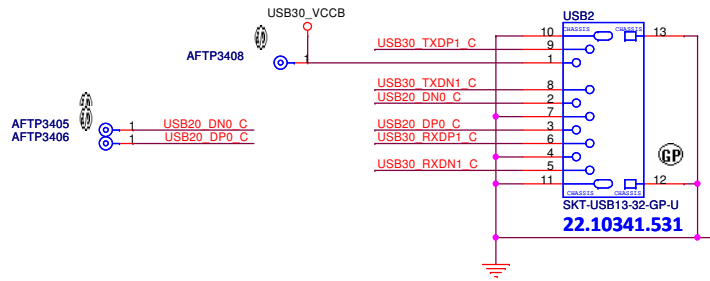
USB3.0 Port1 with power share



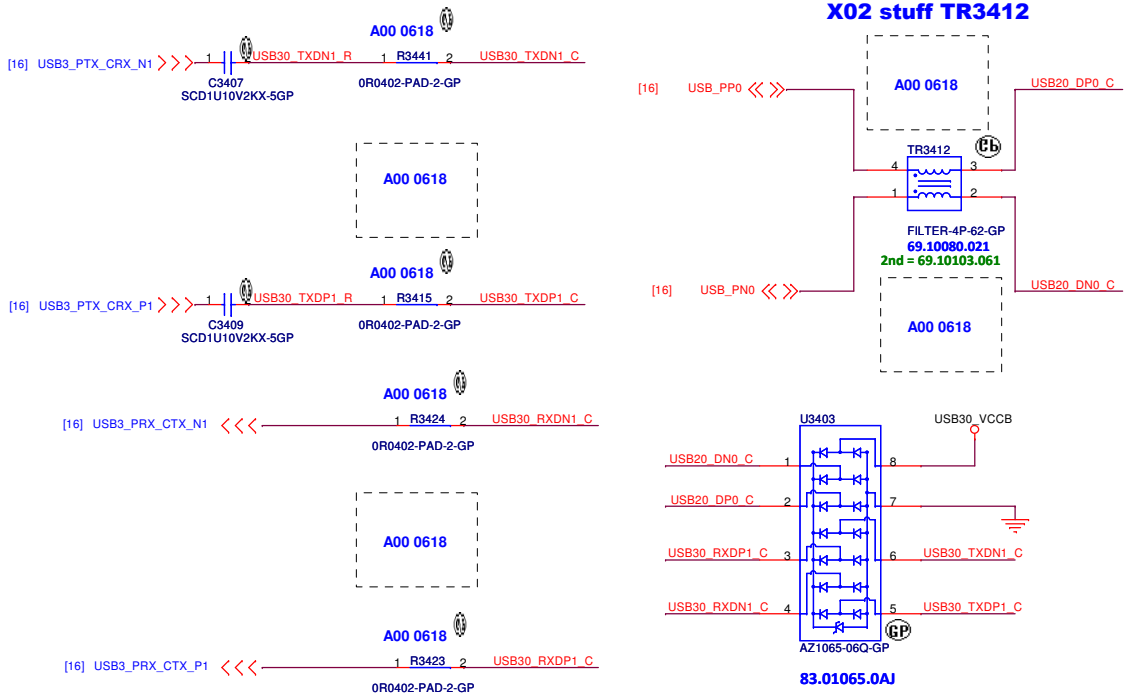
X02 stuff TR3403



USB3.0 Port2



X02 stuff TR3412



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB3.0(1)	
Size: A3	Document Number: Hadley 15"	Rev: X02
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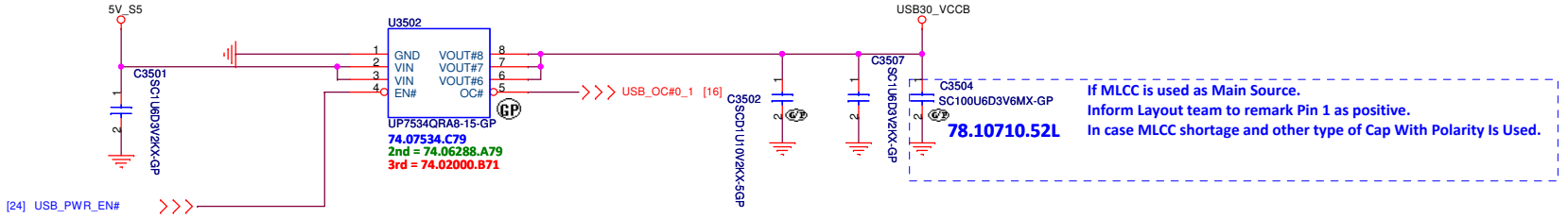
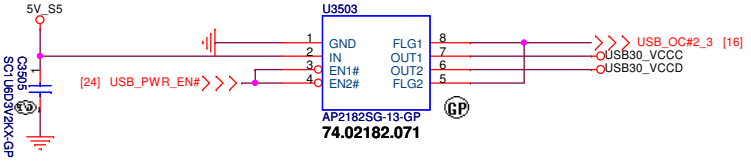
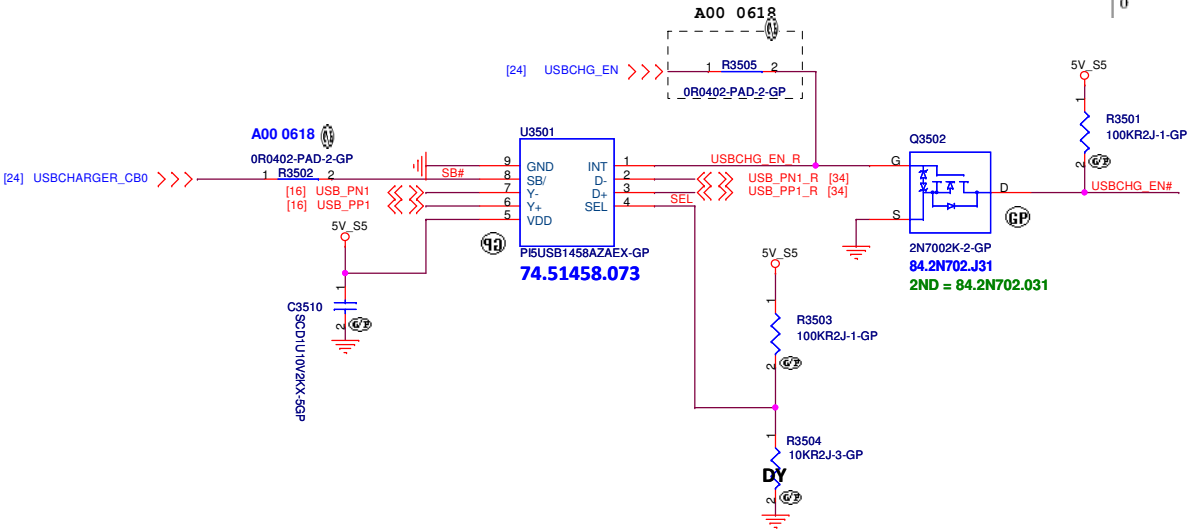
SSID = USB

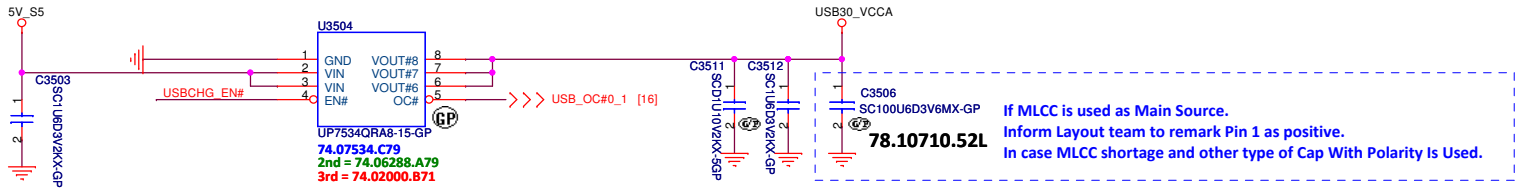




SB/ (pin 8)	SEL(pin 4)	Feature	pin 1 role (INT or INT/)
0	0	Auto S & C without mouse/keyboard pass through	INT or INT/
0	1	Auto S & C with mouse/keyboard pass through	INT or INT/
1	0	S0 charging with SDP only	INT or INT/
1	1	S0 charging with CDP or SDP only (depending on external device)	INT or INT/
0	M= (1/2)*V_{DD}	Test Mode, M = $V_{DD/2}$ = (1/2)*V_{DD}	

0319 modify USB Charger circuit





USB Power SW (U3504)

Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DII (Diodes)	AP2301MPG-13	74.02301.071	2ND
GMT	G547I2P81U	74.00547.F79	3RD

<Core Design>

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Title: USB Power SW

Size | Document Number: Hadley 15" | Rev: X02

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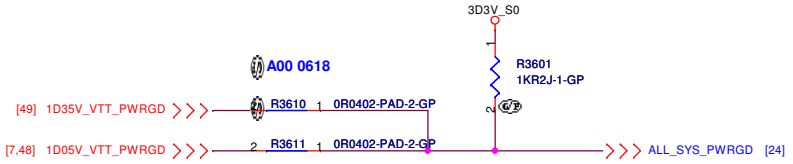
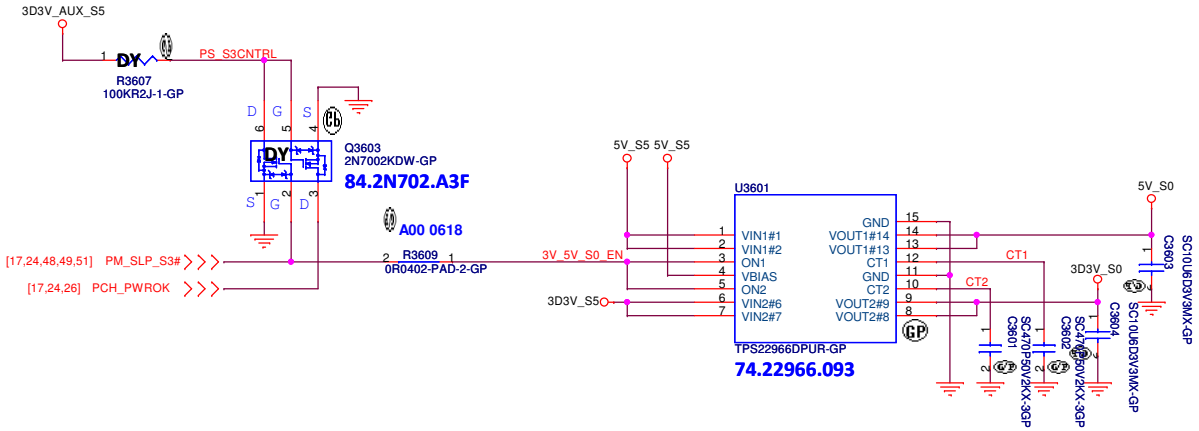
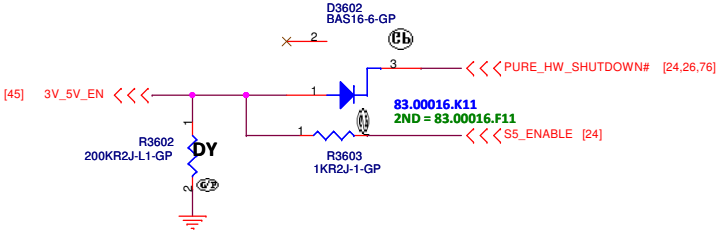
SSID = Reset.Suspend

Power Good



ROSA Run Power





5V_S0

5V_S0 Comsumption
Peak current 4.033A

3D3V_S0

3D3V_S0 Comsumption
Peak current 3A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable		
Size: A3	Document Number: Hadley 15"	Rev: X02
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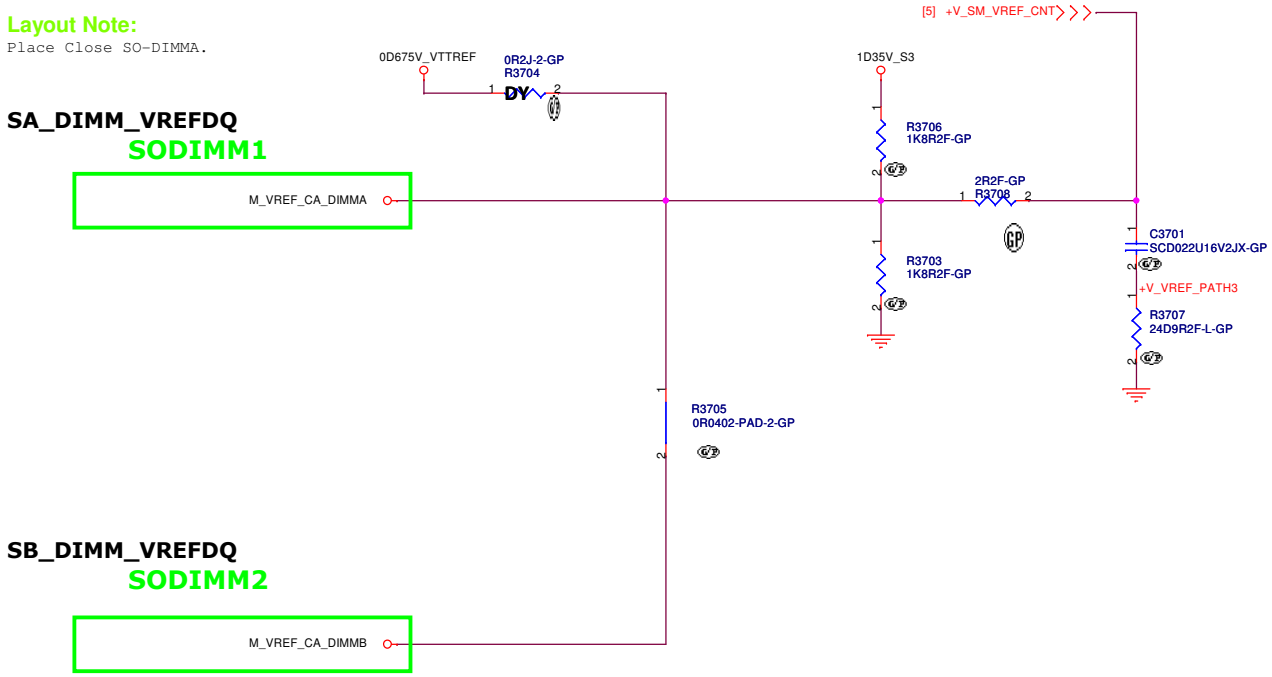
SSID = Reset.Suspend

Layout Note:
Place Close SO-DIMMA.



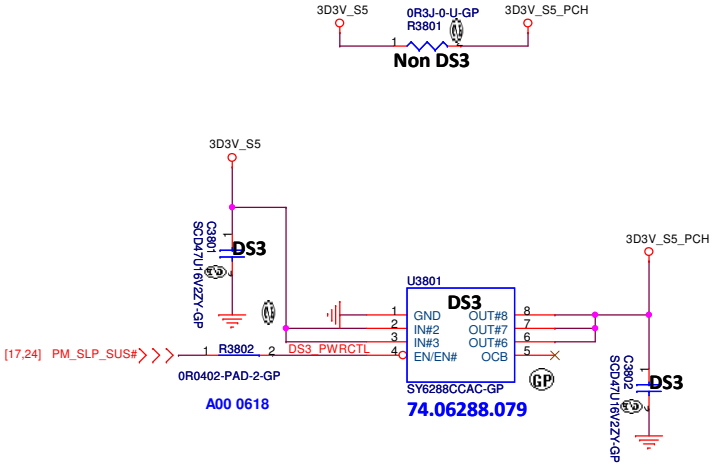
Close to DIMM
S3 Power Reduction Circuit PM_DRAM_PWRGD

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	S3 Power Reduction	
Size A3	Document Number Hadley 15"	Rev X02
Date: Friday, June 28, 2013	Sheet 37 of 101	

SSID = Reset.Suspend



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DSW	
Size: A3	Document Number: Hadley 15"	Rev: X02
Date: Friday, June 28, 2013	Sheet 38 of 101	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 28, 2013 | Sheet 39 of 101

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 28, 2013 | Sheet 40 of 101

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 28, 2013 | Sheet 41 of 101

SSID = PWR.Support

0103 Add EC4203
ndde close to EL4202

Layout Note:
PSID Layout width > 25mil

A00 0618

A00 0619

DT MODE

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm

<Core Design>

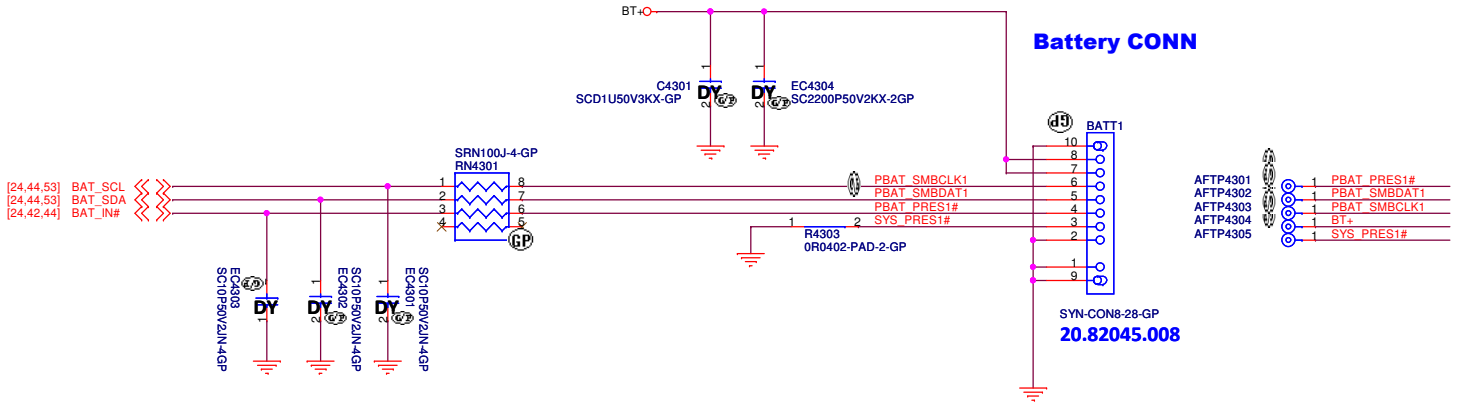
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN

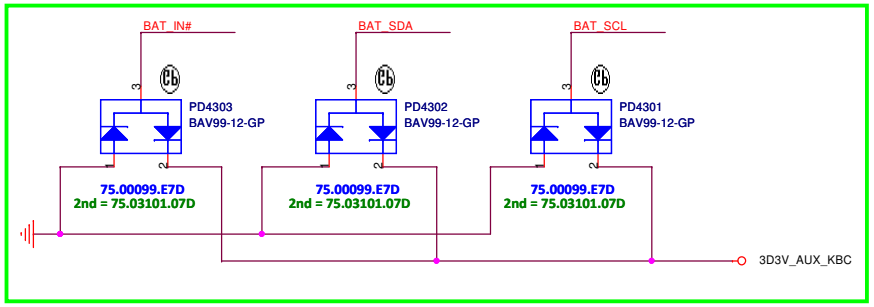
Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 42 of 101

SSID = PWR.Support



0109 DY PD4301~4303



Layout Note:
Place near Battery CONN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 43 of 101

SSID = Charger

KBC FOR DT MODE
CHECK EE PULL HIGH

PU4406 and PU4407:
main source: 84.03660.037

VacDET=2.4V
Acok setting=2.4*((PR4444+PR4411)/PR4411)
Setting=18.178v

ACAV_IN
H=ACIN
L=UNAC

DIS_DTM:
H= cell is plus to GND. (reset charger ic)
L=nornal

Follow custormer circuits

Follow custormer circuits

PWR_CHG_ACOK:
PWR_CHG_REGN=6V
V+=6*(PR4404/(PR4410+PR4404))=3.27V

CHECK EE

Close PR4443

CHECK PM BATTERY TYPE
CHECK CELL for DT mode

PWR_CHG_CMPIN:
V-=3.3*(PR4202/(PR4428+PR4402))=1.099V

CHECK PM ADAPTER TYPE
And setting adapter type

BATTERY MON

A00 0618

DIS_DTM_HW:
PWR_CHG_REGN=6V
V+=6*(PR4440/(PR4441+PR4440))=3.27V
Setting=3.27*((PR4442+PR4447)/PR4447)=9V

CHECK EE
follow custormer circuits.

ADAPTER TYPE	AD_IA_HW	AD_IA_HW_2	SETTING
90W	L	L	1.099V
65W	H	L	0.862329V
45W	L	H	0.659648V

<Core Design>

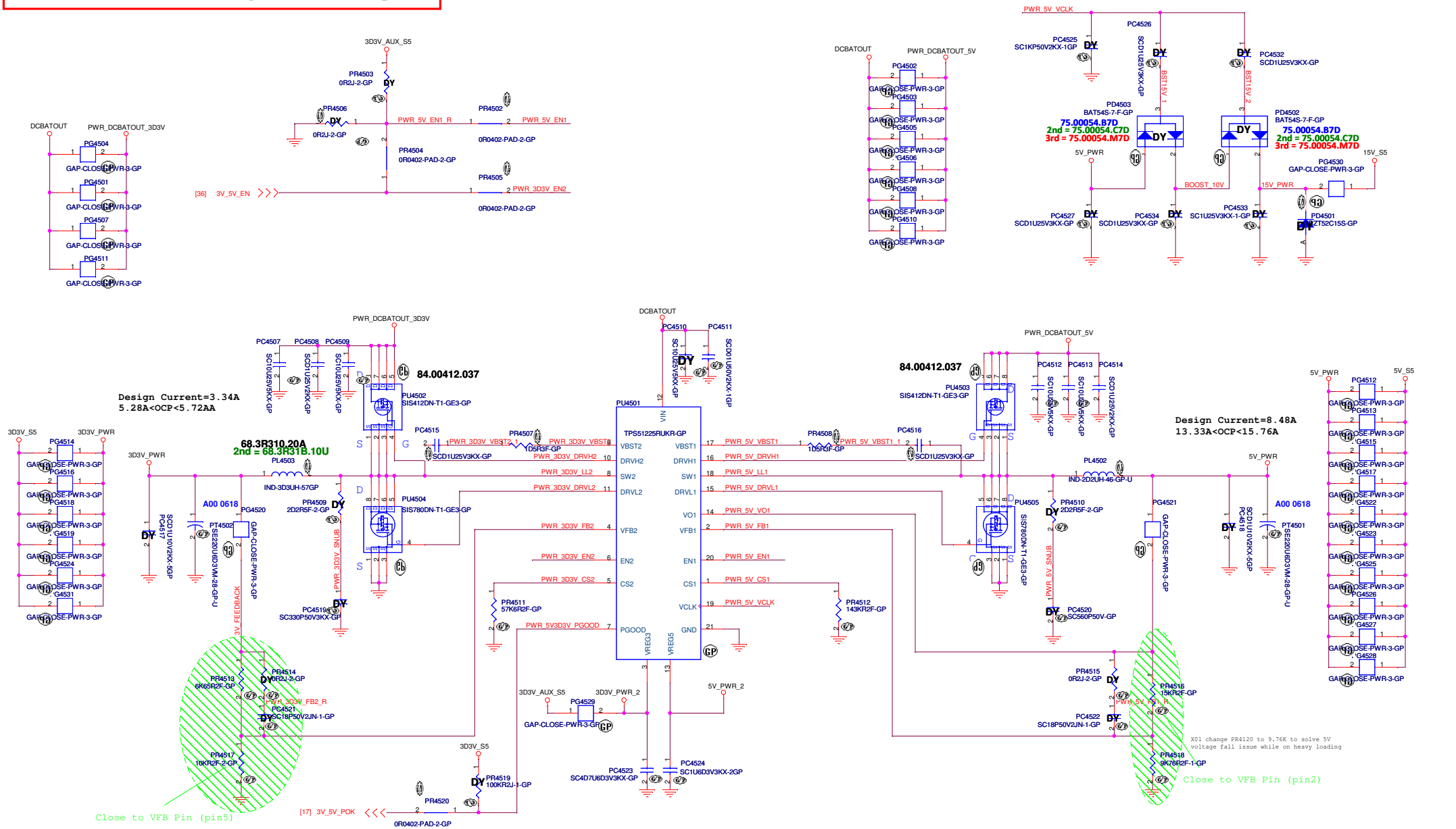
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGE(BQ24715)

Size: Custom | Document Number | Rev: X02

Date: Friday, June 28, 2013 | Sheet 44 of 101

SSID = PWR.Plane.Regulator_5v3p3v



<Core Design>

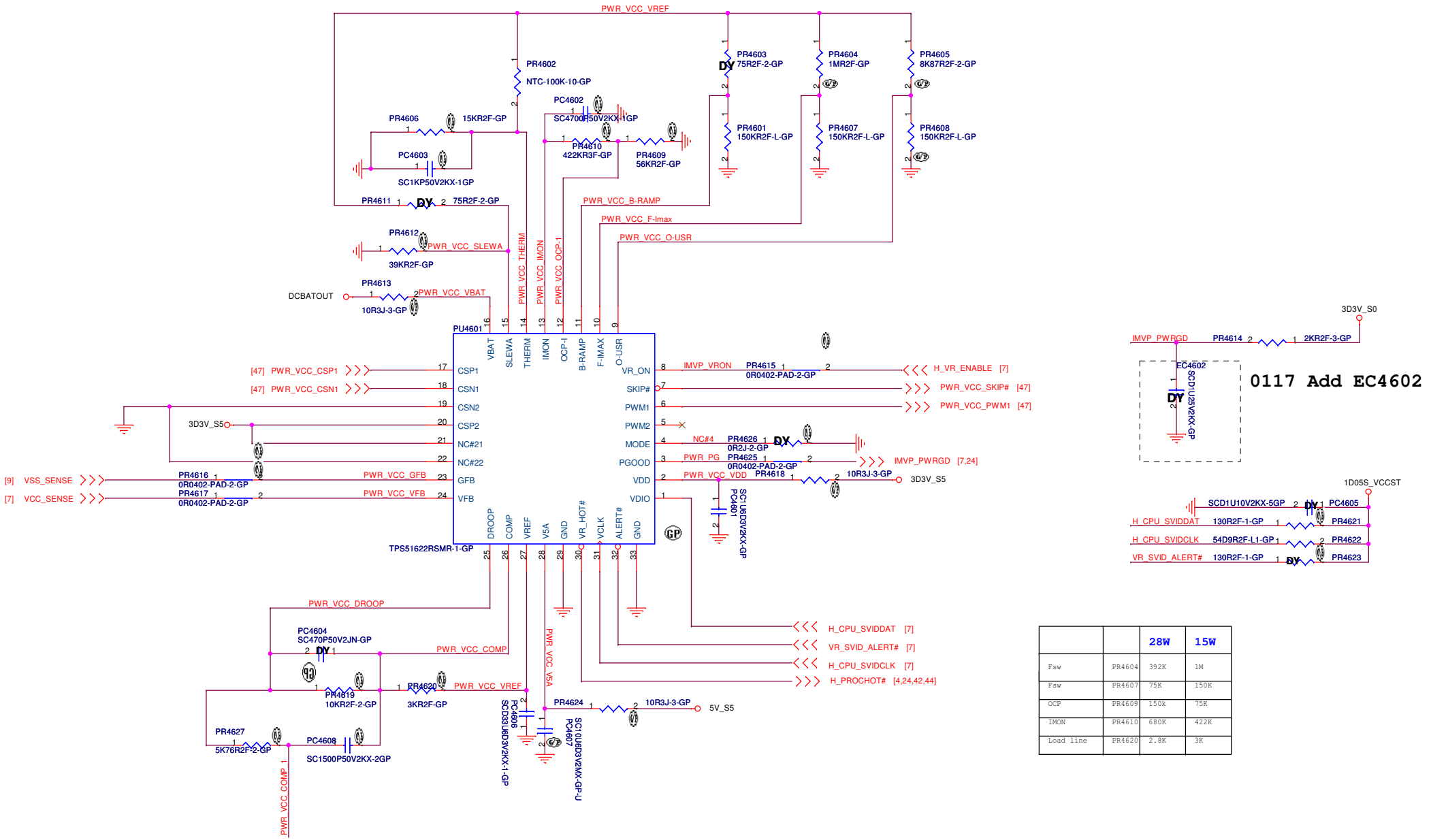
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3V/5V TPS51225

Size	Document Number	Rev
Custom	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 45 of 101

SSID = CPU.Regulator



		28W	15W
Fsw	PR4604	392K	1M
Fsw	PR4607	75K	150K
OCP	PR4609	150k	75K
IMON	PR4610	680K	422K
Load line	PR4620	2.8K	3K

<Core Design>

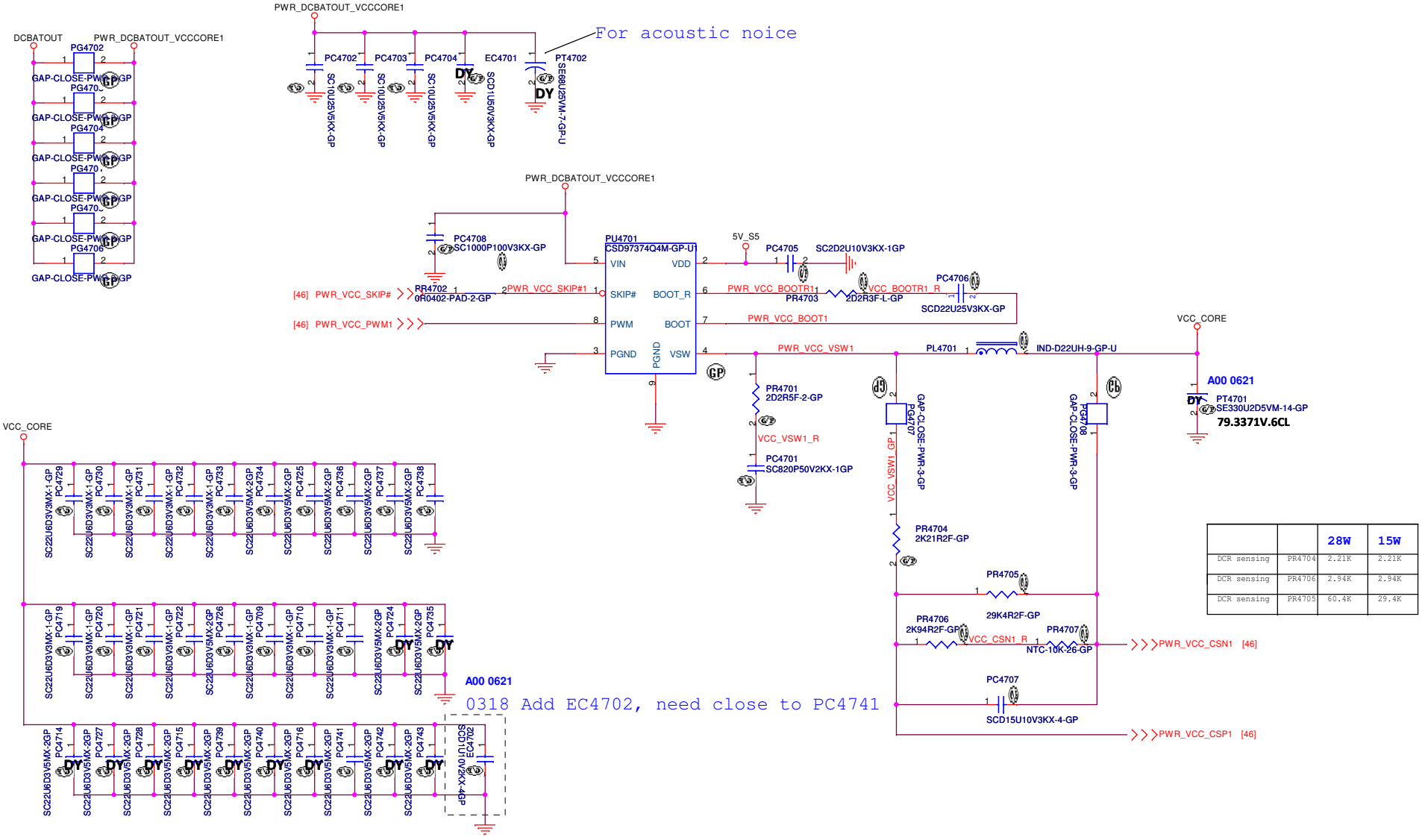
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51622_CPUCORE(1/2)

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 46 of 101

SSID = CPU.Regulator



		28W	15W
DCR sensing	PR4704	2.21K	2.21K
DCR sensing	PR4706	2.94K	2.94K
DCR sensing	PR4705	60.4K	29.4K

A00 0621

0318 Add EC4702, need close to PC4741

28W CPU need stuff PC4743, PC4728, PC4739, PC4724, PC4735, PC4738

<Core Design>

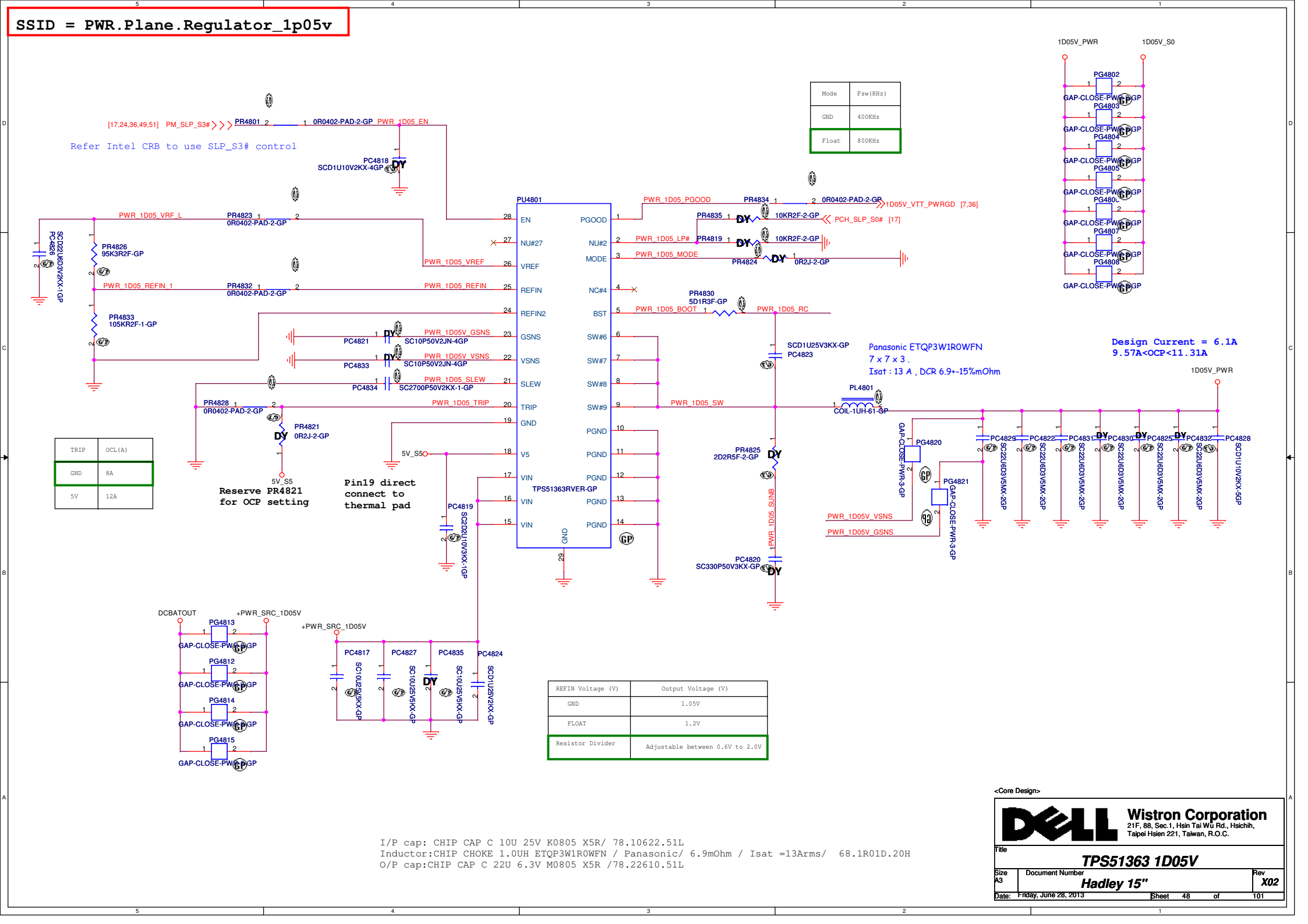
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51622_CPUCORE(2/2)

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 47 of 101

SSID = PWR.Plane.Regulator_1p05v



Mode	Fsw(KHz)
GND	400KHz
Float	800KHz

TRIP	OCL(A)
GND	8A
5V	12A

REFIN Voltage (V)	Output Voltage (V)
GND	1.05V
FLOAT	1.2V
Resistor Divider	Adjustable between 0.6V to 2.0V

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 1.0UH ETQP3W1R0WFN / Panasonic/ 6.9mOhm / Isat =13Arms/ 68.1R01D.20H
O/P cap:CHIP CAP C 22U 6.3V M0805 X5R /78.22610.51L

<Core Design>

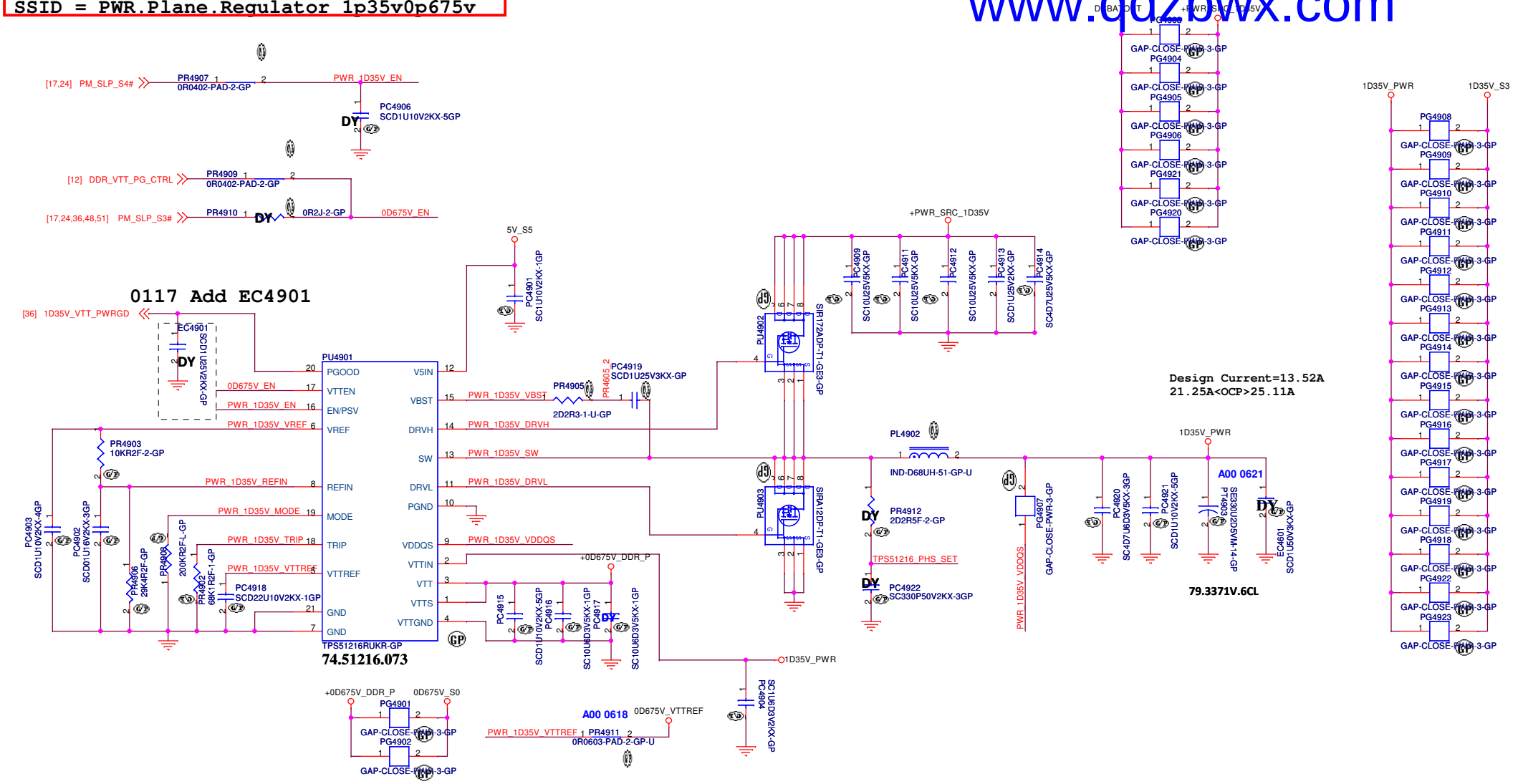
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51363 1D05V

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 48 of 101

SSID = PWR.Plane.Regulator 1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 1.0UH PCMB104T-1R0M/ 3.3mohm/ Isat =28A rms /68.1R01C.10Q
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S: SIR172ADP-T1-GE3 / 8.5mohm/10.5mOhm@4.5Vgs/ 84.00172.A37
L/S: SIRA12DP-T1-GE3 / 4.4mohm/6mOhm@4.5Vgs/ 84.SRA12.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51216_+1.35V_SUS

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 26, 2015 | Sheet 49 of 101

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

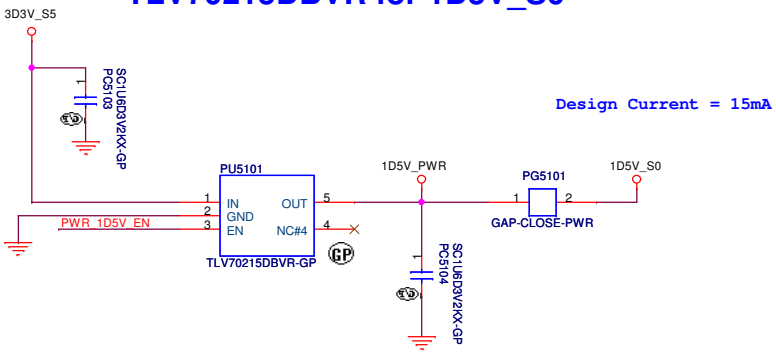
Title: (Reserved)TPS51312 1D8V

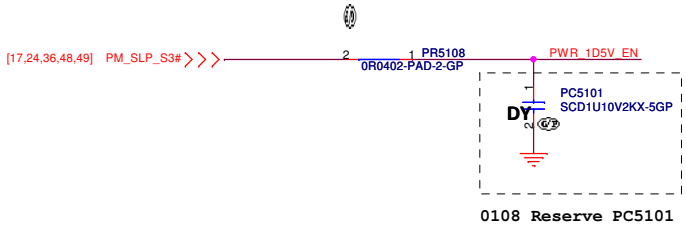
Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 50 of 101

SSID = PWR.Plane.Regulator_1p5v

TLV70215DBVR for 1D5V_S0





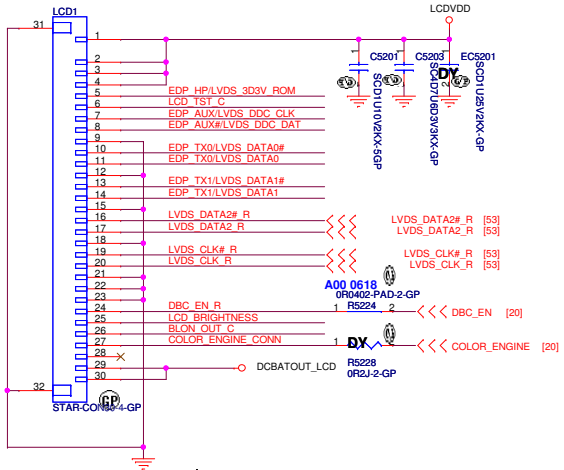
0108 Reserve PC5101

<Core Design>

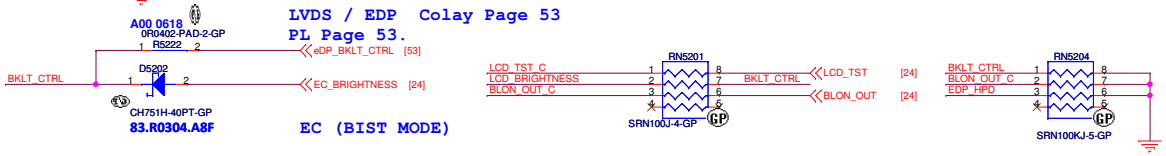
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT9198-15PU5R_1D5V	
Size A3	Document Number Hadley 15"	Rev X02
Date: Friday, June 28, 2013	Sheet 51 of 101	

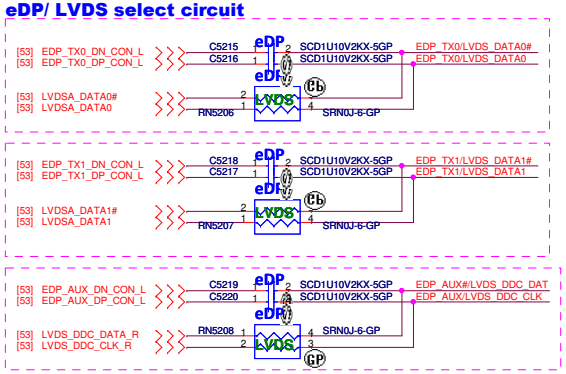
SSID = VIDEO



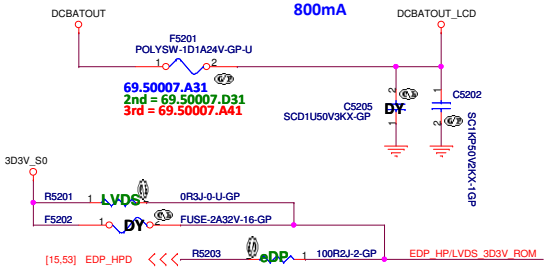
Pin	eDP	LVDS	Pin	eDP	LVDS
1	LCDVDD	LCDVDD	16	NC	LVDS_DATA2#
2	LCDVDD	LCDVDD	17	NC	LVDS_DATA2
3	LCDVDD	LCDVDD	18	GND	GND
4	LCDVDD	LCDVDD	19	NC	LVDS_CLK#_R
5	EDP_HP	3D3V_ROM	20	NC	LVDS_CLK_R
6	LCD_TST_C	LCD_TST_C	21	GND	GND
7	EDP_AUX	LVDS_DDC_CLK	22	GND	GND
8	EDP_AUX#	LVDS_DDC_DAT	23	GND	GND
9	GND	GND	24	DBC_EN	DBC_EN
10	EDP_TX0N	LVDS_DATA0#	25	BRIGHTNESS	BRIGHTNESS
11	EDP_TX0P	LVDS_DATA0	26	BLON_OUT	BLON_OUT
12	GND	GND	27	Color_Engine	Color_Engine
13	EDP_TX1N	LVDS_DATA1#	28	NC	NC
14	EDP_TX1P	LVDS_DATA1	29	DCBATOUT_LCD	DCBATOUT_LCD
15	GND	GND	30	DCBATOUT_LCD	DCBATOUT_LCD



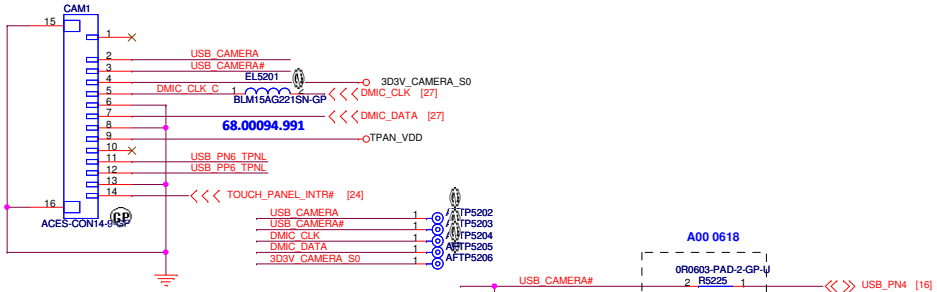
eDP/ LVDS select circuit



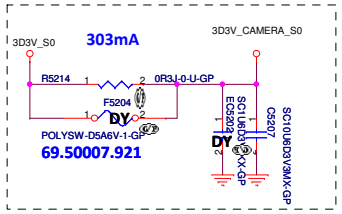
INVERTER POWER



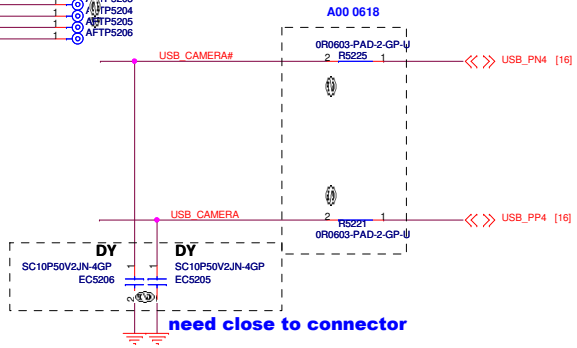
X02 change CAM1 connector



Camera Power

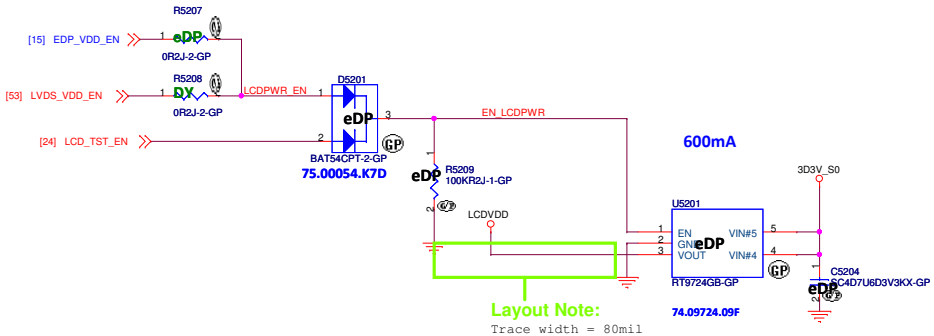


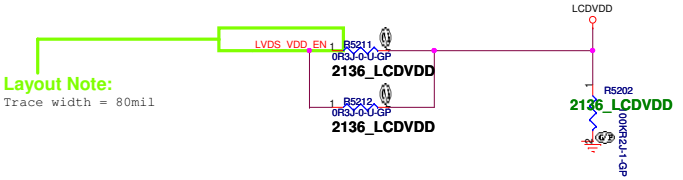
CAMERA



LCDVDD

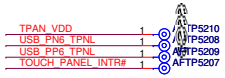
LCD Power

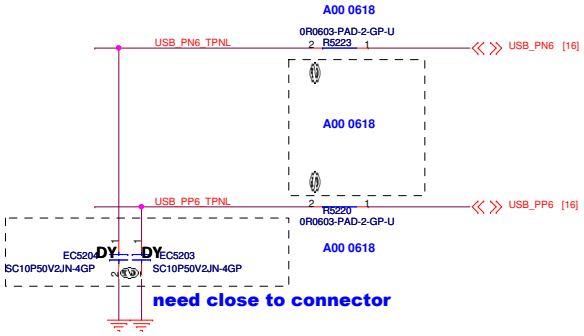




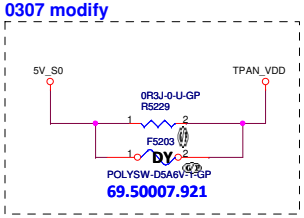
Touch panel

X02 remove TPNL1





0307 modify



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size: Custom | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 52 of 101

SSID = VIDEO

LVDS & EDP Colay

Layout Note:
Place near U5301

[8] EDP_TX1_DN
[8] EDP_TX1_DP
C5209 SCD1U10V2KX-5GP EDP_TX1_DN_RTS2136
C5210 SCD1U10V2KX-5GP EDP_TX1_DP_RTS2136
RN5303 SRN0J-6-GP
EDP_TX1_DN_CON_L
EDP_TX1_DP_CON_L
EDP_TX1_DN_CON_L [52]
EDP_TX1_DP_CON_L [52]

[8] EDP_TX0_DN
[8] EDP_TX0_DP
C5211 SCD1U10V2KX-5GP EDP_TX0_DN_RTS2136
C5212 SCD1U10V2KX-5GP EDP_TX0_DP_RTS2136
RN5302 SRN0J-6-GP
EDP_TX0_DN_CON_L
EDP_TX0_DP_CON_L
EDP_TX0_DN_CON_L [52]
EDP_TX0_DP_CON_L [52]

[8] EDP_AUX_DN
[8] EDP_AUX_DP
C5213 SCD1U10V2KX-5GP EDP_AUX_DN_RTS2136
C5214 SCD1U10V2KX-5GP EDP_AUX_DP_RTS2136
RN5304 SRN0J-6-GP
EDP_AUX_DN_CON_L
EDP_AUX_DP_CON_L
EDP_AUX_DN_CON_L [52]
EDP_AUX_DP_CON_L [52]

Brightness

[15] L_BKLT_CTRL
R5319 0R2J-2-GP 2136_PWM_IN
R5320 0R2J-2-GP eDP_BKLT_CTRL
eDP_BKLT_CTRL [52]
R5302 1KR2J-1-GP
[15,52] EDP_HPD
EDP_HPD_RTS2136

3D3V_S0
L5301 MPZ1608S600AT-GP 68.00212.011
DP_AVCC33
C5312 SCD1U10V2KX-5GP
C5303 SCD1U10V2KX-5GP
C5301 SC10U6D3V3MX-GP

3D3V_S0
L5302 MPZ1608S600AT-GP 68.00212.011
DP_DVCC33
C5317 SCD1U10V2KX-5GP
C5302 SC10U6D3V3MX-GP
C5313 SCD1U10V2KX-5GP

L5303 IND-4D7UH-300-GP
SWR_LX
SWR_V12
2136_SW
A00 0618
0R0603-PAD-2-GP-U
R5314
C5304 SC10U6D3V3MX-GP
C5306 SCD1U10V2KX-5GP

X02 change to 4P2R
RN5306 SRN100KJ-6-GP
TEST_MODE
2136_PWM_IN

[24] LVDS_R2136_BKLT_EN
[52] LVDS_DDC_DATA_R
[52] LVDS_DDC_CLK_R
EEPROM_SDA0
EEPROM_SCL0
SWR_V12
C5311 SCD1U10V2KX-5GP

U5301 RTD2136R-CGT-GP 71.02136.B03
GND
MODE_CFG1
MODE_CFG0
MICSDA
MICSCL
BL_EN
VCCK
TXO0-
TXO0+
TXO1-
TXO1+
TXO2-
TXO2+
HPD
TEST
AUX_N
AUX_P
DP_V33
DP_GND
LANE0_P
LANE0_N
LANE1_P
LANE1_N
DP_V12
DP_REXT
TXOC-
TXOC+
TXO3-
TXO3+
TXE0-
TXE0+
TXE1-
TXE1+
TXE2-
TXE2+
TXEC-
TXEC+
CIICSCL
CIICSDA
SWR_VCCK
SWR_GND
SWR_LX
SWR_VDD
PWM_OUT
PANEL_VCC
PWM_IN
PVCC
TXE3+
TXE3-

LVDSA_DATA0# [52]
LVDSA_DATA0 [52]
LVDSA_DATA1# [52]
LVDSA_DATA1 [52]
LVDSA_DATA2# [52]
LVDSA_DATA2 [52]
LVDS_DATA2_R [52]
LVDS_CLK#_R [52]
LVDS_CLK_R [52]

EDP_HPD_RTS2136
TEST_MODE
EDP_AUX_DN_RTS2136
EDP_AUX_DP_RTS2136
DP_AVCC33
EDP_TX0_DP_RTS2136
EDP_TX0_DN_RTS2136
EDP_TX1_DP_RTS2136
EDP_TX1_DN_RTS2136
SWR_V12
DP_REXT
R5301 12KR2F-L-GP
C5310 SCD1U10V2KX-5GP

Close to PIN5
DP_AVCC33
C5316 SCD1U10V2KX-5GP

CIICSCL1
CIICSDA1
SWR_V12
SWR_LX
DP_DVCC33
C5309 SCD1U10V2KX-5GP
[52] eDP_BKLT_CTRL
[52] LVDS_VDD_EN
2136_PWM_IN

DP_DVCC33
C5308 SCD1U10V2KX-5GP
C5307 SCD1U10V2KX-5GP
Close to PIN13

3D3V_S0
R5306 4K7R2J-4-GP
R5317 4K7R2J-4-GP
EEPROM_SCL0
EEPROM_SDA0
R5318 4K7R2J-2-GP
R5307 4K7R2J-2-GP

Operation Mode Table

		PIN47	
		0	1
PIN48	0	X	EP Mode
	1	ROM	EEPOOM

RN5301 SRN4K7J-10-GP
LVDS_DDC_DATA_R
LVDS_DDC_CLK_R
3D3V_S0
CIICSDA1
CIICSCL1
Q5301 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
3rd = 84.2N702.E3F
4th = 84.2N702.F3F
CIICSDA
CIICSCL
RN5307 SRN0J-6-GP
SML0_DATA [18]
SML0_CLK [18]
PCH
PCH
RN5305 SRN0J-6-GP
BAT_SDA [24,43,44]
BAT_SCL [24,43,44]
KBC
KBC

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS_Switch
Size: Custom
Document Number: Hadley 15"
Rev: X02
Date: Friday, June 28, 2013
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SSID = VIDEO

0307 change RN5401 RN5402 form 680 ohm to 470 ohm

5V_S0 → F5401 POLYSW-1D1A8V-5-GP → 5V_HDMI_S0

U5401 2N7002K-2-GP 84.2N702.J31 (HDMI_PLL_GND)

RN5402 SRN470J-5-GP, RN5401 SRN470J-5-GP

[8] HDMI_CLK#	C5401 SCD1U10V2KX-5GP	HDMI_CLK_R_C#	
[8] HDMI_CLK	C5402 SCD1U10V2KX-5GP	HDMI_CLK_R_C	
[8] HDMI_DATA0#	C5403 SCD1U10V2KX-5GP	HDMI_DATA0_R_C#	
[8] HDMI_DATA0	C5404 SCD1U10V2KX-5GP	HDMI_DATA0_R_C	
[8] HDMI_DATA1#	C5405 SCD1U10V2KX-5GP	HDMI_DATA1_R_C#	
[8] HDMI_DATA1	C5406 SCD1U10V2KX-5GP	HDMI_DATA1_R_C	
[8] HDMI_DATA2#	C5407 SCD1U10V2KX-5GP	HDMI_DATA2_R_C#	
[8] HDMI_DATA2	C5408 SCD1U10V2KX-5GP	HDMI_DATA2_R_C	

0R3J-0-U-GP R5401 — HDMI_CLK_R_C → HDMI_CLK_R_C_CON — A00 0618 — A00 0619 ER5401 150R2J-L1-GP-U

0R3J-0-U-GP R5402 — HDMI_CLK_R_C# → HDMI_CLK_R_C#_CON

0R3J-0-U-GP R5403 — HDMI_DATA0_R_C → HDMI_DATA0_R_C_CON — A00 0618 — A00 0619 ER5402 150R2J-L1-GP-U

0R3J-0-U-GP R5404 — HDMI_DATA0_R_C# → HDMI_DATA0_R_C#_CON

0R3J-0-U-GP R5406 — HDMI_DATA2_R_C# → HDMI_DATA2_R_C#_CON

0R3J-0-U-GP R5407 — HDMI_DATA1_R_C → HDMI_DATA1_R_C_CON — A00 0618 — A00 0619 ER5404 150R2J-L1-GP-U

0R3J-0-U-GP R5408 — HDMI_DATA1_R_C# → HDMI_DATA1_R_C#_CON

ER5401~04 change to 180R

5V_HDMI_S0 → D5401 BAW56-11-GP (D5102 2, D5102 1) 75.00056.B7D 2nd = 75.00056.A7D

RN5203 SRN2K2J-1-GP

3D3V_S0 → Q5401 2N7002KDW-GP 84.2N702.A3F

[15] PCH_HDMI_CLK → DDC_CLK_HDMI

[15] PCH_HDMI_DATA → DDC_DATA_HDMI

HDMI CONN

HDMI1 SKT-HDMI23-97-GP 22.10296.A31

HDMI_DATA2_R_C_CON, HDMI_DATA2_R_C#_CON, HDMI_DATA1_R_C_CON, HDMI_DATA1_R_C#_CON, HDMI_DATA0_R_C_CON, HDMI_DATA0_R_C#_CON, HDMI_CLK_R_C_CON, HDMI_CLK_R_C#_CON, DDC_CLK_HDMI, DDC_DATA_HDMI

5V_HDMI_S0 → AFTP5401 → C5417 SCD1U10V2KX-5GP → TP5411 → HPD_HDMI_CON

3D3V_S0 → PMBS3904-1-GP Q5402 84.03904.L06 — HDMI_HPD_B — R5411 150KR2J-L1-GP

[15] HDMI_PCH_DET → R5413 0R0402-PAD-2-GP — HDMI_HPD_E

R5414 10KR2J-3-GP

DY R5412 20KR2J-L2-GP

<Core Design>

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Title: **HDMI Repeater/Connector**

Size: A3 | Document Number: **Hadley 15"** | Rev: **X02**

Date: Friday, June 28, 2013 | Sheet 54 of 101

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<Core Design>

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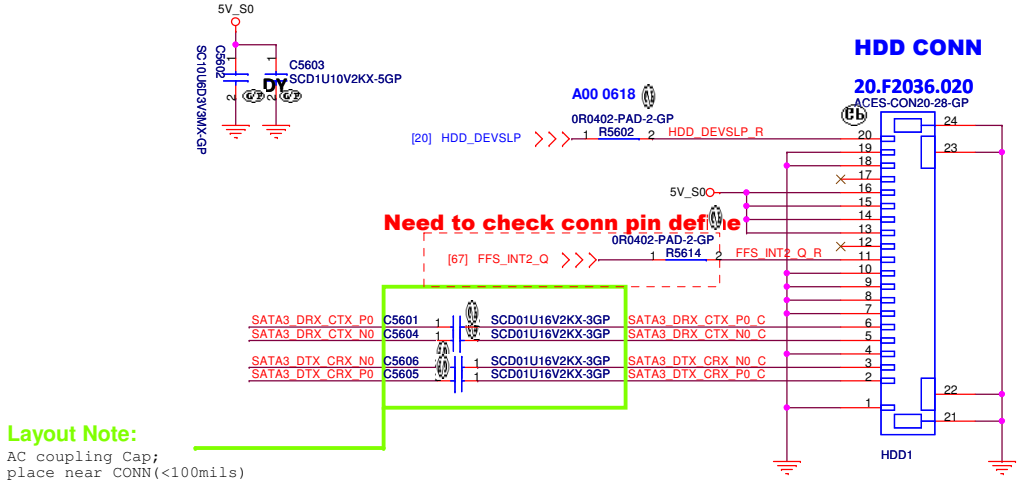
Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 28, 2013 | Sheet 55 of 101

SSID = SATA



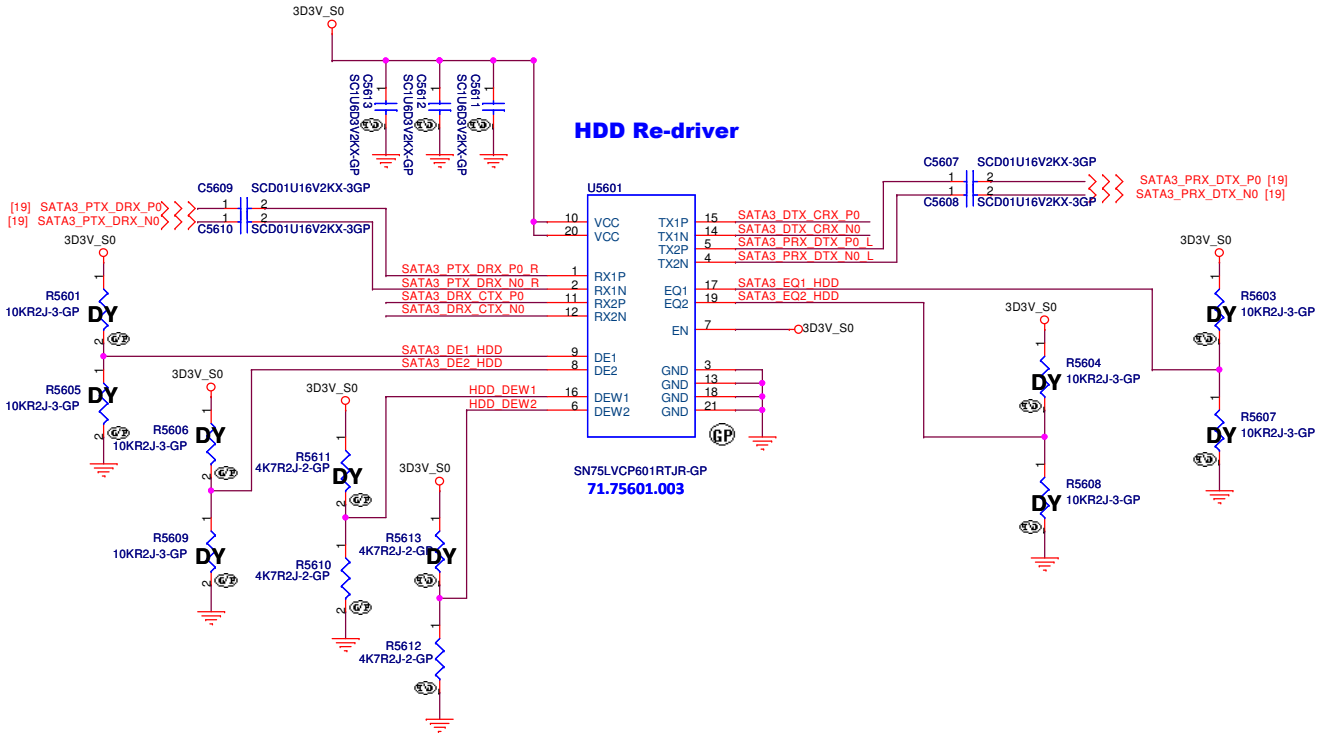


Table 1: Tx/Rx EQ & DE Pulse Width Settings

DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps
NC (*default*)	-6
0	0
1	-3

EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)
NC (*default*)	0
0	7
1	14

DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (*default*)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

<Core Design>

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Title: HDD

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 56 of 101

(Blanking)

<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

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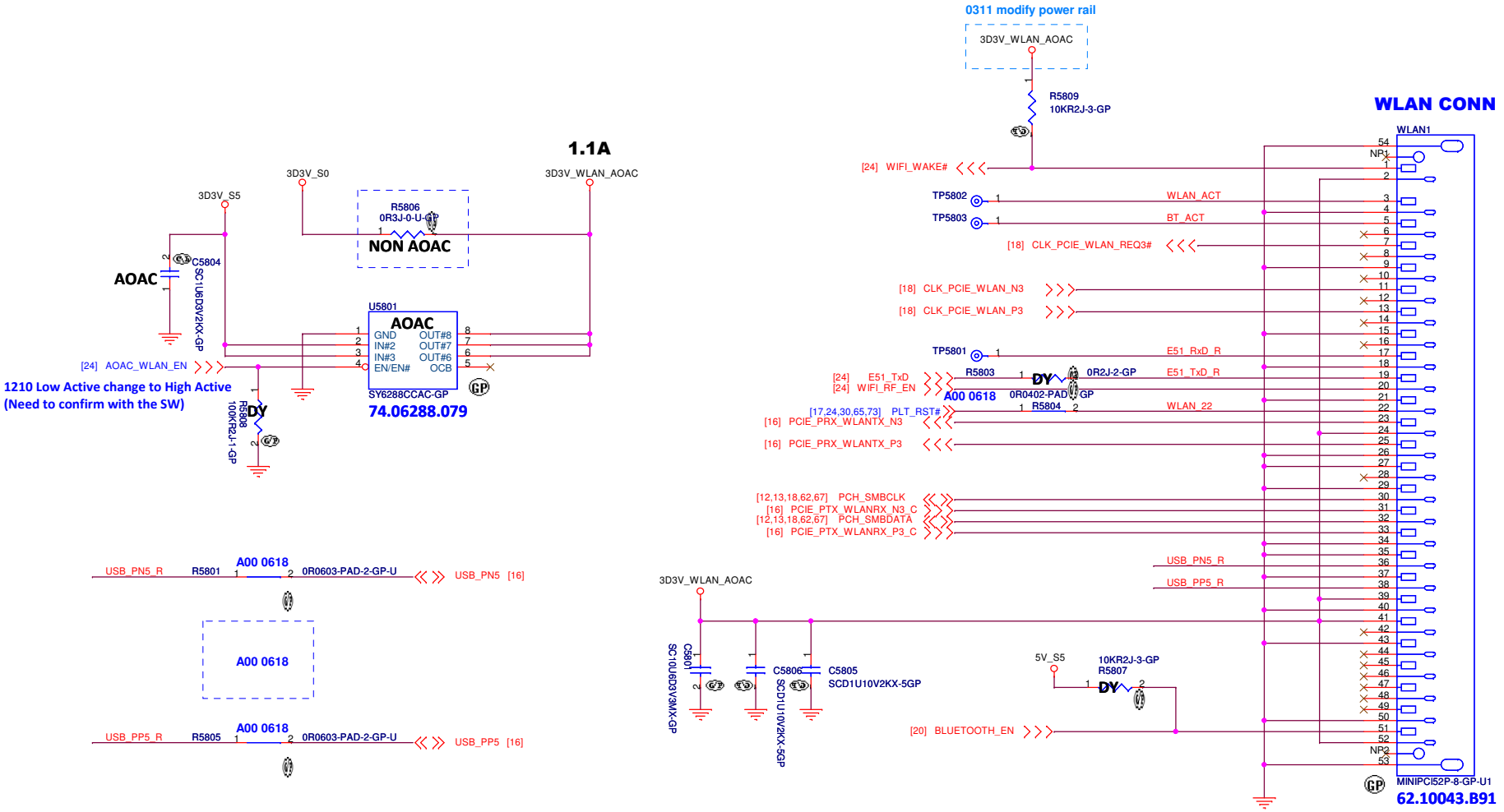
SSID = Wireless



<Core Design>

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Title	WLAN/BT	
Size: A3	Document Number: Hadley 15"	Rev: X02
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Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

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Title: *Reserved*

Size	Document Number	Rev
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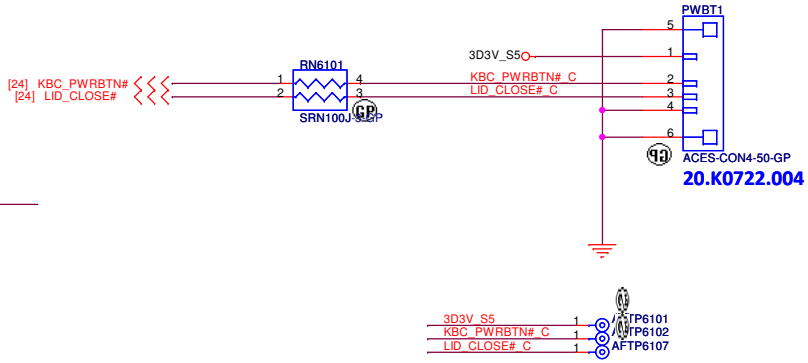
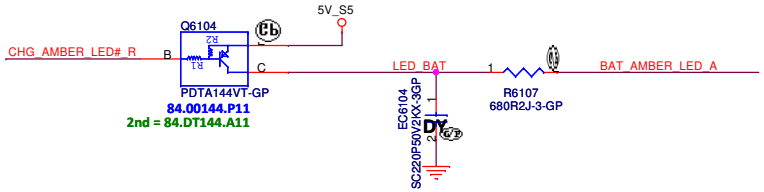
SSID = User.Interface

PWRBTN CONN



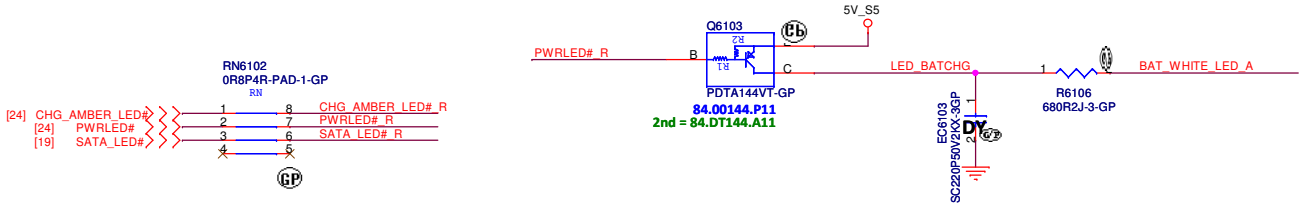
Battery LED1(Amber_LED)

LOW actived from KBC GPIO

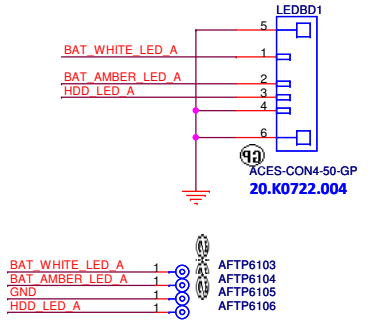


Power & Battery LED2(White_LED)

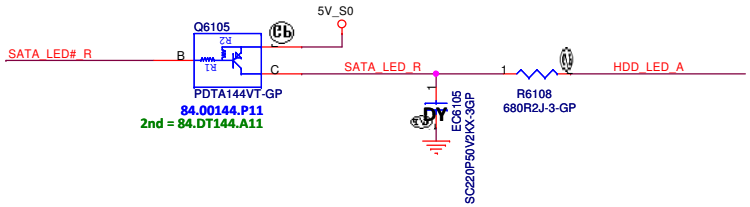
LOW actived from KBC GPIO



LED board CONN



SATA HDD LED



<Core Design>

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Title	LED Bar/Power Button	
Size A3	Document Number: Hadley 15"	Rev: X02
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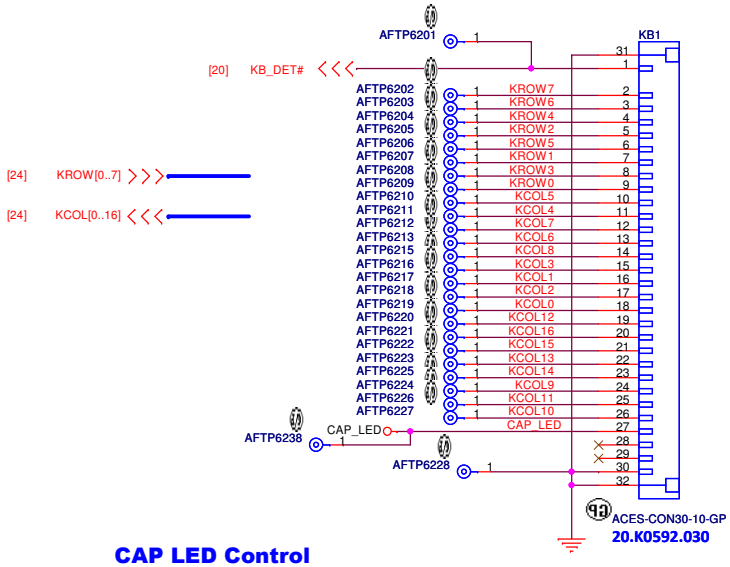
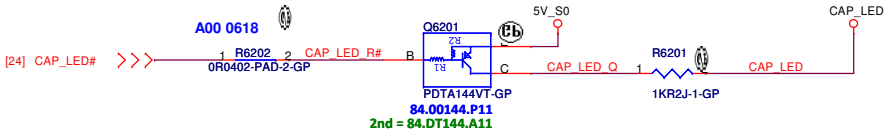
SSID = KBC

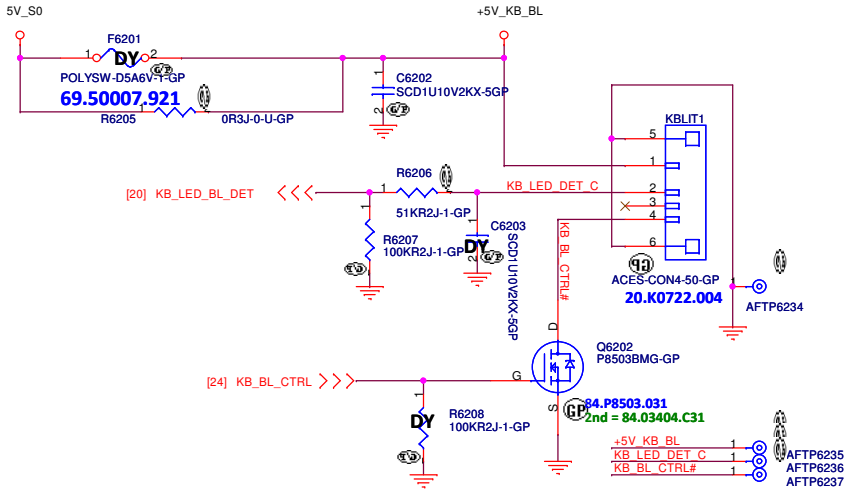
Internal Keyboard Connector



CAP LED Control

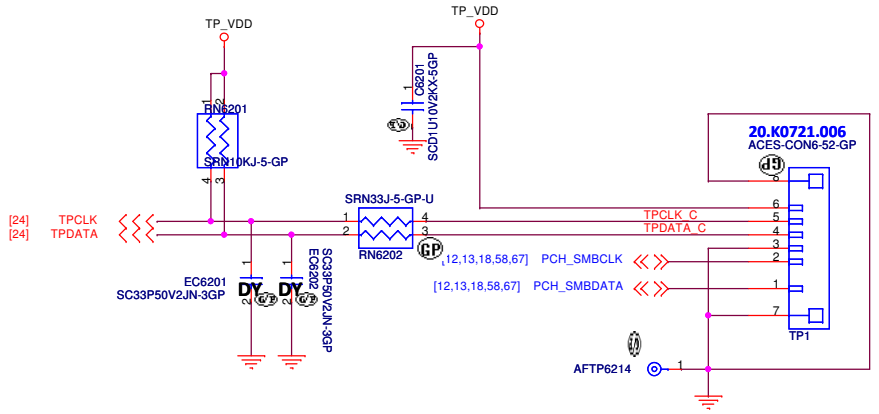
LOW actived from KBC GPIO

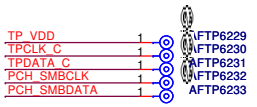




SSID = Touch.Pad

Touch Pad Connector





<Core Design>

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Title: Reserved		
Size: A3	Document Number: Hadley 15"	Rev: X02
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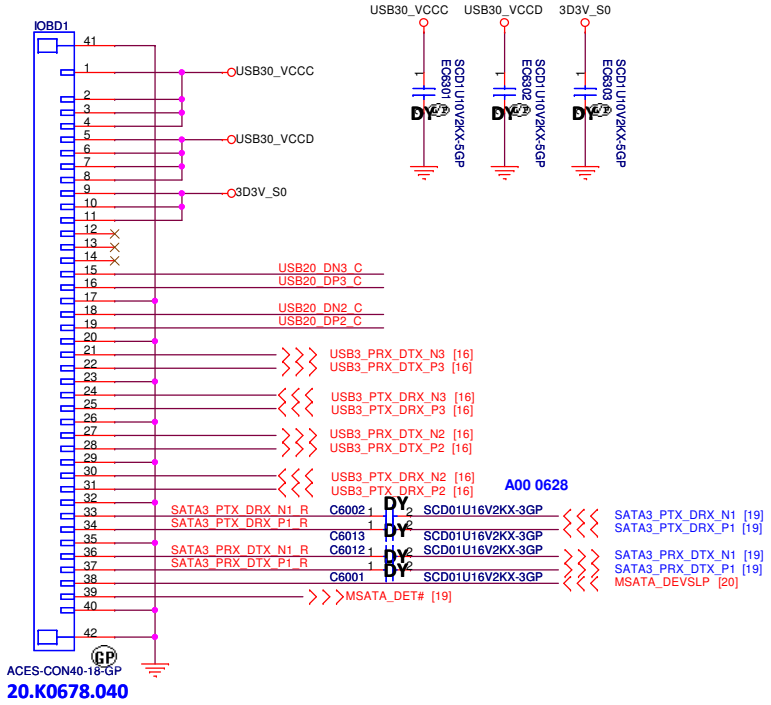
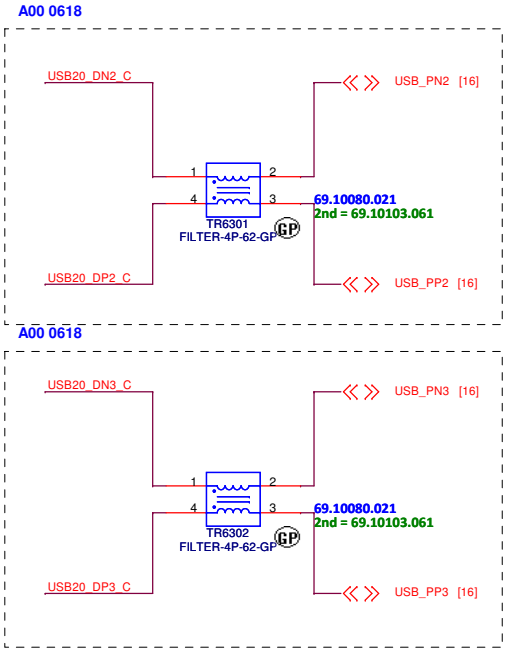
SSID = User.Interface





<Core Design>

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Title: IO Board Connector

Size	Document Number	Rev
A3	Hadley 15"	X02

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

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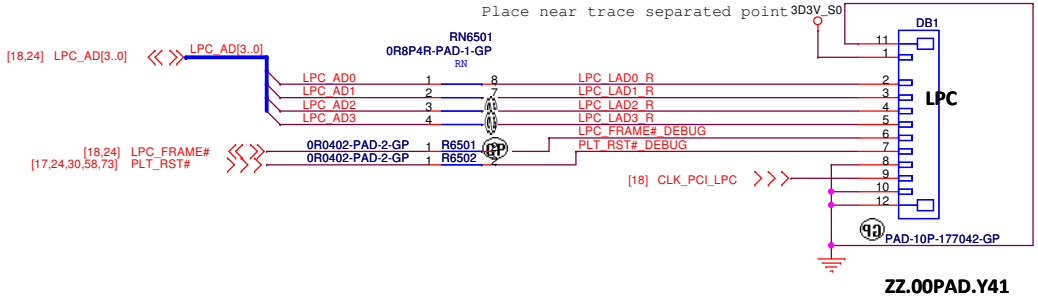
SSID = DEBUG PORT

Debug Connector

A00 0625



ZZ.00PAD.Y41

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Dubug connector*		
Size: A3	Document Number: *Hadley 15"*	Rev: *X02*
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<Core Design>

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Title
Reserved

Size	Document Number	Rev
A4	Hadley 15"	X02

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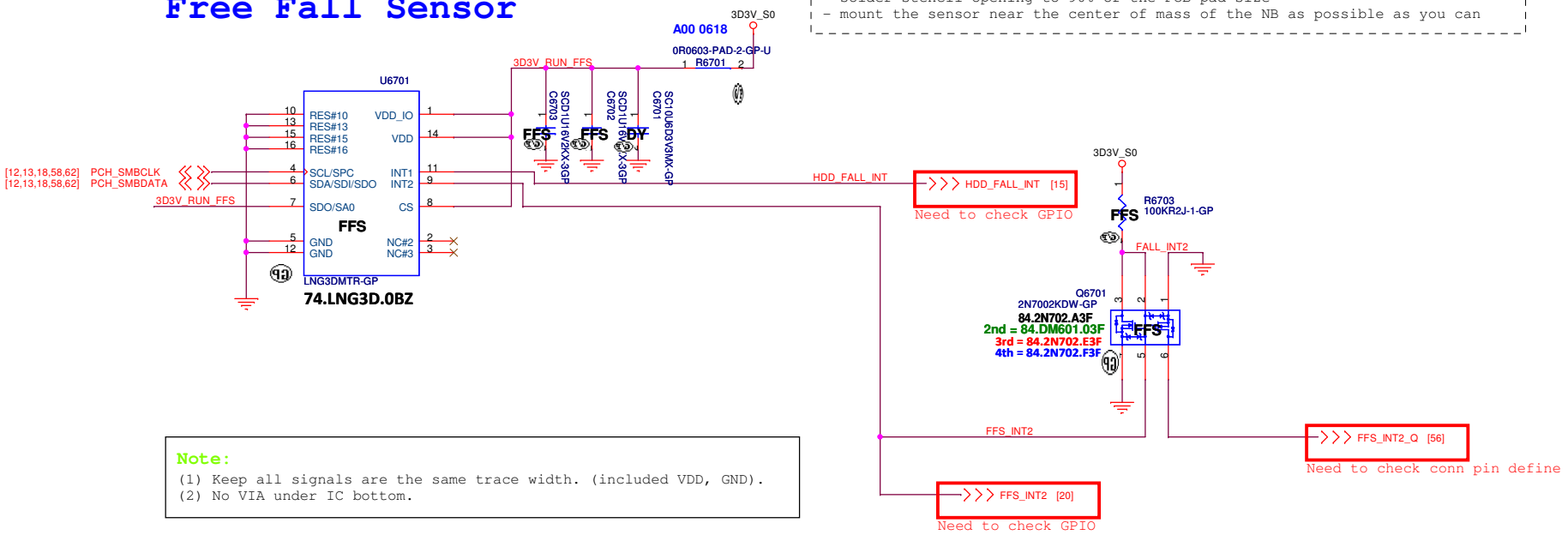
SSID = User.Interface

Free Fall Sensor



<Core Design>

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Title: FFS		
Size: A3	Document Number: Hadley 15"	Rev: X02
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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 28, 2013 | Sheet 68 of 101

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

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Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

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Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

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<Core Design>

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SSID = VIDEO

dGPU Reset

[17,24,30,58,65] PLT_RST# → D7301 1SS400GPT-GP 83.00400.C1F
2ND = 83.27101.01F
3RD = 83.01426.01F
A00 0618
0R0402-PAD-2-GP R7304 → VGA_RST# [76]

[15] DGPU_HOLD_RST#

3D3V_VGA_S0

Q7301 2N7002K-2-GP 84.2N702.J31
[18] PEG_CLKREQ# → R7308 10KR2J-3-GP → VGA_RST#
R7305 0R2J-2-GP → GPU_CLKREQ#

GPU1A 1 OF 17
1/17 PCI_EXPRESS

GK107/GF108 GK208/GF117
NC

PEX_WAKE# AJ11
PEX_RST# AJ12
PEX_CLKREQ# AK12
PEX_REFCLK AL13 ← [18] CLK_PCIE_VGA
PEX_REFCLK# AK13 ← [18] CLK_PCIE_VGA#

[16] CPU_RXP_C_dGPU_TXP0	C7301 SCD22U10V2KX-1GP	dGPU_TXP_CPU_RXP0
[16] CPU_RXN_C_dGPU_TXN0	C7302 SCD22U10V2KX-1GP	dGPU_TXN_CPU_RXN0
[16] CPU_RXP_C_dGPU_TXP1	C7303 SCD22U10V2KX-1GP	dGPU_TXP_CPU_RXP1
[16] CPU_RXN_C_dGPU_TXN1	C7304 SCD22U10V2KX-1GP	dGPU_TXN_CPU_RXN1
[16] CPU_RXP_C_dGPU_TXP2	C7305 SCD22U10V2KX-1GP	dGPU_TXP_CPU_RXP2
[16] CPU_RXN_C_dGPU_TXN2	C7306 SCD22U10V2KX-1GP	dGPU_TXN_CPU_RXN2
[16] CPU_RXP_C_dGPU_TXP3	C7307 SCD22U10V2KX-1GP	dGPU_TXP_CPU_RXP3
[16] CPU_RXN_C_dGPU_TXN3	C7308 SCD22U10V2KX-1GP	dGPU_TXN_CPU_RXN3

[16] dGPU_RXP_C_CPU_TXP0	PEX_TX0 AK14 / PEX_TX0# AJ14
[16] dGPU_RXN_C_CPU_TXN0	PEX_RX0 AN12 / PEX_RX0# AM12
[16] dGPU_RXP_C_CPU_TXP1	PEX_TX1 AH14 / PEX_TX1# AG14
[16] dGPU_RXN_C_CPU_TXN1	PEX_RX1 AN14 / PEX_RX1# AM14
[16] dGPU_RXP_C_CPU_TXP2	PEX_TX2 AK15 / PEX_TX2# AJ15
[16] dGPU_RXN_C_CPU_TXN2	PEX_RX2 AP14 / PEX_RX2# AP15
[16] dGPU_RXP_C_CPU_TXP3	PEX_TX3 AL16 / PEX_TX3# AK16
[16] dGPU_RXN_C_CPU_TXN3	PEX_RX3 AN15 / PEX_RX3# AM15

PEX_TX4 AK17 / PEX_TX4# AJ17
PEX_RX4 AN17 / PEX_RX4# AM17
PEX_TX5 AH17 / PEX_TX5# AG17
PEX_RX5 AP17 / PEX_RX5# AP18
PEX_TX6 AK18 / PEX_TX6# AJ18
PEX_RX6 AN18 / PEX_RX6# AM18
PEX_TX7 AL19 / PEX_TX7# AK19
PEX_RX7 AN20 / PEX_RX7# AM20
PEX_TX8 AK20 / PEX_TX8# AJ20
PEX_RX8 AP20 / PEX_RX8# AP21
PEX_TX9 AH20 / PEX_TX9# AG20
PEX_RX9 AN21 / PEX_RX9# AM21
PEX_TX10 AK21 / PEX_TX10# AJ21
PEX_RX10 AN23 / PEX_RX10# AM23
PEX_TX11 AL22 / PEX_TX11# AK22
PEX_RX11 AP23 / PEX_RX11# AP24
PEX_TX12 AK23 / PEX_TX12# AJ23
PEX_RX12 AN24 / PEX_RX12# AM24
PEX_TX13 AH23 / PEX_TX13# AG23
PEX_RX13 AN26 / PEX_RX13# AM26
PEX_TX14 AK24 / PEX_TX14# AJ24
PEX_RX14 AP26 / PEX_RX14# AP27
PEX_TX15 AL25 / PEX_TX15# AK25
PEX_RX15 AN27 / PEX_RX15# AM27

PEX LANES 8 TO 15 NC FOR GF117/GK208

GF108	GK208/GK107/GF117
NC	PEX_PLL_HVDD AH12
	PEX_SVDD_3V3 AG12

PEX_IOVDD_1 AG19
PEX_IOVDD_2 AG21
PEX_IOVDD_3 AG22
PEX_IOVDD_4 AG24
PEX_IOVDD_5 AH21
PEX_IOVDD_6 AH25

1D05V_VGA_S0
C7323 SC10U6D3V3MX-GP
C7310 SC10U6D3V3MX-GP
C7322 SC10U6D3V3MX-GP
C7312 SC1U6D3V2KX-GP
C7313 SC1U6D3V2KX-GP
C7325 SC10U6D3V3MX-GP
C7326 SC10U6D3V3MX-GP

1.05V +/- 30mV
3.3A

PEX_IOVDDQ_1 AG13
PEX_IOVDDQ_2 AG15
PEX_IOVDDQ_3 AG16
PEX_IOVDDQ_4 AG18
PEX_IOVDDQ_5 AG25
PEX_IOVDDQ_6 AH15
PEX_IOVDDQ_7 AH18
PEX_IOVDDQ_8 AH26
PEX_IOVDDQ_9 AH27
PEX_IOVDDQ_10 AJ27
PEX_IOVDDQ_11 AK27
PEX_IOVDDQ_12 AL27
PEX_IOVDDQ_13 AM28
PEX_IOVDDQ_14 AN28

1D05V_VGA_S0
C7320 SC10U6D3V3MX-GP
C7321 SC10U6D3V3MX-GP
C7309 SC4D7U6D3V3KX-GP
C7311 SC1U6D3V2KX-GP
C7314 SC1U6D3V2KX-GP
C7327 SC10U6D3V3MX-GP
C7328 SC4D7U6D3V3KX-GP

3.3V +/- 5%
210mA

3D3V_VGA_S0
C7316 SC1U10V2KX-5GP
C7315 SC4D7U6D3V3KX-GP
C7324 SC4D7U6D3V3KX-GP

X7R, Under GPU.

POWER IC

VDD_SENSE L4 → VGA_SENSE [82]
GND_SENSE L5 → GND_SENSE [82]
NC_3V3AUX P8

R7303 200R2F-L-GP
PEX_TSTCLK_OUT AJ26 PEXTSTCLK_OUT
PEX_TSTCLK_OUT# AK26 PEXTSTCLK_OUT#

1.05V +/- 30mV
150mA

1D05V_VGA_S0
PEX_PLLVDD AG26
C7318 SC1U10V2KX-5GP
C7317 SC4D7U6D3V3KX-GP
C7319 SC1U6D3V2KX-GP

0102 remove R7307

TESTMODE AK11 TESTMODE ← R7302 10KR2J-3-GP
PEX_TERMP AP29 PEX_TERMP ← R7301 2K49R2F-GP

OPS

N14P-GS-A1-GP
71.0N14P.00U

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)
Size: Custom | Document Number: Hadley 15" | Rev: X02
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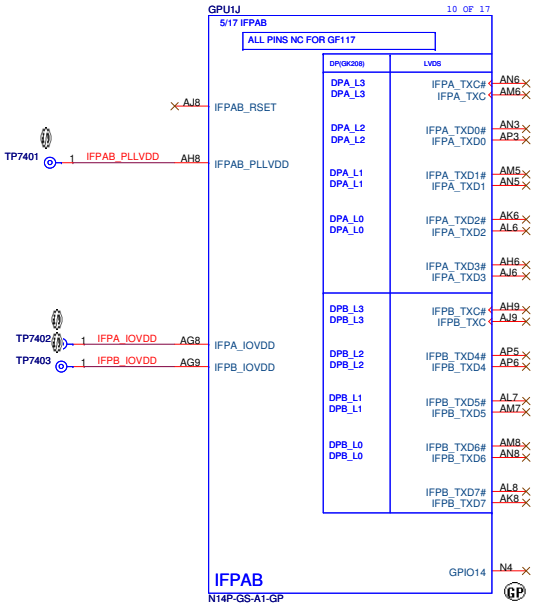
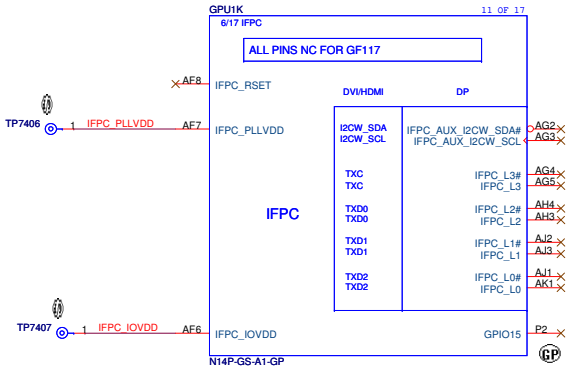
SSID = VIDEO



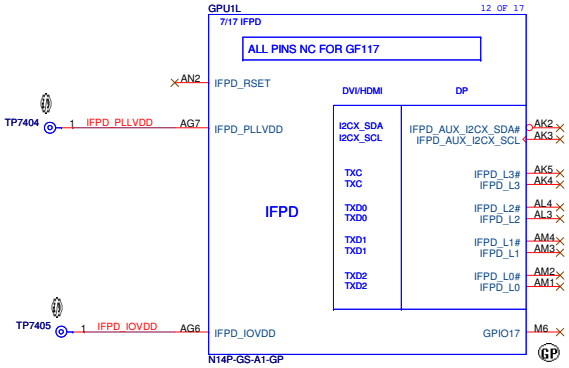
71.0N14P.00U

OPS



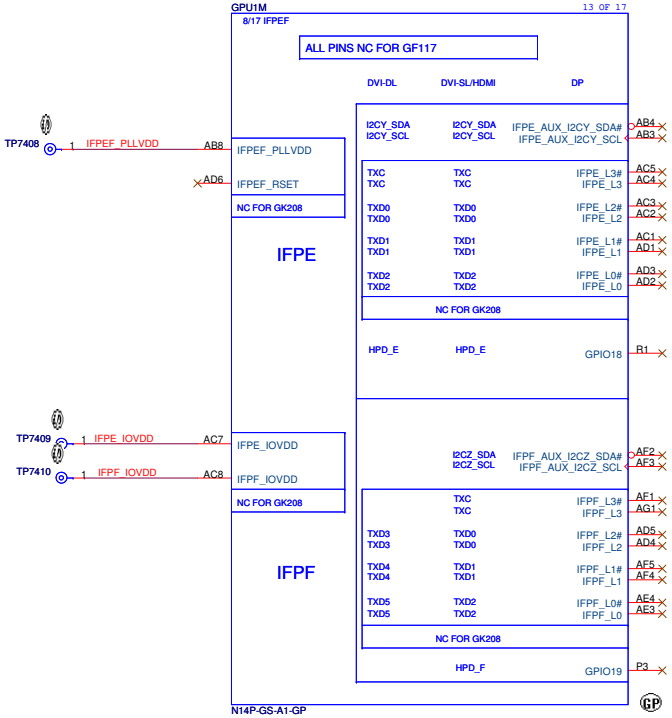
71.0N14P.00U

OPS



71.0N14P.00U

OPS



71.0N14P.00U

OPS

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU Memory(2/5)**

Size	Document Number	Rev
Custom	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 74 of 101

SSID = VIDEO

A00 0618

0102 remove L7502
change K27 pin net name

Layout note:FBA_PLL_AVDD=16mil
Place close to Ball

DA-05691-001_V05 P7

Place under GPU near

0102 remove L7503
change C7506 to 0603 package

1.35V +/- 3%
4.88A

GPU FBVDDQ Decoupling
PLACE CLOSE TO GPU BALLS

PLACE CLOSE TO GPU BALLS

THE FBA_WCKBxx PINS ARE USED ONLY ON GK107 THEY ARE NC FOR GK208/GF108 /GF117

THE FBB_WCKBxx PINS ARE USED ONLY ON GK107 THEY ARE NC FOR GF108

ALL PINS NC FOR GF117/GK208

NC	FBB_PLL_AVDD
GF108	GK107

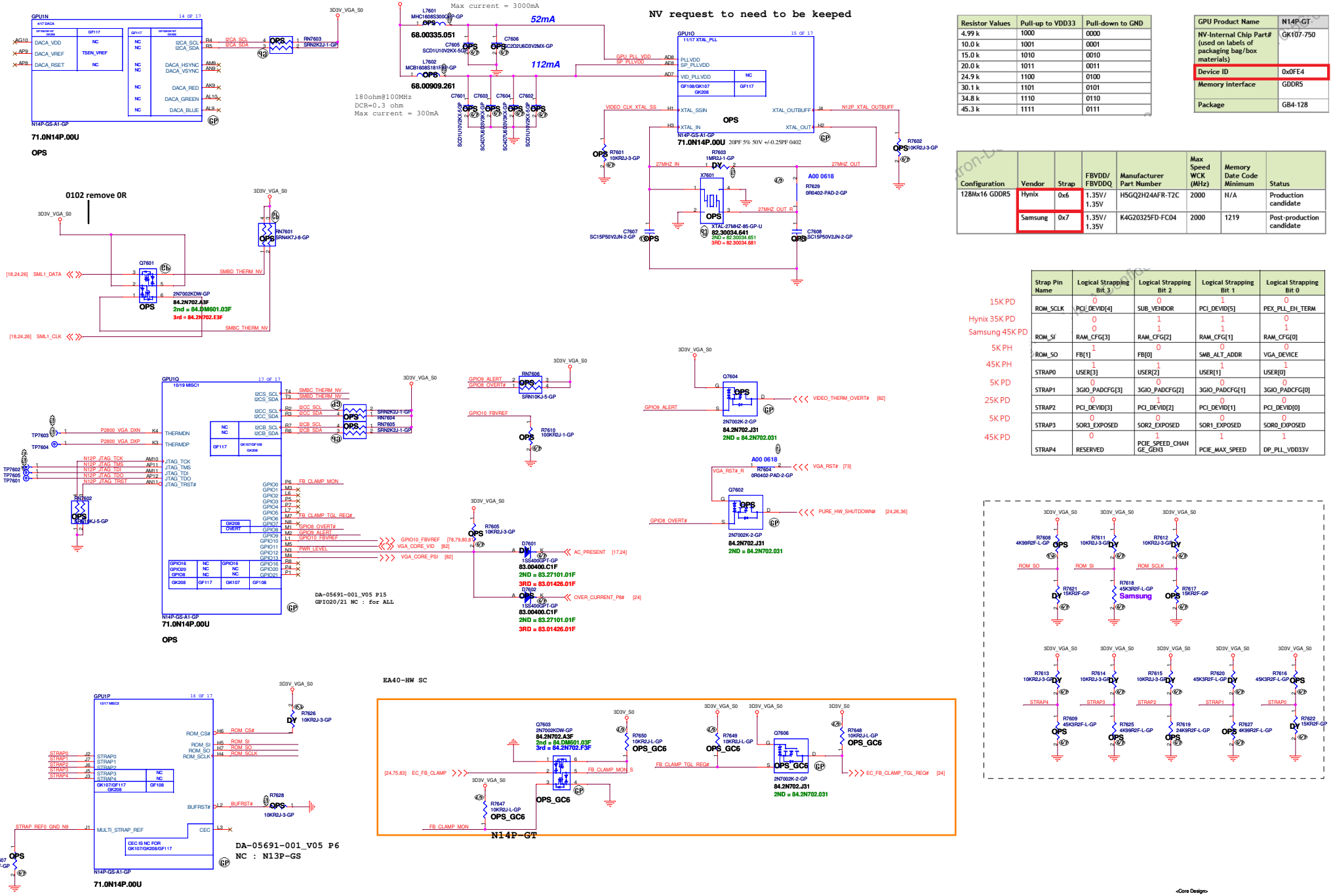
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 75 of 101

SSID = VIDEO



Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

GPU Product Name	N14P-GT
NV-Internal Chip Part# (used on labels of packaging bag/box materials)	GK107-750
Device ID	0x0FE4
Memory interface	GDDR5
Package	GB4-128

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x6	1.35V/ 1.35V	H5GQ2H24AFR-T2C	2000	N/A	Production candidate
	Samsung	0x7	1.35V/ 1.35V	K4G20325FD-FC04	2000	1219	Post-production candidate

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

15K PD
Hynix 35K PD
Samsung 45K PD
5K PH
45K PH
5K PD
25K PD
5K PD
45K PD

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**

Size: Custom | Document Number: **Hadley 15"** | Rev: **X02**

Date: Friday, June 28, 2013 | Sheet 76 of 101

SSID = VIDEO

VGA_CORE

Under GPU

N14P-GT : 45A

C7709 C7707 C7708 C7706 C7702 C7701 — OPS — SC4D7U6D3V3KX-GP

C7725 C7722 C7723 C7724 C7721 C7720 C7719 — OPS — SC4D7U6D3V3KX-GP / SC10U6D3V3MX-GP

C7716 C7715 C7718 C7717 C7714 C7713 C7712 C7711 — OPS — SC1U6D3V2KX-GP / SCD1U10V2KX-GP

NEAR TO GPU

C7703 C7705 C7710 — OPS — SC10U6D3V3MX-GP / SC10U6D3V3KX-GP

R7701 — UMA — 0R3J-0-GP

GPU1H 8 OF 17

13/17 NVDD

AA12	VDD_1	VDD_73	N20
AA14	VDD_2	VDD_74	N22
AA16	VDD_3	VDD_75	P12
AA19	VDD_4	VDD_76	P14
AA21	VDD_5	VDD_77	P16
AA23	VDD_6	VDD_78	P19
AB13	VDD_7	VDD_79	P21
AB15	VDD_8	VDD_80	P23
AB17	VDD_9	VDD_81	R13
AB18	VDD_10	VDD_82	R15
AB20	VDD_11	VDD_83	R17
AB22	VDD_12	VDD_84	R18
AC12	VDD_13	VDD_85	R20
AC14	VDD_14	VDD_86	R22
AC16	VDD_15	VDD_87	T12
AC19	VDD_16	VDD_88	T14
AC21	VDD_17	VDD_89	T16
AC23	VDD_18	VDD_90	T19
M12	VDD_19	VDD_91	T21
M14	VDD_20	VDD_92	T23
M16	VDD_21	VDD_93	U13
M19	VDD_22	VDD_94	U15
M21	VDD_23	VDD_95	U17
M23	VDD_24	VDD_96	U18
N13	VDD_25	VDD_97	U20
N15	VDD_26	VDD_98	U22
N17	VDD_27	VDD_99	V13
N18	VDD_28	GND_100	V15

N14P-GS-A1-GP

71.0N14P.00U

OPS

GPU1F 6 OF 17

15/17 GND_1/2

A2	GND_1	GND_71	AM25
AA17	GND_5	GND_72	AN1
AA18	GND_6	GND_73	AN10
AA20	GND_7	GND_74	AN13
AA22	GND_8	GND_75	AN16
AB12	GND_9	GND_76	AN19
AB14	GND_10	GND_77	AN22
AB16	GND_11	GND_78	AN25
AB19	GND_12	GND_79	AN30
AB2	GND_13	GND_80	AN34
AB21	GND_14	GND_81	AN4
A33	GND_2	GND_82	AN7
AB23	GND_15	GND_83	AP2
AB28	GND_16	GND_84	AP33
AB30	GND_17	GND_85	B1
AB32	GND_18	GND_86	B10
AB5	GND_19	GND_87	B22
AB7	GND_20	GND_88	B26
AC13	GND_21	GND_89	B28
AC15	GND_22	GND_90	B31
AC17	GND_23	GND_91	B34
AC18	GND_24	GND_92	B4
AA13	GND_3	GND_93	B7
AC20	GND_25	GND_94	C10
AC22	GND_26	GND_95	C13
AE2	GND_27	GND_96	C19
AE28	GND_28	GND_97	C22
AE30	GND_29	GND_98	C25
AE32	GND_30	GND_99	C28
AE33	GND_31	GND_100	C7
AE5	GND_32	GND_101	D2
AE7	GND_33	GND_102	D31
AH10	GND_34	GND_103	D33
AA15	GND_4	GND_104	E10
AH13	GND_35	GND_105	E22
AH16	GND_36	GND_106	E25
AH19	GND_37	GND_107	E5
AH2	GND_38	GND_108	E7
AH22	GND_39	GND_109	F28
AH24	GND_40	GND_110	E7
AH28	GND_41	GND_111	G10
AH29	GND_42	GND_112	G13
AH30	GND_43	GND_113	G16
AH32	GND_44	GND_114	G19
AH33	GND_45	GND_115	G2
AH5	GND_46	GND_116	G22
AH7	GND_47	GND_117	G25
AJ7	GND_48	GND_118	G28
AK10	GND_49	GND_119	G3
AK7	GND_50	GND_120	G30
AL12	GND_51	GND_121	G32
AL14	GND_52	GND_122	G33
AL15	GND_53	GND_123	G5
AL17	GND_54	GND_124	G7
AL18	GND_55	GND_125	K2
AL2	GND_56	GND_126	K28
AL20	GND_57	GND_127	K30
AL21	GND_58	GND_128	K32
AL23	GND_59	GND_129	K33
AL24	GND_60	GND_130	K5
AL26	GND_61	GND_131	K7
AL28	GND_62	GND_132	M13
AL30	GND_63	GND_133	M15
AL32	GND_64	GND_134	M17
AL33	GND_65	GND_135	M18
AL5	GND_66	GND_136	M20
AM13	GND_67	GND_137	M22
AM16	GND_68	GND_138	N12
AM19	GND_69	GND_139	N14
AM22	GND_70	GND_140	N16

N14P-GS-A1-GP

71.0N14P.00U

OPS

GPU1G 7 OF 17

16/17 GND_2/2

N19	GND_141	GND_170	T28
N2	GND_142	GND_171	T32
N21	GND_143	GND_172	T5
N23	GND_144	GND_173	T7
N28	GND_145	GND_174	U12
N30	GND_146	GND_175	U14
N32	GND_147	GND_176	U16
N33	GND_148	GND_177	U19
N5	GND_149	GND_178	U21
N7	GND_150	GND_179	U23
P13	GND_151	GND_180	V12
P15	GND_152	GND_181	V14
P17	GND_153	GND_182	V16
P18	GND_154	GND_183	V19
P20	GND_155	GND_184	V21
P22	GND_156	GND_185	V23
R12	GND_157	GND_186	W13
R14	GND_158	GND_187	W15
R16	GND_159	GND_188	W17
R19	GND_160	GND_189	W18
R21	GND_161	GND_190	W20
R23	GND_162	GND_191	W22
T13	GND_163	GND_192	W28
T15	GND_164	GND_193	Y12
T17	GND_165	GND_194	Y14
T18	GND_166	GND_195	Y16
T2	GND_167	GND_196	Y19
T20	GND_168	GND_197	Y21
T22	GND_169	GND_198	Y23
AG11	GND_F	GND_H	AH11
	GND_OPT_1		C16
	GND_OPT_2		W32

Optional CMD GNDs (2)
NC for 4-Lyr cards

N14P-GS-A1-GP

71.0N14P.00U

OPS

GPU1I 9 OF 17

9/17 XVDD

CONFIGURABLE POWER CHANNELS

XVDD_1	U1	XVDD_23	Y1
XVDD_2	U2	XVDD_24	Y2
XVDD_3	U3	XVDD_25	Y3
XVDD_4	U4	XVDD_26	Y4
XVDD_5	U5	XVDD_27	Y5
XVDD_6	U6	XVDD_28	Y6
XVDD_7	U7	XVDD_29	Y7
XVDD_8	U8	XVDD_30	Y8
XVDD_9	V1	XVDD_31	AA1
XVDD_10	V2	XVDD_32	AA2
XVDD_11	V3	XVDD_33	AA3
XVDD_12	V4	XVDD_34	AA4
XVDD_13	V5	XVDD_35	AA5
XVDD_14	V6	XVDD_36	AA6
XVDD_15	V7	XVDD_37	AA7
XVDD_16	V8	XVDD_38	AA8
XVDD_17	W2		
XVDD_18	W3		
XVDD_19	W4		
XVDD_20	W5		
XVDD_21	W7		
XVDD_22	W8		

N14P-GS-A1-GP

71.0N14P.00U

OPS

GPU1E 5 OF 17

17/17 NC/VDD33

DA-05691-001_V05 P20
3V3MISC : N13P-GS

GK107	GK208 GF117
3V3MISC	3V3MISC_1
3V3MISC	3V3MISC_2
	VDD33_1
	VDD33_2

AJ28	NC#AJ28	J8	
C15	NC#C15	K8	
D19	NC#D19		
D20	NC#D20	L8	
D23	NC#D23	M8	
D26	NC#D26		
H31	NC#H31		
V32	NC#V32		
AC6	DNU#AC6	DO NOT CONNECT THESE PINS	
AJ4	DNU#AJ4		
AJ5	DNU#AJ5		
AL11	DNU#AL11		
T8	DNU#T8		

N14P-GS-A1-GP

71.0N14P.00U

OPS

3.3V +/- 5%
85mA

3D3V_VGA_S0

C7704 C7729 C7727 C7728 — OPS — SC1U6D3V2KX-GP / SCD1U10V2KX-5GP / SCD1U10V2KX-5GP / SC1U6D3V2KX-GP

X7R X7R

0.1U Under GPU

4.7U NEAR TO GPU

1U NEAR TO GPU

<Core Design>

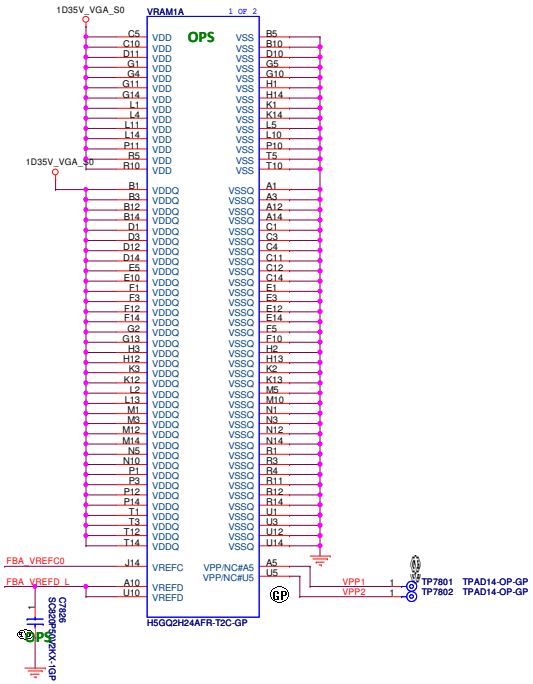
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU_POWER(4/5)**

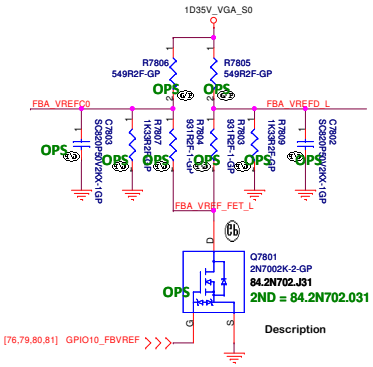
Size: Custom | Document Number: **Hadley 15"** | Rev: **X02**

Date: Friday, June 28, 2013 | Sheet 77 of 101

SSID = VIDEO

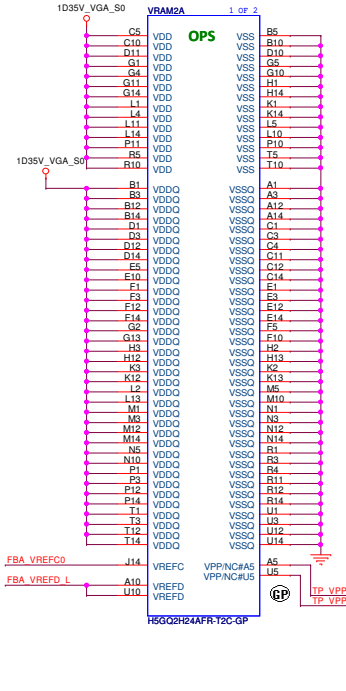


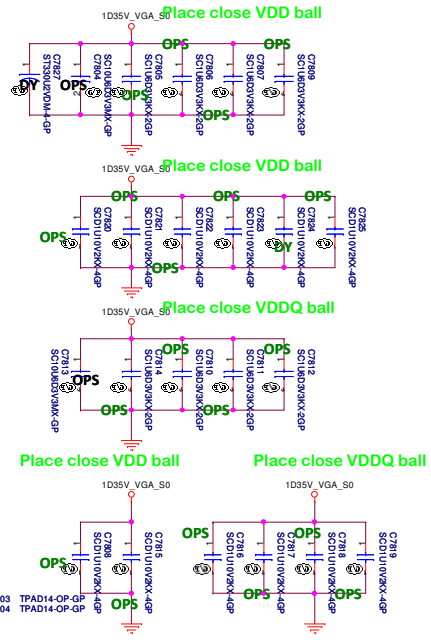
Frame Buffer Patition A-Lower Half

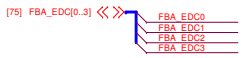


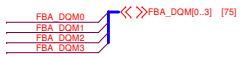
FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low









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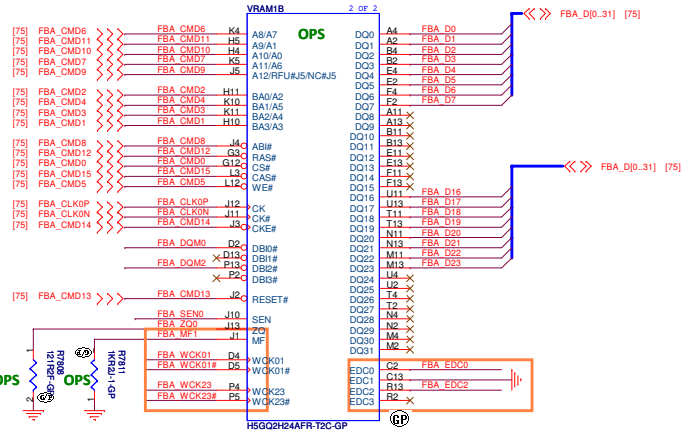
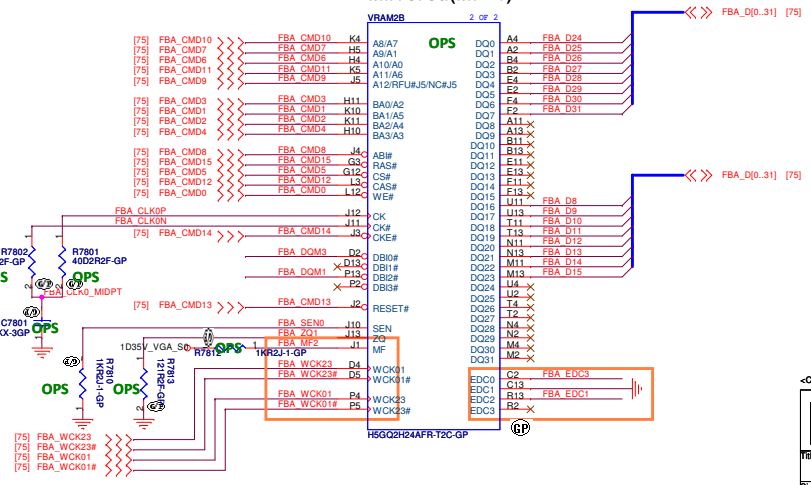


Mirrored(MF=1)



<Core Design>

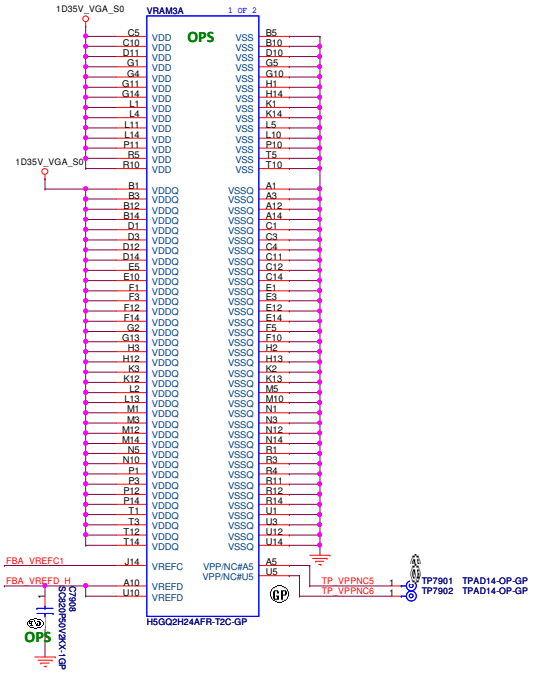
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

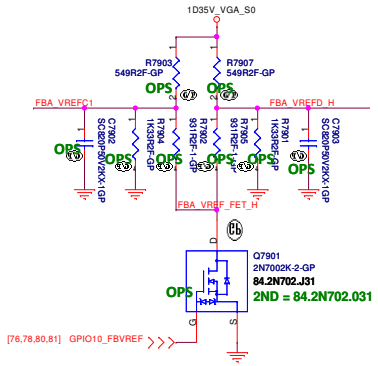
Size	Document Number	Rev
Custom	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 78 of 101

SSID = VIDEO

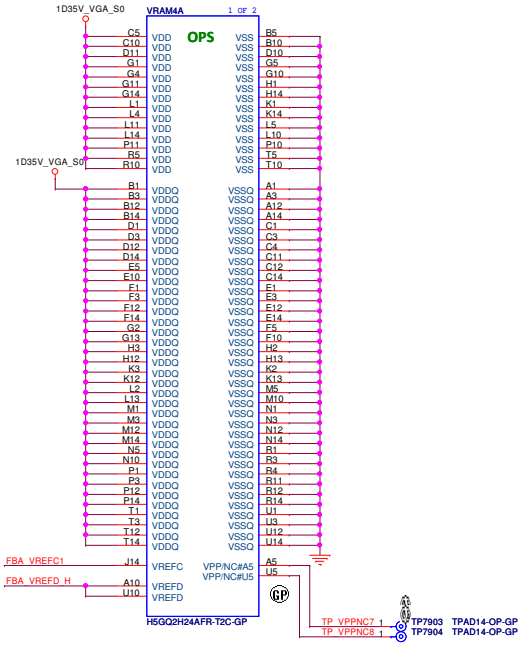


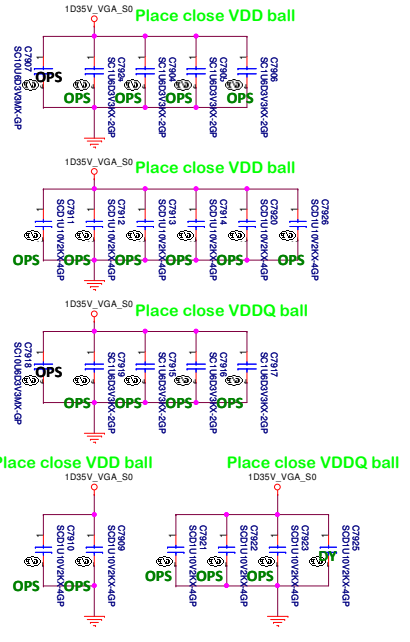
Frame Buffer Patition A-Upper Half

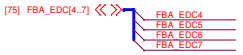


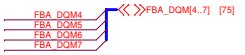
FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

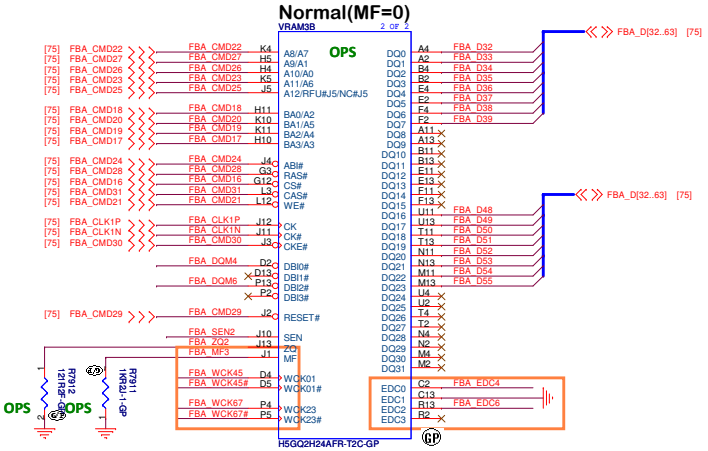




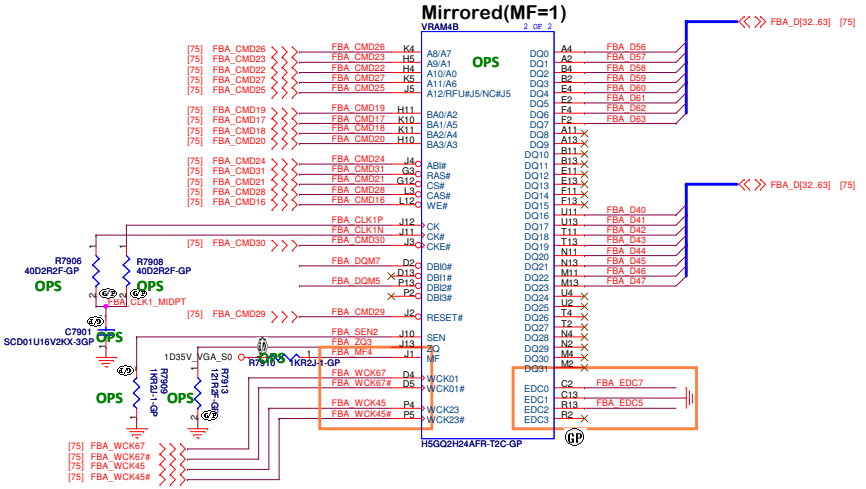




Normal(MF=0)



Mirrored(MF=1)



<Core Design>

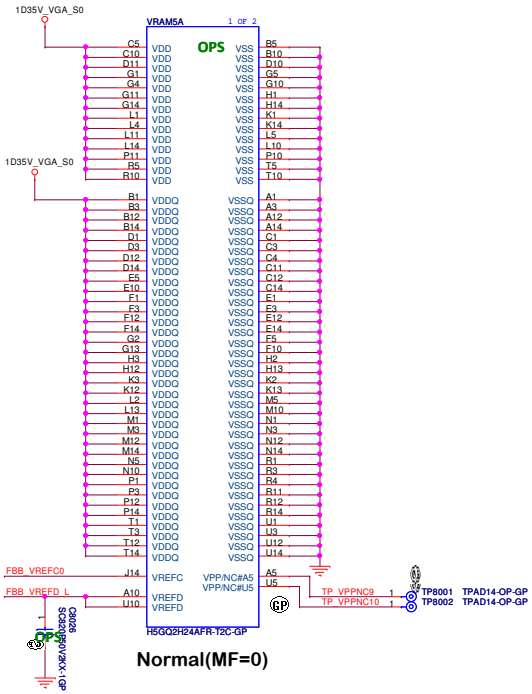
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM3,4 (2/4)*

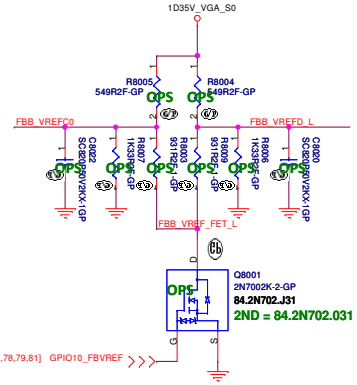
Size: Custom | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 79 of 101

SSID = VIDEO

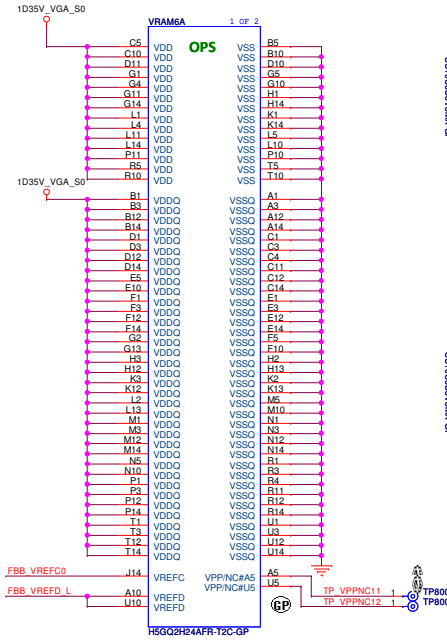


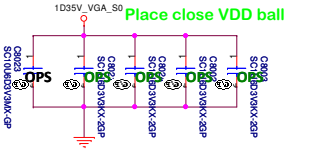
Frame Buffer Patition B-Lower Half

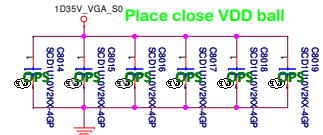


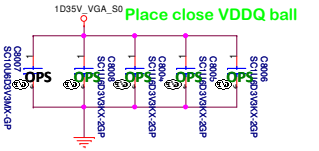
FBVREF Termination

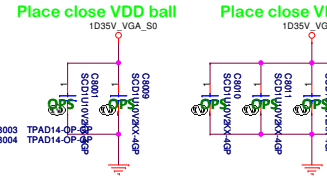
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

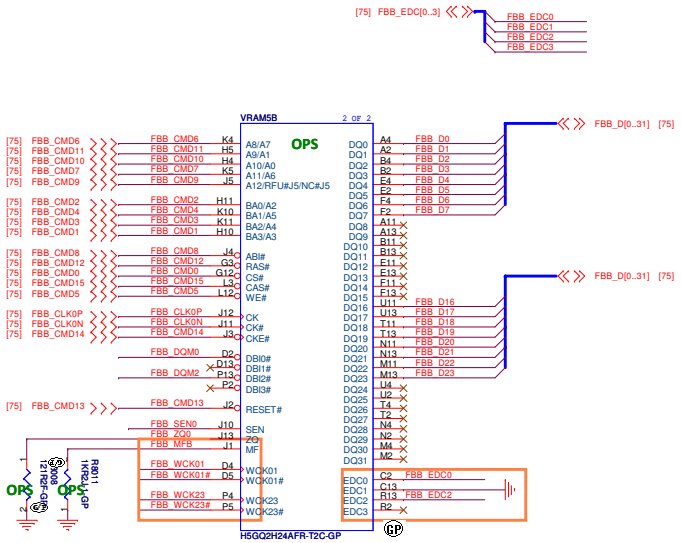


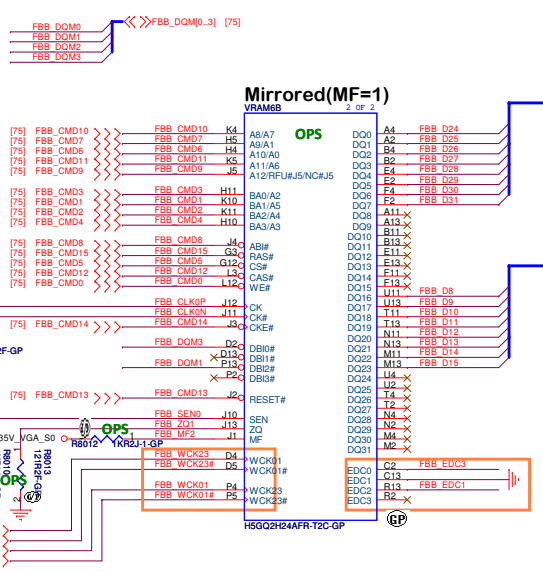












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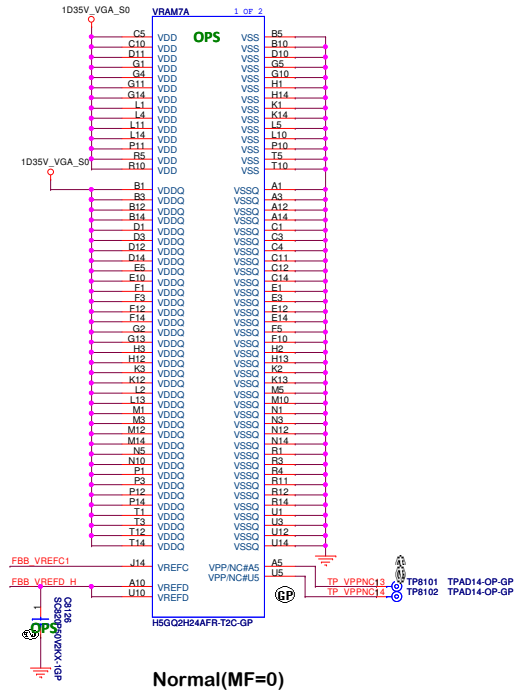
Title: GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
Custom	Hadley 15"	X02

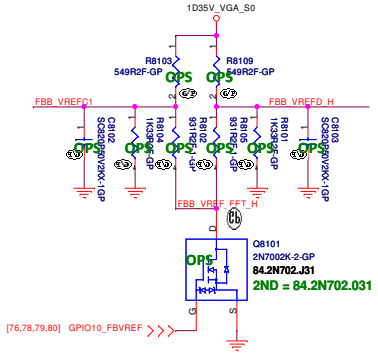
Date: Friday, June 28, 2013 Sheet 80 of 101

SSID = VIDEO



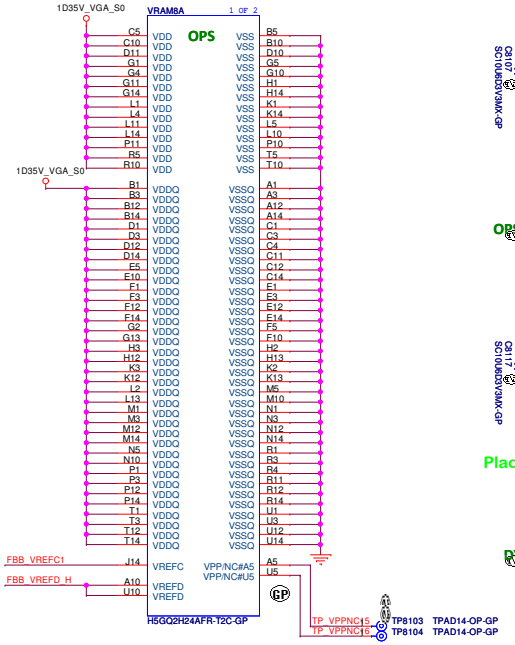
Normal(MF=0)

Frame Buffer Patition B-Upper Half

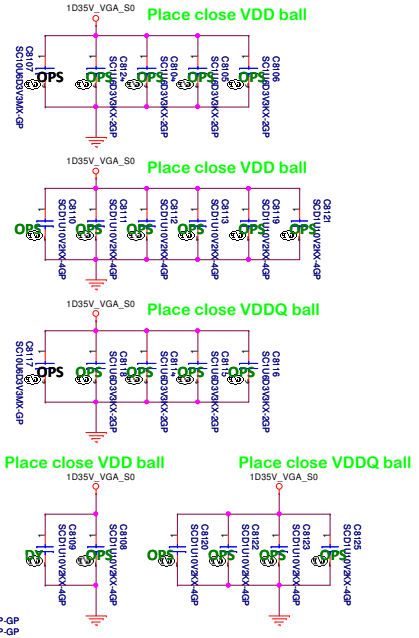


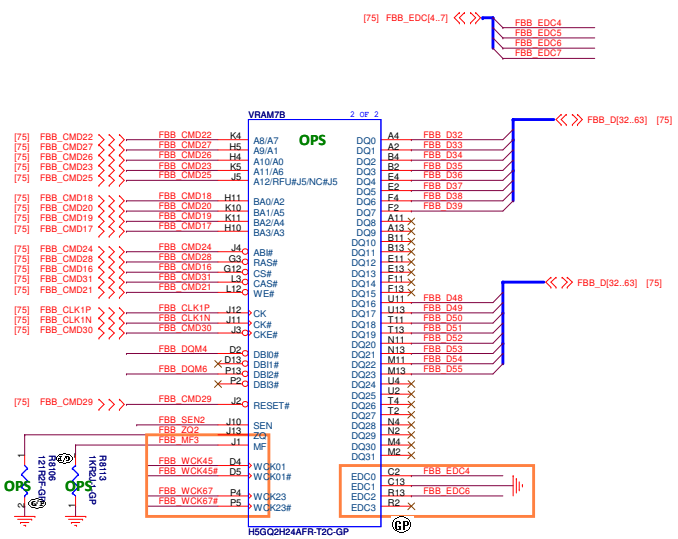
FBVREF Termination

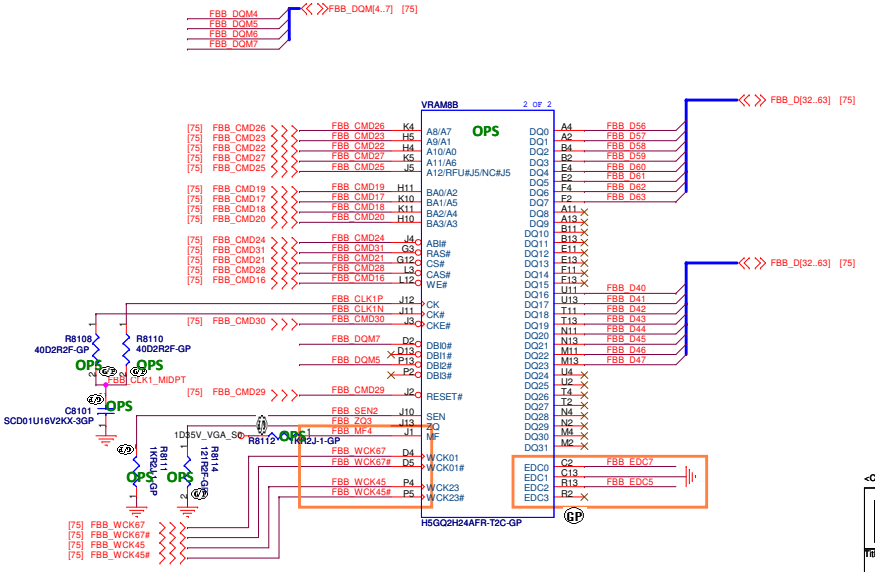
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



Mirrored(MF=1)







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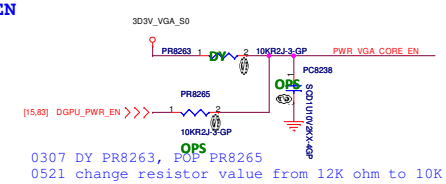
Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
Custom	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 81 of 101

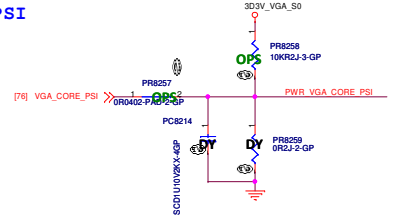
SSID = PWR.Plane.Regulator_vga_core

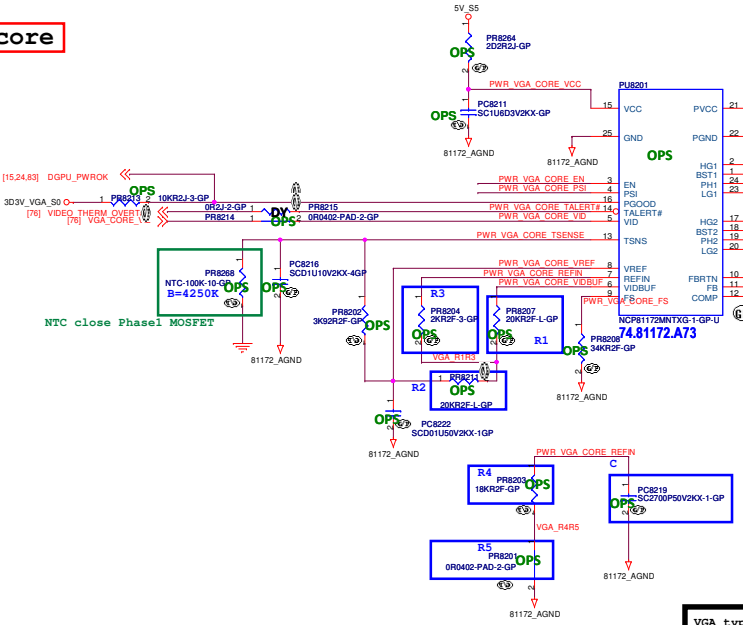
EN



0307 DY PR8263, POP PR8265
0521 change resistor value from 12K ohm to 10K

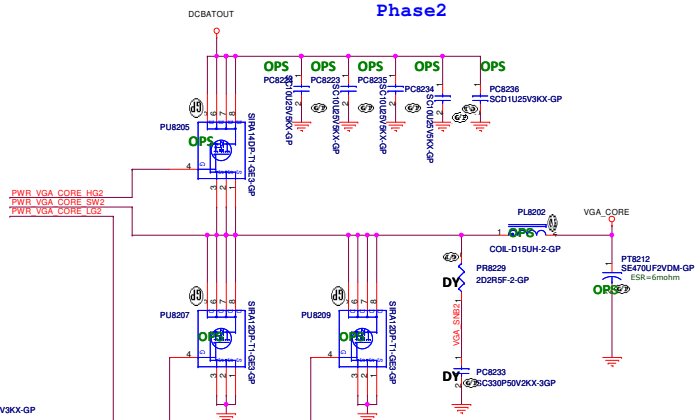
PSI



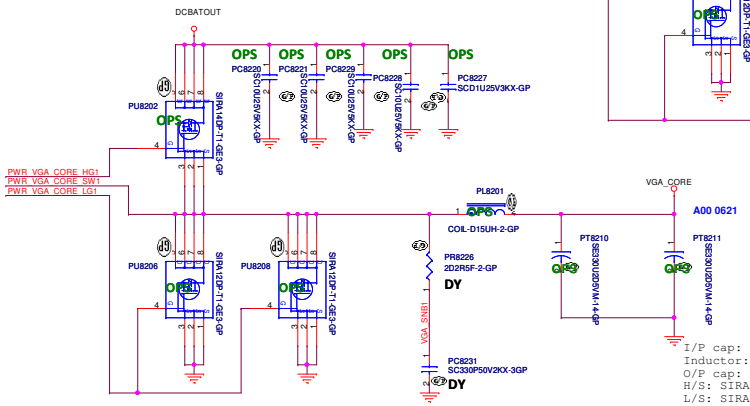


VGA type	Config	Design Current	EDP-peak	OCP	R1/PR8207	R2/PR8211	R3/PR8204	R4/PR8203	R5/PR8201	C/PC8219
N14P-LP	B	25A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GE	B	27A	40A	44A<OCP<52A	20K	20K	2K	18K	0	2.7nF
N14P-GS	B	38A	60A	66A<OCP<78A	20K	20K	2K	18K	0	2.7nF
N14P-GT	B	45A	75A	82.5A<OCP<97.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV	B	24A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV2	B	32A	55A	60.5A<OCP<71.5A	20K	20K	2K	18K	0	2.7nF
N14M-GS	B	26A	45A	49.5A<OCP<58.5A	20K	20K	2K	18K	0	2.7nF
N14M-LP	B	22A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14M-GL	C	24.33A	35.42A	38.96A<OCP<46.04A	39K	30K	3K	24K	3K	1.8nF
N14M-GE	C	35A	40.89A	44.98A<OCP<53.16A	39K	30K	3K	24K	3K	1.8nF
N14E-GTX	A	95A	125A	137.5A<OCP<162.5A	39K	39K	1.5K	30K	1.5K	1.5nF
N14E-GS	B	65.16A	87.87A	96.66A<OCP<114.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE-B	B	65.37A	98.6A	108.5A<OCP<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE	B	65.37A	98.6A	108.5A<OCP<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GL	B	46.35A	71.83A	79.01A<OCP<93.98A	20K	20K	2K	18K	0	2.7nF

Phase2



Phase1



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 0.22UH M PCMC063T-R22MN/ 2.8mohm/ Isat =40A rms /68.R22ND.10V
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm@4.5Vgs/ 84.A14DP.037
L/S: SIRA12DP-T1-GE3 / 4.4mohm/6mOhm@4.5Vgs/ 84.SRA12.037

Table 1. PWM-VID Spec and Component Values

PWM-VID Spec		Config A	Config B	Config C
Vmin	V	0.6	0.6	0.65
Vmax	V	1.2	1.2	1.15
Vboot	V	0.875	0.9	0.9
Voltage Step Vstep	mV	6.25	6.25	25
Number of Voltage Levels N	level	96	96	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74
VID Transient Time T	us	<100	<100	<100
Component Value				
R1 (1%)	KΩ	39	20	39
R2 (1%)	KΩ	39	20	30
R3 (1%)	KΩ	1.5	2	3
R4 (1%)	KΩ	30	18	24
R5 (1%)	KΩ	1.5	0	3
C	nF	1.5	2.7	1.8

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Title: NCP81172_VGA_CORE

Size: A2 | Document Number: Hadley 15" | Rev: X02

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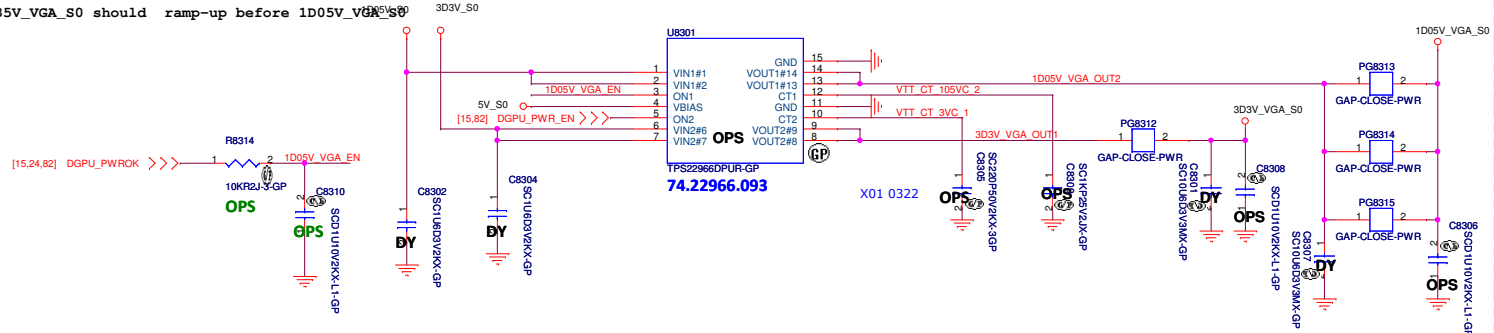
SSID = PWR.Plane.Regulator_3p3v_vga, 1p35v_vga, 1p05v_vga

3D3V_VGA_S0

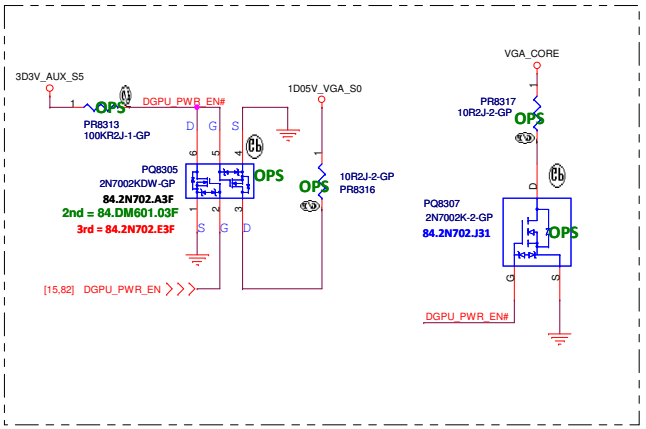
1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0

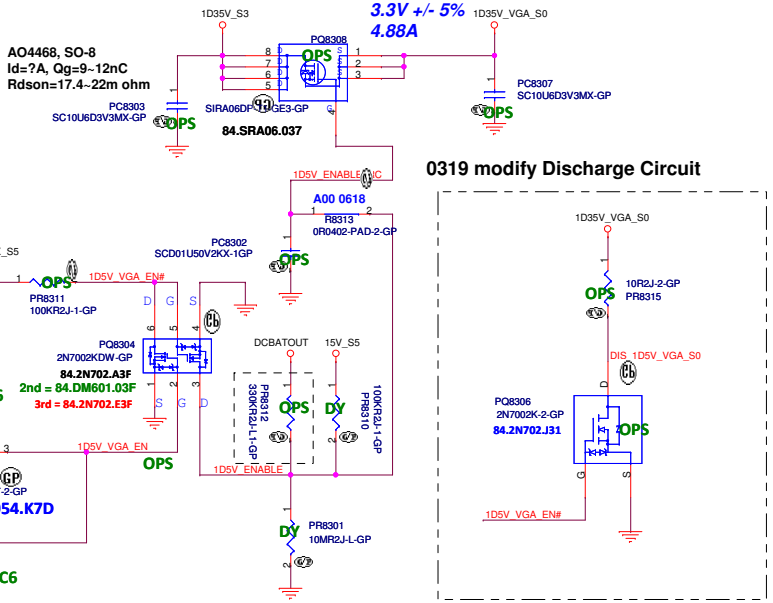
3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0



0307 Add Discharge Circuit



1D35V_VGA_S0



0319 modify Discharge Circuit

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Title: DISCRETE VGA POWER

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SSID = User.Interface

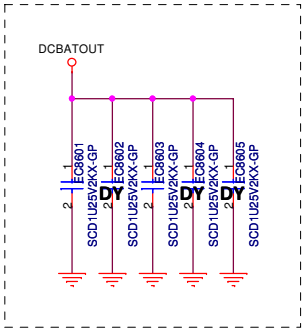
SO1 OPS — STF217R128H83-2-GP — 34.4Y702.301
SO2 OPS — STF217R128H83-2-GP — 34.4Y702.301
SO3 OPS — STF217R128H83-2-GP — 34.4Y702.301

S1 — SPRING-52-GP — 34.4T025.001
S2 — SPRING-52-GP — 34.4T025.001
S3 — SPRING-52-GP — 34.4T025.001
S4 — SPRING-52-GP — 34.4T025.001

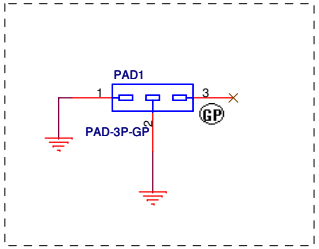
H2 — HOLET256B315R111-GP — ZZ.00PAD.M01
H3 — HT85BE85R29-U-5-GP — ZZ.00PAD.D41
H4 — HOLET256B315R111-GP — ZZ.00PAD.M01

C1 HOLE197R166-1-GP — ZZ.00PAD.V71
C2 HOLE197R166-1-GP — ZZ.00PAD.V71
C3 HOLE197R166-1-GP — ZZ.00PAD.V71

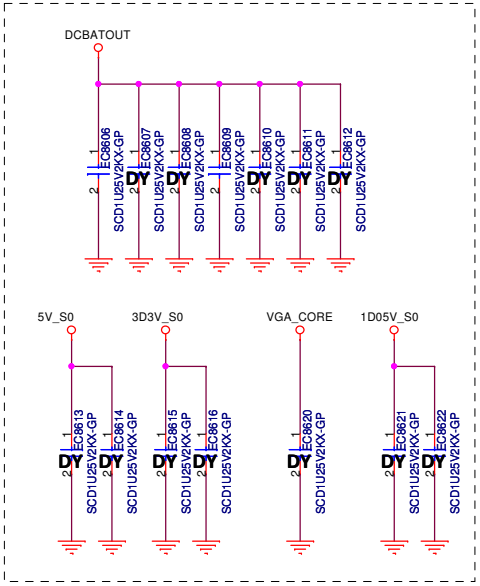
0116 Add RF CAP



0528 Add NPTH hole



0117 Add EMC CAP



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Title: UNUSED PARTS/EMI Capacitors
Size: A3 | Document Number: Hadley 15" | Rev: X02
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<Core Design>

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Title: *Reserved*

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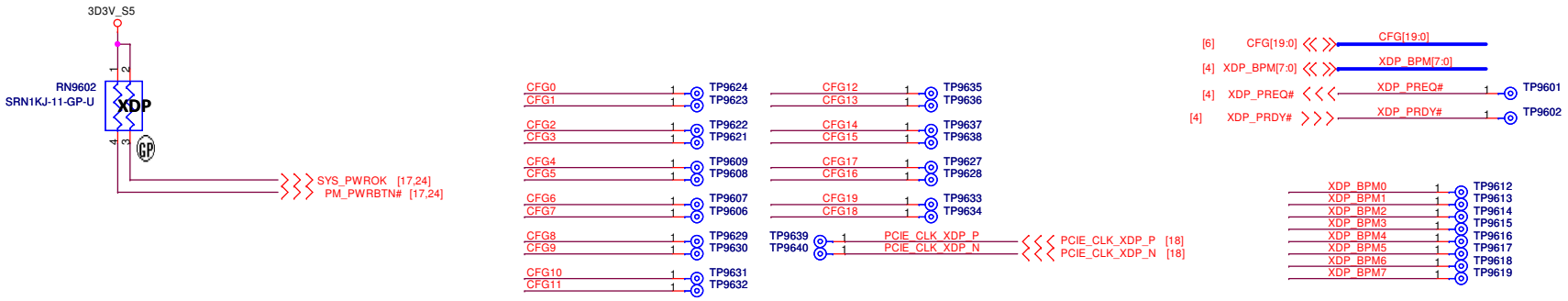
SSID = XDP

CPU XDP



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Title: CPU XDP		
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PCH Strapping

Name	Schematics Notes

Processor Strapping

Pin Name	Strap Description	(Default value for each bit is 1 unless specified otherwise)	Default Value

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION

SMBus ADDRESSES

I²C / SMBus Addresses	CHIEF RIVER ORB	
Device	Address	Bus
EC SMBus 1		
Battery 0	0x16	BAT_SCL/BAT_SDA
CHARGER	0x12	BAT_SCL/BAT_SDA
PS8122(HDMI Switch) (Bottom Dock)	0x9E	BAT_SCL/BAT_SDA
USB3.0 redriver PS8710 (Bottom Dock)	0x40	BAT_SCL/BAT_SDA
EC SMBus 2		
Battery 1	0x16	SML1_CLK/SML1_DATA
PCH	0x96 & 0x94	SML1_CLK/SML1_DATA
Discrete VGA Thermal	0x9C or 0x9E	SML1_CLK/SML1_DATA
PS8321 HDMI level shifter	0x96 & 0X97	SML1_CLK/SML1_DATA
NCT7718W	0x98 or 0x99	SML1_CLK/SML1_DATA
EC SMBus 3		SMB2_CLK/SMB2_DATA
NCT5605Y-0	0x30	SMB2_CLK/SMB2_DATA
NCT5605Y-1	0x32	SMB2_CLK/SMB2_DATA
PCH SMBus		
SO-DIMMA		PCH_SMBDATA/PCH_SMBCLK
SO-DIMMB		PCH_SMBDATA/PCH_SMBCLK
Intel LAN 82579		PCH_SMBDATA/PCH_SMBCLK
G-Sensor		PCH_SMBDATA/PCH_SMBCLK
MINI WWAN		PCH_SMBDATA/PCH_SMBCLK
INTEL LAN82579		PCH_SMBDATA/PCH_SMBCLK

PCIE Routing

LANE1	X
LANE2	X
LANE3	Mini Card1(WLAN)
LANE4	X
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	
3	
4	
5	

USB Table

Pair	Device
0	USB port 1,with Power Share
1	USB 2.0 HDMI
2	USB port2 (usb redriver)
3	X
4	Touch Panel
5	Card Reader
6	BLUETOOTH
7	CAMERA

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Title: Table of Content

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Title
Change History

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	Hadley 15"	***X02***

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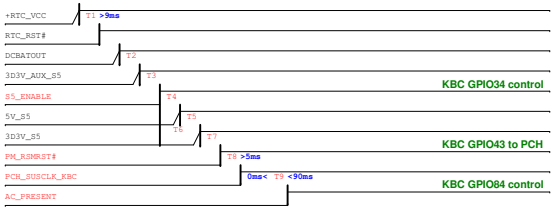
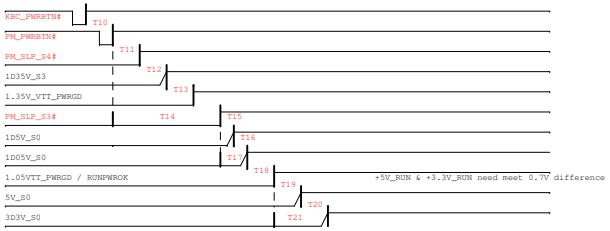
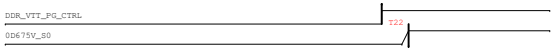
Intel-Power Up Sequence

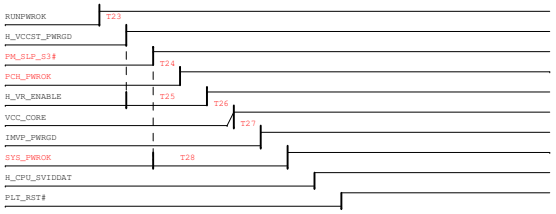
(AC mode)

Red printings:KBC GPIO involved









(DC mode)

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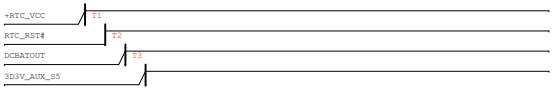

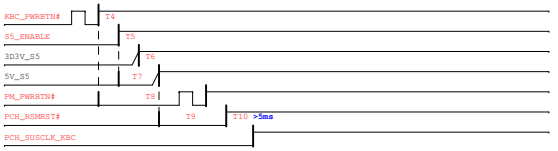

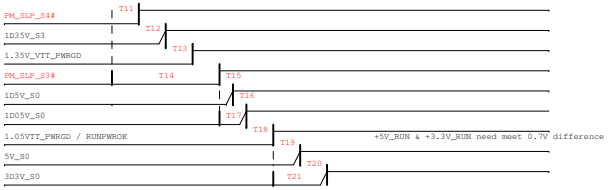

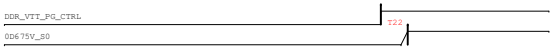

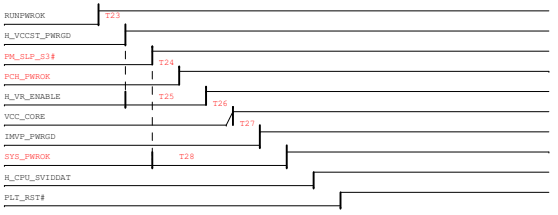

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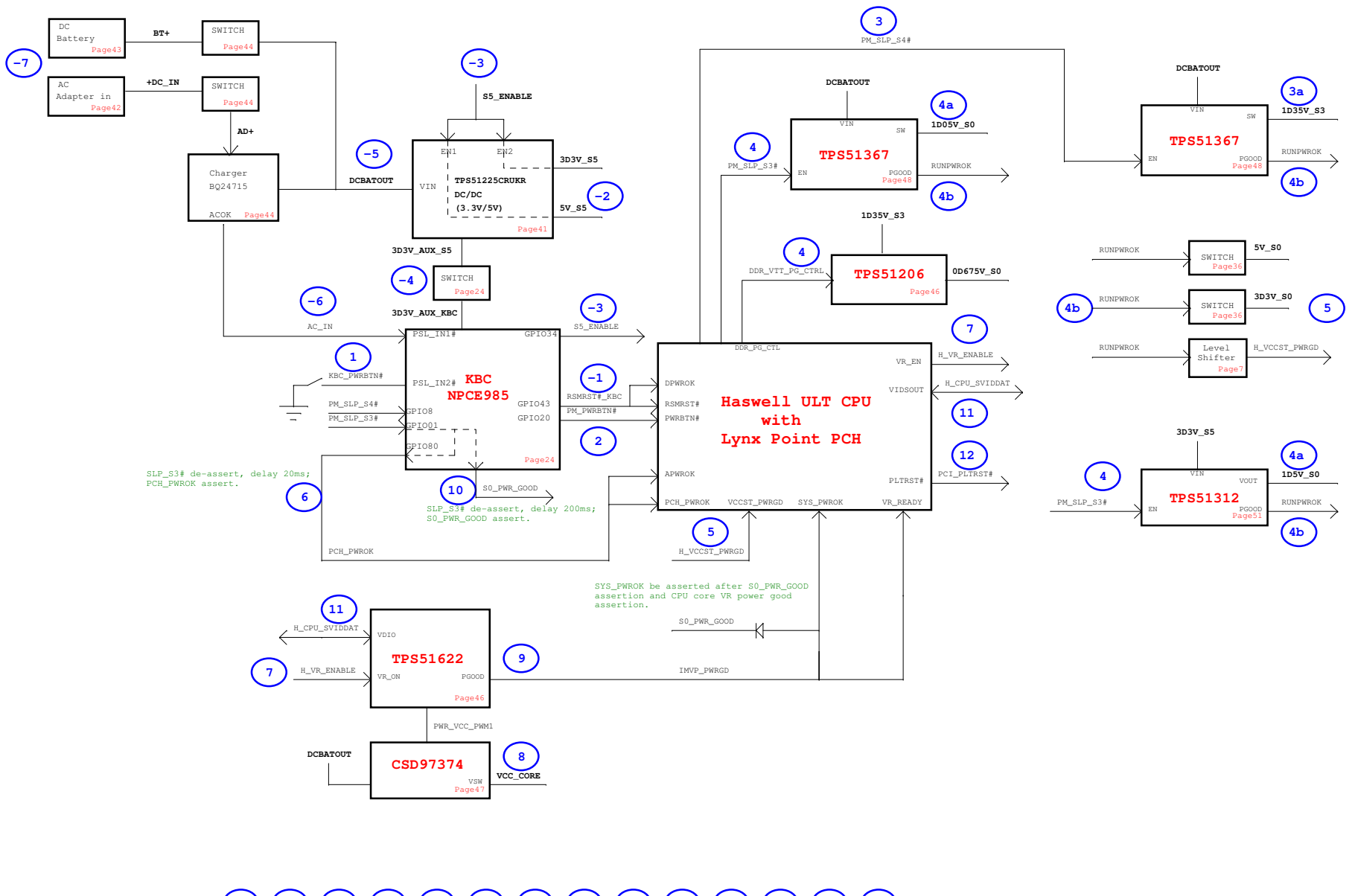
Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



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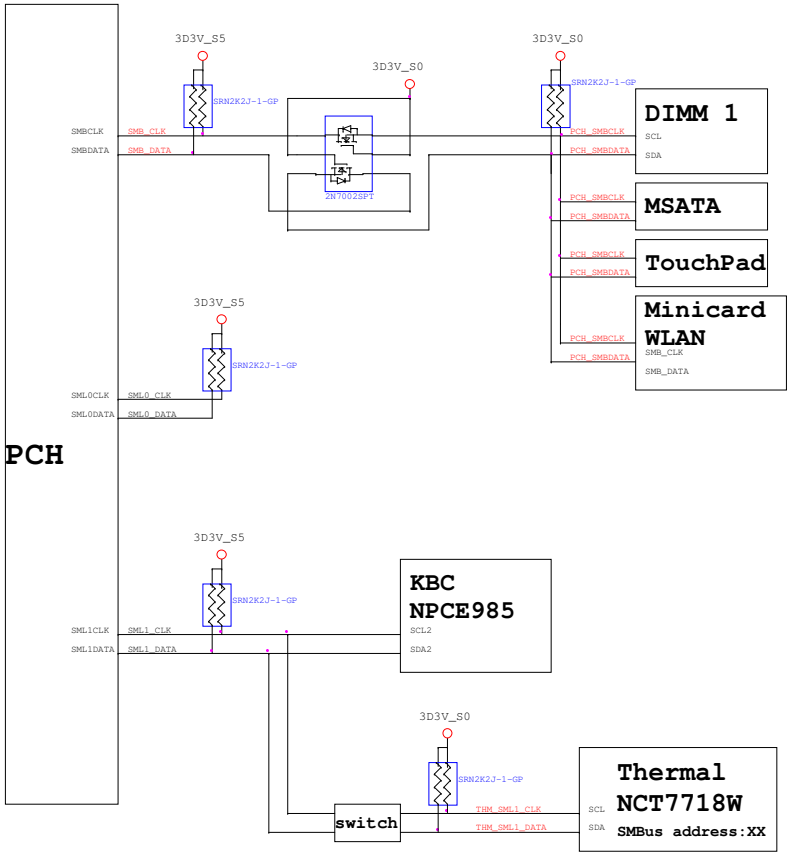
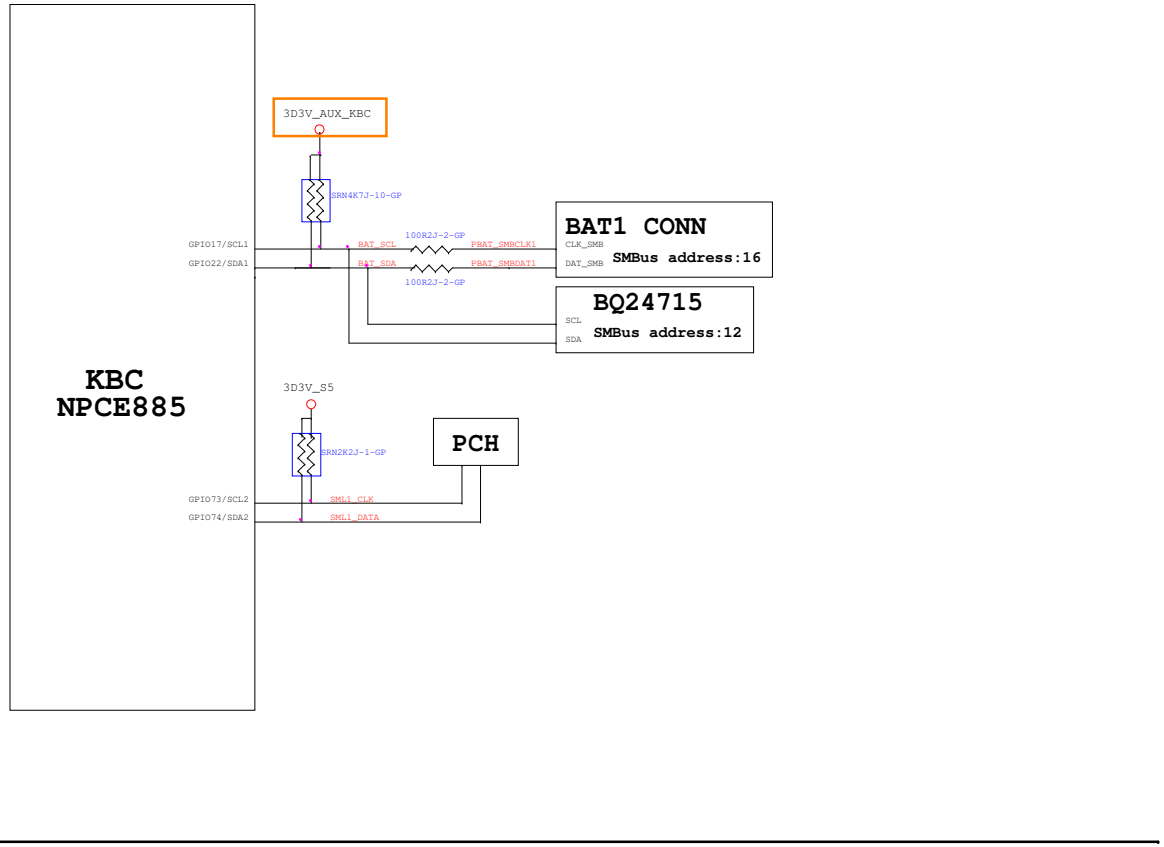
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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