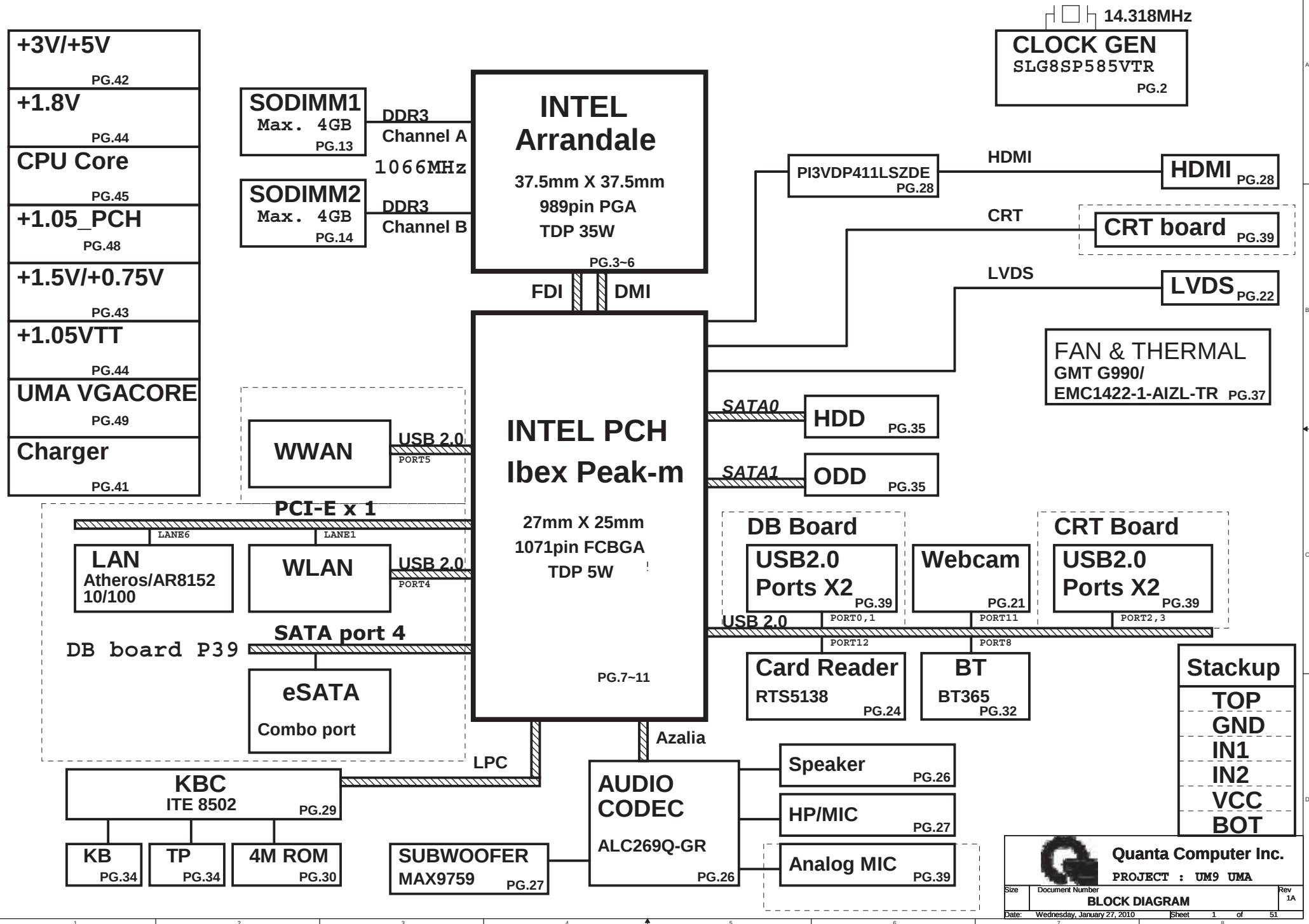
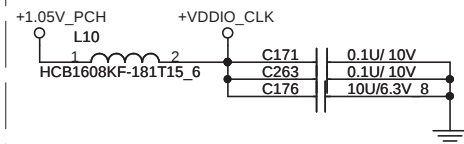


UM9 UMA SYSTEM DIAGRAM

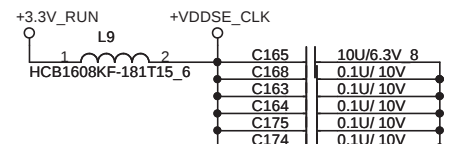


25mA



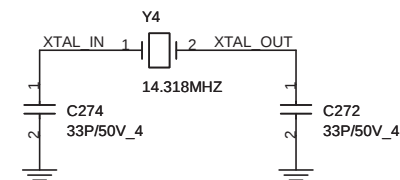
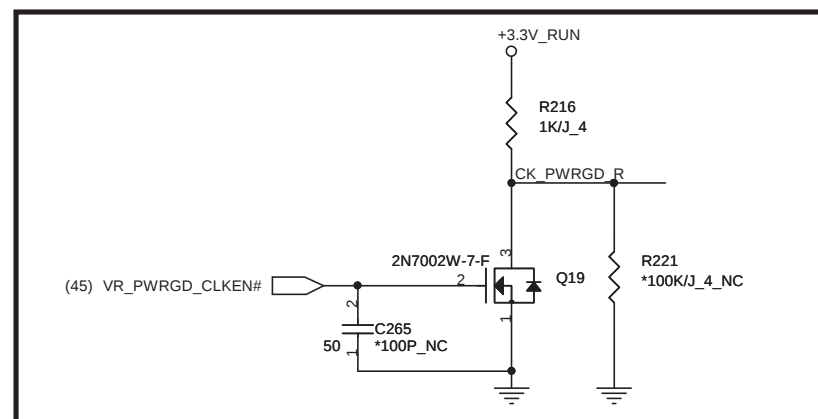
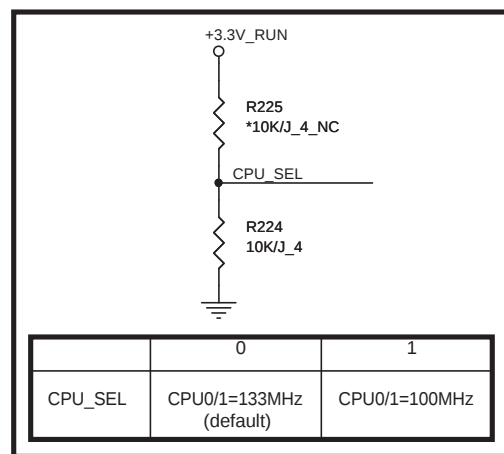
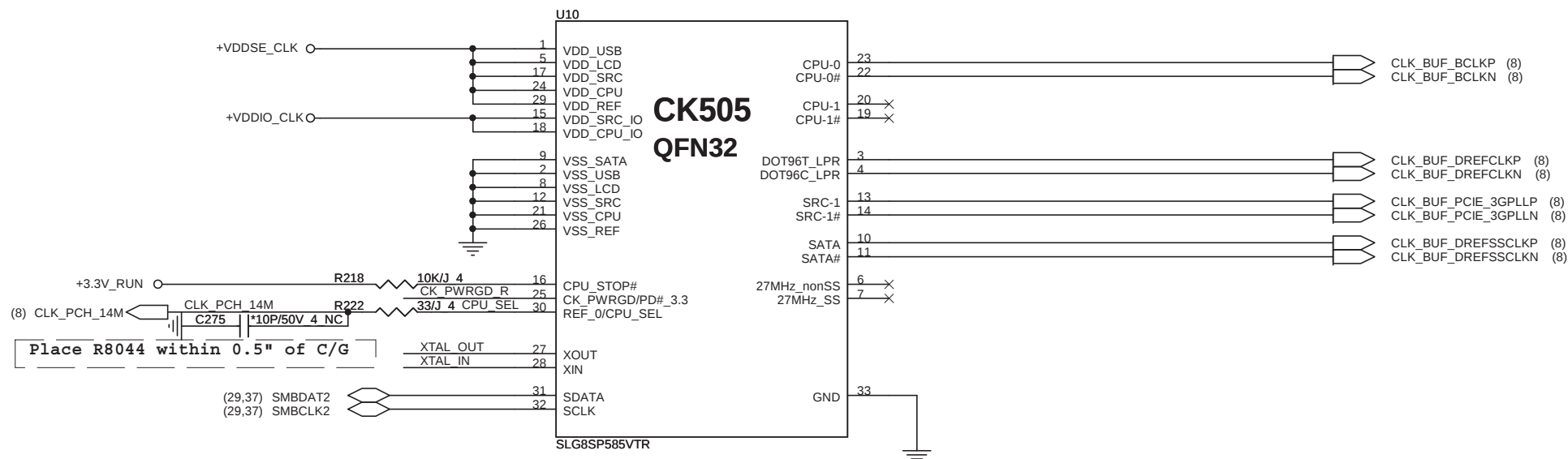
Place each 0.1uF cap close to pin

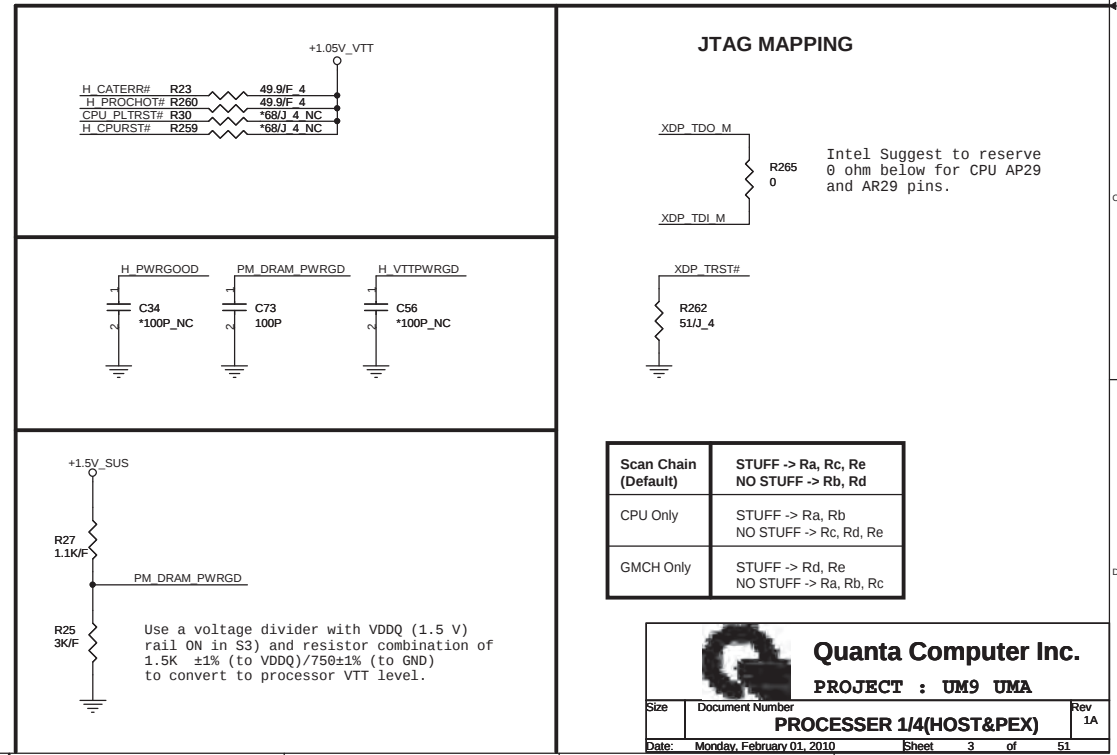
300mA



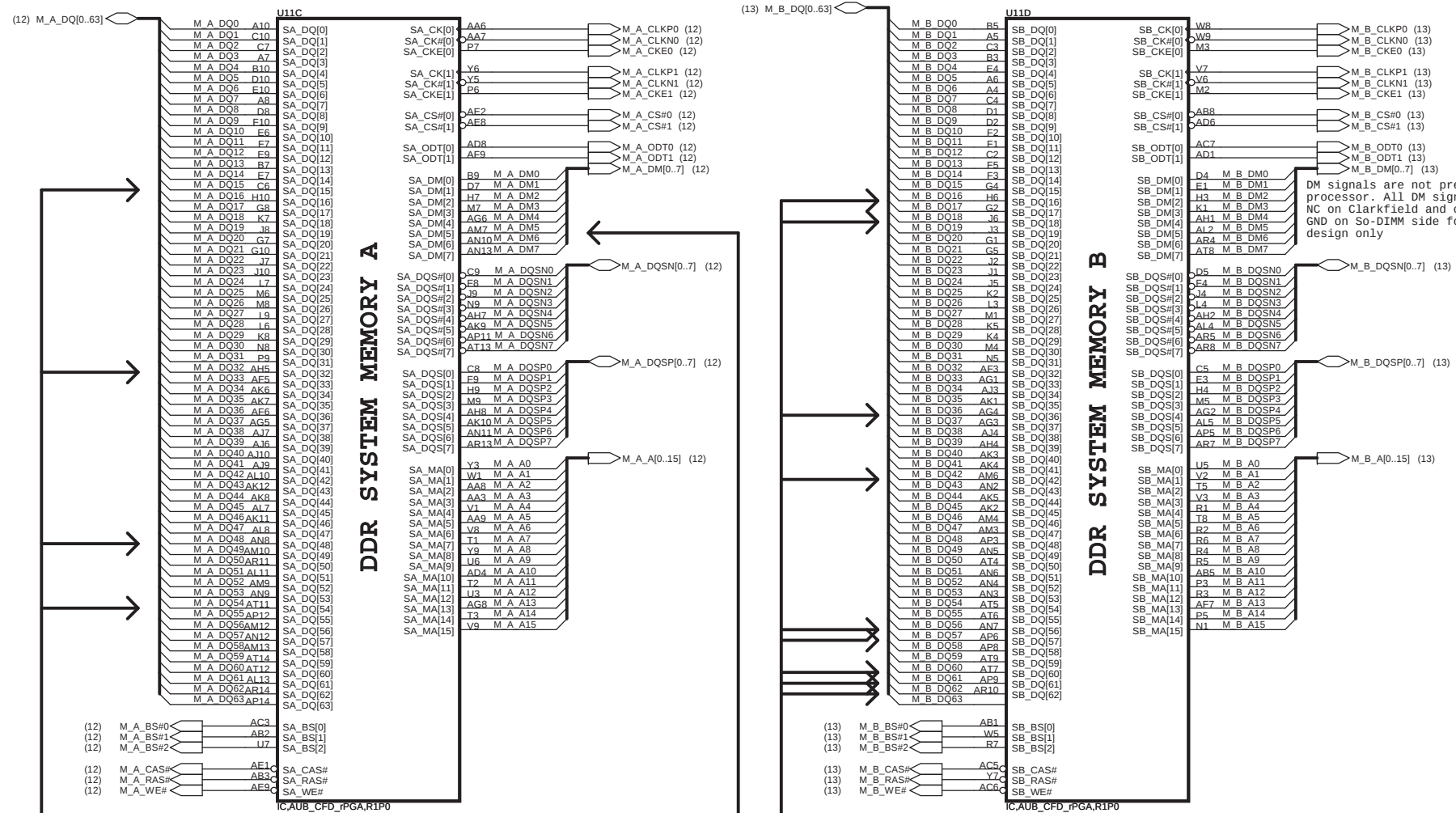
Place each 0.1uF cap close to pin

PDC (Power Cap quantities follow UM3)





AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.



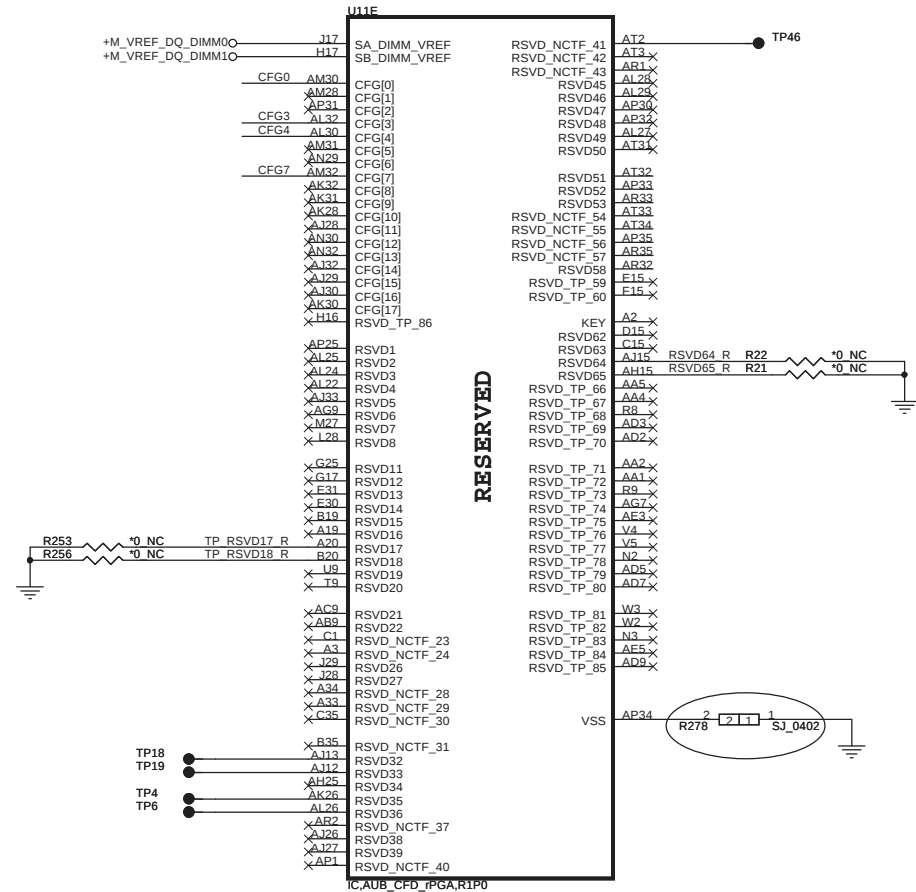
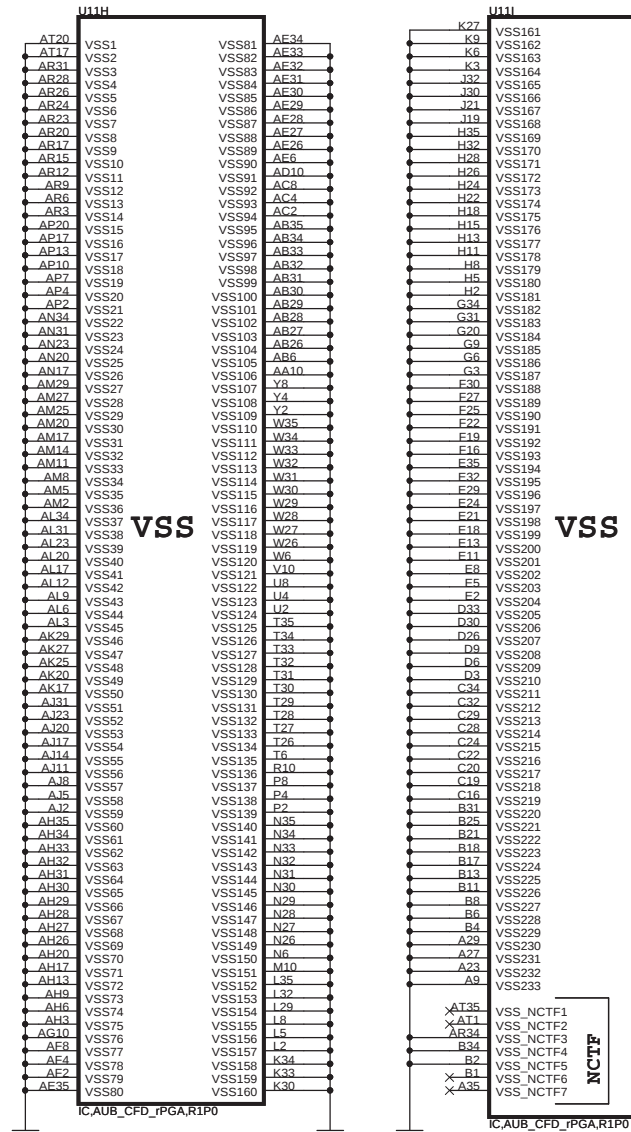
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AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

06



For Discrete only

CFG[1:0] - PCI_Epress Configuration Select

- * 11= 1 x 16 PEG
- * 10= 2 x 8 PEG



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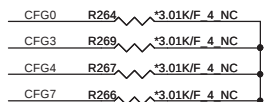
PROJECT : UM9 UMA

Size Document Number

PROCESSOR 4/4 (GND)

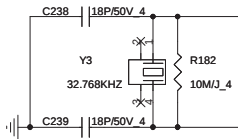
Date: Wednesday, January 27, 2010 Sheet 6 of 51

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

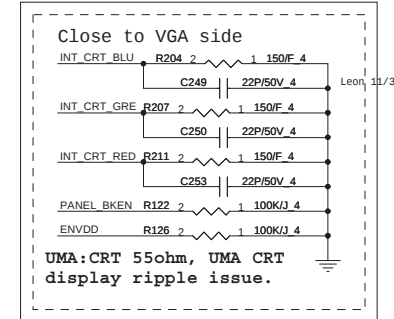
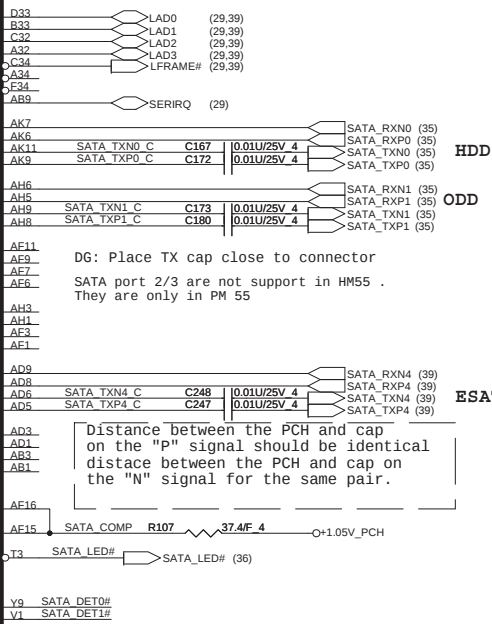
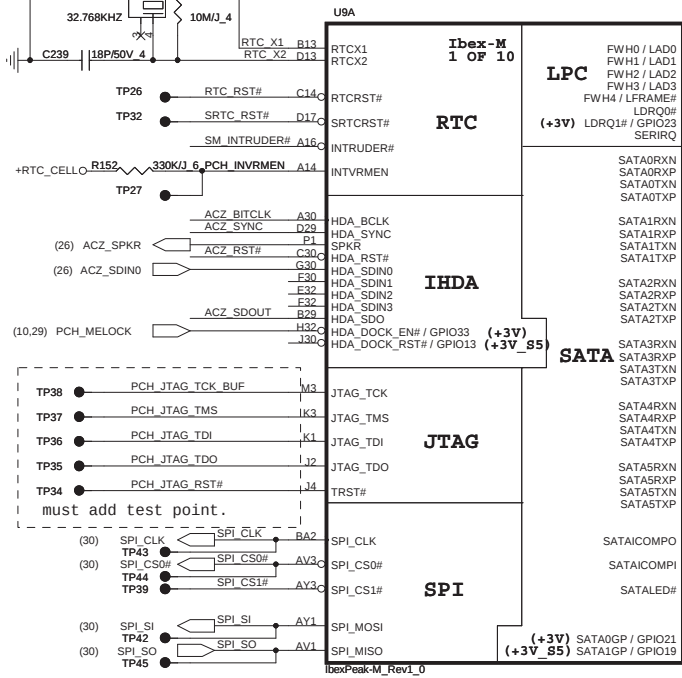


The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

INVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

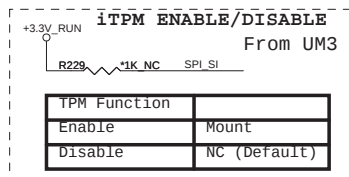
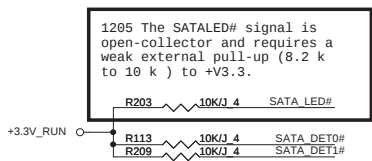
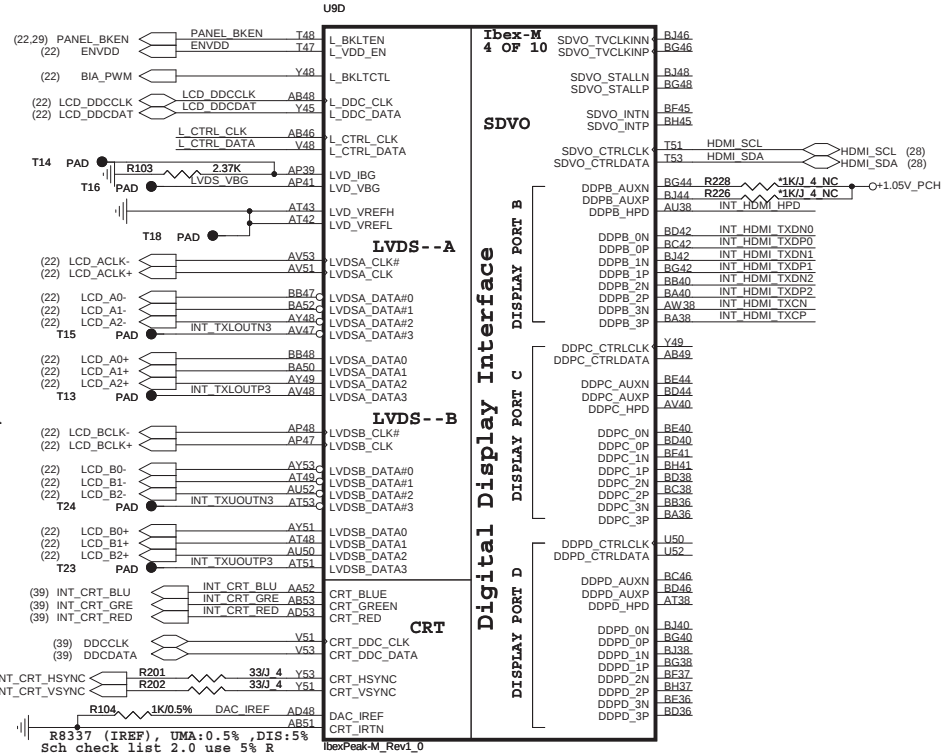


IBEX PEAK-M (HDA,JTAG,SATA)

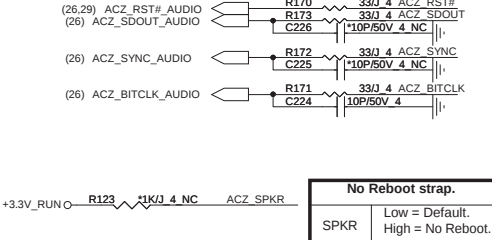


UMA CRT,LVDS&HDMI signals

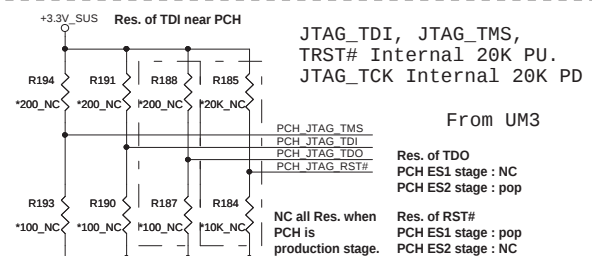
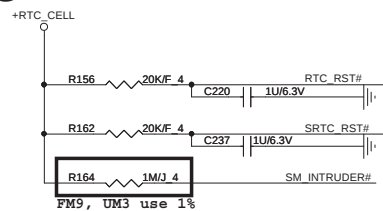
IBEX PEAK-M (LVDS,DDI)



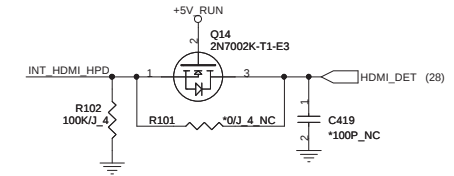
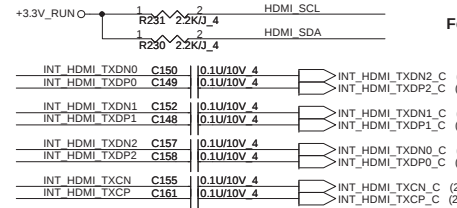
For AUDIO



RTC 1mA

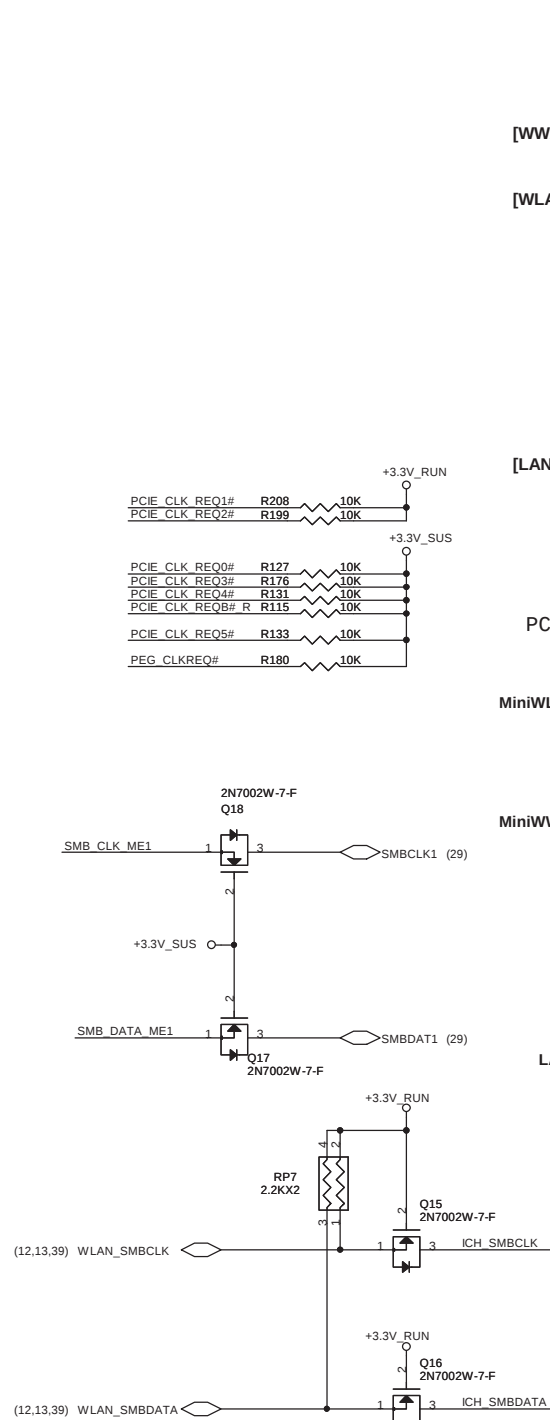


For UMA HDMI Function

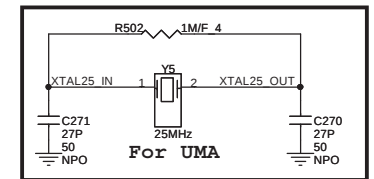
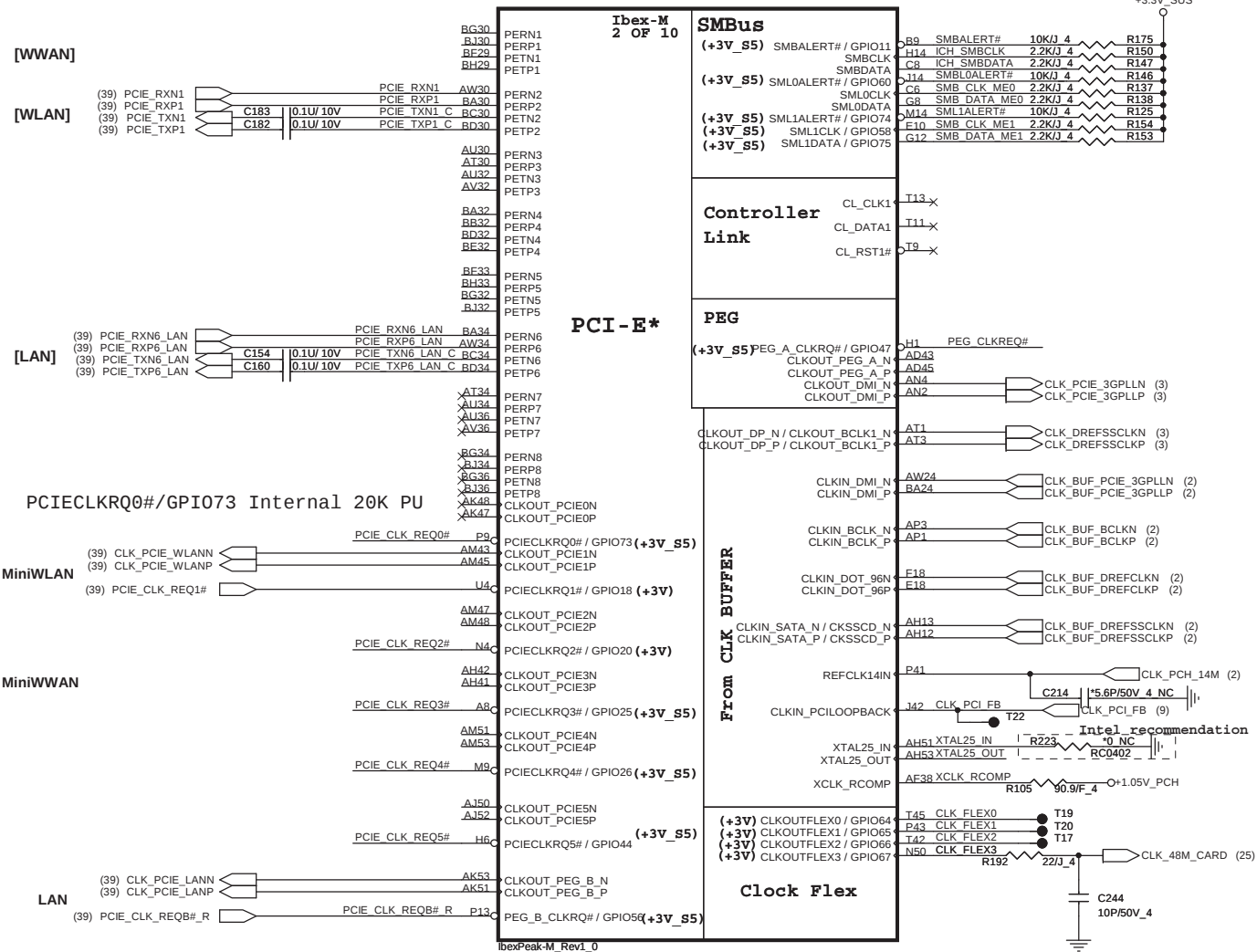


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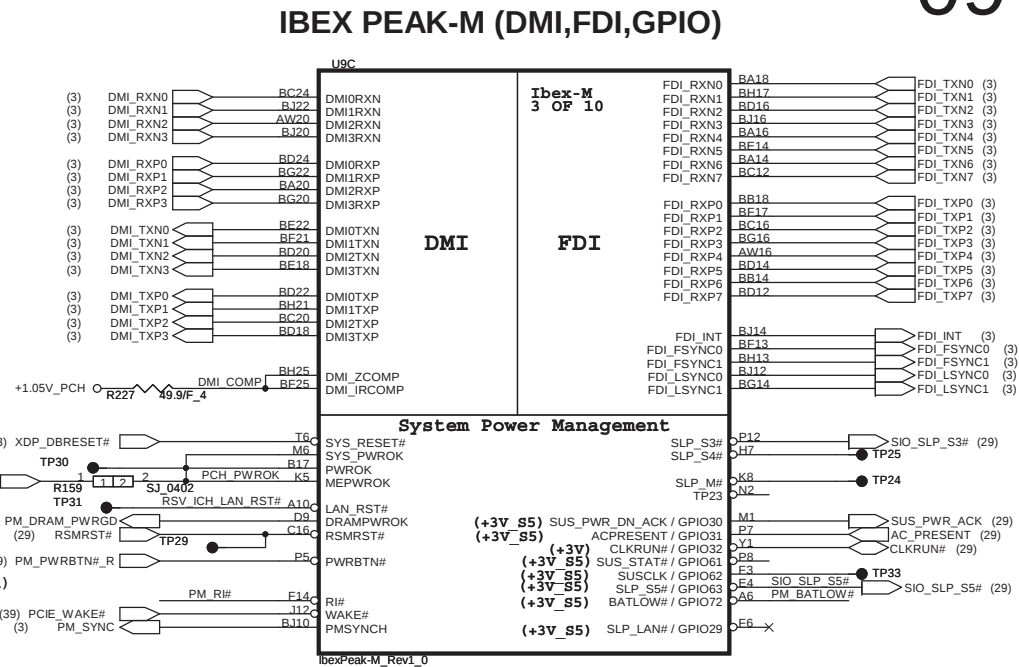
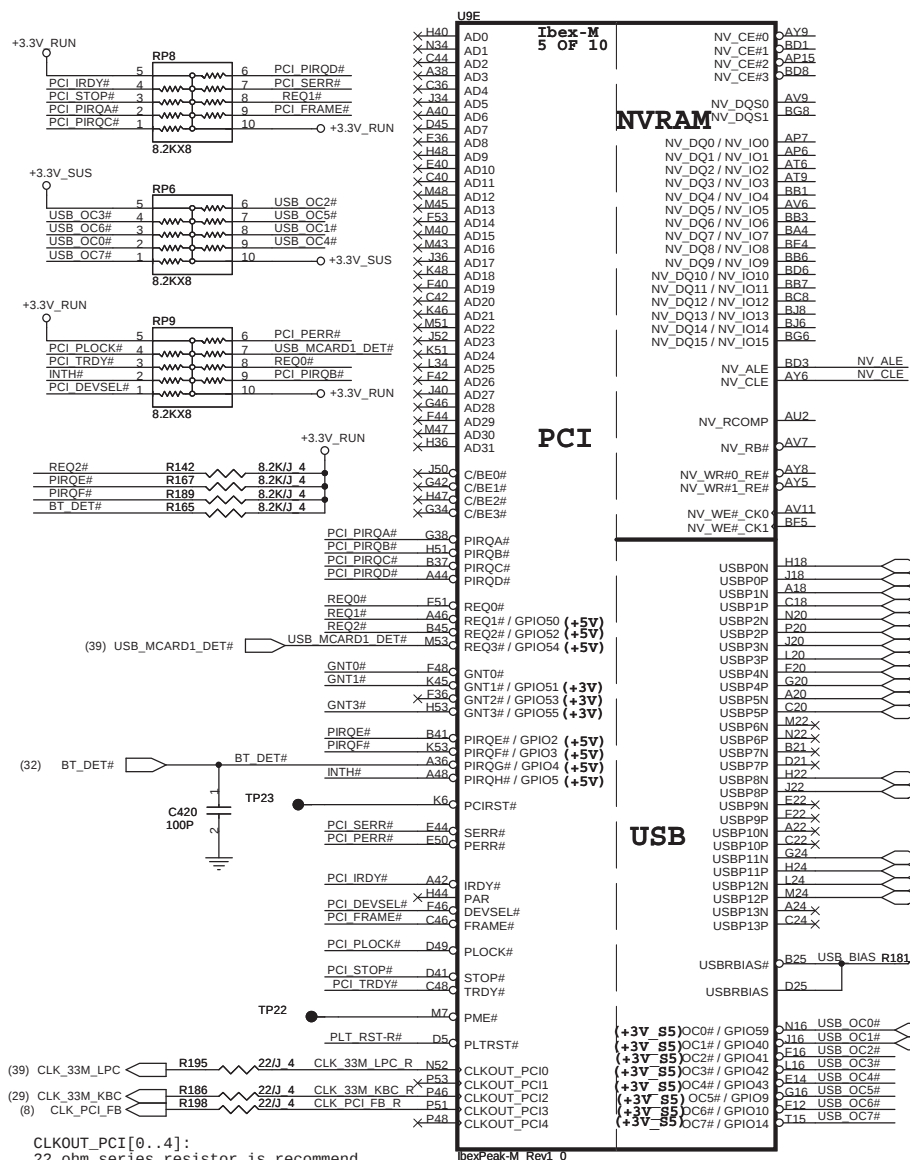
PROJECT : UM9 UMA



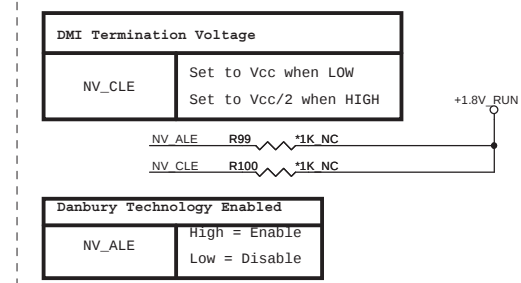
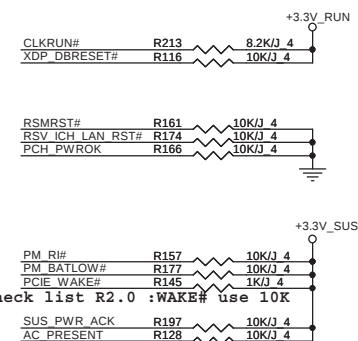
U9B



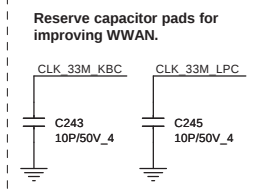
IBEX PEAK-M (PCI,USB,NVRAM)



BATLOW#/GPIO72 Internal 20K PU

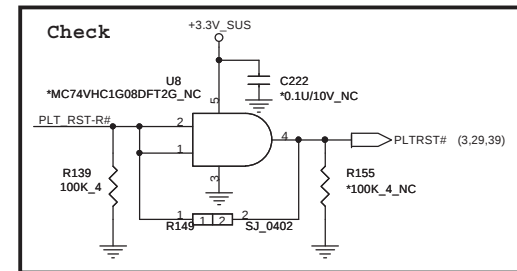


CLKOUT_PCI[0..4]:
22 ohm series resistor is recommend
(single & double load) on PDG v1.1



Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

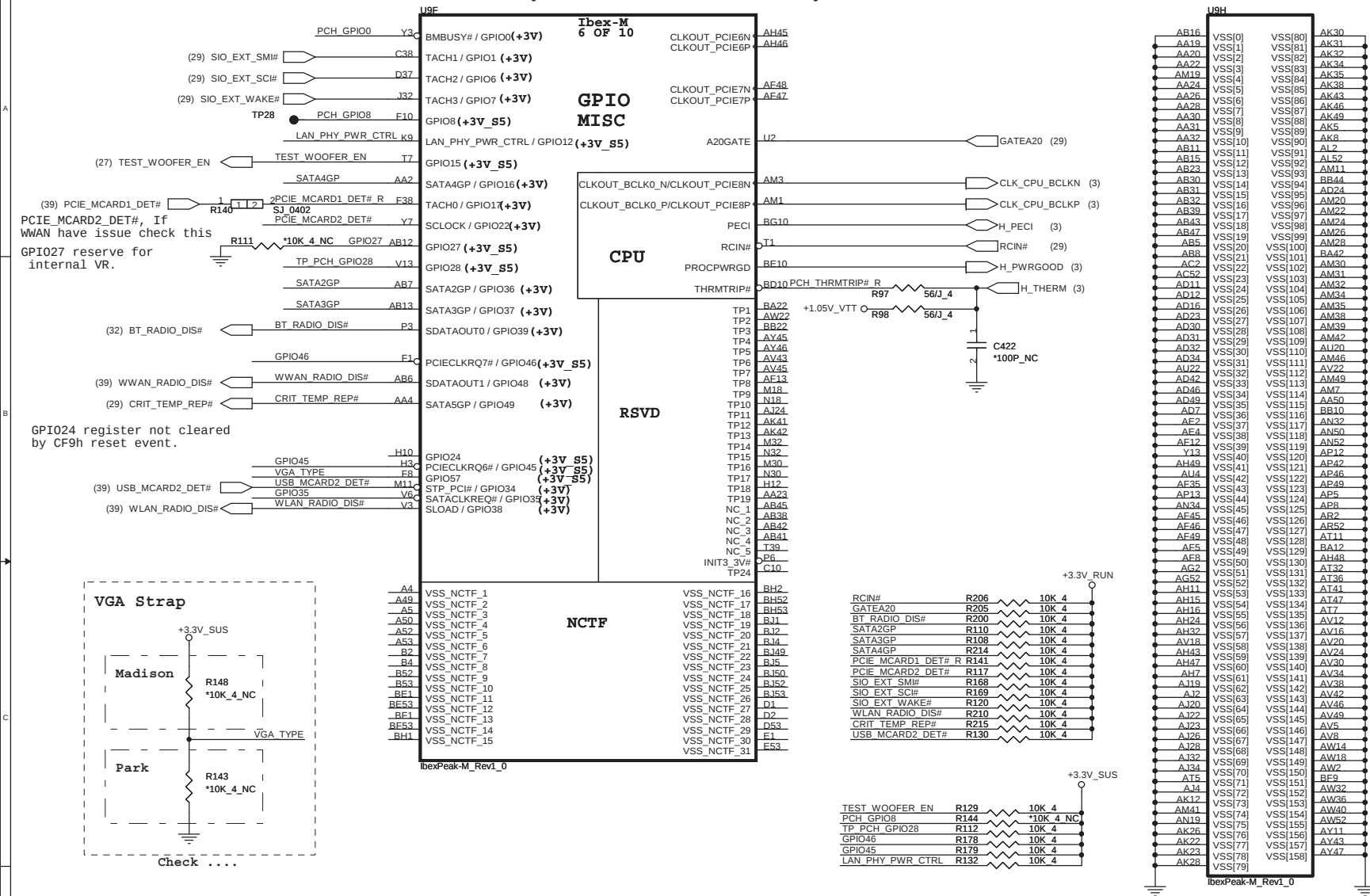
A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

10



GPIO[7,6,1,17], PCIECLKRQ6#/GPIO45,
GPIO28 Internal 20K PU

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up
(8.2- KΩ to 10 KΩ) to Vcc3.3.
CRB(V1.0)P28: it has 1K PU and
100 ohm on this net for validation purpose.

WWAN_RADIO_DIS# 1-X High = Strong (Default)

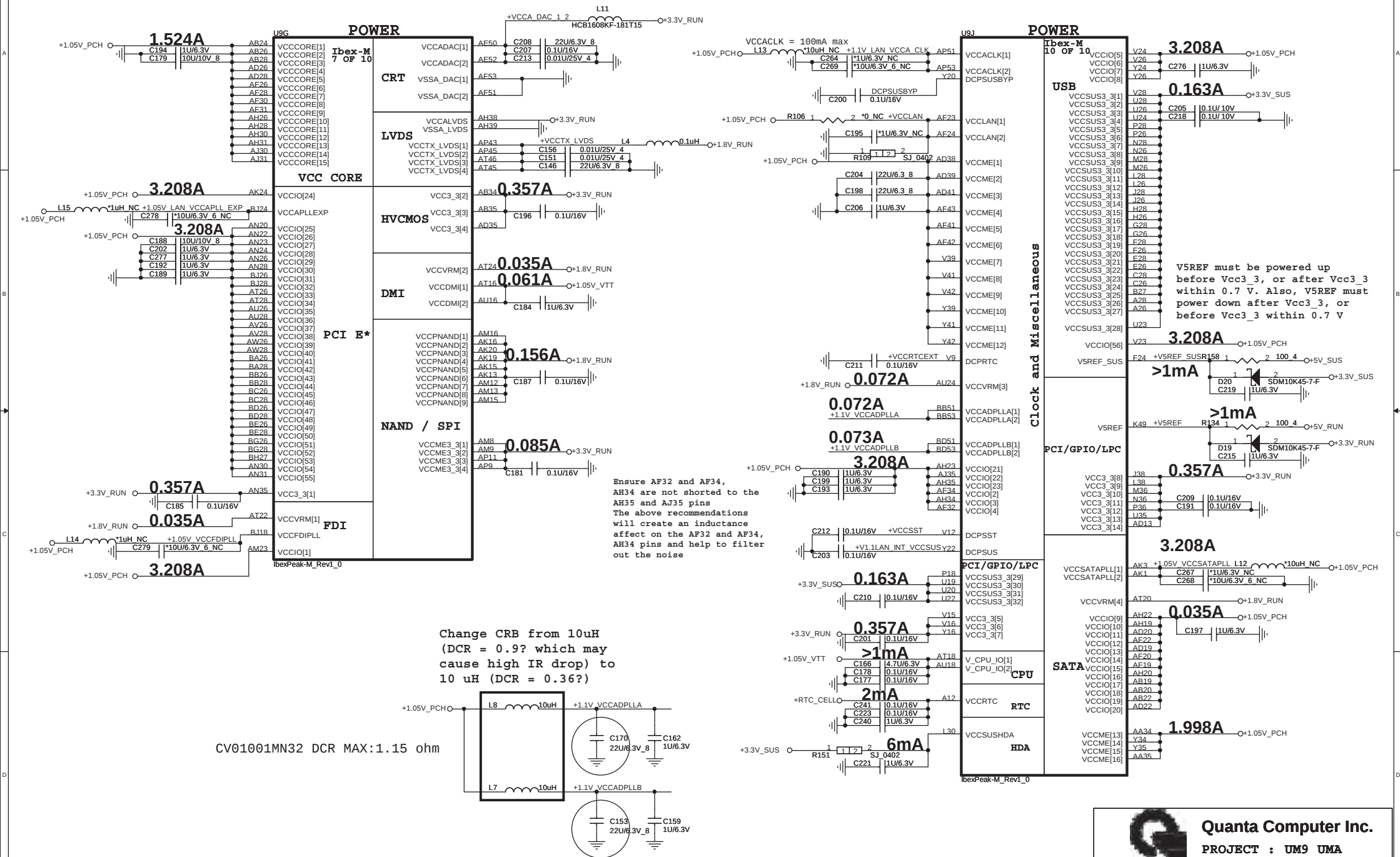


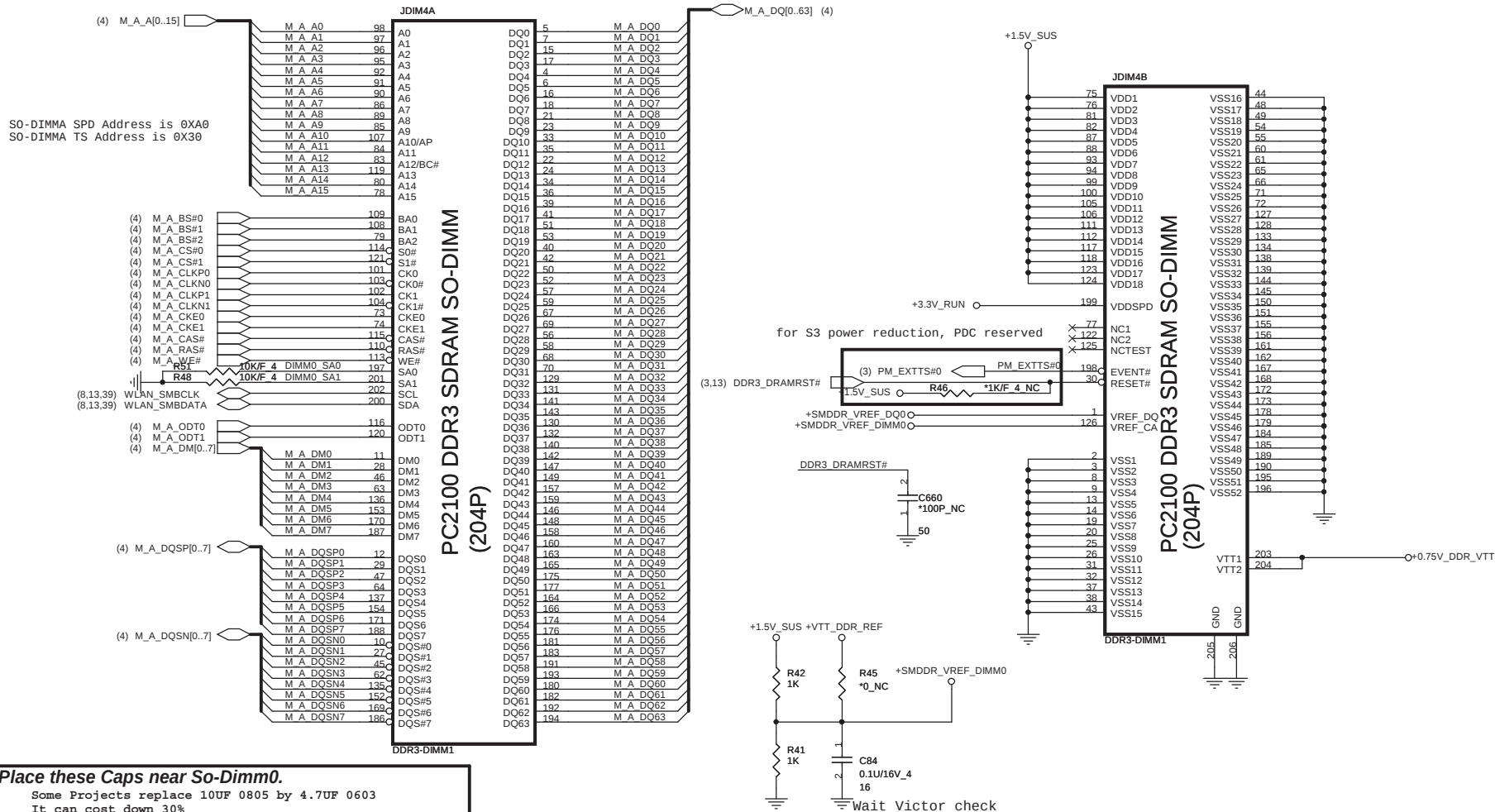
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Cap quantities follow UM3

C8335 UMA:22u, DIS:10u, solve UMA CRT display ripple issue.





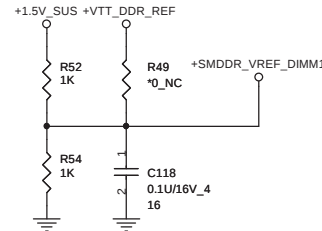
Quantities and M1/M3 follow UM3
Locations follow PDC



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	DDR3 DIMM-0	1A
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D					
C					
B					
A					



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B					
A					



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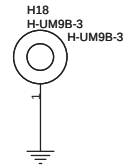
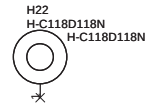
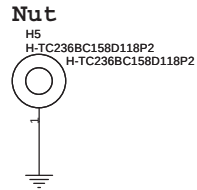
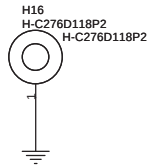
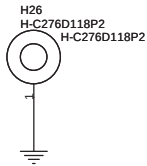
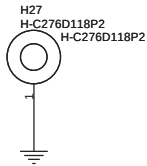
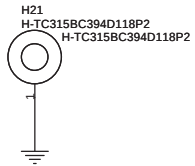
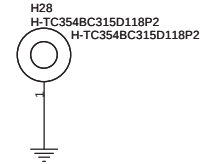
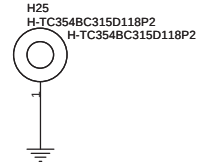
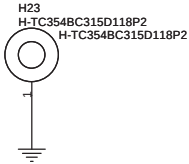
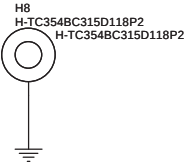
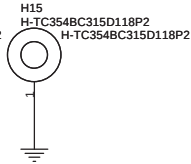
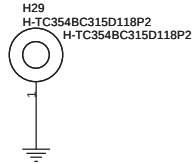
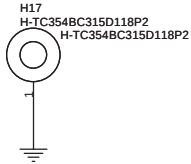
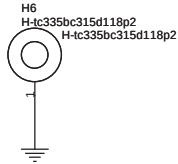
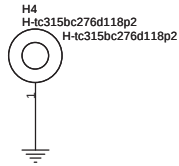
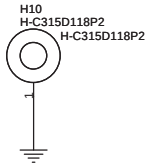
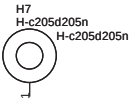
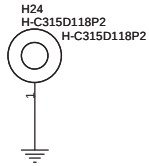
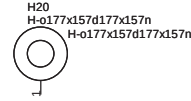
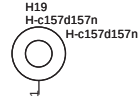
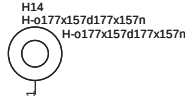
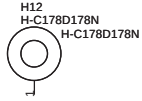
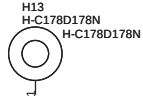
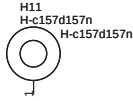


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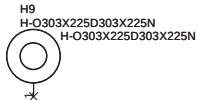
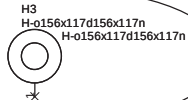
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Del H1&H2



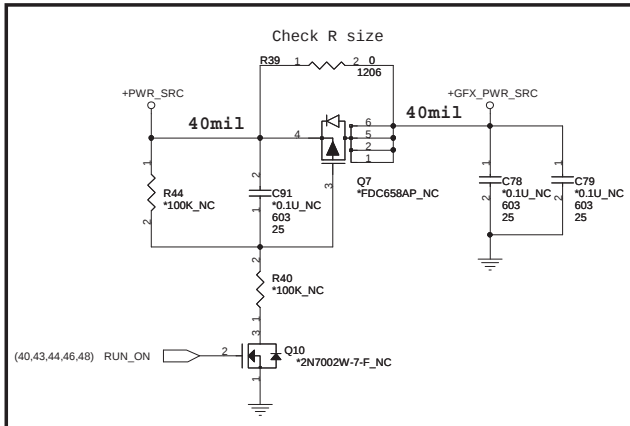
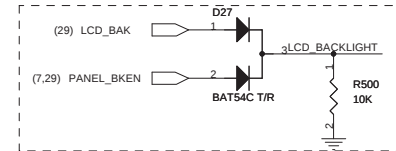
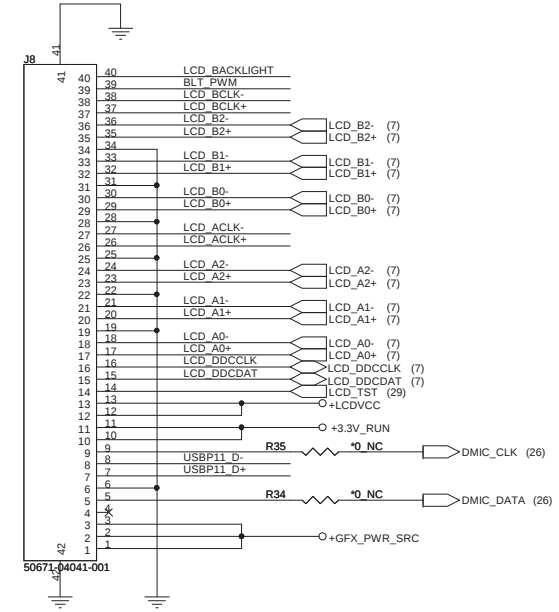
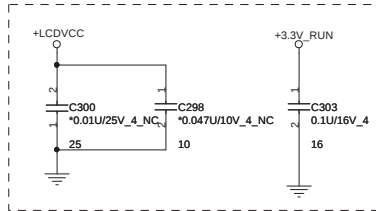
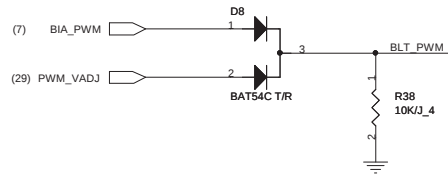
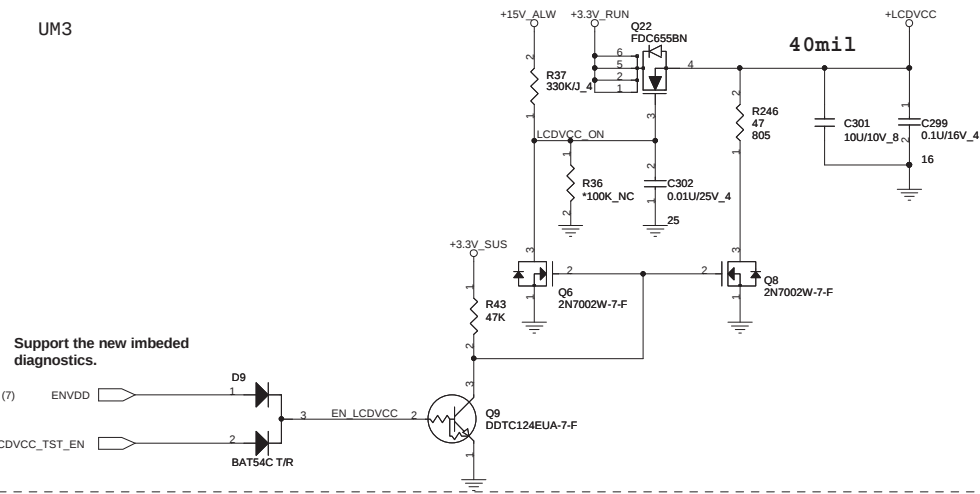
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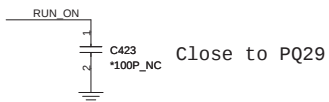
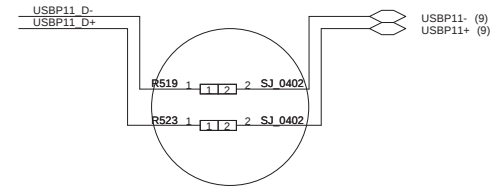
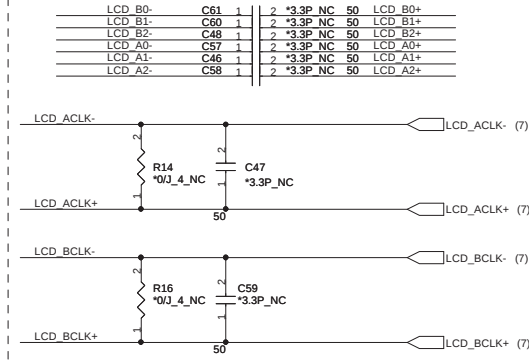
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UM3



Shunt capacitors on LVDS for improving VVWAN.





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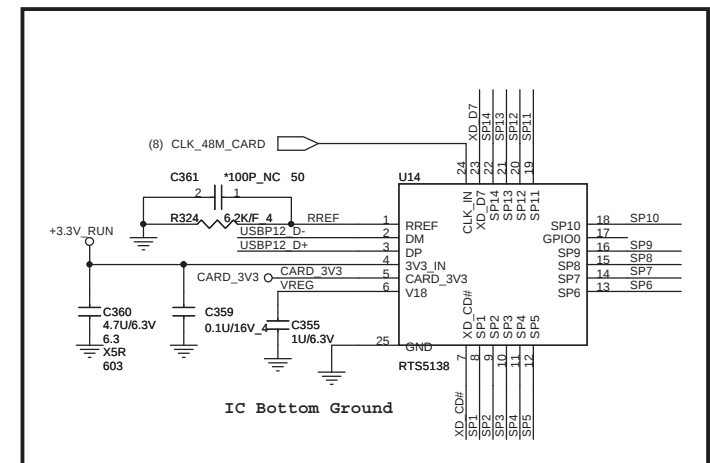
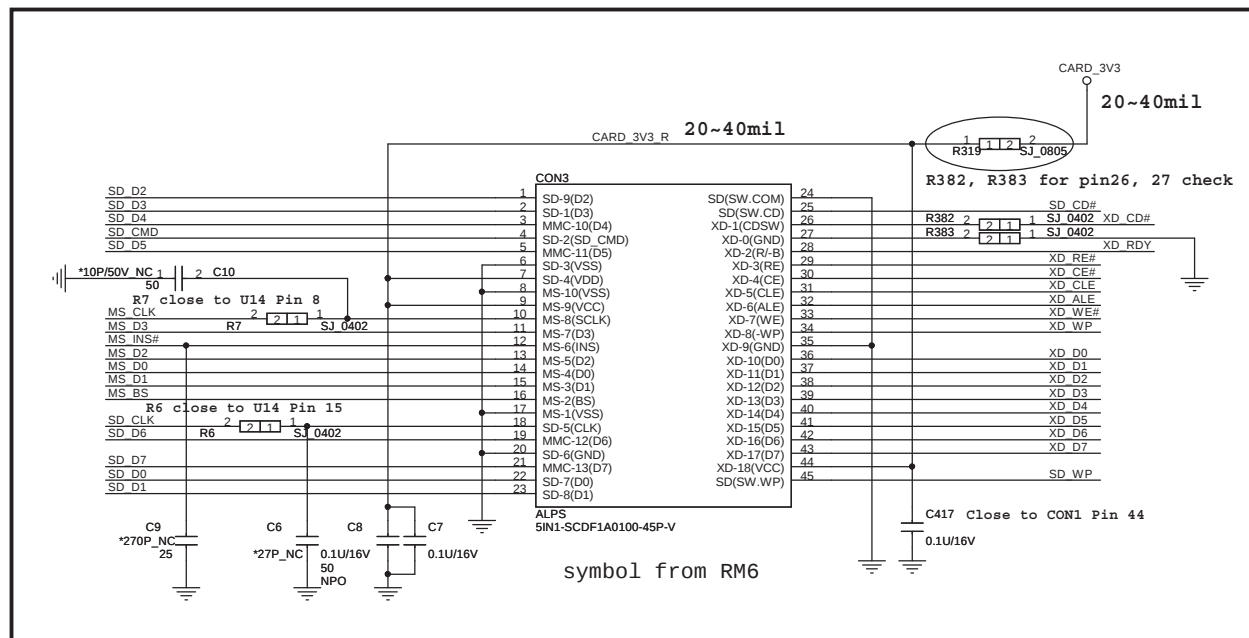
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DB CONN/Left USB

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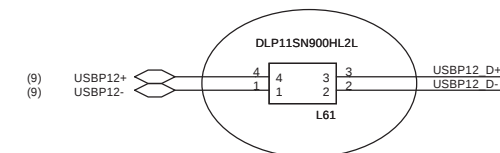
Sheet 24 of 51

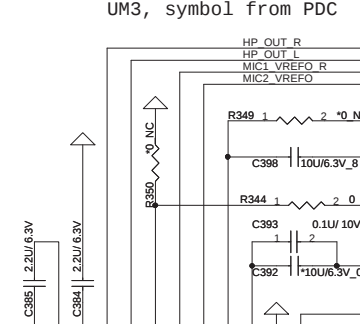


RTS5138-QFN24

SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#		MS INS#
SP3	XD CE#	SD D1	
SP4	XD CLE	SD D0	MS D7
SP5	XD ALE	SD D7	MS D3
SP6	XD WE#	SD CD#	
SP7	XD WP	SD D6	MS D6
SP8	XD D0	SD CLK	MS D2
SP9	XD D1	SD D5	MS D0
SP10	XD D2	SD CMD	
SP11	XD D3	SD D4	MS D4
SP12	XD D4	SD D3	MS D1
SP13	XD D5	SD D2	MS D5
SP14	XD D6		MS B5

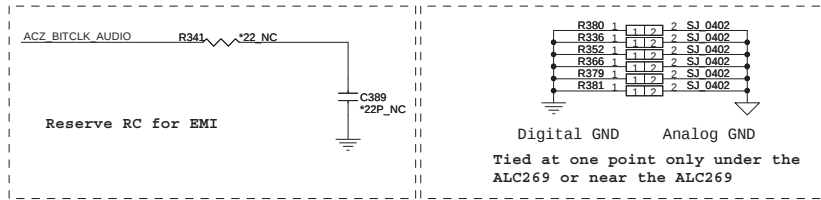
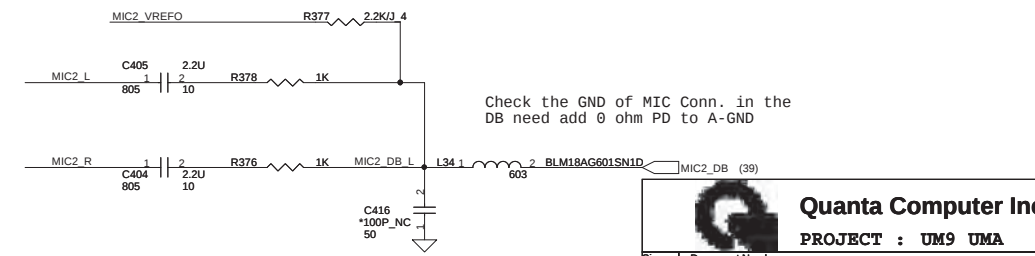
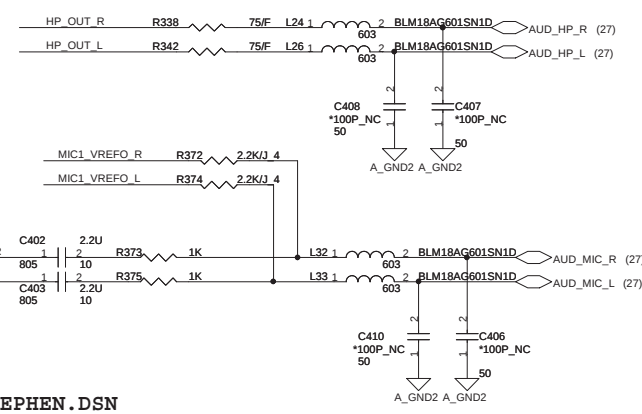
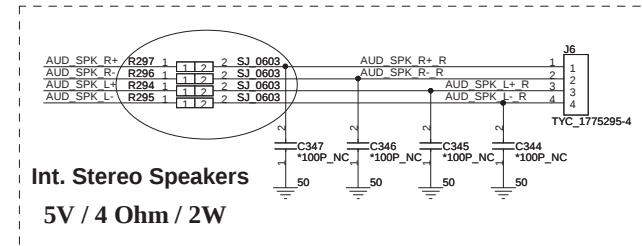
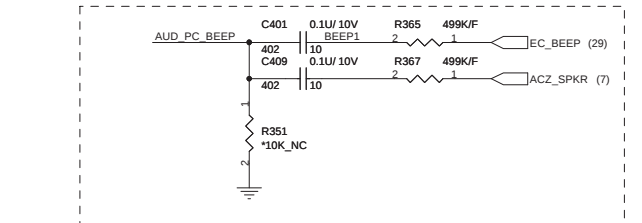
Share Pin



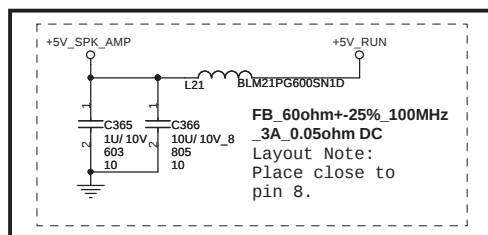
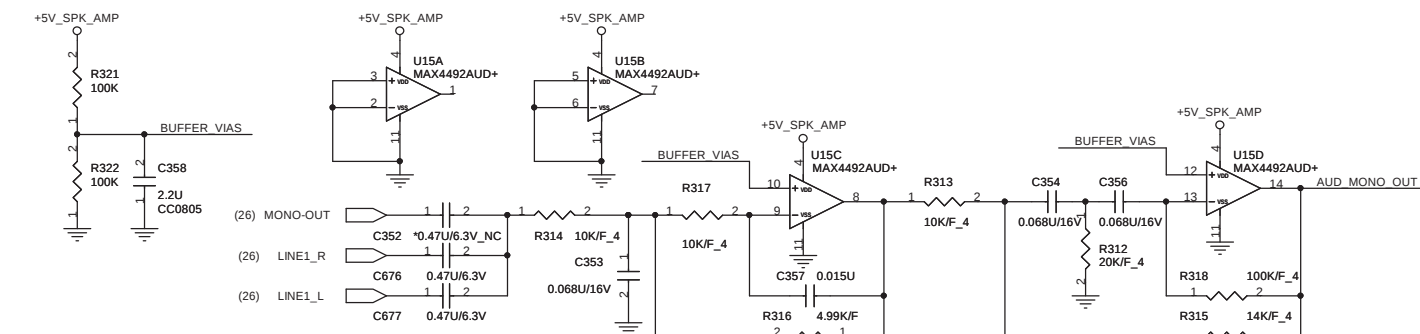
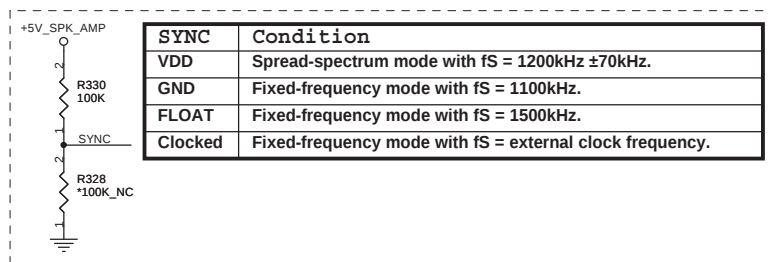


PIN NAME	R350	R344	R349	C398	CODEC IC
28 MIC1_VREF0-L			NC	POP	ALC269
31 CPVREF	NC	POP			VB

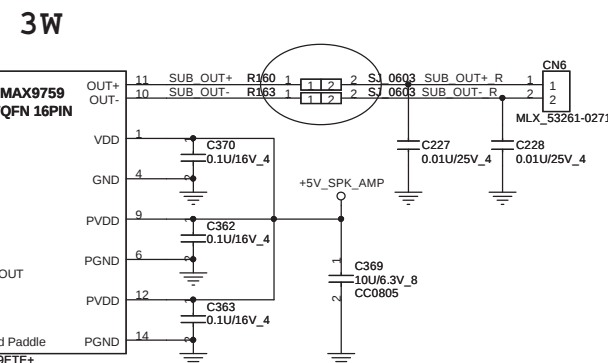
VB type: PIN31 作為MIC之偏壓
PIN28接CAP作為內部LDO
output 輸出濾波用



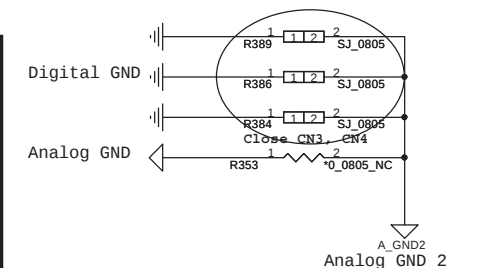
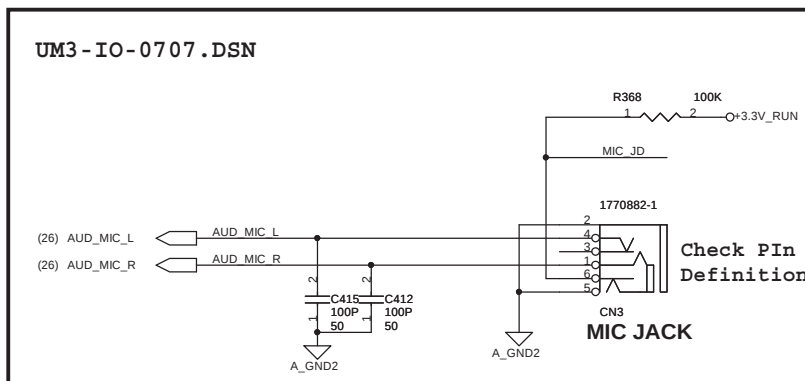
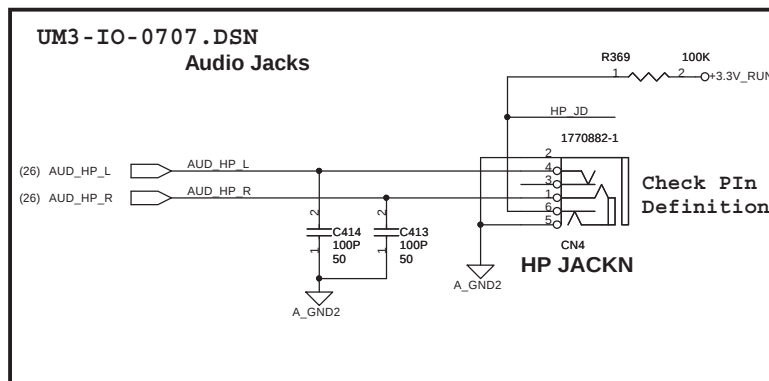
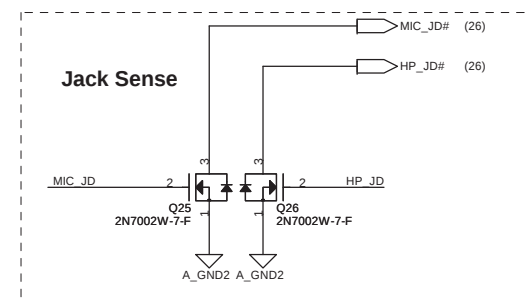
INTERNAL SUBWOOFER AMP Only for 17"



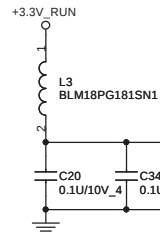
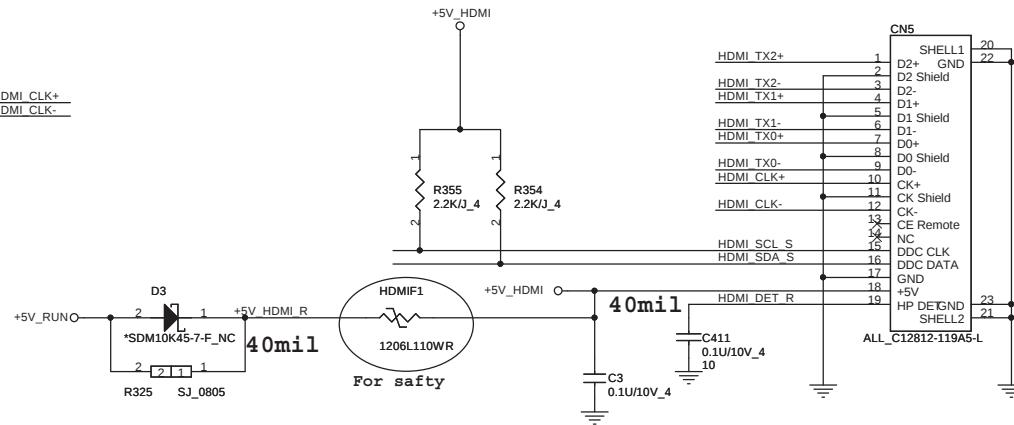
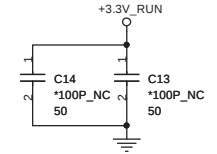
NB_MUTE#	TEST_WOOFER_EN	AUD_SPK PD#	SUB_MUTE#
0	0	L (Disable SPK)	L (Disable Woofer)
0	1	L (Disable SPK)	H (Test Woofer)
1	0	H (Test SPK)	L (Disable Woofer)
1	1	H (Test SPK)	H (Test Woofer)



	GAIN1	GAIN2	GAIN
	0	0	24dB
	1	0	18dB
	0	1	12dB
	1	1	6dB



HDMI



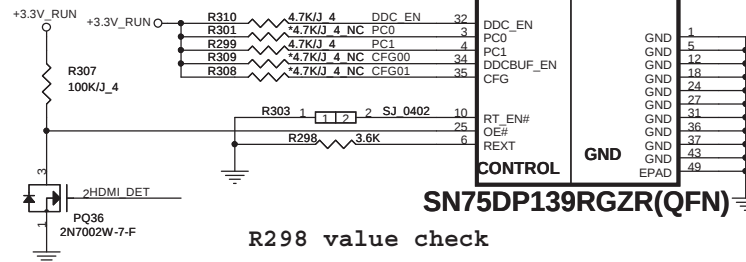
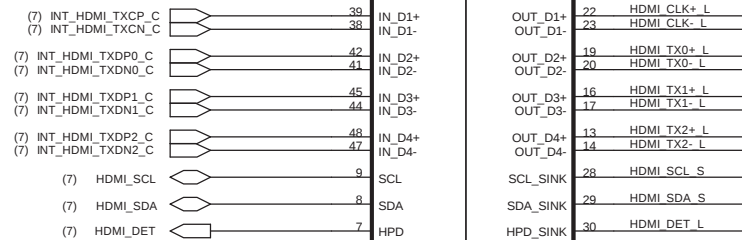
EQUALIZATION SETTING	
PC1:PC0=0:0	8dB
PC1:PC0=0:1	4dB Recommended
PC1:PC0=1:0	12dB
PC1:PC0=1:1	0dB

SCLZ/SDAZ Low-level input/output Voltage	
CFG01:CFG00=0:0	VIL:<0.4V VOL:0.6V (Default)
CGF01:CGF00=0:1	VIL:<0.36V VOL:0.55V
CGF01:CGF00=1:0	VIL:<0.44V VOL:0.65V
CGF01:CGF00=1:1	VIL:<0.36V VOL:0.6V

HDMI_PWR_CTRL
0 is Enable
1 is Disable

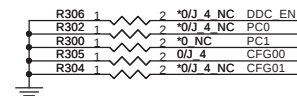
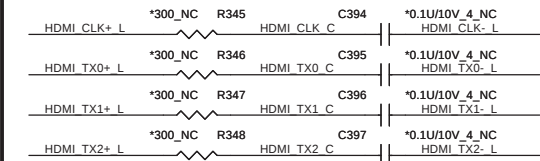
TI SN75DP139

PIN 4 I2C_EN	H	HDMI
	L	DVI
PIN 34 HPDINV	H	HPD Inversion VOH = 0.9V
	L	HPD non-inversion VOH = 3.2V



R298 value check

For EMI



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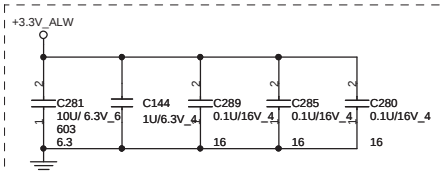
PROJECT : UM9 UMA

Size	Document Number	Rev
	Blank	1A
Date:	Monday, February 01, 2010	Sheet 28 of 51

UM3

(34) KSO[0..17]

(34) KS[0..7]



Place these caps close to ITE8502.

KSO17 57 KSO17/GPC5
KSO16 56 KSO16/GPC3
KSO15 55 KSO15/GPC3
KSO14 54 KSO14
KSO13 53 KSO13
KSO12 52 KSO12/SLCT
KSO11 51 KSO11/ERR
KSO10 46 KSO10/PE
KSO9 45 KSO9/BUSY
KSO8 44 KSO8/ACK
KSO7 43 KSO7/PD7
KSO6 42 KSO6/PD6
KSO5 41 KSO5/PD5
KSO4 40 KSO4/PD4
KSO3 39 KSO3/PD3
KSO2 38 KSO2/PD2
KSO1 37 KSO1/PD1
KSO0 36 KSO0/PD0

KS17 65 KS17
KS16 64 KS16
KS15 63 KS15
KS14 62 KS14
KS13 61 KS13/SLIN
KS12 60 KS12/INT
KS11 59 KS11/AFD
KS10 58 KS10/STB

ITE8502E LQFP-128L

KEYBOARD

ADC/DAC

ADC0/GPI0
ADC1/GPI1
ADC2/GPI2
ADC3/GPI3
ADC4/GPI4
ADC5/GPI5
ADC6/GPI6
ADC7/GPI7

DAC0/GPJ0
DAC1/GPJ1
DAC2/GPJ2
DAC3/GPJ3
DAC4/GPJ4
DAC5/GPJ5

PWM0/GPA0
PWM1/GPA1
PWM2/GPA2
PWM3/GPA3
PWM4/GPA4
PWM5/GPA5
PWM6/GPA6
PWM7/GPA7

LPC

IR/UART

LPC/FWH FLASH

EGPC

GPIO

VBAT1
VCC
VSTBY1
VSTBY2
VSTBY3
VSTBY4
VSTBY5
VSTBY6

HWPB
PAD T28
PAD T29
V ID1
PBAT_PRES#
INP
SIO_SLP_S5#
SIO_SLP_S5#

CRIT_TEMP_REP#
SIO_EXT_WAKE#
USB_LEFT_EN#
FAN1_DA
RSMRST#
PM_PWRBST#_R

BREATH_LED#
FAN1_PWM
PWM_VADJ
PAD T4
EC_BEEP
FAN1_TACH
PANEL_BKEN
LID_SW#
SIO_SLP_S3#

PAD T33
PAD T27
PAD T34
PAD T7
PAD T6
PAD T9
PAD T8
PAD T26
PAD T35

SUS_ON
KB_DET#
EC_FLASH_SPI_DO
EC_FLASH_SPI_DIN
EC_FLASH_SPI_CS#
EC_FLASH_SPI_CLK

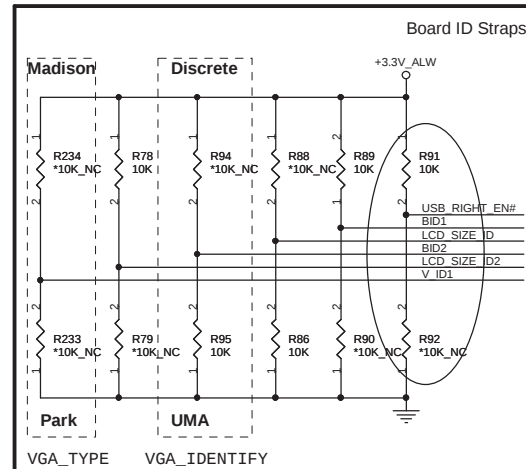
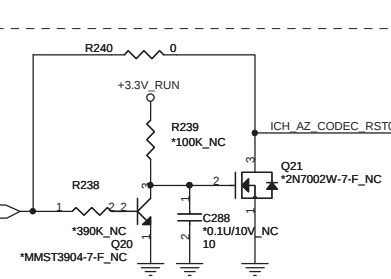
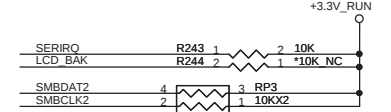
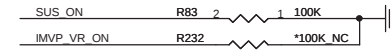
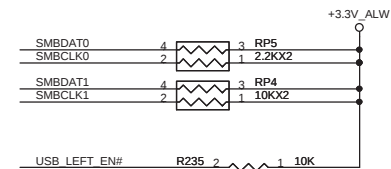
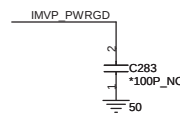
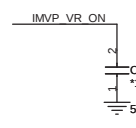
BID2
USB_RIGHT_EN#
USB_RIGHT_EN#
LCD_SIZE_ID
LCD_SIZE_ID2

BID2
USB_RIGHT_EN#
LCD_SIZE_ID
LCD_SIZE_ID2

ACAV_IN
BAT2_LED
AC_PRESENT
SYS_PWR_SW#
LCDVCC_TST_EN

ITE8502E
lqfp128-16x16-4

Close to PU9



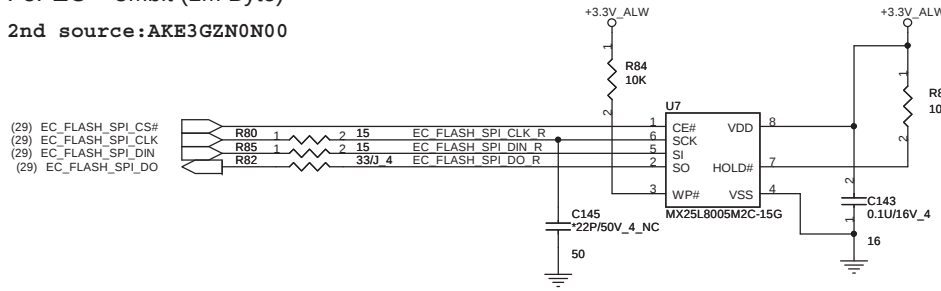
	LCD_SIZE_ID (99)	LCD_SIZE_ID2 (107)
13.3"	0	0
14"	1	0
17"	0	1

BID1	BID0	UM9(UMA)	UM9C (Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	OT (A00)	OT (A00)
0	0	(A01)	(A01)

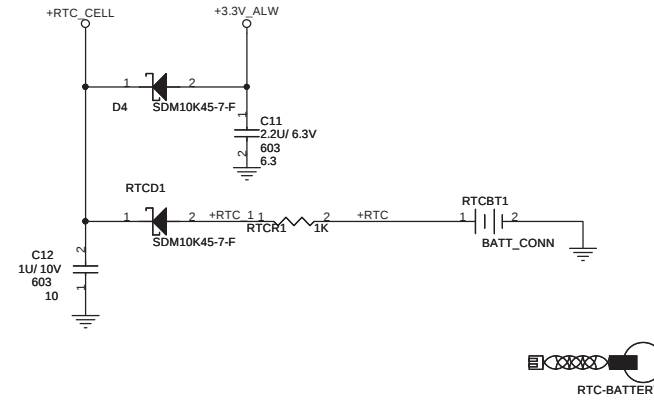
UM3

For EC 8Mbit (1M Byte)

2nd source:AKE3GZN0N00



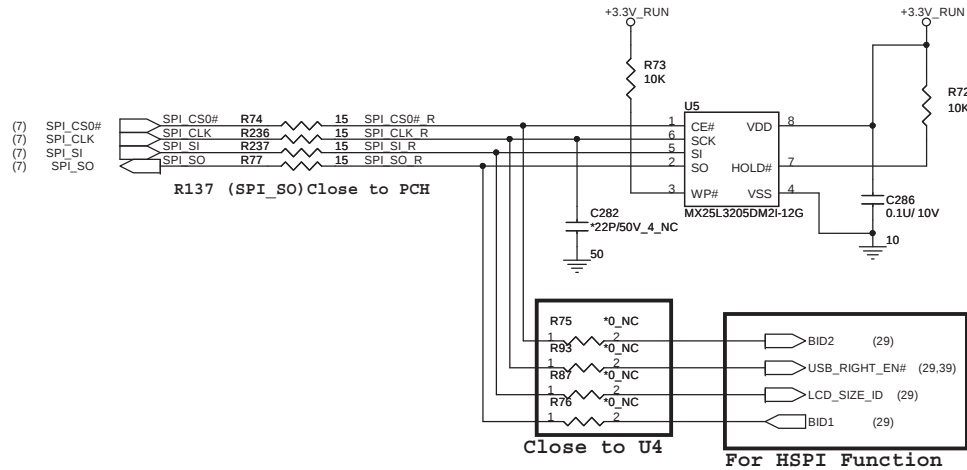
RTC BATTERY



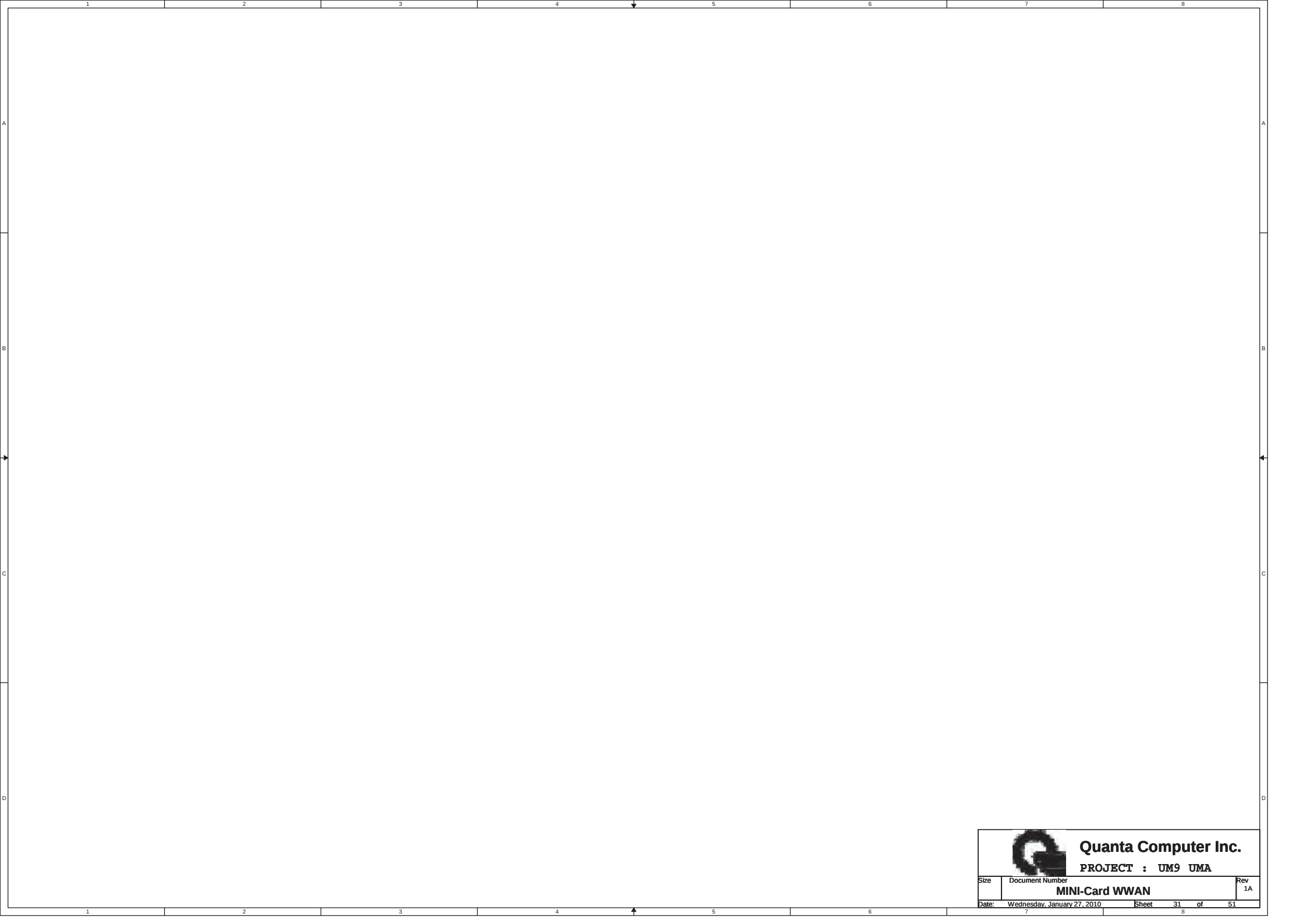
For PCH

32Mbit (4M Byte)

2nd source:AKE39ZP0N00



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PROJECT : UM9 UMA

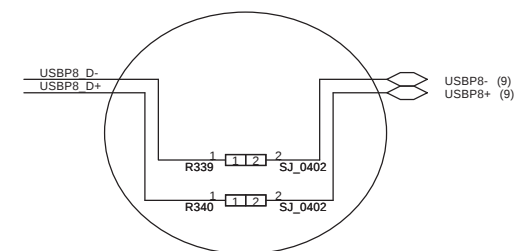
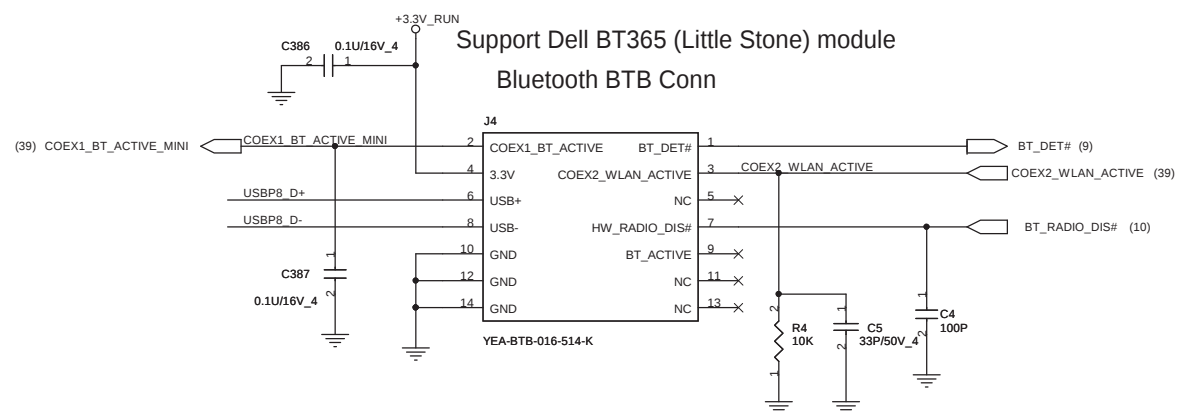


Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
MINI-Card WWAN		1A
Date: Wednesday, January 27, 2010	Sheet	31 of 51

WLAN To DB



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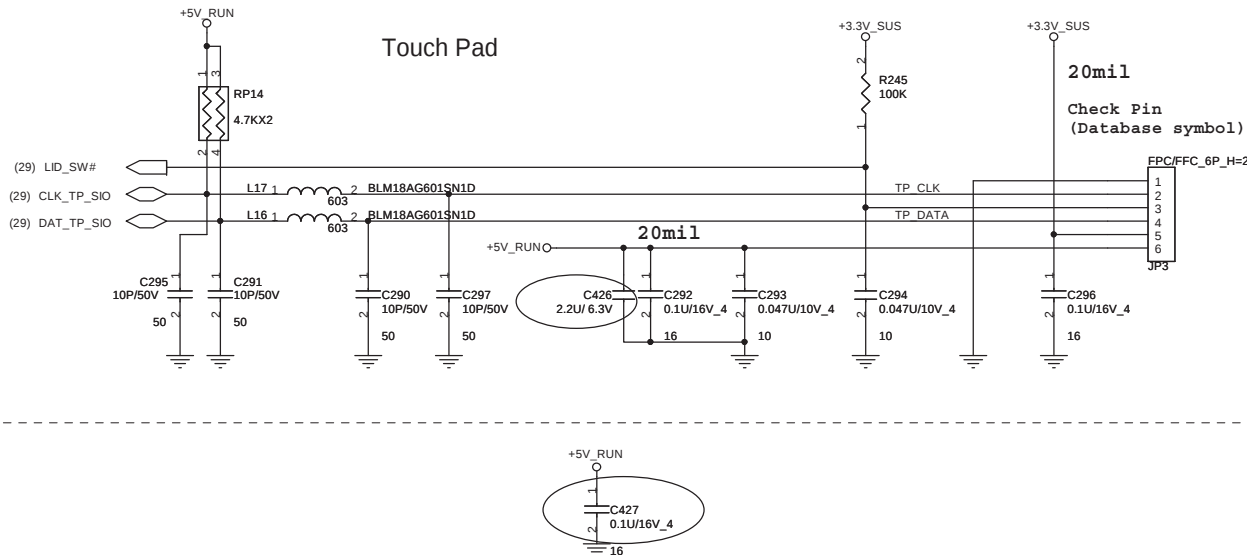
PROJECT : UM9 UMA

Size	Document Number	Rev
	MINI-Card WLAN / BT	1A
Date:	Monday, February 01, 2010	Sheet 32 of 51

1	2	3	4	5	6	7	8
A							
B							
C							
D							

UM3

Touch Pad

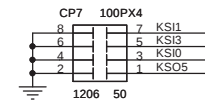
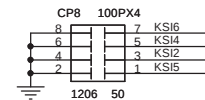
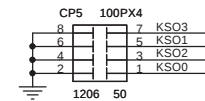
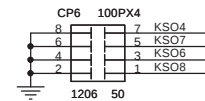
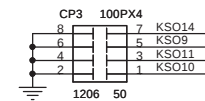
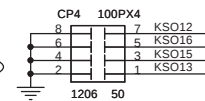
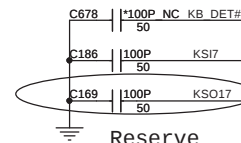
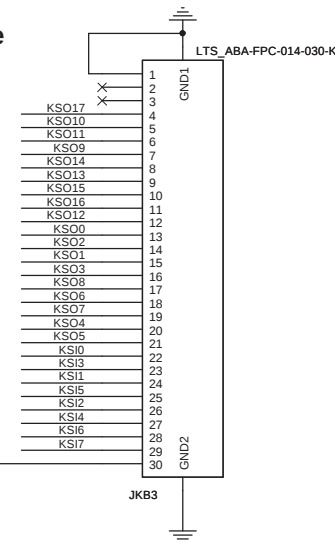


KEYBOARD CONNECTOR

Top side

(29) KSO[0..17]
(29) KSI[0..7]

(29) KB_DET#

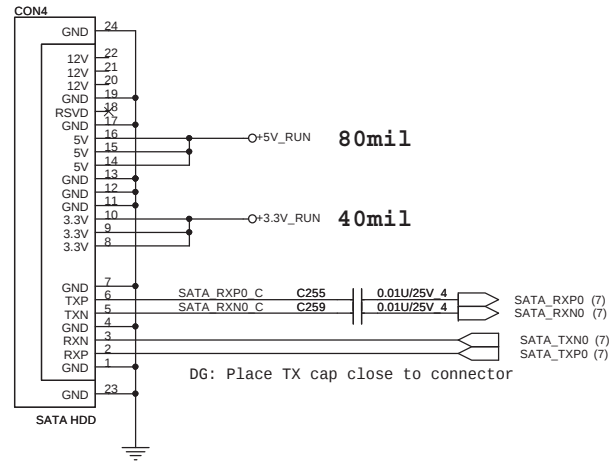


100P CAPS CLOSE TO JKB3

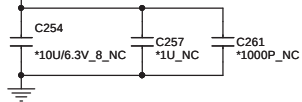


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PROJECT : UM9 UMA

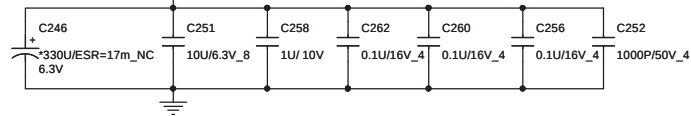
SATA Connector.



+3.3V_RUN Place caps close to connector.

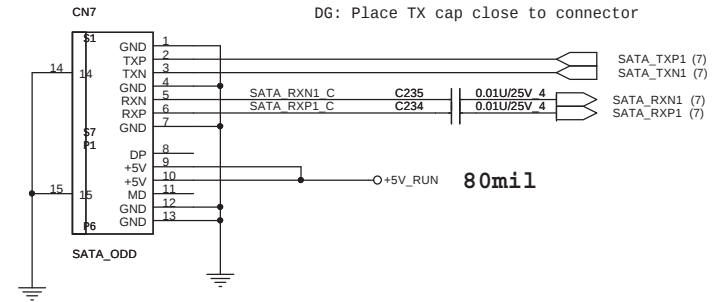


+5V_RUN Place caps close to connector.

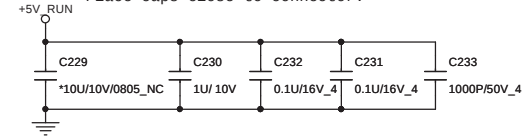


UM3

ODD Connector



Place caps close to connector.

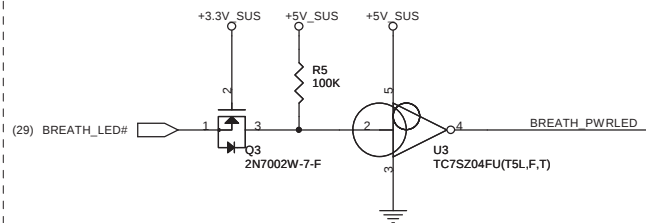


Quanta Computer Inc.

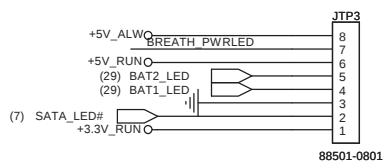
PROJECT : UM9 UMA

Size	Document Number	Rev
	SATA (HDD&CD_ROM)	1A
Date:	Monday, February 01, 2010	Sheet 35 of 51

Power

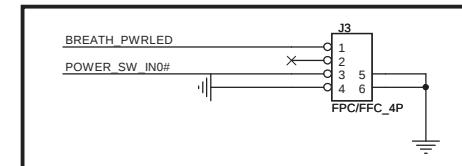


Check Connector P/N and footprint

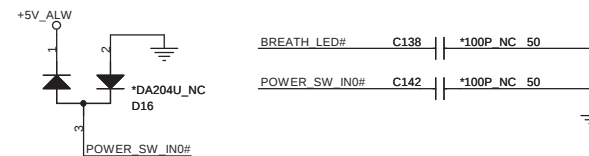
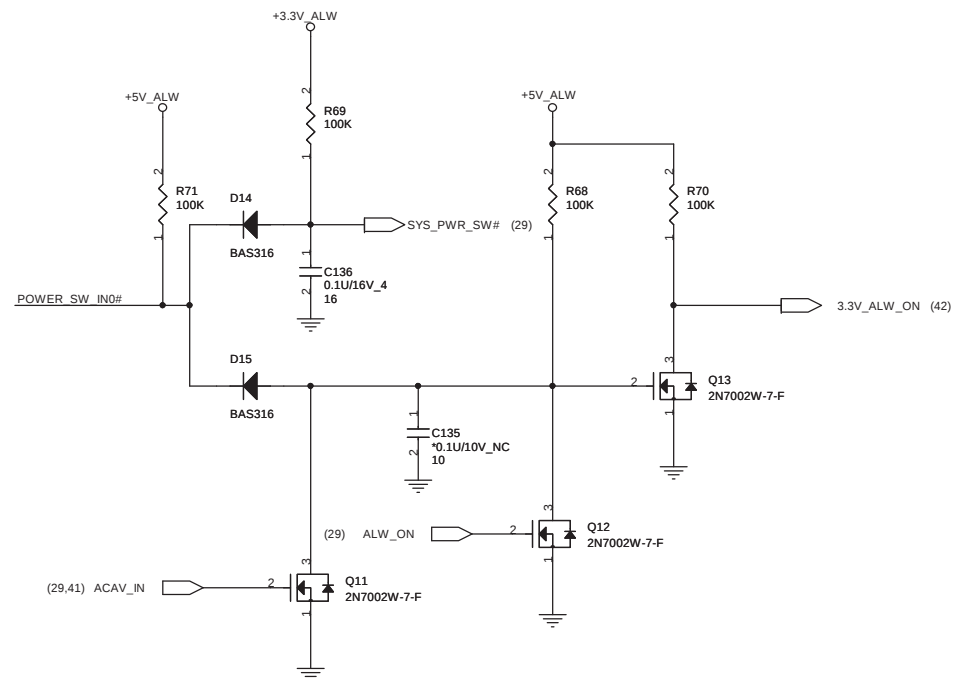


UM3

Power button Cable



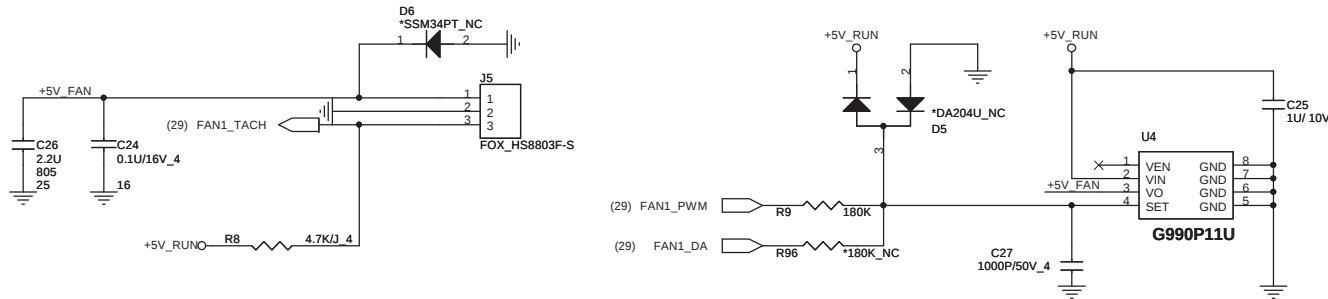
3VALW ON POWER LOGIC



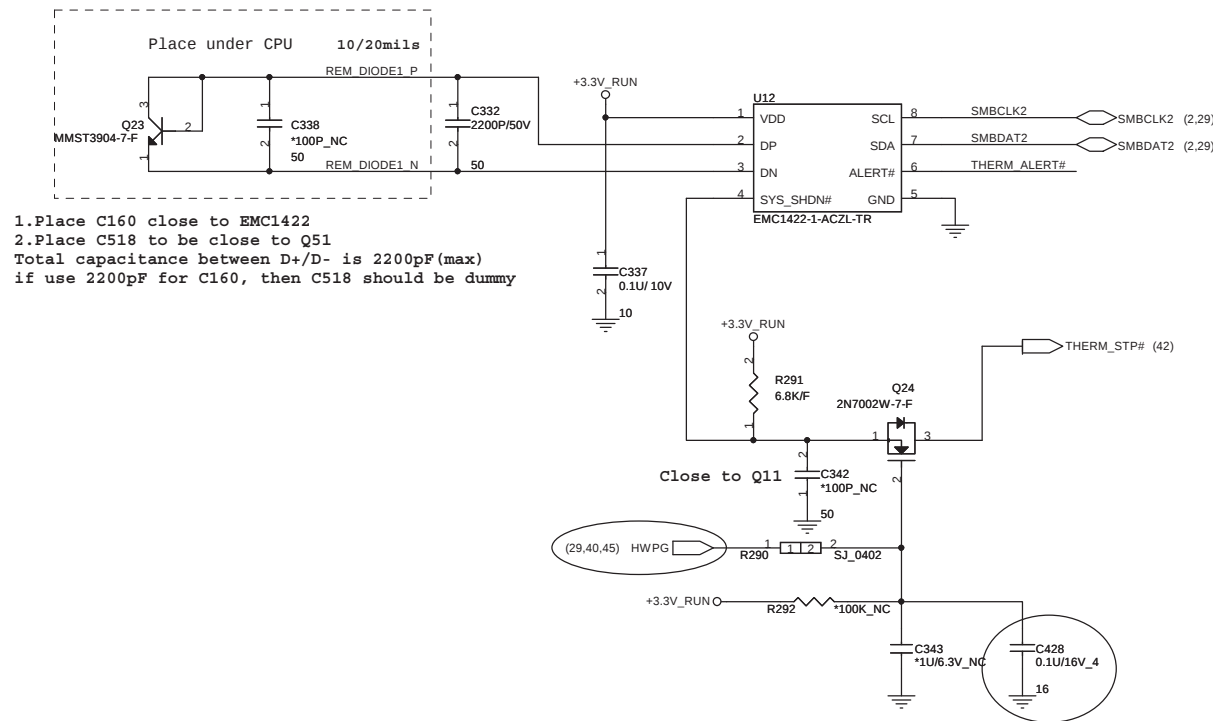
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PROJECT : UM9 UMA

FAN CONTROL

6/23 COPY FROM RM6



UM3



- 1.Place C160 close to EMC1422
 - 2.Place C518 to be close to Q51
- Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C160, then C518 should be dummy

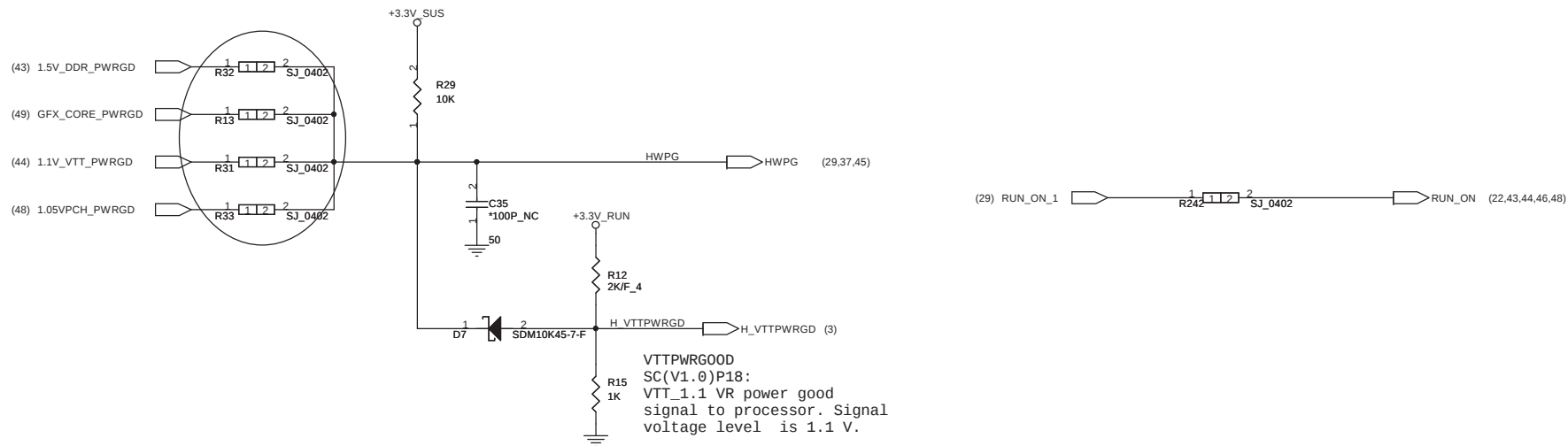
OTP 85 degree C



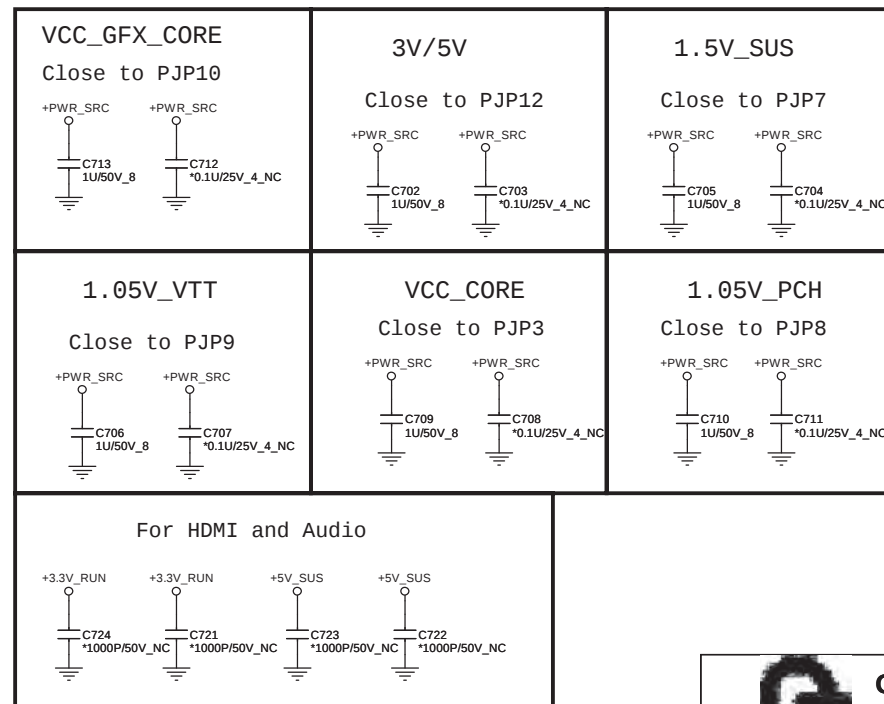
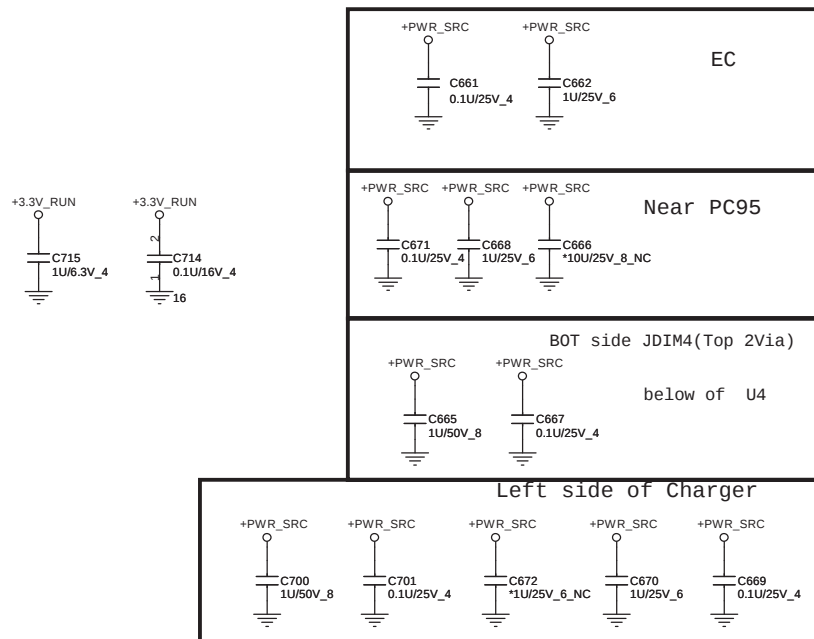
Quanta Computer Inc.
PROJECT : UM9 UMA



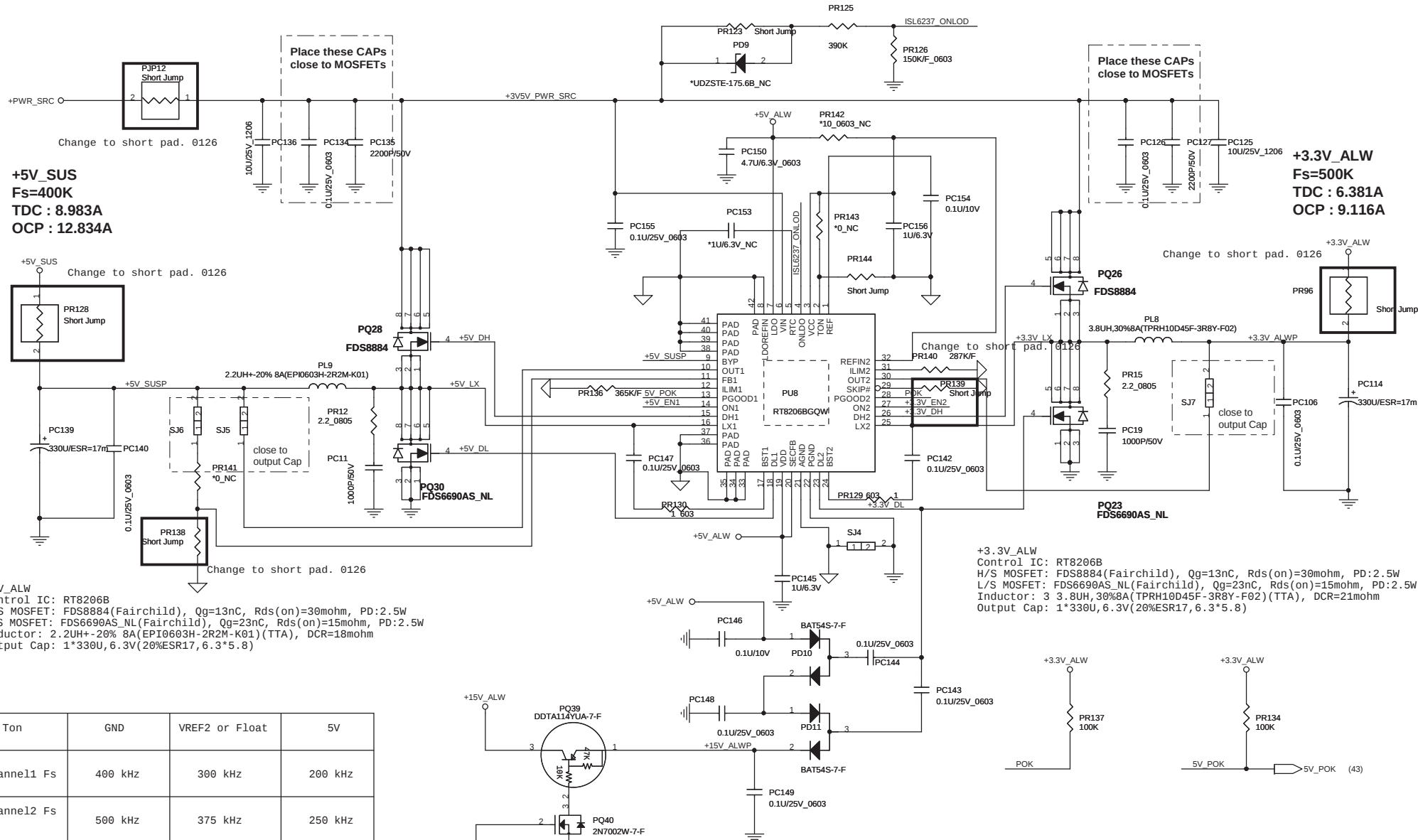
UM3



For FDI bus noise

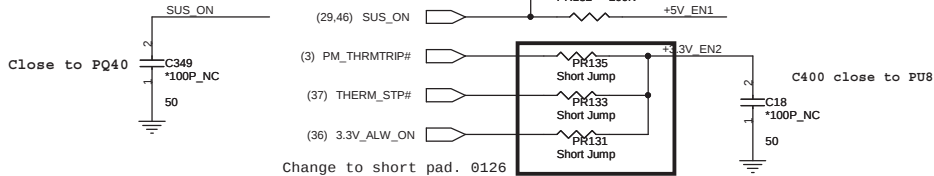


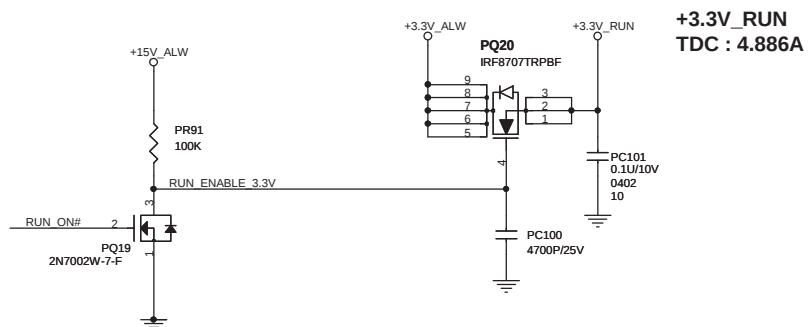
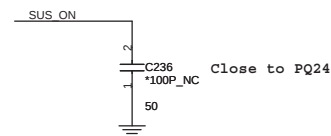
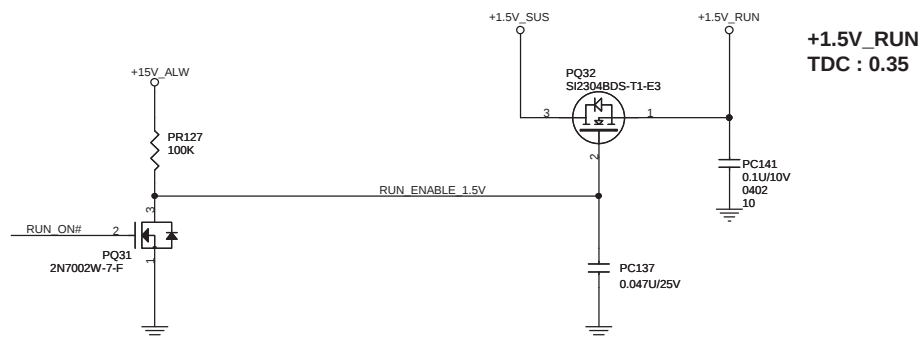
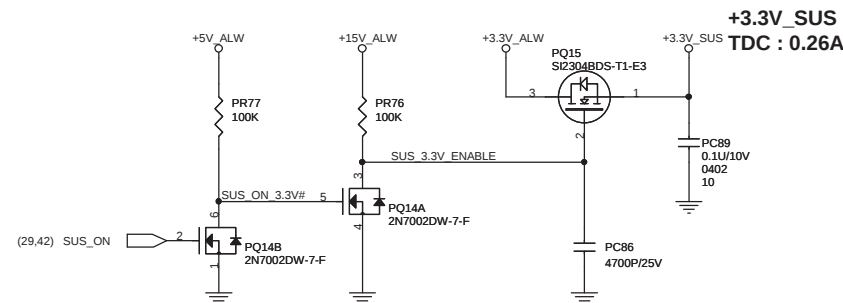
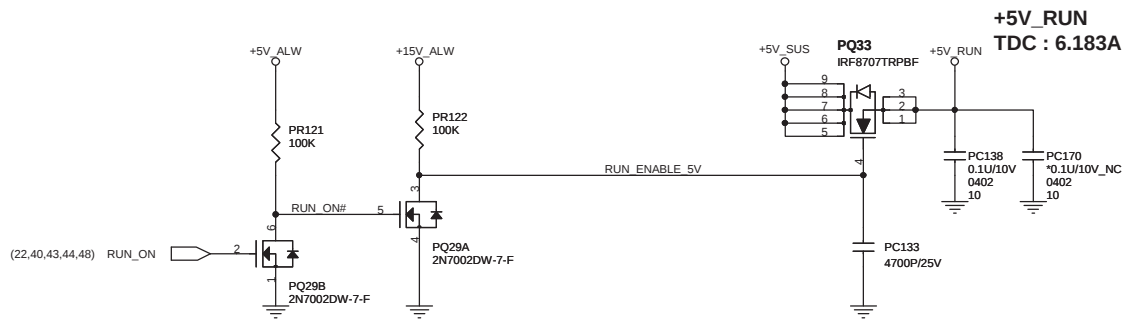




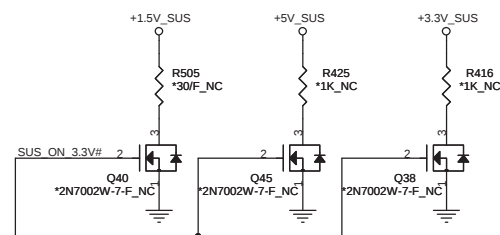
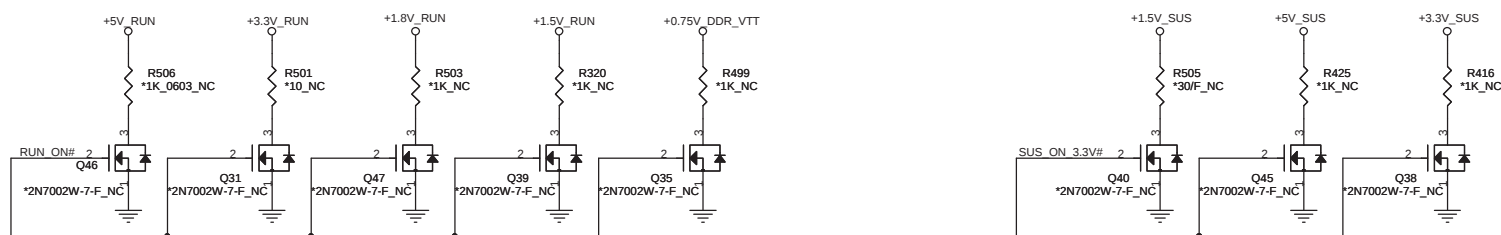
+5V_ALW
Control IC: RT8206B
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
Inductor: 2.2uH+-20% 8A(EPI0603H-2R2M-K01)(TTA), DCR=18mohm
Output Cap: 1*330u, 6.3V(20%ESR17, 6.3*5.8)

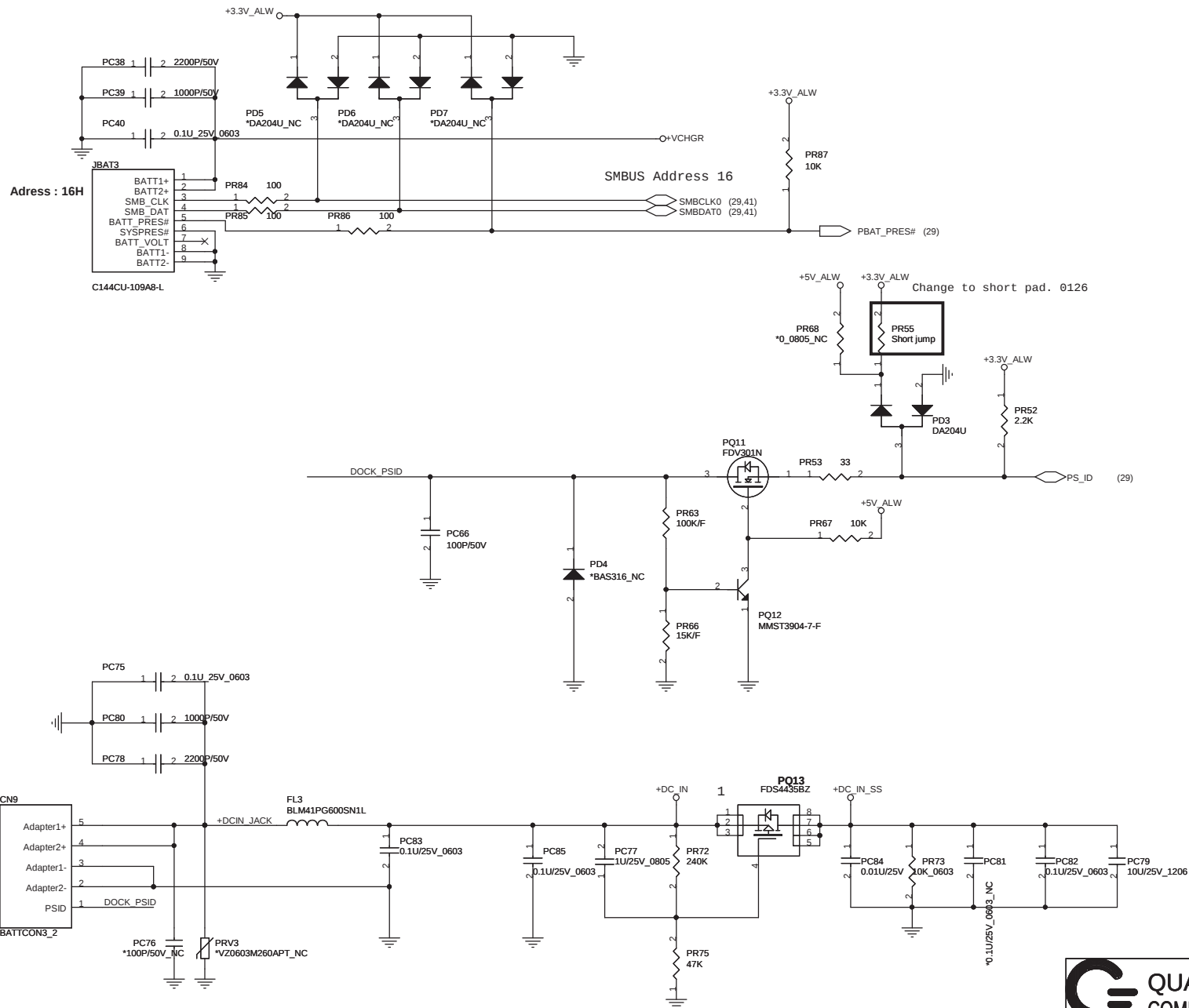
Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz



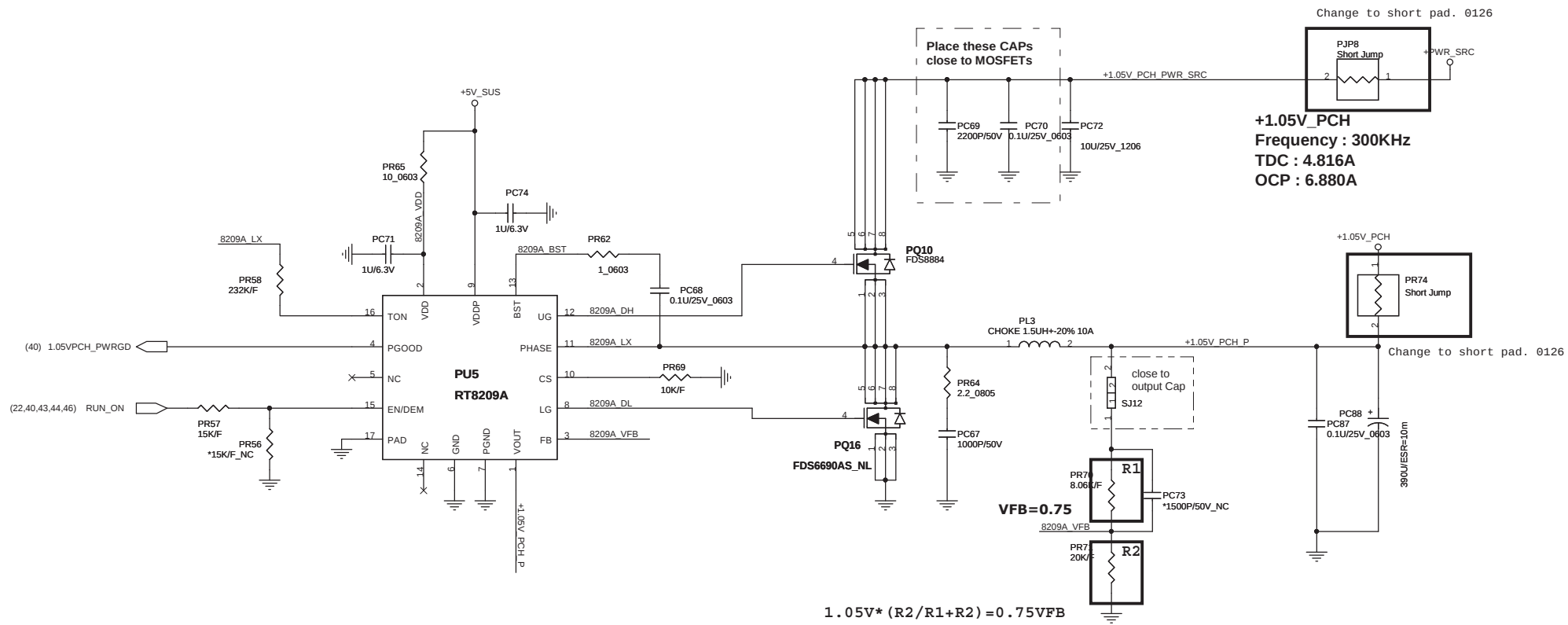


Reserve discharge path





Title		
DCIN, BATT CONNECTOR		
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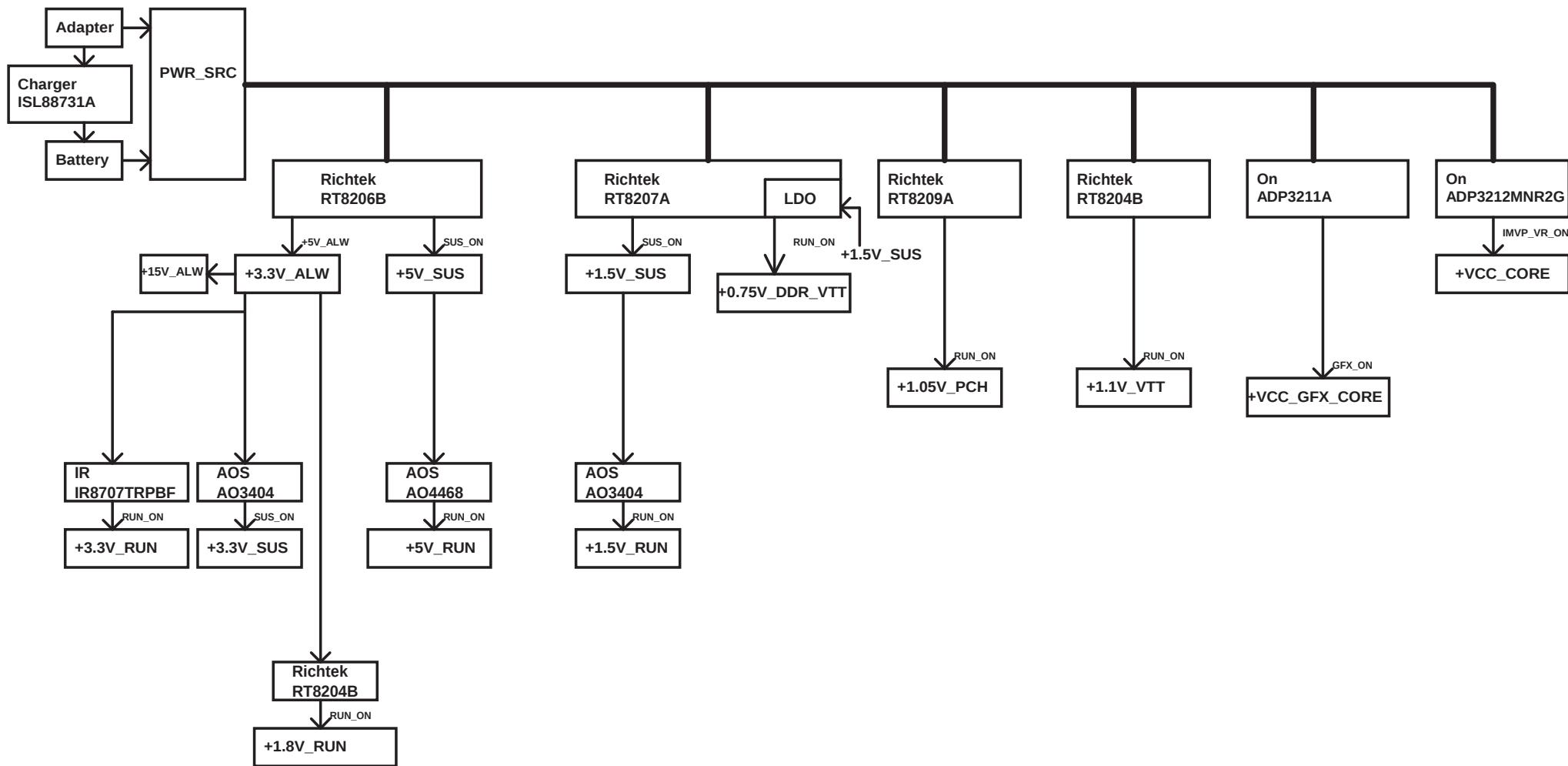


+1.05V_PCH
Frequency : 300KHz
TDC : 4.816A
OCF : 6.880A

$$1.05V * (R2 / (R1 + R2)) = 0.75V_{FB}$$

+1.05V_PCH
 Control IC: RT8209A
 H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
 L/S MOSFET: FDS6690AS_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
 Inductor: 1.5uH+-20% 9A (10D40F-1R5M)(TTA), DCR=10.5mohm
 Output Cap: 1*390U, 2.5V(20%, 105C, 6.3*5.8), ESR=10mohm

Title		
+1.05V_PCH(RT8209A)		
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	UM9 UMA	2B
Date:	Monday, February 01, 2010	Sheet 48 of 51



FM9 Power Design Block Diagram 2009/02/25

