

Compal Confidential

Dali & Astro BKA40/BKA50/BKD40/BKD50 MB Schematic Document

LA-D822P
Rev: 1.0 (A00)
2016.06.06

UC1 KBL_15W_B@
SA0000A382L
KBL U SR2VN
S IC FJ8067702739738 SR2VN H0 2.4G A31!

UC1 KBL_15W_I5@
SA0000A372L
KBL U SR2VL
S IC FJ8067702739739 SR2VL H0 2.5G A31!

UC1 KBL_15W_I7@
SA0000A342L
KBL U SR2VM
S IC FJ8067702739740 SR2VM H0 2.7G A31!

UC1 KBL_15W_2+1@
SA00009QM0L
KBL U QKKO
S IC A31 FJ8067702739920 QKKQ G0 1.7G

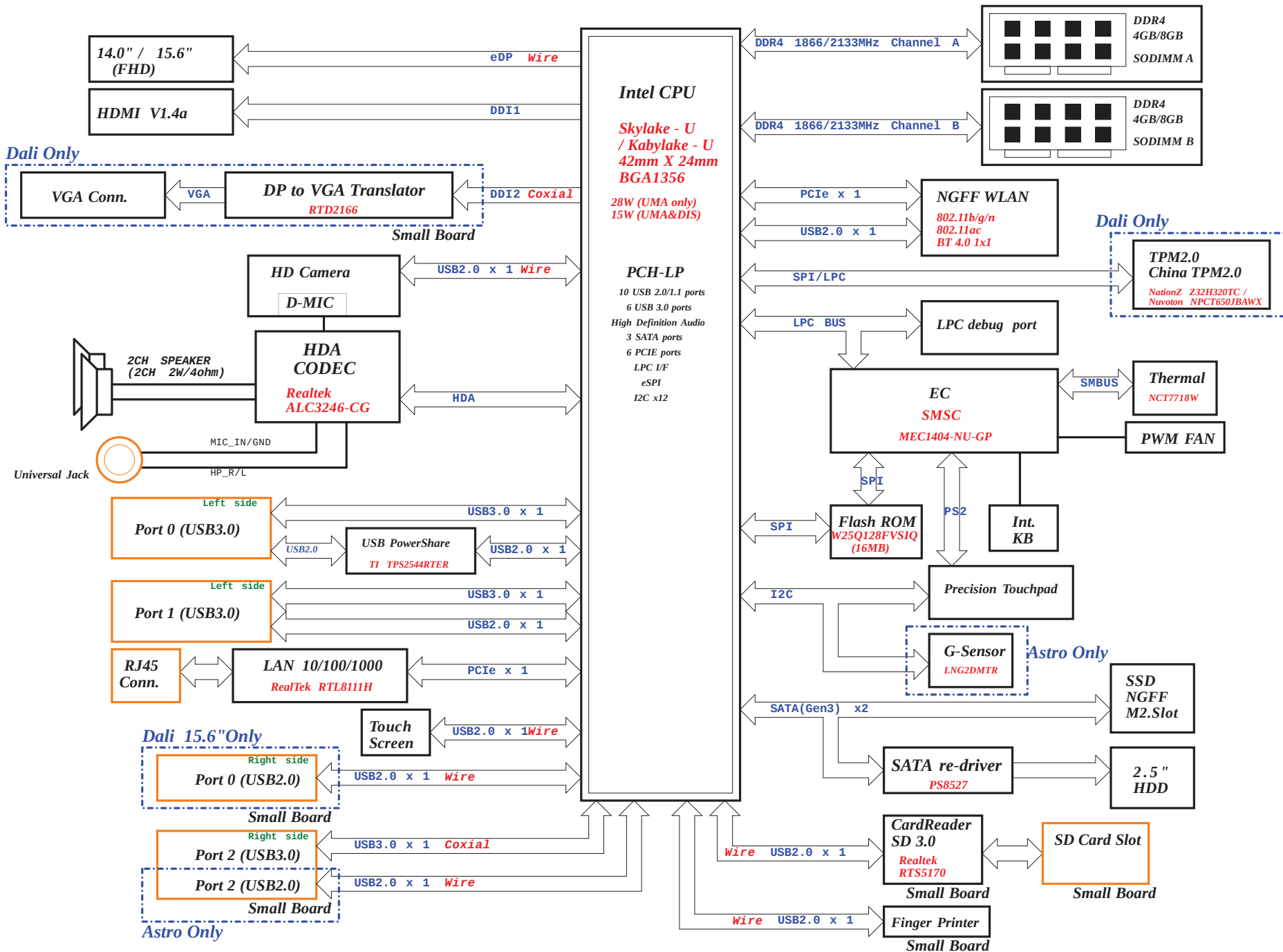


UC1 SKL_15W@
SA000092N4L
SKL U I3-6100U
S IC FJ8066201931104 SR2EU D1 2.3G A31!

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		1.0	
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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+RTC_CELL +RTC_VCC +3VLP +19VB	+1.0V_PRIM +1.0V_MPHYPLL +5VALW +3VALW +3.3V_ALW_DSW +1.8V_PRIM	+1.0V_VCCST +1.2V_DDR +2.5V_MEM +3VALW_PCH	+1.0VS_VCCIO +1.0V_VCCSTG +VCC_GT +VCC_SA +VCC_CORE +GPU_CORE +5VS +3VS +1.8VS +0.6V_DDR_VTT
S0	ON	ON	ON	ON
S3	ON	ON	ON	OFF
S4&S5 / AC	ON	ON	OFF	OFF
S4&S5 / DC	ON	OFF	OFF	OFF

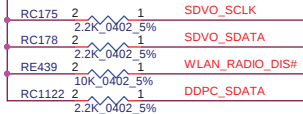
Board ID & Model ID table

Item	Pull-down(K ohm)	Pull-up (K ohm)	Voltage	Board ID/Model ID
1	100	10.0	3.000	EVT(X00)
2	100	13.7	2.902	DVT1(X01)
3	100	17.8	2.801	DVT2(X02)
4	100	22.1	2.703	Pilot(A00)
5	100	27.0	2.598	
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	

USB PORT#	DESTINATION
1	USB3.0 Port0
2	USB3.0 Port1
3	USB3.0 Port2 (IO Board)
4	USB2.0 Port0
5	HD CAM
6	Card Reader
7	Touch Screen
8	BT
9	Finger Printer
10	N/A

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				USB3.0 Port0
USB3.0-2	SSIC-1			USB3.0 Port1
USB3.0-3	SSIC-2			USB3.0 Port2 (IO Board)
USB3.0-4				N/A
USB3.0-5		PCIE-1		N/A
USB3.0-6		PCIE-2		N/A
		PCIE-3		N/A
		PCIE-4		N/A
		PCIE-5		WLAN
		PCIE-6		GLAN
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	N/A
		PCIE-9		N/A
		PCIE-10		N/A
		PCIE-11	SATA-1*	N/A
		PCIE-12	SATA-2	SATA SSD

+3VS



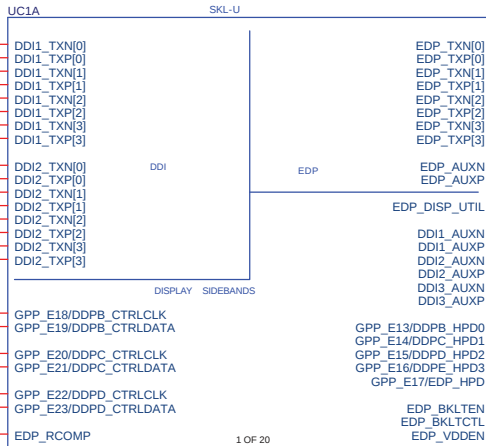
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<26> CPU_DP1_P2
<26> CPU_DP1_N1
<26> CPU_DP1_P1
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<26> CPU_DP1_P0
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<26> CPU_DP1_P3

<33> SOC_DP2_N0
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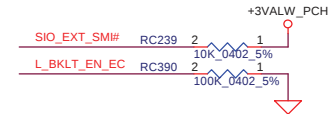
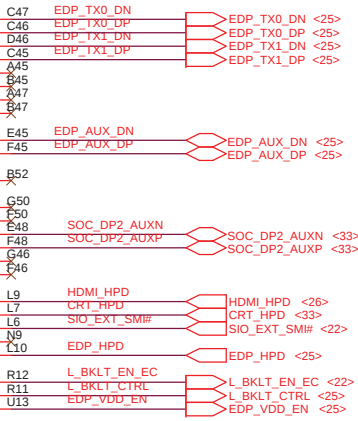
<26> SDVO_SCLK
<26> SDVO_SDATA

+1.0VS_VCCIO 1 24.9 0402 1% RC2 EDP_COMP

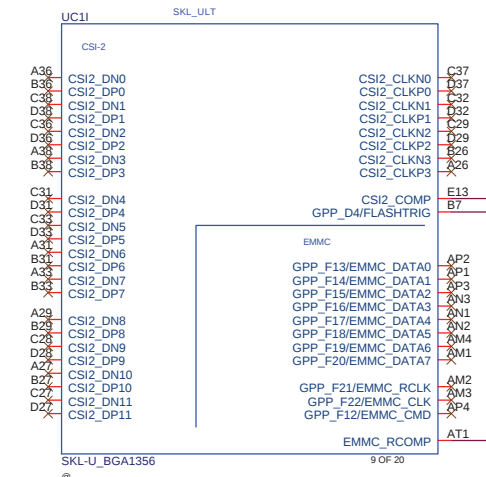
COMPENSATION PU FOR eDP
CAD Note:Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.



SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0



+3VALW_PCH



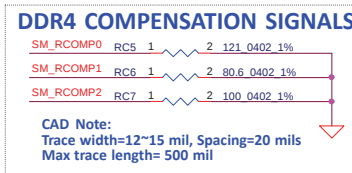
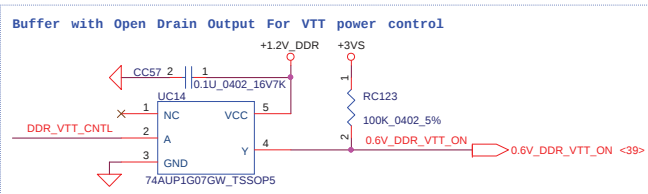
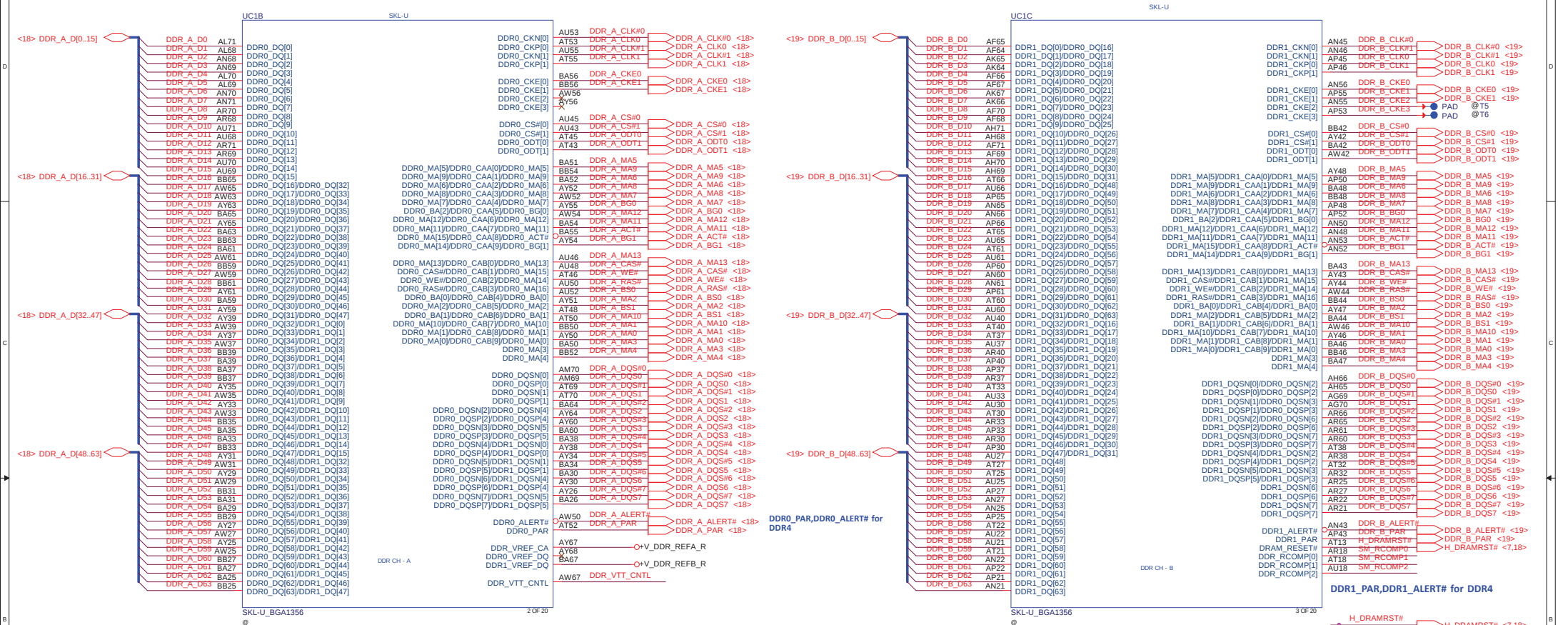
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DDR4, Ballout for B2B(Interleave)



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MCP(2/14)DDR4

LA-D822P

Rev 1.0

Title

Size

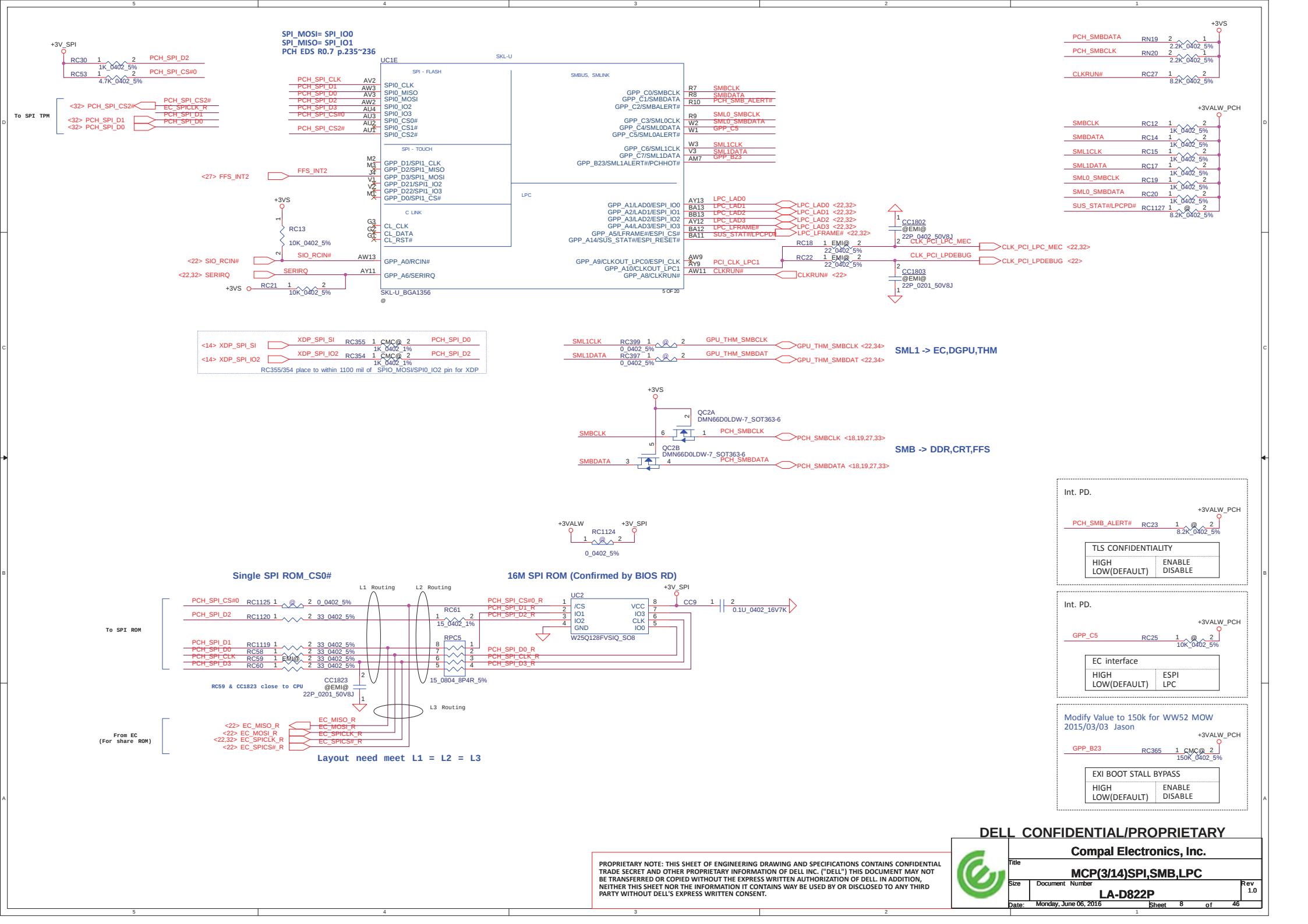
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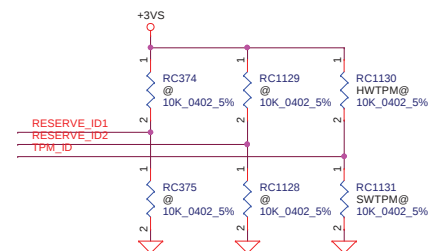
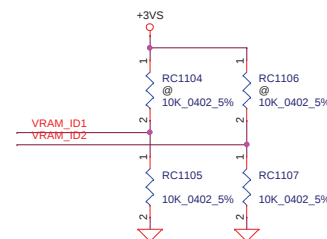
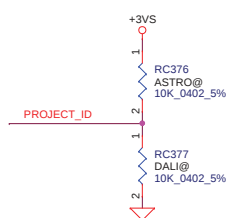
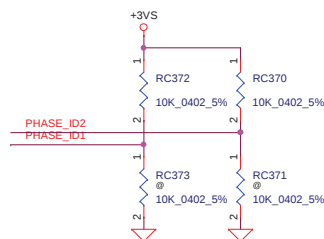
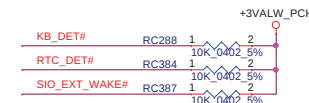
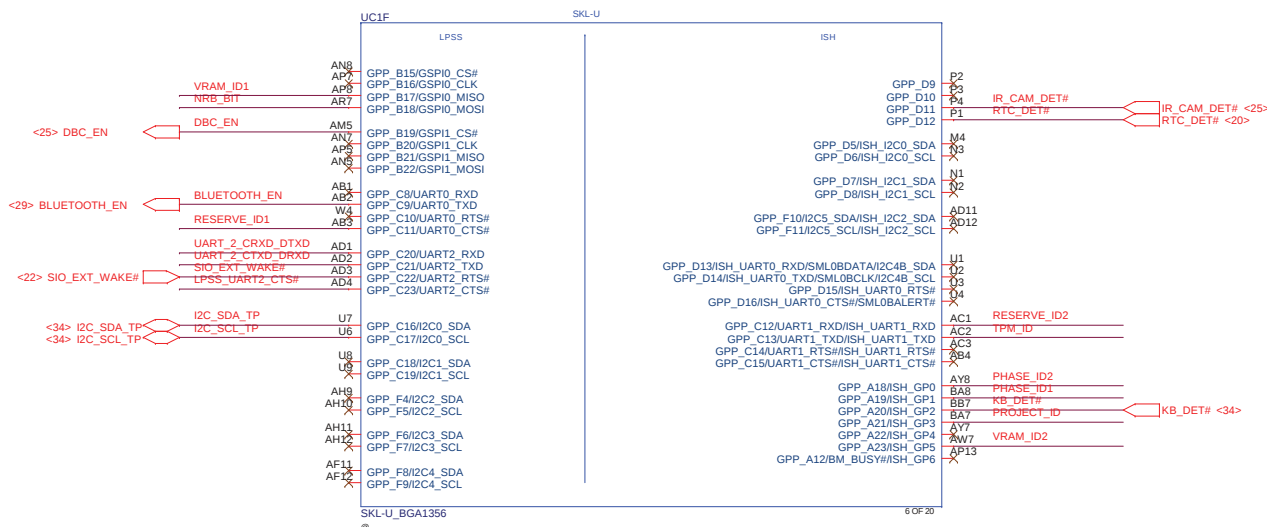
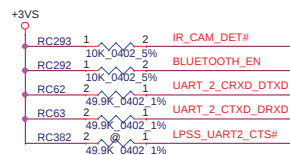
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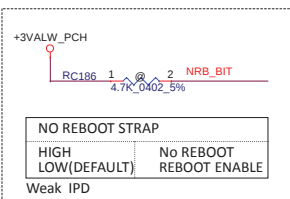
PHASE ID	PHASE ID1 (GPP_A19)	PHASE ID2 (GPP_A18)
EVT	0	0
DVT1	0	1
DVT2	1	0
Pilot	1	1

PROJECT ID	PROJECT ID (GPP_A21)
Dali	0
Astro	1

VRAM ID (PCBA VRAM Size Config.)	VRAM ID2 (GPP_A23)	VRAM ID1 (GPP_B17)
UMA	0	0
2G	0	1
4G	1	0
Reserved	1	1

PROJECT ID	TPM ID (GPP_C13)
SW_TPM	0
HW_TPM	1

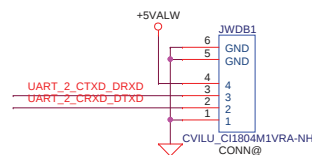
RESERVE ID	RESERVE ID1 (GPP_C11)	RESERVE ID2 (GPP_C12)



NO REBOOT STRAP	
HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE
Weak IPD	

Win7 Debug solution

Option 2 : For Open Chassis Platforms



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MCP(4/14)GSPi,I2C,UART,ISH

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3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U



- There are 16 HSIO lanes on SKL PCH-LP U Series, supporting the following port configurations:
- Up to 12 PCIe* lanes (multiplexed with USB 3.0 ports, SATA Ports)
 - Only a maximum of 6 PCIe* ports (or devices) can be enabled at any time.
 - Ports 1-4, Ports 5-8, and Ports 9-12, can each be individually configured as <4x1, 2x2, 1x2 + 2x1, or 1x4.
 - Up to 3 SATA ports (multiplexed with PCIe*)
 - SATA Port 1 has the flexibility to be mapped to either PCIe* Port 8 or Port 11.
 - Up to 6 USB 3.0 ports (multiplexed with PCIe*)
 - USB Dual Role (OTG) capability is available on USB 3.0 Port 1
 - One SSIC x1 port is multiplexed with USB 3.0 Port 2
 - One GbE line
 - GbE can be mapped into one of the PCIe* Ports 3-5 and Ports 9-10.
 - When GbE is enabled, there can be at most up to 5 PCIe* ports enabled.
 - Devices can be x2 or x4
 - Devices can be implemented on PCIe Ports 5-8 and Ports 9-12

WLAN

<29> PCIE_PRX_WLANTX_N5
<29> PCIE_PRX_WLANTX_P5
<29> PCIE_PTX_C_WLANRX_N5
<29> PCIE_PTX_C_WLANRX_P5

LAN

<30> PCIE_PRX_LANTX_N6
<30> PCIE_PRX_LANTX_P6
<30> PCIE_PTX_C_LANRX_N6
<30> PCIE_PTX_C_LANRX_P6

HDD

<27> SATA3_PRX_HDDTX_N0
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<27> SATA3_PTX_HDDRXX_N0
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SSD

<28> SATA3_PRX_SSDTX_N2
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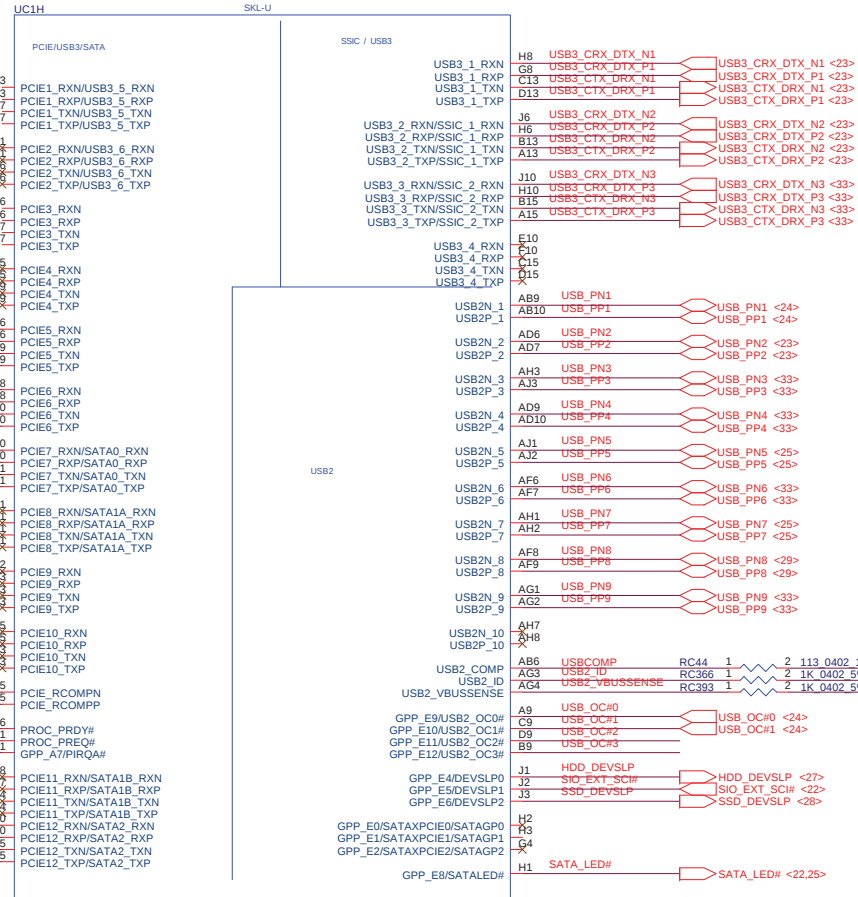


Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

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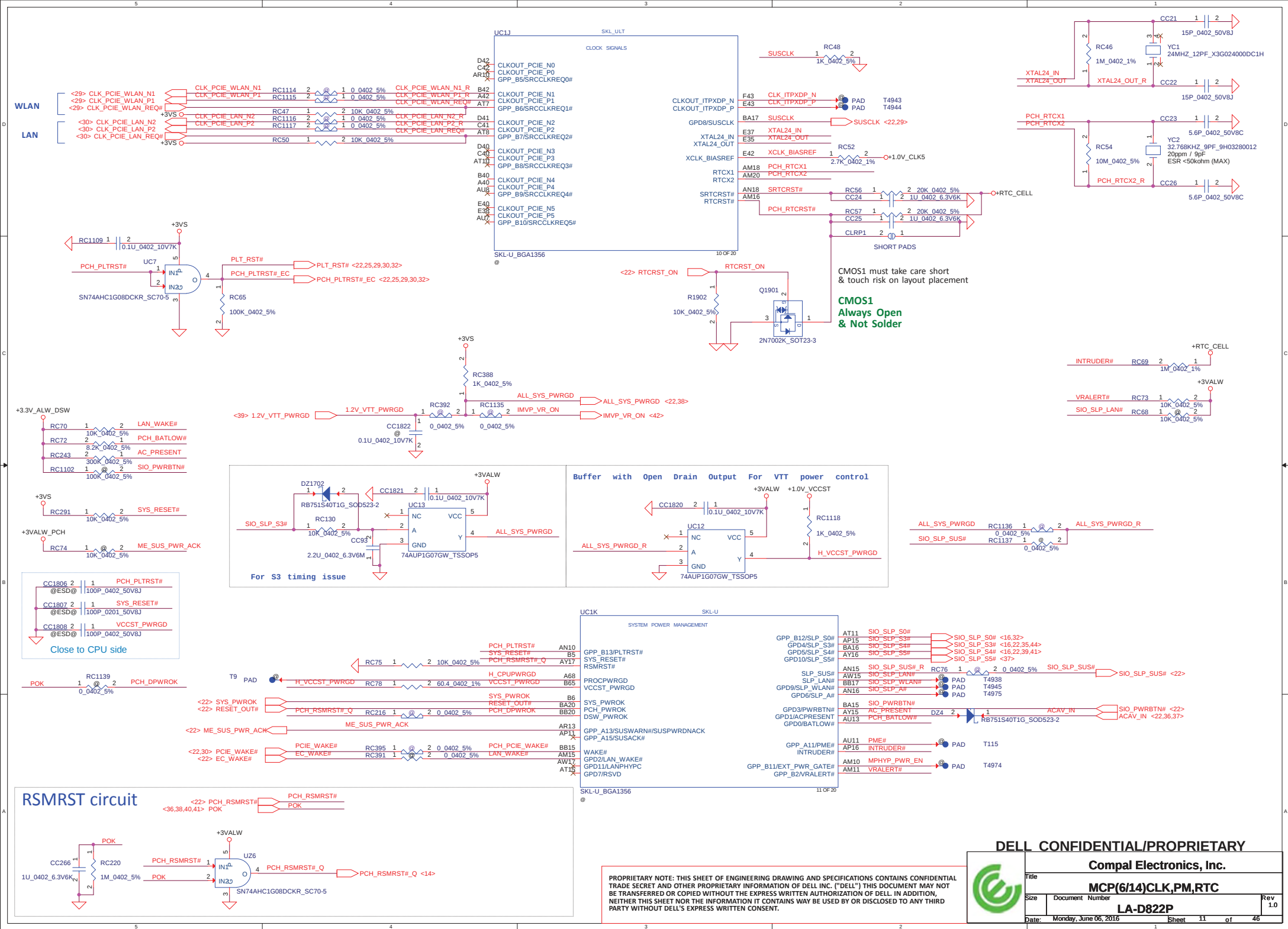
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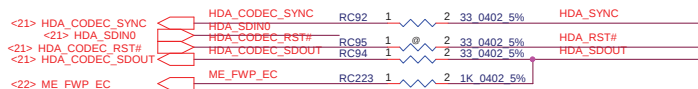
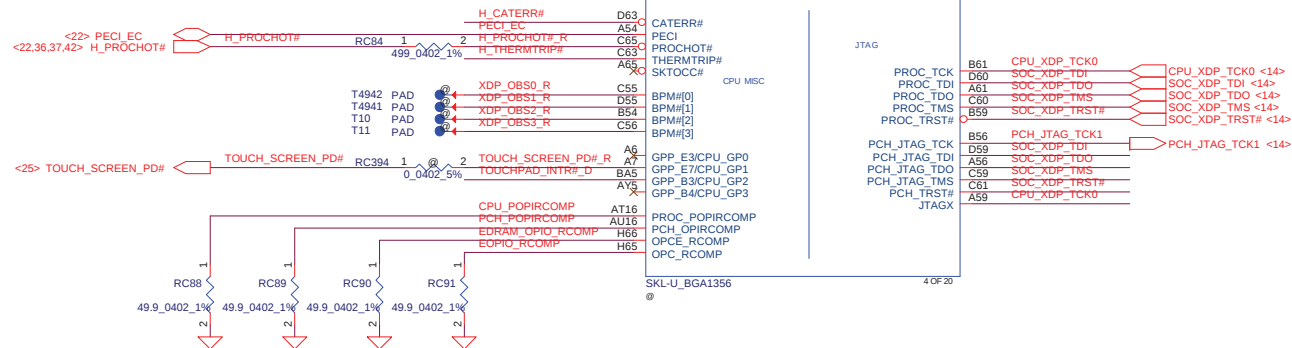
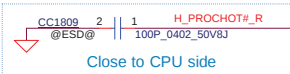
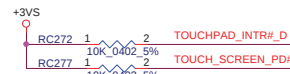
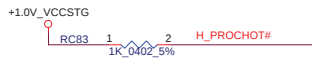
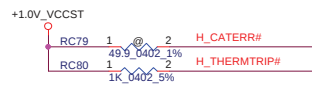
MCP(5/14)PCIE,USB,SATA

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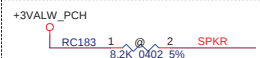
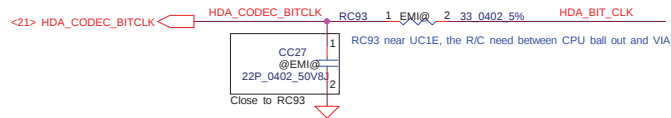
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ME_FWP_EC

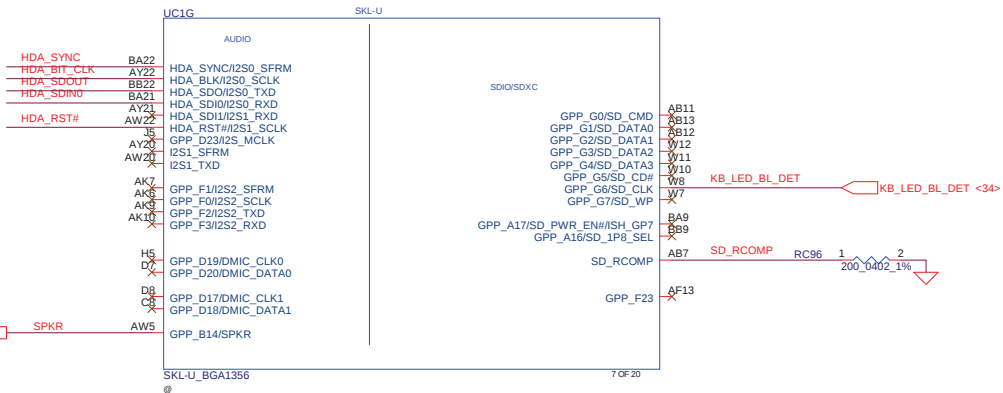
- LOW=ENABLE--> ME lock can't update ME
- HIGH=DISABLE--> ME unlock can update ME



TOP SWAP STRAP	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

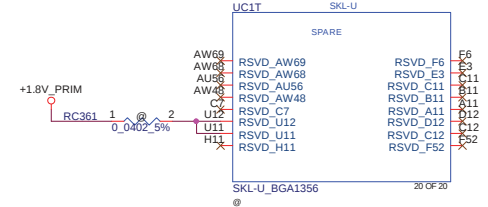
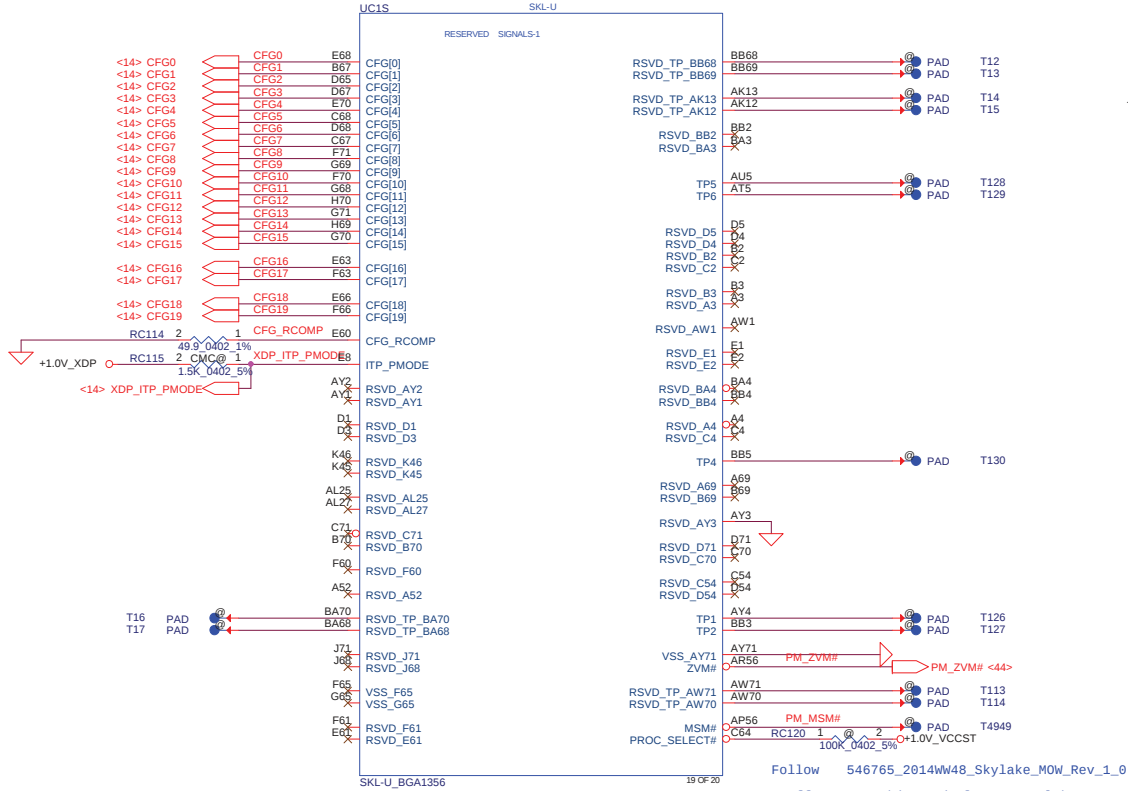
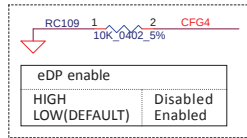
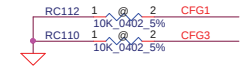
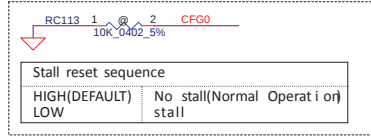


Flash Descriptor Security override	
HIGH	DISABLE
LOW(DEFAULT)	ENABLE



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CFG[2][5][6][7] for SKYLAKE-H CPU CFG strap pin



For 2+3e Solut i on

PM_VZM#
Zero Voltage Mode: Control Signal to OPC VR, when low OPC VR output is 0V.

PM_MSM#
Minimum Speed Mode: Control signal to VccEOPiO VR (connected only in 2 VR solut i onf α OPQ.

Follow 546765_2014W48_Skylake_M0W_Rev_1_0
Stuff 100k(RC184) for Cannonlake.
Un-stuff 100k(RC184) for Skylake

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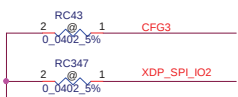
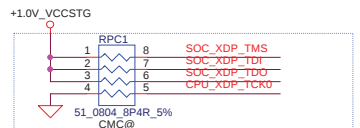
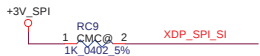
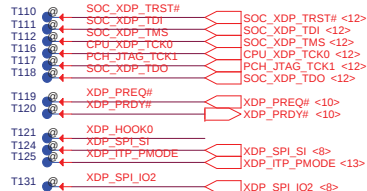
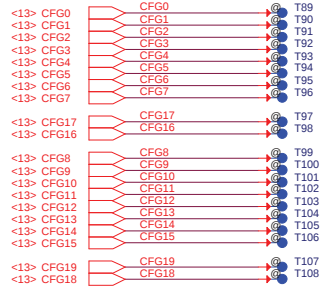
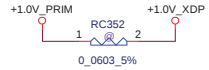


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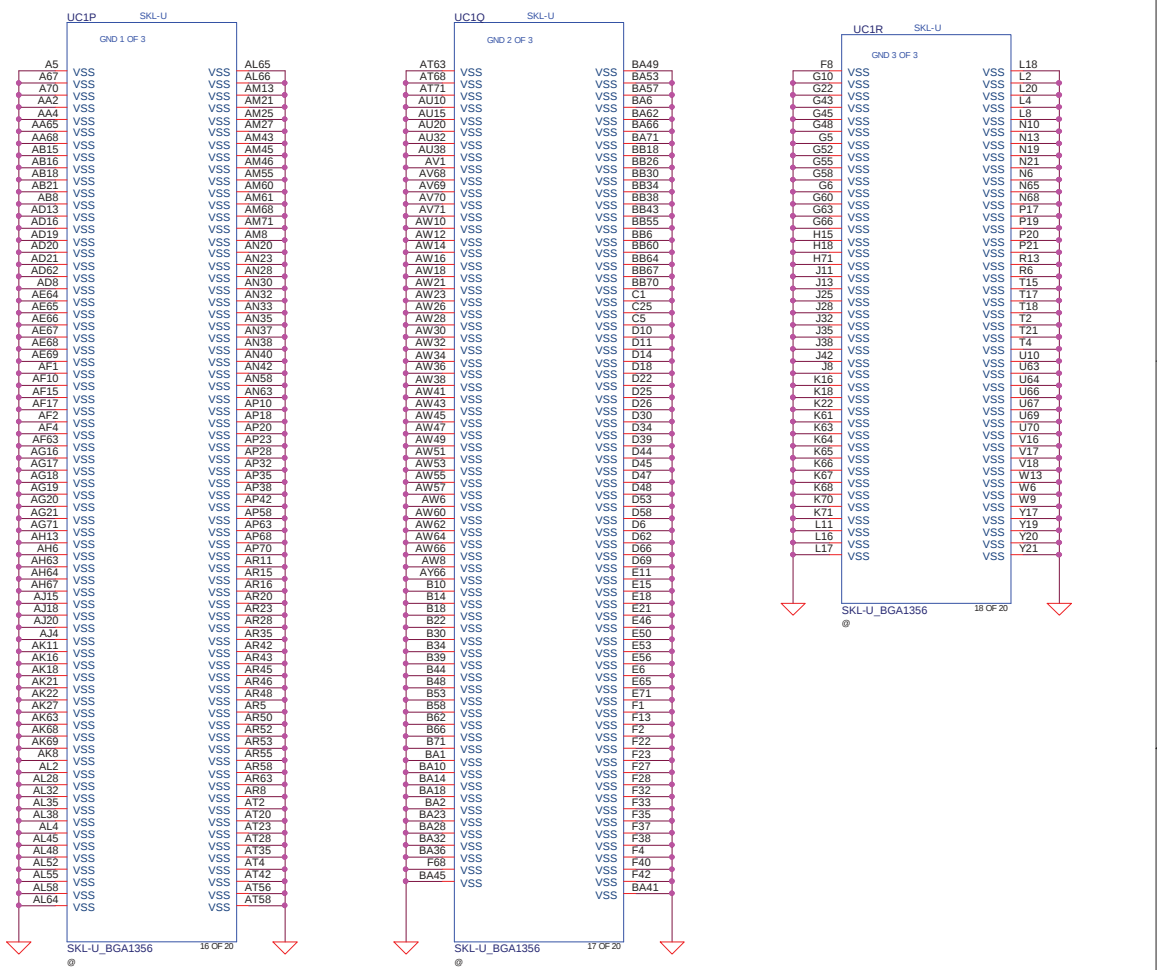
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PRIMARY CMC CONN



CFG3 = XDP_PRSENT_CPU
XDP_SPI_IO2 = XDP_PRSENT_PCH



- For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.
- R1: not populated
 - R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
 - R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption
- For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.
- R1: populated
 - R2, R3: not populated
 - R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values
- For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

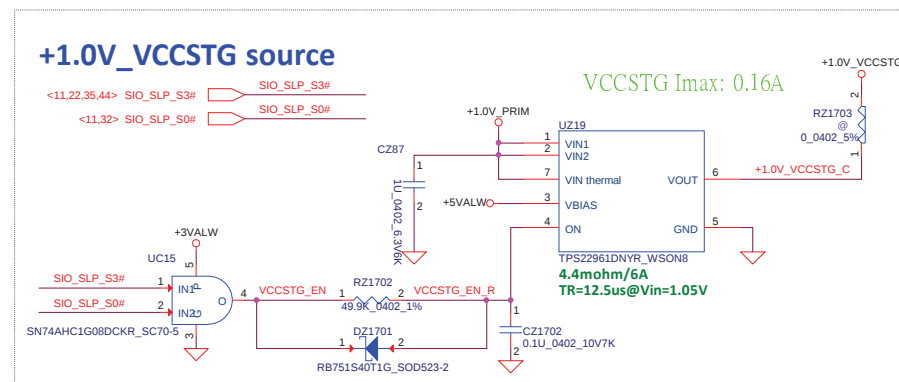
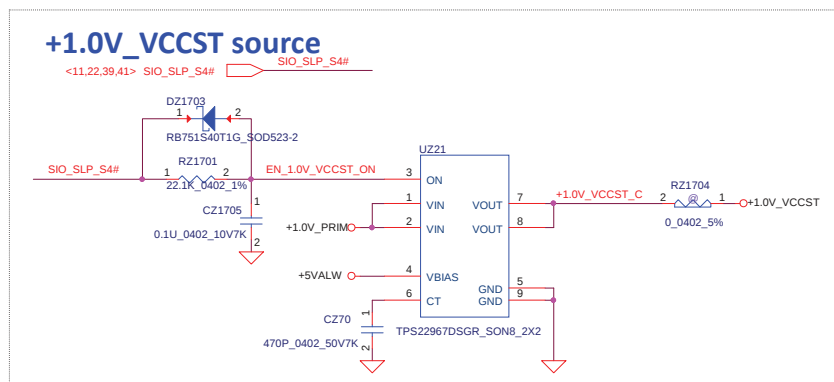
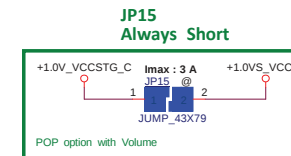
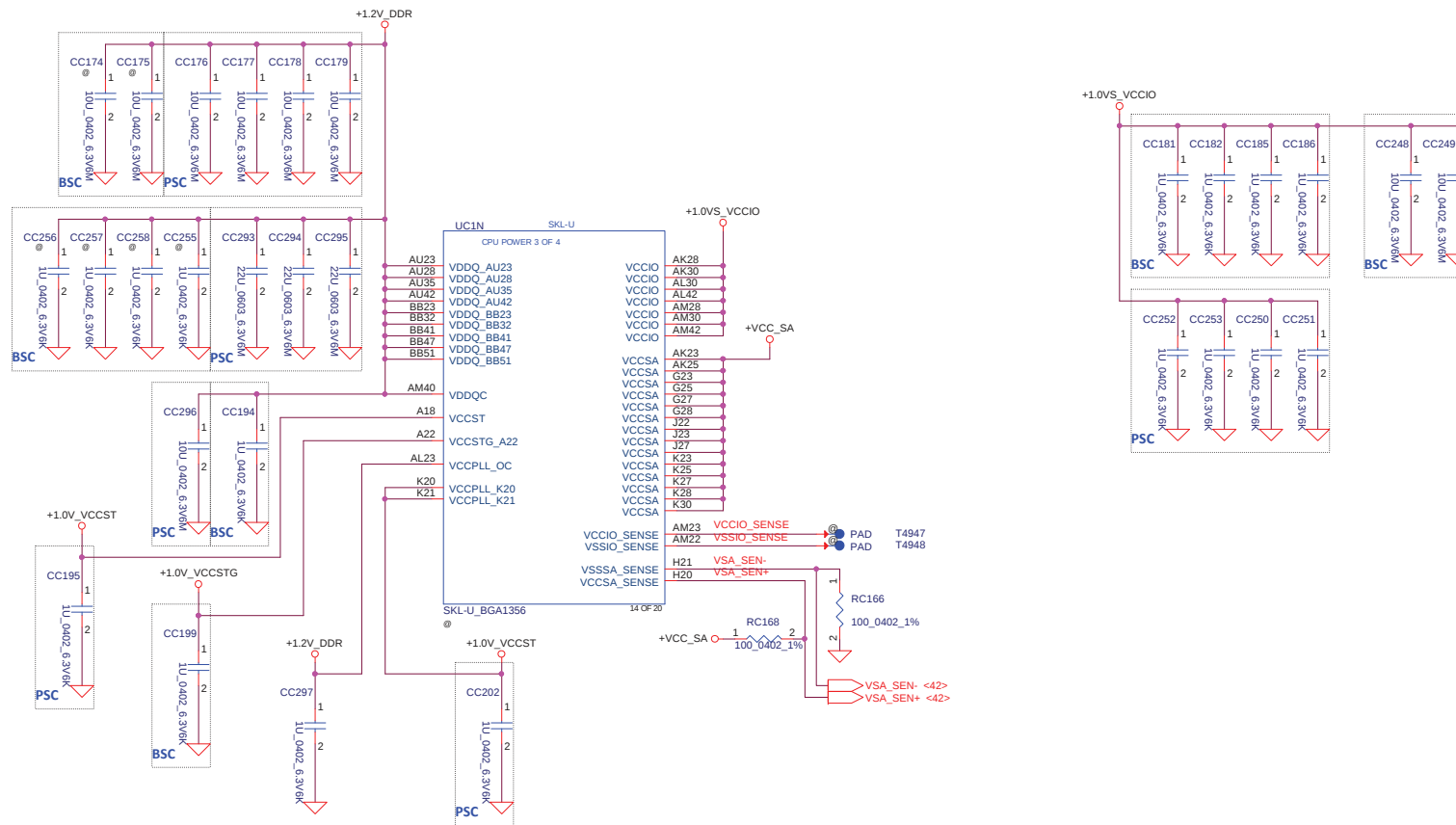
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Compal Electronics, Inc.			
Title			
MCP(9,14)XDP/VSS			
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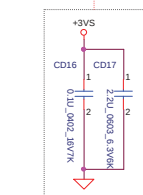
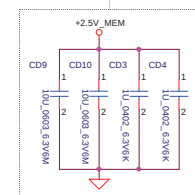
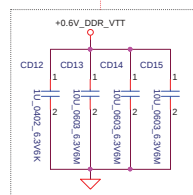
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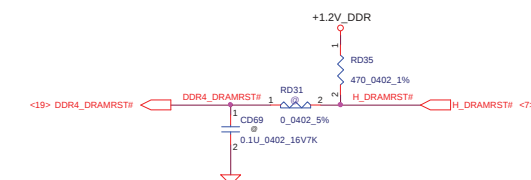
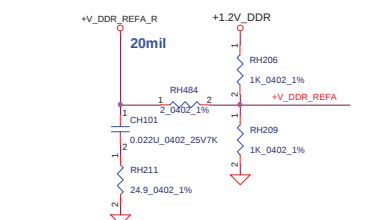
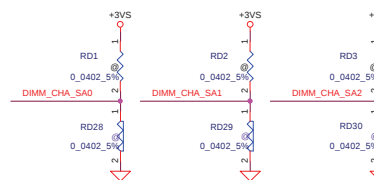
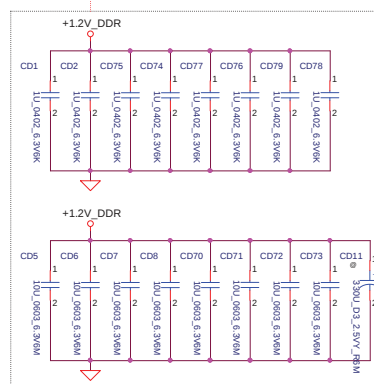
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Layout Note:
Place near JDIMM1.257,259

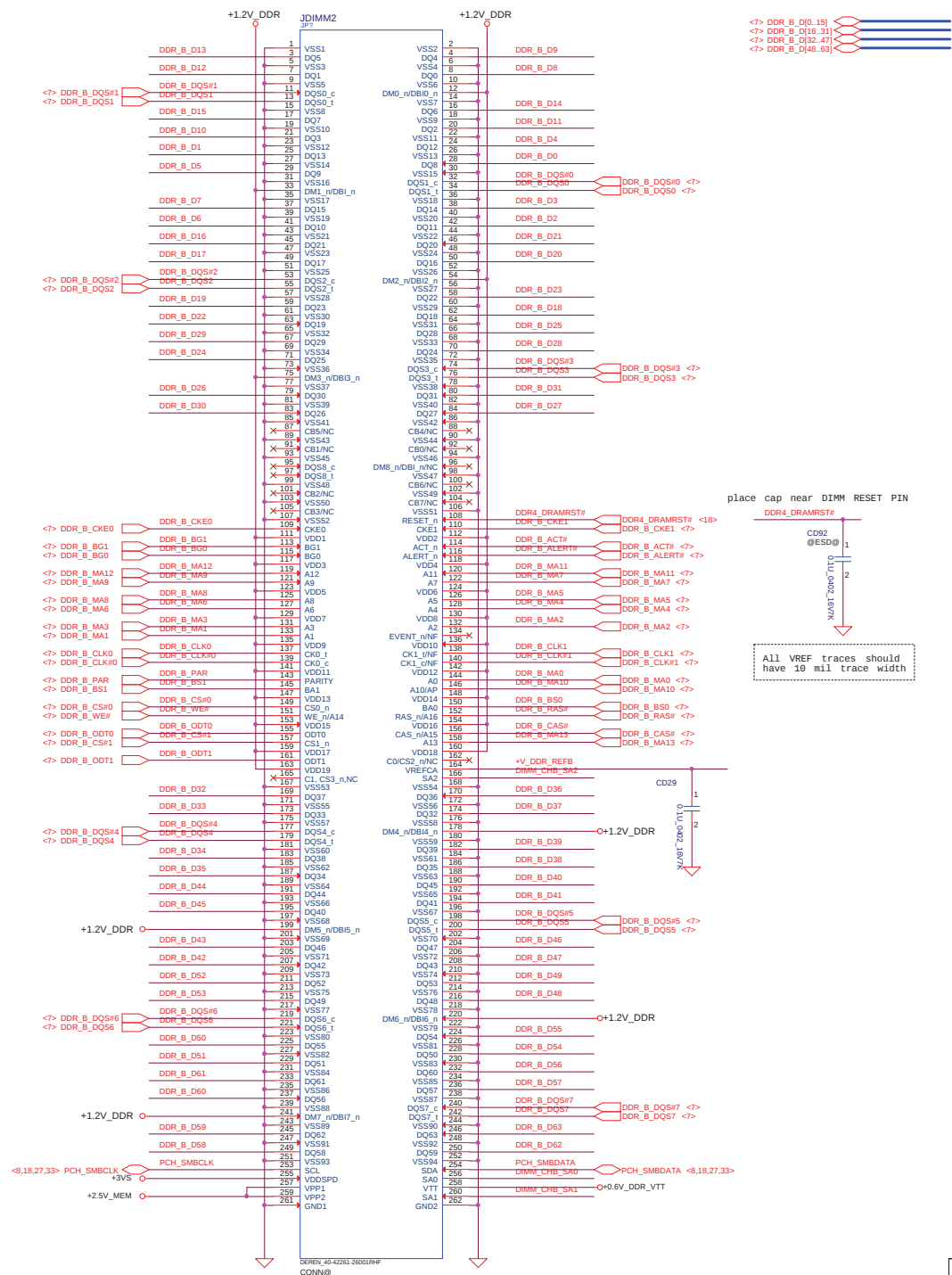
Layout Note:
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Layout Note:
Place near JDIMM1



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								Size		Document Number		Rev		1.0	
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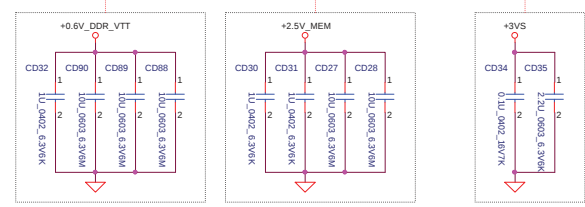


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<?> DDR_B_D16.31
<?> DDR_B_D132.47
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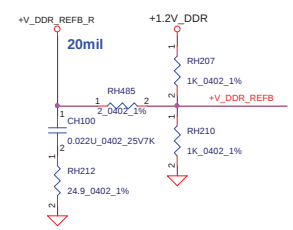
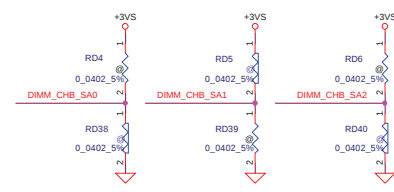
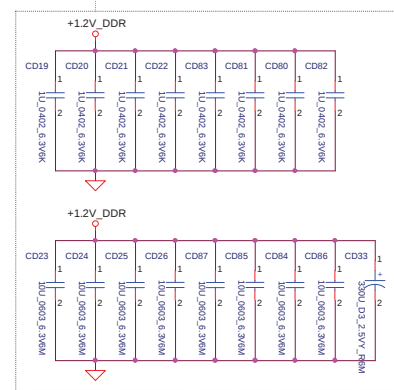
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Layout Note:
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Layout Note:
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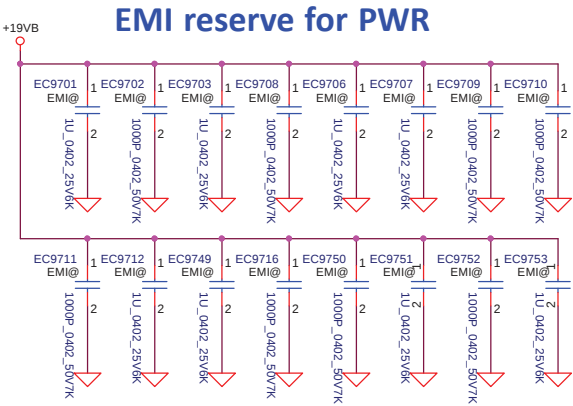
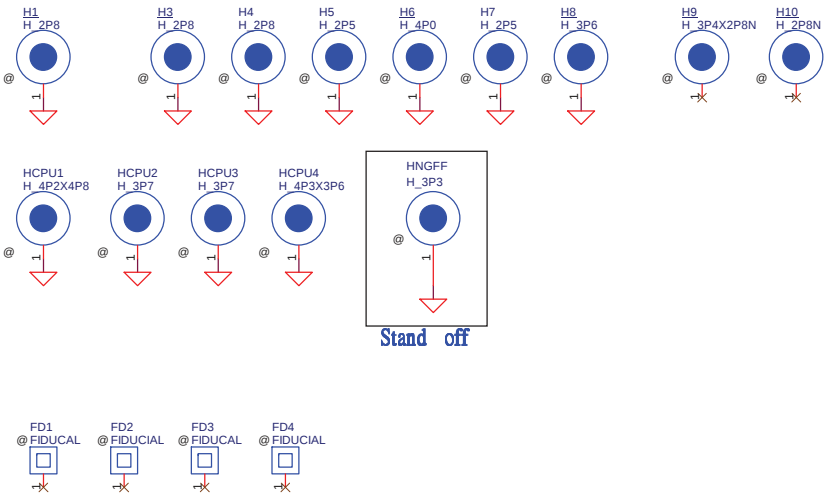
Layout Note:
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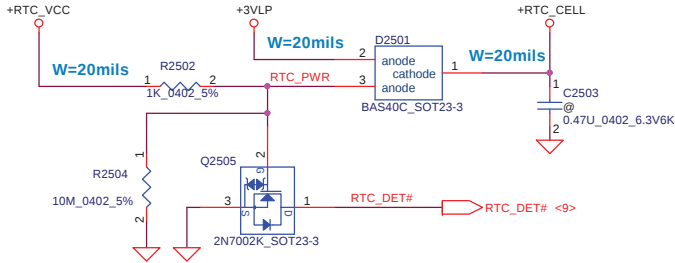
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Main Func = Other

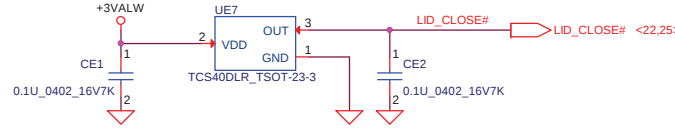
Screw hole/FD/EMI stop



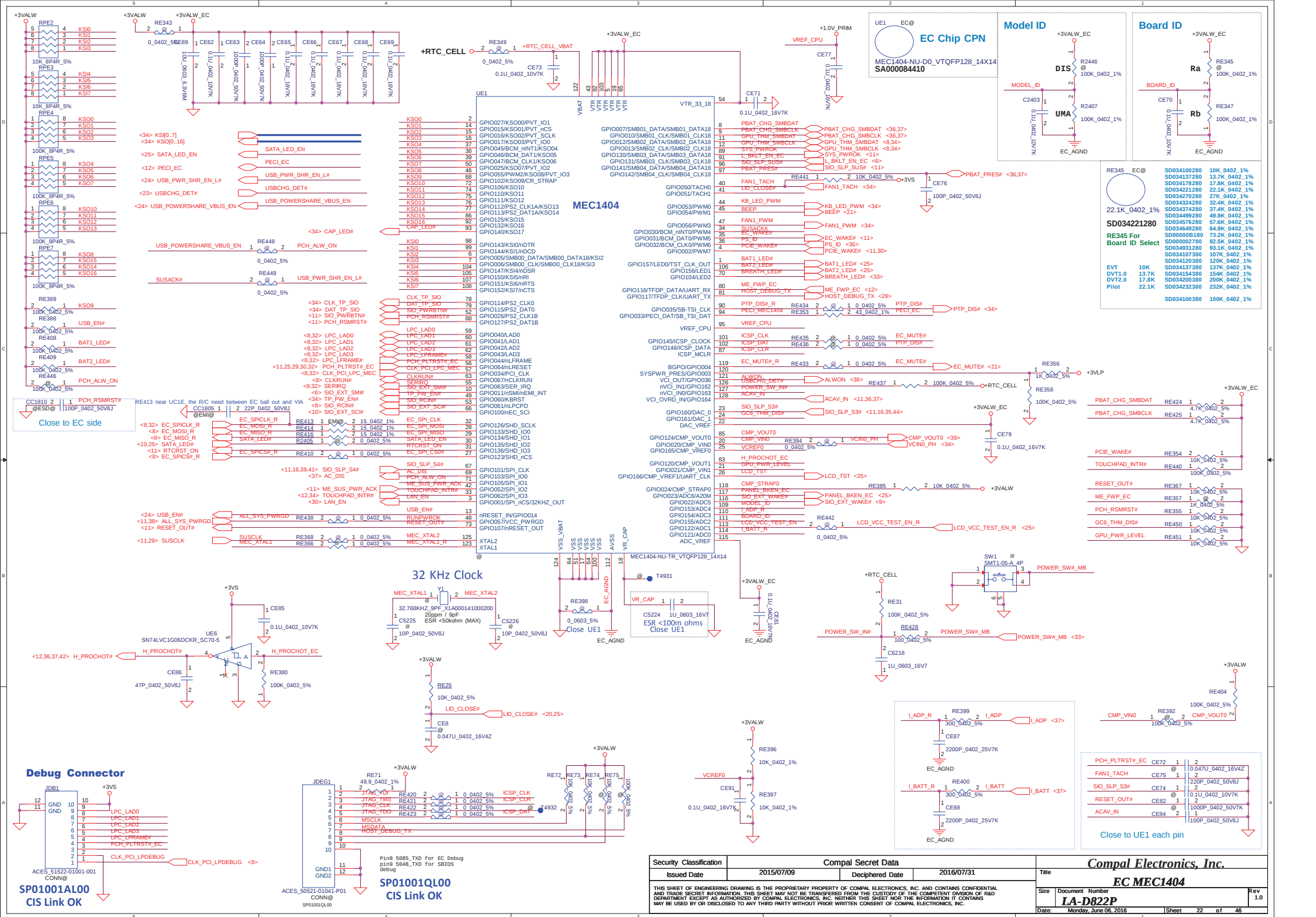
Main Func = RTC



Main Func = LID Switch

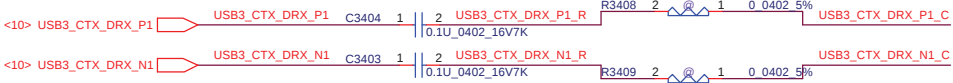


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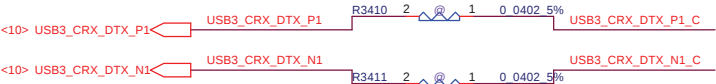


Main Func = USB3.0 Port1/Port2

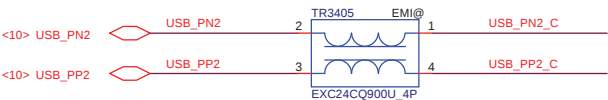
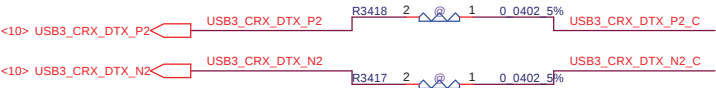
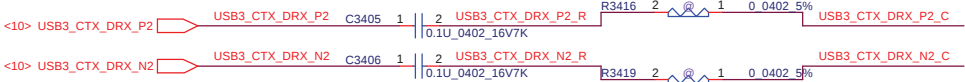
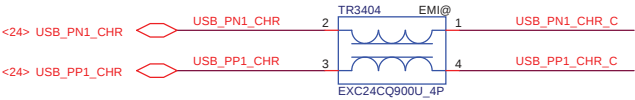
USB3.0 90ohm
Main SM070003V00(S COM FL_INPAQ HCM1012GH900BP)
2nd SM070004000(S COM FL_TAIYO MCF12102G900-T)
3rd SM070004300(S COM FL_PANASONIC EXC24CH900U)



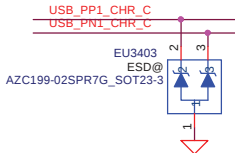
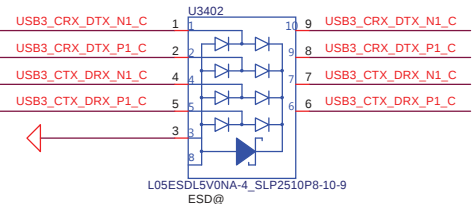
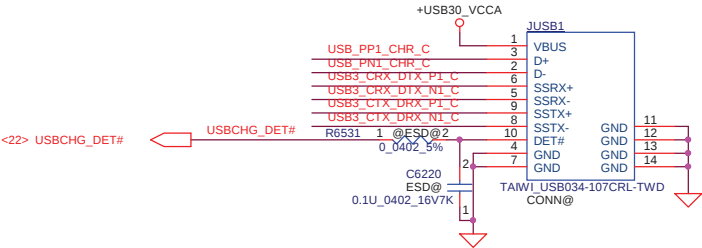
USB3.0 90ohm
Main SM070003V00(S COM FL_INPAQ HCM1012GH900BP)
2nd SM070004000(S COM FL_TAIYO MCF12102G900-T)
3rd SM070004300(S COM FL_PANASONIC EXC24CH900U)



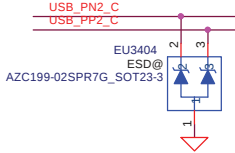
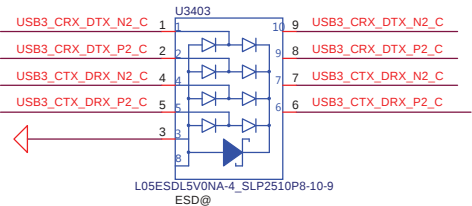
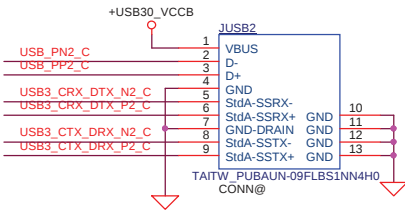
USB2.0 90ohm
Main SM070003Z00(S COM FL_INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FL_MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FL_PANASONIC EXC24CQ900U)



USB3.0 Port1



USB3.0 Port2

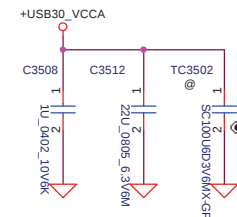


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										Size	
										Document Number	
										LA-D822P	
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										1.0	

The diagram shows the USB OTG module circuit. It includes a U3505 IC (EM5203J-20_SOT25-5) with the following connections:

- Pin 1: +USB30_VCC
- Pin 2: USB_OC#1
- Pin 3: USB_OC#1
- Pin 4: USB_EN#
- Pin 5: +5VALW

The schematic diagram illustrates the USB3.0 PHY circuit for the TPS2546RTER_QFN16_3x3. The central component is the UUS5 PHY block, which is connected to various power and control signals. The circuit includes a CUS20 capacitor, a 0.1uF 0402 16V7K capacitor, and a 1M 0402 5% resistor. The power supply is +5VALW, and the USB3.0 power supply is +USB30_VCCA. The diagram shows the connection of the PHY to the TPS2546RTER_QFN16_3x3 chip, which is a USB3.0 PHY controller. The circuit also includes a USB_PN1 and USB_PP1 signal, which are connected to the PHY. The USB_PN1_CHR and USB_PP1_CHR signals are connected to the PHY. The USB_POWERSHARE_VBUS_EN signal is connected to the PHY. The UUS5_CTL1 signal is connected to the PHY. The USB_PWR_SHR_EN_L# signal is connected to the PHY. The USB_POWERSHARE_VBUS_EN signal is connected to the PHY. The diagram also shows the connection of the PHY to the TPS2546RTER_QFN16_3x3 chip, which is a USB3.0 PHY controller.

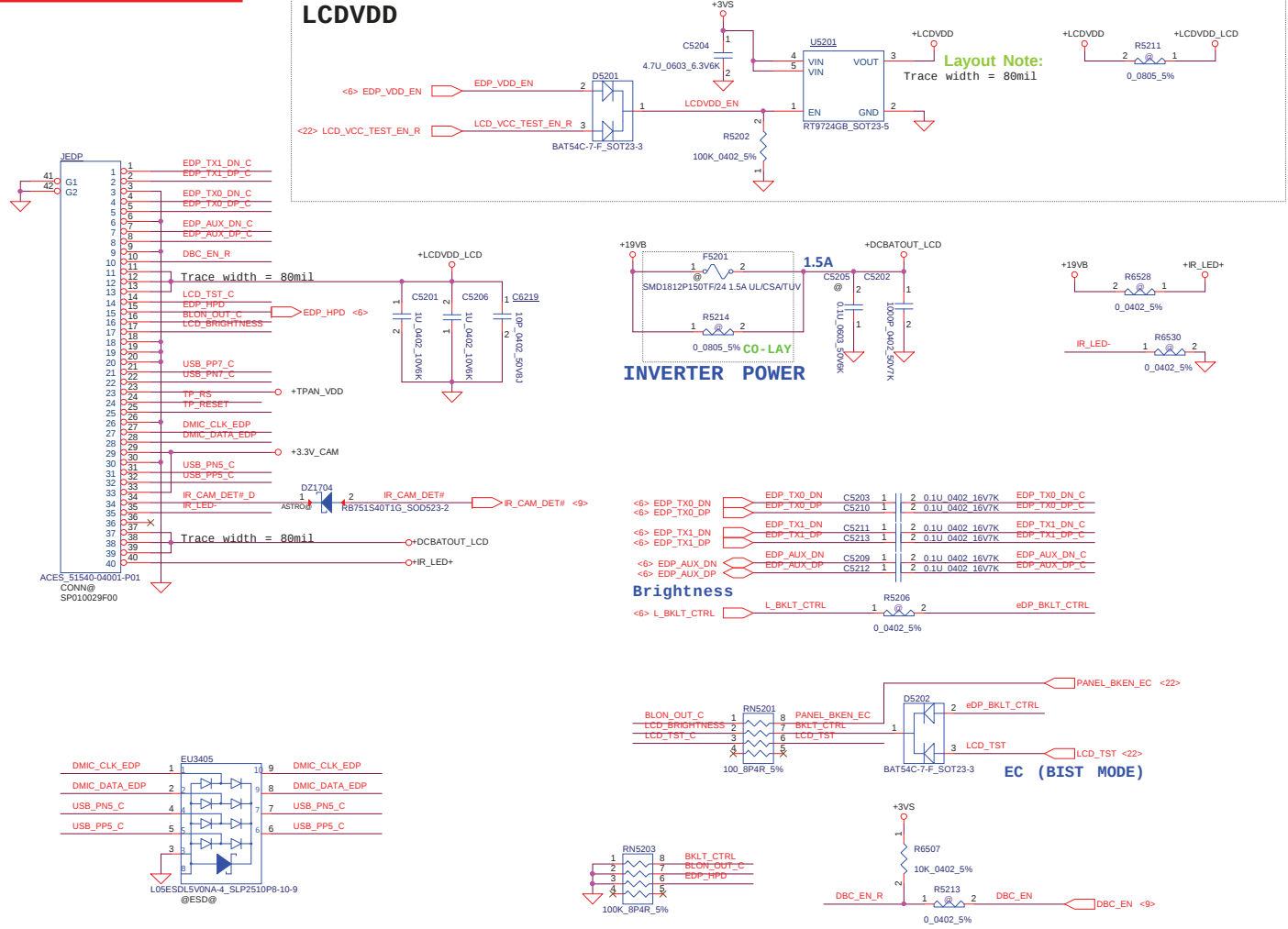


IC \ PIN	PIN9
TPS2546	STATUS#
TPS2544	NC

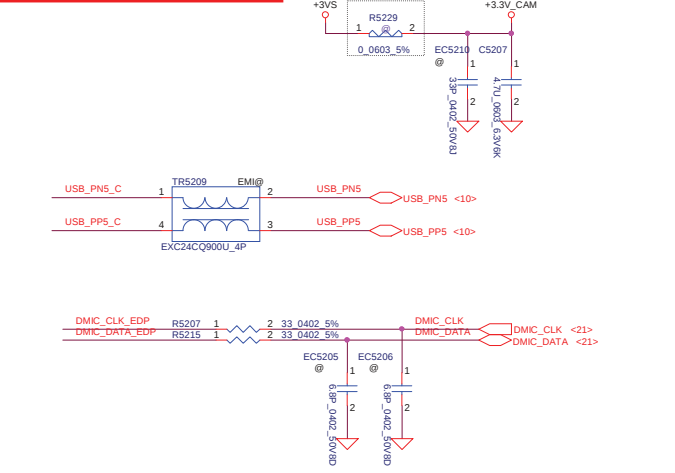


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				Size	Document Number	Rev
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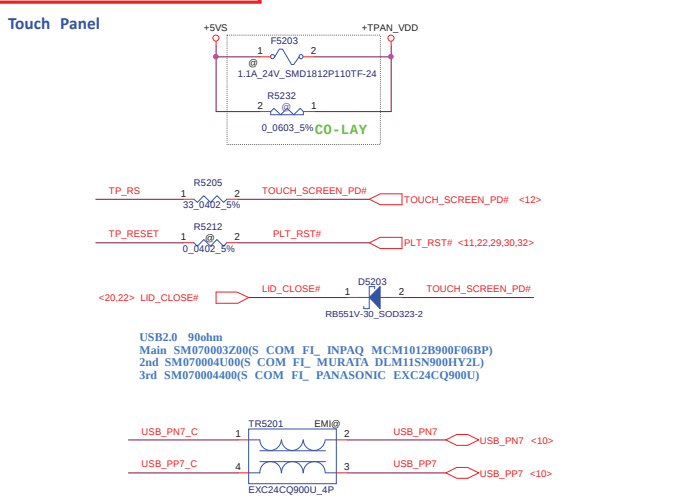
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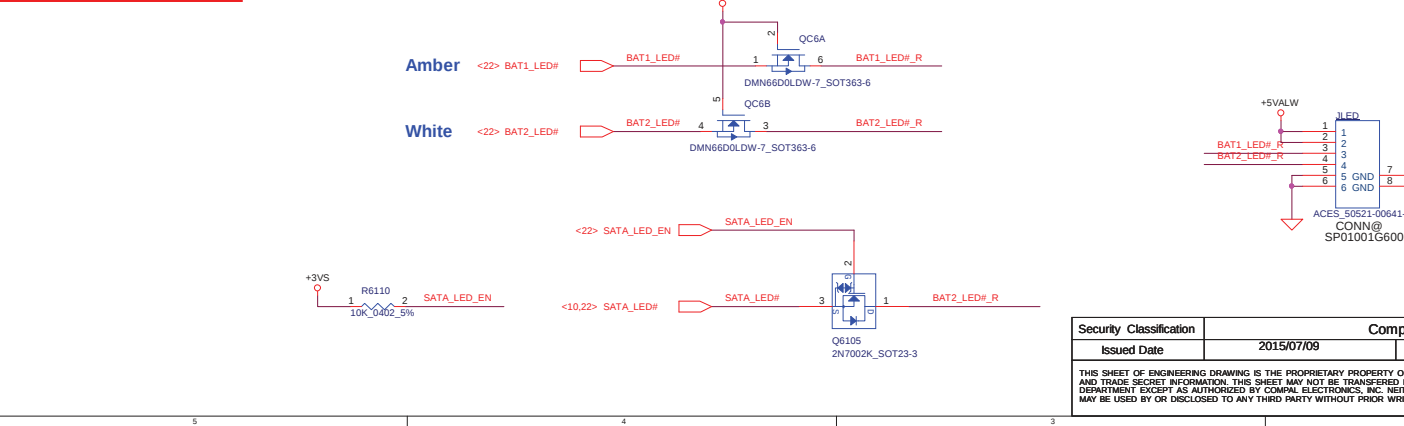
Main Func = CAM



Main Func = TS



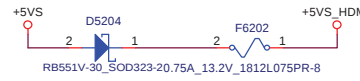
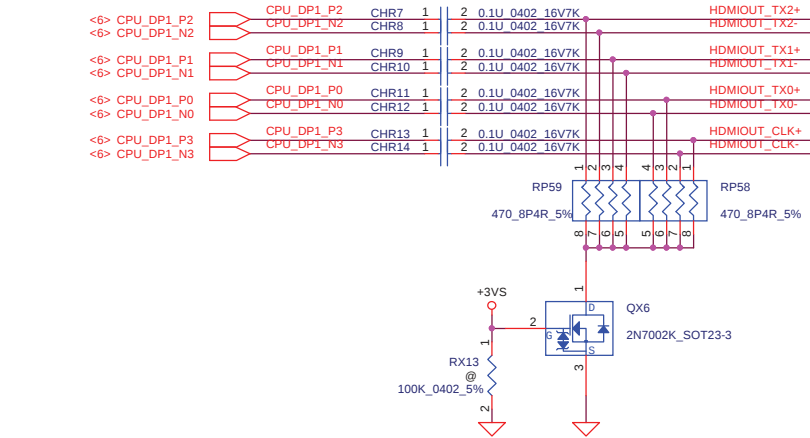
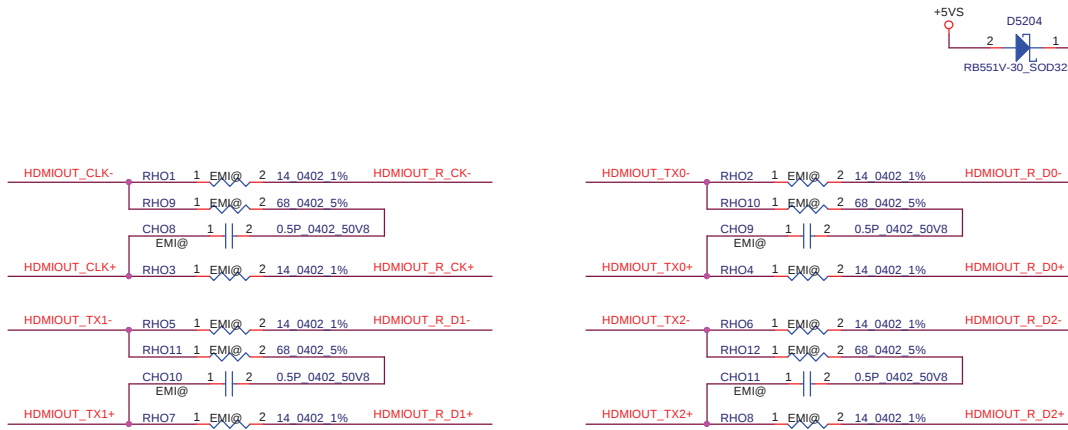
Main Func = LED



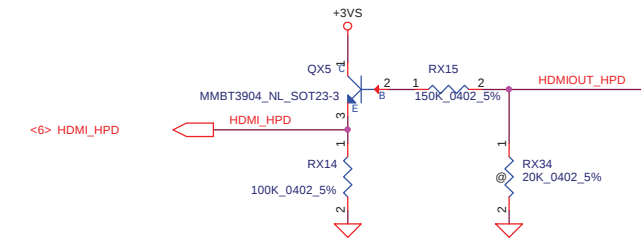
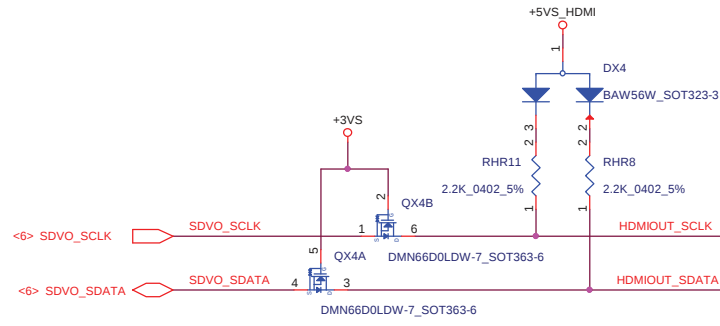
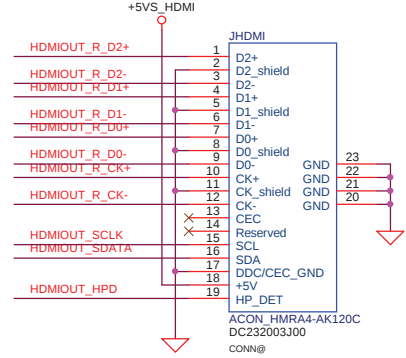
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Main Func = HDMI

- 2014.12.25
1. LH01 LH02 LH03 LH04 change root pin (SI ZE : 050 4) and unpp
 2. RH01, RH03, RH05, RH07, RH02, RH04, RH06, RH08, RH013, RH014, RH015, RH016, change to pop.

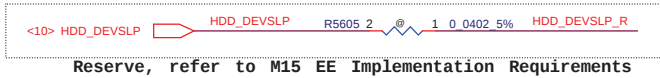
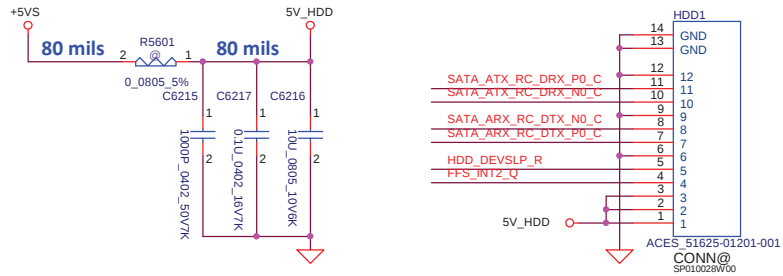


HDMI-OUT Connector



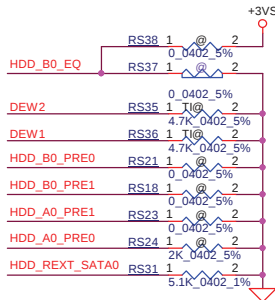
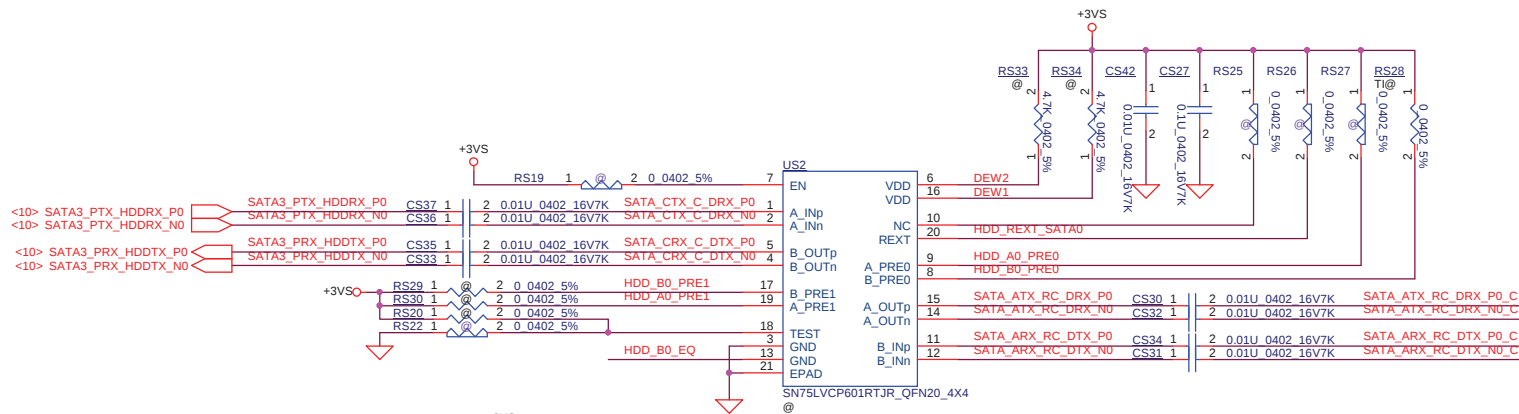
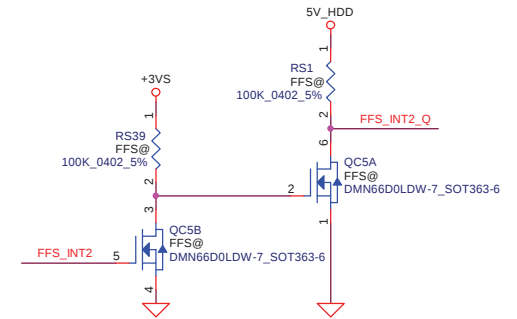
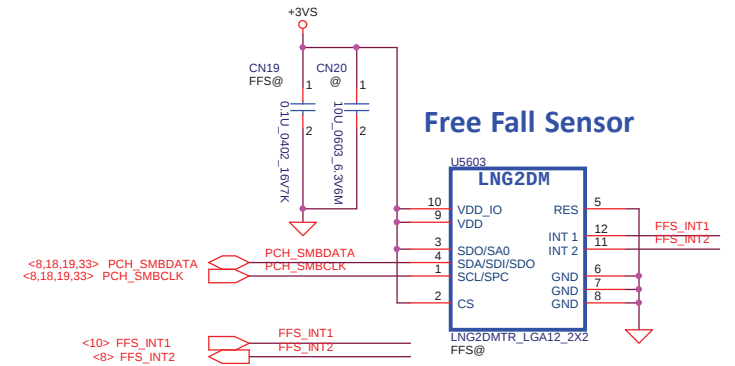
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SATA HDD Connector



Reserve, refer to M15 EE Implementation Requirements

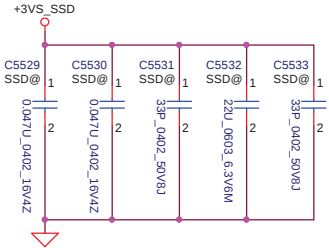
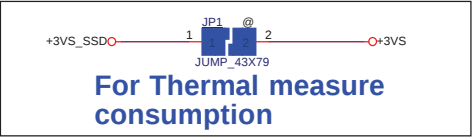
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	



	US2	RS35	RS36	RS18	RS22	RS23	RS24	RS28
TI	SA00003ZX00	4.7K	4.7K	NC	NC	NC	2K	V
PARADE	SA00007JU00	7.5K	NC	V	V	V	NC	NC

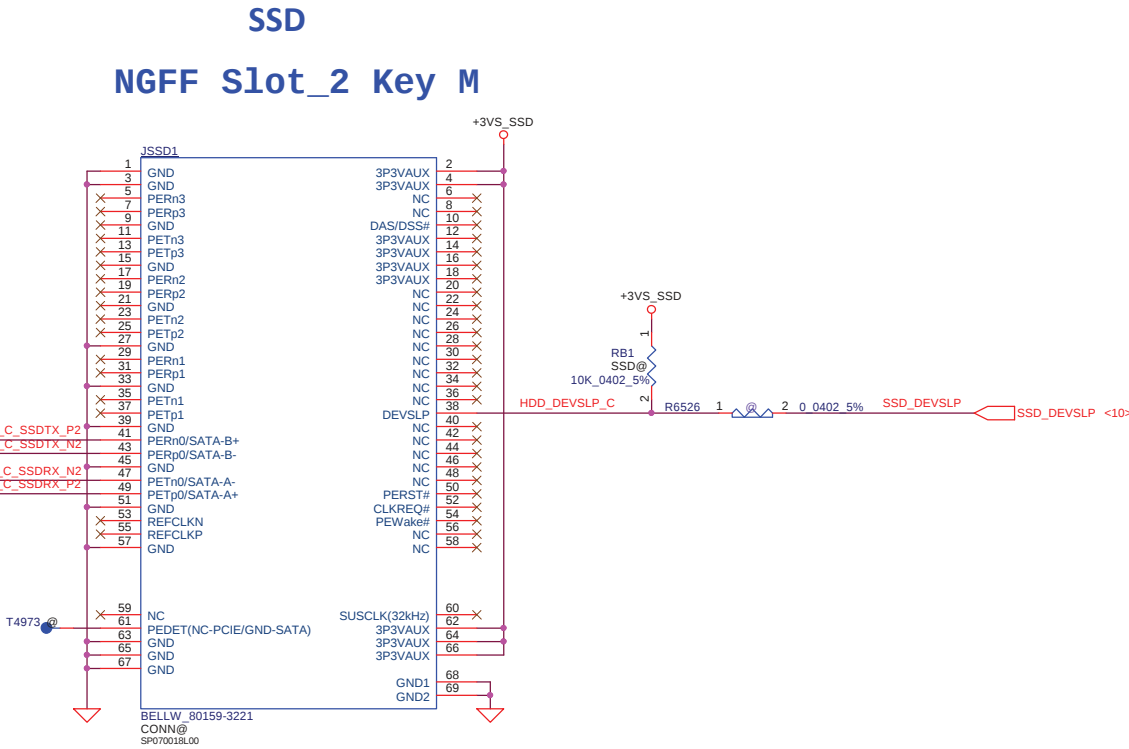


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Size	Document Number	Rev		1.0	
Date:	Monday, June 06, 2016	Sheet	27 of 46		



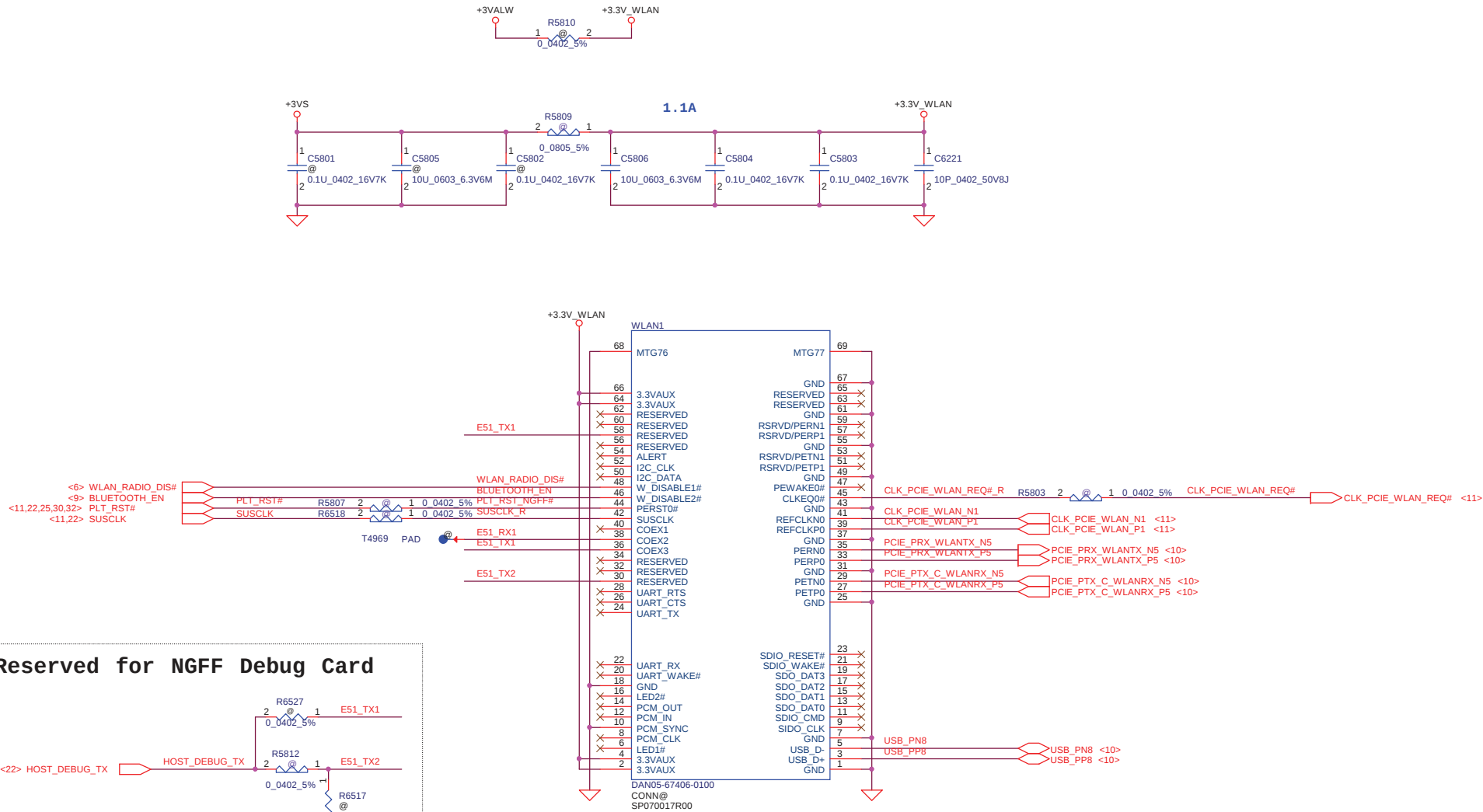
2/6 TX Cap change P/N,
Now It's 0402 0ohm resistor.

<10> SATA3_PRX_SSDTX_P2	SATA3_PRX_SSDTX_P2	CHD1	SSD@	1	2	0.01U 0402 16V7K	SATA3_PRX_C_SSDTX_P2
<10> SATA3_PRX_SSDTX_N2	SATA3_PRX_SSDTX_N2	CHD2	SSD@	1	2	0.01U 0402 16V7K	SATA3_PRX_C_SSDTX_N2
<10> SATA3_PTX_SSDRX_N2	SATA3_PTX_SSDRX_N2	CHD3	SSD@	1	2	0.01U 0402 16V7K	SATA3_PTX_C_SSDRX_N2
<10> SATA3_PTX_SSDRX_P2	SATA3_PTX_SSDRX_P2	CHD4	SSD@	1	2	0.01U 0402 16V7K	SATA3_PTX_C_SSDRX_P2



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Size	Document Number					Rev
	LA-D822P					1.0
Date:	Monday, June 06, 2016		Sheet	28	of	46

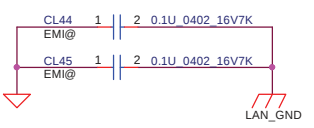
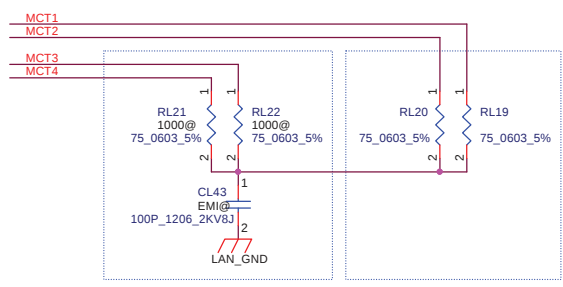
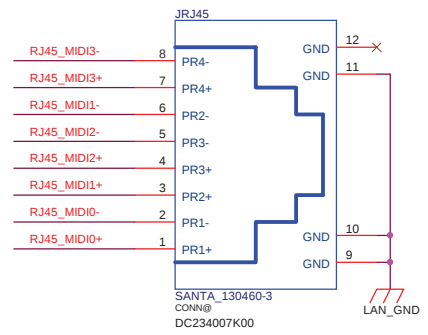
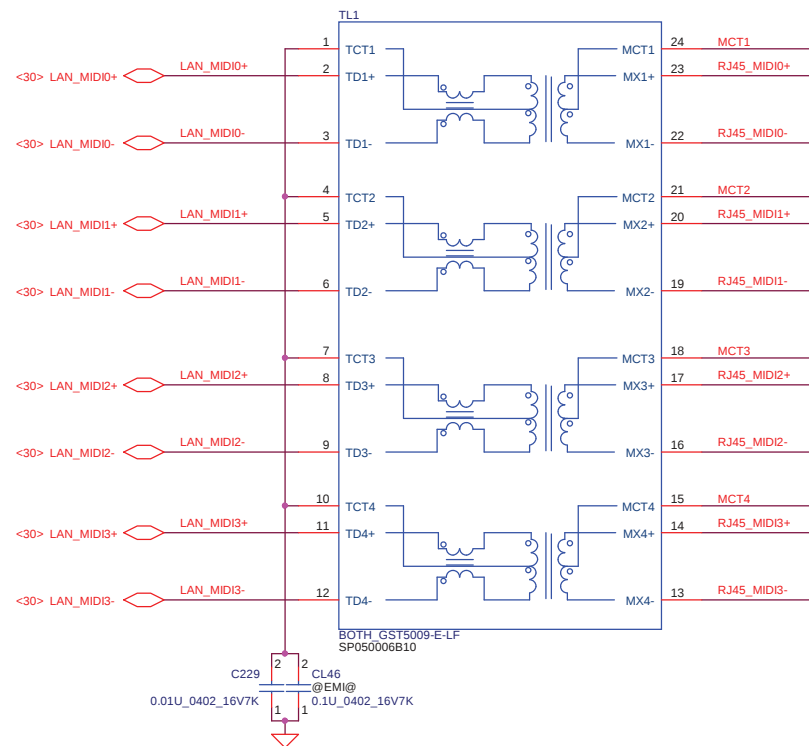
Main Func = WLAN



Support: Intel Dual Band Wireless-AC 3160

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		LA-D822P			1.0
Date:		Monday, June 06, 2016		Sheet	29 of 46

Main Func = LAN



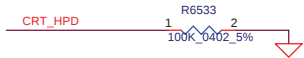
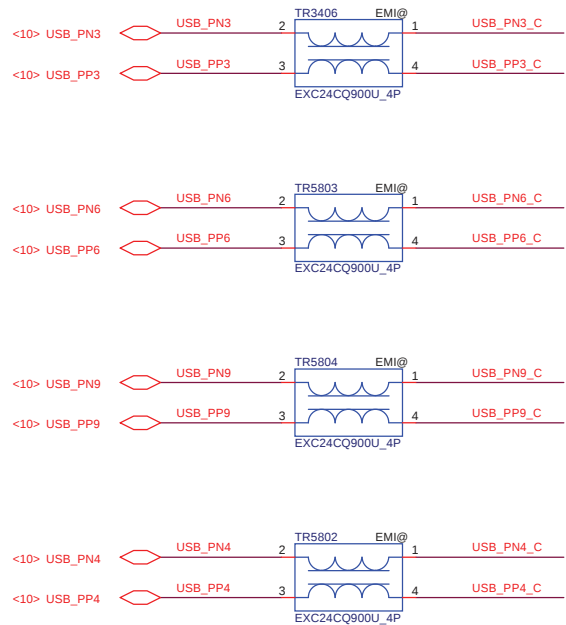
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				Document Number	1.0
				LA-D822P	
				Date:	Monday, June 06, 2016
				Sheet	31 of 46

Main Func = TPM2.0

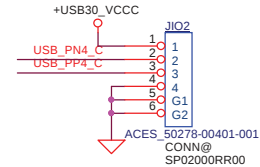
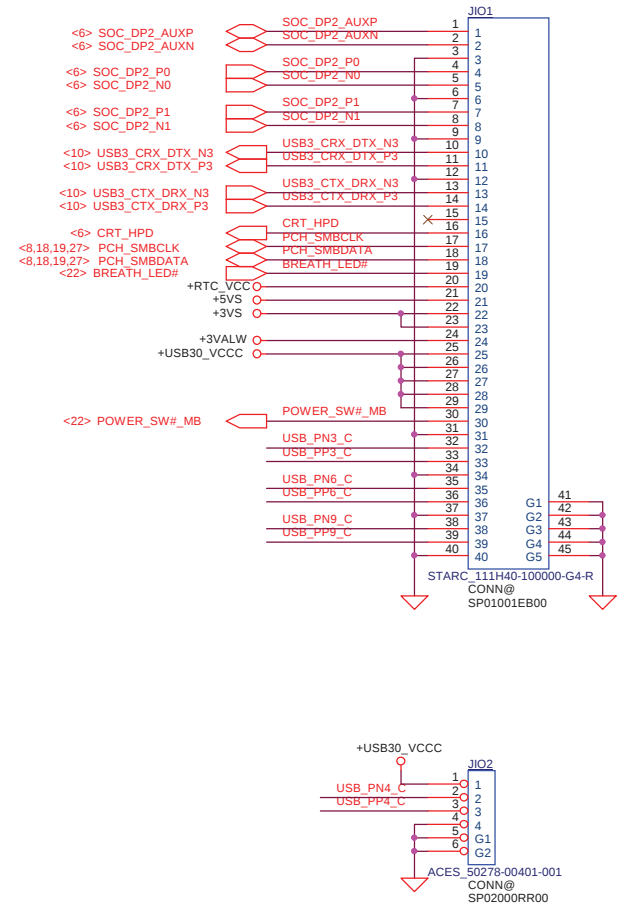
TPM2.0 Schematic Diagram

Components:

- U13: NPCT6503A00009D510 (TPM Controller)
- U21: QZ11 ME2301DC-G_SOT23-3 (TPM Controller)
- RZ115, RZ116, RZ117, RZ118, RZ119, RZ120, RZ121, RZ122, RZ123, RZ124, RZ125, RZ126, RZ127, RZ128, RZ129, RZ130, RZ131, RZ132, RZ133, RZ134, RZ135, RZ136, RZ137, RZ138, RZ139, RZ140, RZ141, RZ142, RZ143, RZ144, RZ145, RZ146, RZ147, RZ148, RZ149, RZ150, RZ151, RZ152, RZ153, RZ154, RZ155, RZ156, RZ157, RZ158, RZ159, RZ160, RZ161, RZ162, RZ163, RZ164, RZ165, RZ166, RZ167, RZ168, RZ169, RZ170, RZ171, RZ172, RZ173, RZ174, RZ175, RZ176, RZ177, RZ178, RZ179, RZ180, RZ181, RZ182, RZ183, RZ184, RZ185, RZ186, RZ187, RZ188, RZ189, RZ190, RZ191, RZ192, RZ193, RZ194, RZ195, RZ196, RZ197, RZ198, RZ199, RZ200, RZ201, RZ202, RZ203, RZ204, RZ205, RZ206, RZ207, RZ208, RZ209, RZ210, RZ211, RZ212, RZ213, RZ214, RZ215, RZ216, RZ217, RZ218, RZ219, RZ220, RZ221, RZ222, RZ223, RZ224, RZ225, RZ226, RZ227, RZ228, RZ229, RZ230, RZ231, RZ232, RZ233, RZ234, RZ235, RZ236, RZ237, RZ238, RZ239, RZ240, RZ241, RZ242, RZ243, RZ244, RZ245, RZ246, RZ247, RZ248, RZ249, RZ250, RZ251, RZ252, RZ253, RZ254, RZ255, RZ256, RZ257, RZ258, RZ259, RZ260, RZ261, RZ262, RZ263, RZ264, RZ265, RZ266, RZ267, RZ268, RZ269, RZ270, RZ271, RZ272, RZ273, RZ274, RZ275, RZ276, RZ277, RZ278, RZ279, RZ280, RZ281, RZ282, RZ283, RZ284, RZ285, RZ286, RZ287, RZ288, RZ289, RZ290, RZ291, RZ292, RZ293, RZ294, RZ295, RZ296, RZ297, RZ298, RZ299, RZ300, RZ301, RZ302, RZ303, RZ304, RZ305, RZ306, RZ307, RZ308, RZ309, RZ310, RZ311, RZ312, RZ313, RZ314, RZ315, RZ316, RZ317, RZ318, RZ319, RZ320, RZ321, RZ322, RZ323, RZ324, RZ325, RZ326, RZ327, RZ328, RZ329, RZ330, RZ331, RZ332, RZ333, RZ334, RZ335, RZ336, RZ337, RZ338, RZ339, RZ340, RZ341, RZ342, RZ343, RZ344, RZ345, RZ346, RZ347, RZ348, RZ349, RZ350, RZ351, RZ352, RZ353, RZ354, RZ355, RZ356, RZ357, RZ358, RZ359, RZ360, RZ361, RZ362, RZ363, RZ364, RZ365, RZ366, RZ367, RZ368, RZ369, RZ370, RZ371, RZ372, RZ373, RZ374, RZ375, RZ376, RZ377, RZ378, RZ379, RZ380, RZ381, RZ382, RZ383, RZ384, RZ385, RZ386, RZ387, RZ388, RZ389, RZ390, RZ391, RZ392, RZ393, RZ394, RZ395, RZ396, RZ397, RZ398, RZ399, RZ400, RZ401, RZ402, RZ403, RZ404, RZ405, RZ406, RZ407, RZ408, RZ409, RZ410, RZ411, RZ412, RZ413, RZ414, RZ415, RZ416, RZ417, RZ418, RZ419, RZ420, RZ421, RZ422, RZ423, RZ424, RZ425, RZ426, RZ427, RZ428, RZ429, RZ430, RZ431, RZ432, RZ433, RZ434, RZ435, RZ436, RZ437, RZ438, RZ439, RZ440, RZ441, RZ442, RZ443, RZ444, RZ445, RZ446, RZ447, RZ448, RZ449, RZ450, RZ451, RZ452, RZ453, RZ454, RZ455, RZ456, RZ457, RZ458, RZ459, RZ460, RZ461, RZ462, RZ463, RZ464, RZ465, RZ466, RZ467, RZ468, RZ469, RZ470, RZ471, RZ472, RZ473, RZ474, RZ475, RZ476, RZ477, RZ478, RZ479, RZ480, RZ481, RZ482, RZ483, RZ484, RZ485, RZ486, RZ487, RZ488, RZ489, RZ490, RZ491, RZ492, RZ493, RZ494, RZ495, RZ496, RZ497, RZ498, RZ499, RZ500, RZ501, RZ502, RZ503, RZ504, RZ505, RZ506, RZ507, RZ508, RZ509, RZ510, RZ511, RZ512, RZ513, RZ514, RZ515, RZ516, RZ517, RZ518, RZ519, RZ520, RZ521, RZ522, RZ523, RZ524, RZ525, RZ526, RZ527, RZ528, RZ529, RZ530, RZ531, RZ532, RZ533, RZ534, RZ535, RZ536, RZ537, RZ538, RZ539, RZ540, RZ541, RZ542, RZ543, RZ544, RZ545, RZ546, RZ547, RZ548, RZ549, RZ550, RZ551, RZ552, RZ553, RZ554, RZ555, RZ556, RZ557, RZ558, RZ559, RZ560, RZ561, RZ562, RZ563, RZ564, RZ565, RZ566, RZ567, RZ568, RZ569, RZ570, RZ571, RZ572, RZ573, RZ574, RZ575, RZ576, RZ577, RZ578, RZ579, RZ580, RZ581, RZ582, RZ583, RZ584, RZ585, RZ586, RZ587, RZ588, RZ589, RZ590, RZ591, RZ592, RZ593, RZ594, RZ595, RZ596, RZ597, RZ598, RZ599, RZ600, RZ601, RZ602, RZ603, RZ604, RZ605, RZ606, RZ607, RZ608, RZ609, RZ610, RZ611, RZ612, RZ613, RZ614, RZ615, RZ616, RZ617, RZ618, RZ619, RZ620, RZ621, RZ622, RZ623, RZ624, RZ625, RZ626, RZ627, RZ628, RZ629, RZ630, RZ631, RZ632, RZ633, RZ634, RZ635, RZ636, RZ637, RZ638, RZ639, RZ640, RZ641, RZ642, RZ643, RZ644, RZ645, RZ646, RZ647, RZ648, RZ649, RZ650, RZ651, RZ652, RZ653, RZ654, RZ655, RZ656, RZ657, RZ658, RZ659, RZ660, RZ661, RZ662, RZ663, RZ664, RZ665, RZ666, RZ667, RZ668, RZ669, RZ670, RZ671, RZ672, RZ673, RZ674, RZ675, RZ676, RZ677, RZ678, RZ679, RZ680, RZ681, RZ682, RZ683, RZ684, RZ685, RZ686, RZ687, RZ688, RZ689, RZ690, RZ691, RZ692, RZ693, RZ694, RZ695, RZ696, RZ697, RZ698, RZ699, RZ700, RZ701, RZ702, RZ703, RZ704, RZ705, RZ706, RZ707, RZ708, RZ709, RZ710, RZ711, RZ712, RZ713, RZ714, RZ715, RZ716, RZ717, RZ718, RZ719, RZ720, RZ721, RZ722, RZ723, RZ724, RZ725, RZ726, RZ727, RZ728, RZ729, RZ730, RZ731, RZ732, RZ733, RZ734, RZ735, RZ736, RZ737, RZ738, RZ739, RZ740, RZ741, RZ742, RZ743, RZ744, RZ745, RZ746, RZ747, RZ748, RZ749, RZ750, RZ751, RZ752, RZ753, RZ754, RZ755, RZ756, RZ757, RZ758, RZ759, RZ760, RZ761, RZ762, RZ763, RZ764, RZ765, RZ766, RZ767, RZ768, RZ769, RZ770, RZ771, RZ772, RZ773, RZ774, RZ775, RZ

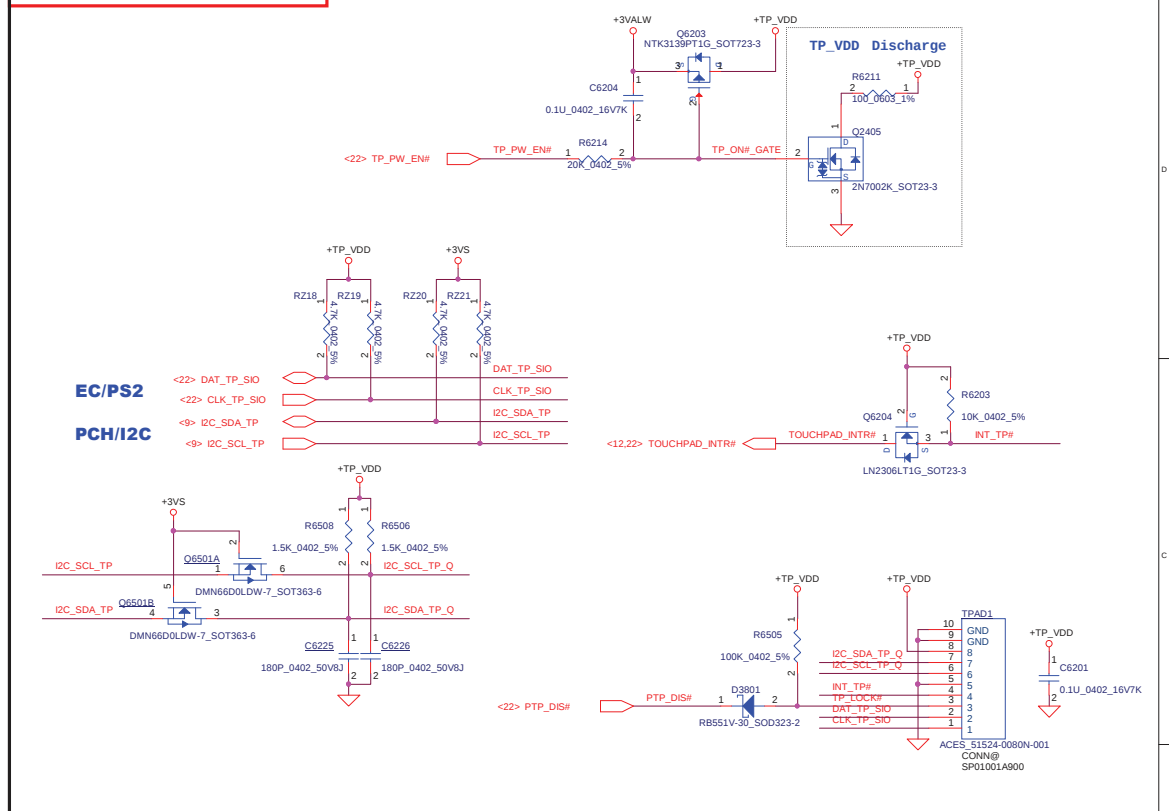


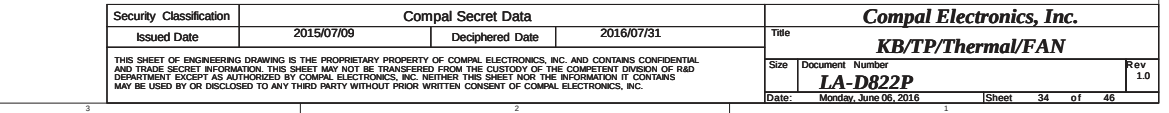
I/O Board Connector



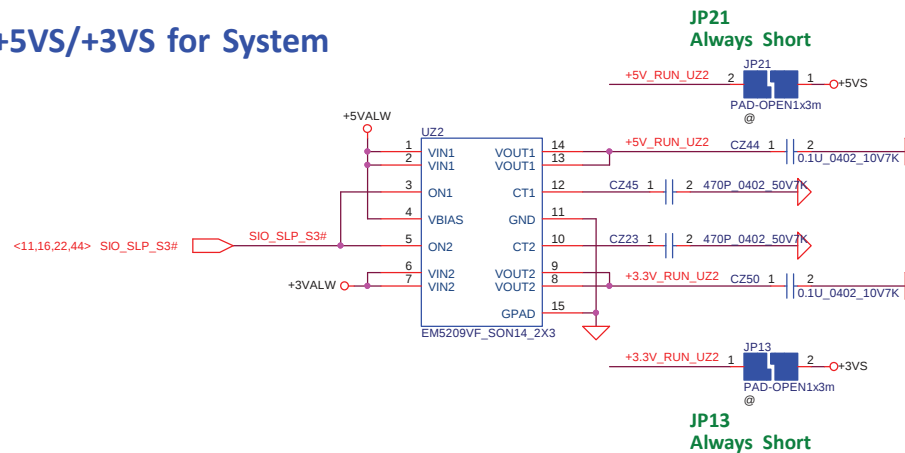
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3
Main Func = TPAD

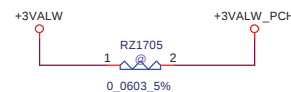




+5VS/+3VS for System

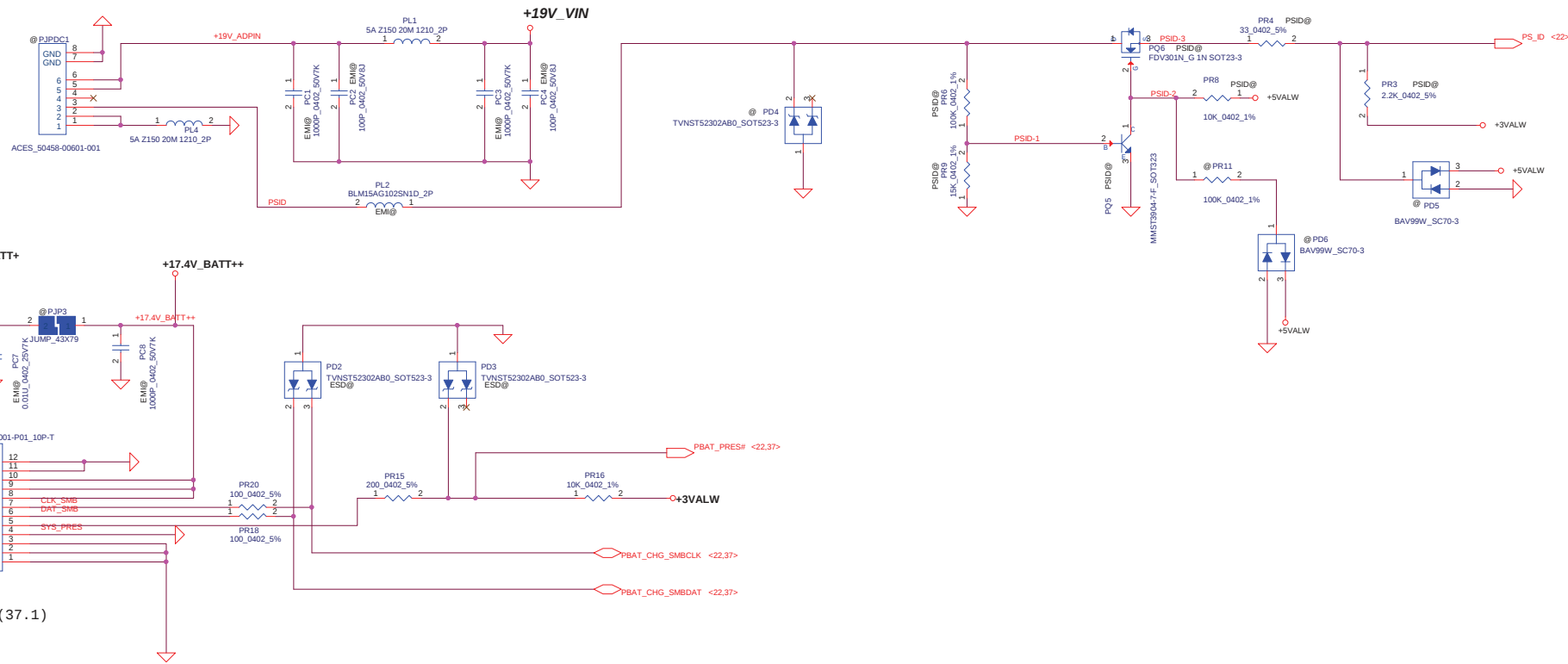


+3VALW_PCH for System



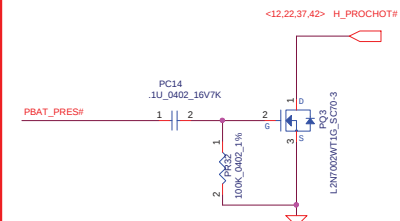
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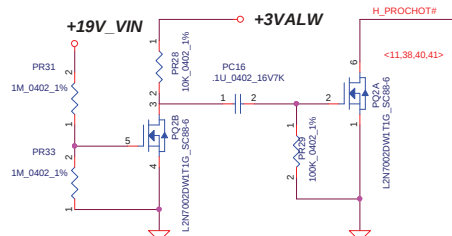
Adapter protection

if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep @ in BOM since battery can not
be removed by end user

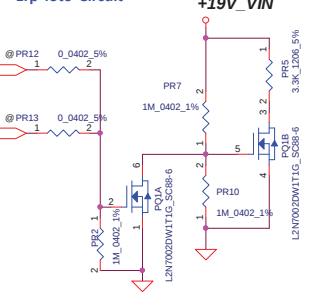


Battery protection

asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW_PROCHOT# is issued by EC



Erp lot6 Circuit



15W_U22(SK1)
X63:PSID@/U22_SK1@/15W@_U22
X4P:EMIO/BSDO/RFO

15W_U22(KBL)
X63:PSID@/U22_KBL@/15W@_U22
X4P:EMIO/BSDO/RFO

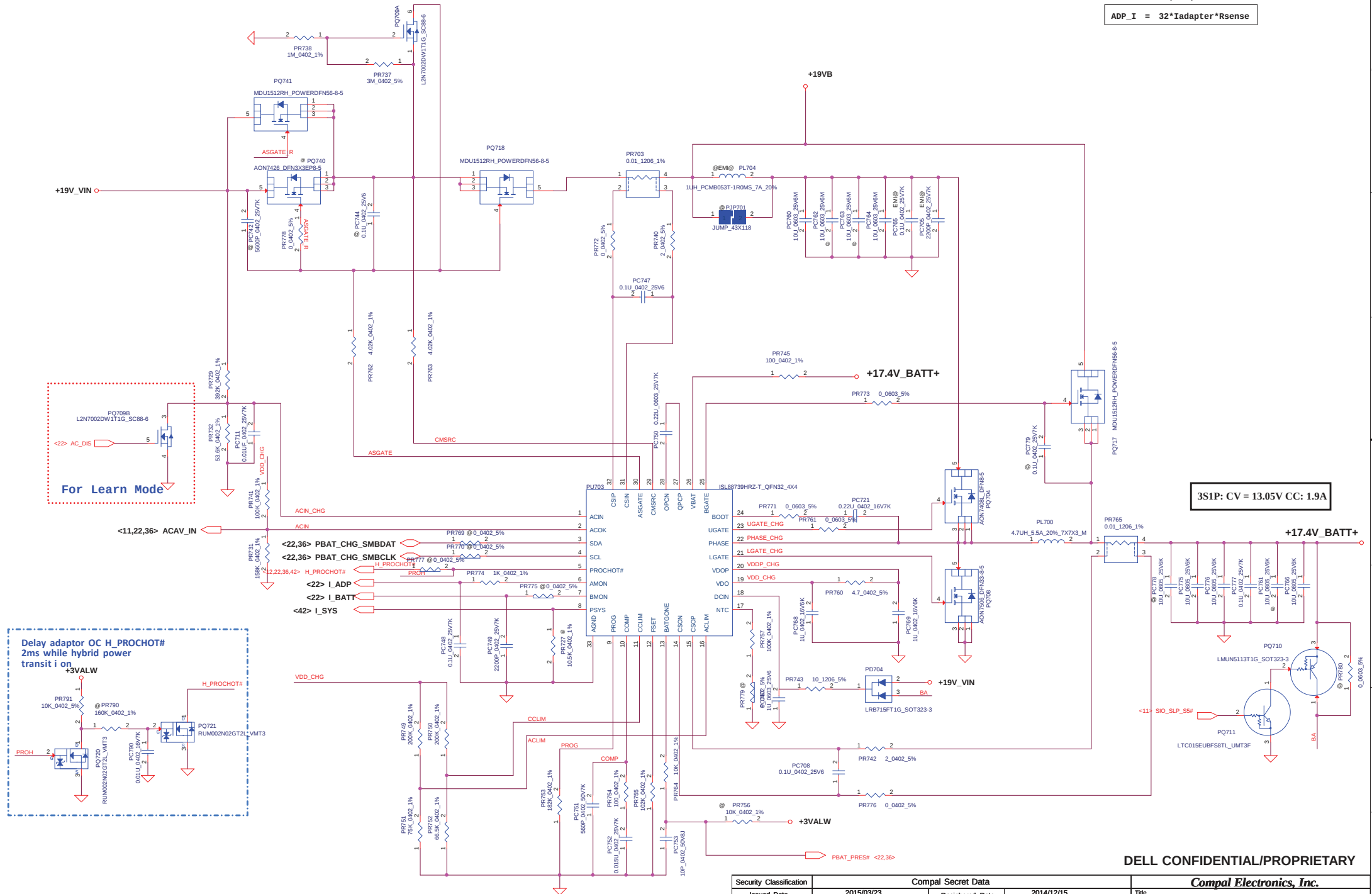
28W_U23e
X63:PSID@/U23@/28W@
X4P:EMIO/BSDO/RFO

15W_U23e(Unused)
X63:PSID@/U23@/15W@_U22/15W@_U23
X4P:EMIO/BSDO/RFO

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Date:	Monday, June 06, 2016	Sheet	36 of 46	PWR DCIN/BATT CONN/OTP	

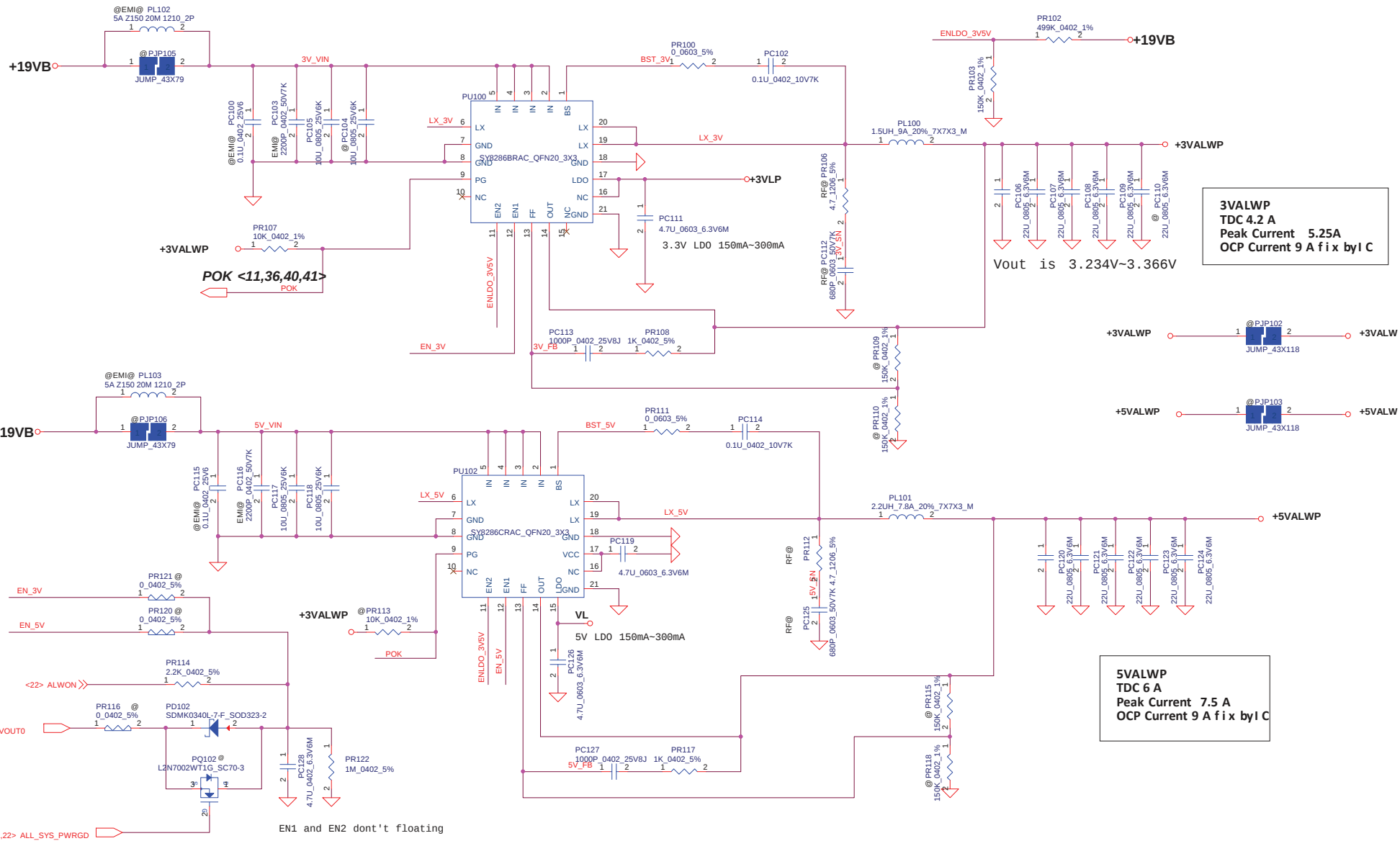
I_{ada}=0~2.30A(45W)

$$ADP_I = 32 \cdot I_{\text{adapter}} \cdot R_{\text{sense}}$$


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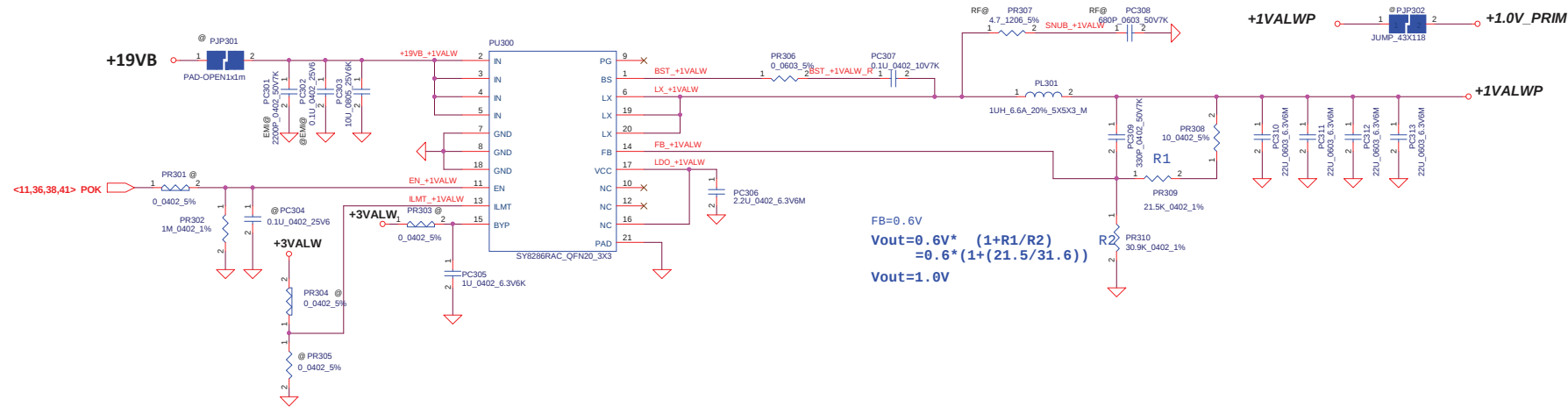
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Title			
PWR_3.3VALWP/5VALWP			
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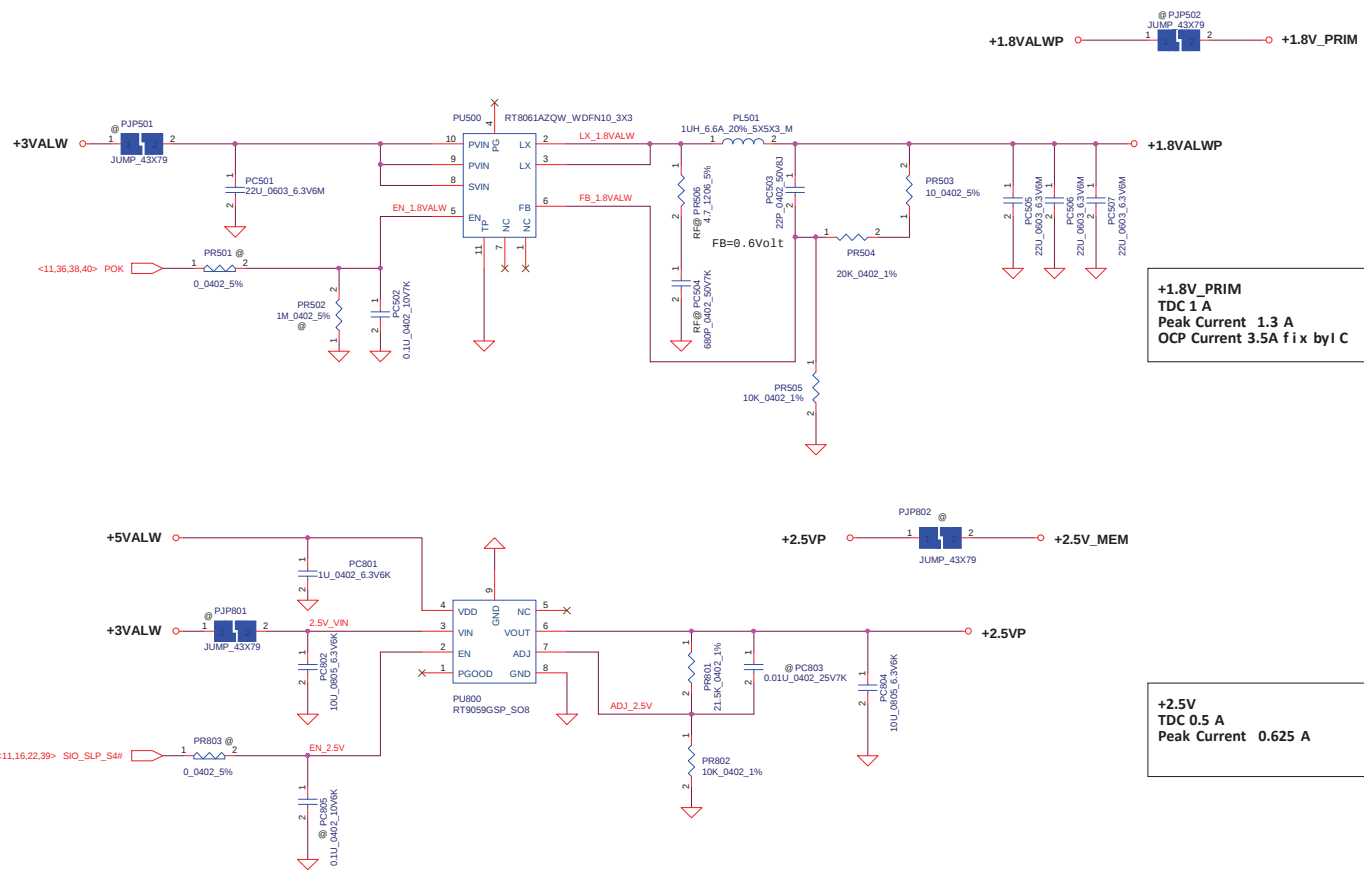
$FB = 0.6V$
 $V_{out} = 0.6V \cdot \left(\frac{1 + R1/R2}{1} \right)$
 $= 0.6V \cdot (1 + 21.5/31.6)$
 $V_{out} = 1.0V$

+1.0V_PRIM
 TDC 6 A
 Peak Current 8.6 A
 OCP Current 12 A Fix by IC
 TYP MAX
 Choke DCR 11.0mohm , 12.0mohm

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

OCP setting	ILMT(pin3)
6A	Pull low
9A	Floating
12A	Pull high

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				X01(0.2)
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Local sense put on HW site

+1.0V_VCCST

+3VS

+5VALW

Local sense put on HW site

VCC_SA
Loadline : 10.3m-ohm

TDC 5A
Peak Current 5A
OCP current 7A
Choke DCR 12 +-5% m ohm

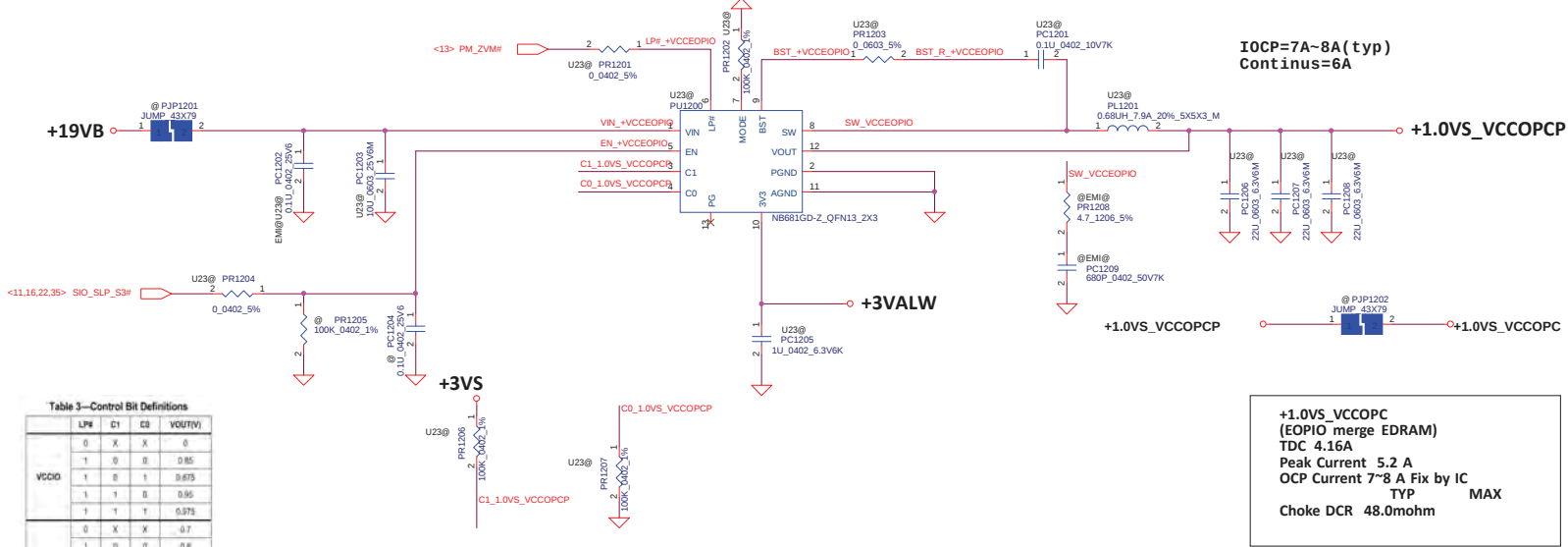
VCCSA_B+ CPU_B+
PAD-OPEN1xm

VCCSA_B+

+5VALW

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Issued Date		2015/12/07		Deciphered Date		2017/01/31		Title PWR_+VCC_SA											
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												Date:		Monday, June 06, 2016				Sheet	

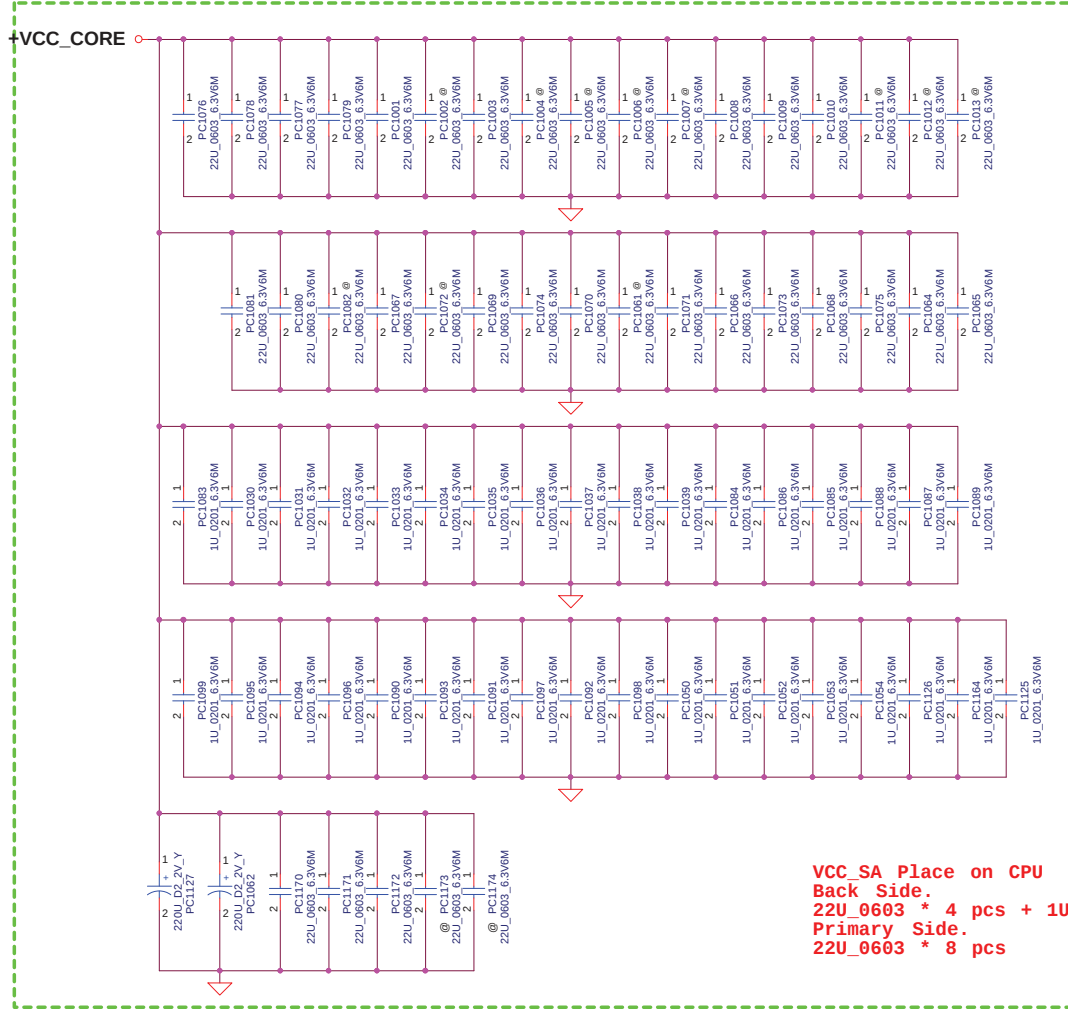


+1.0VS_VCCOPCP
 (EOPIO merge EDRAM)
 TDC 4.16A
 Peak Current 5.2 A
 OCP Current 7~8 A Fix by IC
 TYP MAX
 Choke DCR 48.0mohm

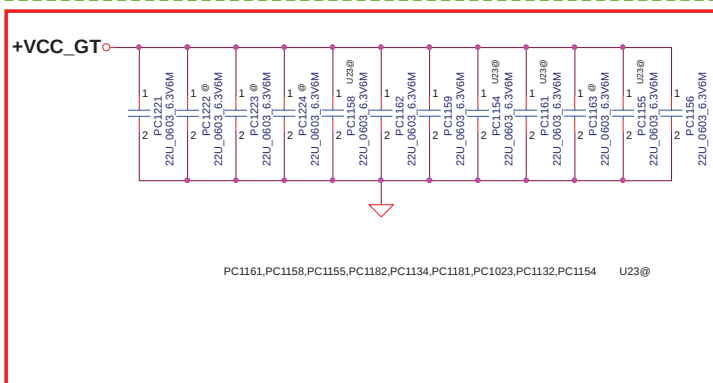
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VCC_CORE Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*35 pcs
Primary Side.
22U_0603 * 20 pcs+220u_D2*2 pcs



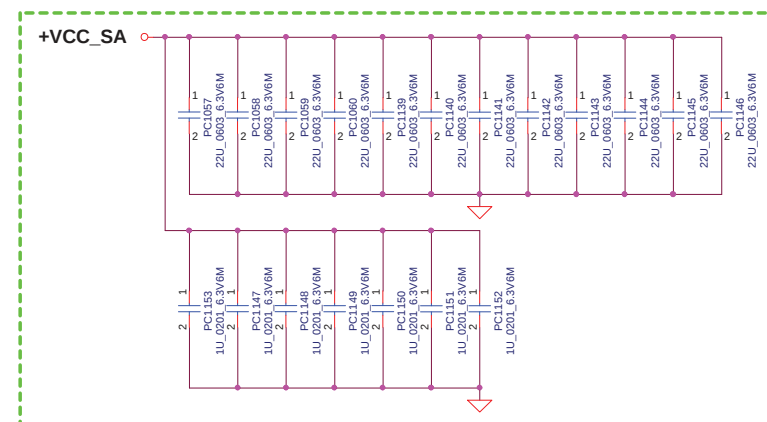
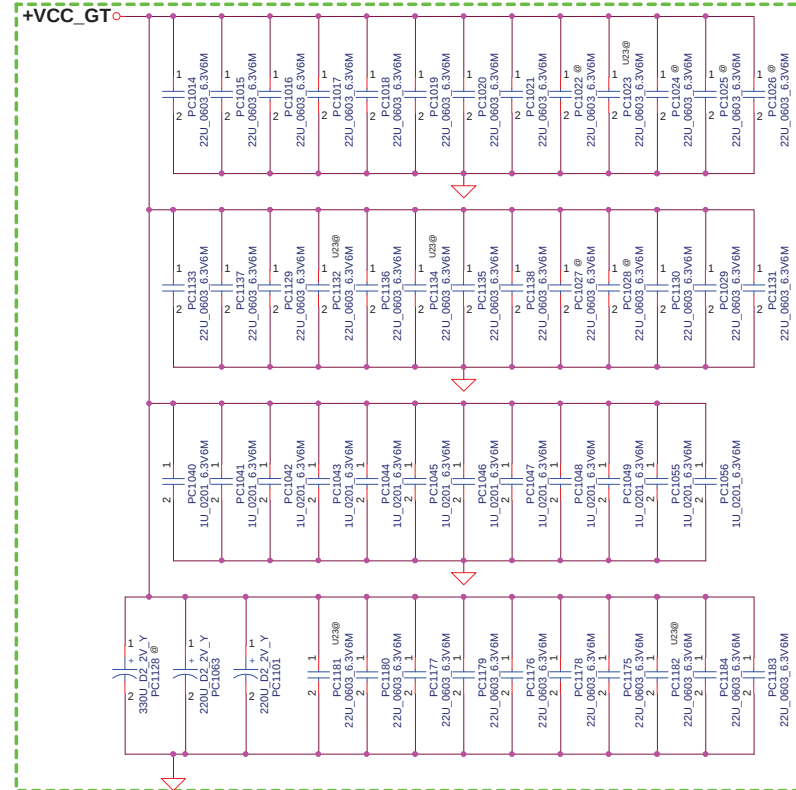
VCC_SA Place on CPU
Back Side.
22U_0603 * 4 pcs + 1U_0201*7 pcs
Primary Side.
22U_0603 * 8 pcs



PC1161,PC1158,PC1155,PC1182,PC1134,PC1181,PC1023,PC1132,PC1154 U23@

For GTX

VCC_GT Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*12 pcs
Primary Side.
22U_0603 * 13 pcs +220u_D2*2 pcs



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				Rev	X000(0.1)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P37	PWR	20160303	COMPAL	to change charger IC	change charger IC(PU703) to ISL88739	0.2(X01)
2	P39 P43 P45 P46	PWR	20160303	COMPAL	to prevent RF issue	add PC208 add PC666,PR676,PC678 add PC1116,PR1122,PC1109, add PC1402,PR1408,PC1408	
3	P42	PWR	20160303	COMPAL	to adjust +VCC_CORE and +VCC_GT load line	change PR622 to 1.91K,PR638 to 287 ohm,PC626 to 0.1uF,PC642 to 0.1uF	
4	P36,P42	PWR	20160303	COMPAL	to save layout space	delete PL3,PL602(reserve location)	
5	P36	PWR	20160303	COMPAL	to fix battery connector ME issue	to change battery connector	
6	P37	PWR	20160304	COMPAL	to fix Temp/Voltage 19.5V DC-IN issue	change PR732 to 53.6K	
7	P44	PWR	20160304	COMPAL	to fix DFB solder open problem	change PC1127,PC1062,PC1128 footprint	
8	P38	PWR	20160308	COMPAL	to prevent OTP functions abnormal issue	to reserve PQ102 and connect to ALL_SYS_PWRGD	
9	P37	PWR	20160316	COMPAL	to save layout space by EMI request	change PC760,PC762,PC763,PC764 to 0603 size and delete PR766,PC767	
10	P43	PWR	20160328	COMPAL	according to test result to adjust VCC_CORE and GT_CORE's load line	to unmount PC624 and PC646	
11	P45	PWR	20160328	COMPAL	according to test result to adjust VCC_CORE and GT_CORE's output MLCC's location(only change BOM) and bulk cap	unmount:PC1021,PC1135,PC1133,PC1131,PC1022,PC1025,PC1027,PC1028,PC1063,PC1008,PC1003,PC1011,PC1072,PC1076,PC1071,PC1081,PC1082,PC1004,PC1007,PC1012 to mount:PC1176,PC1175,PC1177,PC1179,PC1178,PC1180,PC1183,PC1184,PC1170,PC1173,PC1174 to change PC1127,PC1062 to 220uF/9m ohm	0.3(X02)
12	P36	PWR	20160429	COMPAL	To improve EMI and reduce inrush current to mount π filter' s bead and change cap	unmount:PL1,PL4 change:PC2,PC4 to 100pF	
13	P37	PWR	20160429	COMPAL	ISL88739 doesn't support PSYS function	unmount:PR727 change PR774 to 1K ohm change PC748 0.1uF	
14	P39	PWR	20160429	COMPAL	to adjust 1.2V OCP to 10.2A	change PR205 to 11K	
15	P37	PWR	20160429	COMPAL	to aviod inrush to damage MOS	to reserve PQ741	

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