UM8 UMA SYSTEM DIAGRAM

+3V/+5V PG.34
+1.05V/+1.8V PG.36
CPU Core PG.39
VGA Core/+1.1V PG.38
+1.5V/+0.75V PG.35
+1.05VTT PG.37
UMA VGACORE
Charger PG.33

14.318MHz
CLOCK GEN PG.2

SODIMM1 Max. 4GB PG.12 — DDR3 Channel A
SODIMM2 Max. 4GB PG.13 — DDR3 Channel B

INTEL Arrandale
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.3~6

FDI
DMI

PI3VDP411LSZDE PG.27 — HDMI — HDMI PG.24

DB1
CRT — CRT

LVDS — LVDS PG.22

4M ROM PG.26

FAN & THERMAL
GMT G990/
EMC1422-1-AIZL-TR PG.30

DB2

INTEL PCH
Ibex Peak-m
27mm X 25mm
1071pin FCBGA
TDP 5W
PG.7~11

LANE0
WWAN — USB 2.0 PORT5

SATA0 — HDD PG.28
SATA1 — ODD PG.28

PCI-E x 1
LANE6
LAN
Atheros/AR8152
10/100

PCI-E x 1
LANE1
WLAN — USB 2.0 PORT4

USB2.0 X1 — PORT0,1,7
USB2.0 X1 — PORT0,1,7
Webcam PG.22 — PORT11
USB 2.0
PORT12
PORT9
Card Reader
RTS5138 PG.23
BT
BT365 PG.32

PCI-E x 1
LANE5
eSATA
SN75LVCP412
Combo port PG.27
USB 2.0 PORT8

LPC

KBC
ITE 8502 PG.25
KB PG.28
TP PG.28
1M ROM PG.26

Azalia
AUDIO CODEC
ALC269-GR
Speaker PG.31
HP/MIC
Analog MIC

Stackup
TOP
VCC
IN1
IN2
GND
BOT

Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

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25mA

+1.05V_PCH — L14 HCB1608KF-181T15_6 — +VDDIO_CLK

C113 0.1U/ 10V/X7R
C109 0.1U/ 10V/X7R
C112 10U/6.3V_8/X5R

Place each 0.1uF cap close to pin

8/20 Wait Victor check

300mA

+3.3V_RUN — L13 HCB1608KF-181T15_6 — +VDDSE_CLK

C106 10U/6.3V_8/X5R
C101 0.1U/ 10V/X7R
C110 0.1U/ 10V/X7R
C108 0.1U/ 10V/X7R
C107 0.1U/ 10V/X7R
C111 0.1U/ 10V/X7R

Place each 0.1uF cap close to pin

PDC (Power Cap quantities follow UM3)

Check CLK P/N and footprint

U6 — 9LRS3197 — QFN32

+VDDSE_CLK → VDD_LCD, VDD_REF
+VDDIO_CLK → VDD_CPU_IO, VDD_SRC_IO
VDD_USB, VDD_SRC, VDD_CPU

25,30 SMBDAT2 → SDATA
25,30 SMBCLK2 → SCLK

+3.3V_RUN — R113 10K — R99 33/J_4 — CPU_SEL
8 CLK_PCH_14M → CLK_PCH_14M — C96 *10P/50V_4_NC/COG

Place R8044 within 0.5" of C/G

CK_PWRGD_R → CK_PWRGD/PD#_3.3
XTAL_OUT, XTAL_IN → XOUT, XIN
VSS_SATA, VSS_USB, VSS_LCD

CPU_STOP#, REF_0/CPU_SEL

CPU-0 → CLK_BUF_BCLKP_R, CLK_BUF_BCLKN_R
CPU-1 → CLK_BUF_DREFCLKP_R, CLK_BUF_DREFCLKN_R
SRC-1 → CLK_BUF_PCIE_3GPLLP_R, CLK_BUF_PCIE_3GPLLN_R
SATA → CLK_BUF_DREFSSCLKP_R, CLK_BUF_DREFSSCLKN_R
DOT96T_LPR, DOT96C_LPR
27MHz_nonSS, 27MHz_SS
GND, VSS_REF, VSS_CPU, VSS_SRC

Place within 0.5" of C/G

RP4: CLK_BUF_BCLKP_R, CLK_BUF_BCLKN_R → CLK_BUF_BCLKP 8, CLK_BUF_BCLKN 8
RP5: CLK_BUF_DREFCLKP_R, CLK_BUF_DREFCLKN_R → CLK_BUF_DREFCLKP 8, CLK_BUF_DREFCLKN 8
RP6: CLK_BUF_PCIE_3GPLLP_R, CLK_BUF_PCIE_3GPLLN_R → CLK_BUF_PCIE_3GPLLP 8, CLK_BUF_PCIE_3GPLLN 8
RP7: CLK_BUF_DREFSSCLKP_R, CLK_BUF_DREFSSCLKN_R → CLK_BUF_DREFSSCLKP 8, CLK_BUF_DREFSSCLKN 8
0X2

Discrete only

SLG: SLG8SP590VTR Seligo QPN: AL8SP590000
SLG: SLG8SP585VTR Seligo QPN: AL8SP585000
RSC: RTM875N-632-VB-GRT Realtek QPN: AL000875002

+3.3V_RUN — R107 *10K_NC — CPU_SEL — R101 10K

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

BOM check

+3.3V_RUN — R106 1K/J_4 — CK_PWRGD_R
39 VR_PWRGD_CLKEN# → Q14 FDN357N
R105 *100K/F_4_NC

R8253 => UM7 POP
UM9 DE-POP
0918 check

Y4 14.318MHZ
XTAL_IN — C99 33P/50V_4/NPO
XTAL_OUT — C100 33P/50V_4/NPO

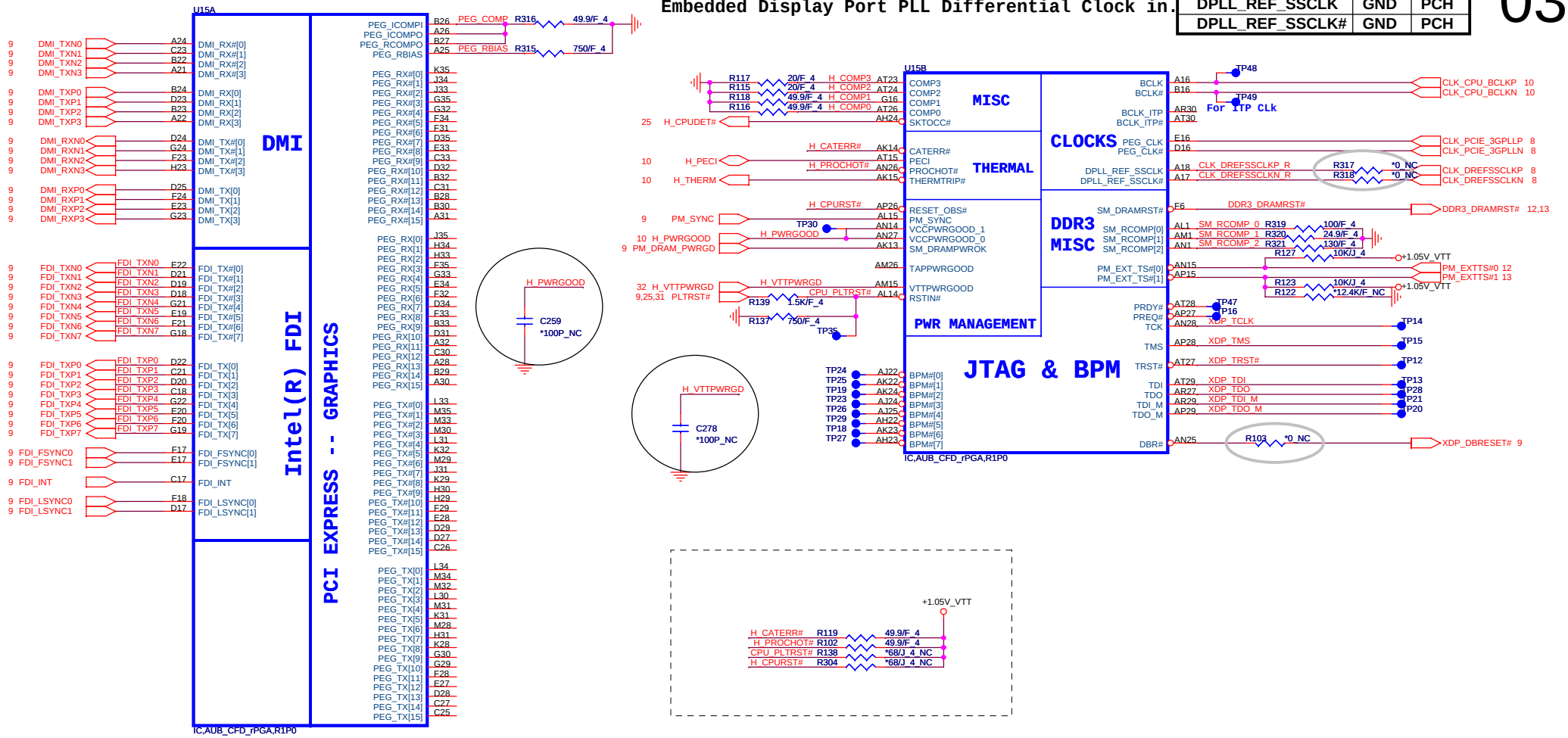
Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	Clock Gen(9LRS3197)/HOLES	1A
Date: Wednesday, February 10, 2010	Sheet 2 of 46	

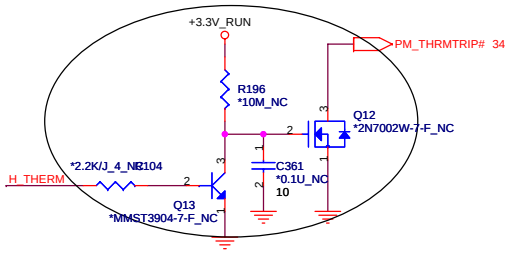
DPLL_REF_SSCLK/DPLL_REF_SSCLK#:
Embedded Display Port PLL Differential Clock in.

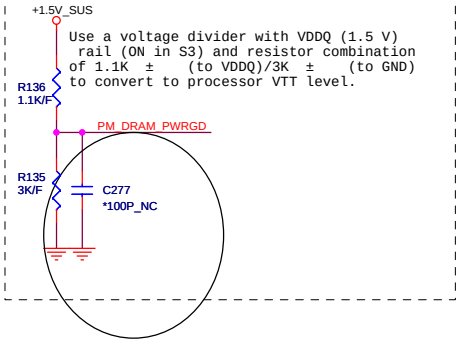
	DIS	UMA
DPLL_REF_SSCLK	GND	PCH
DPLL_REF_SSCLK#	GND	PCH

03

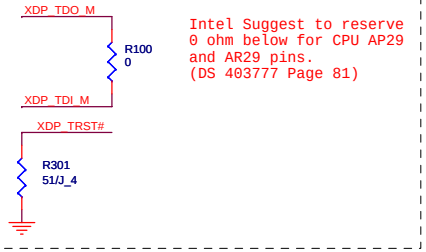


CPU THERMTRIP





JTAG MAPPING

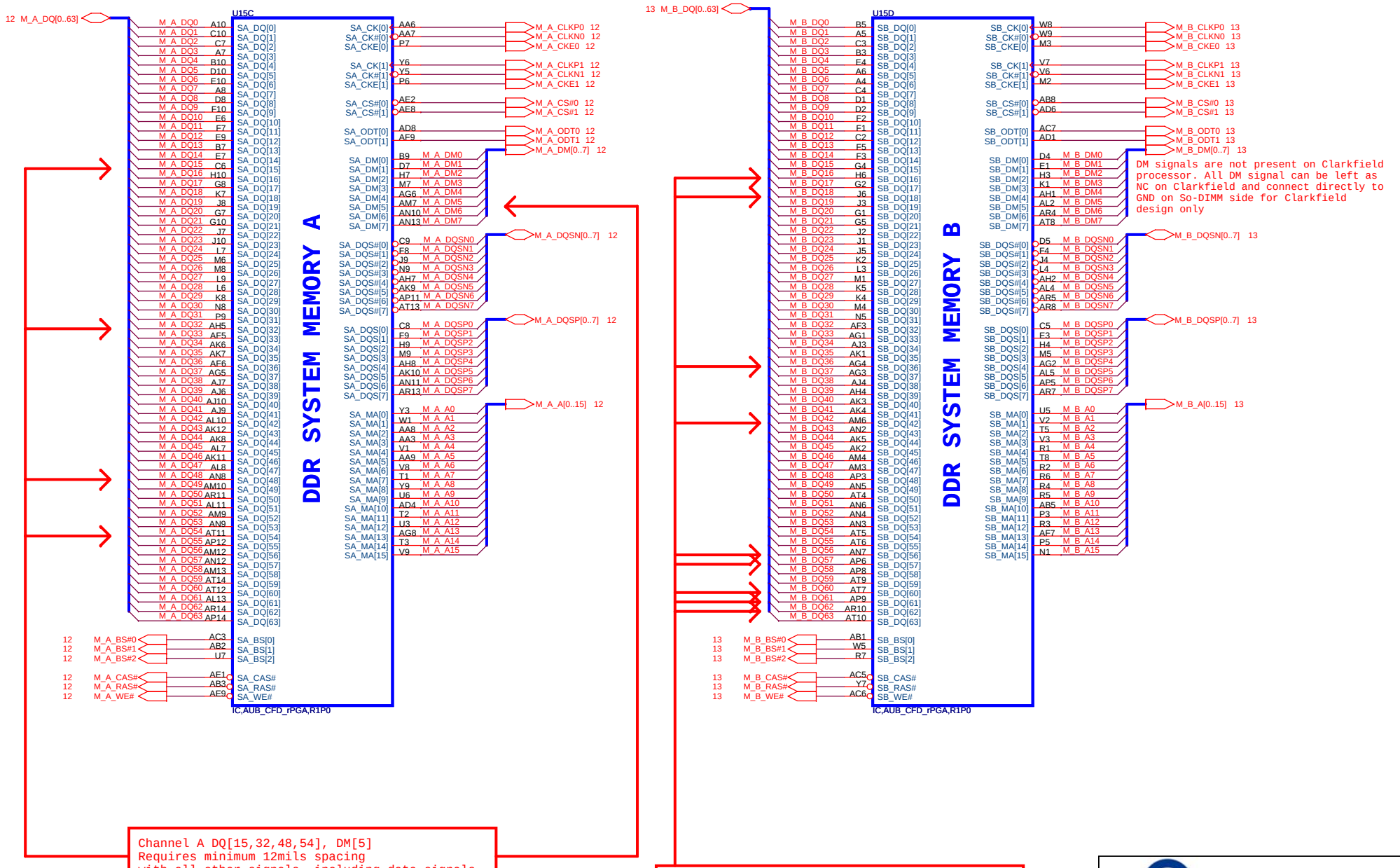


Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	PROCESSER 1/4(HOST&PEX)	1A

Date: Wednesday, February 10, 2010 Sheet 3 of 46

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.			
PROJECT : UM8 UMA			
Size	Document Number		Rev
	PROCESSER 2/4(DDR)		1A
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Name different with power

+VCC_CORE

C308 *22U/6.3V_8/X5R_NC
C329 22U/6.3V_8/X5R
C104 *22U/6.3V_8/X5R_NC
C102 22U/6.3V_8/X5R
C116 22U/6.3V_8/X5R
C128 22U/6.3V_8/X5R
C328 22U/6.3V_8/X5R
C117 22U/6.3V_8/X5R
C306 *22U/6.3V_8/X5R_NC
C319 *22U/6.3V_8/X5R_NC
C125 22U/6.3V_8/X5R
C97 22U/6.3V_8/X5R
C103 *10U/6.3V_8/X5R_NC
C330 10U/6.3V_8/X5R
C325 *10U/6.3V_8/X5R_NC
C305 10U/6.3V_8/X5R
C118 *10U/6.3V_8/X5R_NC
C307 10U/6.3V_8/X5R
C326 10U/6.3V_8/X5R
C119 10U/6.3V_8/X5R
C333 10U/6.3V_8/X5R
C320 10U/6.3V_8/X5R
C115 *10U/6.3V_8/X5R_NC
C98 10U/6.3V_8/X5R
C318 *10U/6.3V_8/X5R_NC
C332 10U/6.3V_8/X5R
C105 *10U/6.3V_8/X5R_NC
C122 *10U/6.3V_8/X5R_NC

C304 *470U_NC
C296 *470U_NC

U15F

CPU CORE SUPPLY

POWER

1.1V RAIL POWER

CPU VIDS

SENSE LINES

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

IC,AUB_CFD_rPGA,R1P0

18A

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

C341 10U/6.3V_8/X5R
C339 10U/6.3V_8/X5R
C121 10U/6.3V_8/X5R
C133 10U/6.3V_8/X5R
C124 *10U/6.3V_8/X5R_NC
C336 *10U/6.3V_8/X5R_NC
C127 *10U/6.3V_8/X5R_NC
C137 *10U/6.3V_8/X5R_NC
C136 *10U/6.3V_8/X5R_NC
C342 22U/6.3V_8/X5R
C130 22U/6.3V_8/X5R
C340 *22U/6.3V_8/X5R_NC

+1.05V_VTT

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

C139 22U/6.3V_8/X5R
C134 22U/6.3V_8/X5R

+1.05V_VTT

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

PSI# → H_PSI# 39

VID[0] VID[1] VID[2] VID[3] VID[4] VID[5] VID[6] PROC_DPRSLPVR

VID0 VID1 VID2 VID3 VID4 VID5 VID6 DPRSLPVR 39

VTT_SELECT → TP32

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

ISENSE → I_MON 39

VTT_SENSE → VTT_SENSE 37
VSS_SENSE_VTT → TP_VSS_SENSE_VTT → T28

VCC_SENSE → VCCSENSE 39
VSS_SENSE → VSSSENSE 39

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND
or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

+VCC_CORE

R97 100/F
R98 100/F

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options in the design for the Turbo functionality.
The stuffing and no-stuffing of the resistors will depend on the POC configuration of AUB and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

VTT_SELECT:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield

0525 Steg : As an option, VTT_SENSE pin on the processor can be left floating. But the platform needs to have the FB (feedback) pin of the VR tied to the VTT plane regulation.

U15G

POWER

GRAPHICS

FDI

PEG & DMI

DDR3 - 1.5V RAILS

1.1V

1.8V

SENSE LINES

GRAPHICS VIDs

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36

+VCC_GFX_CORE

C120 10U/6.3V_8/X5R
C126 10U/6.3V_8/X5R

8

+C140 330U/2V_7343
C129 22U/6.3V_8/X5R
C123 22U/6.3V_8/X5R

VTT1_45 VTT1_46 VTT1_47

+1.05V_VTT

C132 22U/6.3V_8/X5R
C327 *22U/6.3V_8/X5R_NC

VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58

+1.05V_VTT

C131 22U/6.3V_8/X5R
C138 22U/6.3V_8/X5R
C135 *22U/6.3V_8/X5R_NC
C141 *22U/6.3V_8/X5R_NC

VAXG_SENSE → VCC_AXG_SENSE 38
VSSAXG_SENSE → VSS_AXG_SENSE 38

GFX_VID[0] GFX_VID[1] GFX_VID[2] GFX_VID[3] GFX_VID[4] GFX_VID[5] GFX_VID[6]

GFXVR_VID_0 38
GFXVR_VID_1 38
GFXVR_VID_2 38
GFXVR_VID_3 38
GFXVR_VID_4 38
GFXVR_VID_5 38
GFXVR_VID_6 38

GFX_VR_EN → GFXVR_EN 38
GFX_DPRSLPVR
GFX_IMON → GFXVR_IMON 38

R306 4.7K/F_4
R114 *1K/F_4_NC

2A

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18

+1.5V_SUS

C147 1U/6.3V/X5R
C149 1U/6.3V/X5R
C148 1U/6.3V/X5R
C146 1U/6.3V/X5R
C145 1U/6.3V/X5R
C150 22U/6.3V_8/X5R
C151 *22U/6.3V_8/X5R_NC
C152 330U/2V_7343

VTT0_59 VTT0_60 VTT0_61 VTT0_62 VTT1_63 VTT1_64 VTT1_65 VTT1_66 VTT1_67 VTT1_68

+1.05V_VTT

C337 10U/6.3V_8/X5R
C338 *10U/6.3V_8/X5R_NC
C331 22U/6.3V_8/X5R
C335 *22U/6.3V_8/X5R_NC

VCCPLL1 VCCPLL2 VCCPLL3

+1.8V_RUN

C114 22U/6.3V_8/X5R
C324 4.7U/6.3V/X5R
C323 2.2U/ 6.3V/X5R
C322 1U/6.3V/X5R
C321 1U/6.3V/X5R

IC,AUB_CFD_rPGA,R1P0

VID0 VID1 VID2 VID3 VID4 VID5 VID6 DPRSLPVR H_PSI#

R280 1K/J_4
R290 *1K/J_4_NC
R288 1K/J_4
R298 *1K/J_4_NC
R281 1K/J_4
R291 *1K/J_4_NC
R282 *1K/J_4_NC
R292 1K/J_4
R283 *1K/J_4_NC
R293 1K/J_4
R287 1K/J_4
R297 *1K/J_4_NC
R284 *1K/J_4_NC
R294 1K/J_4
R285 1K/J_4
R295 *1K/J_4_NC
R286 *1K/J_4_NC
R296 1K/J_4

+1.05V_VTT

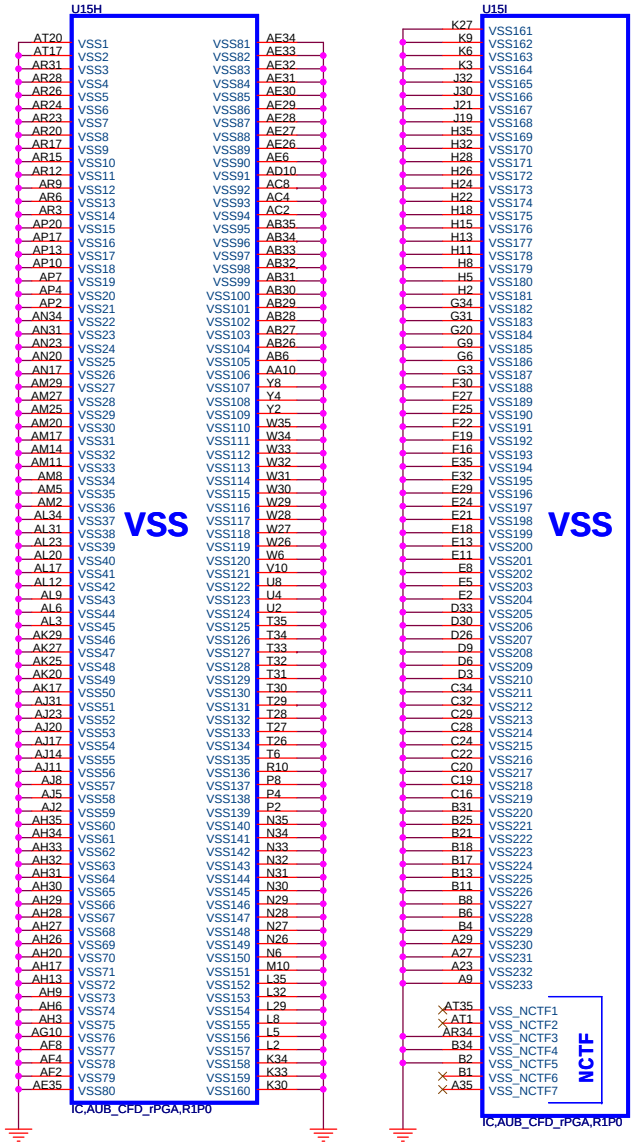
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

Quanta Computer Inc.
PROJECT : UM8 UMA

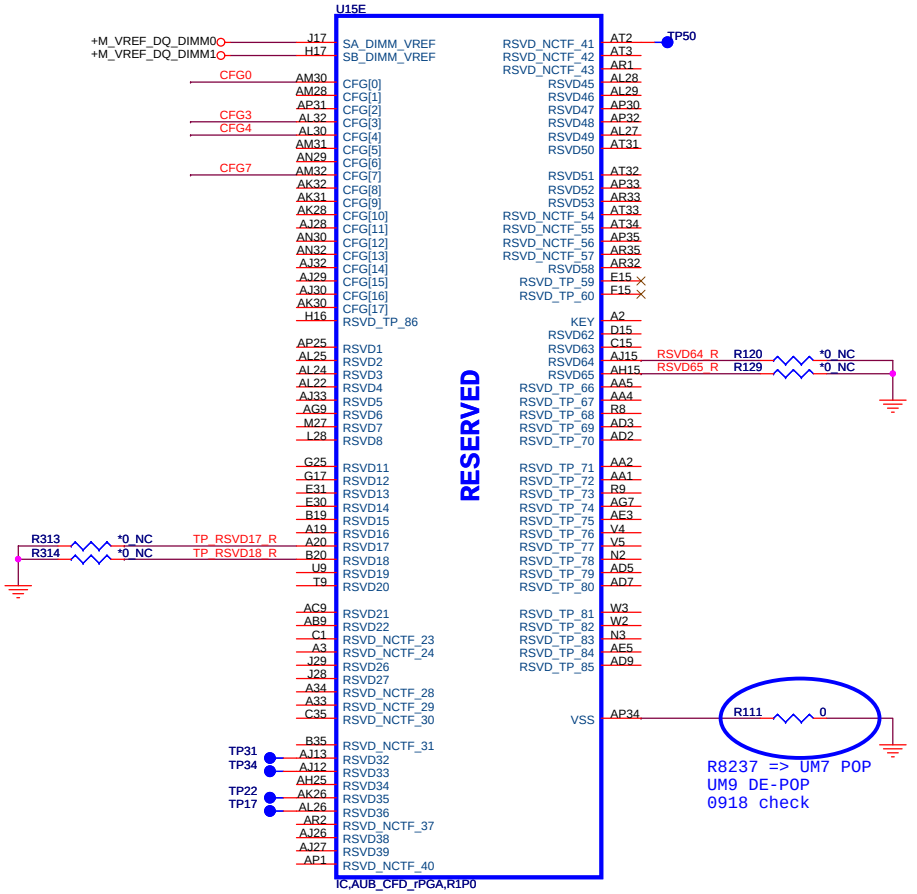
Size	Document Number	Rev
	PROCESSER 3/4(POWER)	1A

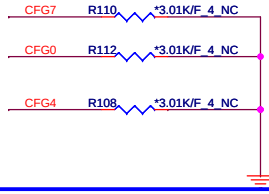
Date: Wednesday, February 10, 2010 Sheet 5 of 46

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)





	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	PROCESSER 4/4 (GND)	1A

Date: Wednesday, February 10, 2010 Sheet 6 of 46

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U14A — Ibex-M 1 OF 10

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN
IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN# / GPIO33 (+3V), HDA_DOCK_RST# / GPIO13 (+3V_S5)
JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, TRST#
SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO
LPC: FWH0 / LAD0, FWH1 / LAD1, FWH2 / LAD2, FWH3 / LAD3, FWH4 / LFRAME#, LDRQ0#, (+3V) LDRQ1# / GPIO23, SERIRQ
SATA: SATA0RXN/RXP/TXN/TXP, SATA1RXN/RXP/TXN/TXP, SATA2RXN/RXP/TXN/TXP, SATA3RXN/RXP/TXN/TXP, SATA4RXN/RXP/TXN/TXP, SATA5RXN/RXP/TXN/TXP, SATAICOMPO, SATAICOMPI, SATALED#, (+3V) SATA0GP / GPIO21, (+3V_S5) SATA1GP / GPIO19

IbexPeak-M_Rev1_0

C287 18P/50V_4/COG, C288 18P/50V_4/COG, Y5 32.768KHZ, R265 10M/J_4
RTC_X1 B13, RTC_X2 D13, T25 PAD RTC_RST# C14, T26 PAD SRTC_RST# D17, SM_INTRUDER# A16, +RTC_CELL R266 330K/J_6 PCH_INVRMEN A14, T24 PAD

ACZ_BITCLK A30, ACZ_SYNC D29, ACZ_SDOUT B29, PCH_GPIO33 H32, ACZ_RST# C30, ACZ_SDIN0 G30
31 ACZ_SPKR, 31 ACZ_SDIN0, 25 PCH_MELOCK, R339 *0_NC

TP37 PCH_JTAG_TCK_BUF M3, TP38 PCH_JTAG_TMS K3, TP39 PCH_JTAG_TDI K1, TP40 PCH_JTAG_TDO J2, TP41 PCH_JTAG_RST# J4
must add test point.

26 SPI_CLK BA2, 26 SPI_CS0# AV3, TP4, TP43 SPI_CS1# AY3
26 SPI_SI AY1, TP6, 26 SPI_SO AV1, TP5, TP3, C362 *100P/NPO_NC

SATA port 2/3 are not support in HM55 . They are only in PM 55

SATA0RXN/RXP/TXN/TXP → SATA_RXN0/RXP0/TXN0/TXP0 28
SATA1RXN/RXP/TXN/TXP → SATA_RXN1/RXP1/TXN1/TXP1 28
SATA2RXN/RXP/TXN/TXP → ESATA: SATA_RXN4/RXP4/TXN4/TXP4 27
SATA3RXN/RXP/TXN/TXP → HDD
SATA4RXN/RXP/TXN/TXP → ESATA
SATA5RXN/RXP/TXN/TXP → ODD

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

SATAICOMPO — SATA_COMP R58 37.4/F_4 +1.05V_PCH
SATALED# T3 — SATA_LED# 29
SATA_DET0# Y9, SATA_DET1# V1

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

R242 10K/J_4 SATA_LED#
+3.3V_RUN — R37 10K/J_4 SATA_DET0#, R240 10K/J_4 SATA_DET1#

Serial ATA LED: This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required.

Flash Descriptor Security Override

GPIO33	Low = Enabled High = Disabled

R62 1 2 *1K_NC PCH_GPIO33
(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

iTPM ENABLE/DISABLE

+3.3V_RUN — R263 *1K_NC SPI_SI

TPM Function	
Enable	Mount
Disable	NC (Default)

For AUDIO

25,31 ACZ_RST#_AUDIO — R276 33/J_4 ACZ_RST#
31 ACZ_SDOUT_AUDIO — R273 33/J_4 ACZ_SDOUT, C292 *10P/50V_4_NC/COG
31 ACZ_SYNC_AUDIO — R274 33/J_4 ACZ_SYNC, C293 *10P/50V_4_NC/COG
31 ACZ_BITCLK_AUDIO — R275 33/J_4 ACZ_BITCLK, C294 10P/50V_4/COG

+3.3V_RUN — R226 *1K/F_4_NC ACZ_SPKR

No Reboot strap.	
SPKR	Low = Default. High = No Reboot.

RTC

1mA
+RTC_CELL
R267 20K/F_4 — C289 1U/6.3V/X5R — RTC_RST#
R271 20K/F_4 — C291 1U/6.3V/X5R — SRTC_RST#
R268 1M/J_4 — SM_INTRUDER#

UMA CRT,LVDS&HDMI signals
IBEX PEAK-M (LVDS,DDI)

U14D — Ibex-M 4 OF 10

LVDS--A: L_BKLTEN, L_VDD_EN, L_BKLTCTL, L_DDC_CLK, L_DDC_DATA, L_CTRL_CLK, L_CTRL_DATA, LVD_IBG, LVD_VBG, LVD_VREFH, LVD_VREFL, LVDSA_CLK#, LVDSA_CLK, LVDSA_DATA#0..#3
LVDS--B: LVDSB_CLK#, LVDSB_CLK, LVDSB_DATA#0..#3
CRT: CRT_BLUE, CRT_GREEN, CRT_RED, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_VSYNC, DAC_IREF, CRT_IRTN
SDVO: SDVO_TVCLKINN/INP, SDVO_STALLN/STALLP, SDVO_INTN/INTP, SDVO_CTRLCLK/CTRLDATA
DISPLAY PORT B: DDPB_AUXN/AUXP/HPD, DDPB_0N..3P
DISPLAY PORT C: DDPC_CTRLCLK/CTRLDATA, DDPC_AUXN/AUXP/HPD, DDPC_0N..3P
DISPLAY PORT D: DDPD_CTRLCLK/CTRLDATA, DDPD_AUXN/AUXP/HPD, DDPD_0N..3P
Digital Display Interface

22,25 PANEL_BKEN, 22 ENVDD, 22 BIA_PWM, 22 LCD_DDCCLK, 22 LCD_DDCDAT, L_CTRL_CLK, L_CTRL_DATA
R65 2.37K/F_4 — T6 PAD — LVDS_VBG
T3 PAD, T10 PAD
22 LCD_ACLK-, 22 LCD_ACLK+
22 LCD_A0-, 22 LCD_A1-, 22 LCD_A2- — T8 PAD — INT_TXLOUTN3
22 LCD_A0+, 22 LCD_A1+, 22 LCD_A2+ — T9 PAD — INT_TXLOUTP3
T13 PAD, T12 PAD
31 VGA_BLU, 31 VGA_GRN, 31 VGA_RED
31 DDCCLK, 31 DDCDATA
31 VGAHSYNC — R85 33/J_4, 31 VGAVSYNC — R84 33/J_4
R78 1K/D_4

UMA 0.5%
DIS 1%

+3.3V_RUN — R92 2.2K/J_4, R91 2.2K/J_4
HDMI_SCL, HDMI_SDA 24
INT_HDMI_HPD
25
INT_HDMI_TXDN0/TXDP0 C76/C74, TXDN1/TXDP1 C73/C71, TXDN2/TXDP2 C68/C66, TXCN C62, TXCP C57
0.1U/10V_4/K7R
INT_HDMI_TXDN2_C 24, INT_HDMI_TXDP2_C 24, INT_HDMI_TXDN1_C 24, INT_HDMI_TXDP1_C 24, INT_HDMI_TXDN0_C 24, INT_HDMI_TXDP0_C 24, INT_HDMI_TXCN_C 24, INT_HDMI_TXCP_C 24

Close to VGA side
35
VGA_BLU — R95 150/F_4 — C592 *22P_NC
VGA_GRN — R83 150/F_4 — C593 *22P_NC
VGA_RED — R94 150/F_4 — C594 *22P_NC
50

PANEL_BKEN R76 100K/J_4
ENVDD R77 100K/J_4
LCD_DDCDAT R90 2.2K/J_4
LCD_DDCCLK R89 2.2K/J_4
L_CTRL_CLK R86 10K/F_4
L_CTRL_DATA R87 10K/F_4
+3.3V_RUN
+5V_RUN — Q11 2N7002K-T1-E3
INT_HDMI_HPD — R74 100K/J_4, R96 *0/J_4_NC — HDMI_DET 24

+3.3V_SUS Res. of TDI near PCH
R228 *200_NC, R229 *200_NC, R230 *200_NC, R231 20K/F_4_NC
PCH_JTAG_TMS, PCH_JTAG_TDI, PCH_JTAG_TDO, PCH_JTAG_RST#
R245 *100_NC, R246 *100_NC, R247 *100_NC, R248 *10K_NC

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

R244 51/J_4 PCH_JTAG_TCK_BUF

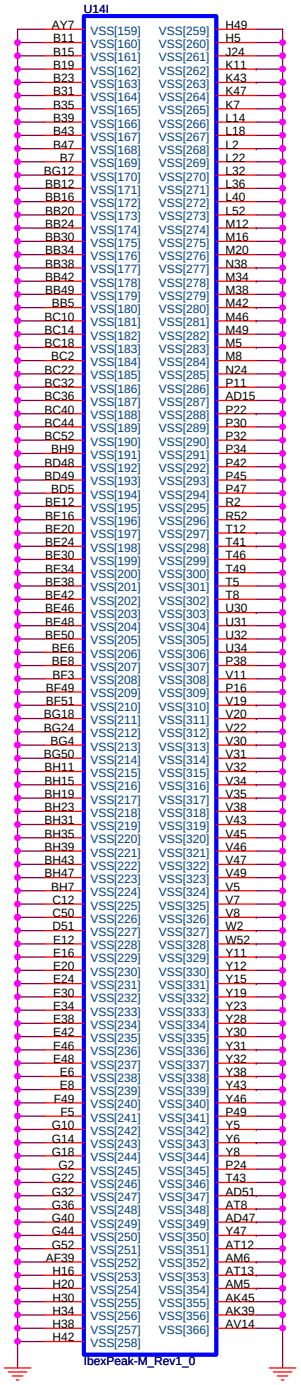
Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	1A

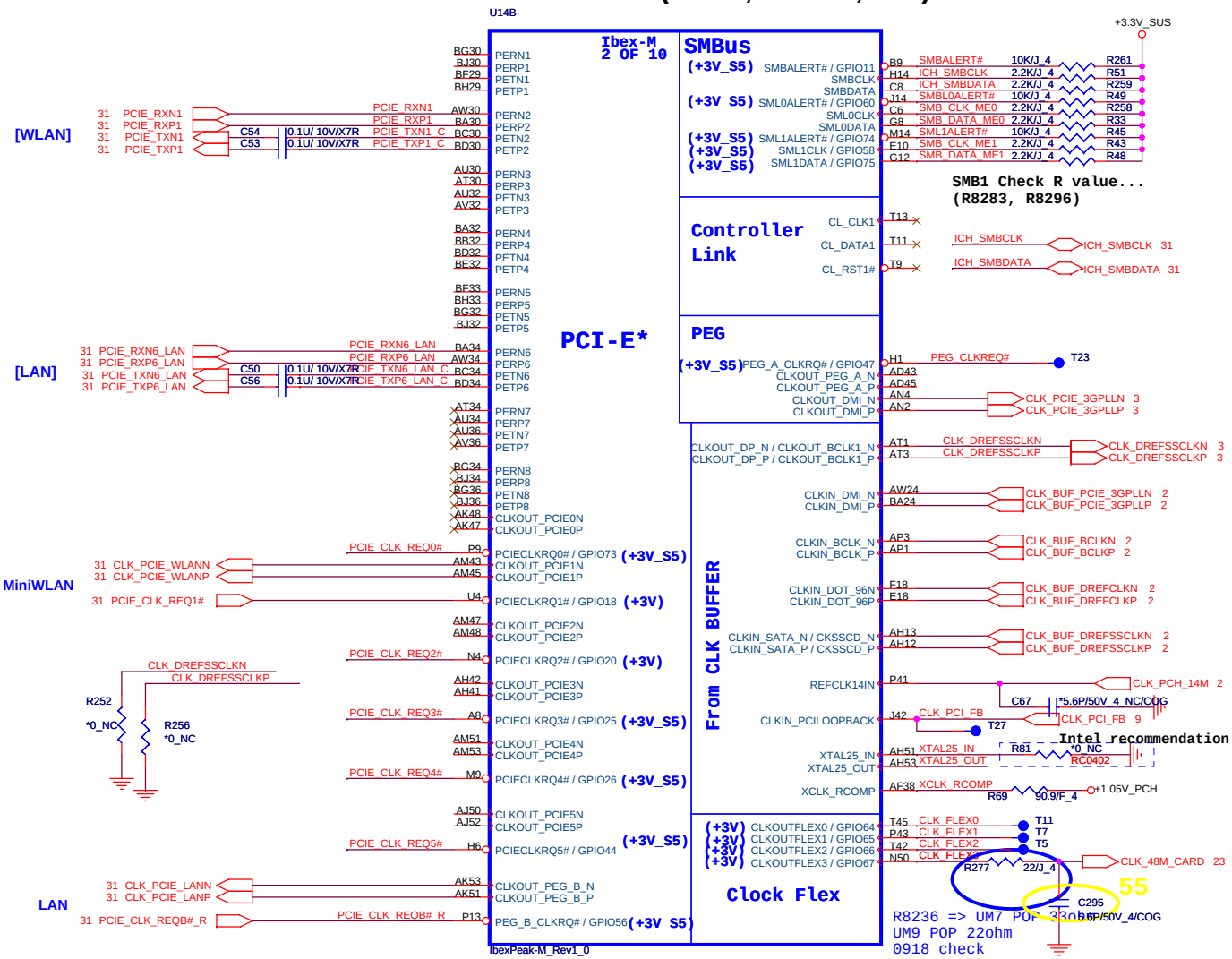
Date: Wednesday, February 10, 2010 Sheet 7 of 46

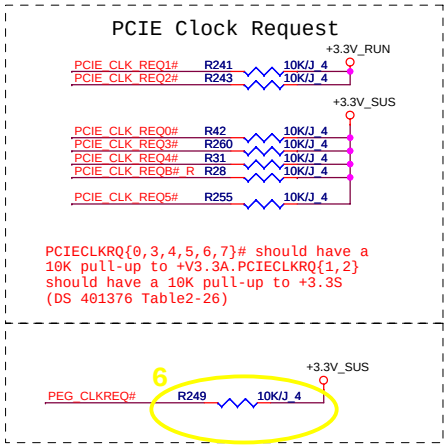
IBEX PEAK-M (GND)



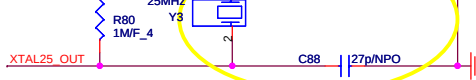
IBEX PEAK-M (PCI-E,SMBUS,CLK)

08





UMA	POP Y8201, C8411, C8412 and R8401, de-POP R8999 for Internal GFX
DIS	de-POP Y8201, C8411, C8412 and R8401, POP R8999 for Internal GFX

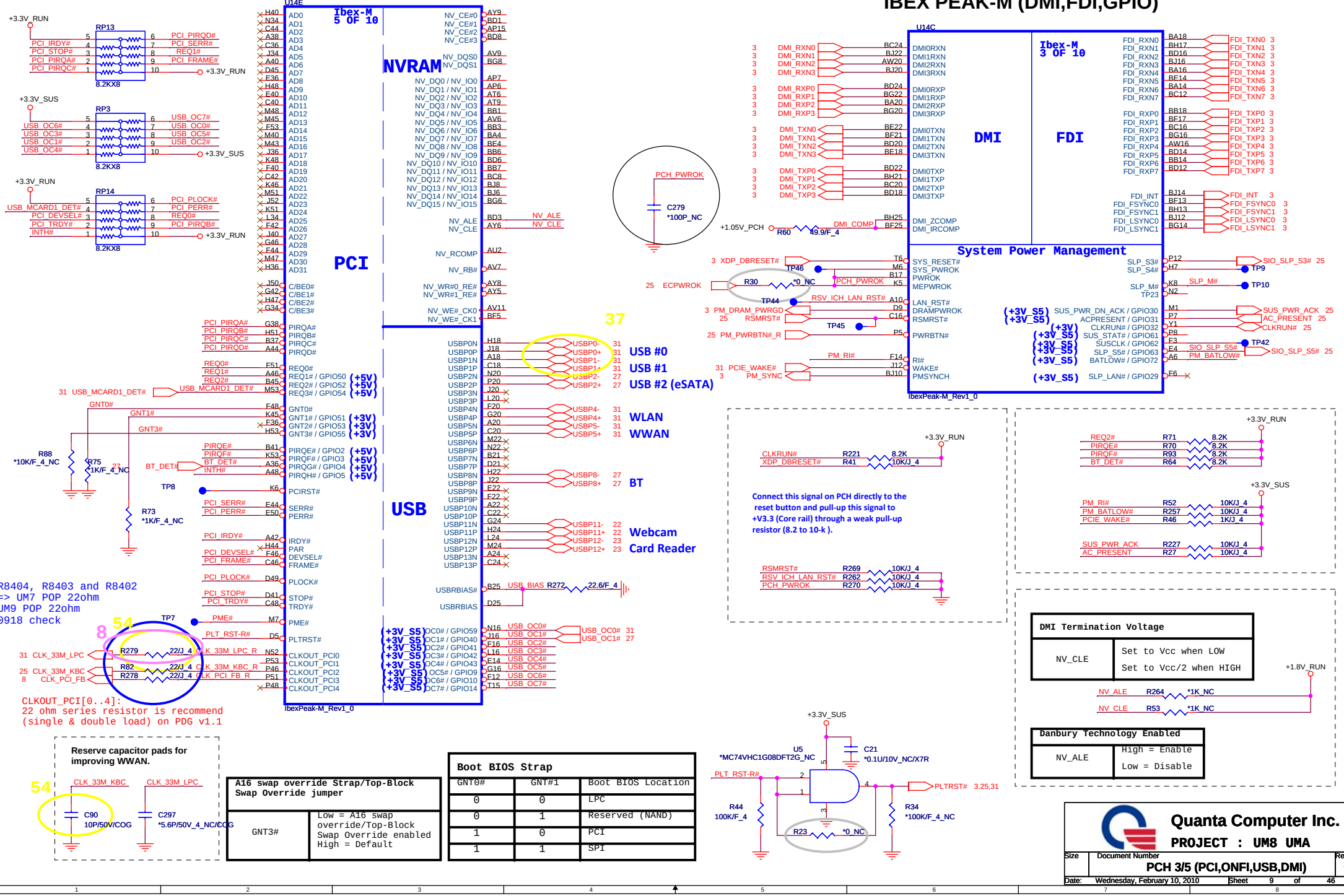


Quanta Computer Inc.	PROJECT : UM8 UMA
Size	Document Number: PCH 2/5 (PCIE, SMBUS, CK) — Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 8 of 46

IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)

09



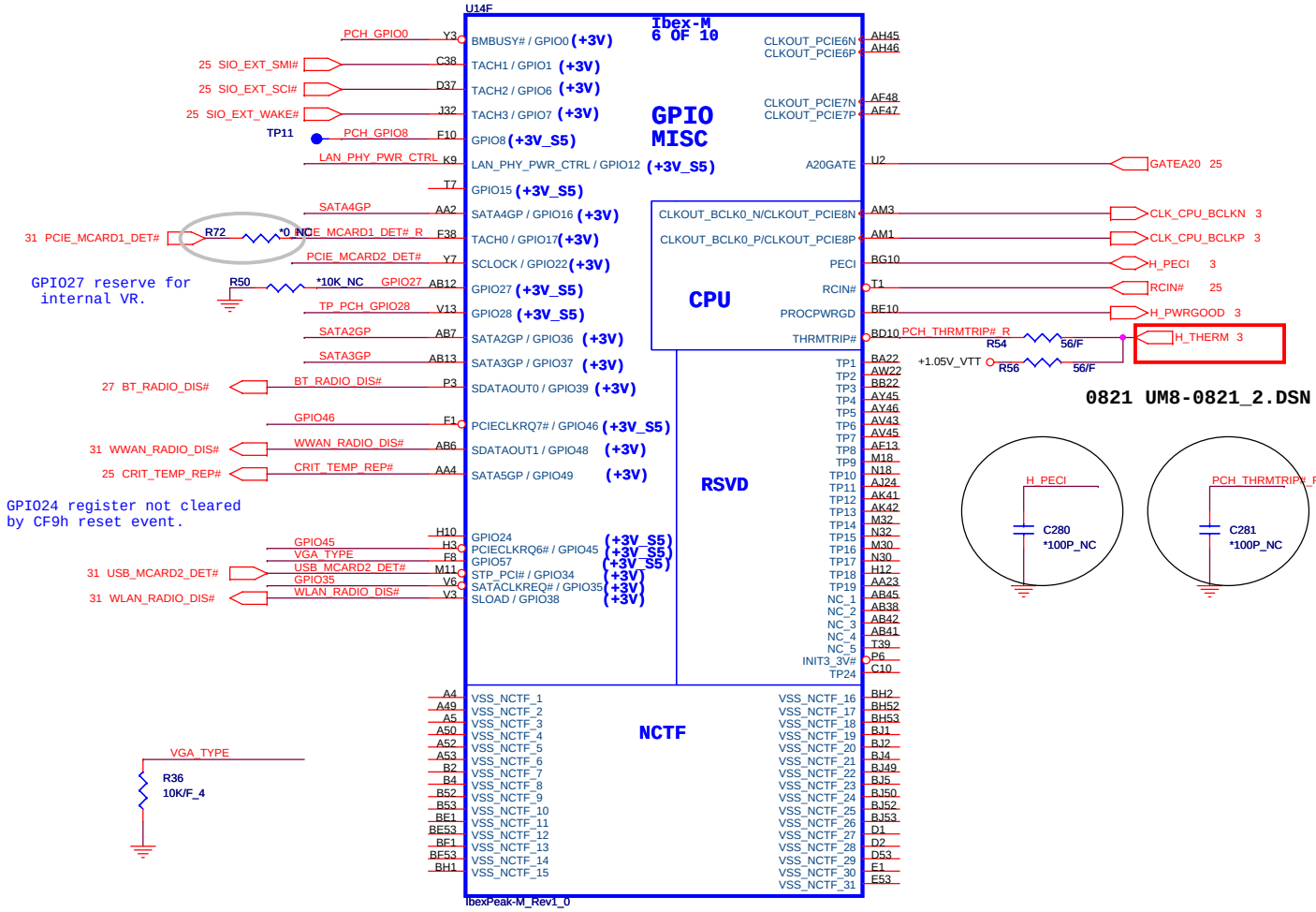
Quanta Computer Inc.

PROJECT : UM8 UMA

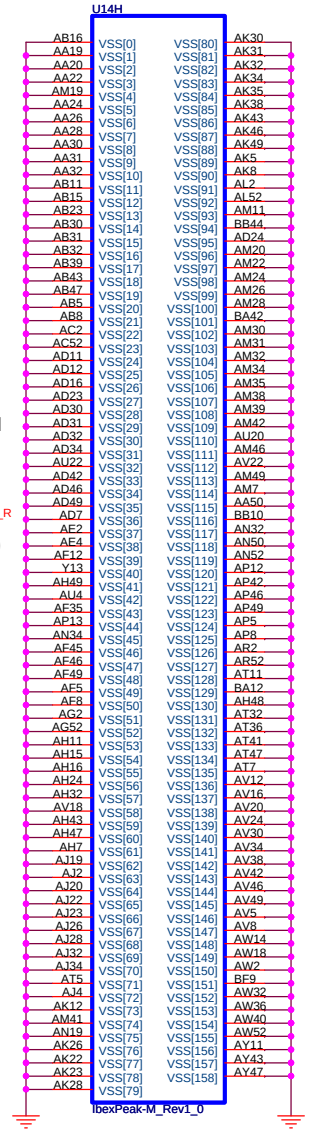
Size	Document Number	Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)	1A

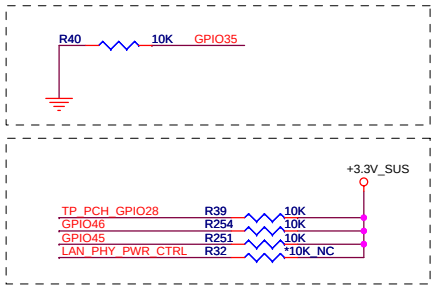
Date: Wednesday, February 10, 2010 Sheet 9 of 46

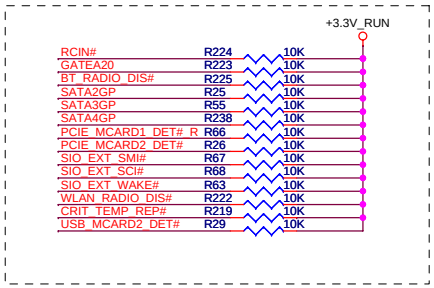
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

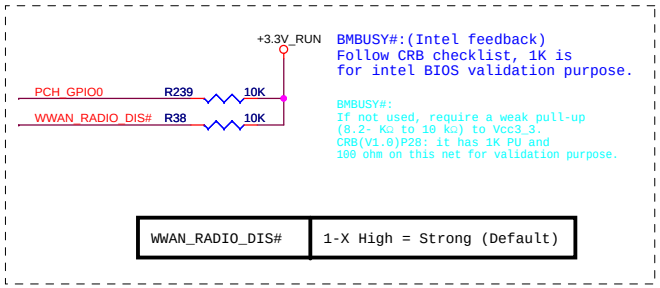


IBEX PEAK-M (GND)









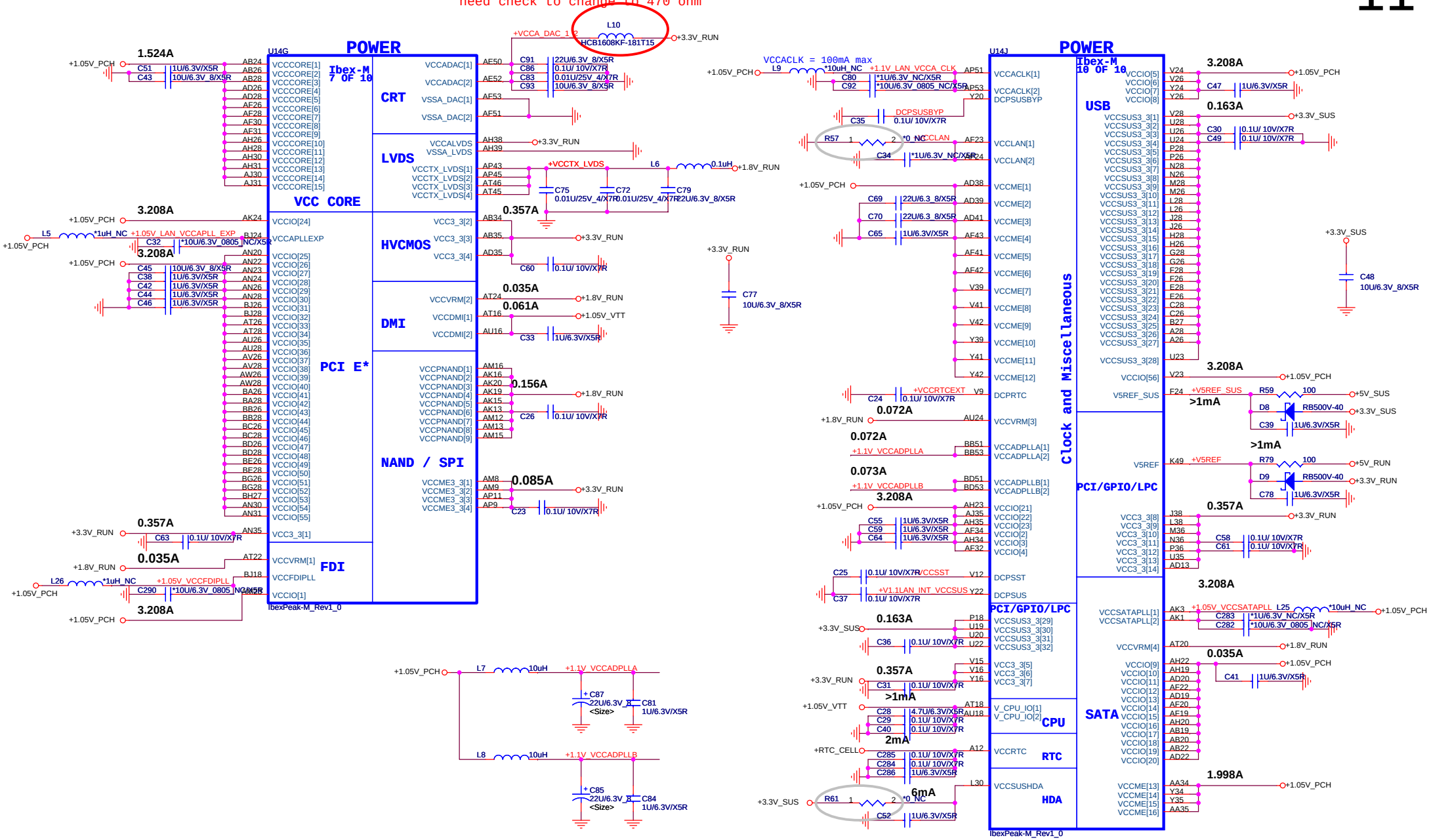
Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	1A
Date: Wednesday, February 10, 2010	Sheet 10 of 46	

Cap quantities follow UM3

need check to change to 470 ohm



Quanta Computer Inc.			
PROJECT : UM8 UMA			
Size	Document Number		Rev
	PCH 5/5 (POWER)		1A
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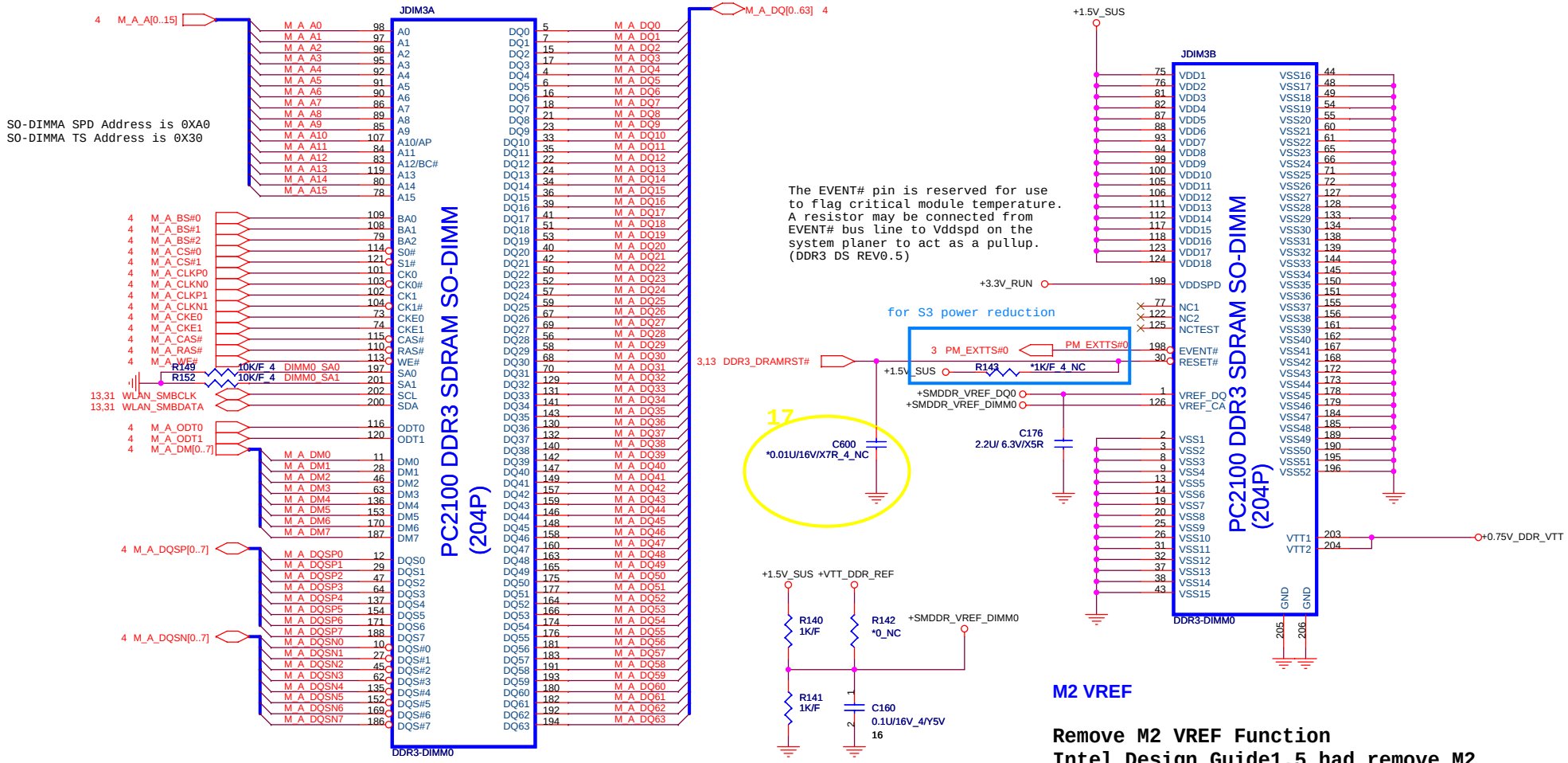


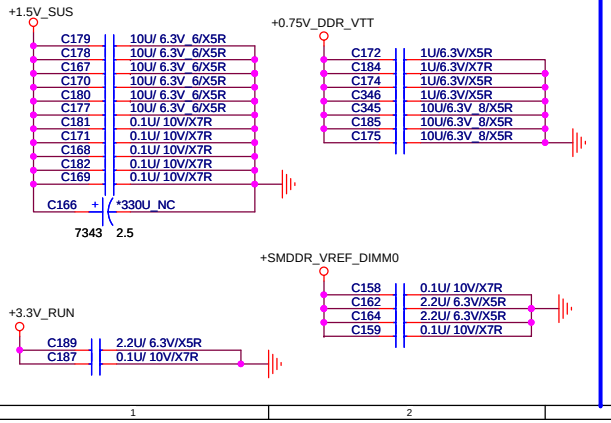
M2 VREF

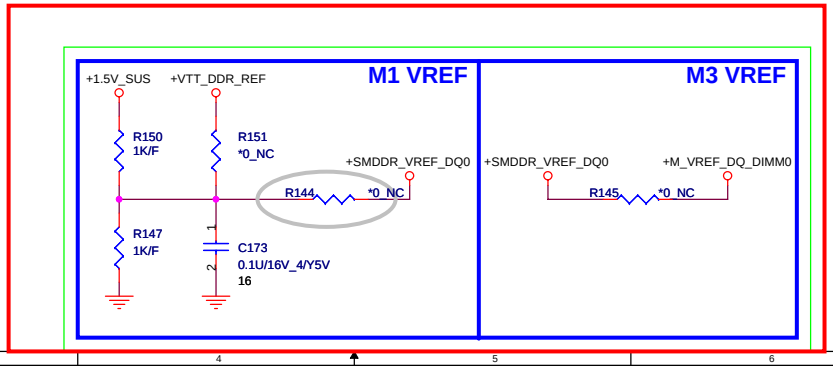
Remove M2 VREF Function
Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarksfield processor

Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

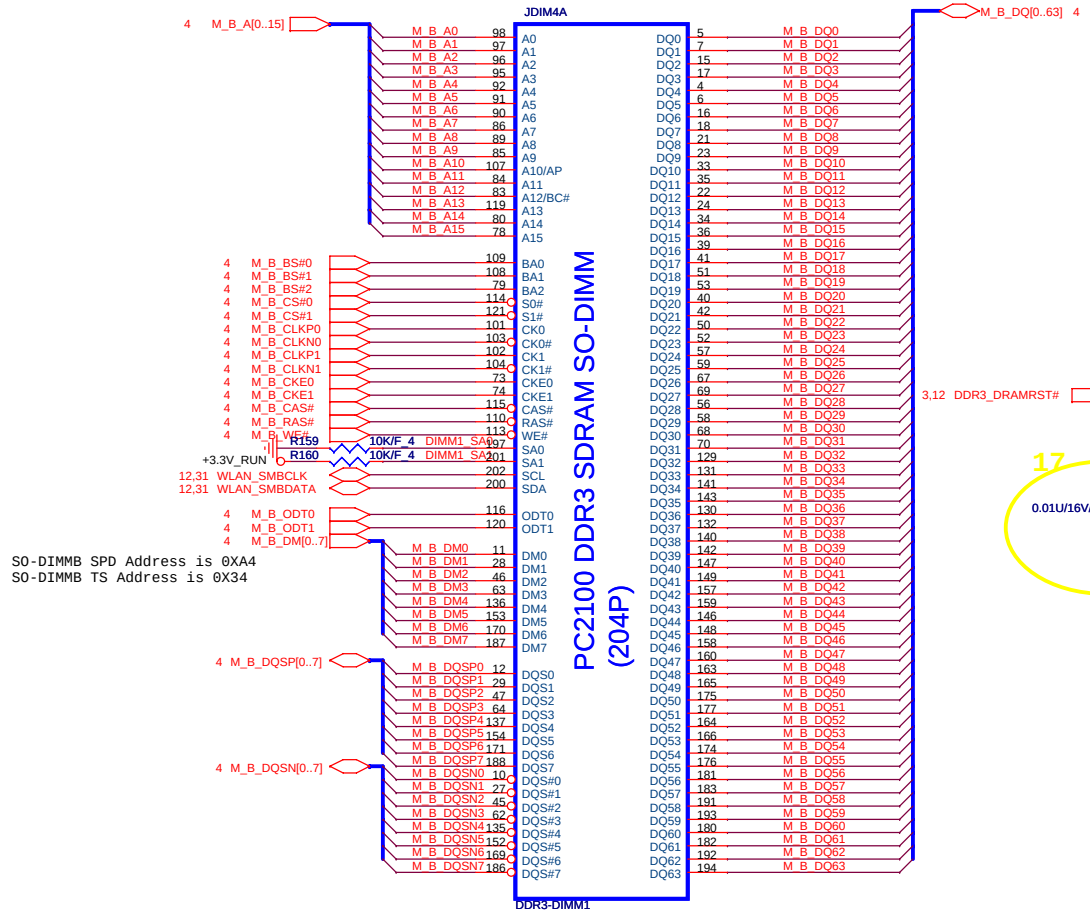


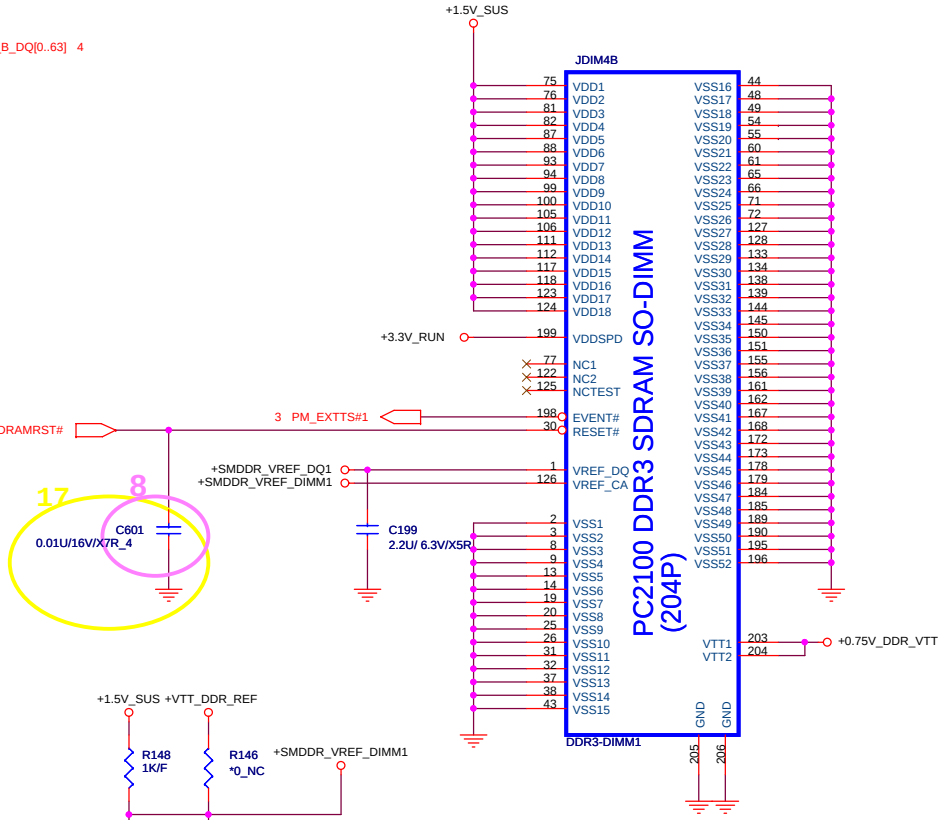


Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	DDR3 DIMM-0	1A

Date: Wednesday, February 10, 2010 Sheet 12 of 46



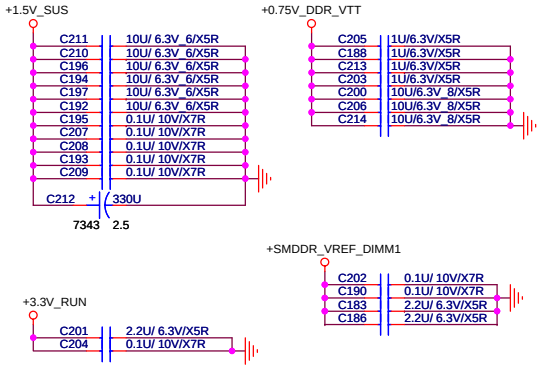


Remove M2 VREF Function
Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarksfield processor

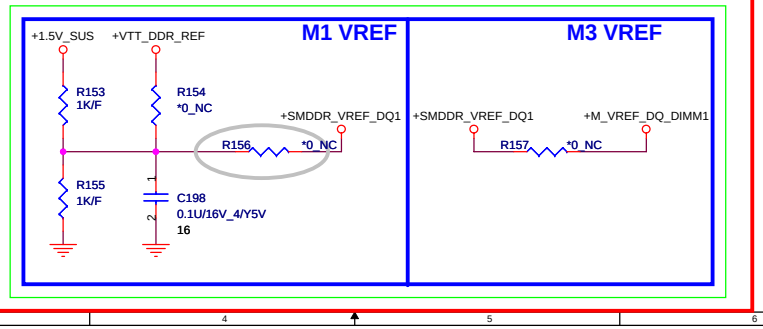
Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



Wait Victor check

for arrandal nc, for clesfied connect



Quanta Computer Inc.		
PROJECT : UM8 UMA		
Size	Document Number: DDR3 DIMM-1	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 13 of 46	

Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	Blank	1A

Date: Wednesday, February 10, 2010 Sheet 14 of 46

Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	Blank	1A

Date: Wednesday, February 10, 2010 Sheet 15 of 46

Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	Blank	1A

Date: Wednesday, February 10, 2010 Sheet 16 of 46

Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	Blank	1A

Date: Wednesday, February 10, 2010 Sheet 17 of 46

Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	Blank	1A

Date: Wednesday, February 10, 2010 Sheet 18 of 46

Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	Blank	1A

Date: Wednesday, February 10, 2010 Sheet 19 of 46

Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	Blank	1A

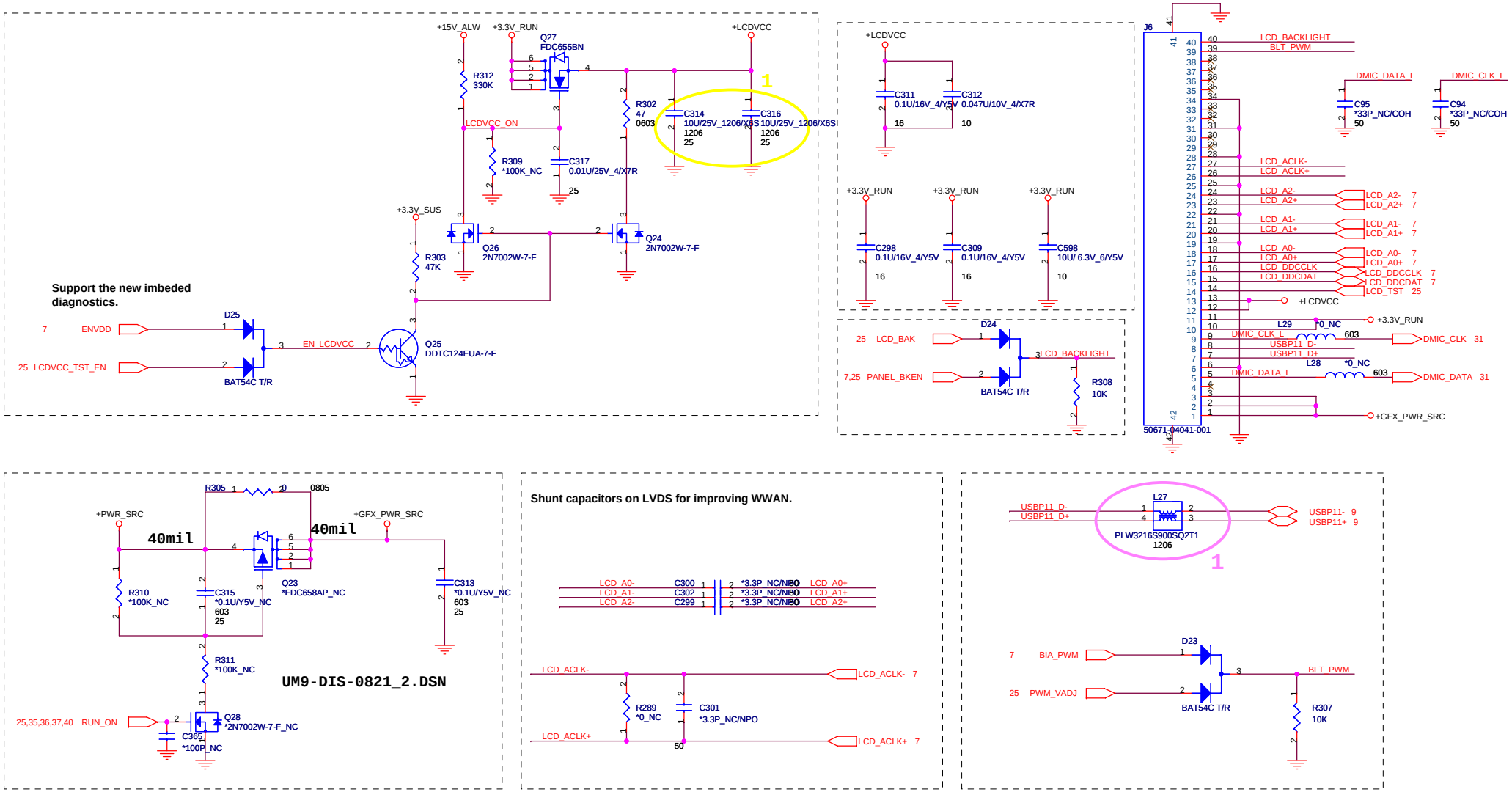
Date: Wednesday, February 10, 2010 Sheet 20 of 46

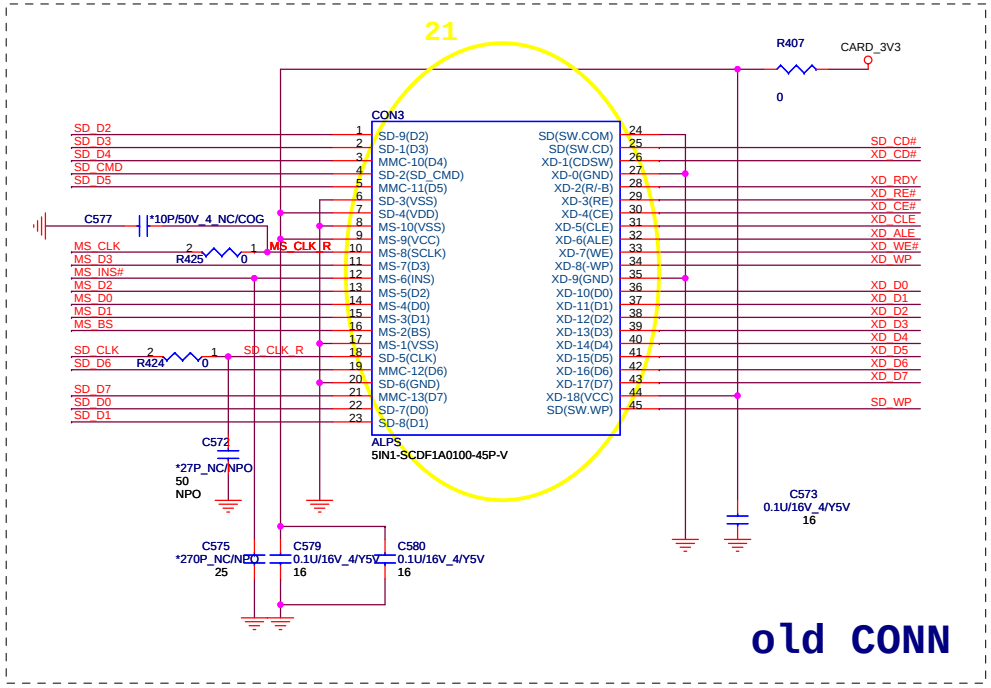
Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	Blank	1A

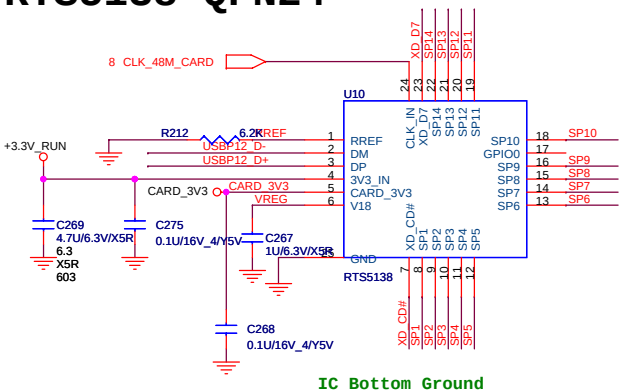
Date: Wednesday, February 10, 2010 Sheet 21 of 46


Support the new imbeded diagnostics.
+15V_ALW
+3.3V_RUN
+LCDVCC
Q27 FDC655BN
R312 330K
LCDVCC_ON
R309 *100K_NC
C317 0.01U/25V_4/X7R
R302 47 0603
C314 10U/25V_1206/X6S 1206 25
C316 10U/25V_1206/X6S 1206 25
+3.3V_SUS
Q26 2N7002W-7-F
Q24 2N7002W-7-F
R303 47K
D25
7 ENVDD
25 LCDVCC_TST_EN
EN_LCDVCC
BAT54C T/R
Q25 DDTC124EUA-7-F
C311 0.1U/16V_4/Y5V
C312 0.047U/10V_4/X7R
C298 0.1U/16V_4/Y5V
C309 0.1U/16V_4/Y5V
C598 10U/ 6.3V_6/Y5V
D24
25 LCD_BAK
7,25 PANEL_BKEN
LCD_BACKLIGHT
R308 10K
J6
50671-04041-001
LCD_BACKLIGHT
BLT_PWM
DMIC_DATA_L
DMIC_CLK_L
C95 *33P_NC/COH
C94 *33P_NC/COH
LCD_ACLK-
LCD_ACLK+
LCD_A2-
LCD_A2+
LCD_A1-
LCD_A1+
LCD_A0-
LCD_A0+
LCD_DDCCLK
LCD_DDCDAT
LCD_TST
L29 *0_NC
L28 *0_NC
USBP11_D-
USBP11_D+
+GFX_PWR_SRC
R305 0 0805
+PWR_SRC
+GFX_PWR_SRC
40mil
40mil
Q23 *FDC658AP_NC
R310 *100K_NC
C315 *0.1U/Y5V_NC 603 25
C313 *0.1U/Y5V_NC 603 25
R311 *100K_NC
UM9-DIS-0821_2.DSN
25,35,36,37,40 RUN_ON
Q28 *2N7002W-7-F_NC
C365 *100P_NC
Shunt capacitors on LVDS for improving WWAN.
C300 C302 C299 *3.3P_NC/NPO
R289 *0_NC
C301 *3.3P_NC/NPO
50
L27
PLW3216S900SQ2T1 1206
USBP11- 9
USBP11+ 9
7 BIA_PWM
25 PWM_VADJ
D23
BAT54C T/R
R307 10K
Quanta Computer Inc.
PROJECT : UM8B DIS
Size
Document Number
LCD CONN
Rev 1A
Date: Wednesday, February 10, 2010
Sheet 22 of 46



old CONN

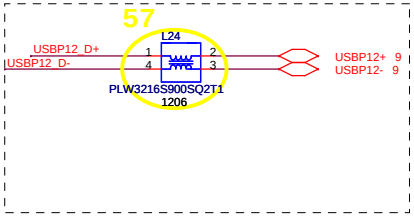
RTS5138-QFN24



IC Bottom Ground

SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

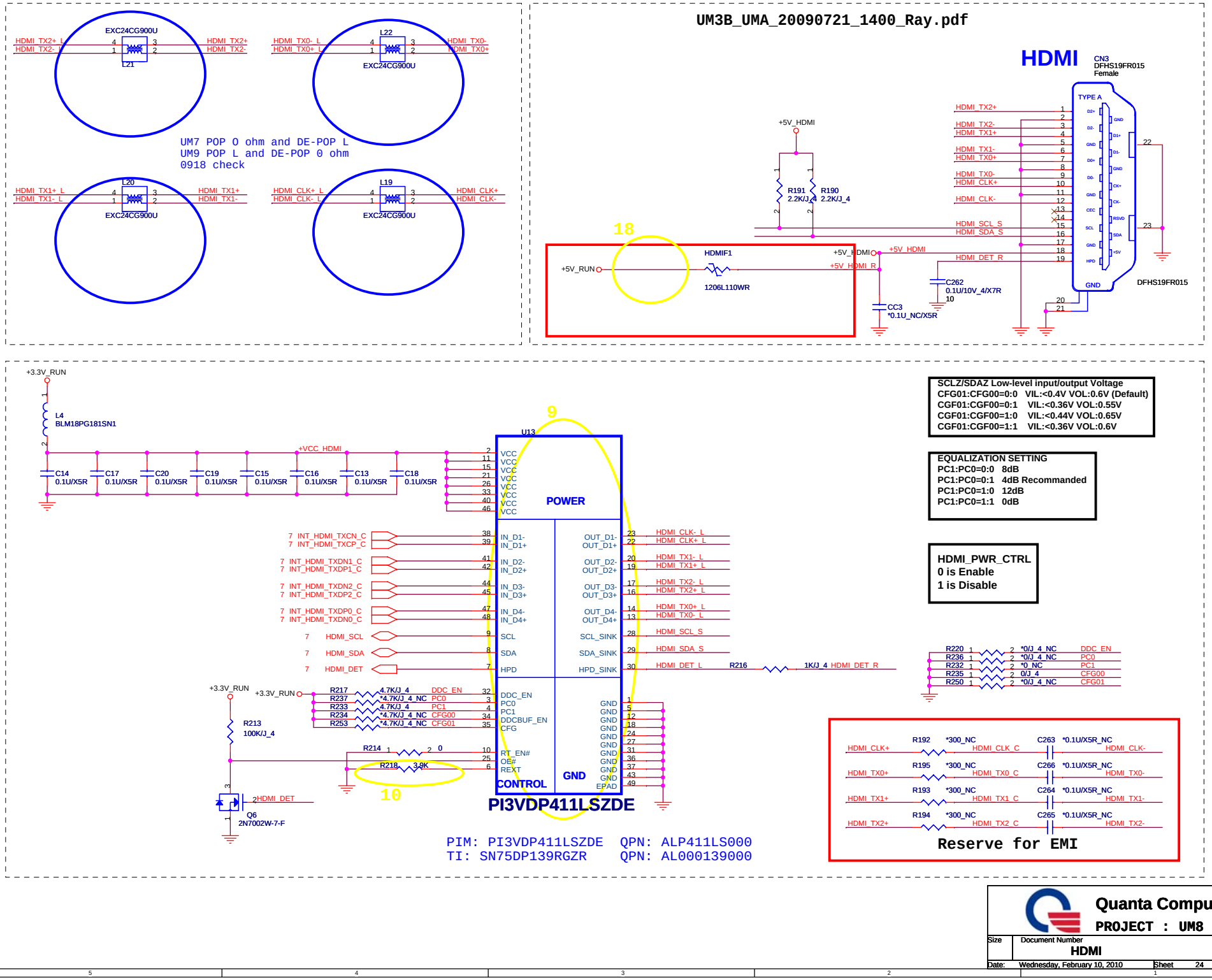
Share Pin



Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	Card Reader(RST5138)	1A
Date: Wednesday, February 10, 2010	Sheet 23 of 46	


UM3B_UMA_20090721_1400_Ray.pdf
EXC24CG900U
L21
L22
L20
L19
HDMI_TX2+_L
HDMI_TX2-_L
HDMI_TX2+
HDMI_TX2-
HDMI_TX0-_L
HDMI_TX0+_L
HDMI_TX0-
HDMI_TX0+
HDMI_TX1+_L
HDMI_TX1-_L
HDMI_TX1+
HDMI_TX1-
HDMI_CLK+_L
HDMI_CLK-_L
HDMI_CLK+
HDMI_CLK-
UM7 POP 0 ohm and DE-POP L
UM9 POP L and DE-POP 0 ohm
0918 check
HDMI
CN3
DFHS19FR015
Female
TYPE A
DFHS19FR015
+5V_HDMI
R191
2.2K/J_4
R190
2.2K/J_4
HDMI_SCL_S
HDMI_SDA_S
HDMI_DET_R
18
HDMIF1
+5V_RUN
1206L110WR
+5V_HDMI_R
C262
0.1U/10V_4/X7R
10
CC3
*0.1U_NC/X5R
+3.3V_RUN
L4
BLM18PG181SN1
+VCC_HDMI
C14
C17
C20
C19
C15
C16
C13
C18
0.1U/X5R
U13
9
POWER
VCC
IN_D1-
IN_D1+
IN_D2-
IN_D2+
IN_D3-
IN_D3+
IN_D4-
IN_D4+
SCL
SDA
HPD
DDC_EN
PC0
PC1
DDCBUF_EN
CFG
RT_EN#
OE#
REXT
OUT_D1-
OUT_D1+
OUT_D2-
OUT_D2+
OUT_D3-
OUT_D3+
OUT_D4-
OUT_D4+
SCL_SINK
SDA_SINK
HPD_SINK
GND
CONTROL
EPAD
PI3VDP411LSZDE
10
INT_HDMI_TXCN_C
INT_HDMI_TXCP_C
INT_HDMI_TXDN1_C
INT_HDMI_TXDP1_C
INT_HDMI_TXDN2_C
INT_HDMI_TXDP2_C
INT_HDMI_TXDP0_C
INT_HDMI_TXDN0_C
HDMI_SCL
HDMI_SDA
HDMI_DET
HDMI_CLK-_L
HDMI_CLK+_L
HDMI_TX1-_L
HDMI_TX1+_L
HDMI_TX2-_L
HDMI_TX2+_L
HDMI_TX0+_L
HDMI_TX0-_L
HDMI_SCL_S
HDMI_SDA_S
HDMI_DET_L
R216
1K/J_4
HDMI_DET_R
R217
R237
R233
R234
R253
4.7K/J_4
*4.7K/J_4_NC
DDC_EN
PC0
PC1
CFG00
CFG01
R213
100K/J_4
R214
0
R218
3.9K
Q6
2N7002W-7-F
HDMI_DET
SCLZ/SDAZ Low-level input/output Voltage
CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V
CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V
CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB
HDMI_PWR_CTRL
0 is Enable
1 is Disable
R220
R236
R232
R235
R250
*0/J_4_NC
*0_NC
0/J_4
DDC_EN
PC0
PC1
CFG00
CFG01
R192
R195
R193
R194
*300_NC
C263
C266
C264
C265
*0.1U/X5R_NC
HDMI_CLK_C
HDMI_TX0_C
HDMI_TX1_C
HDMI_TX2_C
Reserve for EMI
PIM: PI3VDP411LSZDE QPN: ALP411LS000
TI: SN75DP139RGZR QPN: AL000139000
Quanta Computer Inc.
PROJECT : UM8 UMA
Size
Document Number
HDMI
Rev
1A
Date: Wednesday, February 10, 2010
Sheet 24 of 46

UM3

U8

ITE8502E
LQFP-128L

KEYBOARD
ADC/DAC
PWM
LPC
IR/UART
SMBUS
LPC/FWH FLASH
EGPC
PS/2
GPIO

Place these caps close to ITE8502.

Check

UM7 POP 2.2k
UM9 POP 10k
0918 check

UM7 DE-POP
UM9 POP
0918 check

SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

Charge and BAT
PCH
LAN, Clock
Thermal IC

32KHz Clock.

Madison
Discrete
Park
UMA

VGA_TYPE
VGA_IDENTIFY

	LCD_SIZE_ID (99)	LCD_SIZE_ID2 (107)
13"	0	0
14"	1	0
17"	0	1

BID1	USB_RIGHT_EN#	UM9(UMA)	UM9C (Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	QT (A00)	QT (A00)
0	0	(A01)	(A01)

ITE8502E
lqfp128-16x16-4

Quanta Computer Inc.
PROJECT : UM8 UMA

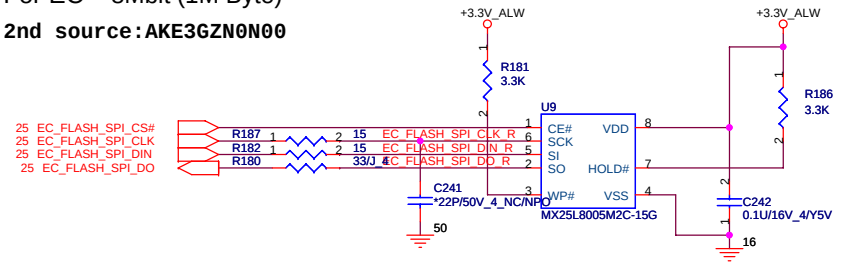
Size	Document Number	Rev
	SIO ITE8502	1A

Date: Wednesday, February 10, 2010 Sheet 25 of 46

UM3

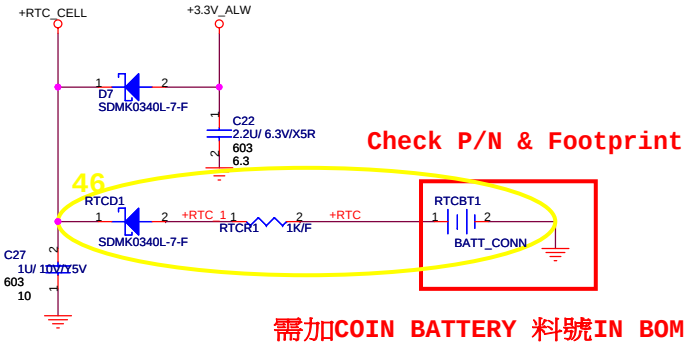
For EC 8Mbit (1M Byte)

2nd source:AKE3GZN0N00



MACRONIX: MX25L3205DM2I-12G QPN: AKE39FP0Z00
WINBOND: W25X32VSSIG QPN: AKE39ZP0N00

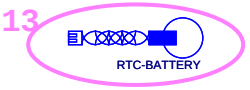
RTC BATTERY



需加COIN BATTERY 料號IN BOM

need modify the location of this portions

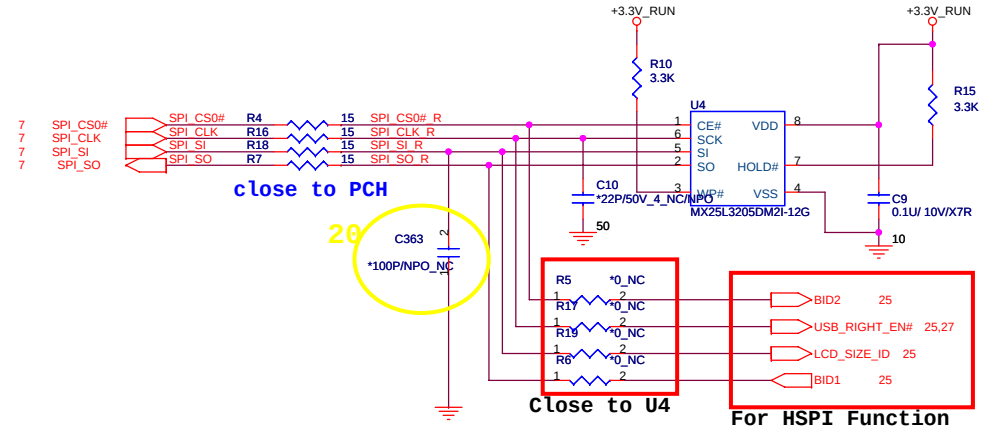
13



For PCH

32Mbit (4M Byte)

MACRONIX: MX25L8005M2C-15G QPN: AKE5GFK0Z09
WINBOND: W25X80AVSSIG QPN: AKE39ZP0N00



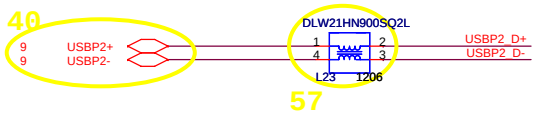
Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	FLASH/RTC	1A
Date: Wednesday, February 10, 2010	Sheet 26 of 46	

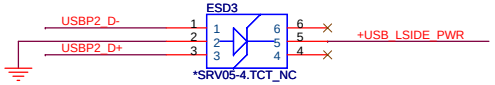
eSATA and USB To DB

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

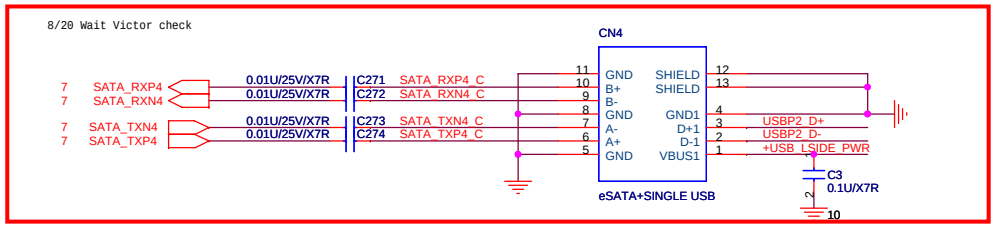


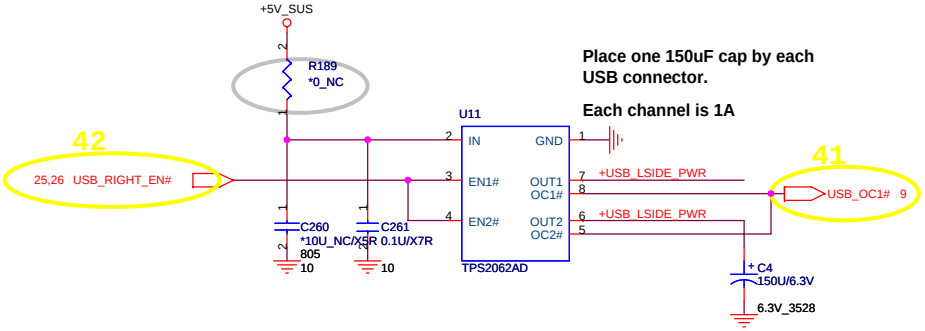
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

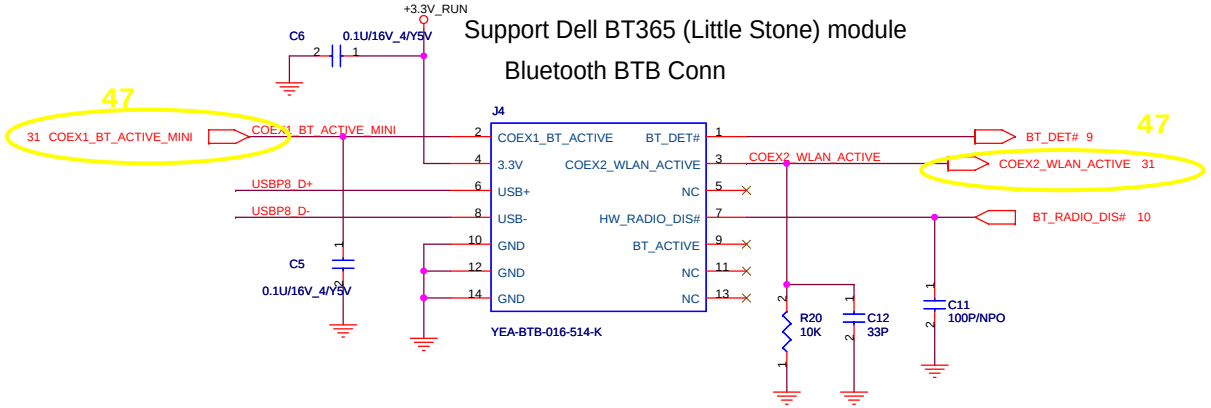
Place ESD diodes as close as USB connector.

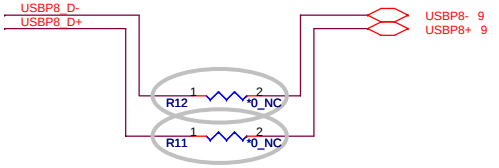


USB and eSATA Conn.







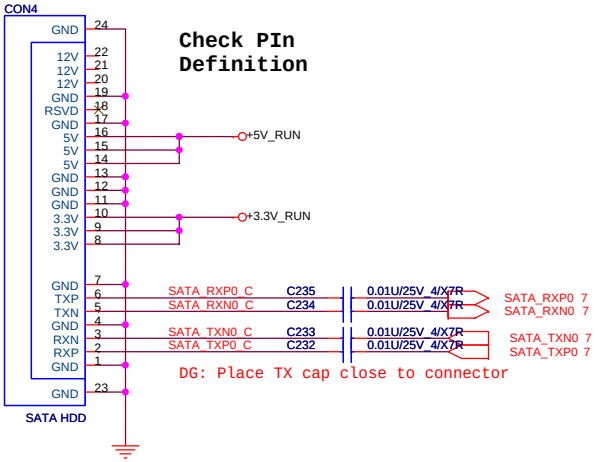


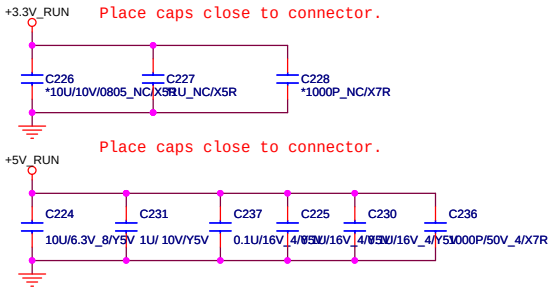
Quanta Computer Inc.

PROJECT : UM8 UMA

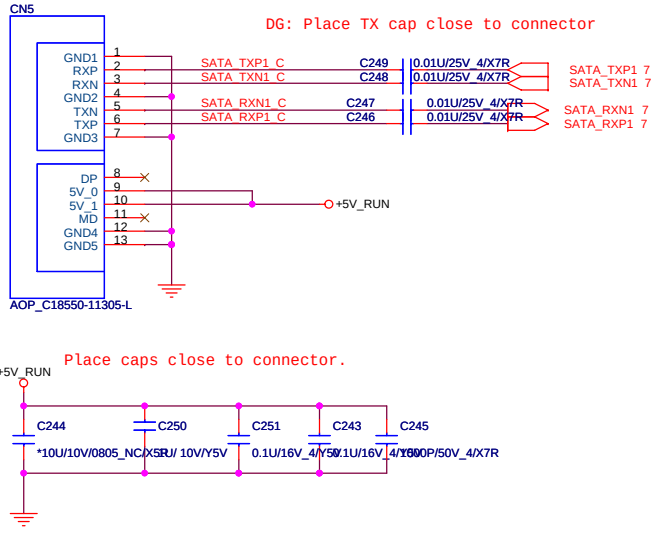
Size	Document Number	Rev
	eSATA & Right USB	1A
Date: Wednesday, February 10, 2010	Sheet 27 of 46	

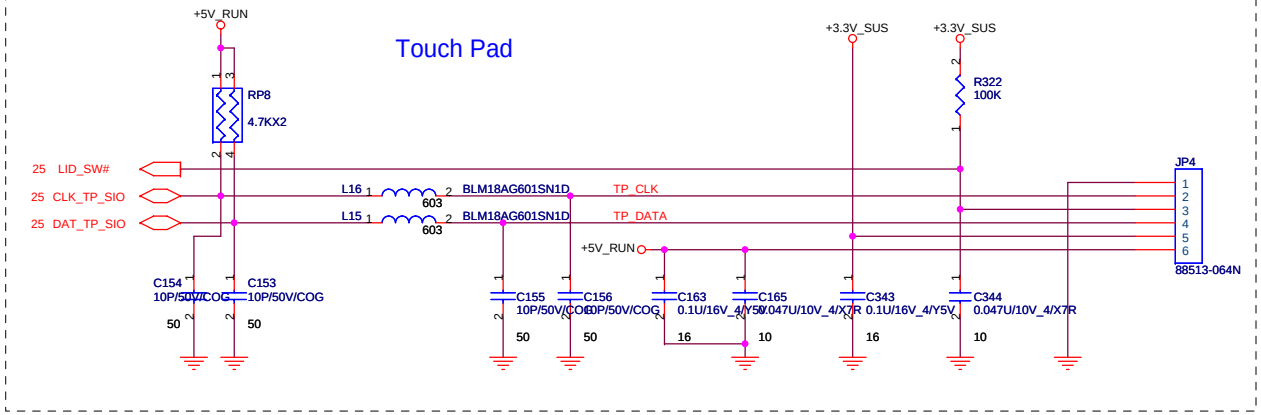
SATA Connector.



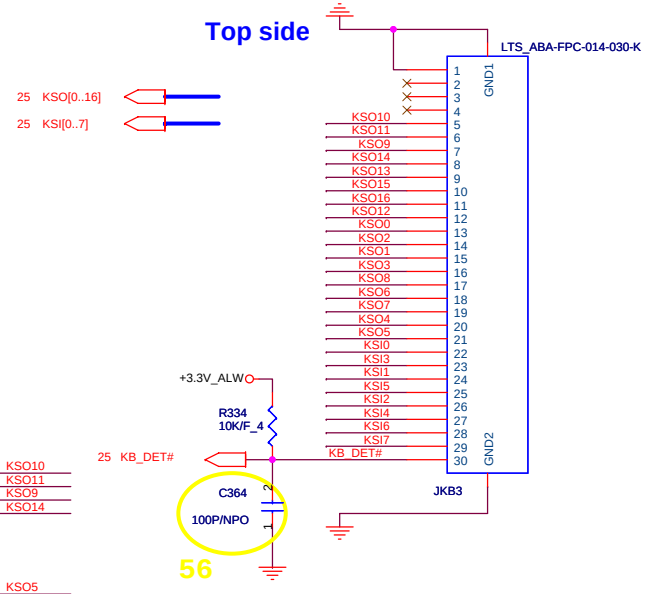


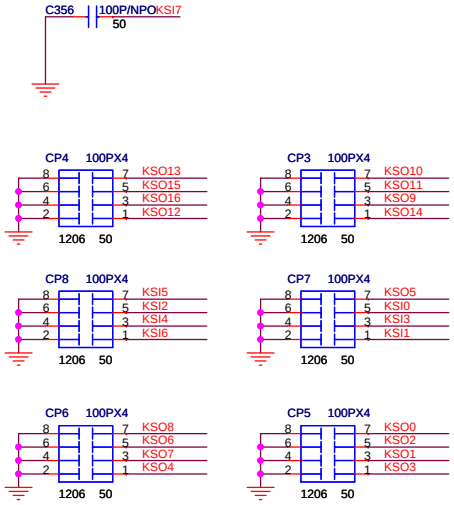
ODD Connector





KEYBOARD CONNECTOR

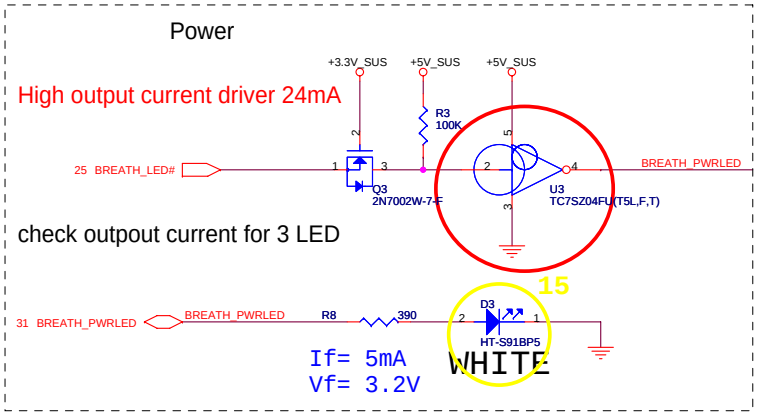


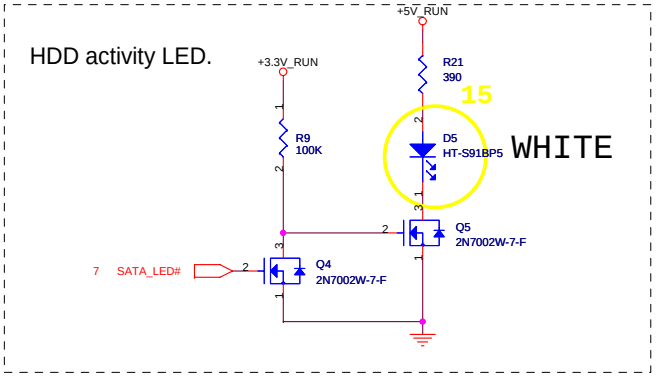


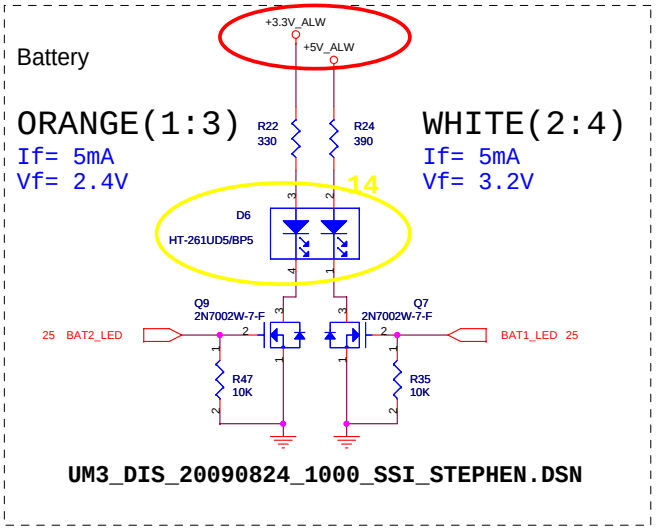
100P CAPS CLOSE TO JKB1

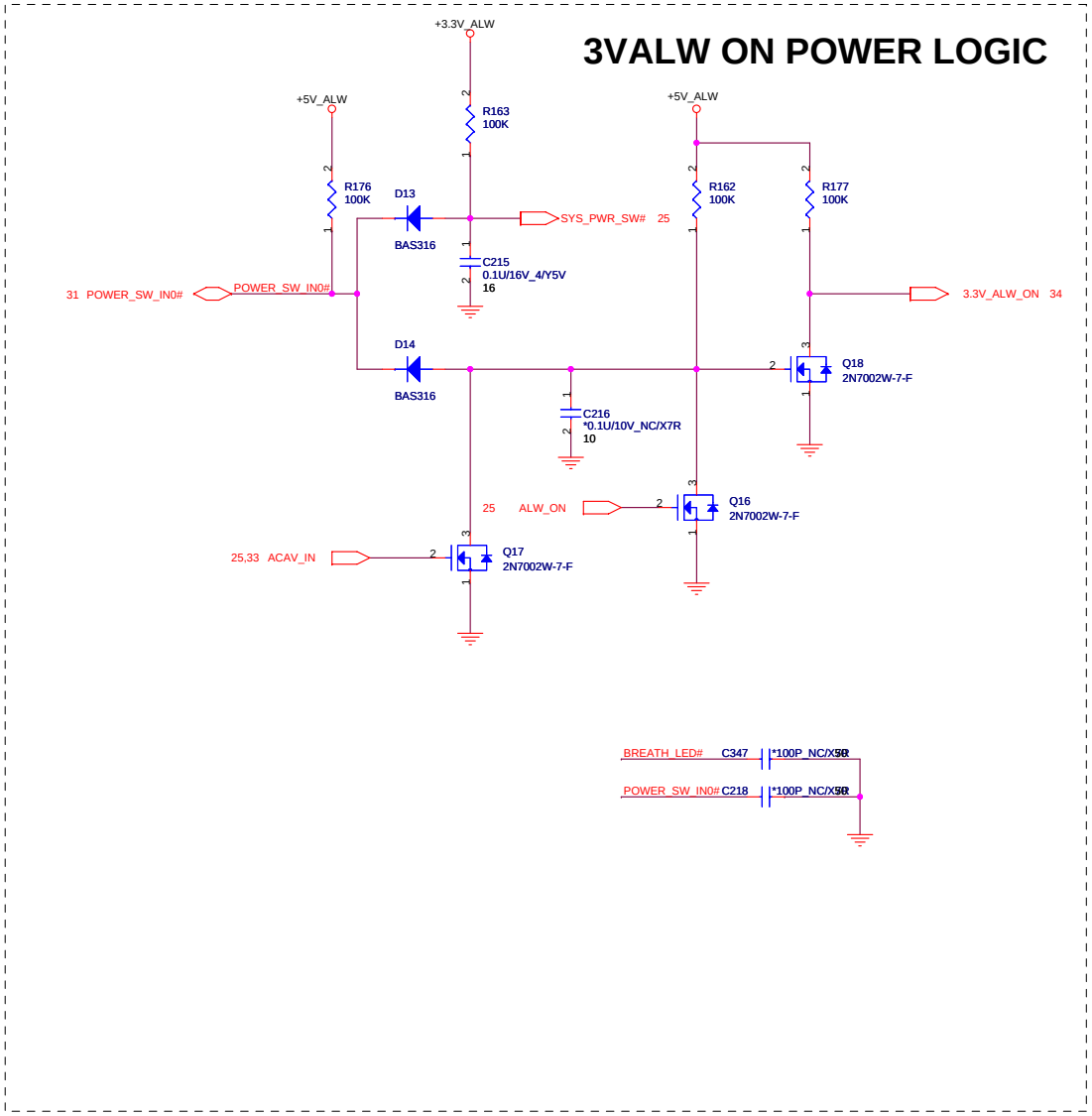
Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	SATA (HDD&ODD) & TP & KB	1A
Date: Wednesday, February 10, 2010	Sheet 28 of 46	









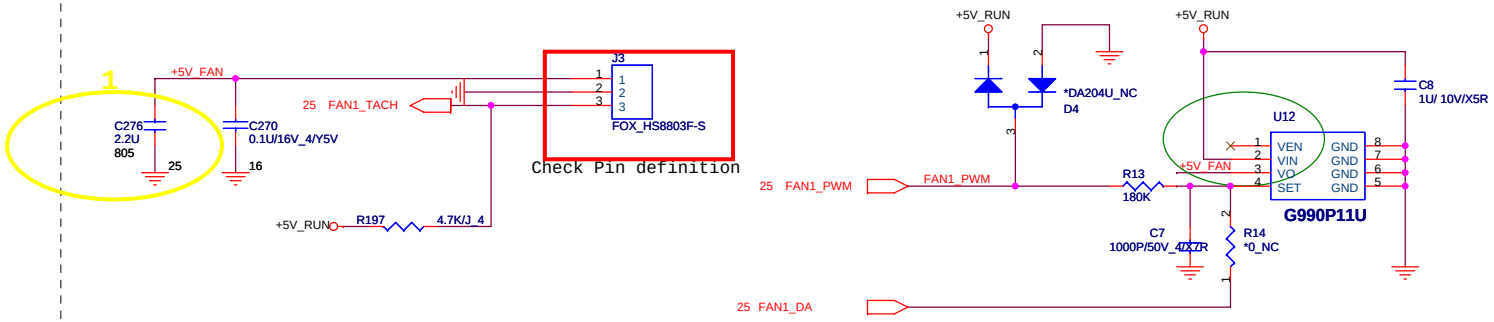
Quanta Computer Inc.

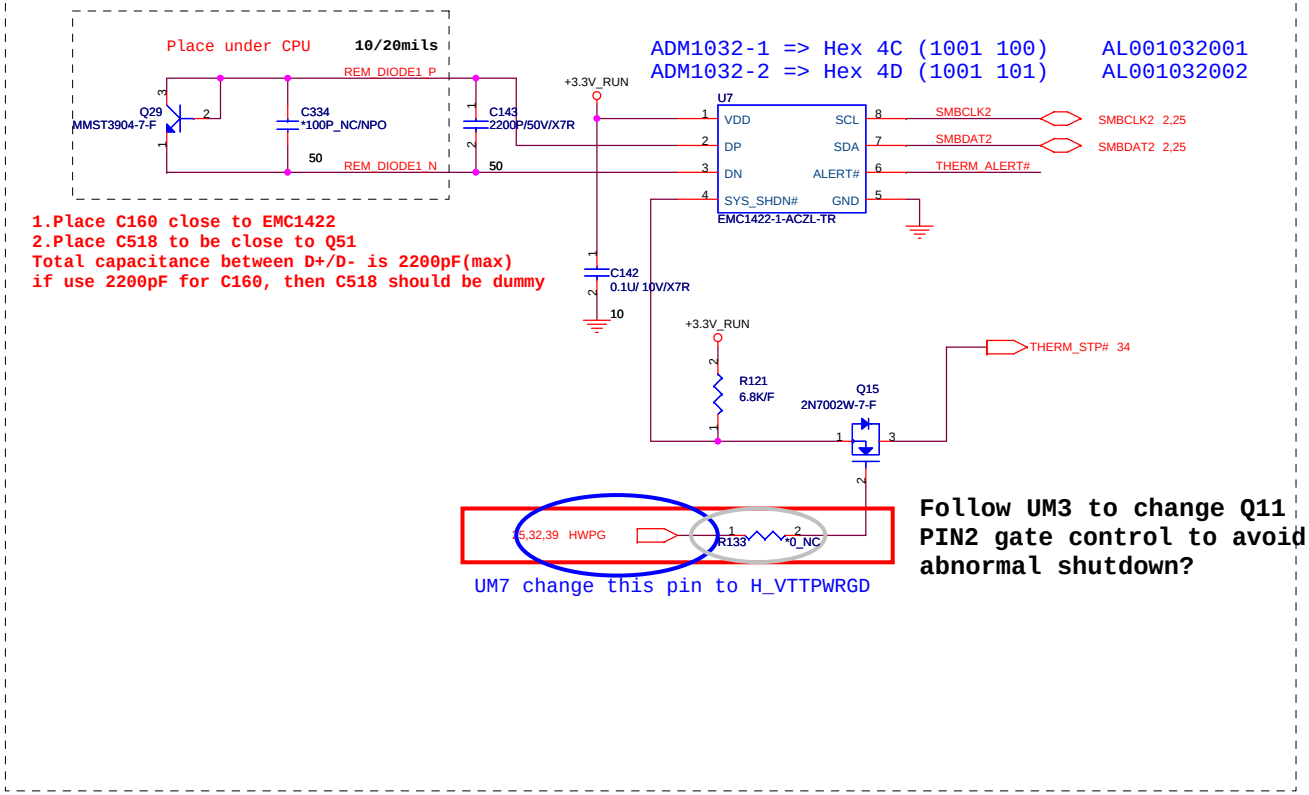
PROJECT : UM8B DIS

Size	Document Number	Rev
	SWITCH, LED	1A

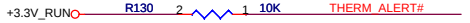
Date: Wednesday, February 10, 2010 Sheet 29 of 46

FAN CONTROL





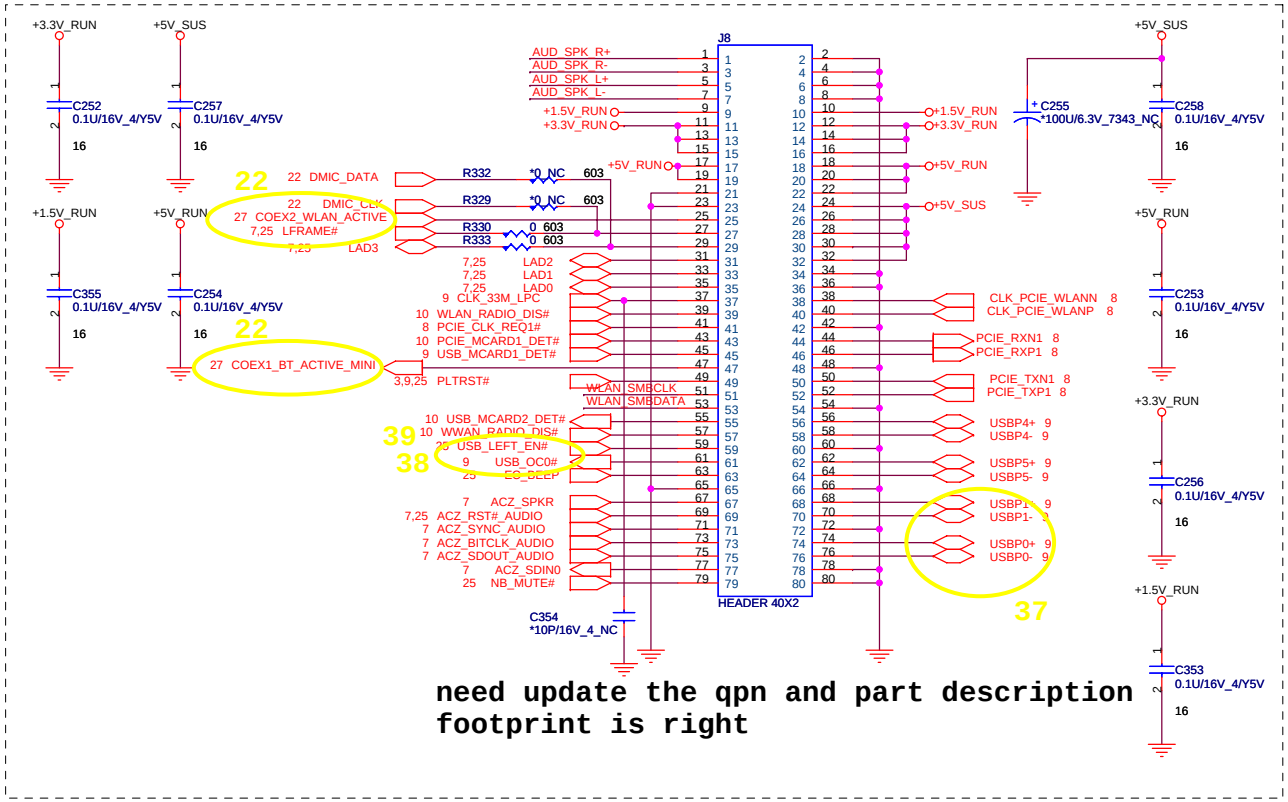
OTP 85 degree C



SYS_SHD# / ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C

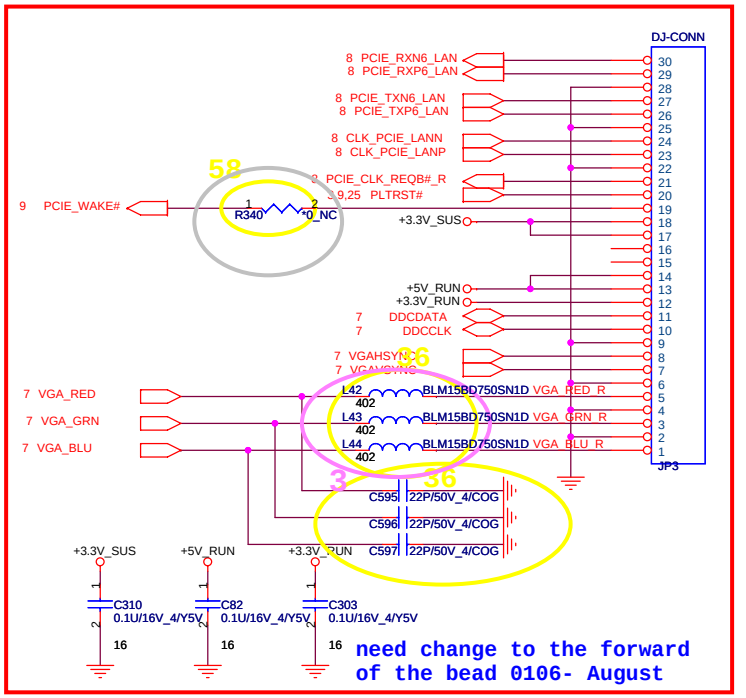
Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	FAN & THERMAL	1A
Date: Wednesday, February 10, 2010	Sheet 30 of 46	



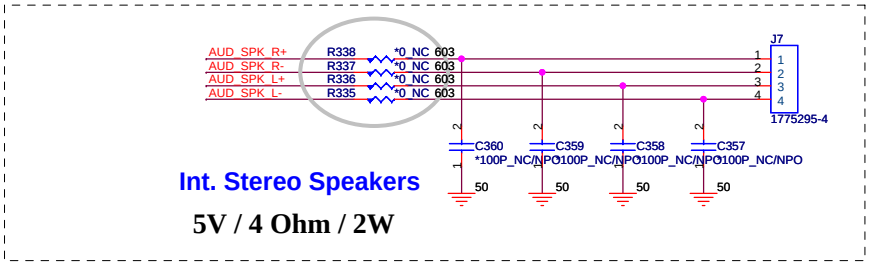
need update the qpn and part description
footprint is right

Check P/N and footprint



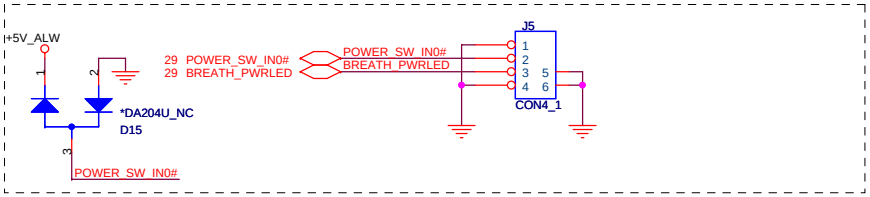
need change to the forward of the bead 0106- August

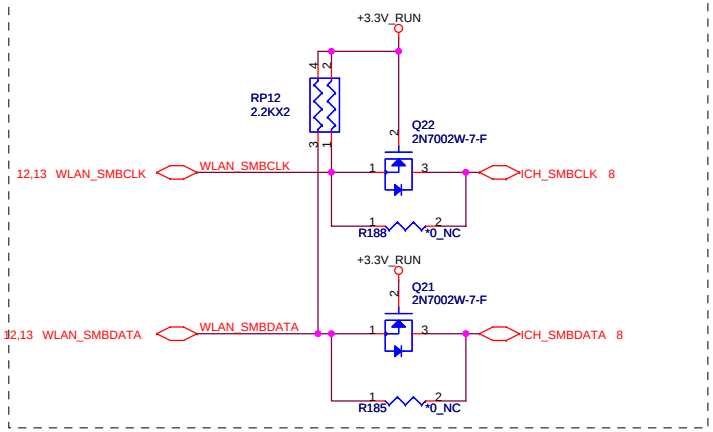
To CRT board



Int. Stereo Speakers

5V / 4 Ohm / 2W

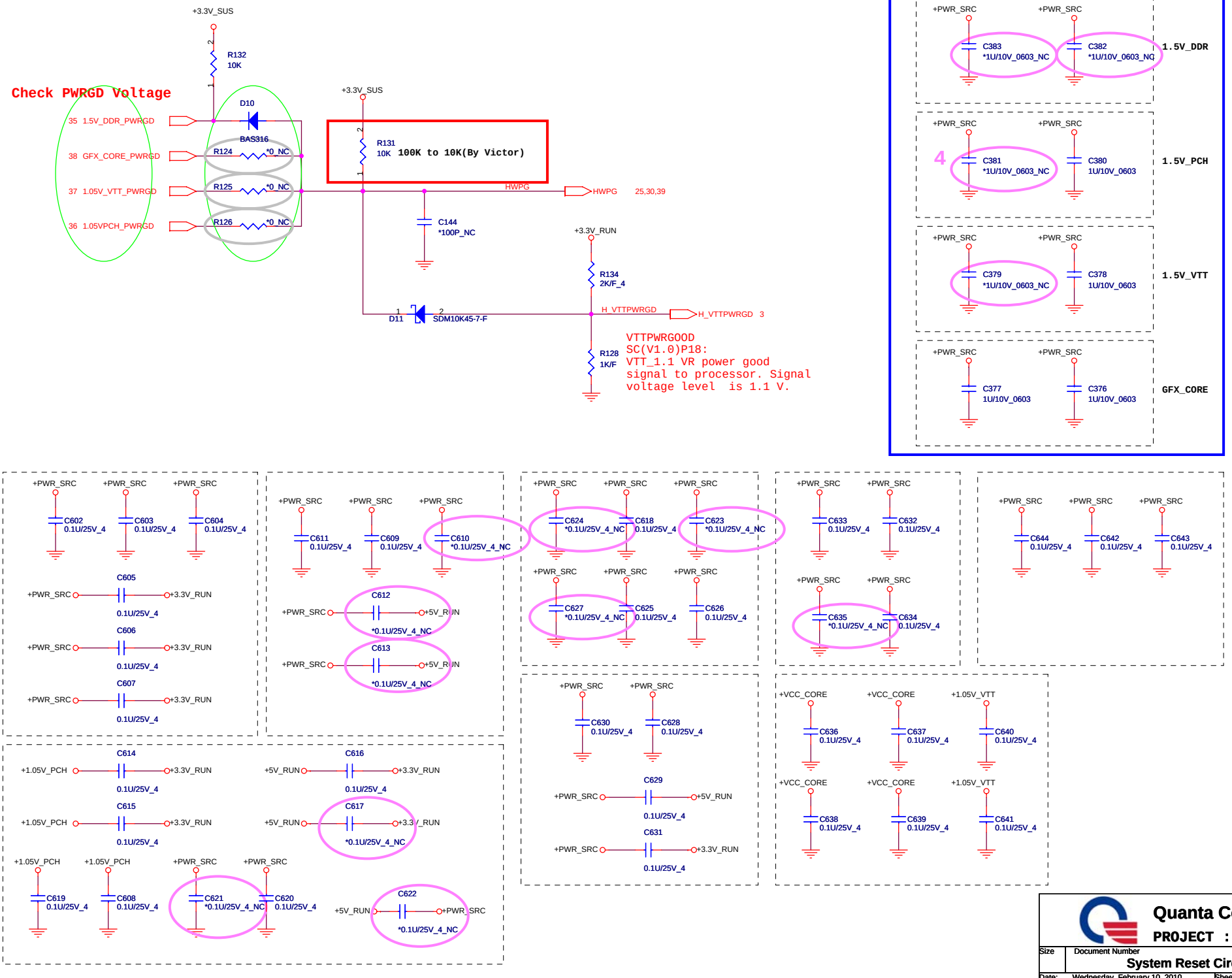




Quanta Computer Inc.

PROJECT : UM8B DIS

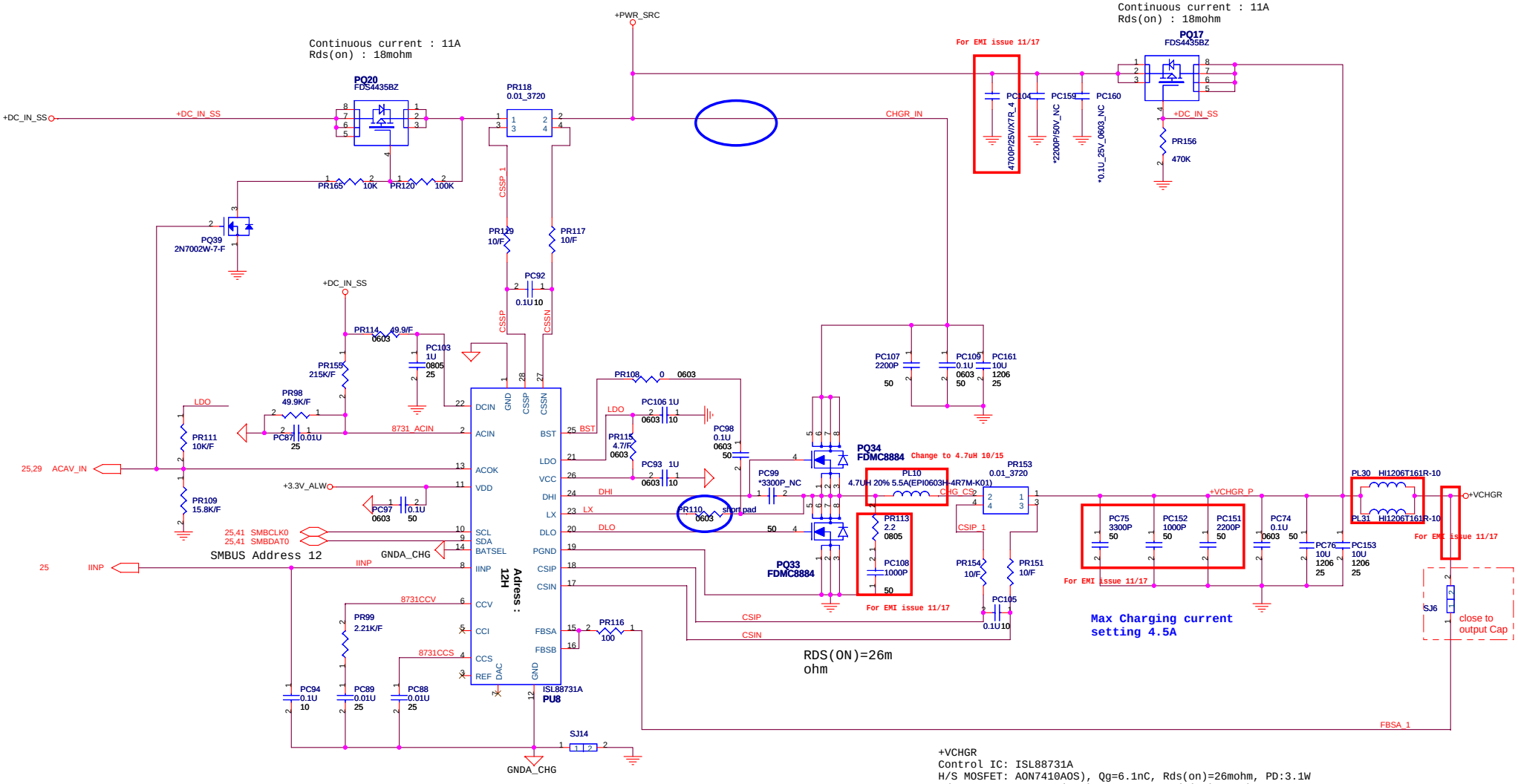
Size	Document Number	Rev
	BTB CONN & Audio conn	1A
Date: Wednesday, February 10, 2010	Sheet 31 of 46	



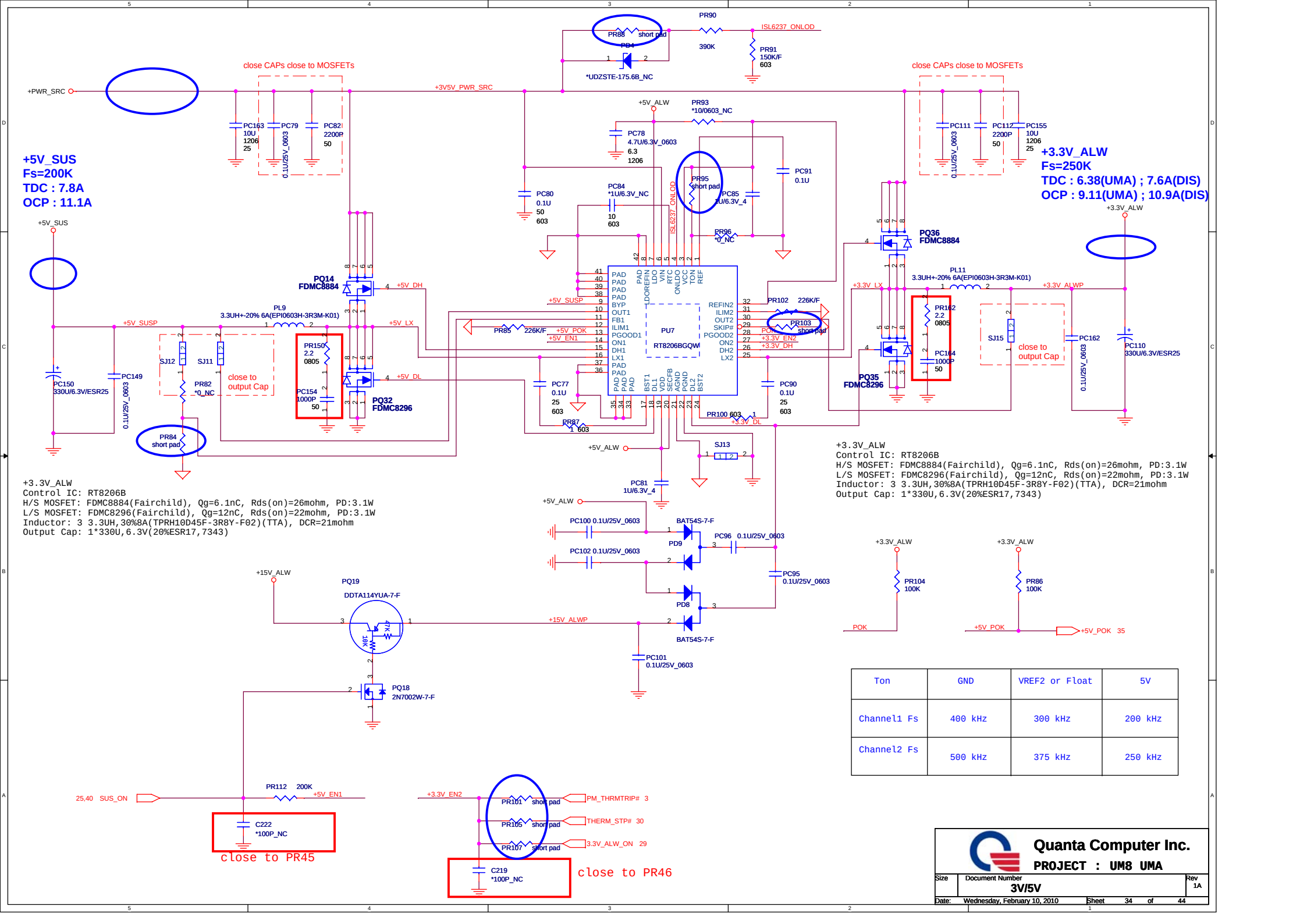
Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	System Reset Circuit	1A
Date: Wednesday, February 10, 2010	Sheet 32 of 46	



Quanta Computer Inc.			
PROJECT : UM8 UMA			
Size	Document Number		Rev
	Charger		1A
Date: Wednesday, February 10, 2010	Sheet 33 of 44		



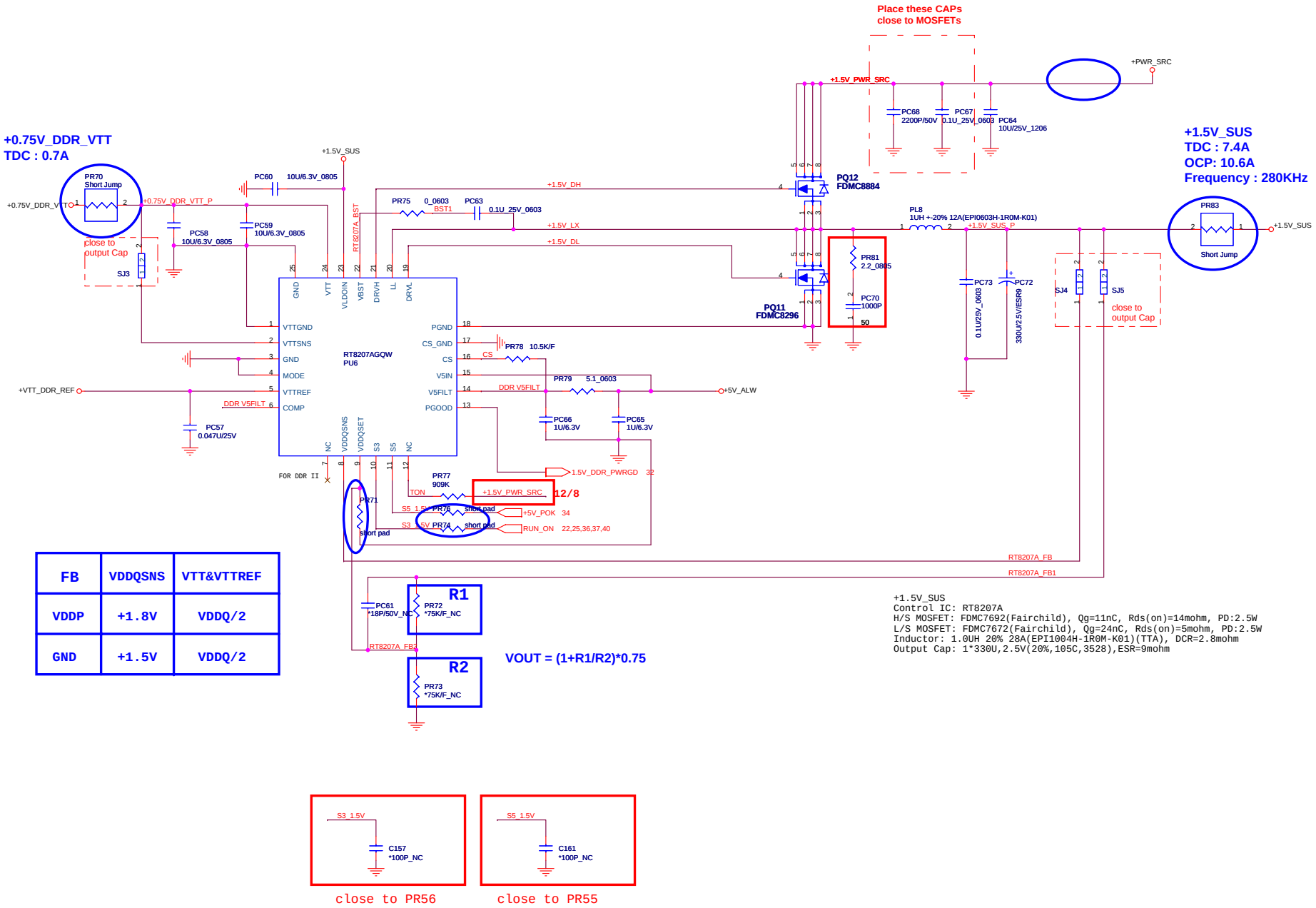
Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz

Quanta Computer Inc.

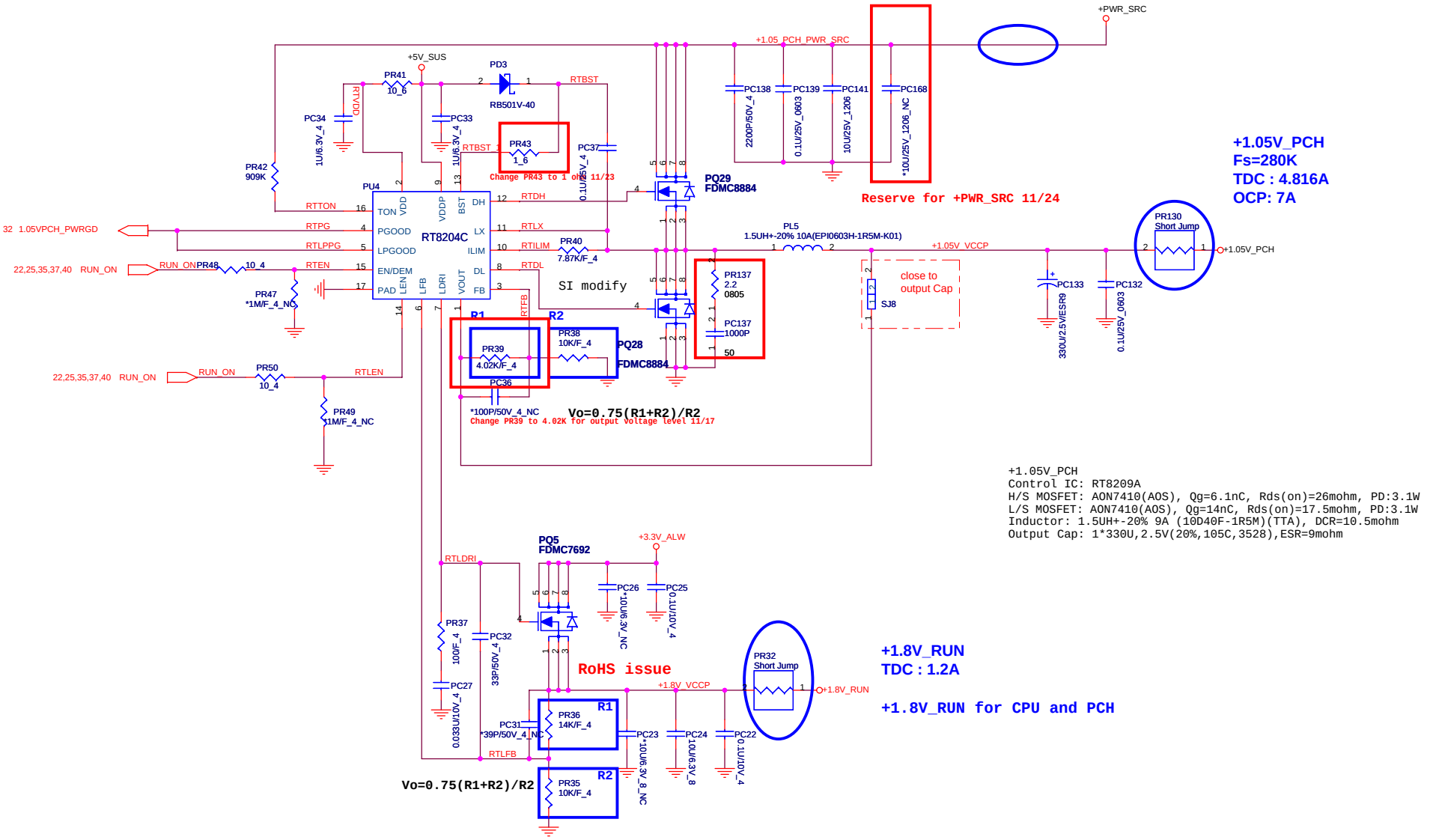
PROJECT : UM8 UMA

Size	Document Number	Rev
	3V/5V	1A

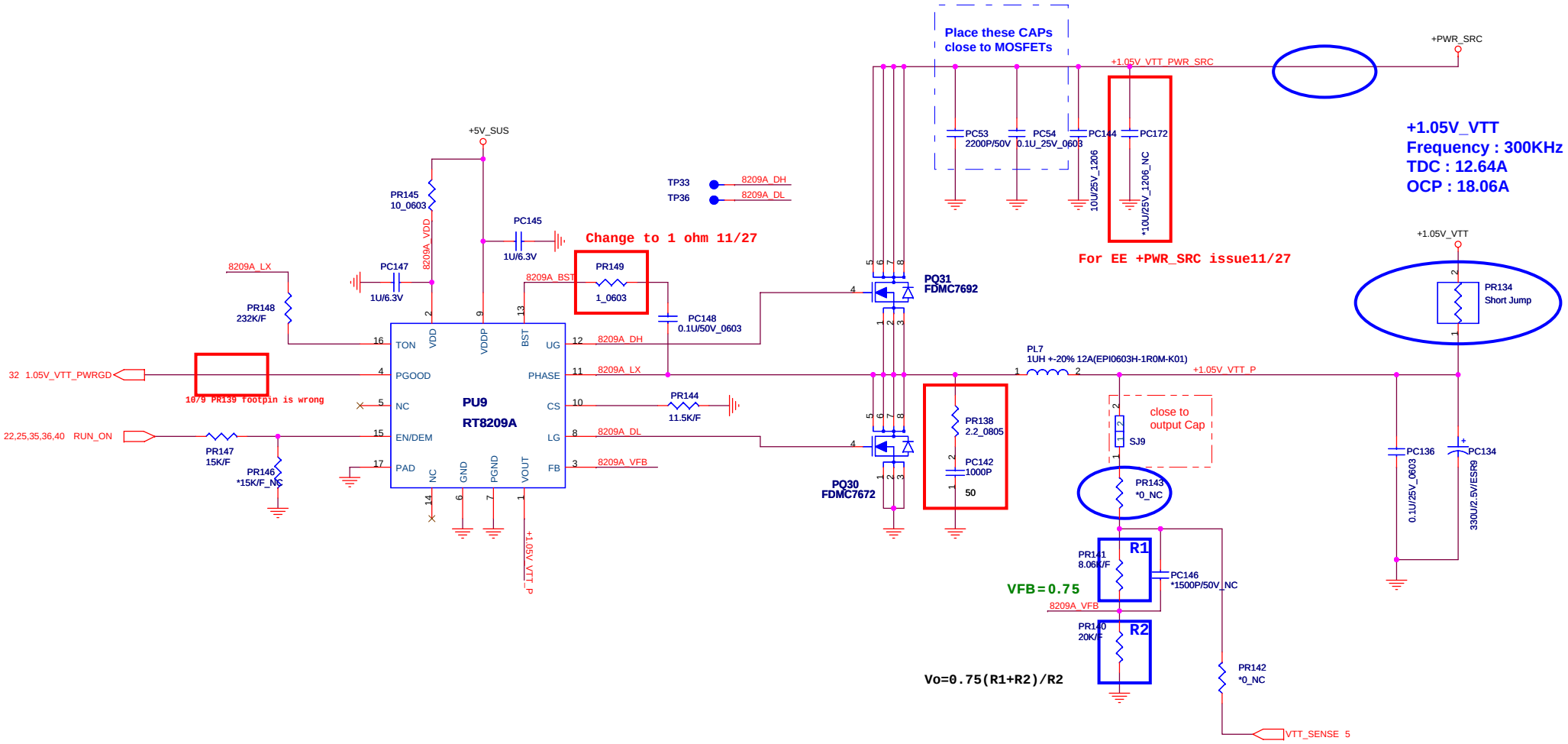
Date: Wednesday, February 10, 2010 Sheet 34 of 44



Quanta Computer Inc.		
PROJECT : UM8 UMA		
Size	Document Number: 1.5V_DDR	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 35 of 44	

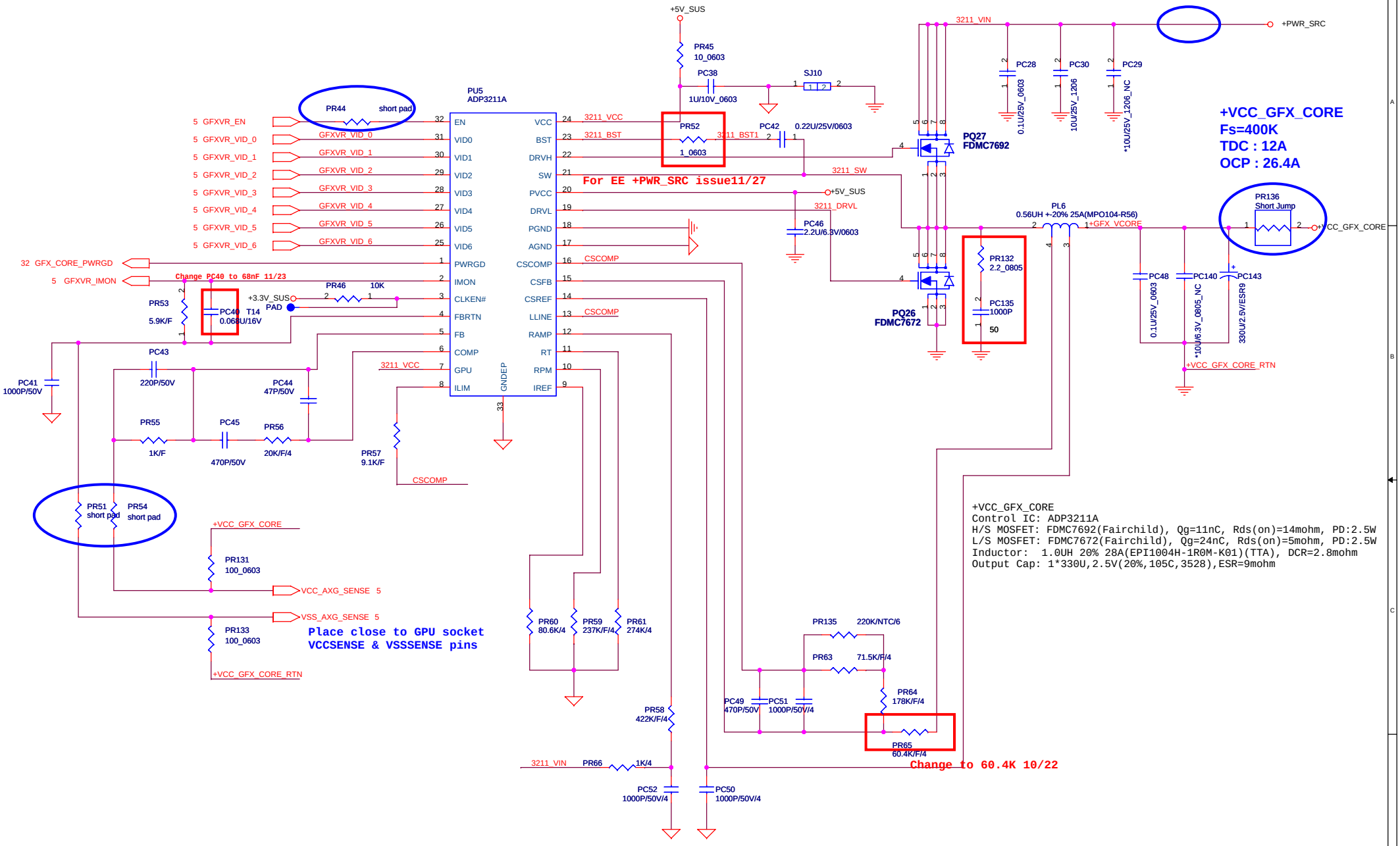


Quanta Computer Inc.		
PROJECT : UM8 UMA		
Size	Document Number: 1.05_PCH	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 36 of 44	

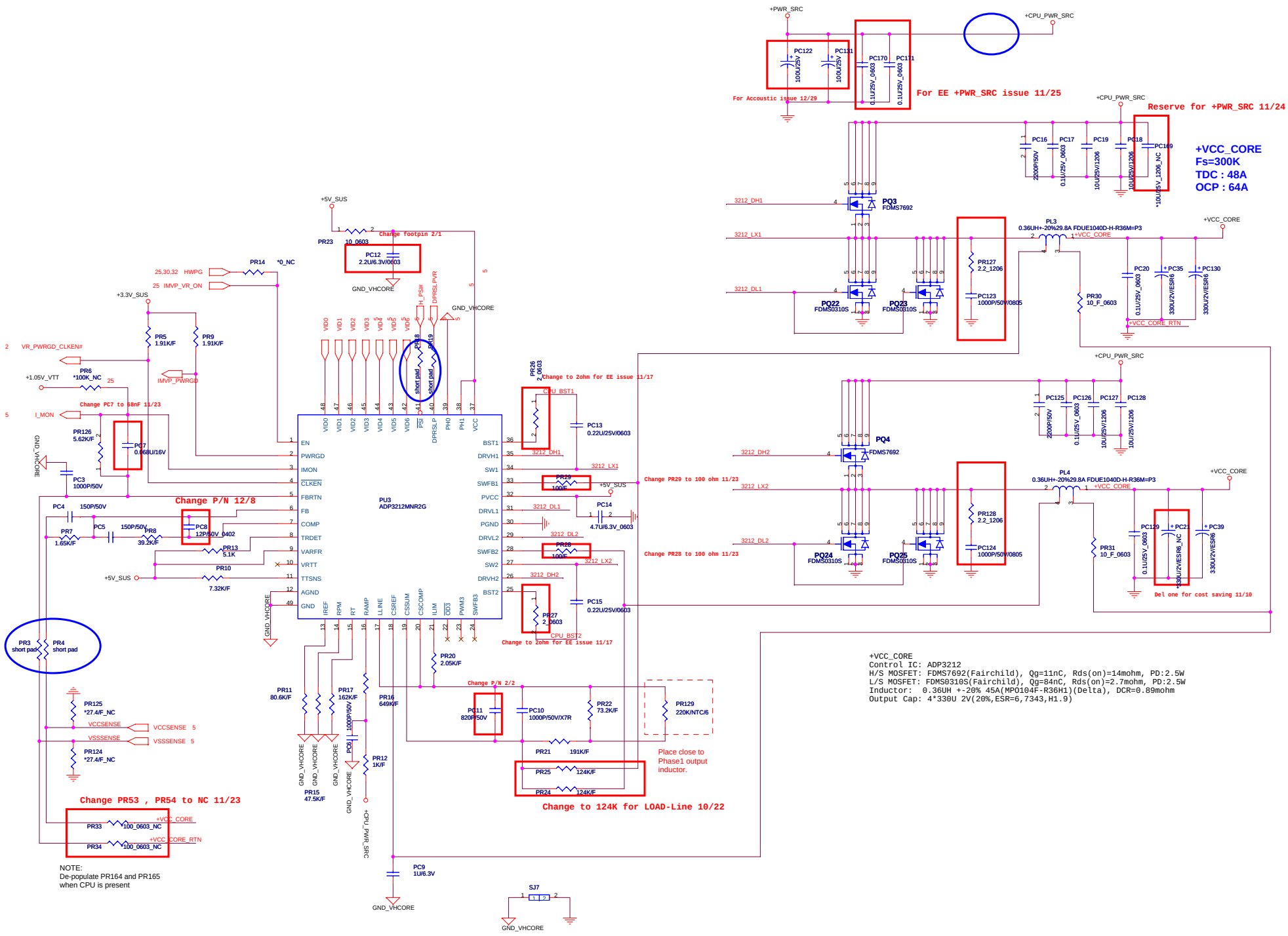


+1.05V_VTT
Control IC: RT8209A
H/S MOSFET: FDMC7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMC7672(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 1.0UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 1*330U,2.5V(20%,105C,3528),ESR=9mohm

Quanta Computer Inc.		
PROJECT : UM8 UMA		
Size	Document Number: 1.05_VTT	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 37 of 44	



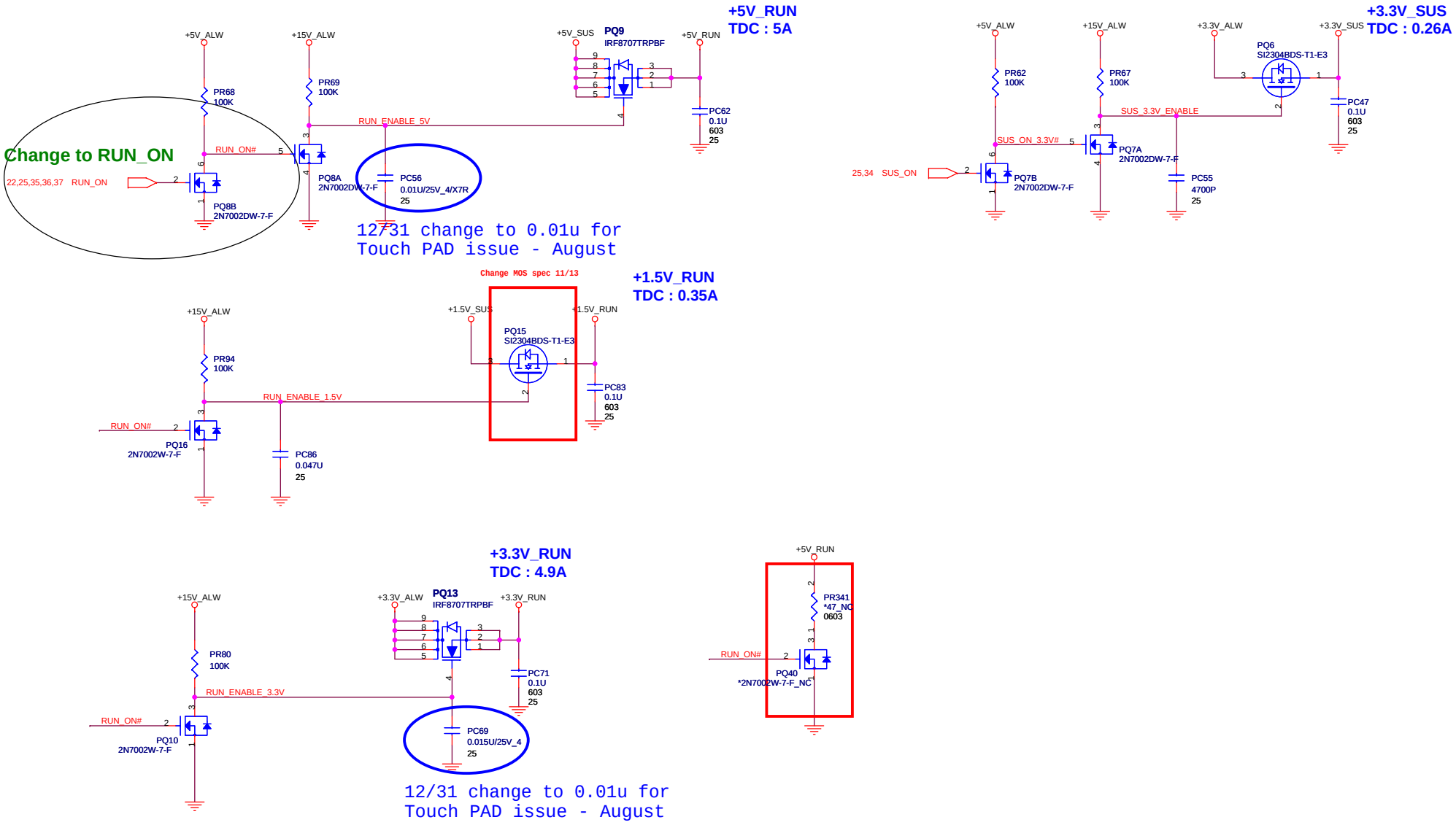
Quanta Computer Inc.		
PROJECT : UM8 UMA		
Size	Document Number: GFX_CORE	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 38 of 44	



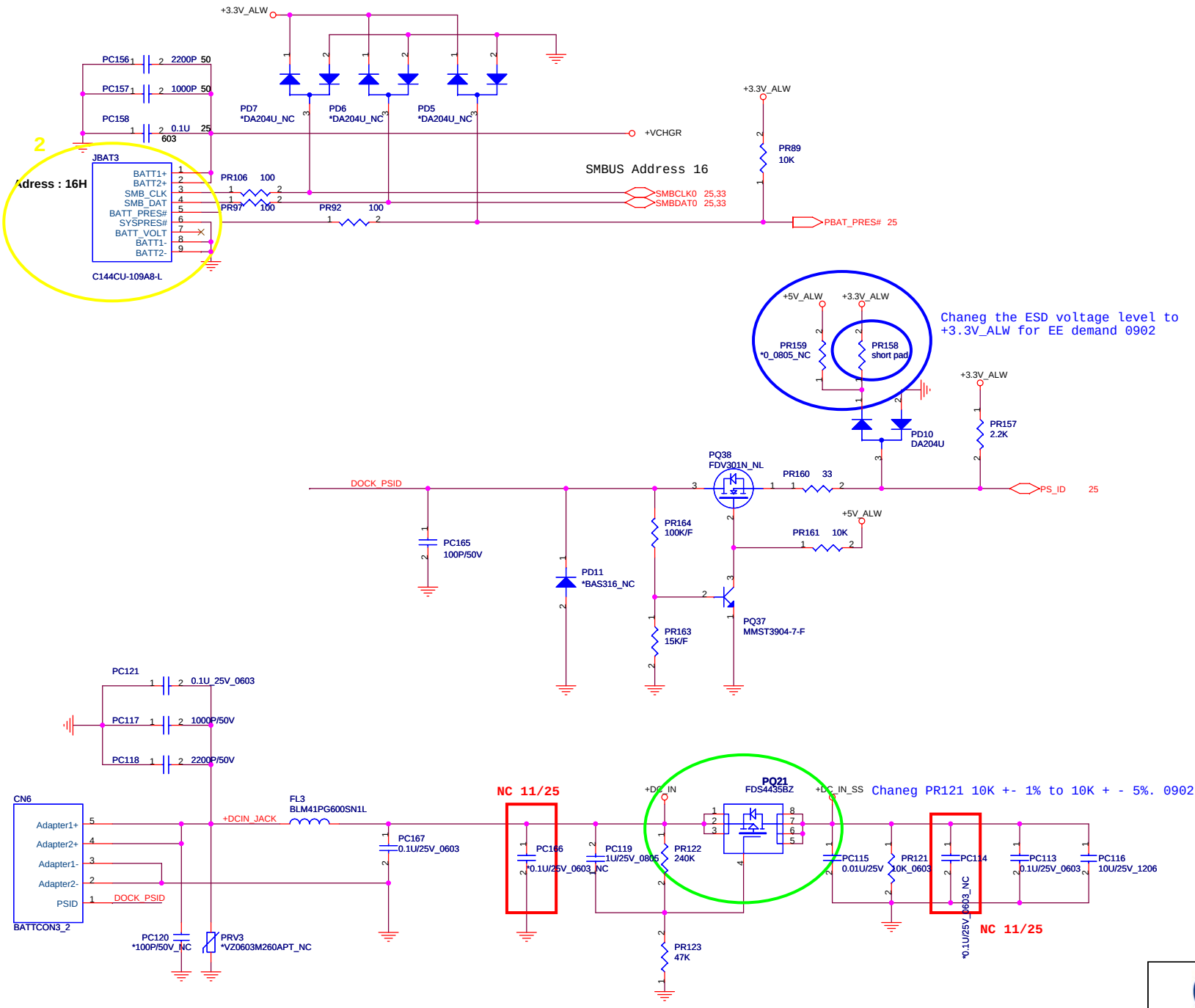
Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	CPU CORE	1A
Date: Wednesday, February 10, 2010	Sheet 39 of 44	

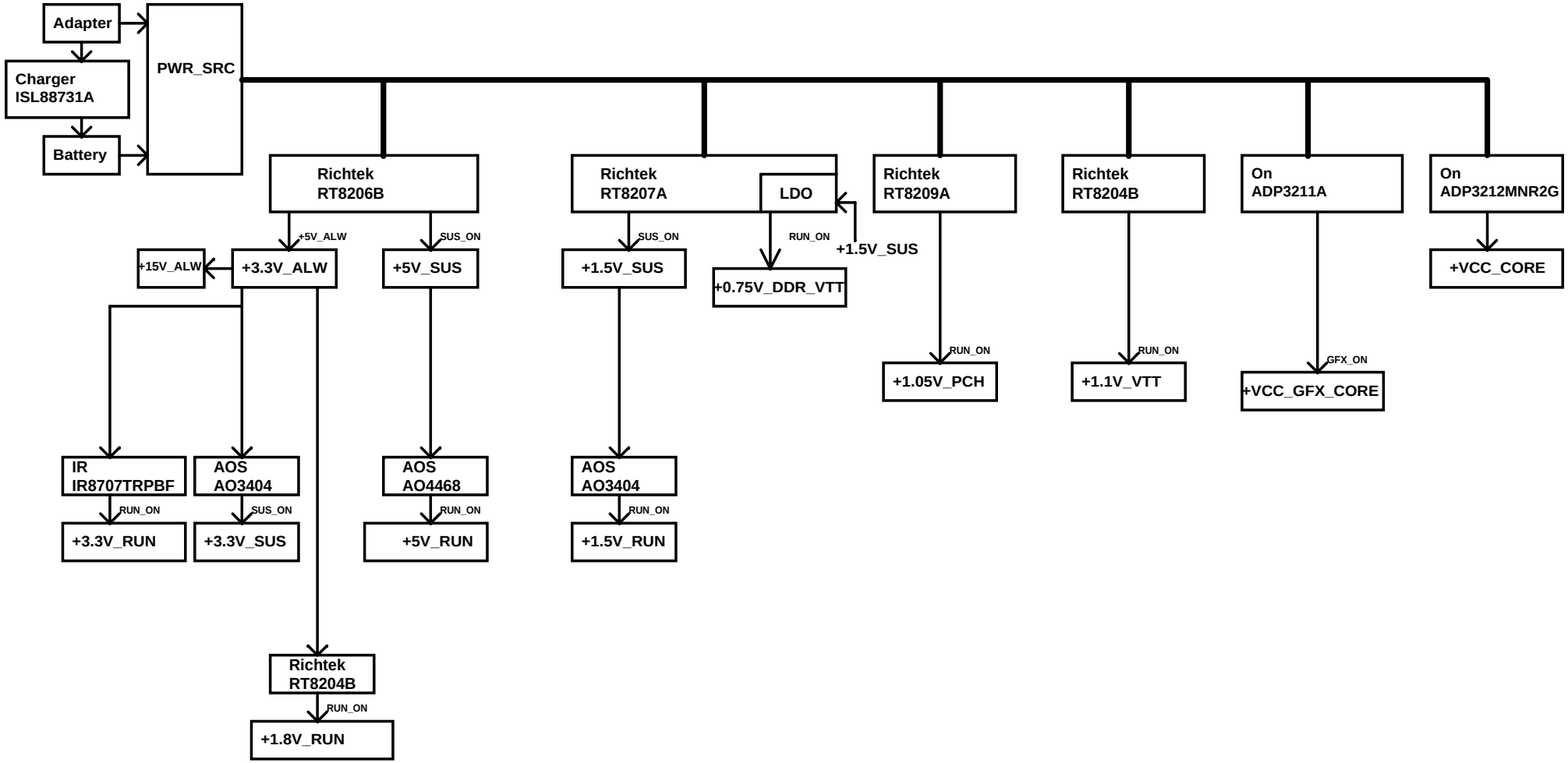


Quanta Computer Inc.		
PROJECT : UM8 UMA		
Size	Document Number: Run Power Switch	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 40 of 44	



Quanta Computer Inc.		
PROJECT : UM8 UMA		
Size	Document Number: Batt & DC-IN	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 41 of 44	

VER : 1A

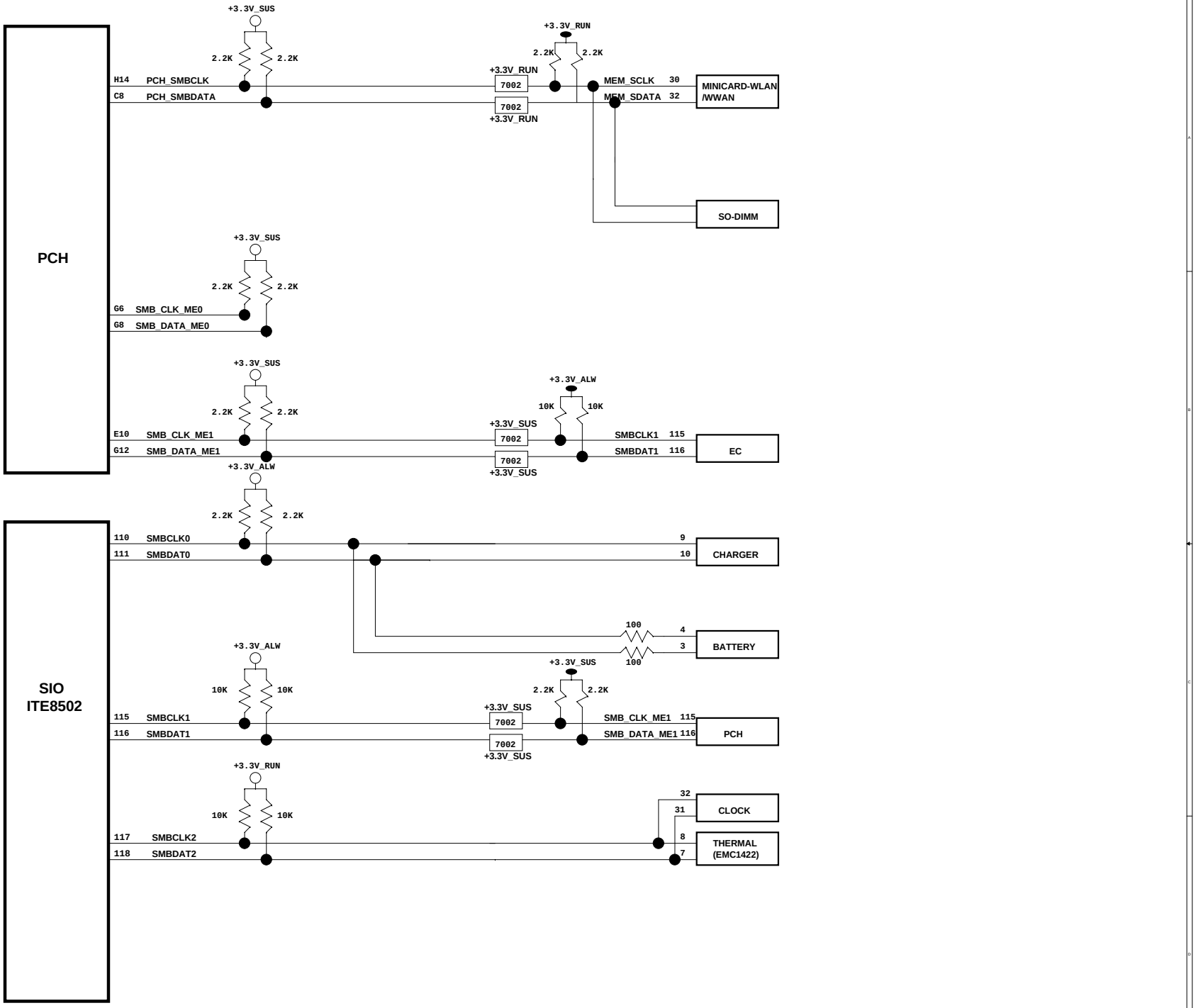


Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	Schematic Block Diagram1	1A

Date: Wednesday, February 10, 2010 Sheet 42 of 46



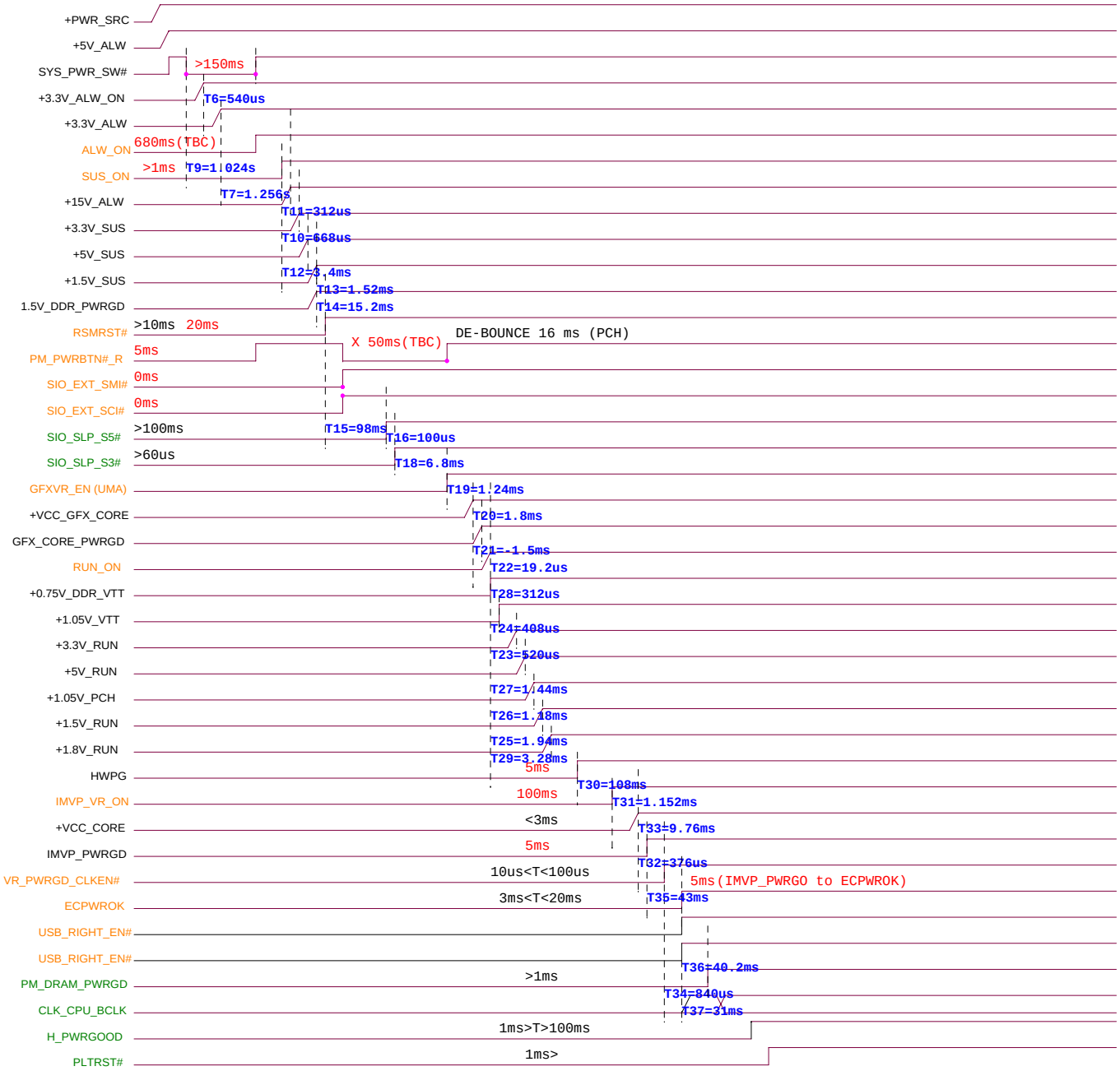
Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	SMBUS BLOCK	1A

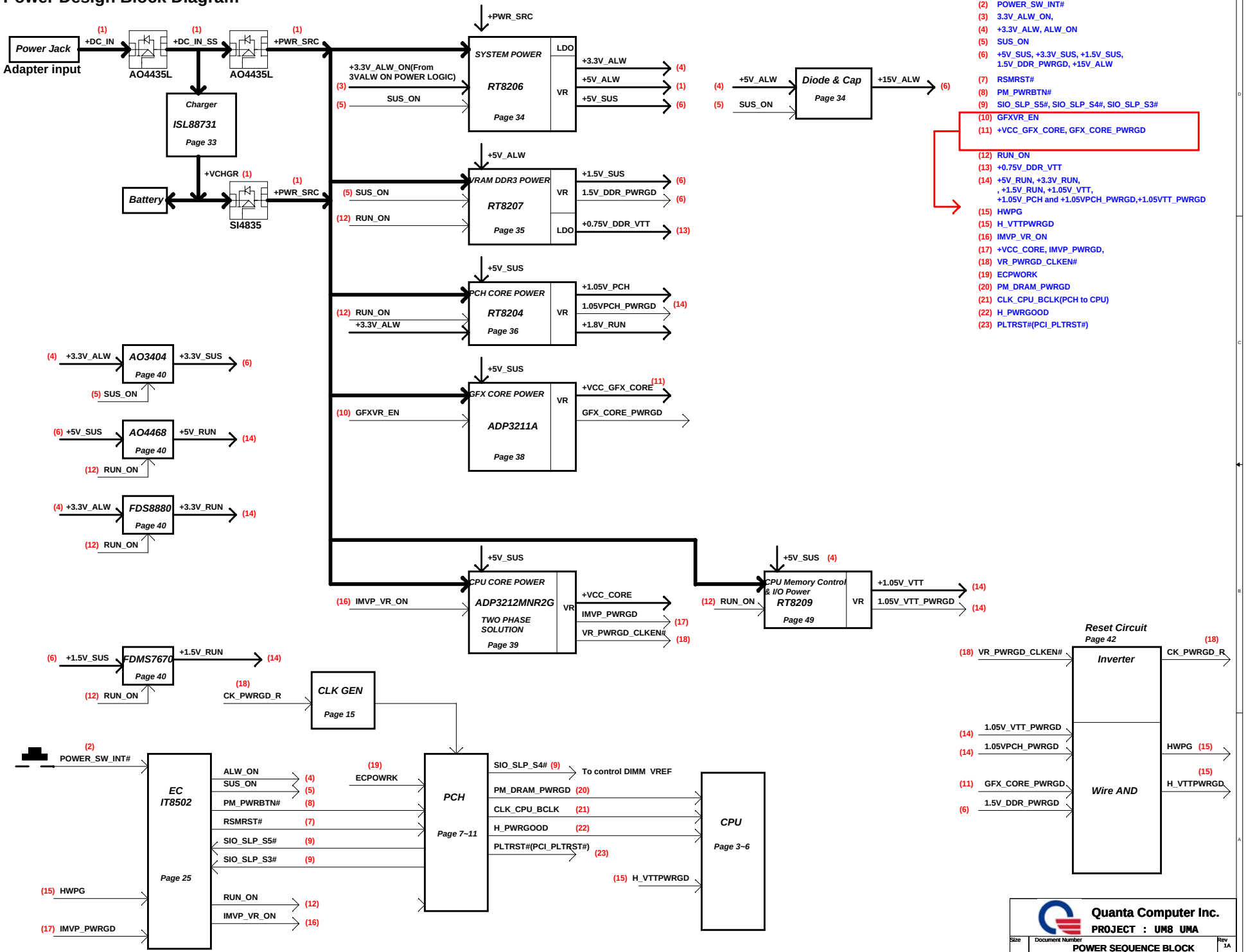
Date: Wednesday, February 10, 2010 Sheet 43 of 46

UM8_ X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)



Quanta Computer Inc.		
PROJECT : UM8 UMA		
Size	Document Number: POWER SEQUENCE	Rev 1A
Date: Wednesday, February 10, 2010	Sheet 44 of 46	

Power Design Block Diagram



(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW
(2) POWER_SW_INT#
(3) 3.3V_ALW_ON,
(4) +3.3V_ALW, ALW_ON
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD, +15V_ALW
(7) RSMRST#
(8) PM_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) GFXVR_EN
(11) +VCC_GFX_CORE, GFX_CORE_PWRGD
(12) RUN_ON
(13) +0.75V_DDR_VTT
(14) +5V_RUN, +3.3V_RUN, , +1.5V_RUN, +1.05V_VTT, +1.05V_PCH and +1.05VPCH_PWRGD,+1.05VTT_PWRGD
(15) HWPG
(15) H_VTTPWRGD
(16) IMVP_VR_ON
(17) +VCC_CORE, IMVP_PWRGD,
(18) VR_PWRGD_CLKEN#
(19) ECPOWRK
(20) PM_DRAM_PWRGD
(21) CLK_CPU_BCLK(PCH to CPU)
(22) H_PWRGOOD
(23) PLTRST#(PCI_PLTRST#)

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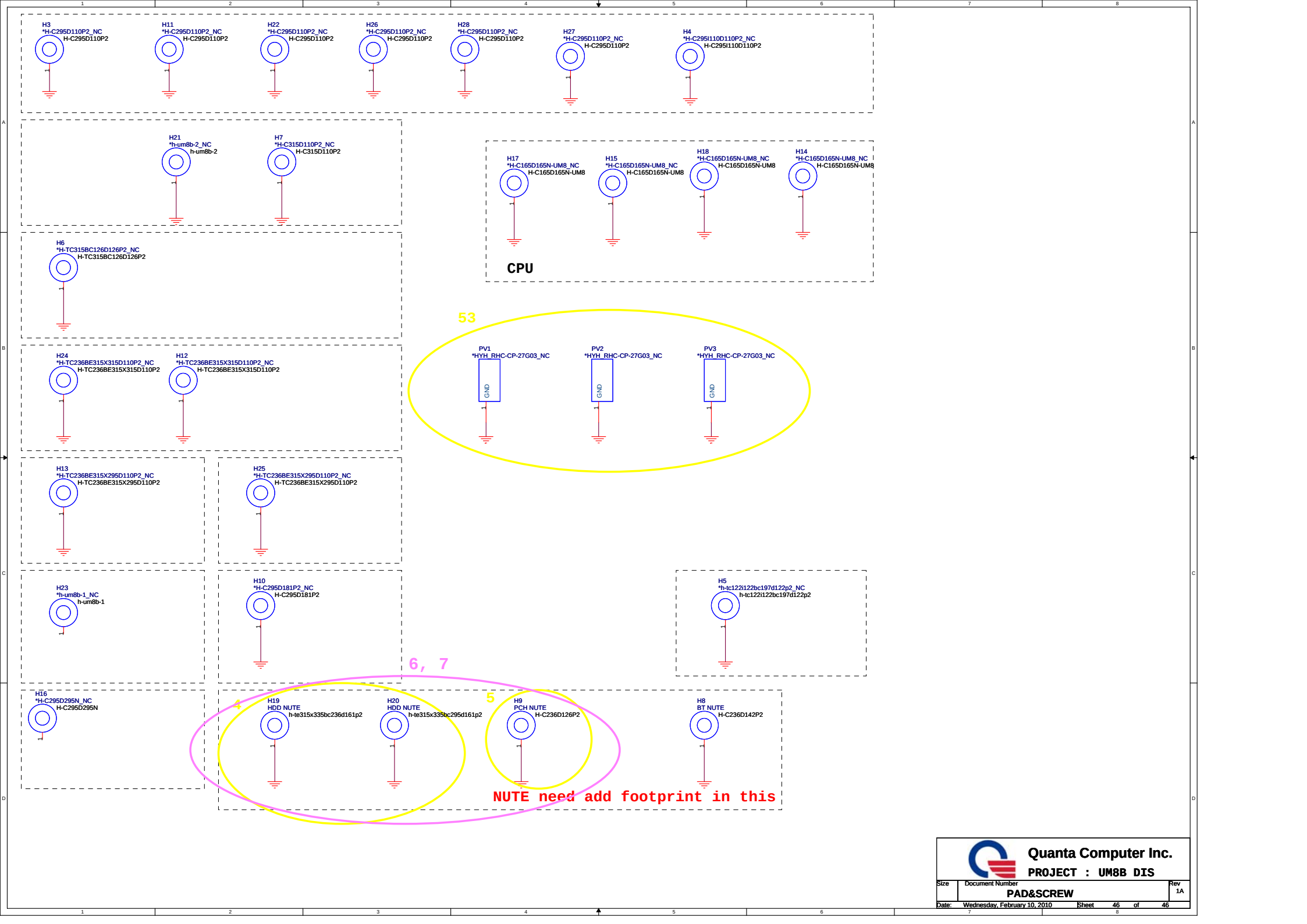

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