

Enrico Caruso 14
Muxless/UMA Schematics Document
Sandy Bridge
Intel PCH
2011-04-07
REV : A00

DY : None Installed
UMA: UMA ONLY installed
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
DIS: MUXLESS solution installed.
Surge: For GO Rural config stuff.
GIGA: For GIGA LAN config stuff.
HDMI: For HDMI config stuff.
DIS_CRT: Pure DIS install

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

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Sheet 1 of 105

Block Diagram (Discrete/UMA co-lay)

##OnMainBoard



gDDR3
900MHz

Seymour-XT S3

83,84,85,86,87

Intel CPU

Sandy Bridge

4,5,6,7,8,9,10

FDIx4x2

DMIx4
1GB/s

Intel
PCH
Cougar Point

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIe ports (8)
LPC I/F
ACPI 1.1

Azalia
CODEC
IDT 92HD87

29

CRT

50

LCD

49

HDMI

51

SD/MMC/MS/
MS Pro

74

CardReader
Realtek
RTS5138

32

Audio board

Internal Analog MIC

58

HP1

82

MIC IN

2CH SPEAKER

58

HDD

56

ODD

56

Flash ROM
4MB

60

Project code: 91.4IU01.001
PCB P/N : 48.4IU16.0SC
Revision : 10315-SC

SYSTEM DC/DC APL5916 48		CPU DC/DC VT1316+1314 42~44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	0D85V_S0	DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51218 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51125 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5

SYSTEM DC/DC TPS51216R 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC VT1316+1317 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208B 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24707 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC APW7153B 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9731 93	
INPUTS	OUTPUTS
1D5V_S3 3D3V_S0	1V_VGA_S0 1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER	
L1:Top L2:GND L3:Signal	L4:Signal L5:VCC L6:Bottom

10/100/1000 LOM
Realtek RTL8111E (Giga LAN)
Realtek RTL8105E (10M/100M)

31

RJ45
CONN

59

Mini-Card
WLAN+BT3.0

802.11a/b/g

64

PCIE
100MHz
2.5Gbps

USB 2.0
480Mbps

LPC Bus
33MHz

KBC
NUVOTON
NPCE795BA0DX

27

Thermal
ENE P2800

28

Touch
PAD

69

Int.
KB

69

ENE P2793
Fan

28

<Core Design>

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Title: **Block Diagram**

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PCH Strapping		Huron River Schematic Checklist Rev.0_7			
Name	Schematics Notes				
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-k - 10-k weak pull-up resistor.				
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".				
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.				
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.				
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)				
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.				
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.				
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.				
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.				
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.				
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.				
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.				

Pair	Device
0	X
1	USB Ext. port 2 (MB)
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 3
9	USB Ext. port 1
10	X
11	Mini Card1 (WLAN+BT)
12	CAMERA
13	X

SMBus ADDRESSES		HURON RIVER ORB		
I ² C / SMBus Addresses	Ref Des	Address	Hex	Bus
Device				
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	ACTIVE IN S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	X
LANE2	LAN
LANE3	X
LANE4	Wireless
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table		Huron River Schematic Checklist Rev.0_7	
Pair	Device		
0	HDD1		
1	N/A		
2	N/A		
3	N/A		
4	ODD		
5	N/A		

DN15ATI Whistler	
	
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Note:
Intel DMI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Intel FDI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Lane reversal does not apply to
FDI sideband signals.

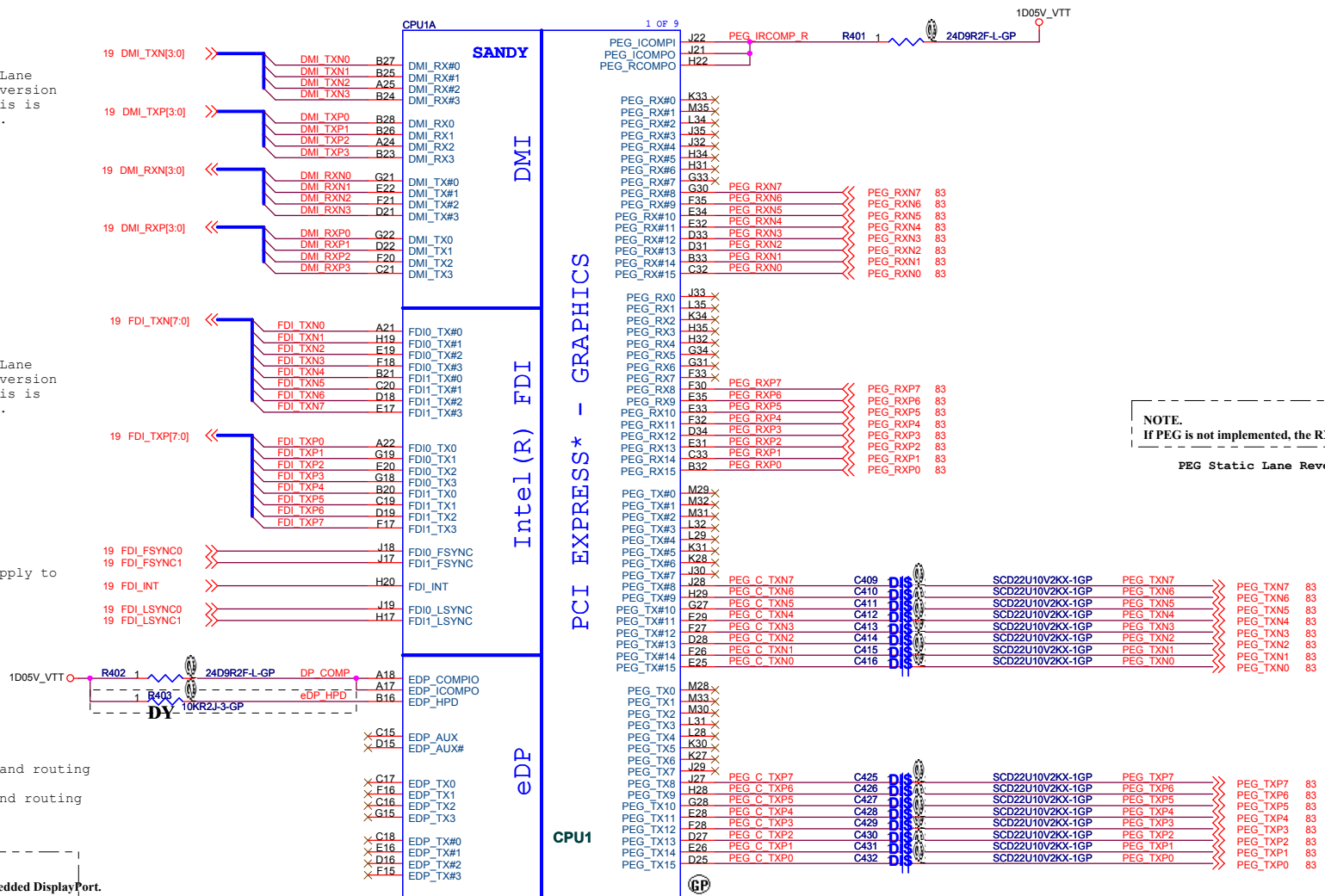
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing
length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing
length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics
function for power saving.

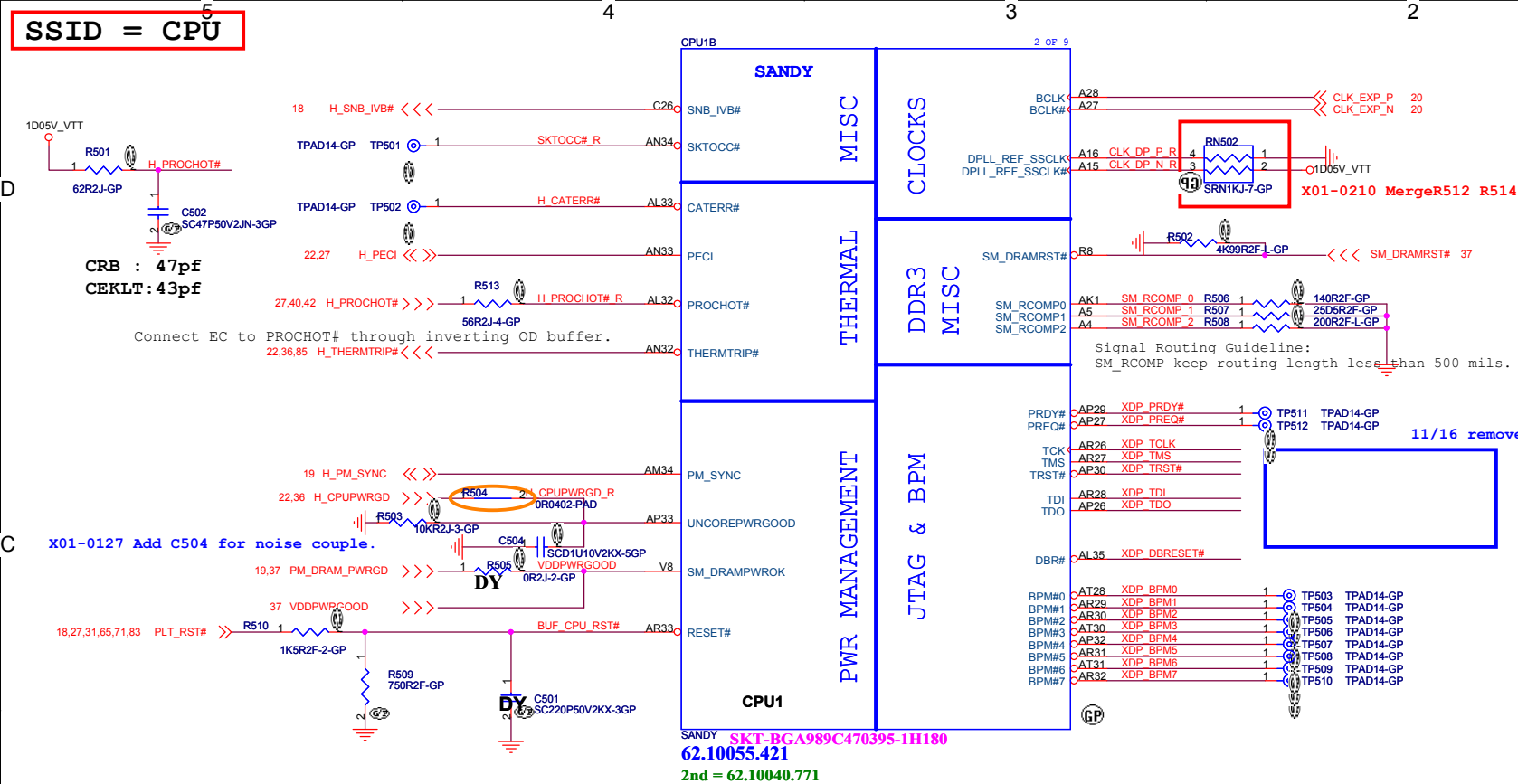
NOTE:
Select a Fast FET similar to 2N7002E whose rise/
fall time is less than 6 ns. If HPD on eDP interface is
disabled, connect it to CPU VCCIO via a 10-k pull-Up
resistor on the motherboard.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



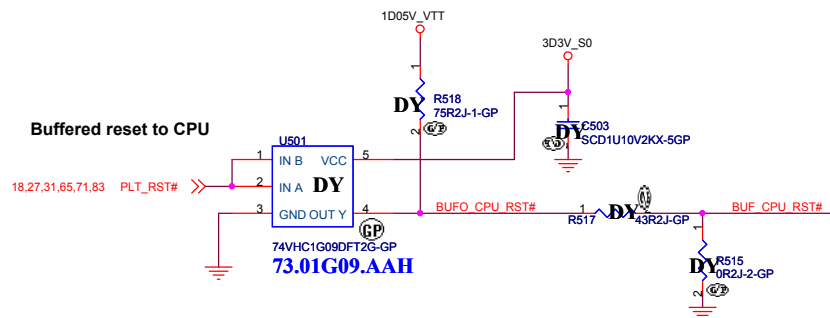
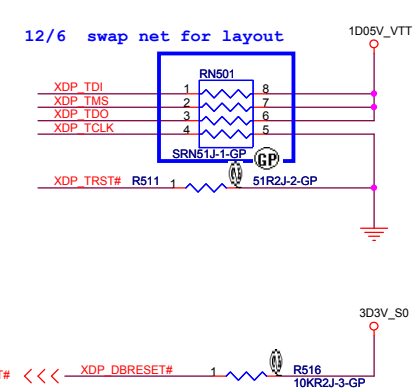
NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect
PEG Static Lane Reversal

SSID = CPU⁵



1

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through
1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP
through 1K +/- 5% resistor. power (~15 mW) may be
wasted.

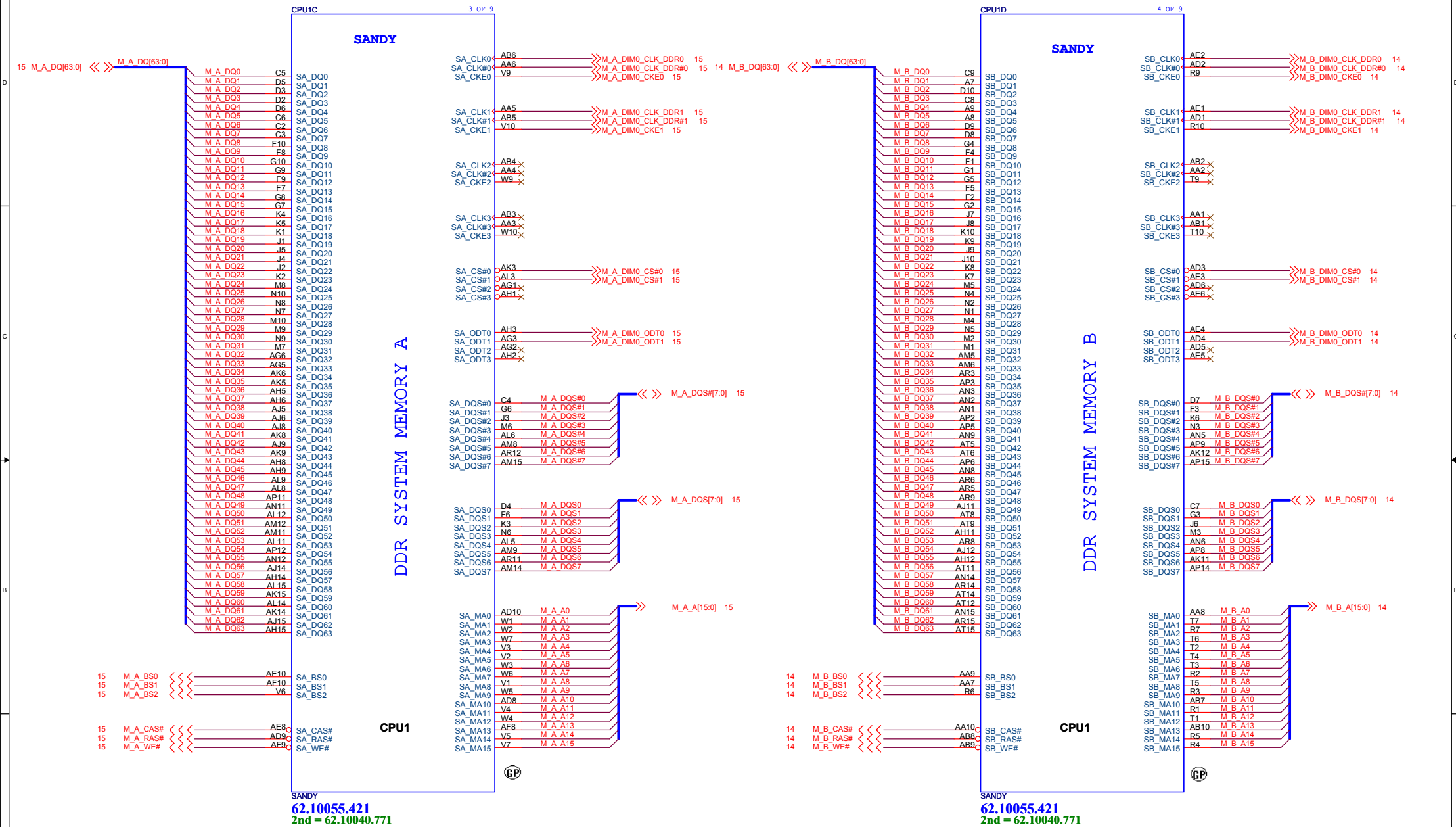


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Title	CPU (THERMAL/CLOCK/PM)
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SSID = CPU



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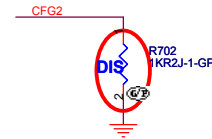
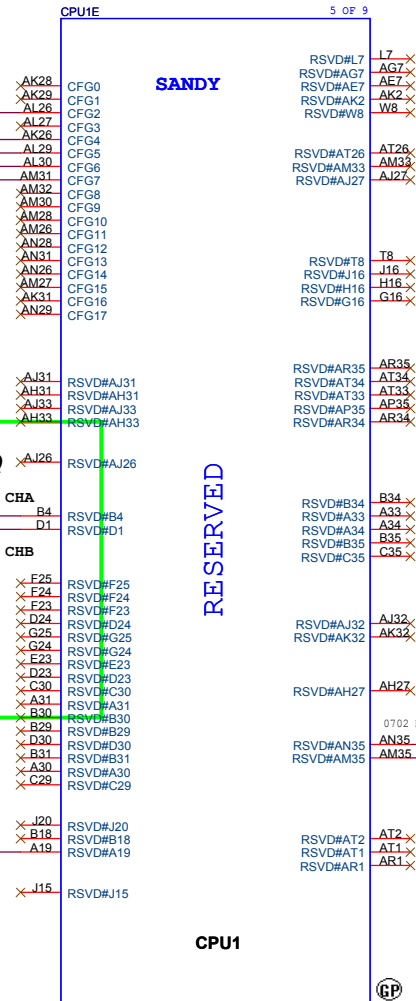
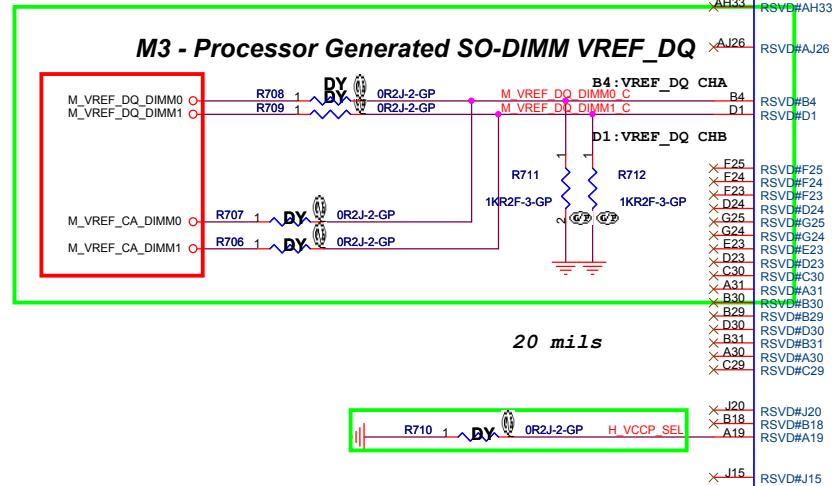


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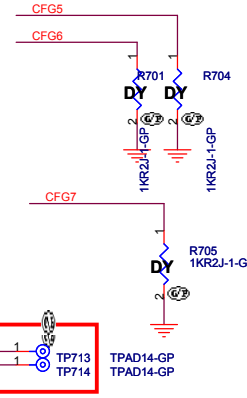
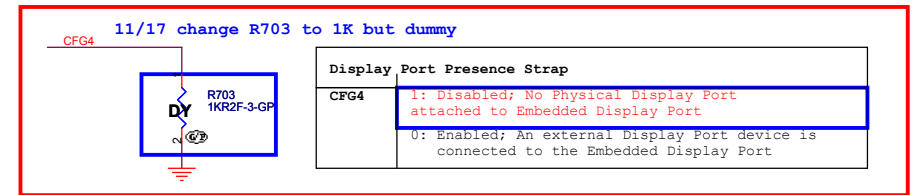
Title		
CPU (DDR)		
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SSID = CPU

11/17 remove TP715



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

SANDY SKT-BGA989C470395-1H180
62.10055.421
2nd = 62.10040.771

DN15AT1 Whistler

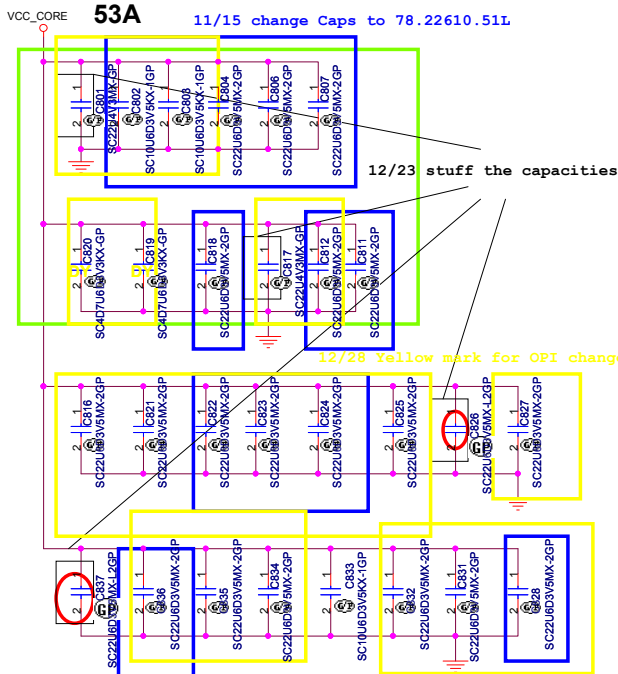
SSID = CPU

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

PROCESSOR CORE POWER

53A

11/15 change Caps to 78.22610.51L



VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

11/4 add Caps to 28 location as vendor recommend.
X01-0127 Stuff C812, C822, C831, C834
for VCC core noise issue.

X01-0217 Stuff C801=22uF
change C817 to 22uF

VCC_CORE

CPU1F

POWER

6 OF 9

SANDY

CORE SUPPLY

SVID

SENSE LINES

CPU1

SANDY

62.10055.421
2nd = 62.10040.771

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

12/28 Yellow mark for OPI change

PROCESSOR VCCIO: 8.5A

12/23 stuff the capacities

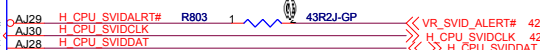
No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

11/16 follow DN13 to meet schematic check list

These resistors need to close to power IC
11/17 change part reference R807 to R805



VIDALERT#
VIDSCLK
VIDSOUT



VCC_CORE

R801
100R2F-1.1-GP-U

VCC_SENSE
VSS_SENSE

VCCIO_SENSE
VSSIO_SENSE

<Core Design>

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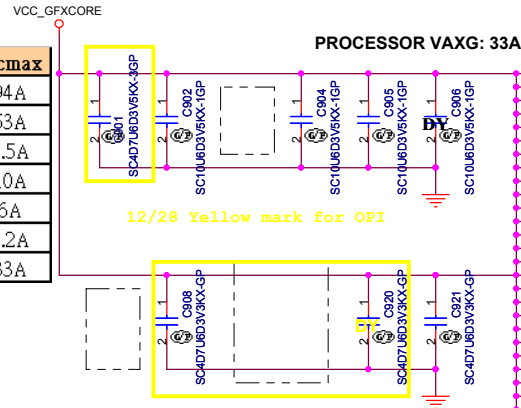
Title	CPU (VCC_CORE)	
Size	Document Number	Rev
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SSID = CPU

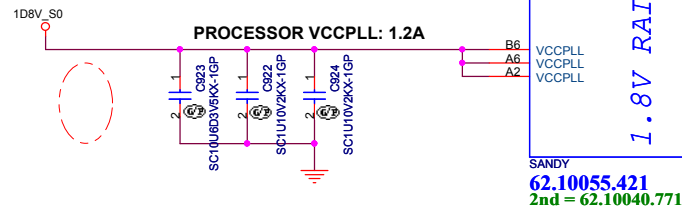
VAXG Output Decoupling Recommendation:

- 2 x 470 uF at Bottom Socket Edge
- 2 x 22 uF at Top Socket Cavity
- 4 x 22 uF at Top Socket Edge
- 2 x 22 uF at Bottom Socket Cavity
- 4 x 22 uF at Bottom Socket Edge

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

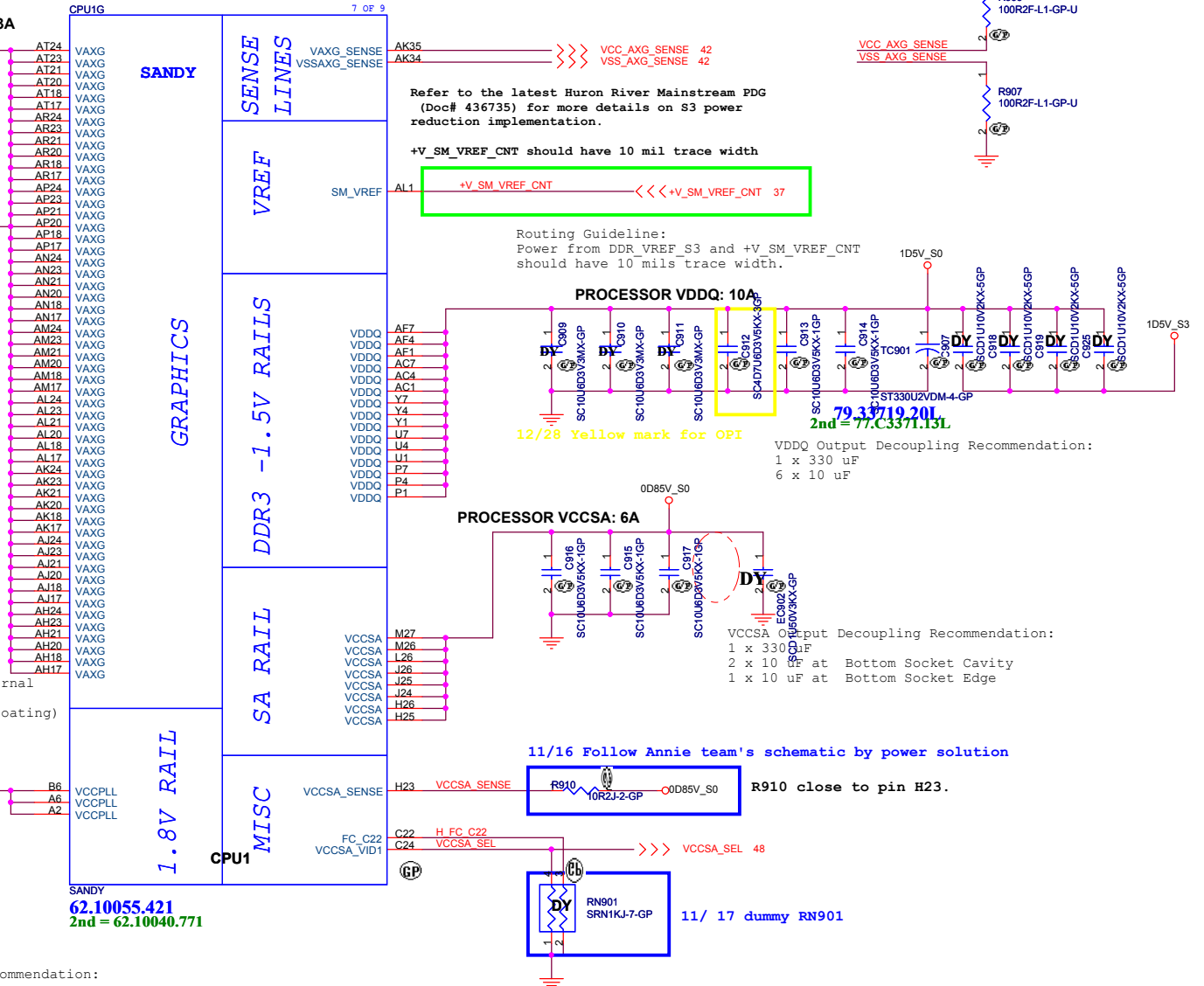


Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed



VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

POWER



<Core Design>



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CPU (VCC GFXCORE)Size
A3

Document Number

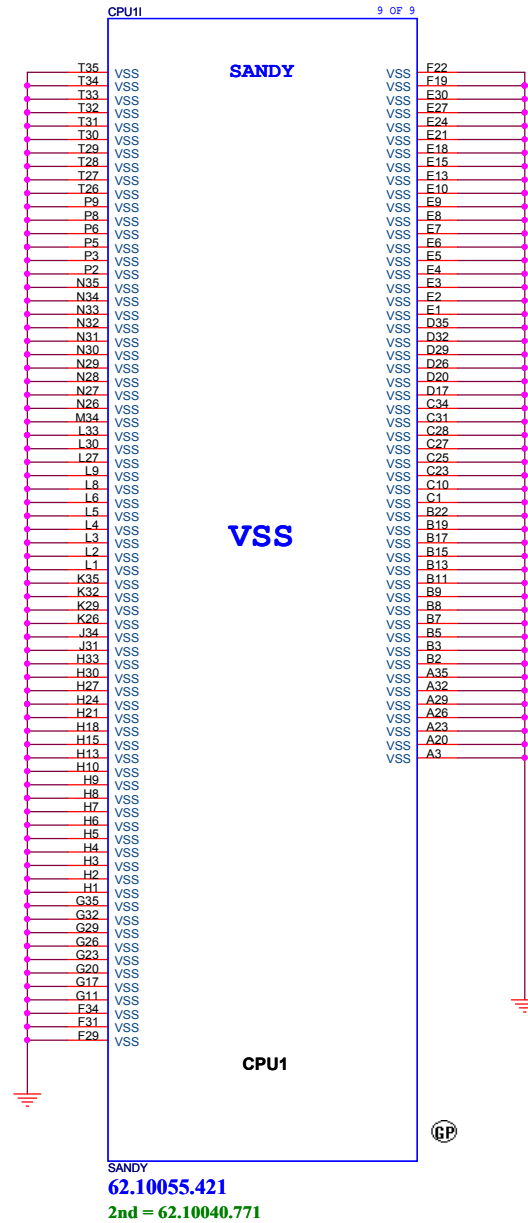
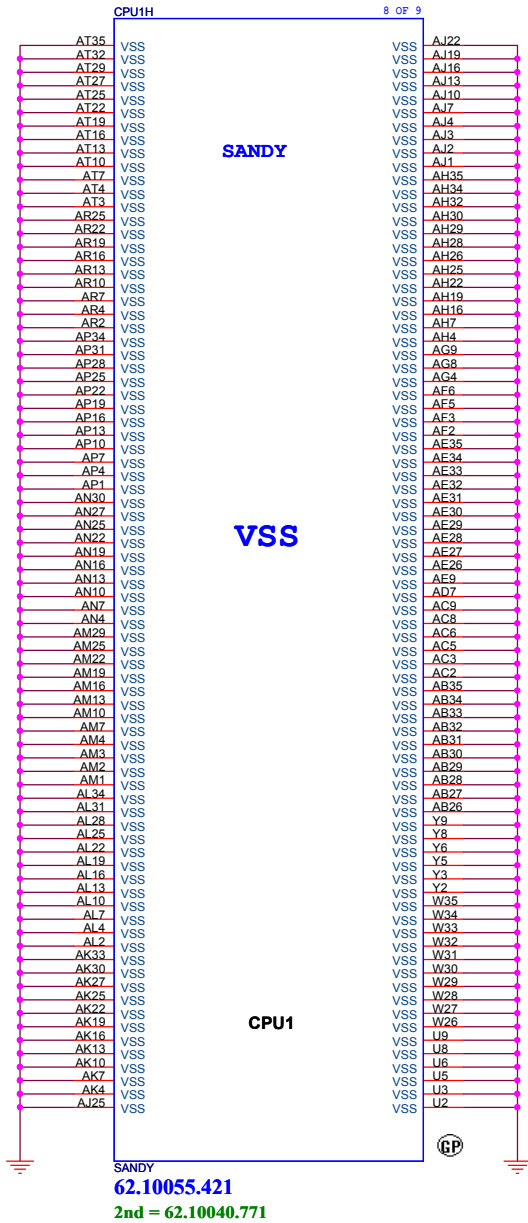
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SSID = CPU



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CPU (VSS)

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XDP

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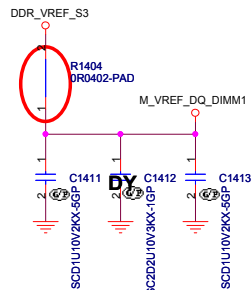
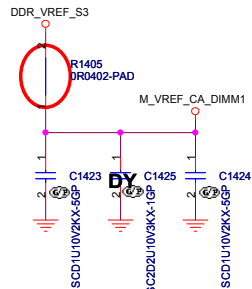
Rev
A00

Date: Wednesday, April 13, 2011

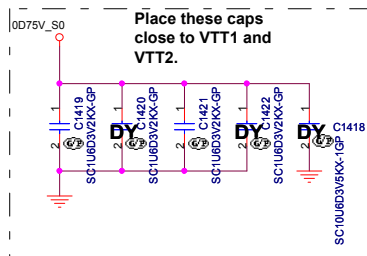
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Reserved

SSID = MEMORY



X02-0303 change 0R to short pad



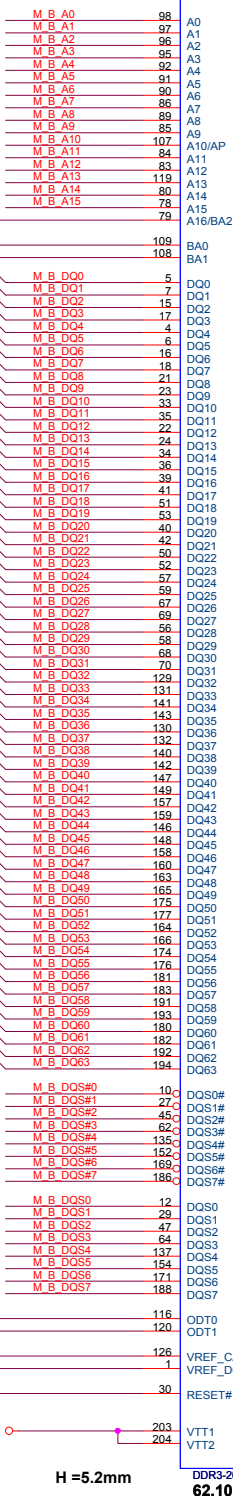
M_B_DQS# [7:0] 6

M_B_DQS [7:0] 6

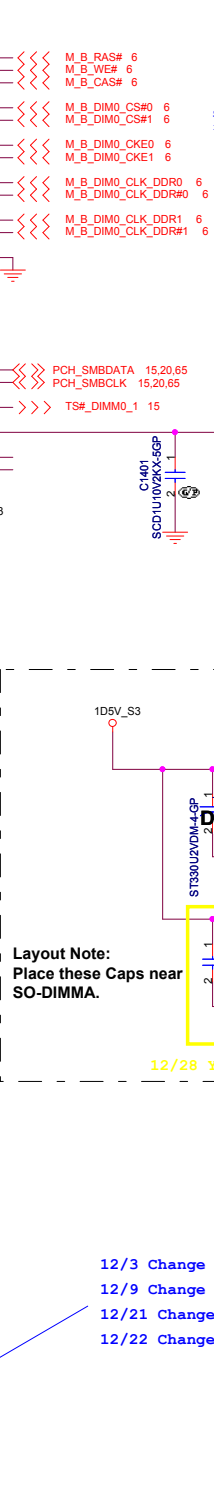
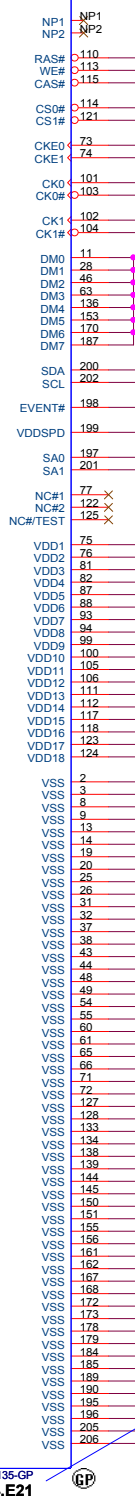
6 M_B_DIM0_ODT0 >>>
6 M_B_DIM0_ODT1 >>>
M_VREF_CA_DIMM1 >>>
M_VREF_DQ_DIMM1 >>>

15.37 DDR3_DRAMRST# >>>

0D75V_S0



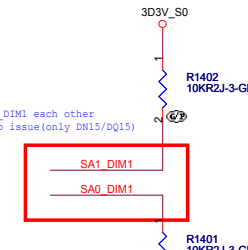
H = 5.2mm
DDR3-204P-135-GP
62.10024.E21



12/3 Change DM2 to 62.10024.E21
12/9 Change DM2 to 62.10017.K01
12/21 Change DM2 to 62.10017.P61
12/22 Change DM2 to 62.10024.E21

M_B_RAS# 6
M_B_WE# 6
M_B_CAS# 6
M_B_DIM0_CS#0 6
M_B_DIM0_CS#1 6
M_B_DIM0_CKE0 6
M_B_DIM0_CKE1 6
M_B_DIM0_CLK_DDR0 6
M_B_DIM0_CLK_DDR#0 6
M_B_DIM0_CLK_DDR1 6
M_B_DIM0_CLK_DDR#1 6

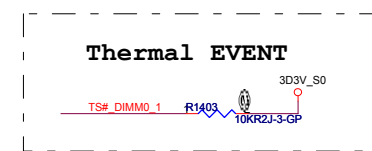
SNAP SA0_DIM1 and SA1_DIM1 each other
for DM2 can't boot up issue (only DN15/DQ15)



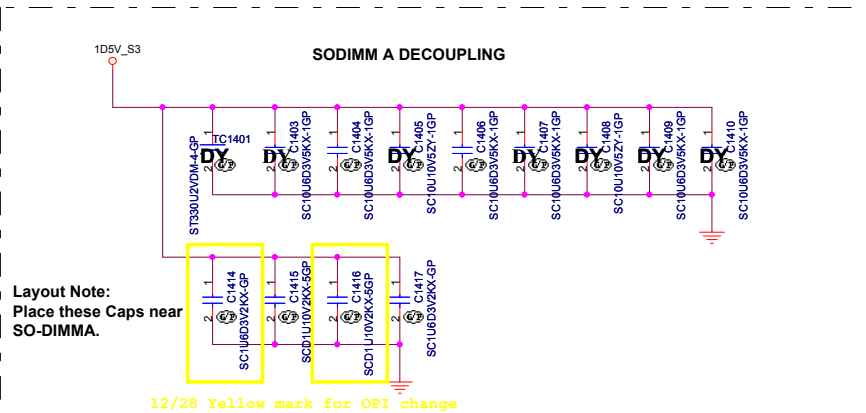
11/ 17 Change SMBus address note

Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34



SODIMM A DECOUPLING



Layout Note:
Place these Caps near
SO-DIMMA.

12/28 Yellow mark for OPI change

DN15ATI Whistler



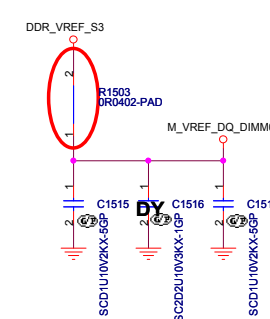
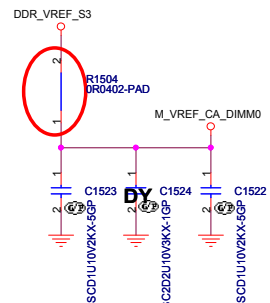
Title				
DDR3-SODIMM2				
Size	Document Number			Rev
Custom	Enrico Caruso 14			A0
Date:	Wednesday, April 13, 2011	Sheet	14	of 105

SSID = MEMORY

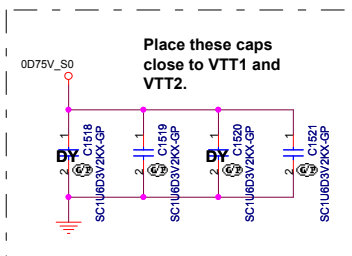
11/ 17 Change Smbus adress note

Note:
SO-DIMMB SPD Address is 0xA0
SO-DIMMB TS Address is 0x30

- SO-DIMMB is placed farther from the Processor than SO-DIMMA



X02-0303 change 0R to short pad



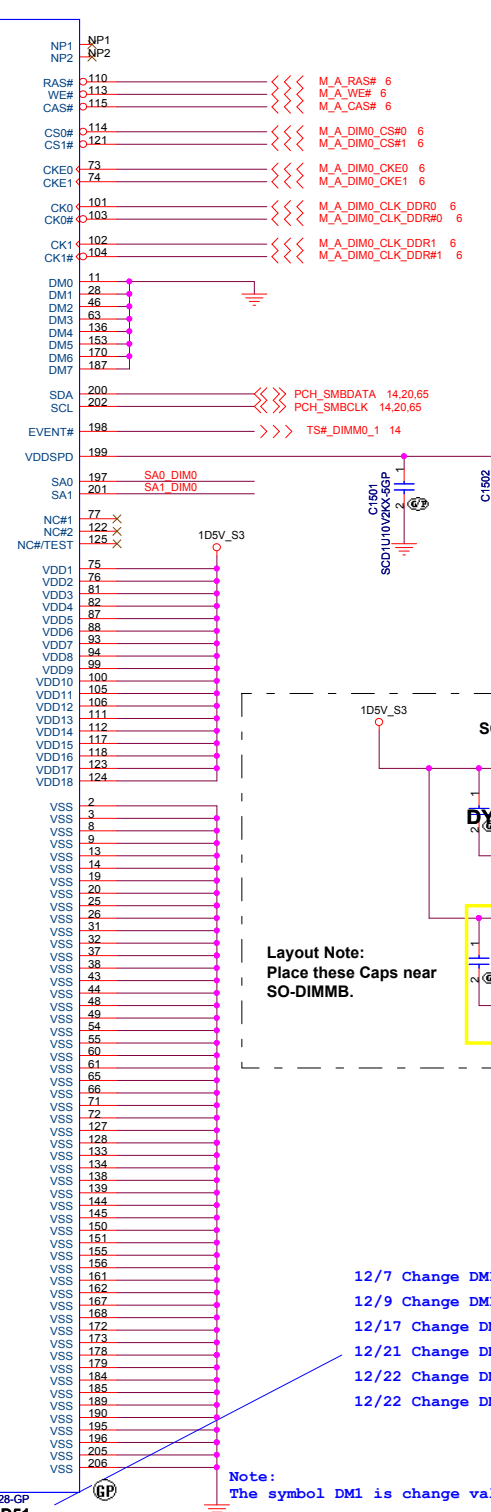
```
6 M_A_DIM0_ODT0 >>>
6 M_A_DIM0_ODT1 >>>
```

M_VREF_CA_DIMM0 
M_VREF_DQ_DIMM0

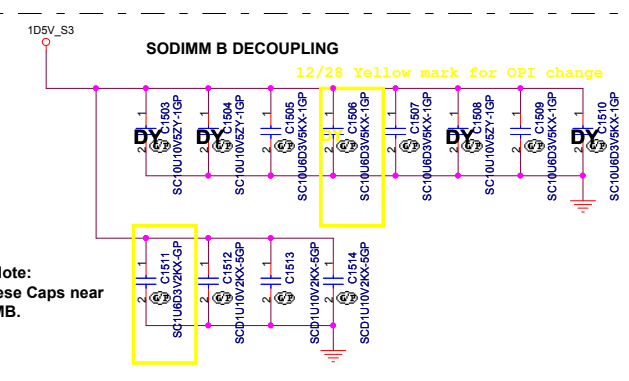
14,37 DDR3 DRAMRST# >>>

0D75V_S0

H =9.2mm

DDR3-204P-128-GP
62.10024.D51

Note:
The symbol DM1 is change value and PN only.



Layout Note:
Place these Caps near
SO-DIMMB.

```
12/7 Change DM1 to 62.10024.D51
12/9 Change DM1 to 62.10017.K11
12/17 Change DM1 to 62.10017.N11
12/21 Change DM1 to 62.10017.Q41
12/22 Change DM1 to 62.10024.D91
12/22 Change DM1 to 62.10024.D51
```

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Title			
DDR3-SODIMM1			
Size	Document Number	Rev	
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Title

Size
A3

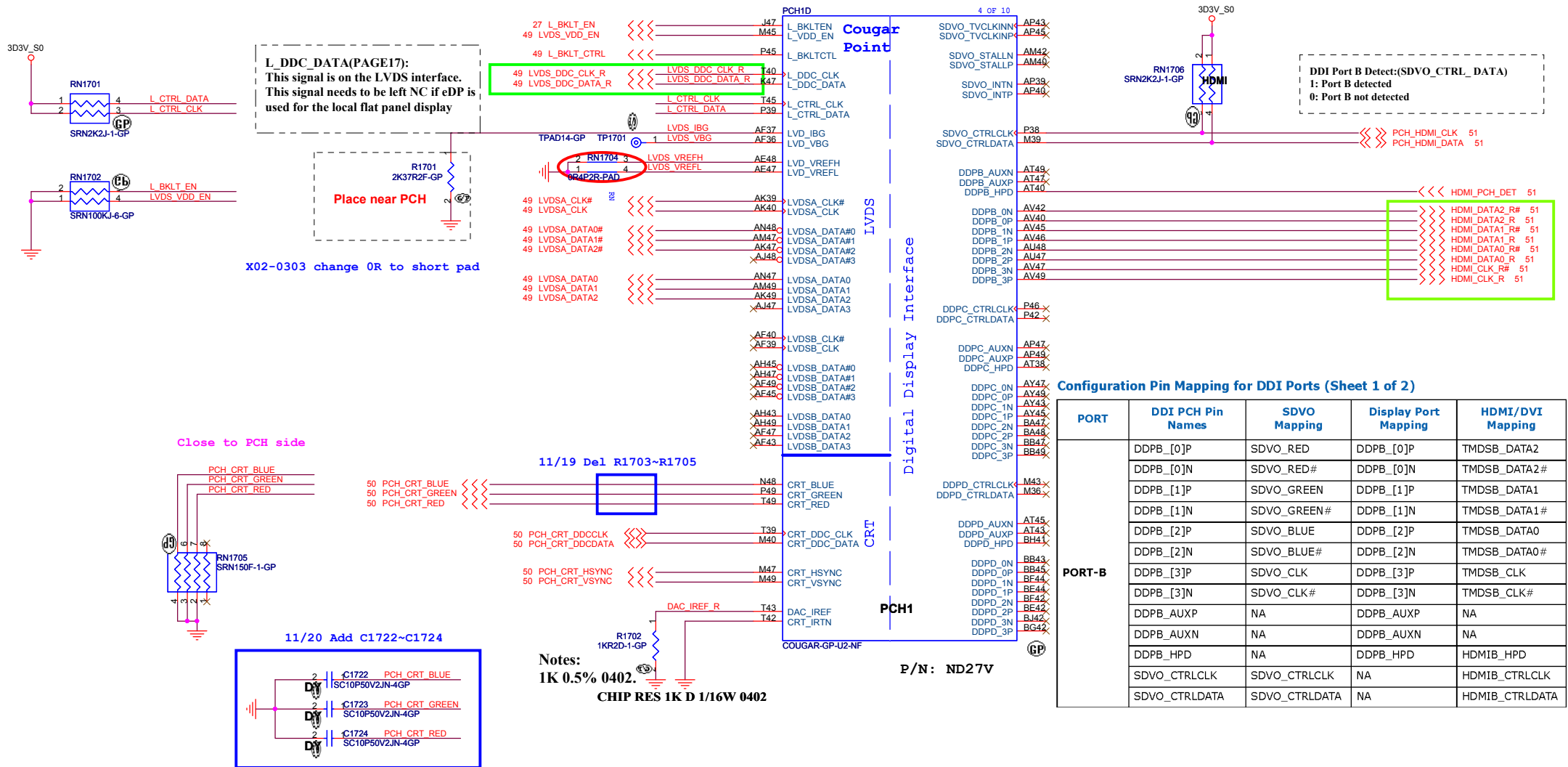
Document Number
Enrico Caruso 14

Rev
A00

Date: Wednesday, April 13, 2011

Sheet 16 of 105

Reserved



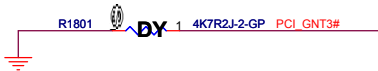
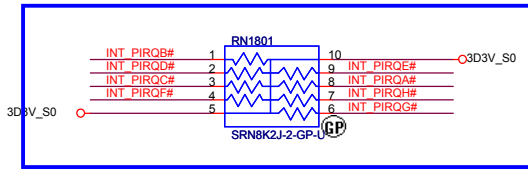
<Core Design>



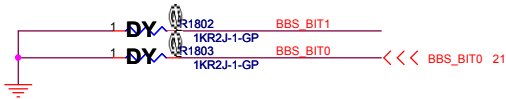
Wistron Corporation
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SSID = PCH

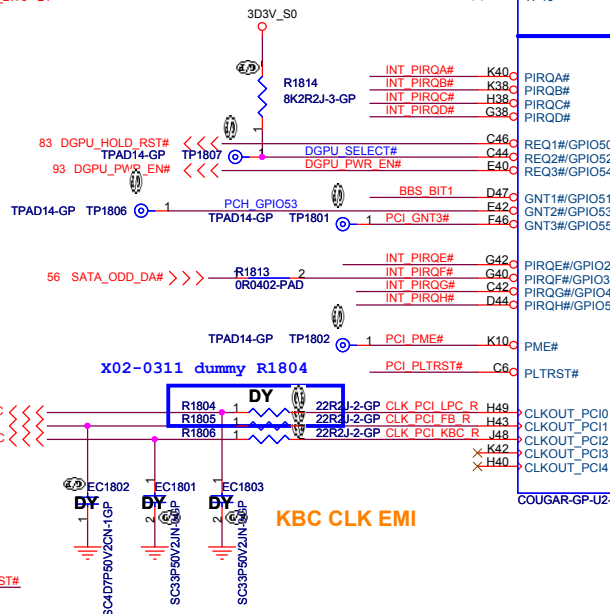
12/2 Net swap for layout



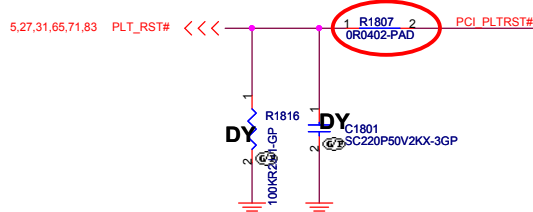
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GF/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)



X02-0303 change 0R to short pad



Cougar
Point

NVRAM

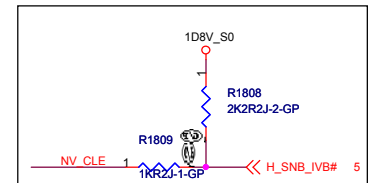
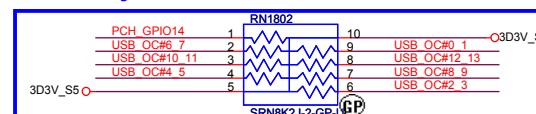
RSVD

USB

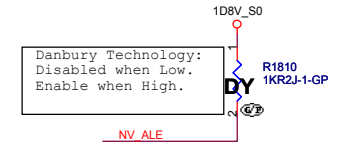
PCH1

Swap net for layout

11/11 change to RN1802 to meet schematic check result.



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



```

X USB Ext. port 1 (HS)
X External debug port use on Huron river platform

```

USB Table

Pair	Device
0	X
1	USB Ext. port 2 (MB)
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 3
9	USB Ext. port 1
10	X
11	Mini Card1 (WLAN+BT)
12	CAMERA
13	X

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

<Core Design>



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Document Number

Date: Wednesday, April 13, 2011

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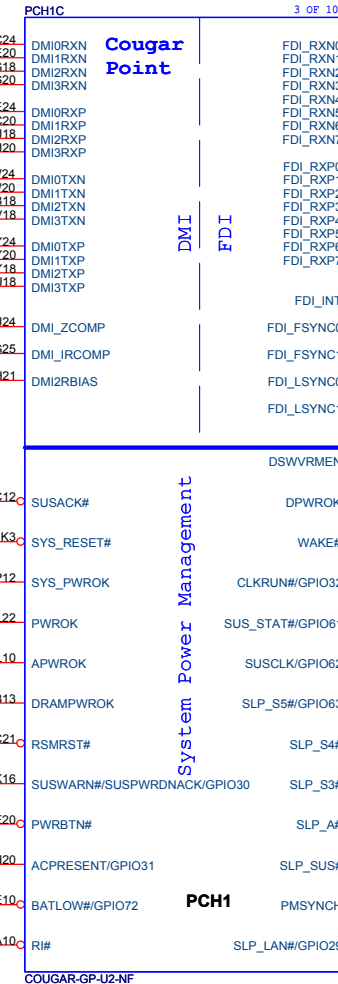
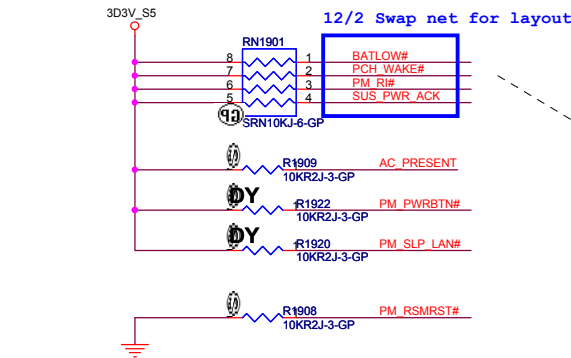
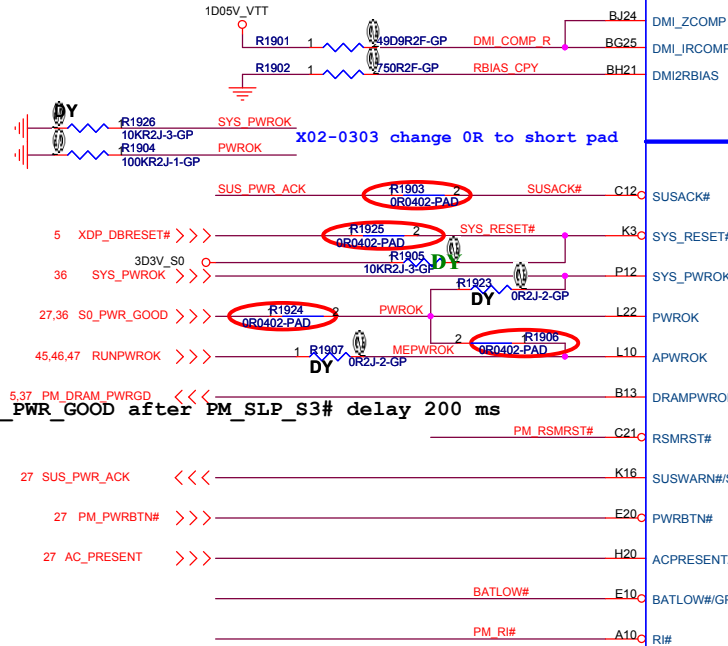
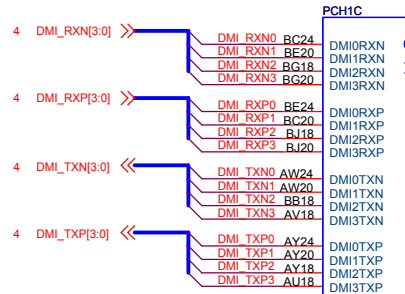
PCH (PCI/USB/NVRAM)

Enrico Caruso 14

A00

SSID = PCH

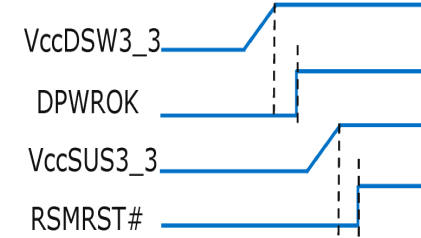
Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



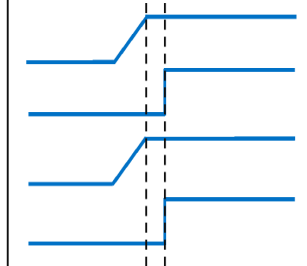
P/N: ND27V

PM_RSMRST# R1912 2 0R0402-PAD <<< RSMRST#_KBC 27

Deep S4/S5 Supported



Deep S4/S5 Not Supported

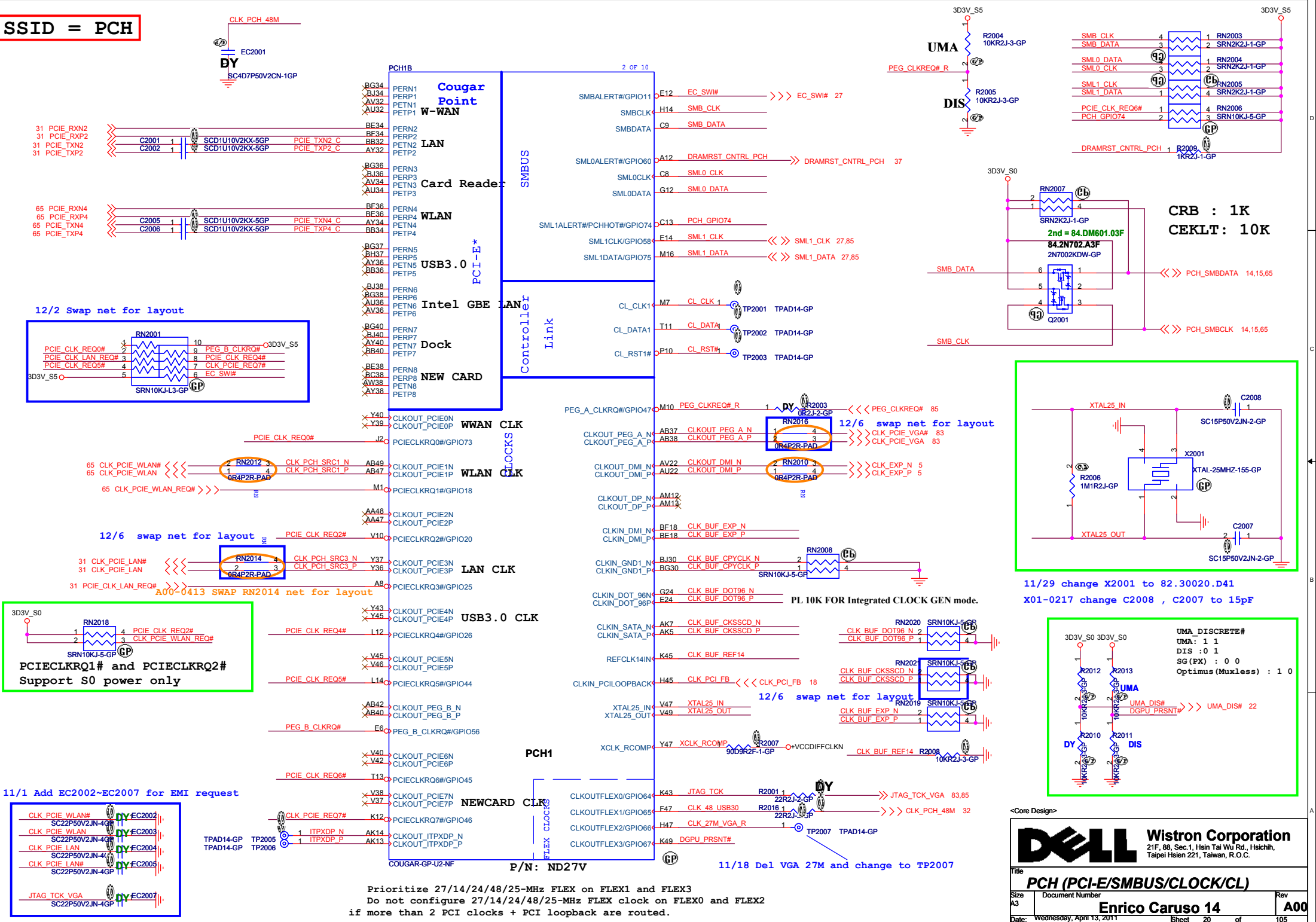


- For platforms not supporting Deep S4/S5
- 1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
 - 2.DPWROK and RSMRST# will rise at the same time (connected on board)
 - 3.SLP_SUS# and SUSACK# are left as "no connect"
 - 4.SUSWARN# used as SUSPWRDNACK/GPIO30

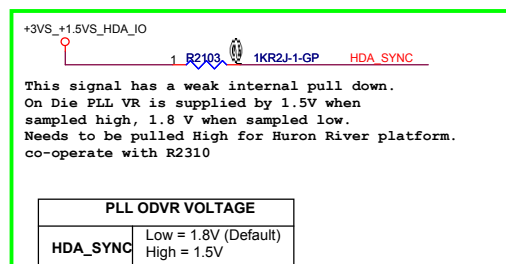
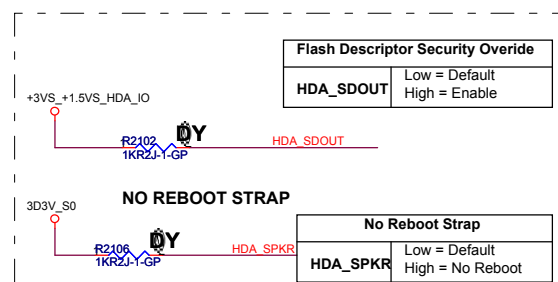
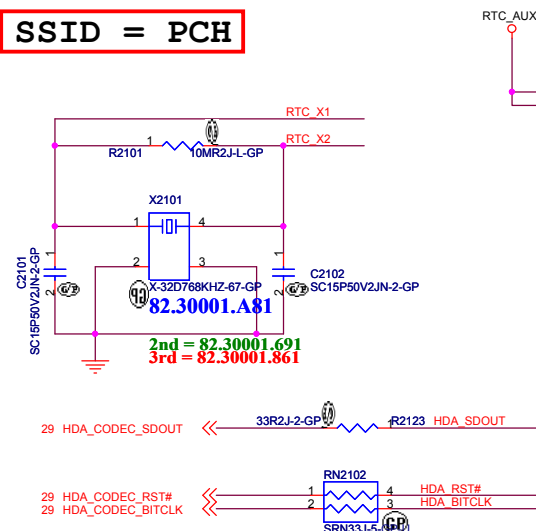
DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

DSWODVREN circuit diagram showing connections for R1917, R1918, R1919, and R1920.

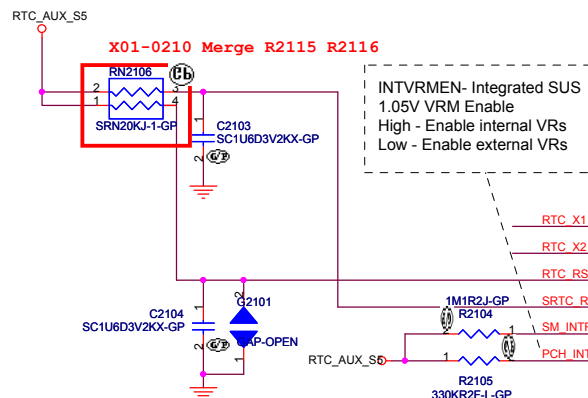
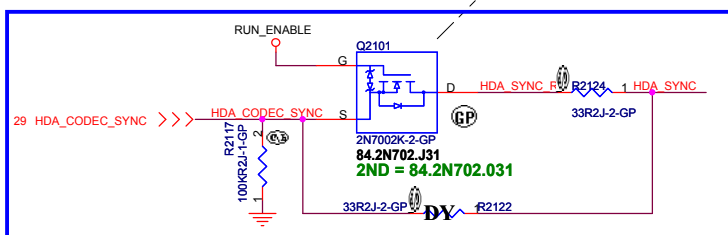
SSID = PCH



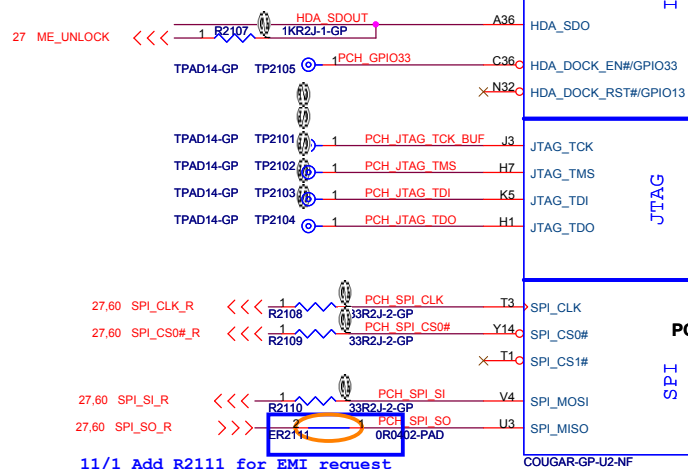
SSID = PCH



11/2 Merge R2122 into Q2101



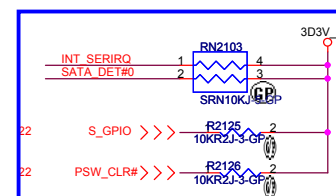
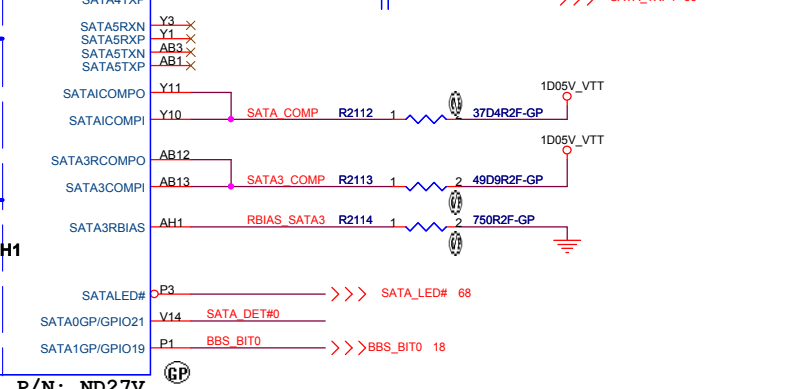
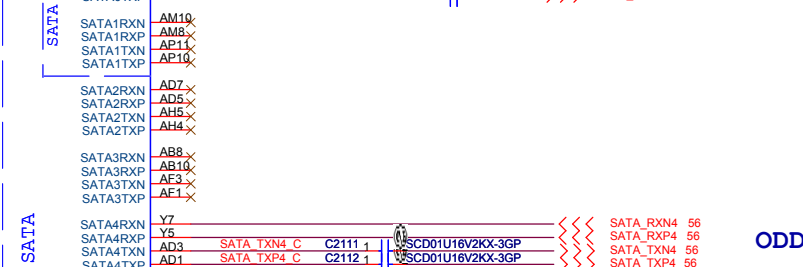
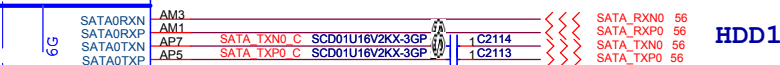
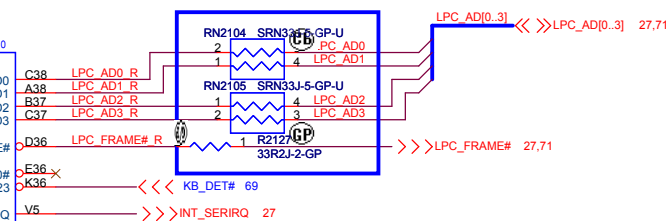
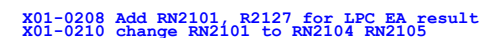
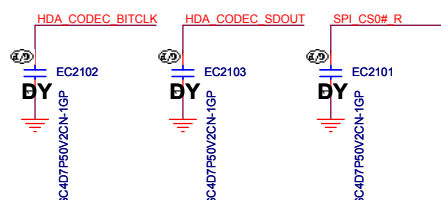
Notes:
ME_UNLOCK (HDA_SDO) connect to EC.
Make sure EC drive this pin "low" all the time.



11/1 Add R2111 for EMI request

11/ 17 change R2111 from 33ohm to 0ohm and change to ER2111

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

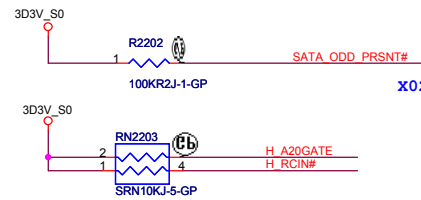


12/6 Separate RN2103 to
R2125 and R2126

11/11Remove RN2104 and FP DET#

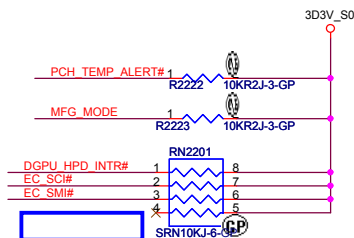
SSID = PCH

Note:
For PCH debug with XDP, need to DUMMY R2218

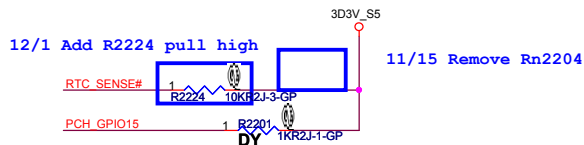


GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

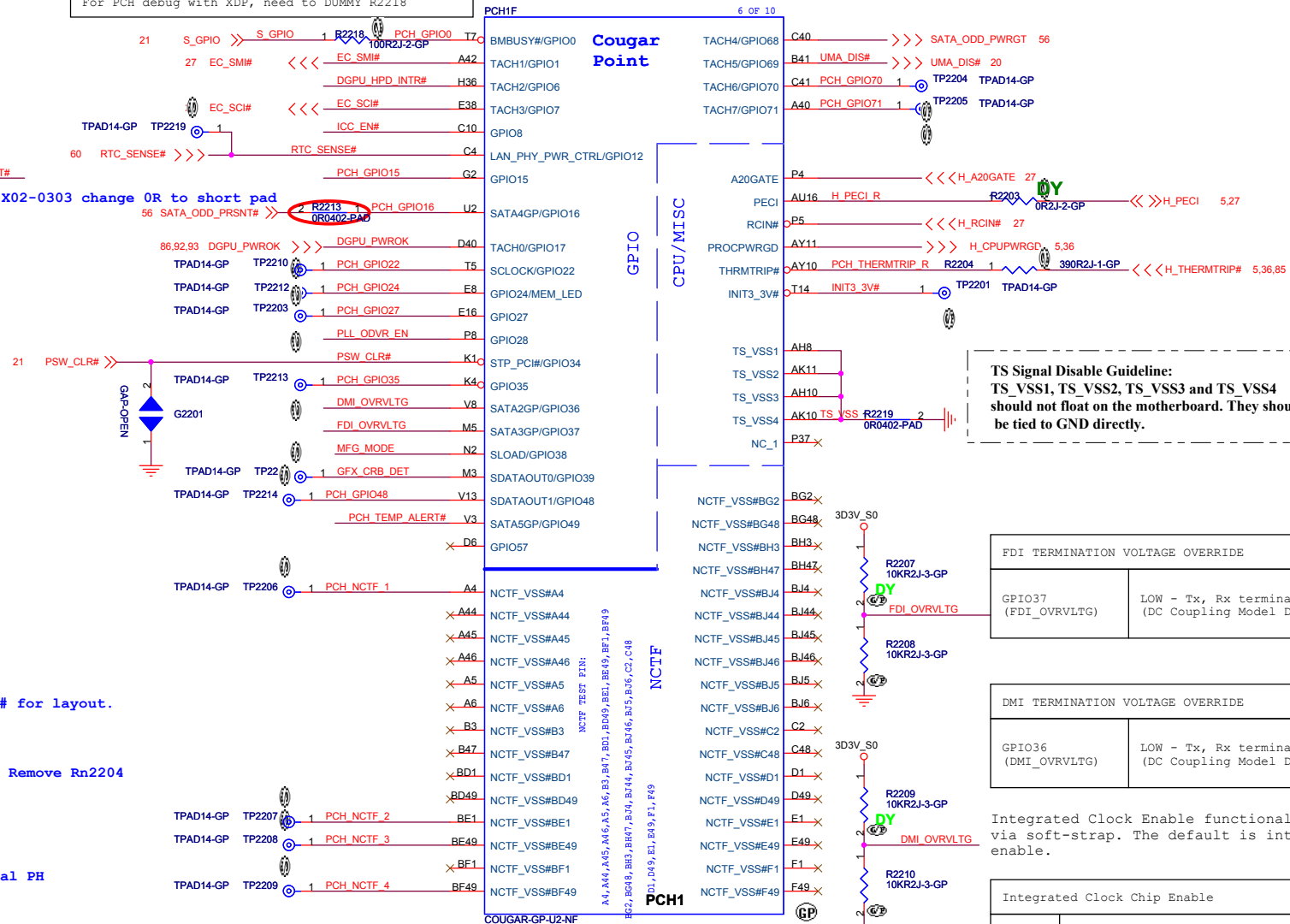
11/11 Remove R2220 for GPIO48 set to GPO



```
11/11Remove DBC EN
X01-0211 swap DGPU_HPD_INTR#, EC_SMI# for layout.
```



11/ 17 Dummy R2201 because GPIO15 internal PH



TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4
 should not float on the motherboard. They should
 be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

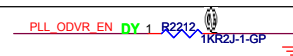
DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT] LOW (R2211) - ENABLED

P GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE: This signal has a weak internal pull-up 20kΩ to VDD.
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)



<Core Design>



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Title

PCH (GPIO/CPU)

Size
A2

Document Number

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Date _____

Wednesday, April 13, 2011

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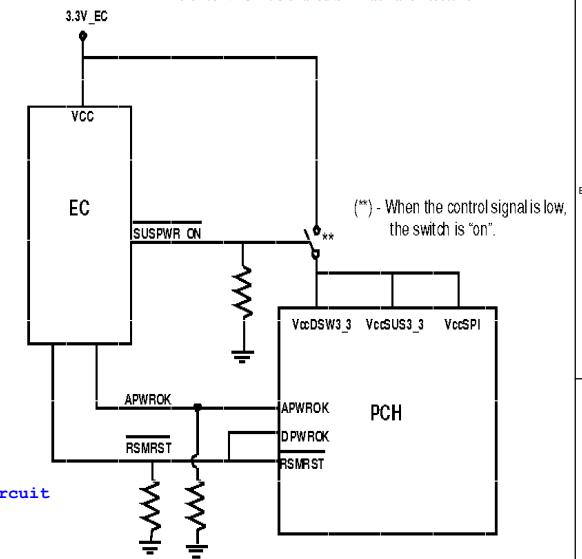
Rev	
A00	

SSID = PCH 6A

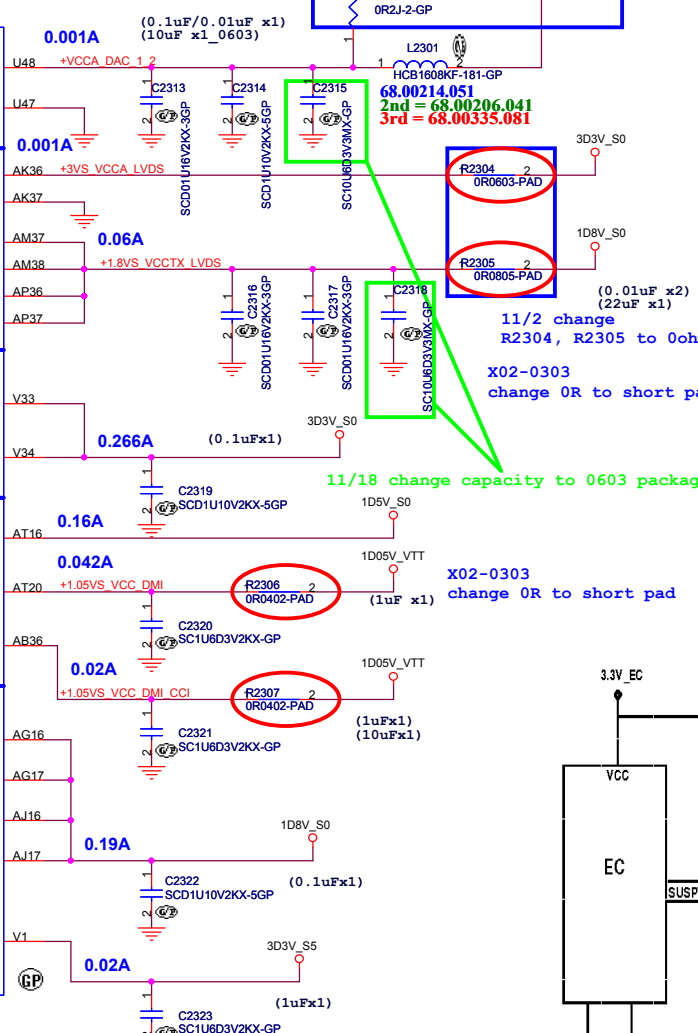
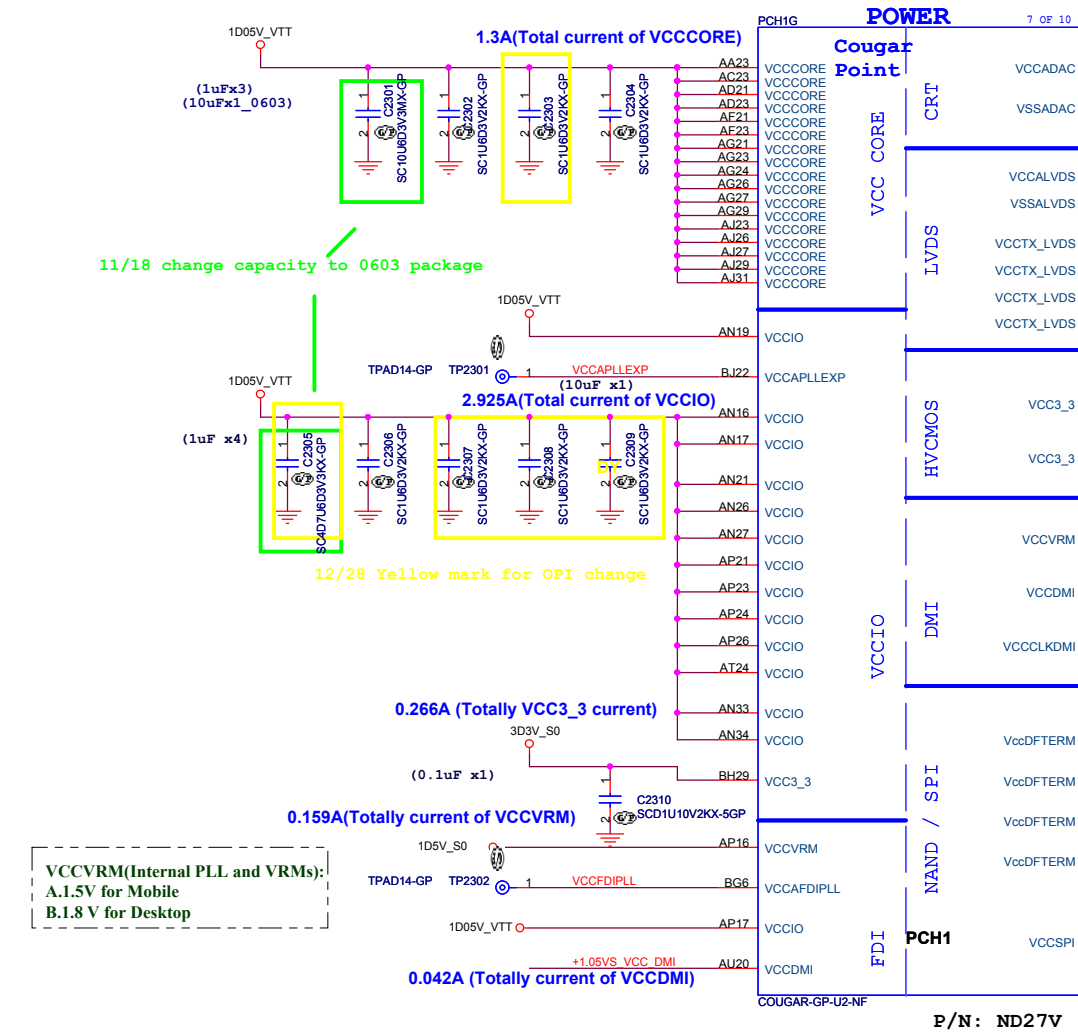
11/ 17 Add R2301 but dummy it
and change L2301 source to 3D3V_DAC_S0

Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLb	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTerm	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Refer to NPCE795 shared SPI flash architecture



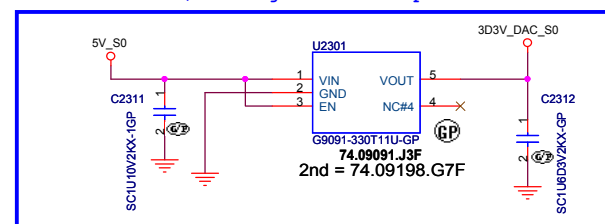
<Core Design>



P/N: ND27V

11/3 Add LDO for CRT DAC power

11/ 17change U2301 Vout power rail and stuff the circuit



VCCVRM(Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop

11/18 change capacity to 0603 package

12/28 Yellow mark for OPI change

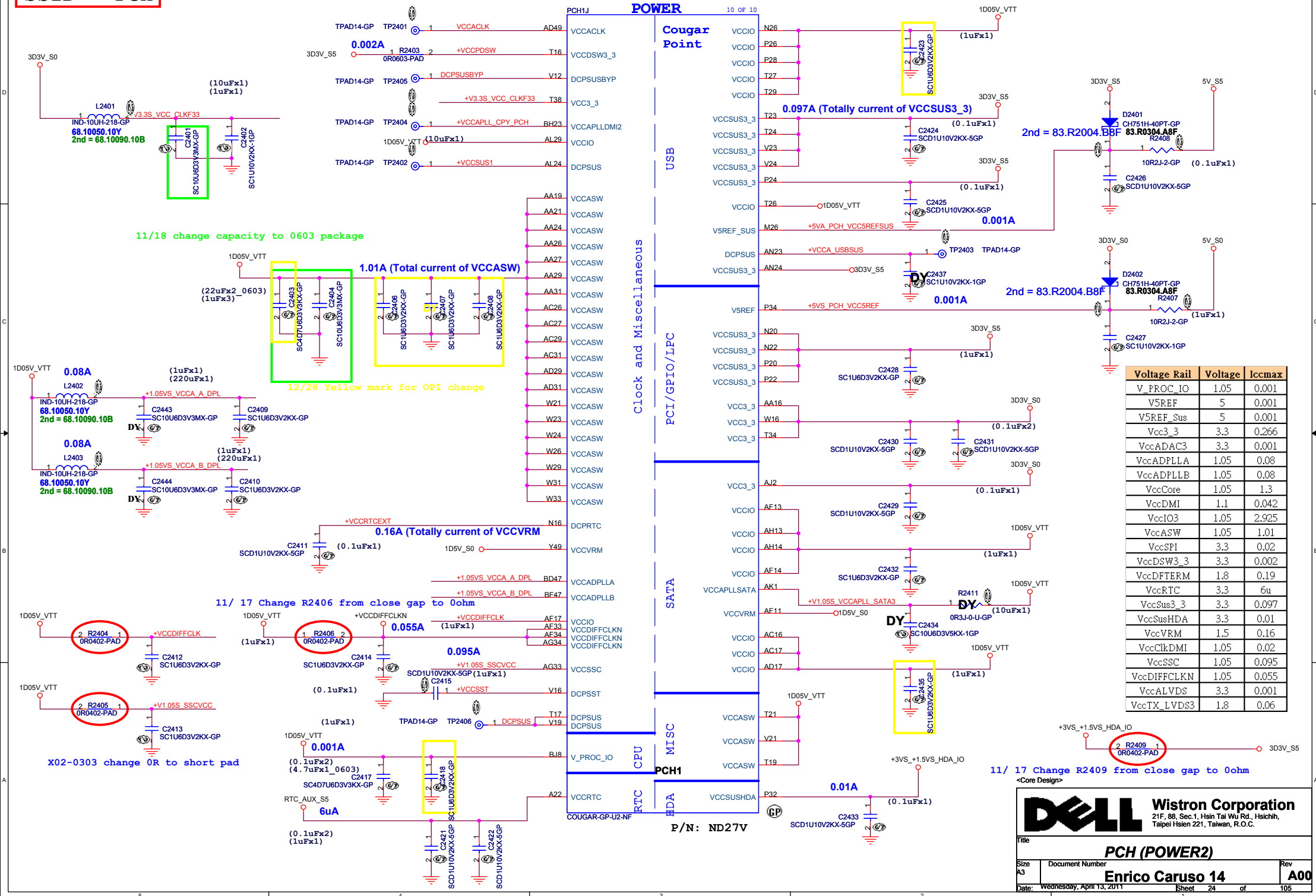
68.00214.051
2nd = 68.00206.041
3rd = 68.00335.081

11/2 change
R2304, R2305 to 0ohm
X02-0303
change 0R to short pad

11/18 change capacity to 0603 package

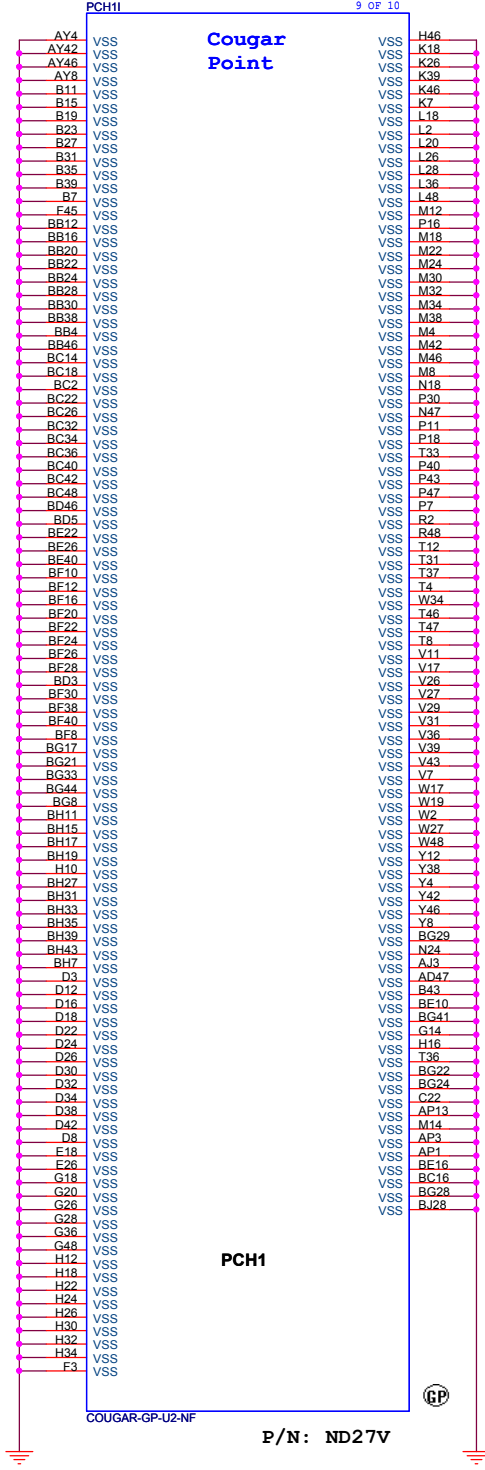
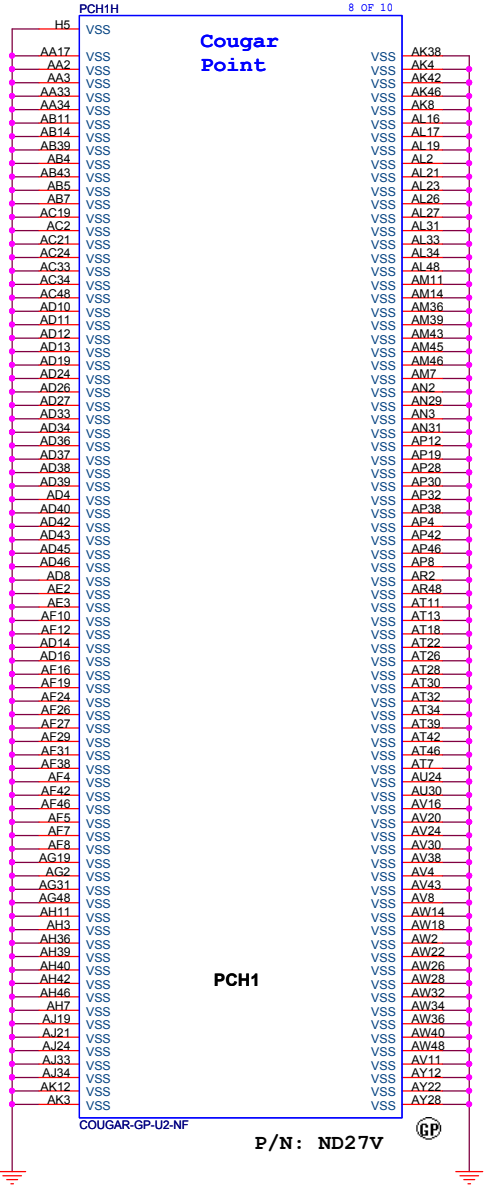
X02-0303
change 0R to short pad

SSID = PCH



Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

SSID = PCH



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Title: **PCH (VSS)**

Size: A3	Document Number: Enrico Caruso 14	Rev: A00
Date: Wednesday, April 13, 2011	Sheet: 25	of: 105

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Title

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A3

Document Number
Enrico Caruso 14

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A00

Date: Wednesday, April 13, 2011

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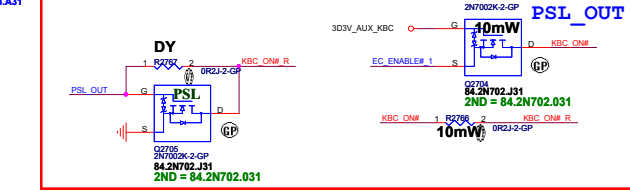
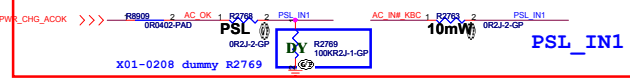
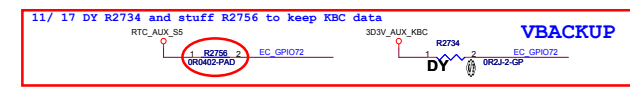
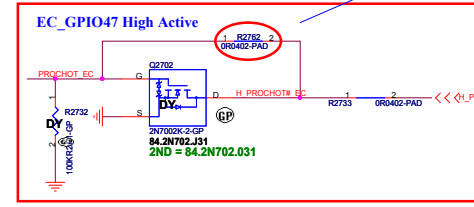
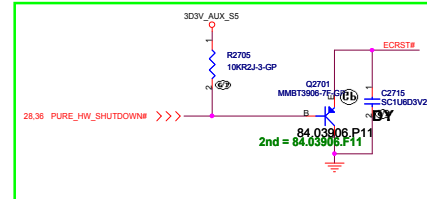
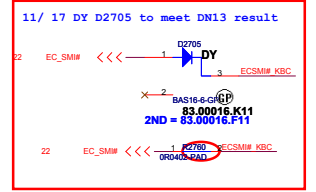
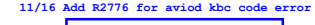
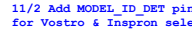
[illegible]

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

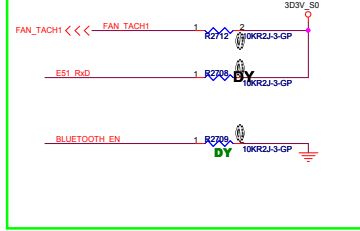
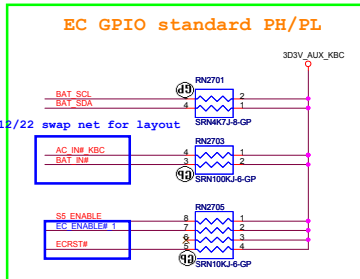
NOTES:
The NPCE795P GPIO/PWM outputs that are connected to LEDs have high drive buffers (20mA) and can be connected directly to the LEDs.

MODEL_ID_DET(GPI007)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Reserved	100.0K	10.0K(64.10025.GDL)	3.0V
Reserved	100.0K	20.0K(64.10025.GDL)	2.75V
D015_GNA with HNM1	100.0K	33.0K	2.48V
D015_GNA without HNM1	100.0K	47.0K(64.47025.GDL)	2.24V
D014_GNA with HNM1	100.0K	64.9K(64.44925.GDL)	2.0V
D014_GNA without HNM1	100.0K	76.8K(64.76825.GDL)	1.87V
D014_D015(12N) with HNM1	100.0K	106.4K(64.10035.GDL)	1.65V
D014_D015(12N) without HNM1	100.0K	143.0K(64.14335.L0L)	1.358V
D014_D015(1G) with HNM1	100.0K	174.0K(64.17435.GDL)	1.204V
D014_D015(1G) without HNM1	100.0K	215.0K(64.21535.GDL)	1.048V

Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil



NOTES:
Please make sure there's no pull-down resistor on USB_PWR_EN#,AC_PRESENT,E51_TX



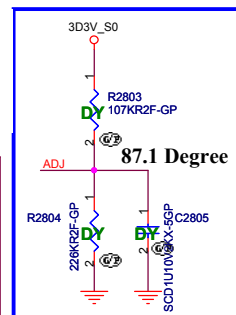
SSID = Thermal

Thermal sensor P2800

Option 1: OTZ=95°C → ADJ=3.3V

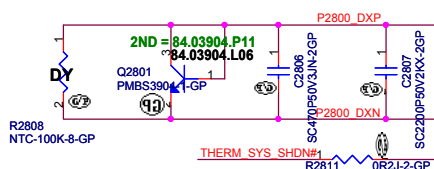
Option 2: OTZ=85°C → ADJ=Floating

Option 3: OTZ=90°C → ADJ=GND

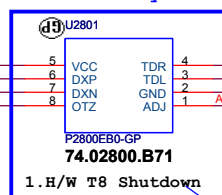


12/14 dummy R2803, R2804 and C2805

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.



2.System Sensor, Put on palm rest

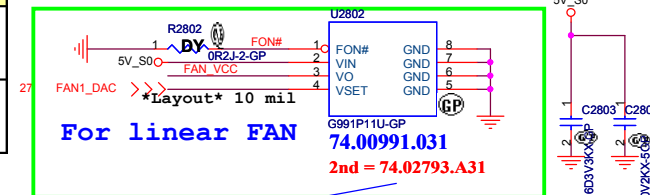


Very Close to CPU1

SYS_THRM 27
CPU_THRM 27

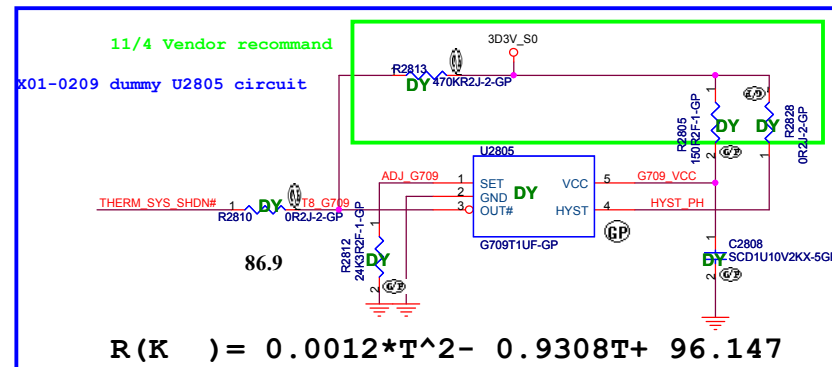
	Pin-1	Definition
P2793A	/FON	Low(<0.4V): VOUT =Vin and the fan is fully-on High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm
P2793B	EN	Low(<0.4): IC is shutdown. High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm

Fan controller P2793



Very close to CPU1

12/15 Remove 3rd source

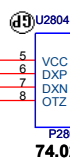
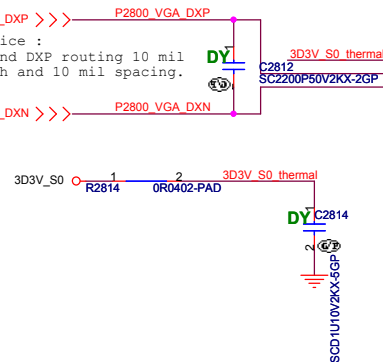


X02-0309 change AFTP to followDV14 AMD

12/13 change P2800 to ver B

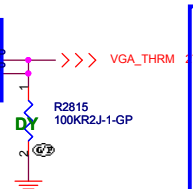
VGA Thermal sensor P2800

85 P2800_VGA_DXP >>> P2800_VGA_DXP
Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.
85 P2800_VGA_DNX >>> P2800_VGA_DNX

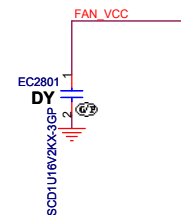


X02-0311 Add R2816& R2817 to
option VGA_THRM
and DY the circuit

11/18 remove R2817, R2818, C2816
and NC U2804 OTZ pin



EMI/ESD

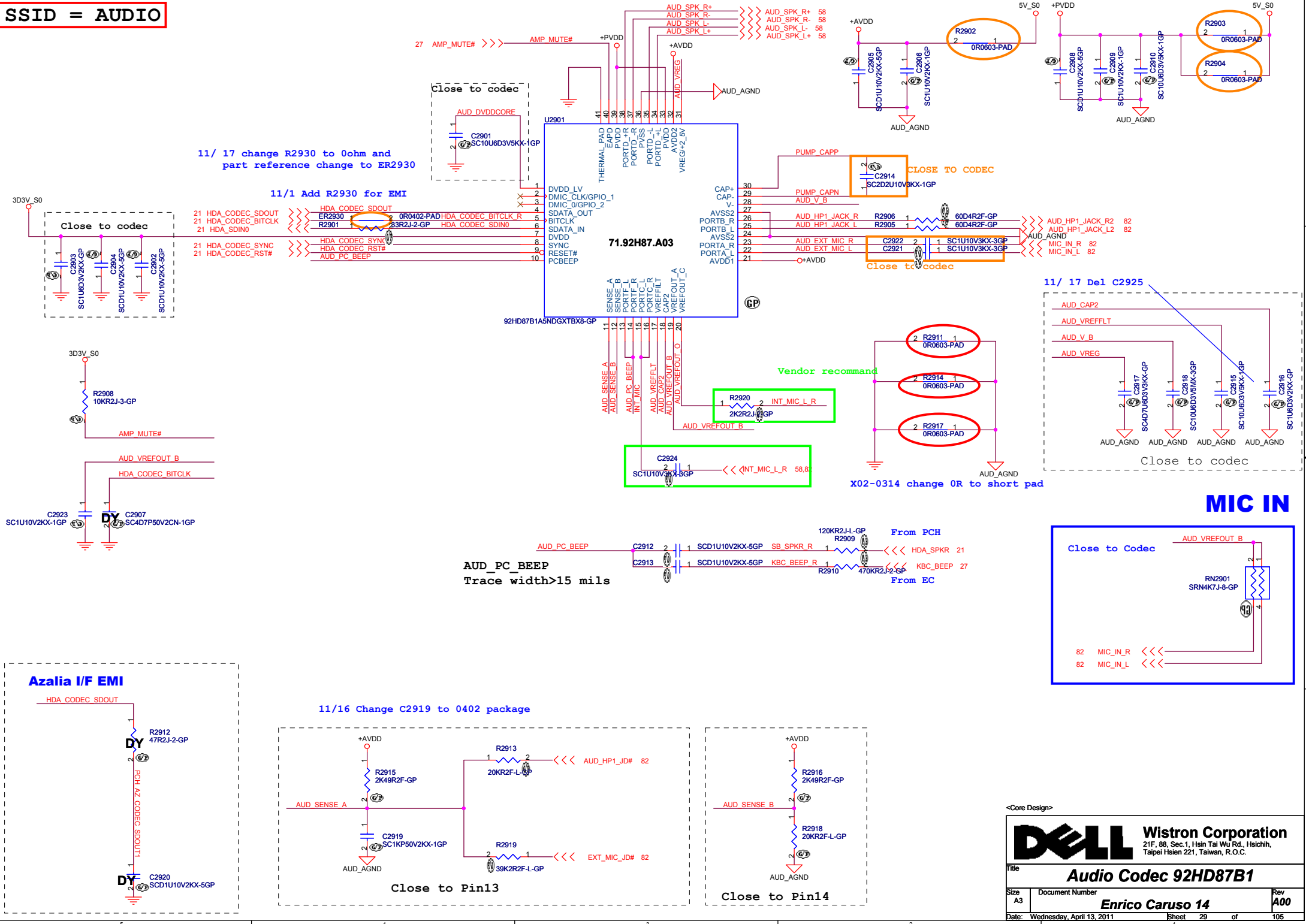


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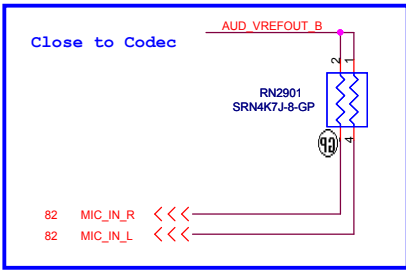


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SSID = AUDIO



MIC IN



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Title Audio Codec 92HD87B1		
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DN15ATI Whistler



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number
Enrico Caruso 14

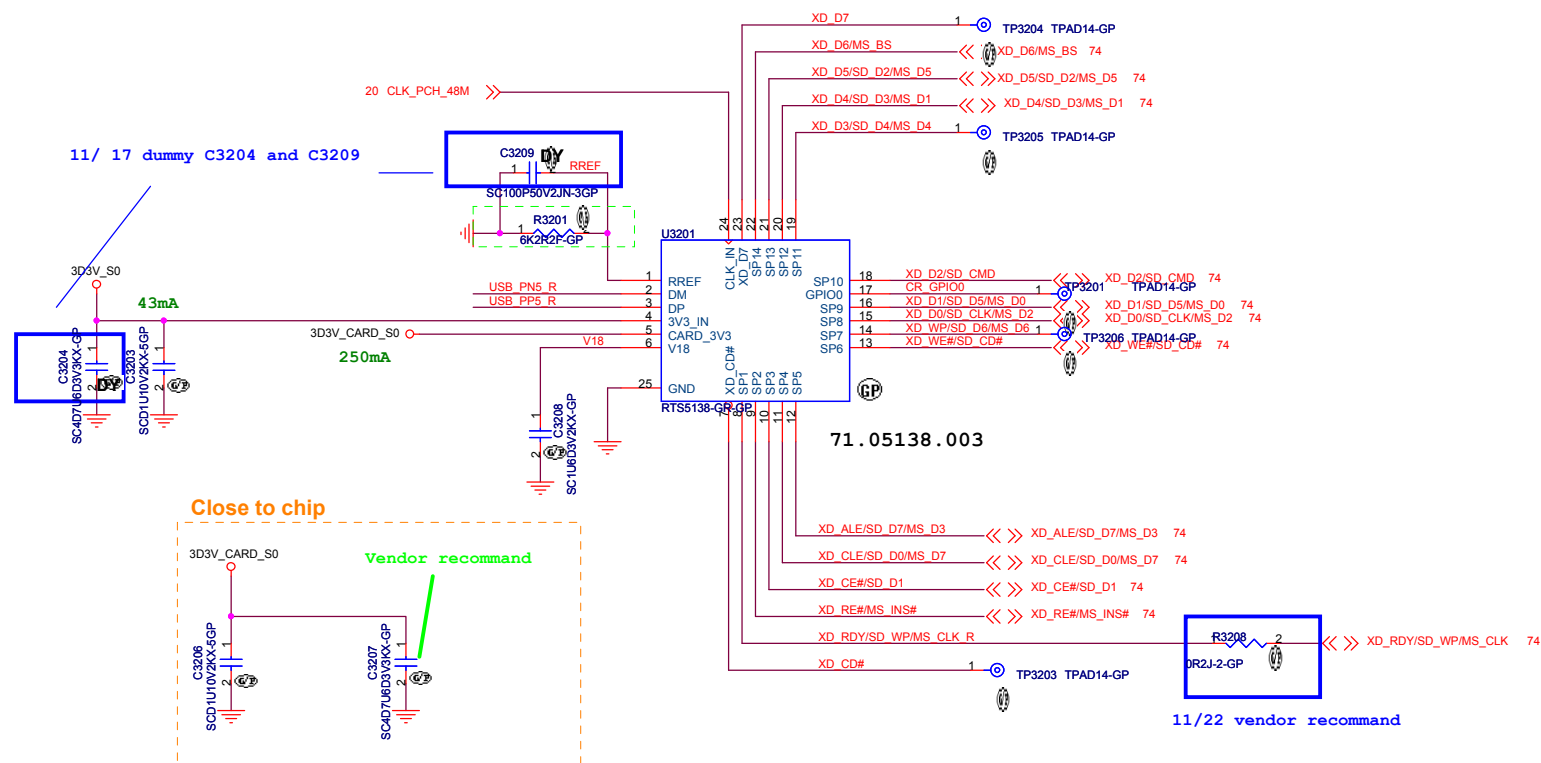
Rev
A00

Date: Wednesday, April 13, 2011

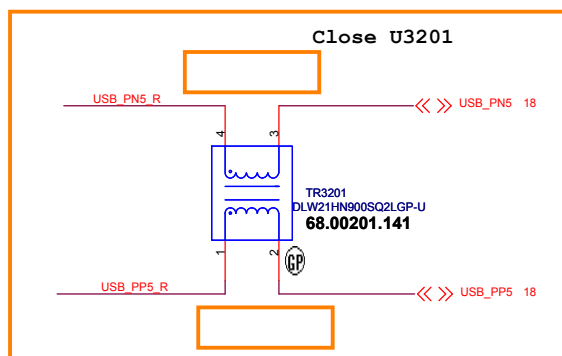
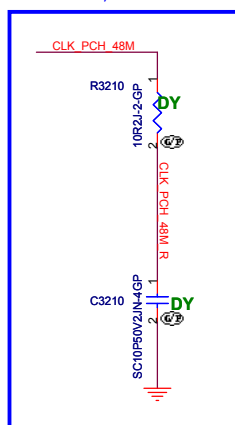
Sheet 30 of 105

Reserved

SSID = SDIO



11/1 Add R3210, C3210 for EMI



X02-0311 stuff TR3201 and change symbol to 68.00201.141

A00-0324 change TR6102 to TR3201

A00-0406 remove R3206, R3207 PAD

<Core Design>

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Reserved

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Title

Size
A3

Document Number
Enrico Caruso 14

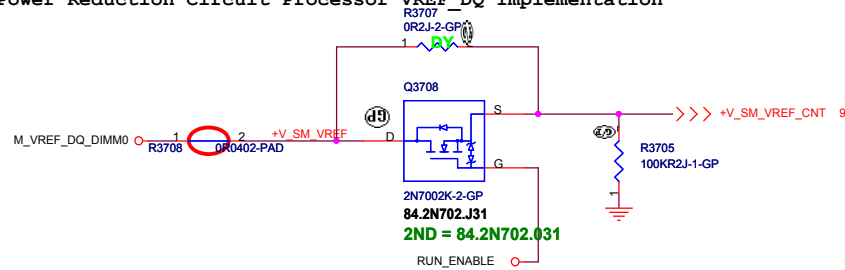
Rev
A00

Date: Wednesday, April 13, 2011

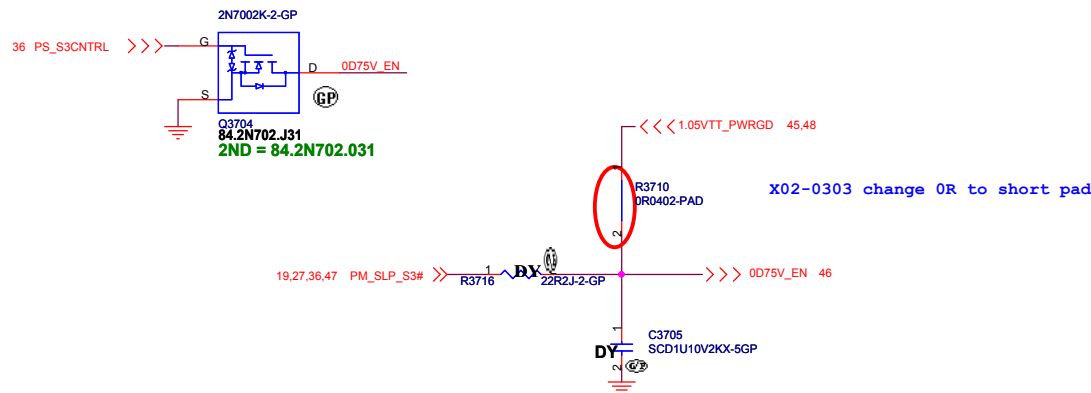
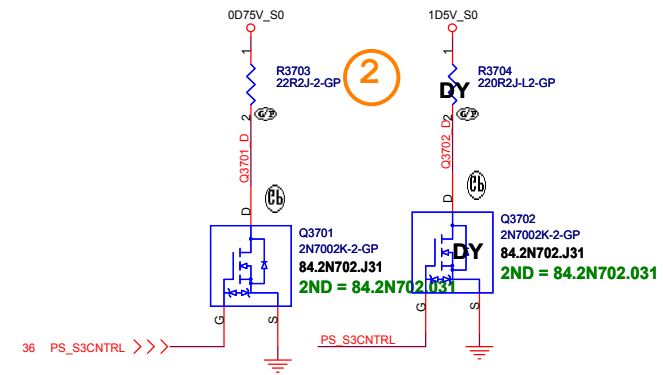
Sheet 35 of 105

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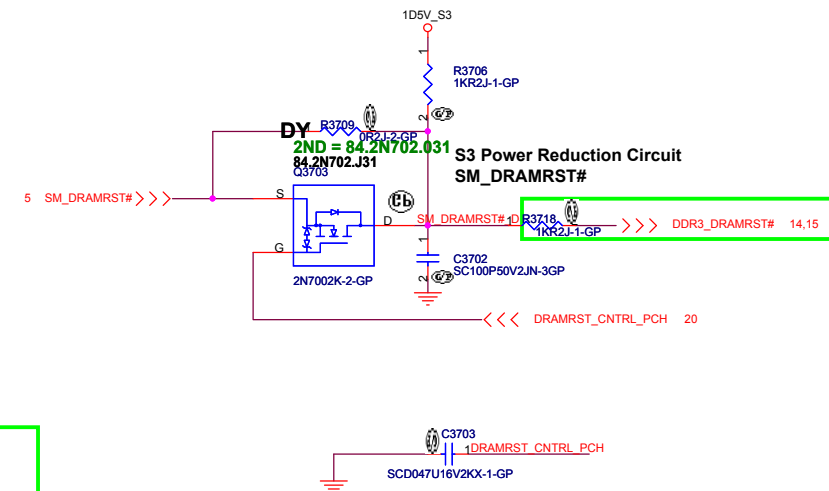
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



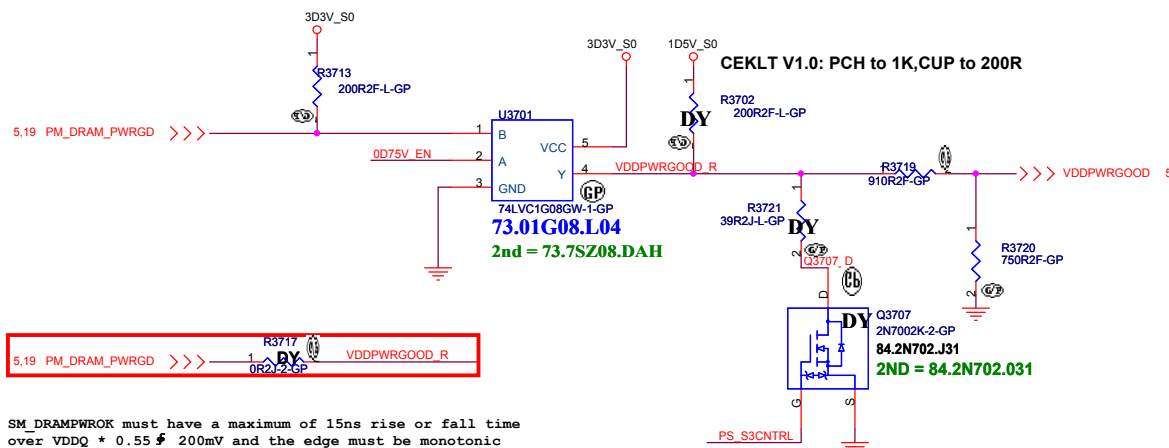
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55 f 200mV and the edge must be monotonic

<Core Design>



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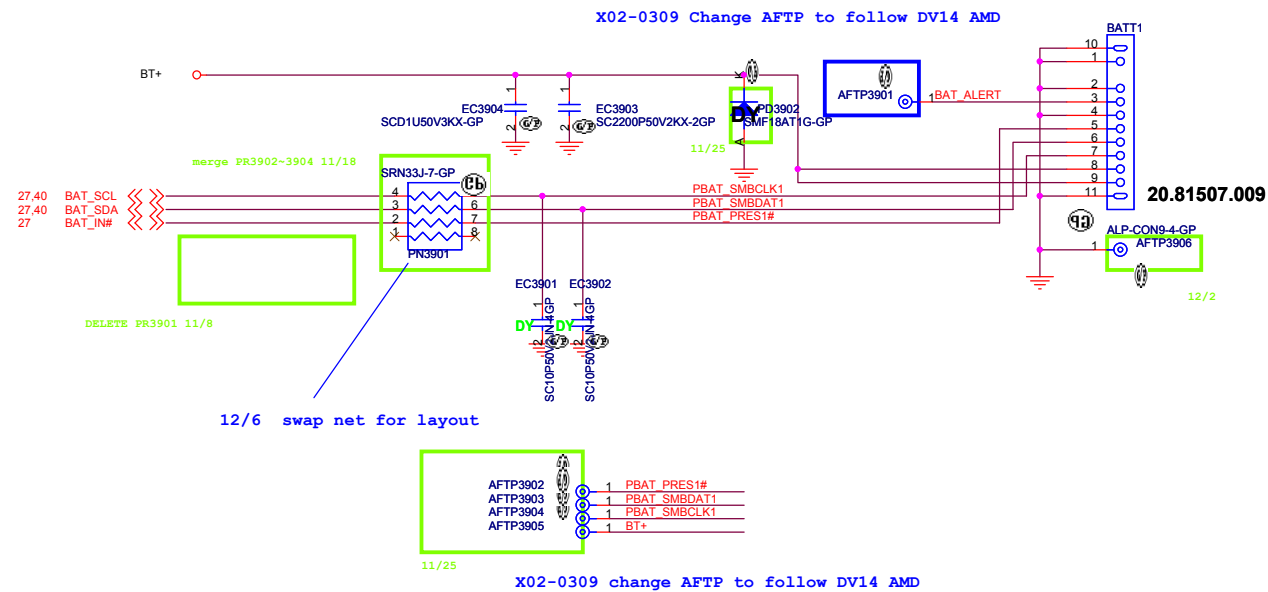
S3 Reduction Circuit		
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DCin CONN



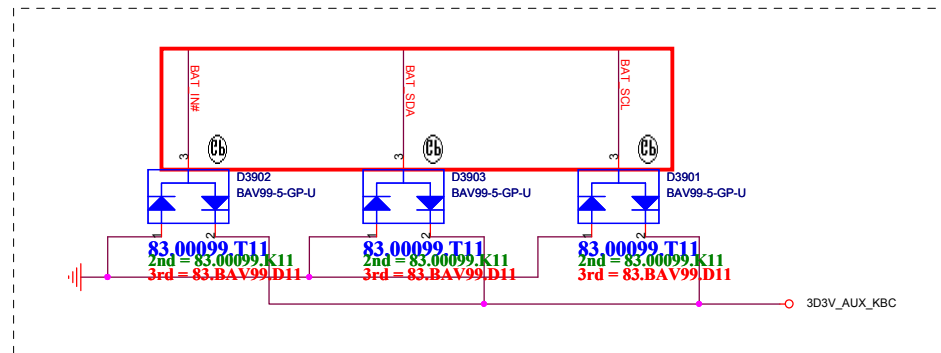
SSID = PWR.Support

Batt Connector



For actual location, need to be swap all pin

Placement: Close to Batt Connector



<Core Design>



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Title		
BATT CONN		
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SSID = Charger

X01-0217 change PU4002, PU4003 to 84.04407.G37

EE need pull high and net name

0802 Rename H_PROCHOT#

27.42 H_PROCHOT#

PWR_CHG_CMPIN

A00-0412 stuff PQ4005

PR4029 54K9R2F-L-GP

A00-0412 Change PR4029 to 54.9K

CHG_AGNND

AD_IA_HW 27

PWR_CHG_CMPIN

PR4027 19K6R2F-GP

A00-0412 Change PR4027 to 19.6K

CHG_AGNND

AD_IA_HW2 27

CHG_AGNND

CHG_AGNND

CHG_AGNND

CHG_AGNND

CHG_AGNND

CHG_AGNND

CHG_AGNND

ROSA

Adapter Type	PR4023
65W	24K
90W	33.2K
130W	59K

EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

PR4034 can dummy if you use external 10mW

X01-0127 DY PQ4007, PR4038, PR4039 for new version BQ24707

Charger Current=1.4~3.6A

X01-0217 change PU4001, PU4004 to 84.04496.037

Add net name 11/10

<Core Design>

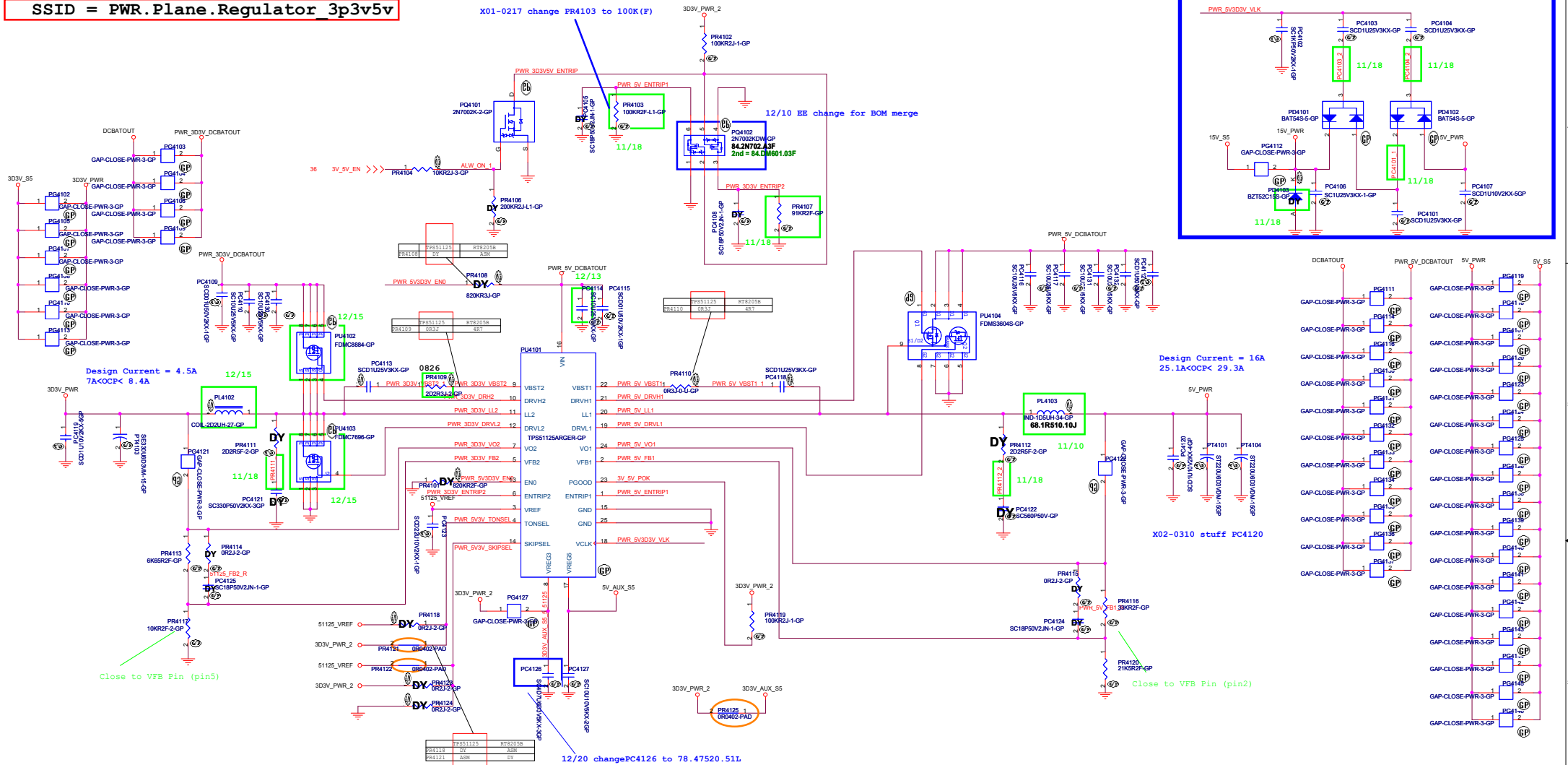
DELL Wistron Corporation
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Title **CHARGER BQ24707**

Size Document Number
Custom **Enrico Caruso 14**

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SSID = PWR.Plane.Regulator 3p3v5v



I/P cap: 10U 25V KU805 X5R/ 78.10622.51L
Inductor: 2.2U PFCM063T-3R22M Cyntec 18mohm/20mohm Isat =10Arms 68.2R210.20B
O/P cap: 330U6.3V M6.35V 15mOhm 3.16Arms Matsuki/77.53371.04L
H/S: SI8412DN / 24mohm/30mOhm/4.5Vgs/ 84.00412.037
L/S: SI7176ADN / 13.5mohm/16.5mOhm/4.5Vgs/ 84.07716.037

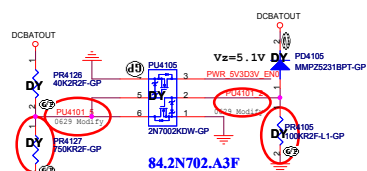
SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820k to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

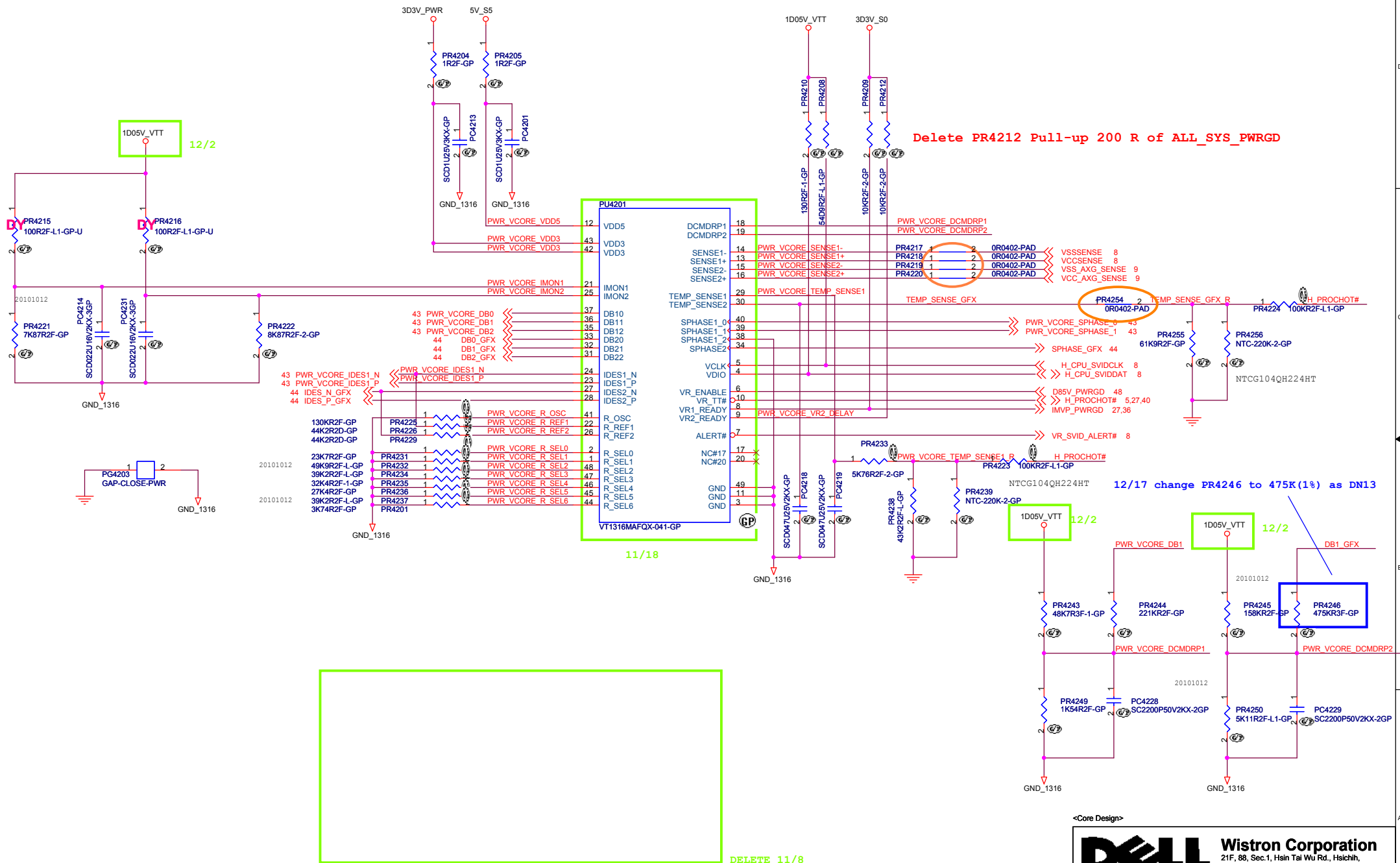
TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

I/P cap:10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.50UH PCMC104T-1R5 Cynet 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 220U 6.3V PSLV0J227M 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S, L/S: FDM33604S / 7.5mohm/9.8mOhm@4.5Vgs, 2.6mohm/3.2mOhm@4.5Vgs/ 84.03604.037



SSID = CPU.Regulator



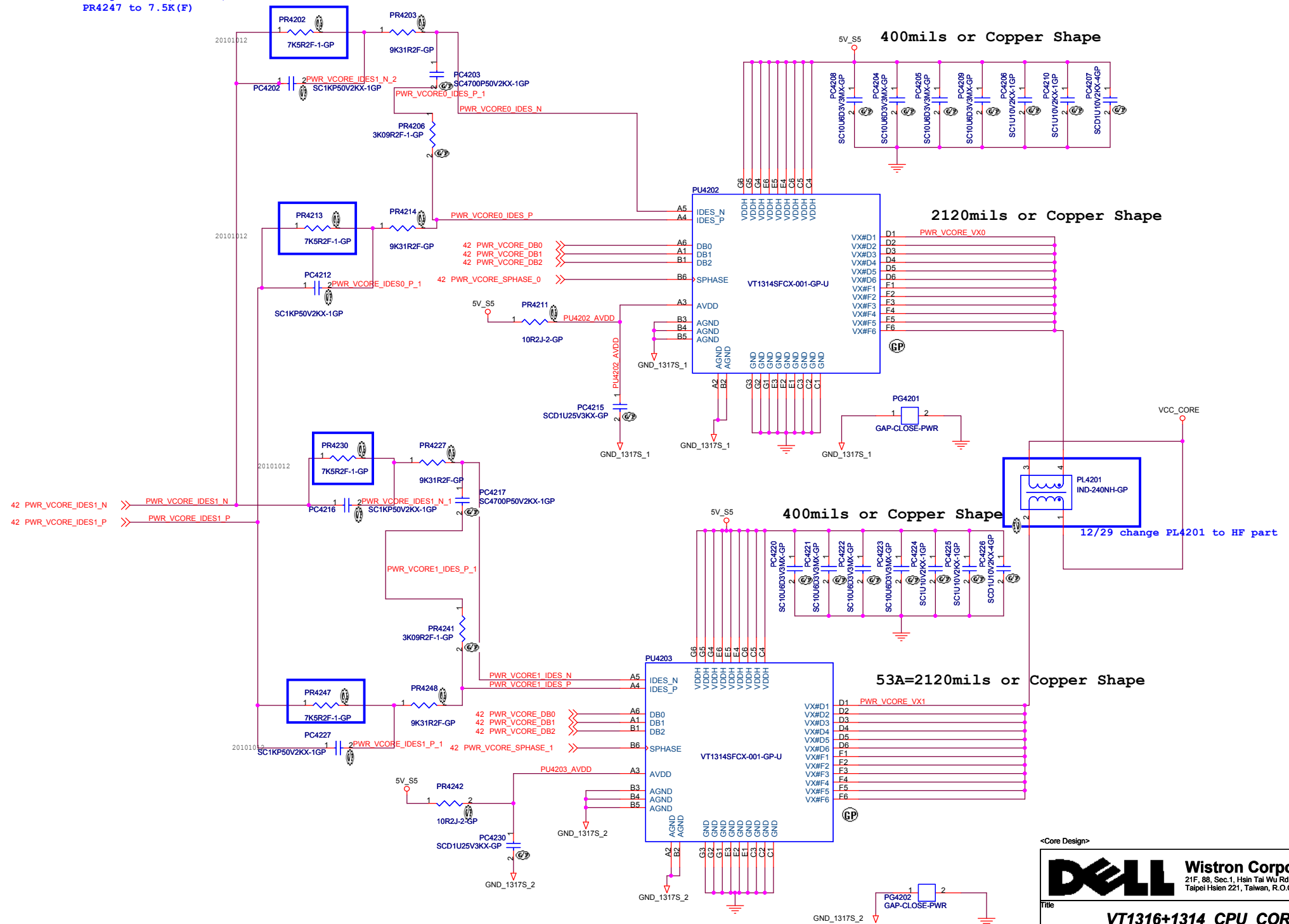
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Title			VT1316+1314 CPU CORE(1/3)	
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X01-0217 change PR4202, PR4213, PR4230
PR4247 to 7.5K(F)



<Core Design>



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Title

VT1316+1314 CPU CORE(2/3)

Size

Document Number	
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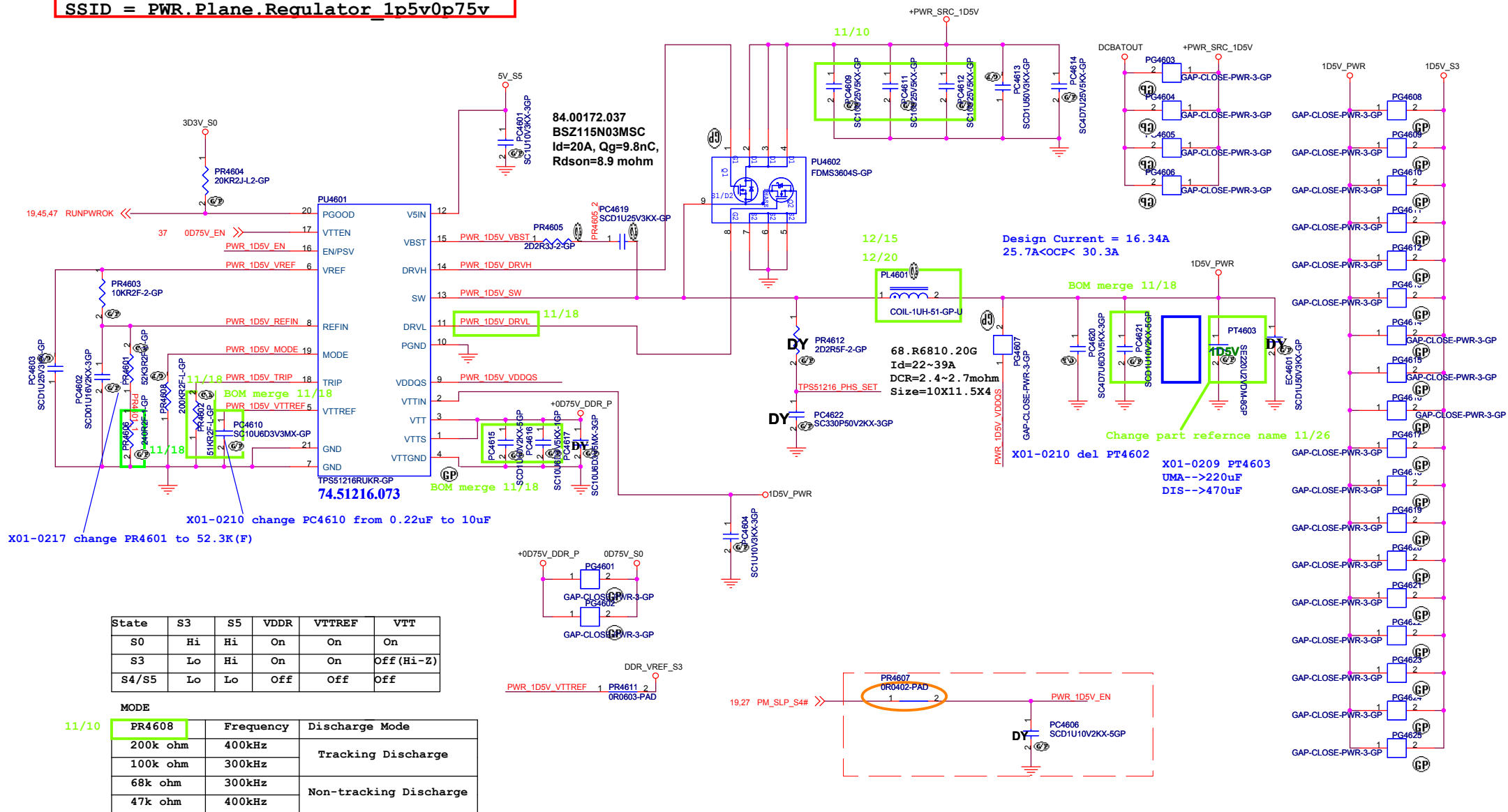
	V
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100
5

SSID = PWR.Plane.Regulator 1p5v0p75v

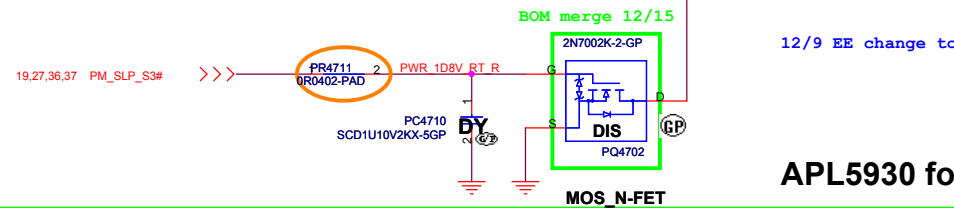
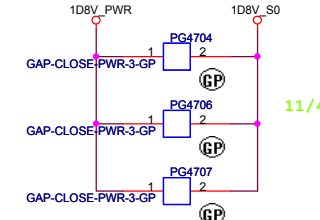
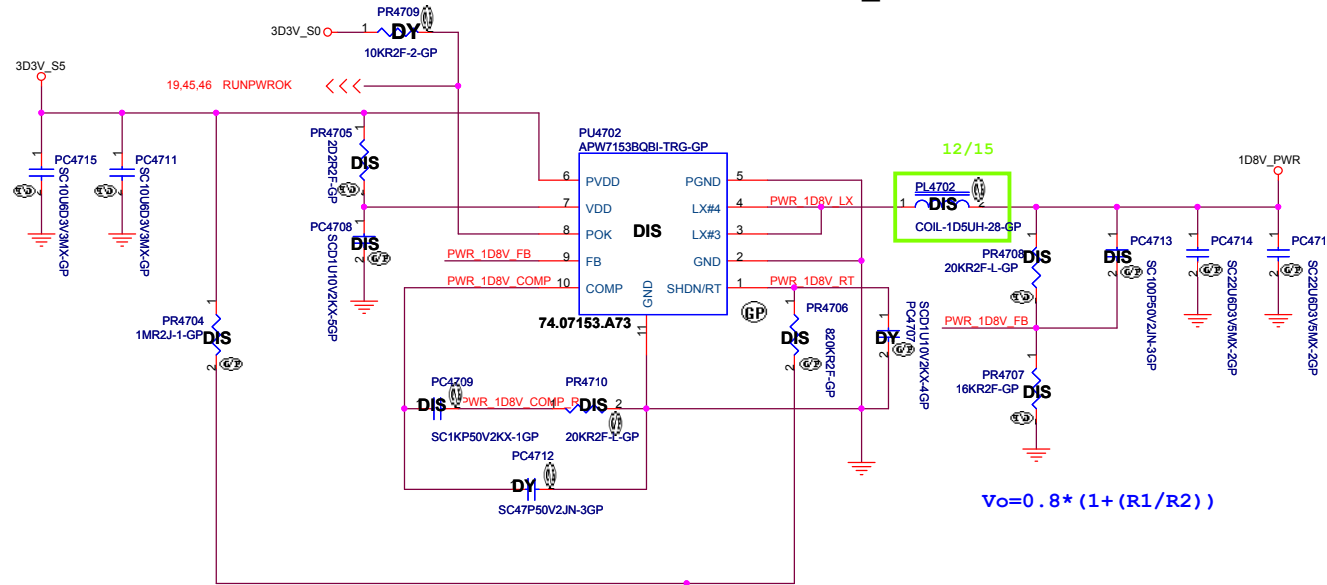


I/P cap:10U 25V K0805 X5R/ 78.10622.51L
Inductor: 0.68UH PCCM104T-R68MN Cyntec 2.4mohm/2.7mohm Isat =39Arms 68.R6810.20G
O/P cap: 220U2V EEFCX0D221R 15mOhm 2.7Arm/ Panasonic / 79.22719.20L
H/S,L/S: FDM33604S / 7.5mohm/ 9.8mOhm@4.5Vgs, 2.6mohm/3.2mOhm@4.5Vgs/ 84.03604.037

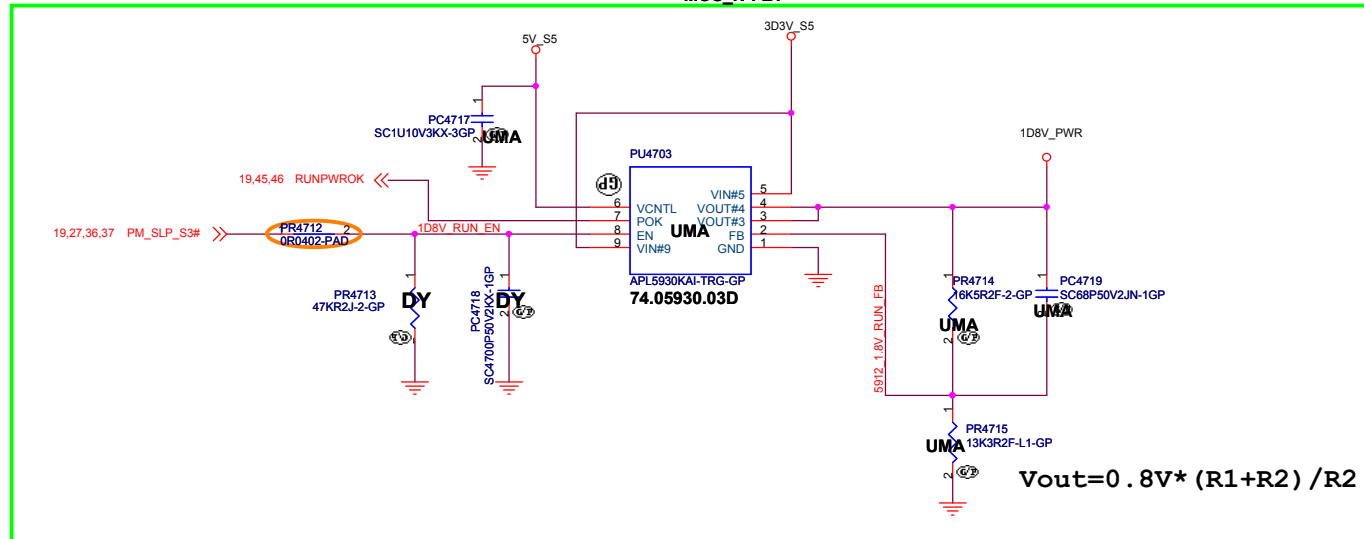
SSID = PWR.Plane.Regulator_1p8v

APW7153B for 1D8V_S0 DIS

+1.8V_RUN
Design current = 1.015A



APL5930 for 1D8V_S0 UMA

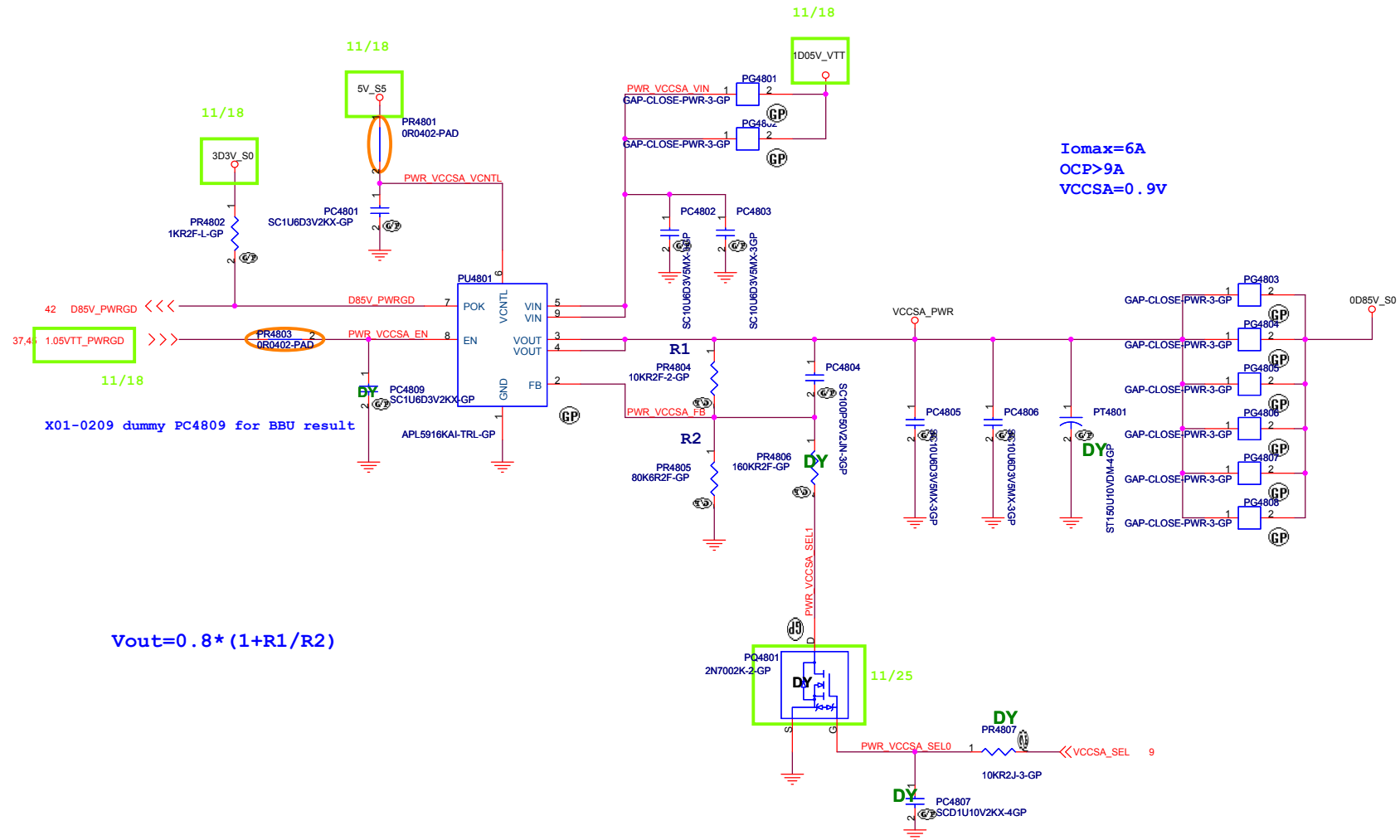


I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L
O/P cap: 22U 25V M0805 X5R/ 78.22610.51L
Inductor: 1.5U PCMC063T Cyntec 14mohm/15mohm Isat =18Arms 68.1R510.10K

<Core Design>

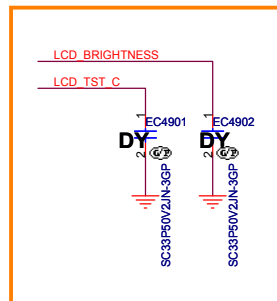
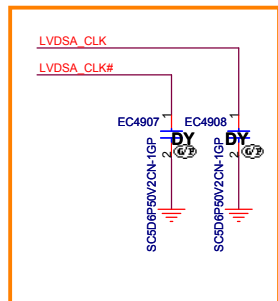
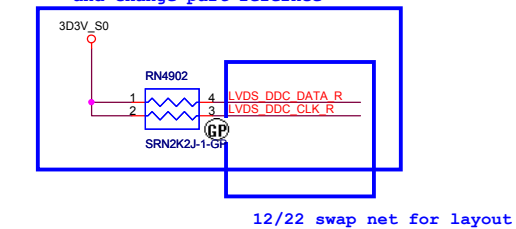
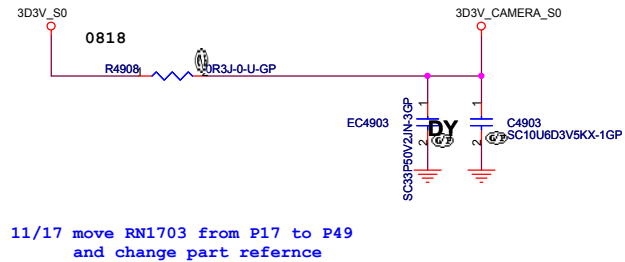
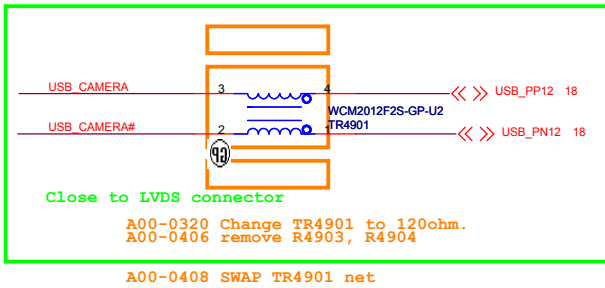
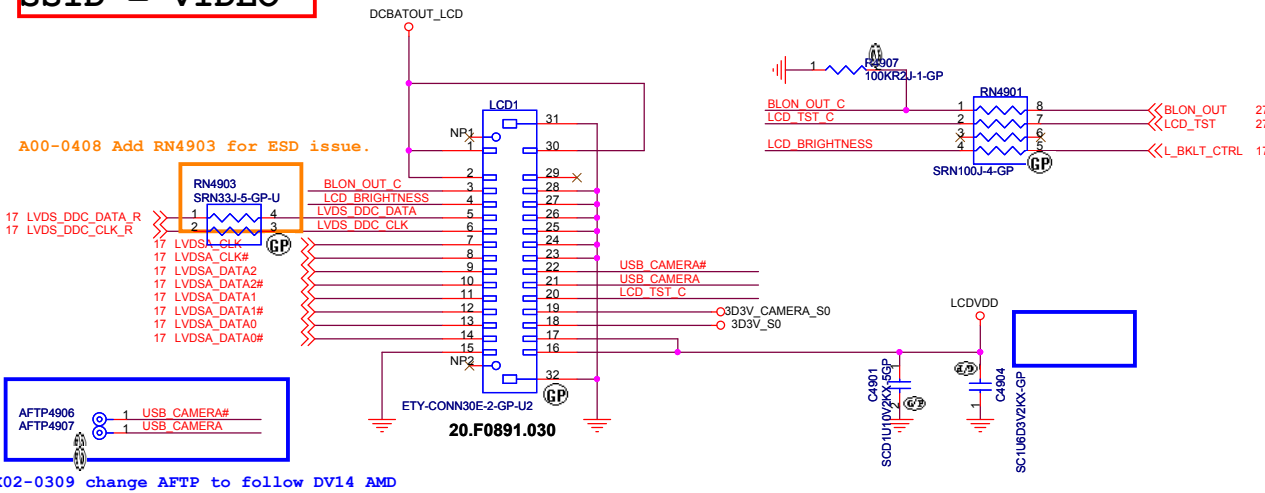
DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
APW7153B +1.8V_RUN			
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APL5916 for VCCSA


$$V_{out} = 0.8 * (1 + R1/R2)$$

I_{omax}=6A
OCP>9A
VCCSA=0.9V

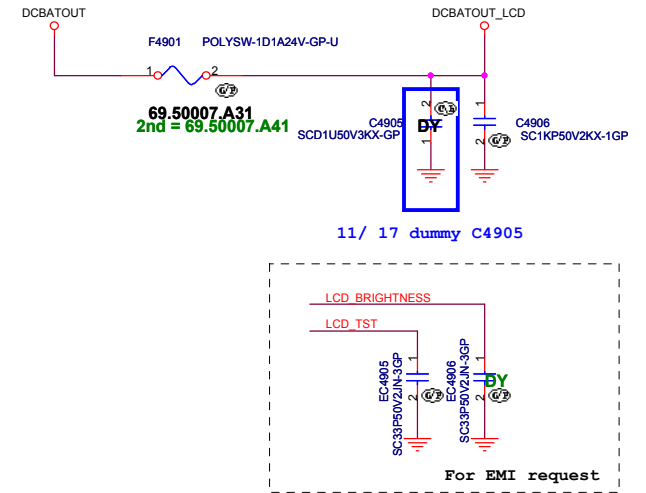
SSID = VIDEO



For EMI request

SSID = Inverter

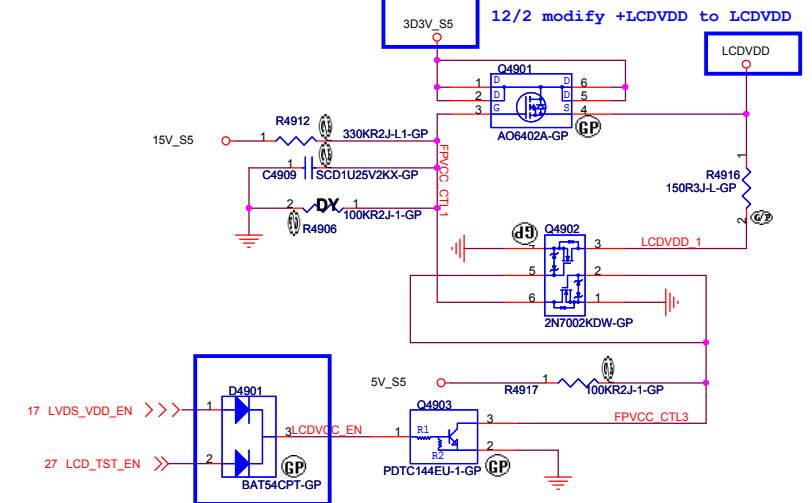
INVERTER POWER



SSID = VIDEO

LCD POWER

```
11/15 change LCDVDD source from S0 to S5
```



12/9 BOM merge

<Core Design>



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LCD Connector

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A2

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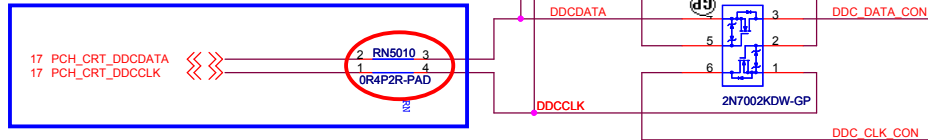
Date: Wednesday, April 13, 2011

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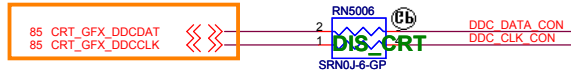
SSID = VIDEO

11/3 Add RN5010 for CRT SMBus
X02-0303 change 0R to short pad

11/ 17 Add RN5012 for SMBus pull high
X01: change RN5012 from 0R to 2.2K

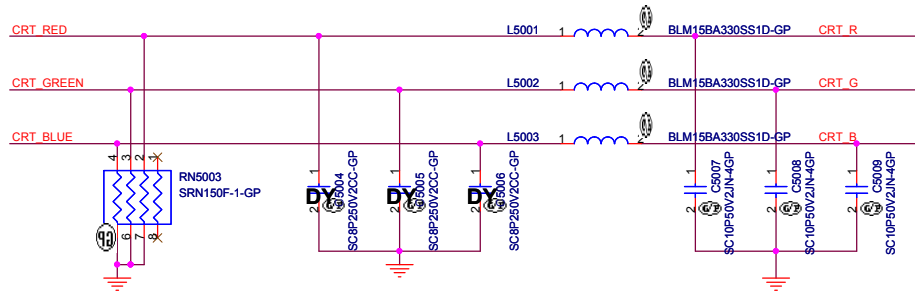


5V Tolerance

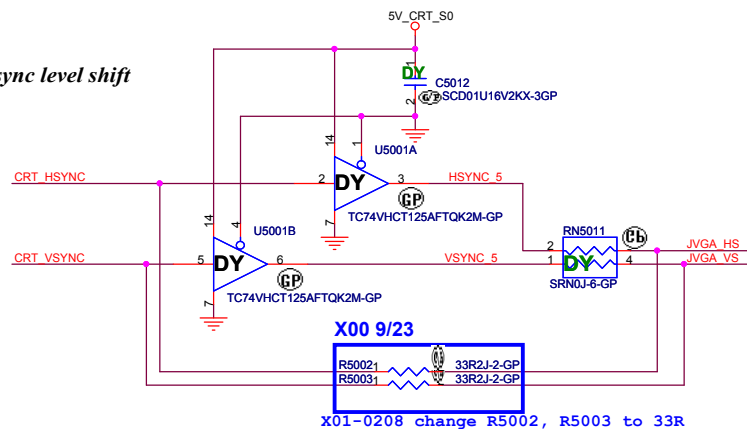


Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

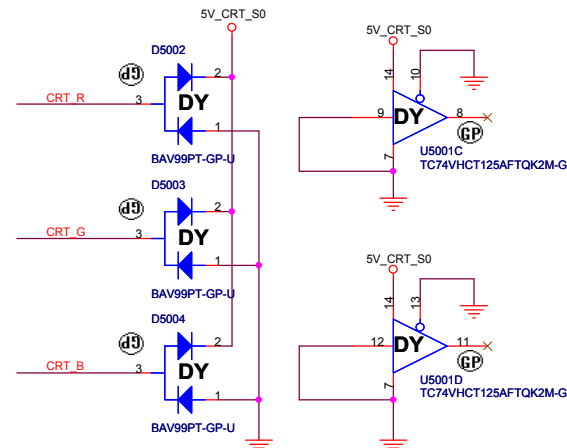


Hsync & Vsync level shift

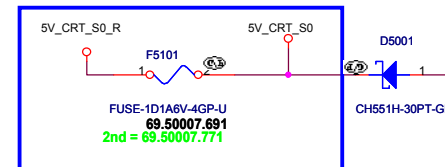


X00 9/23

X01-0208 change R5002, R5003 to 33R



11/18 change Fuse for CRT and HDMI share

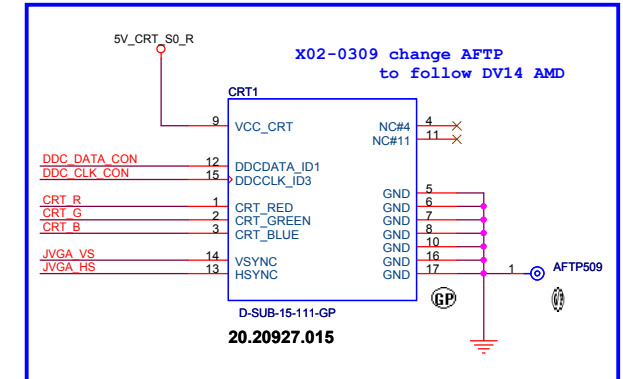


11/15 remove F5501 base on brazos result.
11/ 17 Remove R5001



AFTP501	1	5V CRT_S0
AFTP502	1	DDC_DATA_CON
AFTP503	1	DDC_CLK_CON
AFTP504	1	CRT_R
AFTP505	1	CRT_G
AFTP506	1	CRT_B
AFTP507	1	JVGA_HS
AFTP508	1	JVGA_VS

11/29 change CRT1 to 20.20927.015



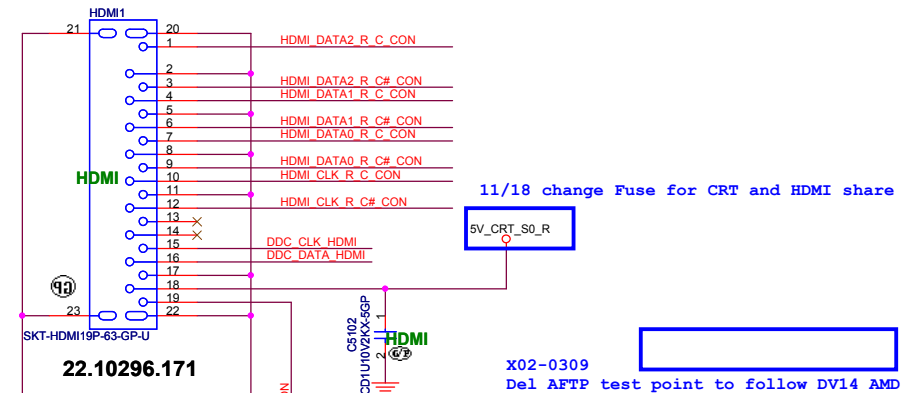
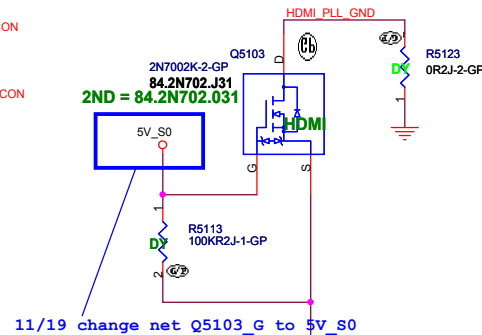
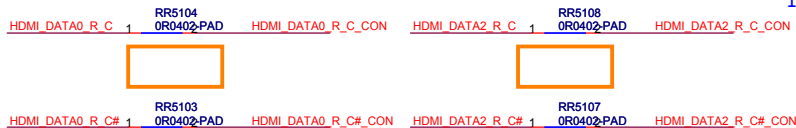
SSID = VIDEO

HDMI Level Shifter & CONNECTOR

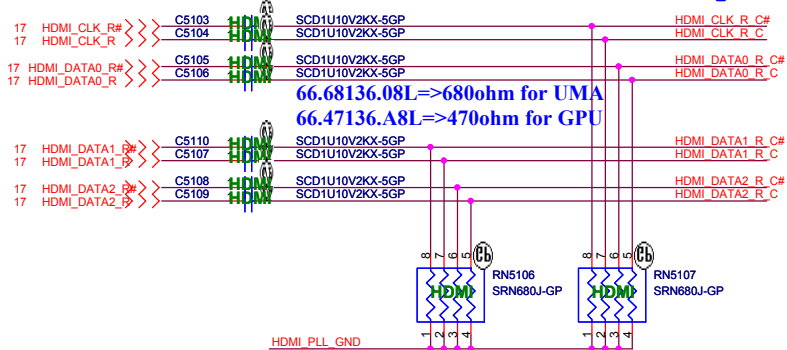
HDMI CONN



A00-0407 remove TR5101, TR5102, TR5103, TR5104 PAD and remove 0R PAD.



HDMI DISCRETE/ UMA Co-lay



11/18 change RN5117 BOM control property to HDMI

17_PCH_HDMI_CLK >>> RN5117 3

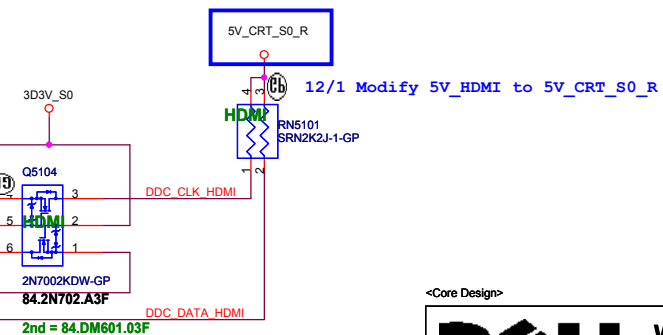
17_PCH_HDMI_DATA >>> 0R4P2R-PAD

X02-0303 change 0R to short pad

11/16 Del RN5112~5115 for no need to reserve for VGA

Routing Guidelines:

CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.



<Core Design>

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Reserved

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LVDS_Switch

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SSID = User.Interface

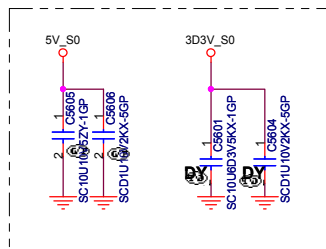
(Blanking)

SSID = SATA

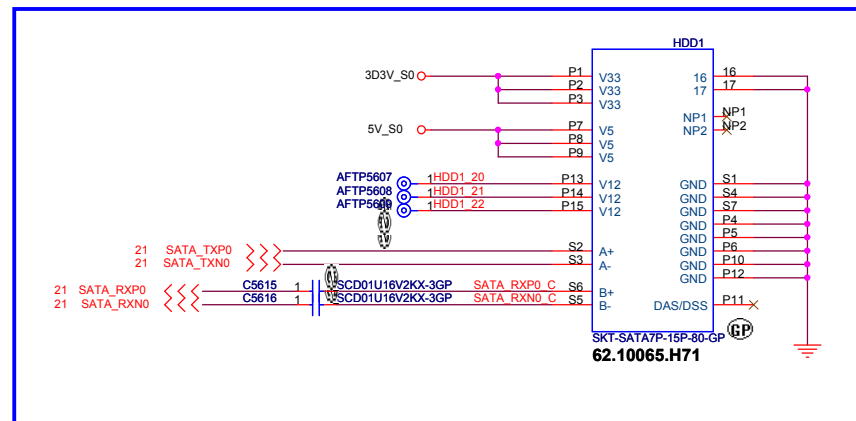
SATA HDD Connector

11/10 Change HDD1 CONN to 62.10065.031

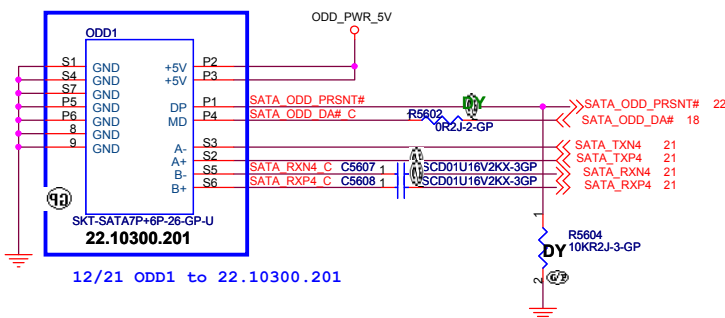
12/22 Change HDD1 CONN to 62.10065.H71



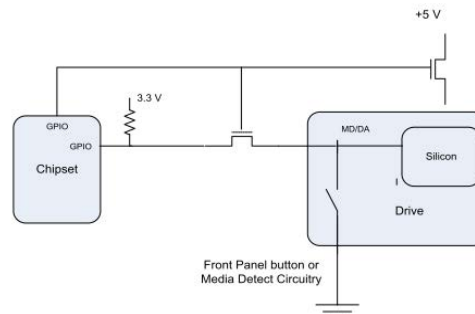
Close to HDD1



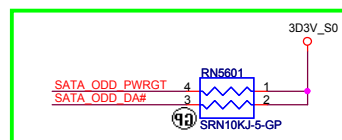
ODD Connector



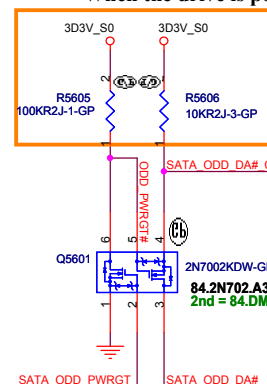
12/21 ODD1 to 22.10300.201



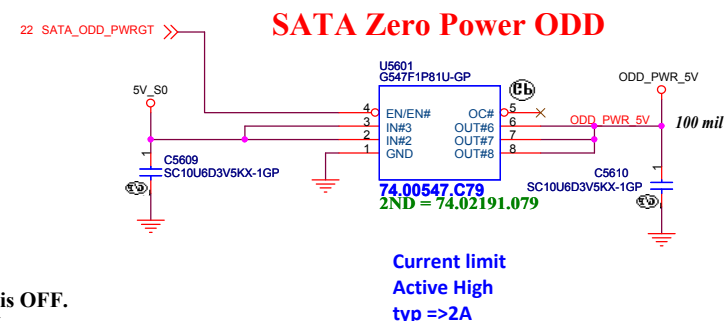
When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



SUPPORT ZERO SATA ODD



A00-0408 Add R5606 to pull high 3.3V_S0
Change pull high to 3.3V_S0



Current limit
Active High
typ => 2A

<Core Design>

SSID = ESATA

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<Core Design>



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Title

ESATA

Size
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Enrico Caruso 14

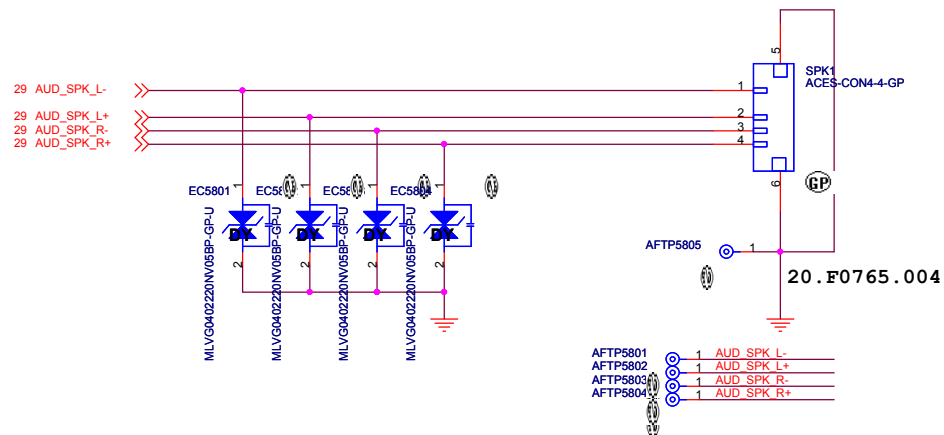
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SSID = AUDIO

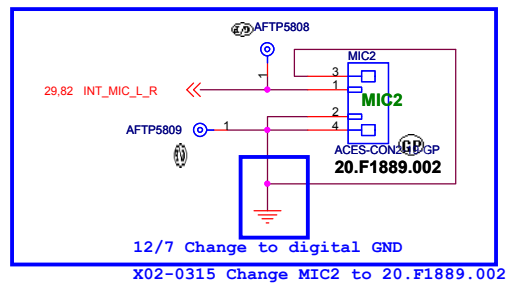
Speaker Connector



11/10 remove MIC1

11/26 reserve MIC2

12/7 change MIC2 to 20.F1050.002



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[illegible]

SPEAKER CONN

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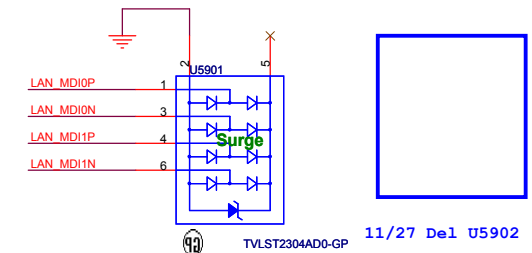
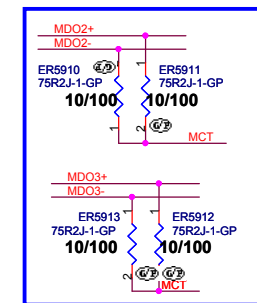
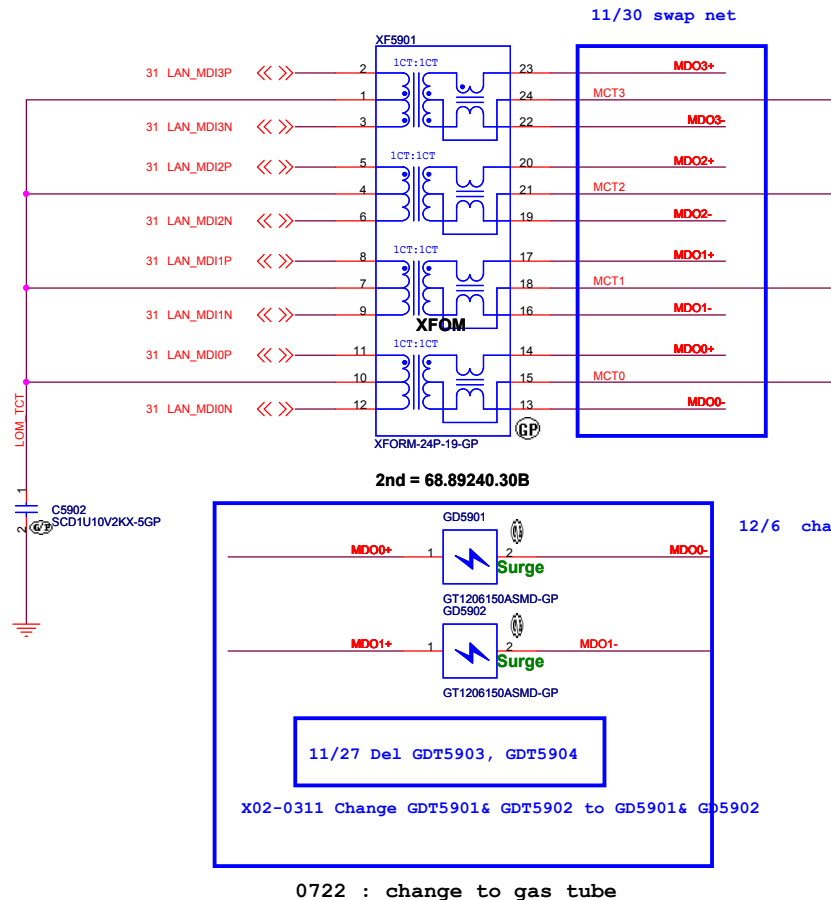
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SSID = LOM

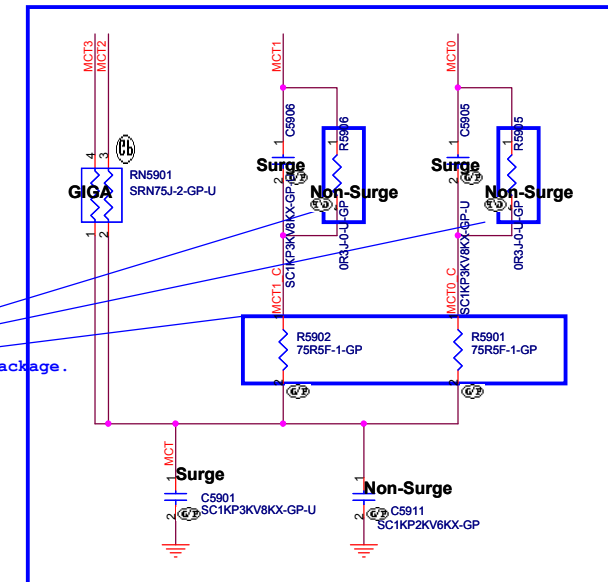
LAN TransFormer

Giga Main: 68.IH601.301
Giga 2nd: 68.05009.30A

10/100 Main: 68.HH035.301
10/100 Main: 68.01284.30A

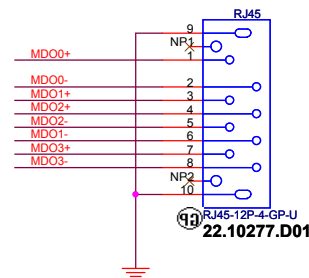


12/6 change resistor package.

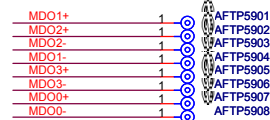


11/25 modify to CRC circuit and divided resistor as EMI suggest
11/29 Change C5911 to 78.1022S.22L

RJ45



11/29 change RJ45 to 22.10277.D01



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SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH

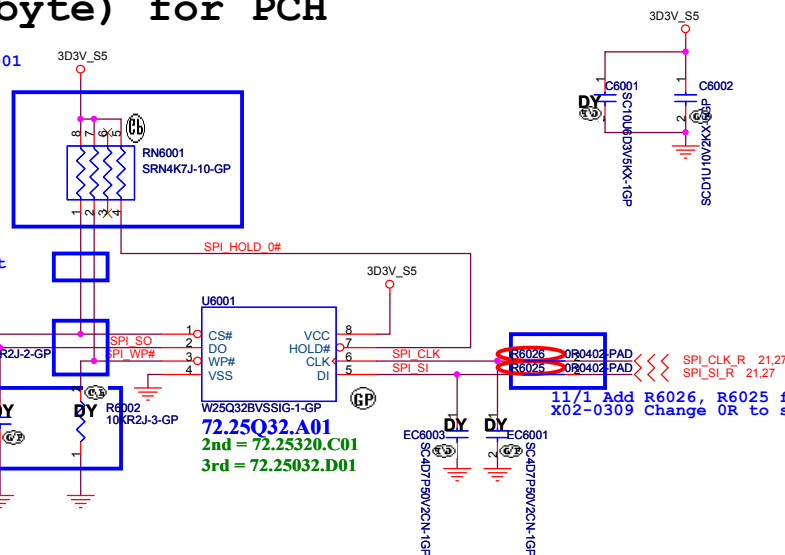
11/18 Merge R6003, R6004, R6005 to RN6001

12/6_swap net for layout
X01-0211 swap CS#, WP# for layout

X01: modify CS#, WP#

21.27 SPI_CS0#_R
21.27 SPI_SO_R

11/18 reserve R6002 for WP# and change
change DO pin pull down to capacity

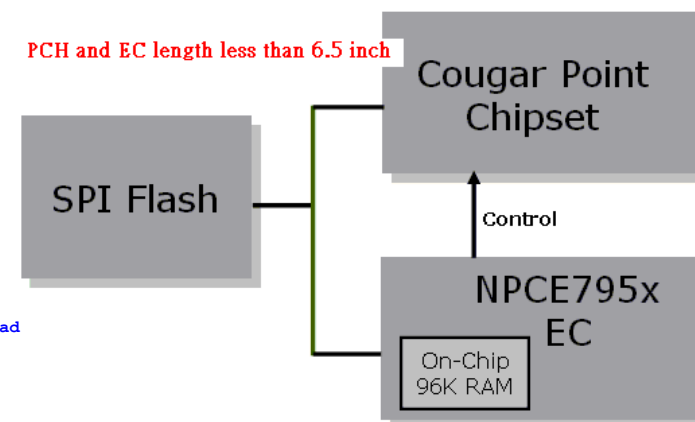


Priority	Wistron P/N	Manufacturer	Vendor P/N
1	72.25Q32.A01	WINBOND	W25Q32BVSSIG
2	72.25320.C01	MXIC	MX25L3206EM2I-12G
3	72.25032.D01	SST	SST25VF032B-80-4I-S2AF
4	72.25P32.C01	Numonyx	M25PX32-VMW6F

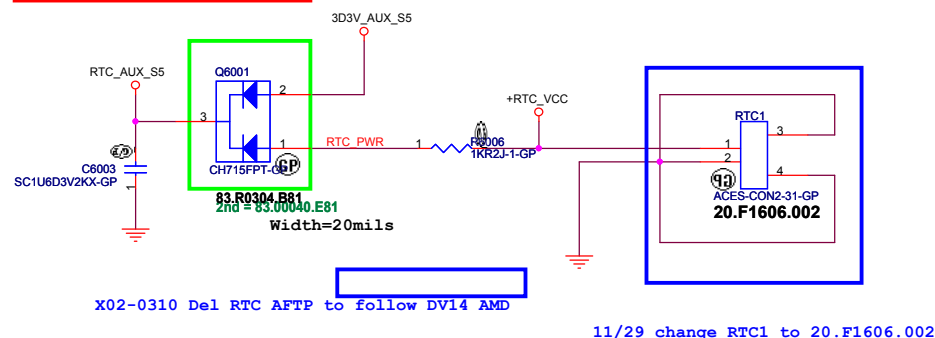
Notes:

The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

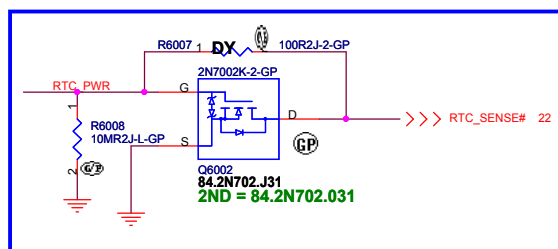
PCH and EC length less than 6.5 inch



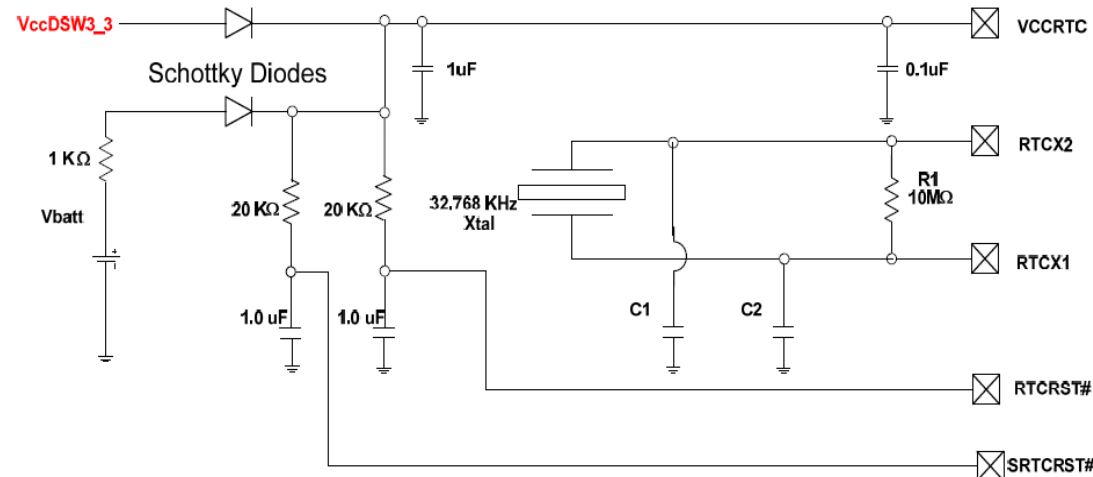
SSID = RBATT



11/29 change RTC1 to 20.F1606.002



11/23 add RTC DET circuit



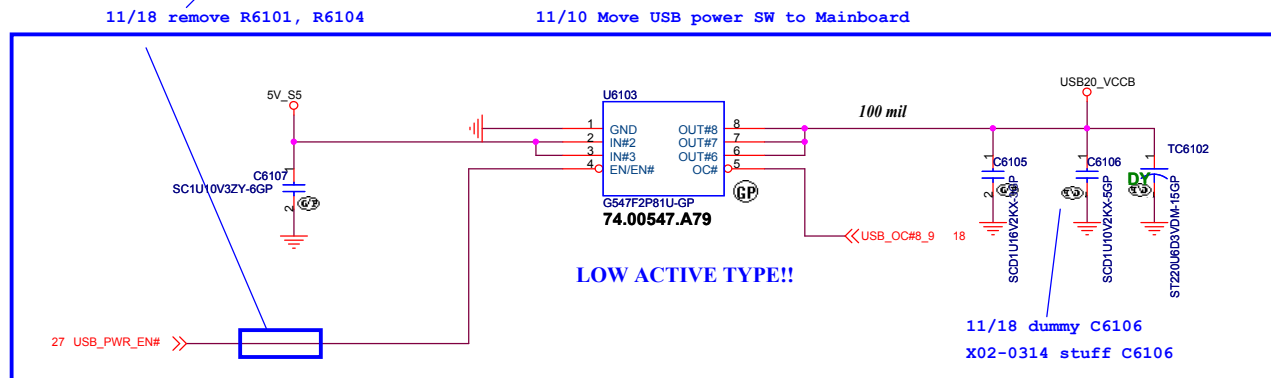
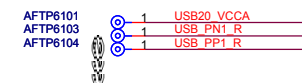
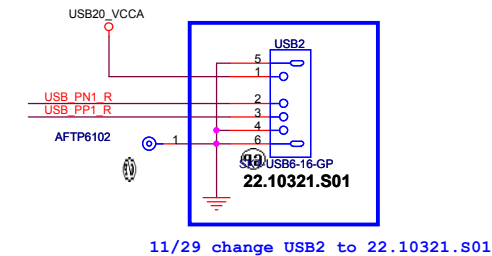
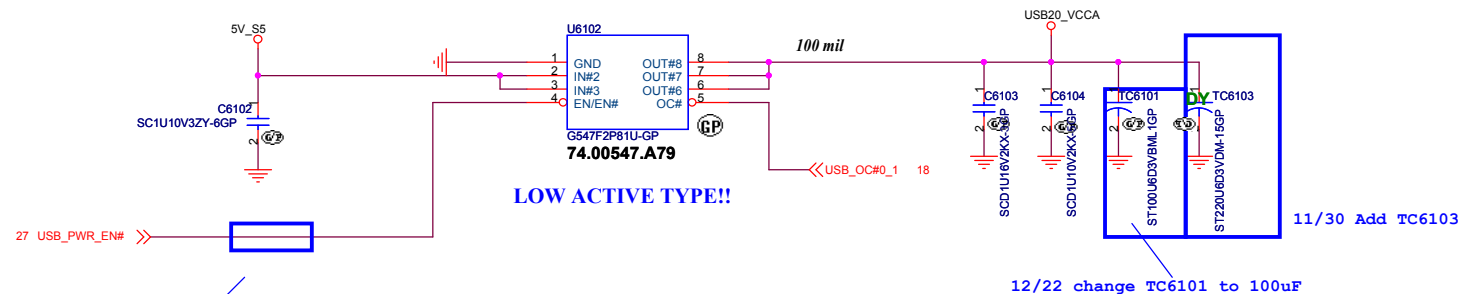
VccRTC is now connected to VccDSW3_3 through the Schottky diode instead of the 3.3V Sus well.

<Core Design>

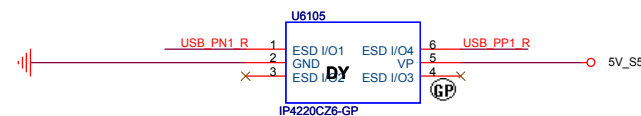
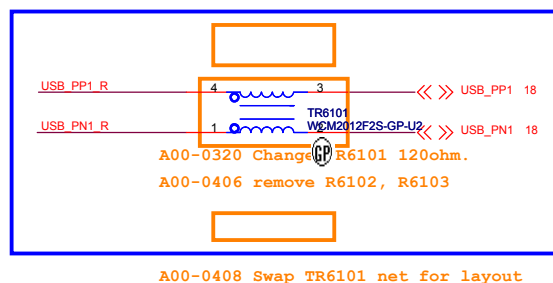
DELL Wistron Corporation
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SSID = USB



11/1 Stuff TR6101 for EMI



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DELL		Wistron Corporation	
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Title			
USB Power SW			
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SSID = User.Interface

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<Core Design>



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Title

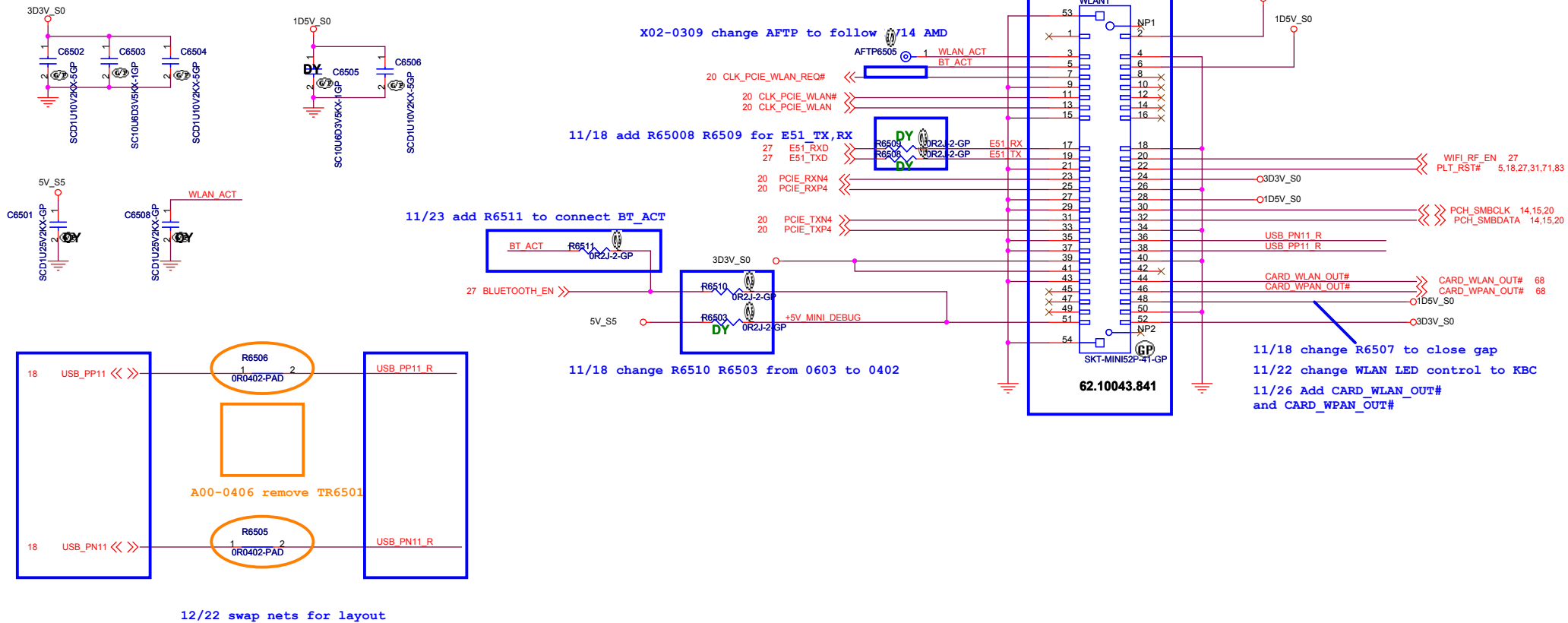
RESERVED

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SSID = Wireless

Mini Card Connector(802.11a/b/g)



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Title

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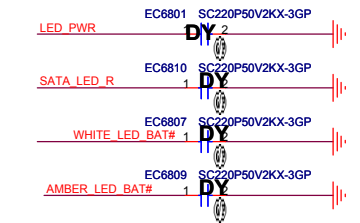
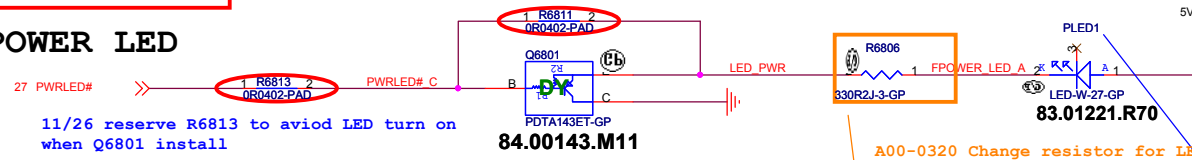
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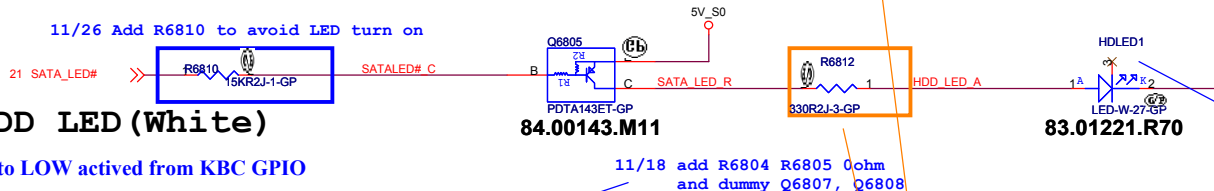
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Reserved

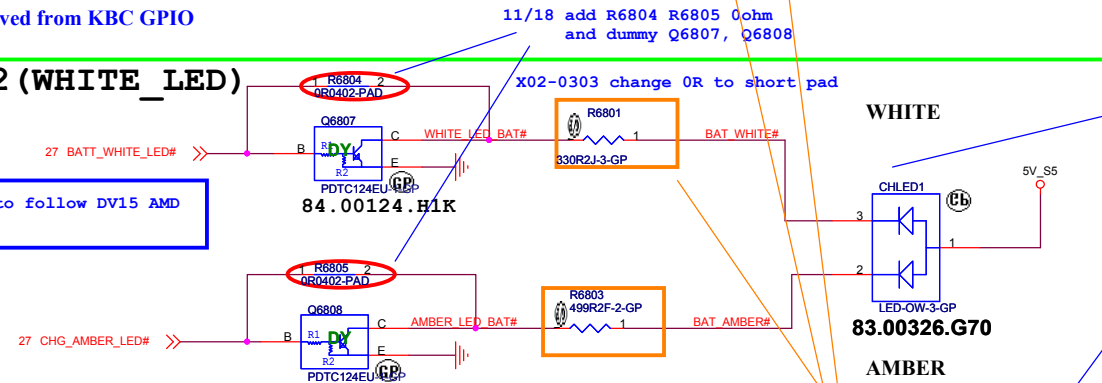
FRONT POWER LED



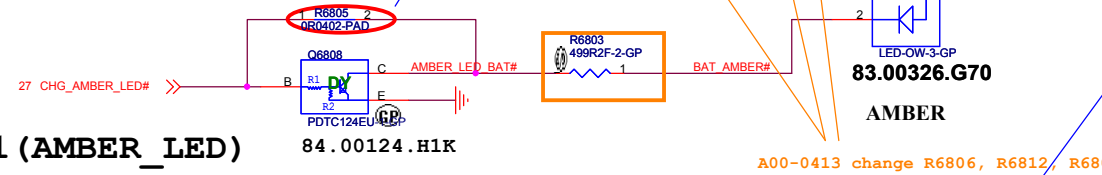
SATA HDD LED (White)



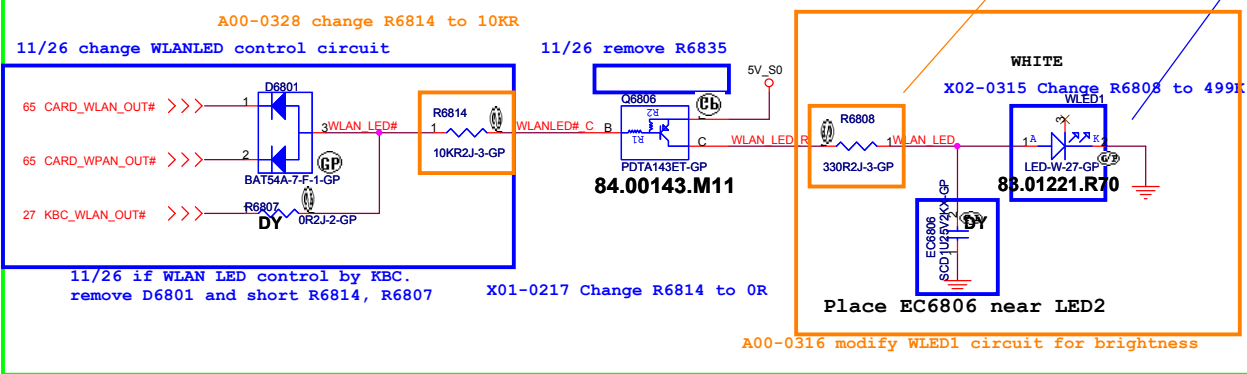
Battery LED2 (WHITE_LED)



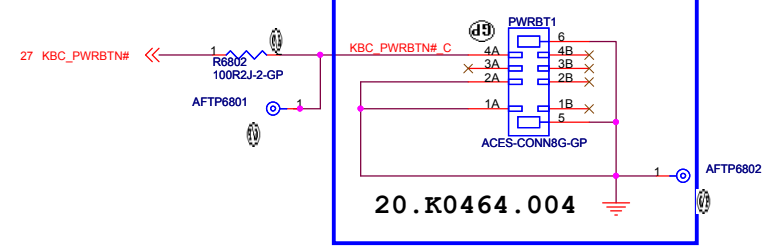
Battery LED1 (AMBER_LED)



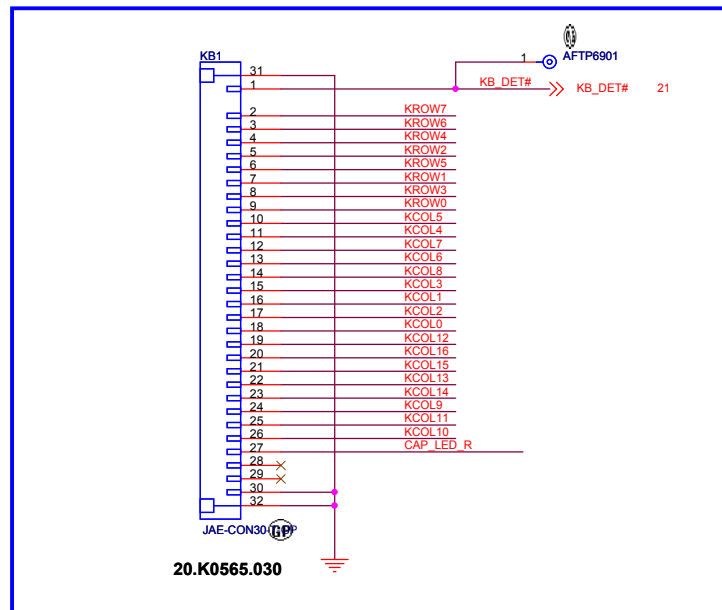
Wireless LED



Power button



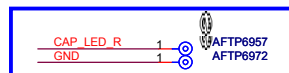
SSID = KBC



11/26 change KB1 to 20.K0597.030

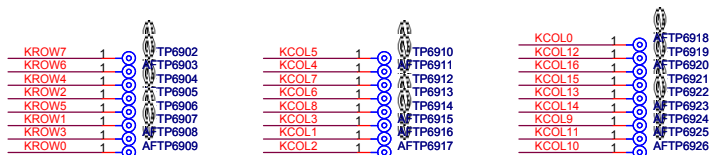
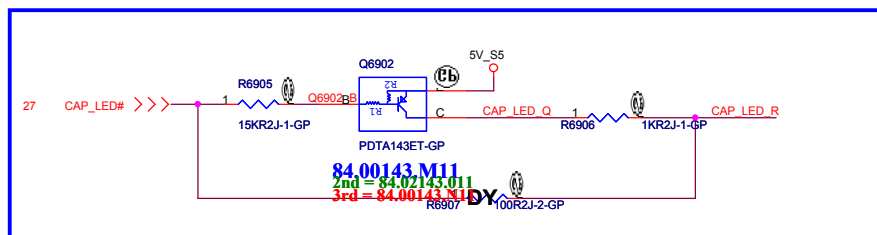
12/8 Change KB1 to 20.K0565.030

X02-0309 change AFTP to follow DV14 AMD



12/8 Add Cap LED control circuit

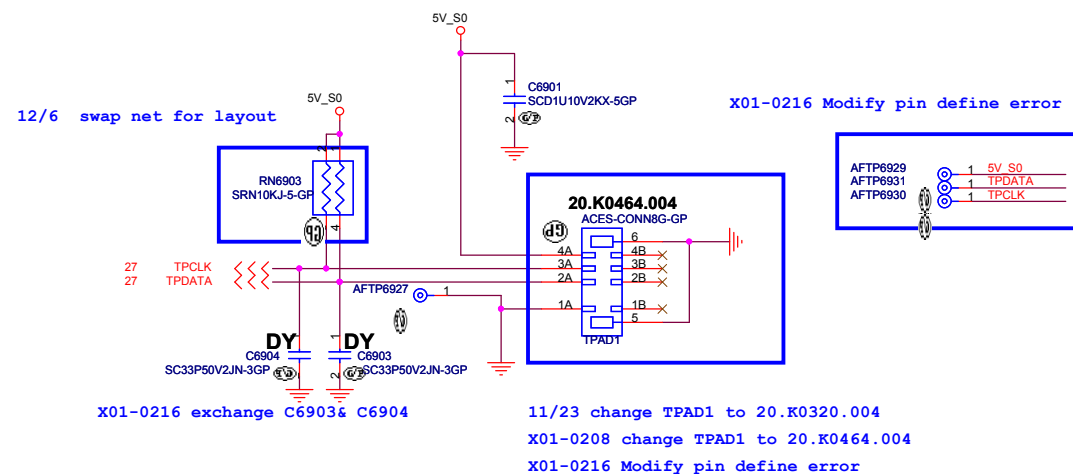
CAP LED CONTROL



SSID = Touch.Pad

X01-0216 Modify pin define error

TouchPad Connector



<Core Design>



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Title		
Key Board/Touch Pad		
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Title

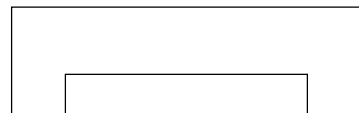
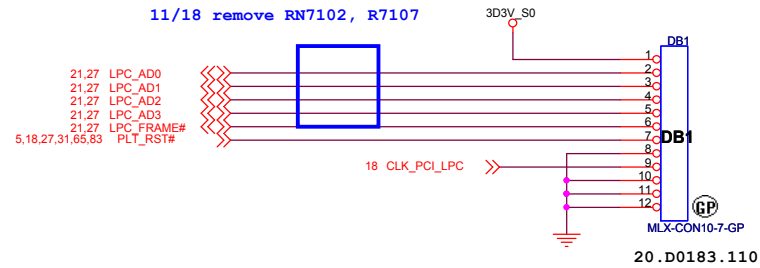
Hall Sensor

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Debug connector			
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DN15ATI Whistler



Wistron Corporation
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DN15ATI Whistler



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Title

Size
A3

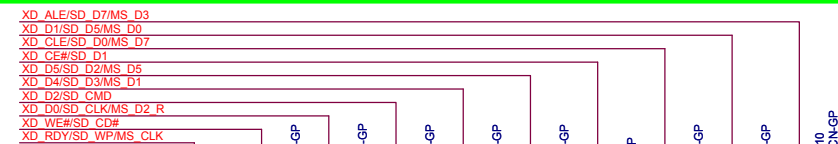
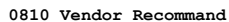
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Reserved

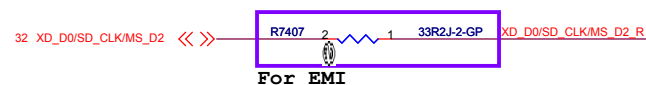


For EM

11/18 Dummy EC7401, EC7403

11/20 vendor recommand to reserve 5P

X01-0216 stuff EC7401~EC7410 for EMI



For EMI

<Core Design>



Wistron Corporation
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Title

SD/XD/MS/MMC Card CONN

Size

Document Number

Rev

Enrico Caruso 14

A00

Date: Wednesday, April 13, 2011

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SSID = ExpressCard

<Core Design>



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Title			Express Card		
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SSID = User.Interface

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Title

Free Fall Sensor

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Title

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Document Number
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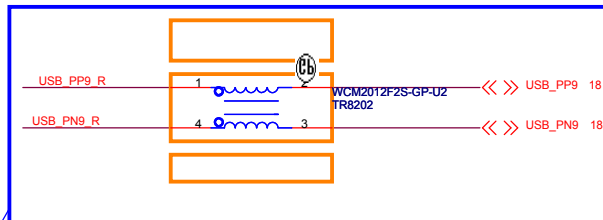
Date: Wednesday, April 13, 2011

Reserved

Rev
A00

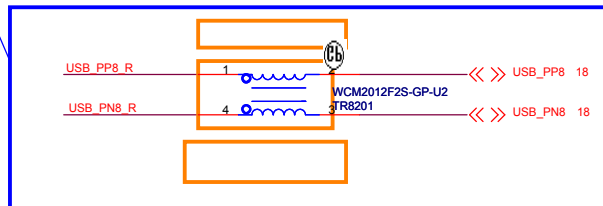
Sheet 81 of 105

11/1 Stuff TR8201, TR8202 for EMI

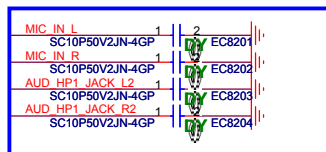


A00-0406 remove R8201, R8202, R8203, R8204 pad
A00-0320 Change TR8201, TR8202 to 120ohm.
A00-0408 Swap net for layout

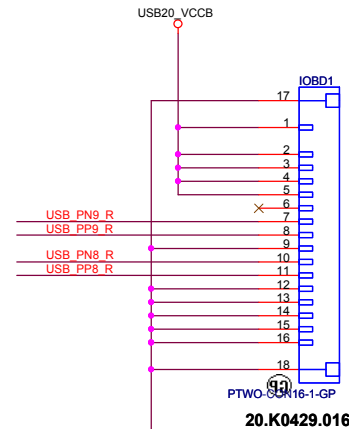
12/6 swap net for layout



11/1 Add EC2901~EC2904 for EMI request



IOBD1 is for USB board

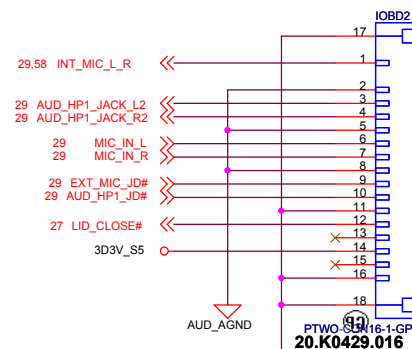


11/10 modify B2B CONN and pin define

X01-0214 add AFTP8201~8210

X02-0309 Del AFTP8201~8210

IOBD2 is for Audio board



X02-0309 Del AFTP8201~8210

12/10 Change pin defien for audio board routing smooth.

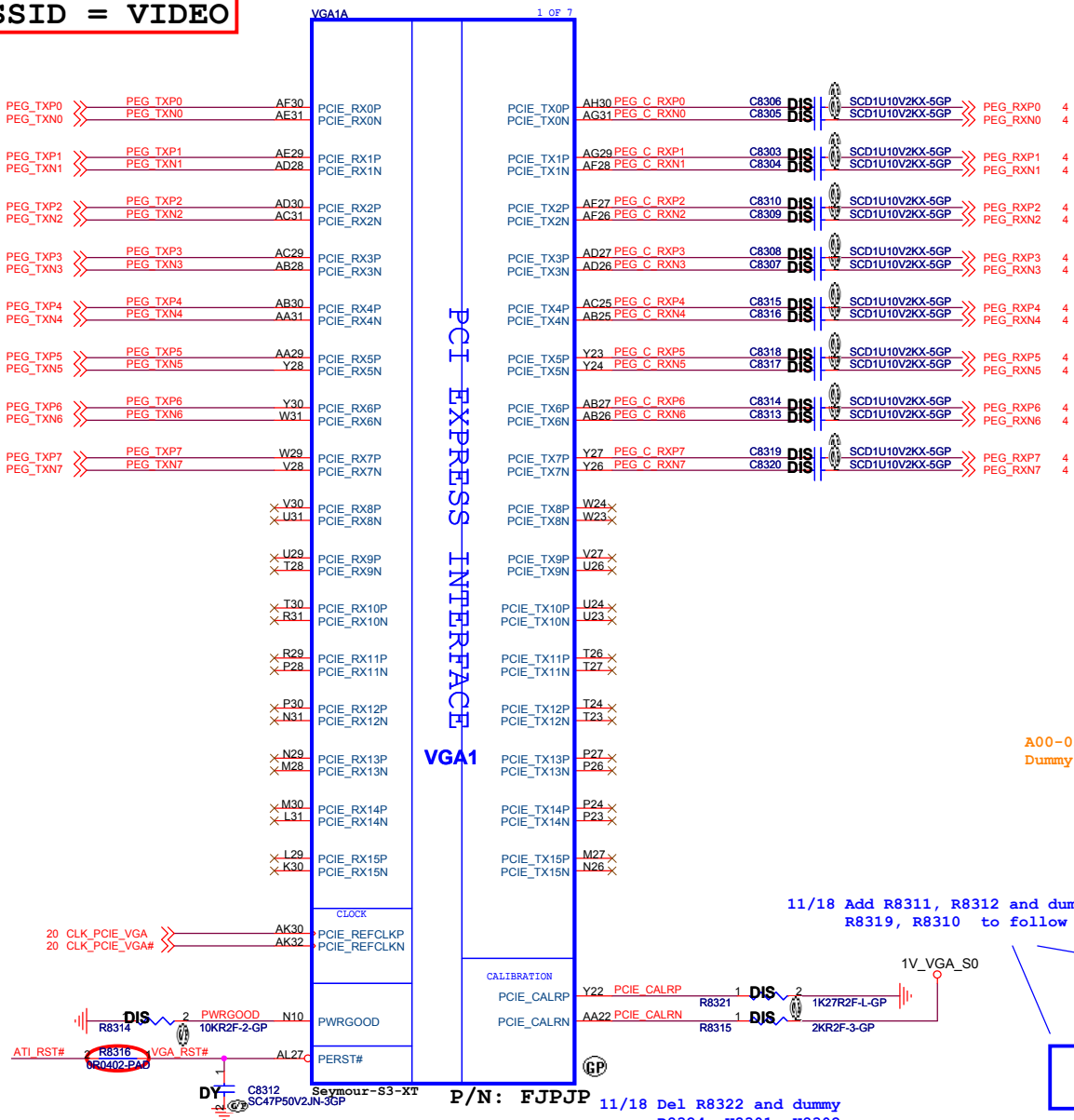
12/14 Change IOBD2 to 20.K0429.016 and change pin define.

<Core Design>

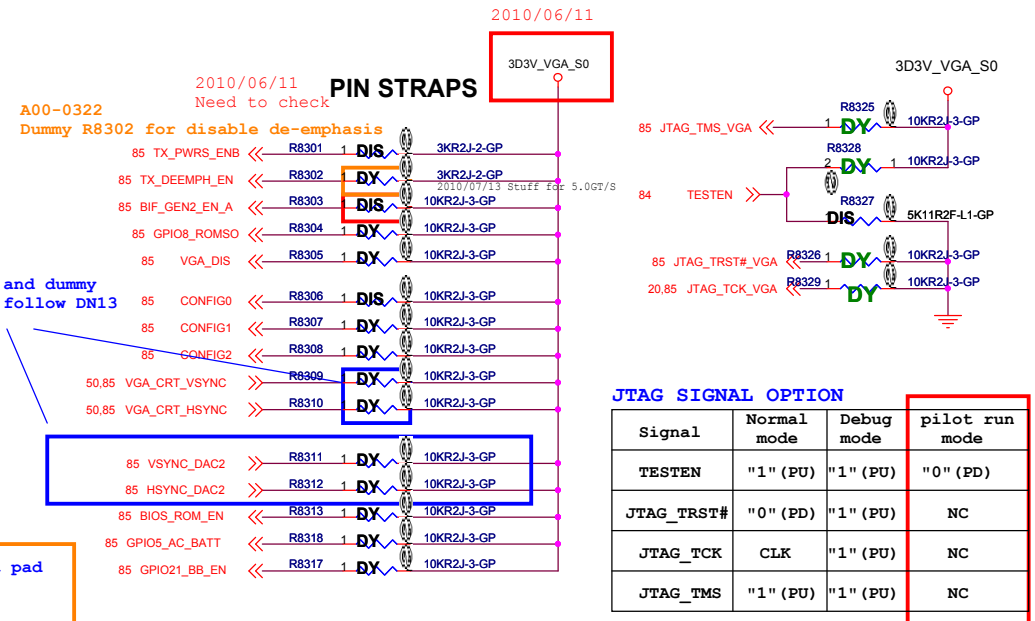
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
IO Board Connector
Size A3 Document Number
Enrico Caruso 14 Rev
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SSID = VIDEO



CONFIGURATION STRAPS				RECOMMENDED SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				0= DO NOT INSTALL RESISTOR 1= INSTALL 3K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE	
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS		RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing		X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled		X	1
BIF_GEN2_EN_A	GPIO2	0: Advertises the PCIe device as 2.5GT/s capable at power on. 1: Advertises the PCIe device as 5.0GT/s capable at power on.		0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.		?	0
GPIO8_ROMSO	GPIO8	RESERVED		0	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device won't be recognized as the system's VGA controller		0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size		X X X	0 0 1 (2.56MB)
GPIO21_BB_EN	GPIO21	RESERVED		0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0: Disable external BIOS ROM device 1: Enable external BIOS ROM device		X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.		X	0
RSVD	H2SYNC	RESERVED		0	0
RSVD	GENERICC	RESERVED		0	0
AUD[1]	HSYNC	AUD[1:0]: 11-Audio for both DisplayPort and HDMI		X	1
AUD[0]	VSXNC			X	1



JTAG SIGNAL OPTION			
Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1" (PU)	"1" (PU)	"0" (PD)
JTAG_TRST#	"0" (PD)	"1" (PU)	NC
JTAG_TCK	CLK	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC

<Core Design>

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Title: **GPU PCIE/STRAPPING(1/5)**

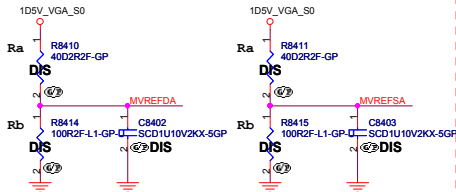
Size A3 Document Number **Enrico Caruso 14** Rev **A00**

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	PE_GPIO0
dGPU mode	H
IGPU	L
IGPU with BACQ	H

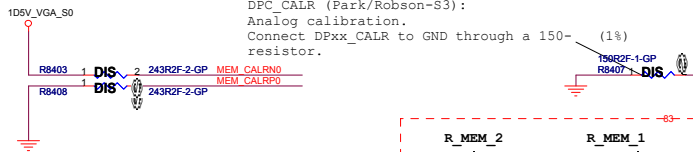
SSID = VIDEO

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



DDR3/GDDR3 Memory Stuff Option (ROBSON-S3/SEYMOUR-XT-S3)

	DDR5	DDR3
MVDDQ	1.5V	1.5V/1.8V
Ra	40.2R	40.2R
Rb	100R	100R

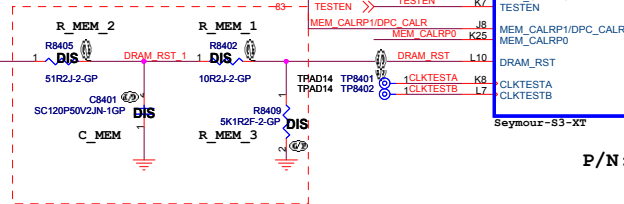


DPC_CALR (Park/Robson-S3):
Analog calibration.
Connect DPxx_CALR to GND through a 150-ohm resistor.

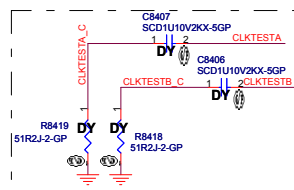
**This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Designator	For SEYMOUR	For Robson
R_MEM_1	10R	10R
R_MEM_2	50R	50R
R_MEM_3	5K	5K
C_MEM	120pF	120pF

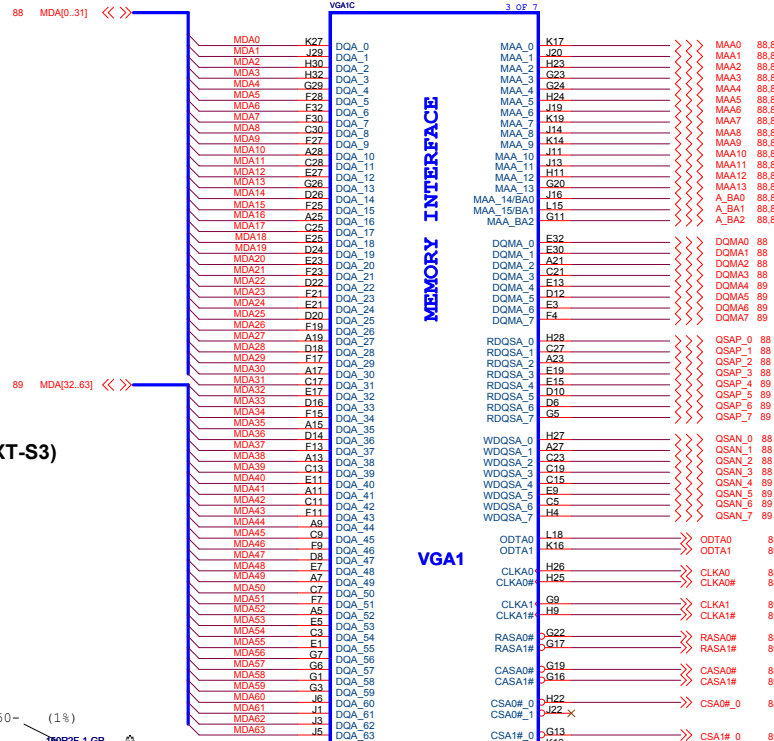
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except R_MEM_2



P/N: FUPJP



For normal GPU operation, these signals can be left floating (do not populate the capacitors and resistors).



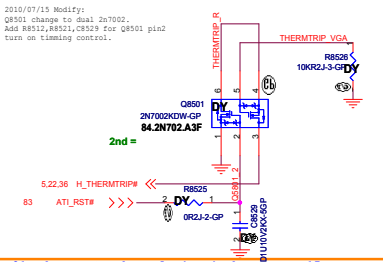
11/16 change part reference to R8441 and stuff
11/18 move R8441 before R8440

2010/07/06
Schematics check list:
A pull-down resistor is required.

DN15ATI Whistler

MEMORY ID Table	
DVDPDATA[3:0]	Description
0000	DDR3 SAMSUNG-K4W1G1646G-BC11 (900MHz) 64M*16
0001	DDR3 Hynix-H5TQ1G63DFR-11C (900MHz) 64M*16
0010	DDR3 SAMSUNG K4W2G1646C-BC11 (900MHz) 128M*16
0011	DDR3 Rynix-H5TQ2G63BFR-11C (900MHz) 128M*16

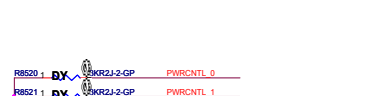
For Seymour,
DPC_PVDD is DPC_VDD18 2010/06/11
DPC_PVSS and all DPC_VSSR are DP_VSSR



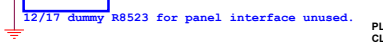
X01: dummy VGA thermal circuit based on DN15
11/18 Del C8529 to follow DN13



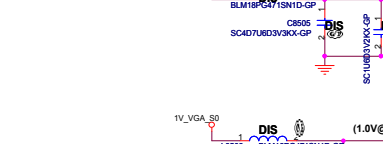
GPIO_6, GPIO_15 PWRCTRL_0, GPIO_16 SSIN, GPIO_20 PWRCTRL_1
Voltage control signals for the core (VDDC and VDDCI).
At Reset, these signals will be inputs with weak internal pull-down resistors.
VDDCI can define all voltage control signals to be either 3.3V or open drain outputs (all signals must be the same type). The output state (high/low) of these signals is programmable for each PowerPlay state.



12/17 dummy R8523 for panel interface unused.



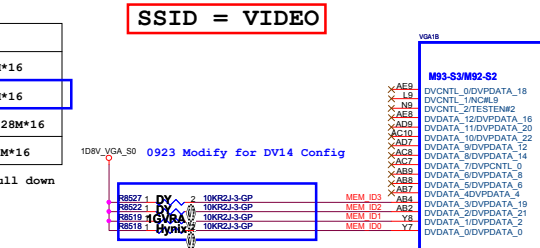
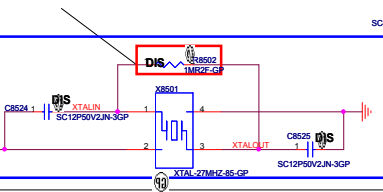
11/18 Del 27M CLK circuit from PCH



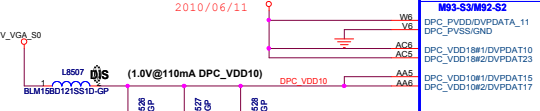
2010/07/06
Schematics check list:
A 1-M ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.



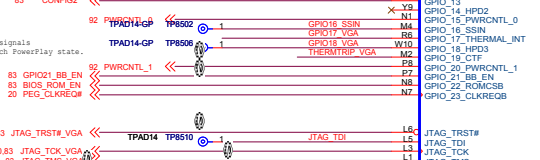
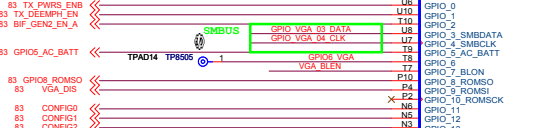
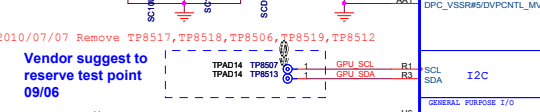
2010/07/06
Schematics check list:
A 1-M ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.



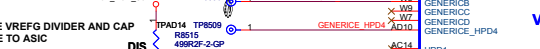
MEM_ID Control



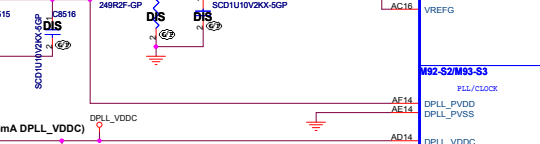
2010/07/07 Remove TP8517, TP8518, TP8506, TP8519, TP8512
Vendor suggest to reserve test point 09/06



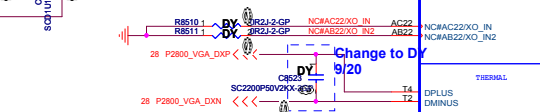
12/17 dummy R8523 for panel interface unused.



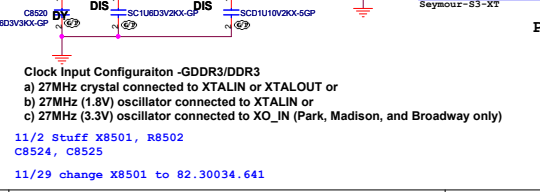
11/18 Del 27M CLK circuit from PCH



2010/07/06
Schematics check list:
A 1-M ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.



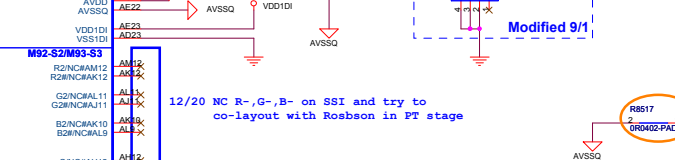
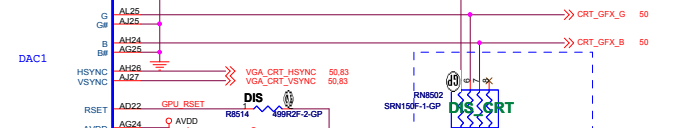
2010/07/06
Schematics check list:
A 1-M ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.



MEM_ID Control



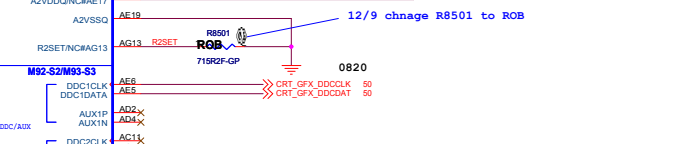
2010/07/07 Remove TP8517, TP8518, TP8506, TP8519, TP8512
Vendor suggest to reserve test point 09/06



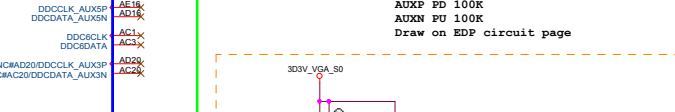
12/17 dummy R8523 for panel interface unused.



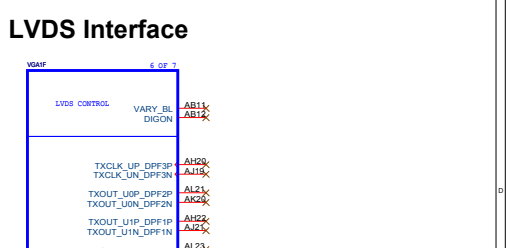
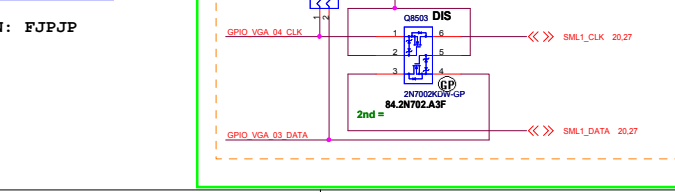
11/18 Del 27M CLK circuit from PCH



2010/07/06
Schematics check list:
A 1-M ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.



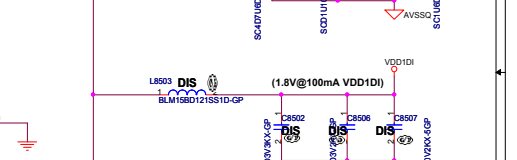
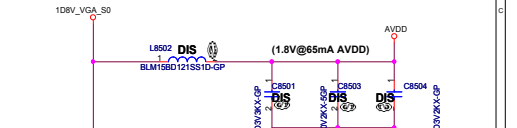
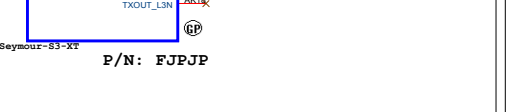
2010/07/06
Schematics check list:
A 1-M ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.



MEM_ID Control



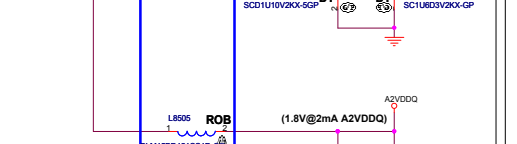
2010/07/07 Remove TP8517, TP8518, TP8506, TP8519, TP8512
Vendor suggest to reserve test point 09/06



12/17 dummy R8523 for panel interface unused.



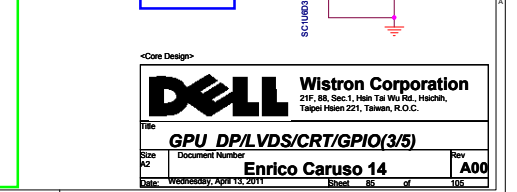
11/18 Del 27M CLK circuit from PCH



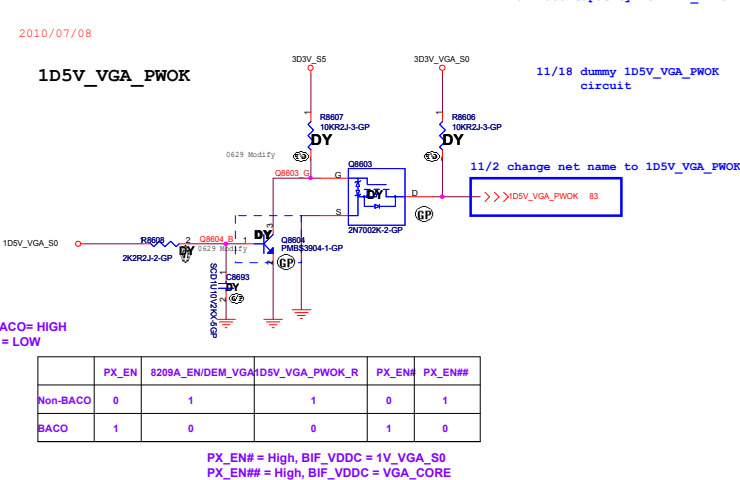
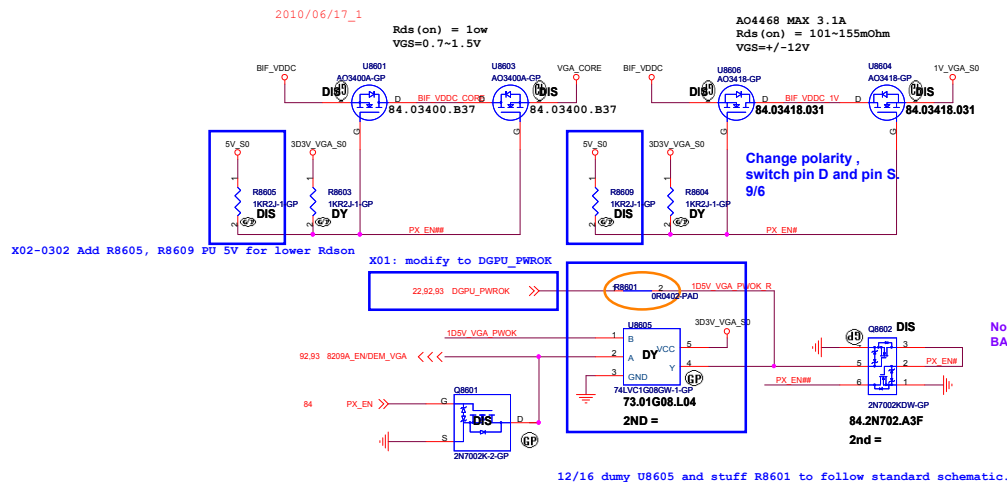
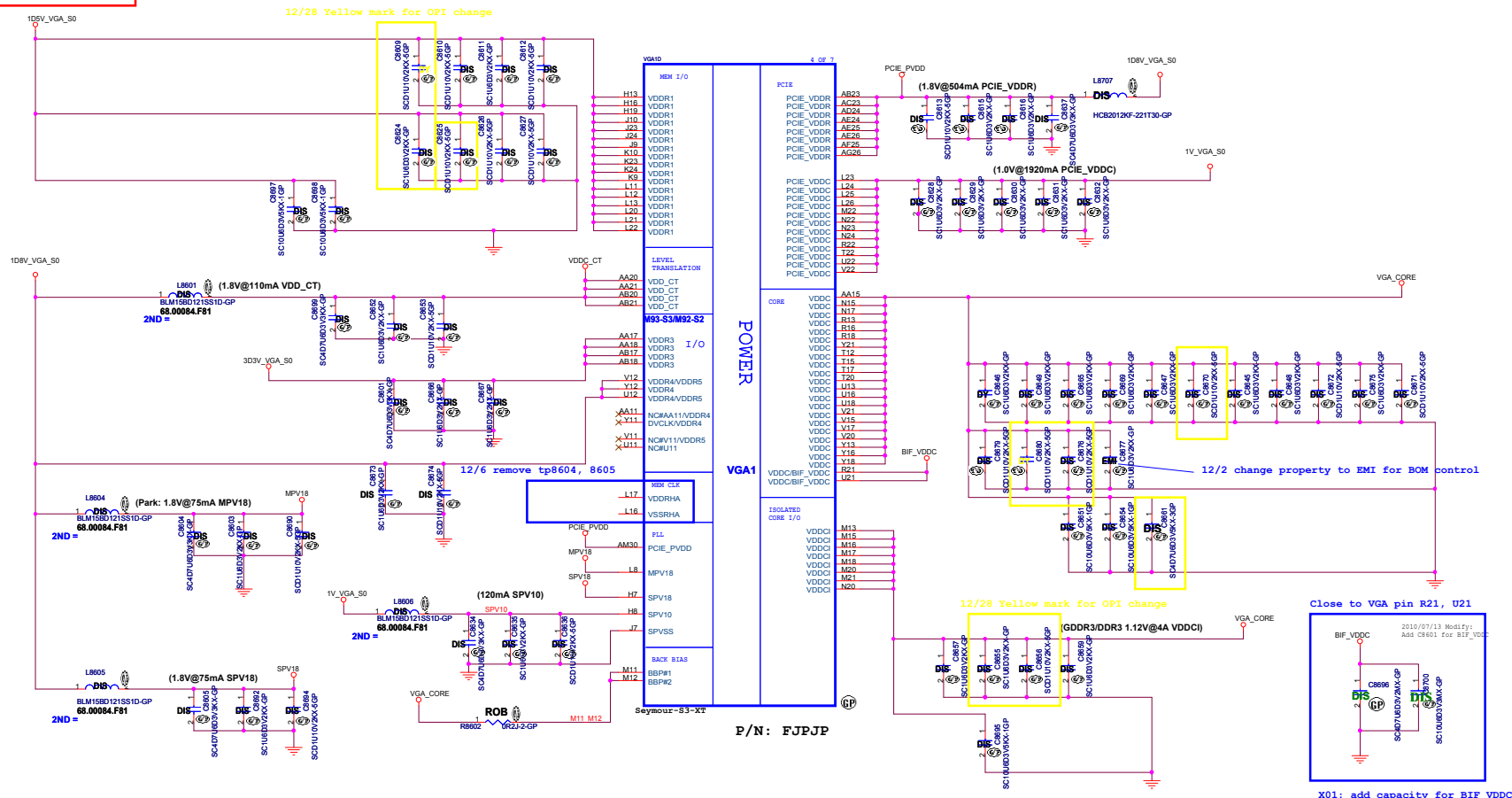
2010/07/06
Schematics check list:
A 1-M ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.



2010/07/06
Schematics check list:
A 1-M ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.



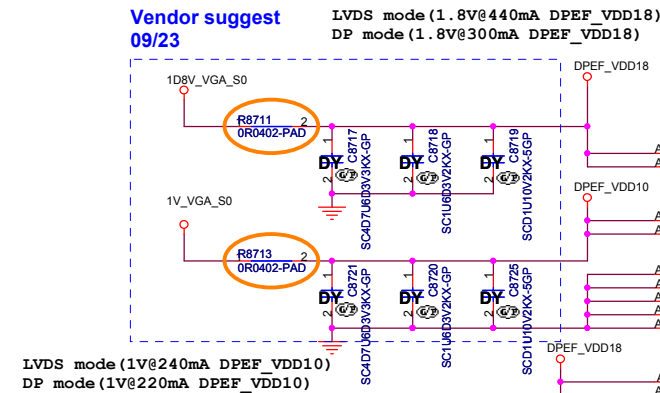
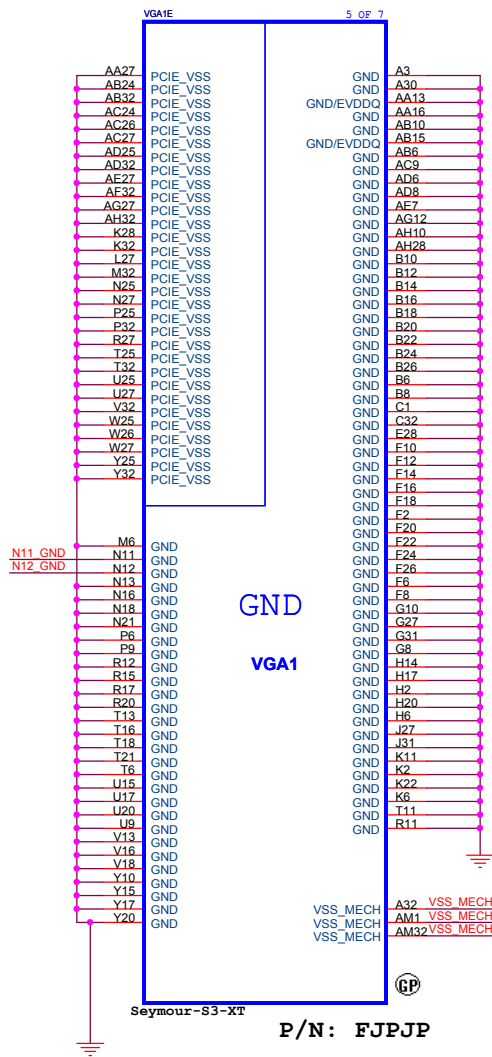
SSID = VIDEO



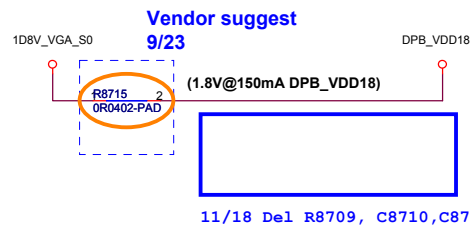
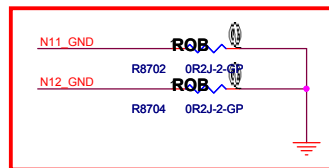
	PX_EN	8209A_EN/DEM_VGA	AD5V_VGA_PWOK_R	PX_EN#	PX_EN#
Non-BACO	0	1	1	0	1
BACO	1	0	0	1	0

PX_EN# = High, BIF_VDDC = 1V_VGA_S0
PX_EN## = High, BIF_VDDC = VGA_CORE

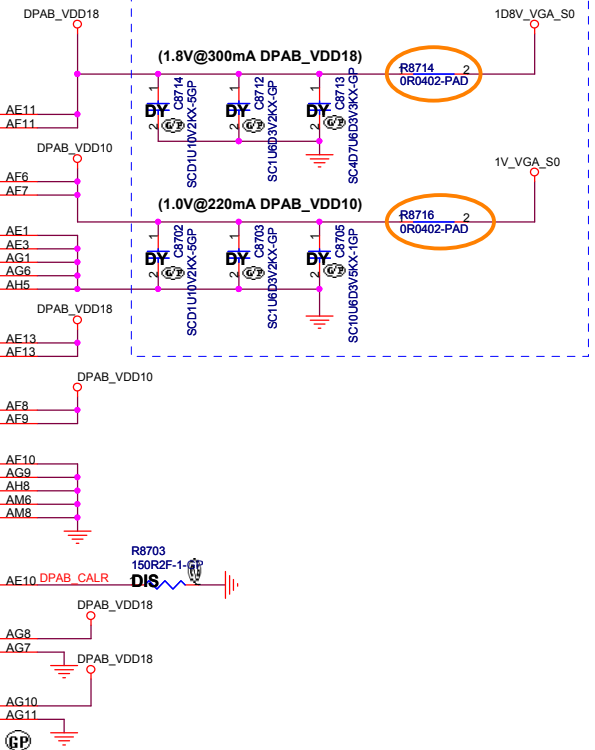
SSID = VIDEO



2010/07/09 N11 and N12: in Seymour is NC

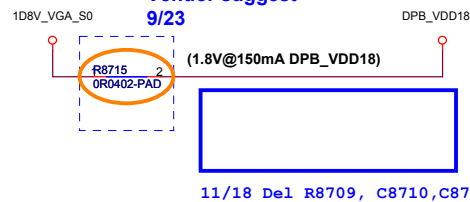


Vendor suggest
09/23



P/N: FJJPJ

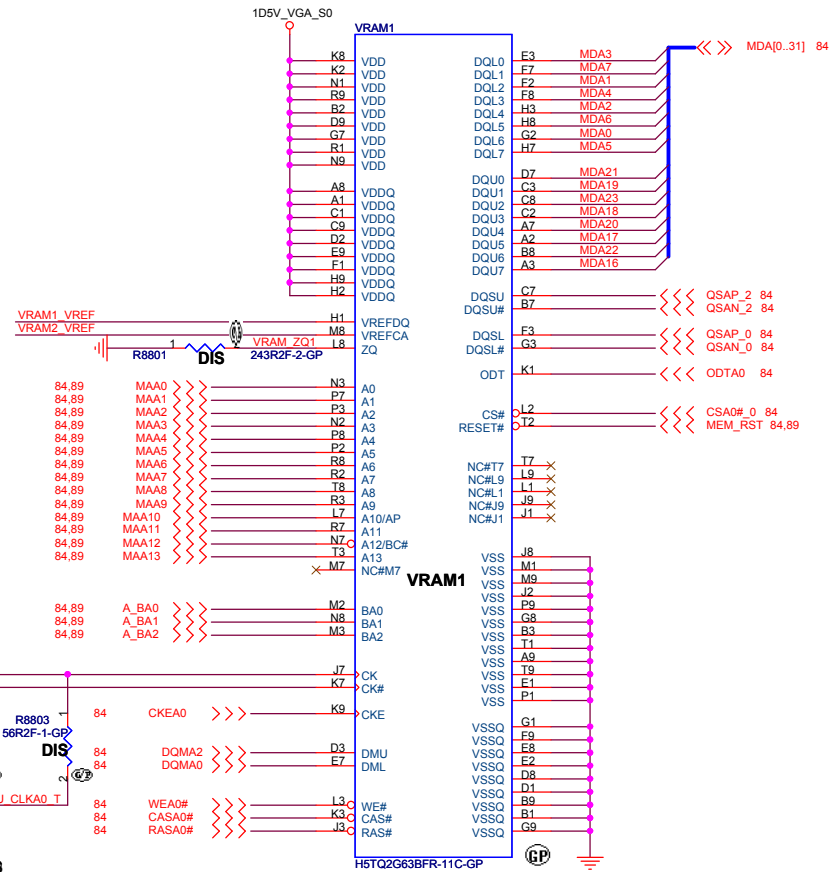
Vendor suggest
9/23



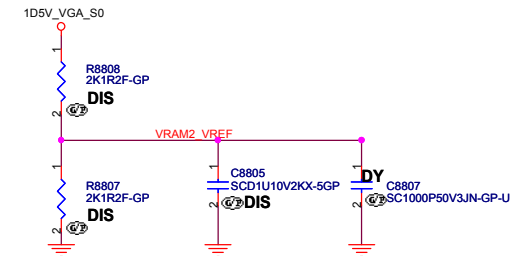
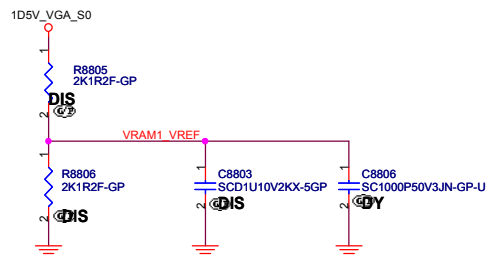
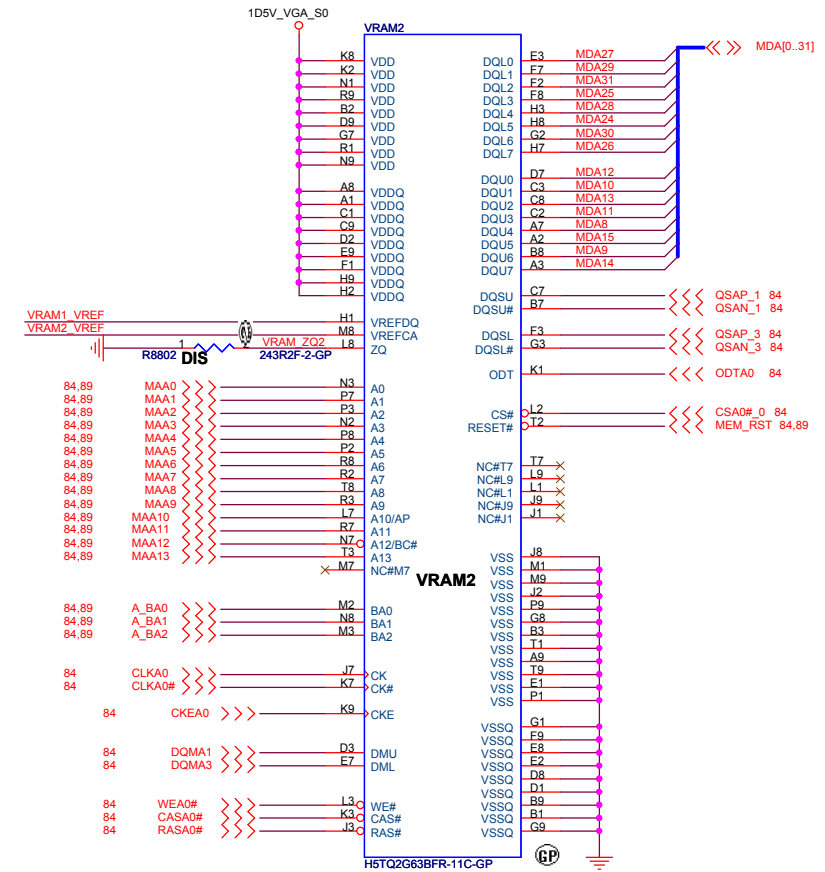
11/18 Del R8709, C8710, C8711

<Core Design>

SSID = VIDEO



X01-0211 change VRAM symbol for layout (larger package)



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GPU-VRAM1,2 (1/4)

Size	
Custom	

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SSID = VIDEO

Simulation 10/07

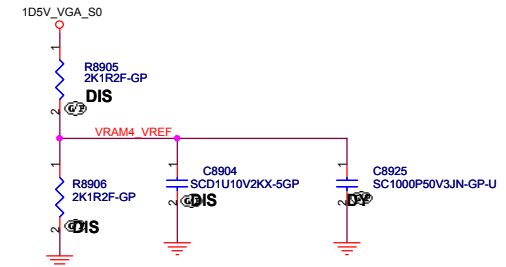
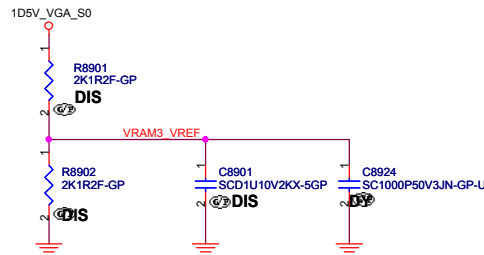
12/28 Yellow mark for OPI change

Simulation 10/07

Simulation 10/07

12/28 Yellow mark for OPI change

X01-0211 change VRAM symbol for layout (larger package)



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Title GPU-VRAM3,4 (2/4)		
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GPU-VRAM5,6 (3/4)

Size
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Title

GPU-VRAM7,8 (4/4)

Size
A3

Document Number

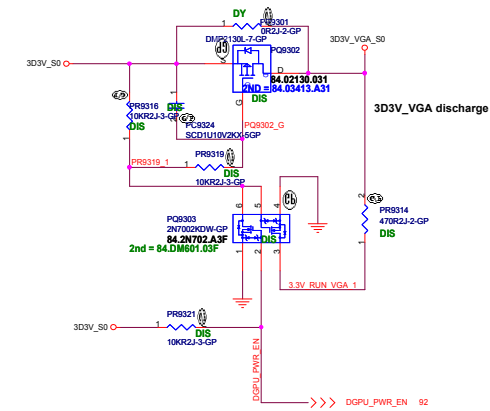
Rev
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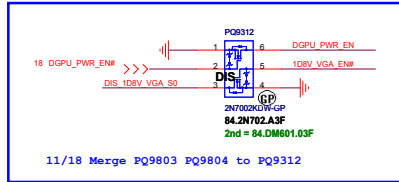
Sheet 91 of 105

3D3V_S0 to 3D3V_VGA_S0 Transfer

Change DUMMY Reference Name to PX_BACO

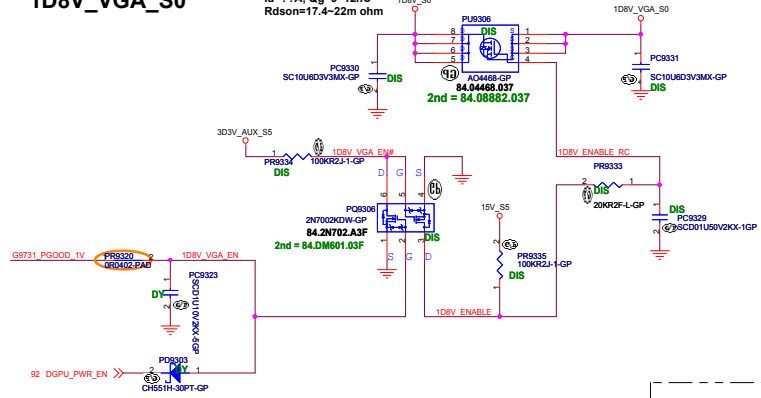


dGPU mode	DGPU_PWR_EN#
IGPU	H
IGPU with BACO	L

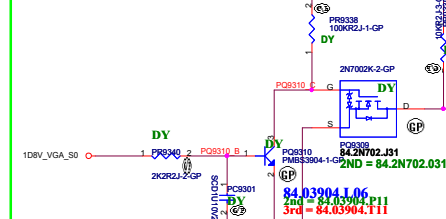


1D8V_VGA_S0

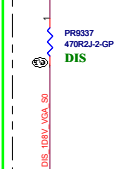
AO4468, SO-8
Id=77A, Qg=9-12nC
Rds(on)=17.4-22m ohm



1D8V_VGA_S0_PG



Discharge Circuit



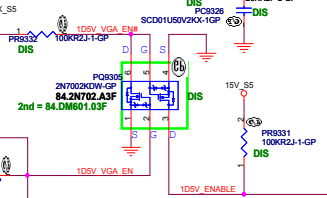
1D5V_VGA_S0

change low Rds(on) MOSFET

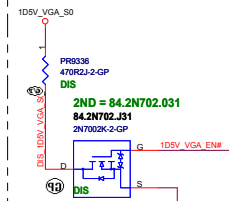
AO4468, SO-8
Id=7A, Qg=9-12nC
Rds(on)=17.4-22m ohm

1D5V_S3 to 1D5V_VGA_S0 trace need increase to avoid 1D5V_VGA_S0 DROP Voltage.

Park Madison Does Not Support BACO, So follow Old Sequence
Seymour Whistler Robson Support BACO, So Change Sequence



Discharge Circuit



G9731 for 1V_VGA_S0

Park Madison Does Not Support BACO, So follow Old Sequence
Seymour Whistler Robson Support BACO, So Change Sequence

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

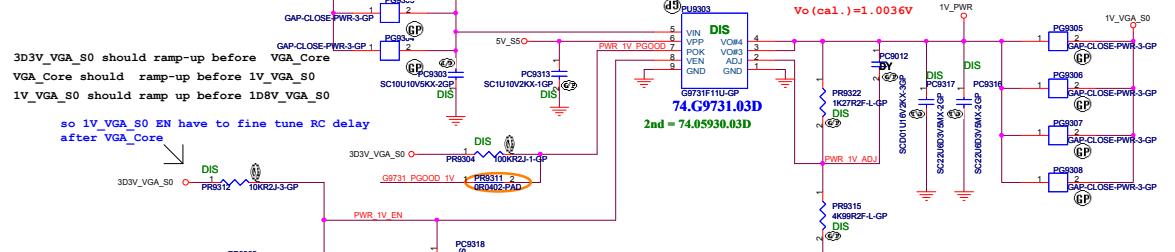
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

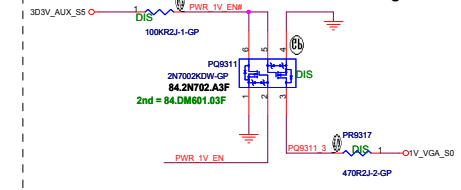
1V_VGA_S0
Design current = 2.445A

$$V_{out} = 0.8V * (R1 + R2) / R2 = 1.0036V$$

$$V_o (cal.) = 1.0036V$$



Discharge Circuit



<Core Design>

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Title

LVDS Switch

Size
A3

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Title

CRT Switch

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SSID = SDIO

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Title

TOUCH PANEL

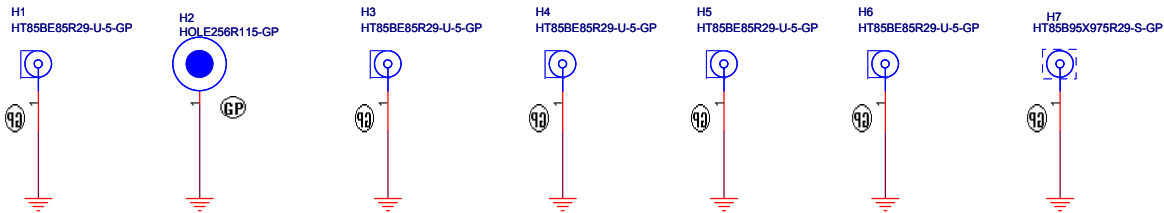
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Document Number
Enrico Caruso 14

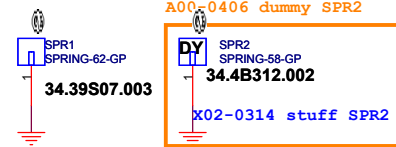
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X01-0208 stuff SPR1 and add SPR2



SSID = Mechanical

12/17 add SPR1 for EMI
12/21 change SPR1 to 34.4B312.002
12/22 change SPR1 to 34.39S07.003

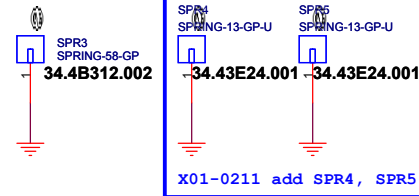
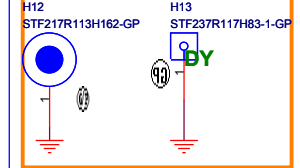
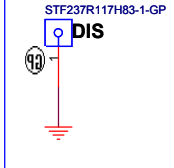
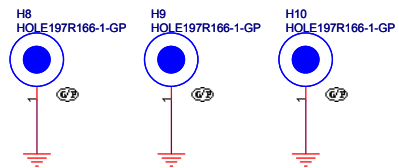
X01-0211 change SPR2, SPR3 to 34.4B312.002

X01-0210 add SPR3

For CPU BRACKET

VGA Stand-Off

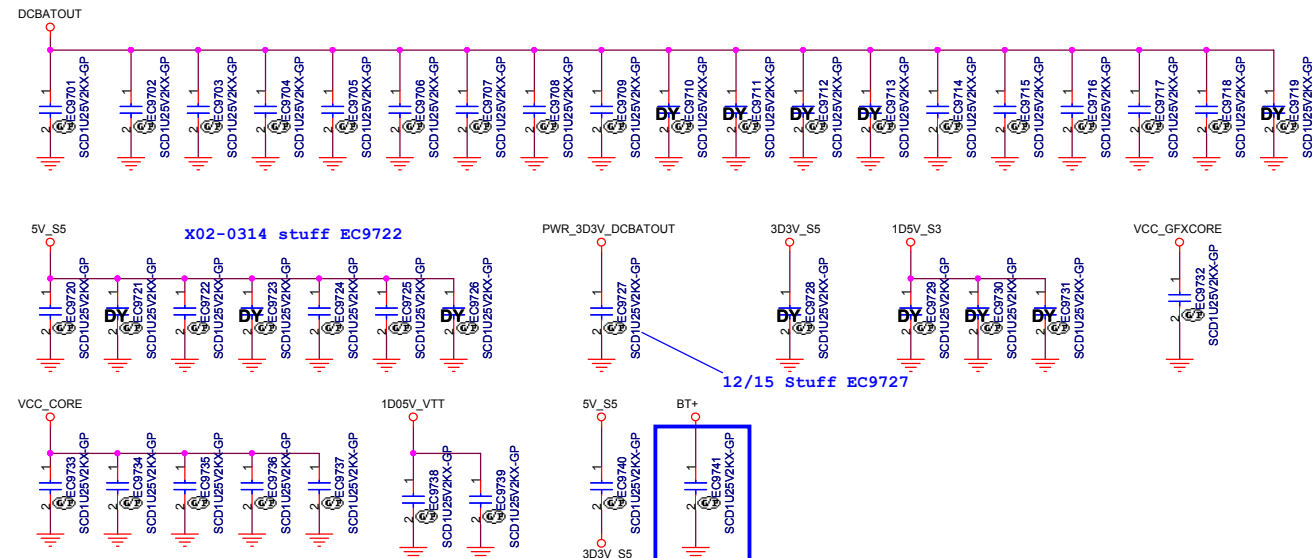
PCH Stand-Off



A00-0412 dummy H12, H13 for remove PCH Heatsink

A00-0413 change H12 to 34.4HL17.001

12/2 Delete SPR1, SPR2

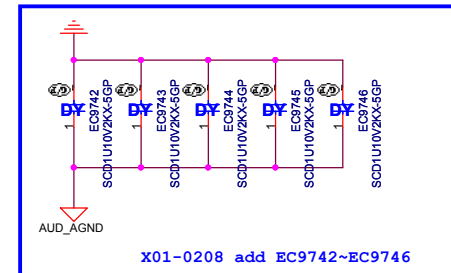


12/15 Stuff EC9727

12/17 Add EC9741

12/6 Add EMI capacities

12/20 change EMI caps to 0402 package

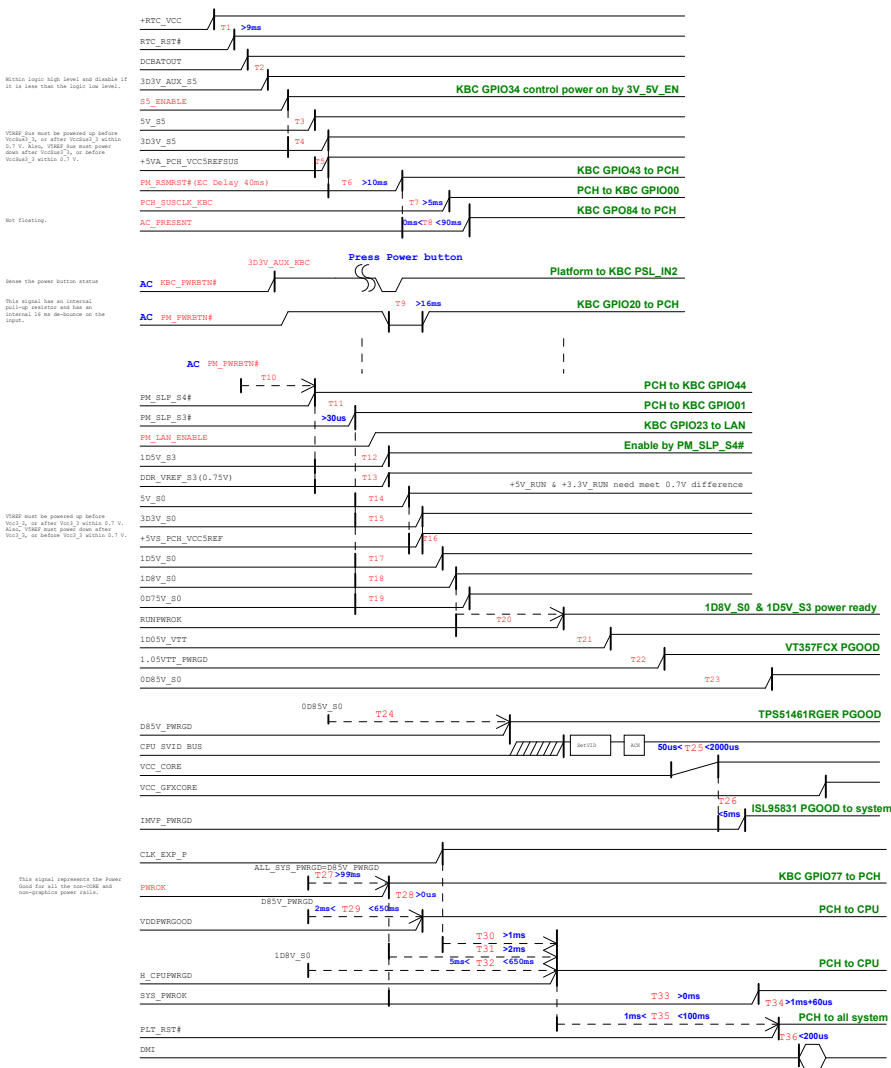


<Core Design>

Huron River Platform Power Sequence

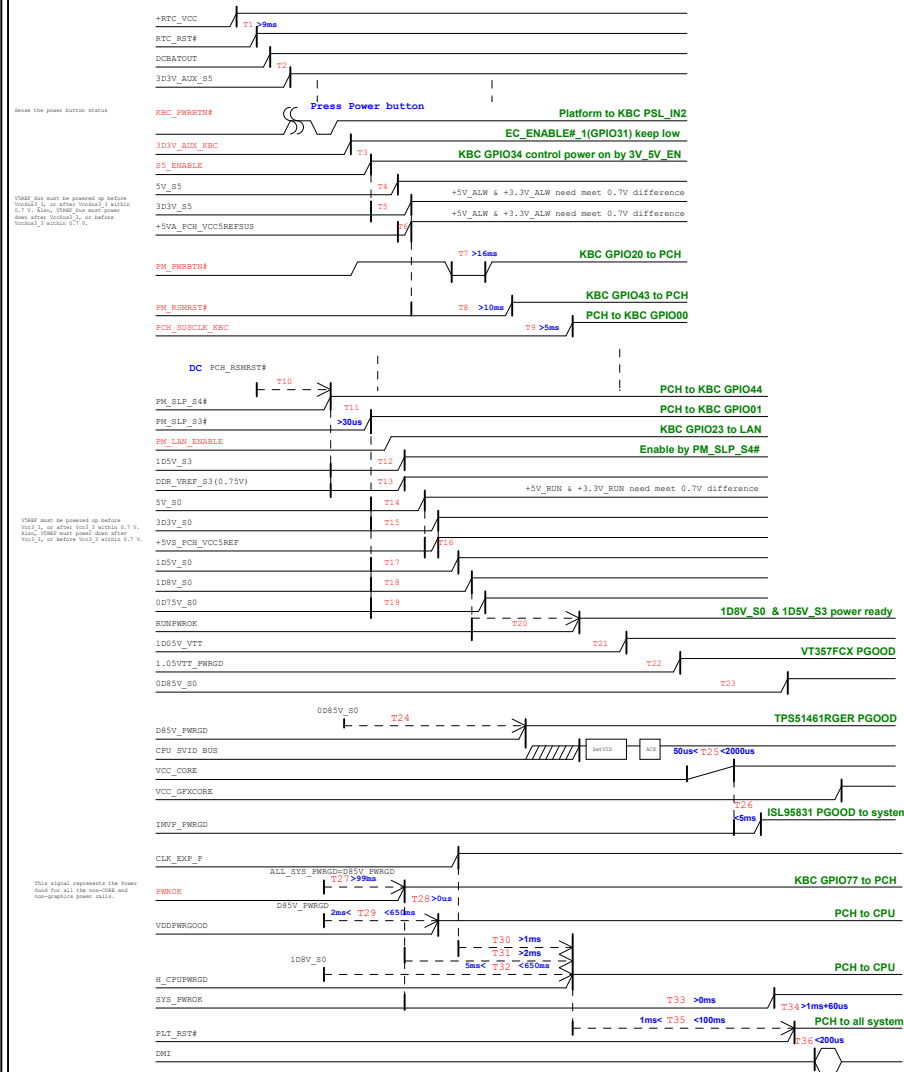
(AC mode)

red word: KBC GPIO

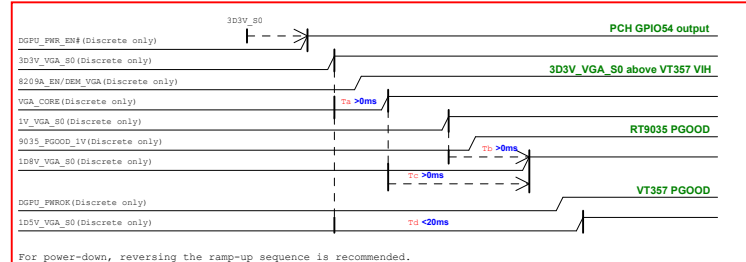


(DC mode)

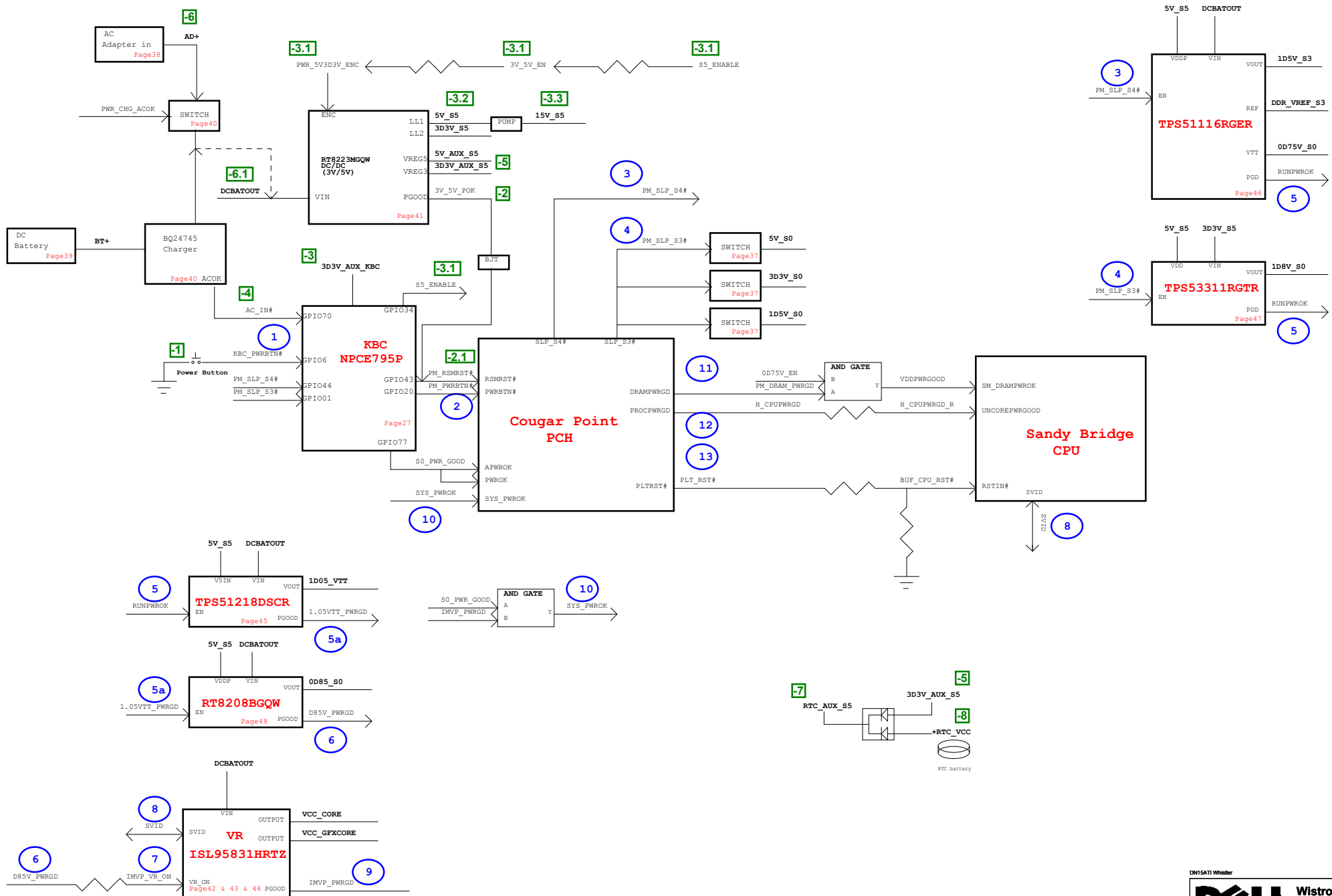
red word: KBC GPIO



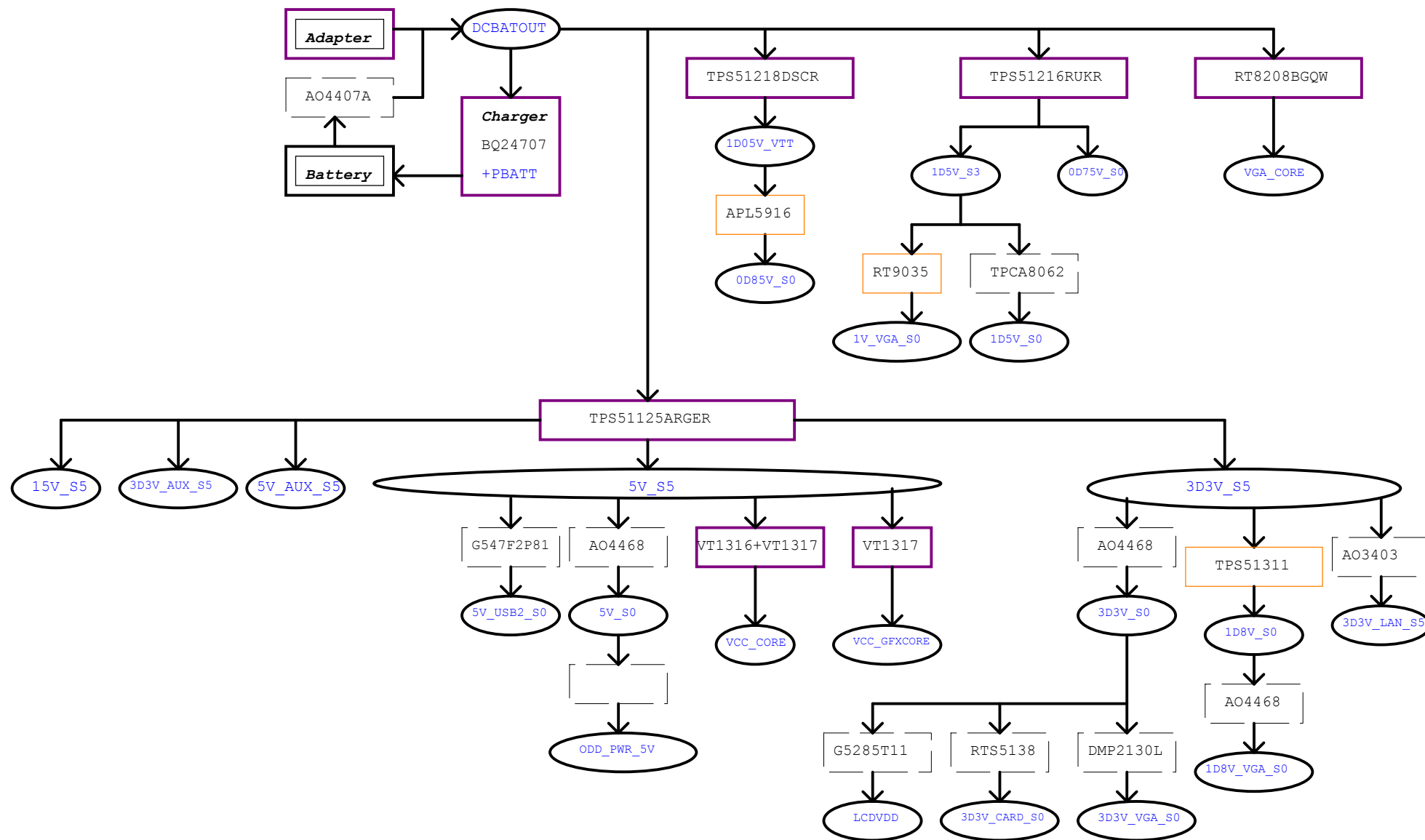
Robson XT Power-Up/Down Sequence



Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 13



Power Shape

Regulator

LDO

Switch

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Power Block Diagram

Size

Document Number

Rev

A3

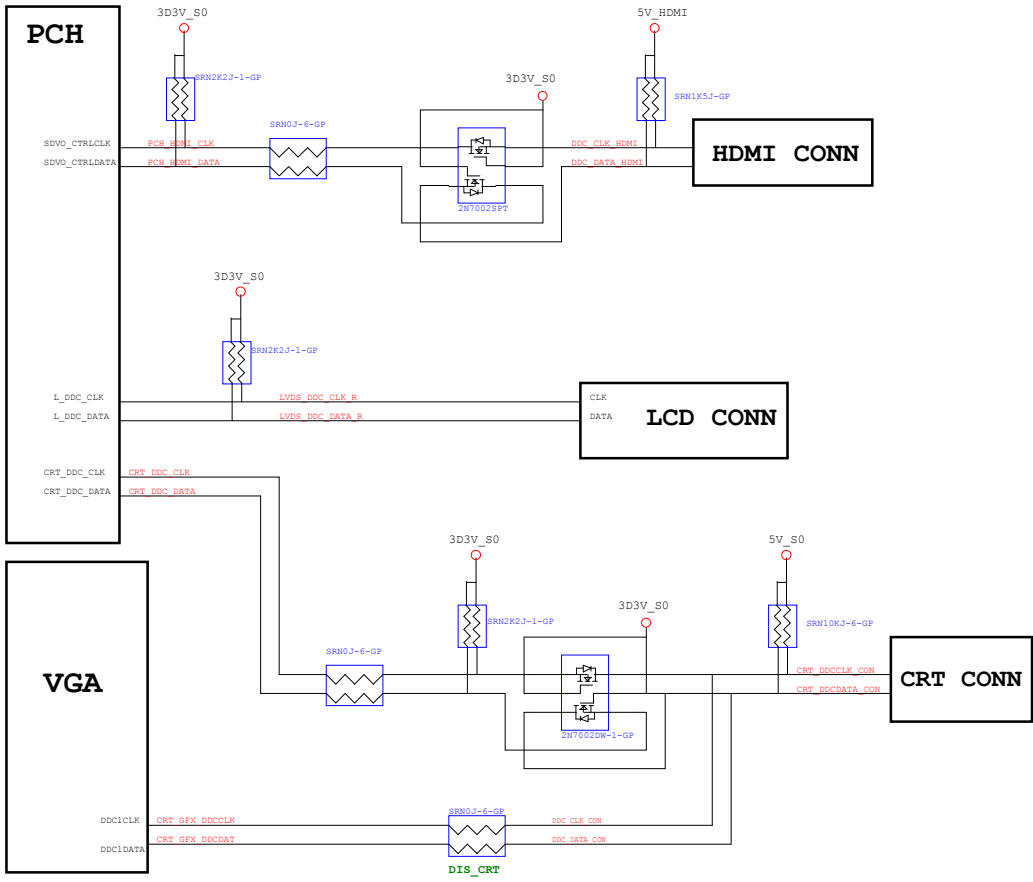
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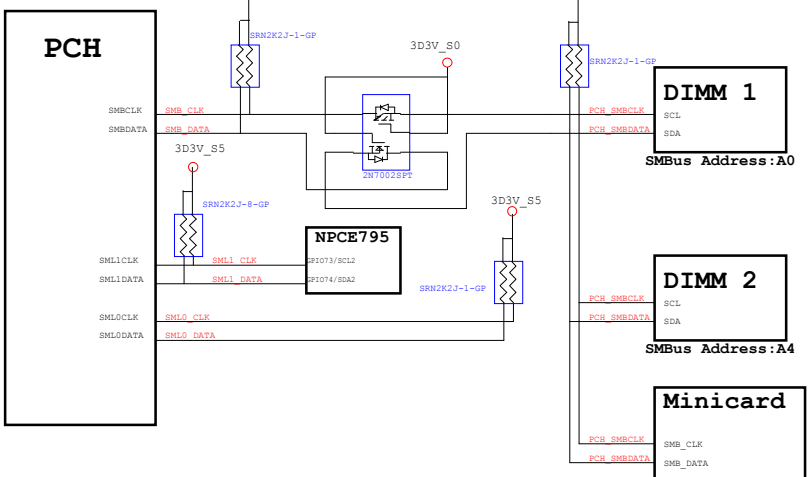
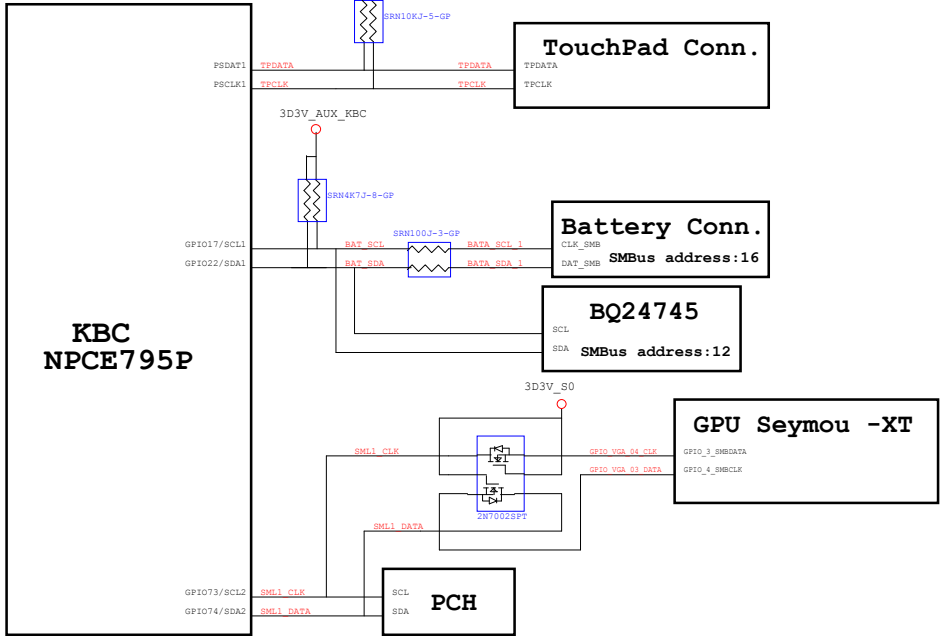
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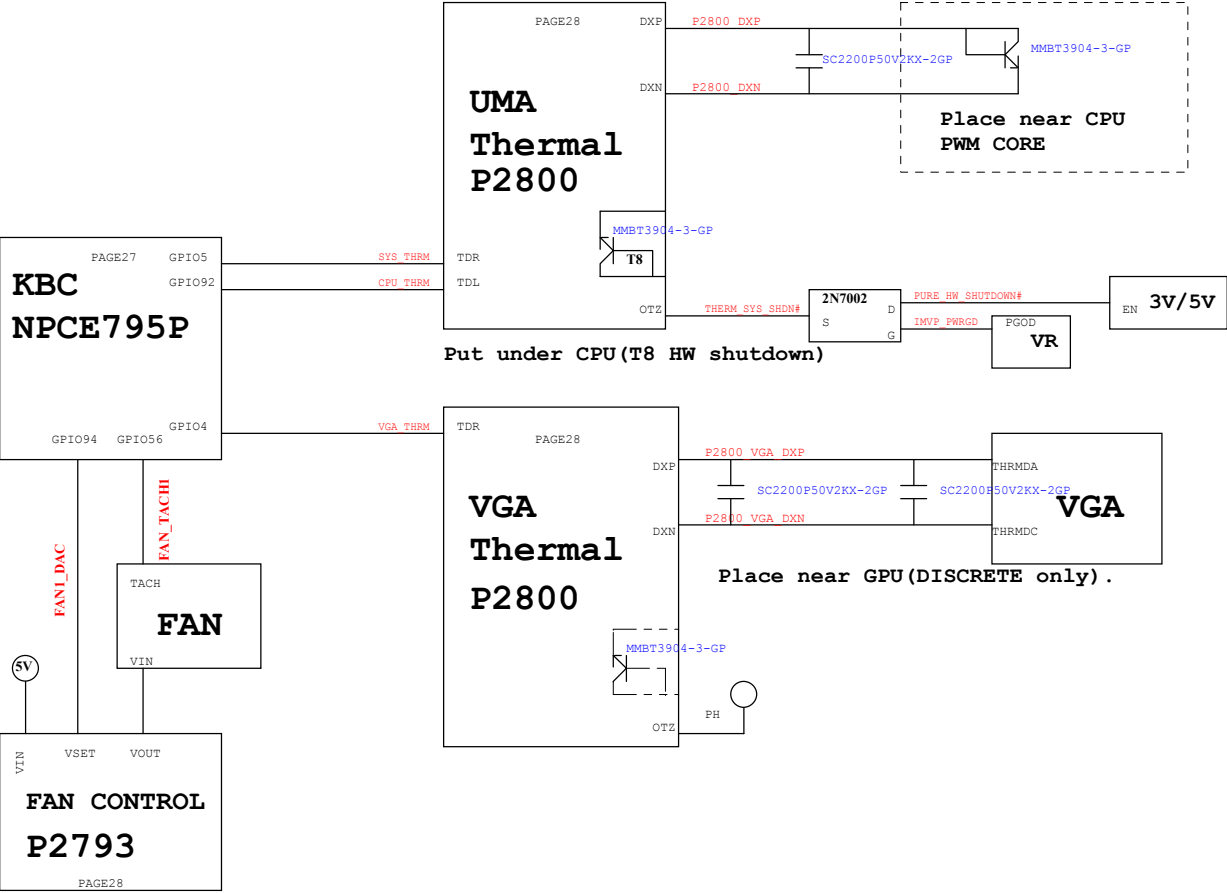
PCH SMBus Block Diagram



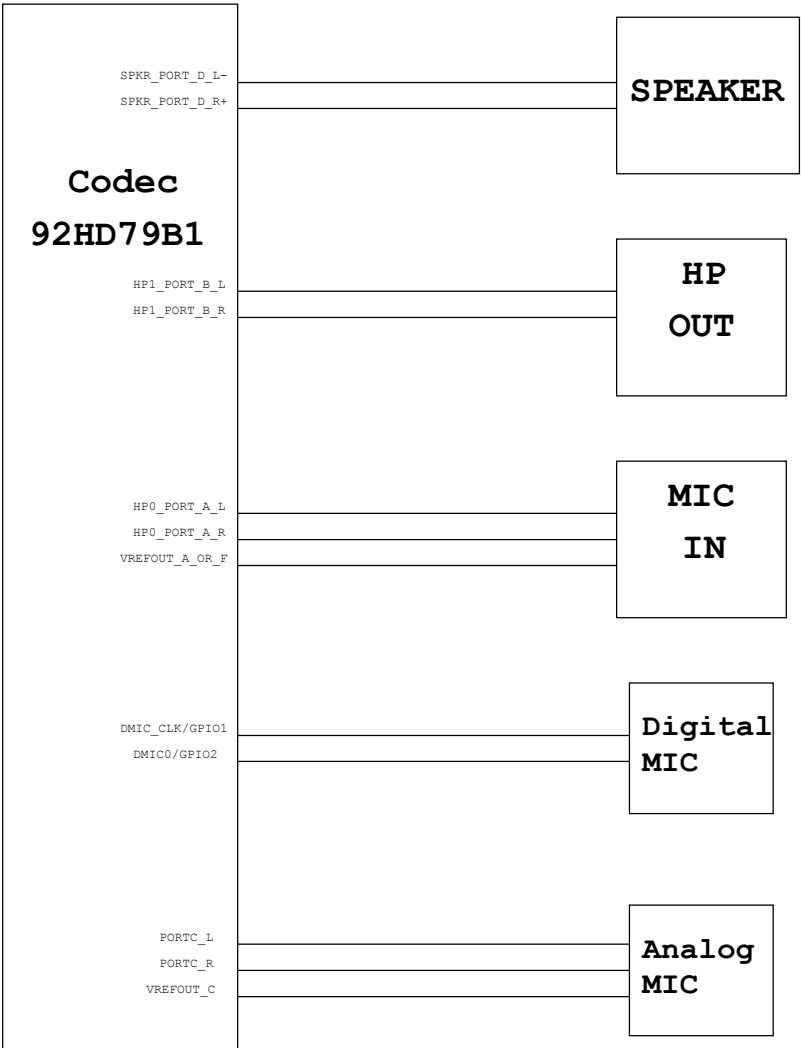
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



DATA	PAGE	Change Description	Version
12/28	85	dummy VGA thermal circuit	X01
12/28	86	modify to DGPU_PWROK	X01
12/28	86	add capacity for BIF_VDDC	X01
12/28	93	dummy PR9326	X01
1/14	93	modify CS#, WP#	X01
1/27	5	Add C504 for noise couple.	X01
1/27	8	Stuff C812, C822, C831, C834 for VCC core noise issue.	X01
1/27	27	Del R2757 to follow standard 10mW circuit	X01
1/27	31	change Q3101 base power rail for leakage issue.	X01
1/27	40	X01-0127 DY PQ4007, PR4038, PR4039 for new version BQ24707	X01
2/8	21	Add RN2101, R2127 for LPC EA result	X01
2/8	27	Dummy R2769	X01
2/8	50	change R5002, R5003 to 33R	X01
2/8	69	TPAD1 to 20.K0464.004	X01
2/8	27	change R5002, R5003 to 33R	X01
2/8	97	add EC9742~EC9746	X01
2/8	97	stuff SPR1 and add SPR2	X01
2/9	28	dummy U2805 circuit	X01
2/9	46	PT4603 UMA-->220uF DIS-->470uF	X01
2/9	48	dummy PC4809 for BBU result.	X01
2/10	5	Merge R512 R514	X01
2/10	21	change RN2101 to RN2104 RN2105	X01
2/10	27	change R2724 to meet X01 PCB ver	X01
2/10	46	del PT4602	X01
2/10	46	change PC4610 from 0.22uF to 10uF	X01
2/10	97	add SPR3	X01
2/10	21	Merge R5115 R2116	X01
2/11	31	add C3122 for soft-sart	X01
2/11	59	Add EMI solution for Surge	X01
2/11	19,27	Change R1925, R1924, R1906, R1913, R2720, R2758, R2759, R2760 to short-pad	X01
2/14	82	add AFTP8201~8210	X01

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DATA	PAGE	Change Description	Version
0212	40	Change charger IC to new version	X01
0302	31	Dummy PCIE_CLK_LAN_REQ# circuit	X02
0302	86	Add R8605, R8609 PU 5V for lower Rdson	X02
0303	14,15,17,18 19,22,23,24 27,29,31,36 37,50,51,68	Change R1404, R1405,R1504, R1503,RN1704, R1807, R1903, R1910, R1912, R2214, R2304, R2305, R2306, R2307, R2404, R2405, R2406, R2409, R2702, R2735,R2762, R2756, R2911,R2914, R2917, R3104, R3115, R3117, R3614, R3710, RN5010, RN5117, R6811, R6813, R6804, R6805 0R to short pad	X02
0309	86	Change AFTP test point to follow DV14 AMD	X02
0310	41,45,92,97	Stuff PC4120, EC4501, PC9205, EC9708, EC9709, EC9714, EC9715, EC9716, EC9717, EC9718, EC9720, EC9724, EC9725, EC9740	X02
0311	28	Add R2816& R2817 to option VGA_THRM and DY the circuit	X02
0311	83	Change R8316, R8331 to short pad	X02
0311	59	Change GDT5901& GDT5902 to GD5901& GD5902	X02
0311	18	dummy R1804	X02
0311	31	add rest circuit to provent leakage.	X02
0311	32	Stuff TR3201 and change symbol to 68.00201.141	X02
0314	38	Del short pad PAD1 to prevent system burn.	X02
0314	97	Stuff SPR2	X02
0314	61,97	Stuff EC9722,C6106	X02
0314	36	Change U3606 footprint.	X02
0315	58	Change MIC2 to 20.F1889.002	X02
0315	88,89	Modify VRAM property PN and footprint	X02
0315	32,59	Modify part reference problem of ER5912& TR3201.	X02
0316	68	Modify WLED1 cirucit for brightness.	A00
0320	31	Change R3118 for LOM power sequence	A00
0320	49	Change TR4901 to 120ohm.	A00
0320	61	Change TR601 120ohm.	A00
0320	68	Change resistor for LED brightness	A00
0320	82	Change TR8201, TR8202 to 120ohm.	A00
0320	83	Dummy R8302 for disable de-emphasis	A00
0329	27	change R2735 to 10R and C2711 to 220p	A00
0329	68	Change R6814 to 10KR	A00
0406	97	Dummy SPR2	A00
0406	32, 49, 61, 65,82	Remove R3206, R3207, R4903, R4904, R6102, R6103, TR6501, R8201, R8202, R8203, R8204 PAD	A00

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