

SULLIVAN

REV : X01

@ : Depop Component for All

Dothan Schematic with Capture CIS and Function field

uFCPGA Dothan
02-11-2004
REV: 0.2

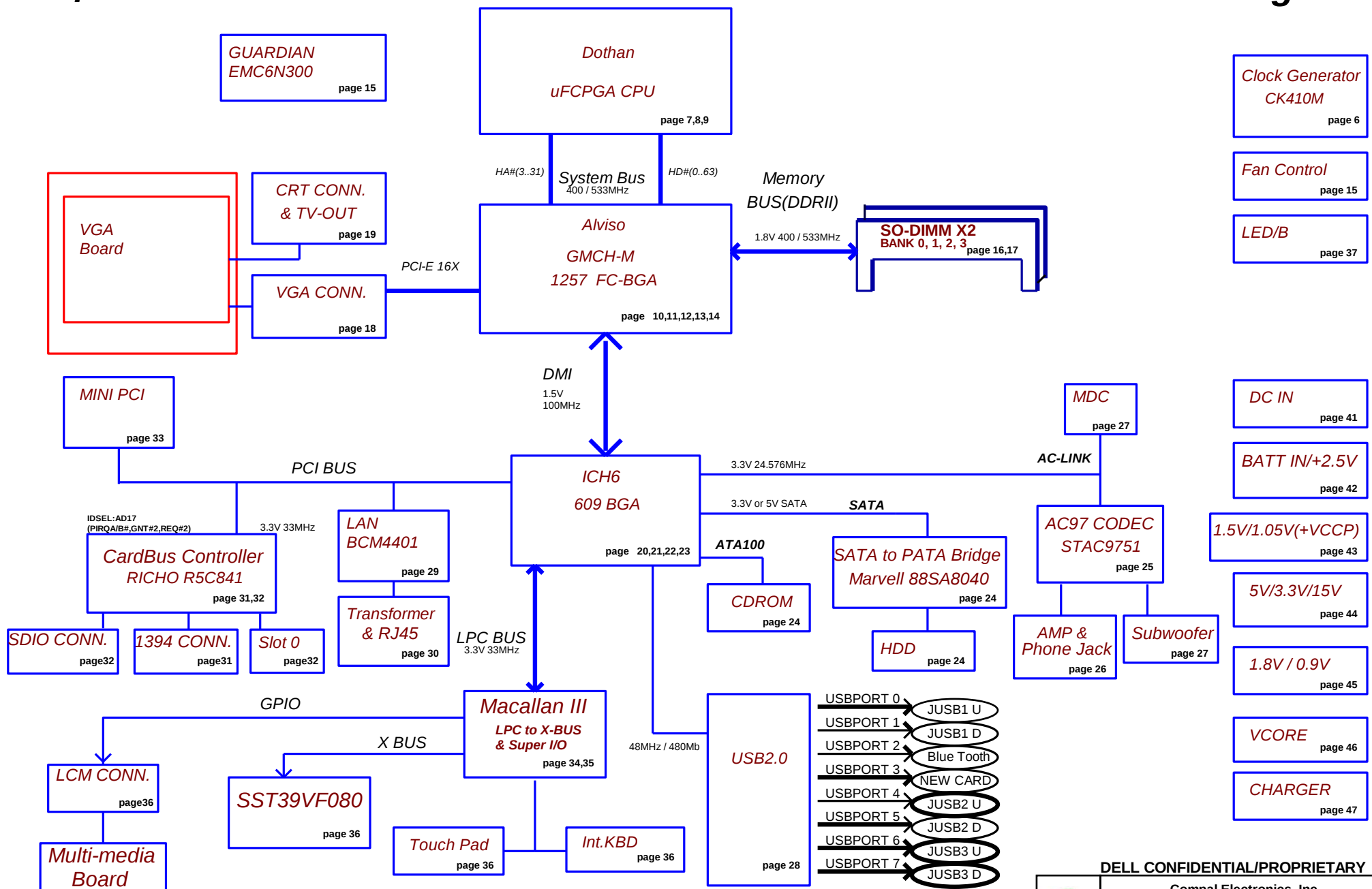
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Cover Sheet			
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PM TABLE

State \ power plane	+3VALW +5VALW	+3VSUS +5VSUS +1.8VSUS +1.5VSUS	+5VRUN +3VRUN +0.9V_DDR_VTT +2.5VRUN +1.8VRUN +1.5VRUN +VCC_CORE +VCCP +15V
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	1	D,C
MINI PCI	AD19	3	D,B
LAN	AD16	4	C

USB TABLE

USB PORT#	DESTINATION
0	JUSB1 (Top)
1	JUSB1 (Bottom)
2	Blue Tooth
3	NEW CARD
4	JUSB2 (Top)
5	JUSB2 (Bottom)
6	JUSB3 (Top)
7	JUSB3 (Bottom)

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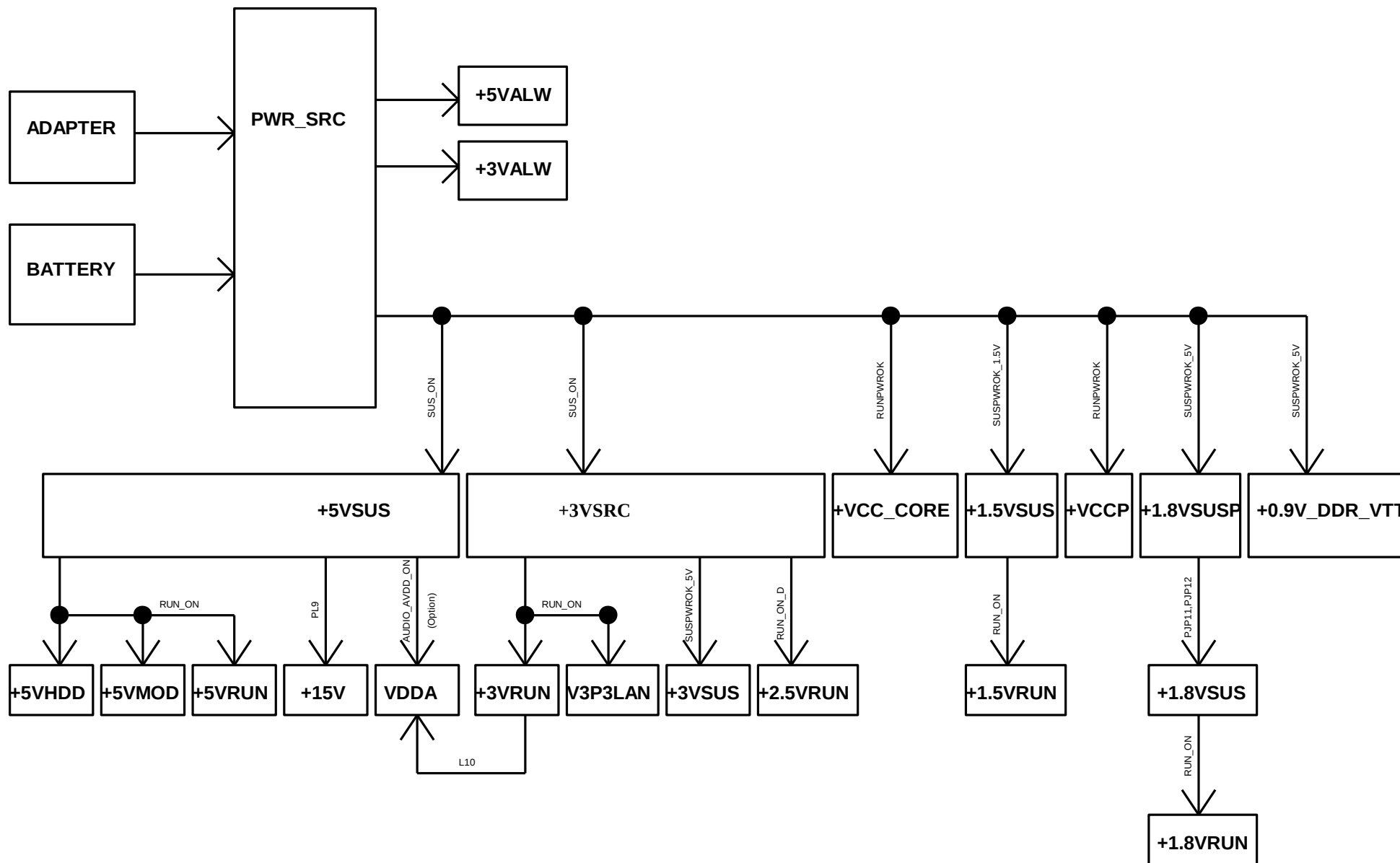


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Index and Config.

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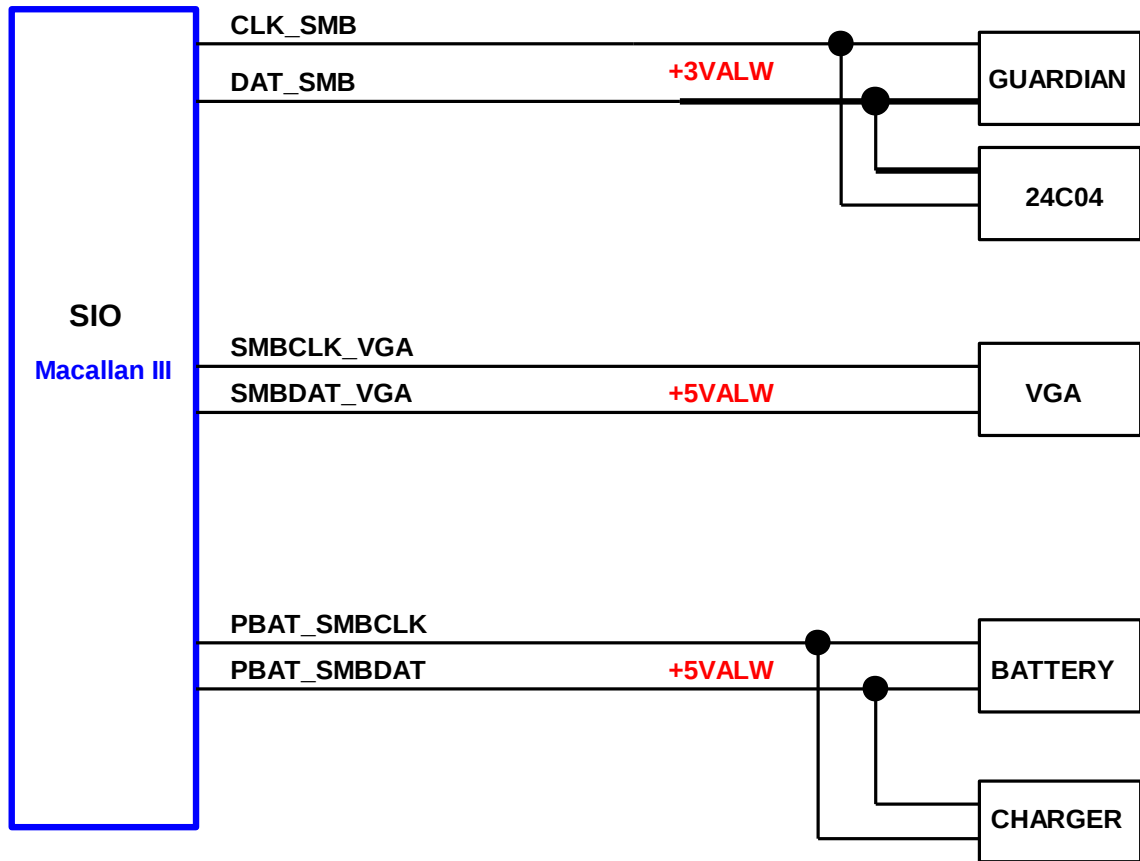
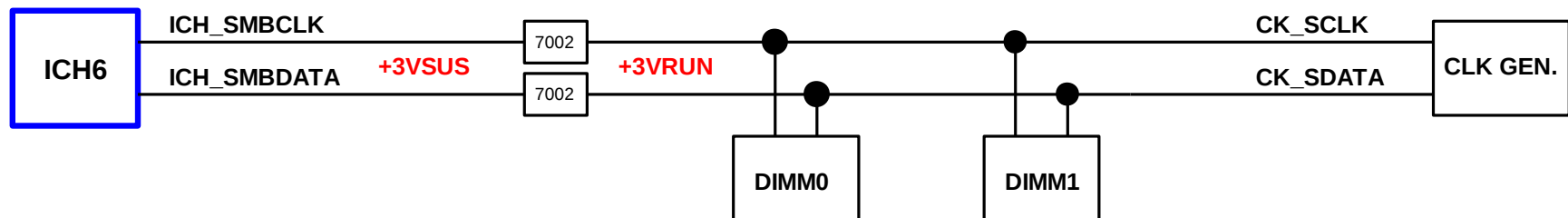


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Power Rail

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	Device	Address
ICH6-SMBus	DIM0	A0h
	DIM1	A2h
	CLK GEN.	D2h
EC-SMBus	GUARDIAN	5Eh
	24C04	A2h
	VGA	58h
	Battery	16h
	Charger	12h

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FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL0	CLKSEL1	CLKSEL2	MHz	MHz	MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	0	RESERVED		

Table 1: ICS 954201 / Cypress CY28411

Dothan-A 400MHz, Install R390, No pop. R394, R395
Dothan-A 533MHz, Install R394, No pop. R390, R395

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Clock Generator

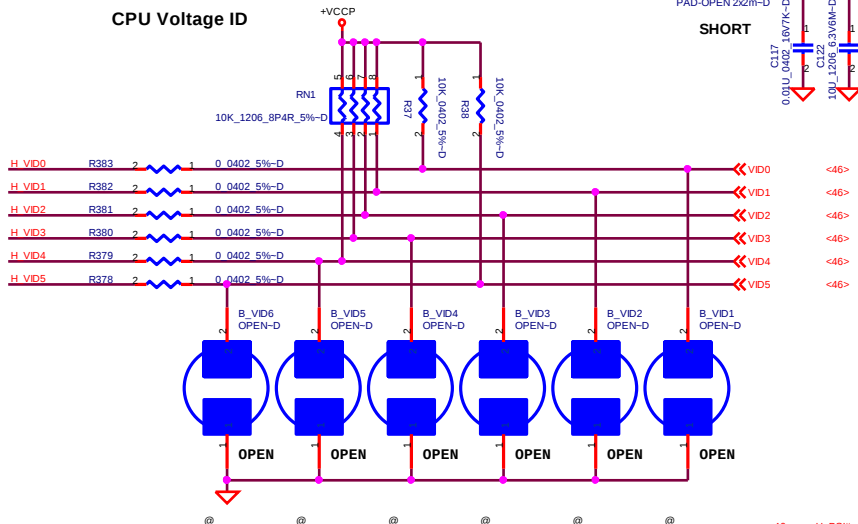
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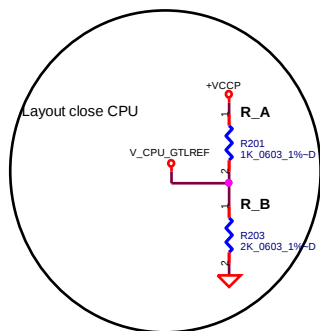


For test only ,Cmos output

CPU Voltage ID



Layout close CPU



Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.

Dothan

POWER, GROUND, RESERVED SIGNALS AND NC

Dothan

POWER, GROUND

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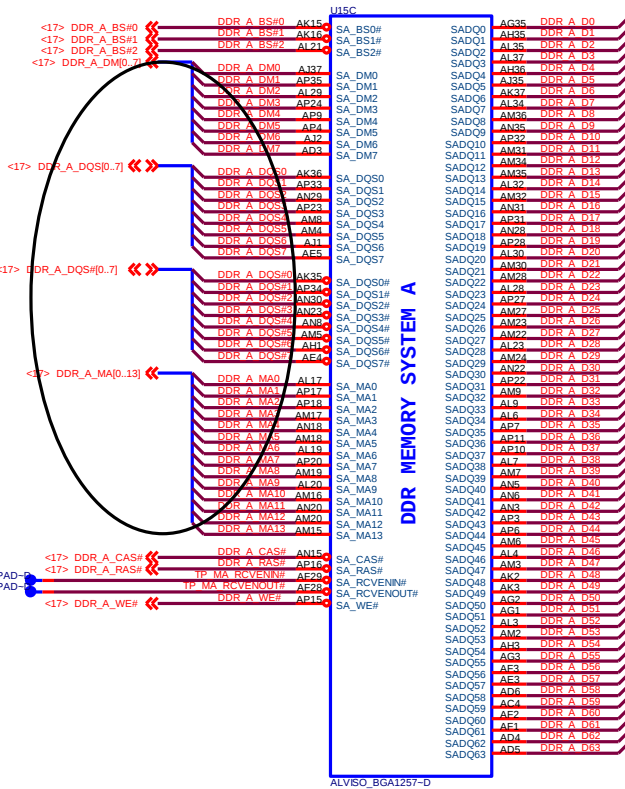
Dothan Processor(2/2)

LA-2171

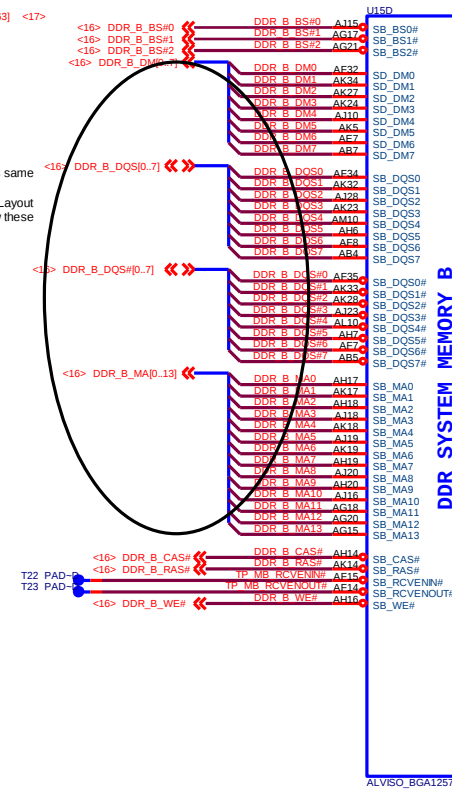
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This Symbol as same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.



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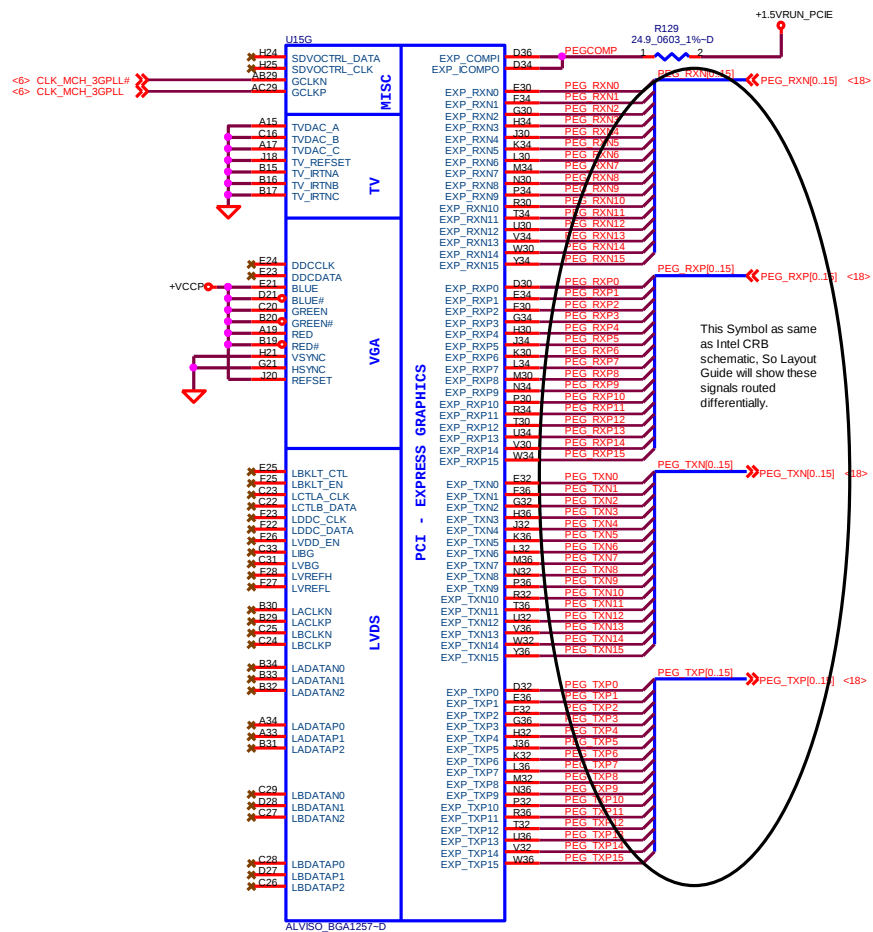
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Alviso(2 of 5)

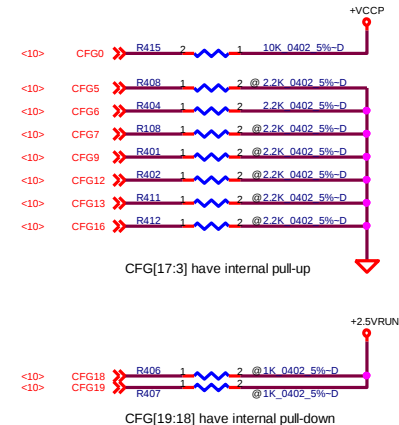
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CFG[2:0]	Refer to sheet 6 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II * High = DDR-I
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V



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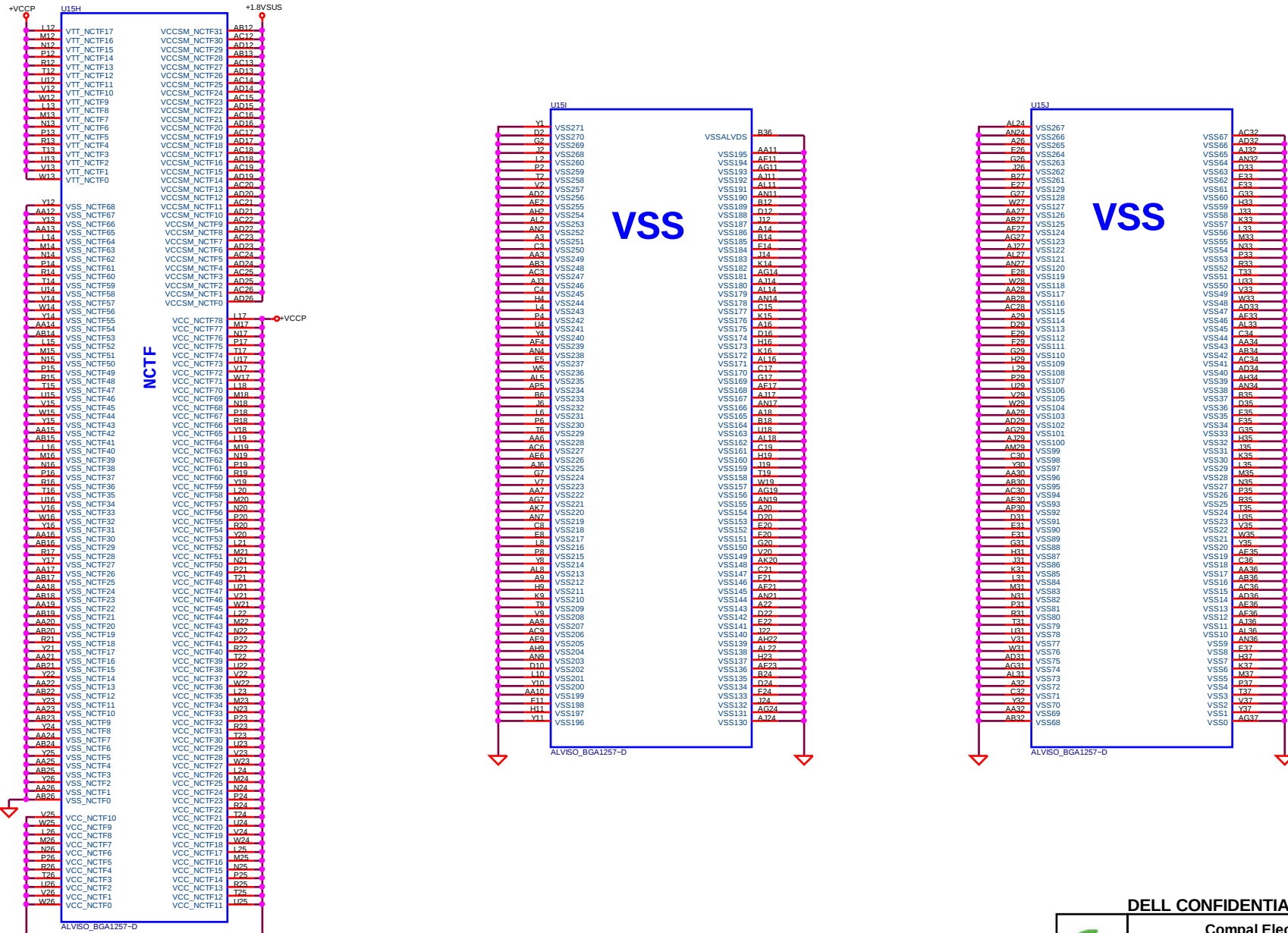
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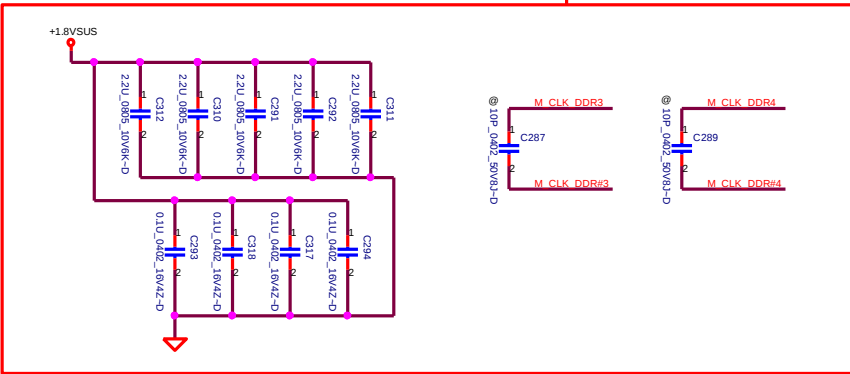


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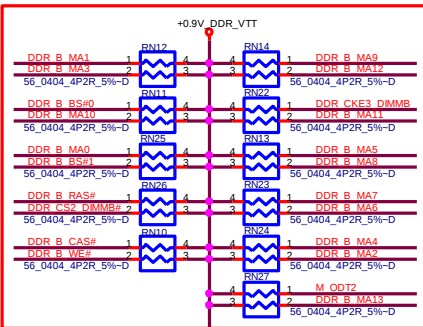
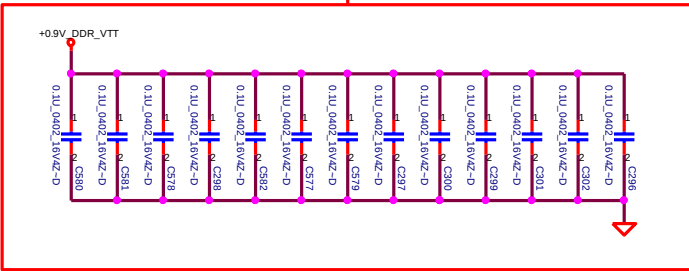
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<11> DDR_B_DQS[0..7] <<>>
 <11> DDR_B_D[0..63] <<>>
 <11> DDR_B_DM[0..7] <<>>
 <11> DDR_B_DQS[0..7] <<>>
 <11> DDR_B_MA[0..13] <<>>

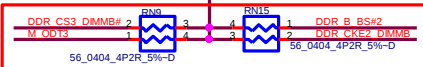
Layout Note:
Place near JDIM1



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT

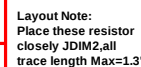
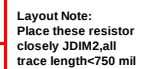
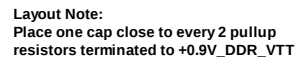
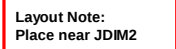


Layout Note:
Place these resistor
closely JDIM1,all
trace length<750 mil



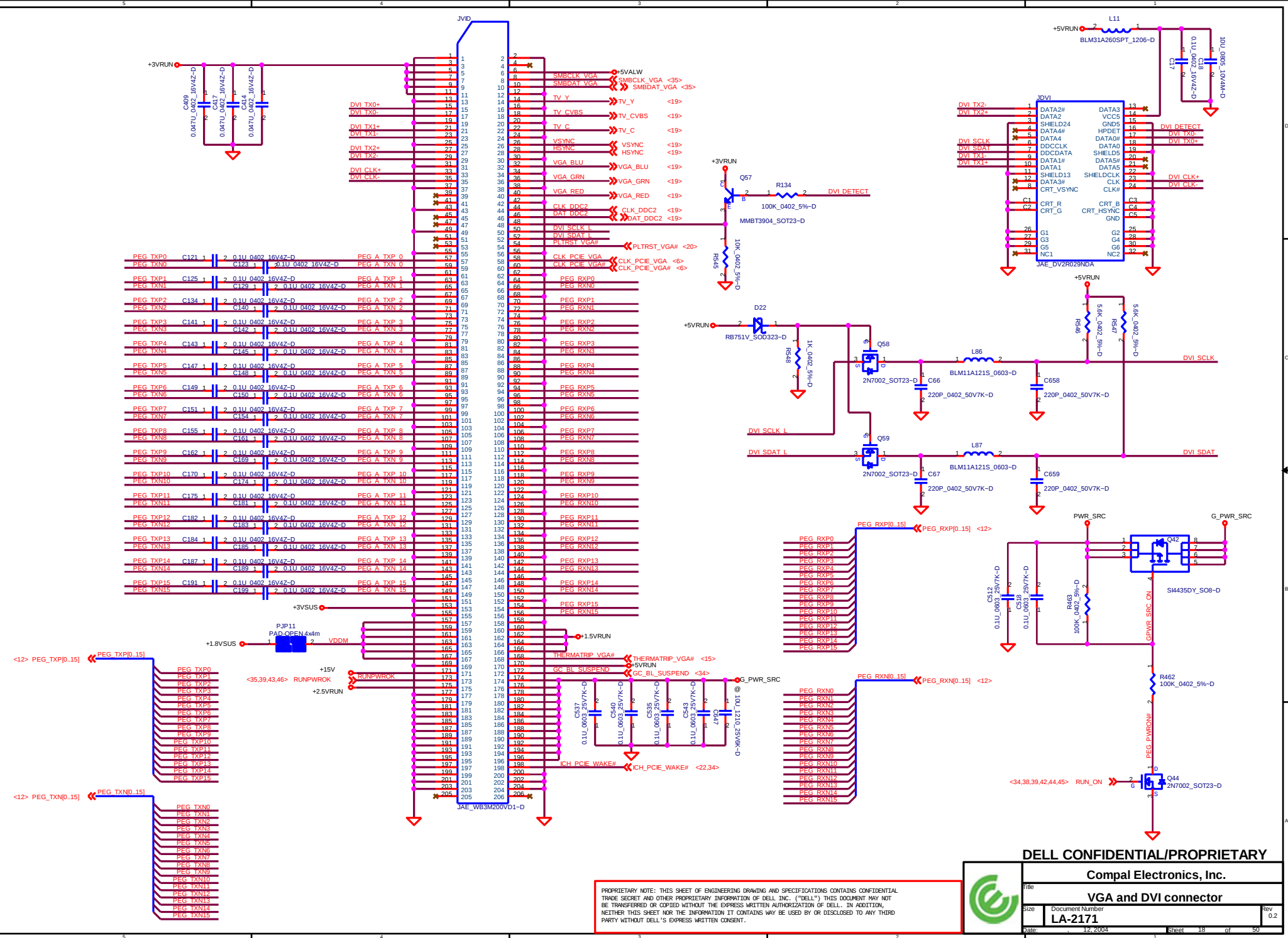
Layout Note:
Place these resistor
closely JDIM1,all
trace length
Max<1.3"

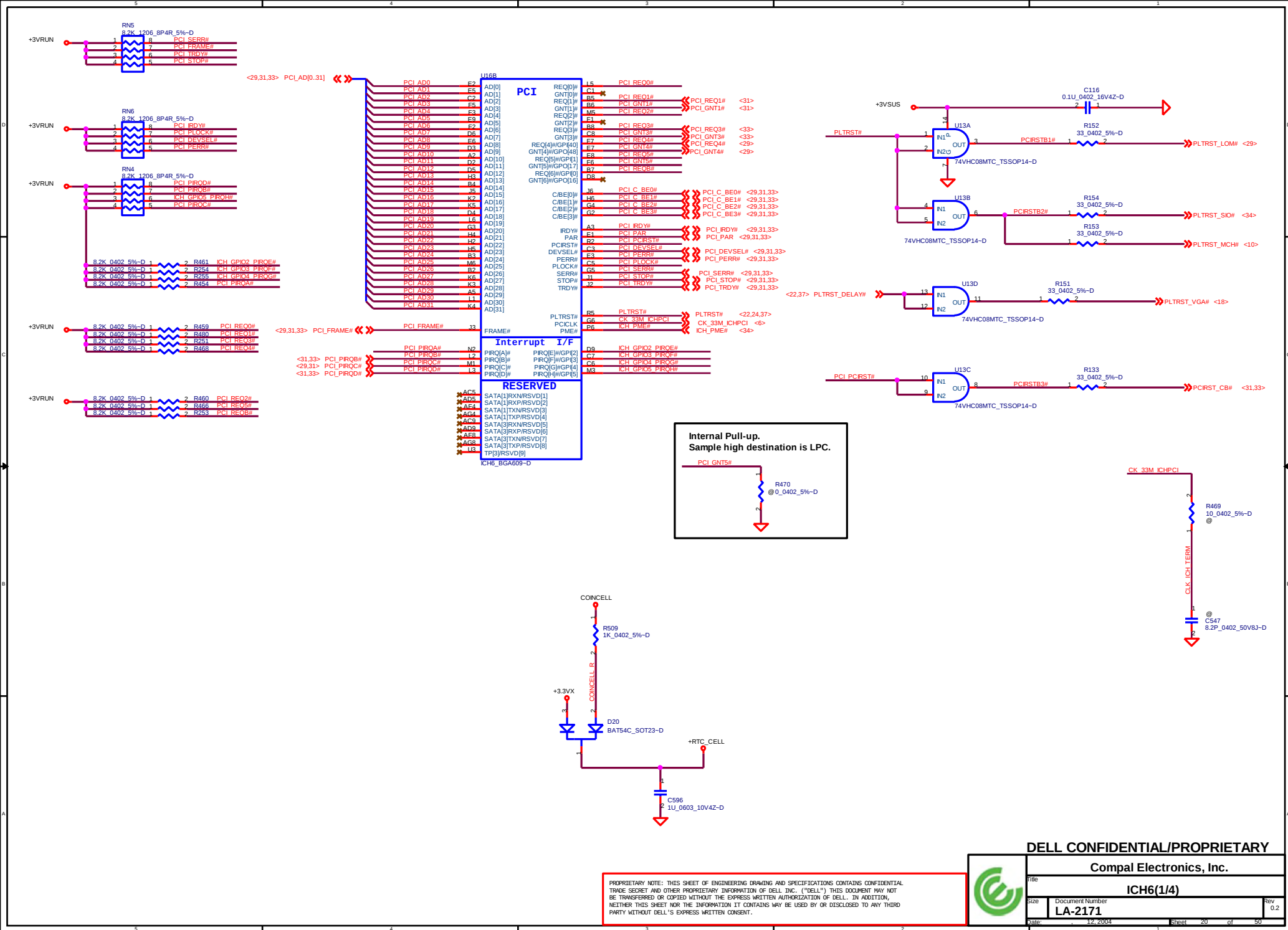




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The schematic diagram illustrates the internal circuitry and pin connections of the 885AB040_TQFP64-D package. The top section shows a crystal oscillator circuit with XTALIN and XTALOUT pins, a 25MHz_20P_1BK25000CK1A-D crystal, a 0.0402_5%_D capacitor, and a 33P_0402_50VB3-D capacitor. A 1M_0402_5%_D resistor (R494) is connected to the XTALOUT pin. The central section shows a parallel ATA interface with pins HD00-HD15, HDA0-HDA2, HCS0#, HCS1#, and HCS1#. The bottom section shows an UART interface with pins T40 PAD-D, T41 PAD-D, and HRES1#. The package is labeled 885AB040_TQFP64-D.

T4	T3	
0	0	20MHz
0	1	25MHz
1	0	30MHz
1	1	40MHz

Pin Name	Pin No.	Int. PU/PD	Settings
SATATEST0	33	PD	NC
SATATEST1	34	PU	NC
SATATEST2	35	PD	NC
SATATEST3	36	PD	1
SATATEST4	37	PD	NC
SATATEST5	38	PU	0
SATATEST6	39	PD	1
SATATEST7	40	PD	NC
CFG0	20	PD	NC
CFG1	19	PU	0
CFG2	18	PD	NC

Pinout diagram for the FOX-HH93223-5A REVERS-D module. The diagram shows a 44-pin connector with pins numbered 1 to 44. Pins 1-10 are labeled DE_HRESET#, DE_HD07, DE_HD08, DE_HD09, DE_HD05, DE_HD04, DE_HD03, DE_HD02, DE_HD01, and DE_HD00. Pins 11-20 are labeled DE_HD06, DE_HD02, DE_HD01, DE_HD00, DE_HD06, DE_HD07, DE_HD08, DE_HD09, DE_HD05, DE_HD04, DE_HD03, DE_HD02, DE_HD01, DE_HD00, DE_HD06, DE_HD07, DE_HD08, DE_HD09, DE_HD05, DE_HD04, DE_HD03, DE_HD02, DE_HD01, DE_HD00. Pins 21-30 are labeled DE_HD06, DE_HD07, DE_HD08, DE_HD09, DE_HD05, DE_HD04, DE_HD03, DE_HD02, DE_HD01, DE_HD00. Pins 31-40 are labeled DE_HD06, DE_HD07, DE_HD08, DE_HD09, DE_HD05, DE_HD04, DE_HD03, DE_HD02, DE_HD01, DE_HD00. Pins 41-44 are labeled DE_HD06, DE_HD07, DE_HD08, DE_HD09. The diagram also shows power supply connections: +5VHDD to pins 1, 21, 31, 41, and 43; +5VHDD to pins 2, 22, 32, 42, and 44. Ground connections are shown at pins 1, 21, 31, 41, and 43. The diagram includes a table of pin numbers and labels, and a list of components: R285 (510 Ohm 5% D), R296 (470 Ohm 5% D), R291 (10K Ohm 5% D), C407 (0.1uF 0.0025 10V/Z-D), C406 (0.1uF 0.0025 10V/Z-D), C405 (0.1uF 0.0025 10V/Z-D), and C404 (0.1uF 0.0025 10V/Z-D).

Pinout diagram of the IMC04 microcontroller. The diagram shows the following connections:

- Pin 1:** Connected to C350 (10k) and 47P_0402_5V0B3-D.
- Pin 2:** Connected to IDE_RST*MOD.
- Pin 3:** Connected to IDE_D07.
- Pin 4:** Connected to IDE_D08.
- Pin 5:** Connected to IDE_D05.
- Pin 6:** Connected to IDE_D04.
- Pin 7:** Connected to IDE_D03.
- Pin 8:** Connected to IDE_D02.
- Pin 9:** Connected to IDE_D01.
- Pin 10:** Connected to IDE_D00.
- Pin 11:** Connected to IDE_D07.
- Pin 12:** Connected to IDE_D08.
- Pin 13:** Connected to IDE_D05.
- Pin 14:** Connected to IDE_D04.
- Pin 15:** Connected to IDE_D03.
- Pin 16:** Connected to IDE_D02.
- Pin 17:** Connected to IDE_D01.
- Pin 18:** Connected to IDE_D00.
- Pin 19:** Connected to IDE_D07.
- Pin 20:** Connected to IDE_D08.
- Pin 21:** Connected to IDE_D05.
- Pin 22:** Connected to IDE_D04.
- Pin 23:** Connected to IDE_D03.
- Pin 24:** Connected to IDE_D02.
- Pin 25:** Connected to IDE_D01.
- Pin 26:** Connected to IDE_D00.
- Pin 27:** Connected to IDE_D07.
- Pin 28:** Connected to IDE_D08.
- Pin 29:** Connected to IDE_D05.
- Pin 30:** Connected to IDE_D04.
- Pin 31:** Connected to IDE_D03.
- Pin 32:** Connected to IDE_D02.
- Pin 33:** Connected to IDE_D01.
- Pin 34:** Connected to IDE_D00.
- Pin 35:** Connected to IDE_D07.
- Pin 36:** Connected to IDE_D08.
- Pin 37:** Connected to IDE_D05.
- Pin 38:** Connected to IDE_D04.
- Pin 39:** Connected to IDE_D03.
- Pin 40:** Connected to IDE_D02.
- Pin 41:** Connected to IDE_D01.
- Pin 42:** Connected to IDE_D00.
- Pin 43:** Connected to IDE_D07.
- Pin 44:** Connected to IDE_D08.
- Pin 45:** Connected to IDE_D05.
- Pin 46:** Connected to IDE_D04.
- Pin 47:** Connected to IDE_D03.
- Pin 48:** Connected to IDE_D02.
- Pin 49:** Connected to IDE_D01.
- Pin 50:** Connected to IDE_D00.

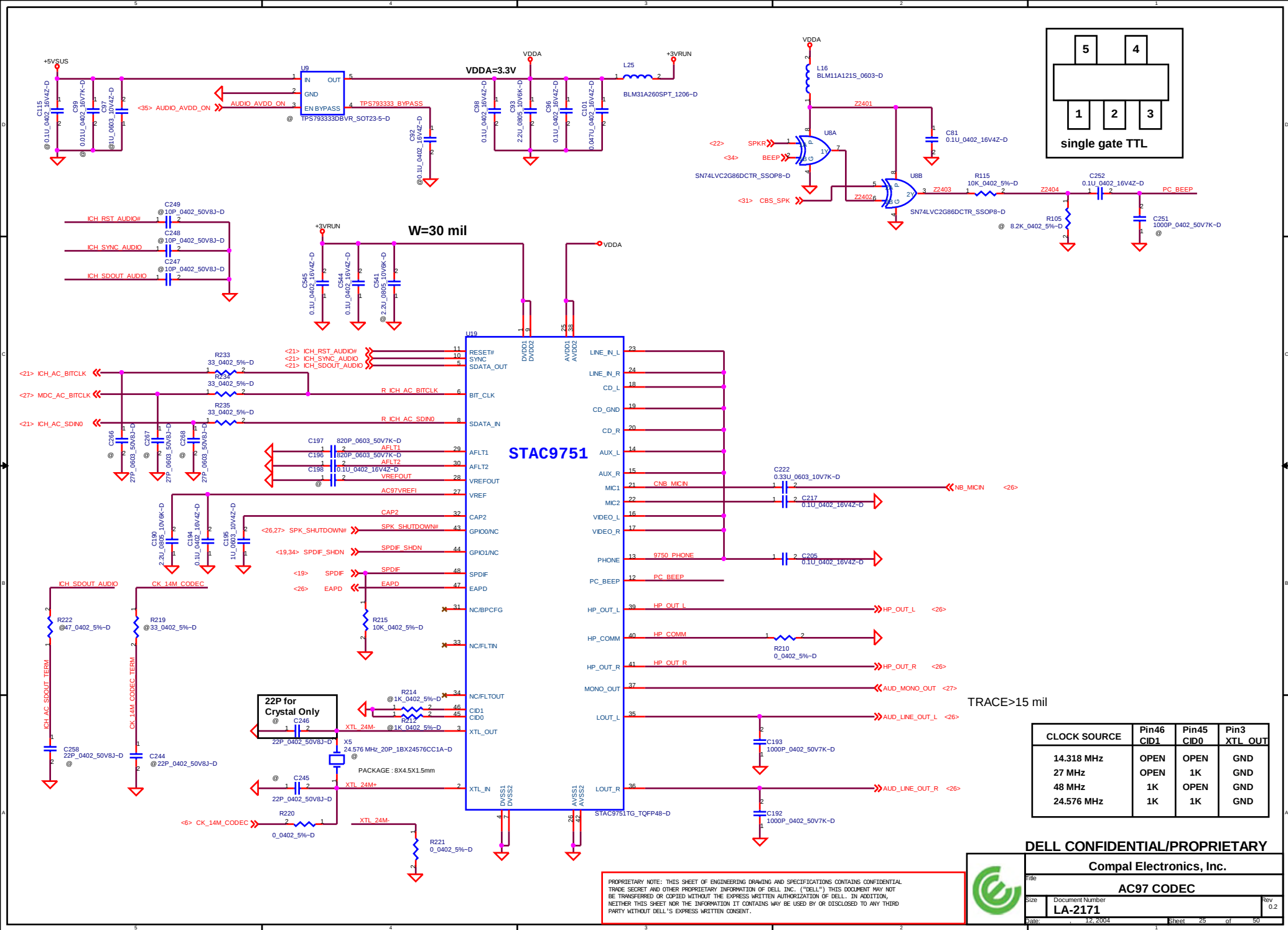
Additional connections and components shown:

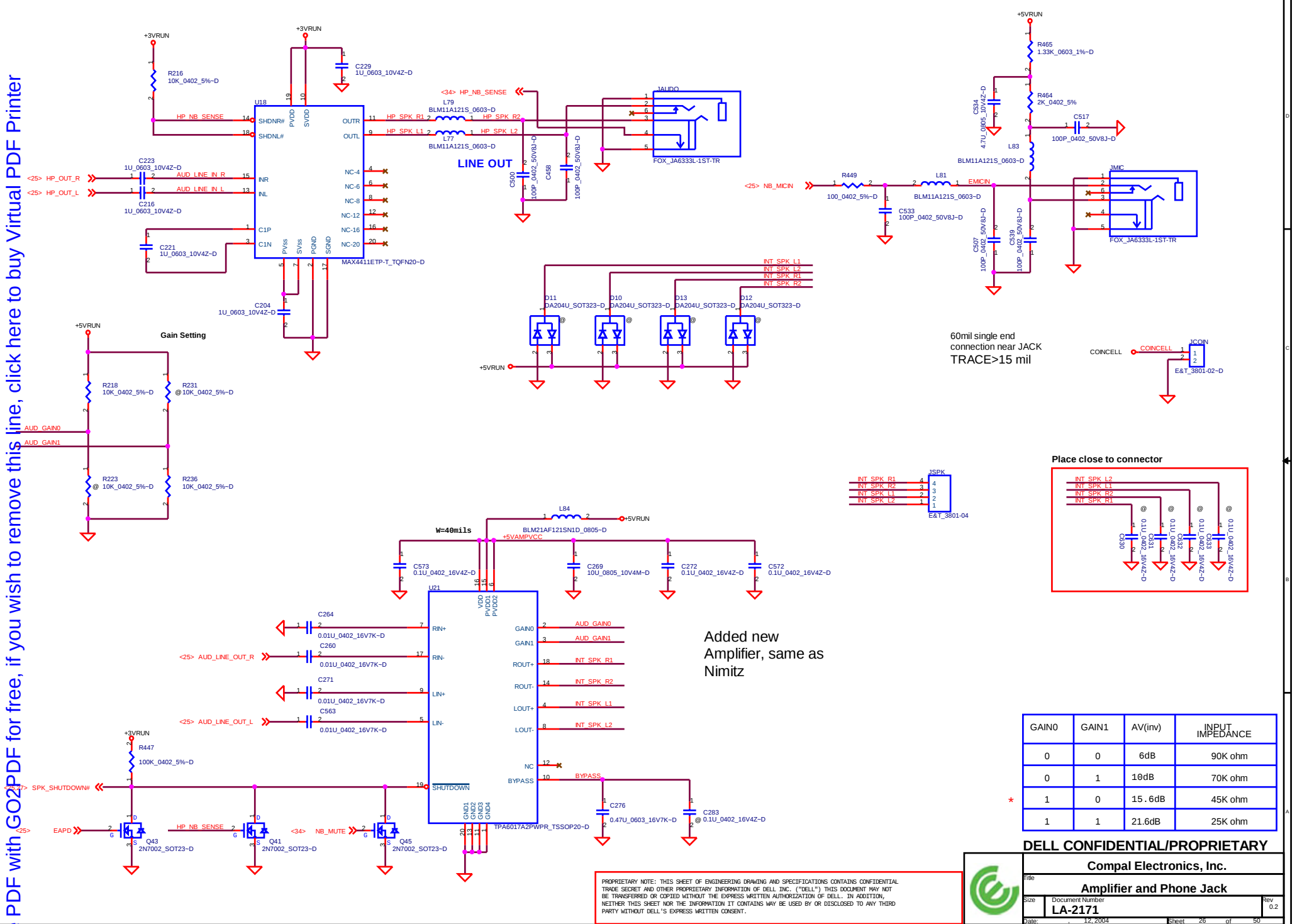
- Pin 19:** Connected to +5VMOD.
- Pin 20:** Connected to +5VMOD.
- Pin 21:** Connected to +5VMOD.
- Pin 22:** Connected to +5VMOD.
- Pin 23:** Connected to +5VMOD.
- Pin 24:** Connected to +5VMOD.
- Pin 25:** Connected to +5VMOD.
- Pin 26:** Connected to +5VMOD.
- Pin 27:** Connected to +5VMOD.
- Pin 28:** Connected to +5VMOD.
- Pin 29:** Connected to +5VMOD.
- Pin 30:** Connected to +5VMOD.
- Pin 31:** Connected to +5VMOD.
- Pin 32:** Connected to +5VMOD.
- Pin 33:** Connected to +5VMOD.
- Pin 34:** Connected to +5VMOD.
- Pin 35:** Connected to +5VMOD.
- Pin 36:** Connected to +5VMOD.
- Pin 37:** Connected to +5VMOD.
- Pin 38:** Connected to +5VMOD.
- Pin 39:** Connected to +5VMOD.
- Pin 40:** Connected to +5VMOD.
- Pin 41:** Connected to +5VMOD.
- Pin 42:** Connected to +5VMOD.
- Pin 43:** Connected to +5VMOD.
- Pin 44:** Connected to +5VMOD.
- Pin 45:** Connected to +5VMOD.
- Pin 46:** Connected to +5VMOD.
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- Pin 49:** Connected to +5VMOD.
- Pin 50:** Connected to +5VMOD.

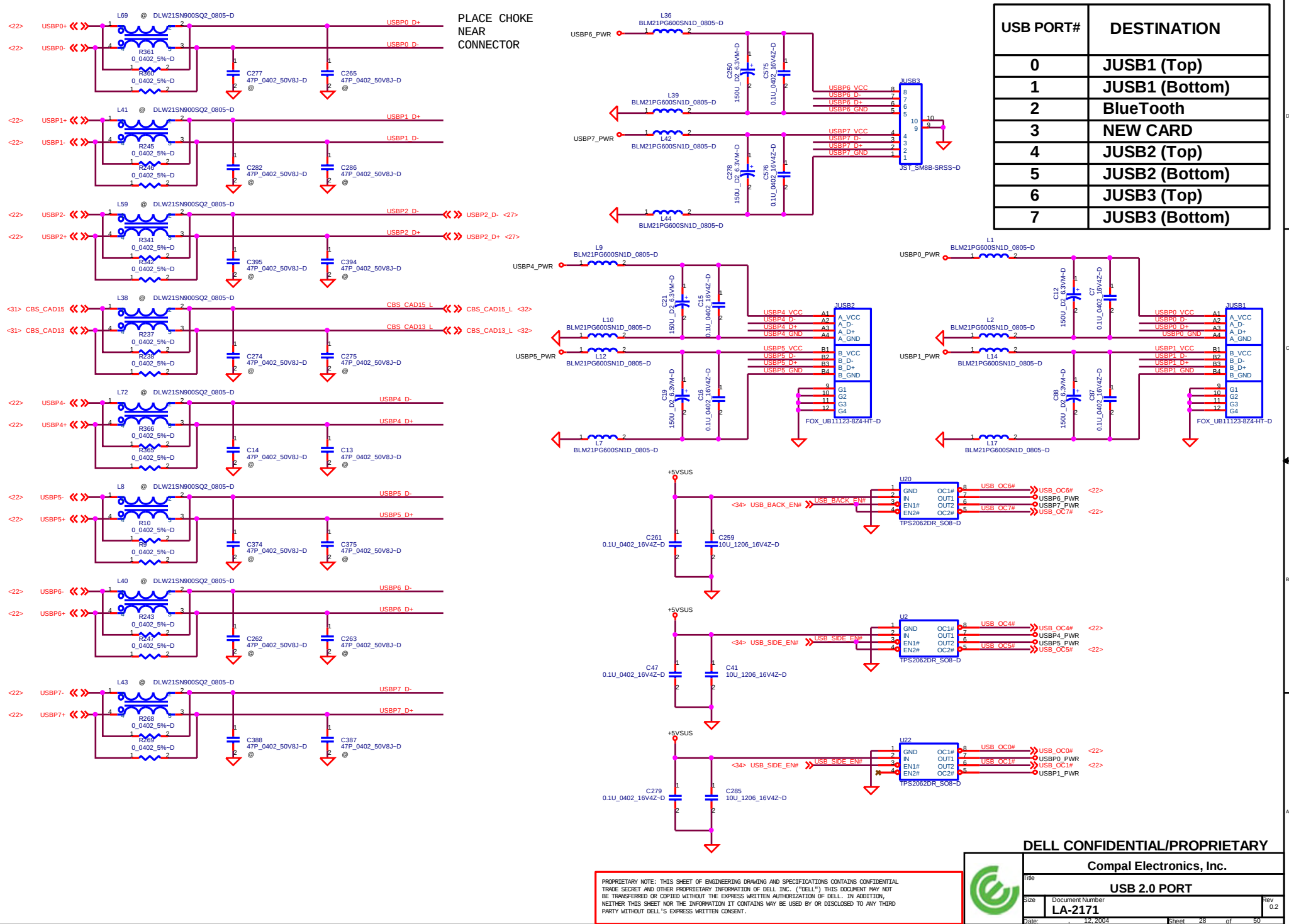
Layout Note: W=80 mils

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USB PORT#	DESTINATION
0	JUSB1 (Top)
1	JUSB1 (Bottom)
2	BlueTooth
3	NEW CARD
4	JUSB2 (Top)
5	JUSB2 (Bottom)
6	JUSB3 (Top)
7	JUSB3 (Bottom)

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USB 2.0 PORT

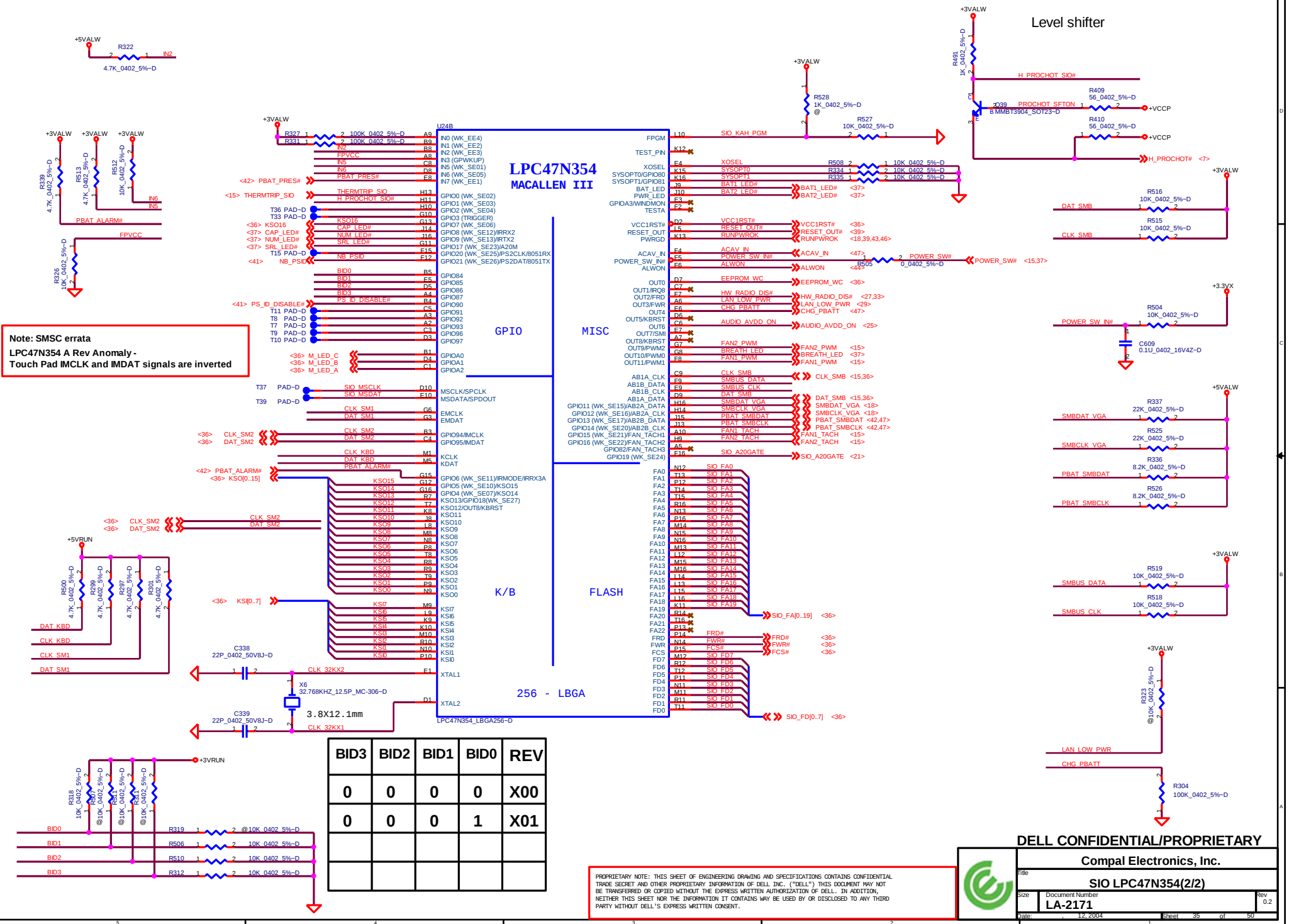
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Note: SMSC errata
LPC47N354 A Rev Anomaly -
Touch Pad IMCLK and IMDAT signals are inverted

BID3	BID2	BID1	BID0	REV
0	0	0	0	X00
0	0	0	1	X01



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SIO LPC47N354(2/2)

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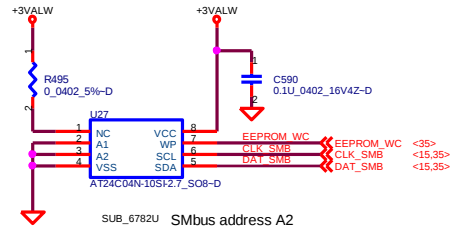
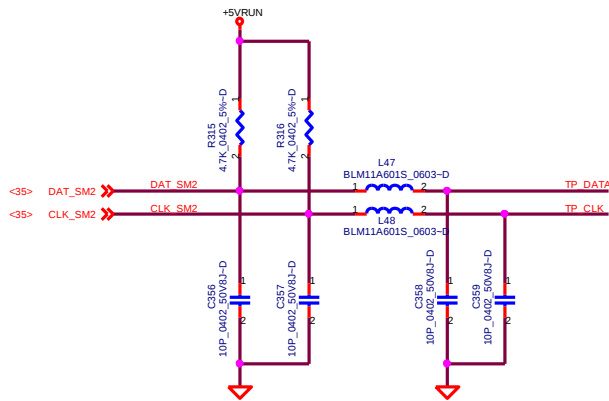
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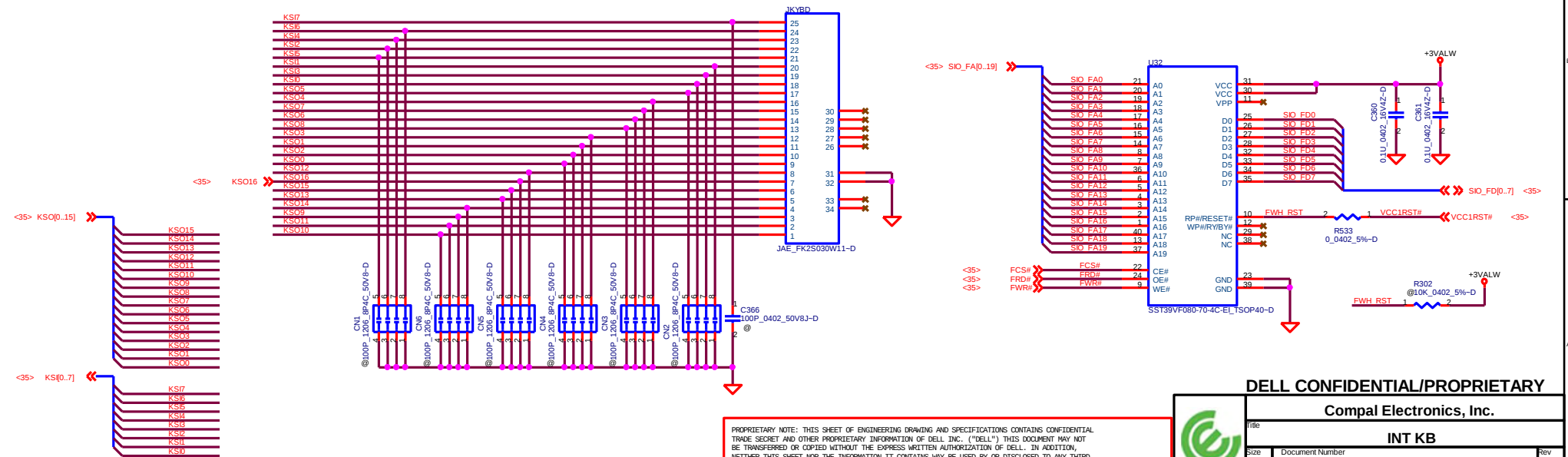
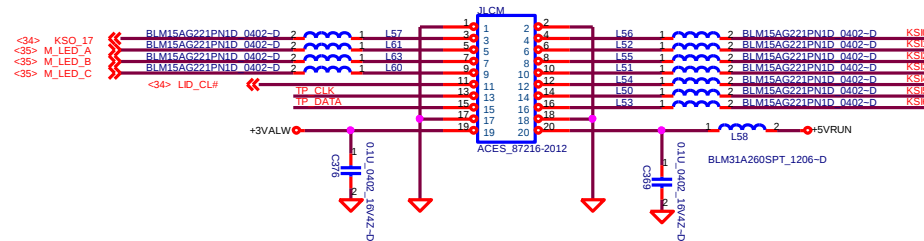
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Note: SMSC errata
LPC47N354 A Rev Anomaly - Touch Pad IMCLK and IMDAT signals are inverted



LCM & Direct play SW & T PAD



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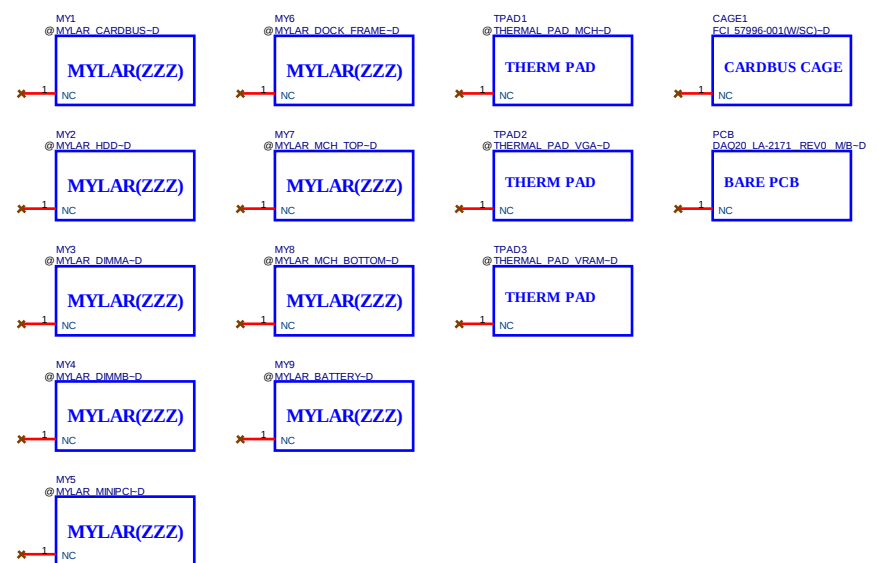
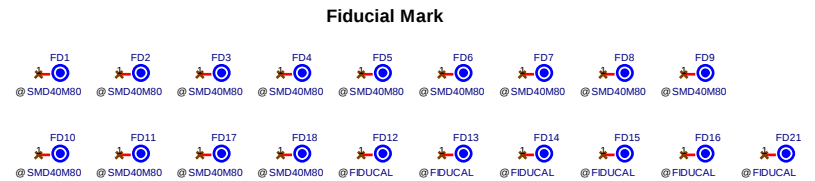
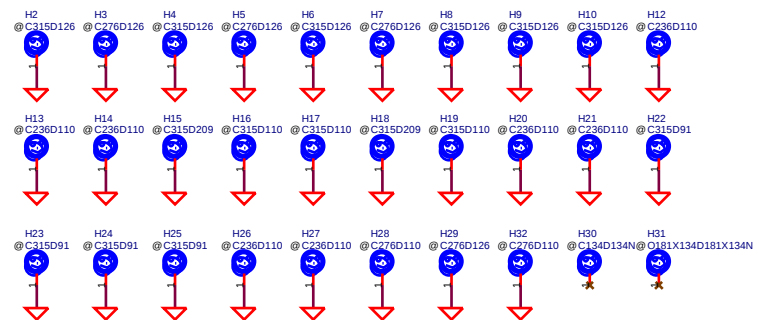
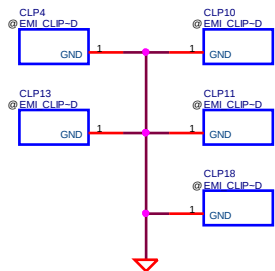
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POWER CONTROL

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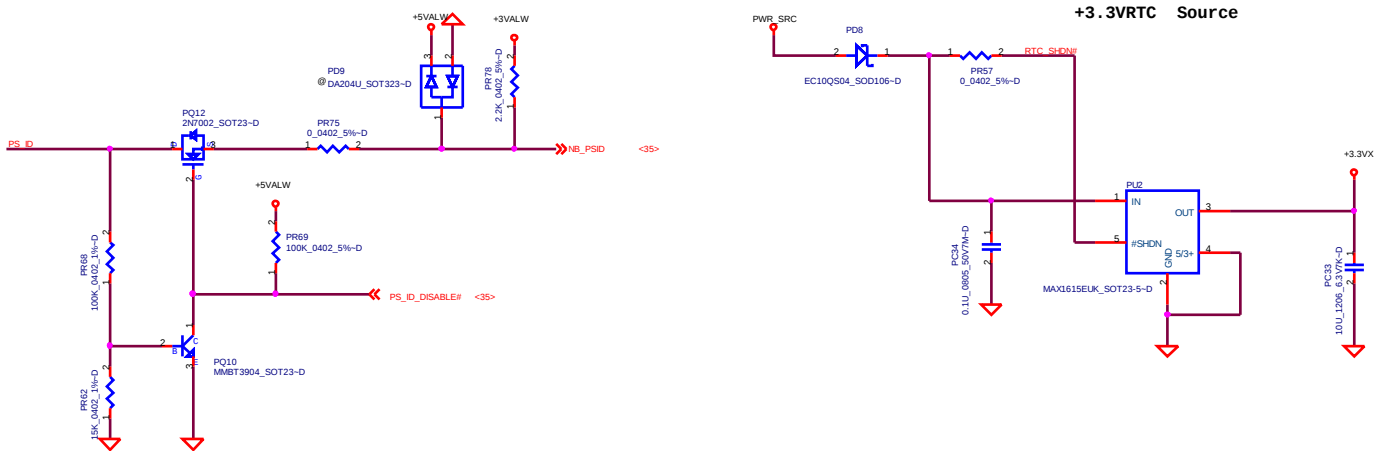
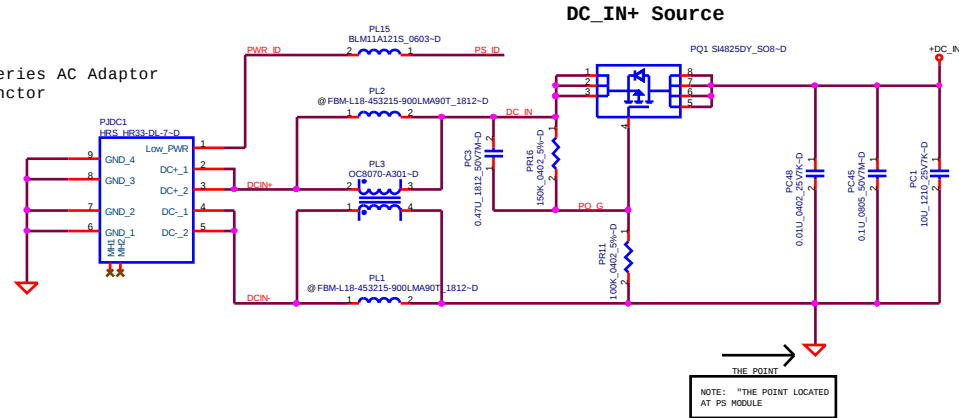
PAD and Standoff



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Z-series AC Adaptor
Connctor

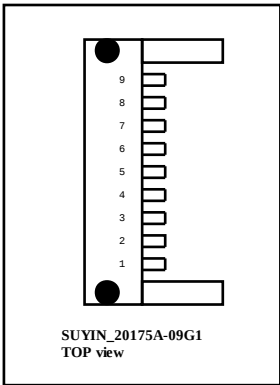
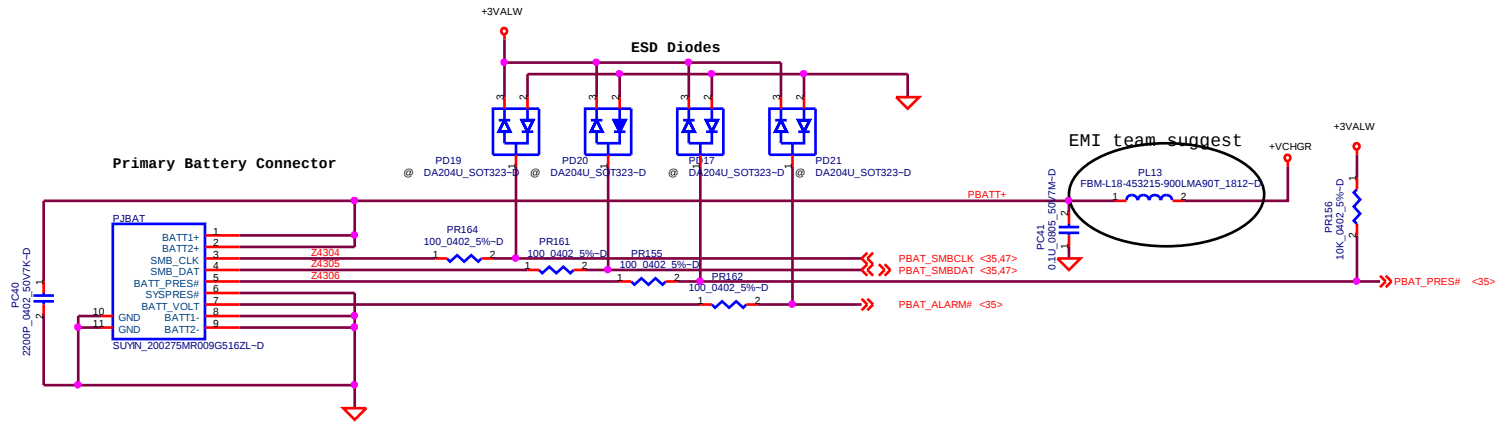


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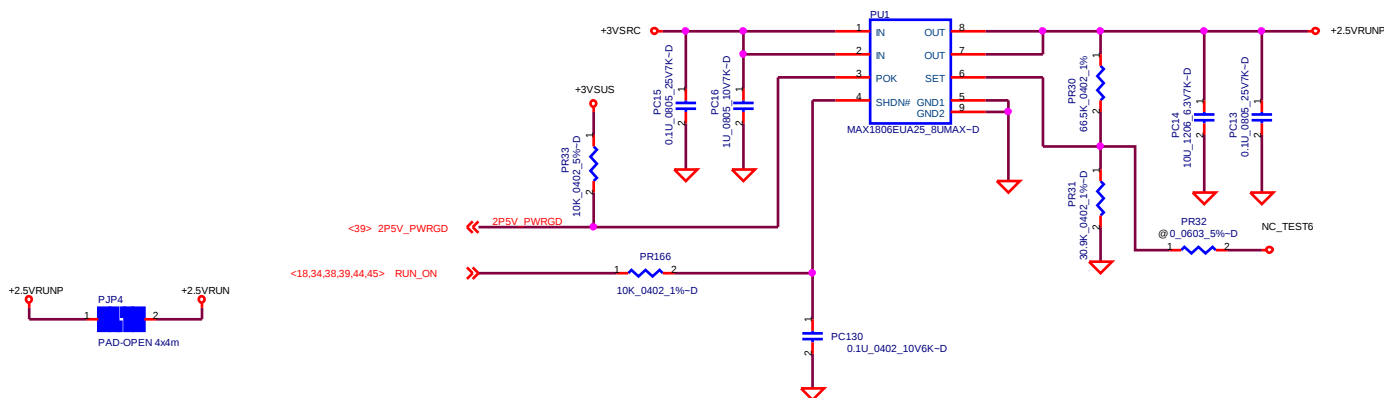


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+2.5V RUN $R1=R2 * (Vo / 0.8 - 1)$, $R2:25K-100K$.



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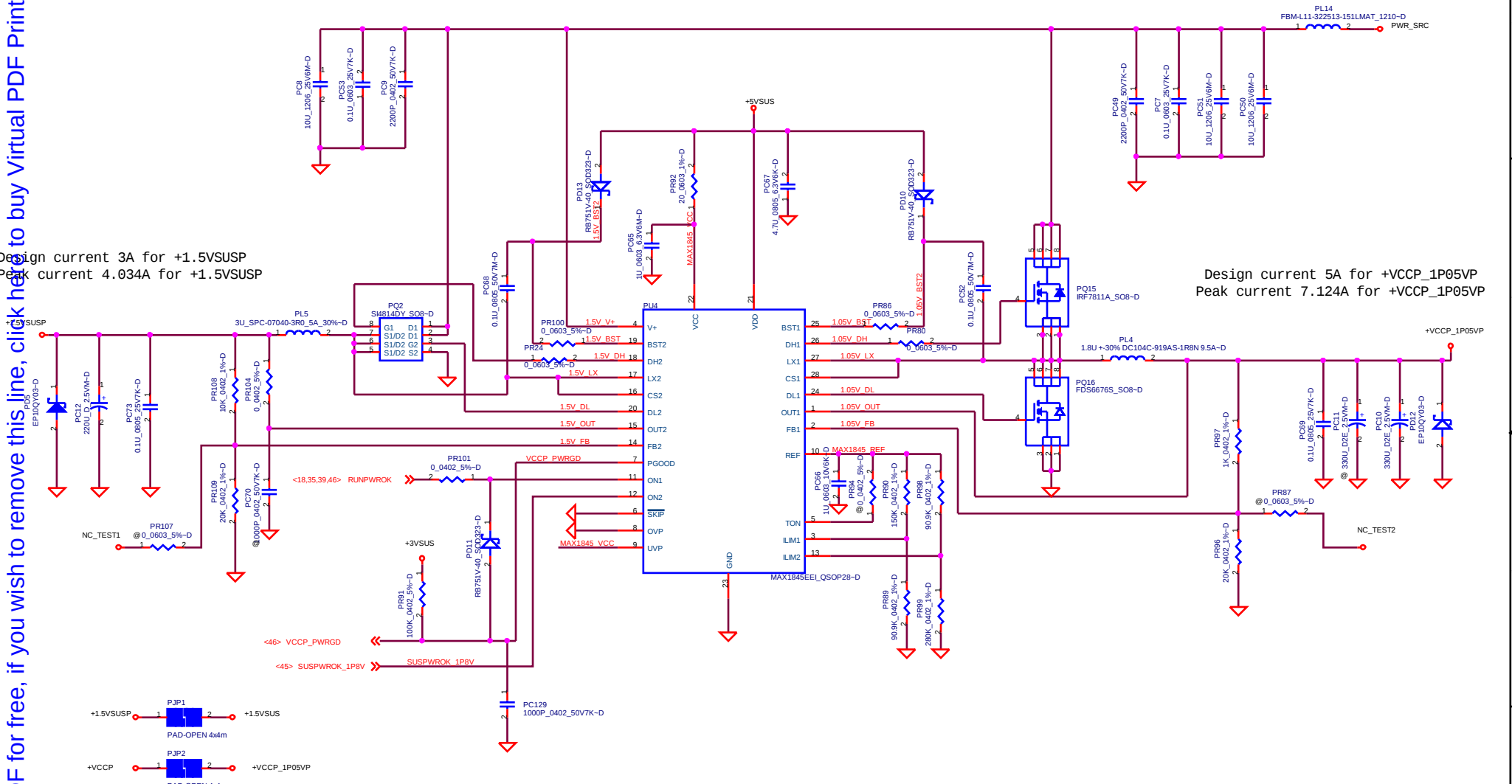
Battery Conn./+2.5V

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+1.5VSUSP / +VCCP_1P05VP

Design current 3A for +1.5VSUSP
Peak current 4.034A for +1.5VSUSP

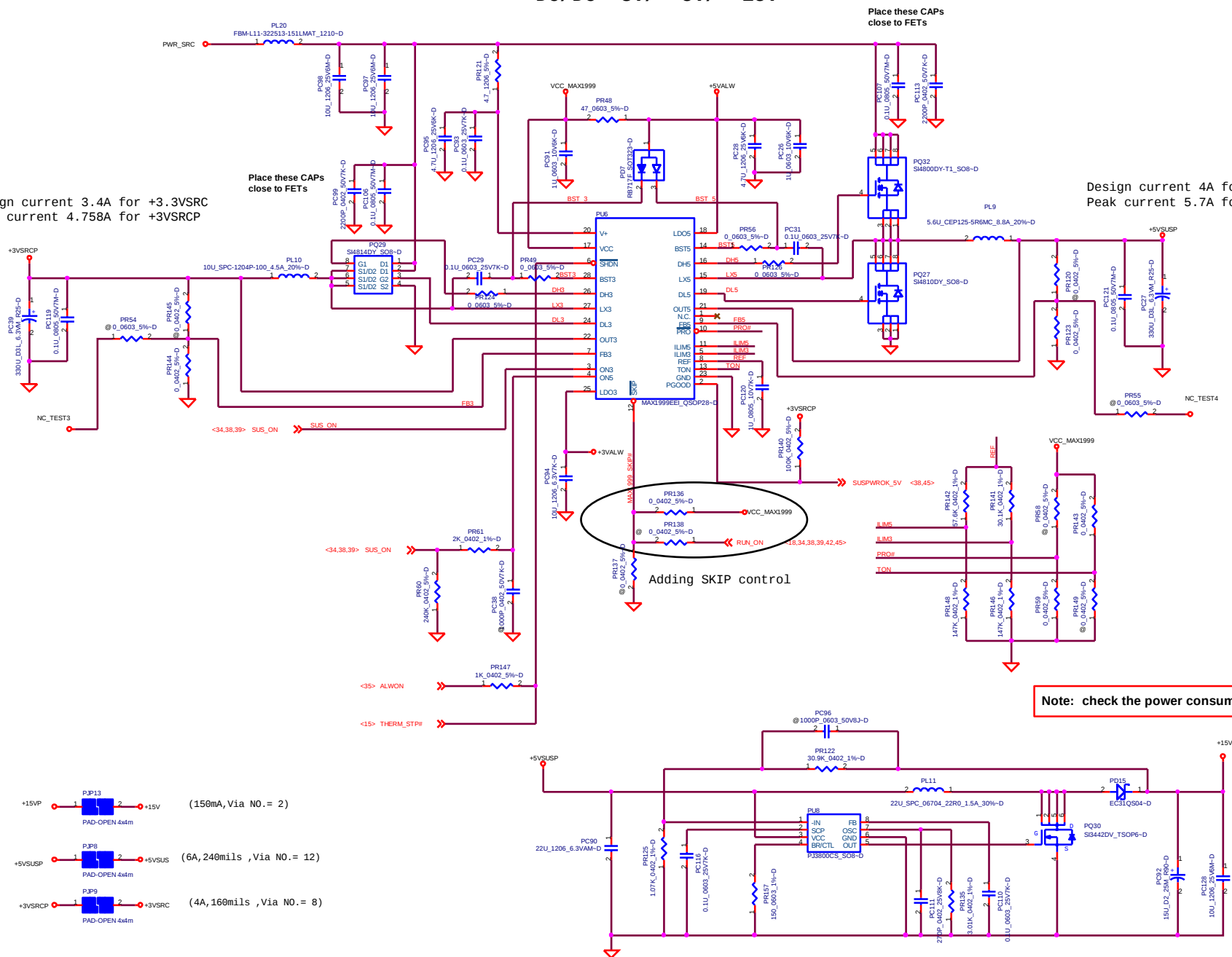
Design current 5A for +VCCP_1P05VP
Peak current 7.124A for +VCCP_1P05VP



DC/DC +3V/ +5V/ +15V

Design current 3.4A for +3.3VSRCP
Peak current 4.758A for +3VSRCP

Design current 4A for +5VSUS
Peak current 5.7A for +5VSUSP



- +15VP (150mA, Via NO.= 2)
- +5VSUSP (6A, 240mils, Via NO.= 12)
- +3VSRCP (4A, 160mils, Via NO.= 8)

Note: check the power consumption of +15V plane

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gn current 7A for +1.8V_SUSP
current 10.1A for +1.8VSUSP

+1.8VSUSP

3300µD 2.5VW-D

PC24

3300µD 2.5VW-D

PC23

3300µD 2.5VW-D

PC25

0.11µ 0.063 25V7K-D

PC79

100µ 1206 25V6W-D

PC78

100µ 1206 25V6W-D

0.11µ 0.063 25V7K-D

PC81

2200P 0402 50V7K-D

PL17

2.2µ SPC-1205P-2R2B_13A_30W-D

PL8

2.2µ SPC-1205P-2R2B_13A_30W-D

PR116

274K 0603 1%W-D

PR117

@ 0_0603 5%W-D

NC_TESTS

PR118

174K 0402 1%W-D

P3P6

PAD-OPEN 4x4mm

P3P7

PAD-OPEN 4x4mm

+1.8VSUSP

+1.8VSUS

(8A, 320mils, Via N0.=16)

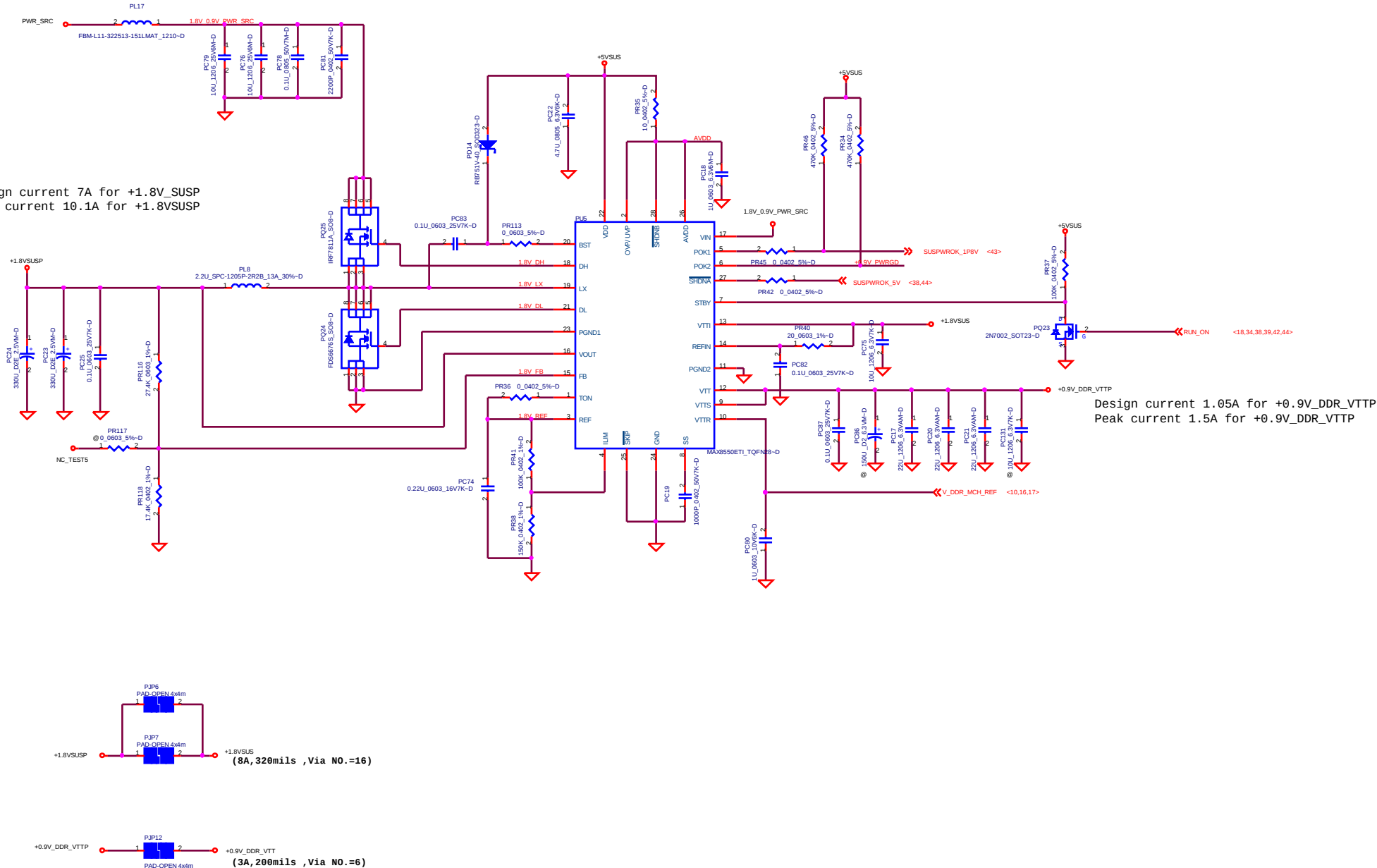
+0.9V_DDR_VTTP

P3P12

PAD-OPEN 4x4mm

+0.9V_DDR_VTTP

(3A, 200mils, Via N0.=6)



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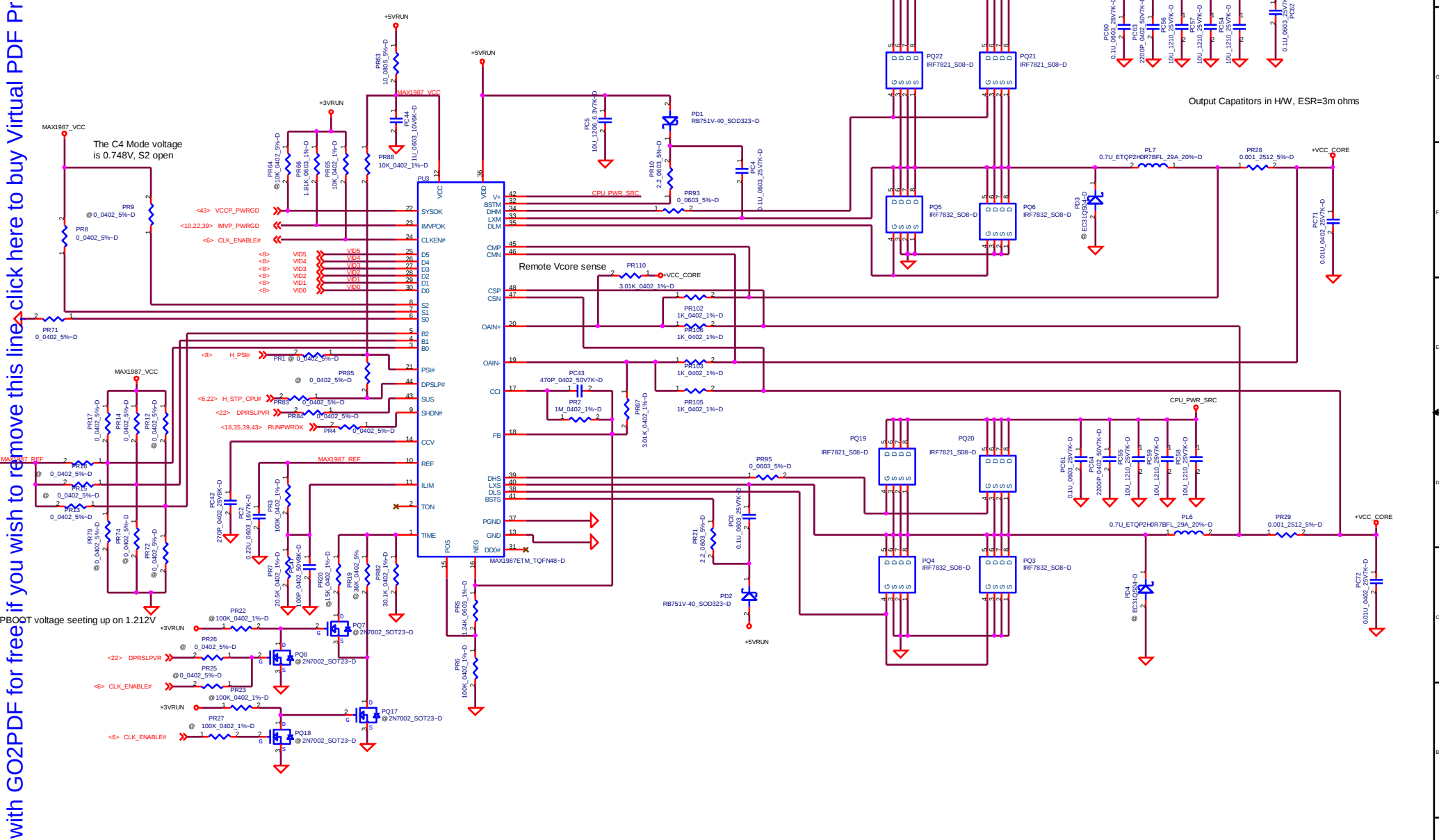
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File	+1.8VSUSP/ +0.9V DDR VT
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V I D							Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V	
0	1	1	1	1	0	1.484	
0	1	1	0	0	1	1.308	
1	0	1	1	1	1	0.956	
1	1	1	1	0	0	0.748	



Change PR62 to 30.1k. Delete PR22/PQ8/PQ17/PQ7/PQ18/PR20/PR26/PR23
PR19 for BANIAS and DOTHAN
PR22/PQ8/PQ17/PQ7/PQ18/PR20/PR26/PR23 and PR19 are only for YONAH CPU.
TRANSITION TIMING:
(a) START-UP and SHUTDOWN (SUS=LOW, RUNPWROK=LOW): 2mV/us
(b) ENTER SUSPEND (SUS=HIGH, RUNPWROK=HIGH): 8.6mV/us
(c) EXIT SUSPEND (SUS=LOW, RUNPWROK=HIGH): 24.7mV/us

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+VCORE

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Date

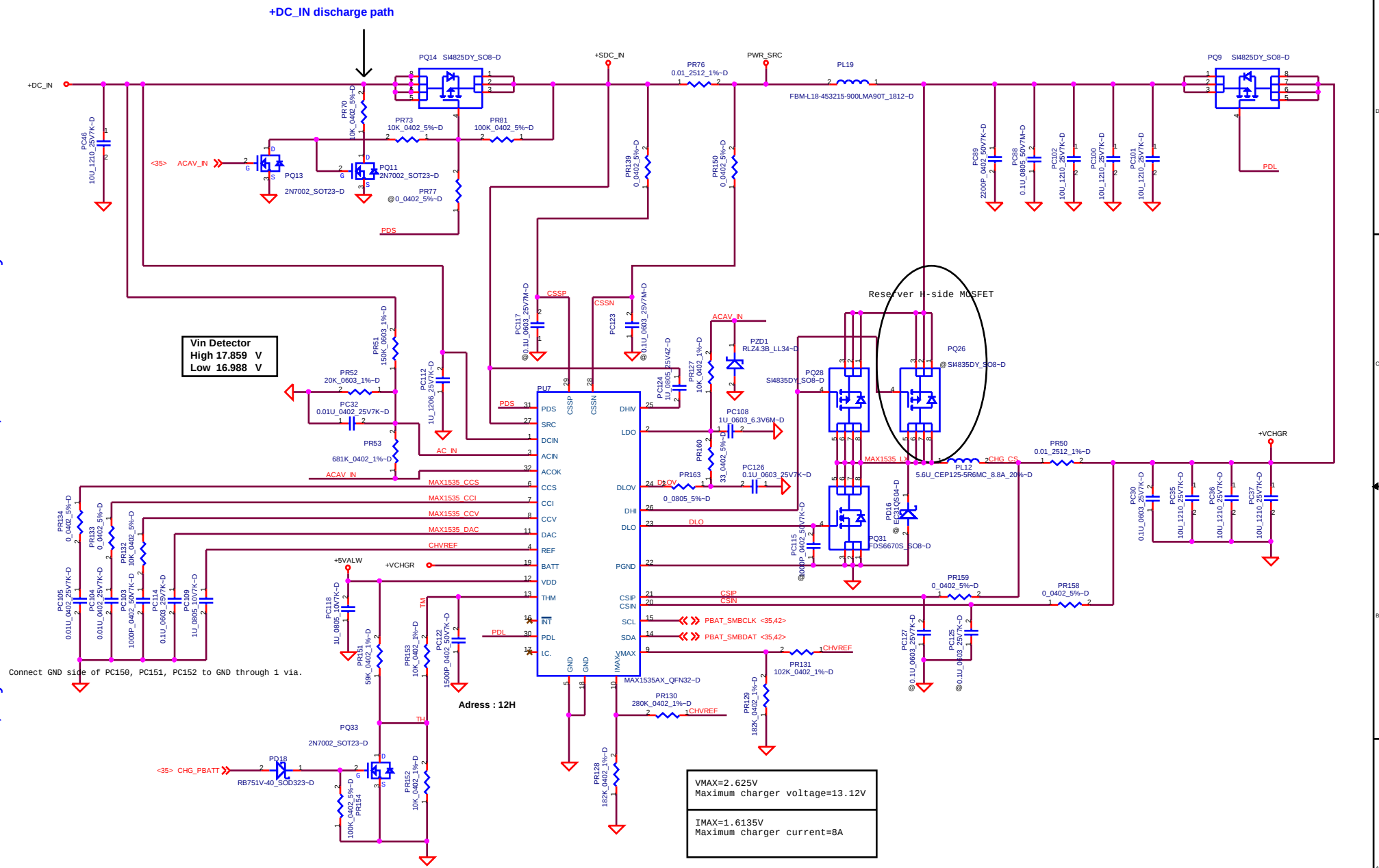
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	31&32	Cardbus	10/15/03	Dell	Change cardbus controller to TI PCI4515.	Change U162	M00
2	18	VGA/B & DVI CONN.	10/16/03	Dell	Add DVI connector.	Add JDVI	M00
3	25	SATA Bridge	10/16/03	Dell	Add SATA to PATA circuit.	Add page 25	M00
4	28	Subwoofer	10/16/03	Dell	Add subwoofer circuit.	Add page 28	M00
5	40	LED/B	10/16/03	Dell	Removed IR circuit.	Delete U52	M00
6	27	Amplifier & Phone JACK	10/17/03	Dell	Removed internal MIC circuit.		X00
7	31&32	LOM	10/17/03	Dell	Change LAN controller (U164) from 5751M to 4401. Add pop option for the 5705 like Kapalua/Lindbergh board.		X00
8	33	Cardbus	10/17/03	Dell	Depop 1394 choke, L142 and pop bypass resistors, R1025, R1026, R1027, R1028		X00
9	1	Cover page	10/17/03	Dell	Change schematic revision from M00 to X00.		X00
10	40	PAD & ME & spare parts	01/07/04	Compal	For EMI requirement.	Pop CLP4,5,10,11,13 and depop CLP18	X01
11	22	ICH6(3/4)	01/08/04	Dell	Connected PCIE channel 1 to TV-Tuner connector.	Delete T4,T5,T29,T30 and add C661,C662	X01
12	37	LED/B & TV TUNER	01/08/04	Dell	Connected TV tuner signals.	Add C663,C664	X01
13	40	PAD & ME & spare parts	01/08/04	Compal	Added ME standoff.	Pop H12,H13,H14,H17,H20,H21,H26,H27	X01
14	32	CardBus(2/2)	01/28/04	Compal	Fixed SD card issue.	The pin11 of JSD need to be connected to GND and pin 12 need to be connected to U17 pin b3.	X01
15	10	Alviso(1/5)	01/28/04	Dell	From Intel Message.	Change C124 from 220pF to 0.1uF and move capacitor as close as possible to the HVREF pin (pin J11 of U15).	X01
16	6	Clock Generator	01/28/04	Dell	Per Intel and ICS recommendation.	Connect the SATA clock to SRC4 and connect the VGA clock to SRC1.	X01
17	7&10	Dothan(1/2) & Alviso(1/5)	01/28/04	Dell	Per the Intel Check list 1.301	Change R397 and R114 to 75 ohm.	X01
18	36	Internal K/B & LCM CONN.	01/29/04	Compal	The BIOS debug connector is for bring up only.	Delete JDEBUG.	X01
19	1	Cover page	01/29/04	Compal	Change schematic revision from X00 to X01.		X01
20	35	Macallen(2/2)	01/29/04	Compal	Board ID X01.	Pop R318 and depop R319.	X01
21	34	Macallen(1/2)	01/29/04	Compal	Reserved a inverter for serial port debug.	Add U36 and T13.	X01
22	40	PAD & ME & spare parts	01/30/04	Compal	This clip have interferenced with screw hole.	Delete CLP5 and add H32	X01
23	37	LED/B & TV TUNER	02/02/04	Compal	The indicative LED of HDD doesn't work well.	Remove R12 and connect the pin3 of Q2 to +3VRUN.	X01
24	37	LED/B & TV TUNER	02/04/04	Dell	Changed JTUNR pin definitions	Added PCIRST#, CLK_PCIE_TV/TV# signals	X01
25	6	Clock Generator	02/04/04	Dell	Added PCIE clock connection to JTUNR	Added R551, R552, R553, R554	X01

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Changed-List History



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Version Change List (P. I. R. List)

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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	49	Charger selector	2003/10/14	Compal	Modify charger selector circuit.	Need to discuss.	0.0
2	42	PSID & +3VX	2003/10/15	Compal	Modify PSID circuit same as Nimitas. And add current limit resistor on RTC charger.	Add ESD solution on PSID, and limit RTC charge current.	0.0
3	44	+15VP	2003/11/4	Compal	+15VP current rating is not enough for subwoofer	Use MB3800 Boost IC to genearte +15VP from +5VSUSP	X00
4	47	Charger	2003/11/5	Compal	That has leakage current from battery goes through PQ22 and PQ44 to DC_IN.	Move Adaptor current sense PR144 after PQ24 and before PWR_SRC. That is same as Nimitaz.	X00
5	44	+15VP	2003/12/11	Compal	Test +15VP on Demon board.The output ripple voltage is large and improve efficiency.	Add PC128 10U_1206_25V,change PQ30 from SI2302DS to SI3442DV, change PR157 form 392_0603_1% to 150_0603_1%, no-pop PC96.	M00
6	45	+1.8VSUSP	2004/2/1	DELL	Change DDRII DC-DC solution for cost down.	Using MAXIM MAX8550 .	X01
7	43	+VCCP_1P05VP	2004/2/1	Compal	VCCP_1p05VP has two 330uF caps on it(PC10, PC11), Laguna only has one. Do we need two?	Can de-populate PC11,and test is OK.	X01
8	45	+1.8VSUSP	2004/2/5	Compal	Voltage divider setting is error, the FB regulate on 0.7V.	Change PR116 from 45.3K_0402_1% to 27.4K_0603_1%. Change PC22 from 1U_0603_6.3V to 4.7U_0805_6.3V	X01
9	46	+VCC_CORE	2004/2/5	Compal	Choke height is over mechanical height limitation	Change PL6 and PL7 from 0.6U_HK_AE26A0R6 to 0.7U_ETQP2H0R7BFL.	X01
10	46	+VCC_CORE	2004/2/6	Compal	EMI broad band test is over 1~2 db	Change PR10 and PR21 from 0_0603_5% to 2.2_0603_5%.	X01
11	41	PS_ID	2004/2/11	DELL	Open issue #60 Change PS_ID pullup resistor, PR78, from 1.5K to 2.2K	Change PR78 from 1.5K_0603_1% to 2.2K_0402_5%.	X01
12	45	+0.9V_DDR_VTTP	2004/2/11	DELL	Open issue#63 Please add a 10uf, 1206 package capacitor at the output of PU5 pin 12, +0.9V_DDR_VTTP.	Add and reserve PC131 10U_1206_6.3V7K.	X01
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