DJ2 Montevina UMA Schematics Document

uFCPGA Mobile Penryn

Intel GM45+ICH9M

2010-06-02

REV : X00

```
DY      : Nopop Component
HDMI    : Pop for HDMI
GIGA    : Pop for GIGA LAN
10/100  : Pop for 10/100 LAN
```

<Core Design>

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Title: Cover Page		
Size: A3	Document Number: DJ2 Montevina UMA	Rev: X00
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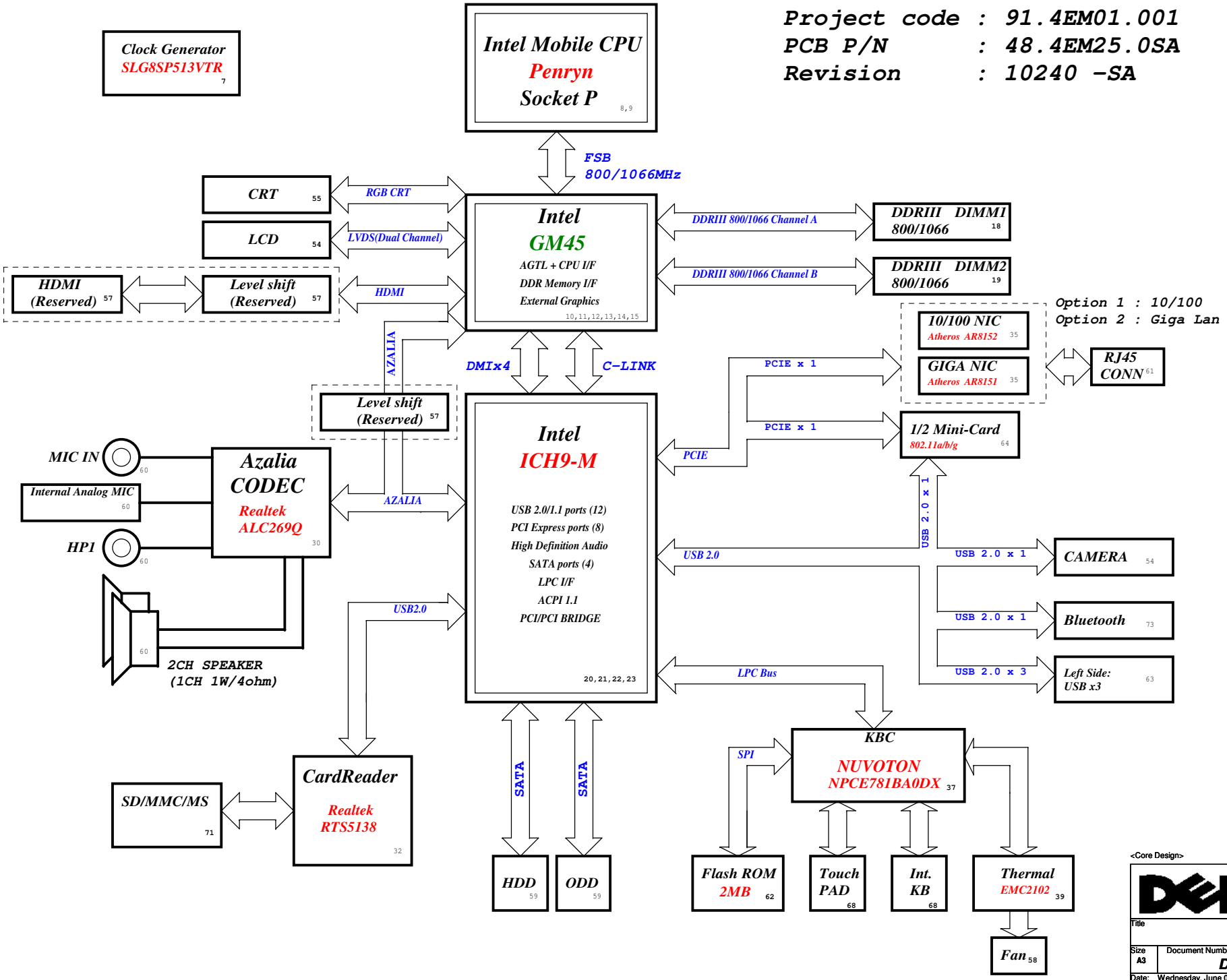
DJ2 Montevina UMA Block Diagram

Project code : 91.4EM01.001
PCB P/N : 48.4EM25.0SA
Revision : 10240 -SA



CPU DC/DC TPS51620 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP

SYSTEM DC/DC TPS51125 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW

SYSTEM DC/DC TPS51116 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

MAXIM CHARGER BQ24745 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN

PCB LAYER

L1: Top
L2: GND
L3: Signal
L4: Signal
L5: VCC
L6: Bottom

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Title: Block Diagram

Size	Document Number	Rev
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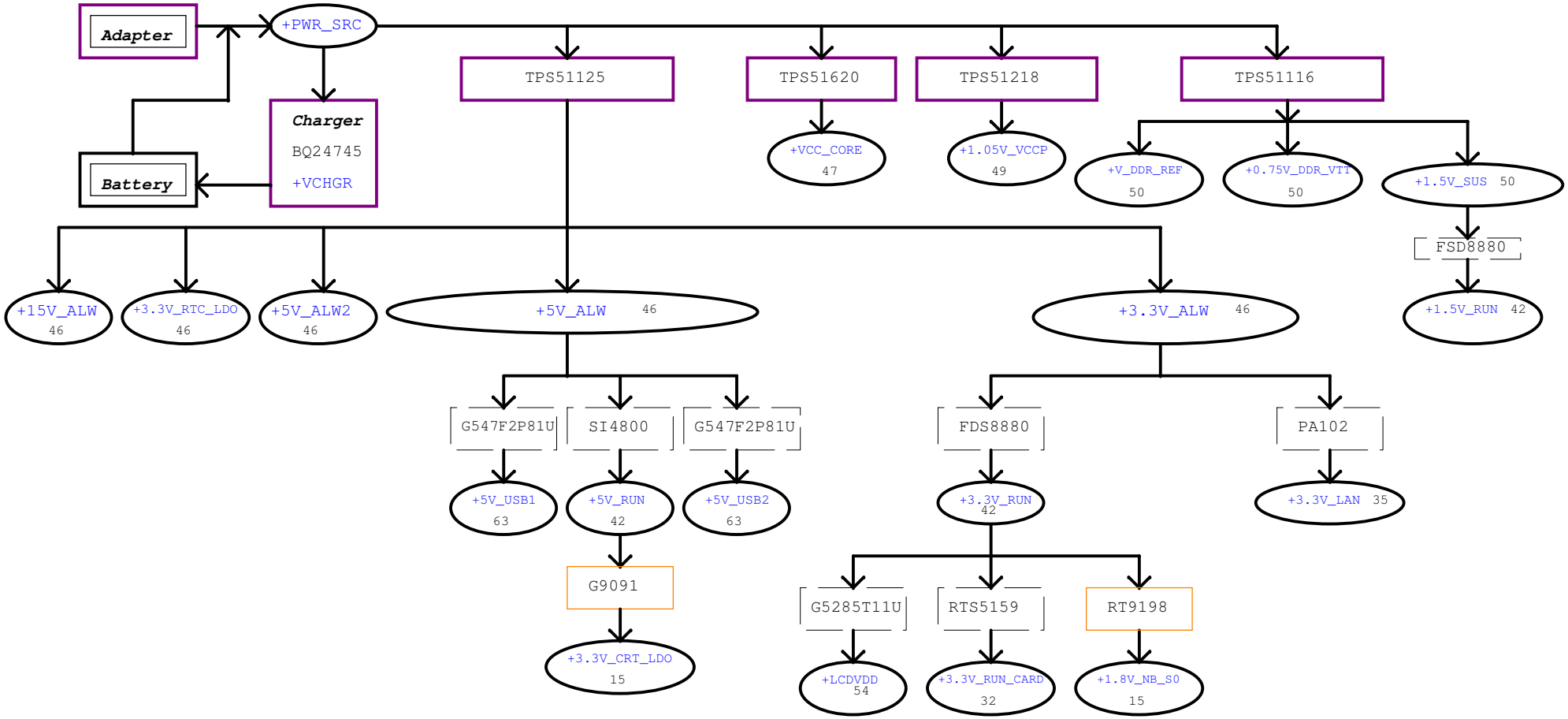
DJ1 Montevina UMA Power Block Diagram



Power Shape

Regulator	LDO	Switch

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Title		
Power Block Diagram		
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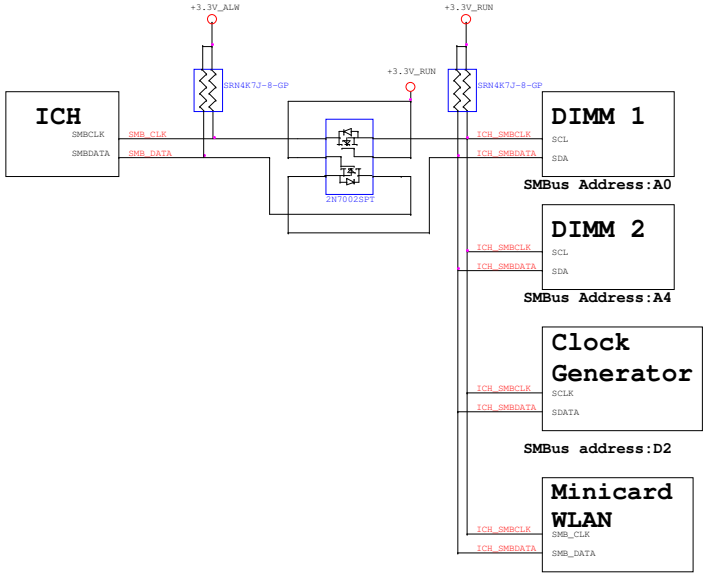
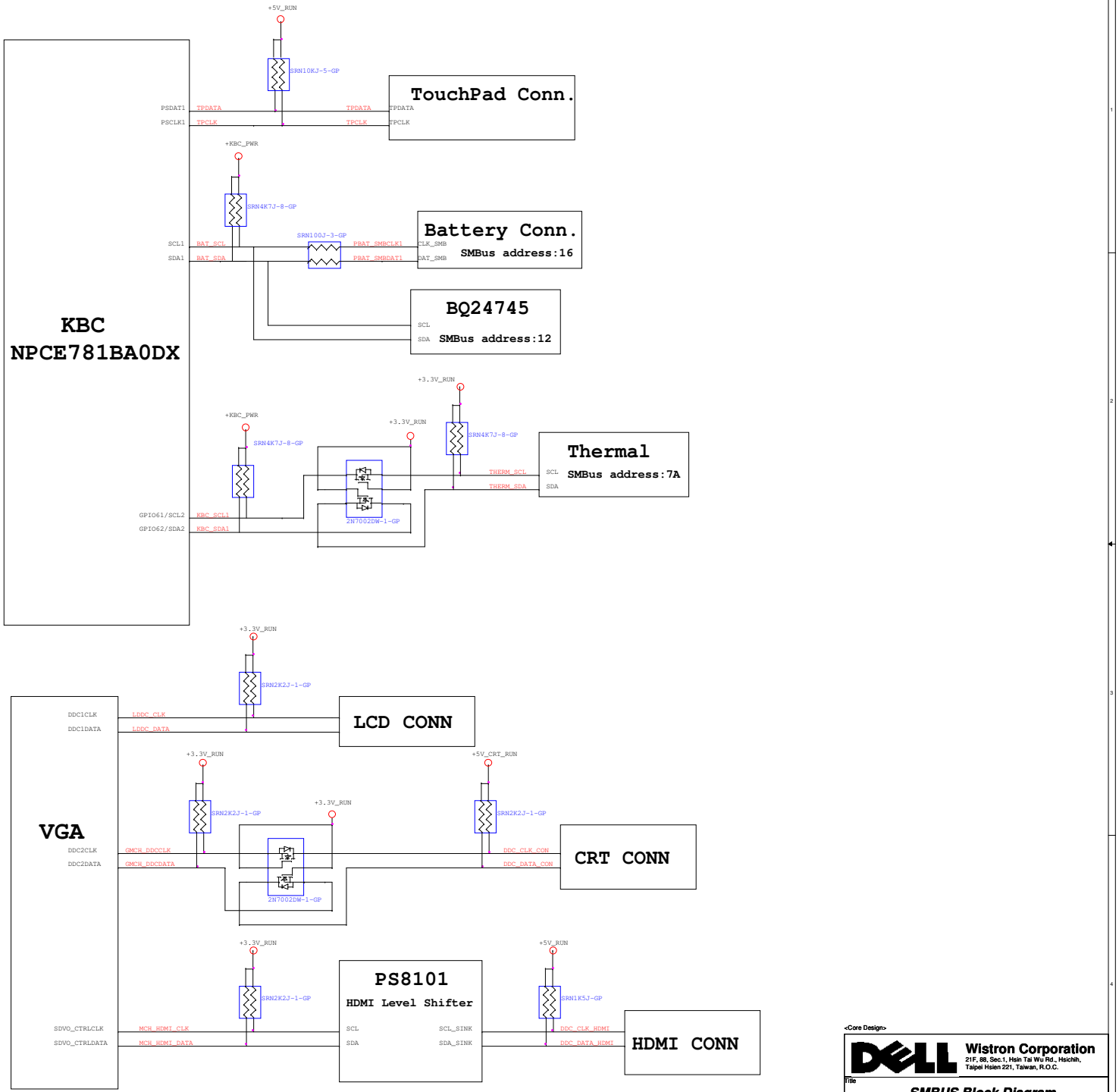
ICH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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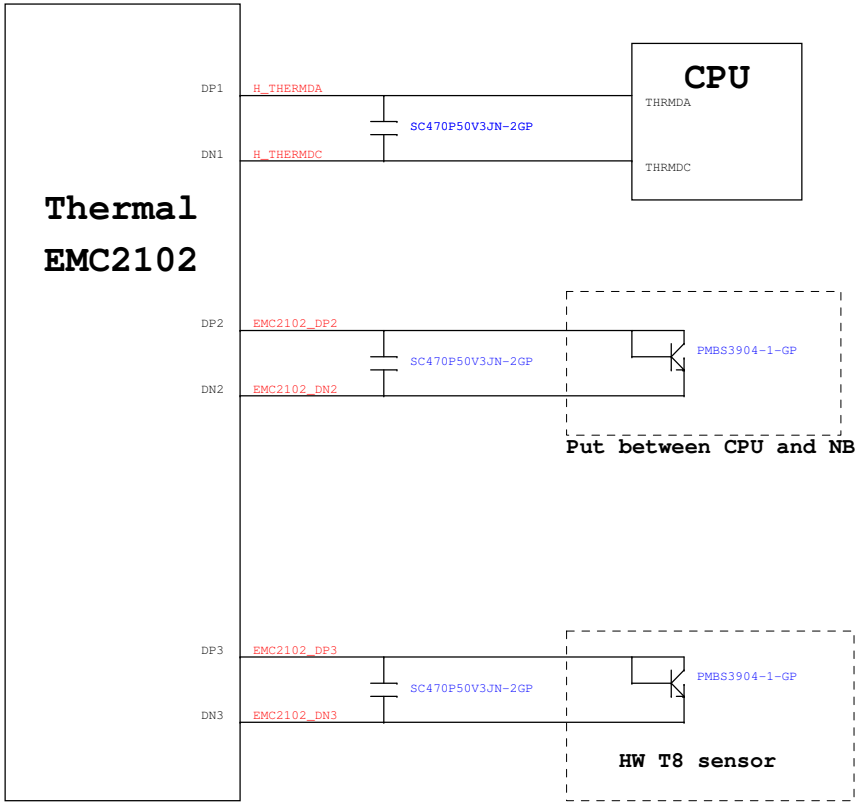
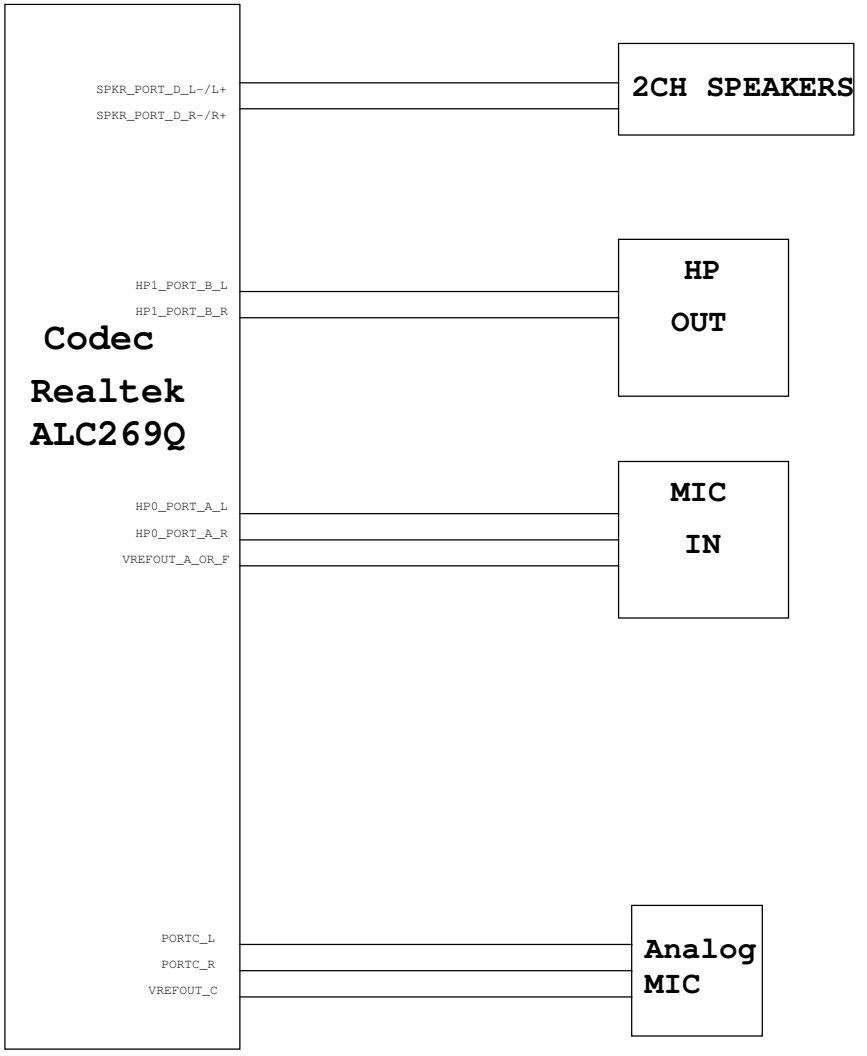
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.2.3

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance / PCI Express* Port Config 1 bit 1 (Port 1-4), Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Config Registers: Offset 224h).This signal has a weak internal pull-down.
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4), Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Config Registers: Offset 224h)
GNT2#/ GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6), Rising Edge of PWROK	This signal has a weak internal pull-up. Sets bit 2 of RPC.PC2 (Chipset Config Registers:Offset 0224h) when sampled low.
GPIO20	Reserved, Rising Edge of PWROK	This signal has a weak internal pull-down. NOTE: This signal should not be pulled high
GNT1#/ GPIO51	ESI Strap (Server Only), Rising Edge of PWROK.	Tying this strap low configures DMI for ESIcompatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: this indicates that the system is strapped to the "top-block swap" mode (IntelR ICH9 inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers:Offset 3414h: bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#	Boot BIOS Destination Selection 1, Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. Bit11 (GNT0#) / Bit 10 (SPI_CS1#) / Boot BIOS Destination 0 / 1 / SPI 1 / 0 / PCI 1 / 1 / LPC 0 / 0 / Reserved
SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0, Rising Edge of CLPWROK.	Controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 (GNT0#) / Bit 10 (SPI_CS1#) / Boot BIOS Destination 0 / 1 / SPI 1 / 0 / PCI 1 / 1 / LPC 0 / 0 / Reserved
SATALED#	PCI Express Lane Reversal (Lanes 1-4). Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0: Offset D8)
SPKR	No Reboot, Rising Edge of PWROK.	Sampled high: this indicates that the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers:Offset 3410h:bit 5).
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33 / HDA_DOCK_EN# (Mobile Only)	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. Sampled high: the security measures will be in effect. This strap should only be enabled in manufacturing environments.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be high for mobile applications.
SPI_MOSI (Moble Only)	Integrated TPM Enable. Rising Edge of CLPWROK.	Sampled low: the Integrated TPM will be disabled. Sampled high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enabled. NOTE: This signal is required to be floating or pulled low for desktop applications.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.2.3

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRSLPVR/GPIO16	PULL-DOWN 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT0#, GNT[3:1]#/ GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LAD[3:0]# / FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ0	PULL-UP 20K
LDRQ1 / GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1# / GPIO58 (Desktop Only) / CLGPIO6 (Digital Office Only)	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP3	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

PCIE Routing

LANE1	
LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB Pair	Device
0	USB0
1	RESERVED
2	USB2
3	USB3
4	BLUETOOTH
5	RESERVED
6	WLAN
7	RESERVED
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 355648 Rev.2.3

Pin Name	Strap Description	Configuration
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Others = Reserved
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	ITPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	**0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality** **1 = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	**0 = Reverse Lanes, 15->0, 14->1 etc.** **1 = Normal operation (default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG12	ALLZ	0 =ALLZ mode enabled (Note 3) **1 = Disable (Default)**
CFG13	XOR	0 = XOR mode enabled (Note 3) **1 = Disable (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIe	**0 = Only digital DisplayPort (SDVO/DP/HDMI) or PCIe is operational (default)** **1 = Digital DisplayPort (SDVO/DP/HDMI) and PCIe are operating simultaneously via the PEG port**
SDVO _CTRLDATA (Note4)	SDVO Present	0 = No SDVO/HDMI/DP interface disabled (default) 1 = SDVO/HDMI/DP interface enabled
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled
DDPC _CTRLDATA (Note4)	Digital Display Present	**0 = Digital display (HDMI/DP) device absent (default)** **1 = Digital display (HDMI/DP) Device Present**
CFG4:3 CFG8 CFG11 CFG14 CFG15 CFG17 CFG18	Reserved	

NOTE:

1. All strap signals are sampled with respect to the leading edge of the GMCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
3. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.
4. DDPC_CTRL_DATA & SDVO_CTRL_DATA straps should both be high to enable Display Port.

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Title: Table of Content

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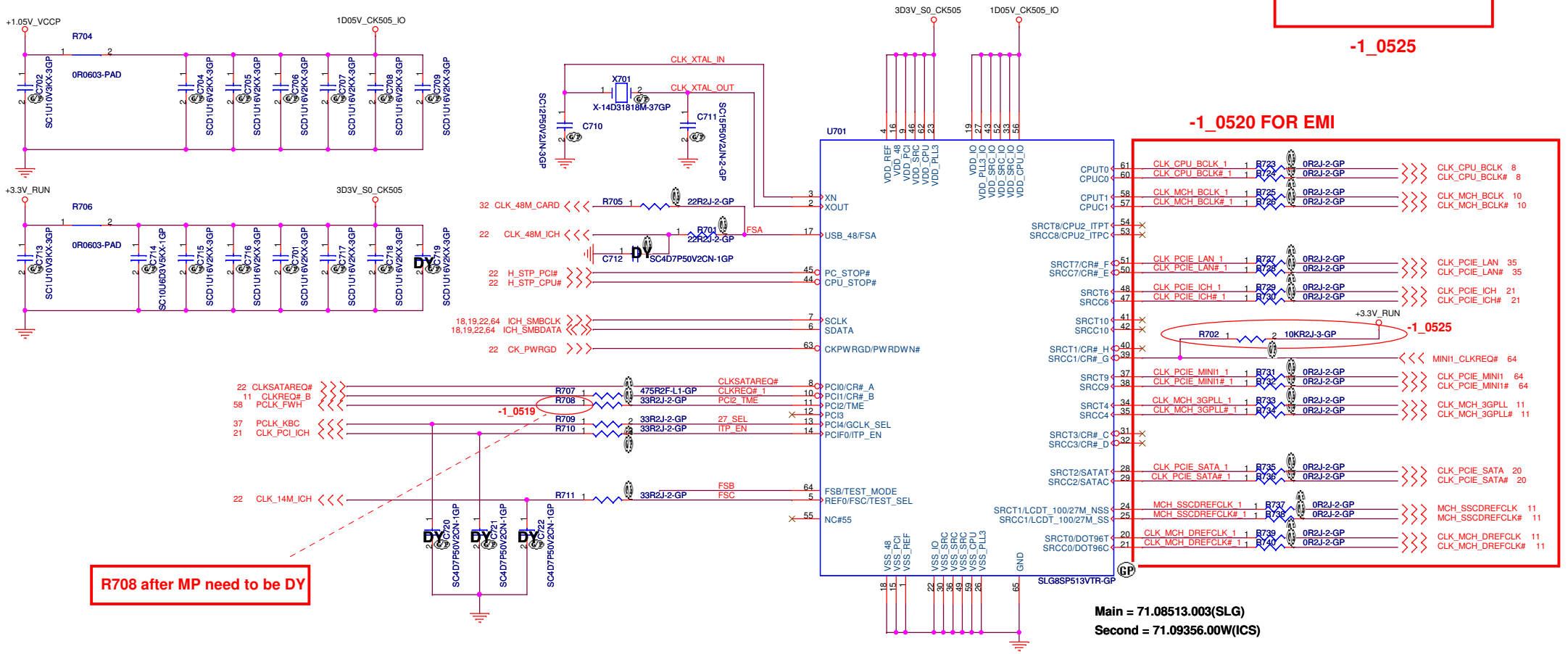
SSID = CLOCK

-1_0525

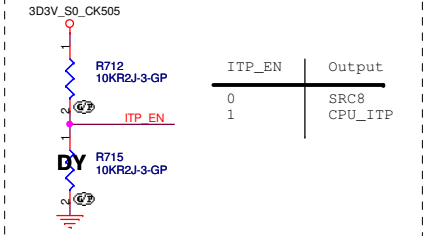
-1_0520 FOR EMI



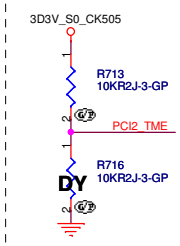
R708 after MP need to be DY

Main = 71.08513.003(SLG)

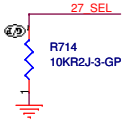
Second = 71.09356.00W(ICS)



ITP_EN	Output
0	SRC8
1	CPU_ITP

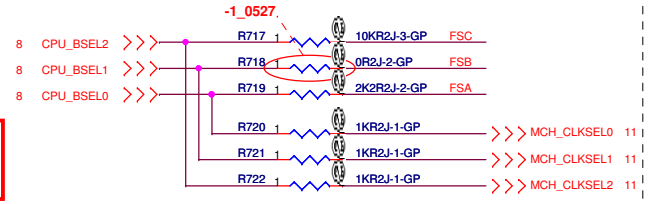


PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed



27_SEL	PIN20/21	PIN24/25
0	96M	100M
1	100M	27M

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M



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Title: Clock Generator SLG8SP513VTR

Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00

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SSID = CPU

CPU1A 1 OF 4

TP801

H_A#[35..3] 10

H_ADSTB#0 10
H_REQ#[4..0] 10

H_A#[35..3]
H_REQ#0 H_REQ#1 H_REQ#2 H_REQ#3 H_REQ#4
H_ADSTB#0
A3# A4# A5# A6# A7# A8# A9# A10# A11# A12# A13# A14# A15# A16#
REQ0# REQ1# REQ2# REQ3# REQ4#
ADSTB0#
ADDR GROUP 0

H_A#17 H_A#18 H_A#19 H_A#20 H_A#21 H_A#22 H_A#23 H_A#24 H_A#25 H_A#26 H_A#27 H_A#28 H_A#29 H_A#30 H_A#31 H_A#32 H_A#33 H_A#34 H_A#35
A17# A18# A19# A20# A21# A22# A23# A24# A25# A26# A27# A28# A29# A30# A31# A32# A33# A34# A35#
ADSTB1#
ADDR GROUP 1

H_ADSTB#1 10

20 H_A20M#
20 H_FERR#
20 H_IGNNE#
A20M# FERR# IGNNE#

20 H_STPCLK#
20 H_INTR
20 H_NMI
20 H_SMI#
STPCLK# LINT0 LINT1 SMI#
ICH

TP802 RSVD_CPU_1
TP803 RSVD_CPU_2
TP804 RSVD_CPU_3
TP805 RSVD_CPU_4
TP806 RSVD_CPU_5
TP807 RSVD_CPU_6
TP808 RSVD_CPU_7
TP809 RSVD_CPU_8
TP810 RSVD_CPU_9
TP811 RSVD_CPU_10
TP812 RSVD_CPU_11
RSVD#M4 RSVD#N5 RSVD#T2 RSVD#V3 RSVD#B2 TEST7 RSVD#D2 RSVD#D22 RSVD#D3 RSVD#F6 KEY_NC
RESERVED

BGA479-SKT6-GPU7
62.10079.001

ADS# BNR# BPRI#
DEFER# DRDY# DBSY#
BR0#
IERR# INIT#
LOCK#
RESET# RS#0 RS#1 RS#2 TRDY#
HIT# HITM#
CONTROL

H_ADS# 10
H_BNR# 10
H_BPRI# 10
H_DEFER# 10
H_DRDY# 10
H_DBSY# 10
H_BREQ#0 10
CPU_IERR# R802 1 56R2J-4-GP +1.05V_VCCP
H_INIT# 20
H_LOCK# 10
H_CPURST# 10
H_RS#[2..0] 10
H_TRDY# 10
H_HIT# 10
H_HITM# 10

BPM0# BPM1# BPM2# BPM3# PRDY# PREQ# TCK TDI TDO TMS TRST# DBR#
XDP/ITP SIGNALS

ITP_BPM#5
ITP_TCK
ITP_TDI
ITP_TDO
ITP_TMS
ITP_TRST#
ITP_DBRESET#

THERMAL
PROCHOT# THRMDA THRMDC THERMTRIP#

R803 1 DY 0R2J-2-GP CPU_PROCHOT# 47
R804 1 56R2J-4-GP +1.05V_VCCP
H_THERMDA 39
H_THERMDC 39
R805 1 DY 56R2J-4-GP +1.05V_VCCP
H_THRMTRIP# 11,20,37,42

H_THERMDA
DY C849 SC2200P50V2KX-2GP
H_THERMDC

H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

H_THRMTRIP# should connect to
ICH9 and MCH without T-ing.

HCLK
BCLK0 BCLK1
CLK_CPU_BCLK 7
CLK_CPU_BCLK# 7

+1.05V_VCCP
R806 1KR2F-3-GP
CPU_GTLREF0
R812 2KR2F-3-GP
C801 SC1KP50V2KX-1GP

Layout notes
Z= 55 Ohm 0.5" MAX for CPU_GTLREF0

ITP_TMS R816 51R2F-2-GP
ITP_TDI R817 51R2F-2-GP
ITP_BPM#5 R818 51R2F-2-GP
ITP_TDO R801 DY 51R2F-2-GP
+3.3V_RUN
ITP_DBRESET# R825 DY 1KR2J-1-GP
ITP_TCK R819 51R2F-2-GP
ITP_TRST# R820 51R2F-2-GP
All place within 2" to CPU

H_DINV#[3..0] H_DINV#[3..0] 10
H_DSTBN#[3..0] H_DSTBN#[3..0] 10
H_DSTBP#[3..0] H_DSTBP#[3..0] 10
H_D#[63..0] H_D#[63..0] 10

CPU1B 2 OF 4

H_D#0 H_D#1 H_D#2 H_D#3 H_D#4 H_D#5 H_D#6 H_D#7 H_D#8 H_D#9 H_D#10 H_D#11 H_D#12 H_D#13 H_D#14 H_D#15
D0# D1# D2# D3# D4# D5# D6# D7# D8# D9# D10# D11# D12# D13# D14# D15#
DSTBN0# DSTBP0# DINV0#
DATA GRP0

10 H_DSTBN#0
10 H_DSTBP#0
10 H_DINV#0
DSTBN2# DSTBP2# DINV2#
H_DSTBN#2 10
H_DSTBP#2 10
H_DINV#2 10

D32# D33# D34# D35# D36# D37# D38# D39# D40# D41# D42# D43# D44# D45# D46# D47#
H_D#32 H_D#33 H_D#34 H_D#35 H_D#36 H_D#37 H_D#38 H_D#39 H_D#40 H_D#41 H_D#42 H_D#43 H_D#44 H_D#45 H_D#46 H_D#47
DATA GRP2

H_D#16 H_D#17 H_D#18 H_D#19 H_D#20 H_D#21 H_D#22 H_D#23 H_D#24 H_D#25 H_D#26 H_D#27 H_D#28 H_D#29 H_D#30 H_D#31
D16# D17# D18# D19# D20# D21# D22# D23# D24# D25# D26# D27# D28# D29# D30# D31#
DSTBN1# DSTBP1# DINV1#
DATA GRP1

10 H_DSTBN#1
10 H_DSTBP#1
10 H_DINV#1
DSTBN3# DSTBP3# DINV3#
H_DSTBN#3 10
H_DSTBP#3 10
H_DINV#3 10

D48# D49# D50# D51# D52# D53# D54# D55# D56# D57# D58# D59# D60# D61# D62# D63#
H_D#48 H_D#49 H_D#50 H_D#51 H_D#52 H_D#53 H_D#54 H_D#55 H_D#56 H_D#57 H_D#58 H_D#59 H_D#60 H_D#61 H_D#62 H_D#63
DATA GRP3

GTLREF TEST1 TEST2 TEST3 TEST4 TEST5 TEST6
R808 1 DY 1KR2J-1-GP TEST1
R810 1 DY 1KR2J-1-GP TEST2
R813 1 DY 1KR2J-1-GP CPU_TEST3
R815 1 DY 1KR2J-1-GP CPU_TEST5
BSEL0 BSEL1 BSEL2
7 CPU_BSEL0
7 CPU_BSEL1
7 CPU_BSEL2
MISC

COMP0 COMP1 COMP2 COMP3
R807 1 27D4R2F-L1-GP
R809 1 54D9R2F-L1-GP
R811 1 27D4R2F-L1-GP
R814 1 54D9R2F-L1-GP
DPRSTP# DPSLP# DPWR# PWRGOOD SLP# PSI#
H_DPRSTP# 11,20,47
H_DPSLP# 20
H_DPWR# 10
H_PWRGOOD 20,42
H_CPUSLP# 10
PSI# 47

BGA479-SKT6-GPU7
62.10079.001

TP813 1 H_CPURST#

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

<Core Design>

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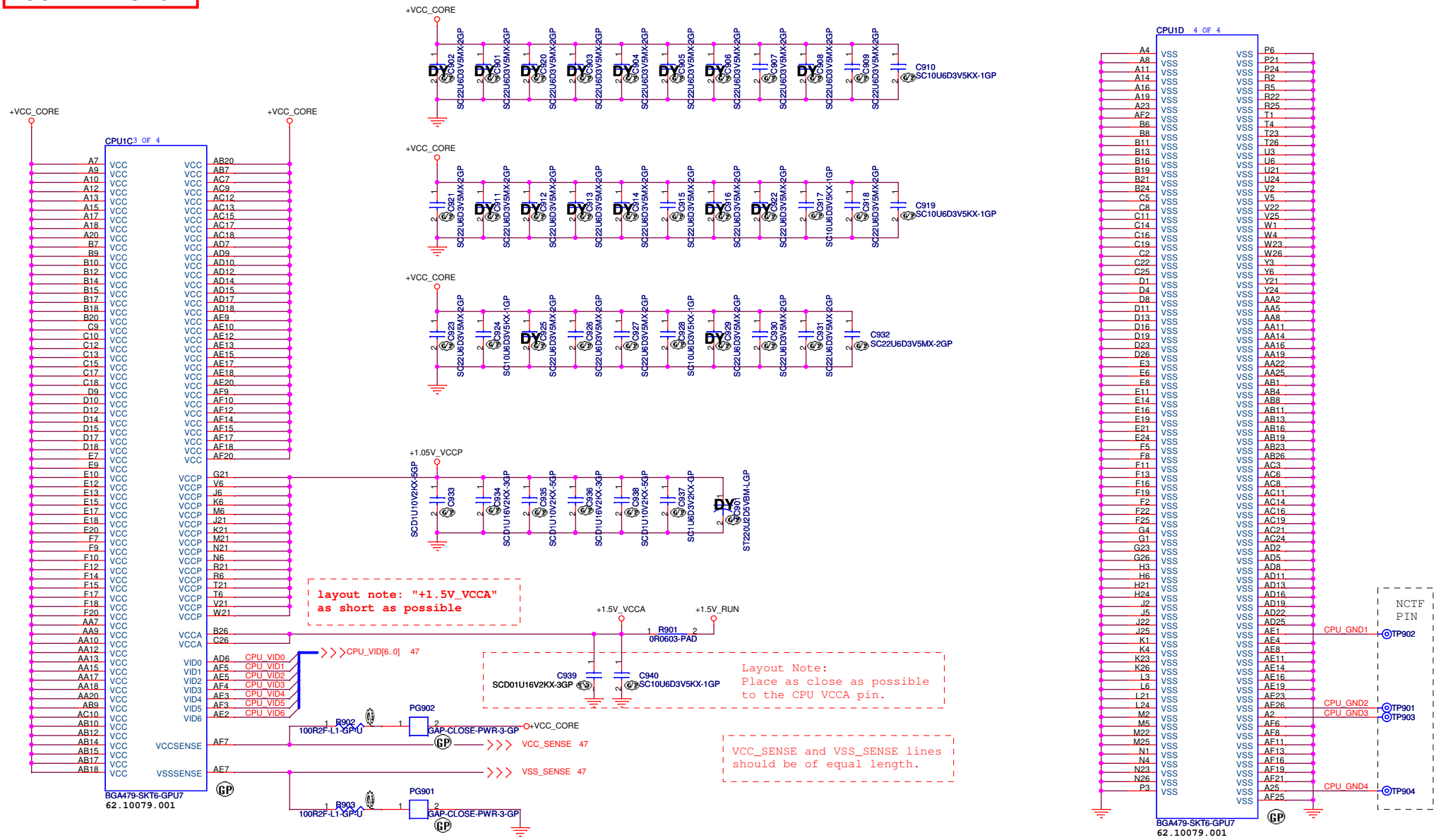
Title: CPU-FSB(1/2)
Size: Custom
Document Number: DJ2 Montevina UMA
Rev: X00
Date: Wednesday, June 02, 2010
Sheet 8 of 88

SSID = CPU



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU-Power(2/2)

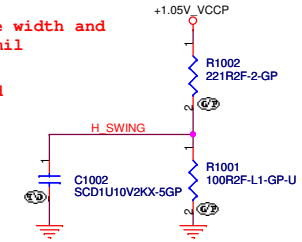
Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00

Date: Wednesday, June 02, 2010 | Sheet 9 of 88

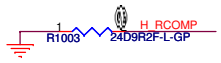
SSID = MCH

H_SWING routing Trace width and Spacing use 10 / 20 mil

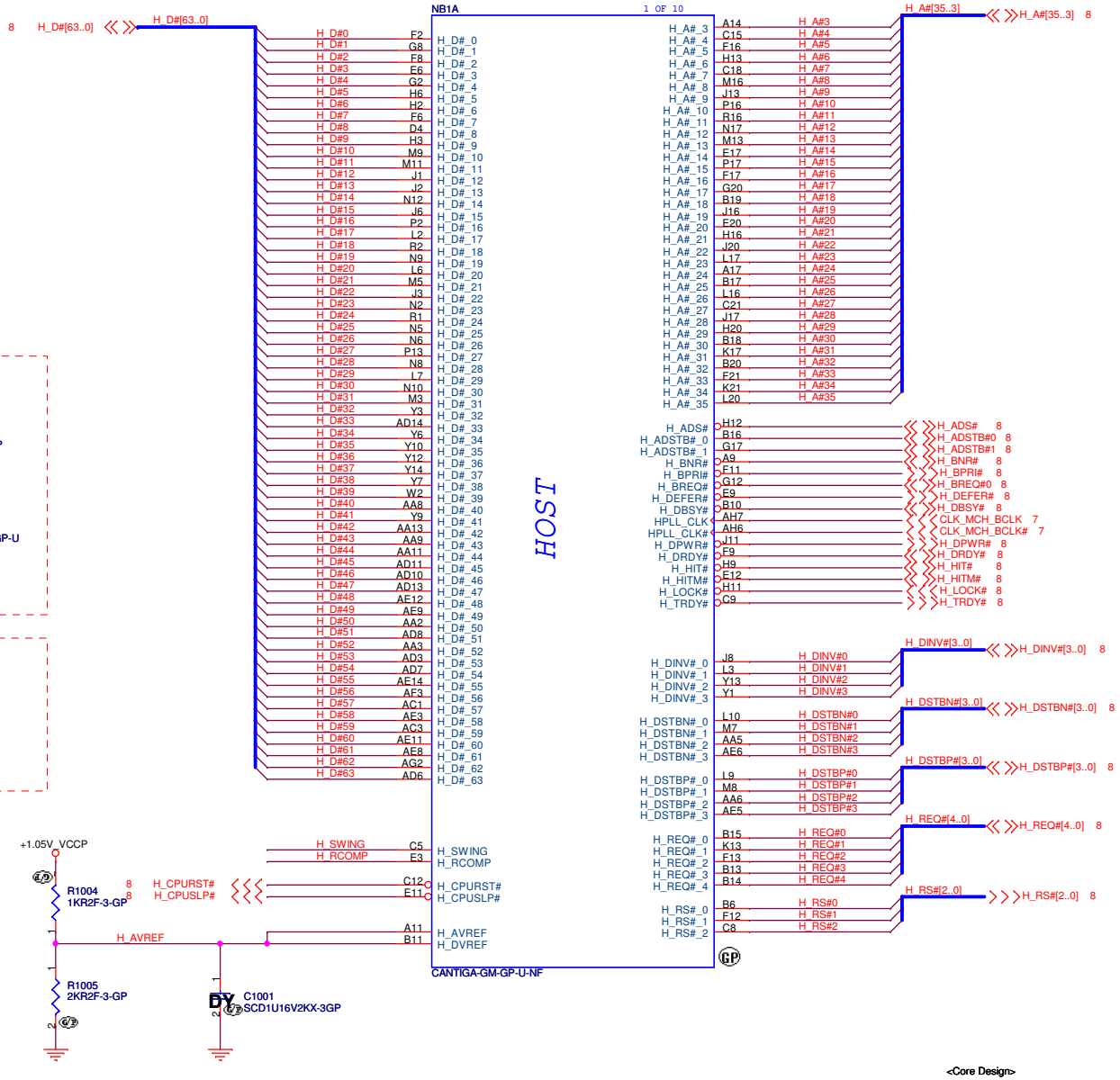
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place R1001 near to the chip (< 0.5")



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-Host(1/6)

Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00

Date: Wednesday, June 02, 2010 | Sheet 10 of 88

SSID = MCH

* is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	ITPM enable	ITPM disable *
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality *
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in oder *
CFG 10	PCIE loopback enable	PCIE loopback disable *
CFG 12	ALLZ mode enable	ALLZ mode disable *
CFG 13	XOR mode enable	XOR mode disable *
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable *
CFG 19 DMI Lane Reserved	Normal operation *	Reverse DMI lanes
CFG 20 SDVO concurrent with PCIE	Only PCIE or SDVO is operational *	PCIE and SDVO are operatiing simultaneously via the PEG port
SDVO_CTRLDATA	SDVO interface disable	SDVO interface enable (HDMI enable) *
L_DDC_DATA	LFP disable *	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled *	SDVO/iHDMI/DP interface enabled

-1_0519

NB1B — 2 OF 10

RESERVED#M36, RESERVED#N36, RESERVED#R33, RESERVED#T33, RESERVED#AH9, RESERVED#AH10, RESERVED#AH12, RESERVED#AH13, RESERVED#K12, RESERVED#AL34, RESERVED#AK34, RESERVED#AN35, RESERVED#AM35, RESERVED#T24, RESERVED#B31, RESERVED#B2, RESERVED#M1, RESERVED#AY21, RESERVED#BG23, RESERVED#BF23, RESERVED#BH18, RESERVED#BF18

RSVD

DDR CLK/ CONTROL/COMPENSATION

SA_CK_0 AP24 M_CLK_DDR0 18
SA_CK_1 AT21 M_CLK_DDR1 18
SB_CK_0 AV24 M_CLK_DDR2 19
SB_CK_1 AU20 M_CLK_DDR3 19
SA_CK#_0 AR24 M_CLK_DDR#0 18
SA_CK#_1 AR21 M_CLK_DDR#1 18
SB_CK#_0 AU24 M_CLK_DDR#2 19
SB_CK#_1 AV20 M_CLK_DDR#3 19
SA_CKE_0 BC28 M_CKE0 18
SA_CKE_1 AY28 M_CKE1 18
SB_CKE_0 AY36 M_CKE2 19
SB_CKE_1 BB36 M_CKE3 19
SA_CS#_0 BA17 M_CS#0 18
SA_CS#_1 AY16 M_CS#1 18
SB_CS#_0 AV16 M_CS#2 19
SB_CS#_1 AR13 M_CS#3 19
SA_ODT_0 BD17 M_ODT0 18
SA_ODT_1 AY17 M_ODT1 18
SB_ODT_0 BF15 M_ODT2 19
SB_ODT_1 AY13 M_ODT3 19
SM_RCOMP BG22 M_RCOMPP
SM_RCOMP# BH21 M_RCOMPN
SM_RCOMP_VOH BF28 SM_RCOMP_VOH
SM_RCOMP_VOL BH28 SM_RCOMP_VOL
SM_VREF AV42 CANTIGA_SM_VREF
SM_PWROK AR36 SM_PWROK
SM_REXT BF17 SM_REXT
SM_DRAMRST# BC36 DDR3_DRAMRST#

DDR3_DRAMRST# 18,19
SM_PWROK 41

R1103 80D6R2F-L-GP (+1.5V_SUS)
R1105 80D6R2F-L-GP
R1109 499R2F-2-GP
R1108 0R0603-PAD (+V_DDR_REF)
R1102 1KR2F-3-GP (+1.5V_SUS)
R1104 3K01R2F-3-GP
R1106 1KR2F-3-GP
SM_RCOMP_VOH — C1102 SC2D2U6D3V3KX-GP — C1103 SCD01U16V2KX-3GP
SM_RCOMP_VOL — C1104 SC2D2U6D3V3KX-GP — C1101 SCD01U16V2KX-3GP
C1105 SCD1U10V2KX-5GP (DY)
C1106 SCD1U10V2KX-5GP (DY)

DPLL_REF_CLK AB38 CLK_MCH_DREFCLK 7
DPLL_REF_CLK# A38 CLK_MCH_DREFCLK# 7
DPLL_REF_SSCLK E41 MCH_SSCDREFCLK 7
DPLL_REF_SSCLK# F41 MCH_SSCDREFCLK# 7
PEG_CLK F43 CLK_MCH_3GPLL 7
PEG_CLK# E43 CLK_MCH_3GPLL# 7

CLK

DMI_RXN_0 AE41 DMI_ITXN0_MRXN0 21
DMI_RXN_1 AE37 DMI_ITXN1_MRXN1 21
DMI_RXN_2 AE47 DMI_ITXN2_MRXN2 21
DMI_RXN_3 AH39 DMI_ITXN3_MRXN3 21
DMI_RXP_0 AE40 DMI_ITXP0_MRXP0 21
DMI_RXP_1 AE38 DMI_ITXP1_MRXP1 21
DMI_RXP_2 AE48 DMI_ITXP2_MRXP2 21
DMI_RXP_3 AH40 DMI_ITXP3_MRXP3 21
DMI_TXN_0 AE35 DMI_IRXN0_MTXN0 21
DMI_TXN_1 AE43 DMI_IRXN1_MTXN1 21
DMI_TXN_2 AE46 DMI_IRXN2_MTXN2 21
DMI_TXN_3 AH42 DMI_IRXN3_MTXN3 21
DMI_TXP_0 AD35 DMI_IRXP0_MTXP0 21
DMI_TXP_1 AE44 DMI_IRXP1_MTXP1 21
DMI_TXP_2 AF46 DMI_IRXP2_MTXP2 21
DMI_TXP_3 AH43 DMI_IRXP3_MTXP3 21

DMI

CLKREQ#_B — R1129 10KR2J-3-GP (+3.3V_RUN)

+1.05V_VCCP — R1122 56R2J-4-GP — R1123 DY 10KR2J-3-GP (+3.3V_RUN)
TSATN# — Q101 MMBT3904WT1G-GP (DY, GP) — TSATN#_KBC 37

GFX_VID_0 B33
GFX_VID_1 B32
GFX_VID_2 G33
GFX_VID_3 F33
GFX_VID_4 E33
GFX_VR_EN C34

GRAPHICS VID

CL_CLK AH37 CL_CLK0 22
CL_DATA AH36 CL_DATA0 22
CL_PWROK AN36 M_PWROK 22
CL_RST# AJ35 CL_RST#0 22
CL_VREF AH34 MCH_CLVREF

MCH_CLVREF ~= 0.35V

R1126 1KR2F-3-GP (+1.05V_VCCP)
R1128 499R2F-2-GP
C1108 SCD1U10V2KX-5GP

ME

DDPC_CTRLCLK N28
DDPC_CTRLDATA M28
SDVO_CTRLCLK G36 MCH_HDMI_CLK
SDVO_CTRLDATA E36 MCH_HDMI_DATA

-1_0511

CLKREQ#_B 7
MCH_ICH_SYNC# 22

CLKREQ# K36
ICH_SYNC# H36
TSATN# B12 TSATN#

MISC

+3.3V_RUN — RN1103 SRN2K2J-1-GP (HDMI) — MCH_HDMI_CLK 57, MCH_HDMI_DATA 57

-1_0511

HDA_BCLK B28 GMCH_HDA_BITCLK 57
HDA_RST# B30 GMCH_HDA_RST# 57
HDA_SDI B29 ICH_AZ_MCH_SDIN1_R — 33R2J-2-GP — HDMI 1 R1136 — GMCH_HDA_SDIN1 57
HDA_SDO C29 GMCH_HDA_SDOUT 57
HDA_SYNC A28 GMCH_HDA_SYNC 57

HDA

-1_0527
HDA level shift for HDMI

FSB setting

MCH_CLKSEL0 7 — TP1102 — CFG3
MCH_CLKSEL1 7 — TP1103 — CFG4
MCH_CLKSEL2 7

CFG_0 T25, CFG_1 R25, CFG_2 P25, CFG_3 P20, CFG_4 P24, CFG_5 C25, CFG_6 N24, CFG_7 M24, CFG_8 E21, CFG_9 C23, CFG_10 C24, CFG_11 N21, CFG_12 P21, CFG_13 T21, CFG_14 R20, CFG_15 M20, CFG_16 L21, CFG_17 H21, CFG_18 P29, CFG_19 R28, CFG_20 T28

CFG9 — TP1104 — CFG14
CFG10 — TP1105 — CFG15
CFG16
TP1101 — CFG17
CFG19
CFG20

CFG

PM_SYNC# R29
PM_DPRSTP# B7
PM_EXT_TS#_0 N33
PM_EXT_TS#_1 P32
PWROK AT40
RSTIN# AT11
THERMTRIP# T20
DPRSLPVR R32

22 PM_SYNC#
8,20,47 H_DPRSTP#
18 PM_EXTTS#0
19 PM_EXTTS#1
22,37 PM_PWROK
21,35,37,57,58,64 PLT_RST#
R1125 0R0402-PAD — PWROK_R — RSTIN#
R1127 100R2J-2-GP
C1107 SC100P50V2JN-3GP (DY)
8,20,37,42 H_THRMTRIP#
22,47 DPRSLPVR

PM

NC#BG48, NC#BF48, NC#BD48, NC#BC48, NC#BH47, NC#BG47, NC#BE47, NC#BH46, NC#BF46, NC#BG45, NC#BH44, NC#BH43, NC#BH6, NC#BH5, NC#BG4, NC#BH3, NC#BF3, NC#BH2, NC#BG2, NC#BE2, NC#BG1, NC#BF1, NC#BD1, NC#BC1, NC#F1, NC#A47

NC

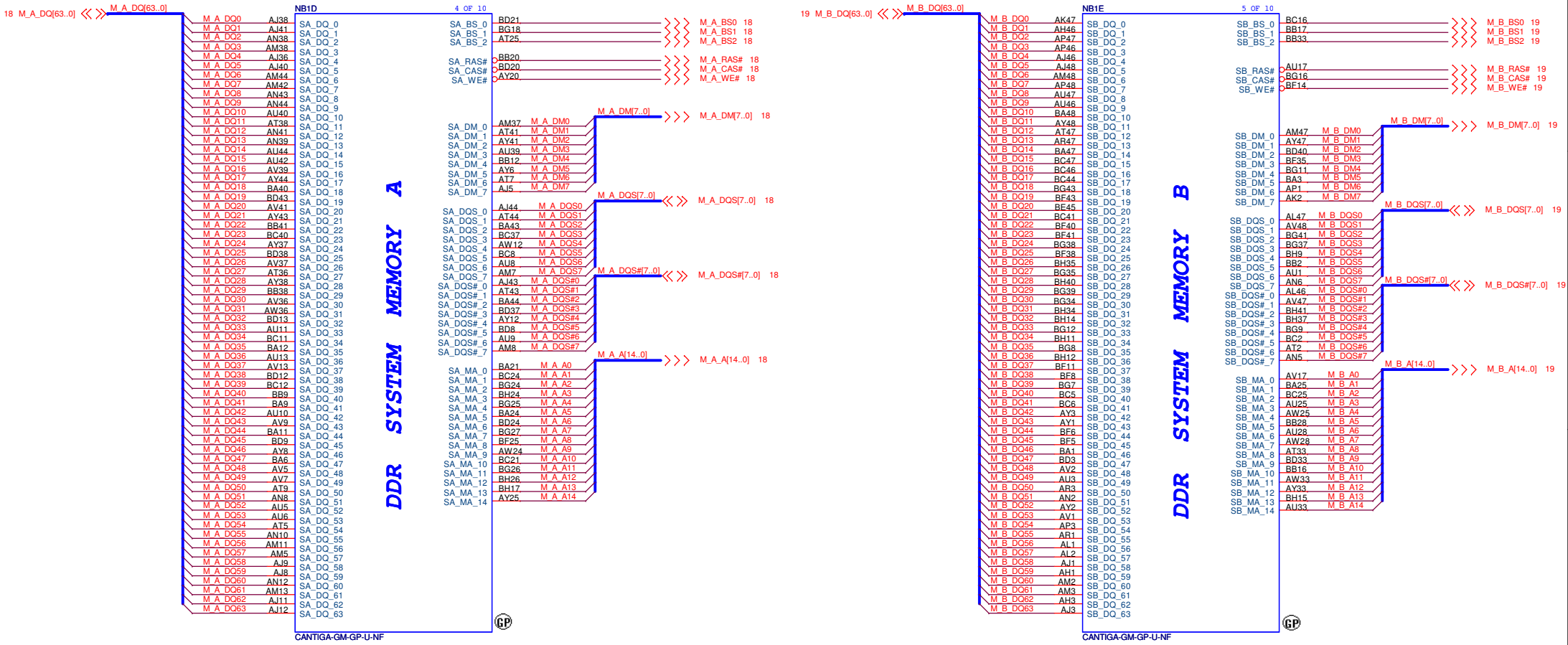
CANTIGA-GM-GP-U-NF

+3.3V_RUN
R1112 DY 4K02R2F-GP CFG19
R1113 DY 4K02R2F-GP CFG20
RN1102 SRN10KJ-5-GP — PM_EXTTS#0, PM_EXTTS#1
R1118 DY 4K02R2F-GP CFG9
R1119 DY 2K21R2F-GP CFG10
R1124 DY 2K21R2F-GP CFG16

Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-DMI/CFG(2/6)
Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00
Date: Wednesday, June 02, 2010 | Sheet 11 of 88

SSID = MCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-DDR(3/6)

Size	Document Number	Rev
Custom	DJ2 Montevina UMA	X00

Date: Wednesday, June 02, 2010 Sheet 12 of 88

SSID = MCH

NB1I 9 OF 10

NB1J 10 OF 10

CANTIGA-GM-GP-U-NF

VSS NCTF

VSS SCB

NC

CRT_IREF routing Trace width use 20 mil.

NCTF PIN

NB1C 3 OF 10

LVDS

PCI-EXPRESS GRAPHICS

TV

VGA

CANTIGA-GM-GP-U-NF

Place R1303 close to MCH within 500 mils.

-1_0517

-1_0511

-1_0511

-1_0519

2N7002EDW-GP

<Core Design>

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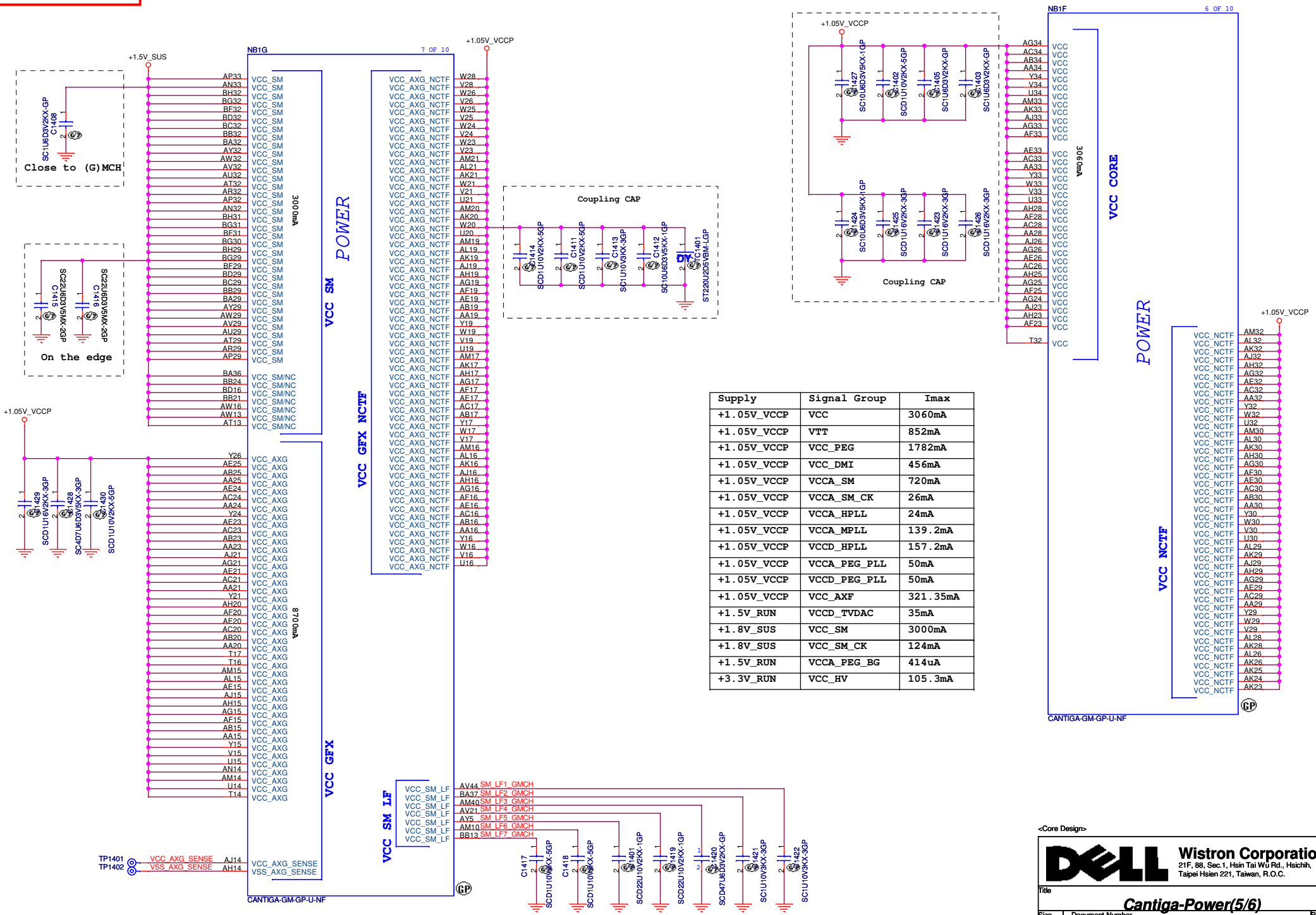
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-GND/LVDS/VGA(4/6)

Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00

Date: Wednesday, June 02, 2010 | Sheet 13 of 88

SSID = MCH



Supply	Signal Group	Imax
+1.05V_VCCP	VCC	3060mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+1.5V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

<Core Design>

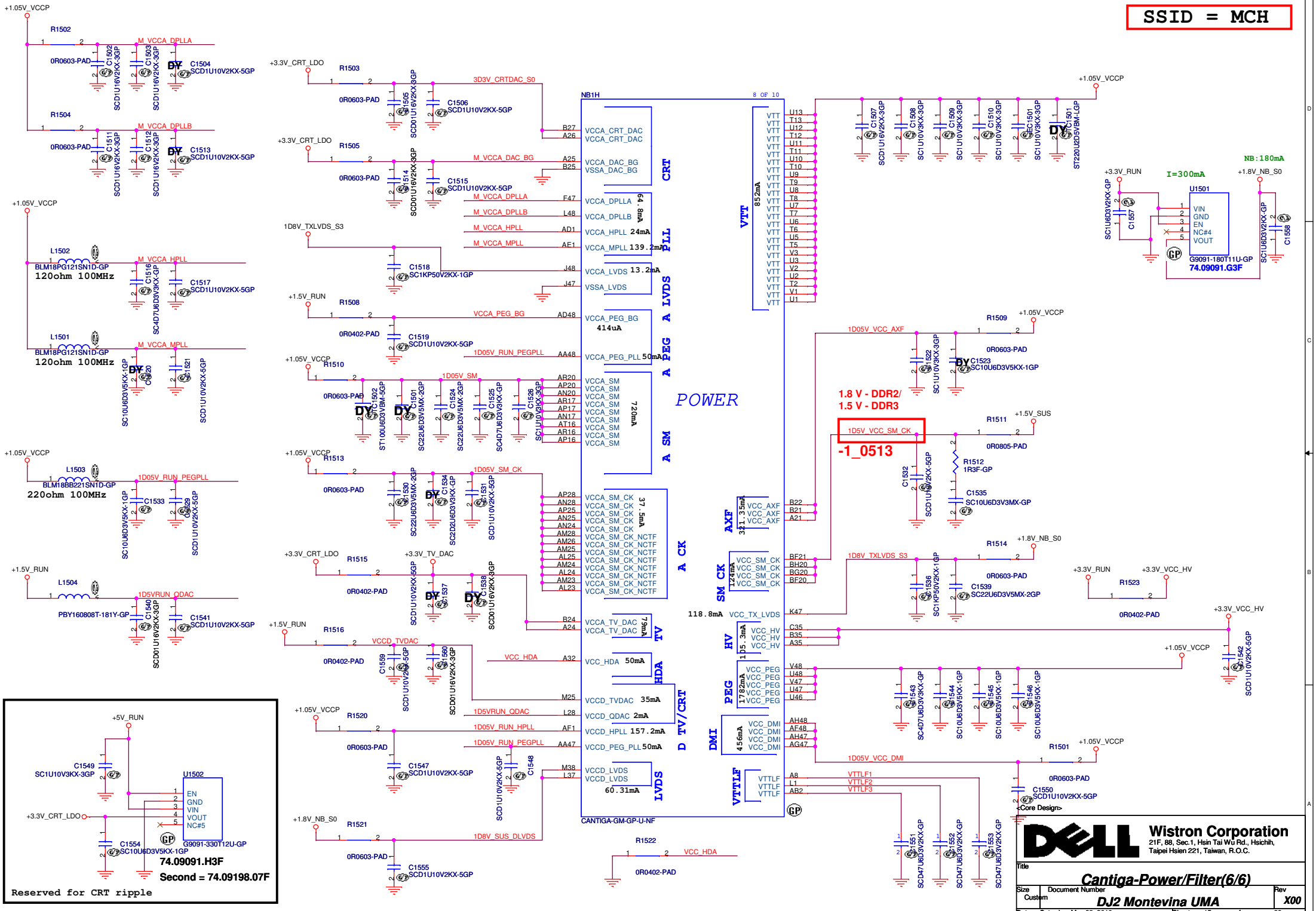
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-Power(5/6)

Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00

Date: Saturday, May 29, 2010 | Sheet 14 of 88

SSID = MCH

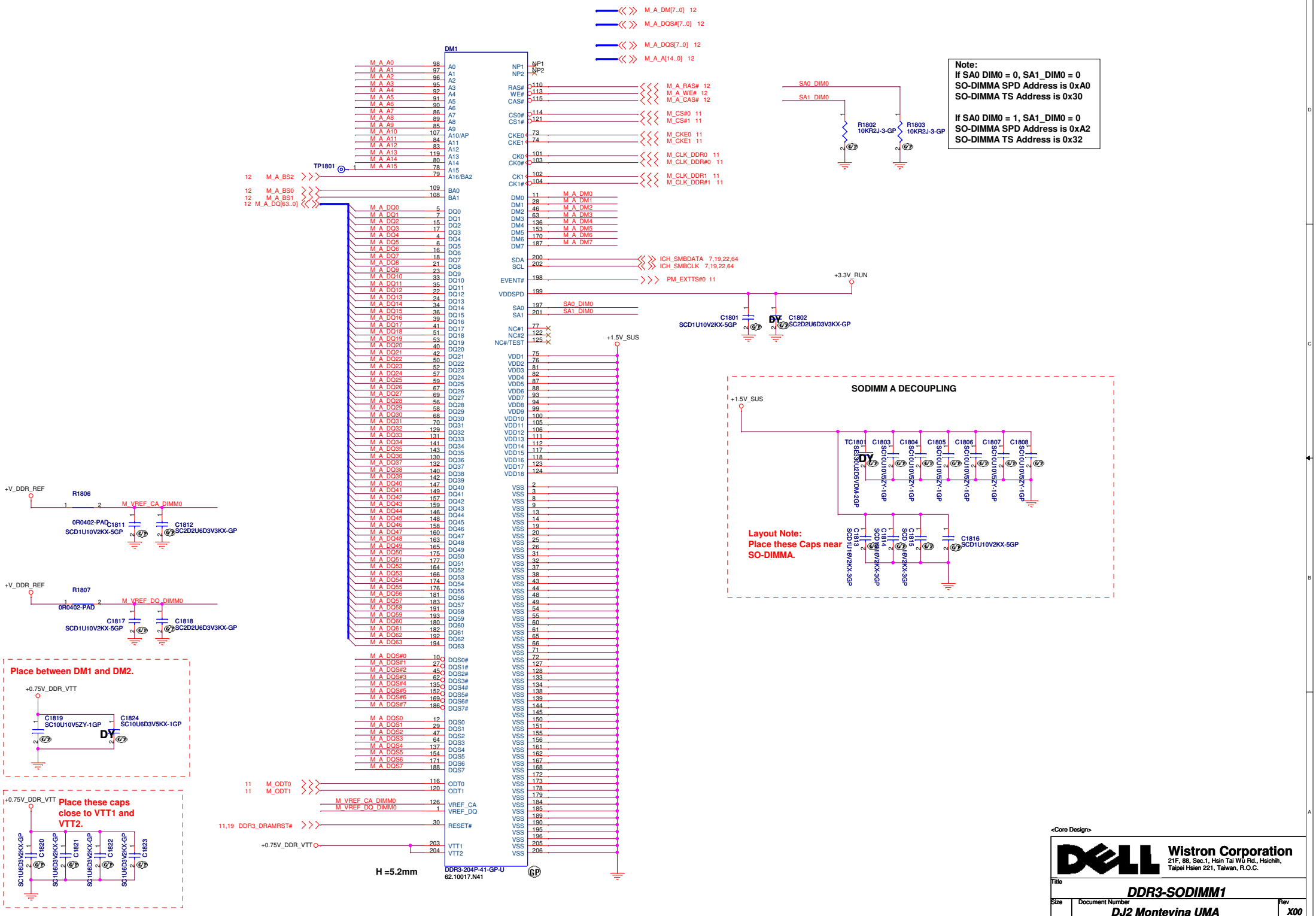


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-Power/Filter(6/6)

Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00

Date: Saturday, May 29, 2010 | Sheet 15 of 88



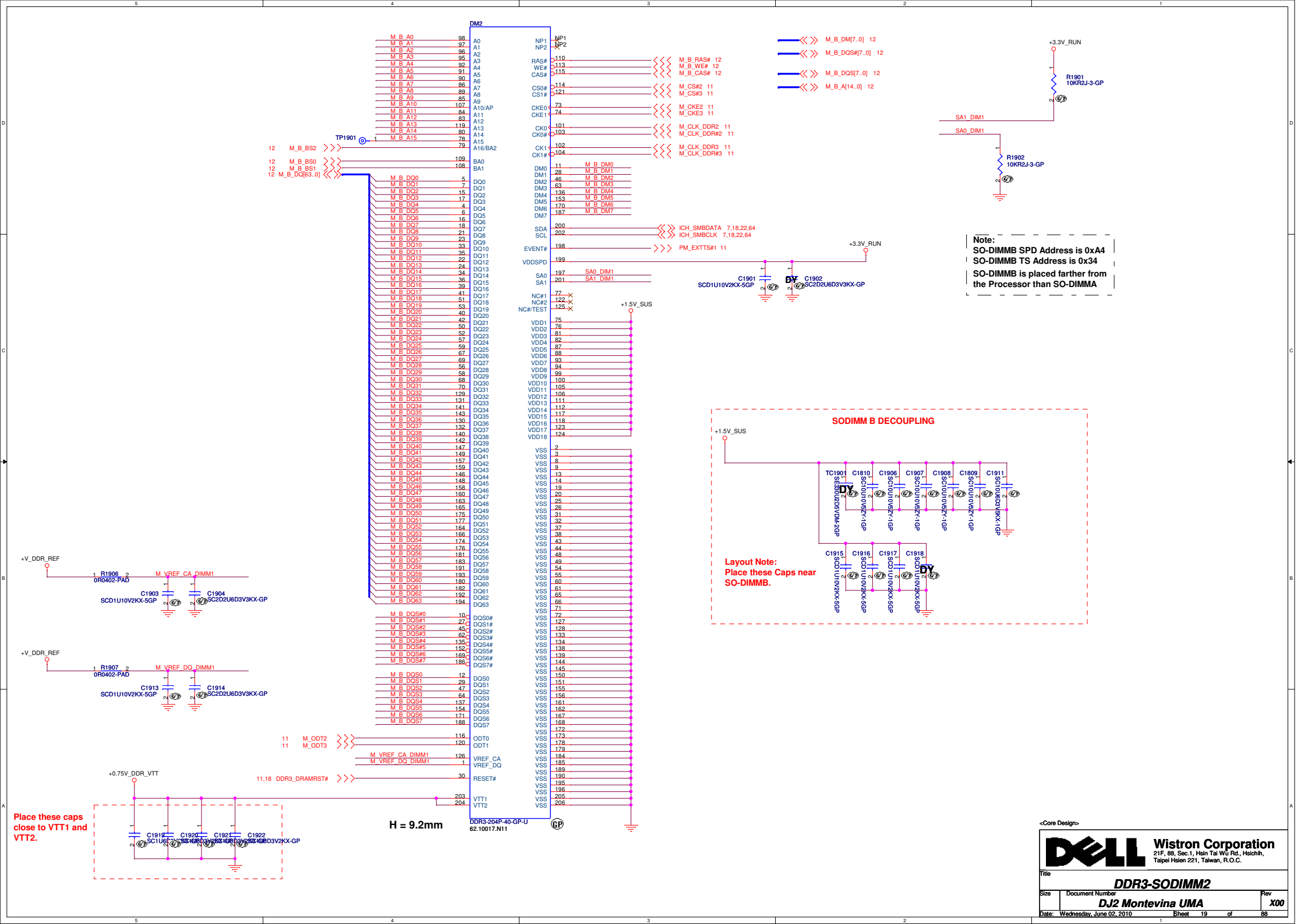
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

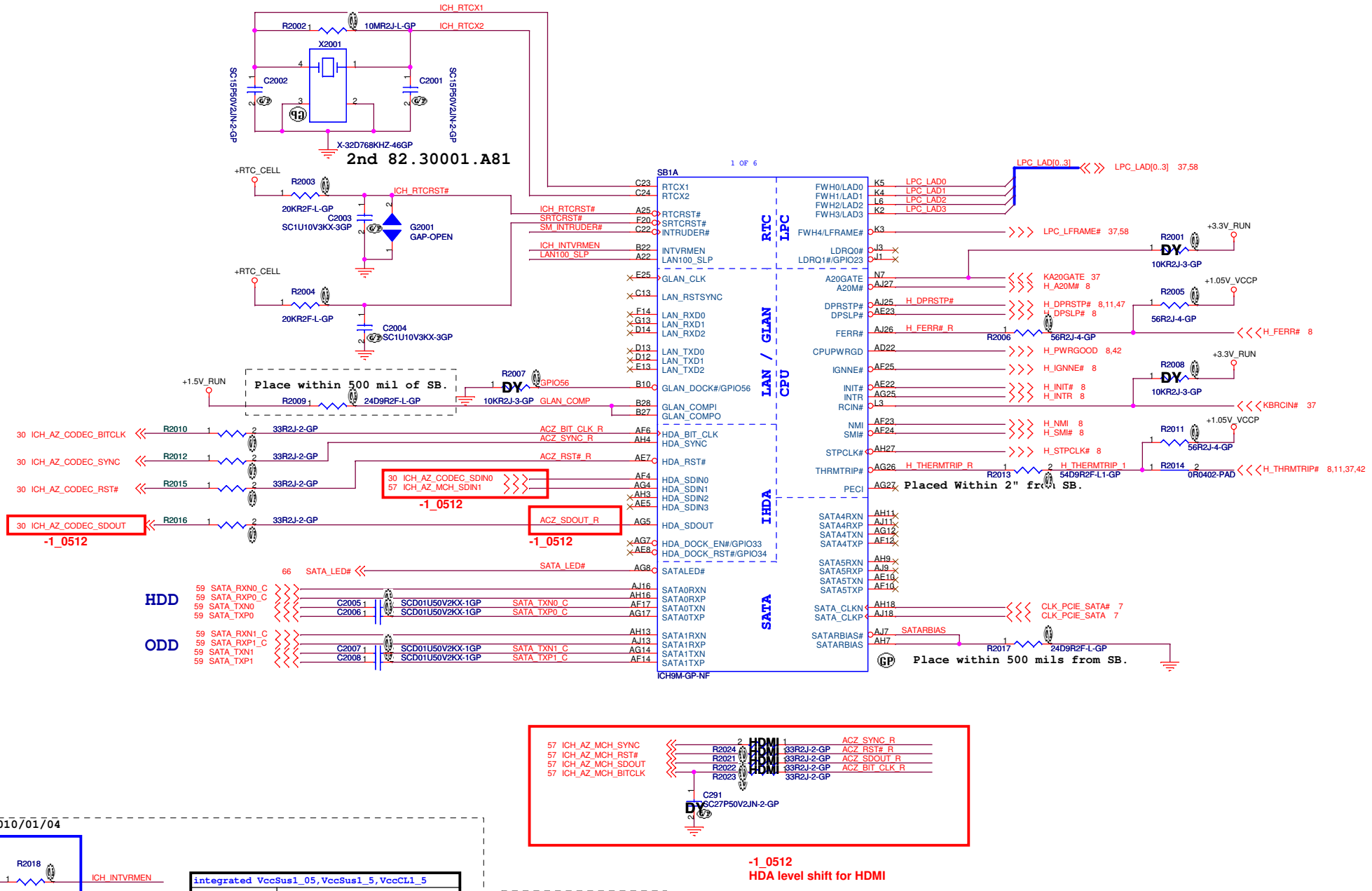
Title: DDR3-SODIMM1

Size | Document Number: DJ2 Montevina UMA | Rev: X00

Date: Wednesday, June 02, 2010 Sheet 18 of 88


DM2
DDR3-204P-40-GP-U
62.10017.N11
H = 9.2mm
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from the Processor than SO-DIMMA
SODIMM B DECOUPLING
Layout Note:
Place these Caps near SO-DIMMB.
Place these caps close to VTT1 and VTT2.
+3.3V_RUN
+1.5V_SUS
+V_DDR_REF
+0.75V_DDR_VTT
R1901 10KR2J-3-GP
R1902 10KR2J-3-GP
R1906 0R0402-PAD
R1907 0R0402-PAD
C1901 SCD1U10V2KX-5GP
C1902 SC2D2U6D3V3KX-GP
C1903 SCD1U10V2KX-5GP
C1904 SC2D2U6D3V3KX-GP
C1913 SCD1U10V2KX-5GP
C1914 SC2D2U6D3V3KX-GP
TP1901
M_B_DQ[63..0]
M_B_DM[7..0] 12
M_B_DQS#[7..0] 12
M_B_DQS[7..0] 12
M_B_A[14..0] 12
ICH_SMBDATA 7,18,22,64
ICH_SMBCLK 7,18,22,64
PM_EXTTS#1 11
11,18 DDR3_DRAMRST#
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR3-SODIMM2
Size
Document Number
DJ2 Montevina UMA
Rev
X00
Date: Wednesday, June 02, 2010
Sheet 19 of 88

SSID = ICH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-LAN/HDA/SATA/LPC(1/4)

Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00

Date: Wednesday, June 02, 2010 | Sheet 20 of 88

SSID = ICH

SB1E — 5 OF 6 — ICH9M-GP-NF

SB1B — 2 OF 6 — PCI / Interrupt I/F — ICH9M-GP-NF

SB1D — 4 OF 6 — PCI-Express / Direct Media Interface / SPI / USB — ICH9M-GP-NF

Layout Note:
Place as close as possible
to the ICH Pin

RP2101 SRN10KJ-L3-GP

RN2106 SRN8K2J-4-GP

RN2102 RN2101 RN2103 RN2104 RN2105 SRN8K2J-4-GP

R2103 R2104 R2105 DY 1KR2J-1-GP

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

USB Pair	Device
0	USB0
1	RESERVED
2	USB2
3	USB3
4	BLUETOOTH
5	RESERVED
6	WLAN
7	RESERVED
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

NCTF PIN

WLAN

LAN

USB0

USB2

USB3

BLUETOOTH

WLAN

Card Reader

CAMERA

<Core Design>

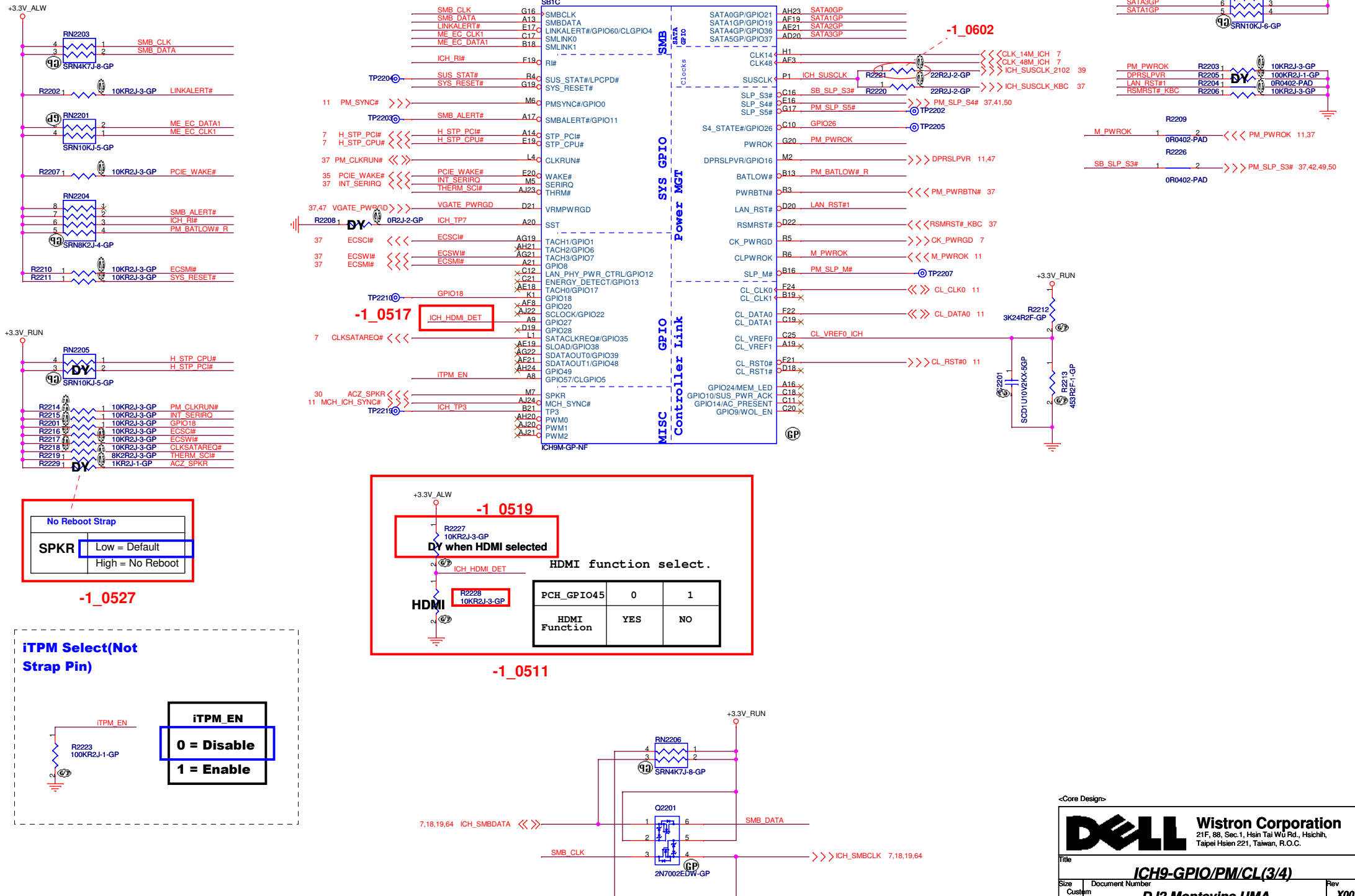
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-PCI/PCIE/DMI/USB/GND(2/4)

Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00

Date: Wednesday, June 02, 2010 | Sheet 21 of 88

SSID = ICH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

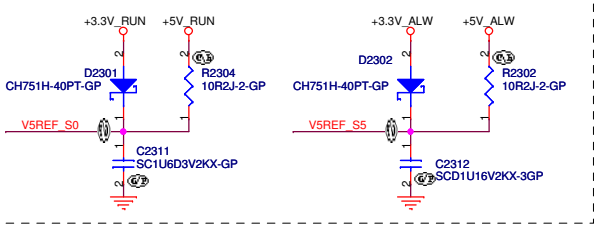
Title: ICH9-GPIO/PM/CL(3/4)

Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00

Date: Wednesday, June 02, 2010 | Sheet 22 of 88

SSID = ICH

**Within a given well, 5VREF needs to be up before the corresponding 3.3V rail*



<Core Design>

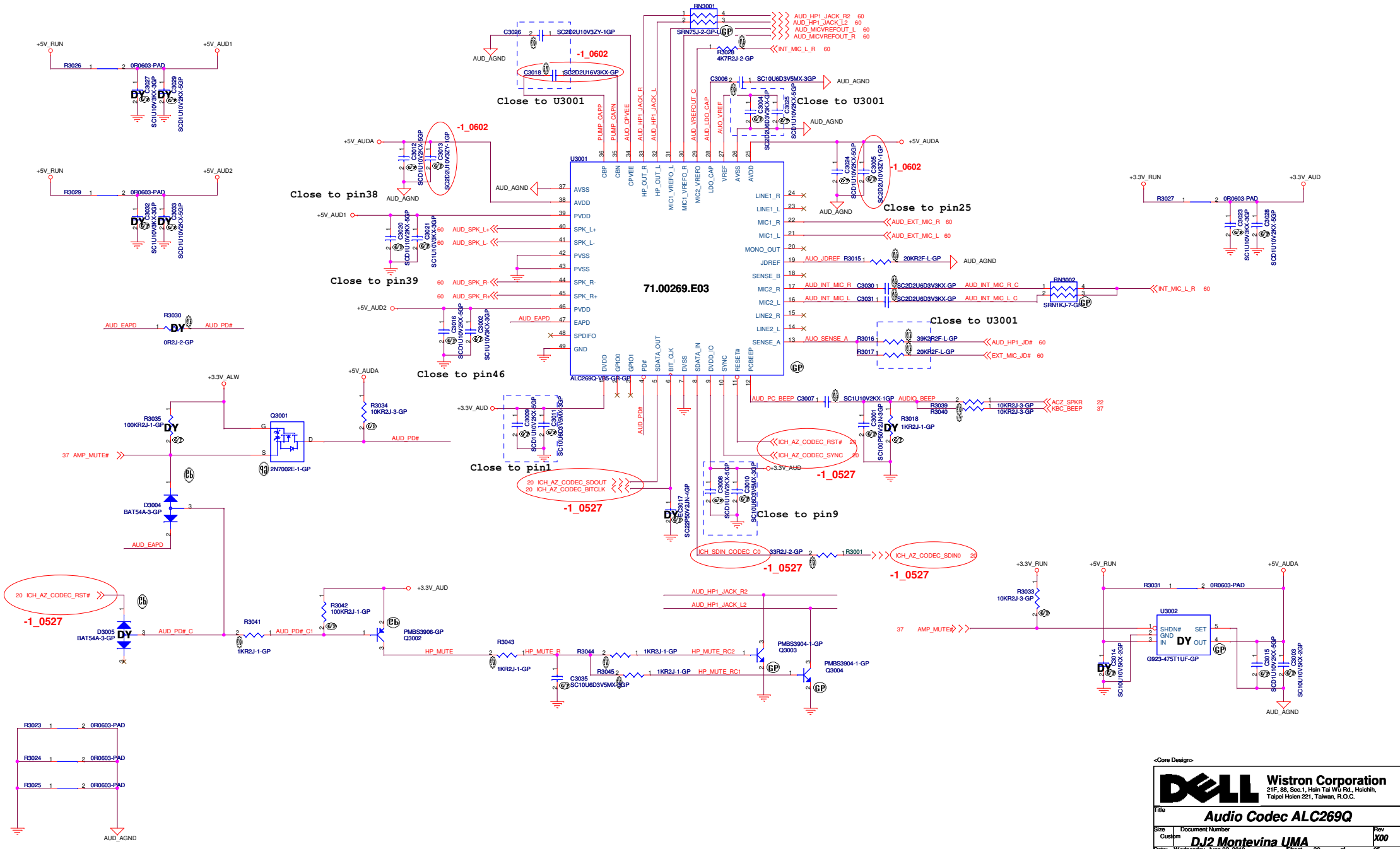
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-Power(4/4)**

Size: Custom | Document Number: **DJ2 Montevina UMA** | Rev: X00

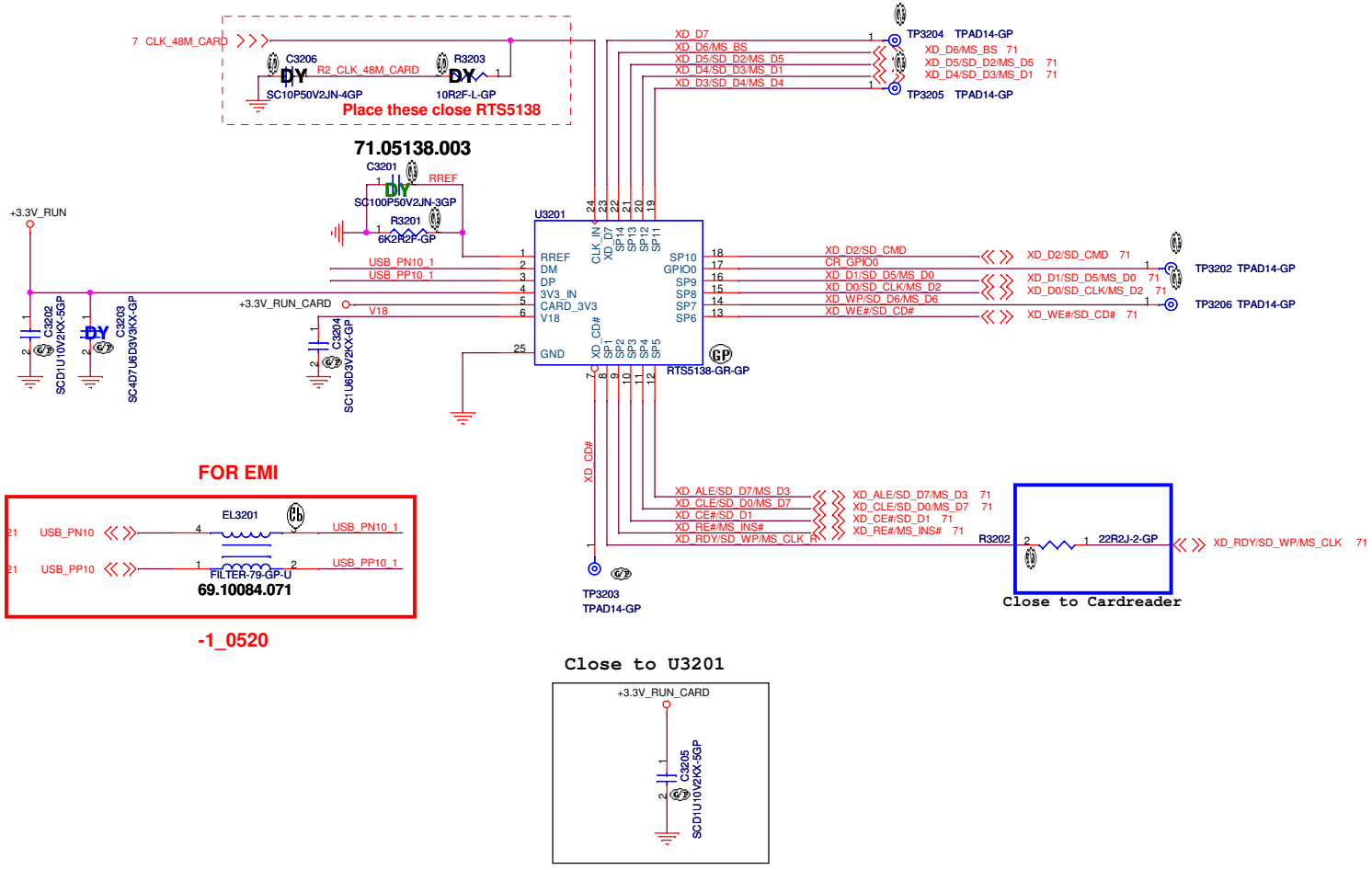
Date: Saturday, May 29, 2010 | Sheet 23 of 88

SSID = AUDIO



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

SSID = SDIO



FOR EMI

-1_0520

Close to U3201

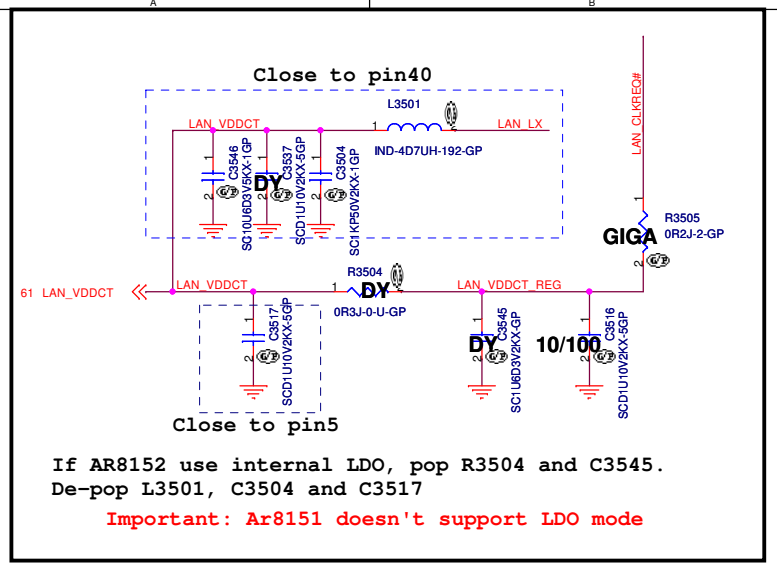
<Core Design>

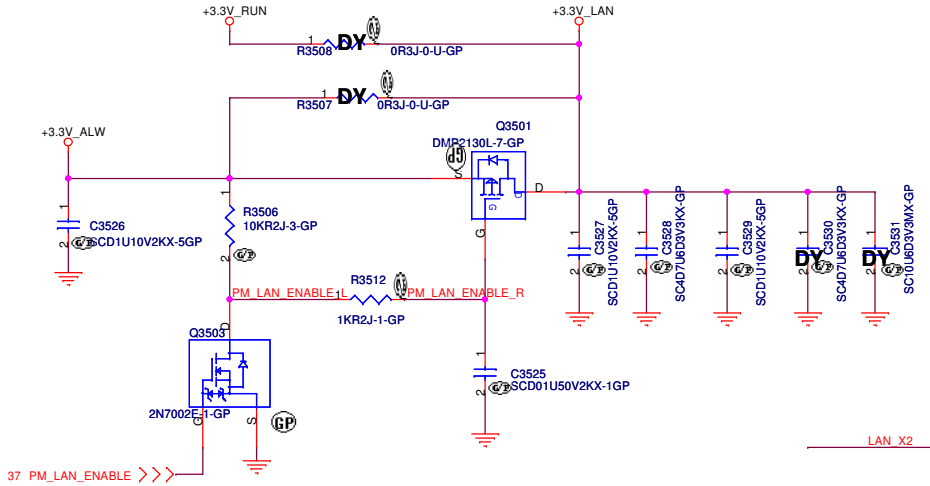
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138

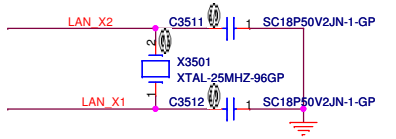
Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00

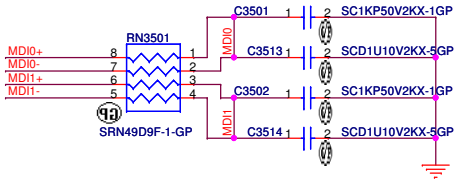
Date: Wednesday, June 02, 2010 | Sheet 32 of 88



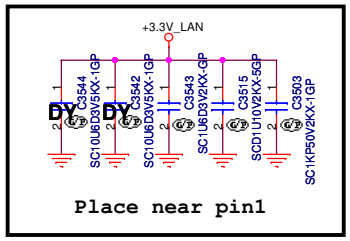


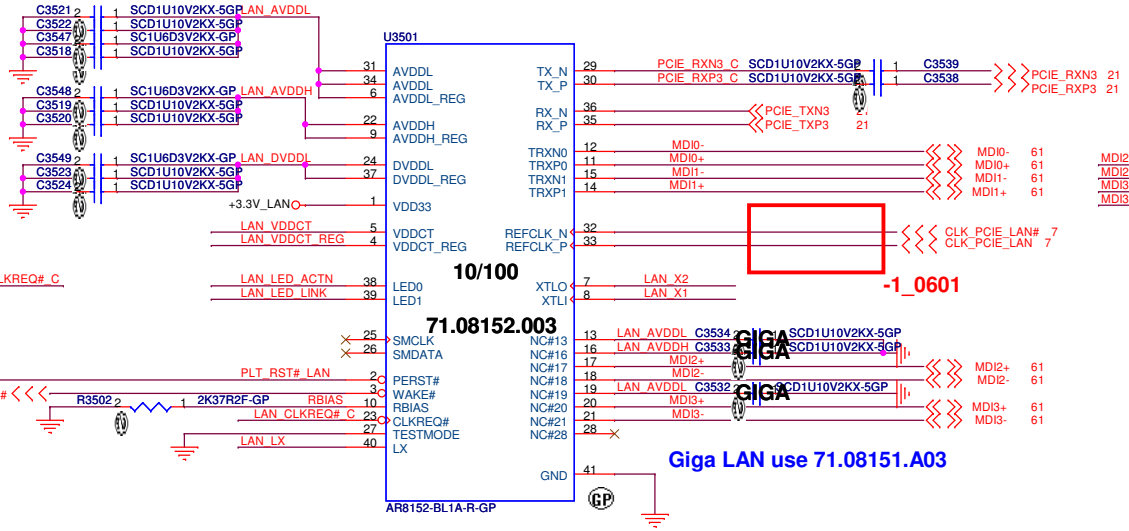
-1_0521



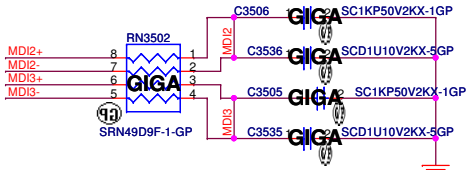


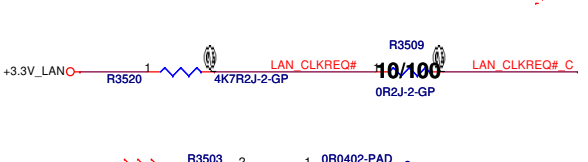
Pin6 is the AVDDL LDO output, 1uF+0.1uF(C3547 and C3518) close to Pin6;
C3522, C3521 close to Pin31, Pin34 respectively.
Pin9 is the AVDDH LDO output, 1uF+0.1uF(C3548 and C3519) close to Pin9;
C3520 close to Pin22.
Pin37 is the DVDDL LDO output, 1uF+0.1uF(C3549 and C3523) close to Pin37;
C3524 close to Pin24.

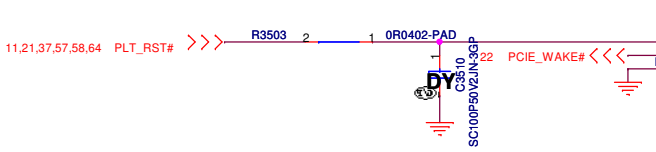




-1_0601

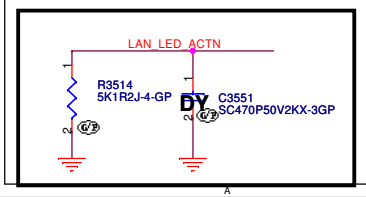




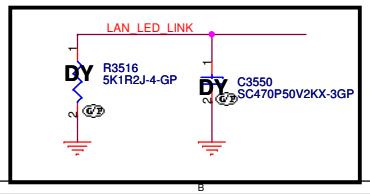


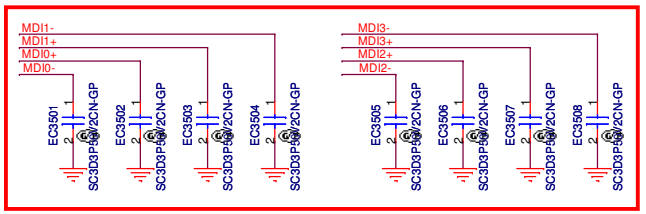
Giga LAN use 71.08151.A03

If overclocking, de-pop R3514



If use LDO mode, pop R3516





-1_0601
for EMI

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AR8152/AR8151

Size: A3 | Document Number: DJ2 Montevina UMA | Rev: X00

Date: Wednesday, June 02, 2010 | Sheet 35 of 88

SSID = KBC

CAP close to VCC-GND pin pair

PH for DJ1/DJ2
PL for DJ3

PH for DJ1
PL for DJ2/DJ3

For RCID Function -1_0516

Layout note:
1. Connect KBC_AGND and GND at one point
2. R3725 close to Pin 103 (AGND)

MB VERSION ID

	VER2	VER1	VER0
X00	0	0	0
A00	0	0	1
	0	1	0
	0	1	1

KBC CLK
EMI

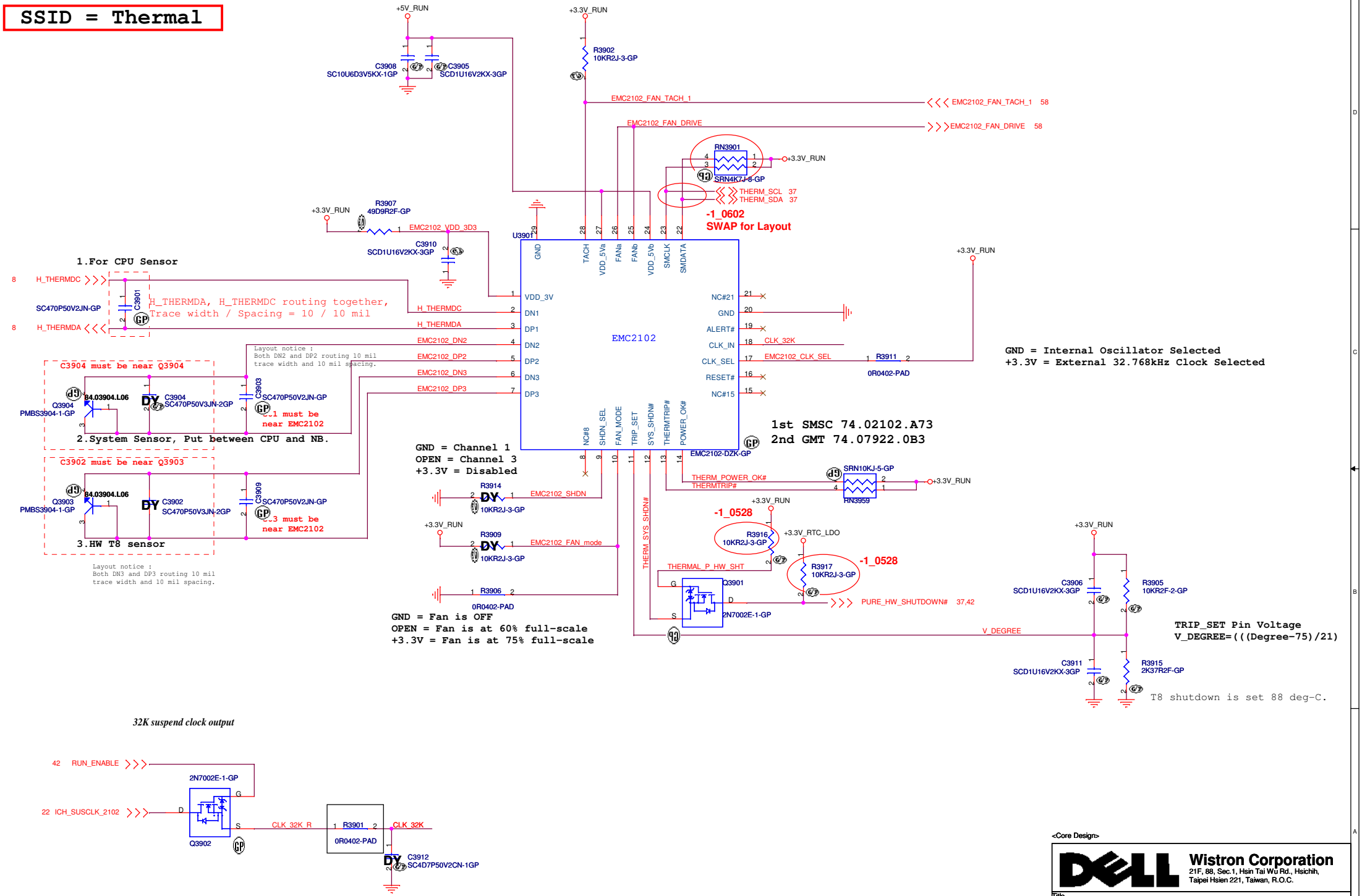
U3701A — NPCE781BA0DX-GP (1 OF 2)
U3701B — NPCE781BA0DX-GP (2 OF 2)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE781BA0DX
Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00
Date: Wednesday, June 02, 2010 | Sheet 37 of 88

SSID = Thermal



<Core Design>

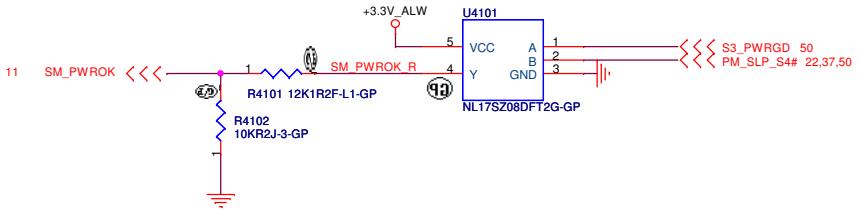
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size	Document Number	Rev
Custom	DJ2 Montevina UMA	X00

Date: Wednesday, June 02, 2010 Sheet 39 of 88

SSID = Reset.Suspend



<Core Design>

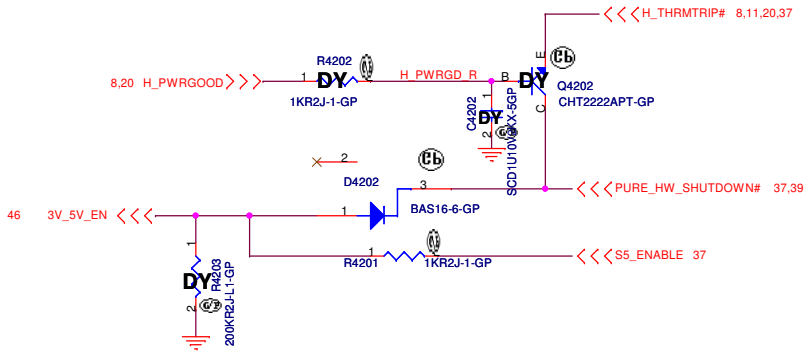
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power On Logic

Size: A3 | Document Number: DJ2 Montevina UMA | Rev: X00

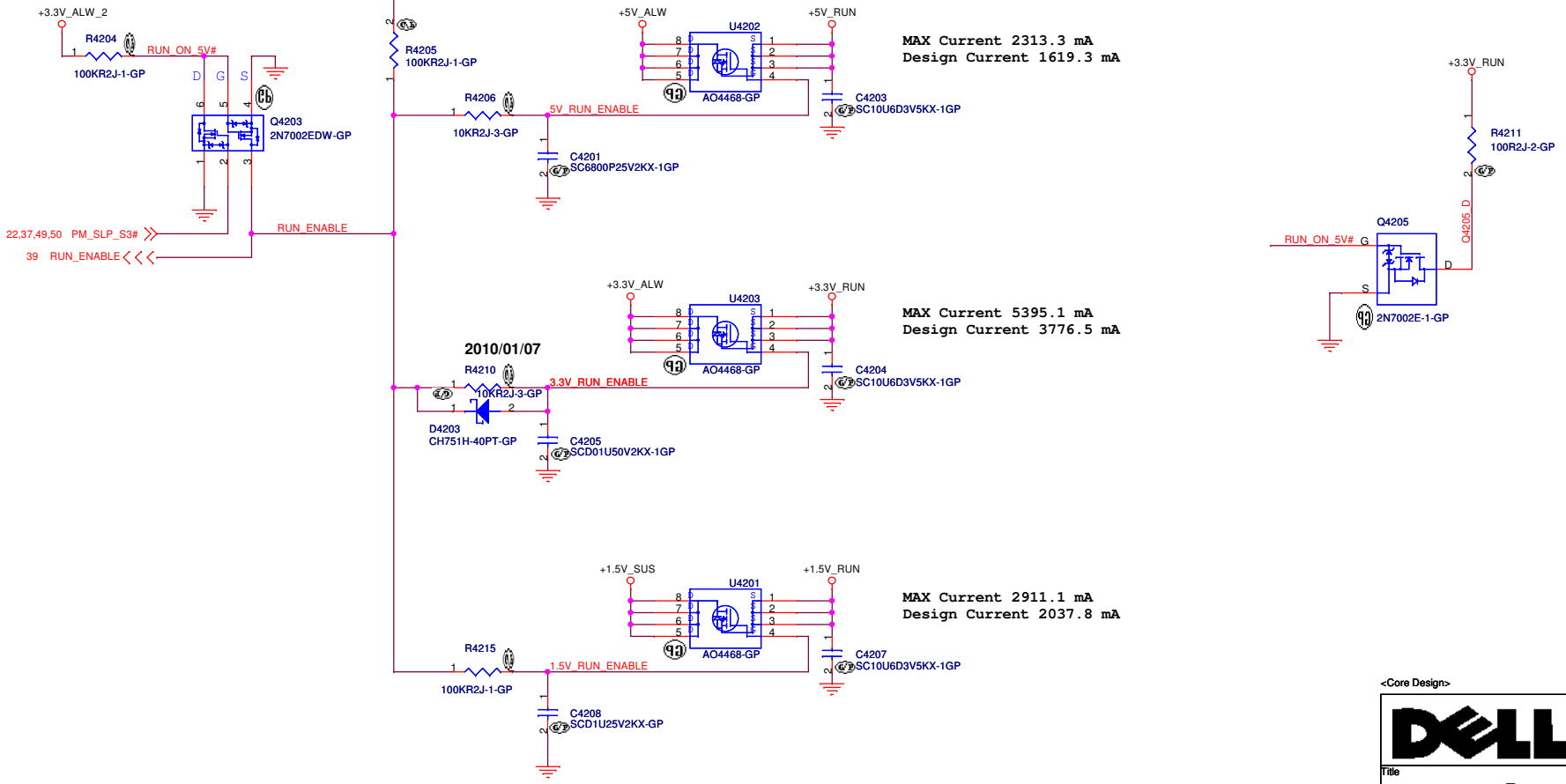
Date: Wednesday, June 02, 2010 | Sheet 41 of 88

SSID = Reset.Suspend



Run Power

AO4468 MAX 11.6A
RDS(ON) < 14mΩ (VGS = 10V)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

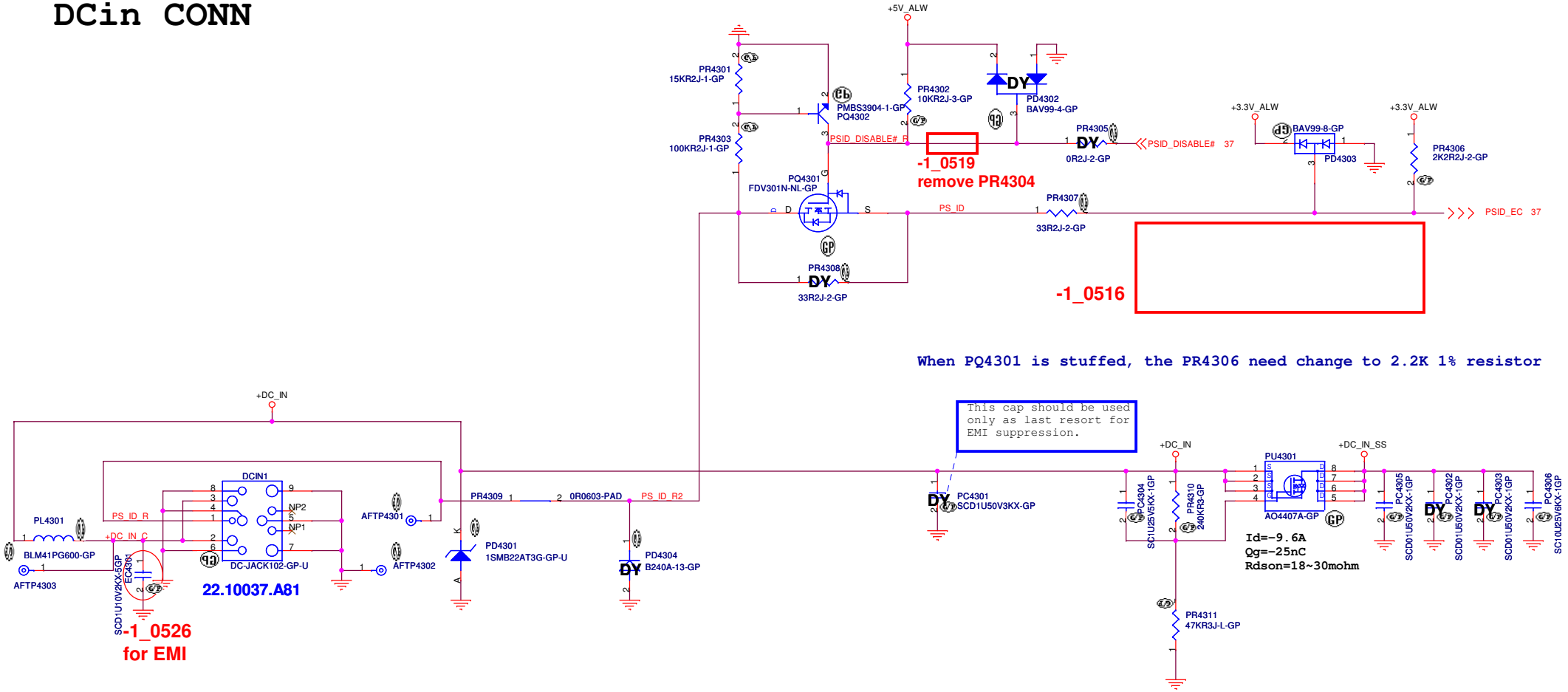
Title: Power Plane Enable

Size	Document Number	Rev
A3	DJ2 Montevina UMA	X00

Date: Wednesday, June 02, 2010 Sheet 42 of 88

SSID = PWR.Support

DCin CONN

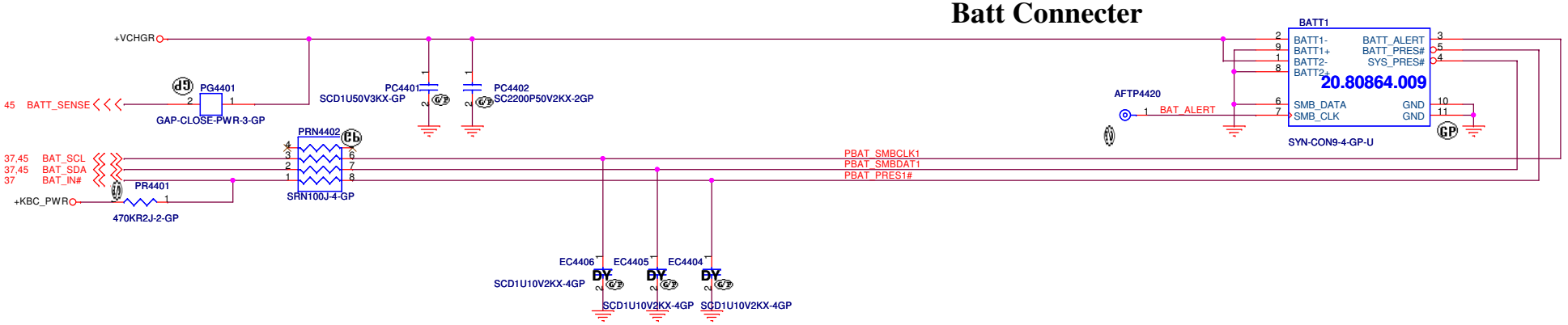


<Core Design>

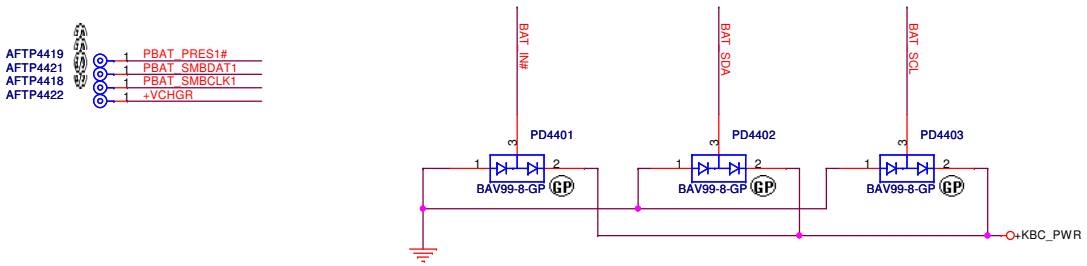
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN Jack		
Size: A3	Document Number: DJ2 Montevina UMA	Rev: X00
Date: Wednesday, June 02, 2010	Sheet 43 of 88	

Batt Connecter



EC404,EC405,EC406 Close BATT1 Connector

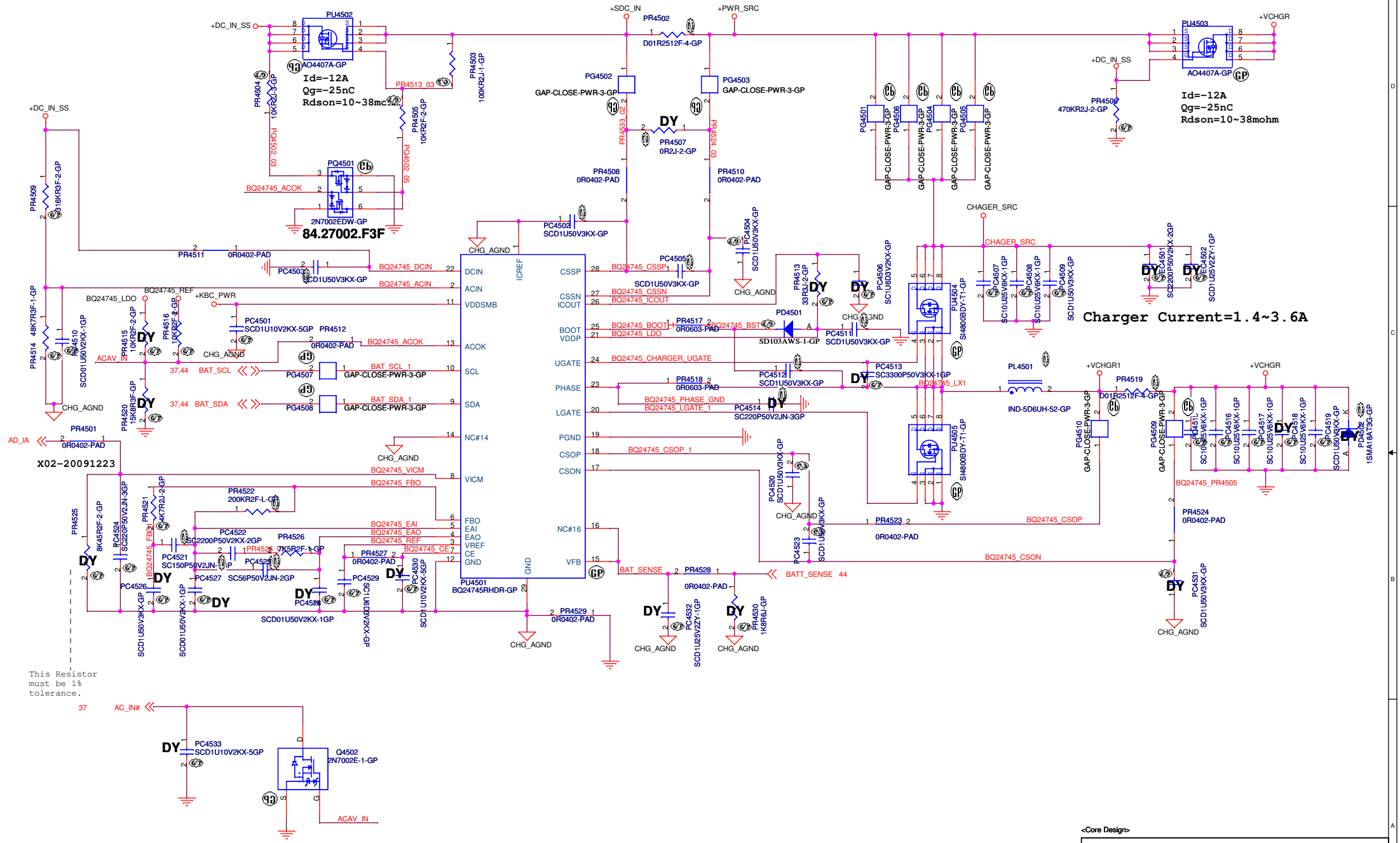


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN		
Size: A3	Document Number: DJ2 Montevina UMA	Rev: X00
Date: Wednesday, June 02, 2010	Sheet 44 of 88	

SSID = Charger



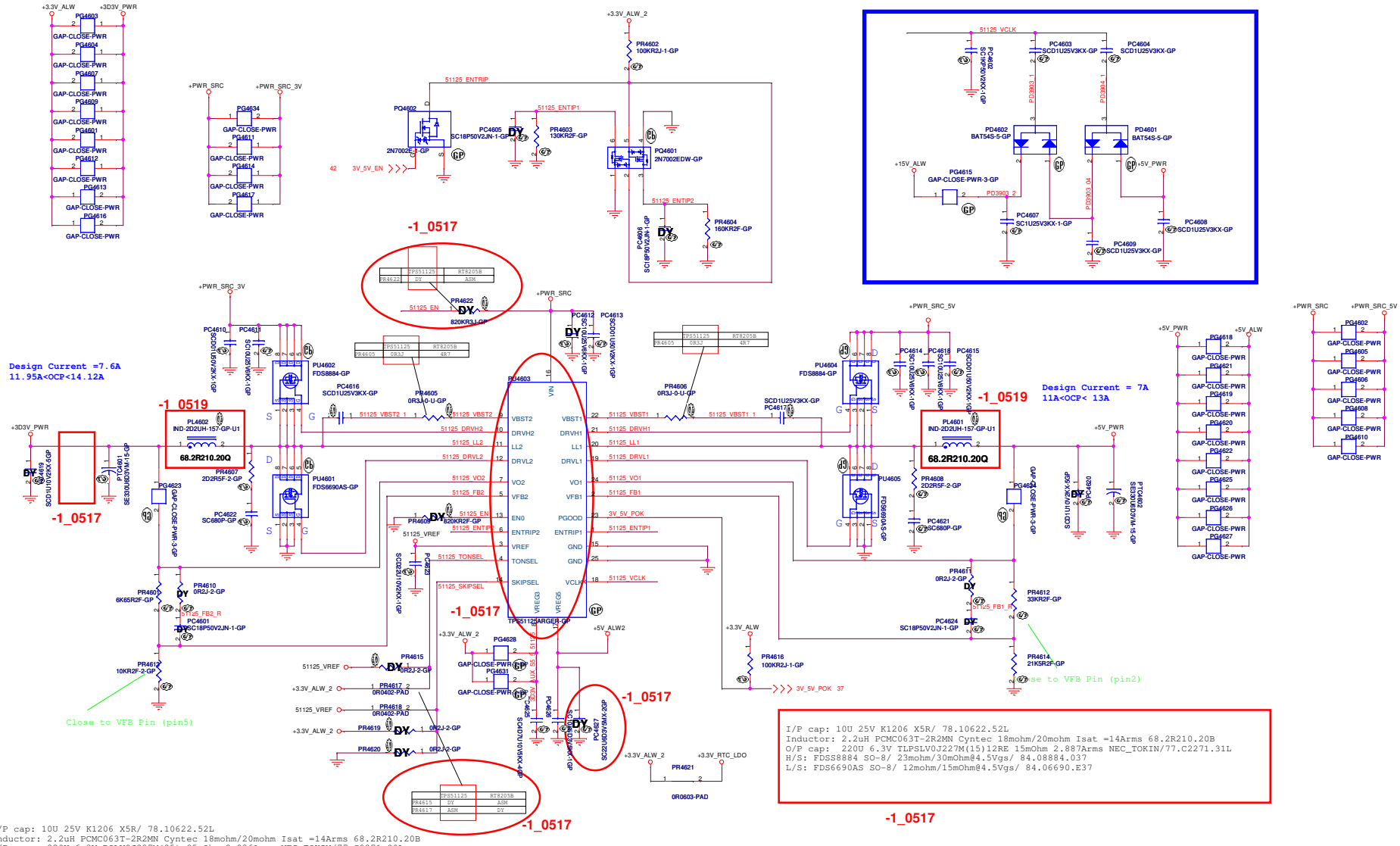
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00

Date: Wednesday, June 02, 2010 | Sheet 45 of 88



TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

RT8205B:

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

<Core Design>

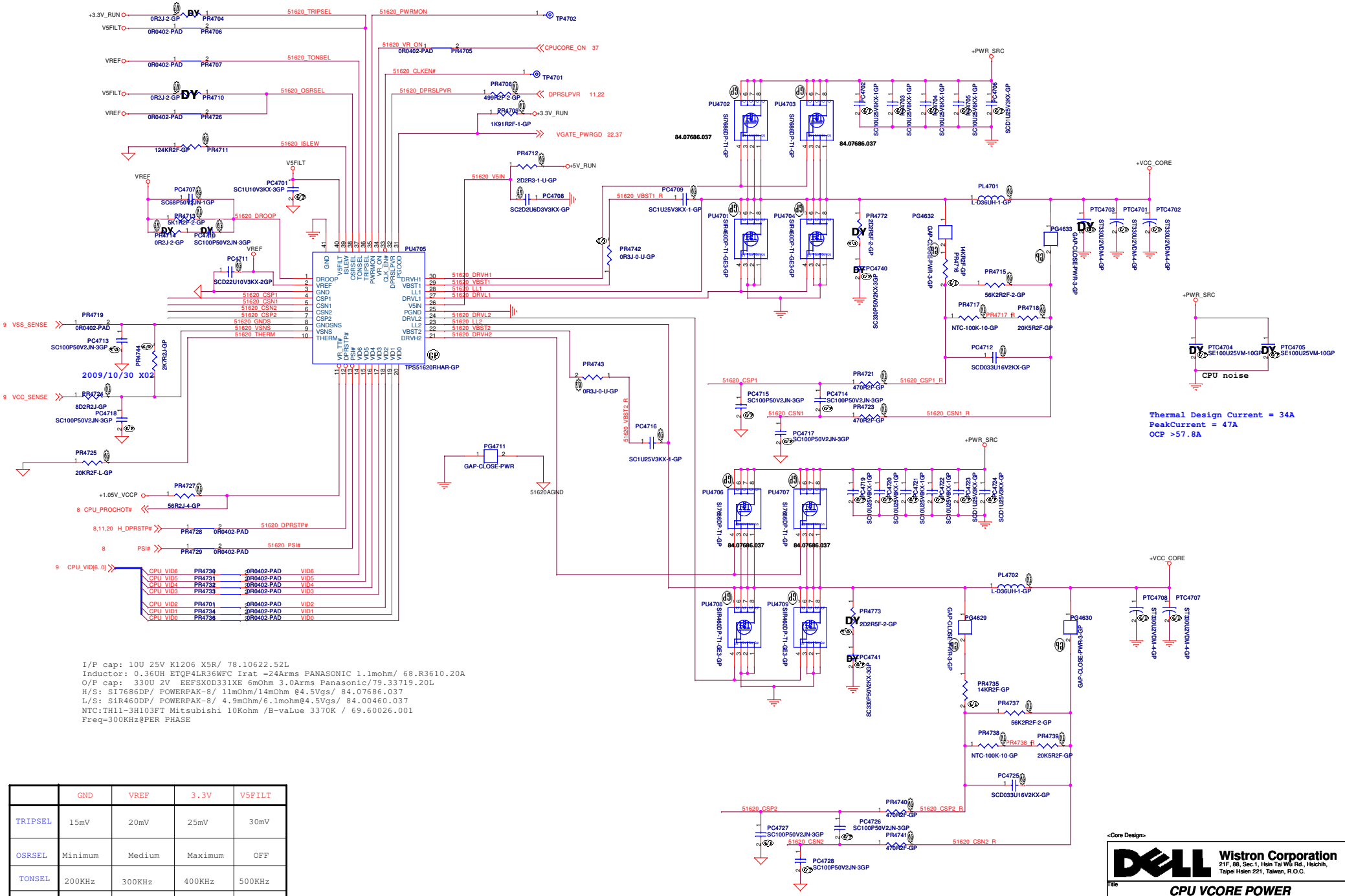
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51125_5V/3D3V

Size: A2 | Document Number: DJ2 Montevina UMA | Rev: X00

Date: Wednesday, June 02, 2010 | Sheet 46 of 88

SSID = CPU.Regulator



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC Irat =24Arms PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.0Arms Panasonic/79.33719.20L
H/S: SI7686DP/ POWERPAK-8/ 11mOhm/14mOhm @4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
NTC:TH11-3H103FT Mitsubishi 10Kohm /B-vaLue 3370K / 69.60026.001
Freq=300KHz@PER PHASE

	GND	VREF	3.3V	V5FILT
TRIPSEL	15mV	20mV	25mV	30mV
OSRSEL	Minimum	Medium	Maximum	OFF
TONSEL	200KHz	300KHz	400KHz	500KHz
OVPSEL	ENABLE	DISABLE	N/A	N/A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

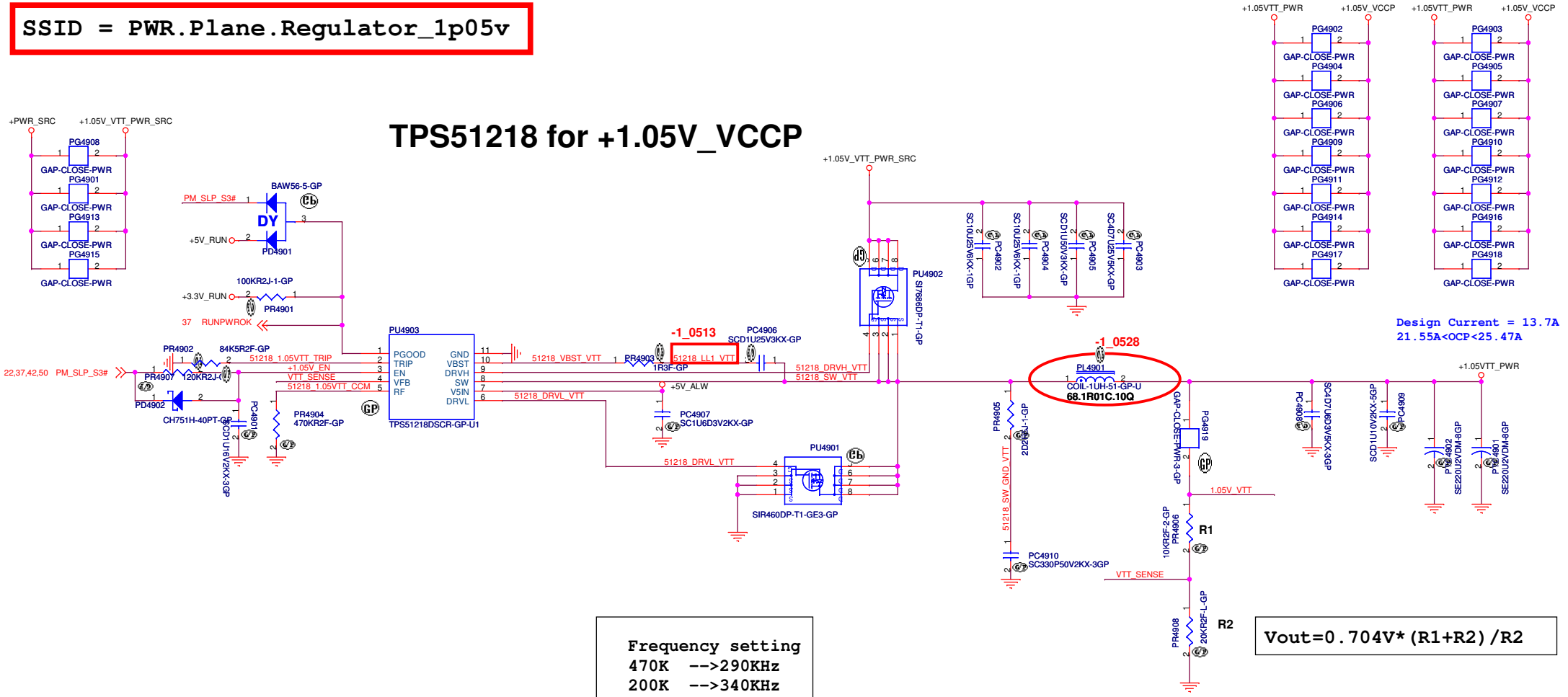
Title: CPU VCORE POWER

Size	Document Number	Rev
Custom	DJ2 Montevina UMA	X00

Date: Wednesday, June 02, 2010 Sheet 47 of 88

SSID = PWR.Plane.Regulator_1p05v

TPS51218 for +1.05V_VCCP



Design Current = 13.7A
21.55A<OCP<25.47A

Frequency setting
470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

Vout=0.704V*(R1+R2)/R2

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1uH FDUE1040D-1R0M=P3 TOKO DCR:2.35mohm Isat =17.9Arms 68.1R01B.10A
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP-T1-E3/11mohm/ 14mOhm@4.5Vgs/ 84.07686.037
L/S: SIR460DP-T1-GE3-GP/4.5mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

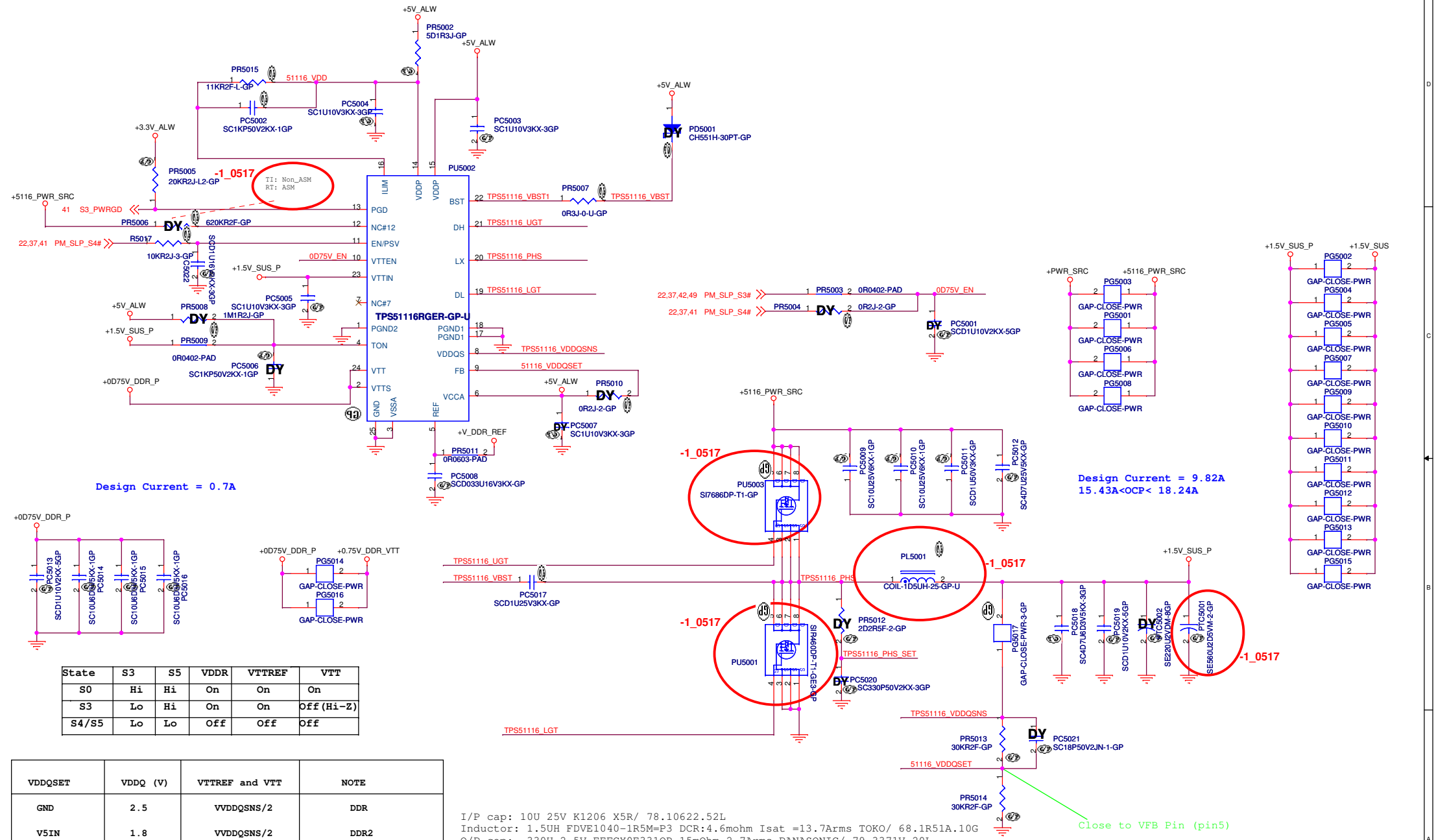
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218 +1.05V VCCP

Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00

Date: Wednesday, June 02, 2010 | Sheet 49 of 88

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH FDVE1040-1R5M=P3 DCR:4.6mohm Isat =13.7Arms TOKO/ 68.1R51A.10G
O/P cap: 330U 2.5V EEFCX0E331QR 15mOhm 2.7Arms PANASONIC/ 79.3371V.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

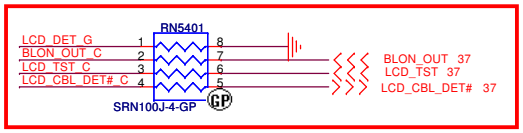
Title: TPS51116 +1.5V SUS

Size: Custom | Document Number: DJ2 Montevina UMA | Rev: X00

Date: Wednesday, June 02, 2010 | Sheet 50 of 88

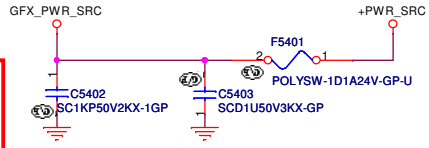
SSID = VIDEO

SSID = Inverter

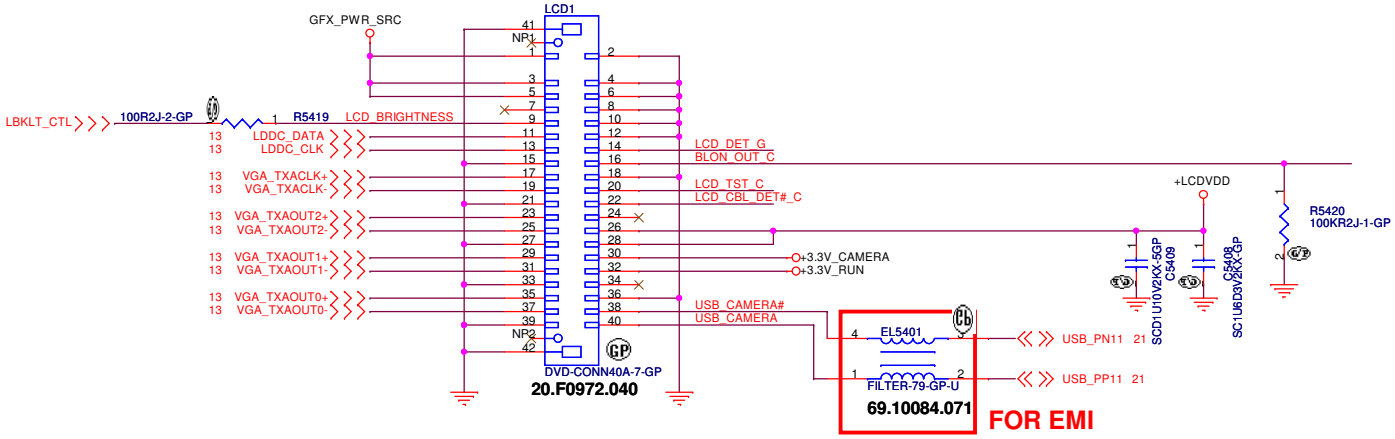


-1_0526
SWAP for Layout

INVERTER POWER



LVDS CONNECTOR

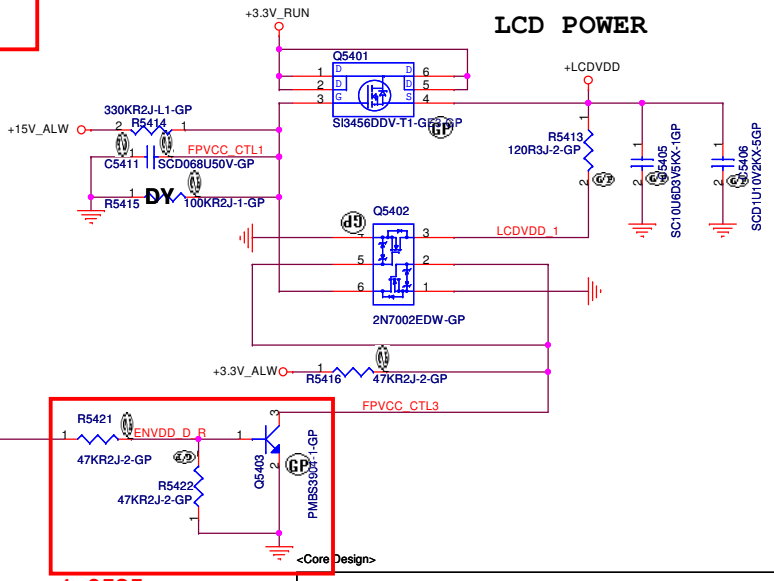


-1_0520

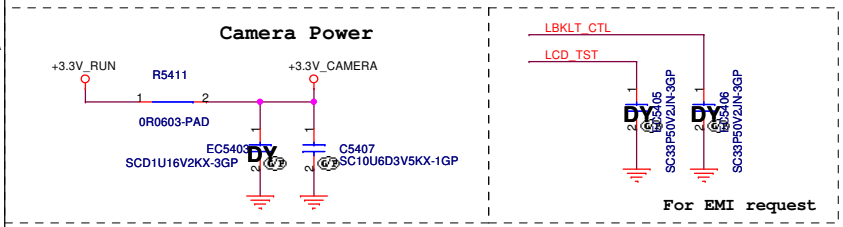
-1_0512

SSID = VIDEO

LCD POWER



-1_0525



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

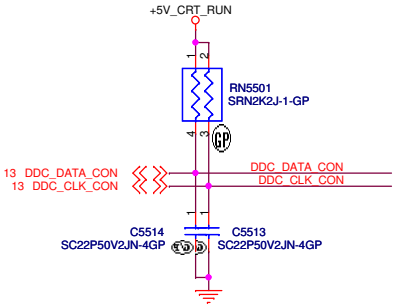
Size	Document Number	Rev
A3	DJ2 Montevina UMA	X00

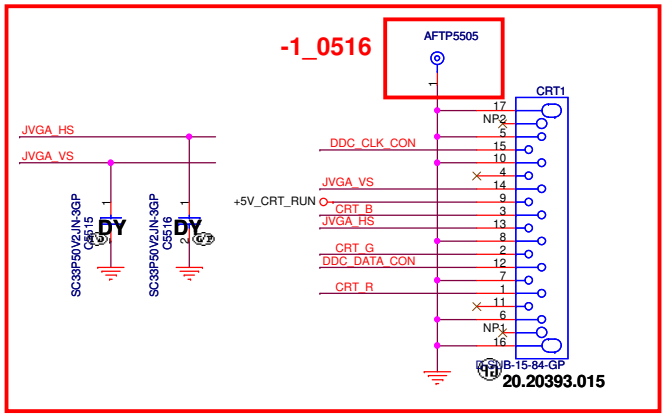
Date: Wednesday, June 02, 2010 Sheet 54 of 88

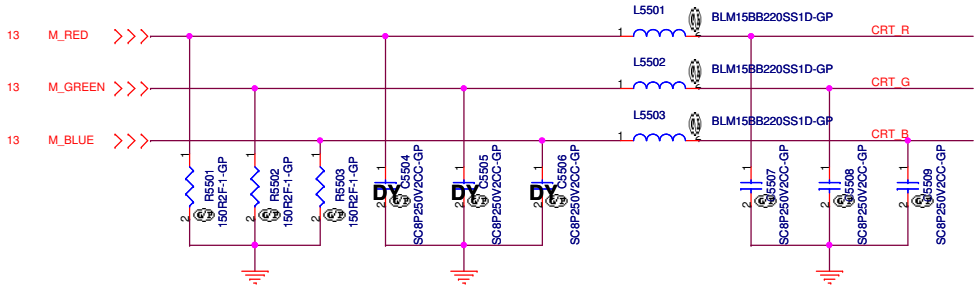
SSID = VIDEO

Layout Note:

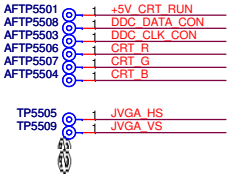
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

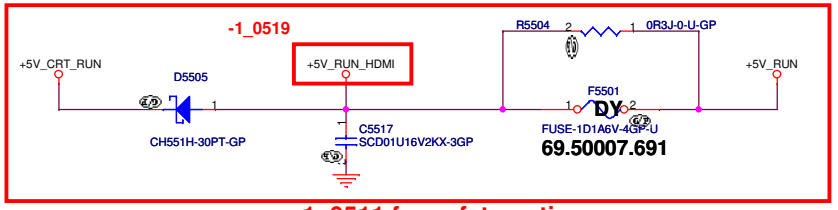






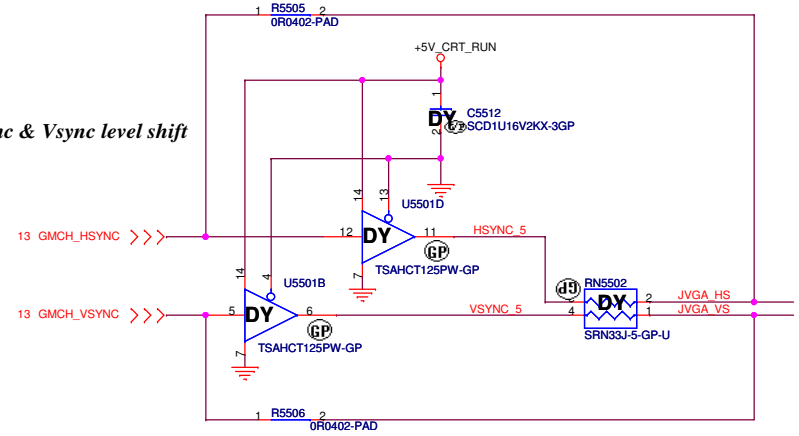
-1_0511

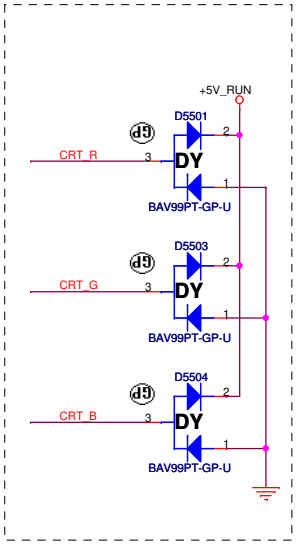


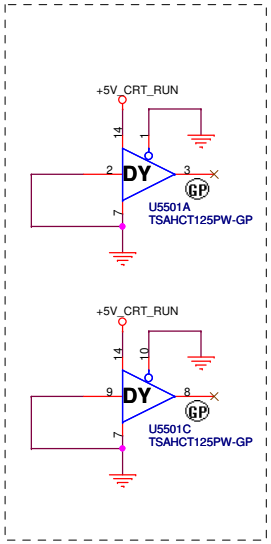


-1_0511 for safety option

Hsync & Vsync level shift







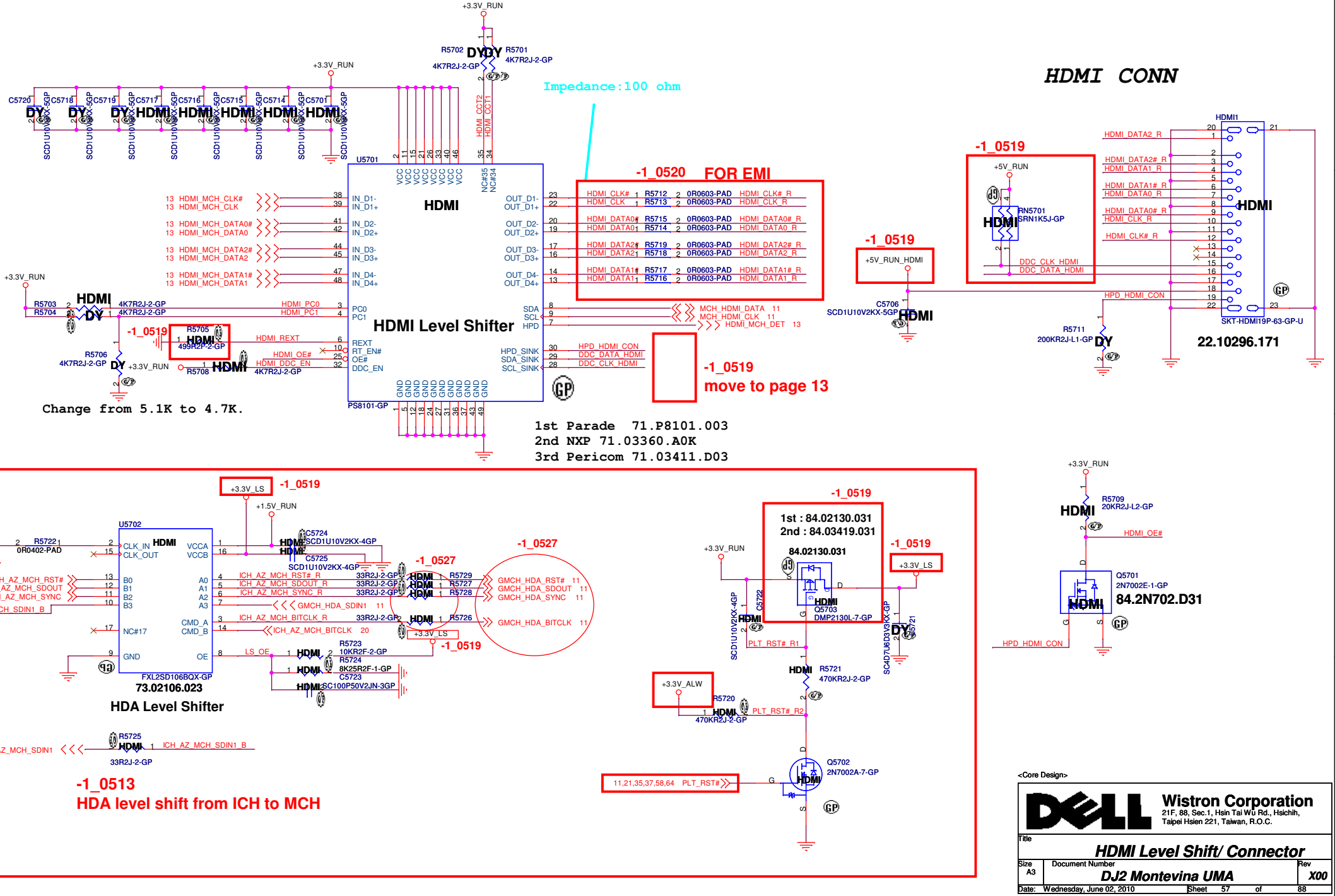
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector
Size | Document Number: DJ2 Montevina UMA | Rev: X00
Date: Wednesday, June 02, 2010 | Sheet 55 of 88

SSID = VIDEO

HDMI Level Shifter & CONNECTOR



<Core Design>

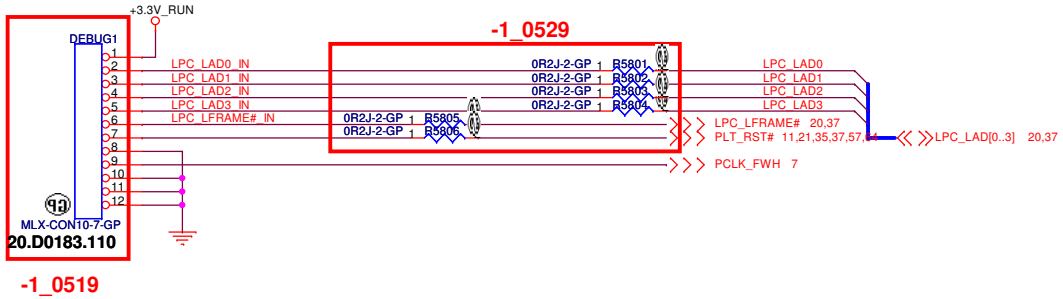
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shift/ Connector

Size	Document Number	Rev
A3	DJ2 Montevina UMA	X00

Date: Wednesday, June 02, 2010 Sheet 57 of 88

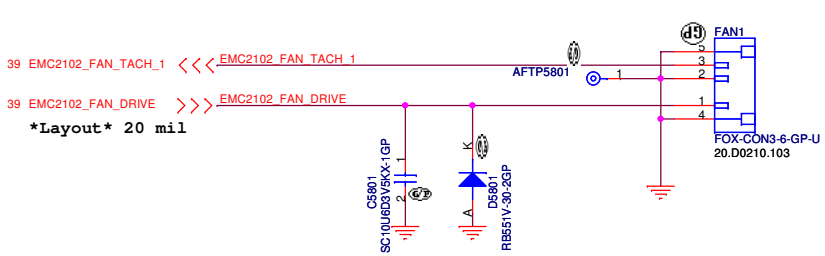
SSID = User.Interface

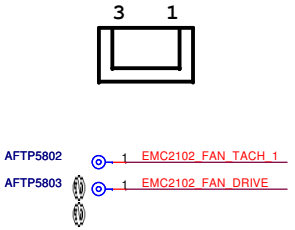


-1_0529

SSID = Thermal

Fan Connector





<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

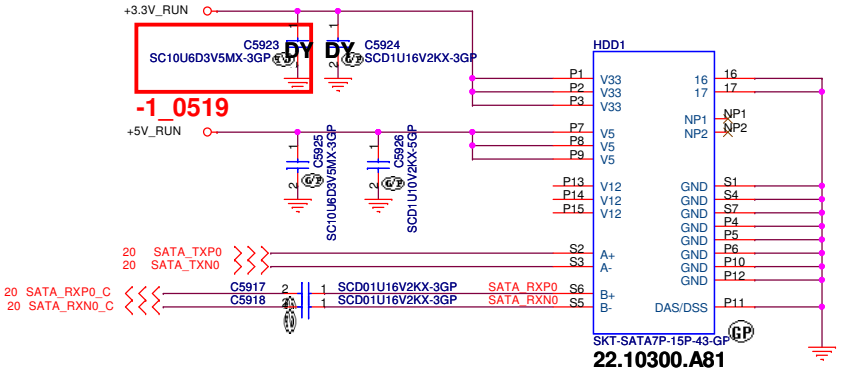
Title: ITP/Fan Connector

Size: A3 | Document Number: DJ2 Montevina UMA | Rev: X00

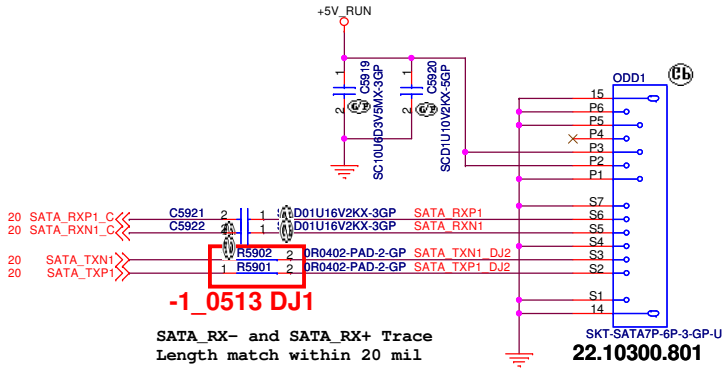
Date: Wednesday, June 02, 2010 | Sheet 58 of 88

SSID = SATA

SATA HDD Connector



ODD Connector



<Core Design>

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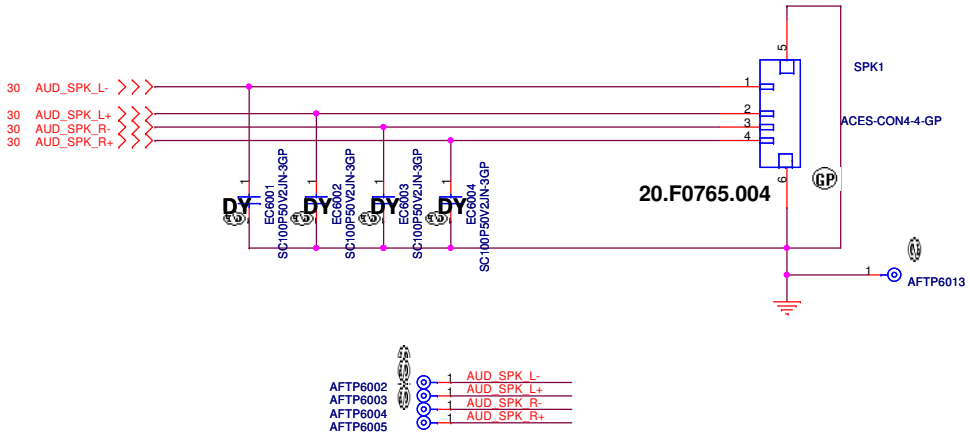
Taipei Hsien 221, Taiwan, R.O.C.

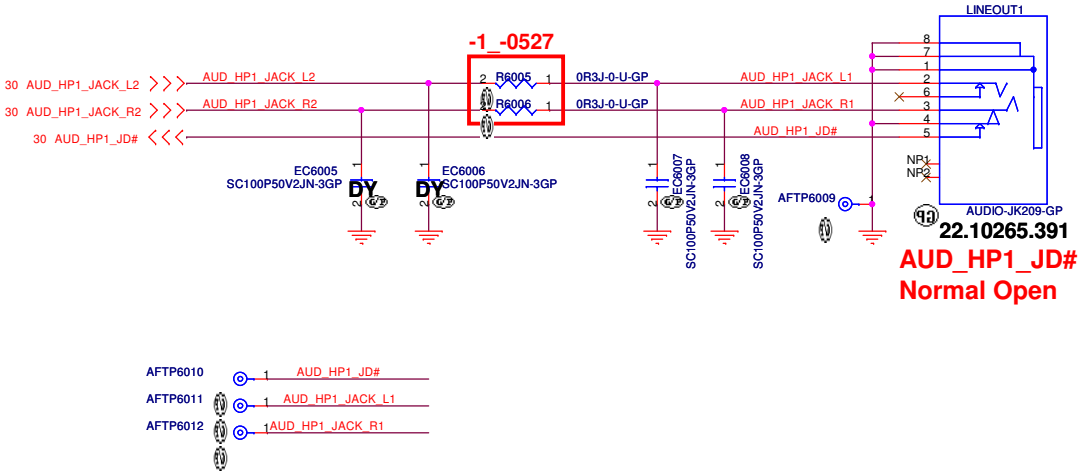
Title: HDD/ODD		
Size: A3	Document Number: DJ2 Montevina UMA	Rev: X00
Date: Wednesday, June 02, 2010	Sheet 59 of 88	

SSID = AUDIO

Speaker Connector

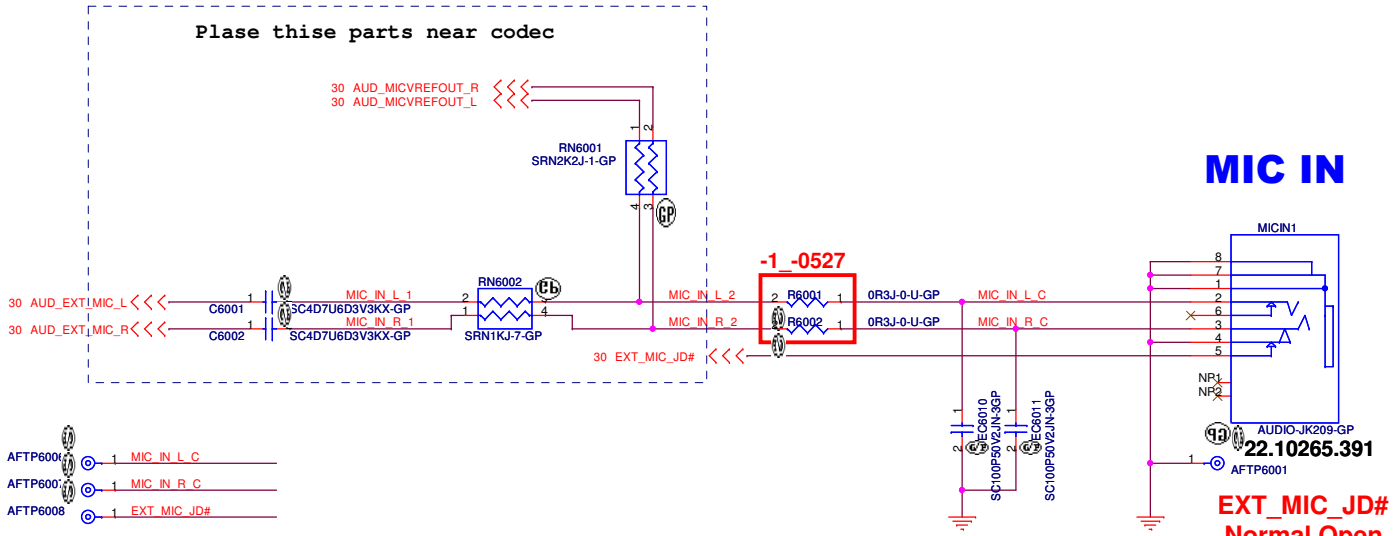


LINE1 OUT



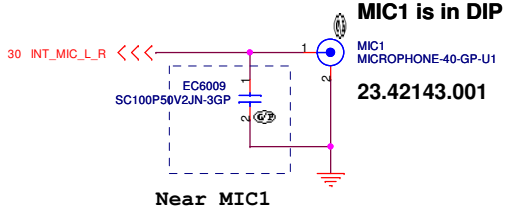
AUD_HP1_JD#
Normal Open

MIC IN



EXT_MIC_JD#
Normal Open

Internal Microphone



<Core Design>

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Title: Audio Jack

Size	Document Number	Rev
A3	DJ2 Montevina UMA	X00

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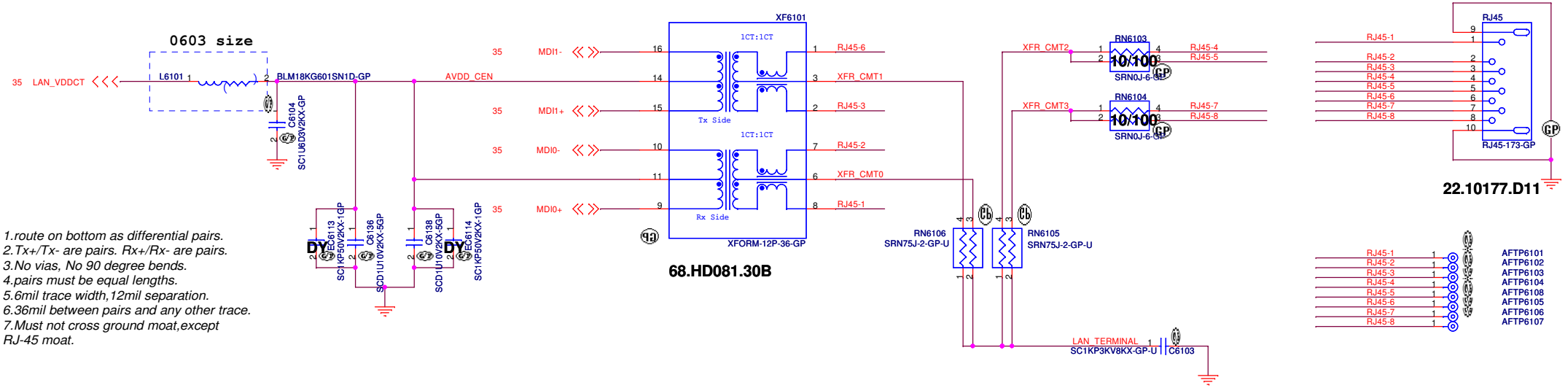
2009-10-1 Change MDI1+(XF601.16) to MDI1+(XF601.15)
Change MDI1-(XF601.15) to MDI1-(XF601.16)
Change MDI0+(XF601.10) to MDI0+(XF601.9)
Change MDI0-(XF601.9) to MDI0-(XF601.10)
Change RJ45-3(XF601.1) to RJ45-3(XF601.2)
Change RJ45-6(XF601.2) to RJ45-6(XF601.1)
Change RJ45-1(XF601.7) to RJ45-1(XF601.8)
Change RJ45-2(XF601.8) to RJ45-2(XF601.7)

-1_0601
Remove for EMI

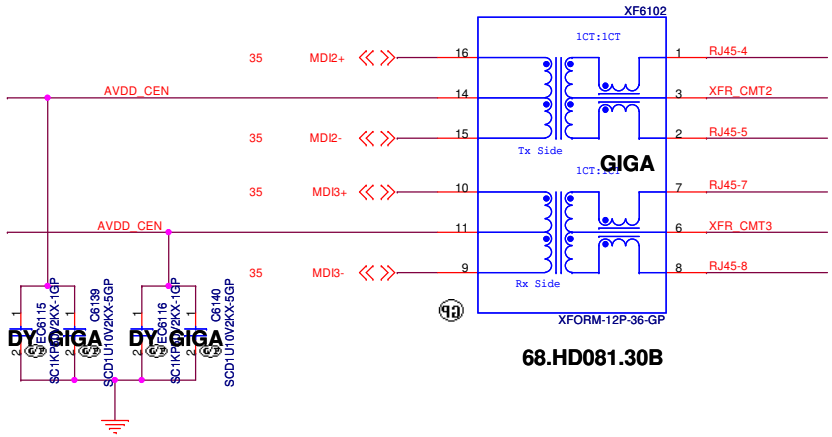
RJ45 Connector

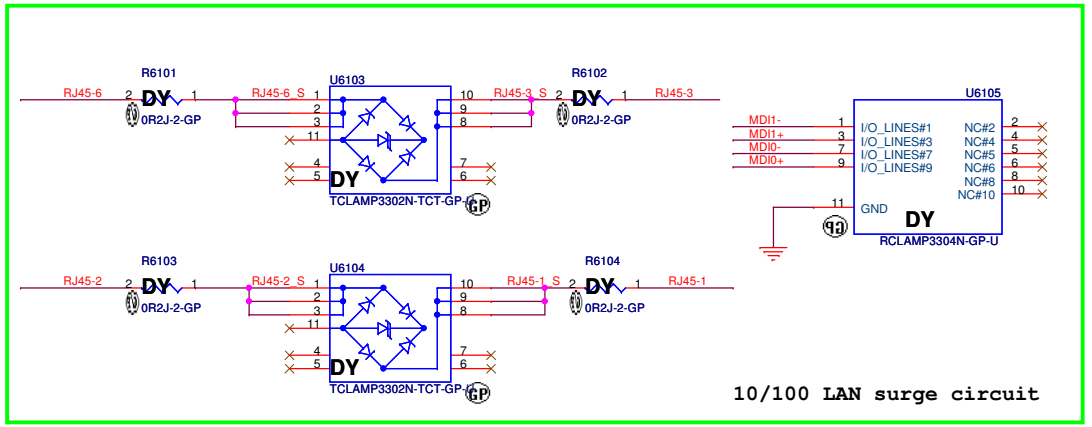
10/100M Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

LAN differential signals use 100 Ohm impedance





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

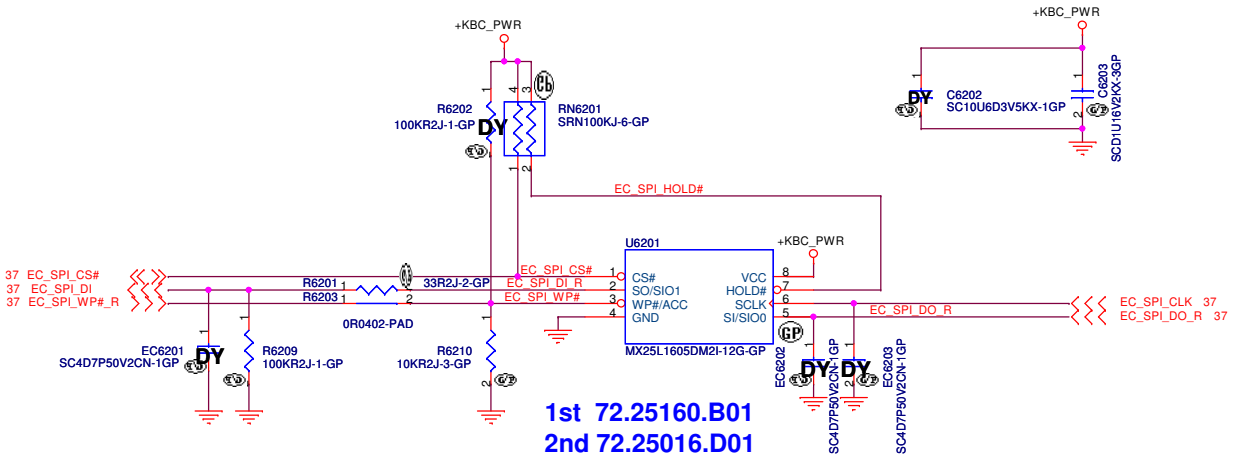
Title: XFORM/RJ45

Size	Document Number	Rev
A3	DJ2 Montevina UMA	X00

Date: Wednesday, June 02, 2010 Sheet 61 of 88

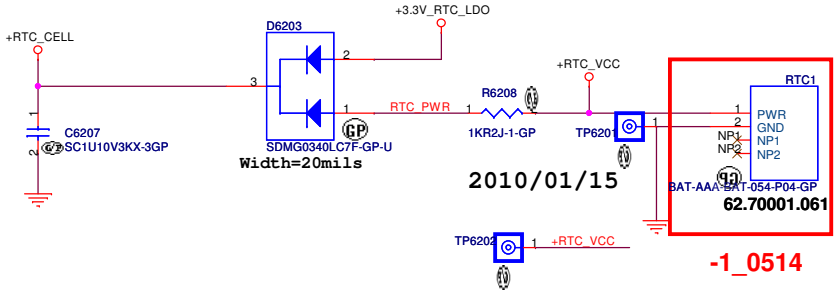
SSID = Flash.ROM

SPI FLASH ROM (16M bits) for KBC



SSID = RBATT

RTC Connector



<Core Design>

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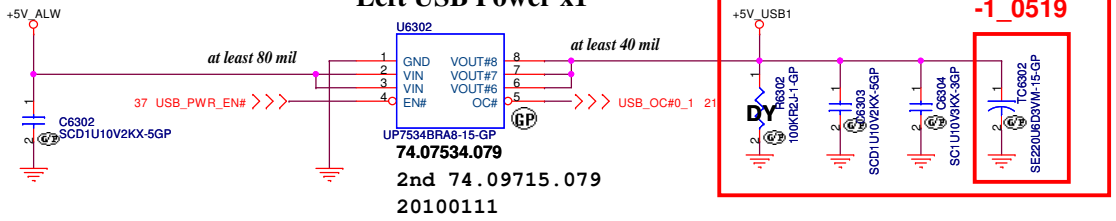
Title	Flash/RTC	
Size: A3	Document Number: DJ2 Montevina UMA	Rev: X00
Date: Wednesday, June 02, 2010	Sheet 62 of 88	

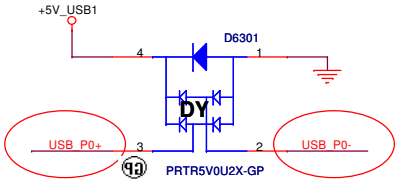
SSID = USB

Left USB Power x1



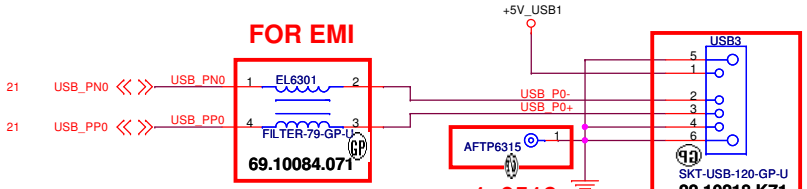
-1_0519

-1_0510



-1_0526
SWAP for Layout

FOR EMI

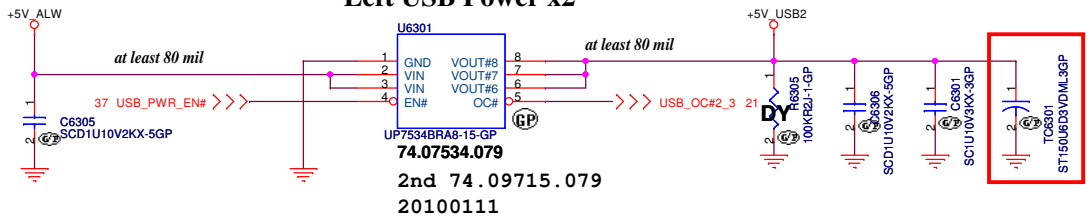


-1_0526
SWAP for Layout

-1_0516

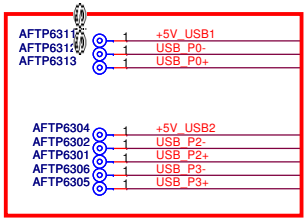
-1_0510

Left USB Power x2



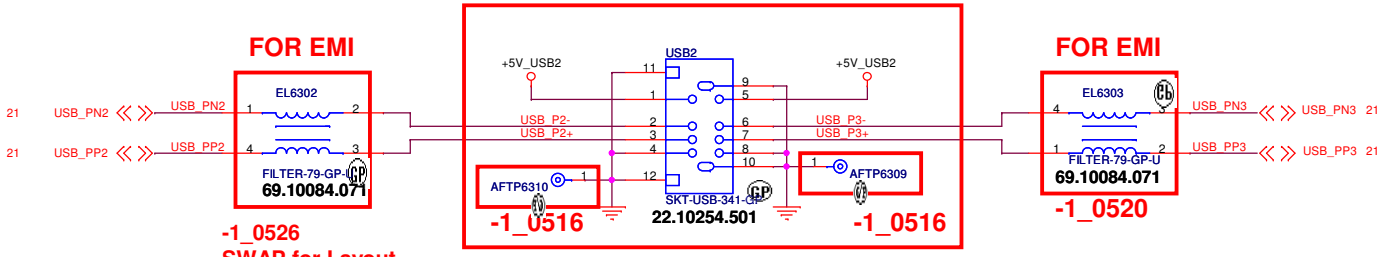
-1_0527
for layout

-1_0526
remove D6302 6303 for EMI



-1_0516

FOR EMI



-1_0526
SWAP for Layout

-1_0516

-1_0510

-1_0516

-1_0520

<Core Design>

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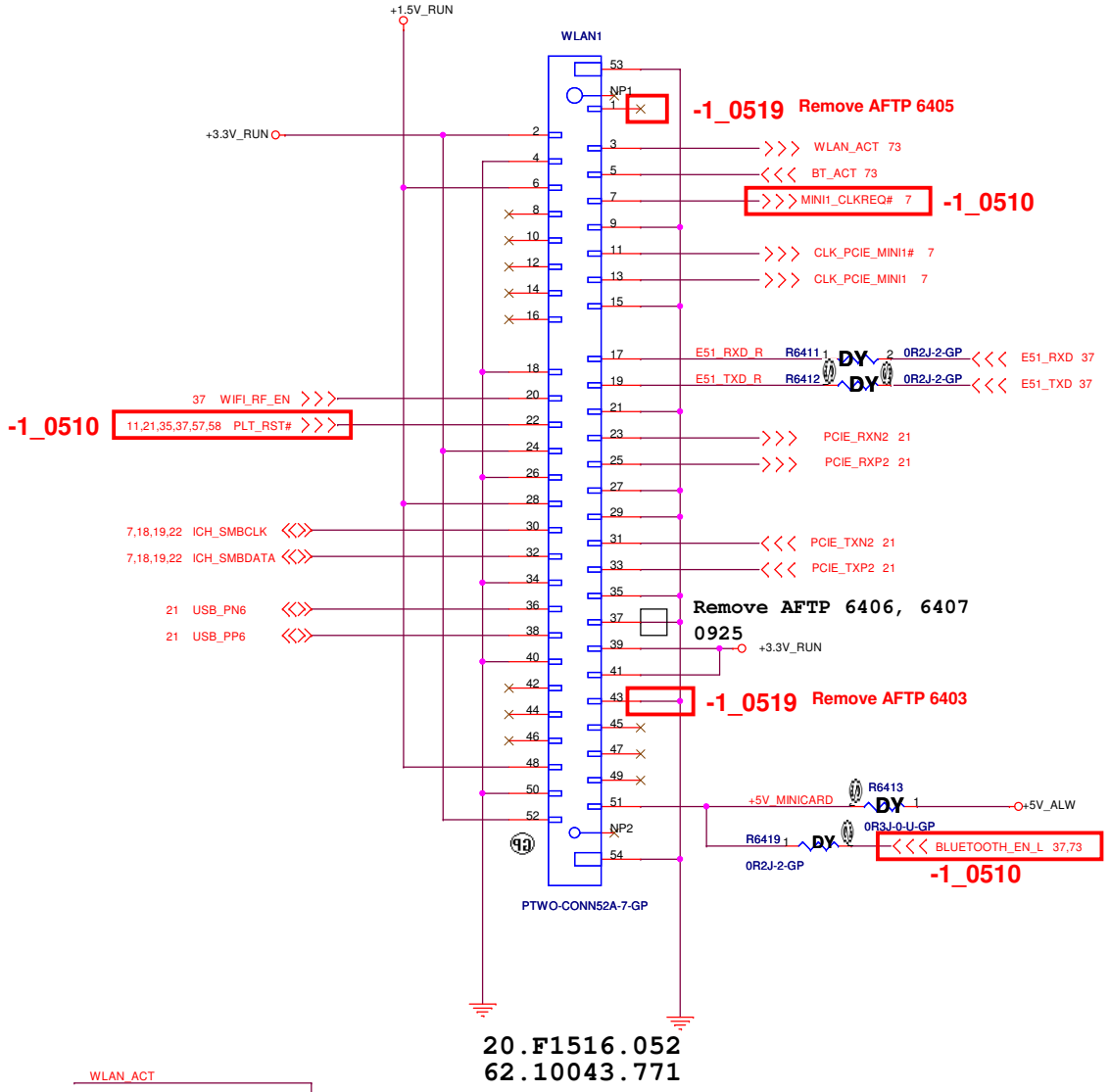
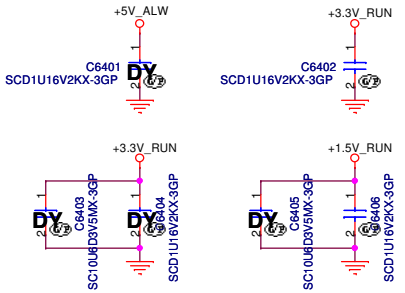
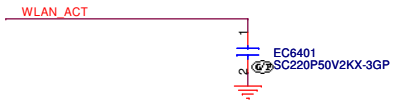
Title	*USB*	
Size	Document Number: *DJ2 Montevina UMA*	Rev: *X00*
Date: Wednesday, June 02, 2010	Sheet 63 of 88	

Mini Card Connector(802.11a/b/g)

SSID = Wireless







<Core Design>

Wistron Corporation
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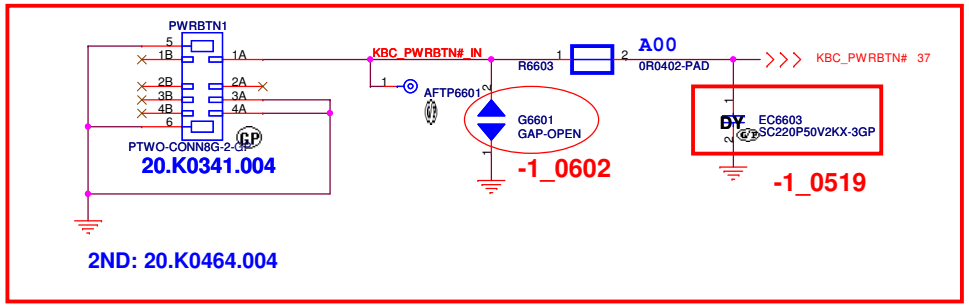
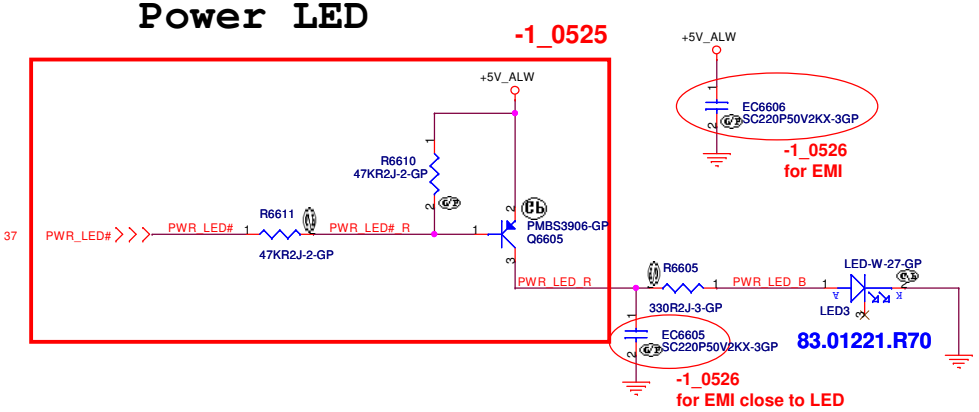
Title			
MINICARD			
Size: A3	Document Number: DJ2 Montevina UMA		Rev: X00
Date: Wednesday, June 02, 2010	Sheet 64 of 88		

SSID = User.Interface

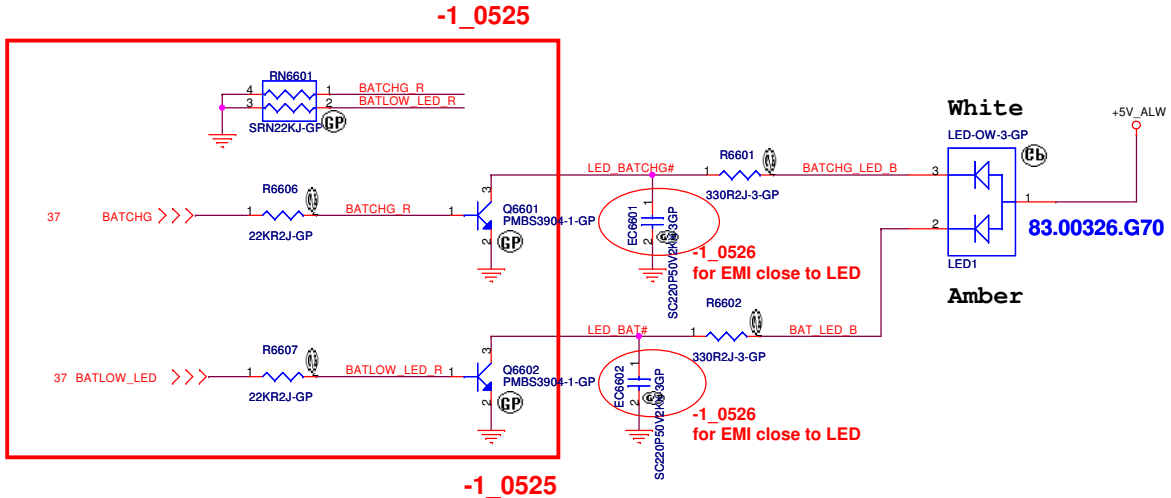
Power BTN Connector



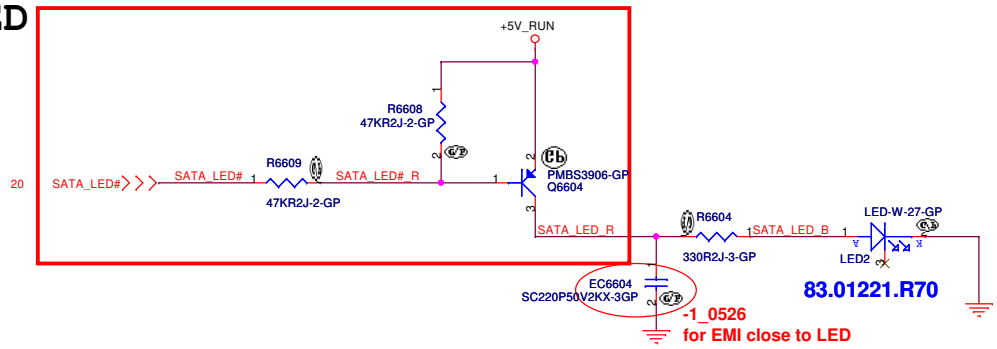
Power LED



Battery LED



HDD LED



<Core Design>

Wistron Corporation
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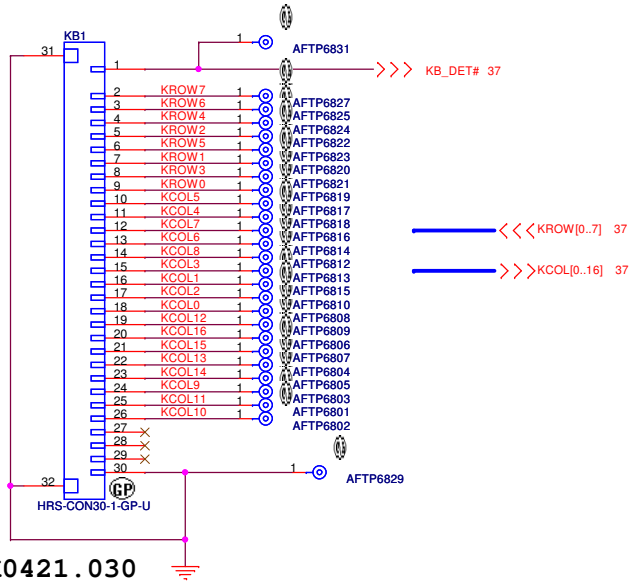
Title: LED

Size	Document Number	Rev
A3	DJ2 Montevina UMA	X00

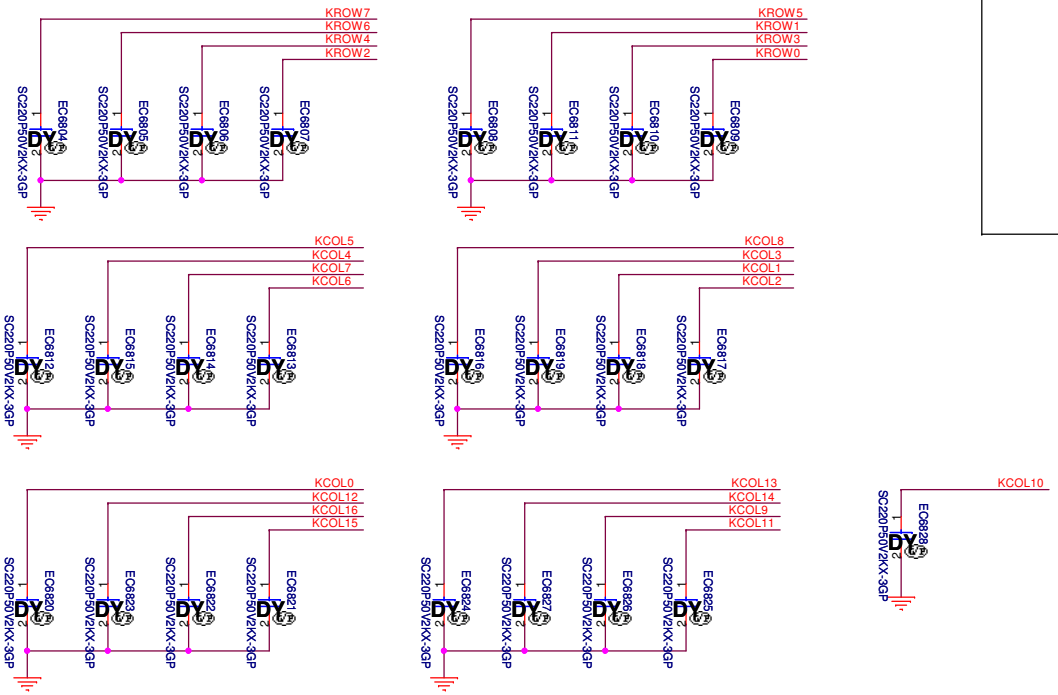
Date: Wednesday, June 02, 2010 Sheet 66 of 88

SSID = KBC

Internal KeyBoard Connector

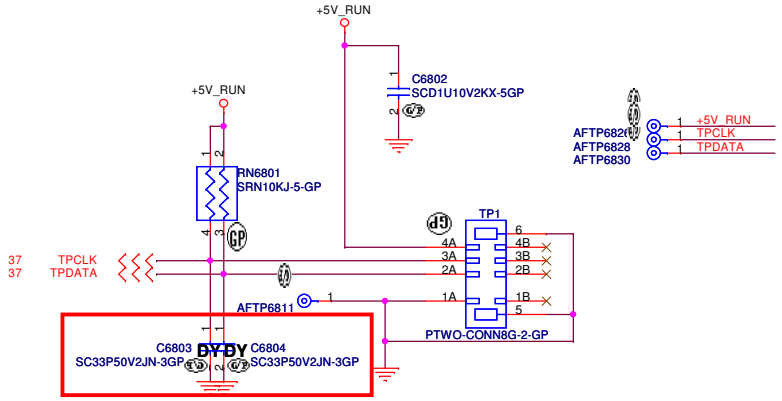


Main 20.K0421.030
20.K0259.030



SSID = Touch.Pad

TouchPad Connector



-1_0519

<Core Design>

Wistron Corporation
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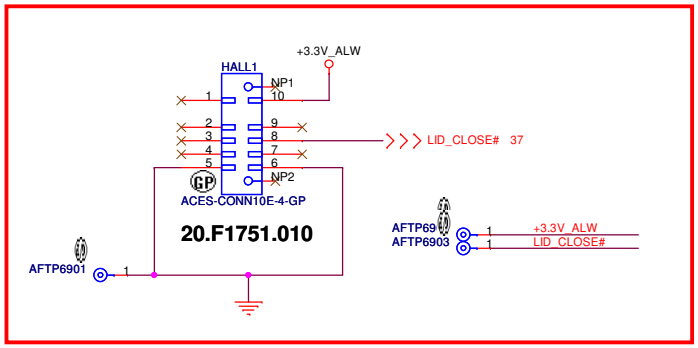
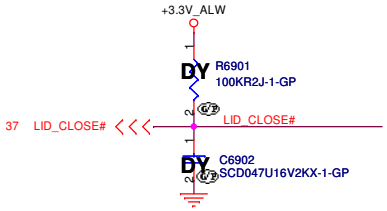
Title	Key Board/Touch Pad	
Size: A3	Document Number: DJ2 Montevina UMA	Rev: X00
Date: Wednesday, June 02, 2010	Sheet 68 of 88	



-1_0511



-1_0516

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Hall Sensor

Size	Document Number	Rev
A3	DJ2 Montevina UMA	X00

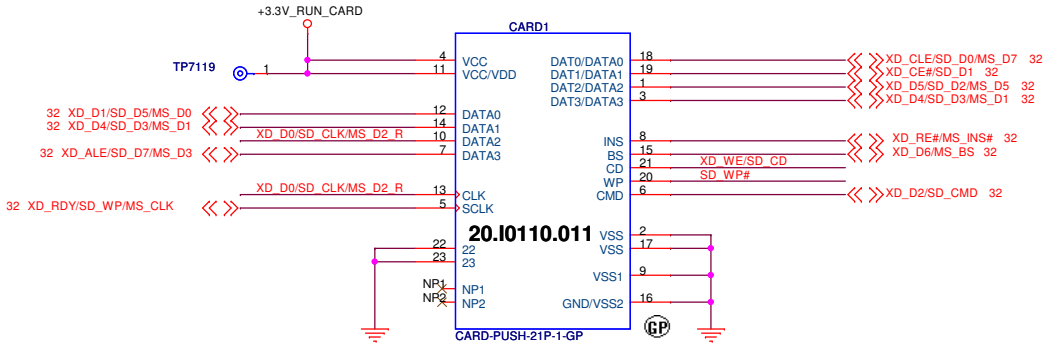
Date: Wednesday, June 02, 2010 Sheet 69 of 88

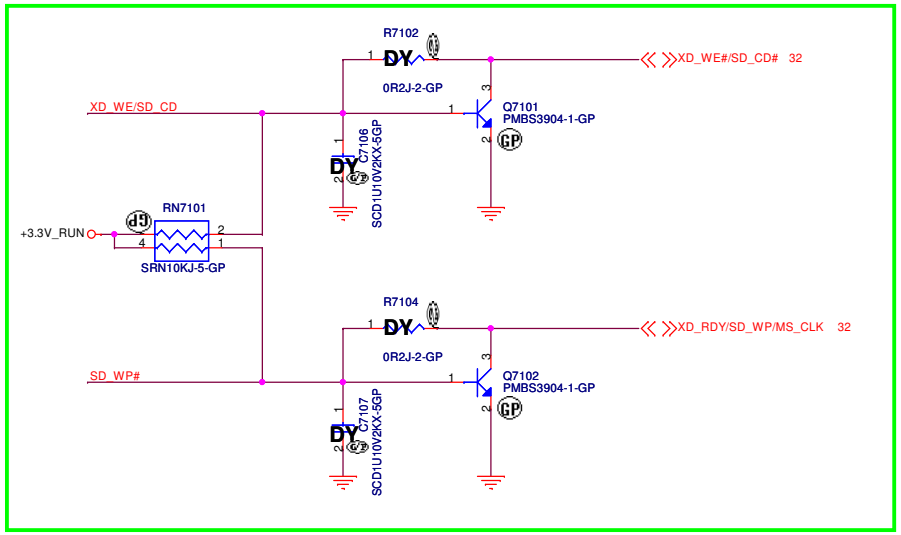
SSID = SDIO

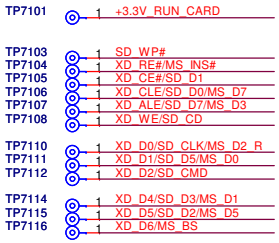
SD/MMC/MS Card Reader

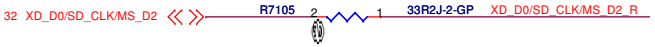
XD_WE/SD_CD
No Card : LO
Inser Card : HI

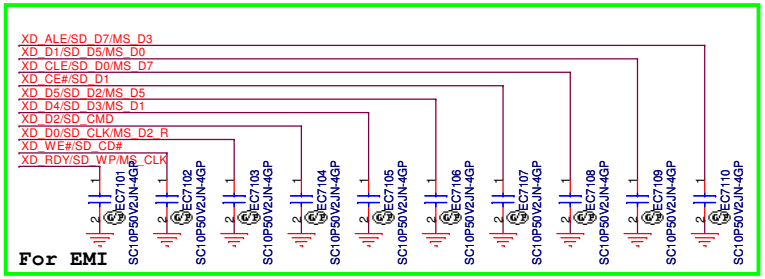
SD_WP#
No Card : LO
Inser Card : HI

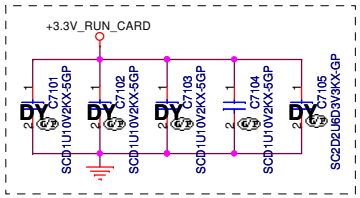












<Core Design>

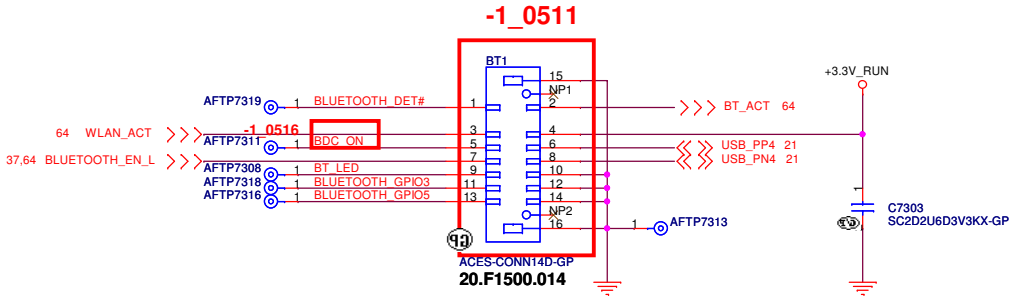
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

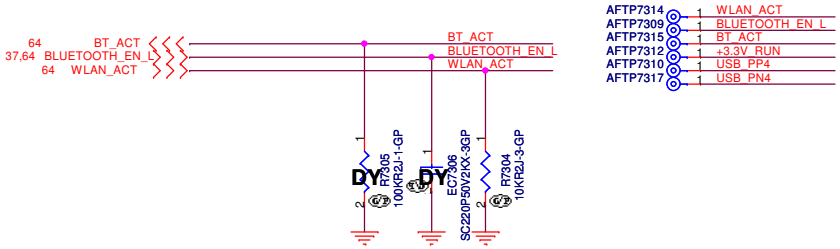
Title: CARD Reader Connector

Size	Document Number	Rev
A3	DJ2 Montevina UMA	X00

Date: Wednesday, June 02, 2010 Sheet 71 of 88

SSID = User.Interface





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Bluetooth*

Size	Document Number	Rev
A3	*DJ2 Montevina UMA*	*X00*

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SSID = Mechanical

H10 HOLE197R166-GP
H11 HOLE197R166-GP
H12 HOLE197R166-GP
H6 HT10X10BE10R32-R-5-GP
H7 HT10X10BE10R32-R-5-GP
H8 HOLET256B315R111-GP
H9 HOLE197R166-GP
34.4EM01.001

H1 HTE95BE95R29-R-5-GP
H2 HTE95BE95R29-R-5-GP
H4 HTE95BE95R29-R-5-GP
H5 HTE95BE95R29-R-5-GP
H3 HTE95BE95R29-R-5-GP

HMI1 STF256R117H119-GP
HTH1 STF237R117H83-1-GP
HBT1 STF237R115H123-GP

SPR1 SPRING-58-GP
SPR2 SPRING-58-GP
SPR3 SPRING-58-GP
SPR5 SPRING-57-GP
SPR6 SPRING-58-GP
SPR7 SPRING-58-GP

-1_0601_2
-1_0601_2

+PWR_SRC
+1.05V_VCCP
+0.75V_DDR_VTT
+1.5V_SUS
+5V_RUN
+3.3V_RUN
+3.3V_ALW
+5V_ALW
+VCC_CORE
+DC_IN

SCD1U10V2KX-5GP

-1_0528 for EMI

-1_0529 for EMI

-1_0601 for EMI

-1_0526 for EMI

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: DJ2 Montevina UMA
Rev: X00
Date: Tuesday, June 01, 2010
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