CHELSEA DJ2 UMA Schematics Document

AMD Danube CPU S1G4

RS880M + SB820M

2010-05-15

REV : A00

DY : Nopop Component
HDMI : Pop for HDMI function
GIGA : Pop for GIGA LAN
10/100 : Pop for 10/100 LAN

<Core Design>

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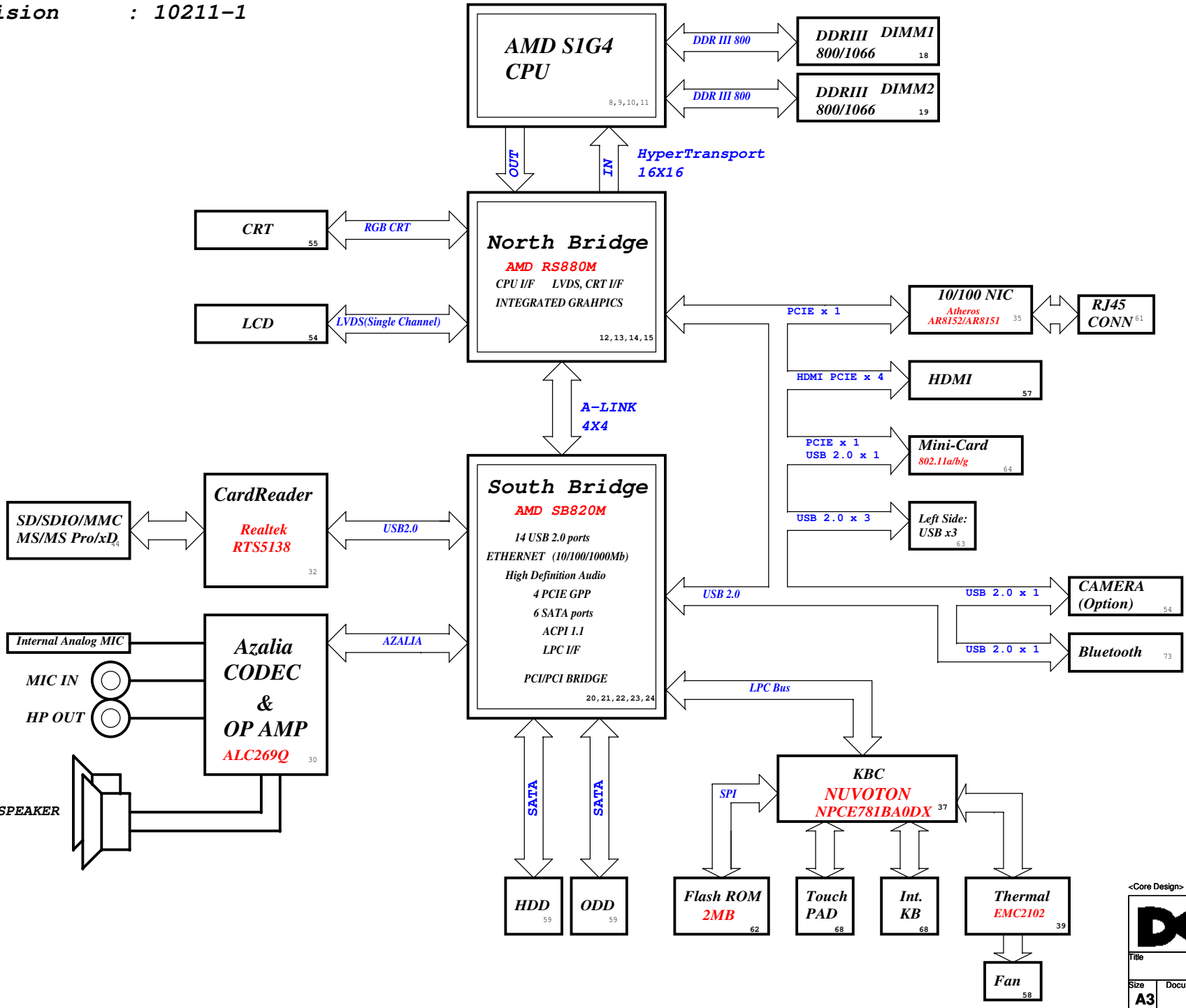
Title	Cover Page	
Size: Custom	Document Number: Chelsea DJ2 AMD UMA	Rev: A00
Date: Friday, May 14, 2010	Sheet 1 of 90	

Project code : 91.4EM01.001
PCB P/N : 48.4EM18.011
Revision : 10211-1

Chelsea DJ2 AMD UMA Block Diagram



CHARGER	
BQ24745RHDR	
INPUTS	OUTPUTS
+DC_IN_SS +CHAGER_SRC	+PWR_SRC

SYSTEM DC/DC		
RT8205BGQW-GP		46
INPUTS	OUTPUTS	
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW	

SYSTEM DC/DC		
RT8209EGQW		50
INPUTS	OUTPUTS	
+PWR_SRC	+1.1V_RUN	

CPU CORE		
ISL6265AHRTZ-T-GP		47
INPUTS	OUTPUTS	
+PWR_SRC	+VCC_CORE +VDDNB	

DDR III SUS&VTT		
TPS51116RGER		49
INPUTS	OUTPUTS	
+PWR_SRC	+1.5V_SUS	

SYSTEM DC/DC		
APL5930KAI		52
INPUTS	OUTPUTS	
+3.3V_ALW	+1.8V_RUN	

SYSTEM DC/DC		
Swithes/RT9013		42,53
INPUTS	OUTPUTS	
+3.3V_ALW	+3.3V_RUN	
+5V_ALW	+5V_RUN	
+1.5V_SUS	+1.5V_RUN	
+3.3V_RUN	+2.5V_RUN	

SYSTEM DC/DC		
TPS51125RGER		48,51
INPUTS	OUTPUTS	
+3.3V_ALW +1.5V_SUS	+1.1V_ALW +CPU_VDDR	

PCB LAYER
L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

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Title: Block Diagram

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	A00

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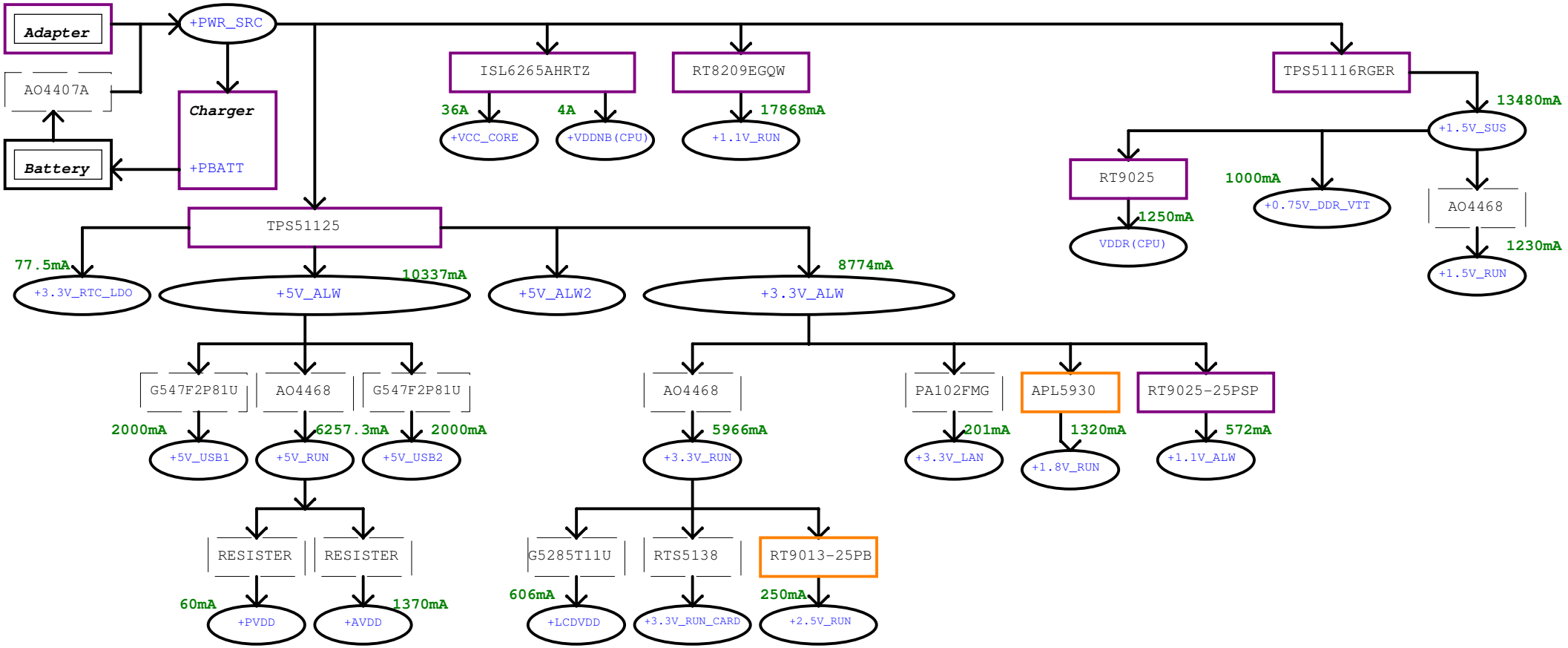
Power Block Diagram

Power Shape

Regulator | LDO | Switch



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Title	Power Block Diagram	
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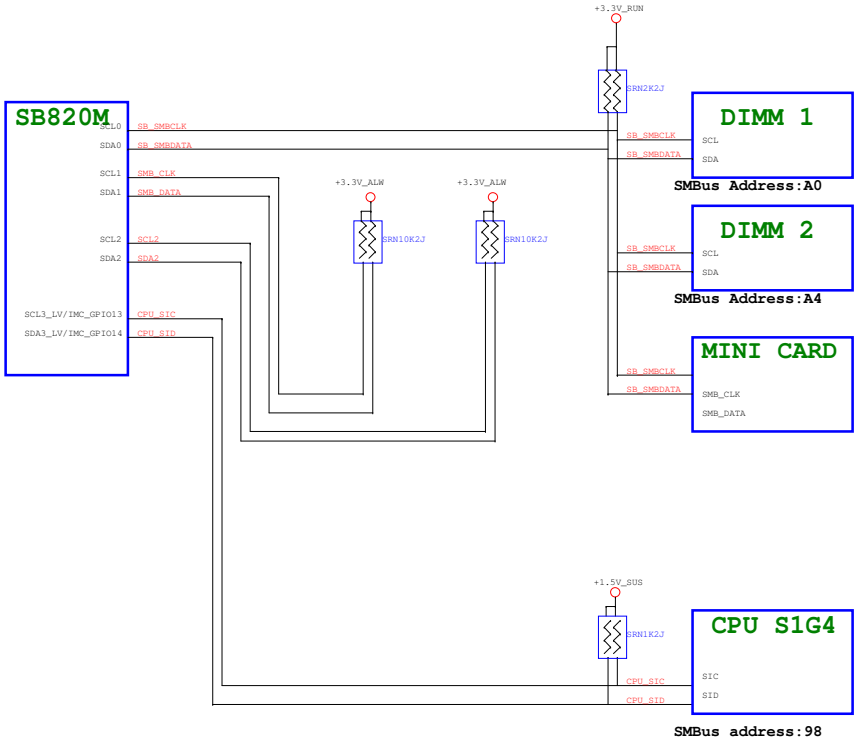
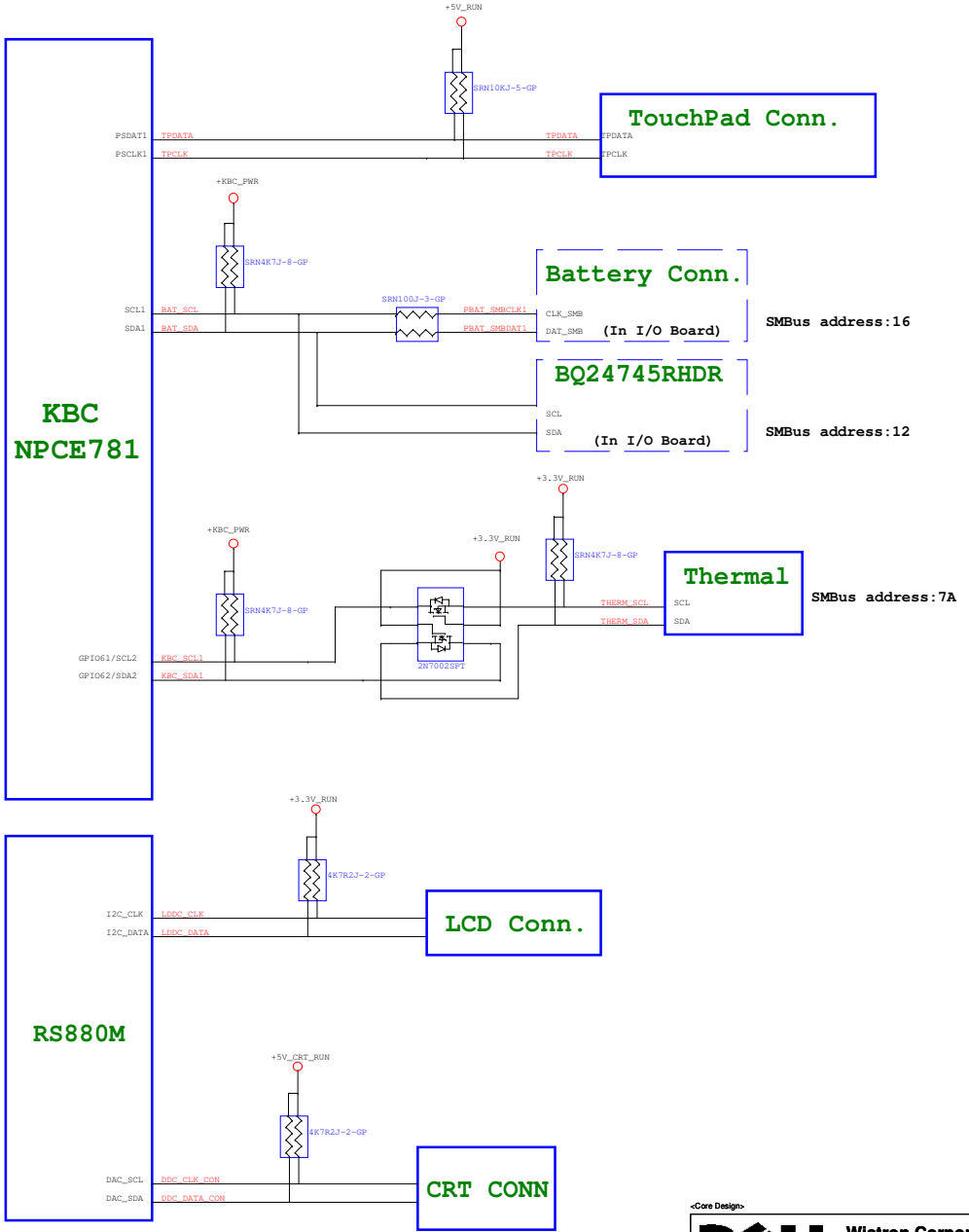
SB820M SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS BLOCK DIAGRAM

Size	Document Number	Rev
A2	Chelsea DJ2 AMD UMA	A00

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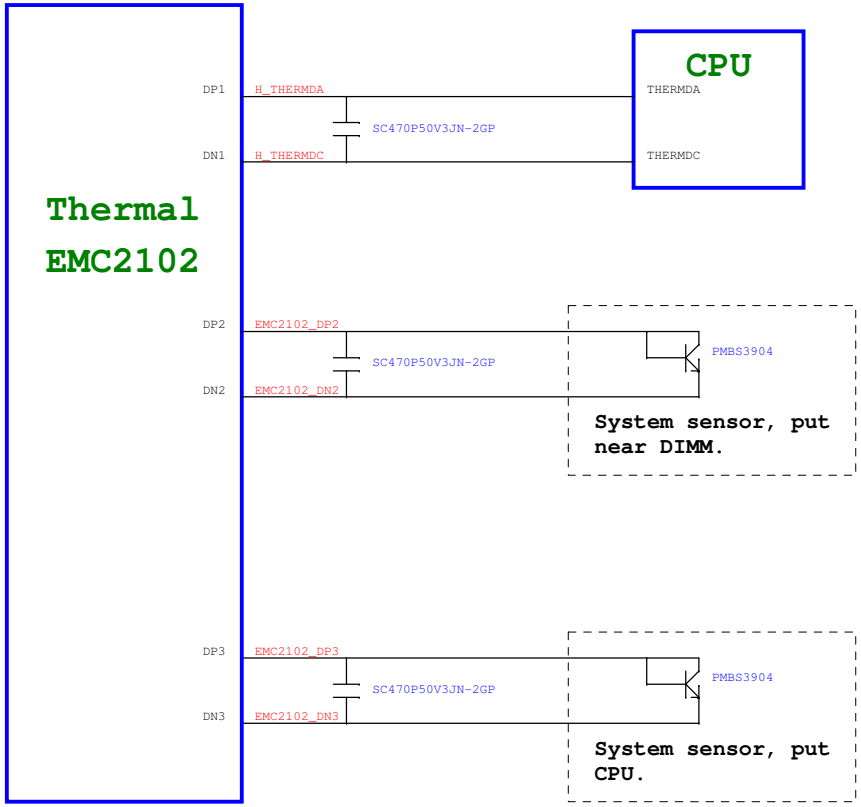
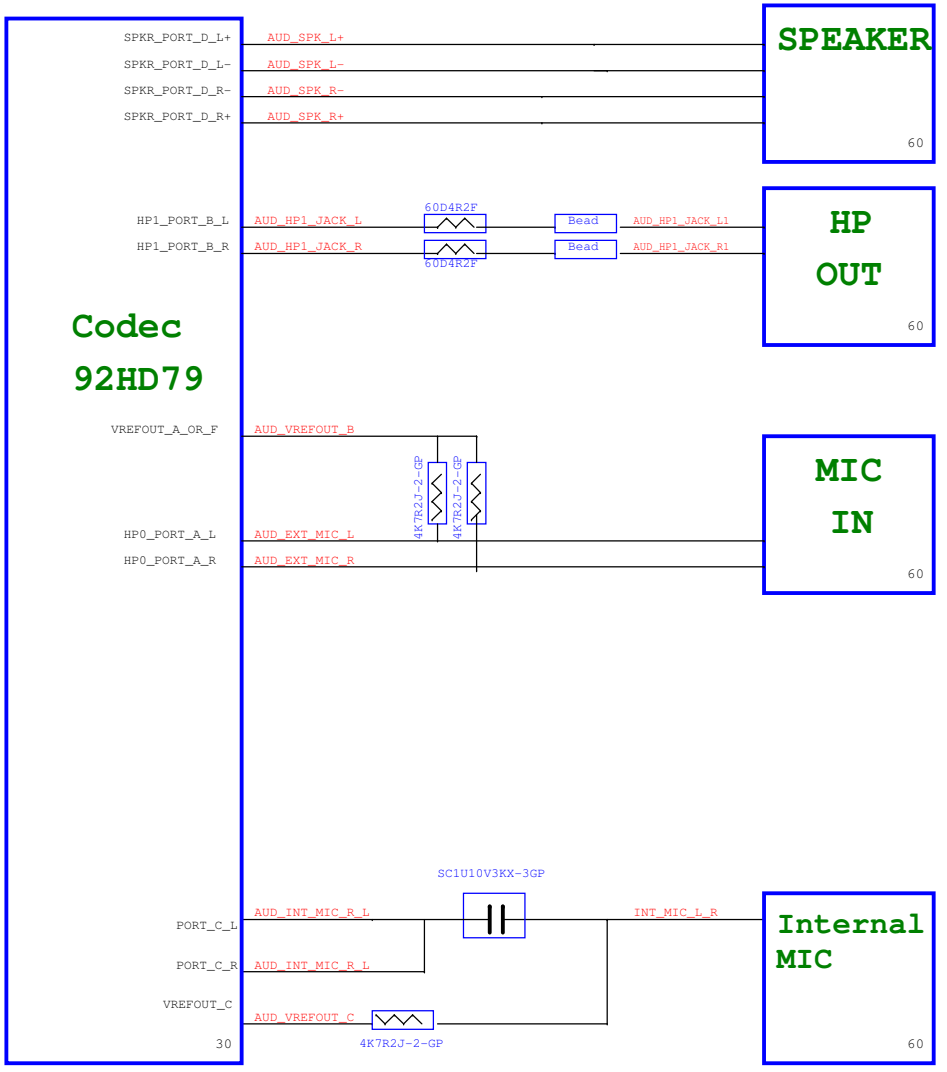
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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SB820M Strapping

Capture from 45484 Rev. 1.02 AMD SB8xx-Series Southbridge Design Guide

Name	Strap Name	Schematic Note
LPCCLK0	ECEnableStrap	Embedded Controller (EC) ★ 0 V - Disabled 3.3 V - Enabled
EC_PWM3 EC_PWM2	{ROMTYPE_1, ROMTYPE_0 }	ROMTYPE_1 / ROMTYPE_0 / ROM TYPE 3.3V / 0V / SPI ROM 3.3V / 3.3V / Reserved 0V / 0V / Firmware Hub ★ 0V / 3.3V / LPC ROM (supports both LPC and PMC ROM types)
LPCCLK1	CLKGEN	Defines clock generator 0V - External clock mode: Use 100-MHz PCIeR clock as reference clock and generate i nternal clocks only. ★ 3.3V- Integrated clock mode: Use 25-MHz crystal clock and generate both internal and external clocks
PCICLK1	BIF_GEN2_ COMPLIANCE_Strap	Set PCIe to Gen II mode 0V- Force PCIe interface at Gen I mode ★ 3.3V- PCIe interfacce is at Gen II mode Not Applicable to SB820M but provision for pull-down is required.
PCICLK2	BootFailTmrEn	Watchdog function ★ 0V- Disable the boot fail timer function 3.3V- Enable the boot fail timer function
PCICLK3	DefaultStrapMode	Default Debug Straps ★ 0V- Disable Debug Straps. 3.3V- Select external Debug Straps
PCICLK4	CPUClkSel	CPU/NB HT Clock Selection 0V- Reserved. ★ 3.3V- Required setting for integrated clock mode. This strap is not used if the strap CLKGEN is configured for external clock generator mode.
AZ_SDOUT	CoreSpeedMode	Slow down core clock for low power platform. ★ 0V- Performance mode 3.3V- Low Power mode

NB880M Strapping

Capture from 46113_rs880m_ds_nda_1.03

Name	Strap Function	Schematic Note
DAC_VSYNC	STRAP_DEBUG_BUS_GPIO _ENABLE#	Enables debug bus access through memory I/O pads and GPIOs. 0: Enable ★ 1: Disable
DAC_HSYNC	SIDE_PORT_EN#	Indicates if memory side-port is available or not 0: Available ★ 1: Not available
SUS_STAT#	LOAD_EEPROM_STRAPS#	Selects loading of strap values from EEPROM. 0: I2C master can load strap values from EEPROM if connected, or use default values if EEPROM is not connected. Please refer to RS880M's reference schematics for system level implementation details. ★ 1: Use default values

USB Table

USB	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB1 (I/O Board, 17")
4	WLAN
5	Reserve
6	Reserve
7	Reserve
8	Reserve
9	Reserve
10	CARD READER
11	CAMERA
12	BLUETOOTH
13	Reserve

PCIE Routing

LANE0	MiniCard WLAN
LANE1	LAN

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Title: Table of Content

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Title: Clock Generator ICS9LPRS480

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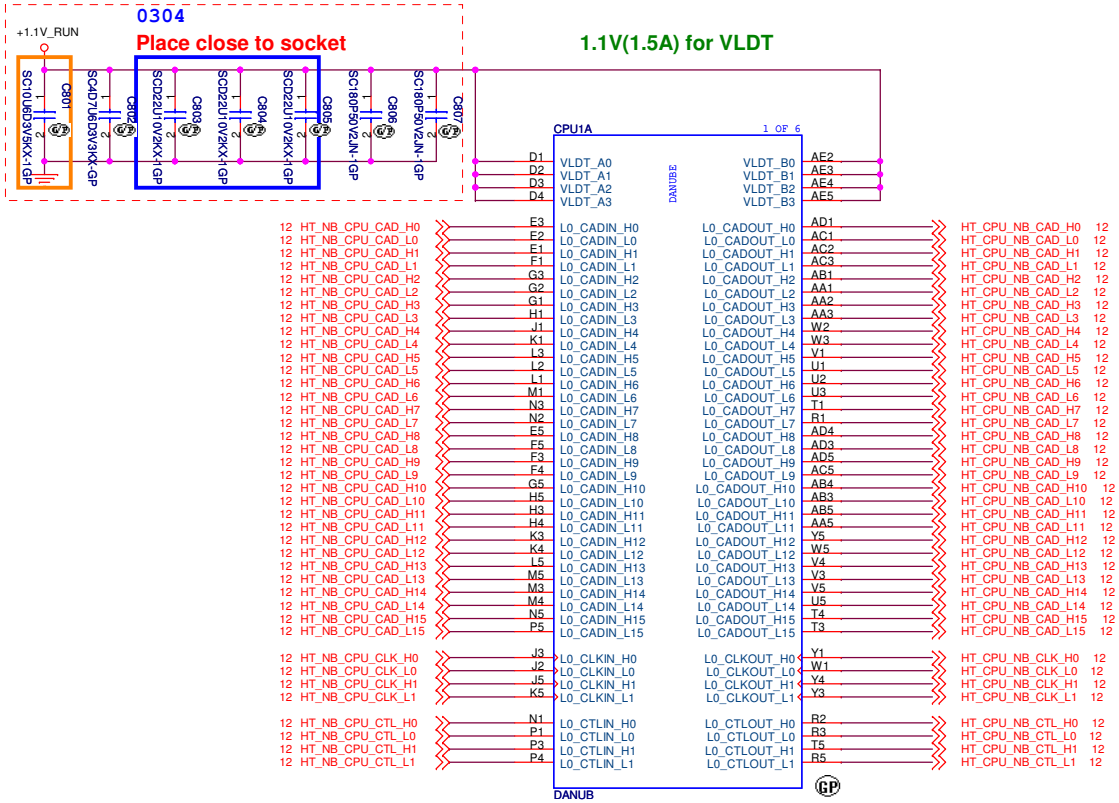
SSID = CPU



SKT-BGA638H176
1'nd 62.10055.111
2'nd 62.10055.181

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Title: CPU_HT_LINK I/F_(1/4)

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Date: Friday, May 14, 2010 | Sheet 8 of 90

SSID = CPU

4.7UF*4
0.22UF*4
1000PF*4
180PF*4

Place near to CPU

+CPU_VDDR

0.9V(1.25A) for VDDR
0.9V--DDR1066
1.05V---DDR1333 (1.75A)

CLOSE TO CPU

CPU1B 2 OF 6 DANUBE

CPU1C 3 OF 6 DANUBE

DANUB <Core Design>

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Title: CPU_DDR(2/4)
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SSID = CPU

LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

2.5V(250mA) for VDDA

CPU_CLK(200MHz)

For HDT DBG

Close CPU

Cloce To CPU

S1G4 not support MEMHOT

to power IC FB

For old HDT tool (3.3V level)

LAYOUT: Route FBCLKOUT_H/L
differentially impedance 80

HDT Connectors

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Title: CPU_Control&Debug_(3/4)

Size: Custom | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

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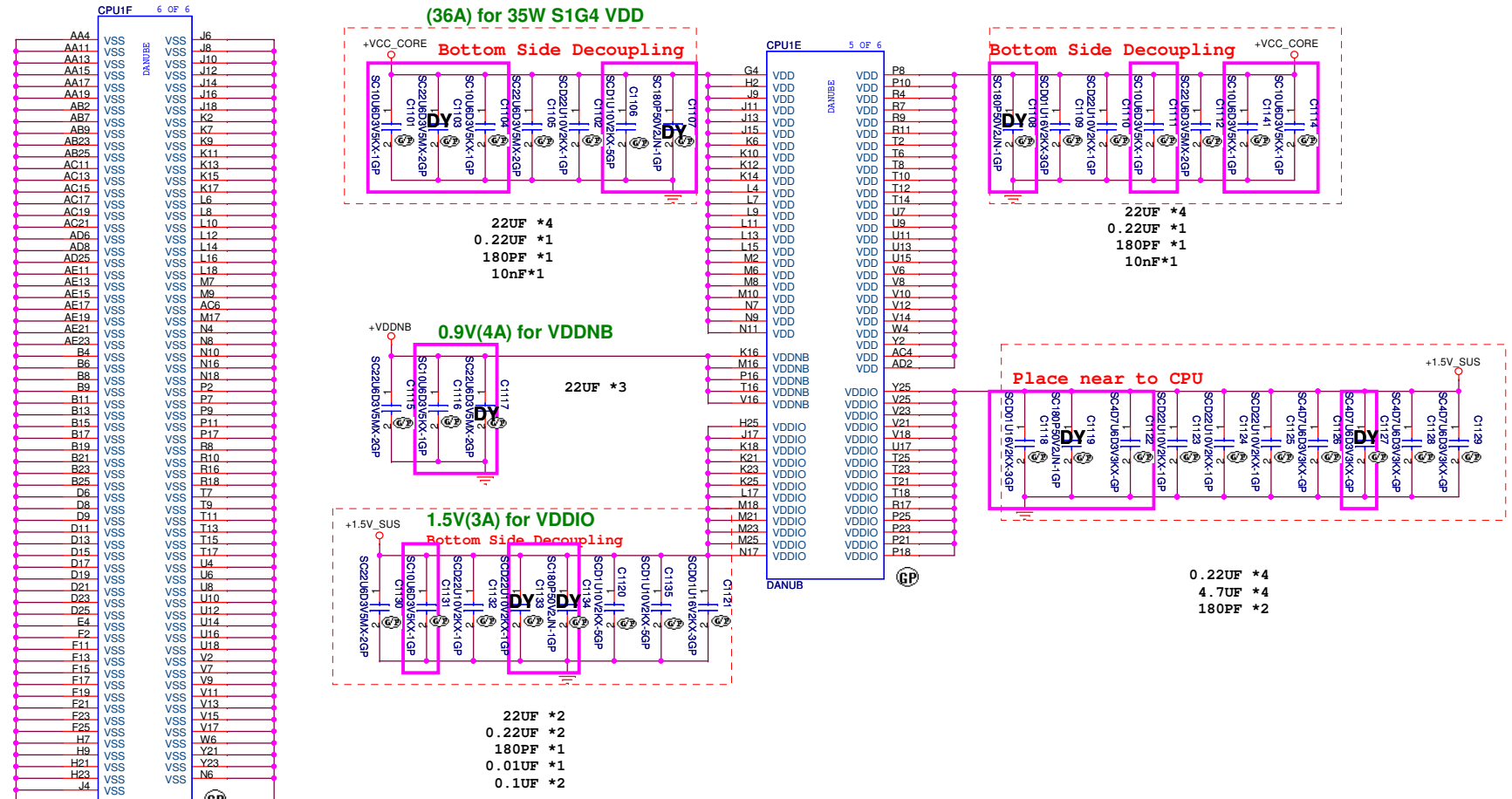
SSID = CPU



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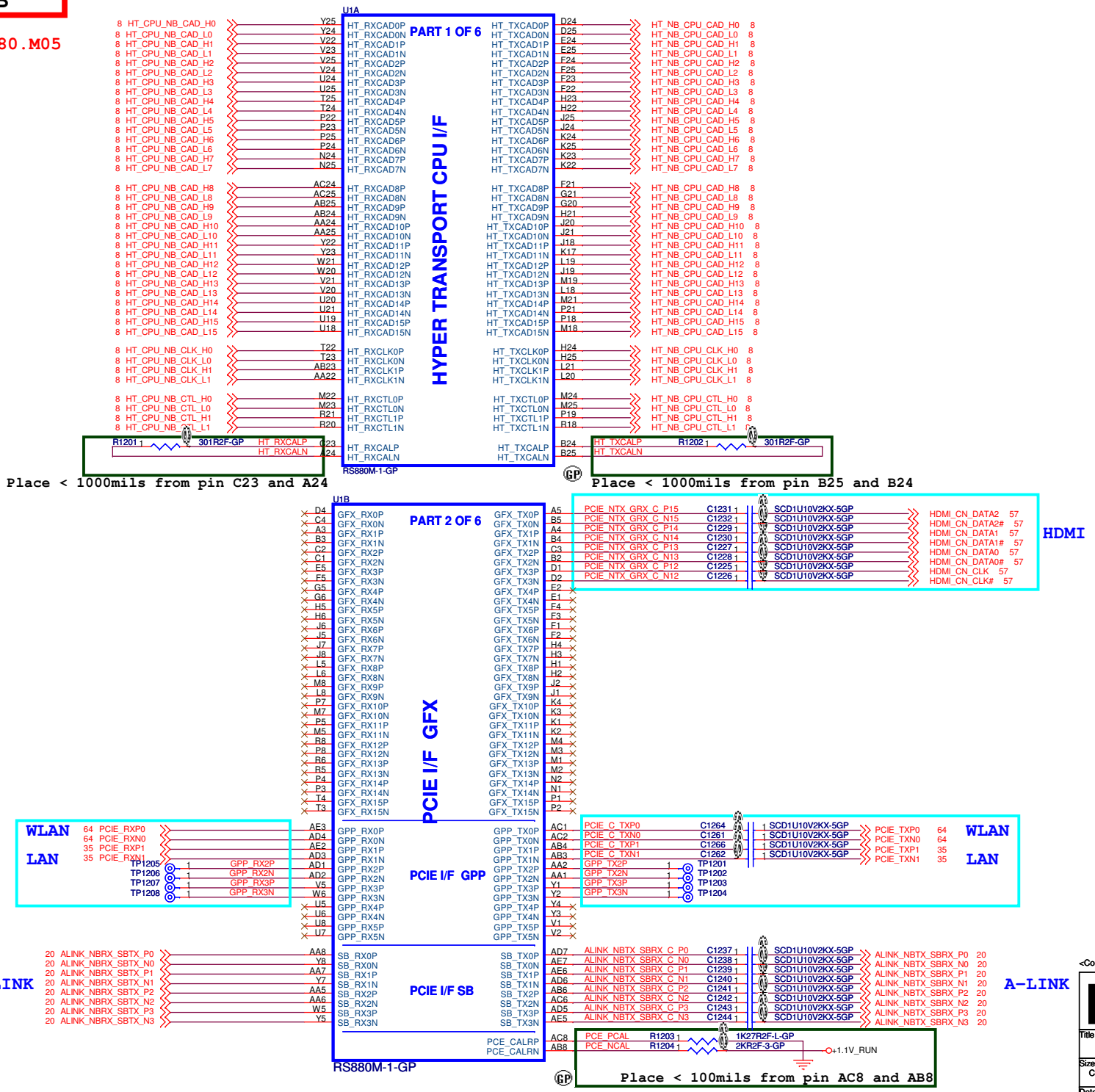
Title: CPU_Power_(4/4)		
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: A00
Date: Friday, May 14, 2010	Sheet 11 of 90	

SSID = N.B

RS880M : 71.RS880.M05



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Title: AMD-RS880M_HT LINK&PCIe(1/4)

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SSID = N.B

RS880M : 71.RS880.M05

STRAP_DEBUG_BUS_GPIO_ENABLE# (RS880M use VGA_VSYNC)
Enables debug bus access through memory I/O pads and GPIOs.
*1 : Disable
0 : Enable

SIDE_PORT_EN# (RS880M use VGA_HSYNC)
*1 = Memory Side port Not available
0 = Memory Side port available

LOAD_EEPROM_STRAPS#(RS880M use SUS_STAT#)
Selects Loading of STRAPS From EEPROM
*1 : use Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

*DEFAULT

+1.1V_RUN — L1308 BLM15AG221SS1D-GP 220 ohm 300mA — 65mA — PLLVDD — C1312 SC2D2U6D3V3KX-GP

+1.8V_RUN — R1323 0R0402-PAD — PLLVDD18 — C1311 SC1U10V3KX-3GP

+3.3V_RUN — R1342 0R0603-PAD-1-GP — +3.3V_RUN_AVDD — 110mA — C1307 SC1U10V3KX-3GP

+1.8V_RUN — 20mA — C1306 SCD1U10V2KX-5GP

+1.8V_RUN — 4mA — C1308 SCD1U10V2KX-5GP

Layout Note
Trace at least 15 mil

+1.8V_RUN — R1324 0R0402-PAD — 2+1.8V_VDDA18HTPLL — 20mA — C1302 SC2D2U6D3V3KX-GP DY — C1303 SCD1U10V2KX-5GP

R1325 0R0402-PAD — 2+1.8V_VDDA18PCIEPLL — 120mA — C1304 SC2D2U6D3V3KX-GP DY — C1305 SCD1U10V2KX-5GP

C1301 SC22U6D3V5MX-2GP DY

+3.3V_RUN — R1302 3KR2J-2-GP — R1303 3KR2J-2-GP — VGA_VSYNC — VGA_HSYNC — R1304 3KR2J-2-GP DY — R1305 3KR2J-2-GP DY

UMA: DAC_CLK and DATA with
5V-tolerant.not need level shift

Trace at least 10 mil

X00

55 M_RED — R1326 150R2F-1-GP
55 M_GREEN — R1327 150R2F-1-GP
55 M_BLUE — R1328 150R2F-1-GP

55 VGA_HSYNC — VGA_HSYNC
55 VGA_VSYNC — VGA_VSYNC
55 DDC_CLK_CON — DDC_CLK_CON
55 DDC_DATA_CON — DDC_DATA_CON
R1306 715R2F-GP — DAC_RSET

+1.8V_VDDA18HTPLL
+1.8V_VDDA18PCIEPLL
20 PLTRST#_NB_GPU
41 NB_PWRGD_IN
NB_LDT_STOP#
NB_ALLOW_LDTSTOP
20 CLK_NBHT_CLK
20 CLK_NBHT_CLK#
20 NB_REFCLK_P
20 NB_REFCLK_N
NB_GFX_CLK
NB_GFX_CLK#
TP1307 TP1308 NB_GPP_CLK NB_GPP_CLK#
20 NB_GPPSB_CLK
20 NB_GPPSB_CLK#
54 LDDC_CLK
54 LDDC_DATA
57 DDC_DATA_HDMI
57 DDC_CLK_HDMI
TP1303 TP1304 TP_NB_DDC_CLK1 TP_NB_DDC_DATA1
TP1305 TP_STRP_DATA TP_NB_RESERVED
R1319 RS780_AUX_CAL 150R2F-1-GP
R1318 2KR2J-1-GP

X01

+3.3V_RUN — RN1302 SRN4K7J-8-GP

U1C — RS880M-1-GP — PART 3 OF 6

CRT/TVOUT: AVDD1 AVDD2 AVDDDI AVSSDI AVDDQ AVSSQ; C_Pr Y COMP_Pb; RED REDb GREEN GREENb BLUE BLUEb; DAC_HSYNC DAC_VSYNC DAC_SCL DAC_SDA; DAC_RSET

PLL PWR: PLLVDD PLLVDD18 PLLVSS; VDDA18HTPLL; VDDA18PCIEPLL1 VDDA18PCIEPLL2

LVTM: TXOUT_L0P TXOUT_L0N TXOUT_L1P TXOUT_L1N TXOUT_L2P TXOUT_L2N TXOUT_L3P TXOUT_L3N; TXOUT_U0P TXOUT_U0N TXOUT_U1P TXOUT_U1N TXOUT_U2P TXOUT_U2N TXOUT_U3P TXOUT_U3N; TXCLK_LP TXCLK_LN TXCLK_UP TXCLK_UN; VDDLTP18 VSSLTP18; VDDLT18_1 VDDLT18_2 VDDLT33_1 VDDLT33_2; VSSLT1 VSSLT2 VSSLT3 VSSLT4 VSSLT5 VSSLT6 VSSLT7

CLOCKs PM: SYSRESET# POWERGOOD LDTSTOP# ALLOW_LDTSTOP; HT_REFCLKP HT_REFCLKN; REFCLK_P/OSCIN REFCLK_N; GFX_REFCLKP GFX_REFCLKN; GPP_REFCLKP GPP_REFCLKN; GPPSB_REFCLKP GPPSB_REFCLKN

MIS.: I2C_CLK I2C_DATA; DDC_DATA0/AUX0N DDC_CLK0/AUX0P DDC_CLK1/AUX1P DDC_DATA1/AUX1N; STRP_DATA; RESERVED; AUX_CAL

TV_OUT

VGA_TXAOUT0+ 54 — VGA_TXAOUT0- 54 — VGA_TXAOUT1+ 54 — VGA_TXAOUT1- 54 — VGA_TXAOUT2+ 54 — VGA_TXAOUT2- 54

VGA_TXACLK+ 54 — VGA_TXACLK- 54

+1.8V_RUN — 220 ohm 300mA — L1305 BLM15AG221SS1D-GP — +1.8V_RUN — 15mA — 300mA — R1329 0R0603-PAD-1-GP — -A00

VDDLTP18_R — VDDLT18_R — C1310 SCD1U10V2KX-5GP — C1313 SC4D7U6D3V3KX-3GP DY — C1309 SC1U10V3KX-3GP

LVDS_DIGON — LCDVDD_EN_R — R1332 0R0402-PAD — LCDVDD_EN 54
LVDS_BLON — BLON_R — R1331 0R0402-PAD — LBKLT_CTL 54
LVDS_ENA_BL — LVDS_BLEN — R1308 0R0402-PAD — PANEL_BKEN 37

RN1301 SRN4K7J-8-GP — X00

TMDS_HPD — TP1311 — HDMI_HPD_DET 57
SUS_STAT# — NB_SUS_STAT# — R1317 0R0402-PAD — SUS_STAT# 21
THERMALDIODE_P THERMALDIODE_N
TESTMODE — TESTMODE_NB — R1320 1K8R2F-GP

+1.5V_RUN — R1309 300R2J-4-GP — R1322 DY 0R2J-2-GP — +1.8V_RUN — R1311 2K2R2J-2-GP

U1301 SN74LVC2G07DCKR-GP — 10,20 CPU_LDT_STOP# — NB_LDT_STOP# — C1314 SCD1U10V2KX-5GP

+1.8V_RUN — R1315 1KR2J-1-GP — 20 ALLOW_LDTSTOP — R1316 0R0402-PAD — NB_ALLOW_LDTSTOP

ALLOW_LDTSTOP:
1 = LDTSTOP# can be asserted
0 = LDTSTOP# has to be de-asserted

X01

NB_GFX_CLK — NB_GFX_CLK# — RN1303 SRN4K7J-8-GP

+3.3V_RUN — R1314 4K7R2J-2-GP — NB_SUS_STAT# — R1321 3KR2J-2-GP DY

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Title: AMD-RS880M_LVDS&CRT_(2/4)
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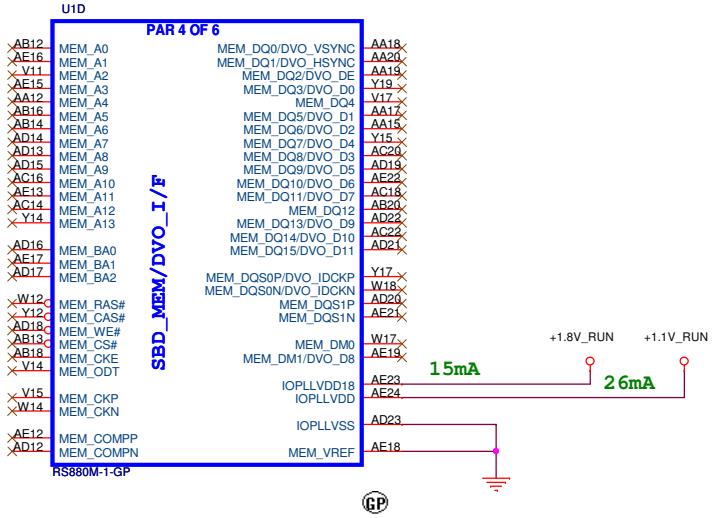
SSID = N.B



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Title: AMD-RS880M_SidePort_(3/4)

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	A00

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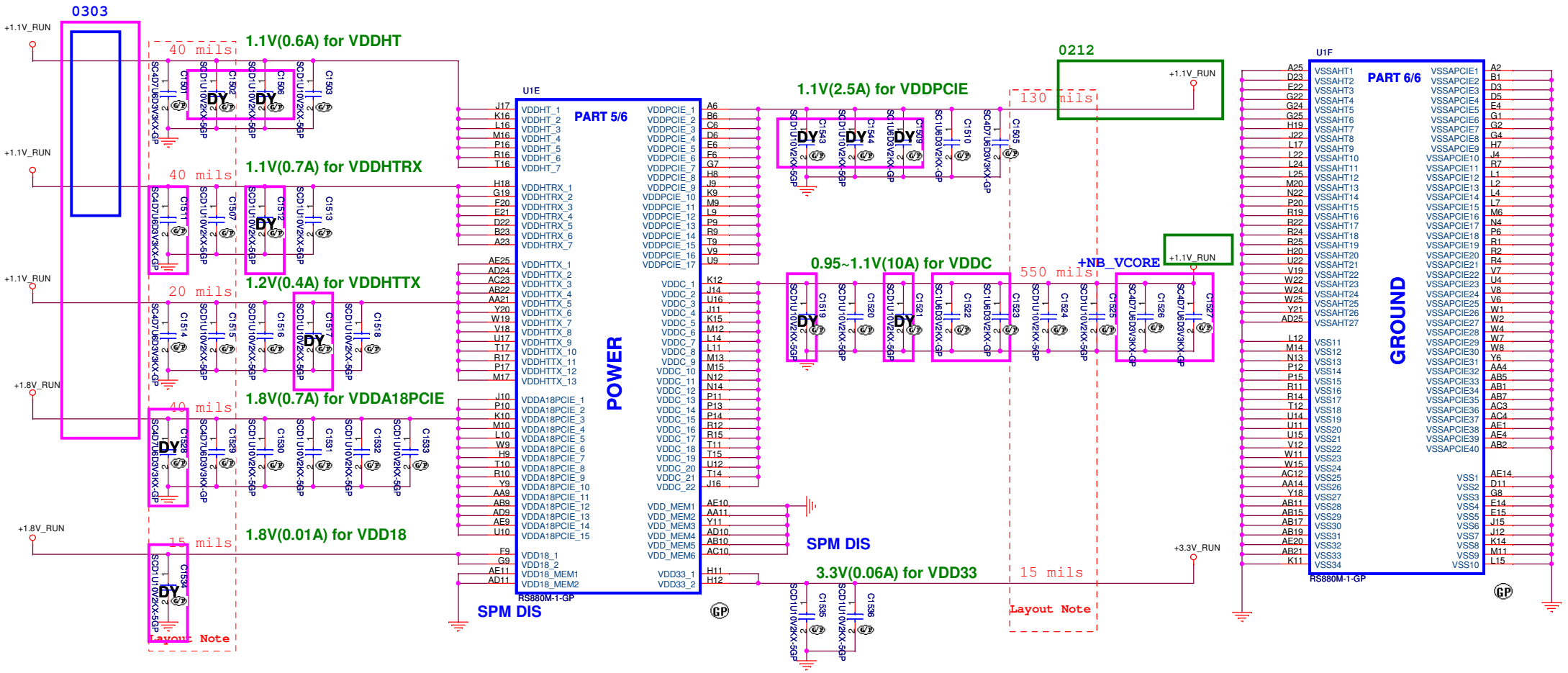
SSID = N.B



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Title	AMD-RS880M_PWR&GD_(4/4)	
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Title

Reserved

Size	Document Number	Rev
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Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *A00*

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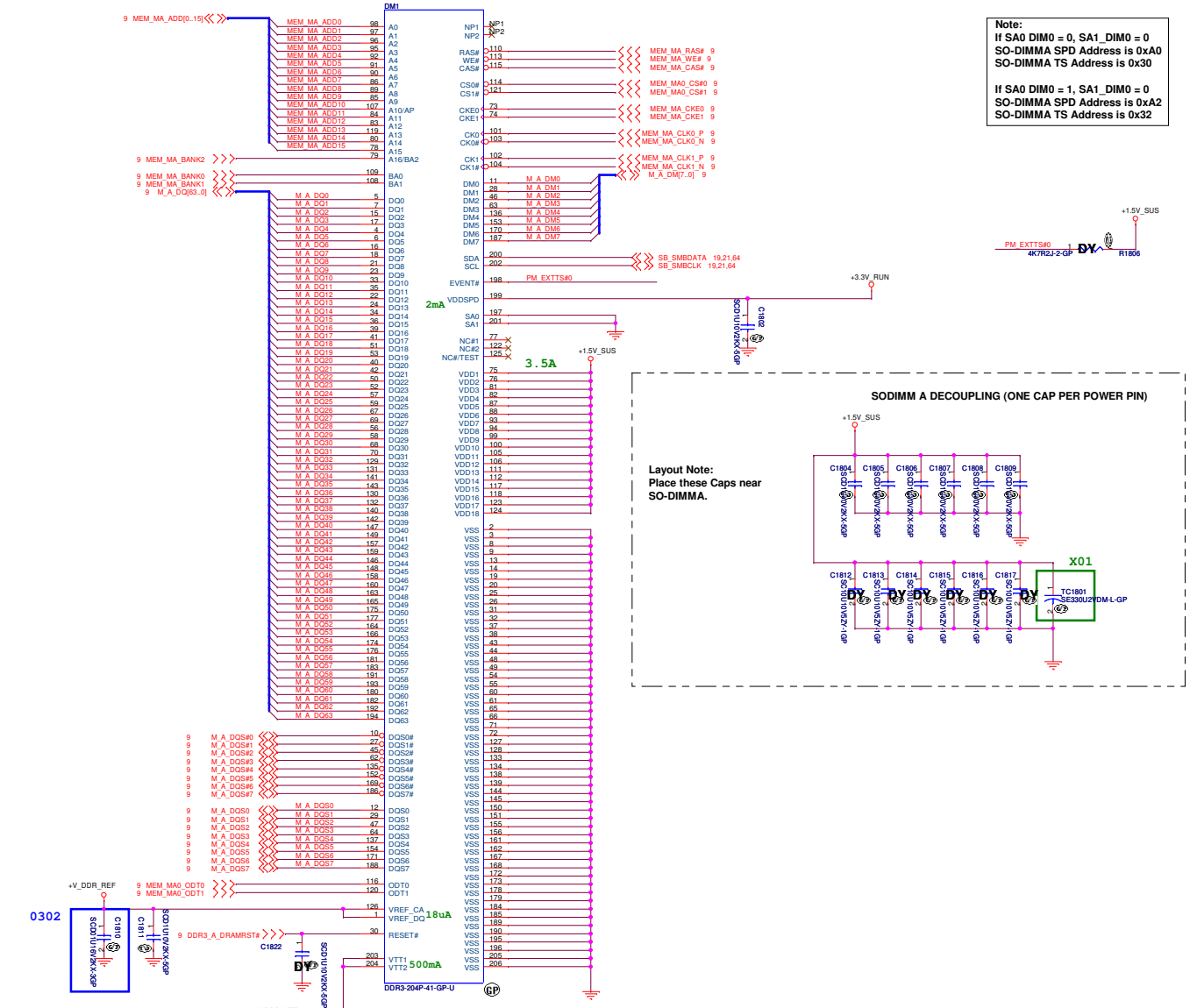

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Title: **DDR3-SODIMM1**

Size	Document Number	Rev
	Chelsea DJ2 AMD UMA	A00

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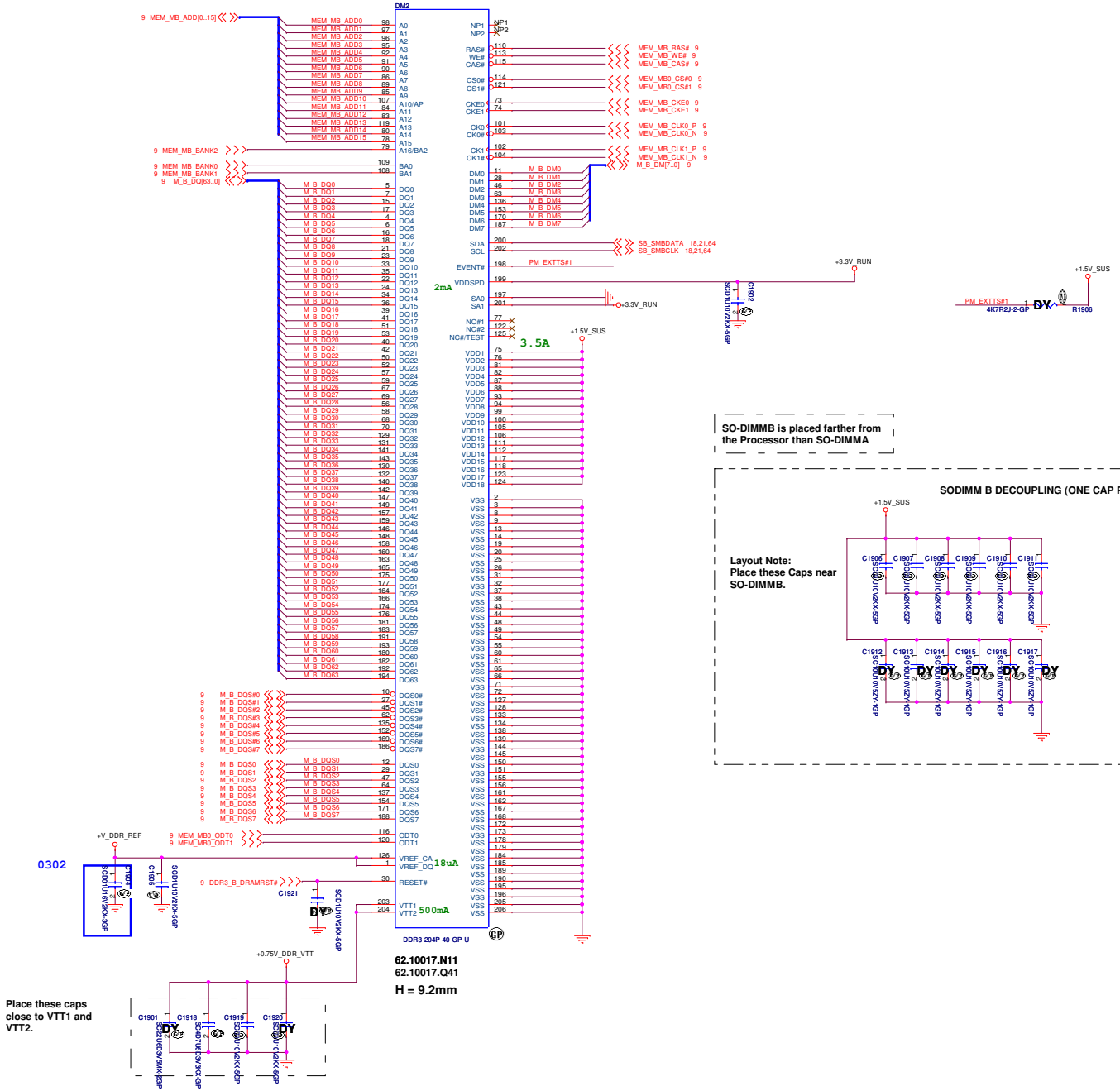

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Title: DDR3-SODIMM2

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SSID = S.B

SB700 A12 : 71.SB8[illegible].M02

placed CAP closed SB820M

Part 1 of 5

U2A

SB820M-1-GP

PCI EXPRESS INTERFACES

PCI INTERFACE

CLOCK GENERATOR

LPC

CPU

RTC

PCI CLKS

STRAP PIN

Place R <100mils form pins AD29,AD28

NOTE: SB8XX ONLY SUPPORTS 2 GPP PORT 2 AND 3 IS NOT SUPPORTED. (From CRB)

1nd 82.30020.851
2nd 82.30020.791

1'nd 73.01G08.DHG
2'nd 73.01G08.L04

LPC Bus Routing first connects to MINICARD then connects to KBC

82.30001.661

Main Source

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Title: SB820M_PCIE&PCI_(1/5)

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

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SSID = S.B

USB	
Pair	Device
0	USB2
1	USB3
2	USB0 (I/O Board)
3	USB1 (I/O Board, 17")
4	WLAN
5	RESERVED
6	RESERVED
7	RESERVED
8	RESERVED
9	RESERVED
10	CARD READER
11	CAMERA
12	BLUETOOTH
13	RESERVED

U2D

Part 4 of 5

SB820M-1-GP

ACPI / WAKE UP EVENTS

USB MISC

USB 2.0

GPIO

USB OC

HD AUDIO

GBE LAN

EMBEDDED CTRL

EMBEDDED CTRL

0225

0225

X01

X00

-A00

-A00

not use

SBD DDR RESET

Close SB

Not use

Strap Pin / define to use LPC or SPI ROM

EC Not Implemented

EC Not Implemented

GbE Controller Not Enabled

HDMI_SEL

0	HDMI
1	non-HDMI

JTAG_TDI

JTAG_RST#

<Core Design>

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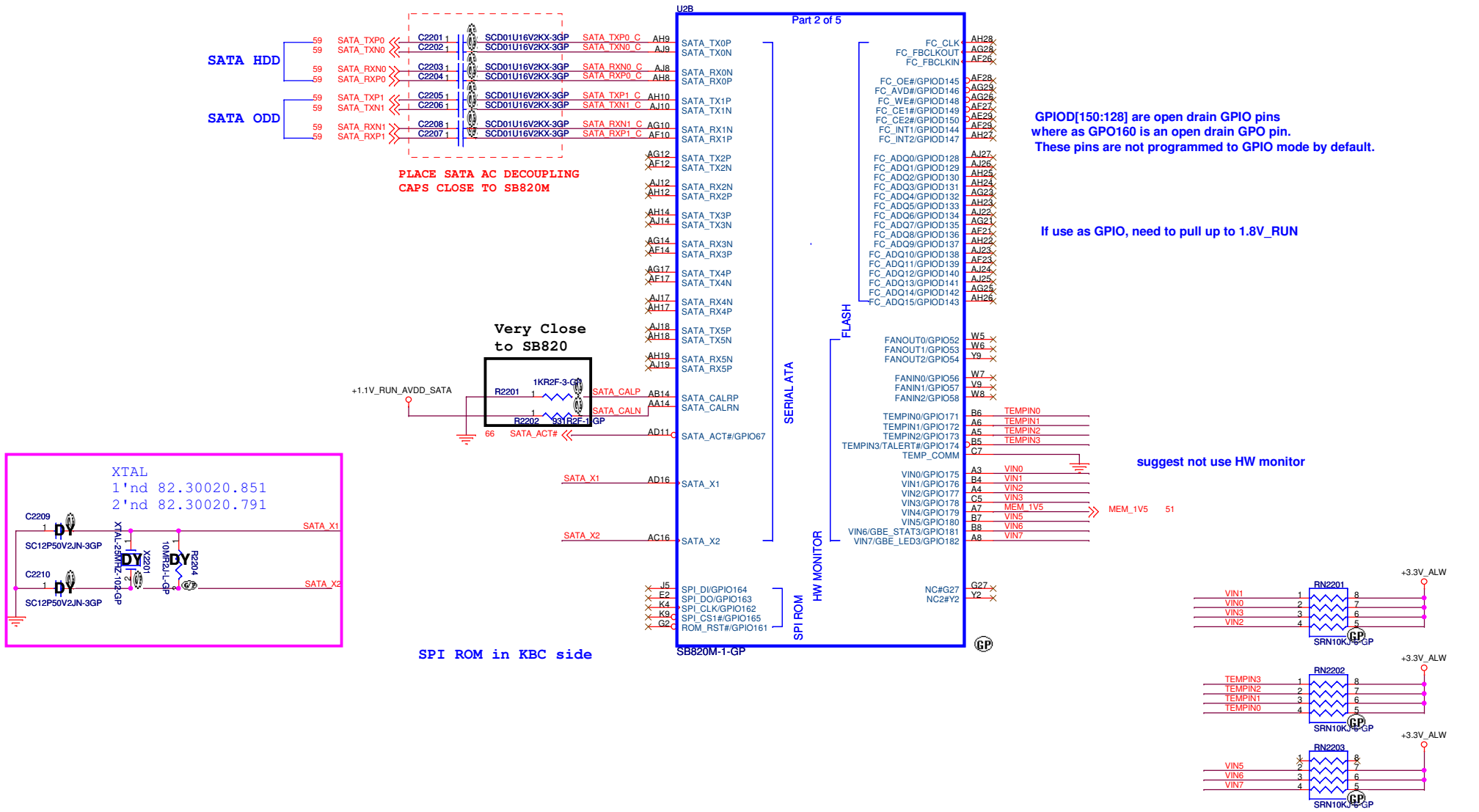
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_USB&GPIO_(2/5)

Size: Custom | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

Date: Friday, May 14, 2010 | Sheet 21 of 90

SSID = S.B

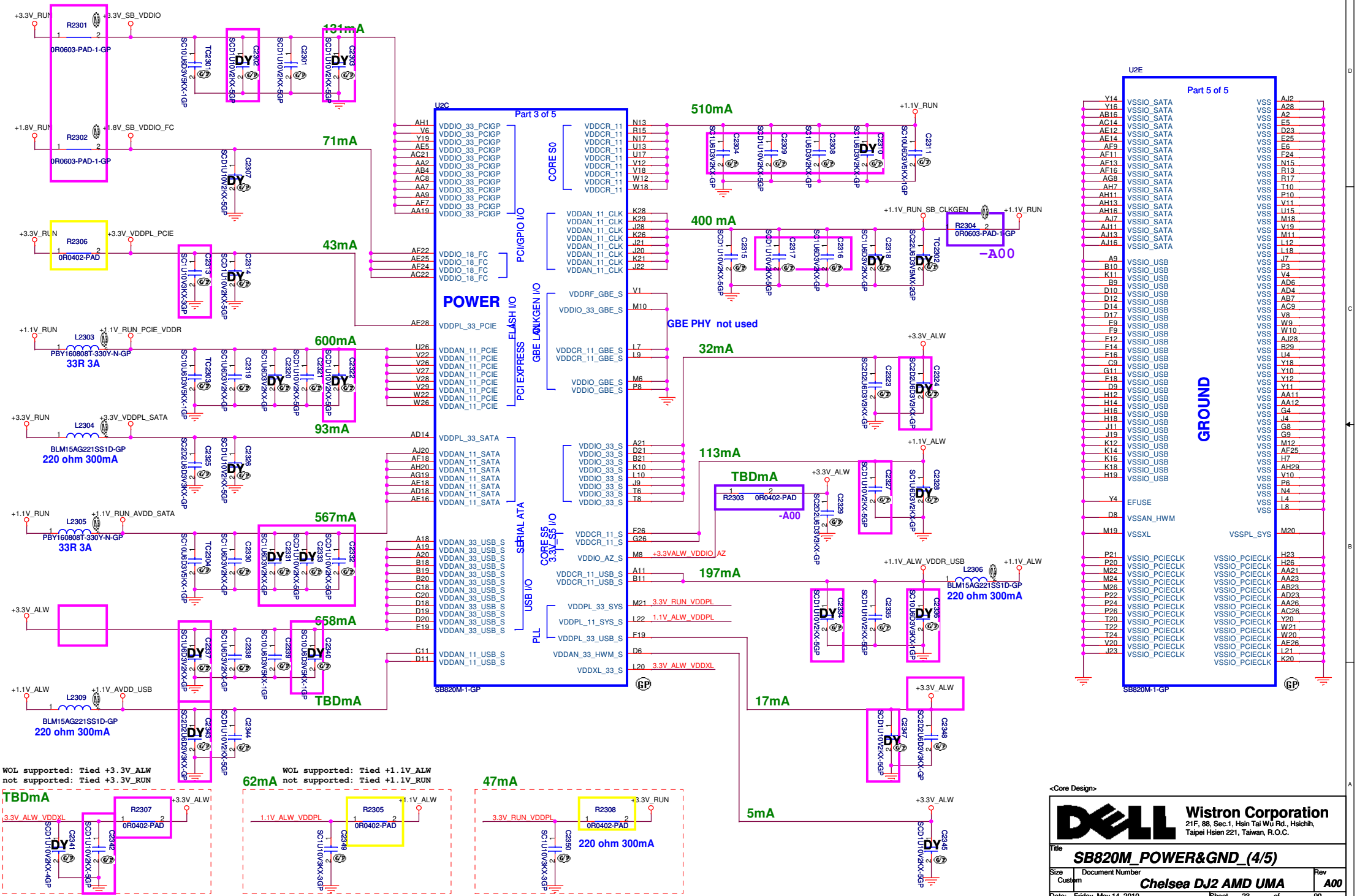


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	SB820M_SATA-IDE_(3/5)	
Size: Custom	Document Number: Chelsea DJ2 AMD UMA	Rev: A00
Date: Friday, May 14, 2010	Sheet 22 of 90	

SSID = S.B



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

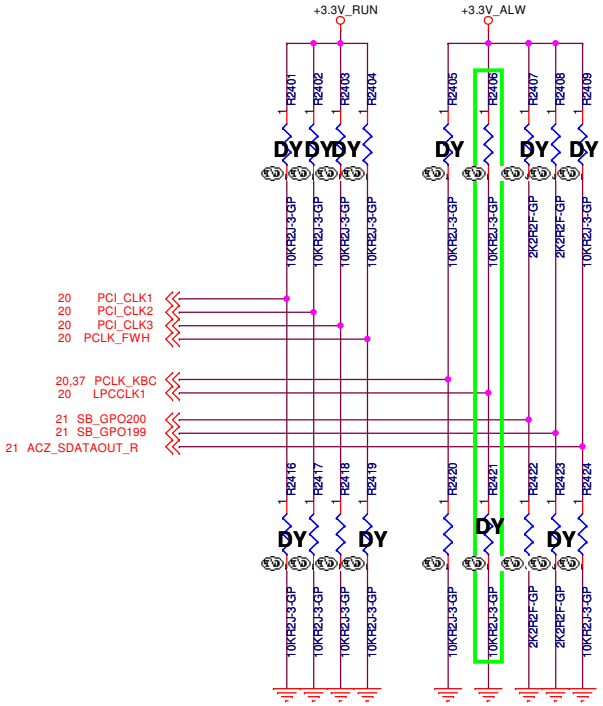
Title: SB820M_POWER&GND_(4/5)

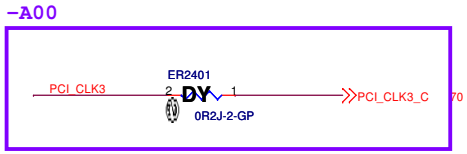
Size: Custom | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

Date: Friday, May 14, 2010 | Sheet 23 of 90

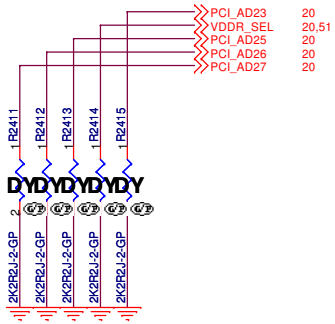
SSID = S.B

REQUIRED STRAPS





DEBUG STRAPS



REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCLK_FWH (PCI_CLK4)	PCLK_KBC (LPCCLK0)	LPCCLK1	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	DEFAULT CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	L, H = LPC ROM DEFAULT L, L = FWH ROM

Not Applicable to SB820M
but provision for pull-down is required.

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

<Core Design>

Wistron Corporation
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Title: SB820M_STRAPPING_(5/5)

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

Date: Friday, May 14, 2010 | Sheet 24 of 90

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<Core Design>

Wistron Corporation
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Title: CPU (VCC_CORE)

Size | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

Date: Friday, May 14, 2010 | Sheet 25 of 90

(Blanking)

<Core Design>

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Title

CPU (VCC_GFXCORE)

Size	Document Number	Rev
	Chelsea DJ2 AMD UMA	A00

Date: Friday, May 14, 2010 Sheet 26 of 90

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

Date: Friday, May 14, 2010 | Sheet 27 of 90

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<Core Design>

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Title

Reserved

Size	Document Number	Rev
A3	*Chelsea DJ2 AMD UMA*	*A00*

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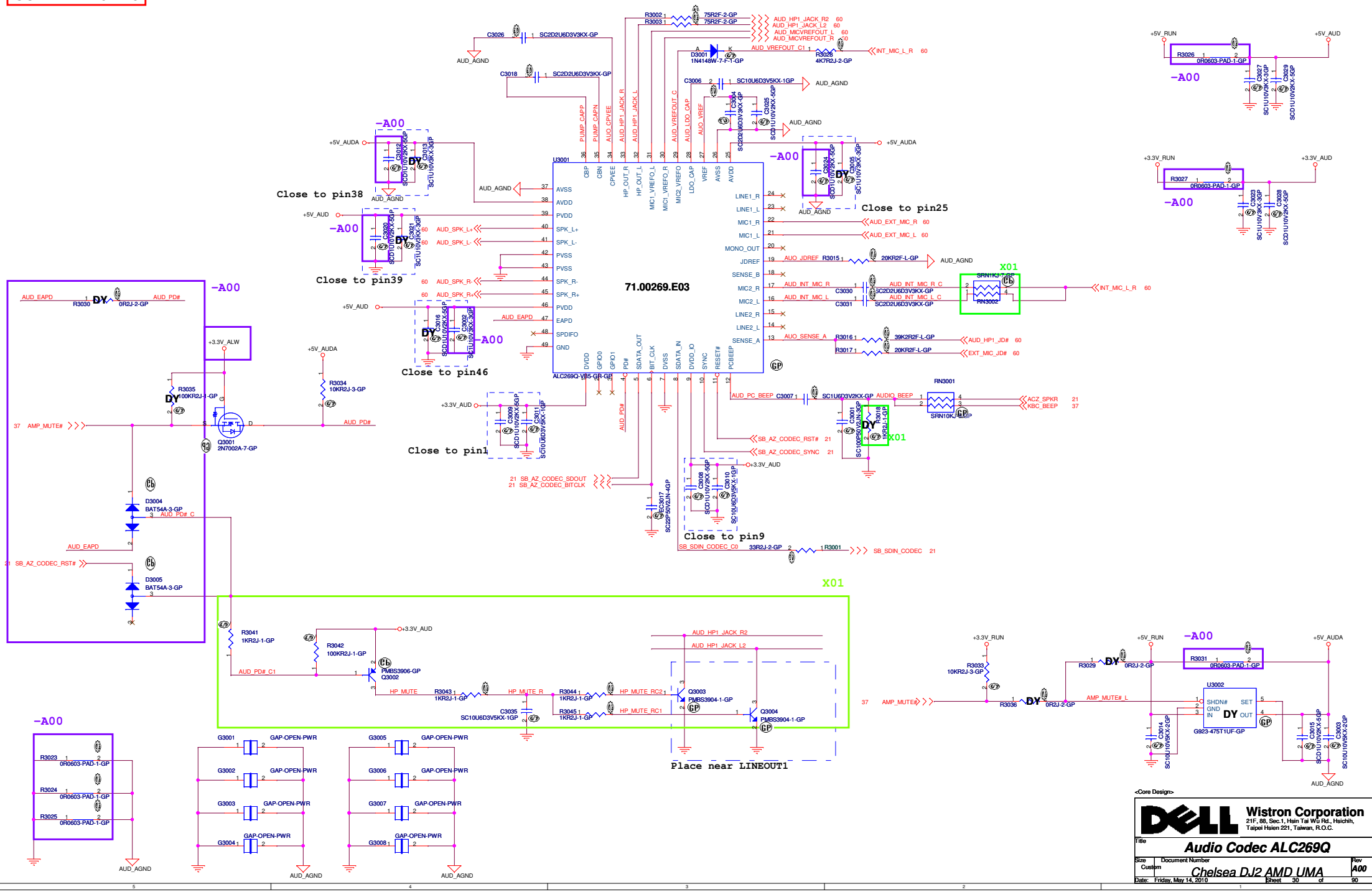
Title

Reserved

Size	Document Number	Rev
A3	*Chelsea DJ2 AMD UMA*	*A00*

SSID = AUDIO



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC269Q

Size: Custom | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

Date: Friday, May 14, 2010 | Sheet 30 of 90

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<Core Design>

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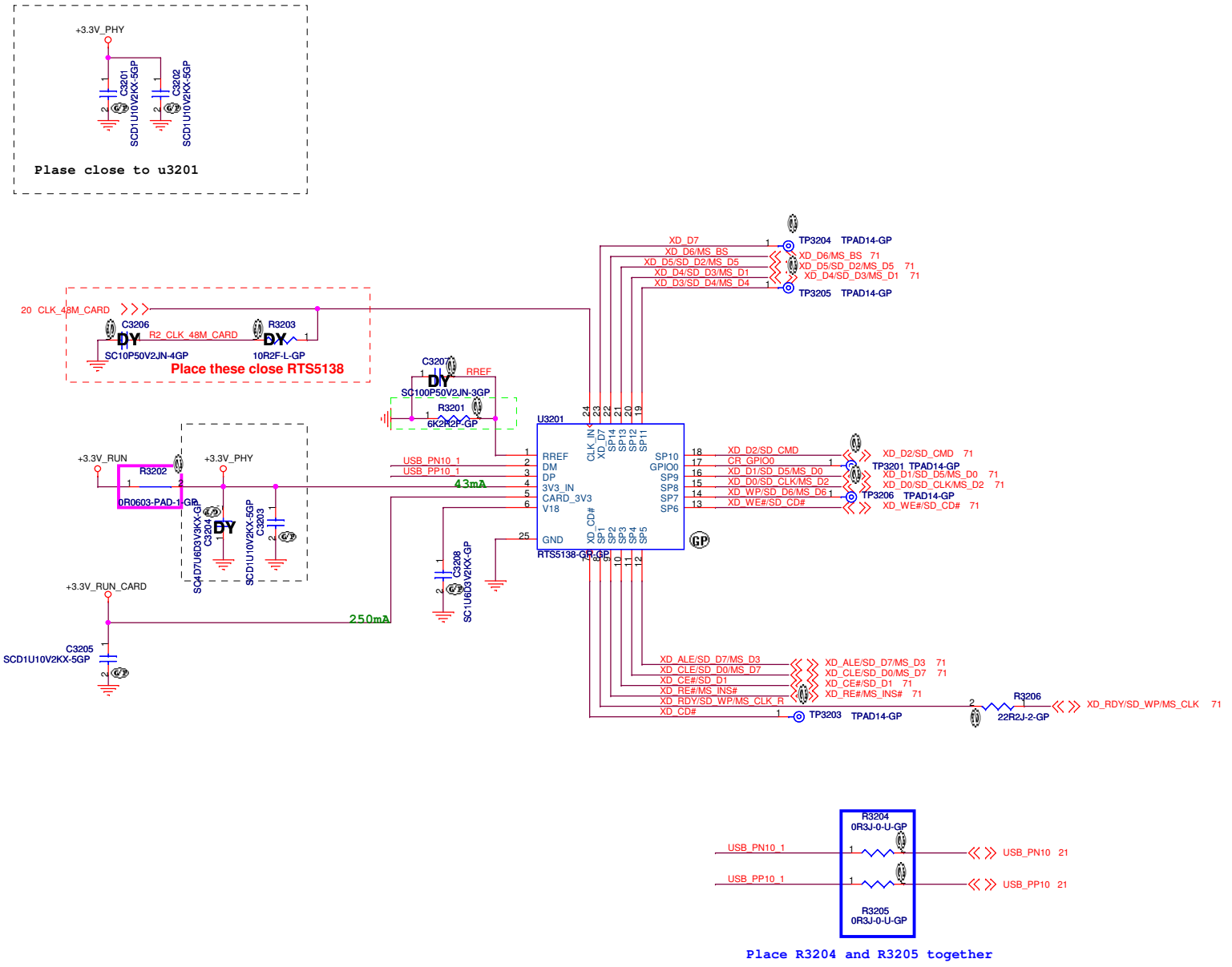
Title: *Reserved*

Size	Document Number	Rev
A3	*Chelsea DJ2 AMD UMA*	*A00*

Date: Friday, May 14, 2010 Sheet 31 of 90

SSID = SDIO



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138

Size: Custom | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

Date: Friday, May 14, 2010 | Sheet 32 of 90

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<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
A3	*Chelsea DJ2 AMD UMA*	*A00*

Date: Friday, May 14, 2010 Sheet 33 of 90

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Title: *Reserved*

Size	Document Number	Rev
A3	*Chelsea DJ2 AMD UMA*	*A00*

Date: Friday, May 14, 2010 Sheet 34 of 90

Close to pin40

0310

L3501

LAN_VDDCT — LAN_LX — IND-4D7UH-192-GP

C3546 SC10U6D3V5KX-1GP (DY)
C3537 SCD1U10V2KX-5GP (DY)
C3504 SC1KP50V2KX-1GP

LAN_CLKREQ# — R3505 0R2J-2-GP — GIGA

61 LAN_VDDCT — LAN_VDDCT — R3504 0R3J-0-U-GP (DY) — LAN_VDDCT_REG

C3517 SCD1U10V2KX-5GP
C3545 SC1U6D3V2KX-GP (DY)
C3516 SCD1U10V2KX-5GP (10/100)

Close to pin5

If use internal LDO, pop R3504 and C3545.
De-pop L3501, C3504 and C3517

Important: Ar8151 doesn't support LDO mode

+3.3V_RUN — R3508 0R3J-0-U-GP (DY) — +3.3V_LAN
R3507 0R3J-0-U-GP (DY)

+3.3V_ALW

0303

Q3501 SI2301CDS-T1-GE3-GP

C3526 SCD1U10V2KX-5GP
R3506 10KR2J-3-GP
PM_LAN_ENABLE — R3512 1KR2J-1-GP — PM_LAN_ENABLE_R

C3527 SCD1U10V2KX-5GP
C3528 SC4D7U6D3V3KX-GP
C3529 SCD1U10V2KX-5GP
C3530 SC4D7U6D3V3KX-GP (DY)

0309

C3525 SCD01U50V2KX-1GP

0225

37 PM_LAN_ENABLE — Q3503 2N7002A-7-GP (GP)

0309

+3.3V_LAN

C3544 SC10U6D3V3MX-GP (DY)
C3542 SC10U6D3V3MX-GP (DY)
C3543 SC1U6D3V2KX-GP
C3515 SCD1U10V2KX-5GP
C3503 SC1KP50V2KX-1GP

Place near pin1

Pin6 is the AVDDL LDO output, 1uF+0.1uF(C3547 and C3518) close to Pin6;
C3522, C3521 close to Pin31, Pin34 respectively.
Pin9 is the AVDDH LDO output, 1uF+0.1uF(C3548 and C3519) close to Pin9;
C3520 close to Pin22.
Pin37 is the DVDDL LDO output, 1uF+0.1uF(C3549 and C3523) close to Pin37;
C3524 close to Pin24.

MDI0- MDI0+ MDI1- MDI1+ MDI2- MDI2+ MDI3- MDI3+ — 61

X01

LAN_X2 — C3511 SC15P50V2JN-2-GP — X3501 XTAL-25MHZ-102-GP — C3512 SC15P50V2JN-2-GP — LAN_X1

C3521 SCD1U10V2KX-5GP LAN_AVDDL
C3522 SCD1U10V2KX-5GP
C3547 SC1U6D3V2KX-GP
C3518 SCD1U10V2KX-5GP

C3548 SC1U6D3V2KX-GP LAN_AVDDH
C3519 SCD1U10V2KX-5GP
C3520 SCD1U10V2KX-5GP

C3549 SC1U6D3V2KX-GP LAN_DVDDL
C3523 SCD1U10V2KX-5GP
C3524 SCD1U10V2KX-5GP

U3501

AVDDL (31, 34) — AVDDL_REG (6) — AVDDH (22) — AVDDH_REG (9) — DVDDL (24, 37) — DVDDL_REG — VDD33 (1) — +3.3V_LAN
VDDCT (5) — VDDCT_REG (4) — LAN_VDDCT, LAN_VDDCT_REG
LED0 (38) — LED1 (39) — LAN_LED_ACTn, LAN_LED_LINK
SMCLK (25) — SMDATA (26)
PERST# (2) — WAKE# (3) — RBIAS (10) — CLKREQ# (23) — TESTMODE (27) — LX (40) — LAN_LX
GND (41)

TX_N (29) — TX_P (30) — PCIE_RXN3_C, PCIE_RXP3_C — SCD1U10V2KX-5GP — C3539, C3538 — PCIE_RXN1 12, PCIE_RXP1 12
RX_N (36) — RX_P (35) — PCIE_TXN1, PCIE_TXP1
TRXN0 (12) — TRXP0 (11) — TRXN1 (15) — TRXP1 (14) — MDI0-, MDI0+, MDI1-, MDI1+ — SRN49D9F-1-GP — RN3501
REFCLK_N (32) — REFCLK_P (33) — CLK_PCIE_LAN# 20, CLK_PCIE_LAN 20
XTLO (7) — XTLI (8) — LAN_X2, LAN_X1
NC#13 (13) — NC#16 (16) — NC#17 (17) — NC#18 (18) — NC#19 (19) — NC#20 (20) — NC#21 (21) — NC#28 (28)

AR8152-BL1A-R-GP

C3501 SC1KP50V2KX-1GP — MDI0
C3513 SCD1U10V2KX-5GP
C3502 SC1KP50V2KX-1GP — MDI1
C3514 SCD1U10V2KX-5GP

+3.3V_LAN — R3520 4K7R2J-2-GP — LAN_CLKREQ# — R3509 0R2J-2-GP (10/100) — LAN_CLKREQ# C

20,64,70 PLTRST#_LAN_WLAN — R3503 0R0402-PAD — PLT_RST#_LAN
21 PCIE_WAKE# — R3502 2K37R2F-GP — RBIAS
LAN_CLKREQ# C
LAN_LX

C3510 SC100P50V2JN-3GP (DY)

LAN_AVDDL C3534 SCD1U10V2KX-5GP (GIGA)
LAN_AVDDH C3533 SCD1U10V2KX-5GP (GIGA)
LAN_AVDDL C3532 SCD1U10V2KX-5GP (GIGA)

MDI2+ MDI2- MDI3+ MDI3- — SRN49D9F-1-GP — RN3502 (GIGA)

C3536 SC1KP50V2KX-1GP (GIGA)
C3505 SCD1U10V2KX-5GP (GIGA)
C3535 SC1KP50V2KX-1GP (GIGA)
SCD1U10V2KX-5GP (GIGA)

If overclocking, de-pop R3514 and C3551

LAN_LED_ACTn — R3514 5K1R2J-4-GP — C3551 SC470P50V2KX-3GP (DY)

If use LDO mode, pop R3516 and C3550

LAN_LED_LINK — R3516 5K1R2J-4-GP (DY) — C3550 SC470P50V2KX-3GP (DY)

GIGA LAN use 71.08151.003

<Core Design>

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Title: AR8152/AR8151

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A3	Chelsea DJ2 AMD UMA	A00

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Title

Reserved

Size	Document Number	Rev
A3	*Chelsea DJ2 AMD UMA*	*A00*

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SSID = KBC

CAP close to VCC-GND pin pair

	VER2	VER1	VER0
X00	0	0	0
X01	0	0	1
X02	0	1	0
A00	0	1	1

KBC CLK EMI

Place close to KBC

Internal PU

For EC to detect leakage

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Title: KBC Nuvoton NPCE781BA0DX

Size: A2 | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *A00*

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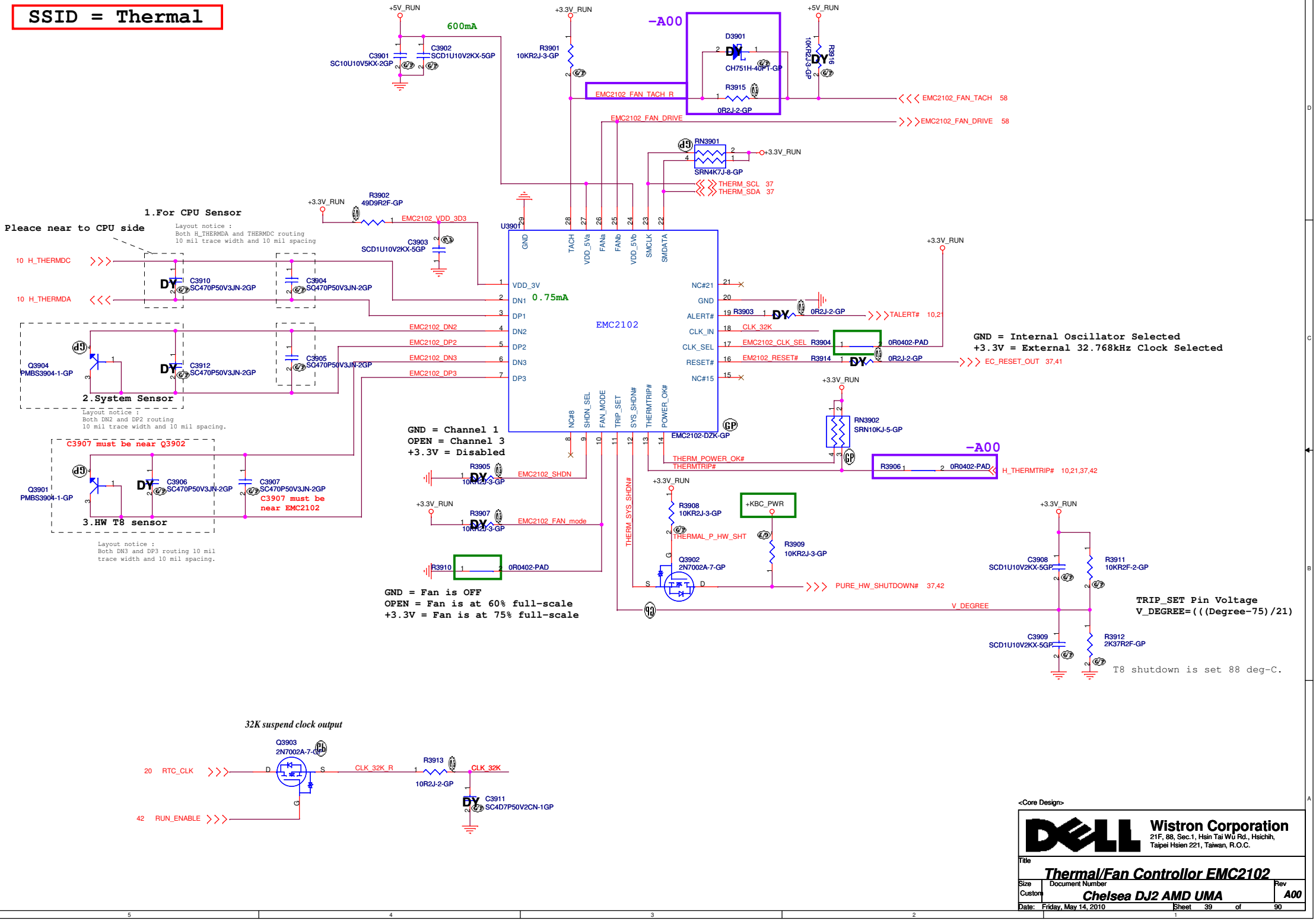
SSID = Thermal



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size	Document Number	Rev
Custom	Chelsea DJ2 AMD UMA	A00

Date: Friday, May 14, 2010 Sheet 39 of 90

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<Core Design>

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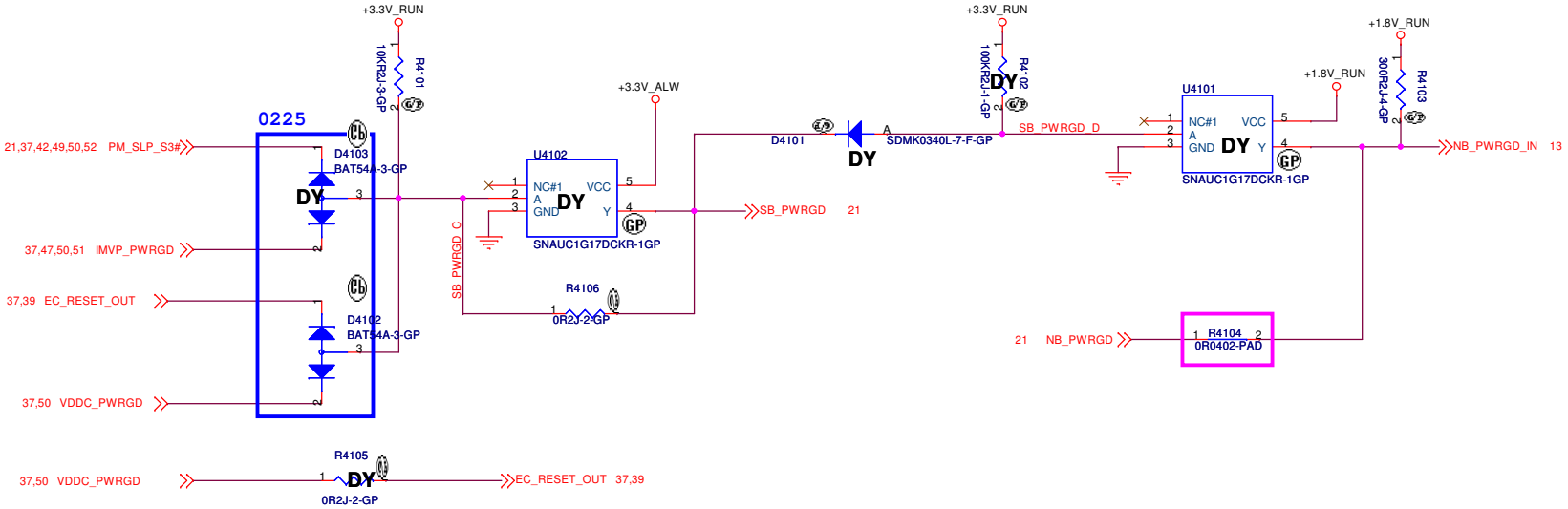
Title: *Reserved*

Size	Document Number	Rev
A3	*Chelsea DJ2 AMD UMA*	*A00*

Date: Friday, May 14, 2010 Sheet 40 of 90

SSID = Reset.Suspend

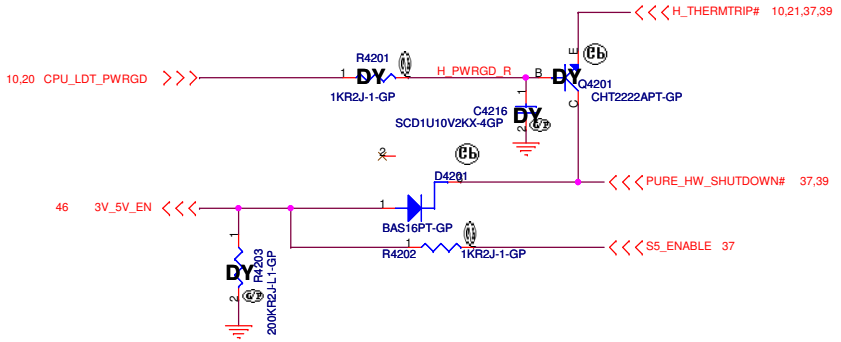


<Core Design>

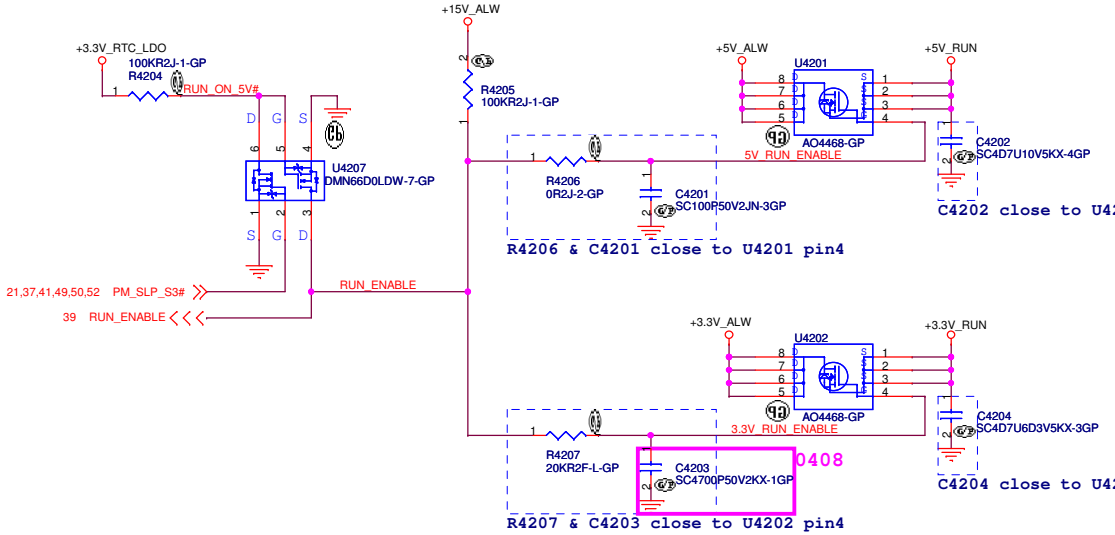
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power On Logic*		
Size: A3	Document Number: *Chelsea DJ2 AMD UMA*	Rev: *A00*
Date: Friday, May 14, 2010	Sheet 41 of 90	

SSID = Reset.Suspend



Run Power



Peak current: 6257.3mA (HD:1100 ODD:2500)
Design current: 4380.11 mA
11.6A
Rds=14m ohm

C4202 close to U4201 pin1~3

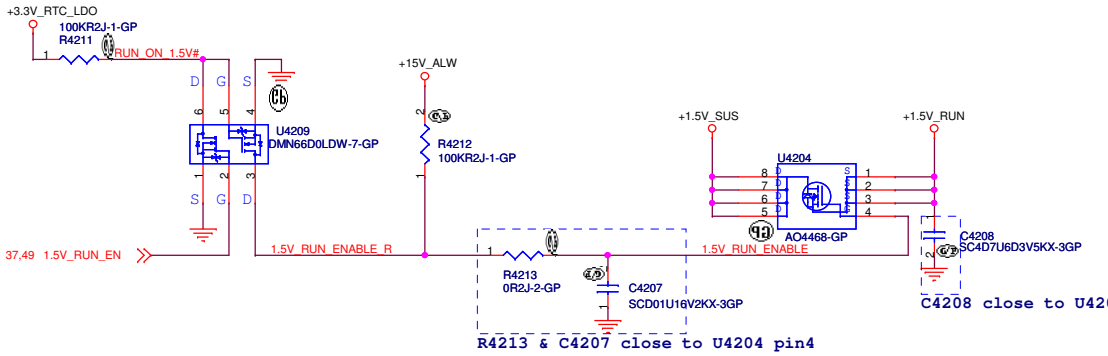
R4206 & C4201 close to U4201 pin4

Peak current: 5966mA
Design current: 4177 mA
11.6A
Rds=14m ohm

0408

C4204 close to U4202 pin1~3

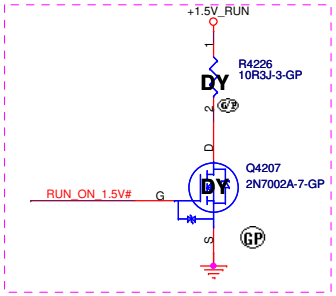
R4207 & C4203 close to U4202 pin4



Peak current: 1230mA
Design current: 861 mA
11.6A
Rds=14m ohm

C4208 close to U4204 pin1~3

R4213 & C4207 close to U4204 pin4



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size: Custom | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

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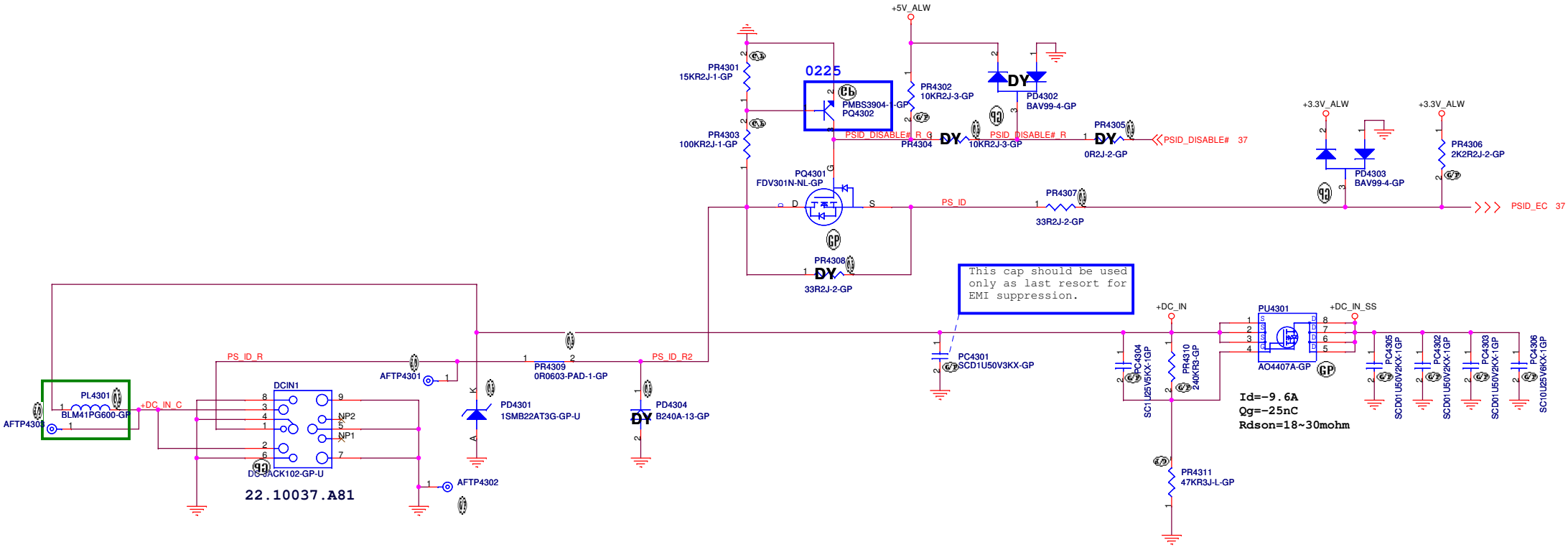
SSID = PWR.Support

DCIN CONN



<Variant Name>

Wistron Corporation
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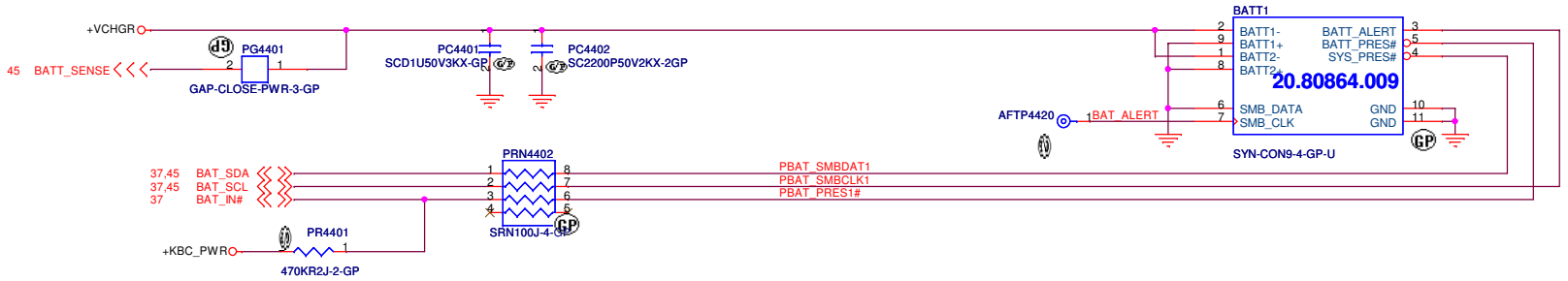
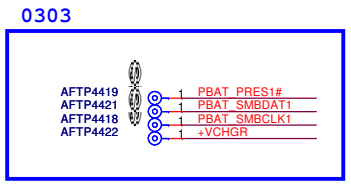
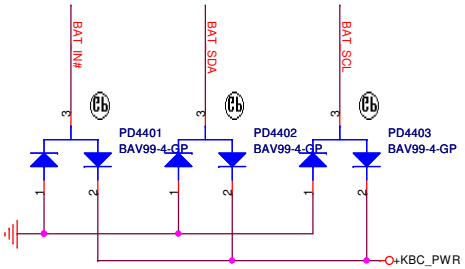
Title			
DCIN			
Size: A3	Document Number: Chelsea DJ2 AMD UMA		Rev: A00
Date: Friday, May 14, 2010	Sheet 43 of 90		

Batt Connecter







<Core Design>

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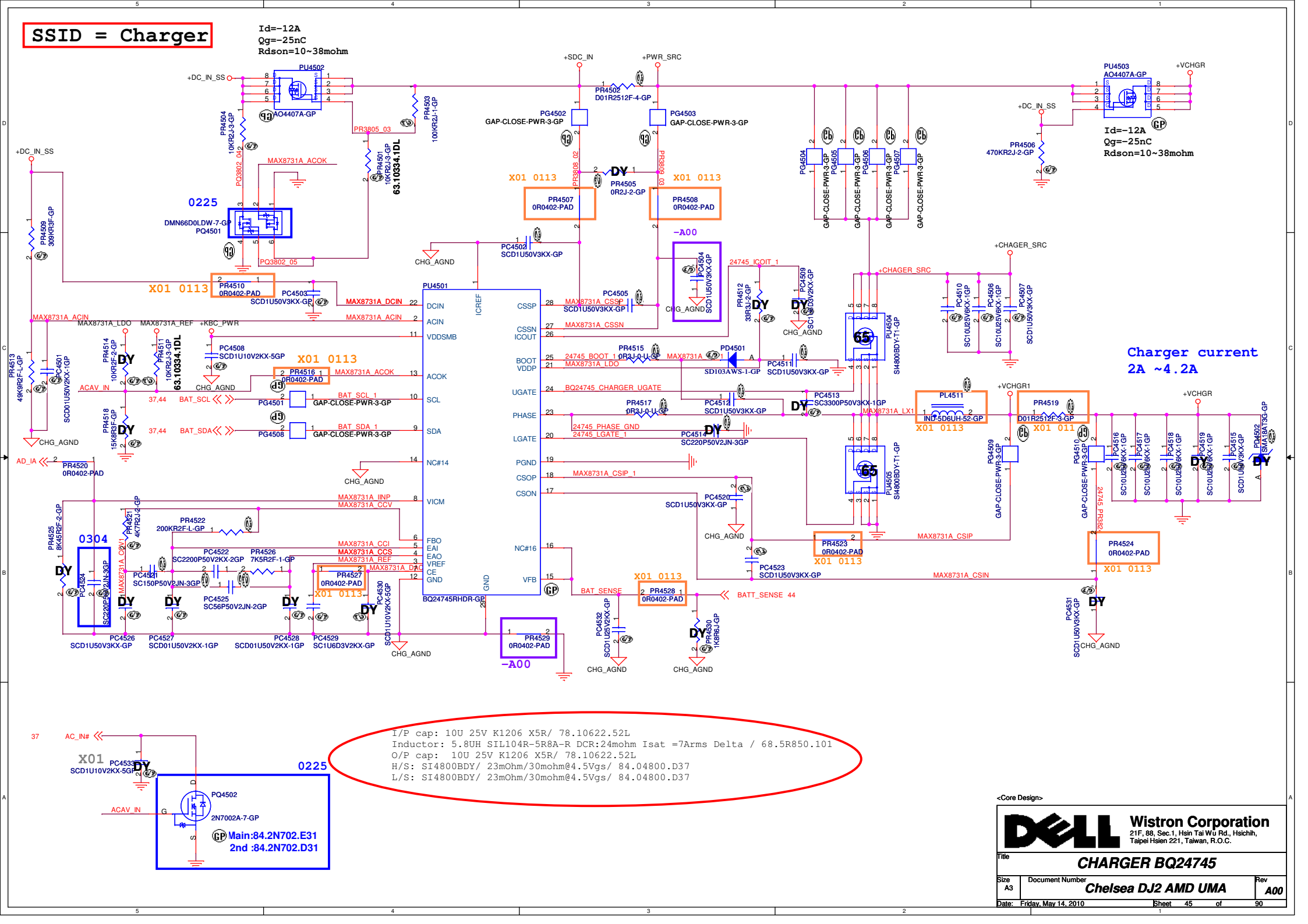
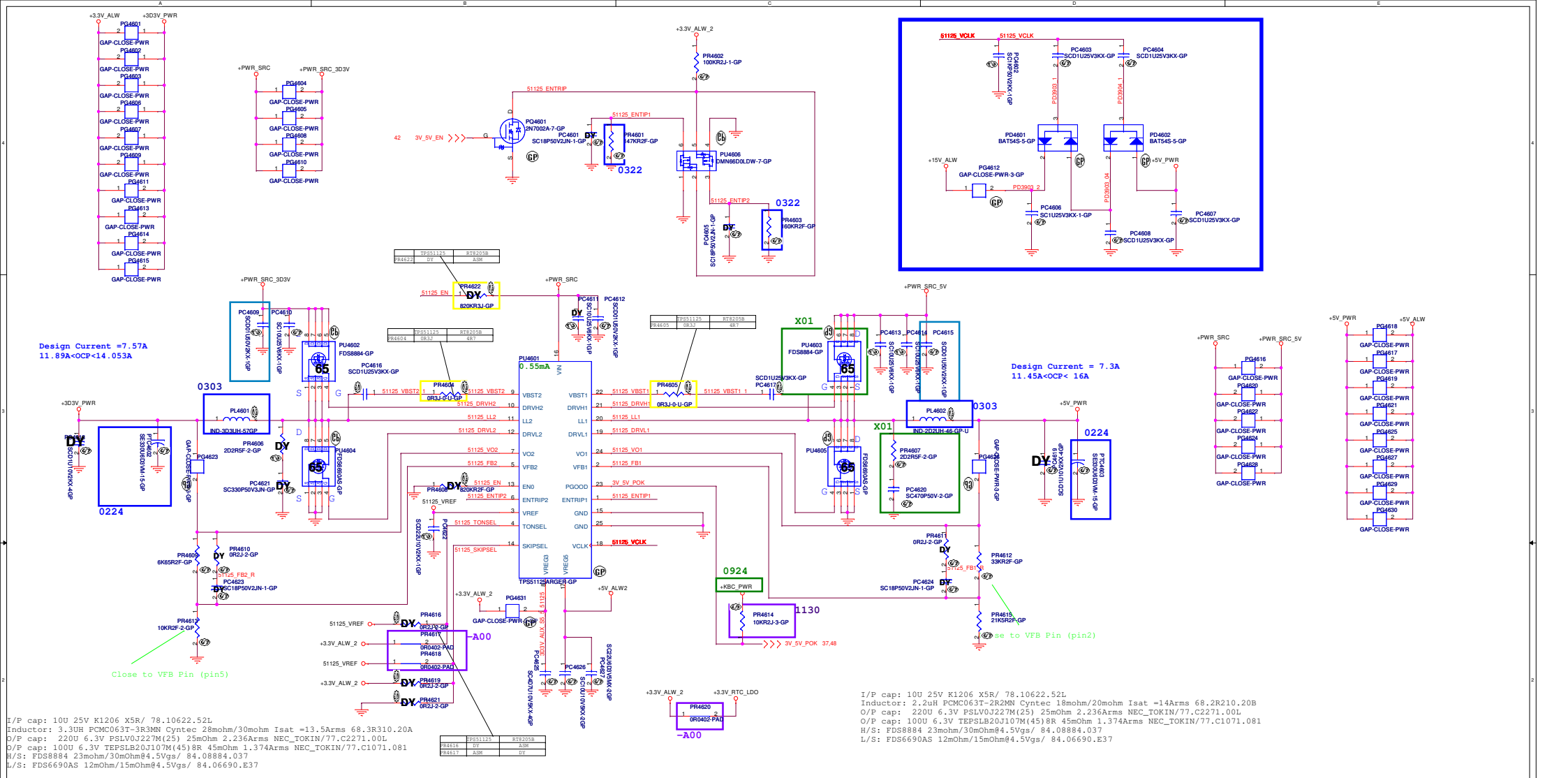
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN		
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: A00
Date: Friday, May 14, 2010	Sheet 44 of 90	


SSID = Charger
Id=-12A
Qg=-25nC
Rdson=10~38mohm
PU4502
AO4407A-GP
+DC_IN_SS
+SDC_IN
+PWR_SRC
PR4502
D01R2512F-4-GP
PG4502
GAP-CLOSE-PWR-3-GP
PG4503
GAP-CLOSE-PWR-3-GP
PU4503
AO4407A-GP
+VCHGR
Id=-12A
Qg=-25nC
Rdson=10~38mohm
PR4506
470KR2J-2-GP
PR4504
10KR2J-3-GP
PR4503
100KR2J-1-GP
PR3805_03
PR4501
10KR2J-3-GP
63.10334.1DL
MAX8731A_ACOK
PQ3802_04
PQ3802_05
0225
DMN66D0LDW-7-GP
PQ4501
PR4509
309KR3F-GP
X01 0113
PR4510
0R0402-PAD
PC4503
SCD1U50V3KX-GP
MAX8731A_DCIN
MAX8731A_ACIN
MAX8731A_LDO
MAX8731A_REF
+KBC_PWR
PR4513
49K9R2F-L-GP
PC4501
SCD1U50V2KX-1GP
PR4514
10KR2F-2-GP
DY
PR4511
10KR2J-3-GP
63.10334.1DL
PC4508
SCD1U10V2KX-5GP
X01 0113
PR4516
0R0402-PAD
MAX8731A_ACOK
ACAV_IN
CHG_AGND
37,44
BAT_SCL
BAT_SCL_1
PG4501
GAP-CLOSE-PWR-3-GP
PR4518
15K9R2F-GP
37,44
BAT_SDA
BAT_SDA_1
PG4508
GAP-CLOSE-PWR-3-GP
AD_IA
PR4520
0R0402-PAD
PU4501
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
NC#16
VFB
ICREF
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
BQ24745RHDR-GP
PR4522
200KR2F-L-GP
PR4521
4K7R2J-2-GP
PR4525
8K45R2F-2-GP
0304
PC4524
SC220P50V2JN-3GP
PC4521
SC150P50V2JN-3GP
PC4522
SC2200P50V2KX-2GP
PR4526
7K5R2F-1-GP
PC4525
SC56P50V2JN-2GP
PR4527
0R0402-PAD
X01 0113
PC4530
SCD1U10V2KX-5GP
PC4526
SCD1U50V3KX-GP
PC4527
SCD01U50V2KX-1GP
PC4528
SCD01U50V2KX-1GP
PC4529
SC1U6D3V2KX-GP
CHG_AGND
PR4529
0R0402-PAD
-A00
PC4502
SCD1U50V3KX-GP
CHG_AGND
PR4507
0R0402-PAD
X01 0113
PR4508
0R0402-PAD
X01 0113
-A00
PC4504
SCD1U50V3KX-GP
CHG_AGND
PR3808_02
PR3809_03
PR4505
0R2J-2-GP
DY
PC4505
SCD1U50V3KX-GP
MAX8731A_CSSP
MAX8731A_CSSN
PR4515
0R3J-0-U-GP
MAX8731A
PD4501
SD103AWS-1-GP
24745_ICOIT_1
PR4512
33R3J-2-GP
PC4509
SCD1U25V2KX-GP
CHG_AGND
24745_BOOT_1
MAX8731A_LDO
BQ24745_CHARGER_UGATE
PR4517
0R3J-0-U-GP
PC4512
SCD1U50V3KX-GP
24745_PHASE_GND
24745_LGATE_1
PC4514
SC220P50V2JN-3GP
MAX8731A_CSIP_1
PC4520
SCD1U50V3KX-GP
CHG_AGND
PR4523
0R0402-PAD
X01 0113
MAX8731A_CSIP
PC4523
SCD1U50V3KX-GP
MAX8731A_CSIN
BAT_SENSE
PR4528
0R0402-PAD
X01 0113
BATT_SENSE 44
PC4532
SCD1U25V2KX-GP
CHG_AGND
PR4530
1K8R6J-GP
CHG_AGND
+CHAGER_SRC
PC4513
SC3300P50V3KX-1GP
DY
MAX8731A_LX1
PL4511
IND-5D6UH-52-GP
X01 0113
PU4504
SI4800BDY-T1-GP
PU4505
SI4800BDY-T1-GP
65
65
PC4510
SC10U25V6KX-1GP
PC4506
SC10U25V6KX-1GP
PC4507
SCD1U50V3KX-GP
+VCHGR1
PR4519
D01R2512F-3-GP
X01 011
PG4509
GAP-CLOSE-PWR-3-GP
PC4510
GAP-CLOSE-PWR-3-GP
PC4516
SC10U25V6KX-1GP
PC4517
SC10U25V6KX-1GP
PC4518
SC10U25V6KX-1GP
PC4519
SC10U25V6KX-1GP
PC4515
SCD1U50V3KX-GP
PD4502
SMAJ5A17G-GP
24745_PBST
PR4524
0R0402-PAD
X01 0113
PC4531
SCD1U50V3KX-GP
CHG_AGND
Charger current
2A ~4.2A
37
AC_IN#
X01
PC4533
SCD1U10V2KX-5GP
0225
PQ4502
2N7002A-7-GP
ACAV_IN
Main:84.2N702.E31
2nd :84.2N702.D31
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 5.8UH SIL104R-5R8A-R DCR:24mohm Isat =7Arms Delta / 68.5R850.101
O/P cap: 10U 25V K1206 X5R/ 78.10622.52L
H/S: SI4800BDY/ 23mOhm/30mohm@4.5Vgs/ 84.04800.D37
L/S: SI4800BDY/ 23mOhm/30mohm@4.5Vgs/ 84.04800.D37
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER BQ24745
Size
A3
Document Number
Chelsea DJ2 AMD UMA
Rev
A00
Date: Friday, May 14, 2010
Sheet 45 of 90



RT8205B(74.08208.A73):

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT8205B(74.08205.B73):

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

TPS51125	74.51125.073
RT8205BGQW	74.08205.B73

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51125_5V/3D3V

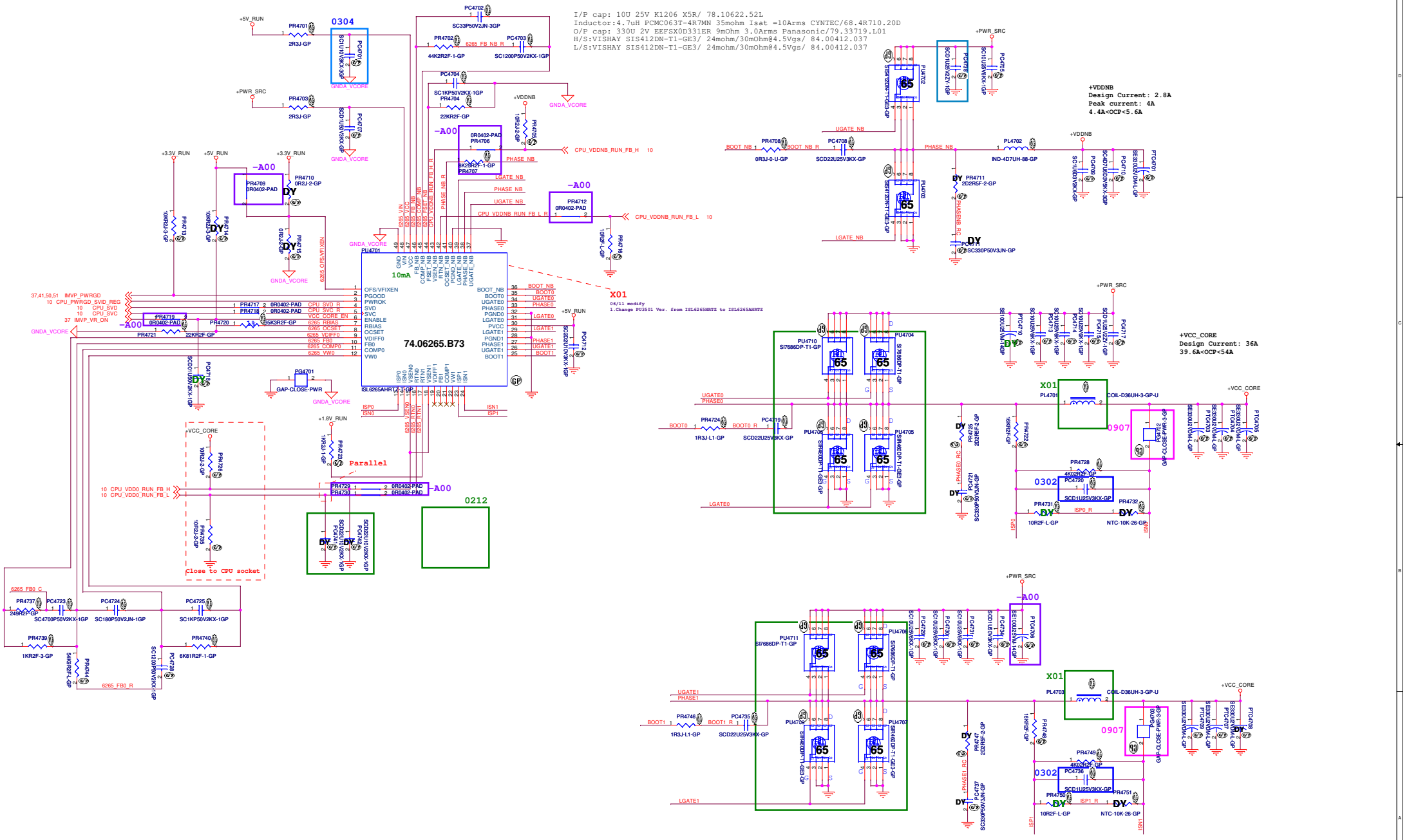
Size: A2 | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

Date: Friday, May 14, 2010 | Sheet 46 of 90

SSID = CPU.Regulator

ISL6265HRTZ-T for +VCC_CORE&+VDDNB

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor:4.7uH PCMC063T-4R7MN 35mohm Isat =10Arms CYNTEC/68.4R710.20D
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm
Isat =60Arms 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

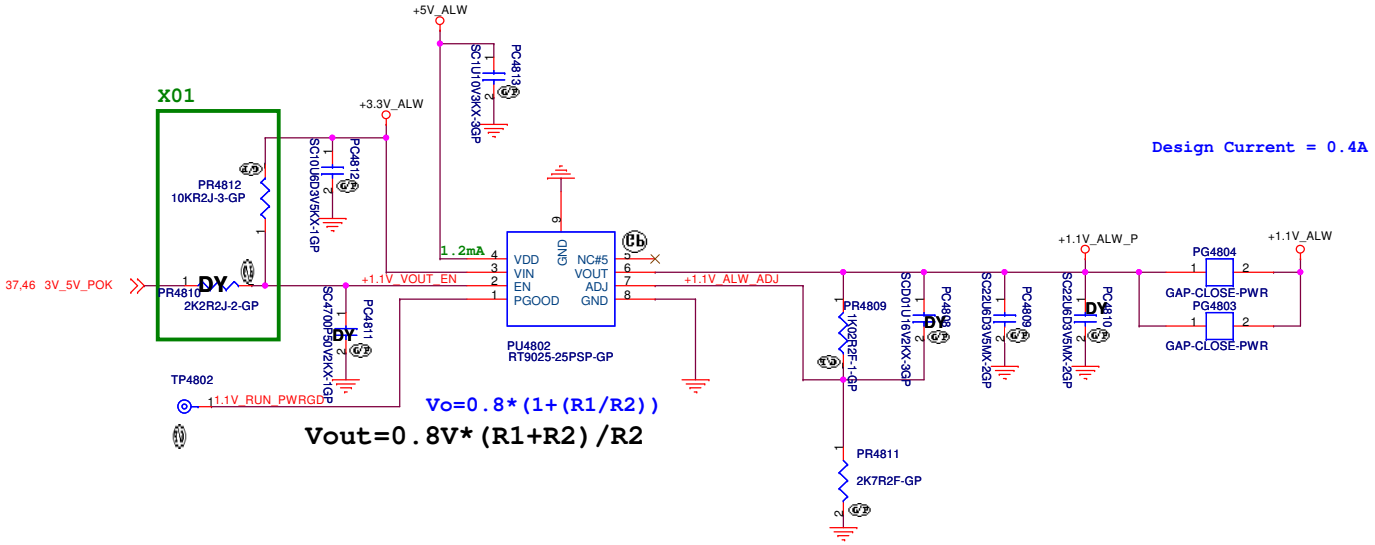
Title: VREG : +VCC_CORE&+VDDNB

Size	Document Number	Rev
A2	Chelsea DJ2 AMD UMA	A00

Date: Friday, May 14, 2010 Sheet 47 of 90

SSID = PWR.Plane.Regulator_+1.1V_RUN

RT9025 for +1.1V_ALW

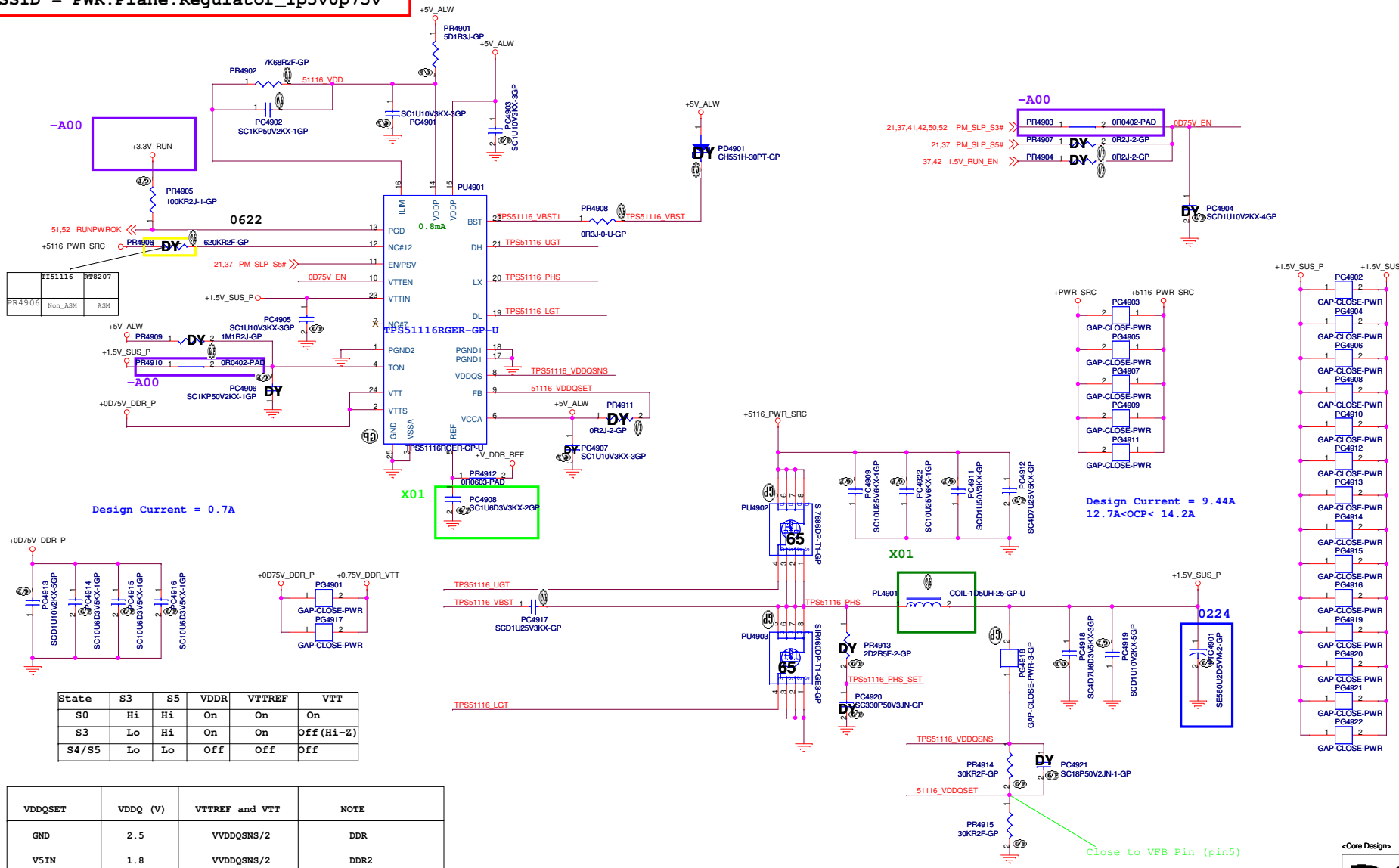


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
RT9025_+1.1VALW		
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: A00
Date: Friday, May 14, 2010	Sheet 48 of 90	

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10J
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: FDS8880 9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mOhm/7.25mOhm@4.5Vgs/ 84.06676.A37

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116RGER_+1.5V_SUS

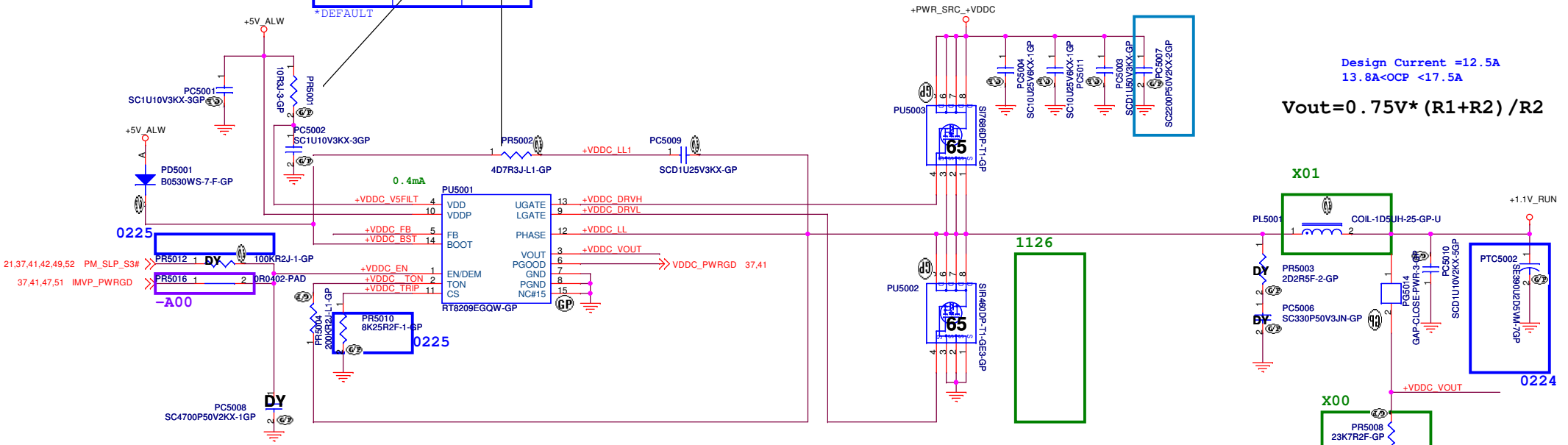
Size	Document Number	Rev
Custom	Chelsea DJ2 AMD UMA	A00

Date: Friday, May 14, 2010 Sheet 49 of 90

SSID = PWR.Plane.Regulator_VDDC

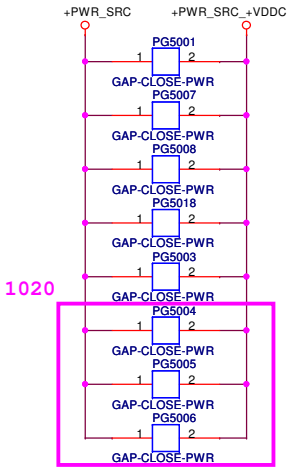
PWM TYPE	PR5001	PR5002
*RT8209E	10 ohm	4.7 ohm
TPS51117	300 ohm	0 ohm

*DEFAULT



Design Current =12.5A
13.8A<OCP <17.5A

Vout=0.75V*(R1+R2)/R2



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

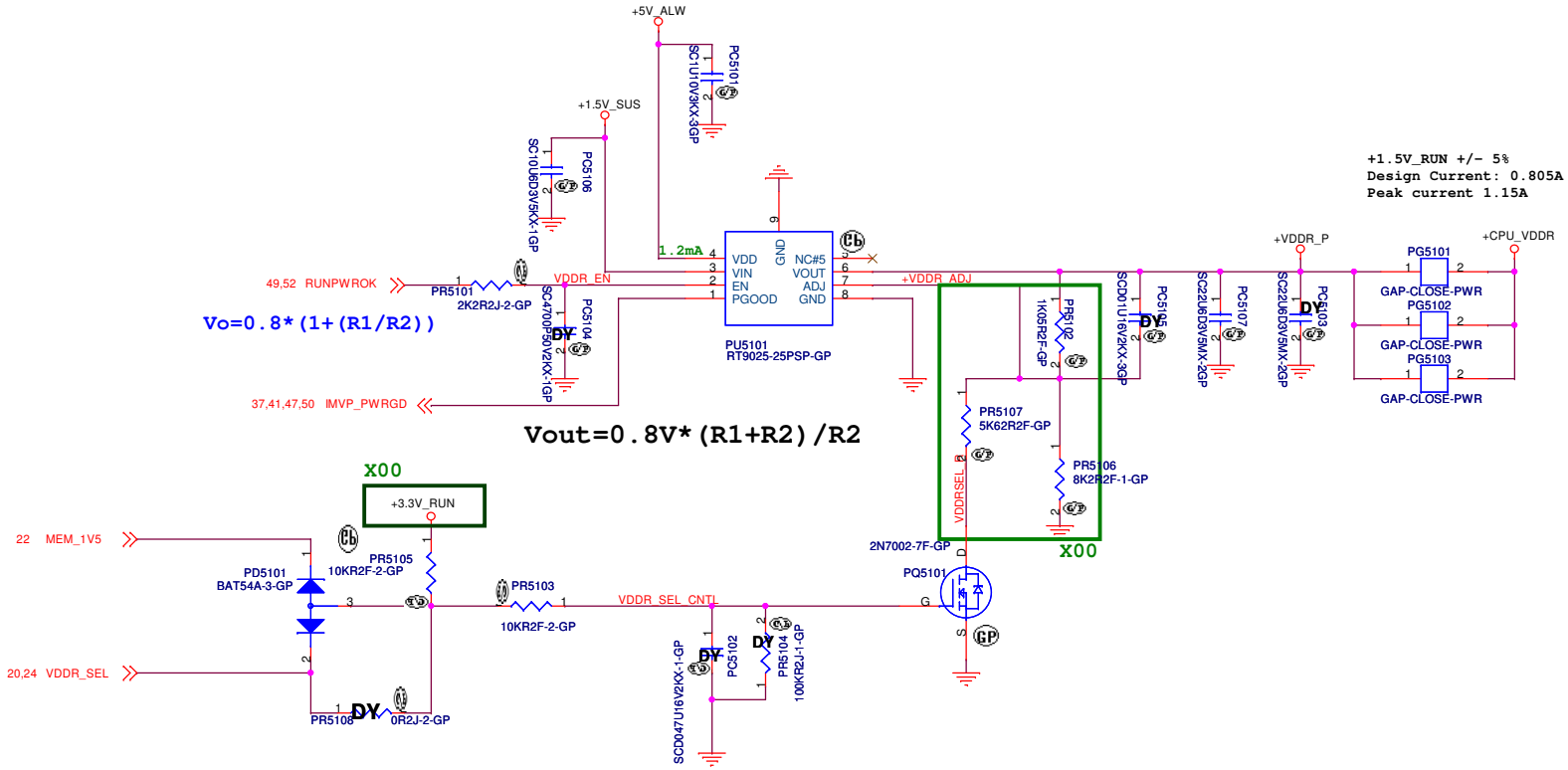
Title: RT8209 +1.1V_RUN

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	A00

Date: Friday, May 14, 2010 Sheet 50 of 90

SSID = PWR.Plane.Regulator_VDDR

RT9025 for +VDDR



VDDR_SEL	+CPU_VDDR
H	1.05V
L	0.9V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

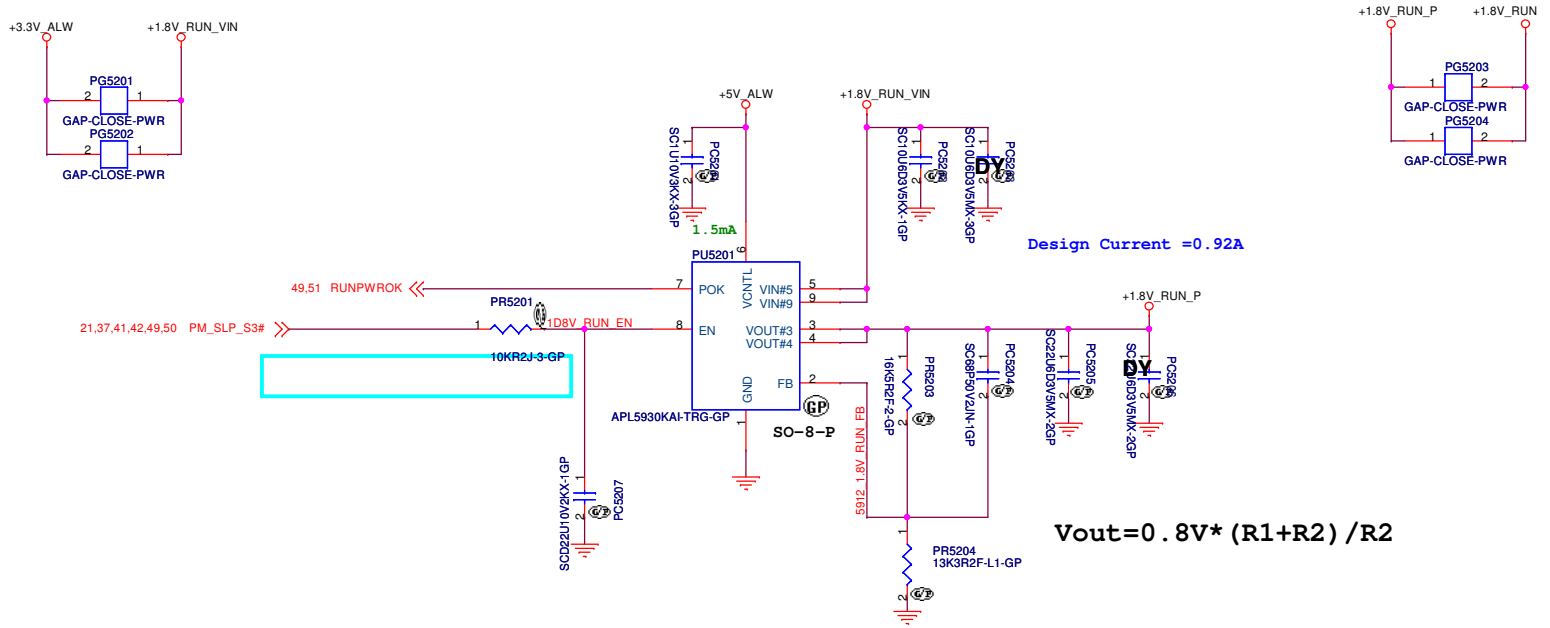
Title: RT9025 +VDDR

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

Date: Friday, May 14, 2010 | Sheet 51 of 90

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



Vout=0.8V*(R1+R2)/R2

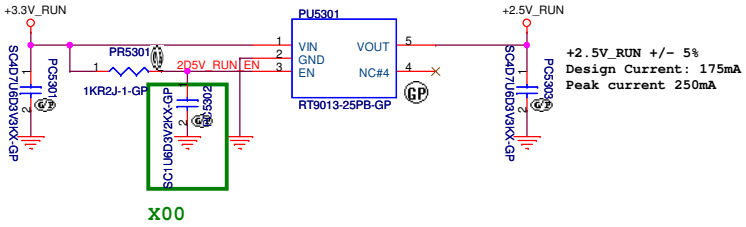
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
APL5930_+1.8V_RUN		
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: A00
Date: Friday, May 14, 2010	Sheet 52 of 90	

SSID = PWR.Plane.Regulator_2p5v

RT9013-25PB for +2.5V_RUN



<Core Design>

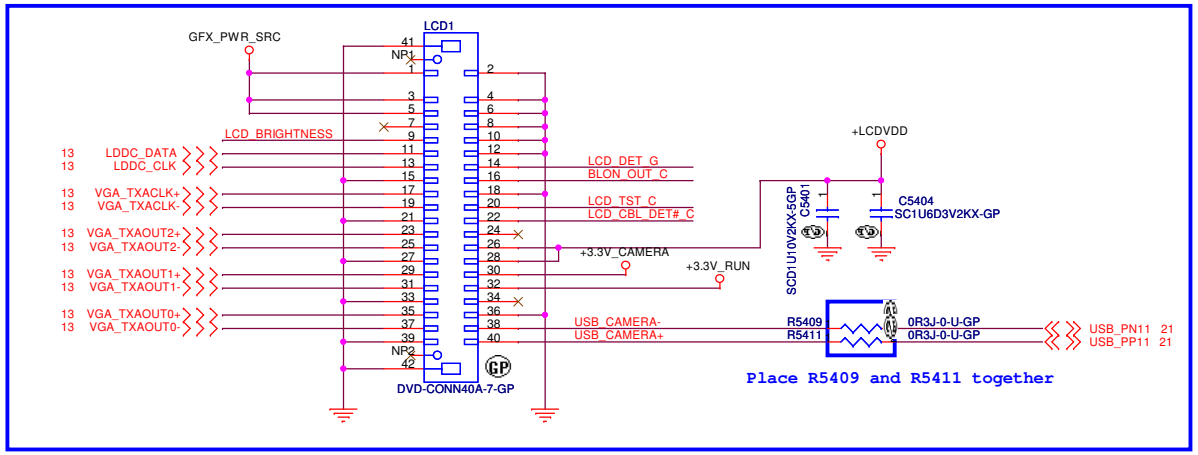
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

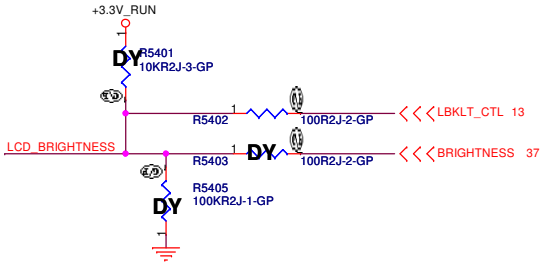
Title: VREG : +CPU_VDDR&+2.5V_RUN		
Size: Custom	Document Number: Chelsea DJ2 AMD UMA	Rev: A00
Date: Friday, May 14, 2010	Sheet 53 of 90	

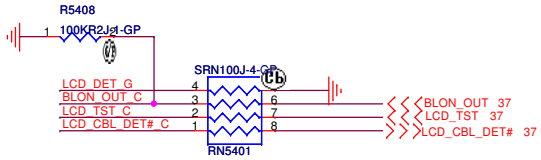
SSID = VIDEO

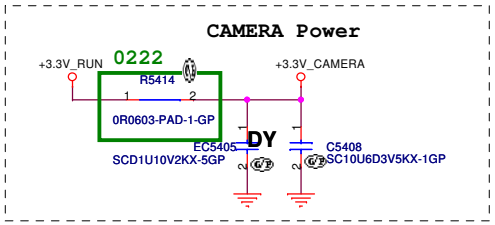
LVDS CONNECTOR

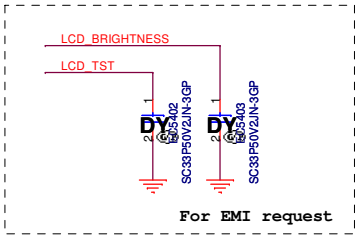
0225





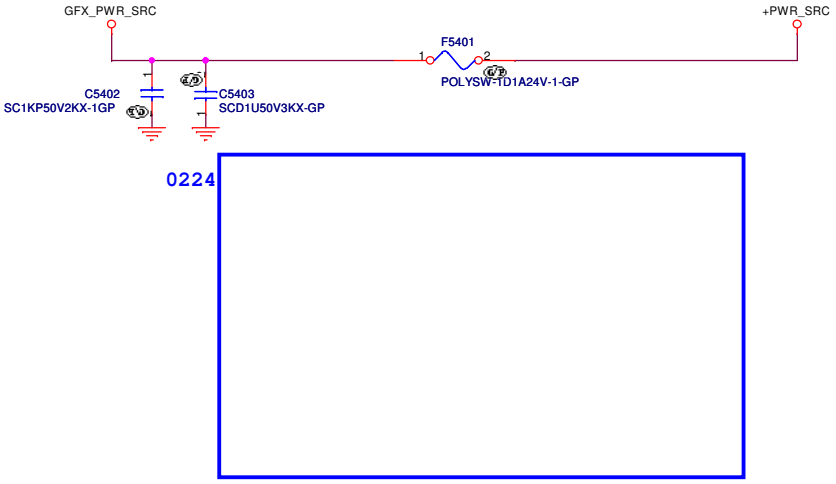






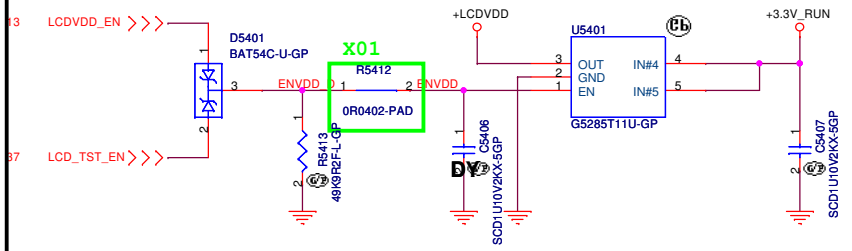
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



<Core Design>

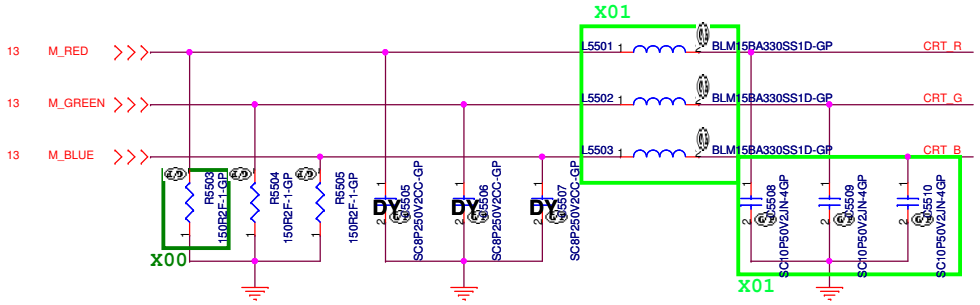
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

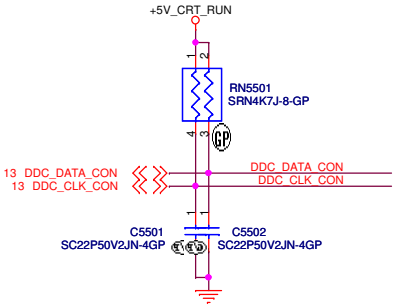
Title		
LCD/Inverter Connector		
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: A00
Date: Friday, May 14, 2010	Sheet 54 of 90	

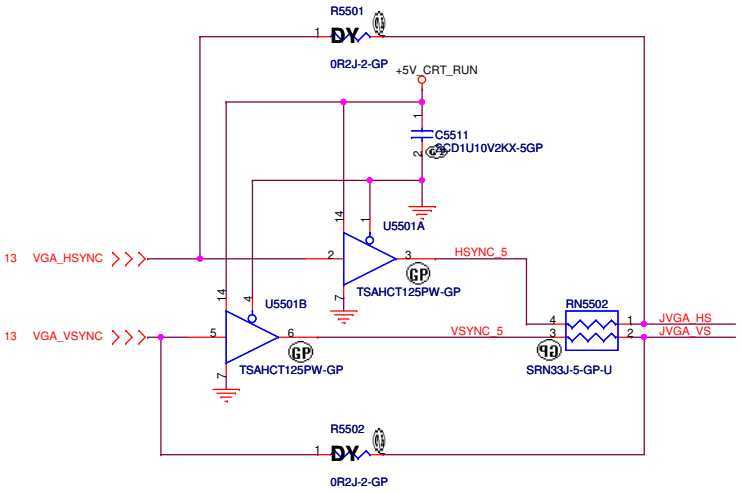
SSID = VIDEO

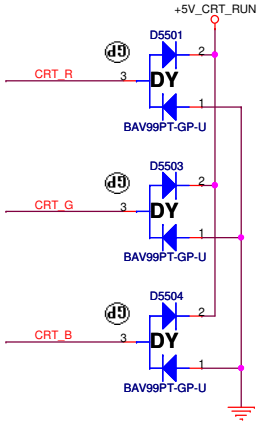
Layout Note:

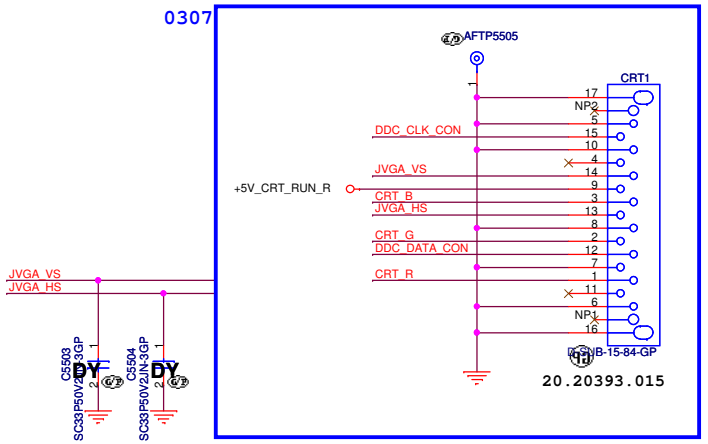
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

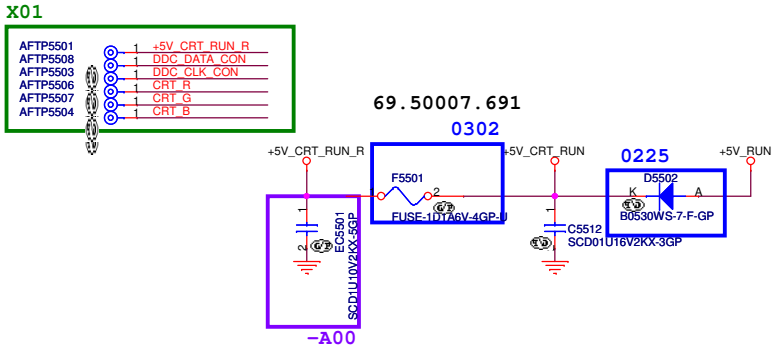


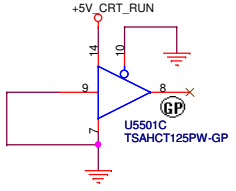


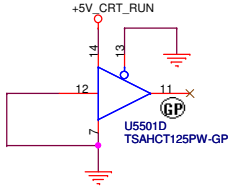












<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size | Document Number: **Chelsea DJ2 AMD UMA** | Rev: A00

Date: Friday, May 14, 2010 | Sheet 55 of 90

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *A00*

Date: Friday, May 14, 2010 | Sheet 56 of 90

SSID = VIDEO

HDMI CONNECTOR

0307

HDMI_CN_DATA2 — R5725 — HDMI_CN_DATA2_R
HDMI_CN_DATA2# — R5726 — HDMI_CN_DATA2#_R

0R3J-0-U-GP

put R5725 and R5726 together

0307

HDMI_CN_DATA1 — R5727 — HDMI_CN_DATA1_R
HDMI_CN_DATA1# — R5728 — HDMI_CN_DATA1#_R

0R3J-0-U-GP

put R5727 and R5728 together

0307

HDMI_CN_DATA0 — R5729 — HDMI_CN_DATA0_R
HDMI_CN_DATA0# — R5730 — HDMI_CN_DATA0#_R

0R3J-0-U-GP

put R5729 and R5730 together

0307

HDMI_CN_CLK — R5731 — HDMI_CN_CLK_R
HDMI_CN_CLK# — R5732 — HDMI_CN_CLK#_R

0R3J-0-U-GP

put R5731 and R5732 together

HDMI CONN

HDMI1 — SKT-HDMI19P-63-GP-U

HDMI_CN_DATA2_R
HDMI_CN_DATA2#_R
HDMI_CN_DATA1_R
HDMI_CN_DATA1#_R
HDMI_CN_DATA0_R
HDMI_CN_DATA0#_R
HDMI_CN_CLK_R
HDMI_CN_CLK#_R
DDC_CLK_HDMI
DDC_DATA_HDMI
HPD_HDMI_CON

0302 +5V_CRT_RUN_R — SCD1U10V2KX-5GP

22.10296.171

0302 +5V_CRT_RUN

RN5701 SRN4K7J-8-GP

5V Tolerance

13 DDC_CLK_HDMI → DDC_CLK_HDMI
13 DDC_DATA_HDMI → DDC_DATA_HDMI

12 HDMI_CN_CLK# → HDMI_CN_CLK#
12 HDMI_CN_CLK → HDMI_CN_CLK
12 HDMI_CN_DATA0# → HDMI_CN_DATA0#
12 HDMI_CN_DATA0 → HDMI_CN_DATA0

12 HDMI_CN_DATA1# → HDMI_CN_DATA1#
12 HDMI_CN_DATA1 → HDMI_CN_DATA1
12 HDMI_CN_DATA2# → HDMI_CN_DATA2#
12 HDMI_CN_DATA2 → HDMI_CN_DATA2

0307

R5715 R5716 R5717 R5718 R5719 R5720 R5721 R5722

+3.3V_RUN

Q5702 PMBS3904-1-GP

HPD_HDMI_1 — R5710 150KR2J-L1-GP — HPD_HDMI_CON

13 HDMI_HPD_DET

R5713 10KR2J-3-GP

R5712 200KR2J-L1-GP

+5V_RUN

R5724 0R2J-2-GP

HDMI_PLL_GND

HDMI_PLL_GATE

Q5703 2N7002A-7-GP

R5714 100KR2J-1-GP

<Core Design>

Wistron Corporation
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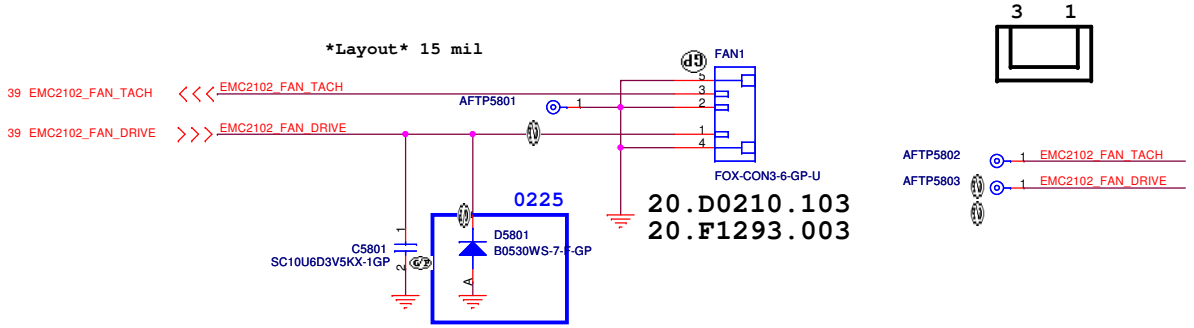
Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDMI Level Shifter/Connector		
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: A00
Date: Friday, May 14, 2010	Sheet 57 of 90	

SSID = Thermal

Fan Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP/Fan Connector		
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: A00
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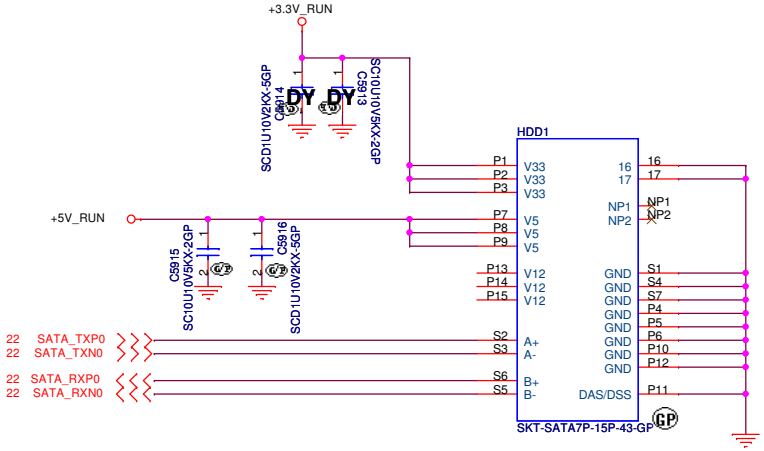
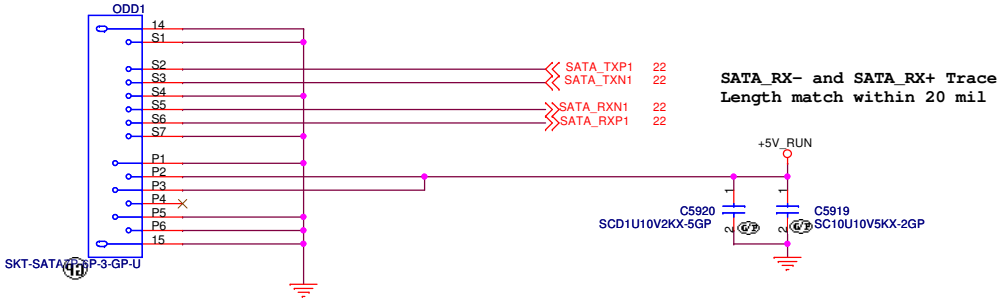
SSID = SATA

SATA HDD Connector



22.10300.A81

ODD Connector



22.10300.801

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
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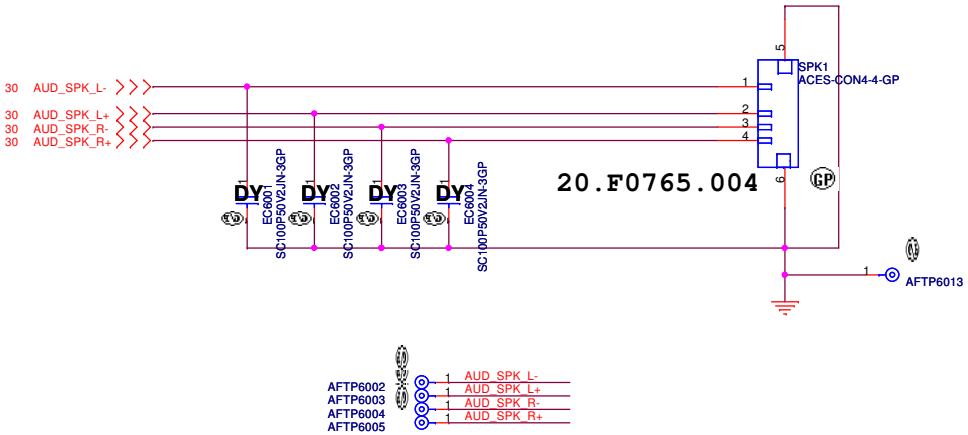
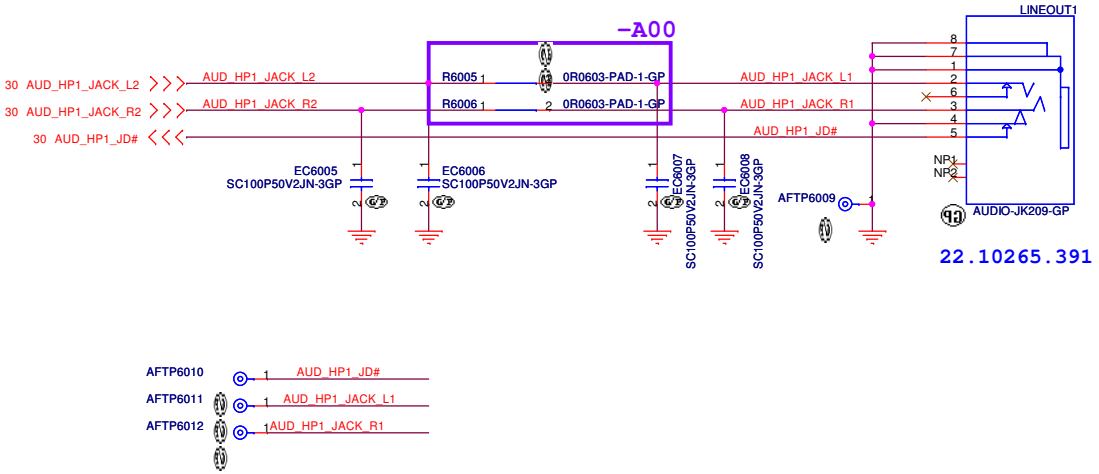
SSID = AUDIO

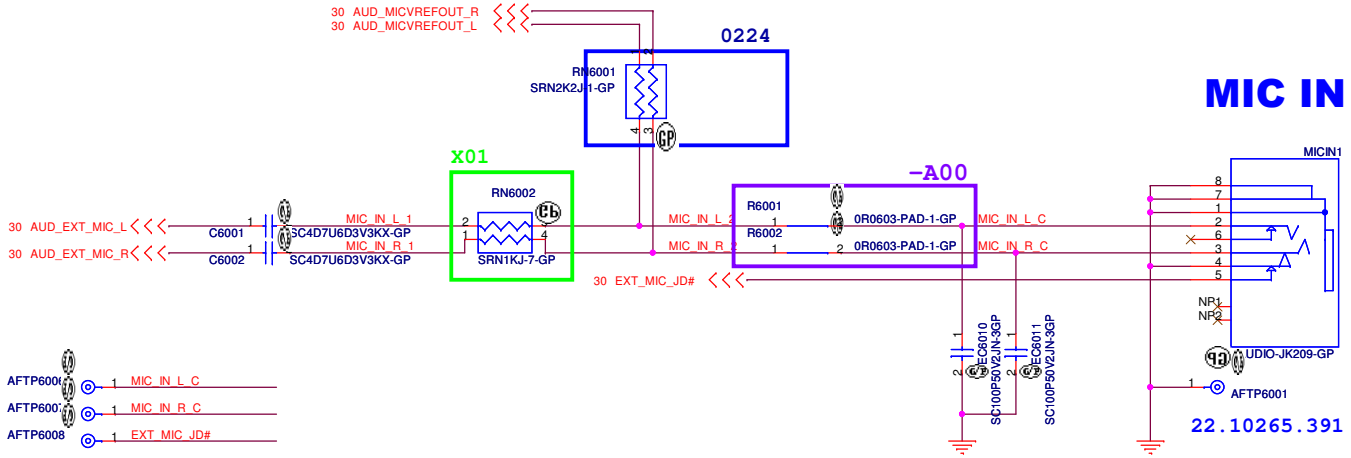
Speaker Connector



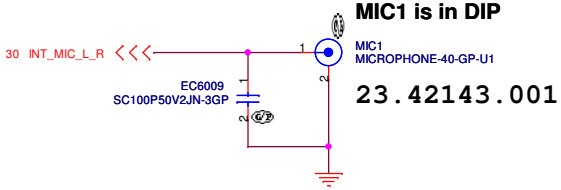
LINE1 OUT



MIC IN



Internal Microphone



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

Size	Document Number	Rev
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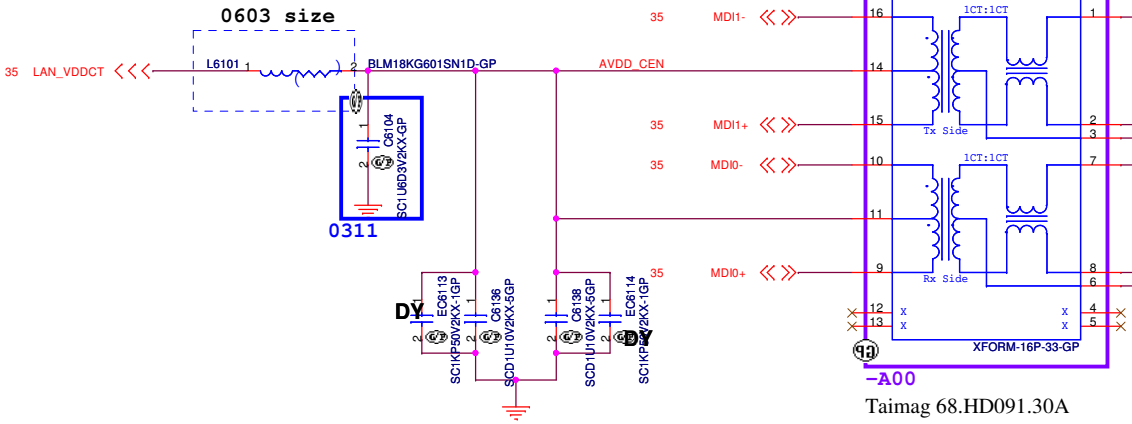
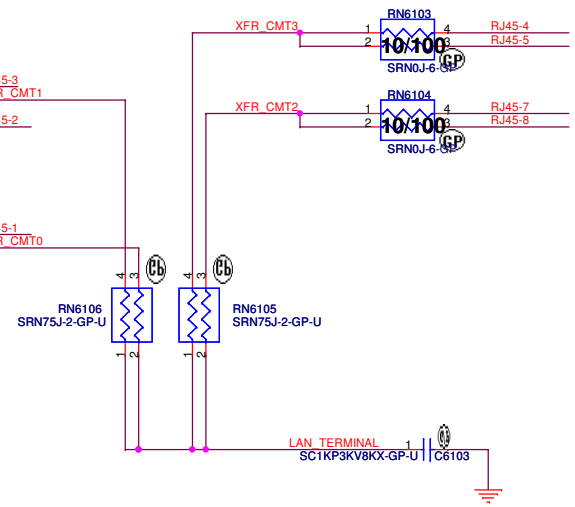
```
2009-10-1 Change MDI1+(XF601.16) to MDI1+(XF601.15)
          Change MDI1-(XF601.15) to MDI1-(XF601.16)
          Change MDI0+(XF601.10) to MDI0+(XF601.9)
          Change MDI0-(XF601.9) to MDI0-(XF601.10)
          Change RJ45-3(XF601.1) to RJ45-3(XF601.2)
          Change RJ45-6(XF601.2) to RJ45-6(XF601.1)
          Change RJ45-1(XF601.7) to RJ45-1(XF601.8)
          Change RJ45-2(XF601.8) to RJ45-2(XF601.7)
```

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

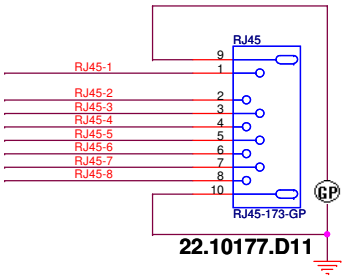
10/100M Lan Transformer

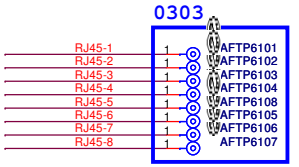


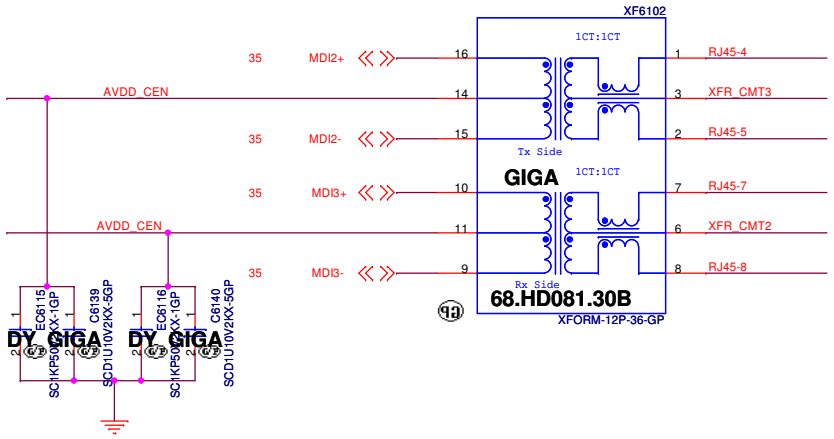
Taimag 68.HD091.30A

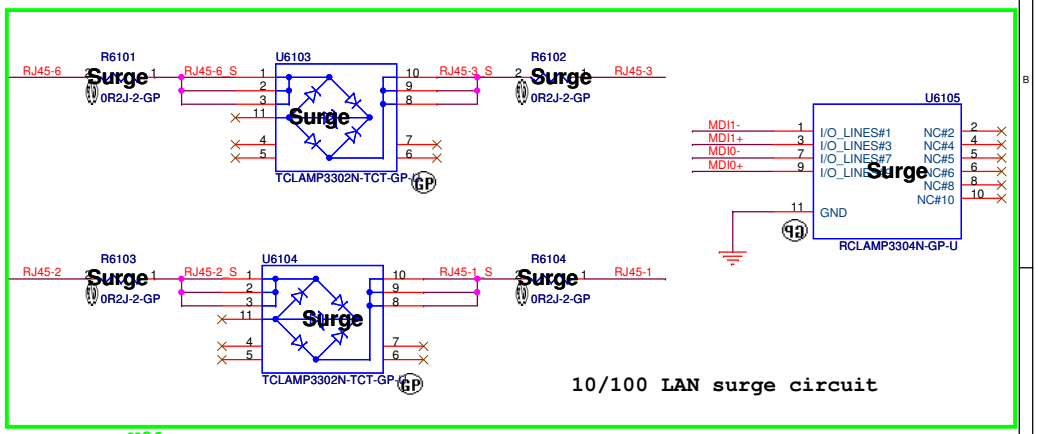


RJ45 Connector









<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	*XFORM/RJ45*	
Size A3	Document Number *Chelsea DJ2 AMD UMA*	Rev *A00*
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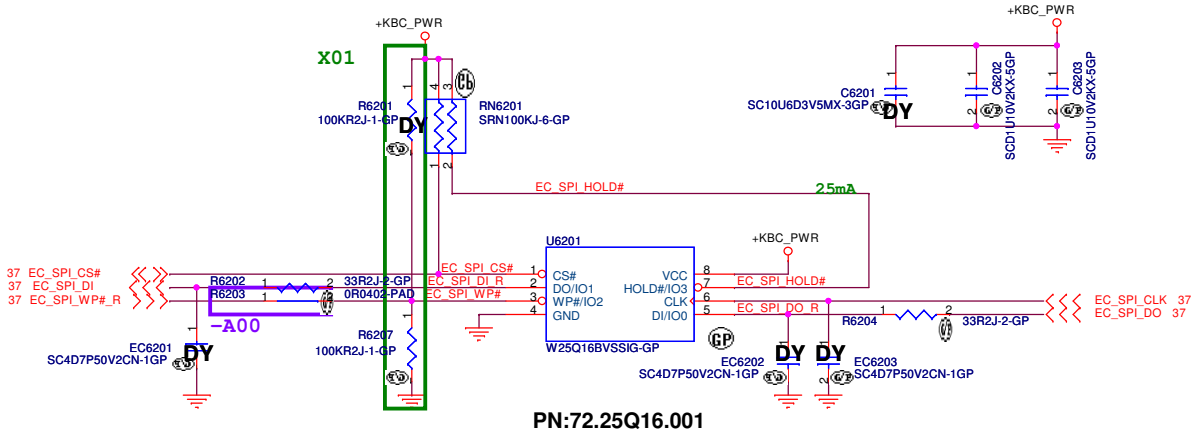
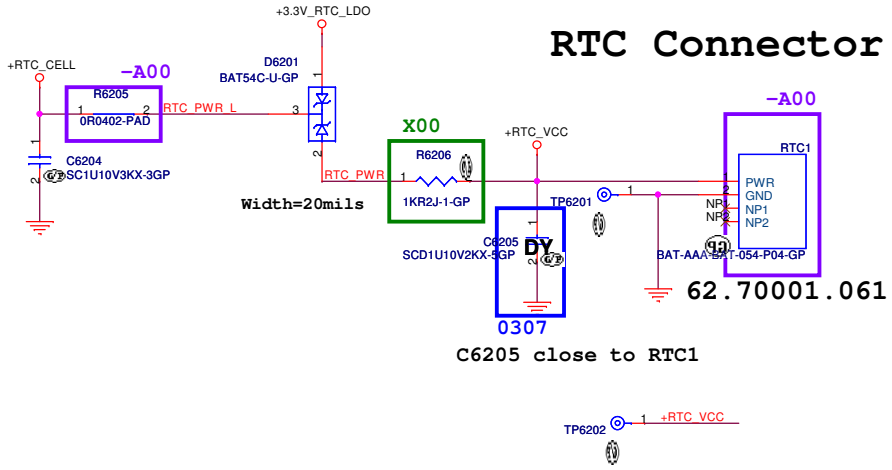
SSID = Flash.ROM

SPI FLASH ROM (16M bits) for KBC



SSID = RBATT



<Core Design>

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Title	Flash/RTC	
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: A00
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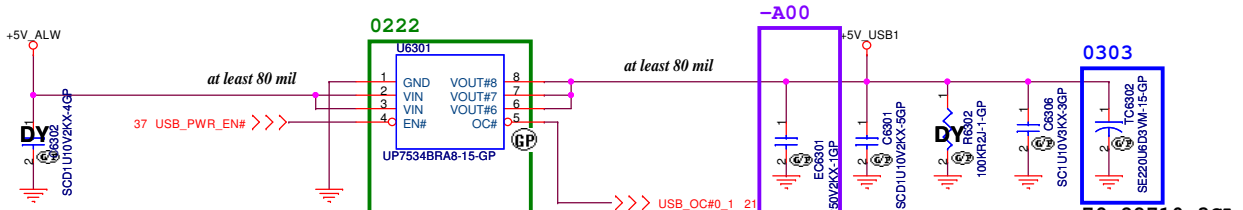
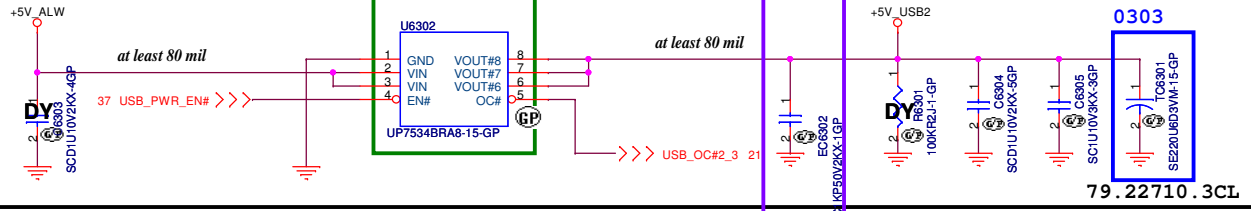
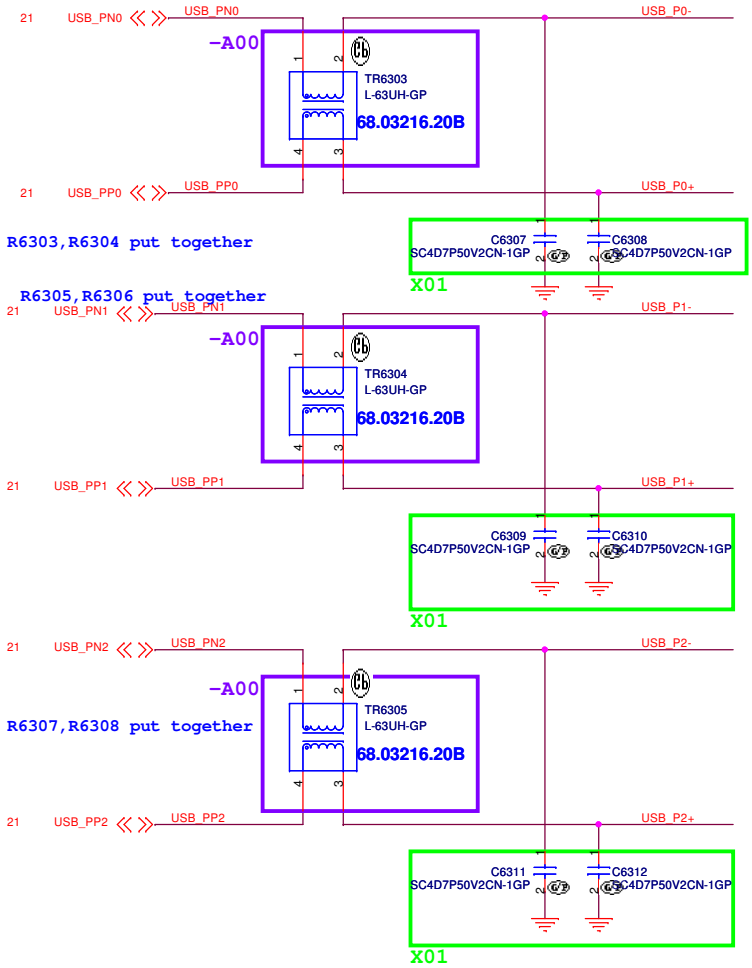
SSID = USB

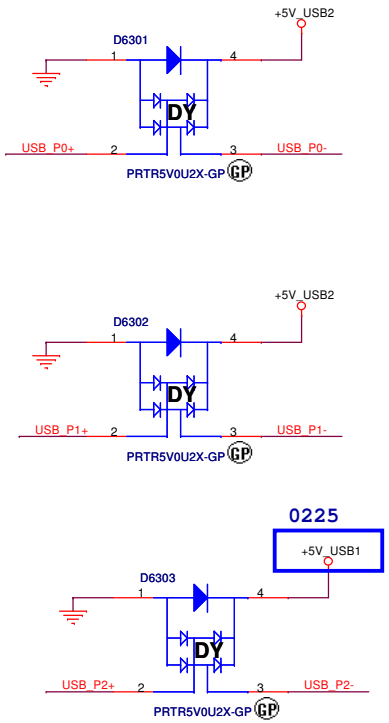
USB Power

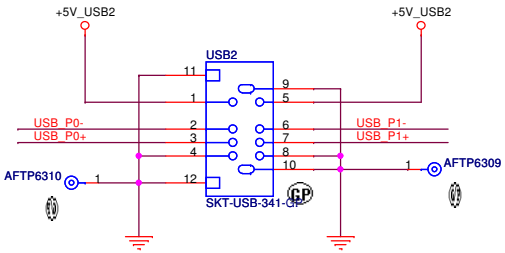


Right USB Power

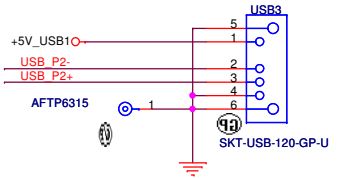




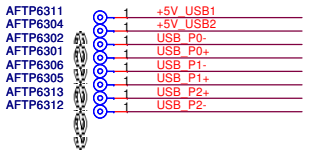




22.10254.501



22.10218.K71



<Core Design>

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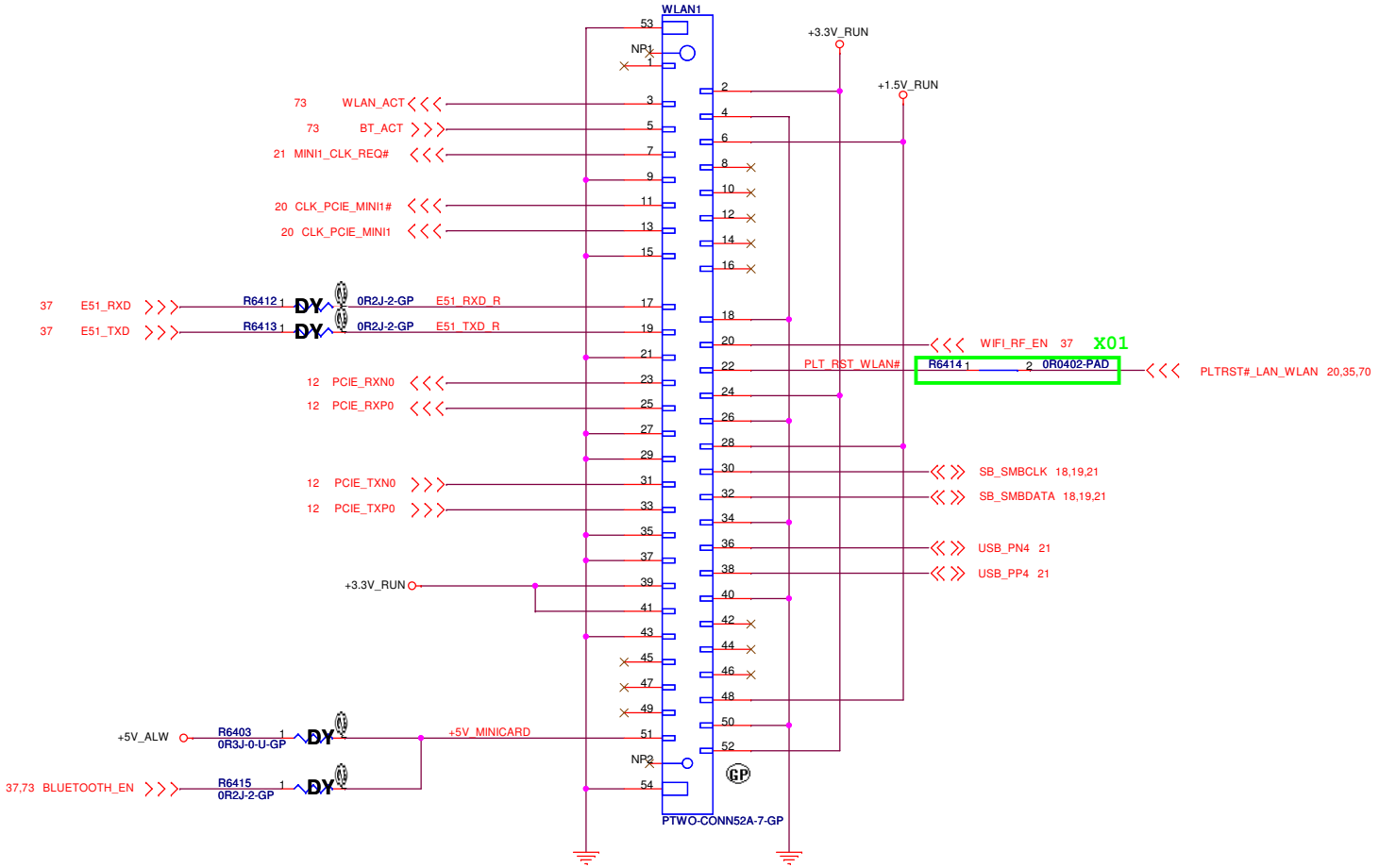
Title: USB

Size | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

Date: Friday, May 14, 2010 | Sheet 63 of 90

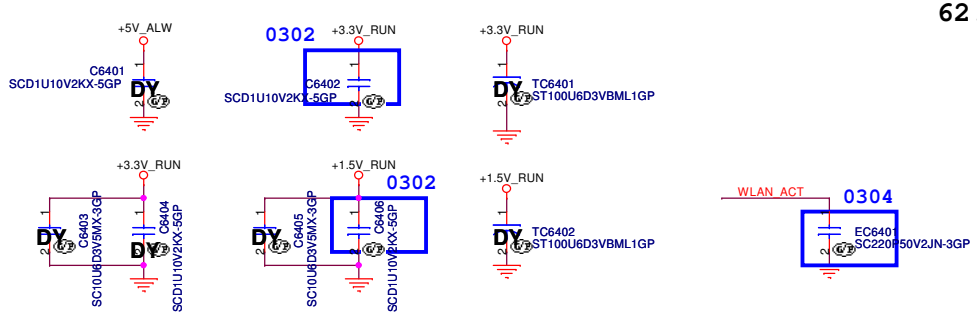
SSID = Wireless

Mini Card Connector(802.11a/b/g)



20.F1516.052

62.10043.771



<Variant Name>

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Title	MINICARD	
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: A00
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<Core Design>

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Title

Reserved

Size	Document Number	Rev
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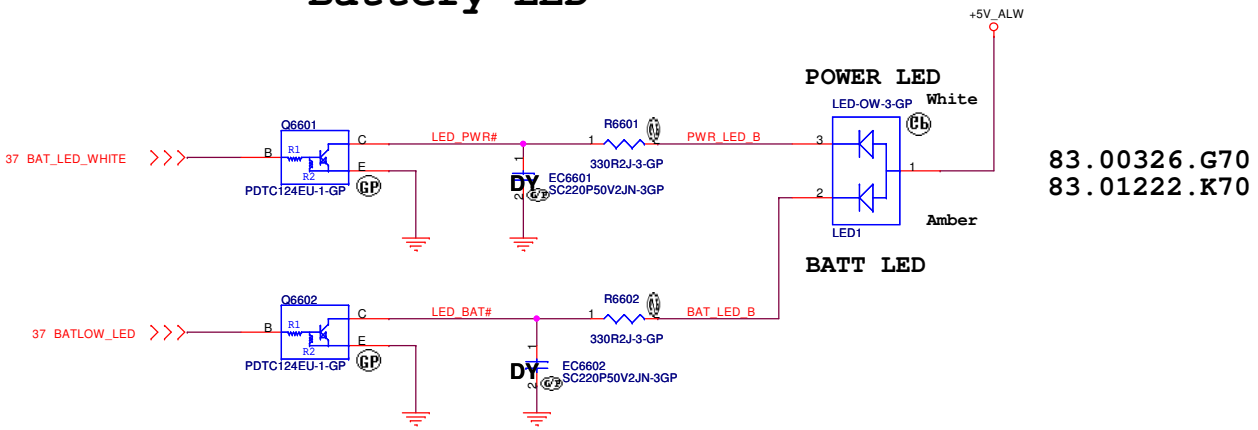
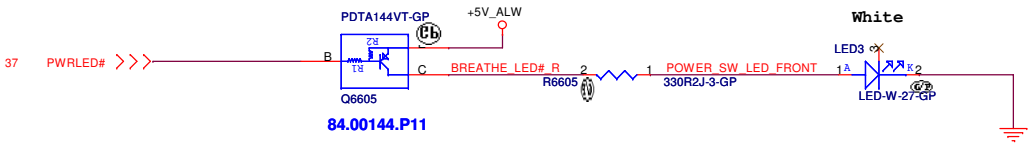
SSID = User.Interface

Battery LED



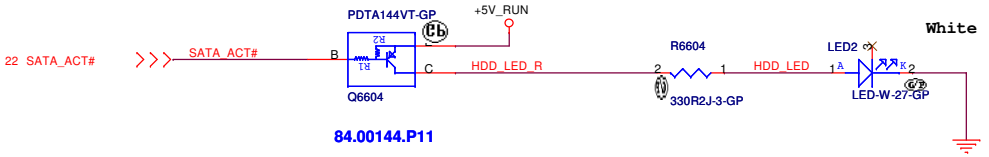
83.00326.G70
83.01222.K70

BREATHE PWR LED (Front)

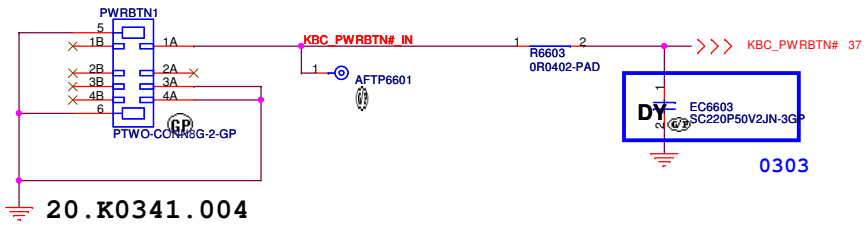


84.00144.P11

HDD LED



84.00144.P11



20.K0341.004

Main DJ1 AMD UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title	LED/PWRBTN	
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<Core Design>

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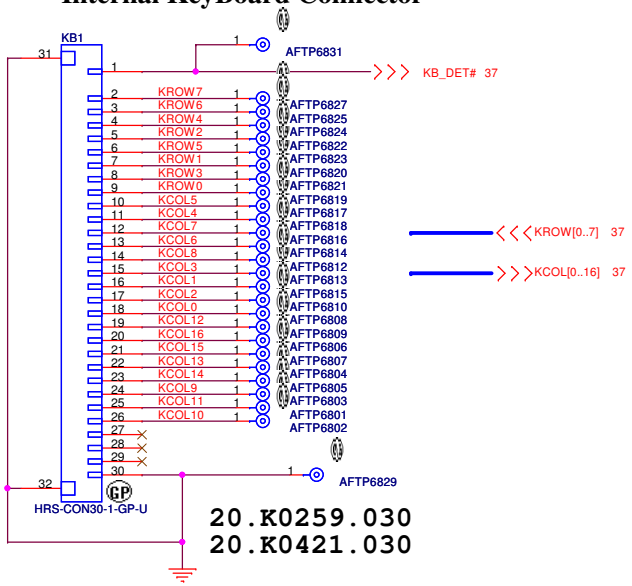
Title

Reserved

Size	Document Number	Rev
A3	*Chelsea DJ2 AMD UMA*	*A00*

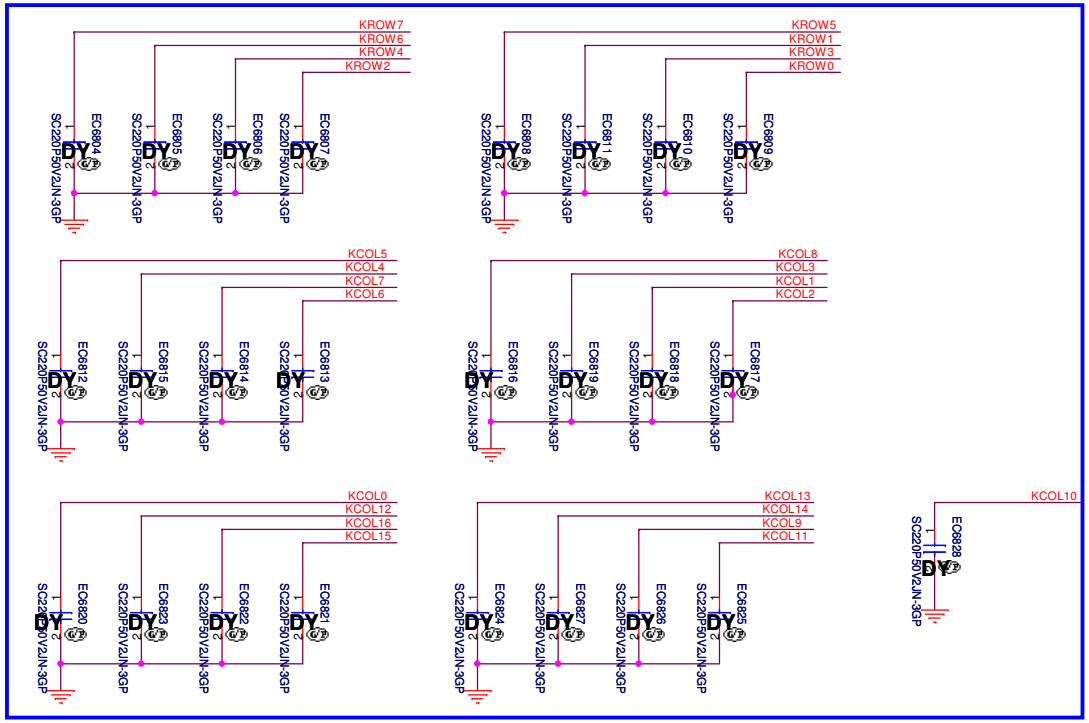
SSID = KBC

Internal KeyBoard Connector



20.K0259.030
20.K0421.030

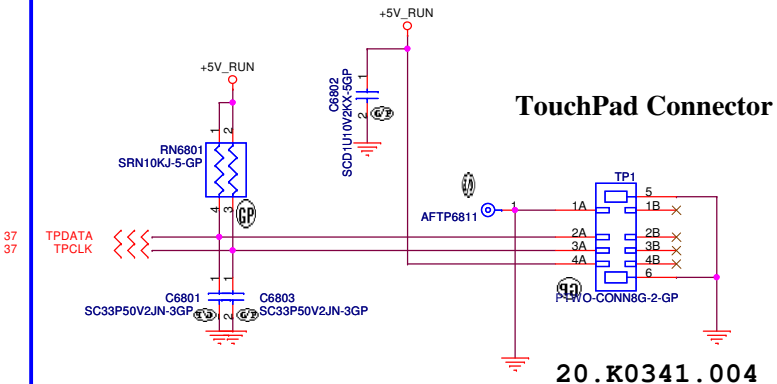
0304



SSID = Touch.Pad

0302

TouchPad Connector



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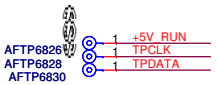
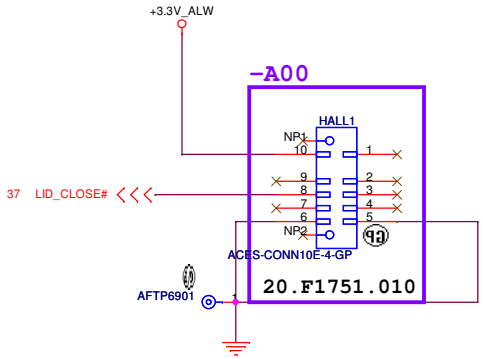


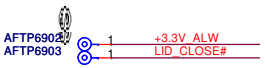
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Key Board/Touch Pad	
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: A00
Date: Friday, May 14, 2010	Sheet 68 of 90	

SSID = User. Interface





-A00

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Hall Sensor

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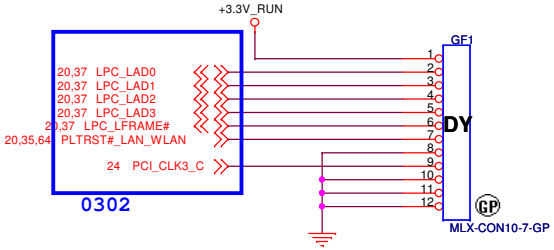

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	***Chelsea DJ2 AMD UMA***	***A00***

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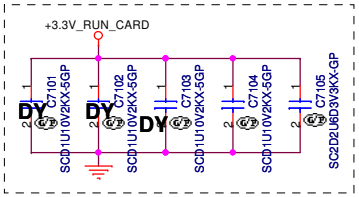
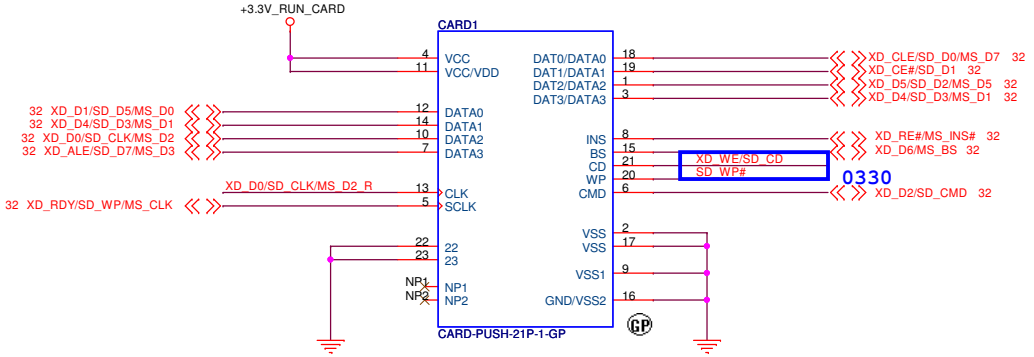
SSID = SDIO

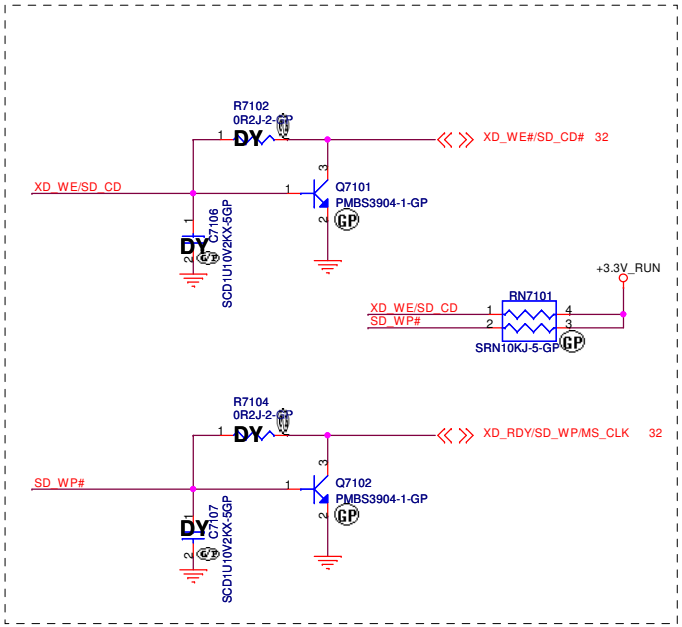
SD/XD/MS Card Reader





20.I0110.011

For reverse card connector 0330



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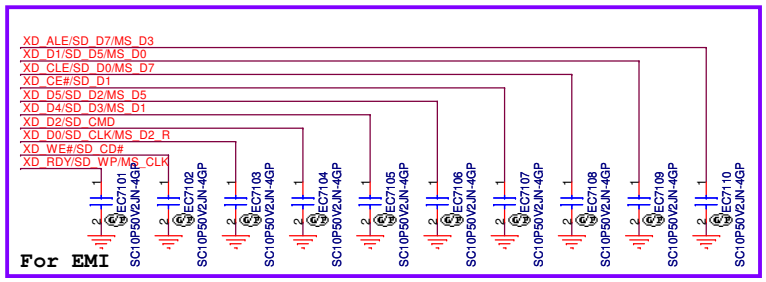
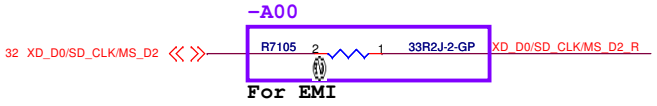


-A00



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader Connector

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size	Document Number	Rev
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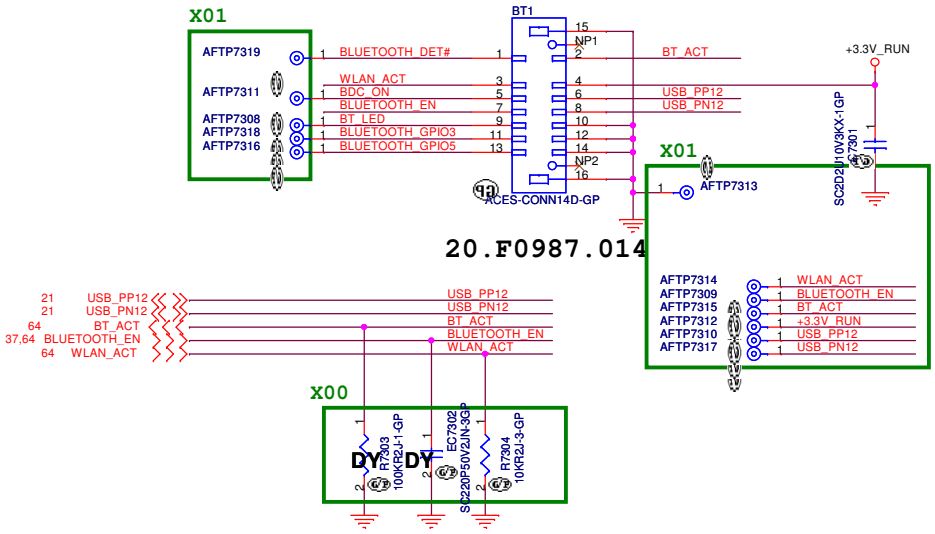
SSID = User.Interface

Bluetooth Module conn.



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Title: Bluetooth		
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Title

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Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *A00*

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Title: IO Board Connector

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Title: *Reserved*

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Title

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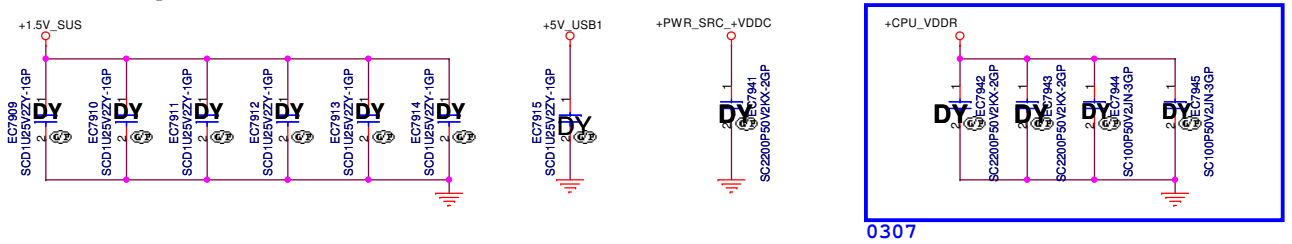
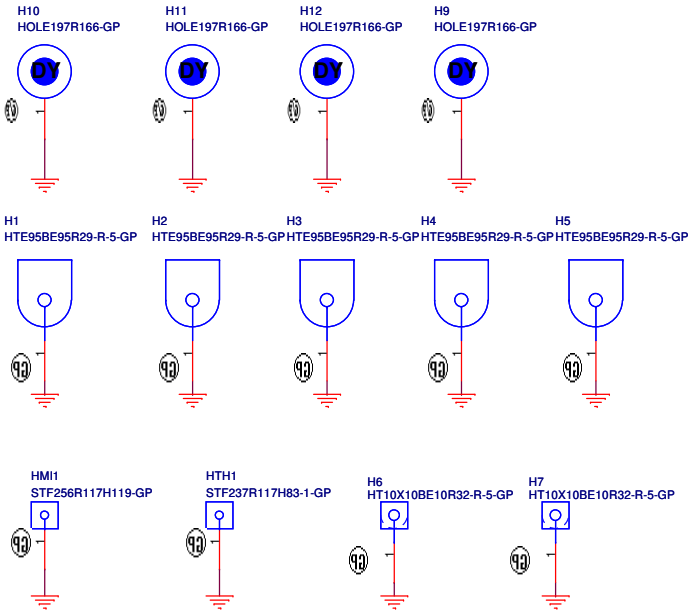
SSID = Mechanical

EMI Request





Main DJ1 AMD UMA

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Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
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Title: VGA PCIE(1/4)

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Title: VGA LVDS/TV/CRT(2/4)

Size: A3 | Document Number: Chelsea DJ2 AMD UMA | Rev: A00

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Title
VGA POWER/GND(3/4)

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	A00

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Title
VGA MEMORY/STRAPS(4/4)

Size	Document Number	Rev
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Title: GPU-VRAM (1/2)

Size	Document Number	Rev
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Title

GPU-VRAM (2/2)

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Title
TPS51117_+VCC_GFXCORE

Size	Document Number	Rev
A3	*Chelsea DJ2 AMD UMA*	*A00*

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Title
APL5930_+1.1V_RUN

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Title: *Reserved*

Size: A3 | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *A00*

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Change notes – Page 1

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	37	pop R3729 , depop R3733	MB version	EE
		2	37	DY R3712	compare DJ1 and DJ2 (for battery)	EE
		3	71	add R7101~R7104; C7106~C7107; Q7101~Q7102	For reversal cardreader connector	EE
						EE
		5	70	depop GF1	non-pop debug port	EE
		6	42	C4203 from 100pF to 4.7nF	For sequence	EE
		7	61	reserve U6103, U5104, U6105	For LAN Surge	EE
		8	47	PR4720 change to 95.3Kohm(64.95325.6DL). PR4721 change to 22Kohm(64.22025.6DL).	For CPU_CORE OCP	EE
		9	20	RN2006 from 0R to 10R	For CLK_LAN slew rate fail	EE
		10	55	C5508~C5510 from 8.2pF to 10pF L5501~L5503 change to 33 ohm bead	For EMI request	EMI
		11	79	add SPR3 and SPR4	For EMI request	EMI
		12	63 21	add C6307~C6312 ; C2106~C2107 4.7pF	Fine tune USB signal	EE
	A00	1	22	add R2131 pull high +3.3V_ALW	no internal pull-high	EE
		2	37	add R3717 pull down	to select DJ2 KBC code	EE
		3	38	Paste R3730, Dumm R3734	MB version	EE
		4	49	PR4905 PWR change from +3.3V_ALW to +3.3V_RUN	PWR saving	EE
		5	39	Dummy D3901 paste R3915	For Fan	EE
		6	30	AMP_MUTE# reconnect	For Audio anti-pop	EE
		7	69	HALL1 change to 20.F1751.010	connector change	ME
		8	54	paste PC4504	PWR team request	PWR
		9	24	Dummy ER2401		EE
		10		Short PAD R1329,R2304,R3023,R3024,R3025,R3026,R3027 R3031,R6001,R6002,R6005,R6006		EE
		11		Short PAD R2303,R3732,R3751,R3757,R3906,R6203,R6205		EE

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Title: *Change History*

Size: Custom | Document Number: *Chelsea DJ2 AMD UMA* | Rev: *A00*

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Change notes – Page 2

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
		12		Delete R6303,R6304,R6305,R6306,R6307,R6308 Add TR6303,TR6304,TR6305	EMC Solution	EMC
		13		Add EC7101,EC7102,EC7103,EC7104,EC7105,EC7106, EC7107,EC7108,EC7109,EC7110,R7105	EMC Solution	EMC
		14		ShortPAD PR4529 PR4617 PR4618 PR4620 PR4706 PR4709 PR4712 PR4719 PR4729 PR4730 PR4903 PR4910 PR5016	cost saving	PWR
		15	61	change XF6101 to 68.HD091.30A	EMC Solution	EMC
		16	30	POP C3002,C3012,C3020,C3024	Vendor suggest	EE
		17	55,73	Add EC5501,EC6301,EC6302	EMC Solution	EMC
		18	21	Add C2108,C2109 change R2129,R2130 33 ohm	SMBUS	EE
		19	62	change RTC1 P/N to 62.70001.061	conn change	ME
		20	79	Delete SPR3,SPR4	EMC Solution	EMC
		21	69	Delete HALL2,R6901,R6902,C6903	Use HALL1	EE
		22	47	change PR4707 to 64.82515.6DL	Tune VDDNB OCP setting	PWR
		23	47	POP PTC4706	Tune alchostic noise	EE

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