Arsenal Discrete Schematics Document

AMD Danube CPU S1G4

VGA ATI PARKS3-LP

RS880M + SB820M

2010-05-07

REV : X01

DY : Nopop Component

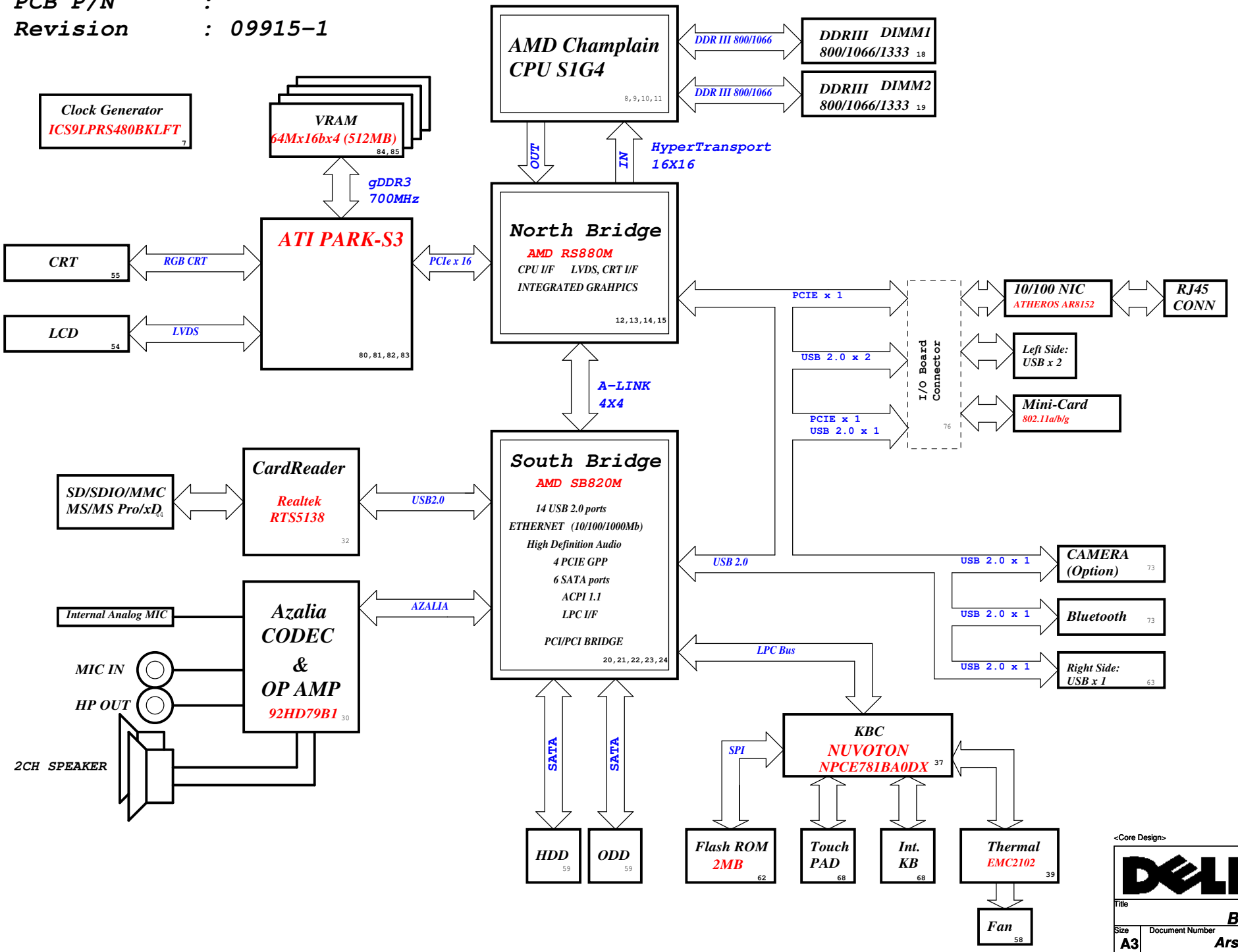
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Cover Page	
Size: Custom	Document Number: Arsenal DJ1 Discrete	Rev: X01
Date: Friday, May 07, 2010	Sheet 1 of 89	

Project code :
PCB P/N :
Revision : 09915-1

Arsenal DJ1 Discrete Block Diagram



CHARGER BQ24745RHDR	
INPUTS	OUTPUTS
+DC_IN_SS +CHAGER_SRC	+PWR_SRC

SYSTEM DC/DC TPS51125RGER-GP 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC RT8209EGQW 48	
INPUTS	OUTPUTS
+PWR_SRC	+1.1V_ALW

CPU CORE ISL6265AHRTZ-T-GP 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE +VDDNB

DDR III SUS&VTT TPS51116RGER-GP-U 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS

SYSTEM DC/DC APL5930KAI 52	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN +1.8V_DELAY

SYSTEM DC/DC Swithes 53	
INPUTS	OUTPUTS
+3.3V_ALW	+3.3V_RUN
+5V_ALW	+5V_RUN
+1.5V_SUS	+1.5V_RUN
+1.1V_ALW	+1.1V_RUN

VGA RT8208AGQW 86	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

PCB LAYER
L1: Top
L2: GND
L3: Signal
L4: Signal
L5: VCC
L6: Signal
L7: GND
L8: Bottom

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

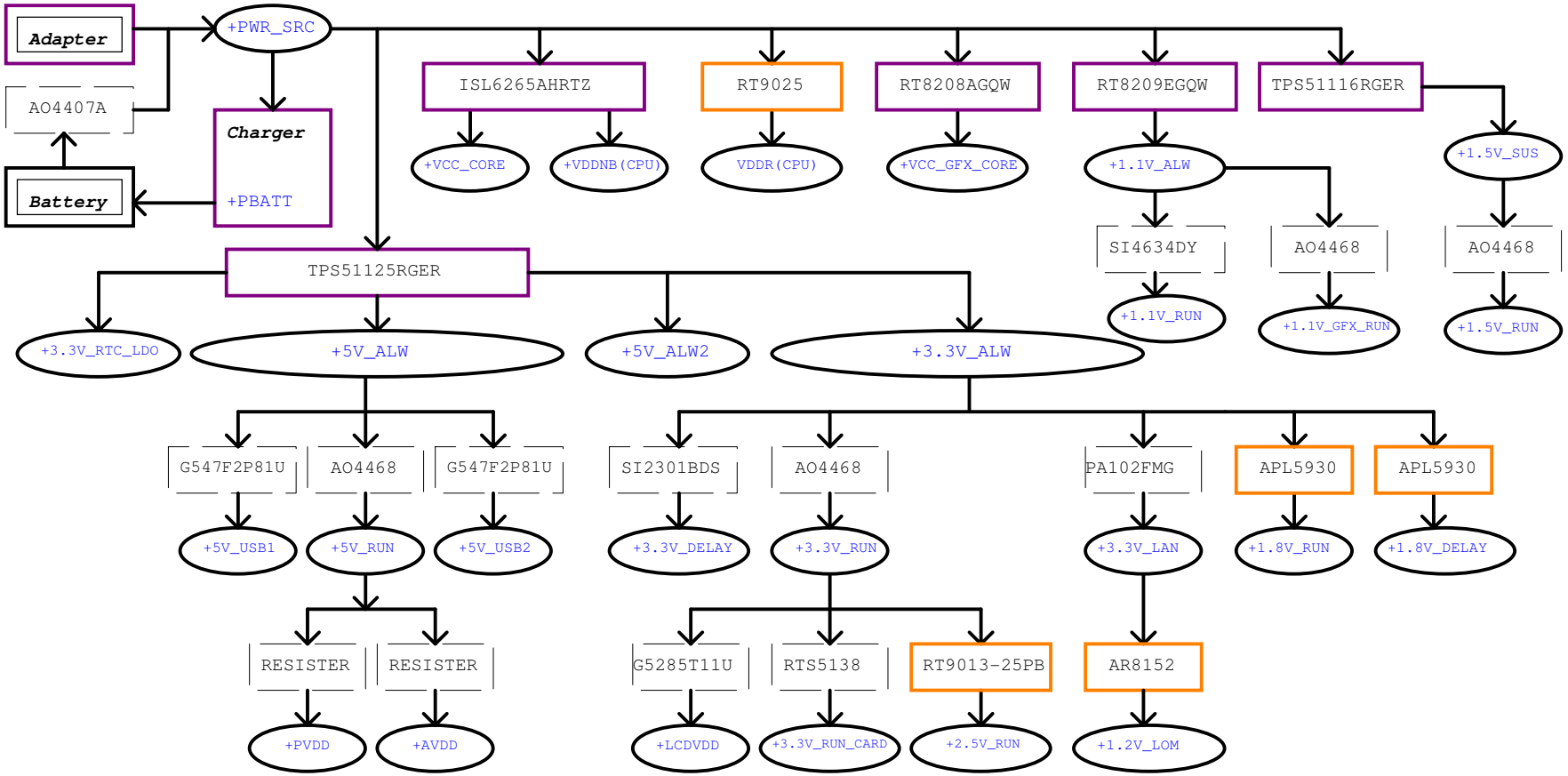
Size	Document Number	Rev
A3	Arsenal DJ1 Discrete	X01

Date: Friday, May 07, 2010 Sheet 2 of 89

Power Block Diagram

Power Shape

Regulator | LDO | Switch

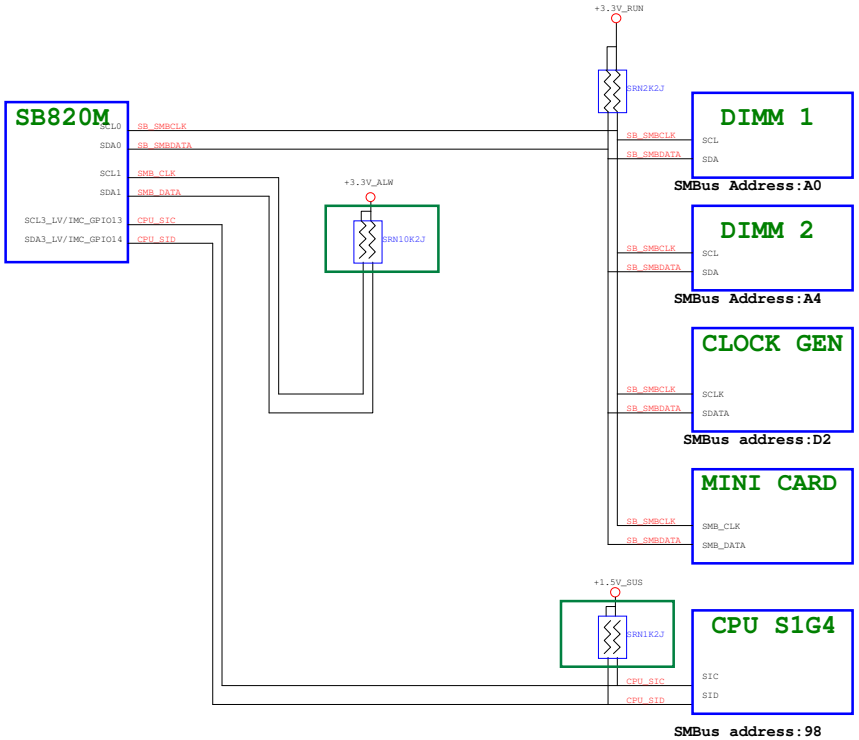


<Core Design>

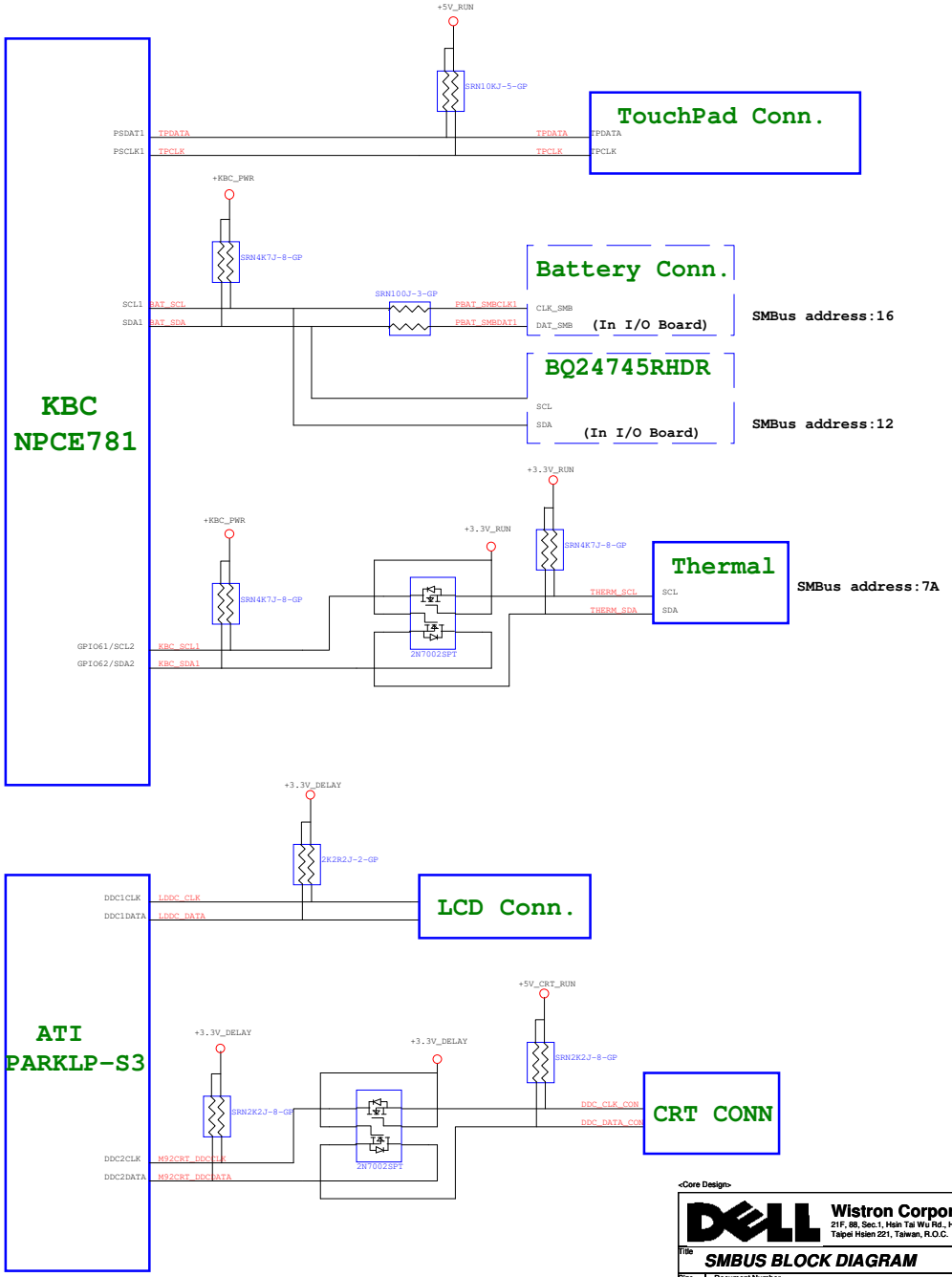
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Power Block Diagram	
Size: Custom	Document Number: Arsenal DJ1 Discrete	Rev: X01
Date: Friday, May 07, 2010	Sheet 3 of 89	

SB820M SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>

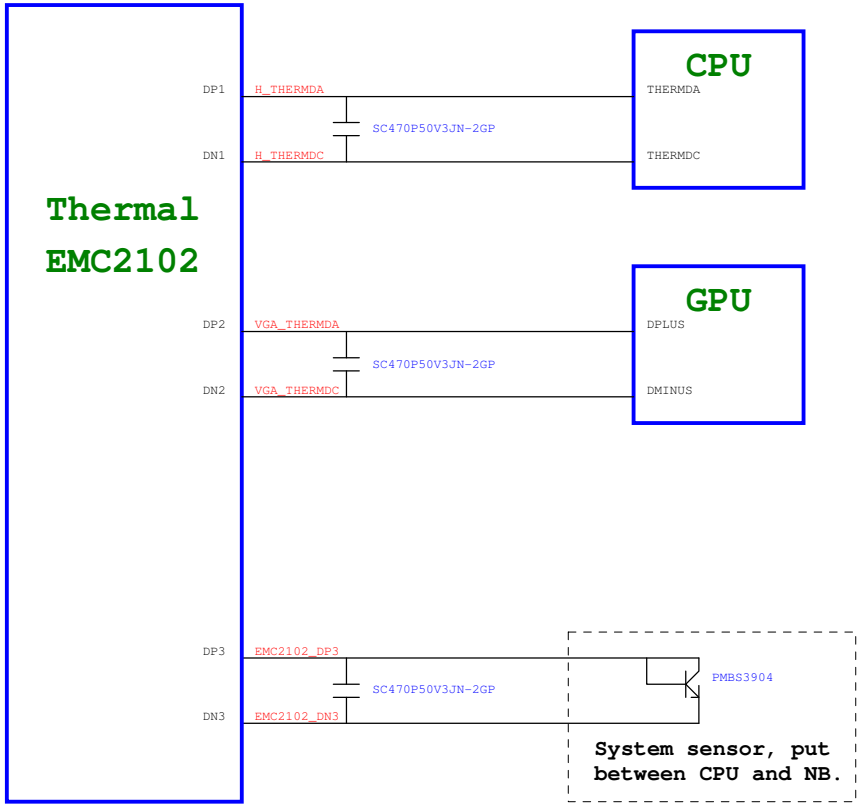
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS BLOCK DIAGRAM

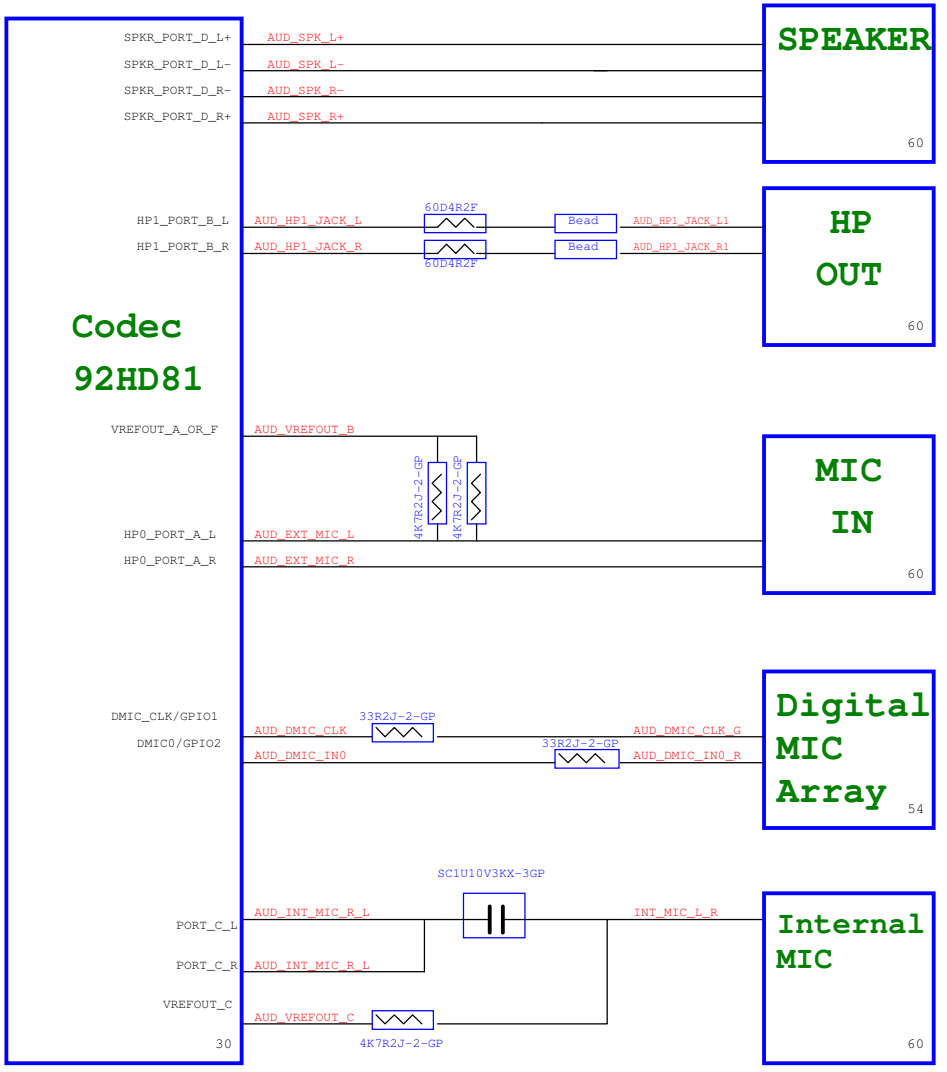
Size	Document Number	Rev
A2	Arsenal DJ1 Discrete	X01

Date: Friday, May 07, 2010 Sheet 4 of 89

Thermal Block Diagram



Audio Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	THERMAL/AUDIO BLOCK DIAGRAM	
Size: Custom	Document Number: Arsenal DJ1 Discrete	Rev: X01
Date: Friday, May 07, 2010	Sheet 5 of 89	

SB820M Strapping

Capture from 45484 Rev. 1.02 AMD SB8xx-Series Southbridge Design Guide

Name	Strap Name	Schematic Note
LPCCLK0	ECEnableStrap	**Embedded Controller (EC)** ★ 0 V - Disabled 3.3 V - Enabled
EC_PWM3 EC_PWM2	{ROMTYPE_1, ROMTYPE_0 }	ROMTYPE_1 / ROMTYPE_0 / ROM TYPE 3.3V / 0V / SPI ROM 3.3V / 3.3V / Reserved 0V / 0V / Firmware Hub ★ 0V / 3.3V / LPC ROM (supports both LPC and PMC ROM types)
LPCCLK1	CLKGEN	**Defines clock generator** ★ 0V – External clock mode: Use 100-MHz PCIeR clock as reference clock and generate i nternal clocks only. 3.3V– Integrated clock mode: Use 25-MHz crystal clock and generate both internal and external clocks
PCICLK1	BIF_GEN2_ COMPLIANCE_Strap	**Set PCIe to Gen II mode** 0V– Force PCIe interface at Gen I mode ★ 3.3V– PCIe interfacce is at Gen II mode Not Applicable to SB820M but provision for pull-down is required.
PCICLK2	BootFailTmrEn	**Watchdog function** ★ 0V– Disable the boot fail timer function 3.3V– Enable the boot fail timer function
PCICLK3	DefaultStrapMode	**Default Debug Straps** ★ 0V– Disable Debug Straps. 3.3V– Select external Debug Straps
PCICLK4	CPUClkSel	**CPU/NB HT Clock Selection** 0V– Reserved. ★ 3.3V– Required setting for integrated clock mode. This strap is not used if the strap CLKGEN is configured for external clock generator mode.
AZ_SDOUT	CoreSpeedMode	**Slow down core clock for low power platform.** ★ 0V– Performance mode 3.3V– Low Power mode

NB880M Strapping

Capture from 46113_rs880m_ds_nda_1.03

Name	Strap Function	Schematic Note
DAC_VSYNC	STRAP_DEBUG_BUS_GPIO _ENABLE#	Enables debug bus access through memory I/O pads and GPIOs. 0: Enable ★ 1: Disable
DAC_HSYNC	SIDE_PORT_EN#	Indicates if memory side-port is available or not ★ 0: Available 1: Not available
SUS_STAT#	LOAD_EEPROM_STRAPS#	Selects loading of strap values from EEPROM. 0: I2C master can load strap values from EEPROM if connected, or use default values if EEPROM is not connected. Please refer to RS880M's reference schematics for system level implementation details. ★ 1: Use default values

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
V 256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO_VGA_00	Tansmitter Power Savings Enable V 0= 50% Tx output swing 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO_VGA_01	Transmitter De-emphasis Enable V 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO_VGA_02	V 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type V if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] V 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI
VGA_DIS (Internal PD)	GPIO_VGA_09	V 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller

USB Table

USB	
Pair	Device
0	USB2
1	USB3
2	USB0 (I/O Board)
3	USB1 (I/O Board, 17")
4	WLAN
5	Reserve
6	Reserve
7	Reserve
8	Reserve
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	Reserve
13	Reserve

PCIE SB820M

	PCI-E Port	Device	Remark
Device 21	PCI-E Port #0	Onboard LAN	ATHEROS AR8132
	PCI-E Port #1	Mini Card	WLAN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content

Size: A2 | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 6 of 89

1'nd 68.00084.A31(MURATA)
2'nd

+3.3V_CLK_VDD (40 mils)

+3.3V_RUN R702 +3.3V_CLK_VDD
0R3J-0-U-GP
SC10U6D3V5KX-1GP
SCD1U10V2KX-4GP C701 C703 C704 C705 C706 C707 C708 C709

+3.3V_RUN R703 +3.3V_CLK_VDDIO
0R3J-0-U-GP
SC10U6D3V5KX-1GP
SC22U6D3V9KX-GP DY C710
SCD1U10V2KX-4GP C711 C712 C713 C714 C715 C716 C717

+3.3V_RUN R701 +3.3V_CLK_VDDREF
0R3J-0-U-GP
SC22U6D3V9KX-GP C720
SCD1U10V2KX-4GP C721

+3.3V_RUN R705 10KR2J-3-GP
R706 DY 0R2J-2-GP
EC702 SC10P50V2JN-4GP
21,41 SB_PWRGD

+3.3V_CLK_VDD +3.3V_CLK_VDDIO +3.3V_CLK_VDDREF

0507

U701
ICS9LPRS480BKLFT-GP

26	VDDATIG	X1	61 CLKGEN_X1
25	VDDATIG_IO	X2	62 CLKGEN_X2
48	VDDCPU	SMBCLK	2 SB_SMBCLK 18,19,21,76
47	VDDCPU_IO	SMBDAT	3 SB_SMBDATA 18,19,21,76
16	VDDSRC	ATIG0T_LPRS	30 GFX_CLKP
17	VDDSRC_IO	ATIG0C_LPRS	29 GFX_CLKN
11	VDDSRC_IO	ATIG1T_LPRS	28 NB_GFX_CLK_R
35	VDDSB_SRC	ATIG1C_LPRS	27 NB_GFX_CLK_R#
34	VDDSB_SRC_IO	CLKREQ0#	23 TP_CLKREQ0#
40	VDDSATA	CLKREQ1#	45 MINI1_CLK_REQ# 76
4	VDD	CLKREQ2#	44 TP_CLKREQ2#
55	VDDHTT	CLKREQ3#	39 TP_CLKREQ3#
56	VDDREF	CLKREQ4#	38 TP_CLKREQ4#
63	VDD48	CPUKG0T_LPRS	50 CPU_HT_CLK
51	PD#	CPUKG0C_LPRS	49 CPU_HT_CLK#
		48MHZ_0	64 48M_CLK
		REF0/SEL_HTT66	59 FS0
		REF1/SEL_SATA	58 FS1
		REF2/SEL_27	57 FS2
22	SRC0T_LPRS	GNDSATA	43
21	SRC0C_LPRS	GNDATIG	24
20	SRC1T_LPRS	GND	7
19	SRC1C_LPRS	GNDHTT	52
15	SRC2T_LPRS	GNDREF	60
14	SRC2C_LPRS	GNDCPU	46
13	SRC3T_LPRS	GND48	1
12	SRC3C_LPRS	GNDSRC	10
9	SRC4T_LPRS	GNDSRC	18
8	SRC4C_LPRS	GNDSB_SRC	33
42	SRC6T/SATAT_LPRS	GND	65
41	SRC6C/SATAC_LPRS		
6	SRC7T_LPRS/27MHZ_SS		
5	SRC7C_LPRS/27MHZ_NSS		
37	SB_SRC0T_LPRS		
36	SB_SRC0C_LPRS		
32	SB_SRC1T_LPRS		
31	SB_SRC1C_LPRS		
54	HTT0T_LPRS/66M		
53	HTT0C_LPRS/66M		

1ST 71.08628.003
71.09480.A03

XTAL
1'nd 82.30005.901
2'nd 82.30005.A51

0423
X701 X-14D318T8M-37GP
C718 SC12P50V2JN-3GP
C719 SC12P50V2JN-3GP

CLKREQ# MAP

CLKREQ0#	No use
CLKREQ1#	CLKSRC1 MINI1
CLKREQ2#	No use
CLKREQ3#	No use
CLKREQ4#	No use

VGA(100MHz)
RN709 SRN0J-6-GP
GFX_CLKP → CLK_PCIE_VGA 80
GFX_CLKN → CLK_PCIE_VGA# 80
RN710 SRN0J-6-GP
NB_GFX_CLK_R → NB_GFX_CLK 13
NB_GFX_CLK_R# → NB_GFX_CLK# 13
1002

MINI1_CLK_REQ# R707 10KR2J-3-GP +3.3V_RUN

CPU_CLK(200MHz)
RN708 SRN0J-6-GP
CPU_HT_CLK → CPU_CLK 10
CPU_HT_CLK# → CPU_CLK# 10

CardReader(48MHz)
SB820M_USB(48MHz)
48M_CLK R709 22R2J-2-GP R710 22R2J-2-GP
→ CLK_48M_CARD 32
→ USB_48M_CLK 21

DY EC706 SC4D7P50V2CN-1GP
DY EC707 SC4D7P50V2CN-1GP
For EMI

+3.3V_RUN
8K2R2J-3-GP R711
8K2R2J-3-GP R712
R715 158R2F-GP
R716 33R2J-2-GP
0824
NB_14M_CLK 13
SB_14M_CLK 21
NB OSCIN(14MHz)
SB OSCIN(14MHz)

9D09R2F-1-GP R718
8K2R2J-3-GP DY R717

Place together

WLAN(100MHz)
76 CLK_PCIE_MINI1
76 CLK_PCIE_MINI1#
RN702 SRN0J-6-GP
CLK_MINI1_R
CLK_MINI1#_R

LAN(100MHz)
76 CLK_PCIE_LAN
76 CLK_PCIE_LAN#
RN703 SRN0J-6-GP
LAN_CLK_R
LAN_CLK#_R

X01
VGA(27MHz)
81 CLK_VGA_27M_SS
81 CLK_VGA_27M_NSS
R713 47R2J-2-GP
R714 33R2J-2-GP
R_VGA_27M_SS_CLK
R_VGA_27M_NSS_CLK

13 NB_GPPSB_CLK
13 NB_GPPSB_CLK#
RN704 SRN0J-6-GP
NB_GPPSB_CLK_R
NB_GPPSB_CLK#_R

20 SB_PCIE_CLK
20 SB_PCIE_CLK#
RN705 SRN0J-6-GP
SB_PCIE_CLK_R
SB_PCIE_CLK#_R

13 CLK_NBHT_CLK
13 CLK_NBHT_CLK#
RN706 SRN0J-6-GP
CLK_NBHT_CLK_R
CLK_NBHT_CLK#_R

TP_CLK_SRC4
TP_CLK_SRC4#
TP_CLK_SRC6
TP_CLK_SRC6#

TP701 TP_CLK_SRC6
TP702 TP_CLK_SRC6#
TP703 TP_CLKREQ0#
TP704 TP_CLKREQ3#
TP705 TP_CLKREQ4#
TP706 TP_CLK_SRC4
TP707 TP_CLK_SRC4#
TP708 TP_CLKREQ2#
TP709 TP_CLK_SRC2
TP710 TP_CLK_SRC2#

0923
EMI
CLK_VGA_27M_SS
CLK_VGA_27M_NSS
EC704 SC4D7P50V2CN-1GP DY
EC705 SC4D7P50V2CN-1GP DY

NB ALINK (100MHz)
SB PCIE (100MHz)
VGA Park (27MHz)

SEL_HTT66 FS0	1	66 MHz 3.3V single ended HTT clock	
	0*	100 MHz differential HTT clock	
SEL_SATA FS1	1*	100 MHz non-spreading differential SRC clock	
	0	100 MHz spreading differential SRC clock	
SEL_27MHz FS2	1*	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6	
	0	100MHz differential spreading SRC clock	

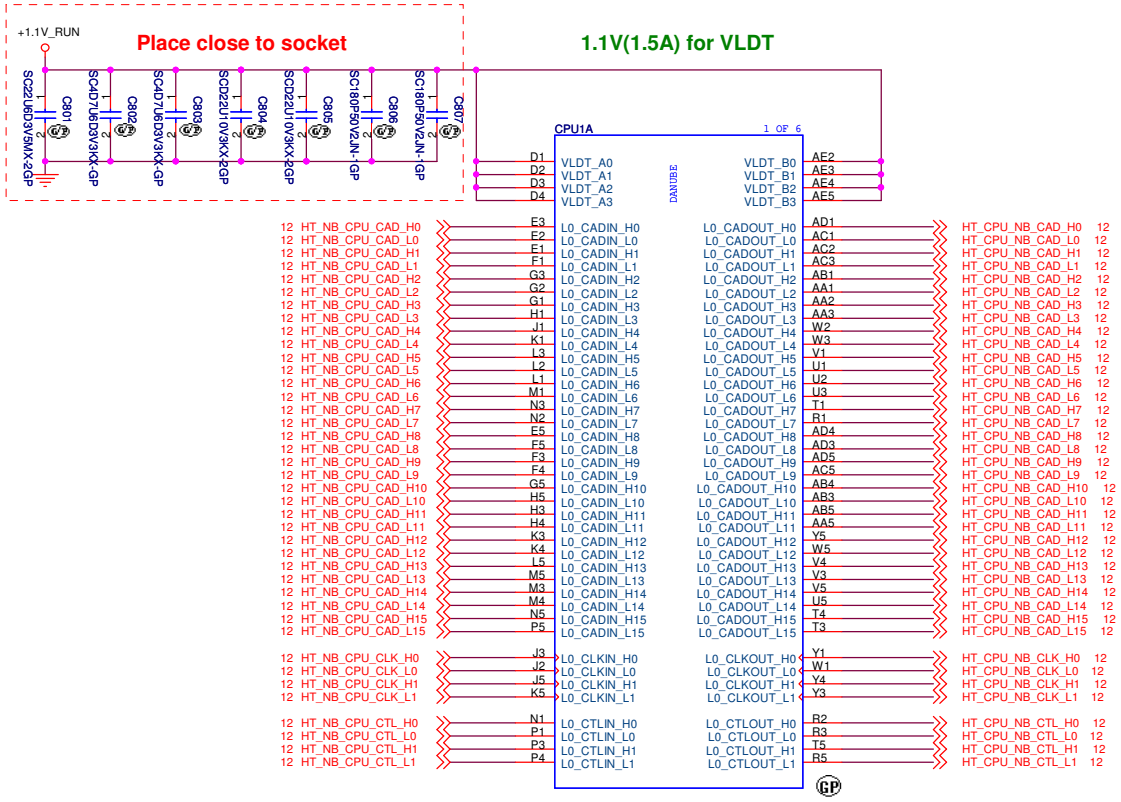
* default

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator ICS9LPRS480
Size: Custom | Document Number: Arsenal DJ1 Discrete | Rev: X01
Date: Friday, May 07, 2010 | Sheet 7 of 89

SSID = CPU



SKT-BGA638H176
1'nd 62.10055.111
2'nd 62.10055.171

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_HT_LINK I/F_(1/4)

Size: Custom | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 8 of 89

SSID = CPU

Place near to CPU

0.9V(1.25A) for VDDR

0.9V--DDR1066

1.05V---DDR1333 (1.75A)

From VDDR SEL

CLOSE TO CPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR_(2/4)

Size: Custom | Document Number: Arsenal DJ1 Discrete | Rev: X00

Date: Friday, May 07, 2010 | Sheet 9 of 89

SSID = CPU

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

2.5V(250mA) for VDDA

+2.5V_RUN +2.5V_RUN_VDDA L1001 PBY160808T-330Y-N-GP

CPU1D 4 OF 6 DANUBE

Cloce To CPU R1008 169R2F-GP

CPU_CLK(200MHz) 7 CPU_CLK 7 CPU_CLK# C1005 SC3900P50V2KX-2GP C1006 SC3900P50V2KX-2GP

CPUCLK_IN CPUCLK_IN# CLKIN_H CLKIN_L

CPU_R_LDT_RST# RESET# CPU_R_LDT_PWRGD PWROK CPU_R_LDT_STOP# LDTSTOP# CPU_LDT_REQ# LDTREQ#

For HDT DBG HDT_RST_R# R1009 0R2J-2-GP

Close CPU- SCD1U16V2ZY-2GP

CPU_SIC SID CPU_SID CPU_ALERT# ALERT#

+1.1V_RUN R1010 44D2R2F-GP R1011 44D2R2F-GP CPU_HTREF0 CPU_HTREF1 HT_REF0 HT_REF1

47 CPU_VDD0_RUN_FB_H 47 CPU_VDD0_RUN_FB_L VDD0_FB_H VDD0_FB_L

47 CPU_VDD1_RUN_FB_H 47 CPU_VDD1_RUN_FB_L VDD1_FB_H VDD1_FB_L

CPU_DBRDY CPU_TMS CPU_TCK CPU_TRST# CPU_TDI DBRDY TMS TCK TRST# TDI

CPU_TEST23 CPU_TEST18 CPU_TEST19 CPU_TEST25_H CPU_TEST25_L CPU_TEST21 CPU_TEST20 CPU_TEST24 CPU_TEST22 CPU_TEST12 CPU_TEST27 CPU_TEST9 TEST23 TEST18 TEST19 TEST25_H TEST25_L TEST21 TEST20 TEST24 TEST22 TEST12 TEST27 TEST9 TEST6

RSVD#A3 RSVD#A5 RSVD#B3 RSVD#B5 RSVD#C1

0423 +1.5V_SUS RN1006 SRN1KJ-7-GP

VSS RSVD#W18 SVC SVD CPU_SVC CPU_SVD

THERMTRIP# PROCHOT# MEMHOT# CPU_THERMTRIP# CPU_PROCHOT# CPU_MEMHOT# TP1002 S1G4 not support MEMHOT

CPU_PROCHOT# 20

THERMDC THERMDA H_THERMDC 39 H_THERMDA 39

VDDIO_FB_H VDDIO_FB_L TP_CPU_VDDIO_SUS_FB_H TP_CPU_VDDIO_SUS_FB_L

VDDNB_FB_H VDDNB_FB_L CPU_VDDNB_RUN_FB_H 47 CPU_VDDNB_RUN_FB_L 47

DBREQ# CPU_DBREQ# R1015 +1.5V_SUS TDO CPU_TDO 300R2J-4-GP

TEST28_H TEST28_L TEST17 TEST16 TEST15 TEST14 TP_CPU_TEST17 TP_CPU_TEST16 TP_CPU_TEST15 TP_CPU_TEST14

TEST7 TEST10 CPU_TEST10 R1021 300R3-GP +1.1V_RUN TEST8

TEST29_H TEST29_L CPU_TEST29H CPU_TEST29L R1024 80D6R2F-L-GP

RSVD#H18 RSVD#H19 RSVD#AA7 RSVD#D5 RSVD#C5

+1.5V_RUN X01 RN1001 SRN300J-3-GP

20 CPU_LDT_RST# R1001 0R0402-PAD CPU_R_LDT_RST#

20,42 CPU_LDT_PWRG R1002 0R0402-PAD CPU_R_LDT_PWRGD

13,20 CPU_LDT_STOP# R1003 0R0402-PAD CPU_R_LDT_STOP#

+1.5V_RUN R1012 DY 300R2J-4-GP CPU_LDT_REQ#

R1013 DY 300R2J-4-GP CPU_DBRDY

R1014 DY 300R2J-4-GP TP_CPU_TEST14

R1016 DY 300R2J-4-GP TP_CPU_TEST15

RN1002 SRN1KJ-7-GP CPU_TEST18 CPU_TEST19

RN1004 SRN1KJ-7-GP CPU_TEST24 CPU_TEST22

RN1003 SRN1KJ-7-GP CPU_TEST23 CPU_TEST12 CPU_TEST20 CPU_TEST21

0423

+1.5V_SUS to power IC FB

R1018 DY 510R2F-L-GP R1019 510R2F-L-GP

R1020 510R2F-L-GP DY R1022 510R2F-L-GP

R1023 CPU_TEST9 0R2J-2-GP

+1.5V_SUS R1026 1KR2J-1-GP CPU_TEST27 R1029 DY 300R2J-4-GP

TP1001 TP_CPU_VDDIO_SUS_FB_H TP1003 TP_CPU_VDDIO_SUS_FB_L TP1006 TP_CPU_TEST17 TP1007 TP_CPU_TEST16 TP1008 TP_CPU_TEST15 TP1009 TP_CPU_TEST14

+1.5V_SUS 0423 RN1005 SRN1KJ-7-GP R1032 2K2R2J-2-GP R1033 1KR2J-1-GP

21 CPU_SIC CPU_SIC

21 CPU_SID CPU_SID

21,39 TALERT# CPU_ALERT# Q1001 PMBS3904-1-GP

+KBC_PWR +1.5V_RUN X01 R1027 8K2R2J-3-GP R1028 2K2R2J-2-GP

21,37,39,42 H_THERMTRIP# CPU_THERMTRIP# Q1002 PMBS3904-1-GP

0423 For old HDT tool (3.3V level)

+3.3V_RUN +1.5V_RUN R1040 8K2R2J-3-GP R1039 2K2R2J-2-GP

37 CPU_PROCHOT#_EC Q1005 CPU_PROCHOT# PMBS3904-1-GP

+3.3V_RUN +1.8V_RUN R1037 10K2R2J-3-GP R1036 2K2R2J-2-GP

HDT_RST# Q1004 HDT_RST_R# PMBS3904-1-GP

+3.3V_RUN +1.8V_RUN R1034 10K2R2J-3-GP R1035 2K2R2J-2-GP

47 CPU_PWRGD_SVID_REG Q1003 CPU_R_LDT_PWRGD PMBS3904-1-GP

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

HDT Connectors

HDT1 SMC-CONN26A-FP

CPU_DBREQ# CPU_DBRDY CPU_TCK CPU_TMS CPU_TDI CPU_TRST# CPU_TDO

1.5V CPU_R_LDT_RST# R1038 0R2J-2-GP +1.5V_SUS

HDT_RST# 3.3V

<Core Design>

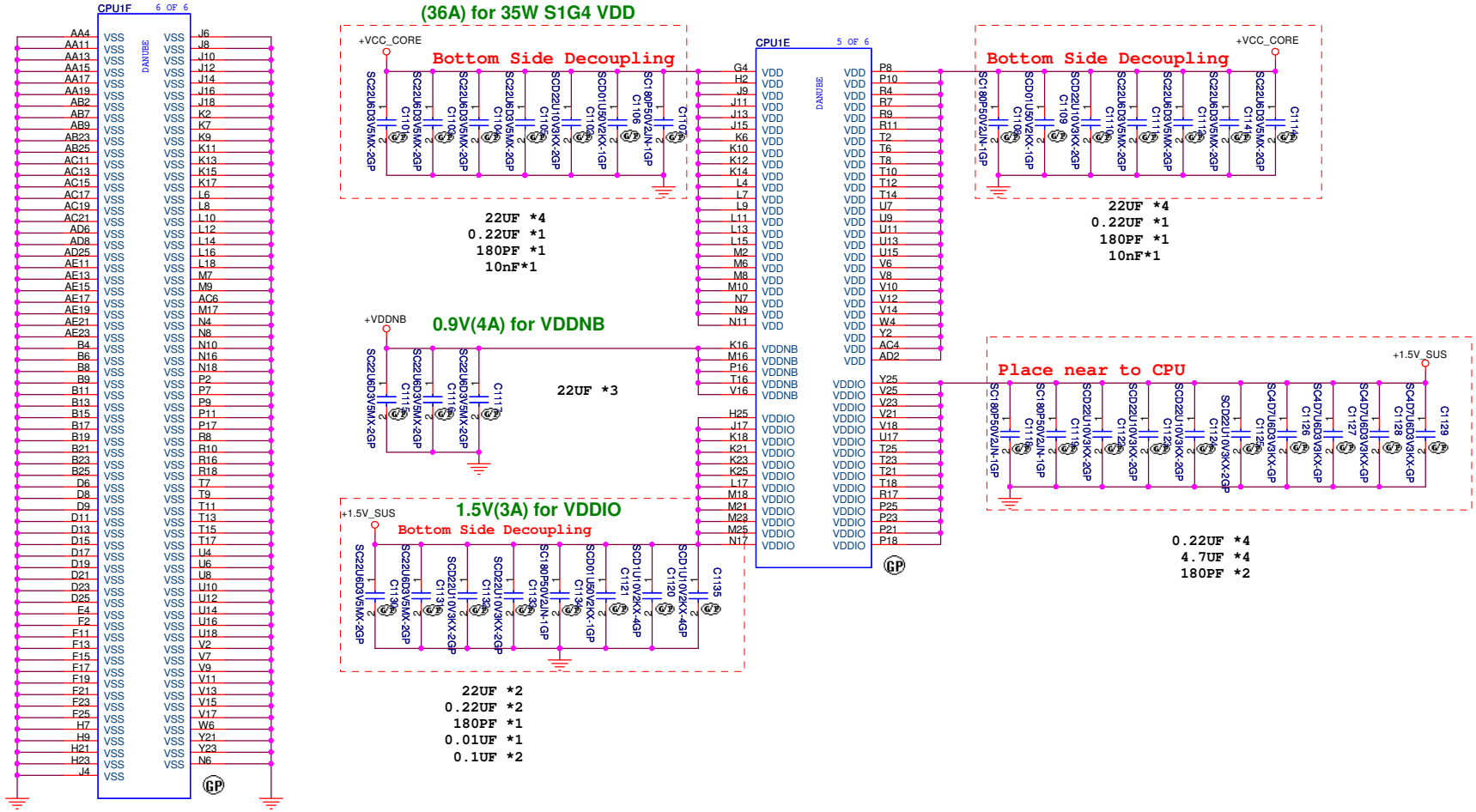
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)

Size: Custom | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 10 of 89

SSID = CPU



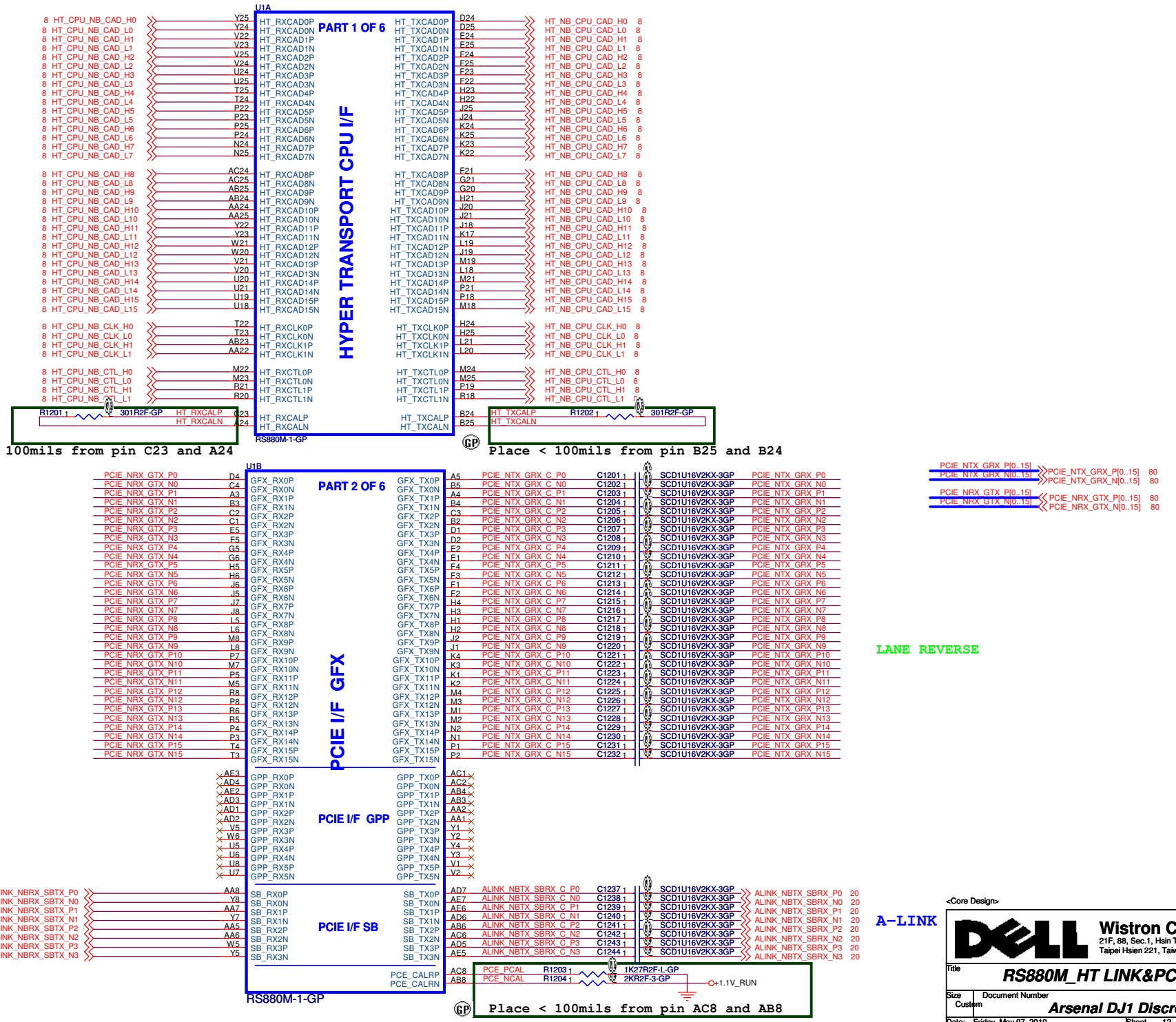
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU_Power_(4/4)*		
Size: A3	Document Number: *Arsenal DJ1 Discrete*	Rev: *X01*
Date: Friday, May 07, 2010	Sheet 11 of 89	

SSID = N.B

RS880M : 71.RS880.M05



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RS880M_HT LINK&PCIe(1/4)

Size: Custom | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 12 of 89

SSID = N.B

RS880M : 71.RS880.M05

Layout Note
Trace at least 15 mil

+1.8V_RUN
L1301 BLM15AG221SS1D-GP 220 ohm 300mA
20mA
+1.8V_VDDA18HTPLL
SC22U6D3V9KX-GP C1308
SCD1U10V2KX-4GP C1309
L1302 BLM15AG221SS1D-GP 220 ohm 300mA
120mA
+1.8V_VDDA18PCIEPLL
SC22U6D3V9KX-GP C1310
SCD1U10V2KX-4GP C1311
SC22U6D3V5MX-2GP C1312

UMA

GREEN/BLUE: Connected to GND through two separate 150- 1% resistors.

RED: Connected to GND through two separate 140- 1% resistors.

+3.3V_RUN
3KR2J-2-GP R1302
3KR2J-2-GP R1303
NB_VGA_VSYNC
NB_VGA_HSYNC
3KR2J-2-GP R1304 DY
3KR2J-2-GP R1305 DY

STRAP_DEBUG_BUS_GPIO_ENABLE# (RS880M use DAC_VSYNC)
Enables debug bus access through memory I/O pads and GPIOs.
*1 : Disable
0 : Enable

SIDE_PORT_EN# (RS880M use DAC_HSYNC)
*1 = Memory Side port Not available
0 = Memory Side port available

LOAD_EEPROM_STRAPS#(RS880M use SUS_STAT#)
Selects Loading of STRAPS From EEPROM
*1 : use Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

*DEFAULT

U1C
PART 3 OF 6
CRT/TVOUT
PLL PWR
LVTM
CLOCKs PM
MIS.

DIS
AVDD1 F12
AVDD2 E12
AVDDDI F14
AVSSDI G15
AVDDQ H15
AVSSQ H14

TV_OUT
C_Pr E17
Y E17
COMP_Pb F15

DIS
RED G18
REDb G17
GREEN E18
GREENb F18
BLUE E19
BLUEb F19

NB_VGA_HSYNC → DAC_HSYNC A11
NB_VGA_VSYNC → DAC_VSYNC B11
DAC_SCL F8
DAC_SDA E8

Trace at least 10 mil
DAC_RSET R1306 715R2F-GP → DAC_RSET G14

PLLVDD A12
PLLVDD18 D14
PLLVSS B12

+1.8V_VDDA18HTPLL → VDDA18HTPLL H17 20mA
+1.8V_VDDA18PCIEPLL → VDDA18PCIEPLL1 D7
VDDA18PCIEPLL2 E7 120mA

20,37 PLTRST#_NB_GPU → SYSRESET# D8
41 NB_PWRGD_IN → POWERGOOD A10
NB_LDT_STOP# → LDTSTOP# C10
NB_ALLOW_LDTSTOP → ALLOW_LDTSTOP C12

+1.1V_RUN
R1312 4K7R2F-GP
R1313 4K7R2F-GP

7 CLK_NBHT_CLK → HT_REFCLKP C25
7 CLK_NBHT_CLK# → HT_REFCLKN C24
NB_REFCLK_N
7 NB_14M_CLK → REFCLK_P/OSCIN E11
REFCLK_N F11

7 NB_GFX_CLK → GFX_REFCLKP T2
7 NB_GFX_CLK# → GFX_REFCLKN T1
TP1307 TP1308
NB_GPP_CLK → GPP_REFCLKP U1
NB_GPP_CLK# → GPP_REFCLKN U2

7 NB_GPPSB_CLK → GPPSB_REFCLKP V4
7 NB_GPPSB_CLK# → GPPSB_REFCLKN V3

I2C_CLK B9
I2C_DATA A9
DDC_DATA0/AUX0N B8
DDC_CLK0/AUX0P A8
DDC_CLK1/AUX1P B7
DDC_DATA1/AUX1N A7

TP1301 TP_NB_DDC_DATA0
TP1302 TP_NB_DDC_CLK0
TP1303 TP_NB_DDC_CLK1
TP1304 TP_NB_DDC_DATA1

STRP_DATA B10
TP1305 TP_NB_RESERVED
RESERVED G11
R1319 RS780_AUX_CAL 150R2F-1-GP
AUX_CAL C8
R1318 2KR2J-1-GP

0423

RS880M-1-GP

TXOUT_L0P A22
TXOUT_L0N B22
TXOUT_L1P A21
TXOUT_L1N B21
TXOUT_L2P B20
TXOUT_L2N A20
TXOUT_L3P A19
TXOUT_L3N B19
TXOUT_U0P B18
TXOUT_U0N A18
TXOUT_U1P A17
TXOUT_U1N B17
TXOUT_U2P D20
TXOUT_U2N D21
TXOUT_U3P D18
TXOUT_U3N D19
TXCLK_LP B16
TXCLK_LN A16
TXCLK_UP D16
TXCLK_UN D17

VDDLTP18 A13
VSSLTP18 B13
VDDLT18_1 A15
VDDLT18_2 B15
VDDLT33_1 A14
VDDLT33_2 B14

VSSLT1 C14
VSSLT2 D15
VSSLT3 C16
VSSLT4 C18
VSSLT5 C20
VSSLT6 E20
VSSLT7 C22

LVDS_DIGON E9
LVDS_BLON F7
LVDS_ENA_BL G12

TMDS_HPD D9
HPD D10
SUS_STAT# D12
THERMALDIODE_P AE8
THERMALDIODE_N AD8
TESTMODE D13

+1.5V_RUN
R1309 300R2J-4-GP
R1322 DY 0R2J-GP
+1.8V_RUN
R1311 2K2R2J-2-GP
U1301 SN74LVC2G07DCKR-GP
10,20 CPU_LDT_STOP#
NB_LDT_STOP#
C1306 SCD1U10V2KX-4GP

+1.8V_RUN
R1315 1KR2J-1-GP
X01
20 ALLOW_LDTSTOP
R1316 0R0402-PAD
NB_ALLOW_LDTSTOP

ALLOW_LDTSTOP:
1 = LDTSTOP# can be asserted
0 = LDTSTOP# has to be de-asserted

+3.3V_RUN
R1314 4K7R2J-2-GP
NB_SUS_STAT#
R1321 6KR2J-2-GP DY

TMDS_HPD → TP1311 TP1306
HPD → R1317 0R2J-2-GP
NB_SUS_STAT# → SUS_STAT# 21

TESTMODE_NB
R1320 1K8R2F-GP

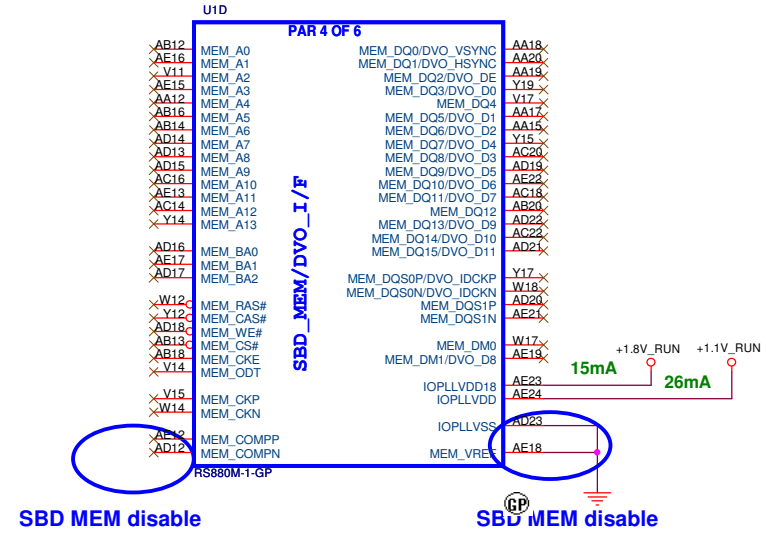
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RS880M_LVDS&CRT_(2/4)
Size: Custom
Document Number: Arsenal DJ1 Discrete
Rev: X01
Date: Friday, May 07, 2010
Sheet 13 of 89

SSID = N.B

RS880M : 71.RS880.M05



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

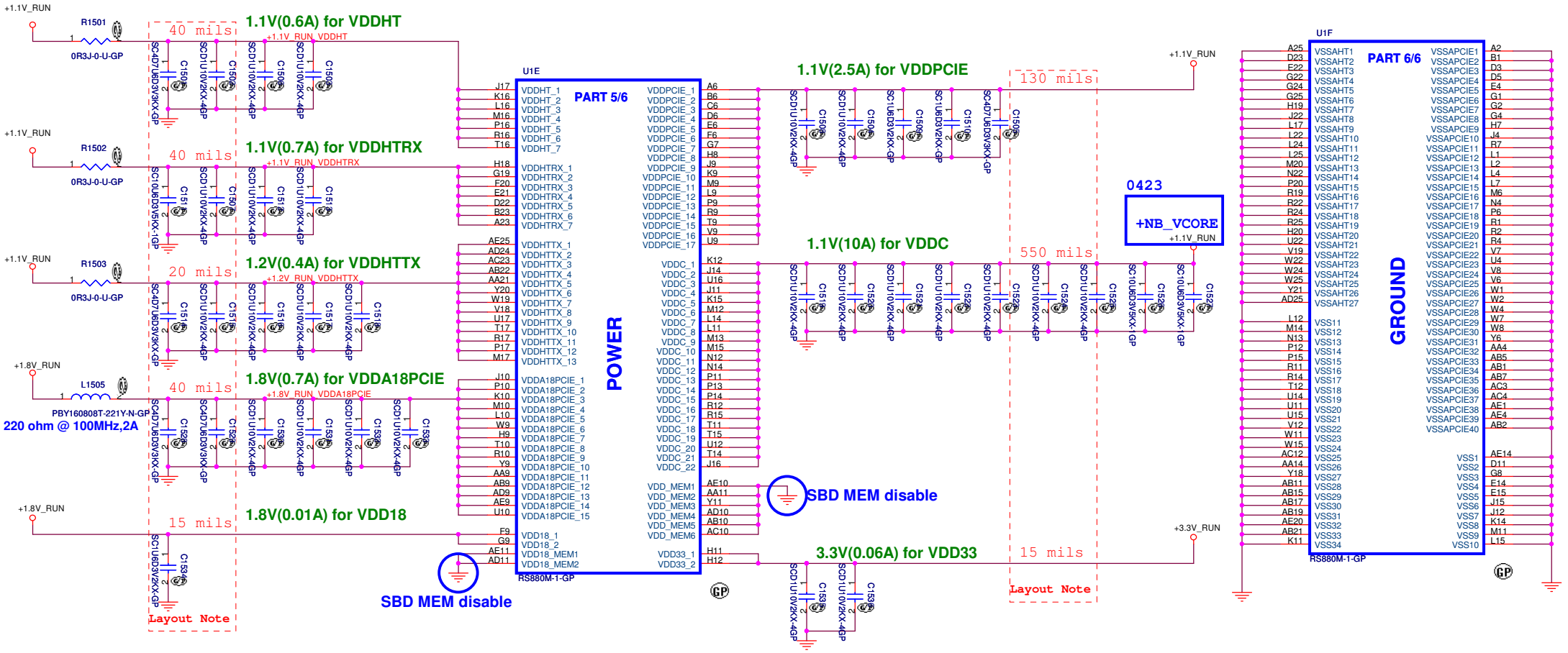
Title: ***RS880M_SidePort_(3/4)***

Size: A3 | Document Number: ***Arsenal DJ1 Discrete*** | Rev: ***X01***

Date: Friday, May 07, 2010 | Sheet 14 of 89

SSID = N.B

RS880M : 71.RS880.M05



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RS880M_PWR&GD_(4/4)	
Size: A3	Document Number: Arsenal DJ1 Discrete	Rev: X01
Date: Friday, May 07, 2010	Sheet 15 of 89	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	***Arsenal DJ1 Discrete***	***X01***

Date: Friday, May 07, 2010 Sheet 16 of 89

(Blanking)

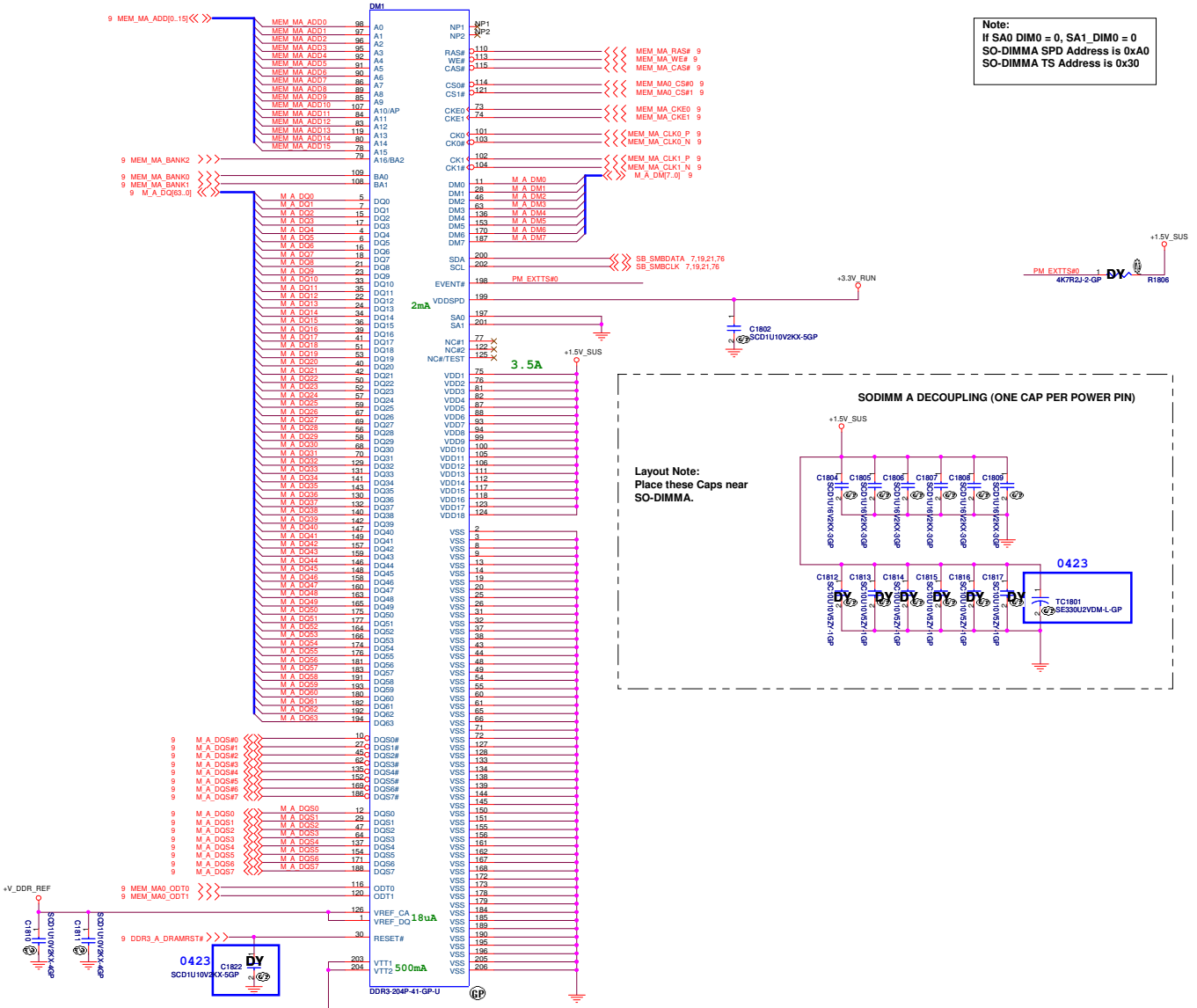
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

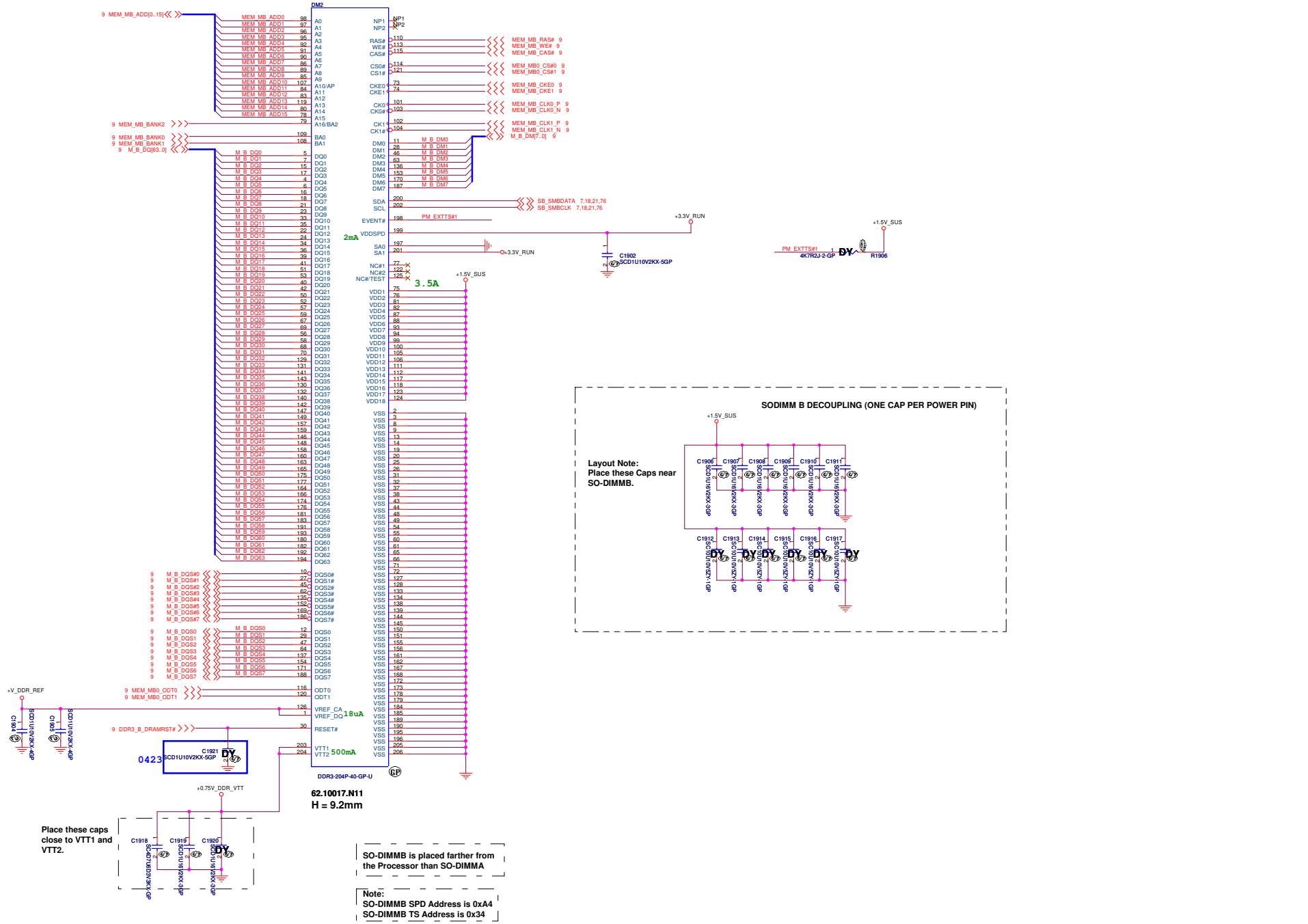
Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*X01*

Date: Friday, May 07, 2010 Sheet 17 of 89



<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR3-SODIMM1		
Size	Document Number: Arsenal DJ1 Discrete	Rev: X01
Date: Friday, May 07, 2010	Sheet 18 of 89	



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
	Arsenal DJ1 Discrete	X01

Date: Friday, May 07, 2010 Sheet 19 of 89

SSID = S.B

SB820M: 71.SB820.M02

placed CAP closed SB820M

0423 PCI_CLK3 EC2002 SC10P50V2JN-4GP DY

U2A

Part 1 of 5

PCI CLKS

PCIE_RST# A_RST#

PCICLK0 PCICLK1/GPO36 PCICLK2/GPO37 PCICLK3/GPO38 PCICLK4/14M_OSC/GPO39 PCIRST#

PCI_CLK1 24, PCI_CLK2 24, PCI_CLK3 24,70, PCLK_FWH 24

R2009 22R2J-2-GP 0423

STRAP PIN

PCI_RST# TP2008

PCI EXPRESS INTERFACES

A_TX0P A_TX0N A_TX1P A_TX1N A_TX2P A_TX2N A_TX3P A_TX3N

A_RX0P A_RX0N A_RX1P A_RX1N A_RX2P A_RX2N A_RX3P A_RX3N

PCIE_CALRP PCIE_CALRN

GPP_TX0P GPP_TX0N GPP_TX1P GPP_TX1N GPP_TX2P GPP_TX2N GPP_TX3P GPP_TX3N

GPP_RX0P GPP_RX0N GPP_RX1P GPP_RX1N GPP_RX2P GPP_RX2N GPP_RX3P GPP_RX3N

PCIE_RCLKP/NB_LNK_CLKP PCIE_RCLKN/NB_LNK_CLKN

NB_DISP_CLKP NB_DISP_CLKN

NB_HT_CLKP NB_HT_CLKN

CPU_HT_CLKP CPU_HT_CLKN

SLT_GFX_CLKP SLT_GFX_CLKN

GPP_CLK0P GPP_CLK0N

GPP_CLK1P GPP_CLK1N

GPP_CLK2P GPP_CLK2N

GPP_CLK3P GPP_CLK3N

GPP_CLK4P GPP_CLK4N

GPP_CLK5P GPP_CLK5N

GPP_CLK6P GPP_CLK6N

GPP_CLK7P GPP_CLK7N

GPP_CLK8P GPP_CLK8N

14M_25M_48M_OSC

25M_X1

25M_X2

SB820M-1-GP

CLOCK GENERATOR

PCI INTERFACE

AD0/GPIO0 AD1/GPIO1 AD2/GPIO2 AD3/GPIO3 AD4/GPIO4 AD5/GPIO5 AD6/GPIO6 AD7/GPIO7 AD8/GPIO8 AD9/GPIO9 AD10/GPIO10 AD11/GPIO11 AD12/GPIO12 AD13/GPIO13 AD14/GPIO14 AD15/GPIO15 AD16/GPIO16 AD17/GPIO17 AD18/GPIO18 AD19/GPIO19 AD20/GPIO20 AD21/GPIO21 AD22/GPIO22 AD23/GPIO23 AD24/GPIO24 AD25/GPIO25 AD26/GPIO26 AD27/GPIO27 AD28/GPIO28 AD29/GPIO29 AD30/GPIO30 AD31/GPIO31

CBE0# CBE1# CBE2# CBE3# FRAME# DEVSEL# IRDY# TRDY# PAR STOP# PERR# SERR# REQ0# REQ1#/GPIO40 REQ2#/CLK_REQ8#/GPIO41 REQ3#/CLK_REQ5#/GPIO42 GNT0# GNT1#/GPO44 GNT2#/GPO45 GNT3#/CLK_REQ7#/GPIO46 CLKRUN# LOCK#

INTE#/GPIO32 INTF#/GPIO33 INTG#/GPIO34 INTH#/GPIO35

PCI_AD23 24, VDDR_SEL 24,51, PCI_AD25 24, PCI_AD26 24, PCI_AD27 24

SB_GPIO28 TP2010, SB_GPIO29 TP2011

SB_GPIO42 TP2003, SB_GPIO46 TP2004

PM_CLKRUN# 37

1'nd 73.01G08.DHG
2'nd 73.01G08.L04

U2002 SNLVC1G08DCKRG4-GP

21 SB_GPIO_PCIE_RST# PCIE_RST#_SB

+3.3V_ALW +3.3V_RUN

33R2J-2-GP R2025 0423 R2026 10KR2J-3-GP

PLTRST#_LAN_WLAN 70,76

C2013 SC150P50V2KX-GP

1'nd 73.01G08.DHG
2'nd 73.01G08.L04

U2001 SNLVC1G08DCKRG4-GP

21 SB_GPIO_A_RST# A_RST#

R2005 0R2J-2-GP PLTRST#_NB_GPU 13,37 GPU, NB

R2008 0R2J-2-GP PLTRST#_EC 37 KBC

R2021 0R0402-PAD X01

LPC

LPCCLK0 LPCCLK1 LAD0 LAD1 LAD2 LAD3 LFRAME# LDRQ0# LDRQ1#/CLK_REQ6#/GPIO49 SERIRQ/GPIO48

RN2008 SRN22-3-GP RN2009 SRN33J-4-GP

PCLK_KBC 24,37 LPCCLK1 24

LPC_LAD0 37,70 LPC_LAD1 37,70 LPC_LAD2 37,70 LPC_LAD3 37,70 LPC_LFRAME# 37,70

TP_LPC_LDRQ0# TP2005 TP_LPC_LDRQ1# TP2006

INT_SERIRQ 37

0423

LPC Bus Routing first connects to MINICARD then connects to KBC

CPU

ALLOW_LDTSTP/DMA_ACTIVE# PROCHOT# LDT_PG LDT_STP# LDT_RST#

ALLOW_LDTSTOP 13 CPU_PROCHOT# 10 CPU_LDT_PWRGD 10,42 CPU_LDT_STOP# 10,13 CPU_LDT_RST# 10

RTC

32K_X1 32K_X2 RTCCLK INTRUDER_ALERT# VDDBT_RTC_G

R2018 10R2J-2-GP RTCCLK_KBC 37 RTC_CLK 39

RTC_CLK INTRUDER_ALERT#

TP2007 +RTC_CELL

SCD1U10V2KX-4GP C2014

32K_X1 32K_X2_R 32K_X2 R2016 0R2J-2-GP

X2002 32D768KHZ-40GPU R2014 20MR3-GP

SC12P50V2JN-3GP C2011 SC12P50V2JN-3GP C2012

<Core Design>

LAN WLAN

12 ALINK_NBRX_SBTX_P0 12 ALINK_NBRX_SBTX_N0 12 ALINK_NBRX_SBTX_P1 12 ALINK_NBRX_SBTX_N1 12 ALINK_NBRX_SBTX_P2 12 ALINK_NBRX_SBTX_N2 12 ALINK_NBRX_SBTX_P3 12 ALINK_NBRX_SBTX_N3

C2001 SC150P50V2KX-GP A_RST# R2024 22R2J-2-GP PCIE_RST#_SB A_RST#_R

C2002 C2003 C2004 C2005 C2006 C2007 C2008 C2009 SCD1U16V2KX-3GP

ALINK_NBRX_SBTX_C_P0 AD26 ALINK_NBRX_SBTX_C_N0 AD27 ALINK_NBRX_SBTX_C_P1 AC28 ALINK_NBRX_SBTX_C_N1 AC29 ALINK_NBRX_SBTX_C_P2 AB29 ALINK_NBRX_SBTX_C_N2 AB28 ALINK_NBRX_SBTX_C_P3 AB26 ALINK_NBRX_SBTX_C_N3 AB27

12 ALINK_NBTX_SBRX_P0 AE24
12 ALINK_NBTX_SBRX_N0 AE23
12 ALINK_NBTX_SBRX_P1 AD25
12 ALINK_NBTX_SBRX_N1 AD24
12 ALINK_NBTX_SBRX_P2 AC24
12 ALINK_NBTX_SBRX_N2 AC25
12 ALINK_NBTX_SBRX_P3 AB25
12 ALINK_NBTX_SBRX_N3 AB24

Place R <100mils form pins AD29,AD28

+1.1V_RUN_PCIE_VDDR R2002 590R2F-GP R2007 2KR2F-3-GP SB_PCIE_CALRP AD29 SB_PCIE_CALRN AD28

76 PCIE_TXP1 76 PCIE_TXN1 76 PCIE_TXP0 76 PCIE_TXN0

SCD1U16V2KX-3GP C2018 C2019 C2020 C2021

PCIE_C_TXP1 AA28 PCIE_C_TXN1 AA29 PCIE_C_TXP0 Y29 PCIE_C_TXN0 Y28

0423

LAN WLAN

76 PCIE_RXP1 76 PCIE_RXN1 76 PCIE_RXP0 76 PCIE_RXN0

AA22 Y21 AA25 AA24

NOTE: SB8XX ONLY SUPPORTS 2 GPP PORT 2 AND 3 IS NOT SUPPORTED. (From CRB)

USE EXTERNAL CLKGEN

7 SB_PCIE_CLK 7 SB_PCIE_CLK#

M23 P23 U29 U28 T26 T27 V21 T21 V23 T23 L29 L28 N29 N28 M29 M28 T25 V25 L24 L23 P25 M25 P29 P28 N26 N27 T29 T28

0824

1nd 82.30020.851
2nd 82.30020.791

TP2009 OSC_CLK L25

25M_X1 L26

25M_X2 L27

R2017 1MR2J-1-GP X2001 XTAL-25MHZ-102-GP C2014 SC12P50V2JN-3GP C2015 SC12P50V2JN-3GP

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_PCIE&PCI_(1/5)

Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 20 of 89

SSID = S.B

SB820M: 71.SB820.M02

USB	
Pair	Device
0	USB2
1	USB3
2	USB0 (I/O Board)
3	USB1 (I/O Board, 17")
4	WLAN
5	RESERVED
6	RESERVED
7	RESERVED
8	RESERVED
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	RESERVED
13	RESERVED

Part 4 of 5

SB820M-1-GP

GbE Controller Not Enabled

EC Not Implemented

EC Not Implemented

Not use

Strap Pin / define to use LPC or SPI ROM

Close SB

SBD DDR RESET

JTAG_TDI

JTAG_RST#

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

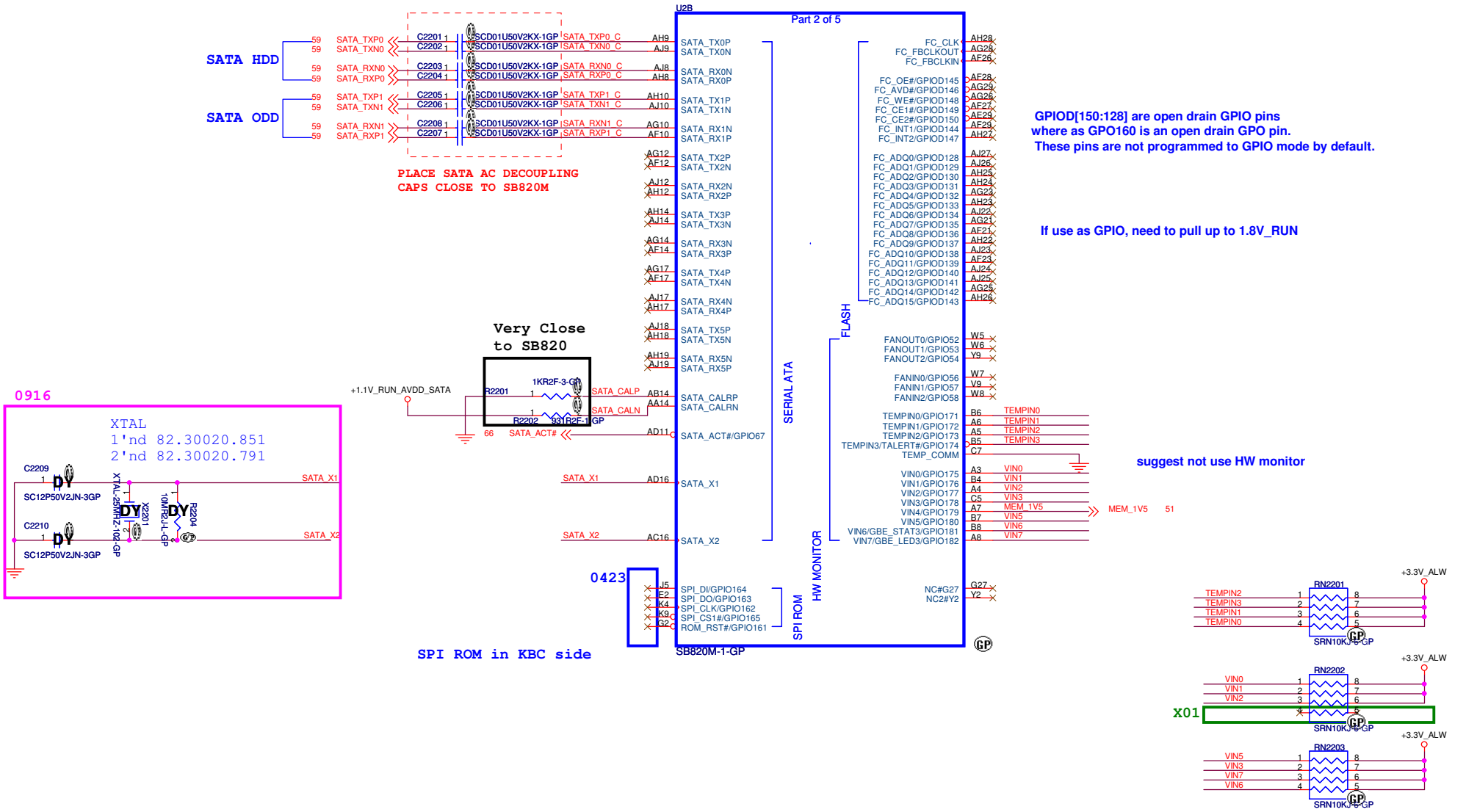
Title: SB820M_USB&GPIO_(2/5)

Size: Custom | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 21 of 89

SSID = S.B

SB820M: 71.SB820.M02



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

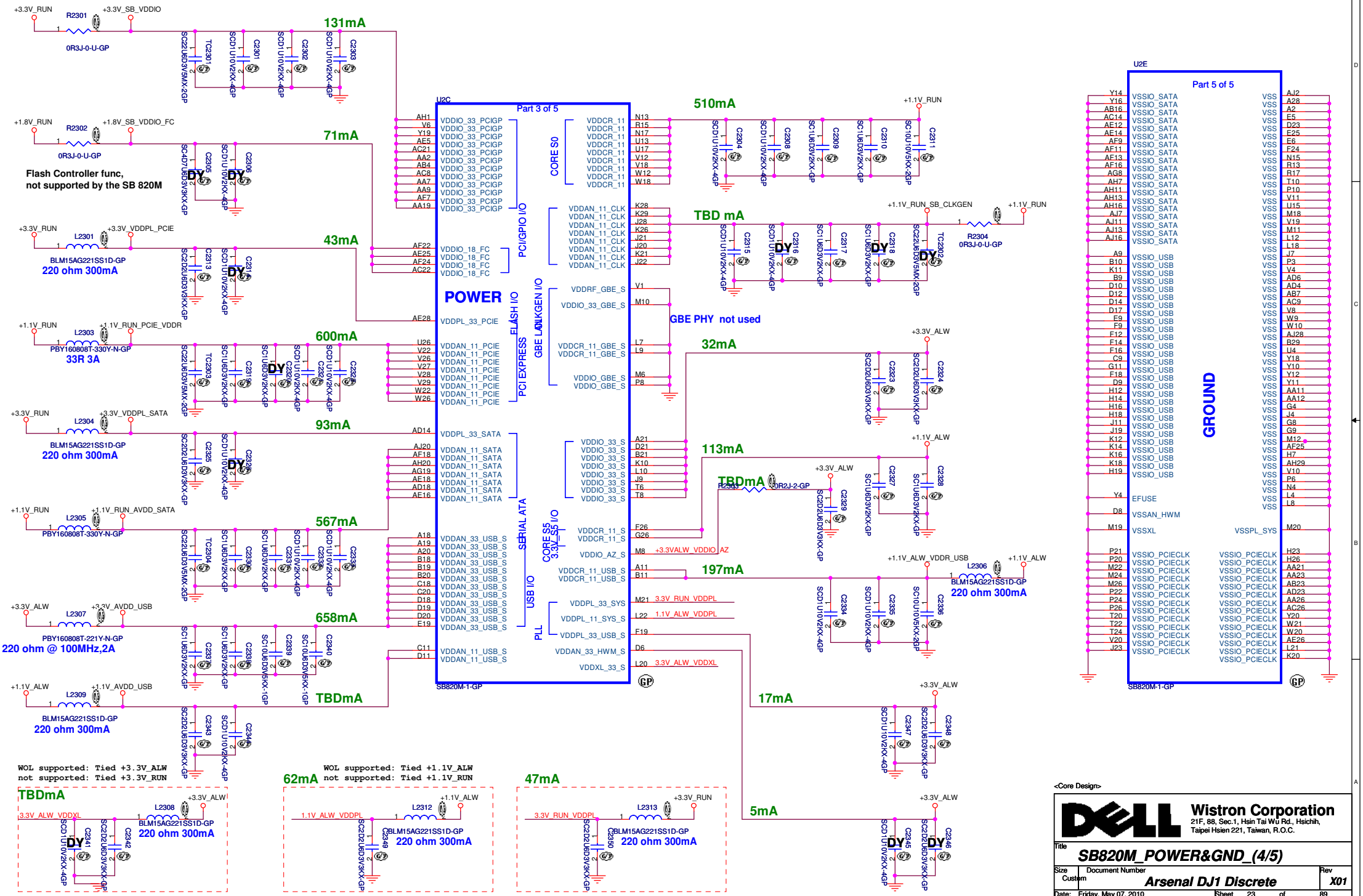
Title: SB820M_SATA-IDE_(3/5)

Size: Custom | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 22 of 89

SSID = S.B

SB820M: 71.SB820.M02



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

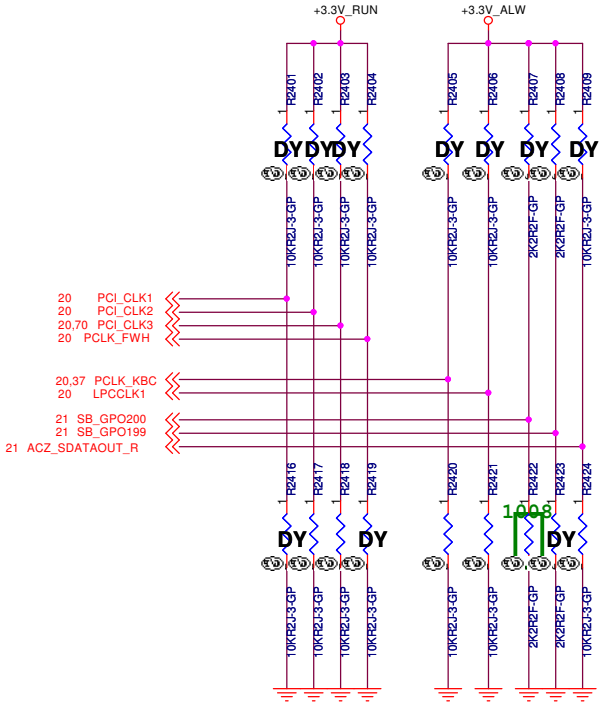
Title: SB820M_POWER&GND_(4/5)

Size: Custom | Document Number: Arsenal DJ1 Discrete | Rev: X01

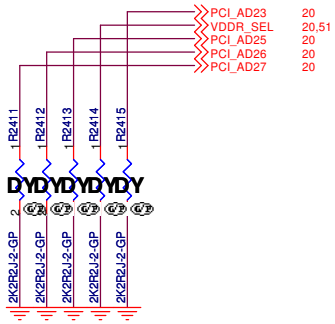
Date: Friday, May 07, 2010 | Sheet 23 of 89

SSID = S.B

REQUIRED STRAPS



DEBUG STRAPS



REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCLK_FWH (PCI_CLK4)	PCLK_KBC (LPCCLK0)	LPCCLK1	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	DEFAULT CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	L, H = LPC ROM DEFAULT L, L = FWH ROM

Not Applicable to SB820M
but provision for pull-down is required.

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_STRAPPING_(5/5)

Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 24 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CPU (VCC_CORE)

Size	Document Number	Rev
	Arsenal DJ1 Discrete	X01

Date: Friday, May 07, 2010 Sheet 25 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CPU (VCC_GFXCORE)

Size | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 26 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 27 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 28 of 89

(Blanking)

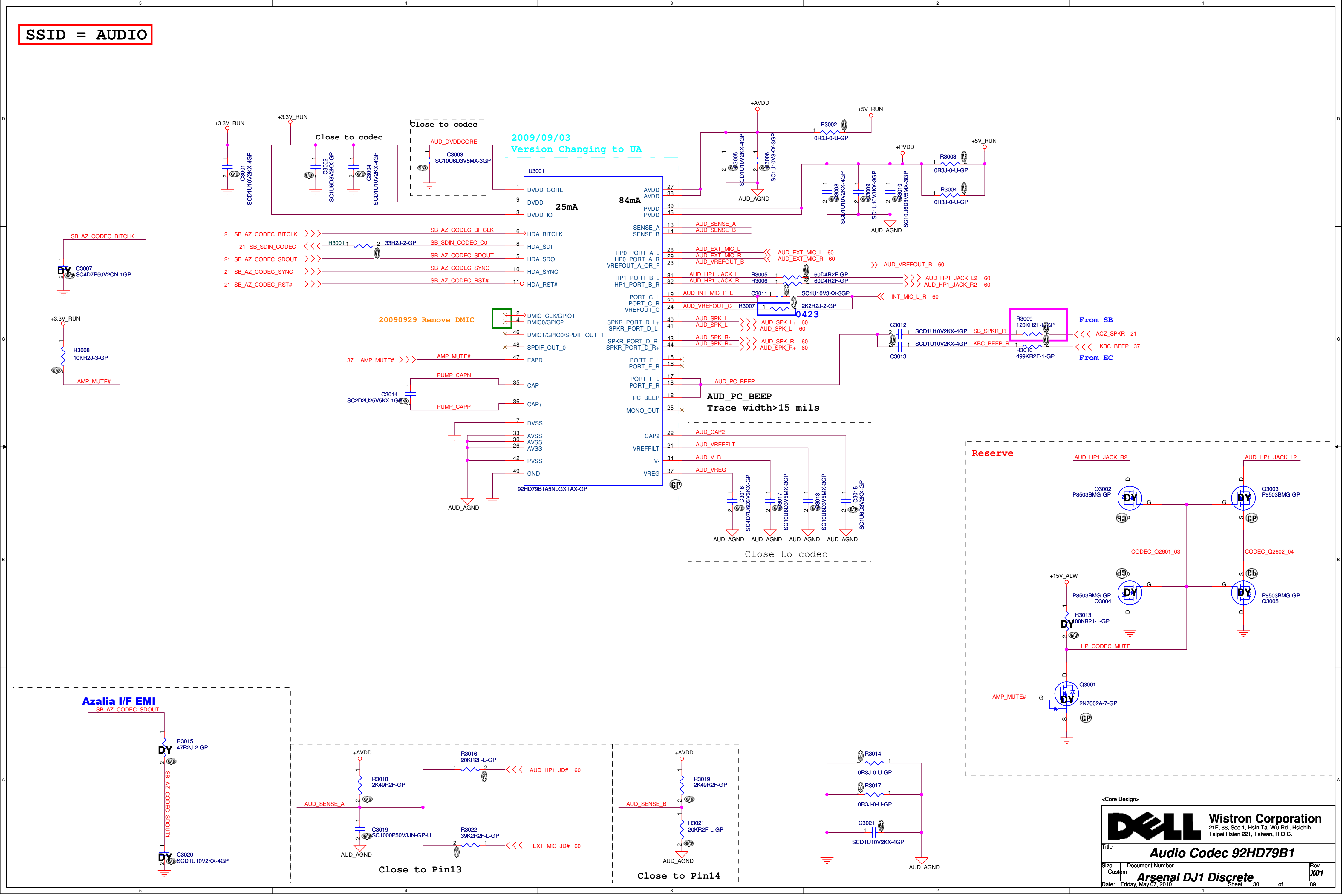
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 29 of 89



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio Codec 92HD79B1	
Size: Custom	Document Number: Arsenal DJ1 Discrete	Rev: X01
Date: Friday, May 07, 2010	Sheet 30 of 89	

(Blanking)

<Core Design>

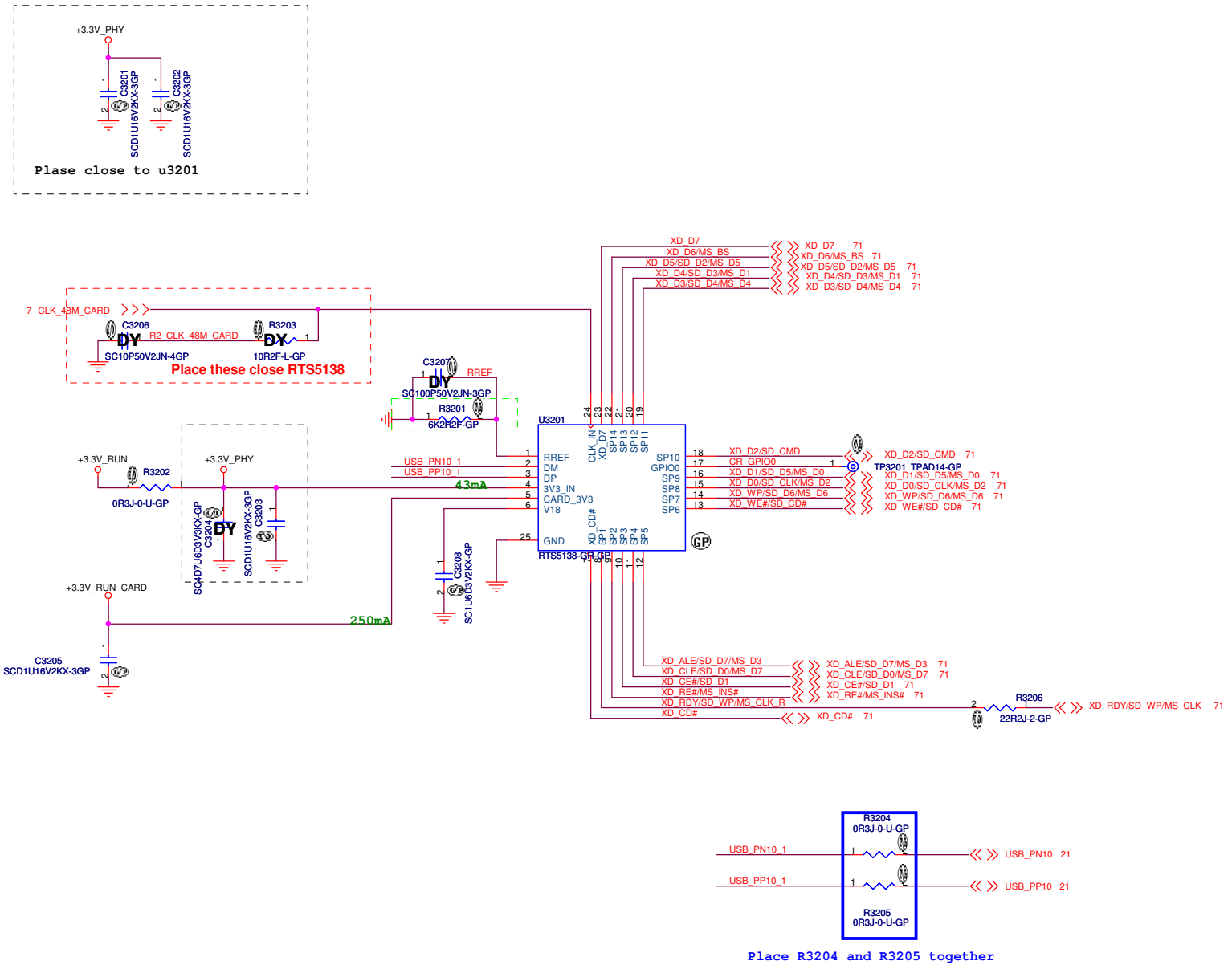
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 31 of 89

SSID = SDIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Card Reader-RTS5138***

Size: Custom | Document Number: ***Arsenal DJ1 Discrete*** | Rev: ***X01***

Date: Friday, May 07, 2010 | Sheet 32 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*X01*

Date: Friday, May 07, 2010 Sheet 33 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 34 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 35 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	***Arsenal DJ1 Discrete***	***X01***

Date: Friday, May 07, 2010 Sheet 36 of 89

SSID = KBC

CAP close to VCC-GND pin pair

U3701A NPCE781BA0DX-GP

A/D D/A LPC SMB SP SPI GPIO SER/IR

DJ1 PU
DJ2 PD

UMA PD
DIS PU

MB VERSION

ID	VER2	VER1	VER0
X00	0	0	0
X01	0	0	1
X02	0	1	0
A00	0	1	1

KBC CLK EMI

Place close to KBC

Remove KBC crystal

Internal PU

For EC to detect leakage

U3701B NPCE781BA0DX-GP

KBC PS/2 FIU

reserve U3703

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE781BA0DX

Size: A2 | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 37 of 89

(Blanking)

<Core Design>

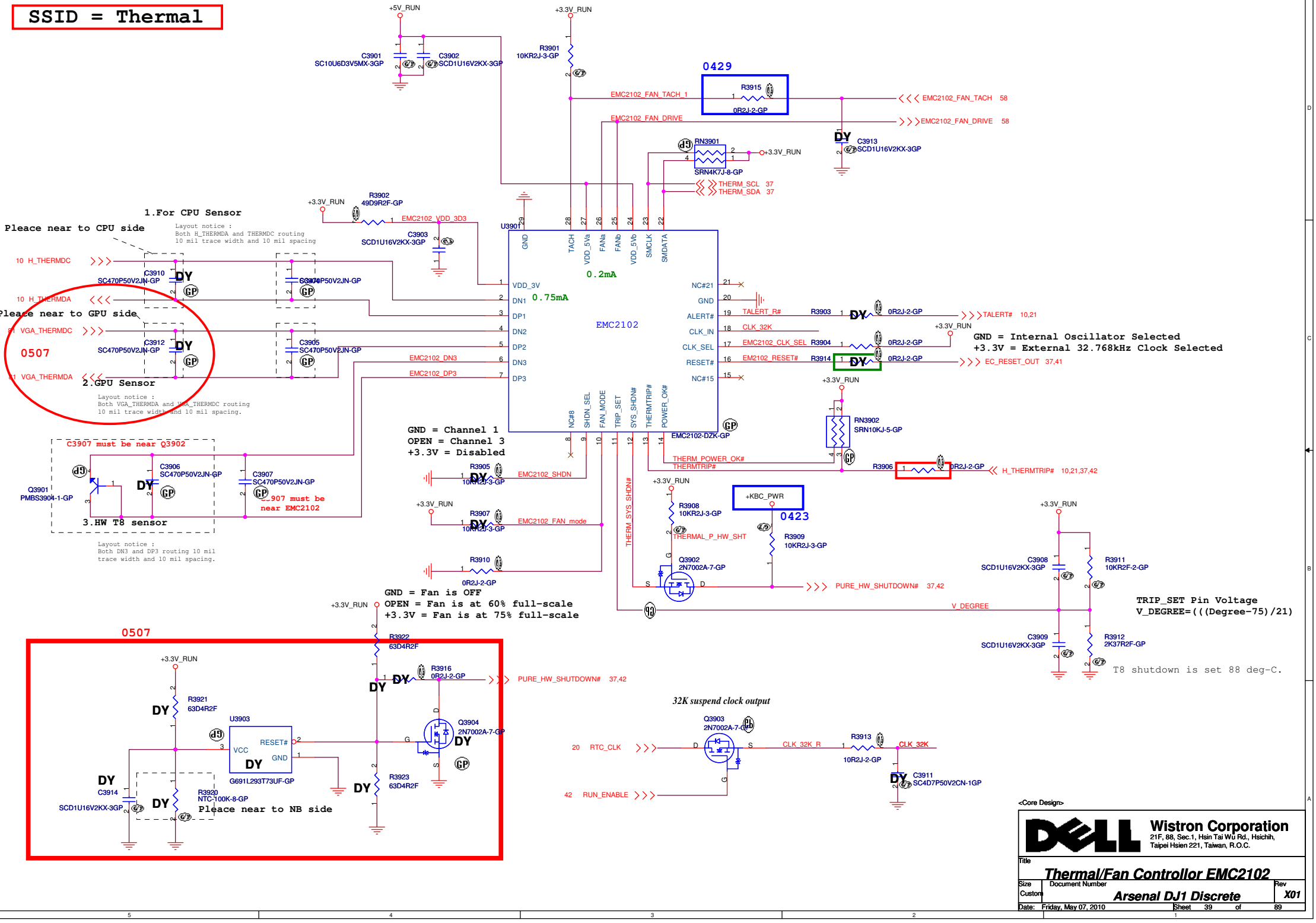
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 38 of 89

SSID = Thermal



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 39 of 89

(Blanking)

<Core Design>

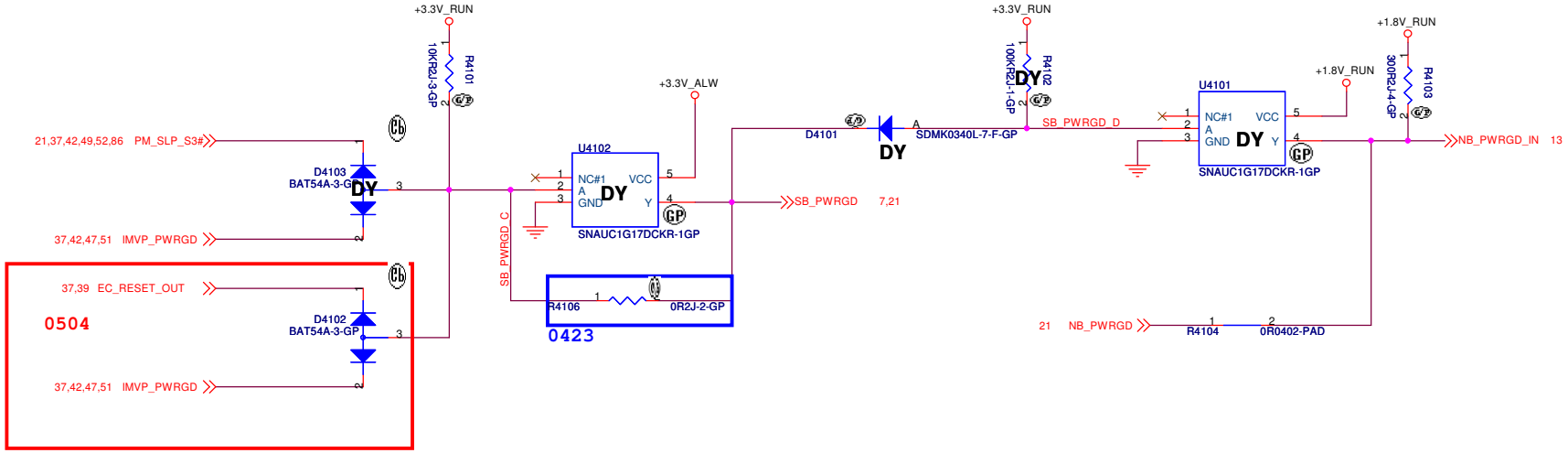
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 40 of 89

SSID = Reset.Suspend

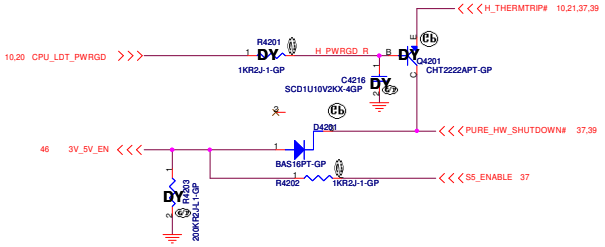


<Core Design>

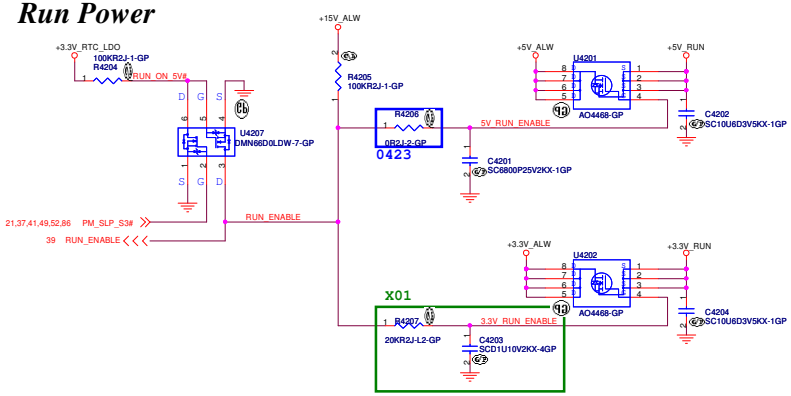
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power On Logic*		
Size: A3	Document Number: *Arsenal DJ1 Discrete*	Rev: *X01*
Date: Friday, May 07, 2010	Sheet 41 of 89	

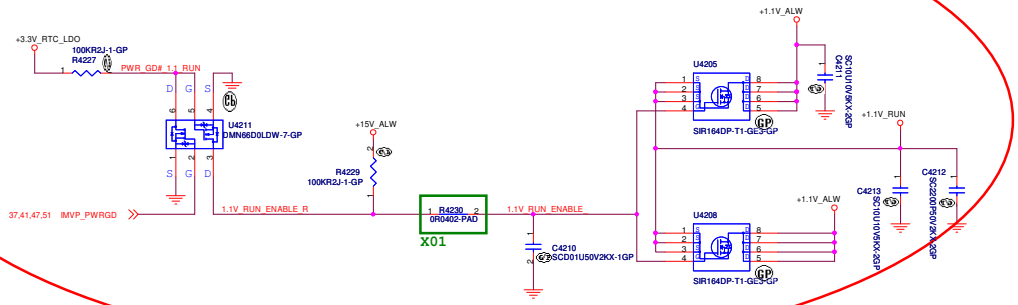
SSID = Reset.Suspend



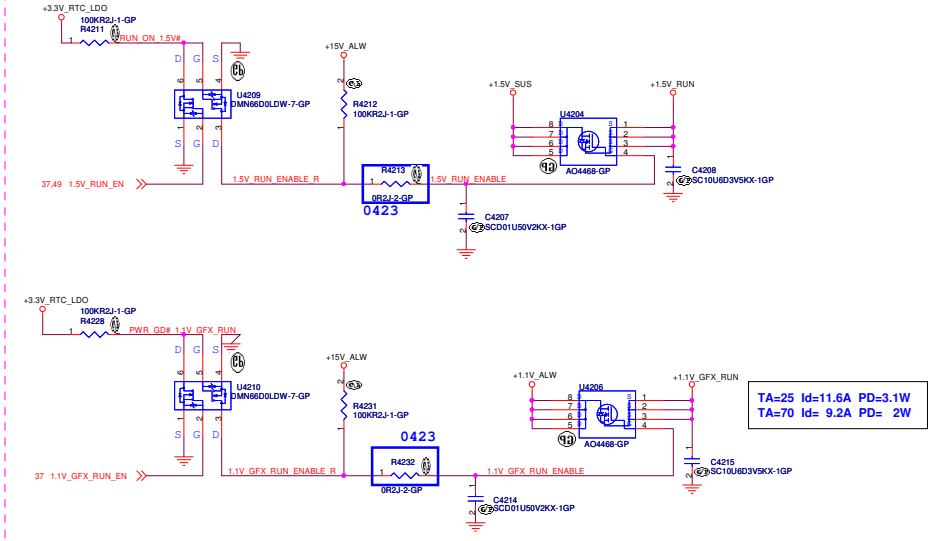
Run Power

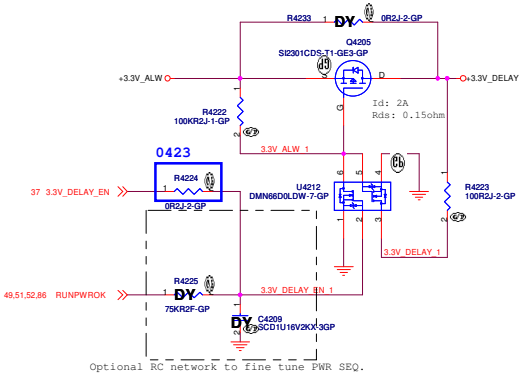


0506 +1.1V_ALW transfer to +1.1V_RUN

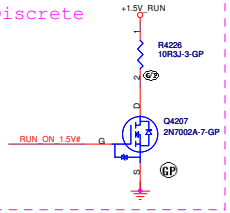


For Discrete





For Discrete



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A2	Arsenal DJ1 Discrete	X01

Date: Friday, May 07, 2010 Sheet 42 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 43 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 44 of 89

(Blanking)

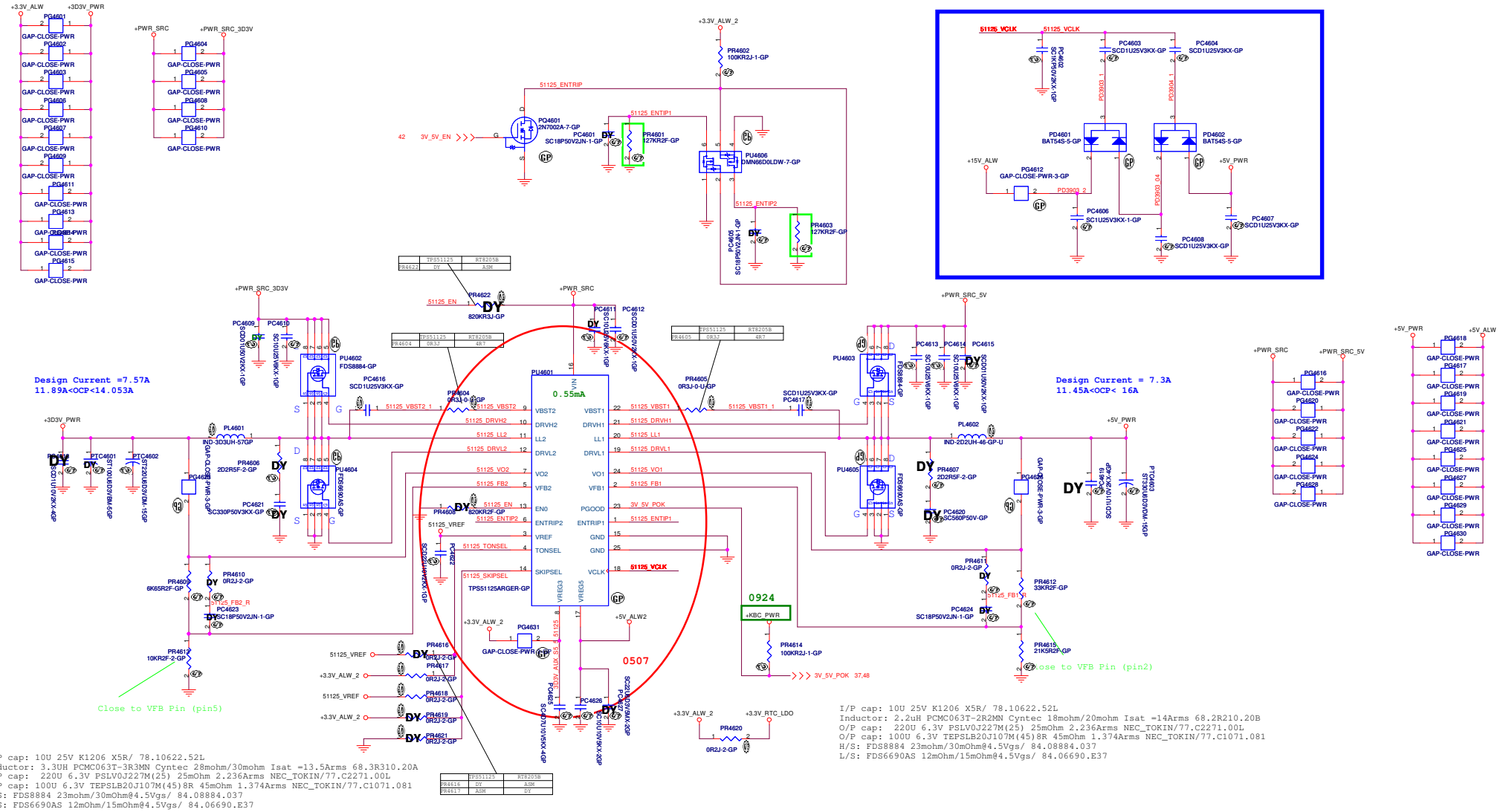
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 45 of 89



TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT8205B(74.08208.A73):

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

TPS51125	74.51125.073
RT8208BGQW	74.08208.A73

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51125_5V/3D3V

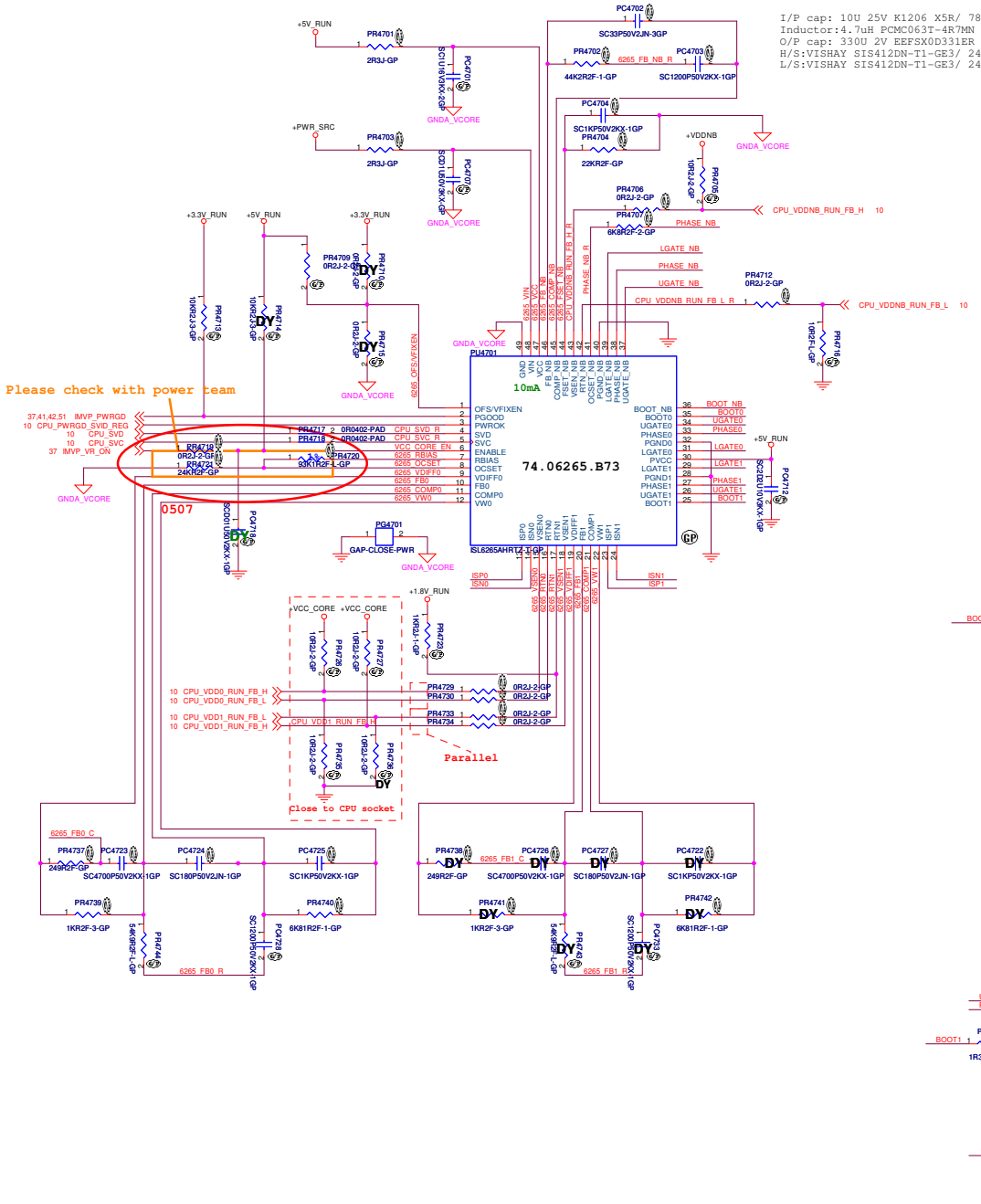
Size	Document Number	Rev
A2	Arsenal DJ1 Discrete	X01

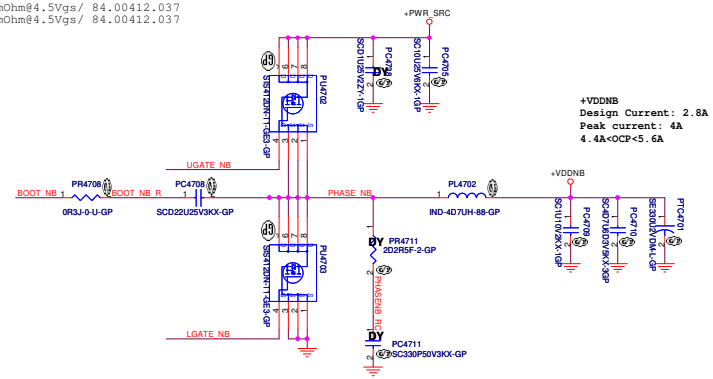
Date: Friday, May 07, 2010 Sheet 46 of 89

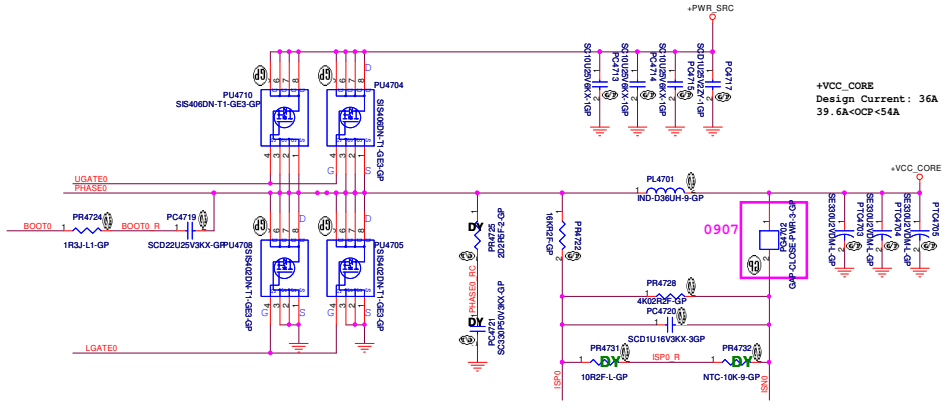
SSID = CPU.Regulator

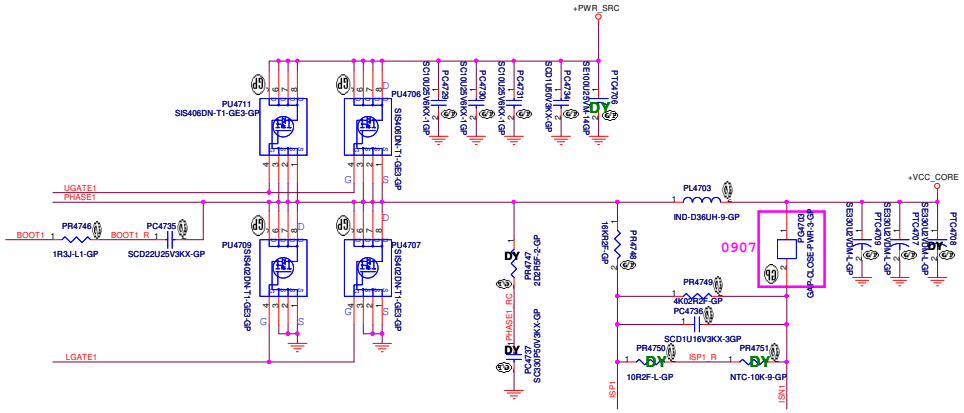
ISL6265HRTZ-T for +VCC_CORE&+VDDNB

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor:4.7uH PCMC063T-4R7MN 35mohm Isat =10Arms CYNTEC/68.4R710.20D
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037









I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm
Isat =60Arms 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S:VISHAY SiR462DP/ POWERPAK-8.2/810mOhm/ 4.5Vgs/ 84.00462.037
L/S:VISHAY SI7658ADP/ POWERPAK-2.3/ 2.8mOhm/ 4.5Vgs/ 84.07658.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VREG : +VCC_CORE&+VDDNB

Size	Document Number	Rev
A2	Arsenal DJ1 Discrete	X01

Date: Friday, May 07, 2010 Sheet 47 of 89

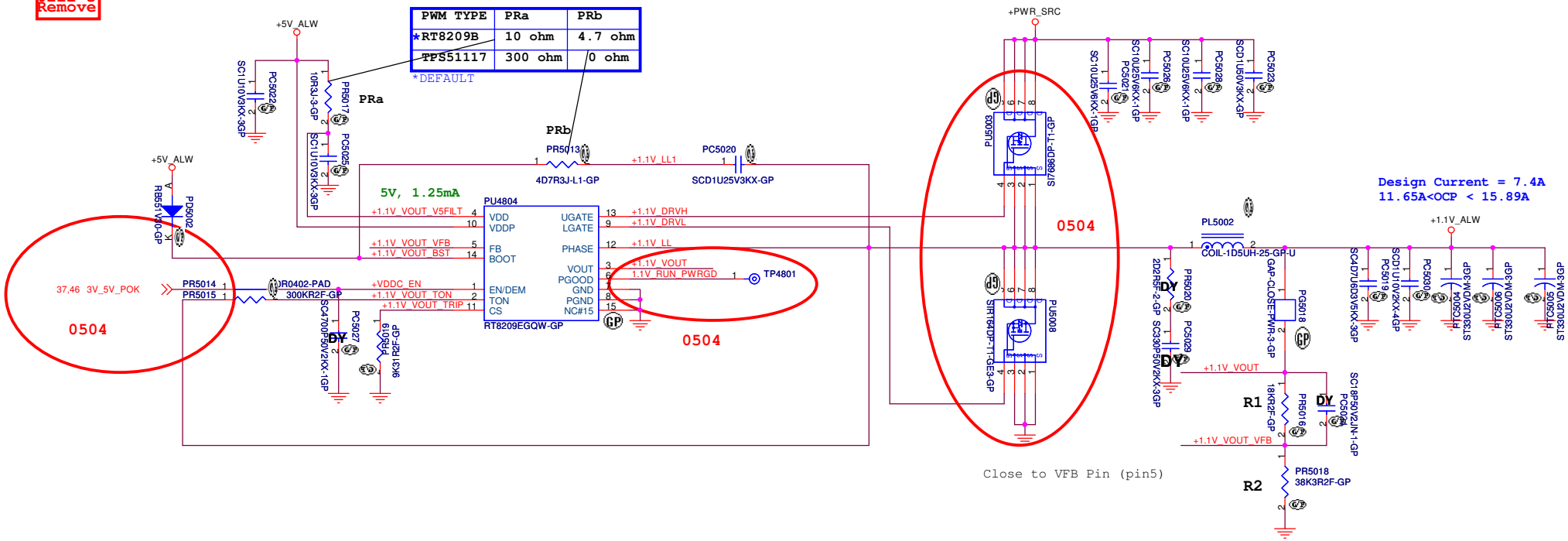
SSID = PWR.Plane.Regulator_+1.1V_ALW

RT8209EGQW for +1.1V_RUN

0222-3 Remove

PWM TYPE	PRa	PRb
*RT8209B	10 ohm	4.7 ohm
~~TPS51117~~	300 ohm	0 ohm

*DEFAULT



Vout=0.75V*(R1+R2)/R2

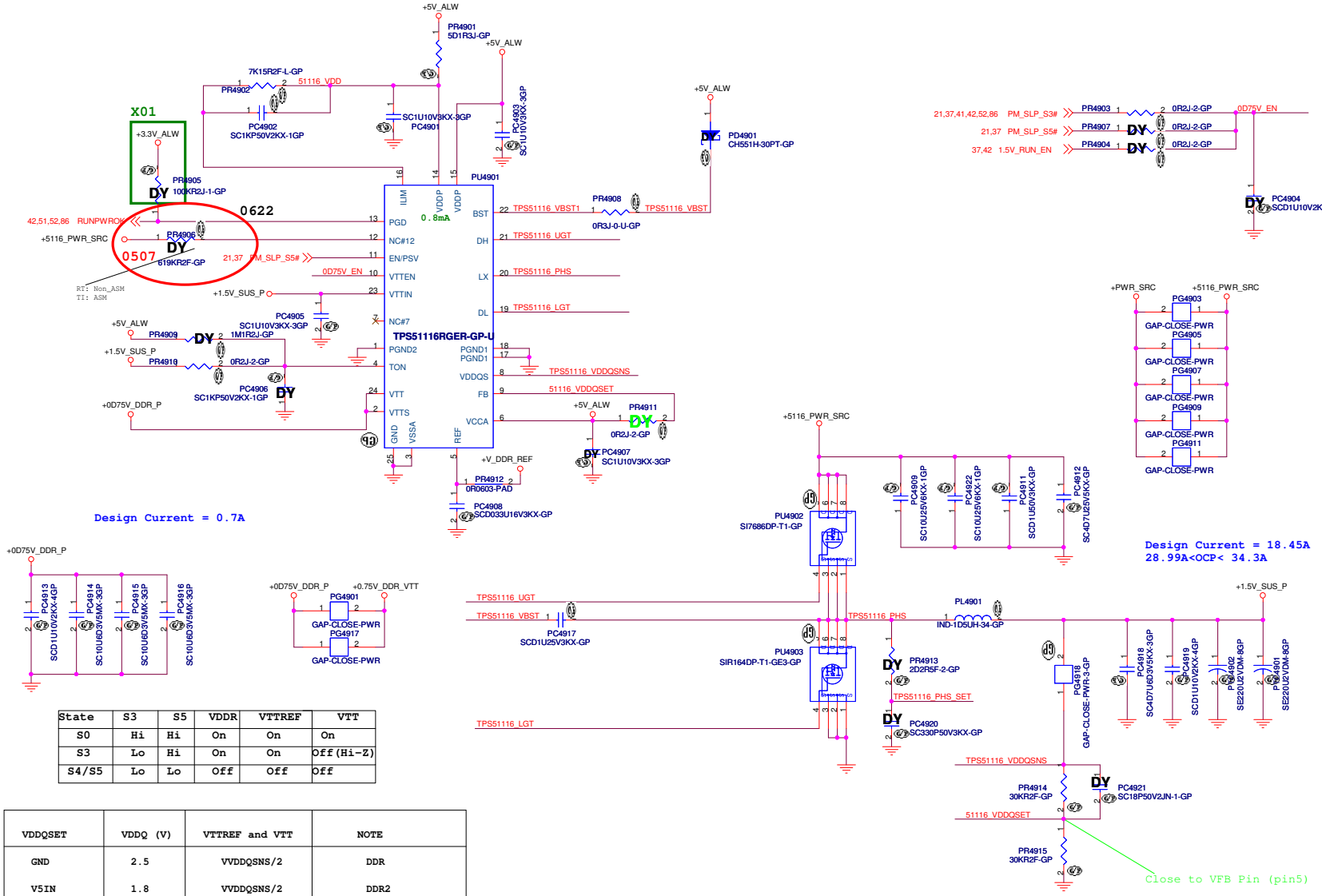
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN 33Arms CYNTEC/ 68.1R510.10J
O/P cap: 330U 2.5V EEFCX0E331QR 15mOhm 2.7Arms PANASONIC/ 79.3371V.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR164DP/ POWERPAK-8/ 2.6mOhm/3.2mohm@4.5Vgs/ 84.00164.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E_+1.1VALW
Size: A3
Document Number: Arsenal DJ1 Discrete
Rev: X01
Date: Friday, May 07, 2010
Sheet 48 of 89

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10J
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR164DP/ POWERPAK-8/ 2.6mOhm/3.2mohm@4.5Vgs/ 84.00164.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116_+1.5V_SUS

Size	Document Number	Rev
Custom	Arsenal DJ1 Discrete	X01

Date: Friday, May 07, 2010 Sheet 49 of 89

SSID = PWR.Plane.Regulator_VDDC

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

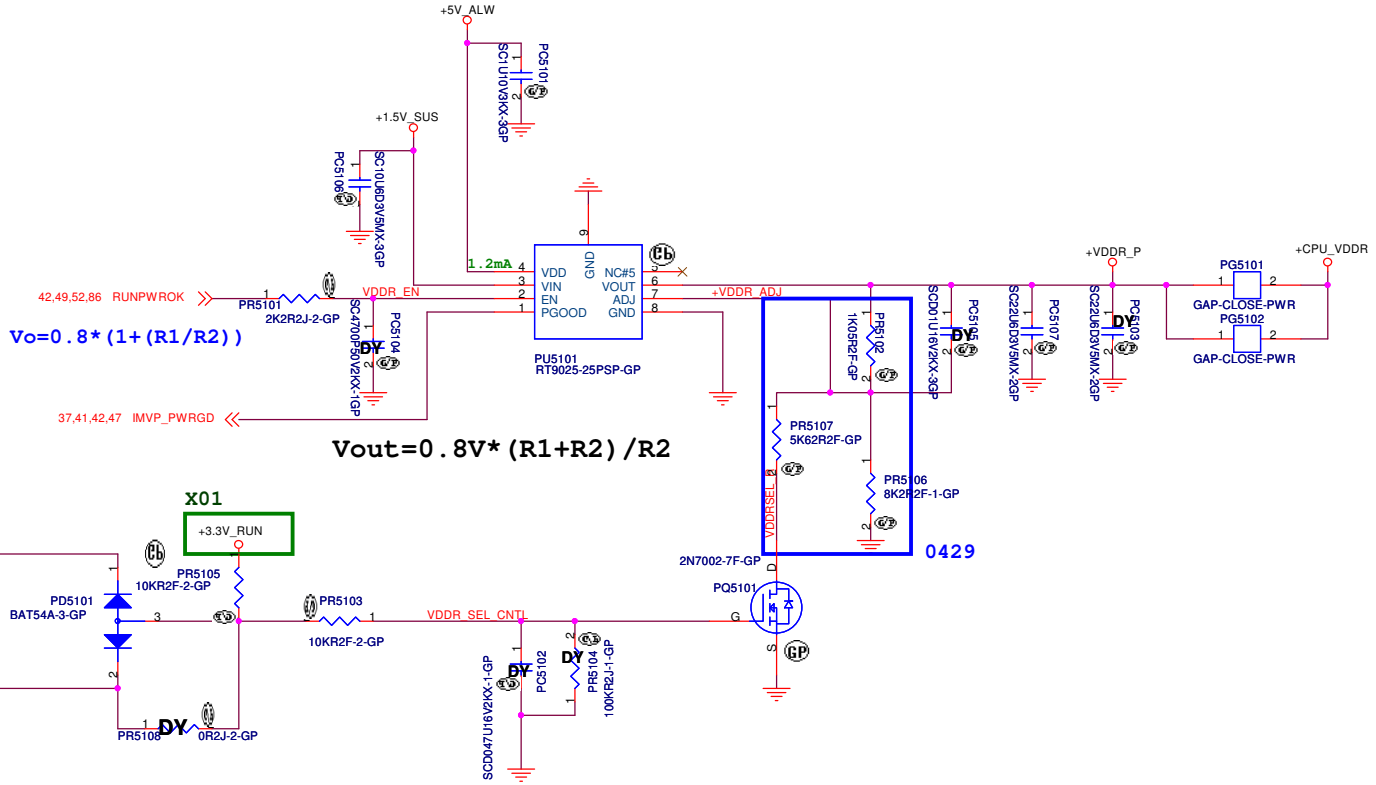
Title: TPS51117 +VDDC

Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 50 of 89

SSID = PWR.Plane.Regulator_VDDR

RT9025 for +VDDR



VDDR_SEL	+CPU_VDDR
H	1.05V
L	0.95V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

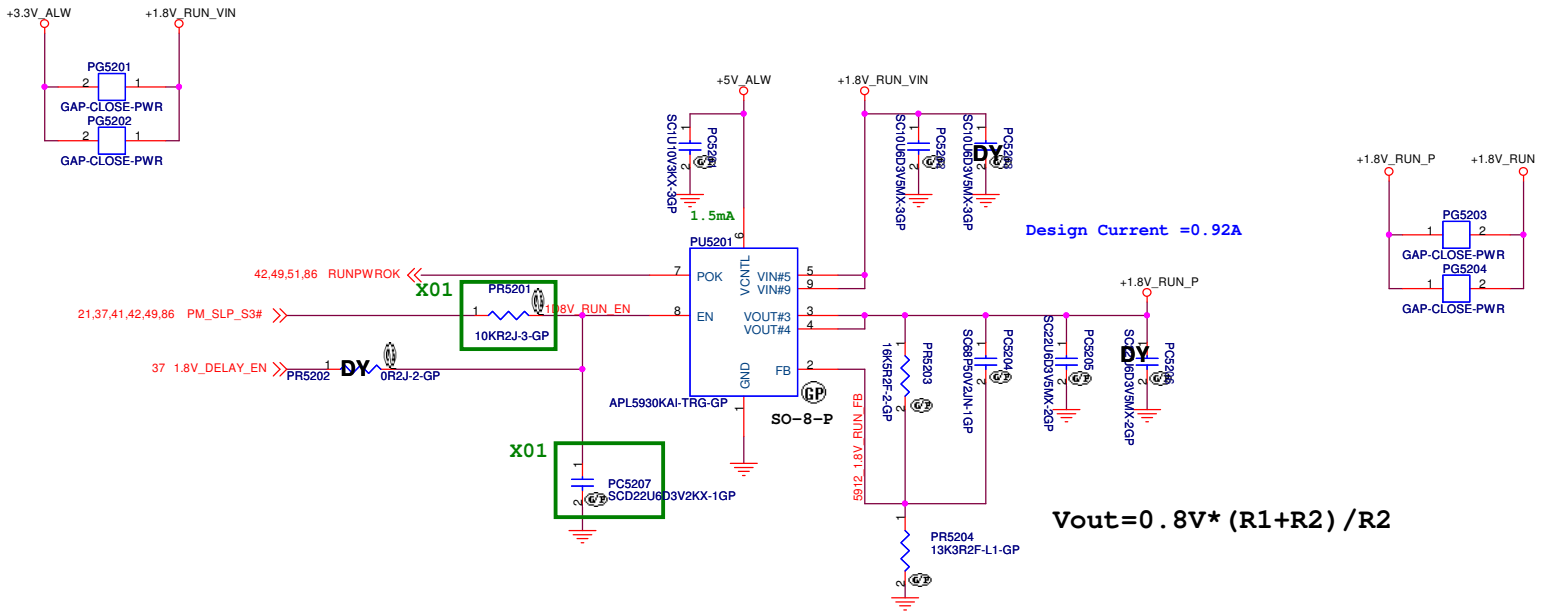
Title: RT9025 +VDDR

Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 51 of 89

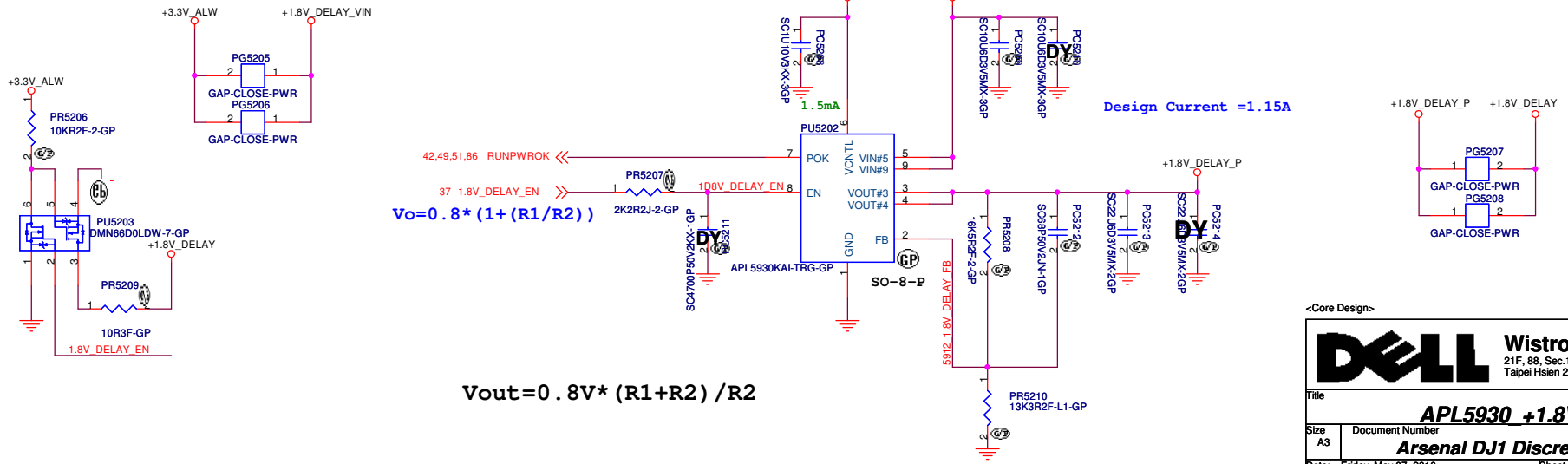
SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_DELAY



<Core Design>

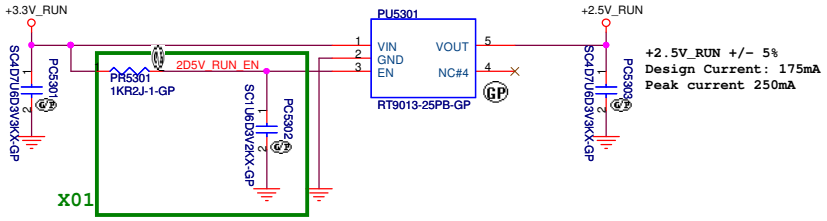
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	APL5930_+1.8V_RUN	
Size: A3	Document Number: Arsenal DJ1 Discrete	Rev: X01
Date: Friday, May 07, 2010	Sheet 52 of 89	

SSID = PWR.Plane.Regulator_0P9v

SSID = PWR.Plane.Regulator_2p5v

RT9013-25PB for +2.5V_RUN



<Core Design>

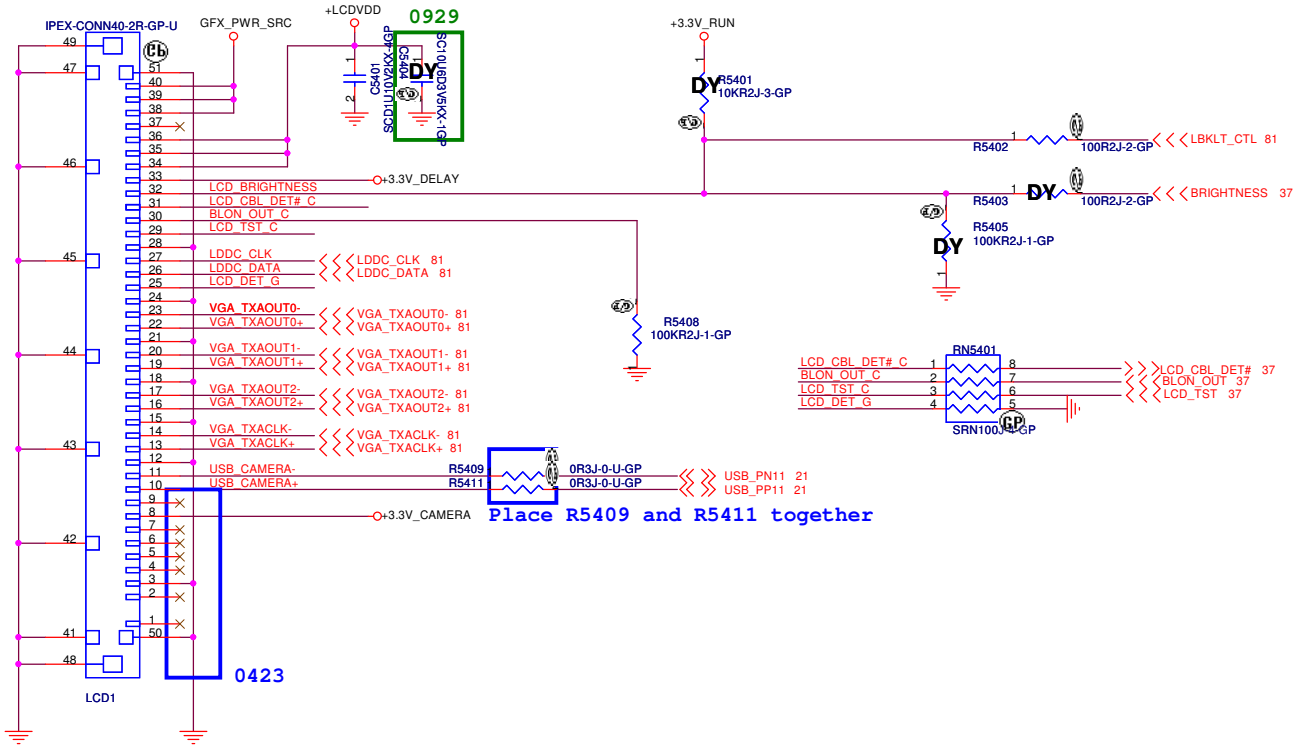
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VREG : +CPU_VDDR&+2.5V_RUN		
Size: Custom	Document Number: Arsenal DJ1 Discrete	Rev: X01
Date: Friday, May 07, 2010	Sheet 53 of 89	

SSID = VIDEO

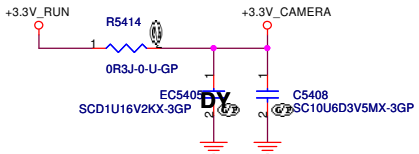
LCD_BRIGHTNESS
LCD_TST
C5402 SC33P50V2JN-3GP (DY)
C5403 SC33P50V2JN-3GP (DY)
For EMI request

LVDS CONNECTOR



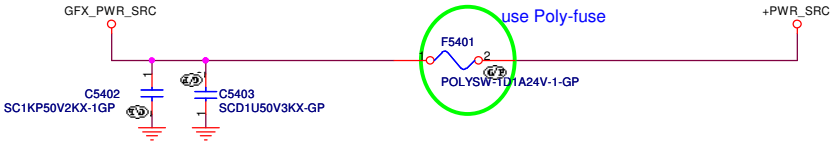
20.F1093.040
20.F1289.040

Camera Power



SSID = Inverter

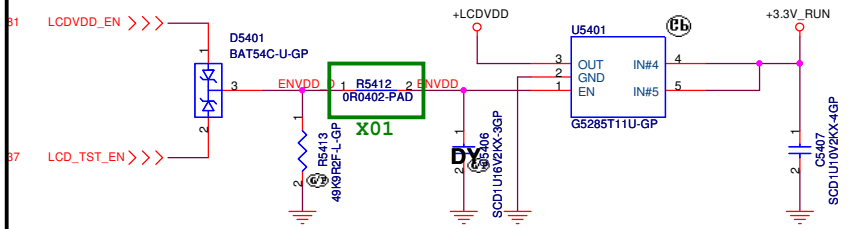
INVERTER POWER



0423

SSID = VIDEO

LCD POWER



<Core Design>

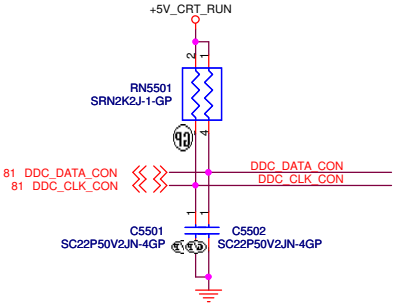
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

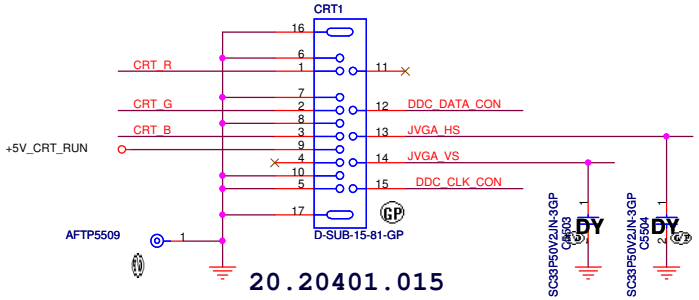
Title		
LCD/Inverter Connector		
Size: A3	Document Number: Arsenal DJ1 Discrete	Rev: X01
Date: Friday, May 07, 2010	Sheet 54 of 89	

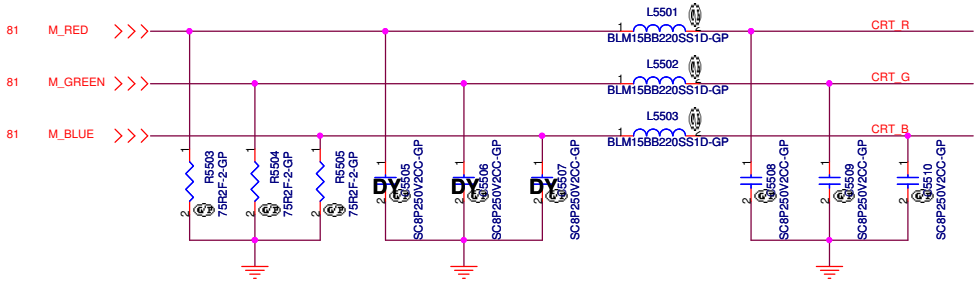
SSID = VIDEO

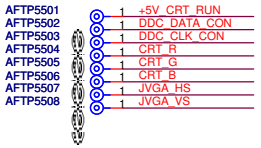
Layout Note:

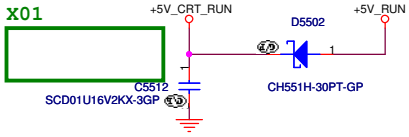
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

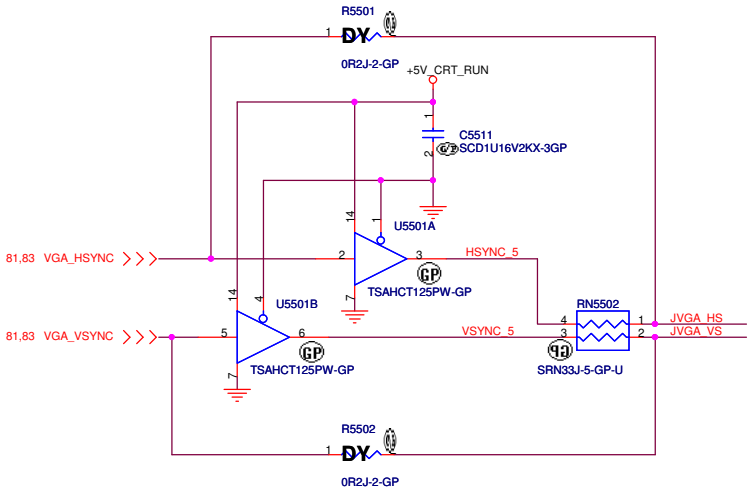


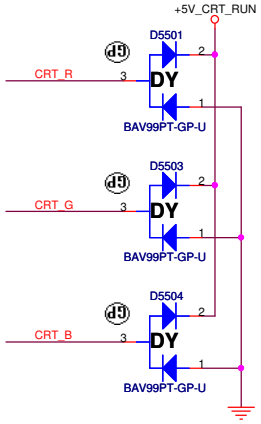


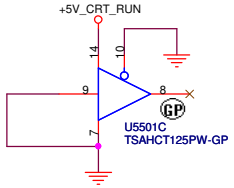


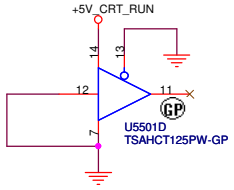












<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 55 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 56 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

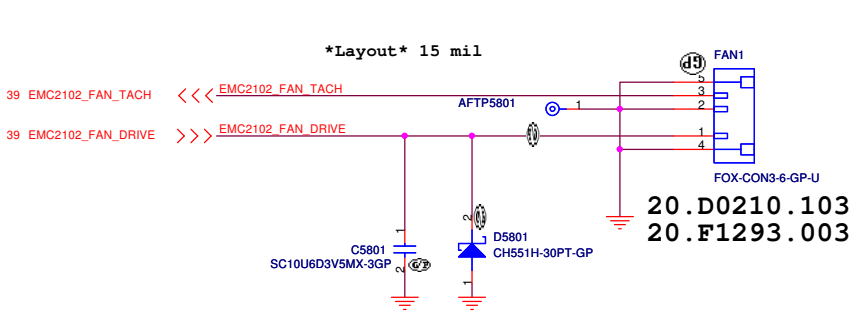
Title: HDMI (Reserved)

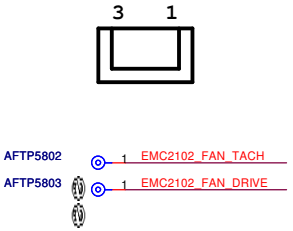
Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 57 of 89

SSID = Thermal

Fan Connector





<Core Design>

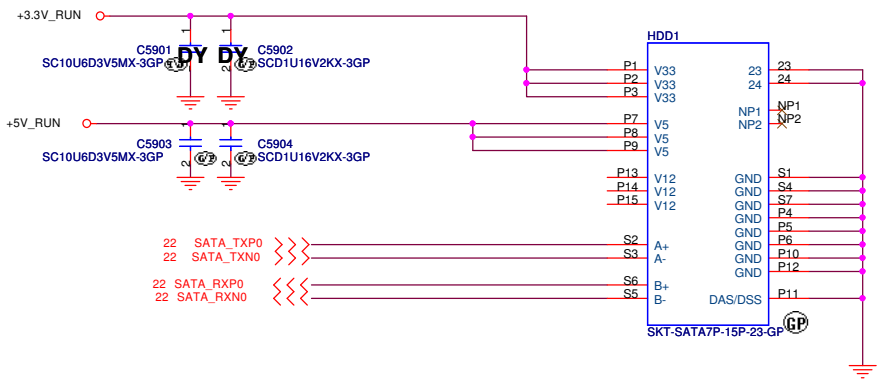
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP/Fan Connector		
Size: A3	Document Number: Arsenal DJ1 Discrete	Rev: X01
Date: Friday, May 07, 2010	Sheet 58 of 89	

SSID = SATA

SATA HDD Connector

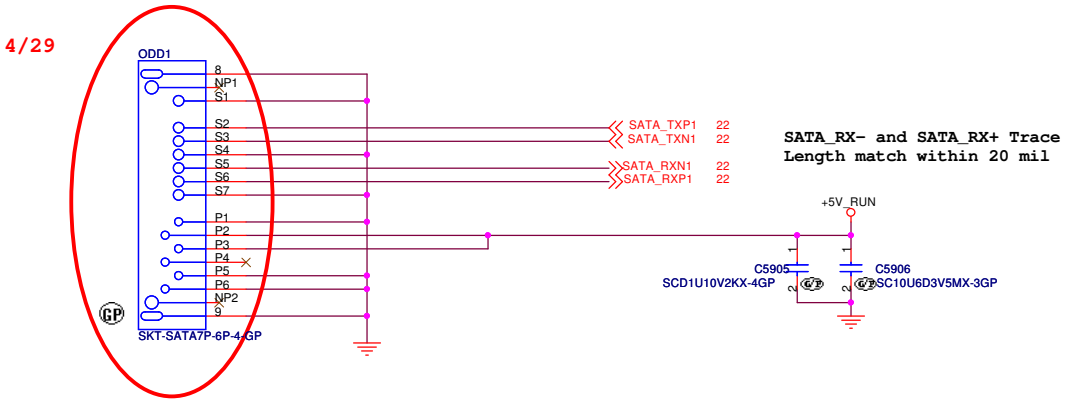
4/29



X02 22.10300.961

ODD Connector

4/29



X02 22.10300.811

22.10300.471

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

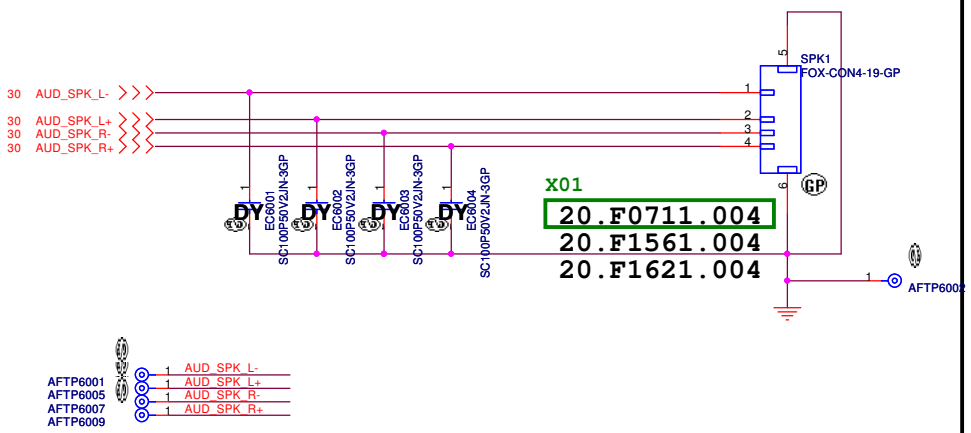
Title: HDD/ODD

Size	Document Number	Rev
A3	Arsenal DJ1 Discrete	X01

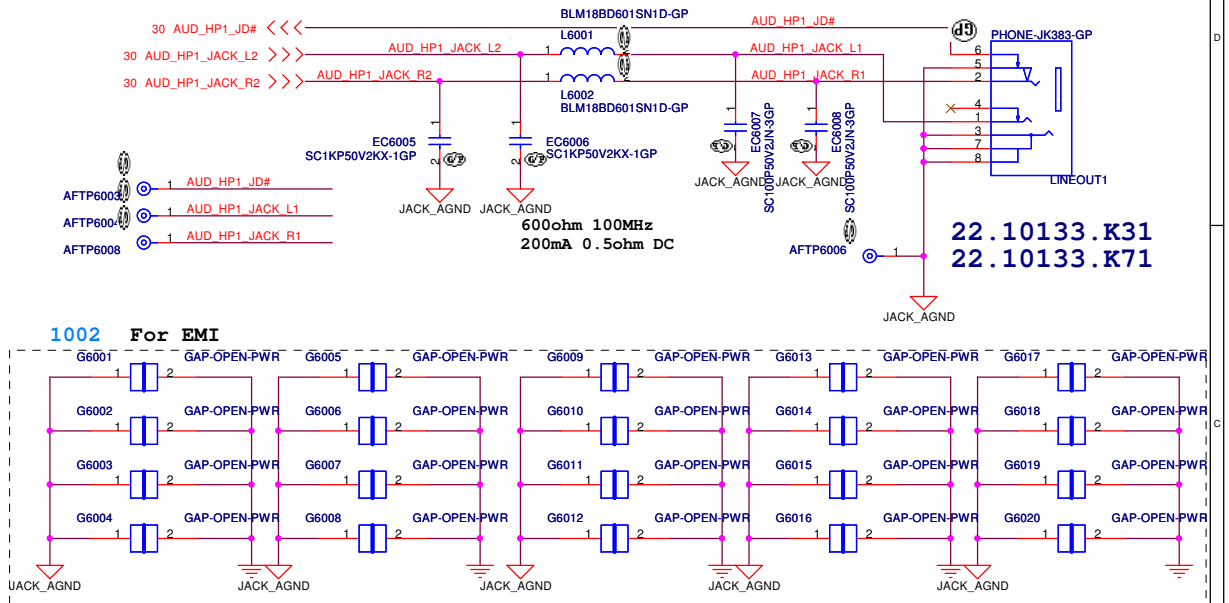
Date: Friday, May 07, 2010 Sheet 59 of 89

SSID = AUDIO

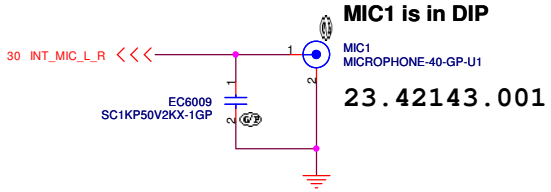
Speaker Connector



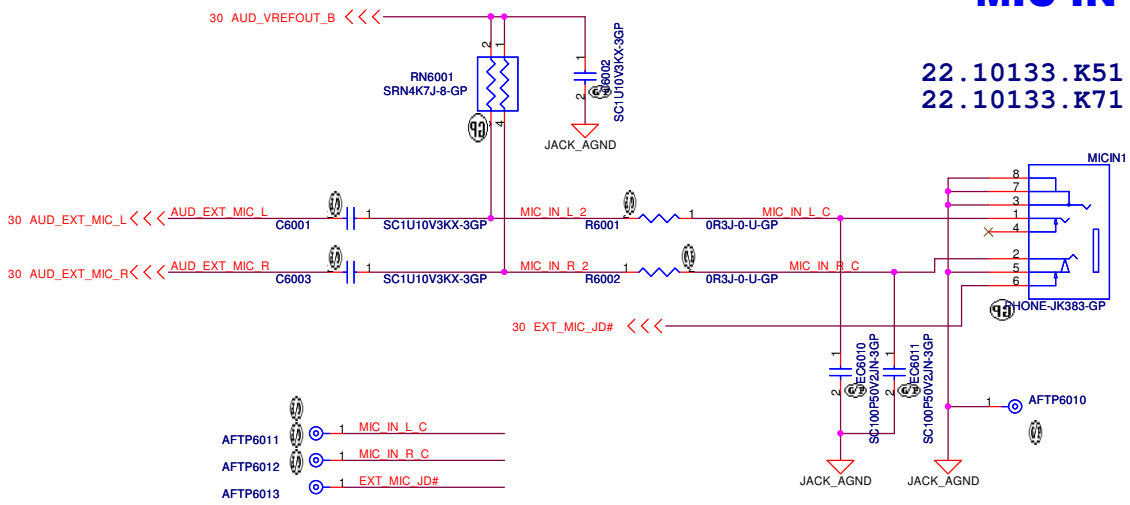
LINE1 OUT



Internal Microphone



MIC IN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio Jack	
Size A3	Document Number Arsenal DJ1 Discrete	Rev X01
Date: Friday, May 07, 2010	Sheet 60 of 89	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

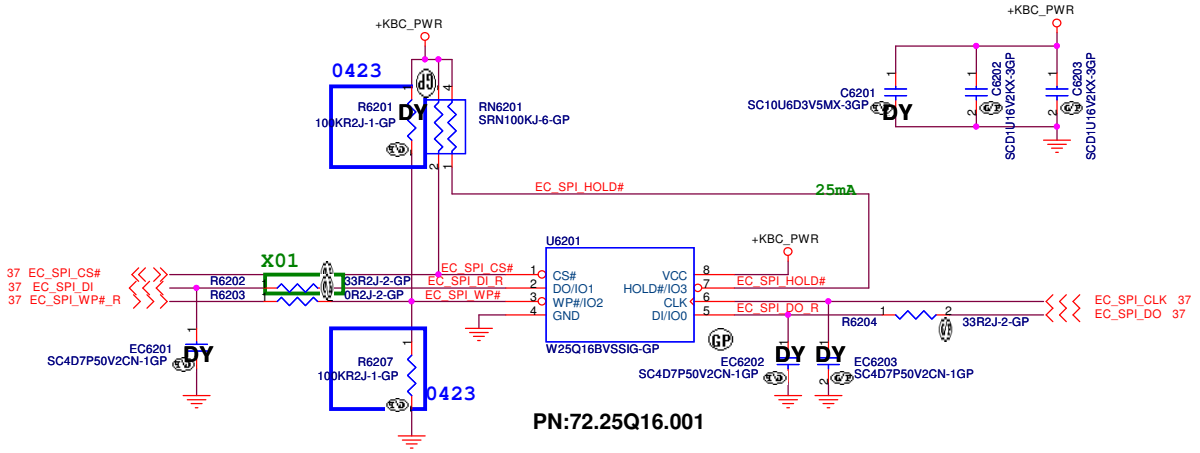
Reserved

Size	Document Number	Rev
A3	***Arsenal DJ1 Discrete***	***X01***

Date: Friday, May 07, 2010 Sheet 61 of 89

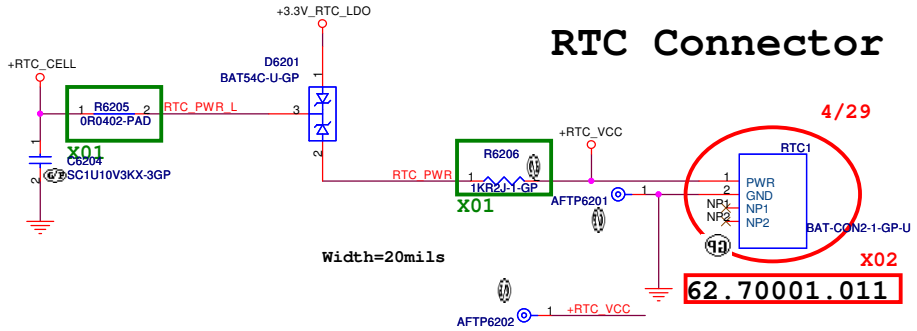
SSID = Flash.ROM

SPI FLASH ROM (16M bits) for KBC



SSID = RBATT

RTC Connector



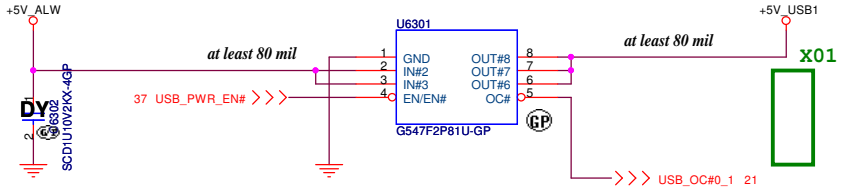
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

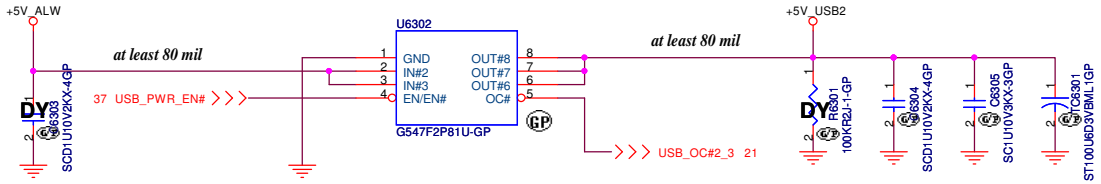
Title		
Flash/RTC		
Size: A3	Document Number: Arsenal DJ1 Discrete	Rev: X01
Date: Friday, May 07, 2010	Sheet 62 of 89	

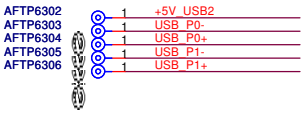
SSID = USB

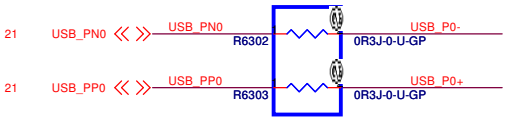
IO Board USB Power



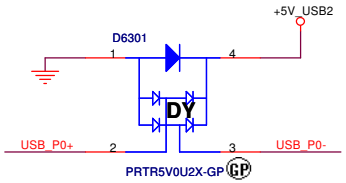
Right USB Power

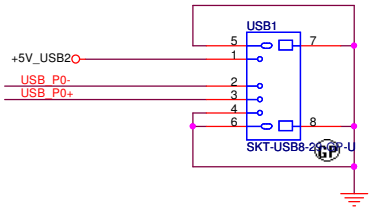




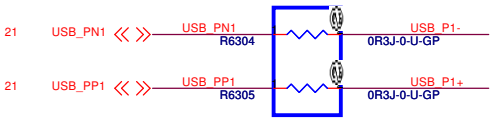


Place R6302 and R6303 together

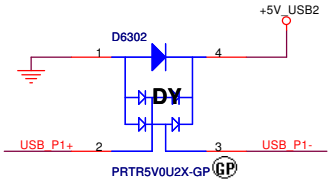


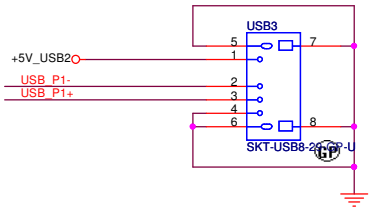


22.10254.451



Place R6304 and R6305 together





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB

Size | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 63 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD

Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 64 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

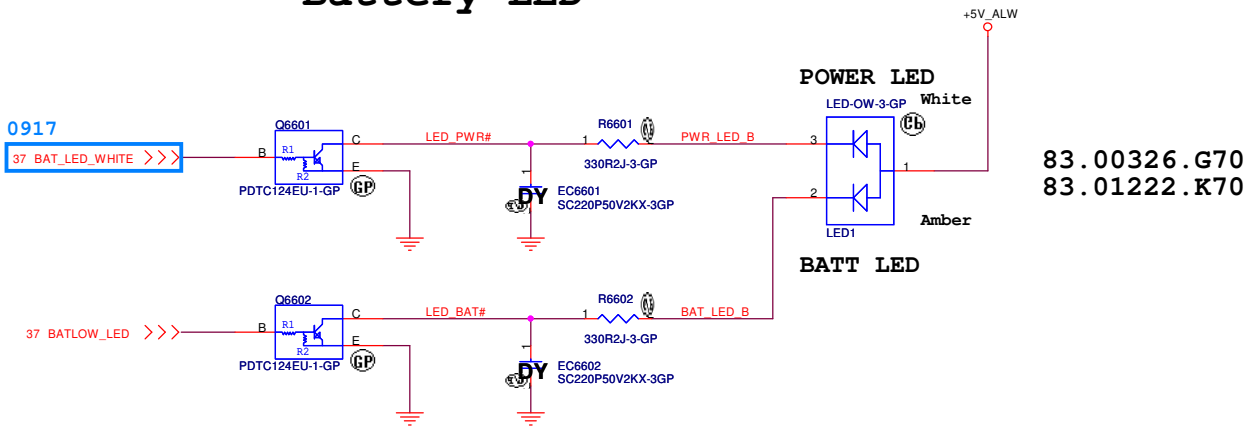
Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 65 of 89

SSID = User.Interface

Battery LED

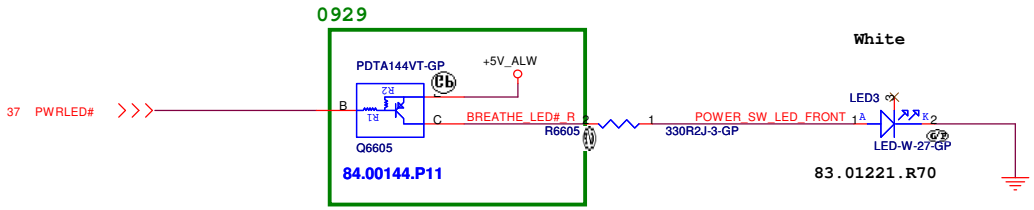


83.00326.G70
83.01222.K70

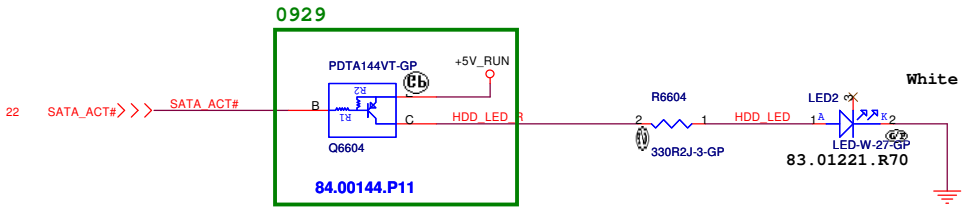
Power button LED

0907

BREATHE PWR LED (Front)



HDD LED



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED		
Size: A3	Document Number: Arsenal DJ1 Discrete	Rev: X01
Date: Friday, May 07, 2010	Sheet 66 of 89	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

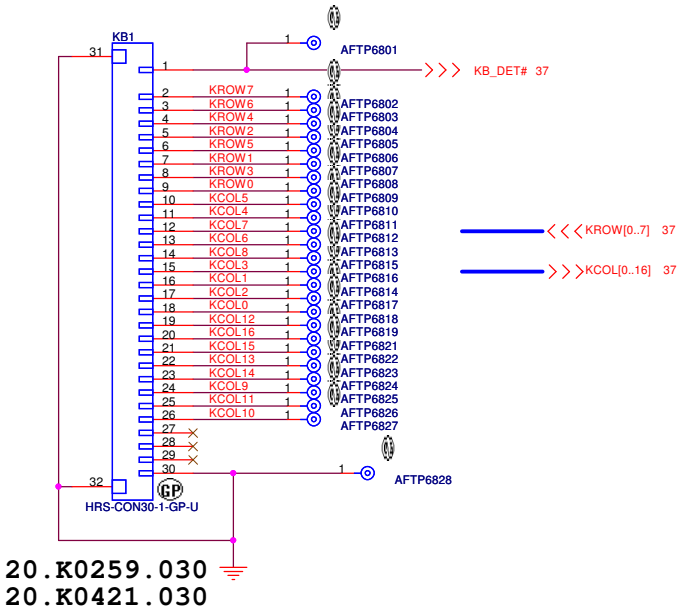
Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 67 of 89

SSID = KBC

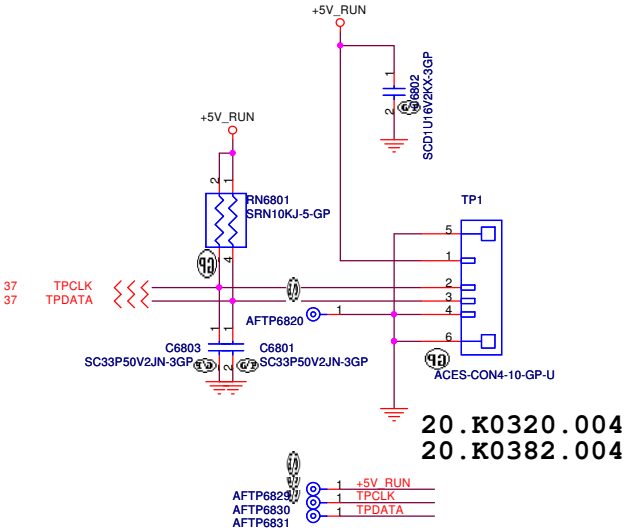
Internal KeyBoard Connector



20.K0259.030
20.K0421.030

SSID = Touch.Pad

TouchPad Connector

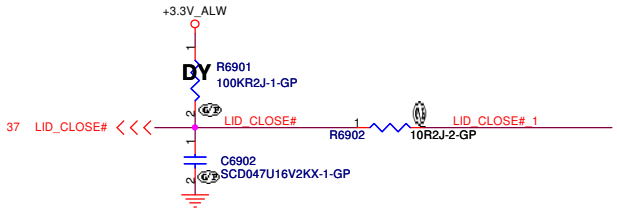


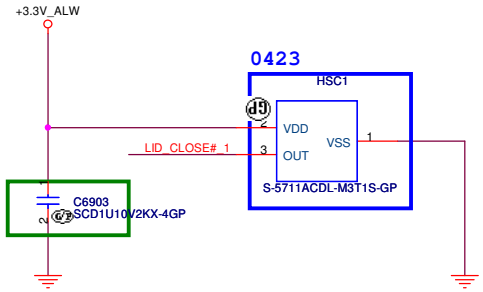
20.K0320.004
20.K0382.004

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad		
Size: A3	Document Number: Arsenal DJ1 Discrete	Rev: X01
Date: Friday, May 07, 2010	Sheet 68 of 89	





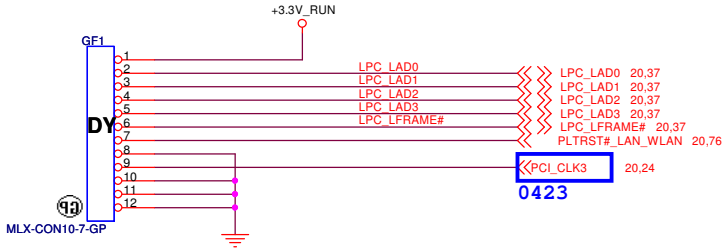
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Hall Sensor

Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 69 of 89



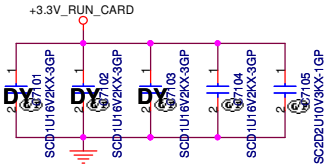
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

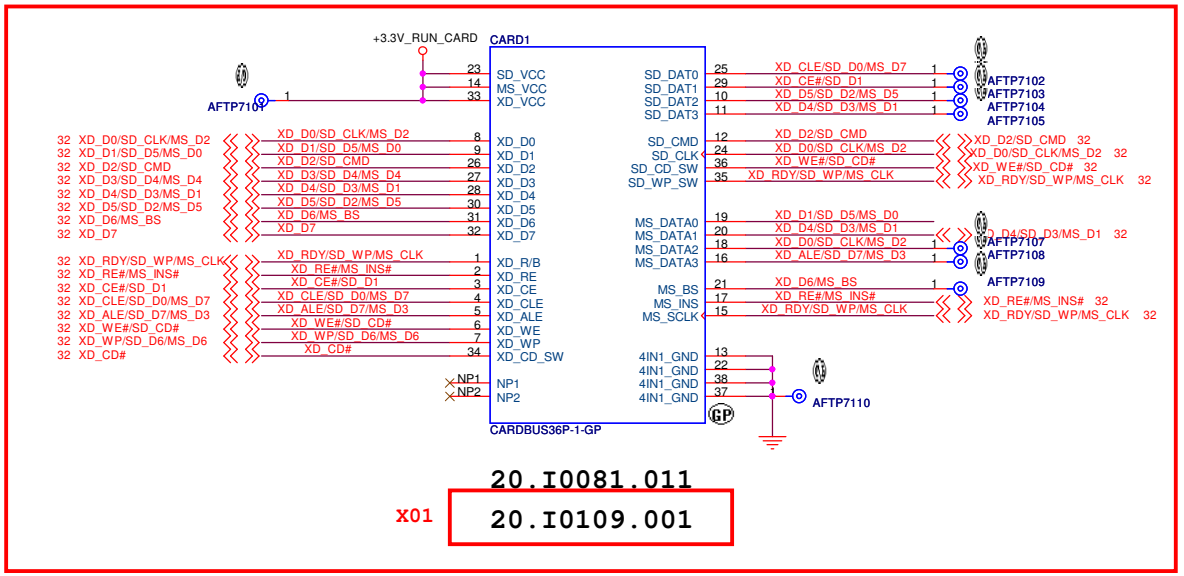
Title	***Reserved***	
Size: A3	Document Number: ***Arsenal DJ1 Discrete***	Rev: ***X01***
Date: Friday, May 07, 2010	Sheet 70 of 89	

SSID = SDIO

SD/XD/MS Card Reader

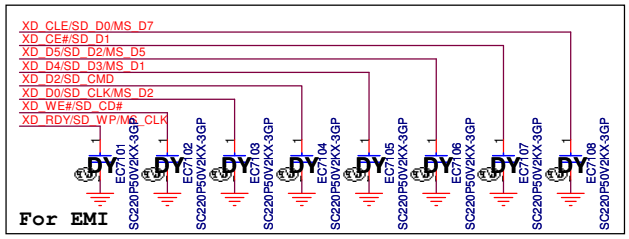


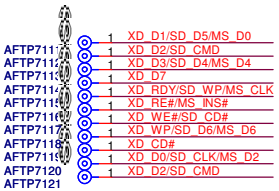
0430



20.I0081.011

X01 20.I0109.001





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 71 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

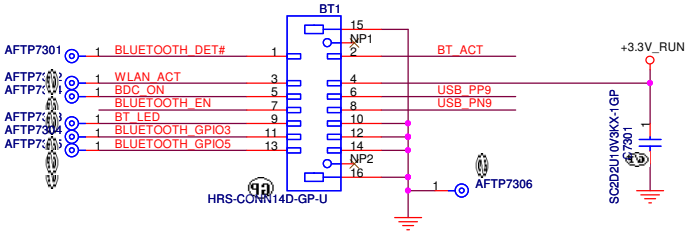
RESERVED

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*X01*

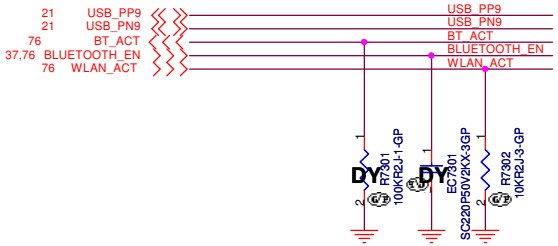
Date: Friday, May 07, 2010 Sheet 72 of 89

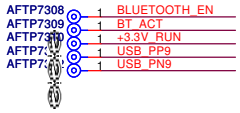
SSID = User.Interface

Bluetooth Module conn.



20.F0987.014
20.F1500.014





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth		
Size: A3	Document Number: Arsenal DJ1 Discrete	Rev: X01
Date: Friday, May 07, 2010	Sheet 73 of 89	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 74 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

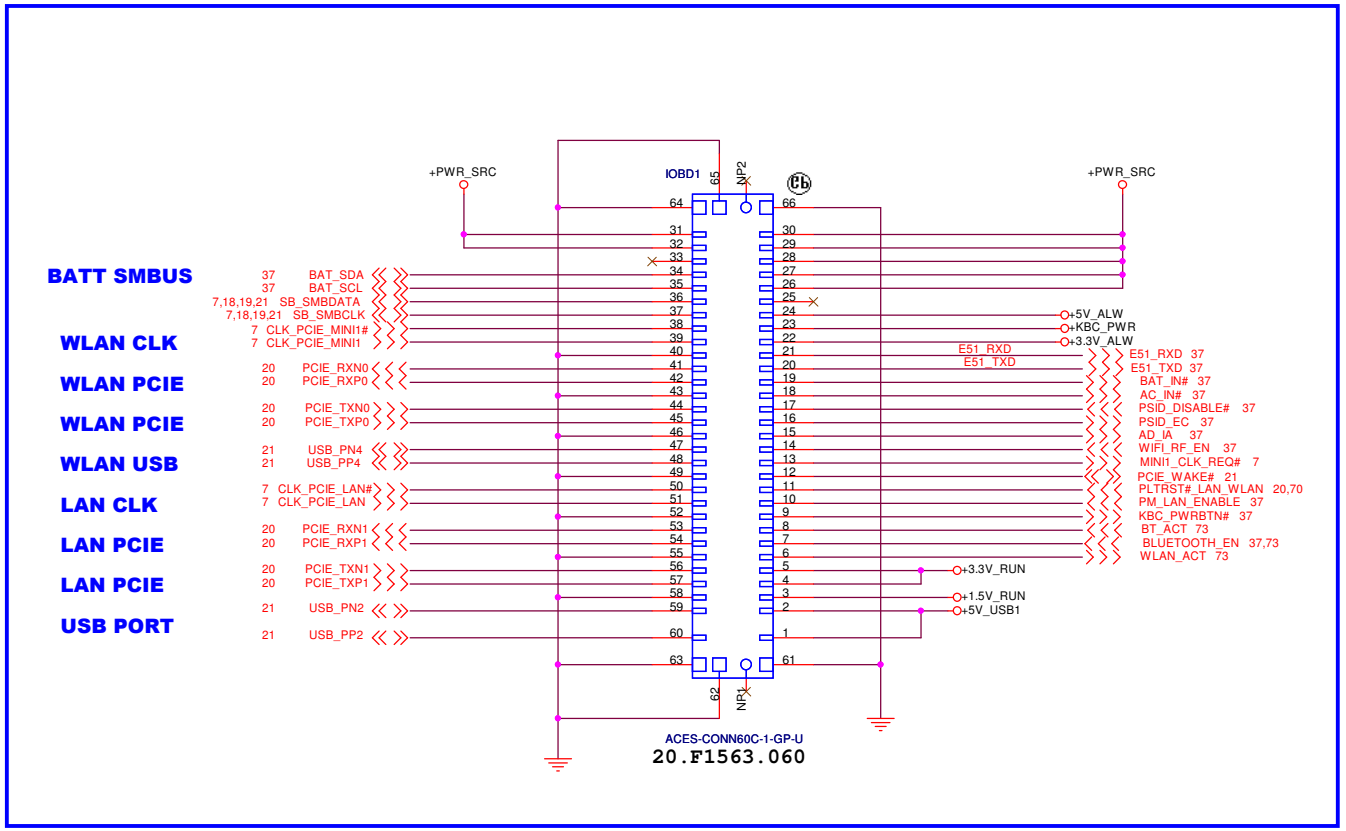
Reserved

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*X01*

Date: Friday, May 07, 2010 Sheet 75 of 89

SSID = PWR.Support

0423



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 76 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*X01*

Date: Friday, May 07, 2010 Sheet 77 of 89

(Blanking)

<Core Design>

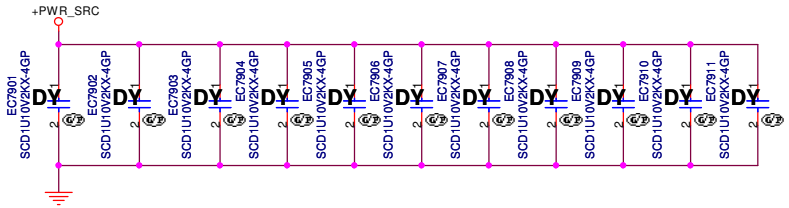
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

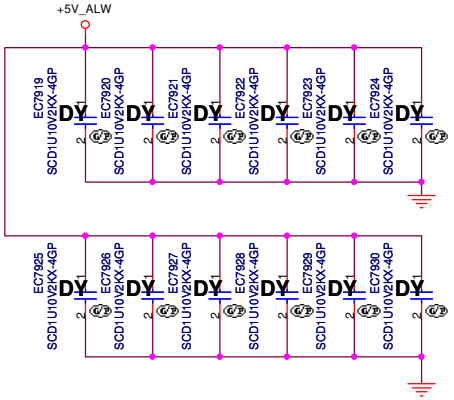
Title: *Reserved*

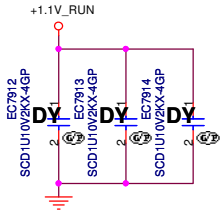
Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

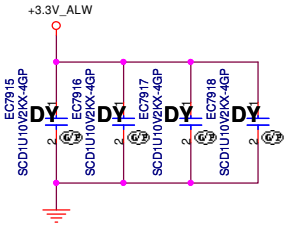
Date: Friday, May 07, 2010 | Sheet 78 of 89

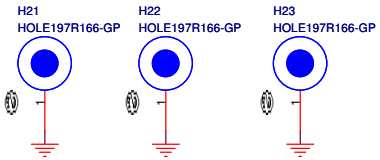
SSID = Mechanical

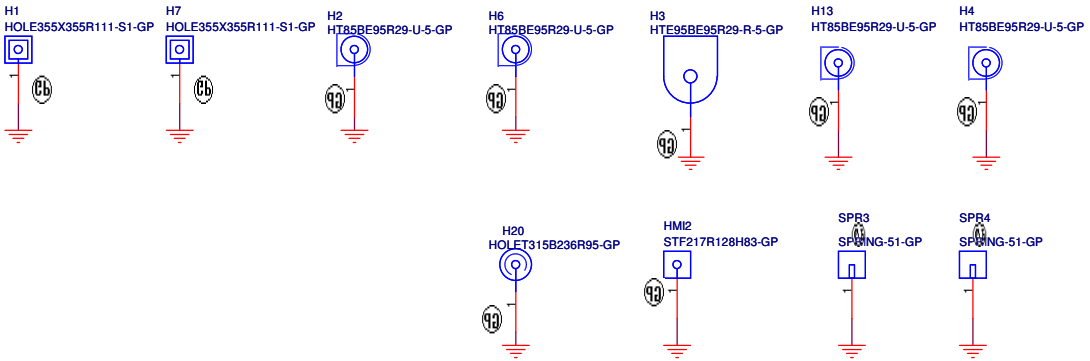












<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A3	Arsenal DJ1 Discrete	X01

Date: Friday, May 07, 2010 Sheet 79 of 89

SSID = VIDEO

PCIE_NTX_GRX_P[0..15] → PCIE_NTX_GRX_P[0..15] 12
PCIE_NTX_GRX_N[0..15] → PCIE_NTX_GRX_N[0..15] 12
PCIE_NRX_GTX_P[0..15] → PCIE_NRX_GTX_P[0..15] 12
PCIE_NRX_GTX_N[0..15] → PCIE_NRX_GTX_N[0..15] 12

U80A 1 OF 7

PCI EXPRESS INTERFACE

PCIE_NTX_GRX_P15	AF30	PCIE_RX0P	PCIE_TX0P	AH30	PCIE_NRX_GTX_C_P15	C8001	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P15
PCIE_NTX_GRX_N15	AE31	PCIE_RX0N	PCIE_TX0N	AG31	PCIE_NRX_GTX_C_N15	C8002	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N15
PCIE_NTX_GRX_P14	AE29	PCIE_RX1P	PCIE_TX1P	AG29	PCIE_NRX_GTX_C_P14	C8003	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P14
PCIE_NTX_GRX_N14	AD28	PCIE_RX1N	PCIE_TX1N	AF28	PCIE_NRX_GTX_C_N14	C8004	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N14
PCIE_NTX_GRX_P13	AD30	PCIE_RX2P	PCIE_TX2P	AF27	PCIE_NRX_GTX_C_P13	C8005	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P13
PCIE_NTX_GRX_N13	AC31	PCIE_RX2N	PCIE_TX2N	AF26	PCIE_NRX_GTX_C_N13	C8006	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N13
PCIE_NTX_GRX_P12	AC29	PCIE_RX3P	PCIE_TX3P	AD27	PCIE_NRX_GTX_C_P12	C8007	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P12
PCIE_NTX_GRX_N12	AB28	PCIE_RX3N	PCIE_TX3N	AD26	PCIE_NRX_GTX_C_N12	C8008	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N12
PCIE_NTX_GRX_P11	AB30	PCIE_RX4P	PCIE_TX4P	AC25	PCIE_NRX_GTX_C_P11	C8009	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P11
PCIE_NTX_GRX_N11	AA31	PCIE_RX4N	PCIE_TX4N	AB25	PCIE_NRX_GTX_C_N11	C8010	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N11
PCIE_NTX_GRX_P10	AA29	PCIE_RX5P	PCIE_TX5P	Y23	PCIE_NRX_GTX_C_P10	C8011	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P10
PCIE_NTX_GRX_N10	Y28	PCIE_RX5N	PCIE_TX5N	Y24	PCIE_NRX_GTX_C_N10	C8012	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N10
PCIE_NTX_GRX_P9	Y30	PCIE_RX6P	PCIE_TX6P	AB27	PCIE_NRX_GTX_C_P9	C8013	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P9
PCIE_NTX_GRX_N9	W31	PCIE_RX6N	PCIE_TX6N	AB26	PCIE_NRX_GTX_C_N9	C8014	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N9
PCIE_NTX_GRX_P8	W29	PCIE_RX7P	PCIE_TX7P	Y27	PCIE_NRX_GTX_C_P8	C8015	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P8
PCIE_NTX_GRX_N8	V28	PCIE_RX7N	PCIE_TX7N	Y26	PCIE_NRX_GTX_C_N8	C8016	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N8
PCIE_NTX_GRX_P7	V30	PCIE_RX8P	PCIE_TX8P	W24	PCIE_NRX_GTX_C_P7	C8017	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P7
PCIE_NTX_GRX_N7	U31	PCIE_RX8N	PCIE_TX8N	W23	PCIE_NRX_GTX_C_N7	C8018	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N7
PCIE_NTX_GRX_P6	U29	PCIE_RX9P	PCIE_TX9P	V27	PCIE_NRX_GTX_C_P6	C8019	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P6
PCIE_NTX_GRX_N6	T28	PCIE_RX9N	PCIE_TX9N	U26	PCIE_NRX_GTX_C_N6	C8020	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N6
PCIE_NTX_GRX_P5	T30	PCIE_RX10P	PCIE_TX10P	U24	PCIE_NRX_GTX_C_P5	C8021	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P5
PCIE_NTX_GRX_N5	R31	PCIE_RX10N	PCIE_TX10N	U23	PCIE_NRX_GTX_C_N5	C8022	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N5
PCIE_NTX_GRX_P4	R29	PCIE_RX11P	PCIE_TX11P	T26	PCIE_NRX_GTX_C_P4	C8023	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P4
PCIE_NTX_GRX_N4	P28	PCIE_RX11N	PCIE_TX11N	T27	PCIE_NRX_GTX_C_N4	C8024	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N4
PCIE_NTX_GRX_P3	P30	PCIE_RX12P	PCIE_TX12P	T24	PCIE_NRX_GTX_C_P3	C8025	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P3
PCIE_NTX_GRX_N3	N31	PCIE_RX12N	PCIE_TX12N	T23	PCIE_NRX_GTX_C_N3	C8026	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N3
PCIE_NTX_GRX_P2	N29	PCIE_RX13P	PCIE_TX13P	P27	PCIE_NRX_GTX_C_P2	C8027	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P2
PCIE_NTX_GRX_N2	M28	PCIE_RX13N	PCIE_TX13N	P26	PCIE_NRX_GTX_C_N2	C8028	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N2
PCIE_NTX_GRX_P1	M30	PCIE_RX14P	PCIE_TX14P	P24	PCIE_NRX_GTX_C_P1	C8029	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P1
PCIE_NTX_GRX_N1	L31	PCIE_RX14N	PCIE_TX14N	P23	PCIE_NRX_GTX_C_N1	C8030	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N1
PCIE_NTX_GRX_P0	L29	PCIE_RX15P	PCIE_TX15P	M27	PCIE_NRX_GTX_C_P0	C8031	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_P0
PCIE_NTX_GRX_N0	K30	PCIE_RX15N	PCIE_TX15N	N26	PCIE_NRX_GTX_C_N0	C8032	1	SCD1U16V2KX-3GP	PCIE_NRX_GTX_N0

CLOCK

7 CLK_PCIE_VGA → CLK_PCIE_VGA AK30 → PCIE_REFCLKP
7 CLK_PCIE_VGA# → CLK_PCIE_VGA# AK32 → PCIE_REFCLKN

M92/Park Switch

PARK
R8002 1 — 10KR2F-2-GP — PWRGOOD
L9 DVCNTL_1
N9 DVCNTL_2
N10 NC_PWRGOOD

37 PLTRST_DELAY# → PLTRST_DELAY# AL27 → PERSTB

CALIBRATION

PCIE_CALRP Y22 — PCIE_CALRP — R8001 1 — 1K27R2F-L-GP
PCIE_CALRN AA22 — PCIE_CALRN — R8003 1 — 2KR2F-3-GP — +1.1V_GFX_RUN

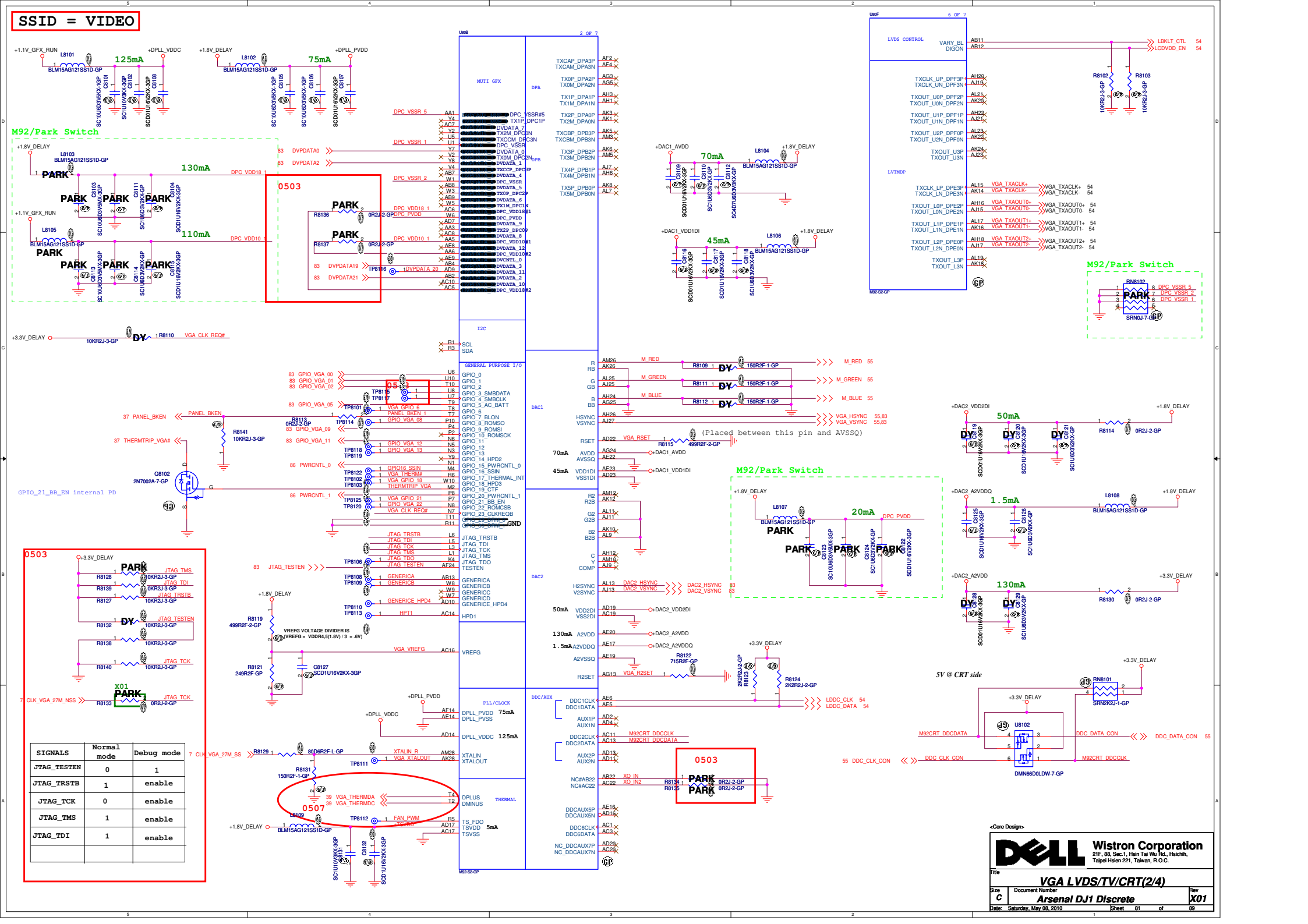
M92-S2-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA PCIE(1/4)
Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: X01
Date: Friday, May 07, 2010 | Sheet 80 of 89

SSID = VIDEO



SIGNALS	Normal mode	Debug mode
JTAG_TESTEN	0	1
JTAG_TRSTB	1	enable
JTAG_TCK	0	enable
JTAG_TMS	1	enable
JTAG_TDI	1	enable

SSID = VIDEO

M92/Park Switch

M92/Park Switch

PARK-S3:120mA@1.0V
M92-S2:170mA@1.1V

PARK-S3:120mA@1.0V
M92-S2:170mA@1.1V

PARK-S3:110mA@1.0V
M92-S2:200mA@1.1V

PARK-S3:110mA@1.0V
M92-S2:200mA@1.1V

Y11 pin--DVCLK (not use)
Y12 pin--VDDR4
U11 pin--NC
U12 pin--VDDR4
V11 pin--NC
V12 pin--VDDR4
AA11 pin--NC
AA12 pin--NC
PARK S3

M92 USE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA POWER/GND(3/4)

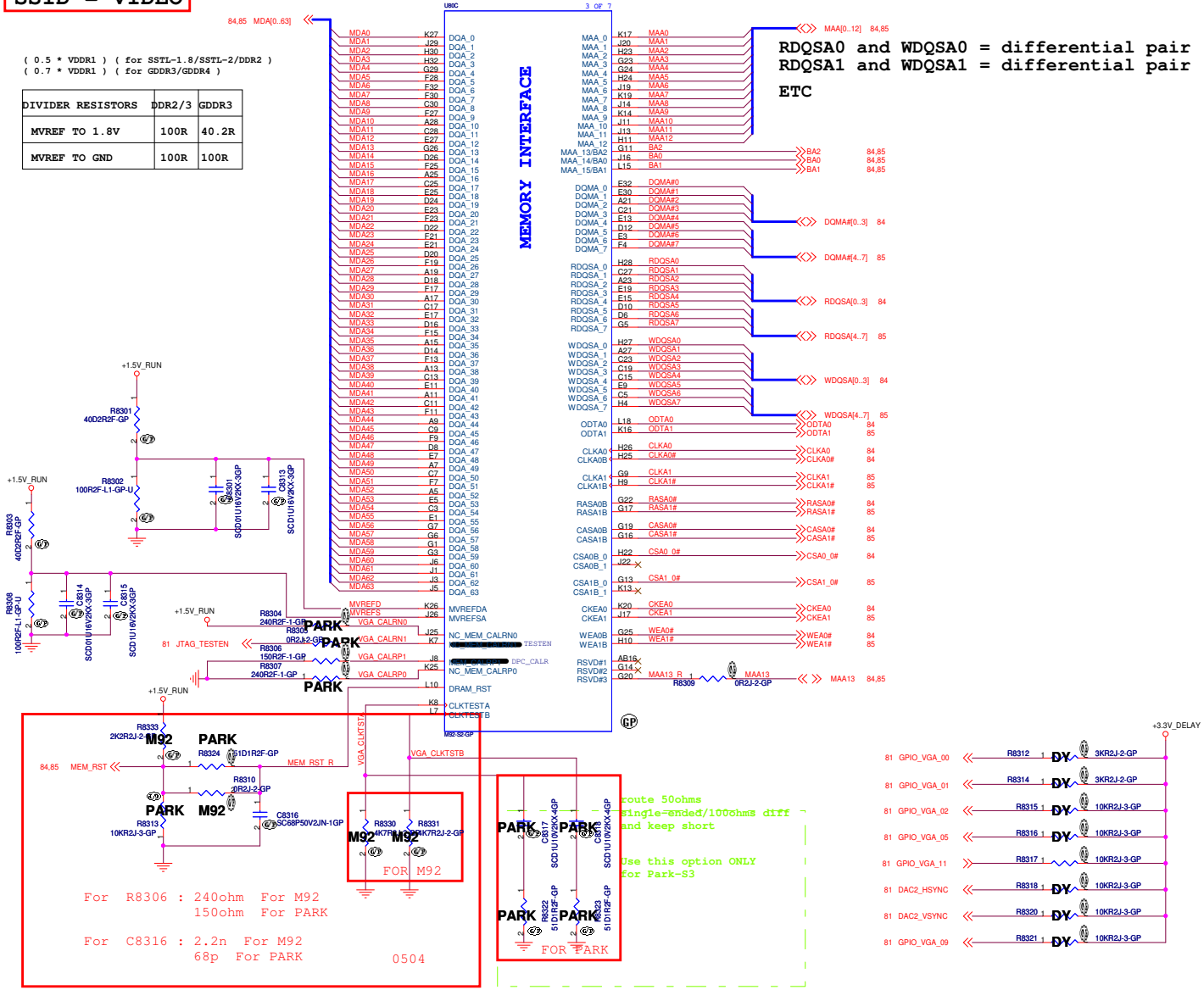
Size: A2 | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 82 of 89

SSID = VIDEO

(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)

DIVIDER RESISTORS	DDR2/3	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

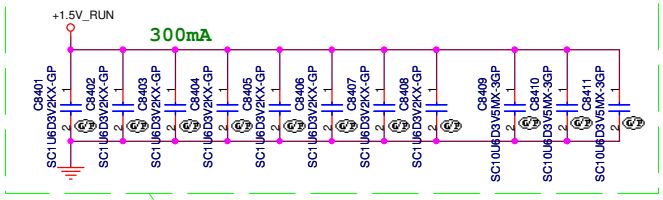
If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
V 256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO_VGA_00	Tansmitter Power Savings Enable V 0= 50% Tx output swing 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO_VGA_01	Transmitter De-emphasis Enable V 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO_VGA_02	V 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type V if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] V 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI
VGA_DIS (Internal PD)	GPIO_VGA_09	V 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller

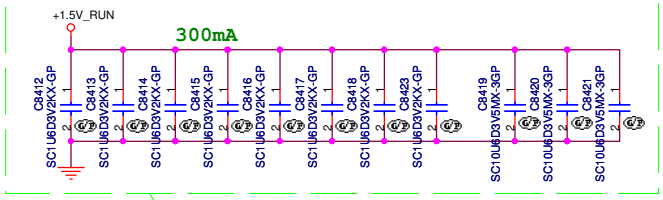
STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(19,21,2,0) (Internal PD)	MEMORY TYPE,MAKE AND SIZE INFO V 0000 – gDDR3 64Mx16 Hynix 0001 – gDDR3 64Mx16 Samsung 0010 – gDDR3 128Mx16 Hynix 0011 – gDDR3 128Mx16 Samsung

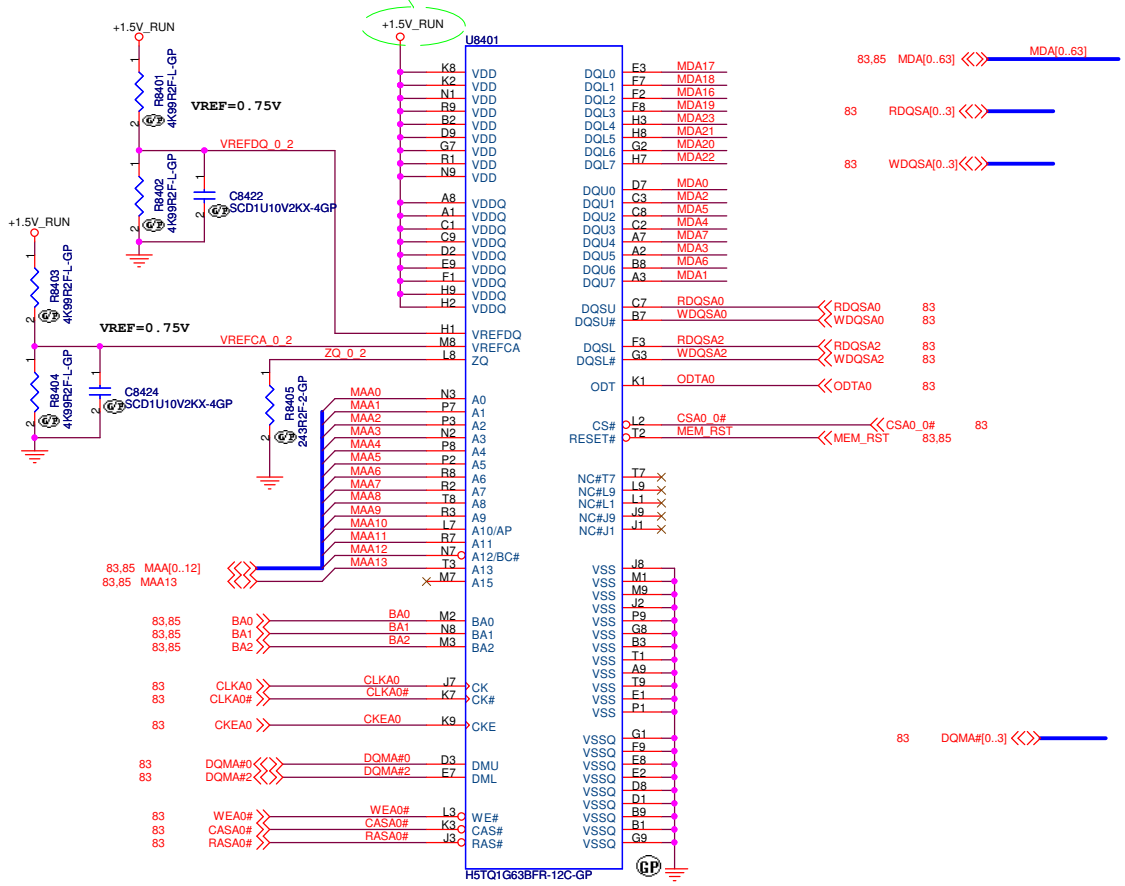
SSID = VIDEO

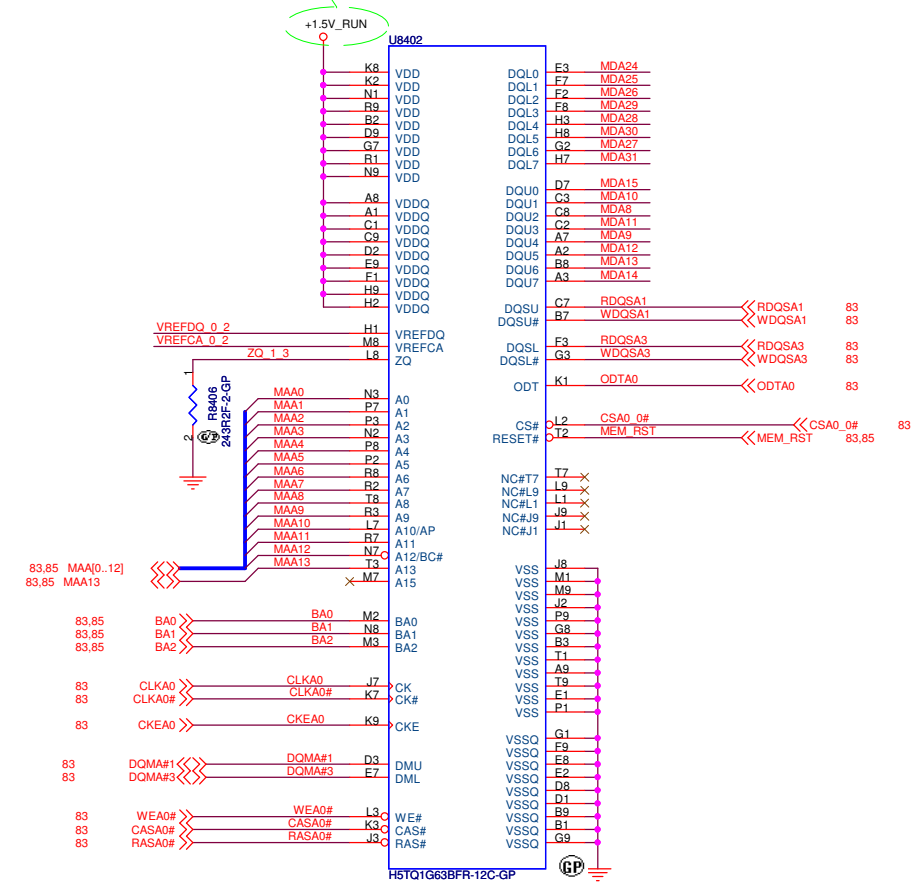
Place blow decouping caps close VDD pin.

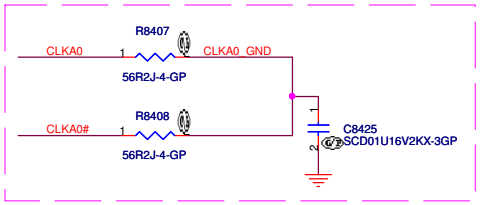


Place blow decouping caps close VDD pin.









<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

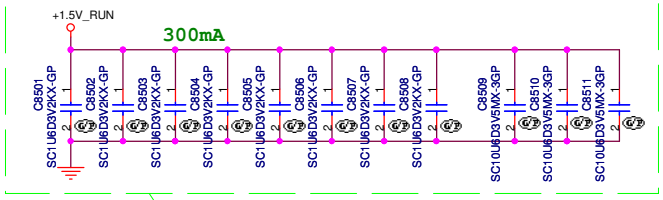
Title: GPU-VRAM (1/2)

Size	Document Number	Rev
Custom	Arsenal DJ1 Discrete	X01

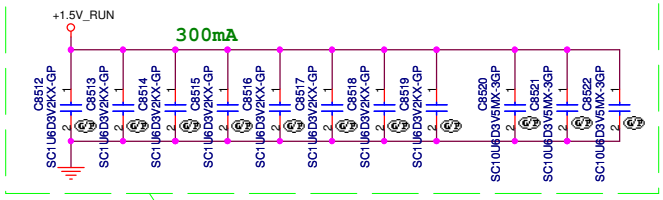
Date: Friday, May 07, 2010 Sheet 84 of 89

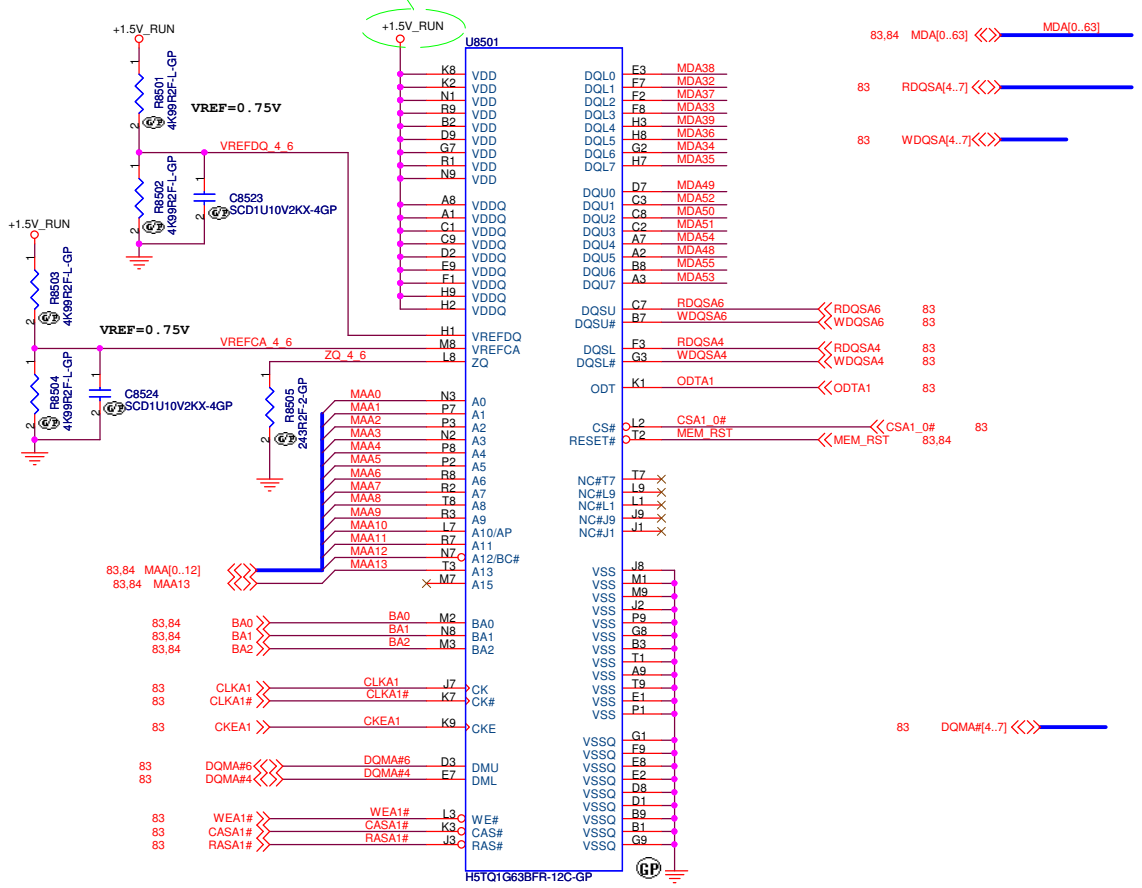
SSID = VIDEO

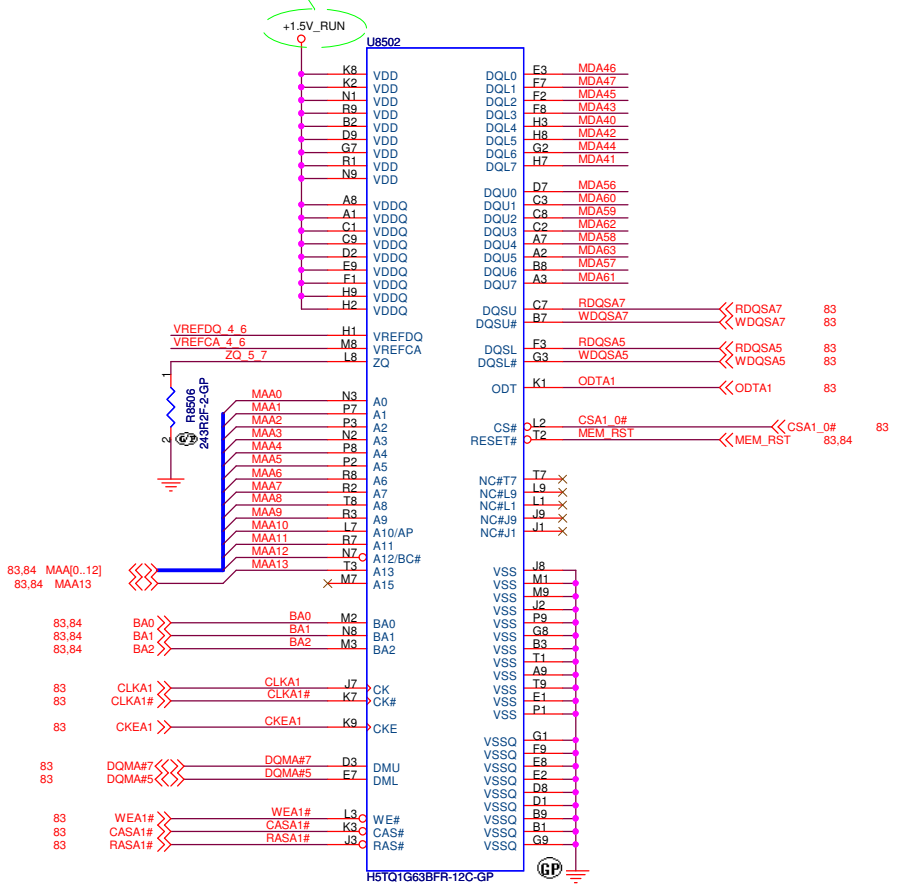
Place blow decouping caps close VDD pin.

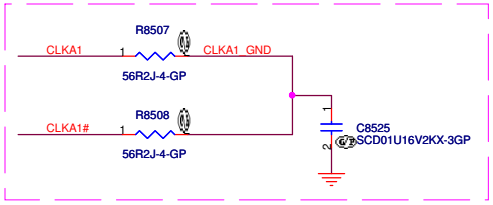


Place blow decouping caps close VDD pin.









<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

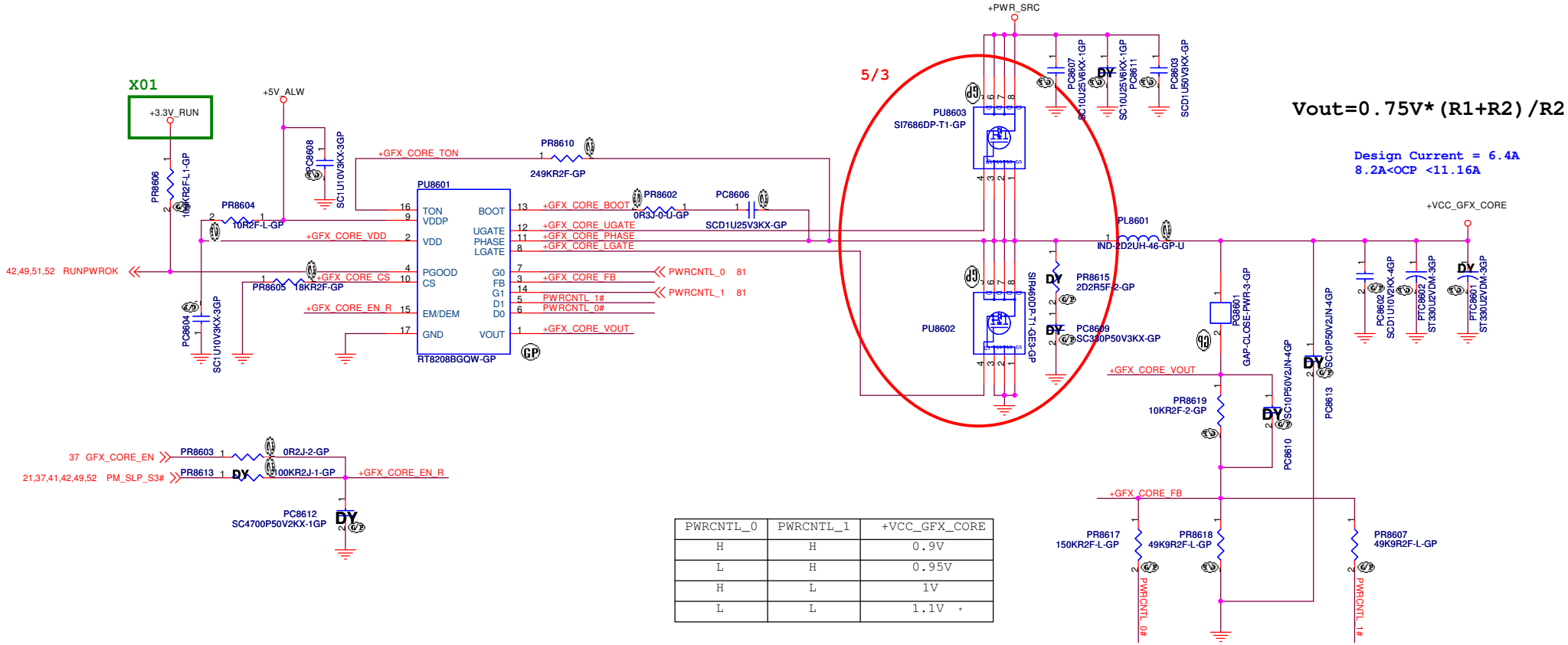
Title: GPU-VRAM (2/2)

Size: Custom | Document Number: Arsenal DJ1 Discrete | Rev: X01

Date: Friday, May 07, 2010 | Sheet 85 of 89

SSID = Video.PWR.Regulator

RT8208BGQW for +VCC_GFX_CORE



PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	0.9V
L	H	0.95V
H	L	1V
L	L	1.1V *

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH PCMC063T-2R2MN Cyntec DCR:18/20mohm Isat =14.5Arms 68.2R210.20B
O/P cap: 330U 2.5VEEFCX0D331R 15mOhm 2.7Arms Panasonic/ 79.33719.20D
H/S: FDS8880 9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mOhm/7.25mOhm@4.5Vgs/ 84.06676.A37

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208_+VCC_GFXCORE
Size: A3
Document Number: Arsenal DJ1 Discrete
Rev: X01
Date: Friday, May 07, 2010
Sheet 86 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
APL5930_+1.1V_RUN

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*X01*

Date: Friday, May 07, 2010 Sheet 87 of 89

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: Custom | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 88 of 89

Change notes – Page 1

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
11/06	X01	1	51	PU5101 +1.5V_SUS and +5V_ALW change	power plane change	EE
		2	81	Change R8133 form 10KΩ to 0Ω	GPU 27MHz to JTAG_CLK	EE
		3	7 81	Change R713 from 33Ω to 47Ω. Change R8129 from 124Ω to 80.6Ω	Adjust GPU 27Mhz Vpp to 1.8V	EE
		4	86	pull resistor R8606 to +3.3V_RUN	aviod leakage cuurent	EE
		5	42	R4206 short	RC delay for +5V_RUN	EE
		6	42	R4207 change to 20K C4203 change to 0.1uf	RC delay for +3.3V_RUN	EE
		7	52	PR5201 change to 10K PC5207 change to 220nf	RC delay for +1.8V_RUN	EE
		8	53	PR5301 change to 1K PC5302 change to 1uf	RC delay for +2.5V_RUN	EE
		9	37	Pop R3703,R3704,D3702,D3703,Q3705,Q3703,R3705,C3717 Depop R3709, R3705,R3701	add 10mW schematic	EE
		10	51	Change PR5105 pull up from +3.3V_ALW to +3.3V_RUN	aviod leakage cuurent	EE
		11	22	Del MEM_1V5 pull up resister (RN2202)	aviod leakage cuurent	EE
		12	10	R1028 pull to +1.5V_RUN	aviod leakage current	EE
		13	7	C718,C719 change to 15pF	As crystal vendor suggest	EE
		14	49	Dummy PR4905	modify RUNPWROK PU plane	EE
		15	62	R6202 change to 33R	For SPI_DI undershoot over spec	EE
		16	62	R6206 change from 510R to 1KR	For Safty request	EE
		17	76	IOBD1 pin define modify	For ME IO BD modify	EE
		18	37	Pop R3729 and depop R3733	For PCB version change	EE
04/29						

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size: Custom | Document Number: *Arsenal DJ1 Discrete* | Rev: *X01*

Date: Friday, May 07, 2010 | Sheet 89 of 89