Enrico/Caruso 15" UMA Schematics Document
Sandy Bridge
Intel PCH
2011-06-02
REV : A00

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*		
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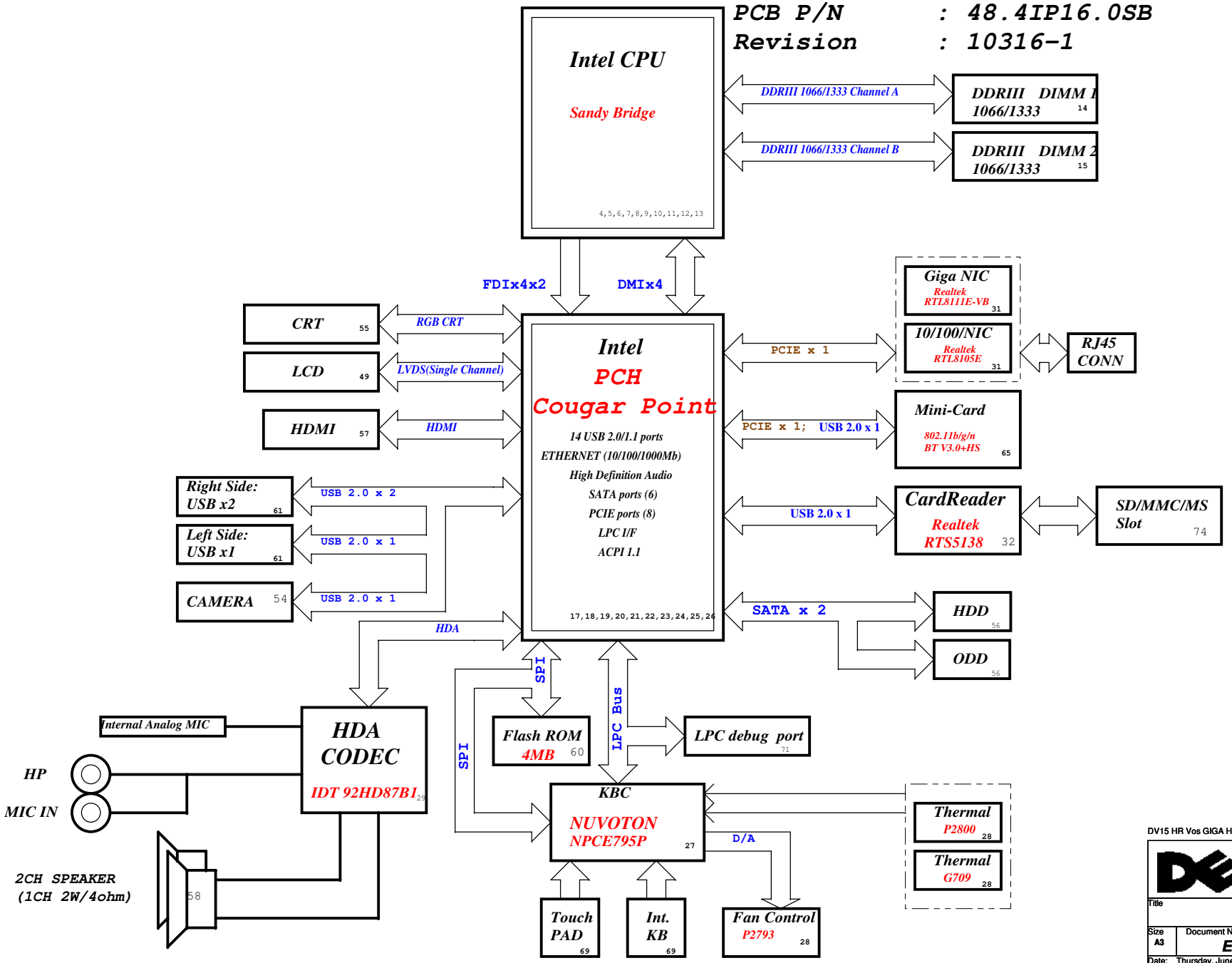
DV15 Huron River UMA Block Diagram

Project code : 91.4IP01.001
PCB P/N : 48.4IP16.0SB
Revision : 10316-1



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC ISL95831HRTZ 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

GFX DC/DC ISL95831HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC TPS51218 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51123RGER 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5

SYSTEM DC/DC TPS51216RUKR 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

MAXIM CHARGER BQ24707 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC TPS51311RGTR 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER	
L1:Top	L4:Signal
L2:GND	L5:VCC
L3:Signal	L6:Bottom

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Title: Block Diagram

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	9V-12.6V 9V-19V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	X
LANE2	Onboard LAN
LANE3	x
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	X
2	X
3	X
4	ODD1
5	X

USB Table

Pair	Device
0	X
1	USB Ext. port 1
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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Title: Table of Content

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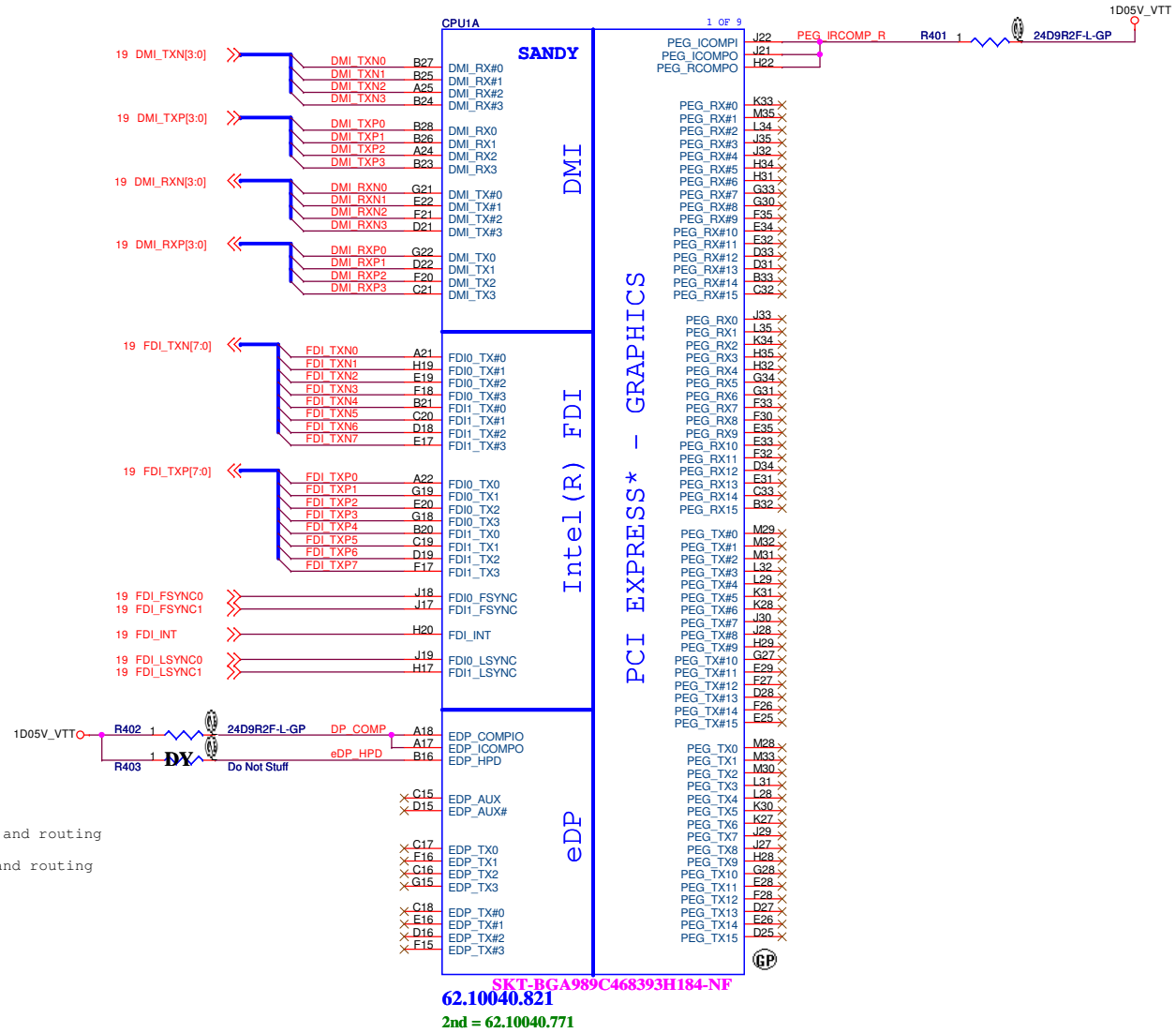
SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

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Title	CPU (PCIE/DMI/FDI)	
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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SSID = CPU

CPU1B — SANDY — 2 OF 9

MISC: SNB_IVB# (C26), SKTOCC# (AN34)
THERMAL: CATERR# (AL33), PECI (AN33), PROCHOT# (AL32), THERMTRIP# (AN32)
PWR MANAGEMENT: PM_SYNC (AM34), UNCOREPWRGOOD (AP33), SM_DRAMPWROK (V8), RESET# (AR33)
CLOCKS: BCLK (A28), BCLK# (A27)
DDR3 MISC: SM_DRAMRST# (R8), SM_RCOMP0 (AK1), SM_RCOMP1 (A5), SM_RCOMP2 (A4)
JTAG & BPM: PRDY# (AP29), PREQ# (AP27), TCK (AR26), TMS (AR27), TRST# (AP30), TDI (AR28), TDO (AP26), DBR# (AL35), BPM#0 (AT28), BPM#1 (AR29), BPM#2 (AR30), BPM#3 (AT30), BPM#4 (AP32), BPM#5 (AR31), BPM#6 (AT31), BPM#7 (AR32)

18 H_SNB_IVB#
TP501 SKTOCC# R
TP502 H_CATERR#
22,27 H_PECI
27,40,42 H_PROCHOT# — R513 56R2J-4-GP — H_PROCHOT# R
22,36 H_THERMTRIP#

1D05V_VTT — R501 62R2J-GP — H_PROCHOT# — C502 SC47P50V2JN-3GP

CRB : 47pf
CEKLT:43pf

19 H_PM_SYNC
22,36 H_CPUPWRGD — R504 Do Not Stuff — H_CPUPWRGD_R
R503 10KR2J-3-GP
19,37 PM_DRAM_PWRGD — R505 DY Do Not Stuff — VDDPWRGOOD
37 VDDPWRGOOD
18,27,31,65,71 PLT_RST# — R510 1K5R2F-2-GP — BUF_CPU_RST#
R509 750R2F-GP
C501 DY Do Not Stuff

SKT-BGA989C468393H184-NF
62.10040.821
2nd = 62.10040.771

BCLK A28 — CLK_EXP_P 20
BCLK# A27 — CLK_EXP_N 20
DPLL_REF_SSCLK A16 — CLK_DP_P_R — R512 1KR2J-1-GP
DPLL_REF_SSCLK# A15 — CLK_DP_N_R — R514 1KR2J-1-GP — 1D05V_VTT

SM_DRAMRST# R8 — R502 4K99R2F-L-GP — SM_DRAMRST# 37

SM_RCOMP0 AK1 — SM_RCOMP_0 — R506 140R2F-GP
SM_RCOMP1 A5 — SM_RCOMP_1 — R507 25D5R2F-GP
SM_RCOMP2 A4 — SM_RCOMP_2 — R508 200R2F-L-GP

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

PRDY# AP29 — XDP_PRDY# — TP511
PREQ# AP27 — XDP_PREQ# — TP512
TCK AR26 — XDP_TCLK
TMS AR27 — XDP_TMS
TRST# AP30 — XDP_TRST#
TDI AR28 — XDP_TDI
TDO AP26 — XDP_TDO
DBR# AL35 — XDP_DBRESET#

BPM#0 AT28 — XDP_BPM0 — TP503
BPM#1 AR29 — XDP_BPM1 — TP504
BPM#2 AR30 — XDP_BPM2 — TP505
BPM#3 AT30 — XDP_BPM3 — TP506
BPM#4 AP32 — XDP_BPM4 — TP507
BPM#5 AR31 — XDP_BPM5 — TP508
BPM#6 AT31 — XDP_BPM6 — TP509
BPM#7 AR32 — XDP_BPM7 — TP510

1D05V_VTT — RN501 SRN51J-1-GP
XDP_TDO
XDP_TMS
XDP_TDI
XDP_TCLK
XDP_TRST# — R511 51R2J-2-GP

3D3V_S0
19 XDP_DBRESET# — XDP_DBRESET# — R516 10KR2J-3-GP

Buffered reset to CPU

1D05V_VTT — R518 DY Do Not Stuff
3D3V_S0 — C503 DY Do Not Stuff
U501 (IN B, VCC, IN A, GND, OUT Y)
18,27,31,65,71 PLT_RST#
BUFO_CPU_RST# — R517 DY Do Not Stuff — BUF_CPU_RST#
R515 DY Do Not Stuff
Do Not Stuff
Do Not Stuff

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Title: CPU (THERMAL/CLOCK/PM)
Size: A3
Document Number: Enrico/Caruso 15 HR
Rev: X01
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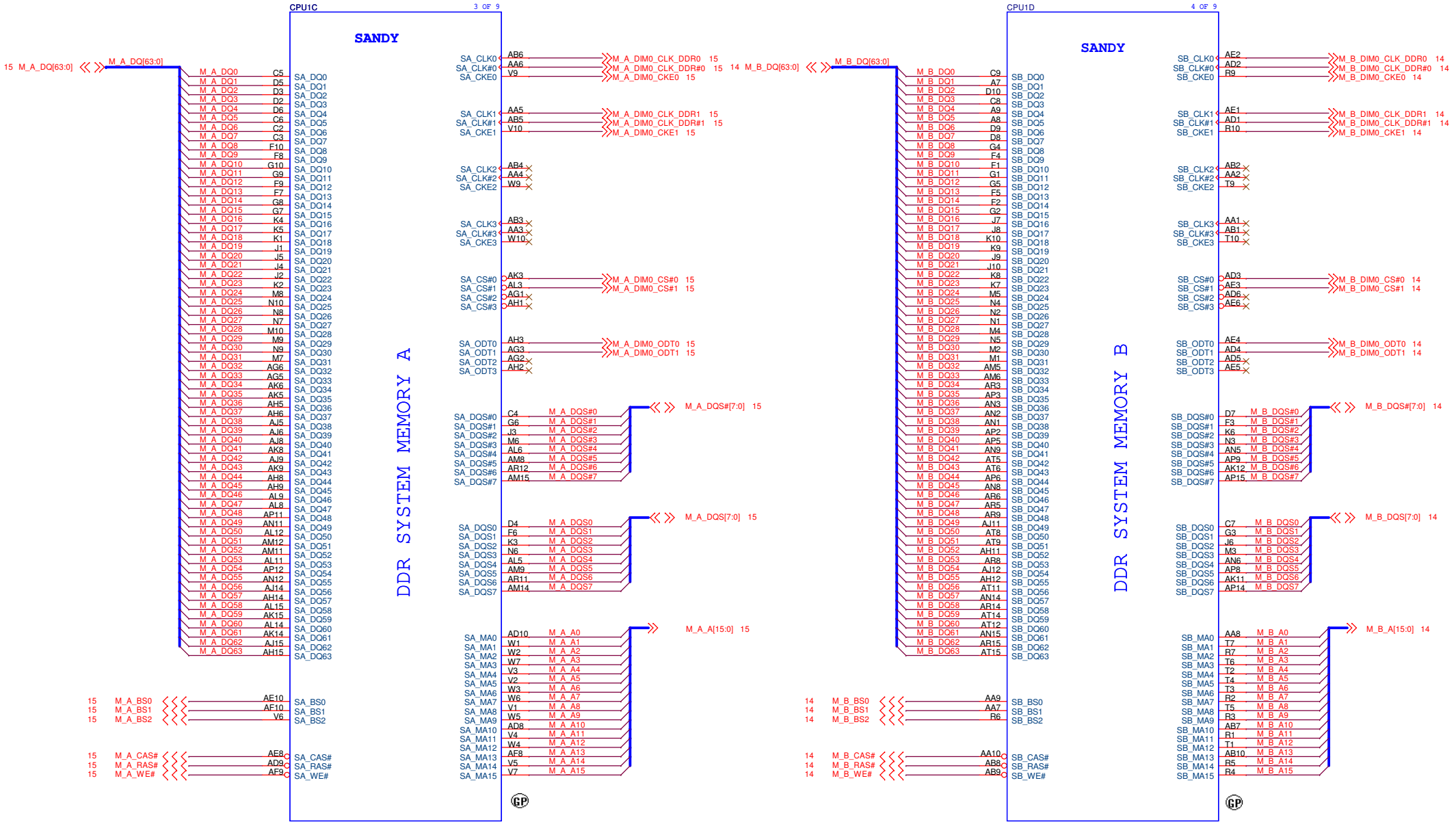
SSID = CPU



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Title: *CPU (DDR)*

Size: A3 | Document Number: Enrico/Caruso 15 HR | Rev: X01

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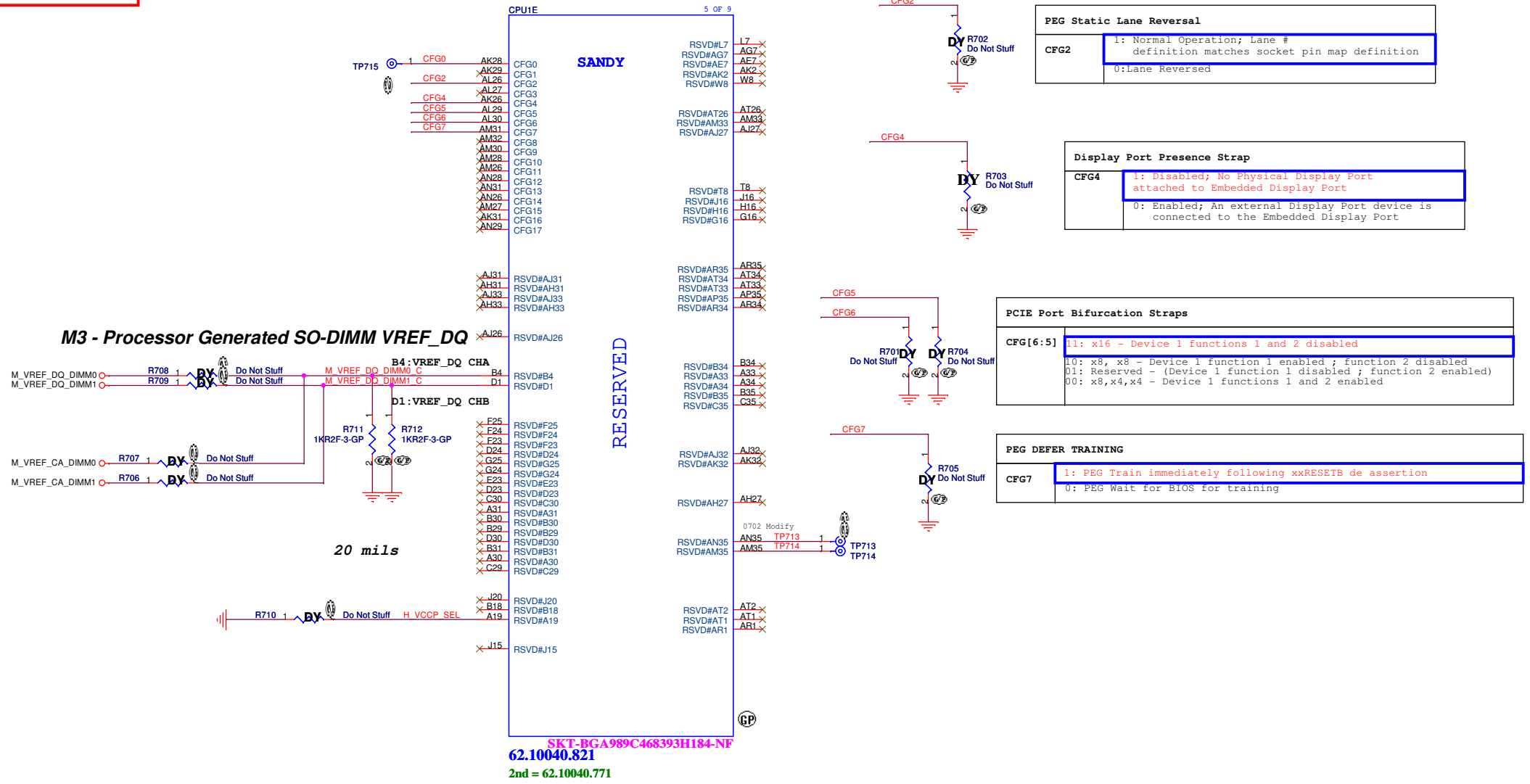
SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

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SSID = CPU

POWER

CPU1F

SANDY

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PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

PROCESSOR CORE POWER

VCC_CORE

53A

C809 C810 C816 C817 C819 C820 C821 C825 C826 C827 C831 C832 C833 C834 C835 C837 — SC10U6D3V5MX-GP / SC22U6D3V5MX-2GP / SC10U6D3V5KX-1GP

PROCESSOR VCCIO: 8.5A

1D05V_VTT

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12 E11 D14 D13 D12 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

C805 DY Do Not Stuff; C808 DY Do Not Stuff; C809 C838 C839 C840 C841 — SC10U6D3V5KX-1GP

C829 C830 C842 C843 C844 C845 — SC10U6D3V5KX-1GP

H_CPU_SVIDDAT R804 130R2F-1-GP

VIDALERT# AJ29 H_CPU_SVIDALRT# R806 43R2J-GP VR_SVID_ALERT# 42

VIDSCLK AJ30 H_CPU_SVIDCLK H_CPU_SVIDCLK 42

VIDSOUT AJ28 H_CPU_SVIDDAT H_CPU_SVIDDAT 42

VCC_CORE

R801 100R2F-L1-GP-U

VCC_SENSE AJ35 VCCSENSE 42

VSS_SENSE AJ34 VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10 VCCIO_SENSE 45

VSSIO_SENSE A10 VSSIO_SENSE 45

1D05V_VTT

R803 DY Do Not Stuff

VCCIO_SENSE

VSSIO_SENSE

R805 DY Do Not Stuff

62.10040.821

2nd = 62.10040.771

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Title: CPU (VCC_CORE)

Size: Custom | Document Number: Enrico/Caruso 15 HR | Rev: X01

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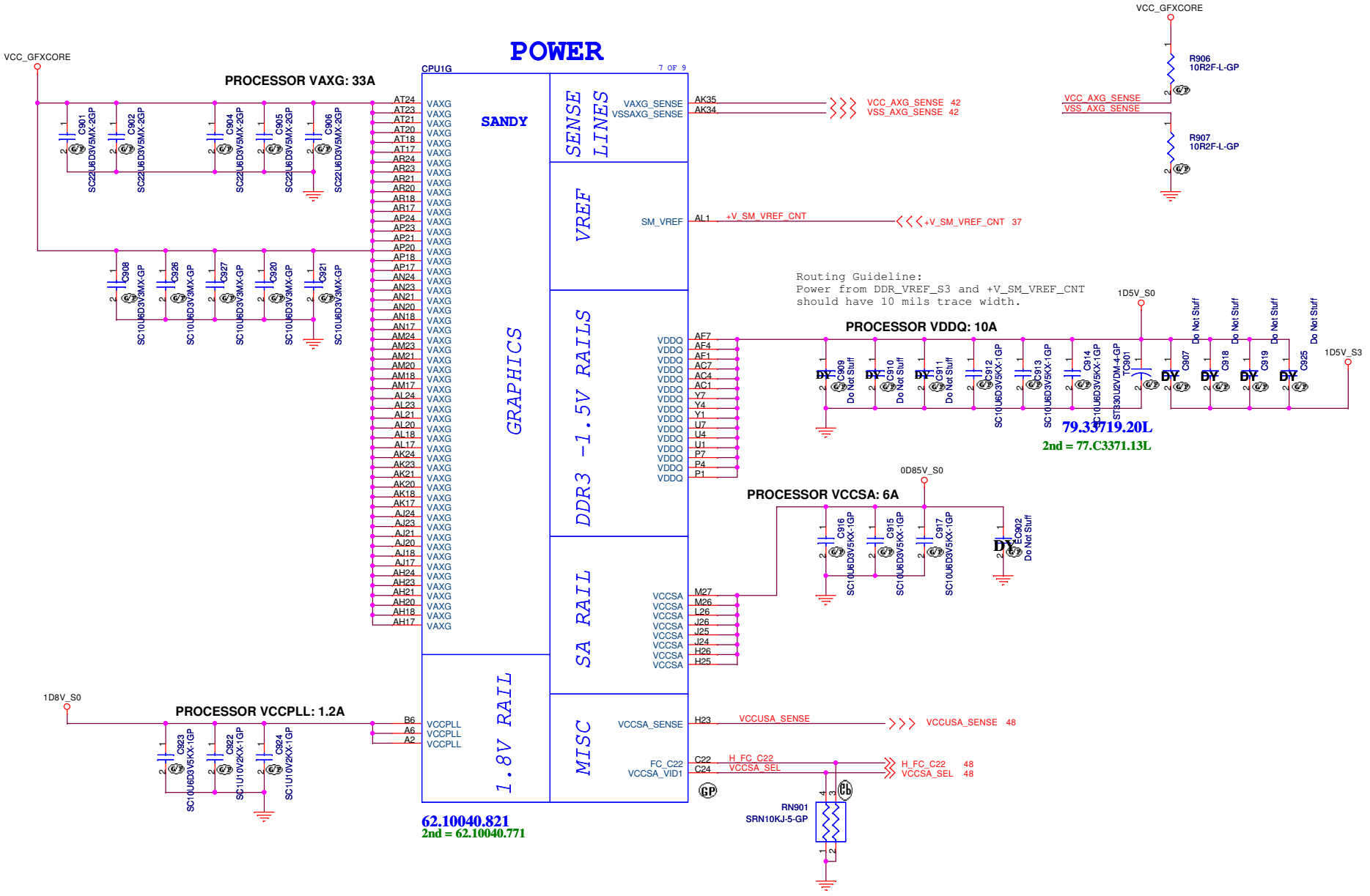
SSID = CPU

POWER



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Title: CPU (VCC_GFXCORE)

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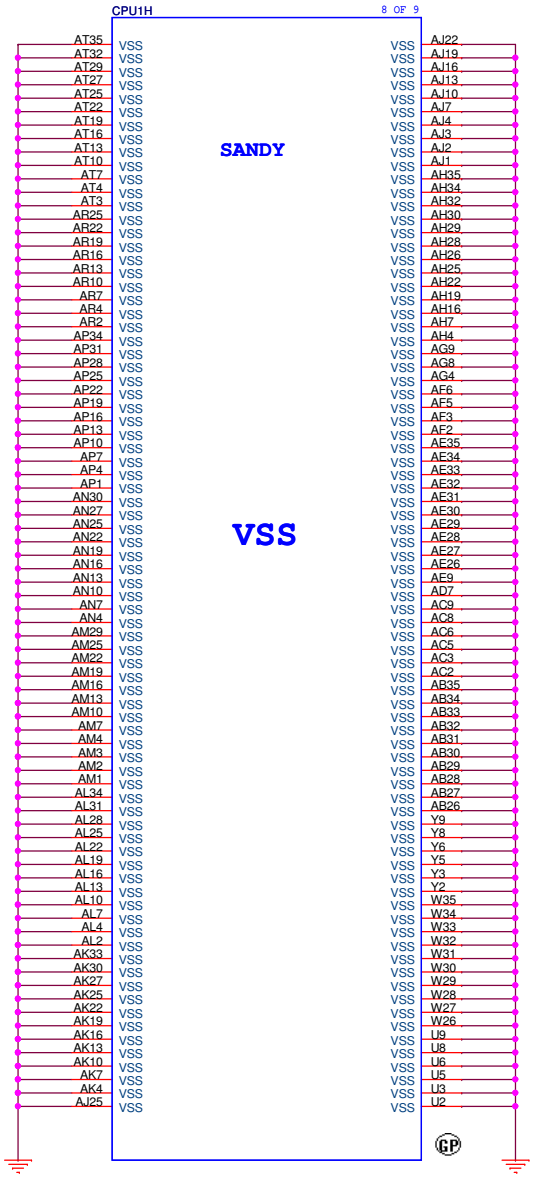
SSID = CPU



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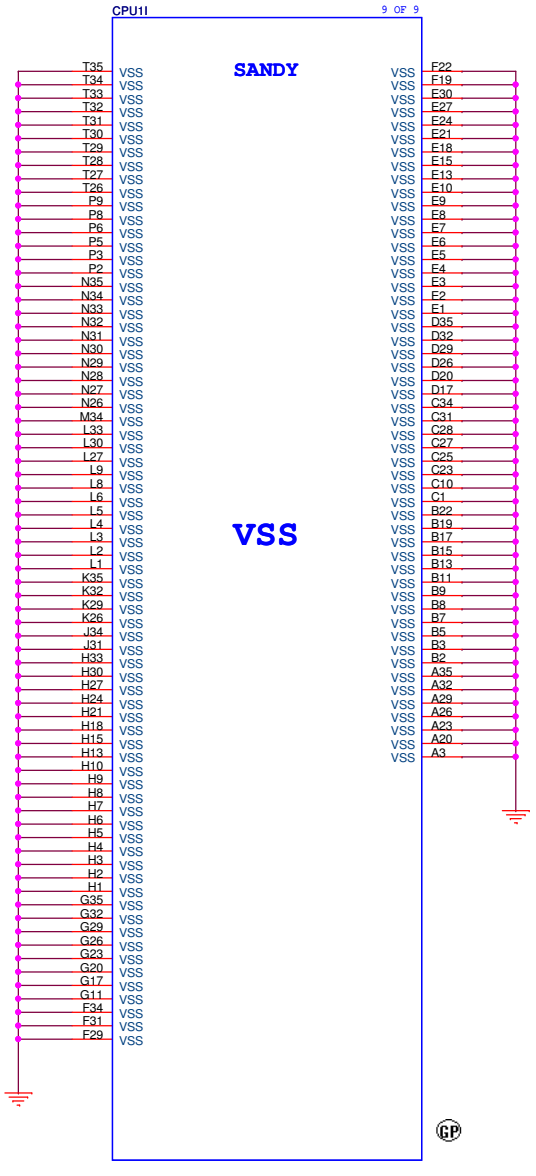

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Title: CPU (VSS)

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Title

XDP

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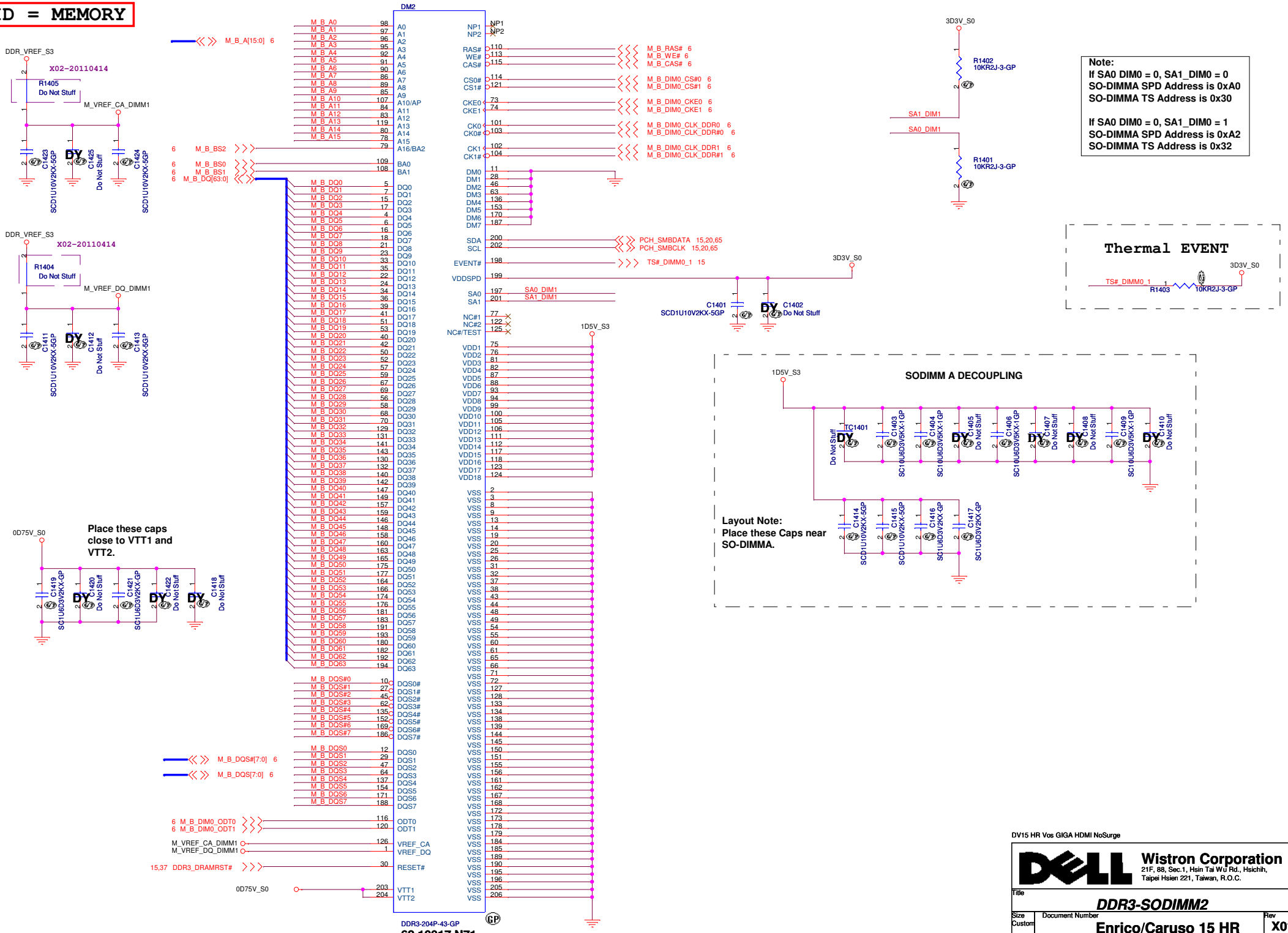
SSID = MEMORY



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

SODIMM A DECOUPLING

Layout Note:
Place these Caps near SO-DIMMA.

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Title: ***DDR3-SODIMM2***

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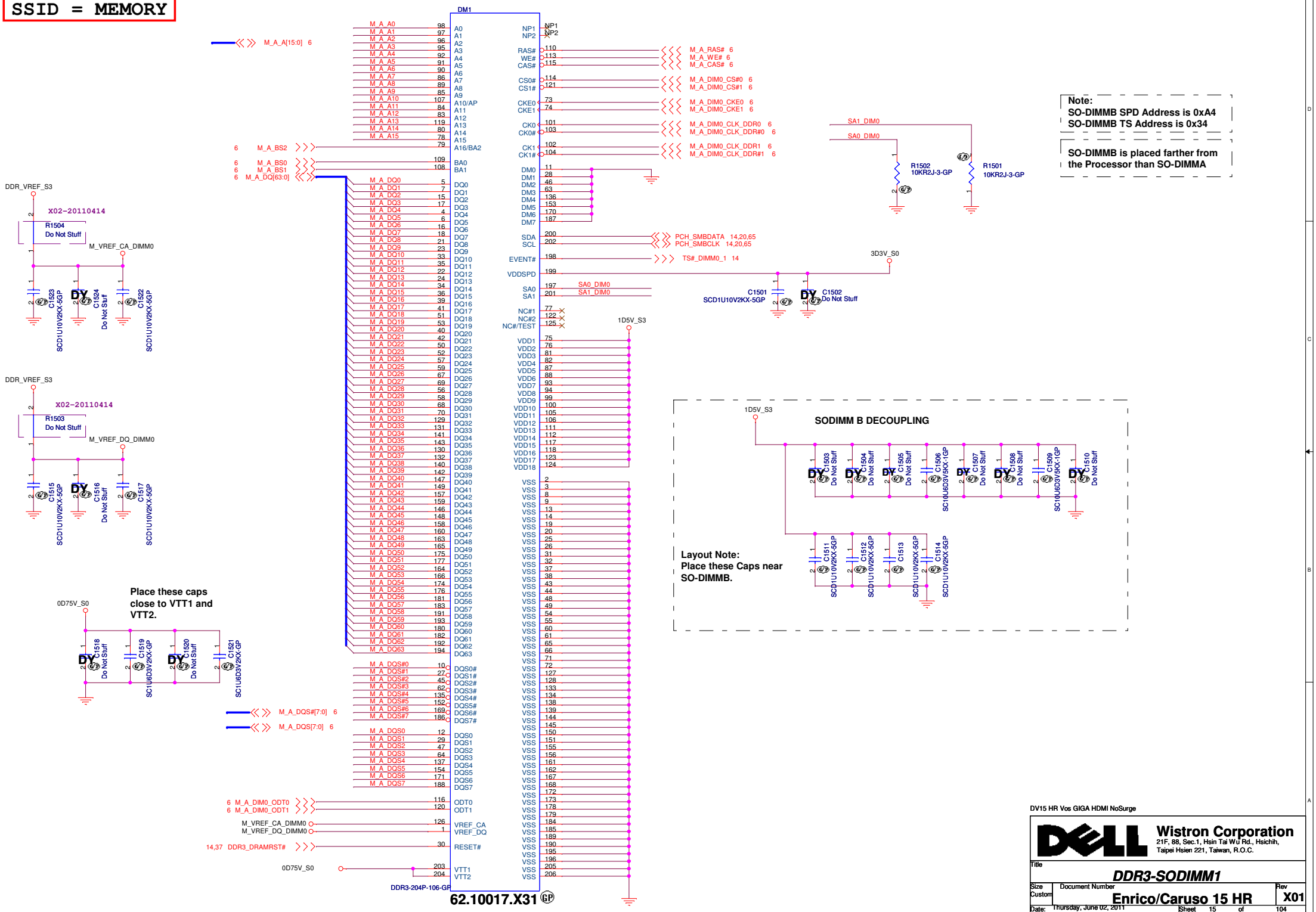

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Title: DDR3-SODIMM1

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Title

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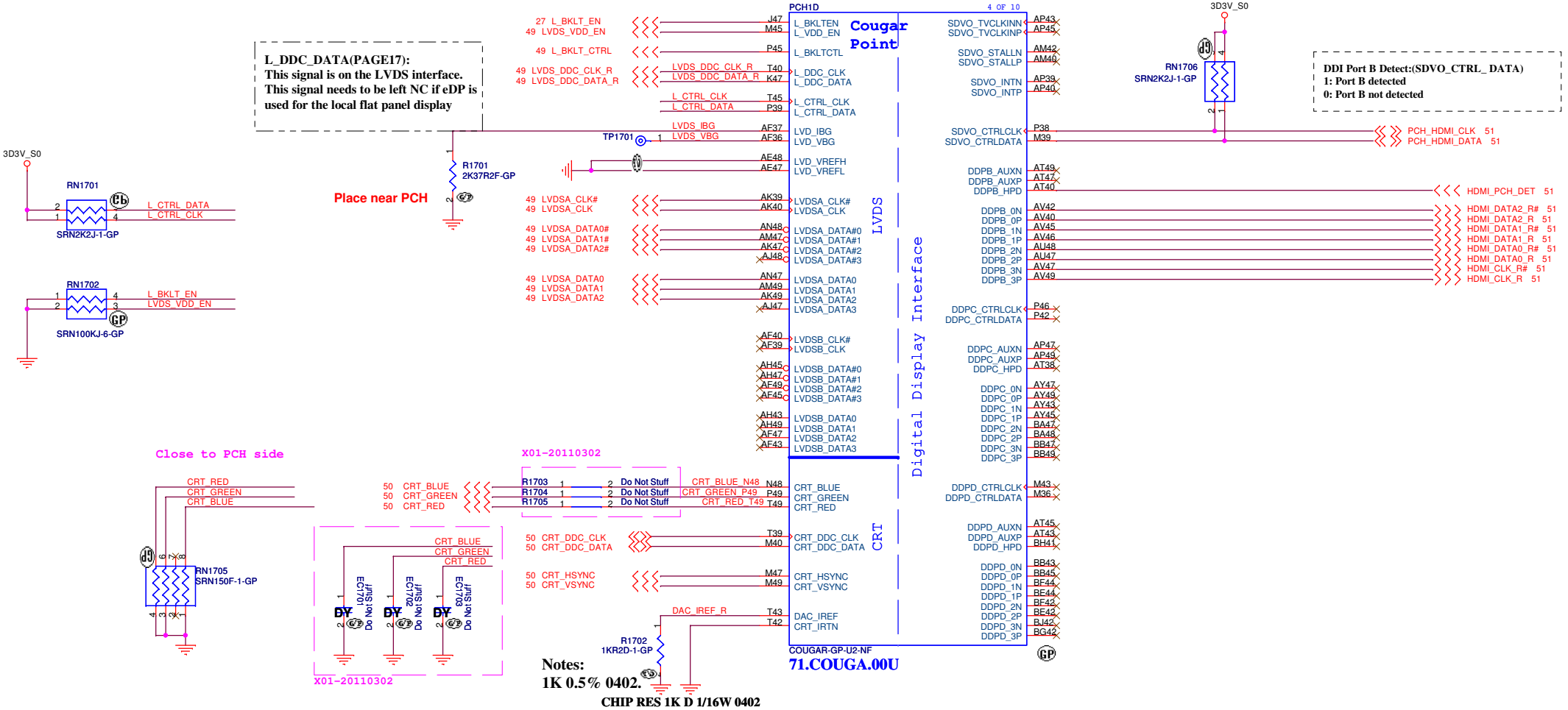

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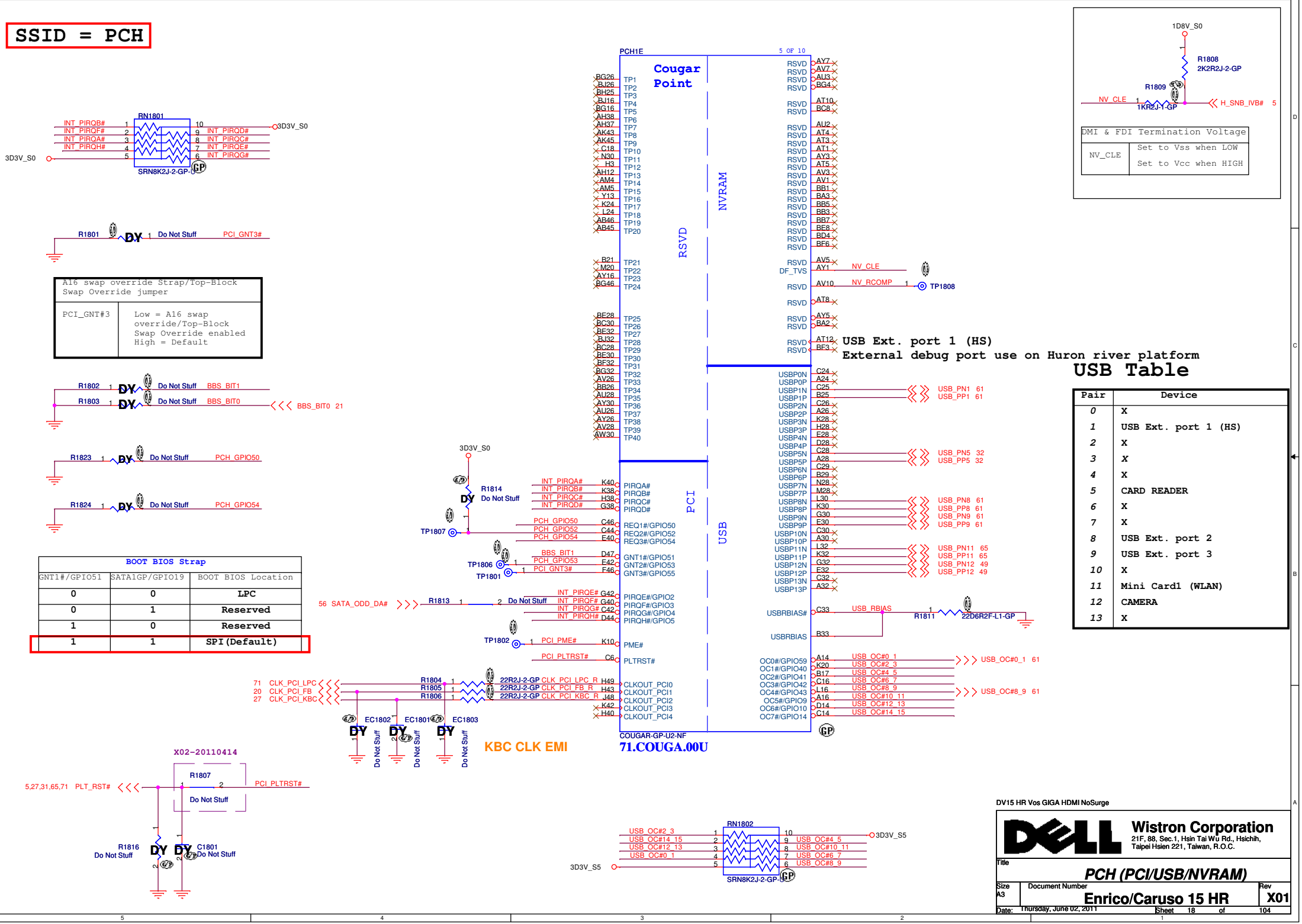
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (LVDS/CRT/DDI)	
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
Date: Thursday, June 02, 2011	Sheet 17 of 104	

SSID = PCH



USB Table

Pair	Device
0	X
1	USB Ext. port 1 (HS)
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

Size	Document Number	Rev
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SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

PCH1C — 3 OF 10 — Cougar Point

DMI: DMI0RXN, DMI1RXN, DMI2RXN, DMI3RXN, DMI0RXP, DMI1RXP, DMI2RXP, DMI3RXP, DMI0TXN, DMI1TXN, DMI2TXN, DMI3TXN, DMI0TXP, DMI1TXP, DMI2TXP, DMI3TXP

FDI: FDI_RXN0–7, FDI_RXP0–7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

System Power Management: DSWVRMEN, DPWROK, WAKE#, CLKRUN#/GPIO32, SUS_STAT#/GPIO61, SUSCLK/GPIO62, SLP_S5#/GPIO63, SLP_S4#, SLP_S3#, SLP_A#, SLP_SUS#, PMSYNCH, SLP_LAN#/GPIO29, SUSACK#, SYS_RESET#, SYS_PWROK, PWROK, APWROK, DRAMPWROK, RSMRST#, SUSWARN#/SUSPWRDNACK/GPIO30, PWRBTN#, ACPRESENT/GPIO31, BATLOW#/GPIO72, RI#

COUGAR-GP-U2-NF

71.COUGA.00U

S0_PWR_GOOD after PM_SLP_S3# delay 150 ms

DSWODVREN – On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)

Size: A3 | Document Number: Enrico/Caruso 15 HR | Rev: X01

Date: Thursday, June 02, 2011 | Sheet 19 of 104

SSID = PCH

PCH1B — Cougar Point — 2 OF 10

PCI-E*: W-WAN, LAN, Card Reader, WLAN, USB3.0, Intel GBE LAN, Dock, NEW CARD

SMBUS: SMBALERT#/GPIO11 (EC_SWI#), SMBCLK (SMB_CLK), SMBDATA (SMB_DATA), SML0ALERT#/GPIO60 (DRAMRST_CNTRL_PCH), SML0CLK (SML0_CLK), SML0DATA (SML0_DATA), SML1ALERT#/PCHHOT#/GPIO74 (PCH_GPIO74), SML1CLK/GPIO58 (SML1_CLK), SML1DATA/GPIO75 (SML1_DATA)

Controller Link: CL_CLK1 (CL_CLK), CL_DATA1 (CL_DATA), CL_RST1# (CL_RST#) — TP2001, TP2002, TP2003

CLOCKS: PEG_A_CLKRQ#/GPIO47 (PEG_CLKREQ#_R), CLKOUT_PEG_A_N/P (TP2009, TP2010), CLKOUT_DMI_N/P (RN2016, Do Not Stuff, A00-20110517), CLKOUT_DP_N/P, CLKIN_DMI_N/P (CLK_BUF_EXP_N/P), CLKIN_GND1_N/P (CLK_BUF_CPYCLK_N/P, RN2008, SRN10KJ-5-GP), CLKIN_DOT_96N/P (CLK_BUF_DOT96_N/P), CLKIN_SATA_N/P (CLK_BUF_CKSSCD_N/P), REFCLK14IN (CLK_BUF_REF14), CLKIN_PCILOOPBACK (CLK_PCI_FB), XTAL25_IN/OUT, XCLK_RCOMP (R2007, 90D9R2F-1-GP, +VCCDIFFCLKN)

FLEX CLOCKS: CLKOUTFLEX0/GPIO64 (PCH_GPIO64, TP2004, R2016, 22R2J-2-GP, CLK_PCH_48M 32), CLKOUTFLEX1/GPIO65 (CLK_48_USB30), CLKOUTFLEX2/GPIO66 (PCH_GPIO66, TP2007), CLKOUTFLEX3/GPIO67 (DGPU_PRSNT#)

CLKOUT_PCIE0N/P (Y40/Y39), CLKOUT_PCIE1N/P (AB49/AB47), CLKOUT_PCIE2N/P (AA48/AA47), CLKOUT_PCIE3N/P (Y37/Y36), CLKOUT_PCIE4N/P (Y43/Y45), CLKOUT_PCIE5N/P (V45/V46), CLKOUT_PEG_B_N/P (AB42/AB40), CLKOUT_PCIE6N/P (V40/V42), CLKOUT_PCIE7N/P (V38/V37), CLKOUT_ITPXDP_N/P (AK14/AK13)

PCIECLKRQ0#/GPIO73 (PCIE_CLK_RQ0#, J2)
PCIECLKRQ1#/GPIO18 (M1)
PCIECLKRQ2#/GPIO20 (V10)
PCIECLKRQ3#/GPIO25 (A8)
PCIECLKRQ4#/GPIO26 (L12)
PCIECLKRQ5#/GPIO44 (L14)
PEG_B_CLKRQ#/GPIO56 (E6)
PCIECLKRQ6#/GPIO45 (T13)
PCIECLKRQ7#/GPIO46 (K12)

TP2005, TP2006 (ITPXDP_N, ITPXDP_P)

COUGAR-GP-U2-NF

71.COUGA.00U

- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

WLAN CLK: 65 CLK_PCIE_WLAN#/WLAN, RN2012, CLK_PCH_SRC1_N/P, Do Not Stuff, 65 CLK_PCIE_WLAN_REQ#

LAN CLK: 31 CLK_PCIE_LAN#/LAN, RN2014, CLK_PCH_SRC3_N/P, Do Not Stuff, 31 PCIE_CLK_LAN_REQ#

A00-20110517

PCIECLKRQ1# and PCIECLKRQ2# Support S0 power only

3D3V_S0 — RN2018 — PCIE_CLK_RQ2#, CLK_PCIE_WLAN_REQ# — SRN10KJ-5-GP

3D3V_S5 — RN2002 — PCIE_CLK_RQ0#, PCIE_CLK_RQ4#, PCIE_CLK_RQ7#, PEG_CLKREQ#_R — SRN10KJ-5-GP

31 PCIE_RXN2, 31 PCIE_RXP2, 31 PCIE_TXN2, 31 PCIE_TXP2 — C2001, C2002 — SCD1U10V2KX-5GP — PCIE_TXN2_C, PCIE_TXP2_C

65 PCIE_RXN4, 65 PCIE_RXP4, 65 PCIE_TXN4, 65 PCIE_TXP4 — C2005, C2006 — SCD1U10V2KX-5GP — PCIE_TXN4_C, PCIE_TXP4_C

3D3V_S5

SMB_CLK, SMB_DATA — RN2003 — SRN2K2J-1-GP
SML0_DATA, SML0_CLK — RN2004 — SRN2K2J-1-GP
SML1_CLK, SML1_DATA — RN2005 — SRN2K2J-1-GP
EC_SWI#, PCH_GPIO74 — RN2006 — SRN10KJ-5-GP
DRAMRST_CNTRL_PCH — R2009 — 1KR2J-1-GP

3D3V_S0 — RN2007 — SRN2K2J-1-GP

2nd = 84.DM601.03F
84.2N702.A3F
2N7002KDW-GP

SMB_DATA — PCH_SMBDATA 14,15,65
SMB_CLK — PCH_SMBCLK 14,15,65
Q2001

X02-20110427

XTAL25_IN — C2008 — SC18P50V2JN-1-GP
X2001
R2006 1M1R2J-GP
XTAL25_OUT — C2007 — SC18P50V2JN-1-GP
XTAL-25MHZ-155-GP

82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.G61

CLK_PCH_48M — DY EC2003 Do Not Stuff

PL 10K FOR Integrated CLOCK GEN mode.

CLK_BUF_DOT96_N/P — RN2020 — SRN10KJ-5-GP
CLK_BUF_CKSSCD_N/P — RN2021 — SRN10KJ-5-GP
CLK_BUF_EXP_N/P — RN2019 — SRN10KJ-5-GP
CLK_BUF_REF14 — 10KR2J-3-GP — R2008

3D3V_S5 — RN2001 — PCIE_CLK_LAN_REQ#, PCIE_CLK_REQ5#, PEG_B_CLKRQ#, PCIE_CLK_REQ6# — SRN10KJ-5-GP

3D3V_S0 — DGPU_PRSNT# — 10KR2J-3-GP — R2017

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: PCH (PCI-E/SMBUS/CLOCK/CL)
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Date: Thursday, June 02, 2011 | Sheet 20 of 104

SSID = PCH

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V High = 1.5V (Default)

COUGAR-GP-U2-NF
71.COUGA.00U

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size	Document Number	Rev
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Date: Thursday, June 02, 2011 Sheet 21 of 104

SSID = PCH

3D3V_S0 — R2202 1 — DY — Do Not Stuff — SATA_ODD_PRSNT#

3D3V_S0 — RN2203 SRN10KJ-5-GP — H_A20GATE — H_RCIN#

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

3D3V_S0 — R2220 — DY — Do Not Stuff — PCH_GPIO48

3D3V_S5 — R2224 — 10KR2J-3-GP — PCH_GPIO12

3D3V_S0 — R2221 — DY — Do Not Stuff — PCH_GPIO6

3D3V_S0 — R2222 — DY — Do Not Stuff — PCH_GPIO17

3D3V_S0 — RN2204 — PSW_CLR# — PCH_GPIO0 — SRN10KJ-5-GP

3D3V_S0 — RN2201 — EC_SMI# — EC_SCI# — MFG_MODE — PCH_TEMP_ALERT# — SRN10KJ-6-GP

3D3V_S5 — R2201 — 1KR2J-1-GP — PCH_GPIO15

3D3V_S0 — R2207 — DY — Do Not Stuff — FDI_OVRVLTG — R2208 10KR2J-3-GP

3D3V_S0 — R2209 — DY — Do Not Stuff — DMI_OVRVLTG — R2210 10KR2J-3-GP

ICC_EN# — R2211 — 1KR2J-1-GP

PCH1F — 6 OF 10 — Cougar Point

GPIO:
- PCH_GPIO0 T7 BMBUSY#/GPIO0
- 27 EC_SMI# A42 TACH1/GPIO1
- PCH_GPIO6 H36 TACH2/GPIO6
- 27 EC_SCI# E38 TACH3/GPIO7
- ICC_EN# C10 GPIO8
- 60 PCH_GPIO12 C4 LAN_PHY_PWR_CTRL/GPIO12
- PCH_GPIO15 G2 GPIO15
- 56 SATA_ODD_PRSNT# — R2213 — Do Not Stuff — PCH_GPIO16 U2 SATA4GP/GPIO16
- PCH_GPIO17 D40 TACH0/GPIO17
- TP2210 PCH_GPIO22 T5 SCLOCK/GPIO22
- TP2216 PCH_GPIO24 E8 GPIO24/MEM_LED
- TP2203 PCH_GPIO27 E16 GPIO27
- PLL_ODVR_EN P8 GPIO28
- PSW_CLR# K1 STP_PCI#/GPIO34
- TP2212 PCH_GPIO35 K4 GPIO35
- DMI_OVRVLTG V8 SATA2GP/GPIO36
- FDI_OVRVLTG M5 SATA3GP/GPIO37
- MFG_MODE N2 SLOAD/GPIO38
- TP2215 PCH_GPIO39 M3 SDATAOUT0/GPIO39
- TP2214 PCH_GPIO48 V13 SDATAOUT1/GPIO48
- PCH_TEMP_ALERT# V3 SATA5GP/GPIO49
- D6 GPIO57

Do Not Stuff — G2201

CPU/MISC:
- C40 TACH4/GPIO68 — SATA_ODD_PWRGT 56
- B41 TACH5/GPIO69 — UMA_DIS#
- C41 TACH6/GPIO70 — TP2204
- A40 TACH7/GPIO71 — TP2205
- P4 A20GATE — H_A20GATE 27
- AU16 PECI — H_PECI_R — R2203 — DY — Do Not Stuff — H_PECI 5,27
- P5 RCIN# — H_RCIN# 27
- AY11 PROCPWRGD — H_CPUPWRGD 5,36
- AY10 THRMTRIP# — PCH_THERMTRIP_R — R2204 — 390R2J-1-GP — H_THERMTRIP# 5,36
- T14 INIT3_3V# — INIT3_3V# — TP2201
- AH8 TS_VSS1
- AK11 TS_VSS2
- AH10 TS_VSS3
- AK10 TS_VSS4 — TS_VSS — R2219 — Do Not Stuff
- P37 NC_1

3D3V_S0 — R2223 — 10KR2J-3-GP — UMA_DIS#

NCTF:
- TP2206 PCH_NCTF_1 A4 NCTF_VSS#A4
- A44 NCTF_VSS#A44
- A45 NCTF_VSS#A45
- A46 NCTF_VSS#A46
- A5 NCTF_VSS#A5
- A6 NCTF_VSS#A6
- B3 NCTF_VSS#B3
- B47 NCTF_VSS#B47
- BD1 NCTF_VSS#BD1
- BD49 NCTF_VSS#BD49
- TP2207 PCH_NCTF_2 BE1 NCTF_VSS#BE1
- TP2208 PCH_NCTF_3 BE49 NCTF_VSS#BE49
- BF1 NCTF_VSS#BF1
- TP2209 PCH_NCTF_4 BF49 NCTF_VSS#BF49

NCTF TEST PIN: A4,A44,A45,A46,A5,A6,B3,B47,BD1,BD49,BE1,BE49,BF1,BF49

- BG2 NCTF_VSS#BG2
- BG48 NCTF_VSS#BG48
- BH3 NCTF_VSS#BH3
- BH47 NCTF_VSS#BH47
- BJ4 NCTF_VSS#BJ4
- BJ44 NCTF_VSS#BJ44
- BJ45 NCTF_VSS#BJ45
- BJ46 NCTF_VSS#BJ46
- BJ5 NCTF_VSS#BJ5
- BJ6 NCTF_VSS#BJ6
- C2 NCTF_VSS#C2
- C48 NCTF_VSS#C48
- D1 NCTF_VSS#D1
- D49 NCTF_VSS#D49
- E1 NCTF_VSS#E1
- E49 NCTF_VSS#E49
- F1 NCTF_VSS#F1
- F49 NCTF_VSS#F49

NCTF TEST PIN: BG2,BG48,BH3,BH47,BJ4,BJ44,BJ45,BJ46,BJ5,BJ6,C2,C48 D1,D49,E1,E49,F1,F49

COUGAR-GP-U2-NF

71.COUGA.00U

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN — DY — R2212 — Do Not Stuff

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

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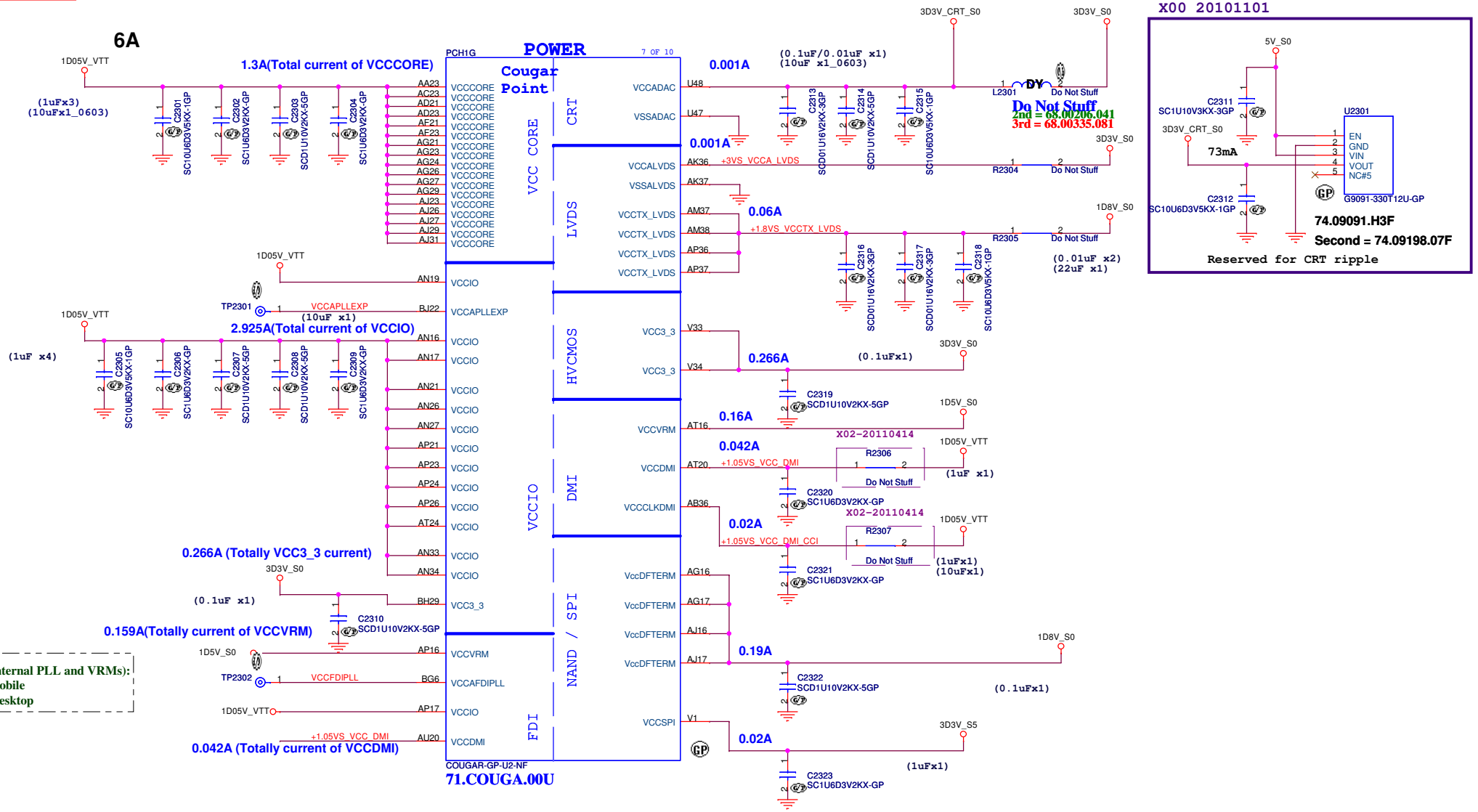
SSID = PCH



DV15 HR Vos GIGA HDMI NoSurge

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (POWER1)**

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POWER

PCH1J — Cougar Point — 10 OF 10

Clock and Miscellaneous

TP2401 VCCACLK → AD49 VCCACLK

3D3V_S5 → 0.002A → T16 VCCDSW3_3 (0.1uFx1)

Do Not Stuff TP2405 DCPSUSBYP → V12 DCPSUSBYP

+V3.3S_VCC_CLKF33 → T38 VCC3_3

TP2404 +VCCAPLL_CPY_PCH → BH23 VCCAPLLDMI2

1D05V_VTT (10uFx1) → AL29 VCCIO

TP2402 +VCCSUS1 → AL24 DCPSUS

3D3V_S0 → L2401 IND-10UH-218-GP (10uFx1) (1uFx1)
68.10050.10Y
2nd = 68.1001E.10N
C2401 SC10U6D3V5KX-1GP
C2402 SC1U10V2KX-1GP

1D05V_VTT → 1.01A (Total current of VCCASW)
(22uFx2_0603) (1uFx3)
C2403 SC10U6D3V5KX-1GP
C2404 SC10U6D3V5KX-1GP
C2406 SCD1U10V2KX-5GP
C2407 SC1U6D3V2KX-GP
C2408 SCD1U10V2KX-5GP

AA19 AA21 AA24 AA26 AA27 AA29 AA31 AC26 AC27 AC29 AC31 AD29 AD31 W21 W23 W24 W26 W29 W31 W33 VCCASW

1D05V_VTT → 0.08A (1uFx1) (220uFx1)
L2402 IND-10UH-218-GP
68.10050.10Y
2nd = 68.1001E.10N
+1.05VS_VCCA_A_DPL
DY C2443 Do Not Stuff
C2409 SC1U6D3V2KX-GP

L2403 IND-10UH-218-GP
68.10050.10Y
2nd = 68.1001E.10N
0.08A (1uFx1) (220uFx1)
+1.05VS_VCCA_B_DPL
DY C2444 Do Not Stuff
C2410 SC1U6D3V2KX-GP

+VCCRTCEXT → N16 DCPRTC
C2411 SCD1U10V2KX-5GP (0.1uFx1)
1D5V_S0 → Y49 VCCVRM
0.16A (Totally current of VCCVRM)

+1.05VS_VCCA_A_DPL → BD47 VCCADPLLA
+1.05VS_VCCA_B_DPL → BF47 VCCADPLLB

1D05V_VTT X02-20110414 Do Not Stuff R2404 +VCCDIFFCLK
C2412 SC1U6D3V2KX-GP

1D05V_VTT X02-20110414 Do Not Stuff R2405 +V1.05S_SSCVCC
C2413 SC1U6D3V2KX-GP

1D05V_VTT (1uFx1) R2406 Do Not Stuff +VCCDIFFCLKN
+VCCDIFFCLK (1uFx1) → AF17 VCCIO
0.055A
AF33 VCCDIFFCLKN
AF34 VCCDIFFCLKN
AG34 VCCDIFFCLKN
C2414 SC1U6D3V2KX-GP
0.095A
+V1.05S_SSCVCC (1uFx1) → AG33 VCCSSC
(0.1uFx1) C2415 +VCCSST SCD1U10V2KX-5GP → V16 DCPSST
TP2406 DCPSUS → T17 DCPSUS
V19 DCPSUS
(1uFx1)

1D05V_VTT → 0.001A → BJ8 V_PROC_IO
(0.1uFx2) (4.7uFx1_0603)
C2417 SC4D7U6D3V3KX-GP
C2418 SCD1U10V2KX-5GP

RTC_AUX_S5 → 6uA → A22 VCCRTC
(0.1uFx2) (1uFx1)
C2421 SCD1U10V2KX-5GP
C2422 SCD1U10V2KX-5GP

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USB

N26 P26 P28 T27 T29 VCCIO → 1D05V_VTT (1uFx1) C2423 SCD1U10V2KX-5GP

T23 T24 V23 V24 P24 VCCSUS3_3 → 3D3V_S5 (0.1uFx1)
0.097A (Totally current of VCCSUS3_3)
C2424 SCD1U10V2KX-5GP
C2425 SCD1U10V2KX-5GP

T26 VCCIO → 1D05V_VTT

M26 V5REF_SUS → +5VA_PCH_VCC5REFSUS → 0.001A
AN23 DCPSUS → +VCCA_USBSUS → TP2403
AN24 VCCSUS3_3 → 3D3V_S5
DY C2437 Do Not Stuff

P34 V5REF → +5VS_PCH_VCC5REF → 0.001A

PCI/GPIO/LPC

N20 N22 P20 P22 VCCSUS3_3 → 3D3V_S5 (1uFx1)
C2428 SC1U6D3V2KX-GP

AA16 W16 T34 VCC3_3 → 3D3V_S0 (0.1uFx2)
C2430 SCD1U10V2KX-5GP
C2431 SCD1U10V2KX-5GP

AJ2 VCC3_3 → 3D3V_S0 (0.1uFx1)
C2429 SCD1U10V2KX-5GP

AF13 AH13 AH14 AF14 VCCIO → 1D05V_VTT (1uFx1)
C2432 SC1U6D3V2KX-GP

AK1 VCCAPLLSATA → +V1.05S_VCCAPLL_SATA3 → 1D05V_VTT
AF11 VCCVRM → 1D05V_S0
R2411 DY Do Not Stuff (10uFx1)
DY C2434 Do Not Stuff

SATA

AC16 AC17 AD17 VCCIO → 1D05V_VTT (1uFx1)
C2435 SCD1U10V2KX-5GP

MISC

T21 V21 T19 VCCASW → 1D05V_VTT

CPU

HDA

P32 VCCSUSHDA → +3VA_+1.5VA_HDA_IO → 0.01A (0.1uFx1)
C2433 SCD1U10V2KX-5GP

RTC

D2401 CH751H-40PT-GP 83.R0304.A8F
2nd = 83.R2004.B8F
3D3V_S5 5V_S5
R2408 10R2J-2-GP (0.1uFx1)
C2426 SCD1U10V2KX-5GP

D2402 CH751H-40PT-GP 83.R0304.A8F
2nd = 83.R2004.B8F
3D3V_S0 5V_S0
R2407 10R2J-2-GP (1uFx1)
C2427 SC1U10V2KX-1GP

+3VA_+1.5VA_HDA_IO
R2409 Do Not Stuff 3D3V_S5

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER2)

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A3	Enrico/Caruso 15 HR	X01

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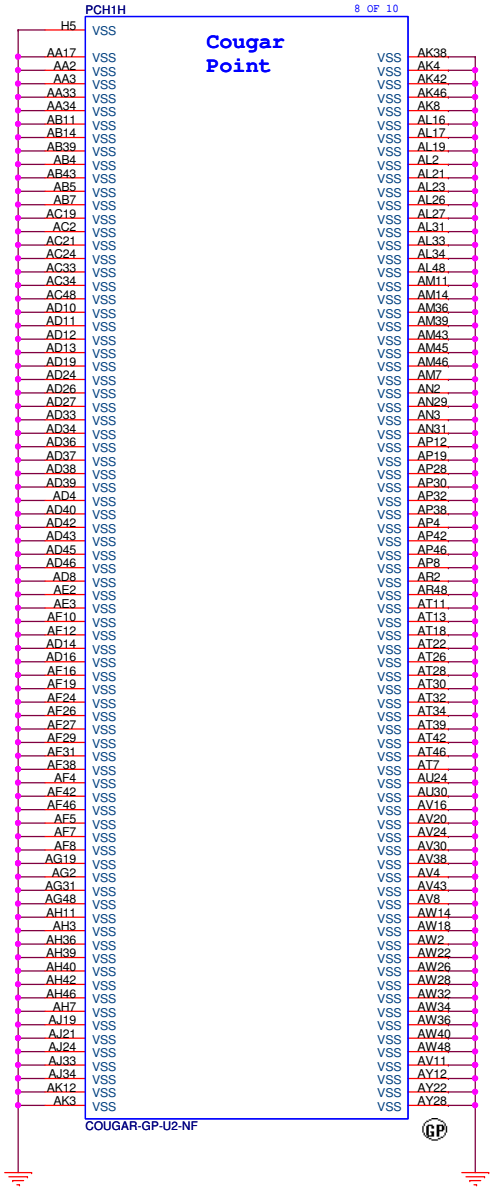
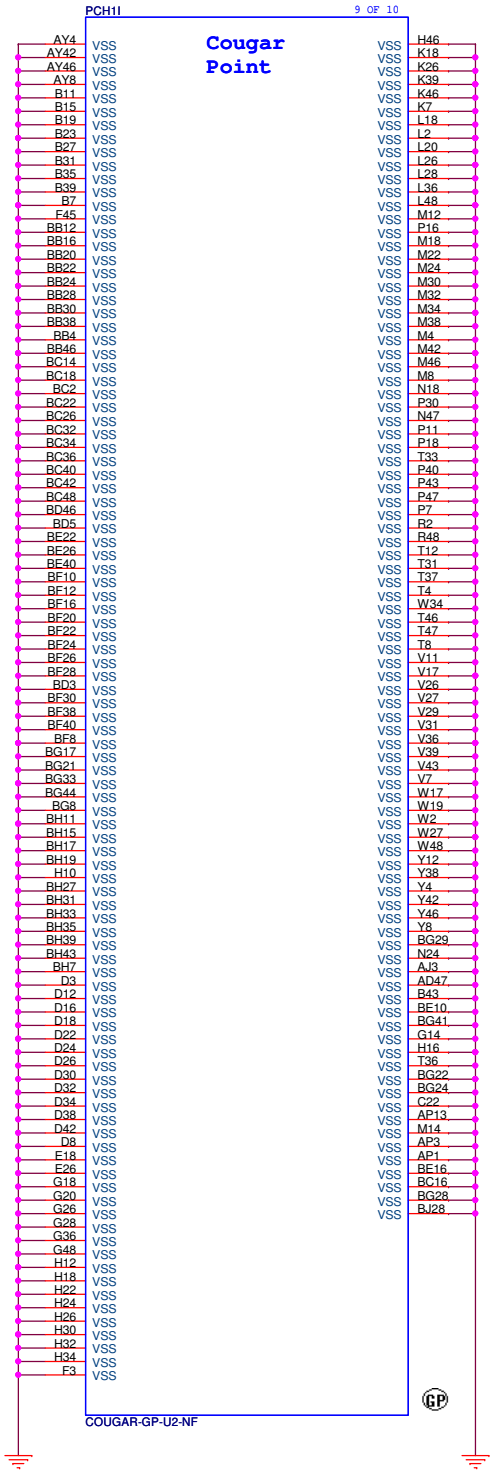
SSID = PCH





DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *PCH (VSS)*

Size	Document Number	Rev
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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
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SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DV14_UMA	100.0K	10.0K(64.10025.6DL)	3.0V
DV14_DIS_PX	100.0K	20.0K(64.20025.6DL)	2.75V
DV15_UMA with HDMI	100.0K	33.0K	2.48V
DV15_UMA without HDMI	100.0K	47.0K(64.47025.6DL)	2.24V
Reserved	100.0K	64.9K(64.64925.6DL)	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

NOTE:
Locate resistors R2736,R2719 and R2722 close to the NPCE795P.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

C2712 Need very close to EC

Need very close to EC

EC_GPIO47 High Active

PSL SOLUTION

10mW SOLUTION

EC GPIO standard PH/PL

NOTES:
Please make sure there's no pull-down resistor on USB_PWR_EN#,AC_PRESENT,E51_TXD.

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

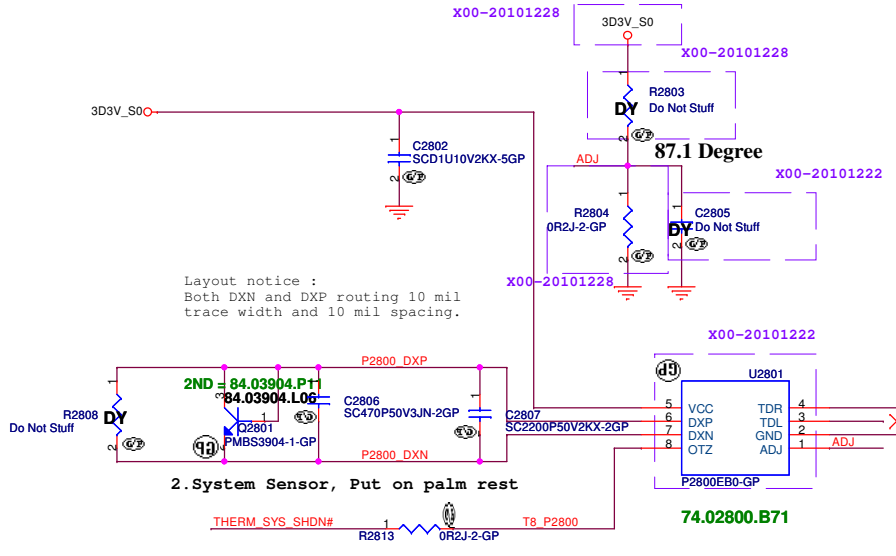
Title: KBC Nuvoton NPCE795

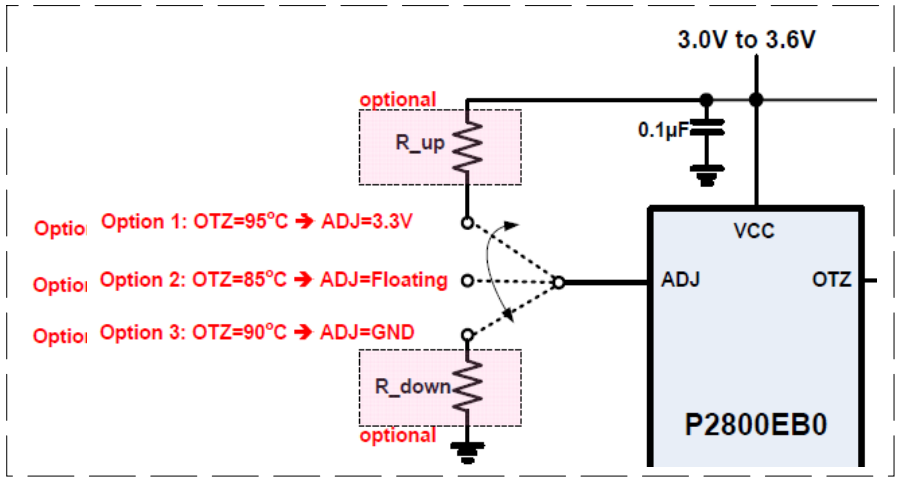
Size: A2 | Document Number: Enrico/Caruso 15 HR | Rev: X01

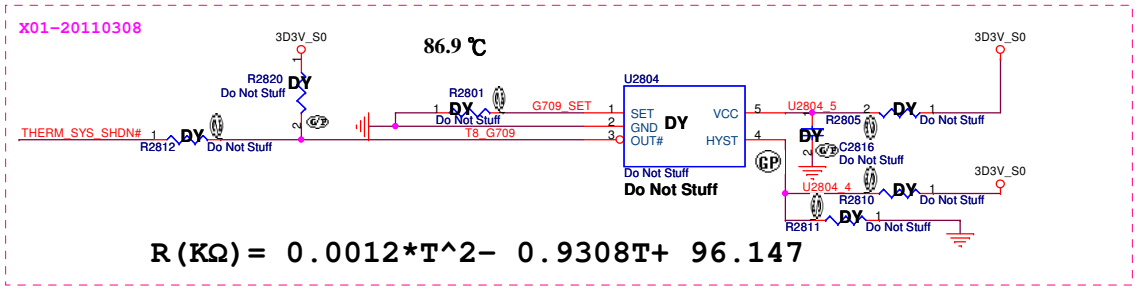
Date: Thursday, June 02, 2011 | Sheet 27 of 104

SSID = Thermal

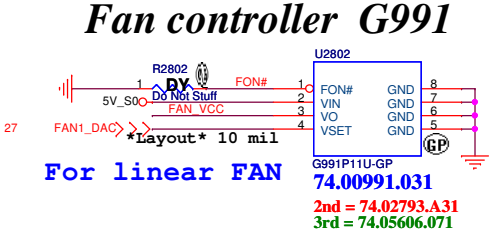
Thermal sensor P2800

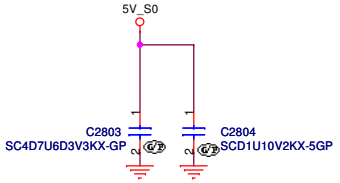


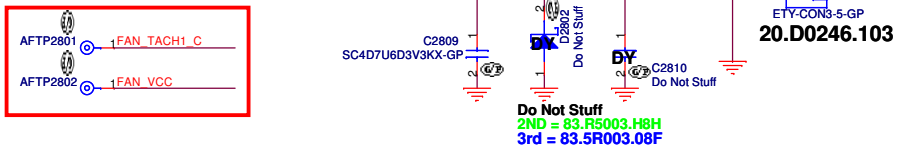




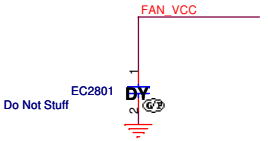
Fan controller G991

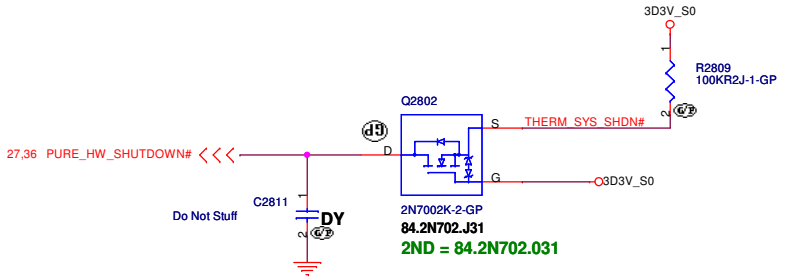






EMI/ESD





DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793

Size	Document Number	Rev
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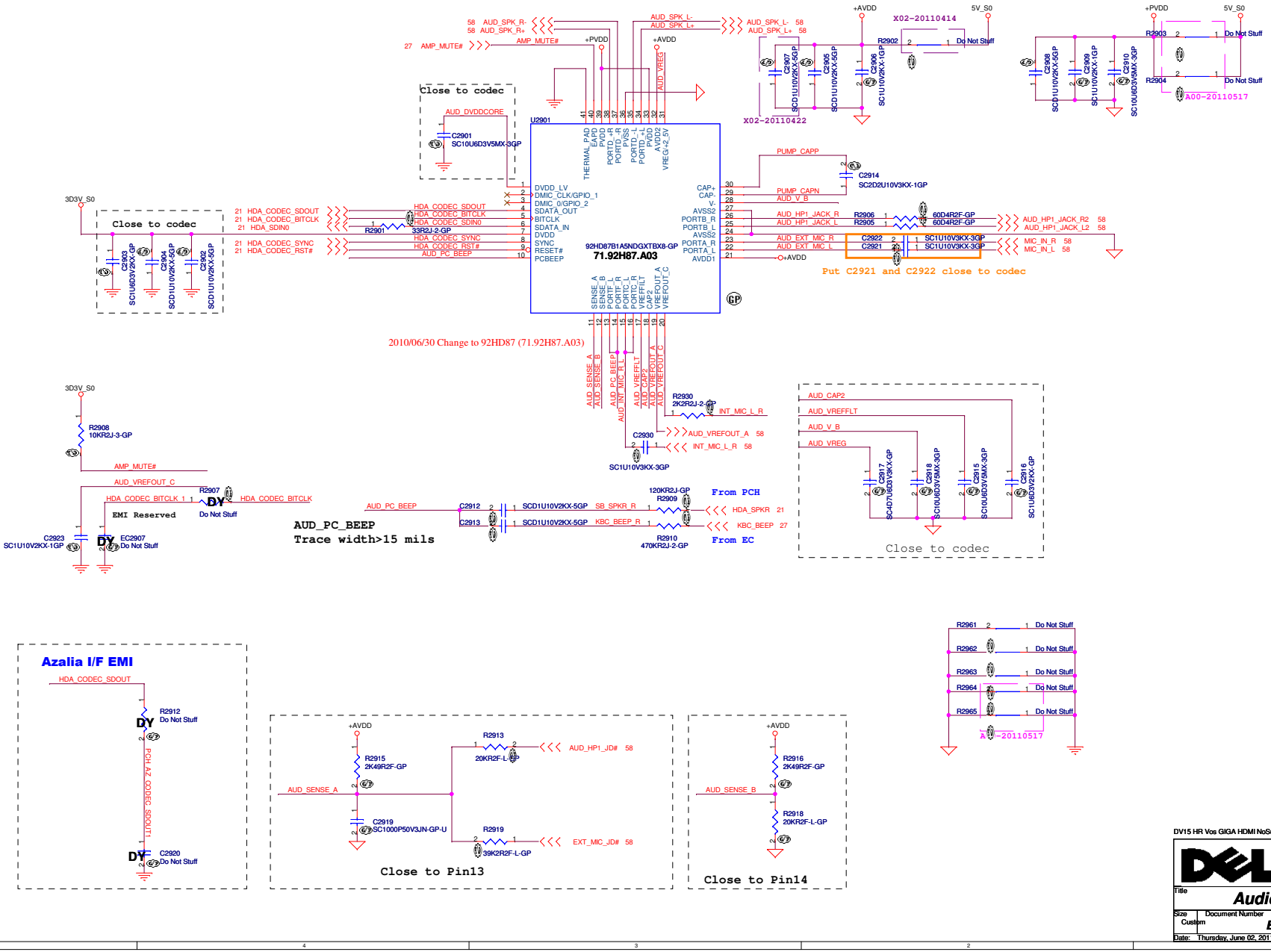
SSID = AUDIO



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD87B1

Size: Custom | Document Number: Enrico/Caruso 15 HR | Rev: X01

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DV15 HR Vos GIGA HDMI NoSurge

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Title: *Reserved*

Size: A3 | Document Number: *Enrico/Caruso 15 HR* | Rev: *X01*

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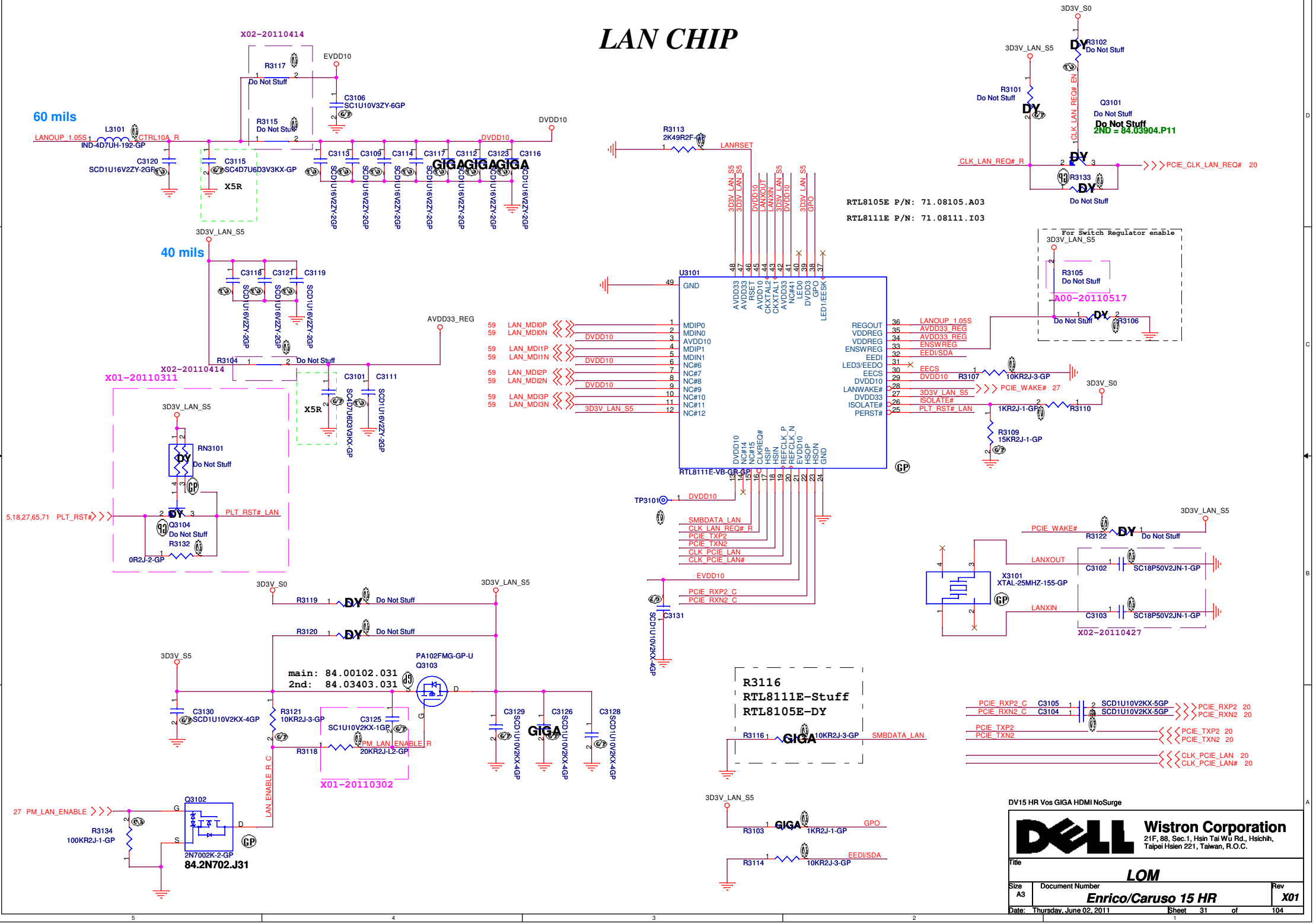
LAN CHIP



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LOM		
Size: A3	Document Number: Enrico/Caruso 15 HR	Rev: X01
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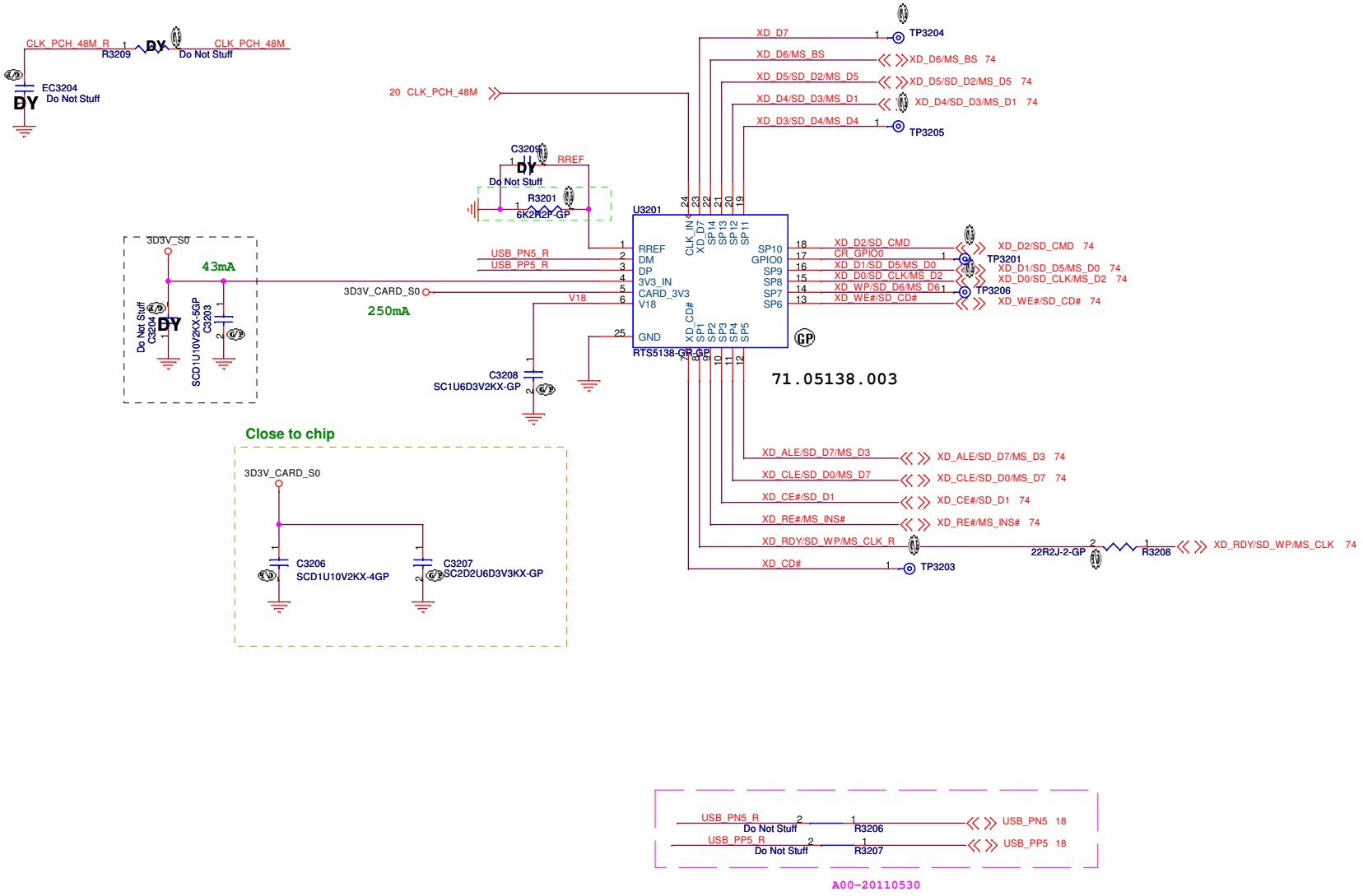
SSID = SDIO



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Card Reader-RTS5138*

Size: A3 | Document Number: *Enrico/Caruso 15 HR* | Rev: *X01*

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DV15 HR Vos GIGA HDMI NoSurge

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Title

Reserved

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DV15 HR Vos GIGA HDMI NoSurge

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Title

Reserved

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DV15 HR Vos GIGA HDMI NoSurge

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Title

Reserved

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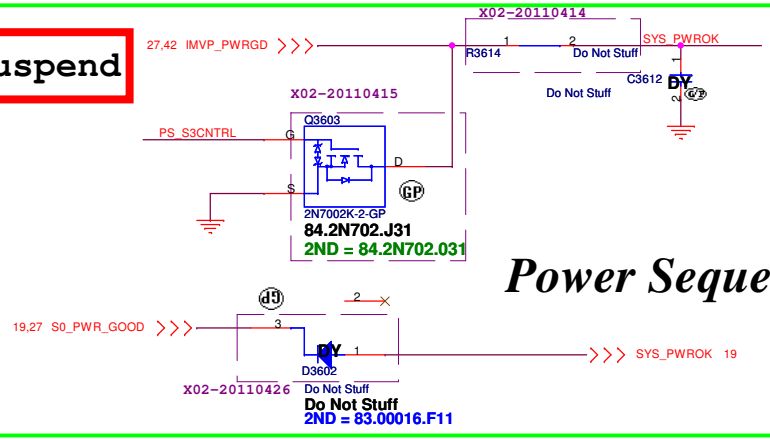
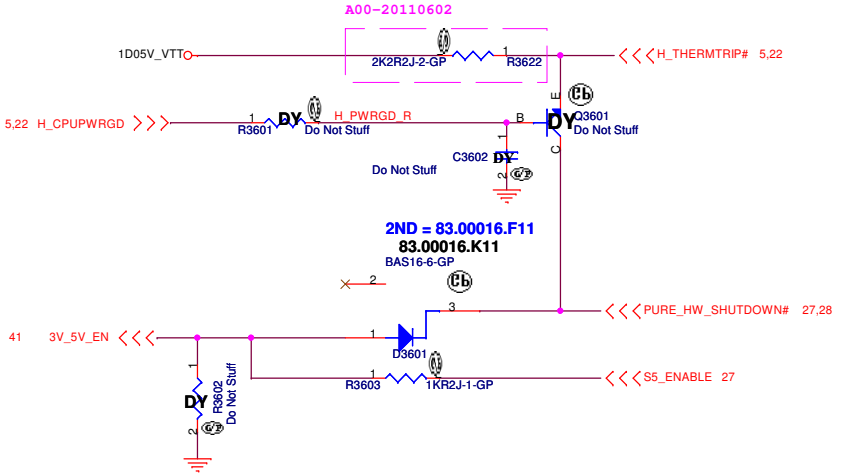
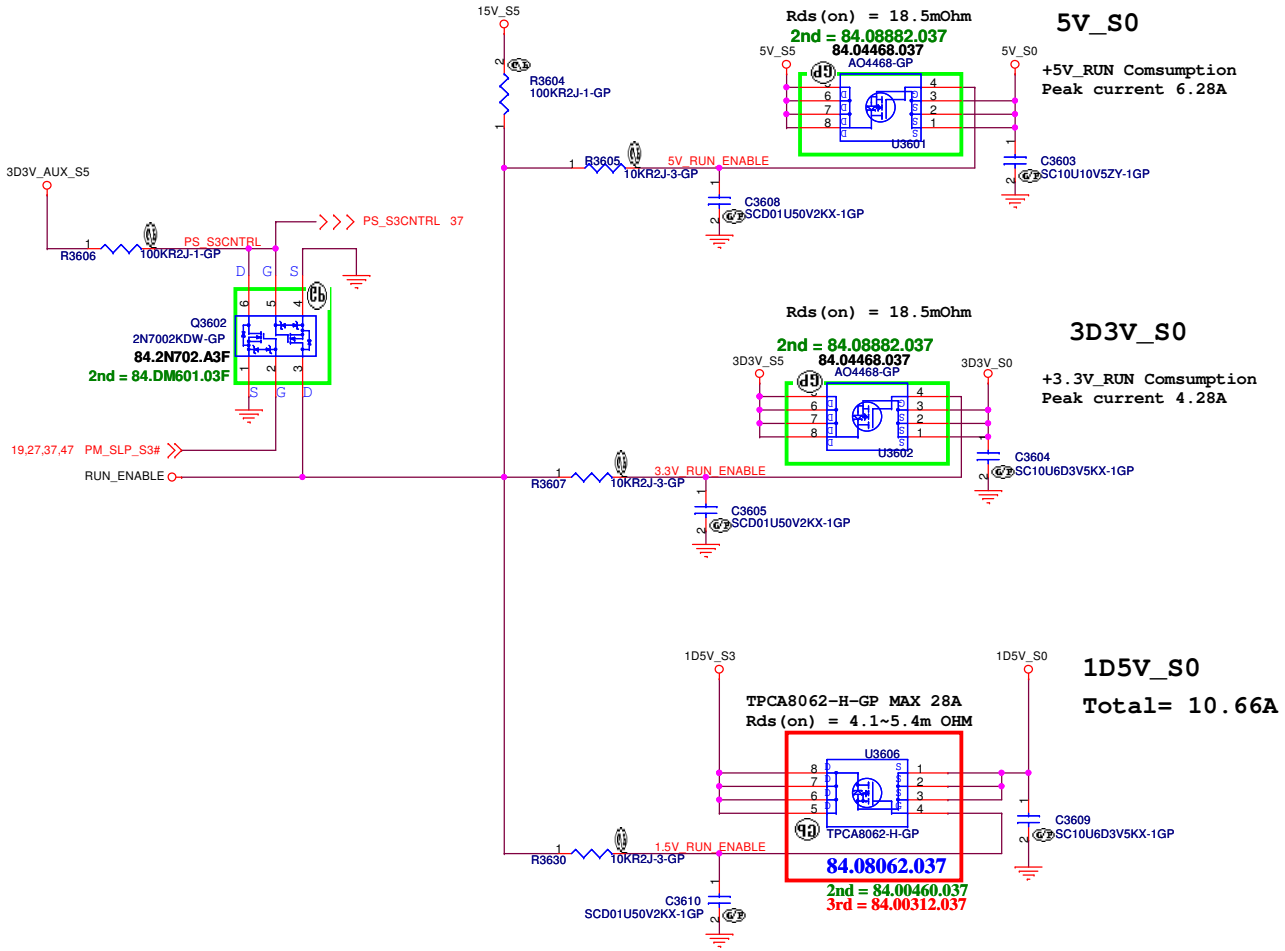
SSID = Reset.Suspend

Power Sequence





ROSA Run Power



5V_S0

+5V_RUN Comsumption
Peak current 6.28A

3D3V_S0

+3.3V_RUN Comsumption
Peak current 4.28A

1D5V_S0

Total= 10.66A

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable		
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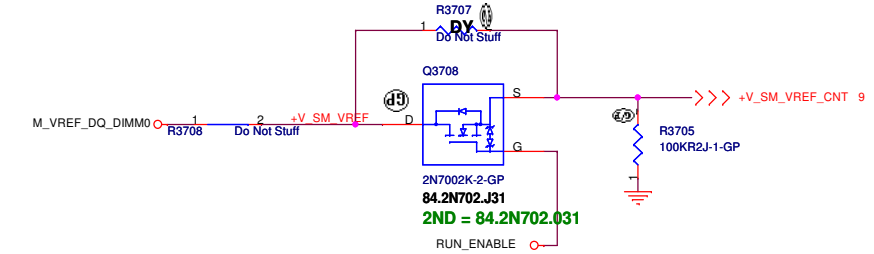
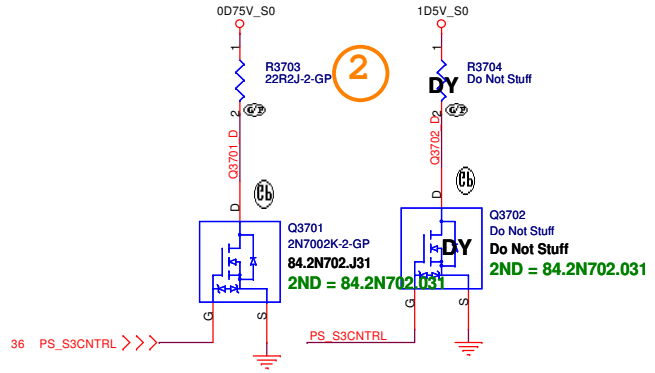
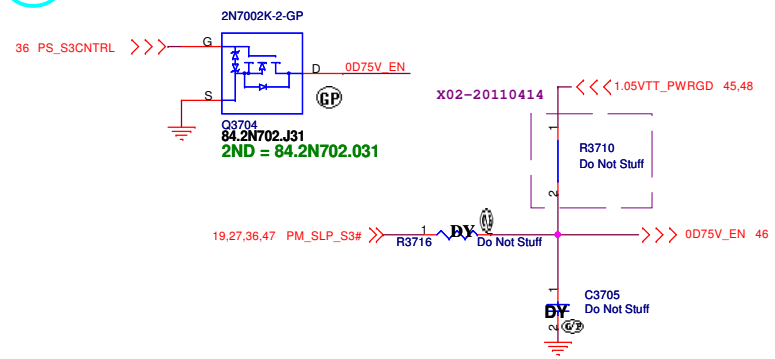
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



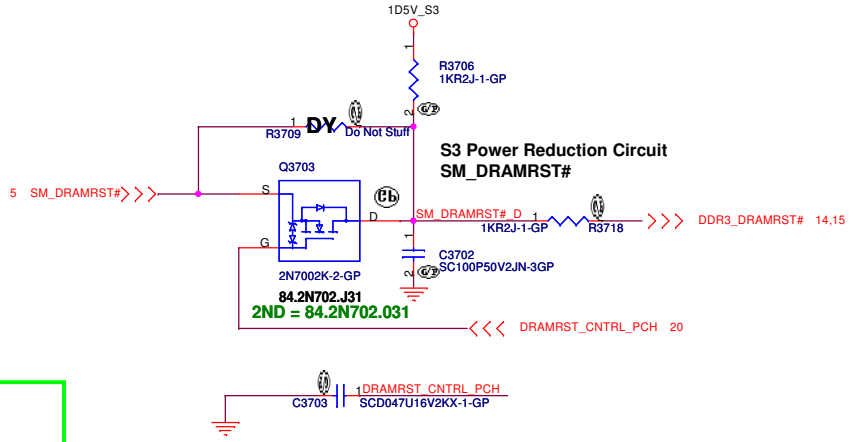
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



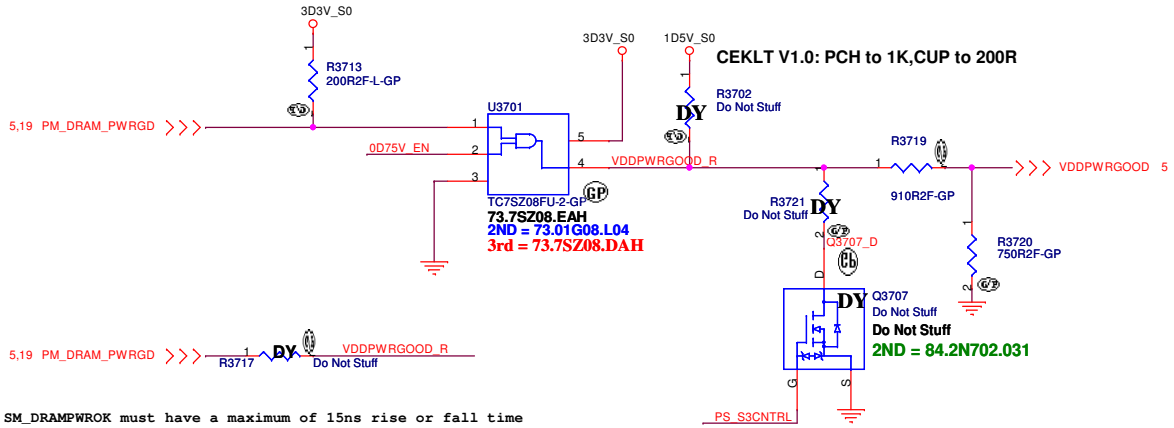
5 S3 Power Reduction



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

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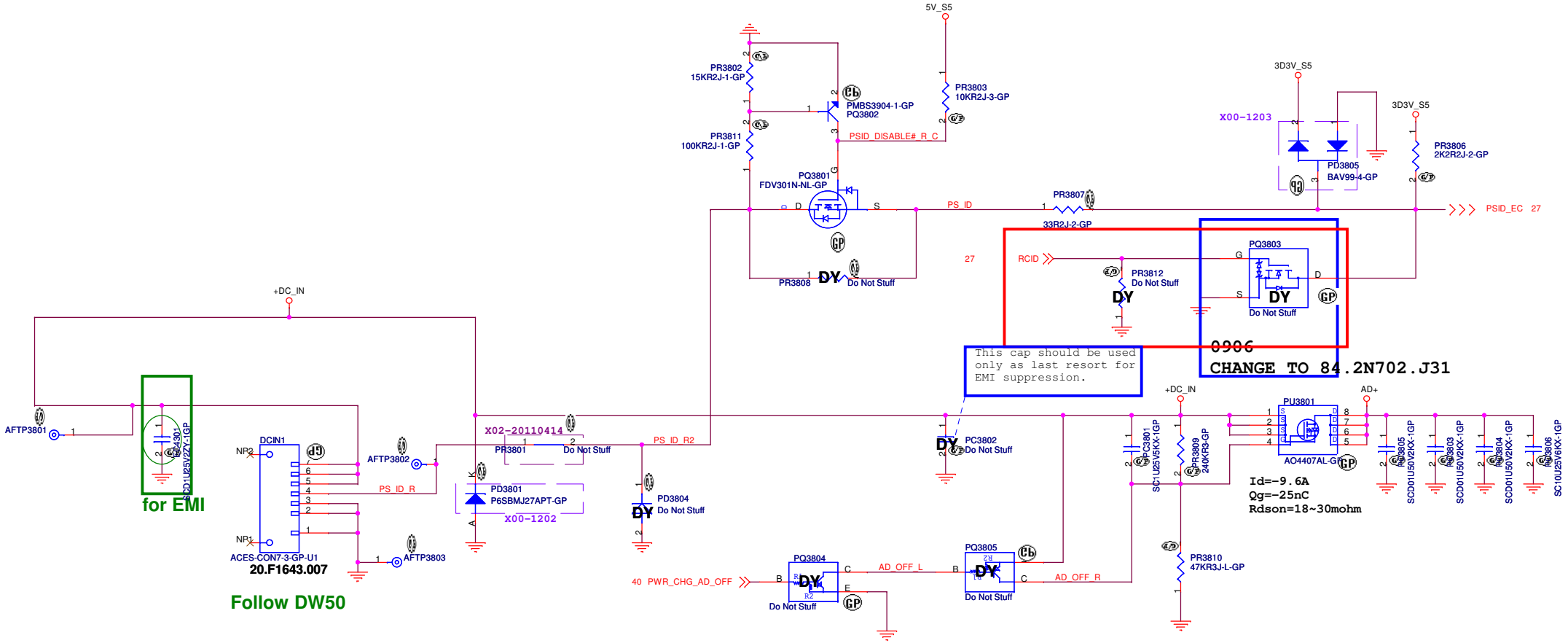
SSID = PWR.Support

DCin CONN



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
DCIN		
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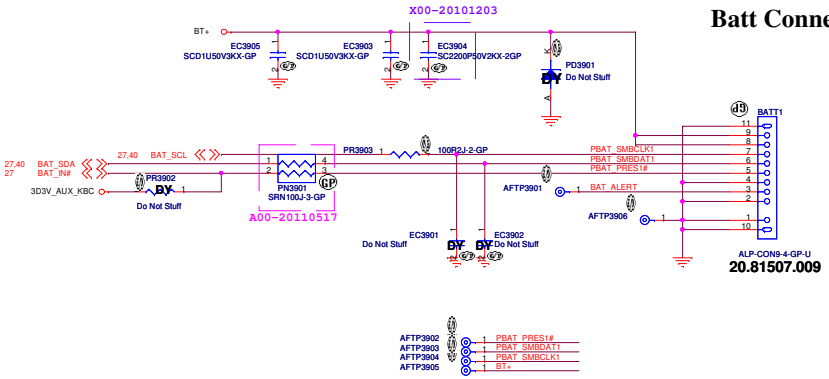
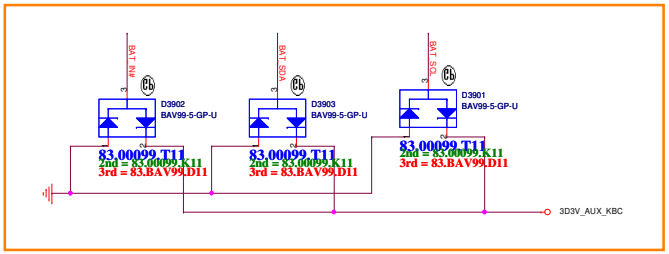
Batt Connecter



For actual location, need to be swap all pin

Close to Batt Connector



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

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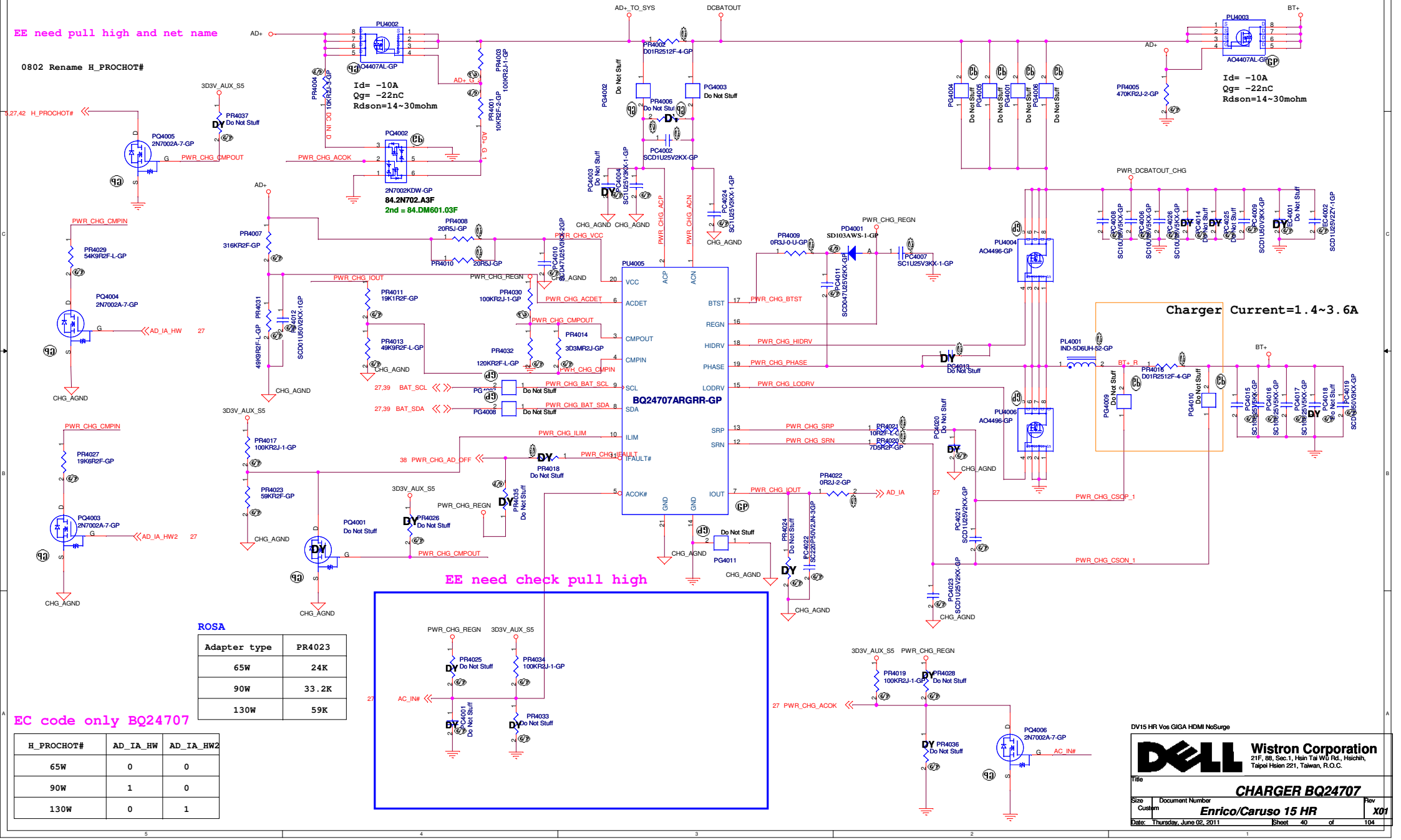
SSID = Charger



Adapter type	PR4023
65W	24K
90W	33.2K
130W	59K

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24707

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SSID = PWR.Plane.Regulator_5v3p3v

ROSA team

Design Current = 3.6A
5.7A<OCP< 6.7A

Design Current = 8.24A
12.3<OCP< 15.3A

Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

Do Not Stuff

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.20UH PCMC104T-2R2 Cyntec 7mohm Isat =27Arms 68.2R210.20C
O/P cap: 330U6.3V M6.3*5.7 15mOhm 3.16Arms Matsuki/77.53371.04L
H/S: TPC8061-H / 21mohm/30mOhm@4.5Vgs/ 84.08061.037
L/S: TPC8065-H / 12mohm/15mOhm@4.5Vgs/ 84.08065.037

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2U PCMC063T-2R2MN Cyntec 20mohm Isat =14Arms 68.2R210.20B
O/P cap: 330U6.3V M6.3*5.7 15mOhm 3.16Arms Matsuki/77.53371.04L
H/S: TPCC8061-H NC 8P / 21mohm/29mOhm@4.5Vgs/ 84.08061.A37
L/S: TPCC8065-H NC 8P / 12.1mohm/17.4mOhm@4.5Vgs/ 84.08065.A37

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V/3D3V(TPS51123RGER)

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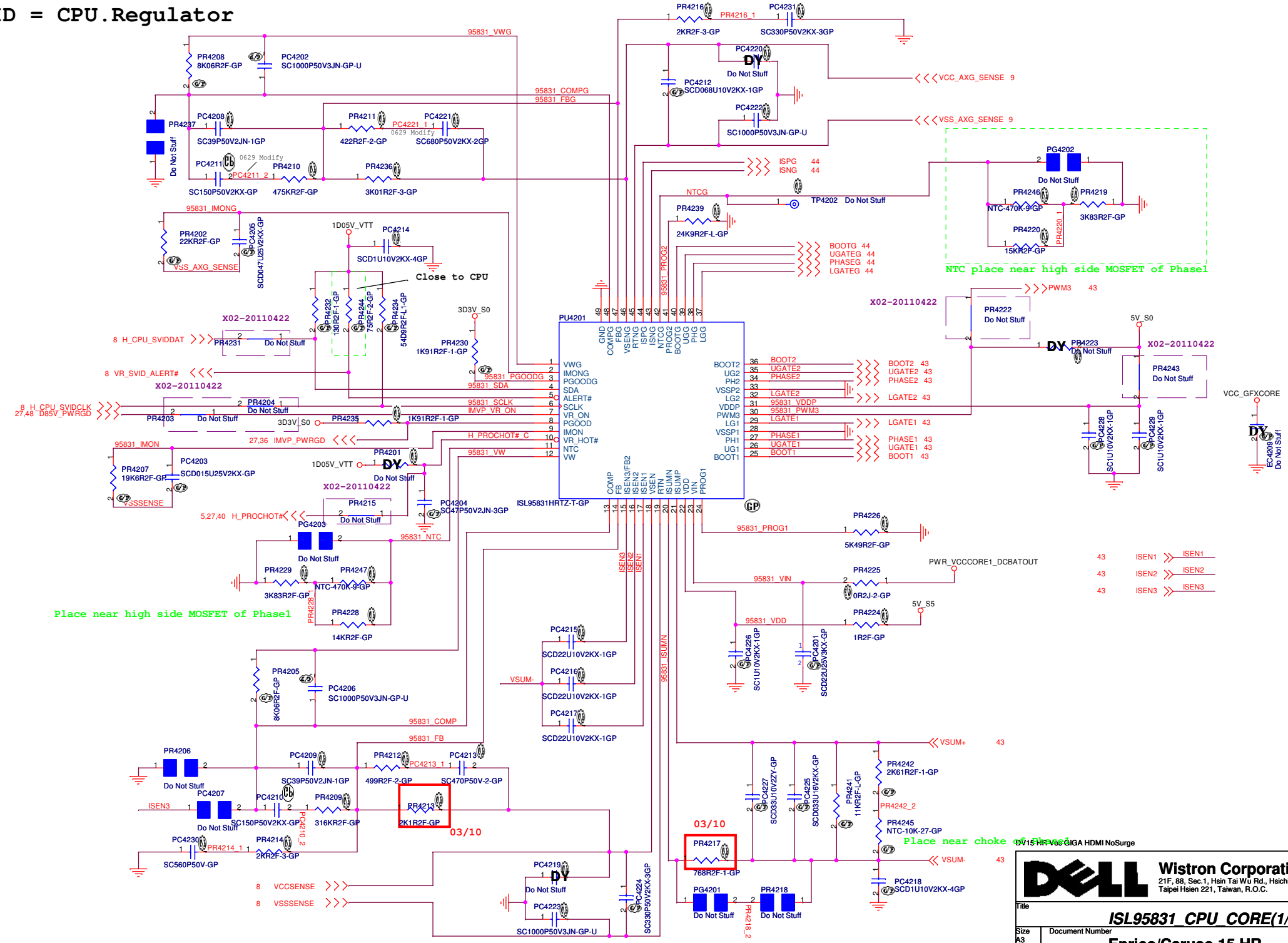
SSID = CPU.Regulator



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95831_CPU_CORE(1/3)

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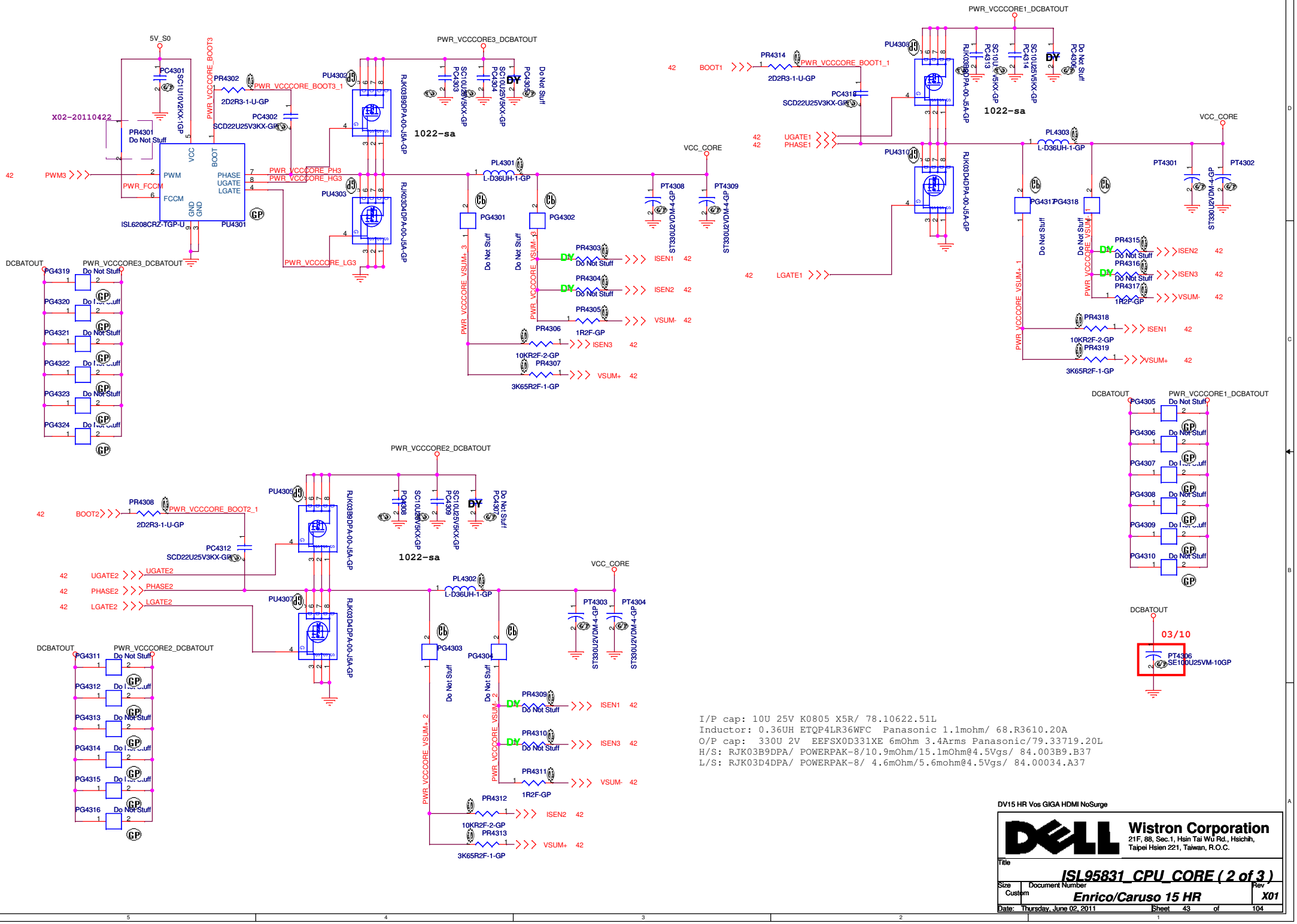
5V_S0
PC4301
SC1U10V2KX-1GP
X02-20110422
PR4301
Do Not Stuff
PWM3
PWR_FCCM
PWM
FCCM
VCC
BOOT
PHASE
UGATE
LGATE
GND
GND
ISL6208CRZ-TGP-U
PU4301
PWR_VCCCORE_BOOT3
PR4302
2D2R3-1-U-GP
PWR_VCCCORE_BOOT3_1
PC4302
SCD22U25V3KX-GP
PWR_VCCCORE_PH3
PWR_VCCCORE_HG3
PWR_VCCCORE_LG3
PU4302
PU4303
RJK0389DPA-00-J5A-GP
RJK03D4DPA-00-J5A-GP
1022-sa
PWR_VCCCORE3_DCBATOUT
PC4303
SC10U25V5KX-GP
PC4304
SC10U25V5KX-GP
DY
PC4305
Do Not Stuff
PL4301
L-D36UH-1-GP
VCC_CORE
PT4308
PT4309
ST330U2VDM-4-GP
PG4301
PG4302
Do Not Stuff
PWR_VCCCORE_VSUM+_3
PWR_VCCCORE_VSUM-_3
PR4303
PR4304
PR4305
ISEN1
ISEN2
VSUM-
PR4306
10KR2F-2-GP
PR4307
3K65R2F-1-GP
ISEN3
VSUM+
42
DCBATOUT
PG4319
PG4320
PG4321
PG4322
PG4323
PG4324
PWR_VCCCORE1_DCBATOUT
PR4314
2D2R3-1-U-GP
PWR_VCCCORE_BOOT1_1
PC4313
PC4314
PC4315
BOOT1
UGATE1
PHASE1
LGATE1
PU4309
PU4310
PL4303
PT4301
PT4302
ST330U2VDM-4-GP
PG4317
PG4318
PR4315
PR4316
PR4317
1R2F-GP
PR4318
10KR2F-2-GP
PR4319
3K65R2F-1-GP
PWR_VCCCORE_VSUM+_1
PWR_VCCCORE_VSUM-_1
PG4305
PG4306
PG4307
PG4308
PG4309
PG4310
PWR_VCCCORE2_DCBATOUT
PR4308
2D2R3-1-U-GP
PWR_VCCCORE_BOOT2_1
PC4312
SCD22U25V3KX-GP
BOOT2
UGATE2
PHASE2
LGATE2
PU4305
PU4307
PC4308
PC4309
PC4307
PL4302
PT4303
PT4304
PG4303
PG4304
PR4309
PR4310
PR4311
PR4312
PR4313
PWR_VCCCORE_VSUM+_2
PWR_VCCCORE_VSUM-_2
PG4311
PG4312
PG4313
PG4314
PG4315
PG4316
03/10
PT4306
SE100U25VM-10GP
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 0.36UH ETQP4LR36WFC Panasonic 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37
DV15 HR Vos GIGA HDMI NoSurge
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL95831_CPU_CORE (2 of 3)
Size
Custom
Document Number
Enrico/Caruso 15 HR
Rev
X01
Date: Thursday, June 02, 2011
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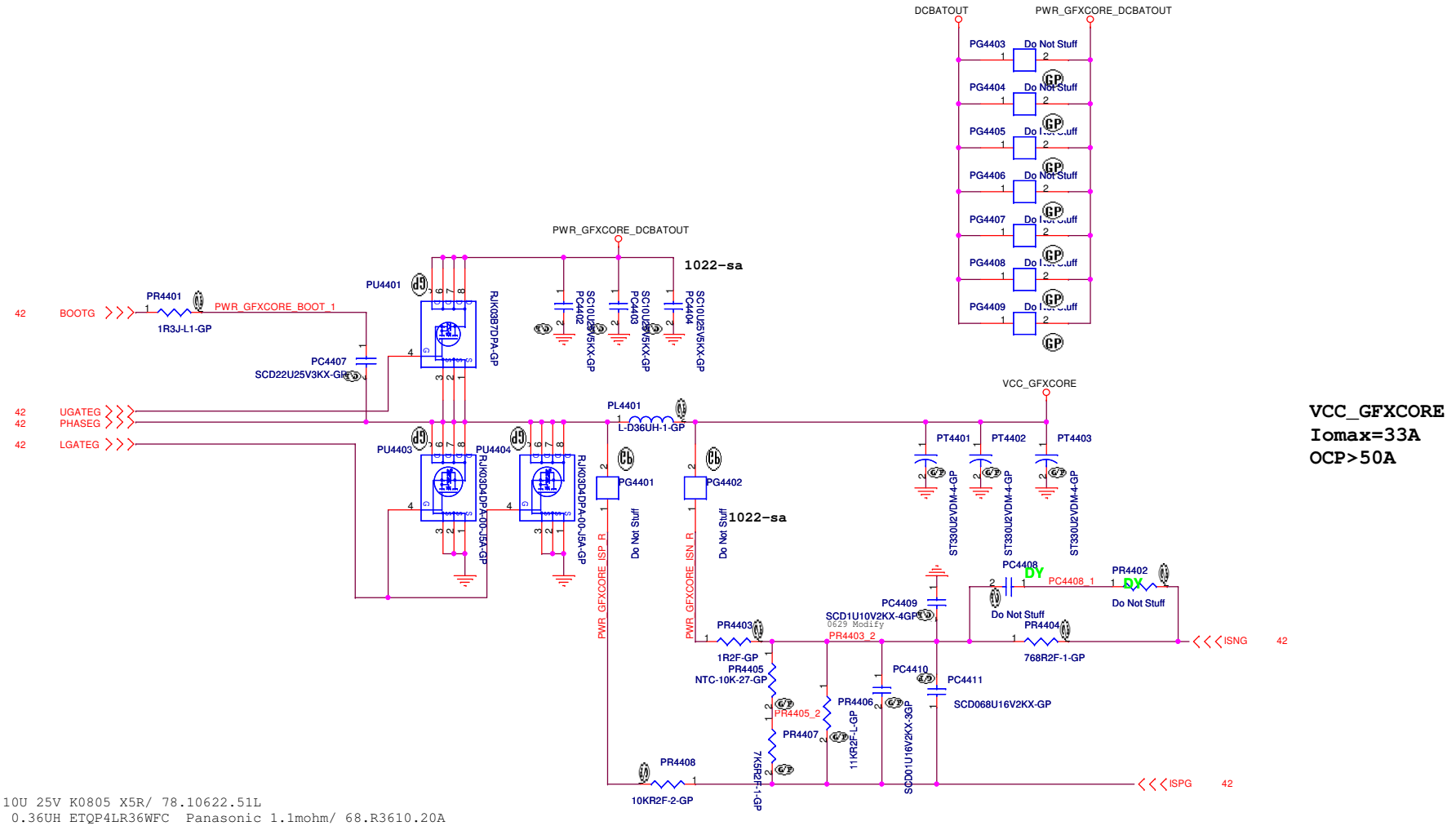
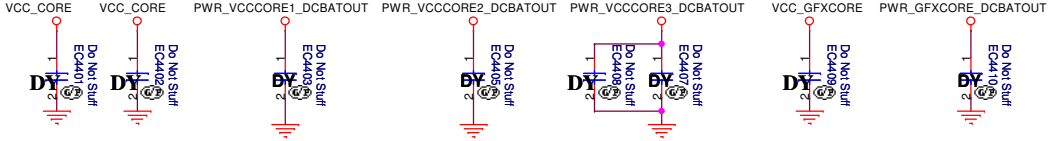


VCC_GFXCORE
Iomax=33A
OCP>50A

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 0.36UH ETQP4LR36WFC Panasonic 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
H/S: RJK03B7DPA NC WPAK 8P/7.7mOhm/10.7mOhm@4.5Vgs/84.003B7.037
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

EMI/ESD



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95831_CPU_CORE(3/3)

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

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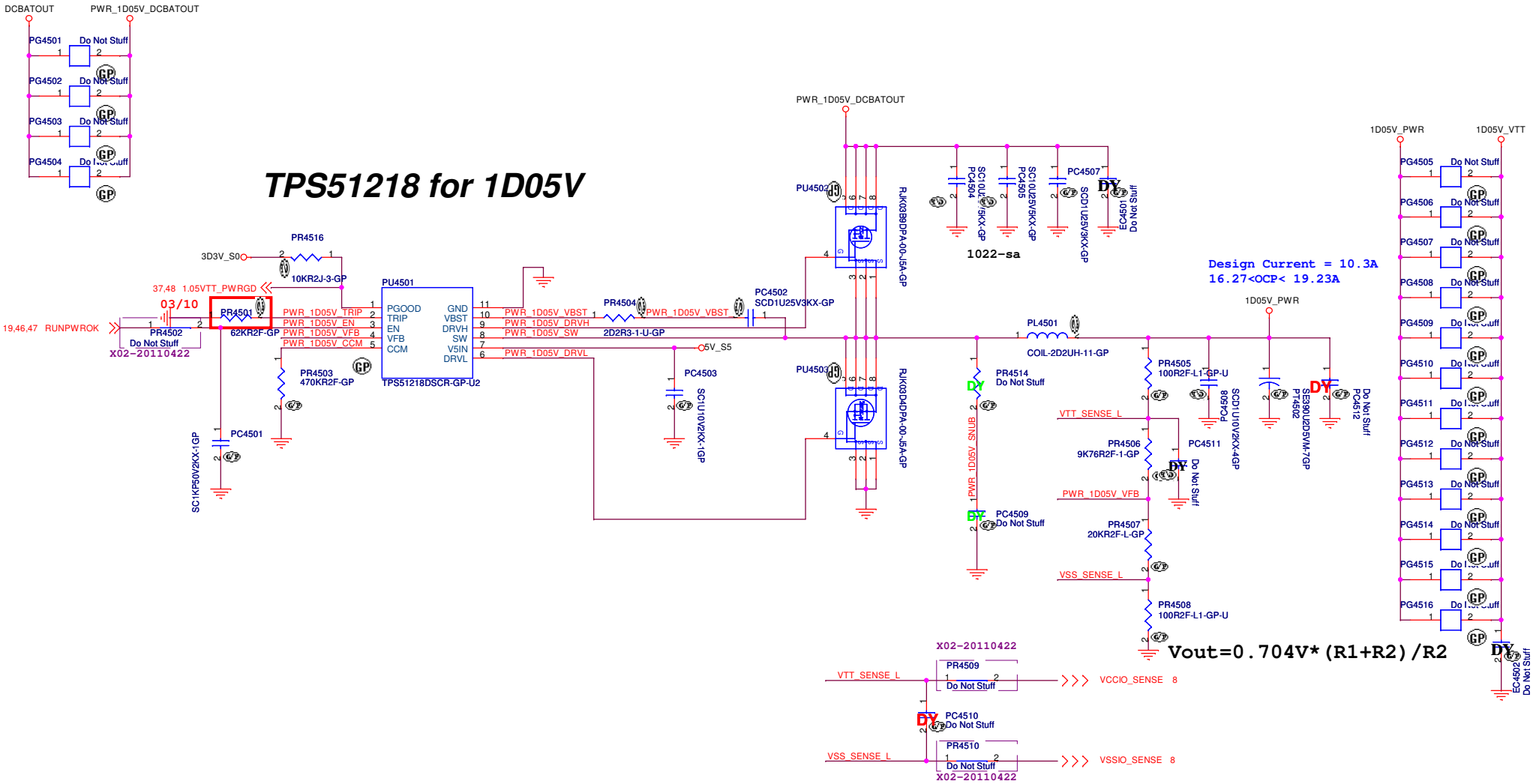

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.20UH PCMC104T-2R2 Cyntec 7mohm Isat =27Arms 68.2R210.20C
O/P cap: 390U 2.5V M 6.3*5.7/ 10mOhm 3.87Arms Matsuki/79.3971V.30L
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218_+1.05V_VTT

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

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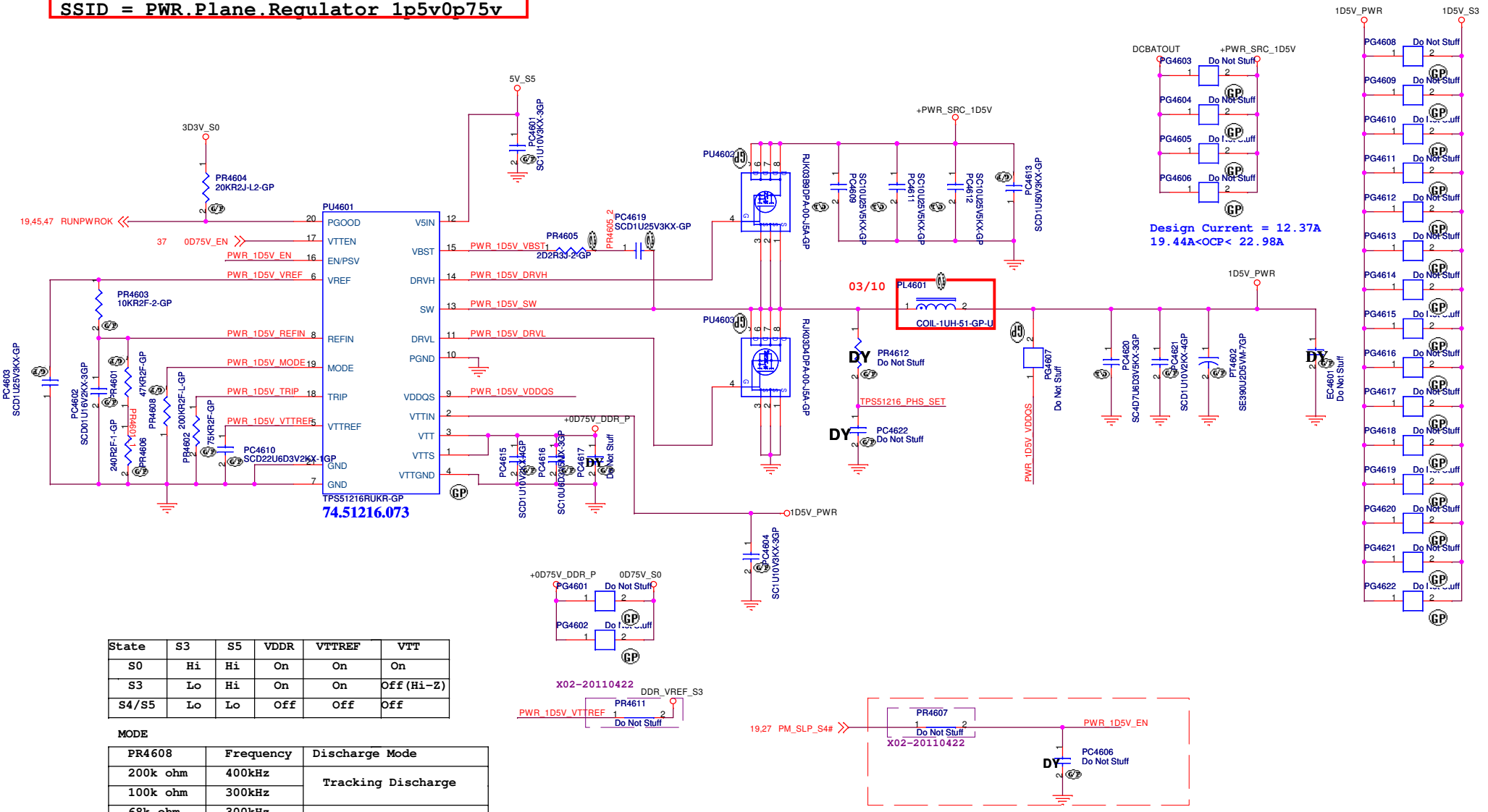
SSID = PWR.Plane.Regulator 1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.0UH PCMB104T-1R0M Cyntec 3mohm Isat =28Arms 68.1R01C.10Q
O/P cap: 390U 2.5V M 6.3*5.7/ 10mOhm 3.87Arms Matsuki/79.3971V.30L
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116_+1.5V_SUS

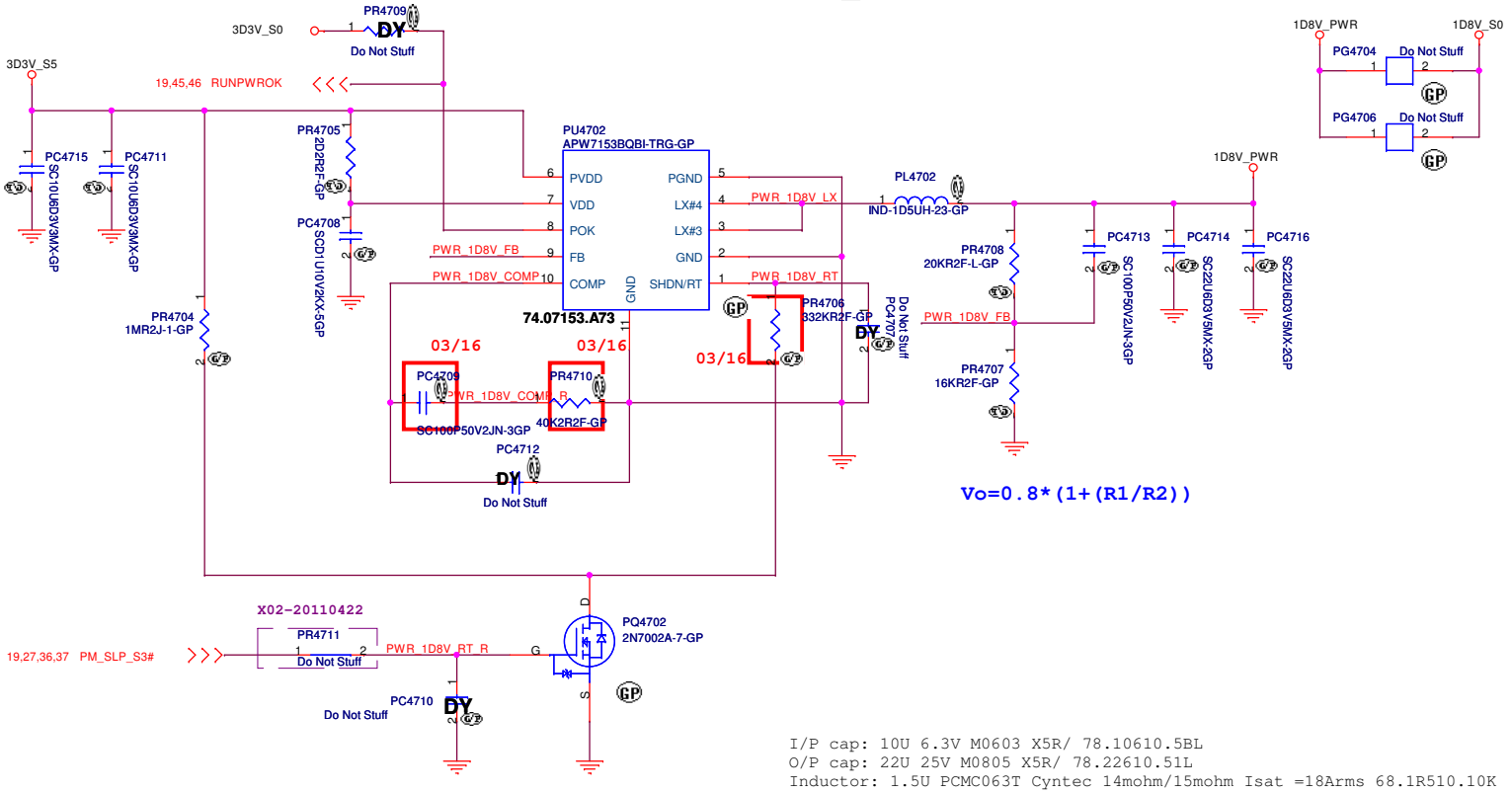
Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

Date: Thursday, June 02, 2011 Sheet 46 of 104

SSID = PWR.Plane.Regulator_1D8V_S0

+1.8V_RUN
Design current = 0.87A

APW7153B for 1D8V_S0



Vo=0.8*(1+(R1/R2))

I/P cap: 10U 6.3V M0603 X5R/ 78.10610.5BL
O/P cap: 22U 25V M0805 X5R/ 78.22610.51L
Inductor: 1.5U PCMC063T Cyntec 14mohm/15mohm Isat =18Arms 68.1R510.10K

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51311 for 1D8V_S0

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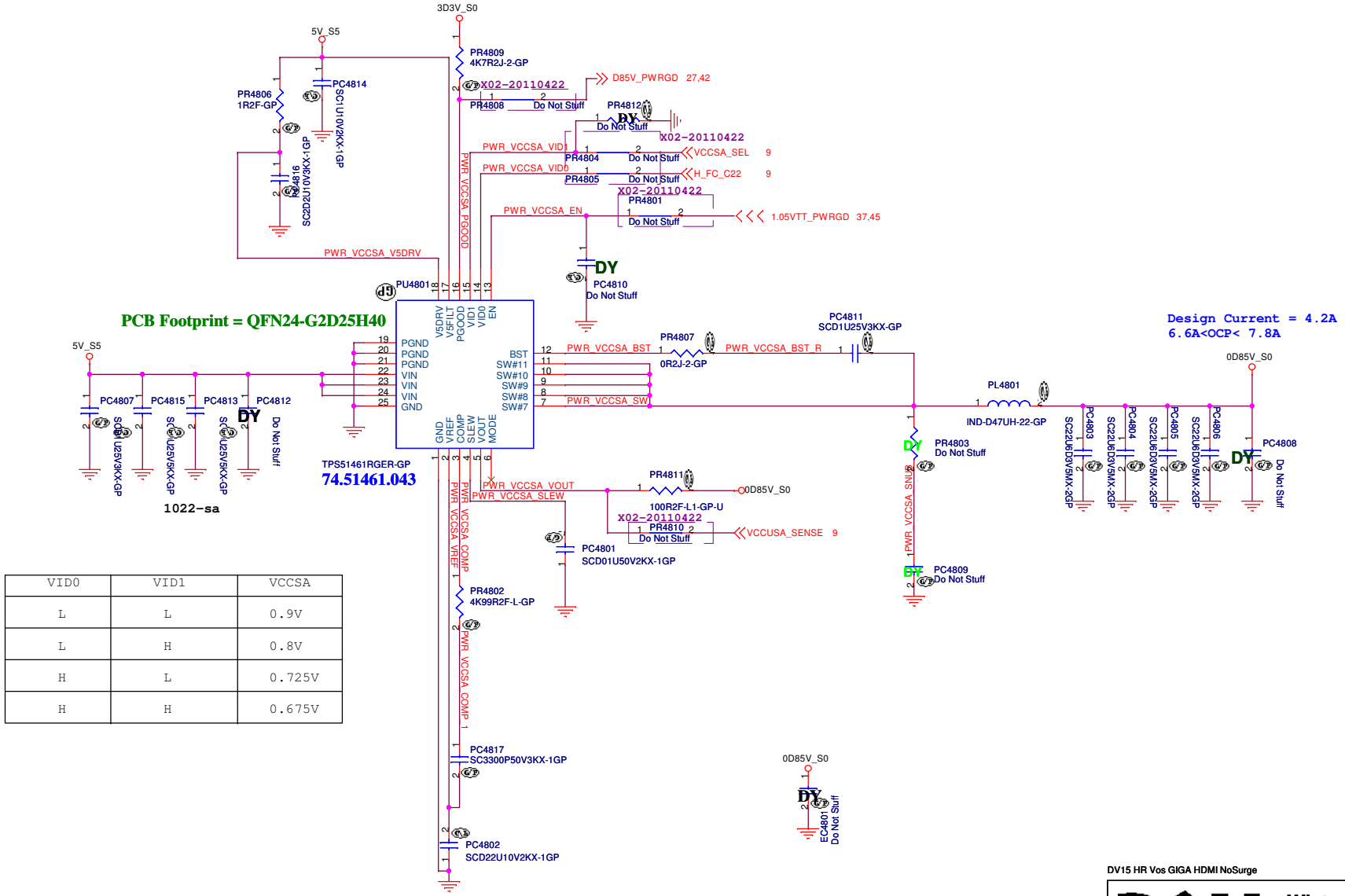
TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51461_VCCSA

Size	Document Number	Rev
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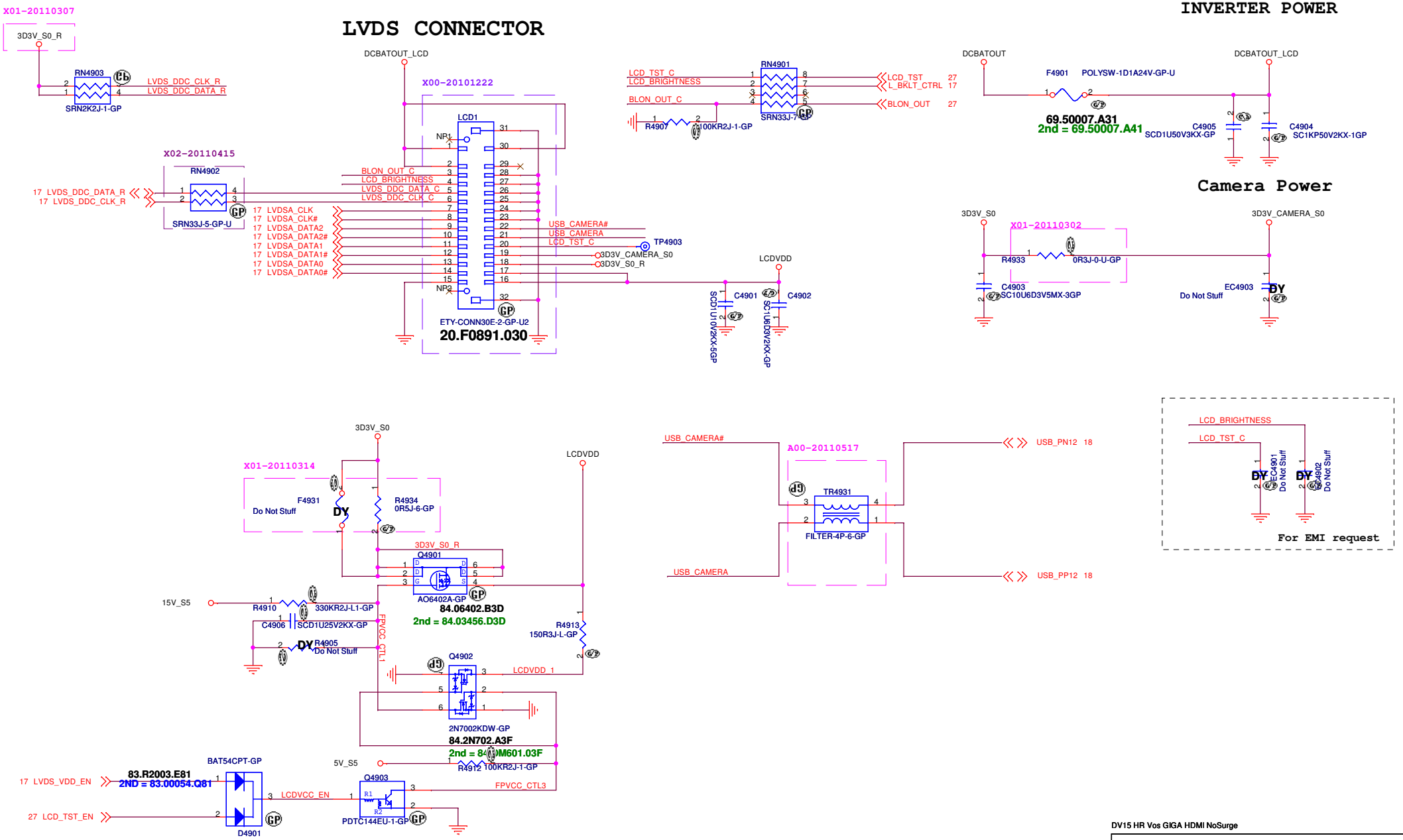

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LCD Connector*

Size	Document Number	Rev
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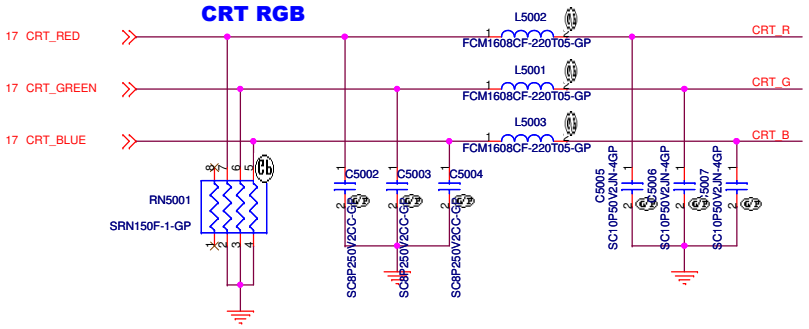
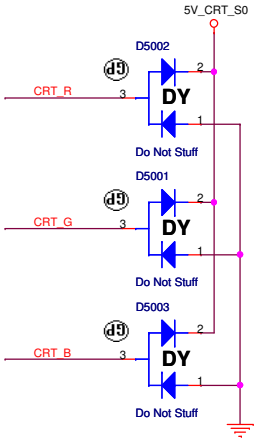
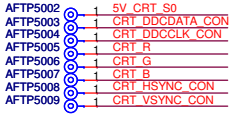
SSID = VIDEO

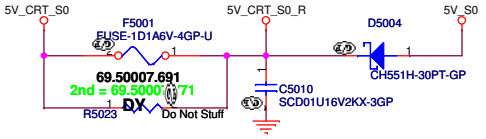
Layout Note:

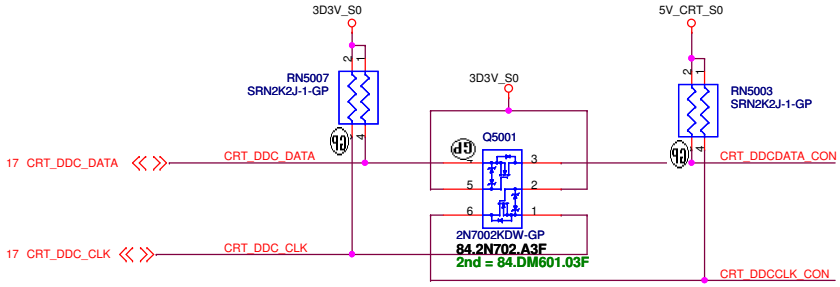
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

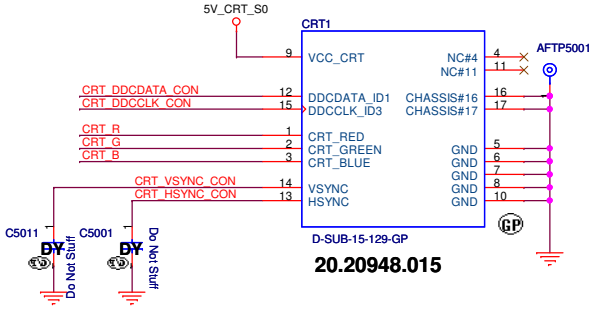




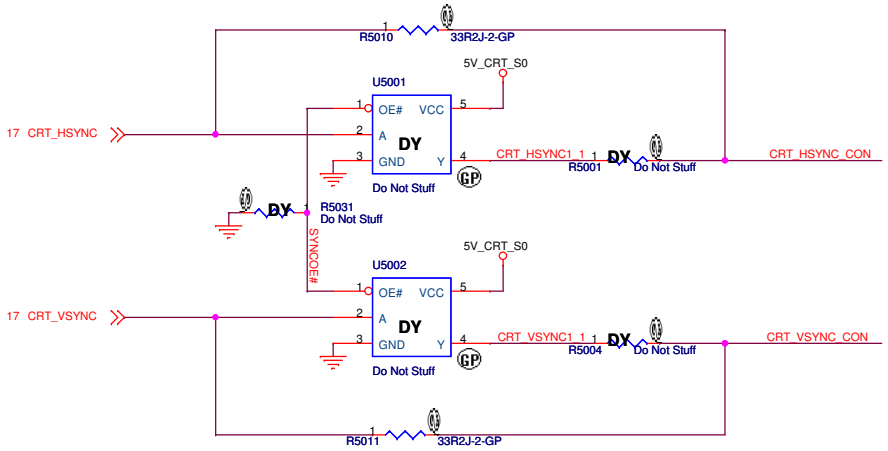


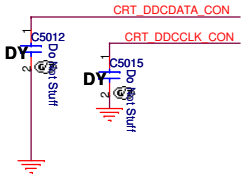






Hsync & Vsync





DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

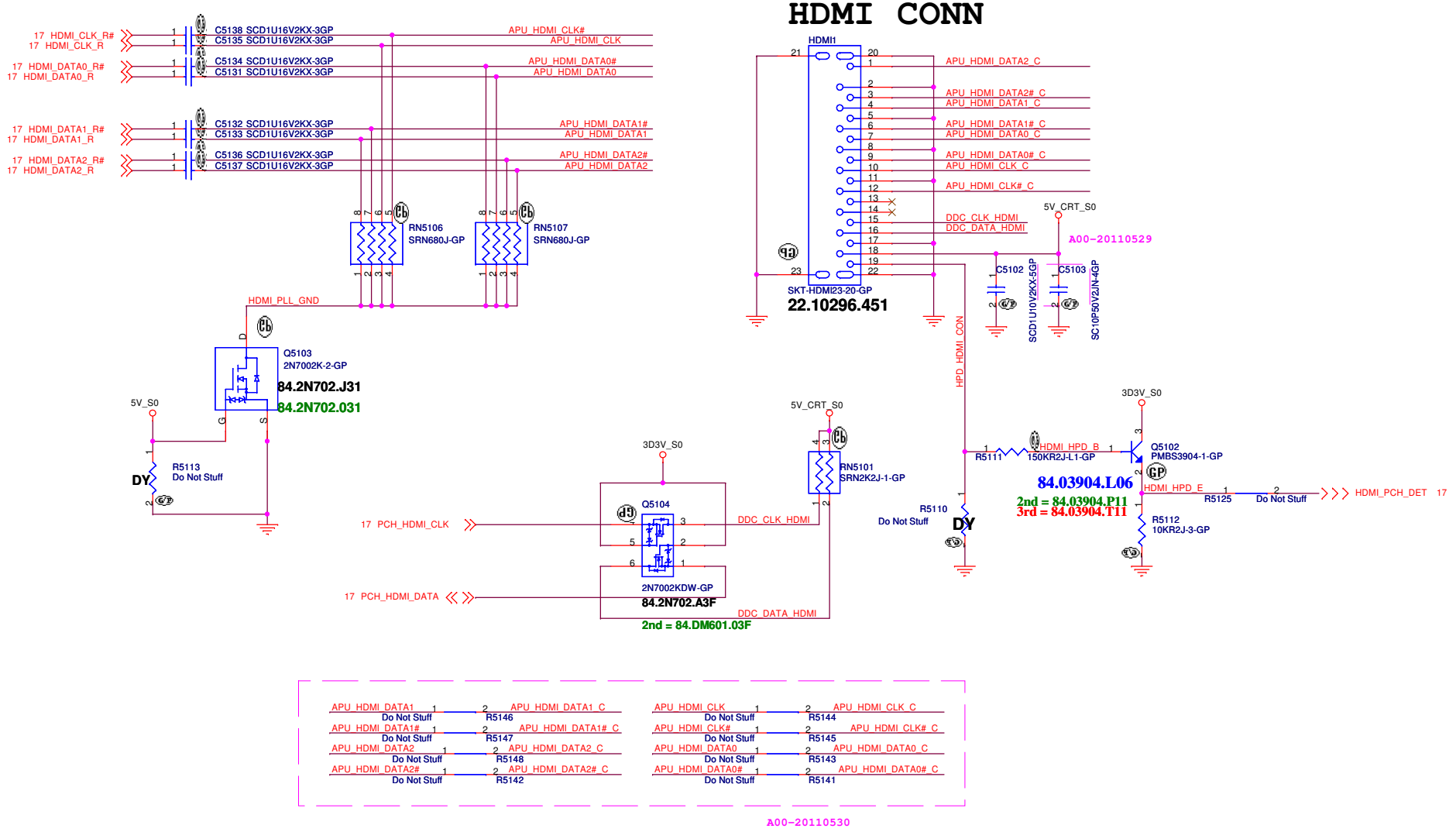
Title: CRT Connector

Size	Document Number	Rev
Custom	Enrico/Caruso 15 HR	X01

Date: Thursday, June 02, 2011 Sheet 50 of 104

SSID = VIDEO

HDMI CONN



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

Size	Document Number	Rev
A3	*Enrico/Caruso 15 HR*	*X01*

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

LVDS_Switch

Size	Document Number	Rev
A3	***Enrico/Caruso 15 HR***	***X01***

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
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Title

Reserved

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SSID = User.Interface

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Title: ITP/Fan Connector

Size	Document Number	Rev
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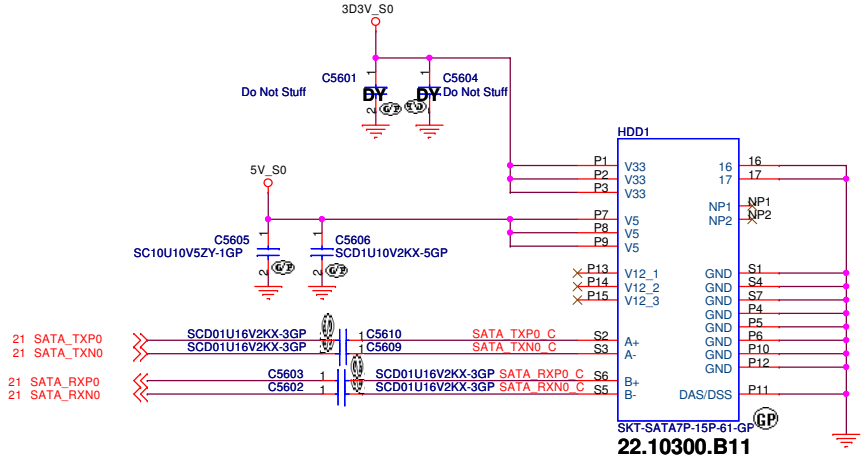
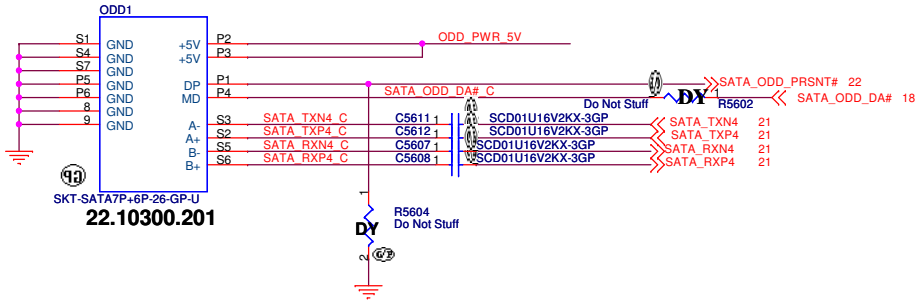
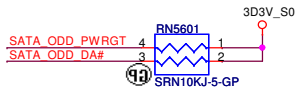
SSID = SATA

SATA HDD Connector

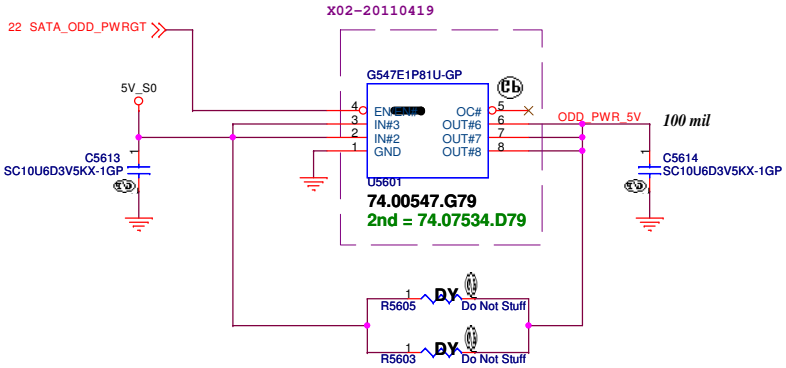


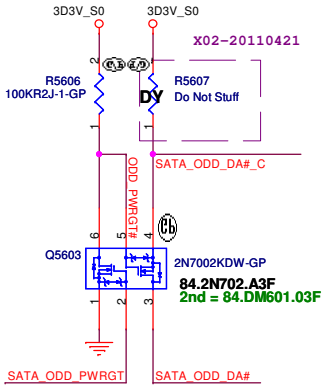
ODD Connector

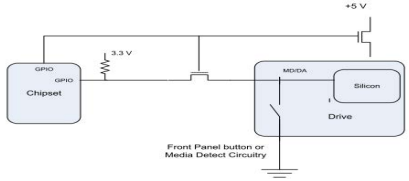




SUPPORT ZERO SATA ODD







When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
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Date: Thursday, June 02, 2011 Sheet 56 of 104

SSID = ESATA

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
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Title: ESATA

Size: A3 | Document Number: Enrico/Caruso 15 HR | Rev: X01

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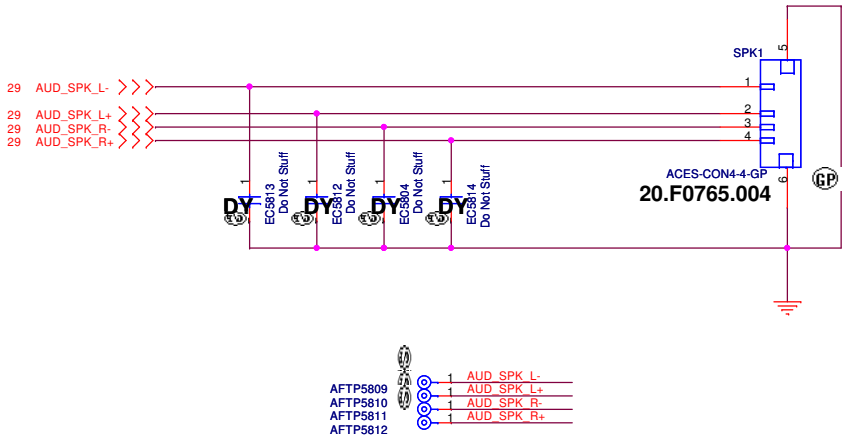
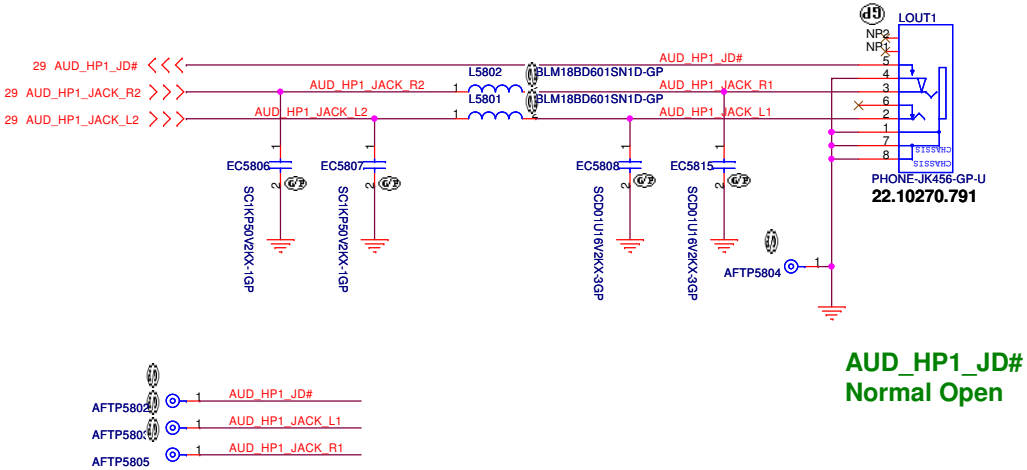
SSID = AUDIO

Speaker Connector

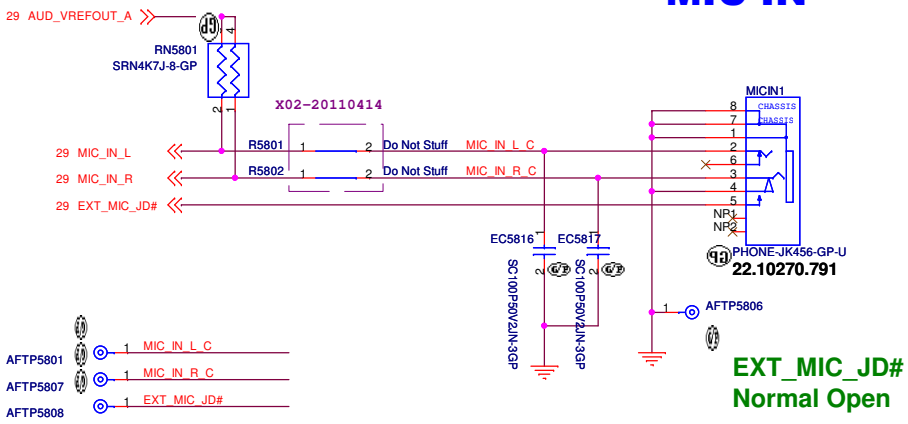


LINE1 OUT



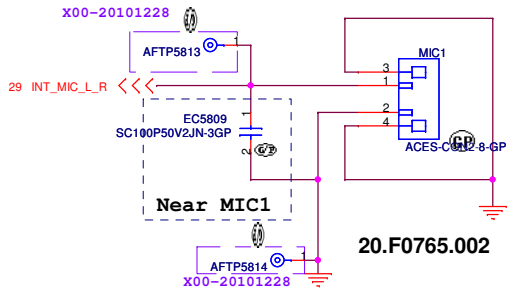
AUD_HP1_JD#
Normal Open

MIC IN



EXT_MIC_JD#
Normal Open

Internal Microphone



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	SPEAKER CONN	
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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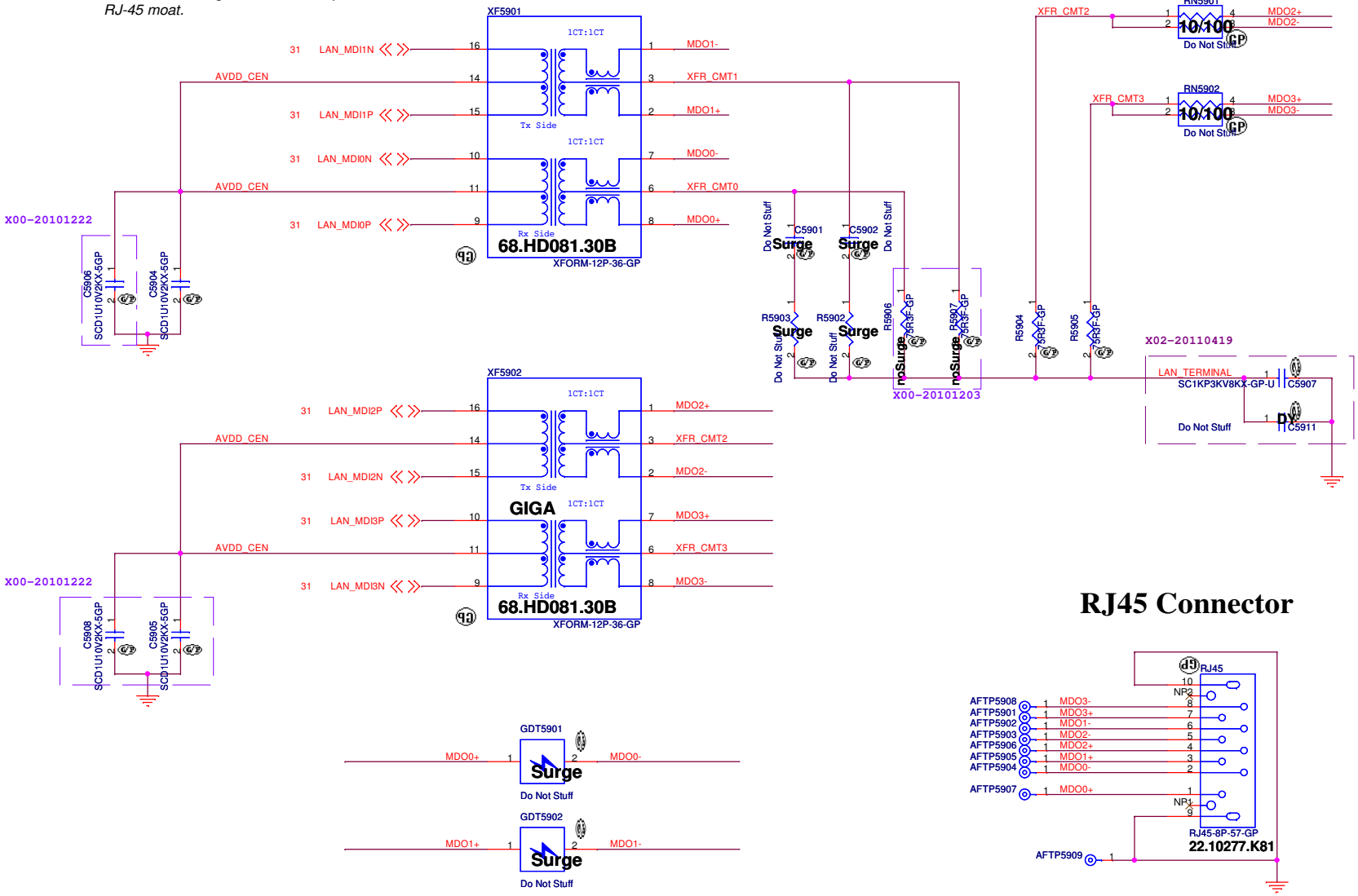
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

10/100M Lan Transformer



RJ45 Connector

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**

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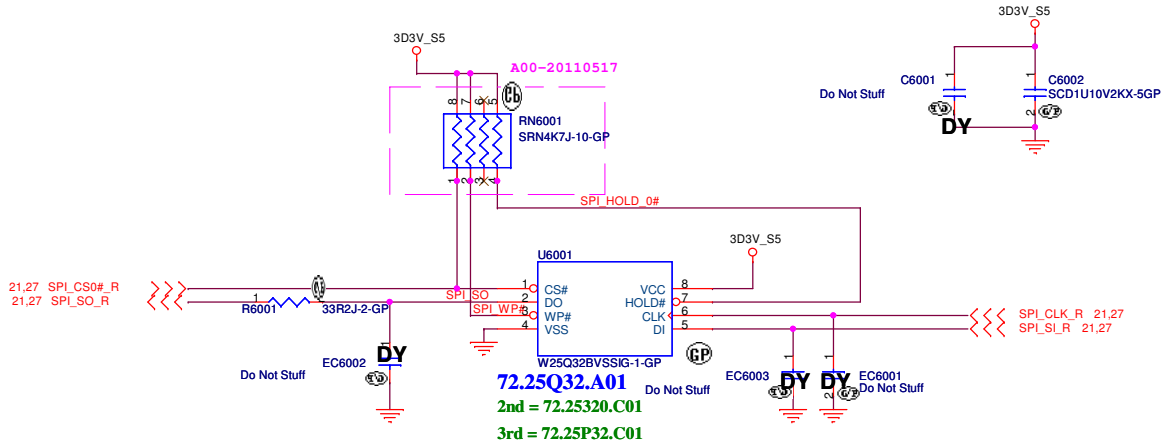
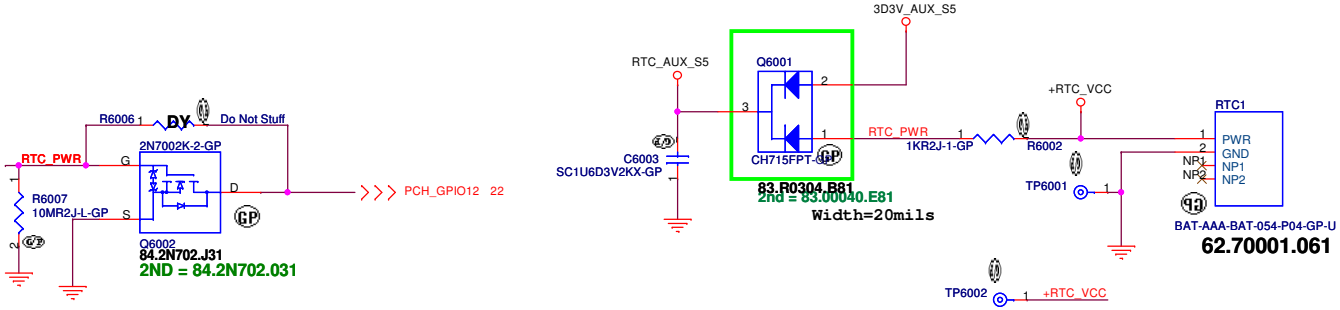
SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Flash/RTC		
Size: A3	Document Number: Enrico/Caruso 15 HR	Rev: X01
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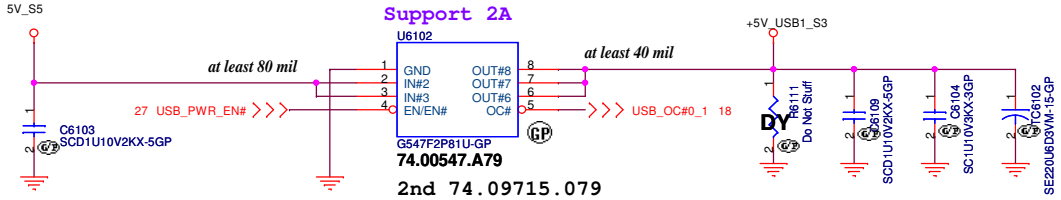
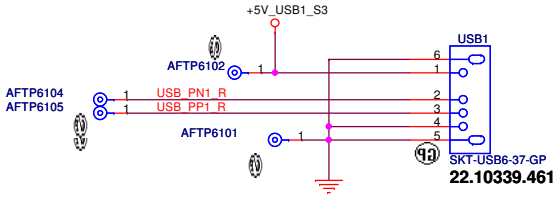
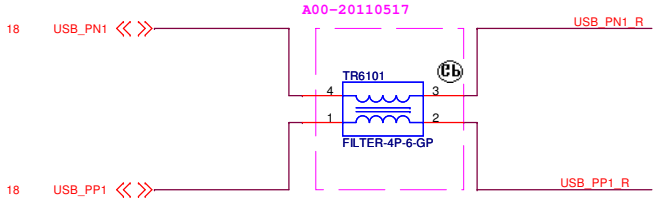
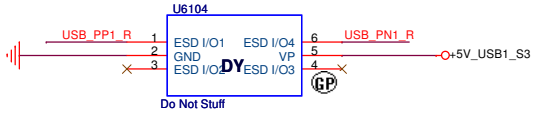
SSID = USB

Left USB Power x1

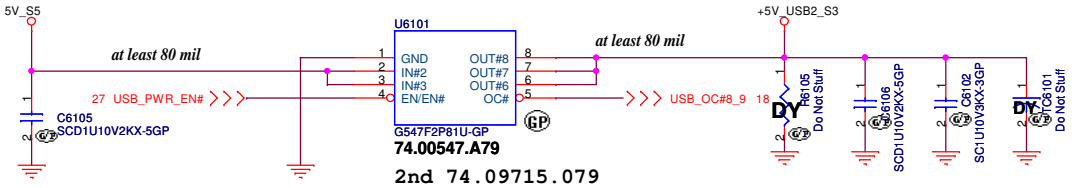


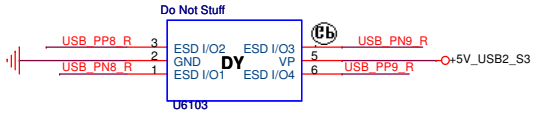




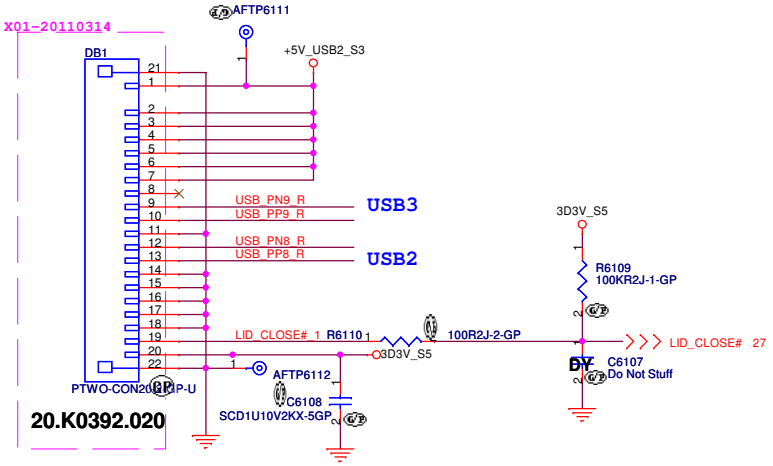


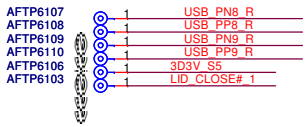
Right USB Power x2

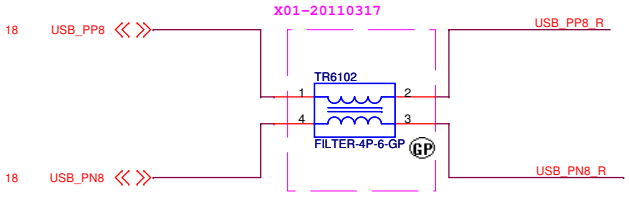


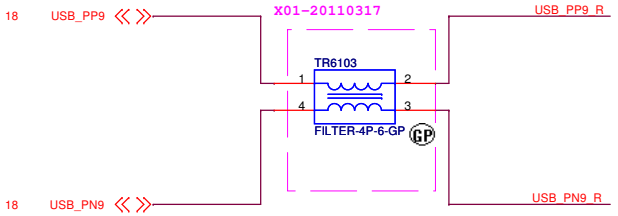


Pitch=0.5mm









DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Power SW

Size | Document Number: Enrico/Caruso 15 HR | Rev: X01

Date: Thursday, June 02, 2011 | Sheet 61 of 104

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	*Enrico/Caruso 15 HR*	*X01*

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SSID = User.Interface

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Bluetooth*

Size	Document Number	Rev
A3	*Enrico/Caruso 15 HR*	*X01*

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

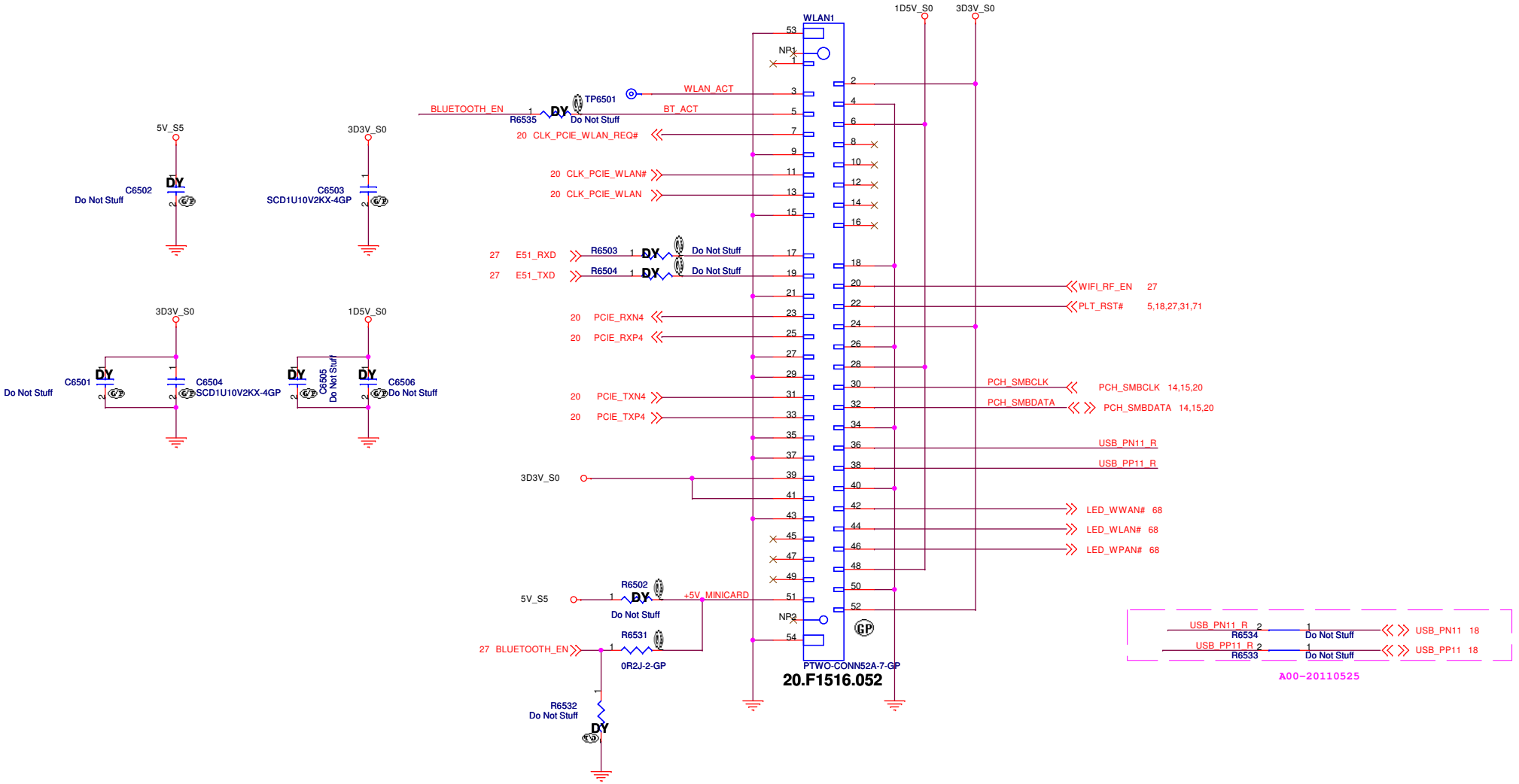
RESERVED

Size	Document Number	Rev
A3	*Enrico/Caruso 15 HR*	*X01*

Date: Thursday, June 02, 2011 Sheet 64 of 104

SSID = Wireless

Mini Card Connector(802.11b/g/n)



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

Size	Document Number	Rev
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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	*Enrico/Caruso 15 HR*	*X01*

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

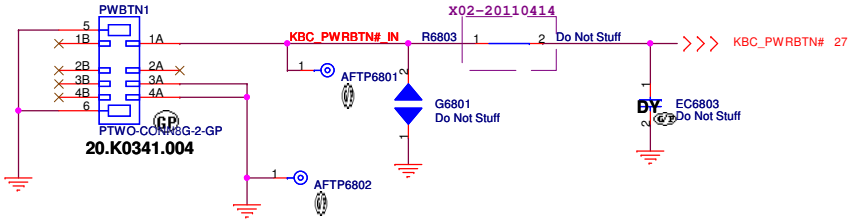
Title: *Reserved*

Size: A3 | Document Number: *Enrico/Caruso 15 HR* | Rev: *X01*

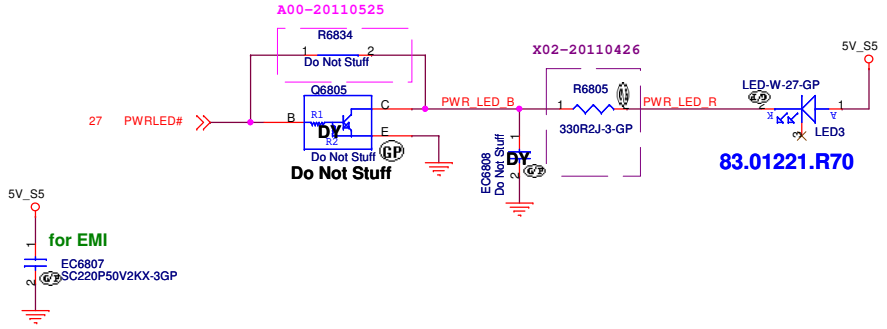
Date: Thursday, June 02, 2011 | Sheet 67 of 104

SSID = User.Interface

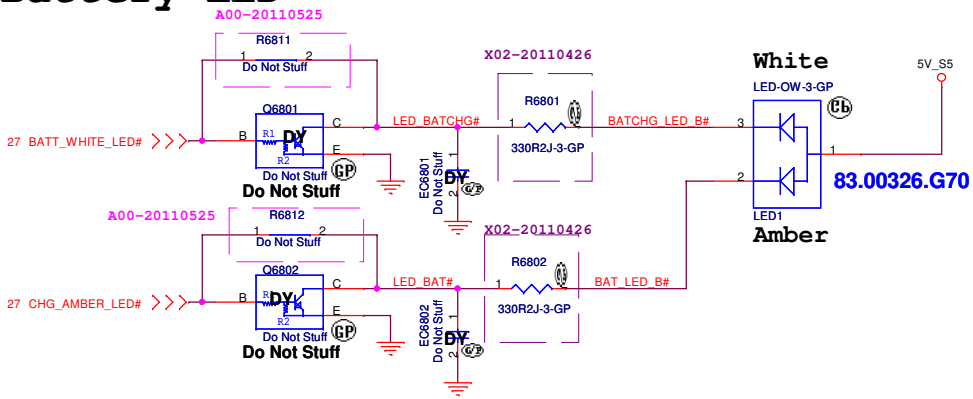
Power BTN Connector



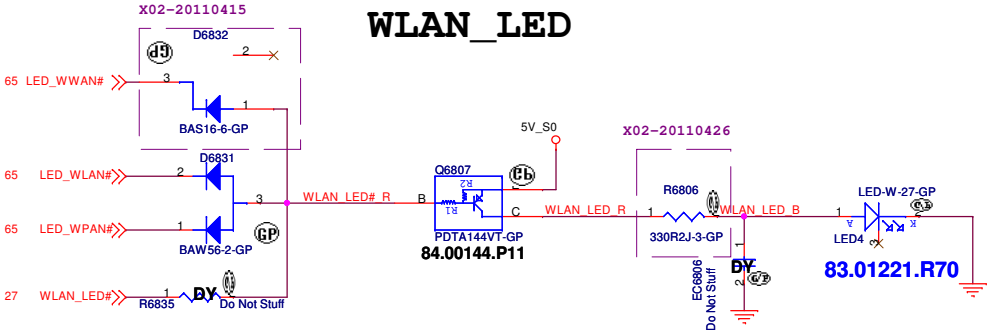
Power LED



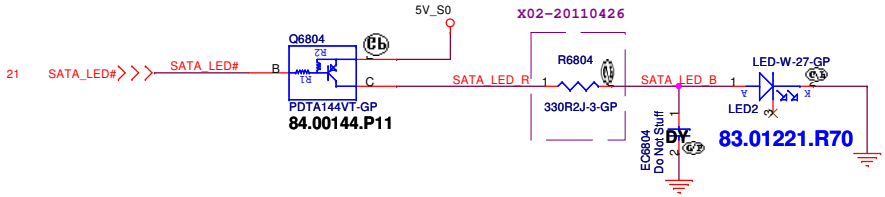
Battery LED



WLAN_LED



HDD LED



LED Location from left to right
(MB, Top View)

LED3	LED2	LED1	LED4
PWR	HDD	Battery	WiFi

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

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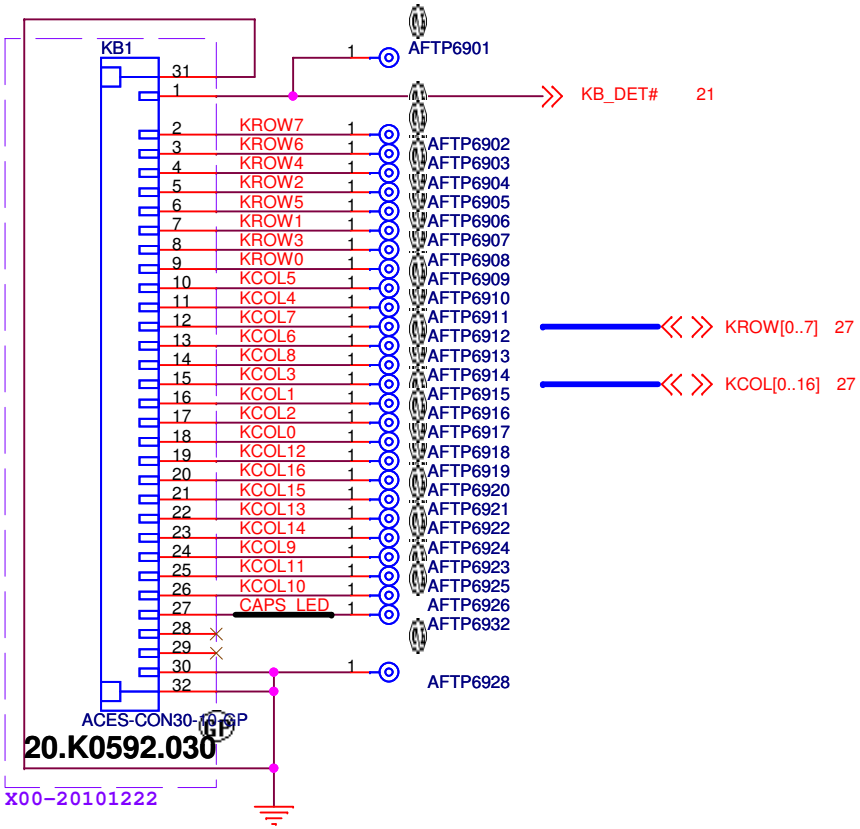
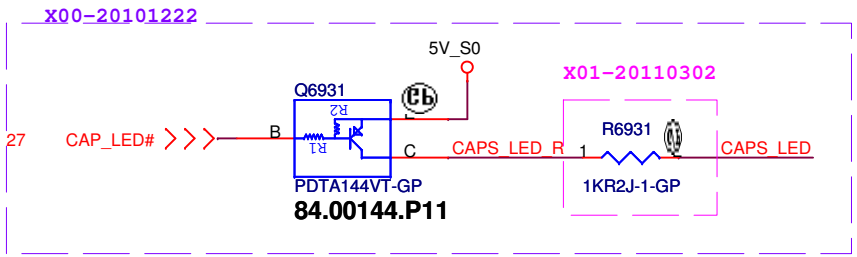
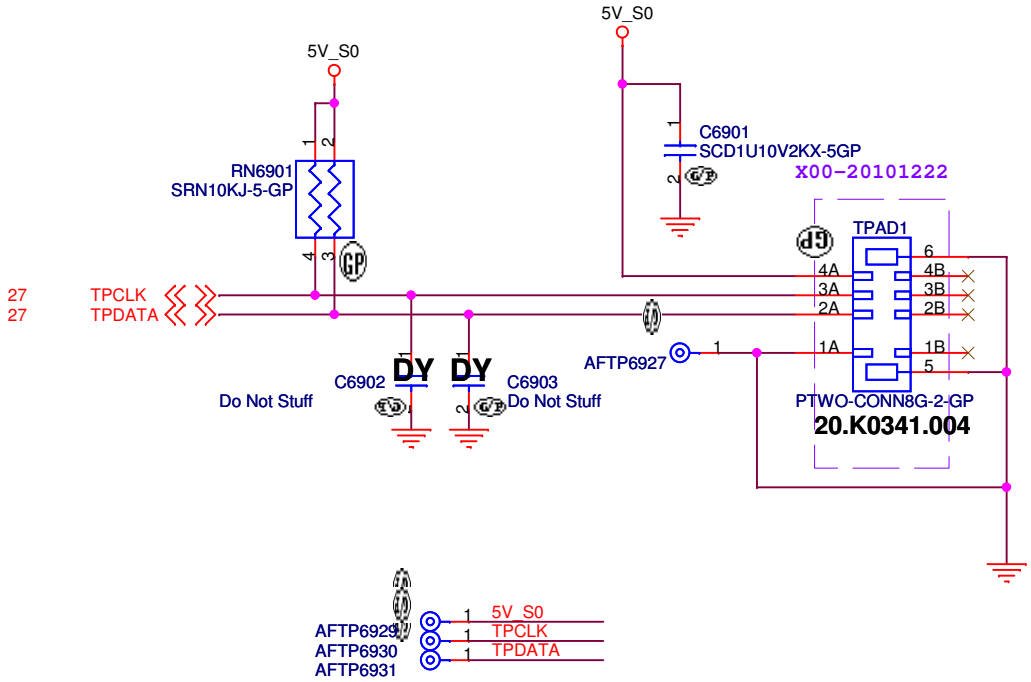
Internal KeyBoard Connector





TouchPad Connector



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Key Board/Touch Pad***

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Hall Sensor

Size	Document Number	Rev
A3	**Enrico/Caruso 15 HR**	**X01**

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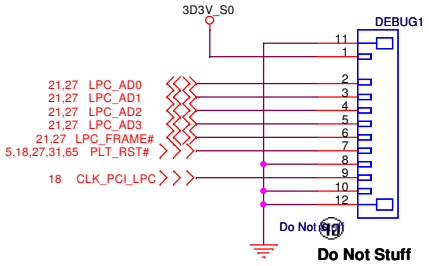

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Dubug connector*		
Size: A3	Document Number: *Enrico/Caruso 15 HR*	Rev: *X01*
Date: Thursday, June 02, 2011	Sheet 71 of 104	

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

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DV15 HR Vos GIGA HDMI NoSurge

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Title

Reserved

Size	Document Number	Rev
A3	*Enrico/Caruso 15 HR*	*X01*

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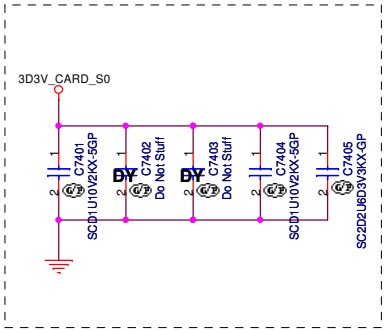
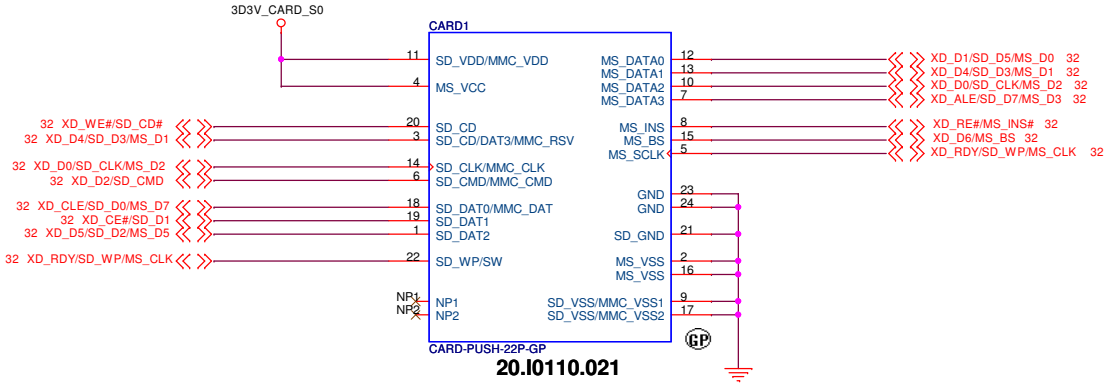
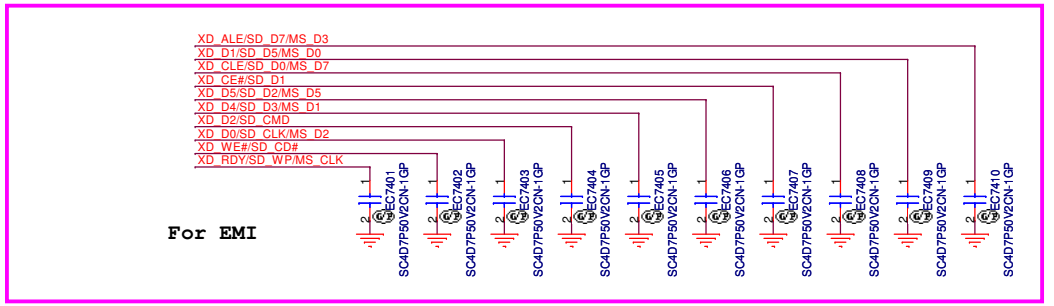
SSID = SDIO

SD/MMC/MS Card Reader





X01-20110315



DV15 HR Vos GIGA HDMI NoSurge

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Taipei Hsien 221, Taiwan, R.O.C.

Title: SD/MS/MMC Card CONN

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

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SSID = ExpressCard

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Express Card

Size: A3 | Document Number: Enrico/Caruso 15 HR | Rev: X01

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

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A3	*Enrico/Caruso 15 HR*	*X01*

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SSID = User.Interface

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor

Size: A3 | Document Number: Enrico/Caruso 15 HR | Rev: X01

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

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A3	***Enrico/Caruso 15 HR***	***X01***

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

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A3	*Enrico/Caruso 15 HR*	*X01*

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

IO Board Connector

Size	Document Number	Rev
A3	*Enrico/Caruso 15 HR*	*X01*

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU_PCIE/STRAPPING(1/5)

Size	Document Number	Rev
A3	**Enrico/Caruso 15 HR**	**X01**

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

GPU Memory(2/5)

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size	Document Number	Rev
A2	Enrico/Caruso 15 HR	X01

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU_POWER(4/5)

Size	Document Number	Rev
A2	Enrico/Caruso 15 HR	X01

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

Size: A2 | Document Number: Enrico/Caruso 15 HR | Rev: X01

Date: Thursday, June 02, 2011 | Sheet 87 of 104

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
Custom	Enrico/Caruso 15 HR	X01

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
Custom	**Enrico/Caruso 15 HR**	**X01**

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A3	**Enrico/Caruso 15 HR**	**X01**

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A3	**Enrico/Caruso 15 HR**	**X01**

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_+VGA_CORE

Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size	Document Number	Rev
A2	Enrico/Caruso 15 HR	X01

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DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LVDS_Switch

Size	Document Number	Rev
A3	**Enrico/Caruso 15 HR**	**X01**

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***CRT_Switch***

Size	Document Number	Rev
A3	**Enrico/Caruso 15 HR**	**X01**

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SSID = SDIO

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TOUCH PANEL

Size: A3 | Document Number: Enrico/Caruso 15 HR | Rev: X01

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SSID = Mechanical

H10 Do Not Stuff DY
H11 Do Not Stuff DY
H12 Do Not Stuff DY
H6 Do Not Stuff Do Not Stuff
H7 Do Not Stuff Do Not Stuff
H8 Do Not Stuff
H9 Do Not Stuff DY
Do Not Stuff

H1 Do Not Stuff Do Not Stuff
H2 Do Not Stuff Do Not Stuff
H4 Do Not Stuff Do Not Stuff
H5 Do Not Stuff Do Not Stuff
H3 Do Not Stuff Do Not Stuff
H15 Do Not Stuff

Top Side

34.4B502.001
HMI1
STF256R117H119-GP

34.4CK01.001
HTH1
STF237R117H83-1-GP

34.4F822.002 SPR1 SPRING-51-GP
34.4F822.002 SPR2 SPRING-51-GP
34.4F822.002 SPR3 SPRING-51-GP

DCBATOUT EC9701 SCD1U25V2ZY-1GP
DCBATOUT EC9702 SCD1U25V2ZY-1GP
DCBATOUT EC9703 SCD1U25V2ZY-1GP
DCBATOUT EC9704 SCD1U25V2ZY-1GP
DCBATOUT EC9705 SCD1U25V2ZY-1GP
DCBATOUT EC9706 SCD1U25V2ZY-1GP
DCBATOUT EC9707 SCD1U25V2ZY-1GP
DCBATOUT C9711 SC1KP25V2JX-GP

DCBATOUT EC9709 SCD1U25V2ZY-1GP
DCBATOUT EC9711 SCD1U25V2ZY-1GP
DCBATOUT EC9712 SCD1U25V2ZY-1GP
DCBATOUT EC9713 SCD1U25V2ZY-1GP
DCBATOUT EC9714 SCD1U25V2ZY-1GP
DCBATOUT EC9708 SCD1U25V2ZY-1GP
DCBATOUT EC9710 SCD1U25V2ZY-1GP

1D5V_S3 EC9734 SCD1U10V2KX-5GP
1D5V_S3 EC9735 SCD1U10V2KX-5GP
1D5V_S0 EC9736 SCD1U10V2KX-5GP
1D05V_VTT EC9745 SCD1U10V2KX-5GP
VCC_CORE EC9748 SCD1U10V2KX-5GP
VCC_CORE EC9749 SCD1U10V2KX-5GP
VCC_GFXCORE EC9750 SCD1U10V2KX-5GP
0D85V_S0 EC9729 SCD1U10V2KX-5GP
5V_S0 EC9717 SCD1U10V2KX-5GP

3D3V_S0 EC9720 SCD1U10V2KX-5GP
3D3V_S0 EC9721 SCD1U10V2KX-5GP
3D3V_S0 EC9722 SCD1U10V2KX-5GP
3D3V_S5 EC9723 SCD1U10V2KX-5GP
3D3V_S5 EC9724 SCD1U10V2KX-5GP
3D3V_S5 EC9725 SCD1U10V2KX-5GP
3D3V_S5 EC9726 SCD1U10V2KX-5GP
5V_S0 EC9715 SCD1U10V2KX-5GP
5V_S0 EC9716 SCD1U10V2KX-5GP

FOR EMI REQUEST

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: Enrico/Caruso 15 HR
Rev: X01
Date: Thursday, June 02, 2011
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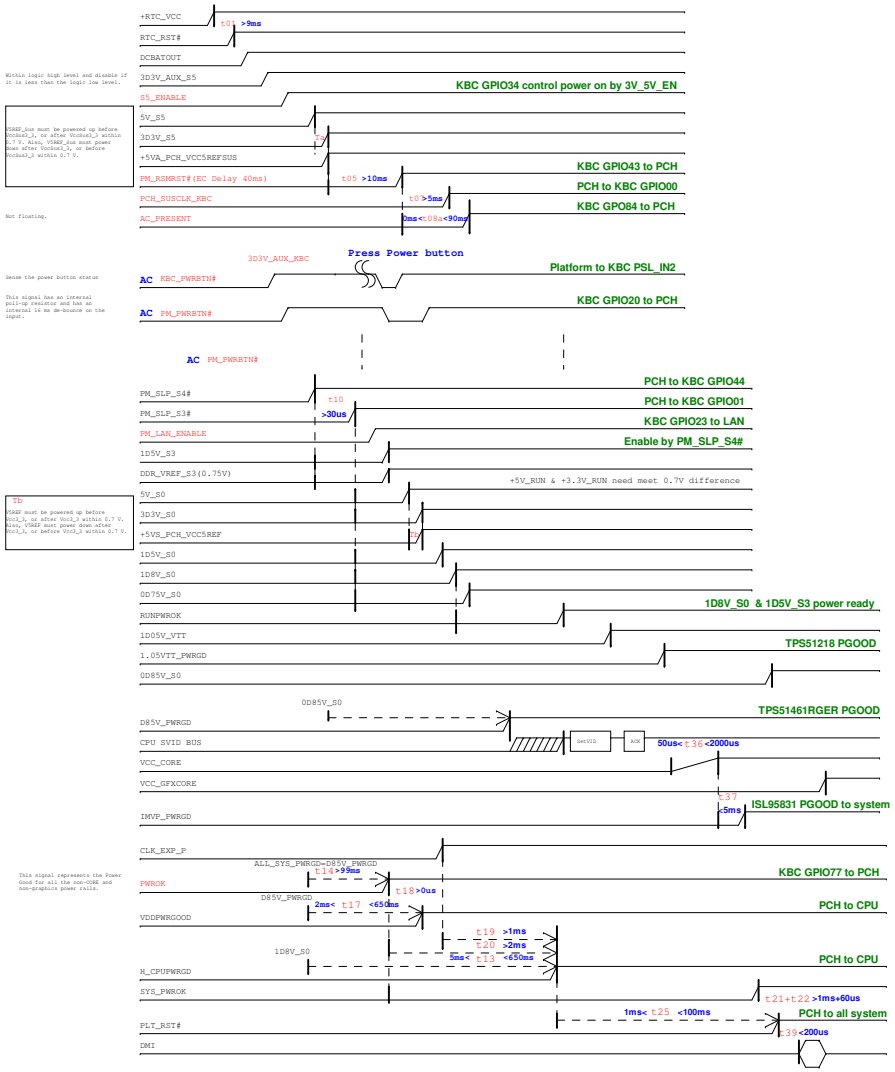
Huron River Platform Power Sequence

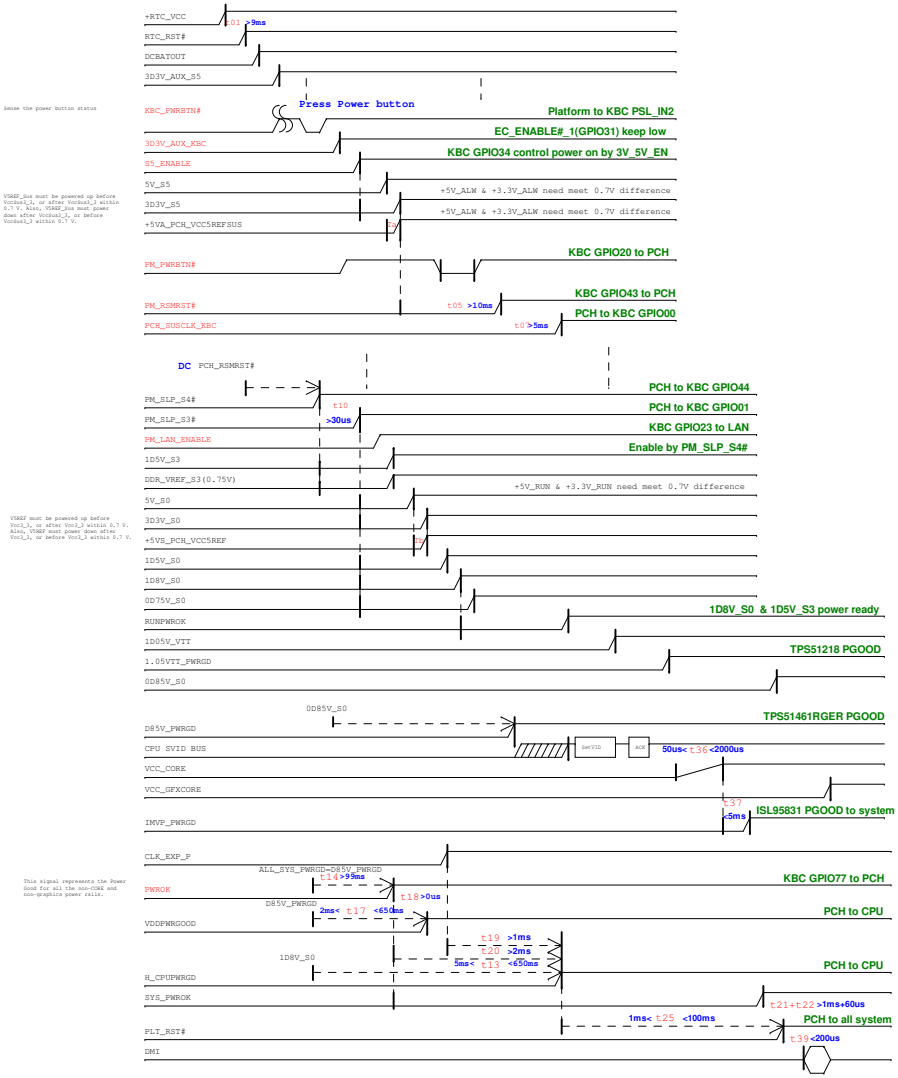
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



DV15 HR Vos GIGA HDMI NoSurge

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

Size	Document Number	Rev
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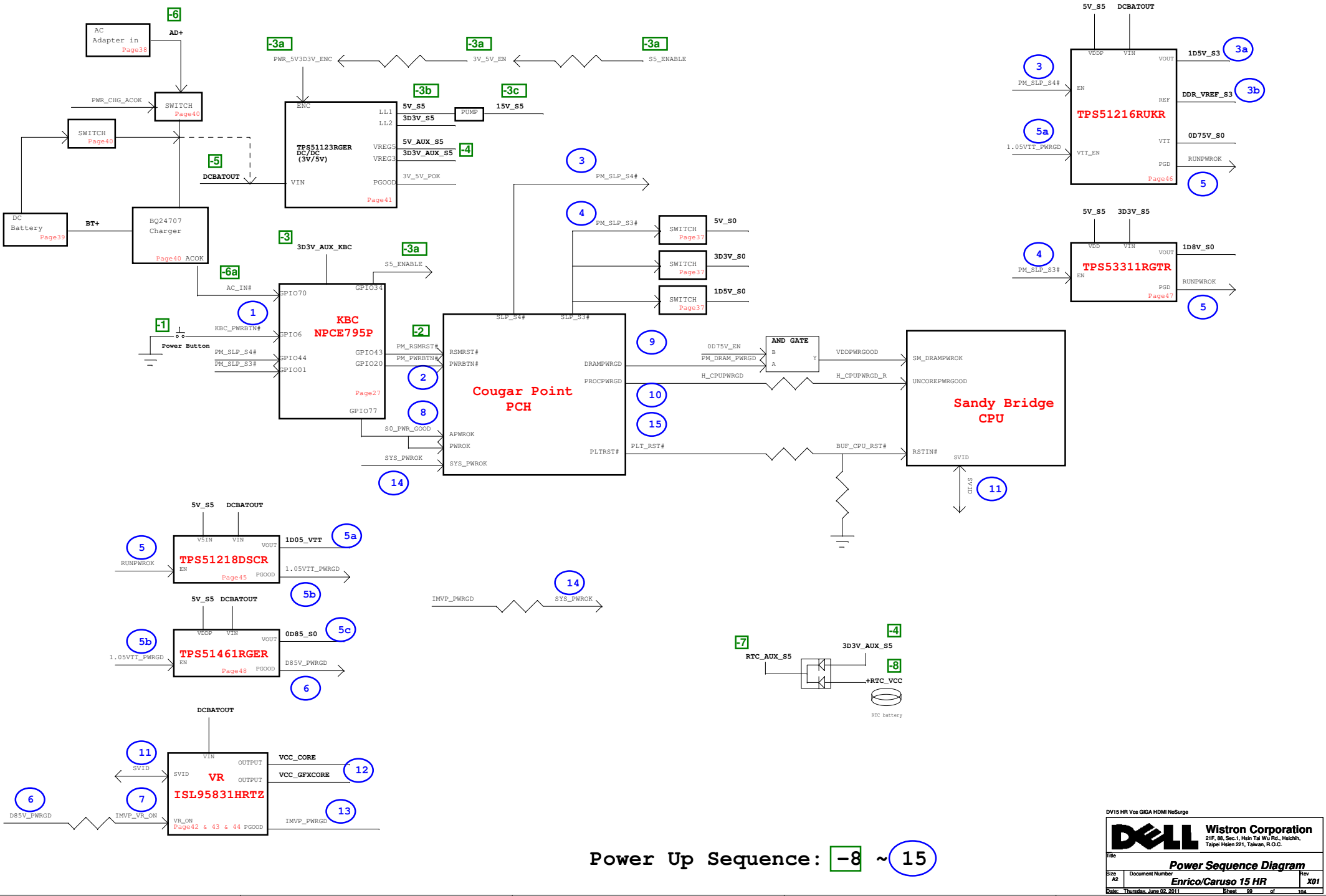
Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 15

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence Diagram

Size	Document Number	Rev
A2	Enrico/Caruso 15 HR	X01

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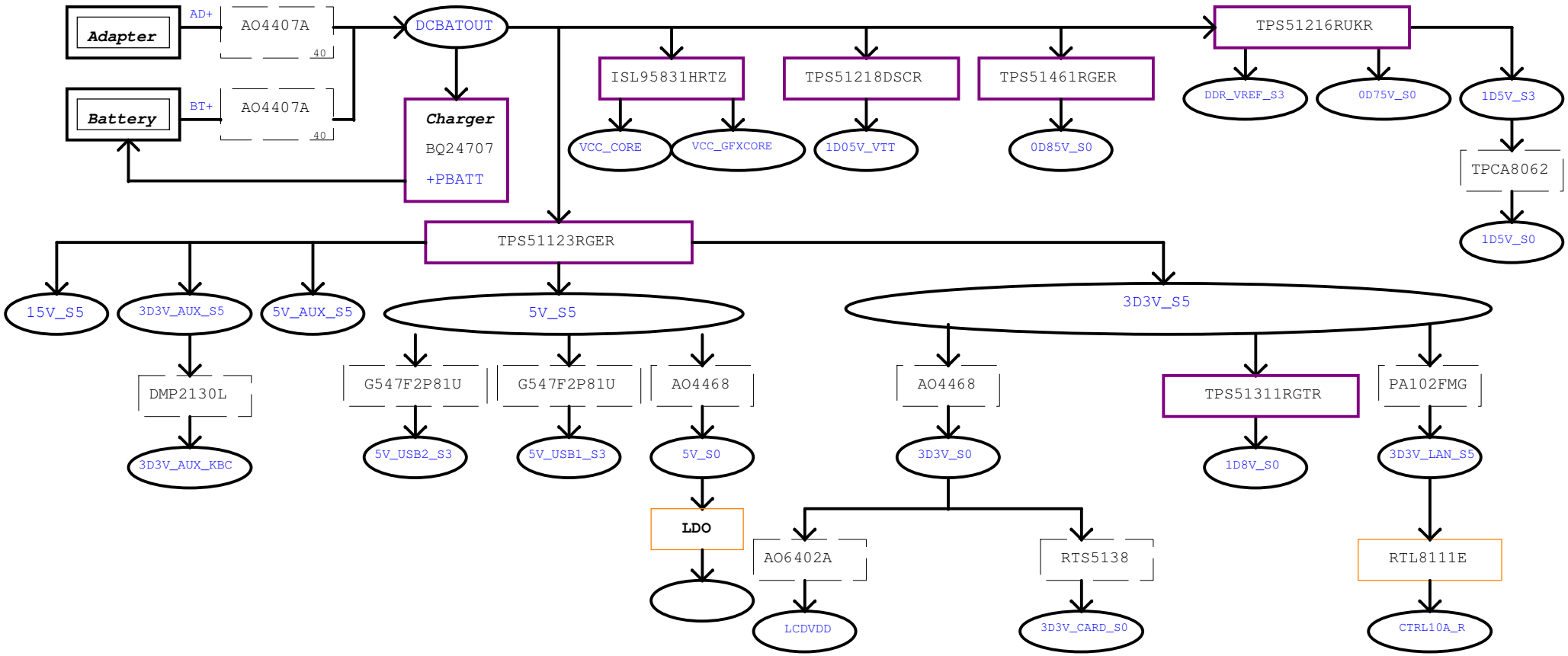

Power Shape

Regulator | **LDO** | **Switch**

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
A3	*Enrico/Caruso 15 HR*	*X01*

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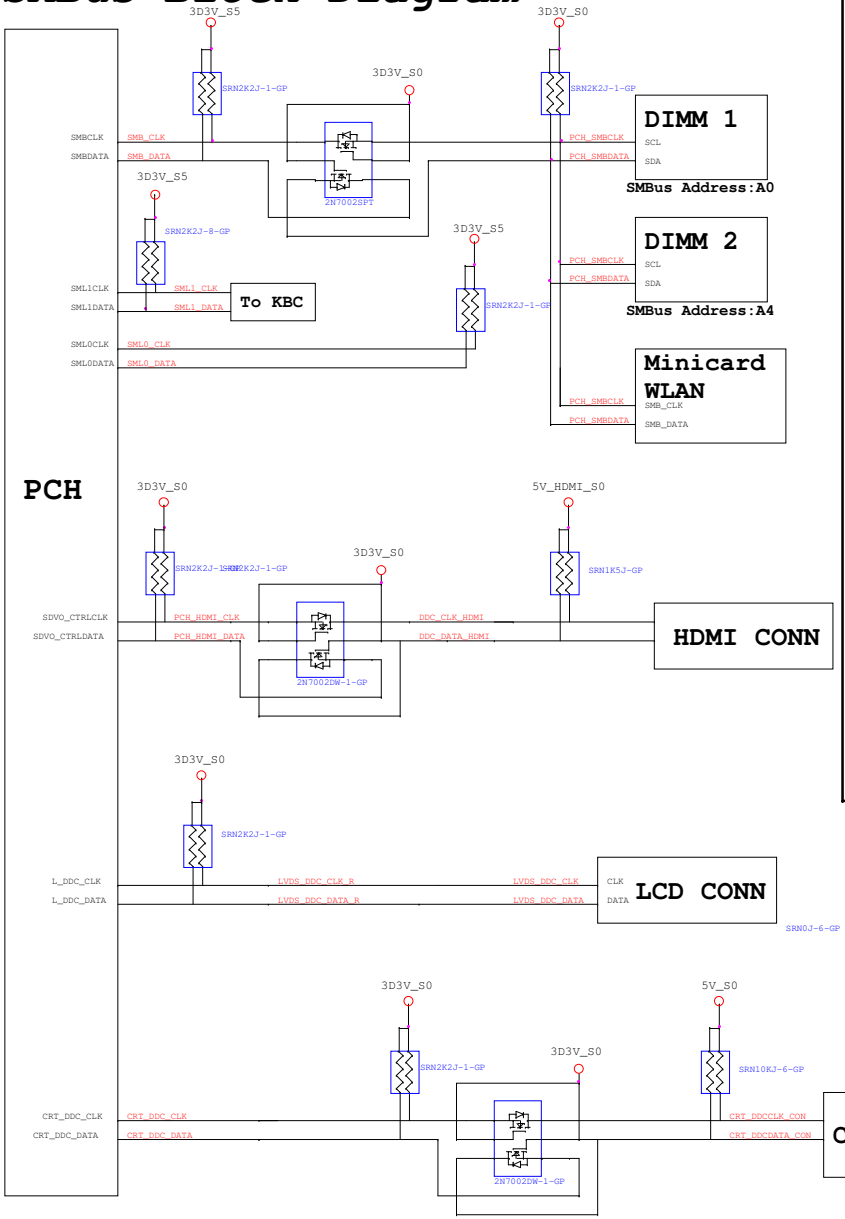
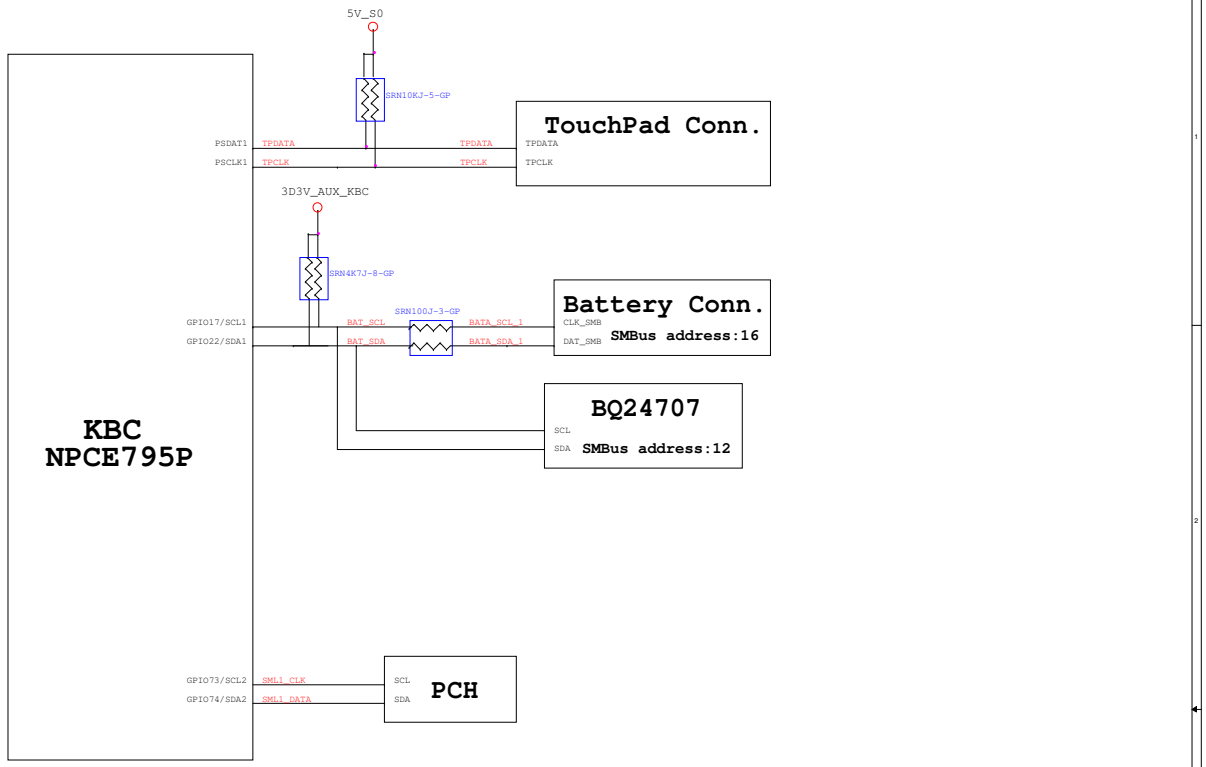
PCH SMBus Block Diagram



KBC SMBus Block Diagram



DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

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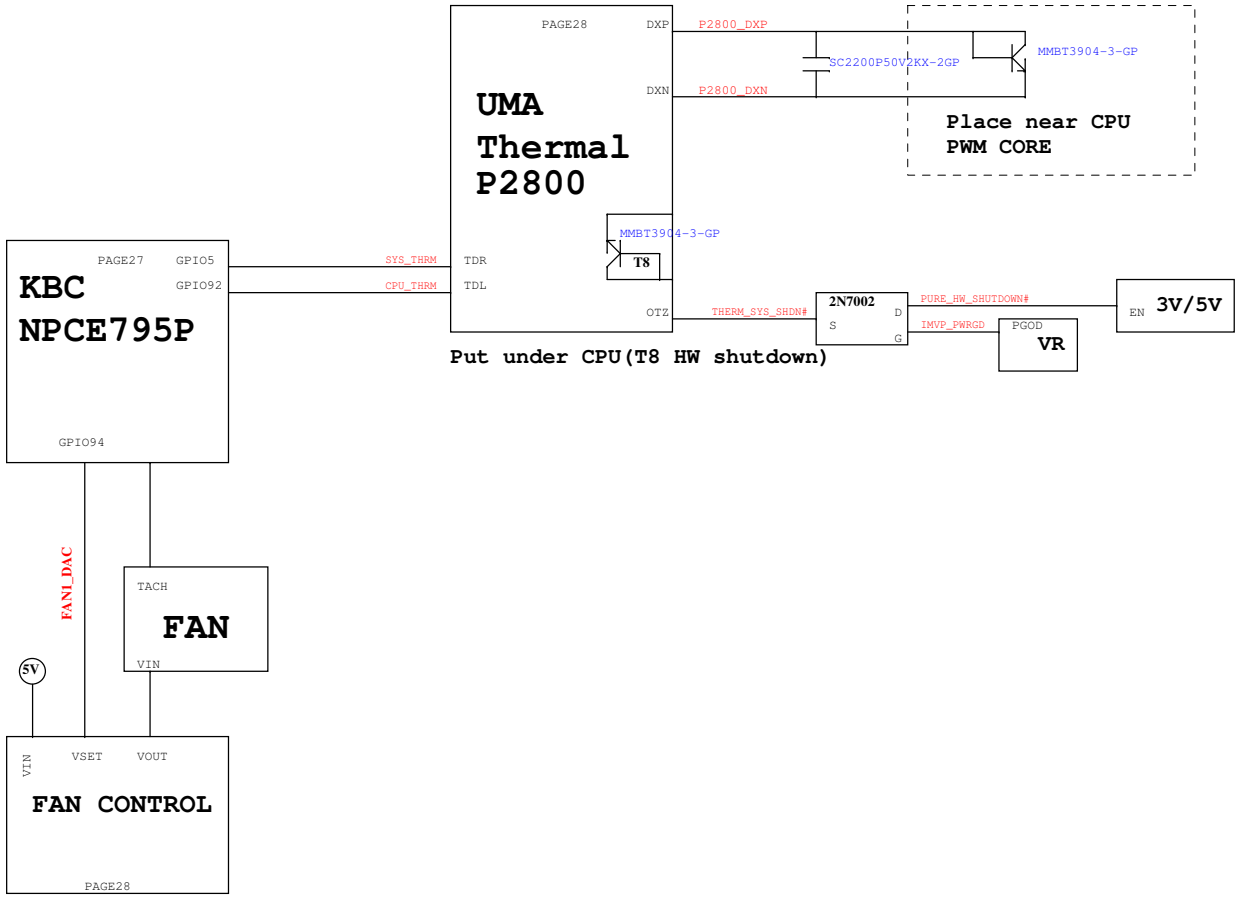
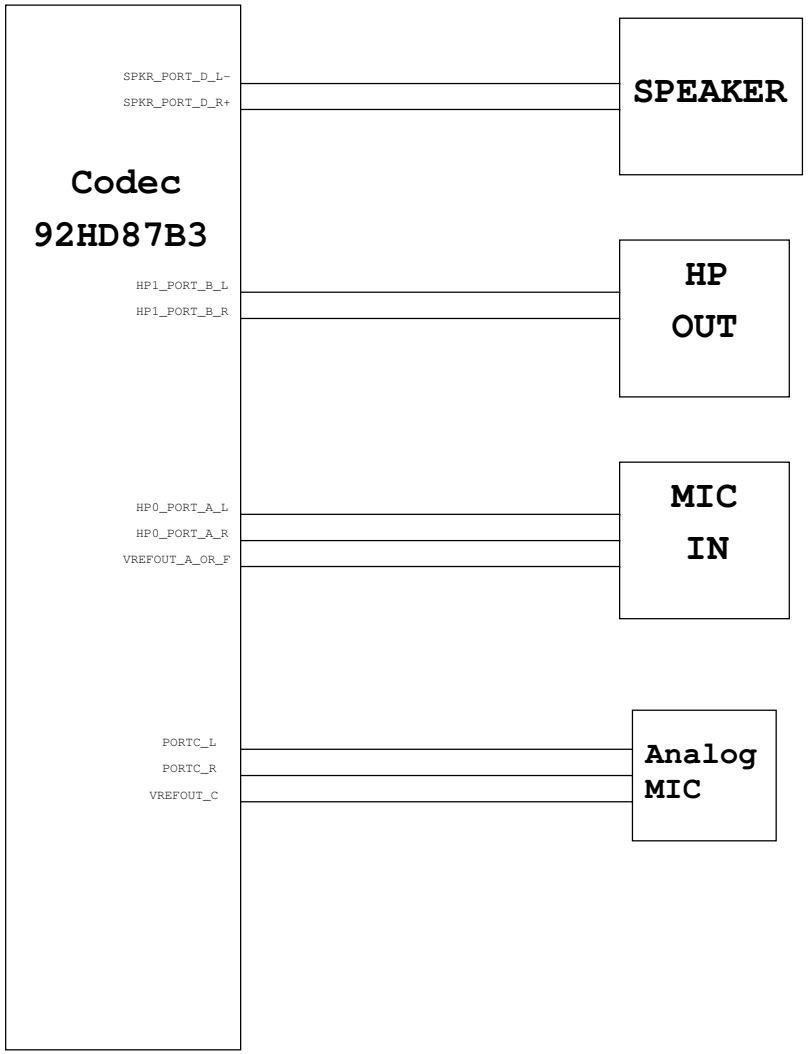
Thermal Block Diagram



Audio Block Diagram



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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

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