MODEL NAME : ***QAR00***

PCB NO : ***LA-7931P (DAA00002T00)***

BOM P/N : ***4319FN31L01***
4319FN31L02

Compal Confidential

Vans 15

rPGA Ivy Bridge + FCBGA PCH Panther Point + MXM III type A x1

Rev: 1.0 (A00)

2012.06.07

@ : Nopop component

CONN@ : ME connector

5@ : 6-bit LCD panel

6@ : 10-bit LCD panel

1@, 2@, 3@, 4@ : for TPM / TCM

PXDP@,JTAG@ : Total debug connector (pop them until ST)

MB Type	BOM P/N	Include 6-bit
TPM	4319FN31L01	1@ 3@ 5@ PXDP@ JTAG@

MB Type	BOM P/N	Include 10-bit
TPM	4319FN31L02	1@ 3@ 6@ PXDP@ JTAG@

SATA Re-driver (U26,U637)	Source	X76 P/N	Page
PS8520B (SA00004WF00)	main source	X7641231L01	35,43
MAX4951C (SA00002EY1L)	2nd source	X7641231L02	

USB3 Re-driver (U638)	Source	X76 P/N	Page
PS8720B (SA00004UI00)	main source	X7641231L03	40
PS8720A (SA00005PO00)	2nd source	X7641231L04	

ROM part	Source	X76 P/N	Page
U52 (SA000039A2L) U53 (SA00003K80L)	main (Winbond)	X7640631L01	17
U52 (SA000046400) U53 (SA00004LI00)	2nd (EON)	X7640631L03	

MB PCB

Part Number	Description
DAA00002T00	PCB 0FE LA-7931P REV0 M/B DIS

power CKT: 05/17

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTI TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIR PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

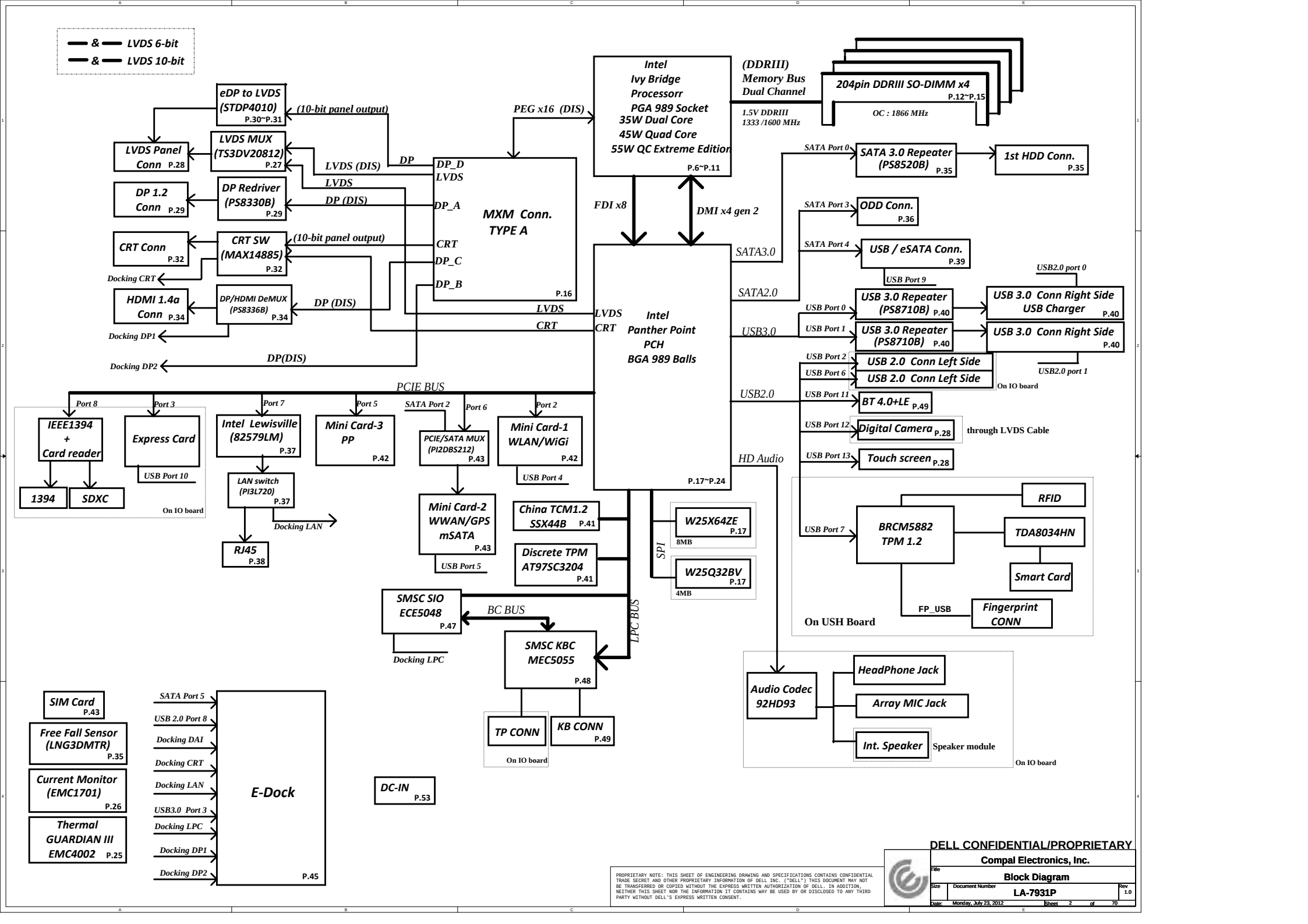
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: **Cover Sheet**

Size | Document Number: **LA-7931P** | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 1 of 70



DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.	
Title	Block Diagram
Size	Document Number: LA-7931P
Rev	1.0
Date:	Monday, July 23, 2012
Sheet	2 of 70

POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane / State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50
			Add Plating		1.00
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080	2.60
2	GND1		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
3	Sig 1		Copper foil	1oz	1.35
		4.1	Prepreg	2116Mx2	8.26
4	GND/PWR		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
5	Sig 2		Copper foil	1oz	1.35
		3.8	Prepreg	1080Hx2	4.30
6	Sig 3		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
7	GND/PWR		Copper foil	1oz	1.35
		4.1	Prepreg	2116Mx2	8.26
8	Sig 4		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
9	GND 3		Copper foil	1oz	1.35
		3.7	Prepreg	1080	2.60
10	Bottom		Copper foil	0.5oz	0.65
			Add Plating		1.00
			SolderMask		0.50
Overall Thickness (1.45mm ± 10%)			57.09		57.26000 1.454404

SATA	DESTINATION
SATA 0	HDD 1
SATA 1	NA
SATA 2	mSATA
SATA 3	ODD
SATA 4	ESATA
SATA 5	Dock

	USB PORT#	DESTINATION
PCH	0	JUSB1 (Ext Right Side) USB3.0
	1	JUSB2 (Ext Right Side) USB3.0
	2	IO Board- JUSB1 (Ext Left Side)
	3	Docking USB3.0
	4	Docking USB 2.0
	5	WWAN
	6	IO Board- JUSB2 (Ext Left Side)
	7	USH
	8	WLAN
	9	ESATA
	10	Express Card
	11	BT 4.0
	12	Carmera
	13	Touch Screen

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	MINI CARD-1 WLAN/DMC
Lane 3	Express Card
Lane 4	NA
Lane 5	MINI CARD-3 (Pink Panther)
Lane 6	MINI CARD-2 WWAN/mSATA/GPS
Lane 7	10/100/1G LOM
Lane 8	Cardreader

DELL CONFIDENTIAL/PROPRIETARY

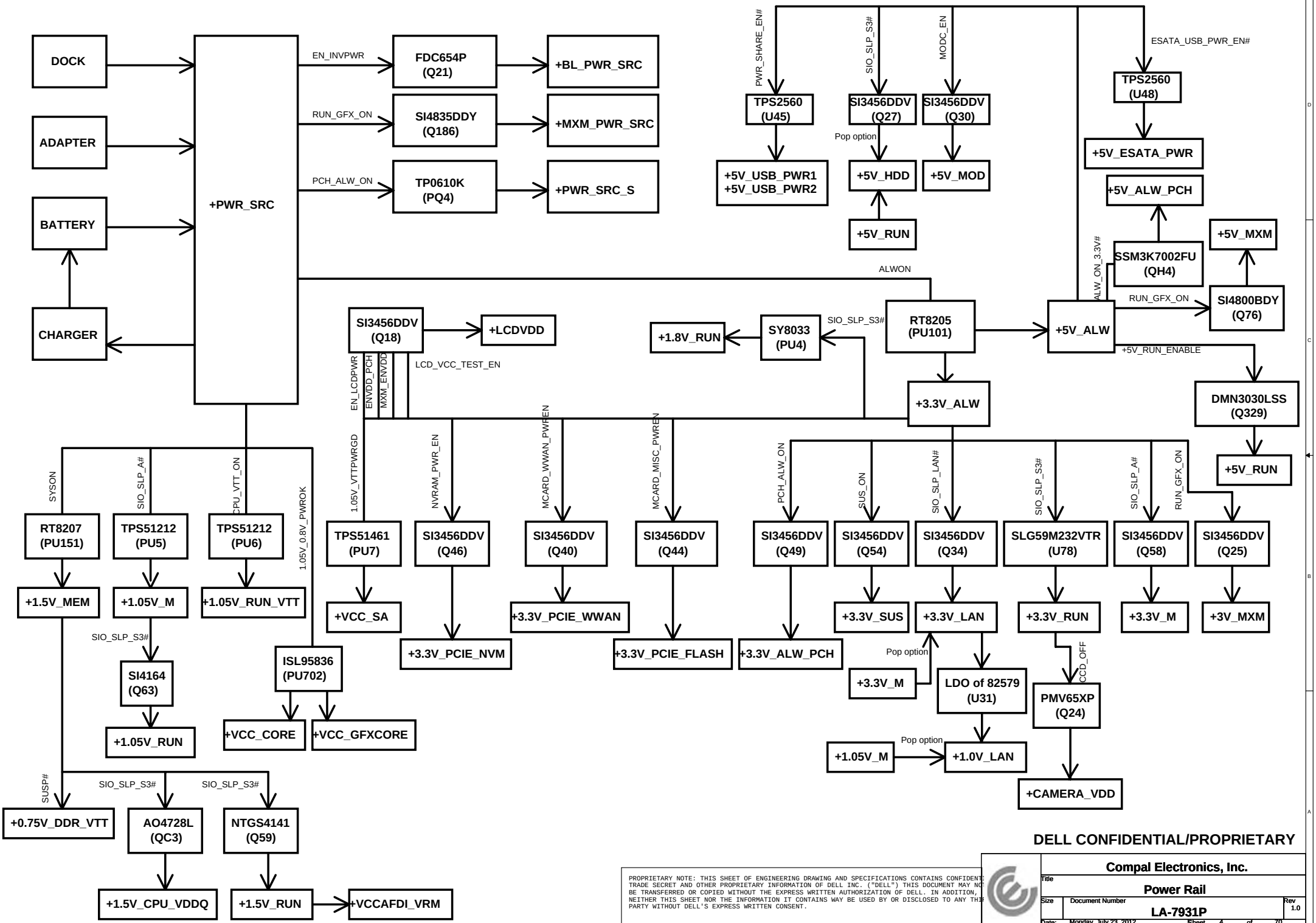
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: Index and Config.

Size | Document Number: LA-7931P | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 3 of 70



DELL CONFIDENTIAL/PROPRIETARY

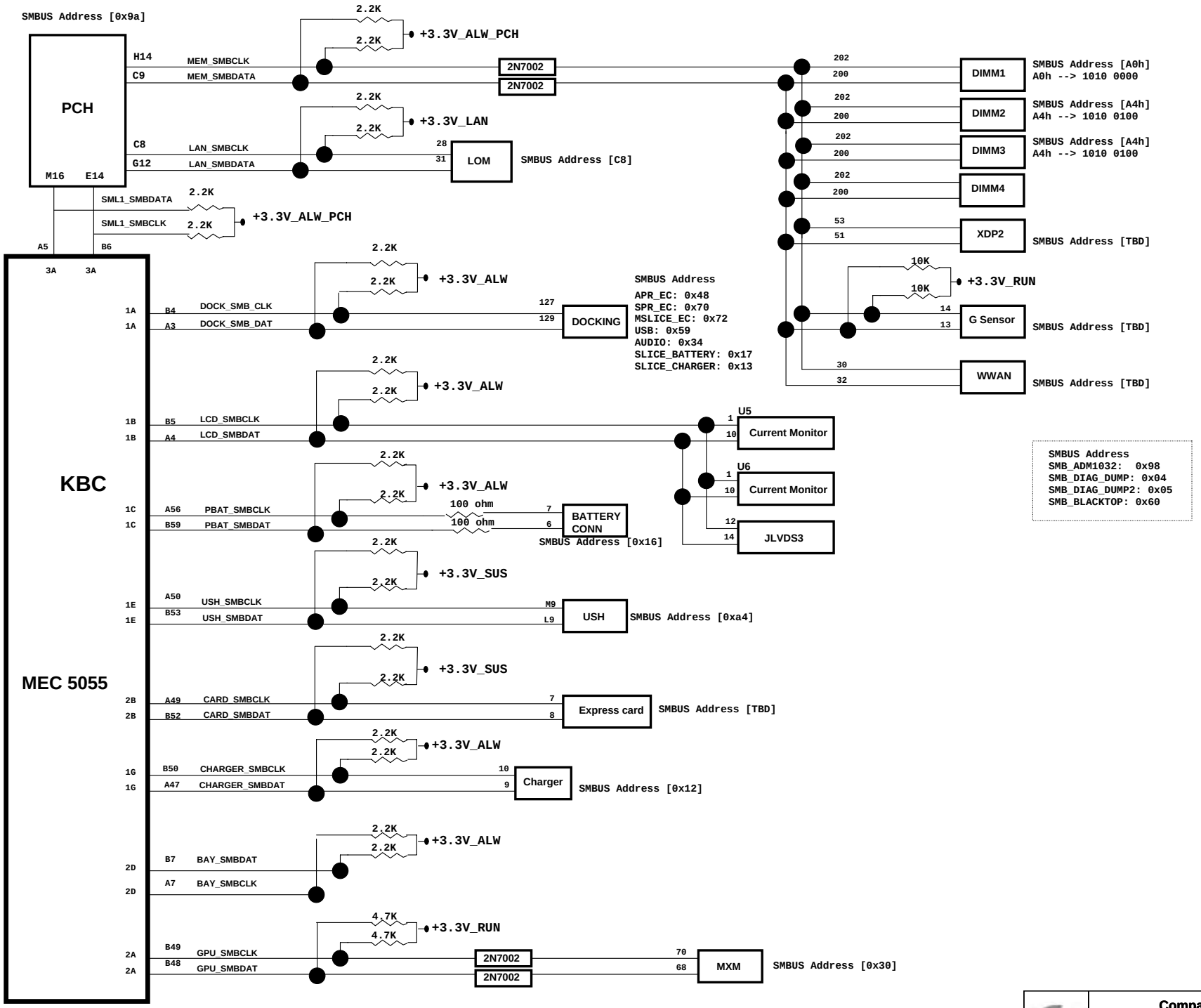
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTI
TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NO
BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION,
NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THI
PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: Power Rail

Size | Document Number: LA-7931P | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 4 of 70



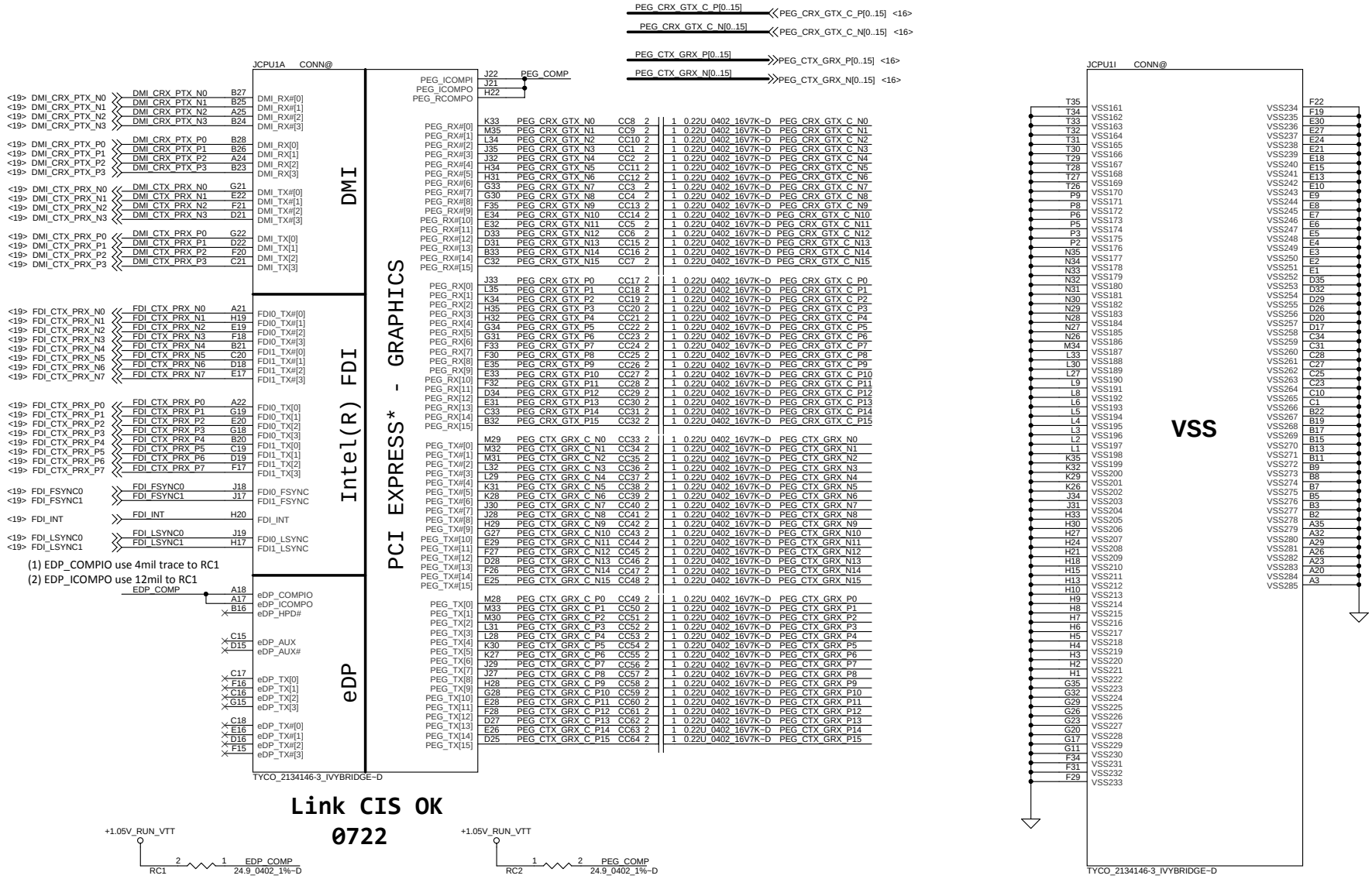
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: SMBUS Bolck Diagram

Size | Document Number: LA-7931P | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 5 of 70



DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

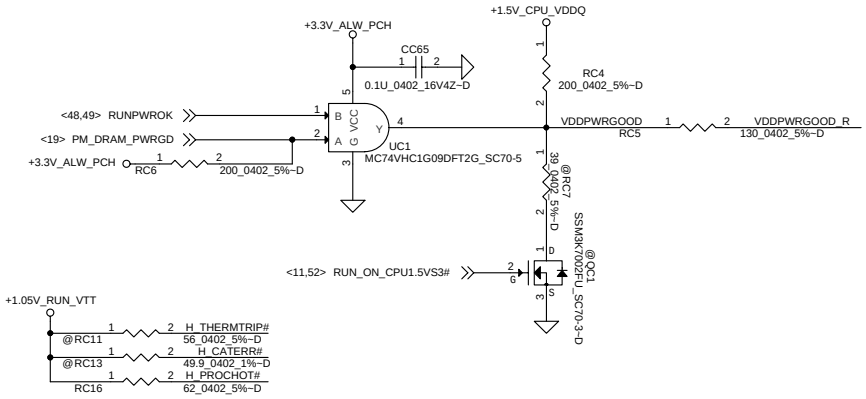
Compal Electronics, Inc.

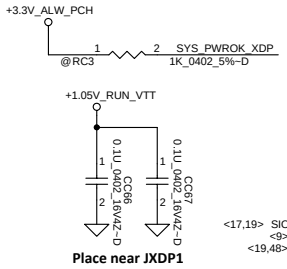
Title: Ivy Bridge (1/6)

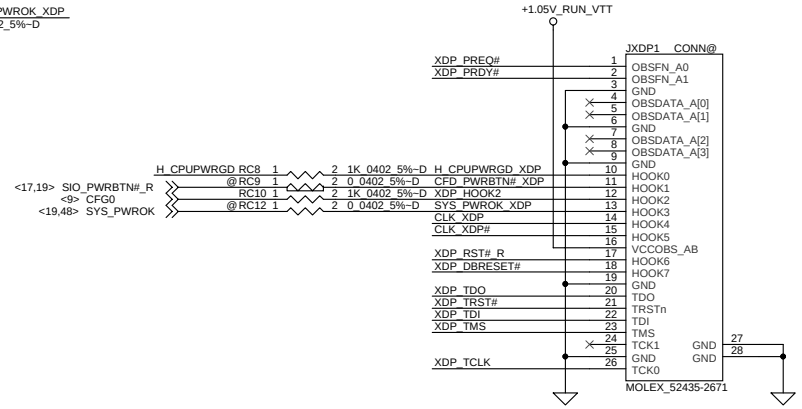
Size | Document Number: LA-7931P | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 6 of 70

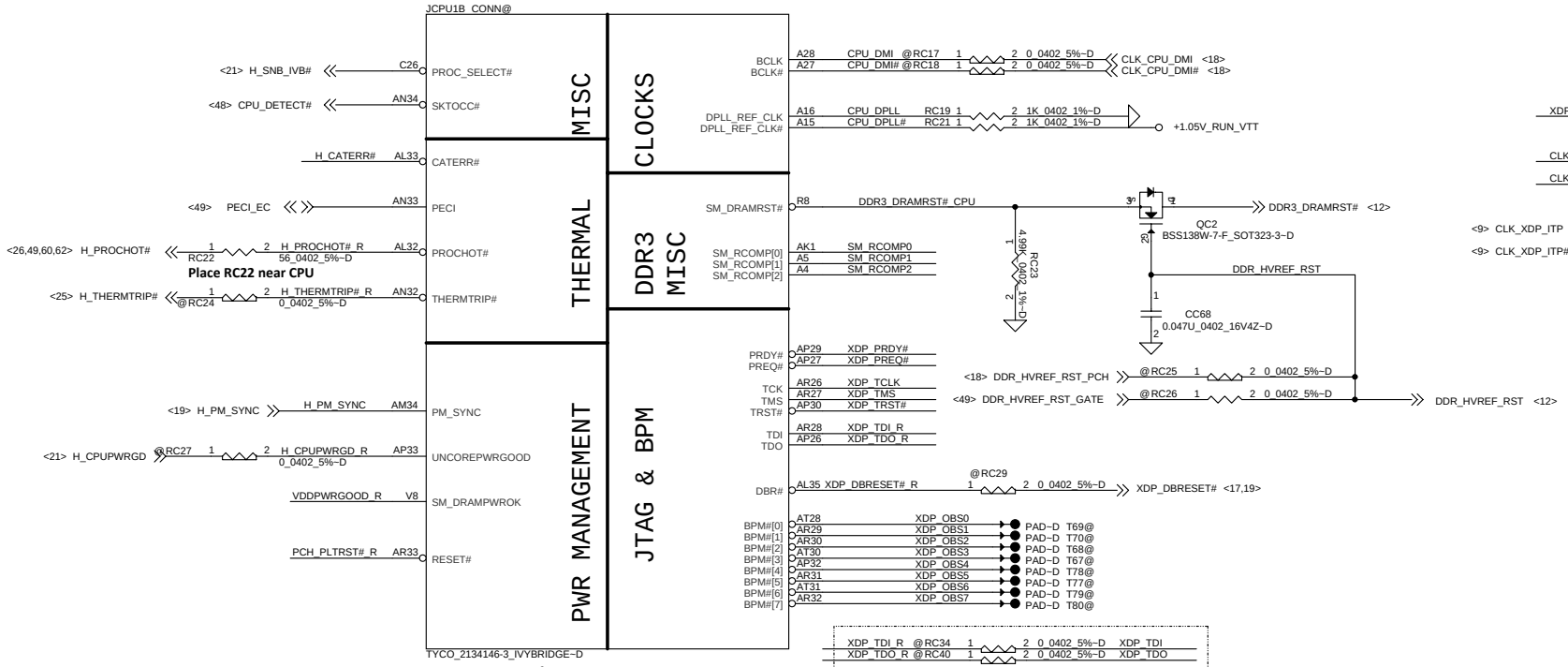
Follow DG Rev0.71 SM_DRAMPWROK topology



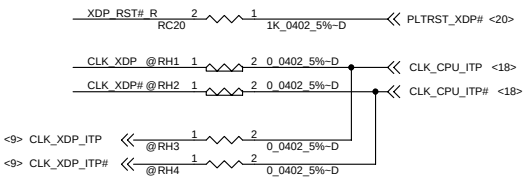


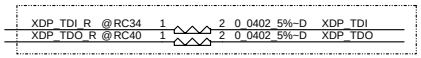


Link CIS OK 0722

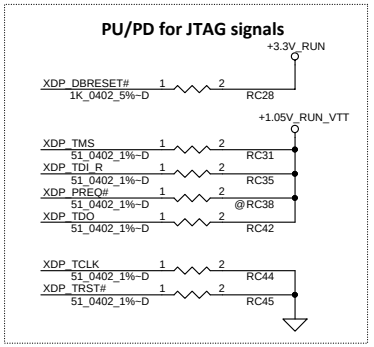


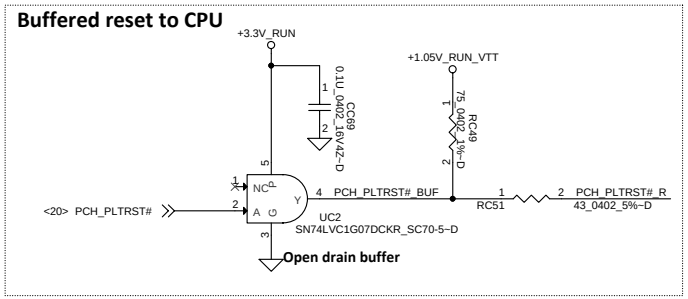
Link CIS OK

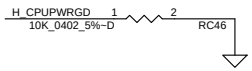




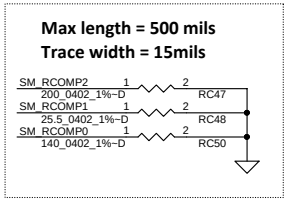
For ESD concern, please put near CPU







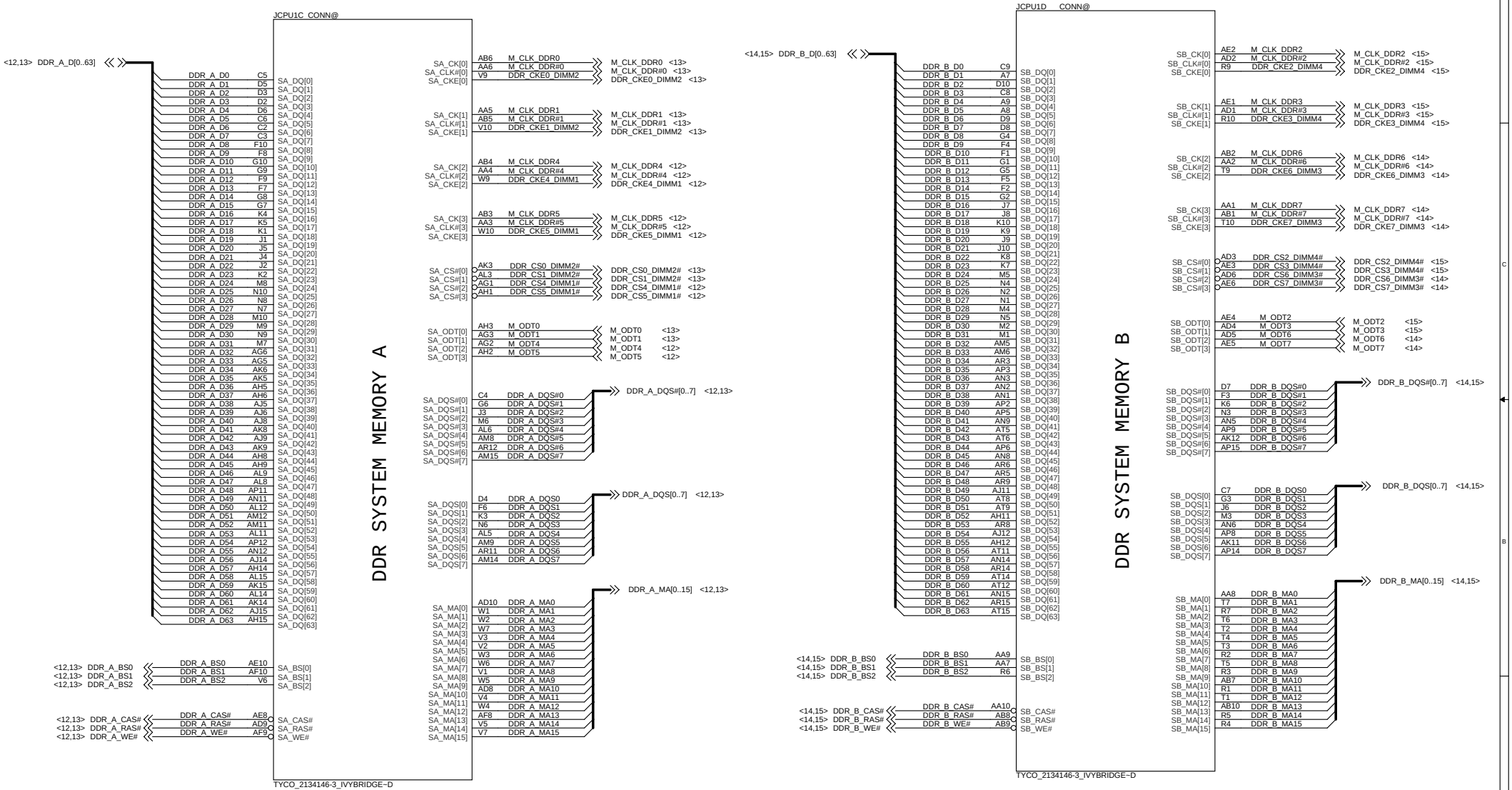
Avoid stub in the PWRGD path while placing resistors RC27& RC46



DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.	
Title	Ivy Bridge (2/6)
Size	Document Number: LA-7931P
Rev	1.0
Date:	Monday, July 23, 2012
Sheet	7 of 70



Link CIS OK

Link CIS OK

DELL CONFIDENTIAL/PROPRIETARY

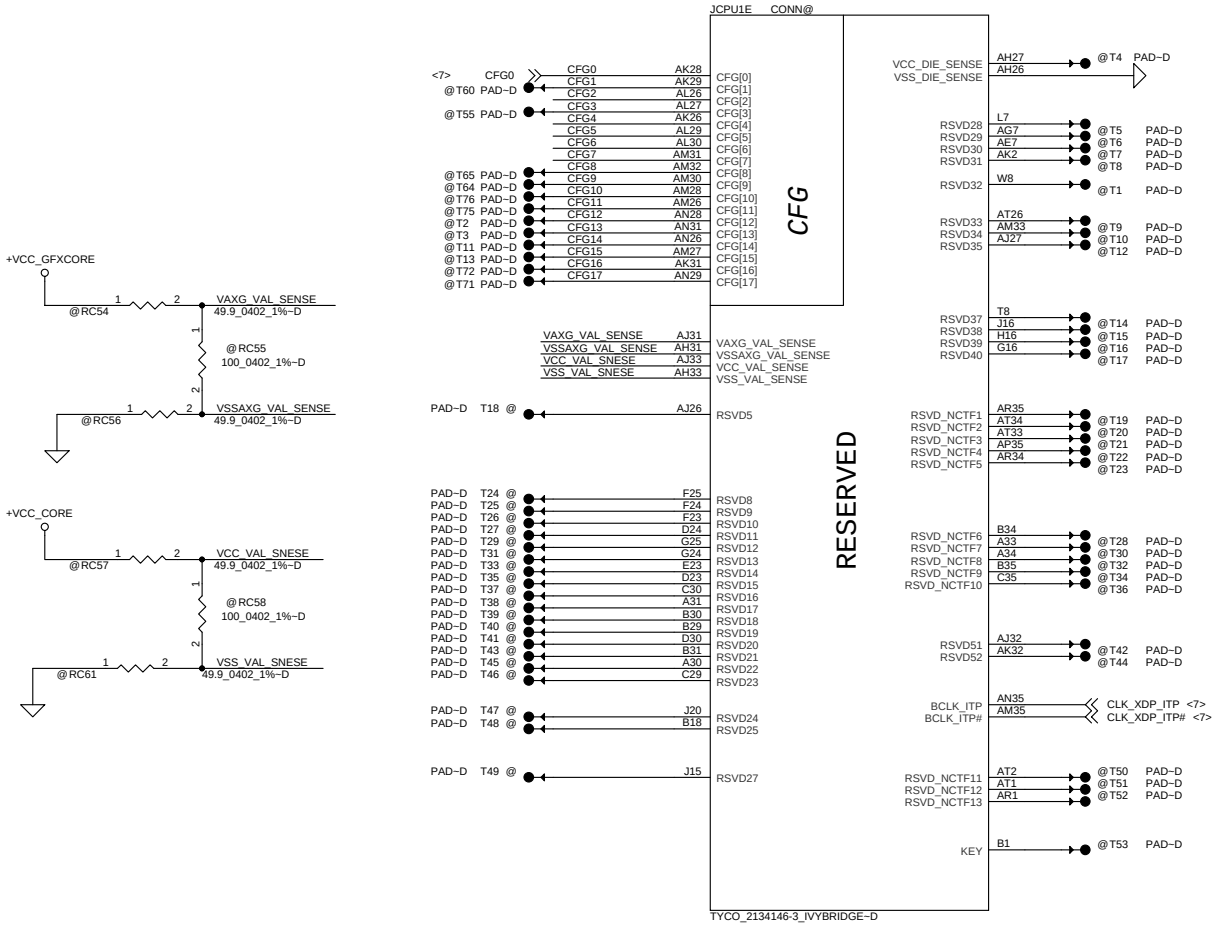
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: Ivy Bridge (3/6)

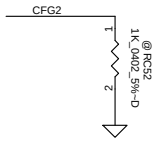
Size | Document Number: LA-7931P | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 8 of 70

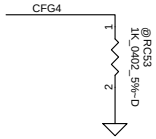


Link CIS OK

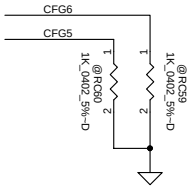
CFG Straps for Processor



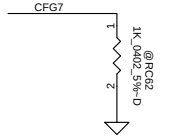
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: Ivy Bridge (4/6)

Size | Document Number: LA-7931P | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 9 of 70

POWER

JCPU1F CONN@

+VCC_CORE
97A

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

CORE SUPPLY

PEG AND DDR

+1.05V_RUN_VTT
8.5A

VCCIO1	AH13
VCCIO2	AH10
VCCIO3	AG10
VCCIO4	AC10
VCCIO5	Y10
VCCIO6	U10
VCCIO7	P10
VCCIO8	L10
VCCIO9	J14
VCCIO10	J13
VCCIO11	J12
VCCIO12	J11
VCCIO13	H14
VCCIO14	H12
VCCIO15	H11
VCCIO16	G14
VCCIO17	G13
VCCIO18	G12
VCCIO19	F14
VCCIO20	F13
VCCIO21	F12
VCCIO22	F11
VCCIO23	E14
VCCIO24	E12
VCCIO25	E11
VCCIO26	D14
VCCIO27	D13
VCCIO28	D12
VCCIO29	D11
VCCIO30	C14
VCCIO31	C13
VCCIO32	C12
VCCIO33	C11
VCCIO34	B14
VCCIO35	B12
VCCIO36	A14
VCCIO37	A13
VCCIO38	A12
VCCIO39	A11
VCCIO40	J23

Note: Place the PU resistors close to CPU
RC63 close to CPU 300 - 1500mils

+1.05V_RUN_VTT
RC63 75_0402_1%~D
H_CPU_SVIDALRT# RC64 43_0402_5%~D
VIDALERT_N <60>

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 VIDSCLK
VIDSOUT AJ28 VIDSOUT

+1.05V_RUN_VTT
RC65 130_0402_1%~D
VIDSCLK <60>
VIDSOUT <60>

CAD Note: Place the PU
resistors close to CPU
RC65 close to CPU 300 - 1500mils

SENSE LINES

+VCC_CORE
RC67 100_0402_1%~D
@RC66 100_0402_1%~D
Place RC68, RC69near CPU

VCC_SENSE AJ35 VCCSENSE_R@RC68 0_0402_5%~D
VSS_SENSE AJ34 VSSSENSE_R@RC69 0_0402_5%~D
VCCSENSE <60>
VSSSENSE <60>

10_0402_1% RC70 +1.05V_RUN_VTT

VCCIO_SENSE B10 VTT_SENSE <58>
VSS_SENSE_VCCIO A10 VSSIO_SENSE_R <58>

RC71 100_0402_1%~D
RC72 10_0402_1%~D

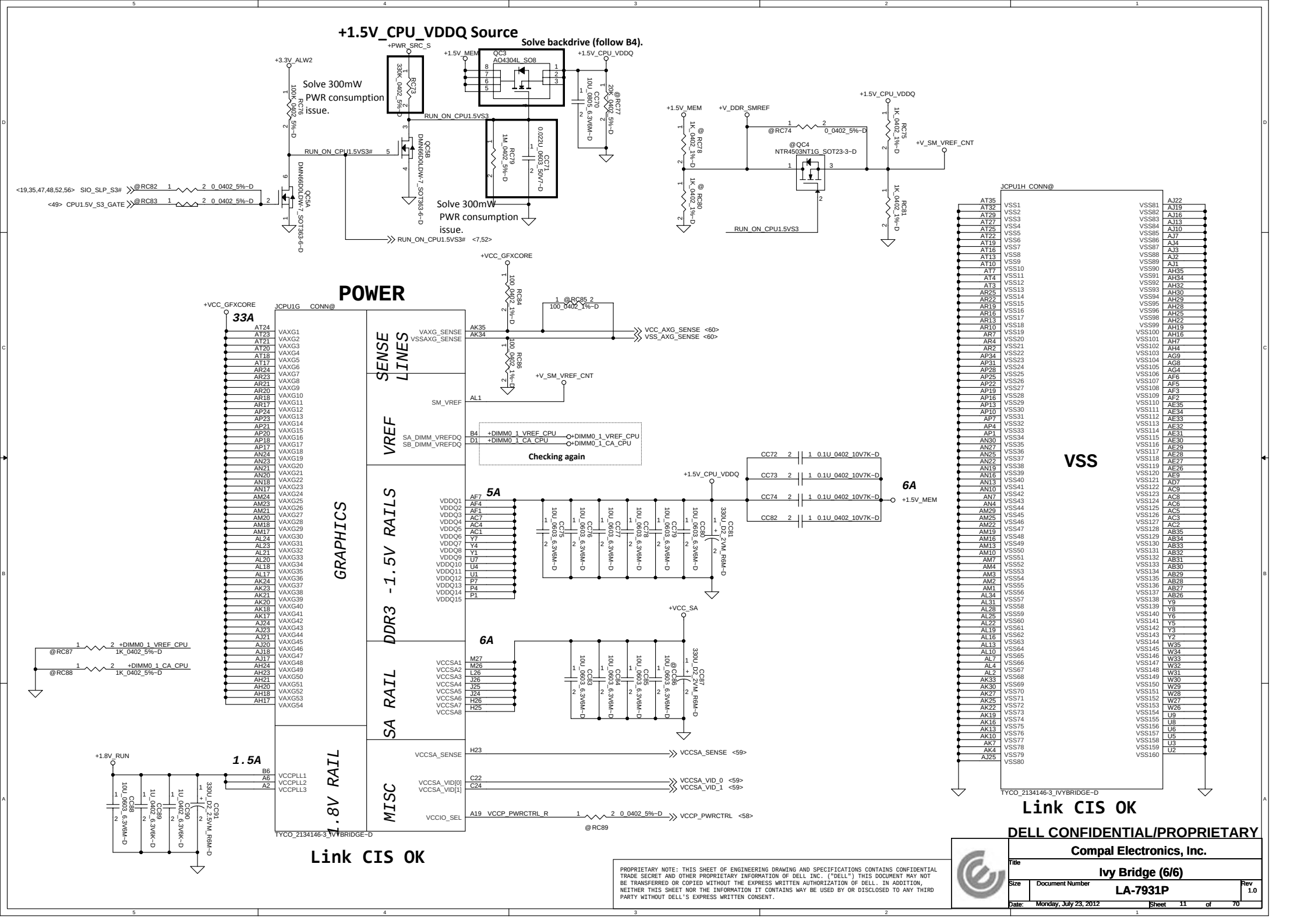
TYCO_2134146-3_IVYBRIDGE~D

Link CIS OK

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.
Title: Ivy Bridge (5/6)
Size: Document Number: LA-7931P
Rev: 1.0
Date: Monday, July 23, 2012
Sheet 10 of 70


+1.5V_CPU_VDDQ Source
Solve backdrive (follow B4).
Solve 300mW PWR consumption issue.
Solve 300mW PWR consumption issue.
POWER
GRAPHICS
DDR3 -1.5V RAILS
SA RAIL
1.8V RAIL
MISC
SENSE LINES
VREF
VSS
Checking again
Link CIS OK
Link CIS OK
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Ivy Bridge (6/6)
LA-7931P
Monday, July 23, 2012
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

All VREF traces should have 10 mil trace width

Populate RD1 for Intel DDR3 VREFDQ multiple methods M1

JDIMM1 STD Type H=5.2

JDIMM3 (Ch B1 H=9.2 STD)

JDIMM1 (Ch A1 H=5.2 STD)

TOP

CPU

BOT

JDIMM2 (Ch A0 H=5.2 REV) JDIMM4 (Ch B0 H=5.2 STD)

<8,13> DDR_A_DQS#[0..7]
<8,13> DDR_A_D[0..63]
<8,13> DDR_A_DQS[0..7]
<8,13> DDR_A_MA[0..15]

+V_DDR_REFA_M3 — @RD1 — 2_0_0402_5%~D — +DIMM1_VREF_DQ
+V_DDR_REF — @RD2 — 2_0_0402_5%~D

+1.5V_MEM — 1U_0402_6.3V6K~D (CD4, CD5, CD3, CD6) — 10U_0603_6.3V6M~D (CD7–CD12) — @CD13 330U_SX_2VY~D (CD14)

+0.75V_DDR_VTT — 1U_0402_6.3V6K~D (CD15–CD18)

Layout Note:
Place near JDIMM1.203,204

DIMM Select

+3.3V_RUN — 10K_0402_5%~D (RD8, @RD9, RD10, @RD11)

SA0	SA1	
1	0	DIMM1
0	0	DIMM2
1	1	DIMM3
0	1	DIMM4

DIMM1_SA0
DIMM1_SA1

JDIMM1 CONN@ — TYCO_2-2013289-1~D

1	VREF_DQ	VSS1	2
3	VSS2	DQ4	4 — DDR_A_D5
DDR_A_D0 — 5	DQ0	DQ5	6 — DDR_A_D1
DDR_A_D4 — 7	DQ1	VSS3	8
9	VSS4	DQS#0	10 — DDR_A_DQS#0
11	DM0	DQS0	12 — DDR_A_DQS0
13	VSS5	VSS6	14
DDR_A_D7 — 15	DQ2	DQ6	16 — DDR_A_D2
DDR_A_D6 — 17	DQ3	DQ7	18 — DDR_A_D3
19	VSS7	VSS8	20
DDR_A_D8 — 21	DQ8	DQ12	22 — DDR_A_D12
DDR_A_D9 — 23	DQ9	DQ13	24 — DDR_A_D13
25	VSS9	VSS10	26
DDR_A_DQS#1 — 27	DQS#1	DM1	28
DDR_A_DQS1 — 29	DQS1	RESET#	30 — DDR3_DRAMRST#_R
31	VSS11	VSS12	32
DDR_A_D15 — 33	DQ10	DQ14	34 — DDR_A_D10
DDR_A_D14 — 35	DQ11	DQ15	36 — DDR_A_D11
37	VSS13	VSS14	38
DDR_A_D16 — 39	DQ16	DQ20	40 — DDR_A_D20
DDR_A_D17 — 41	DQ17	DQ21	42 — DDR_A_D21
43	VSS15	VSS16	44
DDR_A_DQS#2 — 45	DQS#2	DM2	46
DDR_A_DQS2 — 47	DQS2	VSS17	48
49	VSS18	DQ22	50 — DDR_A_D18
DDR_A_D19 — 51	DQ18	DQ23	52 — DDR_A_D22
DDR_A_D23 — 53	DQ19	VSS19	54
55	VSS20	DQ28	56 — DDR_A_D28
DDR_A_D24 — 57	DQ24	DQ29	58 — DDR_A_D29
DDR_A_D25 — 59	DQ25	VSS21	60
61	VSS22	DQS#3	62 — DDR_A_DQS#3
63	DM3	DQS3	64 — DDR_A_DQS3
65	VSS23	VSS24	66
DDR_A_D30 — 67	DQ26	DQ30	68 — DDR_A_D26
DDR_A_D31 — 69	DQ27	DQ31	70 — DDR_A_D27
71	VSS25	VSS26	72
<8> DDR_CKE4_DIMM1 — 73	CKE0	CKE1	74 — DDR_CKE5_DIMM1 <8>
75	VDD1	VDD2	76
77	NC1	A15	78 — DDR_A_MA15
<8,13> DDR_A_BS2 — 79	BA2	A14	80 — DDR_A_MA14
81	VDD3	VDD4	82
DDR_A_MA12 — 83	A12/BC#	A11	84 — DDR_A_MA11
DDR_A_MA9 — 85	A9	A7	86 — DDR_A_MA7
87	VDD5	VDD6	88
DDR_A_MA8 — 89	A8	A6	90 — DDR_A_MA6
DDR_A_MA5 — 91	A5	A4	92 — DDR_A_MA4
93	VDD7	VDD8	94
DDR_A_MA3 — 95	A3	A2	96 — DDR_A_MA2
DDR_A_MA1 — 97	A1	A0	98 — DDR_A_MA0
99	VDD9	VDD10	100
<8> M_CLK_DDR4 — 101	CK0	CK1	102 — M_CLK_DDR5 <8>
<8> M_CLK_DDR#4 — 103	CK0#	CK1#	104 — M_CLK_DDR#5 <8>
105	VDD11	VDD12	106
DDR_A_MA10 — 107	A10/AP	BA1	108 — DDR_A_BS1 <8,13>
<8,13> DDR_A_BS0 — 109	BA0	RAS#	110 — DDR_A_RAS# <8,13>
111	VDD13	VDD14	112
<8,13> DDR_A_WE# — 113	WE#	S0#	114 — DDR_CS4_DIMM1# <8>
<8,13> DDR_A_CAS# — 115	CAS#	ODT0	116 — M_ODT4 <8>
117	VDD15	VDD16	118
DDR_A_MA13 — 119	A13	ODT1	120 — M_ODT5 <8>
<8> DDR_CS5_DIMM1# — 121	S1#	NC2	122
123	VDD17	VDD18	124
125	NCTEST	VREF_CA	126 — +DIMM1_VREF_CA
127	VSS27	VSS28	128
DDR_A_D36 — 129	DQ32	DQ36	130 — DDR_A_D32
DDR_A_D37 — 131	DQ33	DQ37	132 — DDR_A_D33
133	VSS29	VSS30	134
DDR_A_DQS#4 — 135	DQS#4	DM4	136
DDR_A_DQS4 — 137	DQS4	VSS31	138
139	VSS32	DQ38	140 — DDR_A_D38
DDR_A_D34 — 141	DQ34	DQ39	142 — DDR_A_D39
DDR_A_D35 — 143	DQ35	VSS33	144
145	VSS34	DQ44	146 — DDR_A_D40
DDR_A_D44 — 147	DQ40	DQ45	148 — DDR_A_D41
DDR_A_D45 — 149	DQ41	VSS35	150
151	VSS36	DQS#5	152 — DDR_A_DQS#5
153	DM5	DQS5	154 — DDR_A_DQS5
155	VSS37	VSS38	156
DDR_A_D42 — 157	DQ42	DQ46	158 — DDR_A_D46
DDR_A_D43 — 159	DQ43	DQ47	160 — DDR_A_D47
161	VSS39	VSS40	162
DDR_A_D48 — 163	DQ48	DQ52	164 — DDR_A_D52
DDR_A_D49 — 165	DQ49	DQ53	166 — DDR_A_D53
167	VSS41	VSS42	168
DDR_A_DQS#6 — 169	DQS#6	DM6	170
DDR_A_DQS6 — 171	DQS6	VSS43	172
173	VSS44	DQ54	174 — DDR_A_D50
DDR_A_D54 — 175	DQ50	DQ55	176 — DDR_A_D51
DDR_A_D55 — 177	DQ51	VSS45	178
179	VSS46	DQ60	180 — DDR_A_D61
DDR_A_D56 — 181	DQ56	DQ61	182 — DDR_A_D60
DDR_A_D57 — 183	DQ57	VSS47	184
185	VSS48	DQS#7	186 — DDR_A_DQS#7
187	DM7	DQS7	188 — DDR_A_DQS7
189	VSS49	VSS50	190
DDR_A_D62 — 191	DQ58	DQ62	192 — DDR_A_D58
DDR_A_D63 — 193	DQ59	DQ63	194 — DDR_A_D59
DIMM1_SA0 — 195	VSS51	VSS52	196
197	SA0	EVENT#	198
DIMM1_SA1 — 199	VDDSPD	SDA	200 — DDR_XDP_WAN_SMBDAT <13,14,15,17,18,35,43>
201	SA1	SCL	202 — DDR_XDP_WAN_SMBCLK <13,14,15,17,18,35,43>
+0.75V_DDR_VTT — 203	VTT1	VTT2	204 — +0.75V_DDR_VTT
205	G1	G2	206

+3.3V_RUN — 0.1U_0402_16V4Z~D (CD21) — 2.2U_0603_6.3V6K~D (CD22)

Remove 0 ohm, due to layout space limitation.

+1.5V_MEM — 1K_0402_1%~D (RD4) — <13,14,15> DDR3_DRAMRST#_R — RD3 — 1K_0402_1%~D — DDR3_DRAMRST# <7>

+DIMM0_1_VREF_CPU — @RD5 — 2_0_0402_5%~D — +V_DDR_REFA_M3
QD1 BSS138-G_SOT23-3
<7> DDR_HVREF_RST

+DIMM0_1_CA_CPU — @RD6 — 2_0_0402_5%~D — +V_DDR_REFB_M3
QD2 BSS138-G_SOT23-3
DDR_HVREF_RST

M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

+V_DDR_REF — @RD7 — 2_0_0402_5%~D — +DIMM1_VREF_CA — 2.2U_0603_6.3V6K~D (CD19) — 0.1U_0402_16V4Z~D (CD20)

Link CIS OK
0722

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size | Document Number: LA-7931P | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 12 of 70

JDIMM2 REV Type H=5.2

JDIMM3 (Ch B1 H=9.2 STD)

JDIMM1 (Ch A1 H=5.2 STD)

TOP

CPU

BOT

JDIMM2 (Ch A0 H=5.2 REV)

JDIMM4 (Ch B0 H=5.2 STD)

All VREF traces should have 10 mil trace width

<8,12> DDR_A_DQS#[0..7]
<8,12> DDR_A_D[0..63]
<8,12> DDR_A_DQS[0..7]
<8,12> DDR_A_MA[0..15]

+V_DDR_REFA_M3 — @RD14 1 2 0_0402_5%~D
+V_DDR_REF — @RD15 1 2 0_0402_5%~D

+DIMM2_VREF_DQ
CD26 2.2U_0603_6.3V6K~D
CD23 0.1U_0402_16V4Z~D

+1.5V_MEM
CD27 1U_0402_6.3V6K~D
CD24 1U_0402_6.3V6K~D
CD25 1U_0402_6.3V6K~D
CD28 1U_0402_6.3V6K~D

+1.5V_MEM
CD29 10U_0603_6.3V6M~D
CD30 10U_0603_6.3V6M~D
CD31 10U_0603_6.3V6M~D
CD32 10U_0603_6.3V6M~D
CD33 10U_0603_6.3V6M~D
CD34 10U_0603_6.3V6M~D
@CD35 10U_0603_6.3V6M~D
CD36 330U_SX_2V~D

Layout Note:
Place near JDIMM3.Pin 203,204

+0.75V_DDR_VTT
CD37 1U_0402_6.3V6K~D
CD38 1U_0402_6.3V6K~D
CD39 1U_0402_6.3V6K~D
CD40 1U_0402_6.3V6K~D

DIMM Select

+3.3V_RUN
@RD17 10K_0402_5%~D
@RD18 10K_0402_5%~D
DIMM2_SA0
DIMM2_SA1
RD19 10K_0402_5%~D
RD20 10K_0402_5%~D

SA0	SA1	
1	0	DIMM1
0	0	DIMM2
1	1	DIMM3
0	1	DIMM4

+1.5V_MEM

JDIMM2 CONN@ (TYCO_2-2013290-1)

1	VREF_DQ	VSS1	2
3	VSS2	DQ4	4 — DDR_A_D0
5	DQ0	DQ5	6 — DDR_A_D4
7	DQ1	VSS3	8
9	VSS4	DQS#0	10 — DDR_A_DQS#0
11	DM0	DQS0	12 — DDR_A_DQS0
13	VSS5	VSS6	14
15	DQ2	DQ6	16 — DDR_A_D7
17	DQ3	DQ7	18 — DDR_A_D6
19	VSS7	VSS8	20
21	DQ8	DQ12	22 — DDR_A_D8
23	DQ9	DQ13	24 — DDR_A_D9
25	VSS9	VSS10	26
27	DQS#1	DM1	28
29	DQS1	RESET#	30 — DDR3_DRAMRST#_R <12,14,15>
31	VSS11	VSS12	32
33	DQ10	DQ14	34 — DDR_A_D15
35	DQ11	DQ15	36 — DDR_A_D14
37	VSS13	VSS14	38
39	DQ16	DQ20	40 — DDR_A_D16
41	DQ17	DQ21	42 — DDR_A_D17
43	VSS15	VSS16	44
45	DQS#2	DM2	46
47	DQS2	VSS17	48
49	VSS18	DQ22	50 — DDR_A_D19
51	DQ18	DQ23	52 — DDR_A_D23
53	DQ19	VSS19	54
55	VSS20	DQ28	56 — DDR_A_D24
57	DQ24	DQ29	58 — DDR_A_D25
59	DQ25	VSS21	60
61	VSS22	DQS#3	62 — DDR_A_DQS#3
63	DM3	DQS3	64 — DDR_A_DQS3
65	VSS23	VSS24	66
67	DQ26	DQ30	68 — DDR_A_D30
69	DQ27	DQ31	70 — DDR_A_D31
71	VSS25	VSS26	72
73	CKE0	CKE1	74 — DDR_CKE1_DIMM2 <8>
75	VDD1	VDD2	76
77	NC1	A15	78 — DDR_A_MA15
79	BA2	A14	80 — DDR_A_MA14
81	VDD3	VDD4	82
83	A12/BC#	A11	84 — DDR_A_MA11
85	A9	A7	86 — DDR_A_MA7
87	VDD5	VDD6	88
89	A8	A6	90 — DDR_A_MA6
91	A5	A4	92 — DDR_A_MA4
93	VDD7	VDD8	94
95	A3	A2	96 — DDR_A_MA2
97	A1	A0	98 — DDR_A_MA0
99	VDD9	VDD10	100
101	CK0	CK1	102 — M_CLK_DDR1
103	CK0#	CK1#	104 — M_CLK_DDR#1 <8>
105	VDD11	VDD12	106
107	A10/AP	BA1	108 — DDR_A_BS1 <8,12>
109	BA0	RAS#	110 — DDR_A_RAS# <8,12>
111	VDD13	VDD14	112
113	WE#	S0#	114 — DDR_CS0_DIMM2# <8>
115	CAS#	ODT0	116 — M_ODT0 <8>
117	VDD15	VDD16	118
119	A13	ODT1	120 — M_ODT1 <8>
121	S1#	NC2	122
123	VDD17	VDD18	124
125	NCTEST	VREF_CA	126 — +DIMM2_VREF_CA
127	VSS27	VSS28	128
129	DQ32	DQ36	130 — DDR_A_D36
131	DQ33	DQ37	132 — DDR_A_D37
133	VSS29	VSS30	134
135	DQS#4	DM4	136
137	DQS4	VSS31	138
139	VSS32	DQ38	140 — DDR_A_D34
141	DQ34	DQ39	142 — DDR_A_D35
143	DQ35	VSS33	144
145	VSS34	DQ44	146 — DDR_A_D44
147	DQ40	DQ45	148 — DDR_A_D45
149	DQ41	VSS35	150
151	VSS36	DQS5	152 — DDR_A_DQS#5
153	DM5	DQS5	154 — DDR_A_DQS5
155	VSS37	VSS38	156
157	DQ42	DQ46	158 — DDR_A_D42
159	DQ43	DQ47	160 — DDR_A_D43
161	VSS39	VSS40	162
163	DQ48	DQ52	164 — DDR_A_D48
165	DQ49	DQ53	166 — DDR_A_D49
167	VSS41	VSS42	168
169	DQS#6	DM6	170
171	DQS6	VSS43	172
173	VSS44	DQ54	174 — DDR_A_D54
175	DQ50	DQ55	176 — DDR_A_D55
177	DQ51	VSS45	178
179	VSS46	DQ60	180 — DDR_A_D56
181	DQ56	DQ61	182 — DDR_A_D57
183	DQ57	VSS47	184
185	VSS48	DQS#7	186 — DDR_A_DQS#7
187	DM7	DQS7	188 — DDR_A_DQS7
189	VSS49	VSS50	190
191	DQ58	DQ62	192 — DDR_A_D62
193	DQ59	DQ63	194 — DDR_A_D63
195	VSS51	VSS52	196
197	SA0	EVENT#	198
199	VDDSPD	SDA	200 — DDR_XDP_WAN_SMBDAT <12,14,15,17,18,35,43>
201	SA1	SCL	202 — DDR_XDP_WAN_SMBCLK <12,14,15,17,18,35,43>
203	VTT1	VTT2	204 — +0.75V_DDR_VTT
205	G1	G2	206

DDR_A_D5 / DDR_A_D1
DDR_A_D2 / DDR_A_D3
DDR_A_D12 / DDR_A_D13
DDR_A_DQS#1 / DDR_A_DQS1
DDR_A_D10 / DDR_A_D11
DDR_A_D20 / DDR_A_D21
DDR_A_DQS#2 / DDR_A_DQS2
DDR_A_D18 / DDR_A_D22
DDR_A_D28 / DDR_A_D29
DDR_A_D26 / DDR_A_D27
DDR_A_D32 / DDR_A_D33
DDR_A_DQS#4 / DDR_A_DQS4
DDR_A_D38 / DDR_A_D39
DDR_A_D40 / DDR_A_D41
DDR_A_D46 / DDR_A_D47
DDR_A_D52 / DDR_A_D53
DDR_A_DQS#6 / DDR_A_DQS6
DDR_A_D50 / DDR_A_D51
DDR_A_D61 / DDR_A_D60
DDR_A_D58 / DDR_A_D59
DMM2_SA0
DMM2_SA1

<8> DDR_CKE0_DIMM2
<8,12> DDR_A_BS2
DDR_A_MA12 / DDR_A_MA9
DDR_A_MA8 / DDR_A_MA5
DDR_A_MA3 / DDR_A_MA1
<8> M_CLK_DDR0
<8> M_CLK_DDR#0
DDR_A_MA10 / DDR_A_BS0
<8,12> DDR_A_BS0
<8,12> DDR_A_WE#
<8,12> DDR_A_CAS#
DDR_A_MA13
<8> DDR_CS1_DIMM2#

+3.3V_RUN
CD43 0.1U_0402_16V4Z~D
CD44 2.2U_0603_6.3V6K~D
+0.75V_DDR_VTT

+DIMM2_VREF_CA
@RD16 1 2 0_0402_5%~D +V_DDR_REF
CD41 2.2U_0603_6.3V6K~D
CD42 0.1U_0402_16V4Z~D

Remove 0 ohm, due to layout space limitation.

Link CIS OK
0722

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.
Title: DDRIII-SODIMM SLOT2
Size: Document Number: LA-7931P Rev: 1.0
Date: Monday, July 23, 2012 Sheet 13 of 70

JDIMM3 STD Type H=9.2

JDIMM3 (Ch B1 H=9.2 STD)
JDIMM1 (Ch A1 H=5.2 STD)
TOP
CPU
BOT
JDIMM2 (Ch A0 H=5.2 REV) JDIMM4 (Ch B0 H=5.2 STD)

<8,15> DDR_B_DQS#[0..7]
<8,15> DDR_B_D[0..63]
<8,15> DDR_B_DQS[0..7]
<8,15> DDR_B_MA[0..15]

+V_DDR_REFB_M3 — @RD23 1 2 0_0402_5%~D — +DIMM3_VREF_DQ
+V_DDR_REF — 1 2 0_0402_5%~D — @RD24

DFX issue solution.
2.2U_0603_6.3V6M~D (CD63) 0.1U_0402_16V4Z~D (CD46)

All VREF traces should have 10 mil trace width

+1.5V_MEM
1U_0402_6.3V6K~D (CD47, CD48, CD49, CD50)
10U_0603_6.3V6M~D (CD51, CD52, CD53, CD54, CD55, CD56, CD57, @CD58)
330U_SX_2V~D (CD59)

Layout Note:
Place near JDIMM3.Pin 203,204

+0.75V_DDR_VTT
1U_0402_6.3V6K~D (CD58, CD60, CD61, CD62)

DIMM Select

+3.3V_RUN
10K_0402_5%~D (RD26, RD27)
DIMM3_SA0
DIMM3_SA1
10K_0402_5%~D (@RD28, @RD29)

SA0	SA1	
1	0	DIMM1
0	0	DIMM2
1	1	DIMM3
0	1	DIMM4

+3.3V_RUN
0.1U_0402_16V4Z~D (CD65) 2.2U_0603_6.3V6K~D (CD66)

JDIMM3 CONN@ — TYCO_2-2013310-1~D

		1	VREF_DQ	VSS1	2	
		3	VSS2	DQ4	4	DDR_B_D0
DDR_B_D4		5	DQ0	DQ5	6	DDR_B_D1
DDR_B_D5		7	DQ1	VSS3	8	
		9	VSS4	DQS#0	10	DDR_B_DQS#0
		11	DM0	DQS0	12	DDR_B_DQS0
		13	VSS5	VSS6	14	
DDR_B_D2		15	DQ2	DQ6	16	DDR_B_D6
DDR_B_D3		17	DQ3	DQ7	18	DDR_B_D7
		19	VSS7	VSS8	20	
DDR_B_D12		21	DQ8	DQ12	22	DDR_B_D8
DDR_B_D13		23	DQ9	DQ13	24	DDR_B_D9
		25	VSS9	VSS10	26	
DDR_B_DQS#1		27	DQS#1	DM1	28	
DDR_B_DQS1		29	DQS1	RESET#	30	DDR3_DRAMRST#_R — DDR3_DRAMRST#_R <12,13,15>
		31	VSS11	VSS12	32	
DDR_B_D14		33	DQ10	DQ14	34	DDR_B_D10
DDR_B_D15		35	DQ11	DQ15	36	DDR_B_D11
		37	VSS13	VSS14	38	
DDR_B_D16		39	DQ16	DQ20	40	DDR_B_D20
DDR_B_D17		41	DQ17	DQ21	42	DDR_B_D21
		43	VSS15	VSS16	44	
DDR_B_DQS#2		45	DQS#2	DM2	46	
DDR_B_DQS2		47	DQS2	VSS17	48	
		49	VSS18	DQ22	50	DDR_B_D18
DDR_B_D22		51	DQ18	DQ23	52	DDR_B_D19
DDR_B_D23		53	DQ19	VSS19	54	
		55	VSS20	DQ28	56	DDR_B_D28
DDR_B_D24		57	DQ24	DQ29	58	DDR_B_D25
DDR_B_D29		59	DQ25	VSS21	60	
		61	VSS22	DQS#3	62	DDR_B_DQS#3
		63	DM3	DQS3	64	DDR_B_DQS3
		65	VSS23	VSS24	66	
DDR_B_D30		67	DQ26	DQ30	68	DDR_B_D26
DDR_B_D31		69	DQ27	DQ31	70	DDR_B_D27
		71	VSS25	VSS26	72	
<8> DDR_CKE6_DIMM3		73	CKE0	CKE1	74	DDR_CKE7_DIMM3 <8>
		75	VDD1	VDD2	76	
		77	NC1	A15	78	DDR_B_MA15
<8,15> DDR_B_BS2	DDR_B_BS2	79	BA2	A14	80	DDR_B_MA14
		81	VDD3	VDD4	82	
DDR_B_MA12		83	A12/BC#	A11	84	DDR_B_MA11
DDR_B_MA9		85	A9	A7	86	DDR_B_MA7
		87	VDD5	VDD6	88	
DDR_B_MA8		89	A8	A6	90	DDR_B_MA6
DDR_B_MA5		91	A5	A4	92	DDR_B_MA4
		93	VDD7	VDD8	94	
DDR_B_MA3		95	A3	A2	96	DDR_B_MA2
DDR_B_MA1		97	A1	A0	98	DDR_B_MA0
		99	VDD9	VDD10	100	
<8> M_CLK_DDR6	M_CLK_DDR6	101	CK0	CK1	102	M_CLK_DDR7 — M_CLK_DDR7 <8>
<8> M_CLK_DDR#6	M_CLK_DDR#6	103	CK0#	CK1#	104	M_CLK_DDR#7 — M_CLK_DDR#7 <8>
		105	VDD11	VDD12	106	
DDR_B_MA10		107	A10/AP	BA1	108	DDR_B_BS1 — DDR_B_BS1 <8,15>
<8,15> DDR_B_BS0	DDR_B_BS0	109	BA0	RAS#	110	DDR_B_RAS# — DDR_B_RAS# <8,15>
		111	VDD13	VDD14	112	
<8,15> DDR_B_WE#	DDR_B_WE#	113	WE#	S0#	114	DDR_CS6_DIMM3# <8>
<8,15> DDR_B_CAS#	DDR_B_CAS#	115	CAS#	ODT0	116	M_ODT6 — M_ODT6 <8>
		117	VDD15	VDD16	118	
DDR_B_MA13		119	A13	ODT1	120	M_ODT7 — M_ODT7 <8>
<8> DDR_CS7_DIMM3#		121	S1#	NC2	122	
		123	VDD17	VDD18	124	
		125	NCTEST	VREF_CA	126	JDIMM3_VREF_CA
		127	VSS27	VSS28	128	
DDR_B_D36		129	DQ32	DQ36	130	DDR_B_D32
DDR_B_D37		131	DQ33	DQ37	132	DDR_B_D33
		133	VSS29	VSS30	134	
DDR_B_DQS#4		135	DQS#4	DM4	136	
DDR_B_DQS4		137	DQS4	VSS31	138	
		139	VSS32	DQ38	140	DDR_B_D38
DDR_B_D34		141	DQ34	DQ39	142	DDR_B_D39
DDR_B_D35		143	DQ35	VSS33	144	
		145	VSS34	DQ44	146	DDR_B_D40
DDR_B_D44		147	DQ40	DQ45	148	DDR_B_D41
DDR_B_D45		149	DQ41	VSS35	150	
		151	VSS36	DQS#5	152	DDR_B_DQS#5
		153	DM5	DQS5	154	DDR_B_DQS5
		155	VSS37	VSS38	156	
DDR_B_D46		157	DQ42	DQ46	158	DDR_B_D42
DDR_B_D47		159	DQ43	DQ47	160	DDR_B_D43
		161	VSS39	VSS40	162	
DDR_B_D48		163	DQ48	DQ52	164	DDR_B_D52
DDR_B_D49		165	DQ49	DQ53	166	DDR_B_D53
		167	VSS41	VSS42	168	
DDR_B_DQS#6		169	DQS#6	DM6	170	
DDR_B_DQS6		171	DQS6	VSS43	172	
		173	VSS44	DQ54	174	DDR_B_D50
DDR_B_D54		175	DQ50	DQ55	176	DDR_B_D51
DDR_B_D55		177	DQ51	VSS45	178	
		179	VSS46	DQ60	180	DDR_B_D60
DDR_B_D56		181	DQ56	DQ61	182	DDR_B_D61
DDR_B_D57		183	DQ57	VSS47	184	
		185	VSS48	DQS#7	186	DDR_B_DQS#7
		187	DM7	DQS7	188	DDR_B_DQS7
		189	VSS49	VSS50	190	
DDR_B_D62		191	DQ58	DQ62	192	DDR_B_D58
DDR_B_D63		193	DQ59	DQ63	194	DDR_B_D59
		195	VSS51	VSS52	196	
DIMM3_SA0		197	SA0	EVENT#	198	
		199	VDDSPD	SDA	200	DDR_XDP_WAN_SMBDAT <12,13,15,17,18,35,43>
DIMM3_SA1		201	SA1	SCL	202	DDR_XDP_WAN_SMBCLK <12,13,15,17,18,35,43>
+0.75V_DDR_VTT		203	VTT1	VTT2	204	+0.75V_DDR_VTT
		205	G1	G2	206	

+DIMM3_VREF_CA — @RD25 1 2 0_0402_5%~D — +V_DDR_REF
2.2U_0603_6.3V6K~D (CD63) 0.1U_0402_16V4Z~D (CD64)

Due to +PWR_SRC trace width nearby H16 wasn't enough, we have to increase it.so remove RD30 & RD31.

Link CIS OK_1006

follow connector list 1005A.

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT3

Size | Document Number: LA-7931P | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 14 of 70

JDIMM4 STD Type H=5.2

All VREF traces should have 10 mil trace width

<8,14> DDR_B_DQS#[0..7]
<8,14> DDR_B_D[0..63]
<8,14> DDR_B_DQS[0..7]
<8,14> DDR_B_MA[0..15]

+V_DDR_REFB_M3 — @RD32 2_0_0402_5%~D
+V_DDR_REF — @RD33 2_0_0402_5%~D
+DIMM4_VREF_DQ
CD71 2.2U_0603_6.3V6K~D
CD72 0.1U_0402_16V4Z~D

+1.5V_MEM
CD67 1U_0402_6.3V6K~D
CD68 1U_0402_6.3V6K~D
CD69 1U_0402_6.3V6K~D
CD70 1U_0402_6.3V6K~D

+1.5V_MEM
CD73 10U_0603_6.3V6M~D
CD74 10U_0603_6.3V6M~D
CD75 10U_0603_6.3V6M~D
CD76 10U_0603_6.3V6M~D
CD77 10U_0603_6.3V6M~D
CD78 10U_0603_6.3V6M~D
CD79 10U_0603_6.3V6M~D
CD80 330U_SX_2V~D

Layout Note:
Place near JDIMM3.Pin 203,204

+0.75V_DDR_VTT
CD81 1U_0402_6.3V6K~D
CD82 1U_0402_6.3V6K~D
CD83 1U_0402_6.3V6K~D
CD84 1U_0402_6.3V6K~D

DIMM Select

+3.3V_RUN
@RD35 10K_0402_5%~D
RD36 10K_0402_5%~D
DIMM4_SA0
DIMM4_SA1
RD37 10K_0402_5%~D
@RD38 10K_0402_5%~D

SA0	SA1	
1	0	DIMM1
0	0	DIMM2
1	1	DIMM3
0	1	DIMM4

+3.3V_RUN
CD87 0.1U_0402_16V4Z~D
CD88 2.2U_0603_6.3V6K~D
+0.75V_DDR_VTT

+1.5V_MEM
JDIMM4 CONN@
TYCO_2-2013289-1~D

	1	VREF_DQ	VSS1	2	
	3	VSS2	DQ4	4	DDR_B_D4
DDR_B_D0	5	DQ0	DQ5	6	DDR_B_D5
DDR_B_D1	7	DQ1	VSS3	8	
	9	VSS4	DQS#0	10	DDR_B_DQS#0
	11	DM0	DQS0	12	DDR_B_DQS0
	13	VSS5	VSS6	14	
DDR_B_D6	15	DQ2	DQ6	16	DDR_B_D2
DDR_B_D7	17	DQ3	DQ7	18	DDR_B_D3
	19	VSS7	VSS8	20	
DDR_B_D8	21	DQ8	DQ12	22	DDR_B_D12
DDR_B_D9	23	DQ9	DQ13	24	DDR_B_D13
	25	VSS9	VSS10	26	
DDR_B_DQS#1	27	DQS#1	DM1	28	
DDR_B_DQS1	29	DQS1	RESET#	30	DDR3_DRAMRST#_R
	31	VSS11	VSS12	32	
DDR_B_D10	33	DQ10	DQ14	34	DDR_B_D14
DDR_B_D11	35	DQ11	DQ15	36	DDR_B_D15
	37	VSS13	VSS14	38	
DDR_B_D20	39	DQ16	DQ20	40	DDR_B_D16
DDR_B_D21	41	DQ17	DQ21	42	DDR_B_D17
	43	VSS15	VSS16	44	
DDR_B_DQS#2	45	DQS#2	DM2	46	
DDR_B_DQS2	47	DQS2	VSS17	48	
	49	VSS18	DQ22	50	DDR_B_D22
DDR_B_D18	51	DQ18	DQ23	52	DDR_B_D23
DDR_B_D19	53	DQ19	VSS19	54	
	55	VSS20	DQ28	56	DDR_B_D24
DDR_B_D28	57	DQ24	DQ29	58	DDR_B_D29
DDR_B_D25	59	DQ25	VSS21	60	
	61	VSS22	DQS#3	62	DDR_B_DQS#3
	63	DM3	DQS3	64	DDR_B_DQS3
	65	VSS23	VSS24	66	
DDR_B_D26	67	DQ26	DQ30	68	DDR_B_D30
DDR_B_D27	69	DQ27	DQ31	70	DDR_B_D31
	71	VSS25	VSS26	72	
<8> DDR_CKE2_DIMM4	73	CKE0	CKE1	74	DDR_CKE3_DIMM4 <8>
	75	VDD1	VDD2	78	DDR_B_MA15
<8,14> DDR_B_BS2	79	NC1	A15	80	DDR_B_MA14
	81	BA2	A14	82	
DDR_B_MA12	83	VDD3	VDD4	84	DDR_B_MA11
DDR_B_MA9	85	A12/BC#	A11	86	DDR_B_MA7
	87	A9	A7	88	
DDR_B_MA8	89	VDD5	VDD6	90	DDR_B_MA6
DDR_B_MA5	91	A8	A6	92	DDR_B_MA4
	93	A5	A4	94	
DDR_B_MA3	95	VDD7	VDD8	96	DDR_B_MA2
DDR_B_MA1	97	A3	A2	98	DDR_B_MA0
	99	A1	A0	100	
<8> M_CLK_DDR2	101	VDD9	VDD10	102	M_CLK_DDR3
<8> M_CLK_DDR#2	103	CK0	CK1	104	M_CLK_DDR#3
	105	CK0#	CK1#	106	
DDR_B_MA10	107	VDD11	VDD12	108	DDR_B_BS1 <8,14>
<8,14> DDR_B_BS0	109	A10/AP	BA1	110	DDR_B_RAS# <8,14>
	111	BA0	RAS#	112	
<8,14> DDR_B_WE#	113	VDD13	VDD14	114	
<8,14> DDR_B_CAS#	115	WE#	S0#	116	DDR_CS2_DIMM4# <8>
	117	CAS#	ODT0	118	M_ODT2 <8>
DDR_B_MA13	119	VDD15	VDD16	120	M_ODT3 <8>
<8> DDR_CS3_DIMM4#	121	A13	ODT1	122	
	123	S1#	NC2	124	
	125	VDD17	VDD18	126	
	127	NCTEST	VREF_CA	128	
DDR_B_D32	129	VSS27	VSS28	130	DDR_B_D36
DDR_B_D33	131	DQ32	DQ36	132	DDR_B_D37
	133	DQ33	DQ37	134	
DDR_B_DQS#4	135	VSS29	VSS30	136	
DDR_B_DQS4	137	DQS#4	DM4	138	
	139	DQS4	VSS31	140	DDR_B_D34
DDR_B_D38	141	VSS32	DQ38	142	DDR_B_D35
DDR_B_D39	143	DQ34	DQ39	144	
	145	DQ35	VSS33	146	DDR_B_D44
DDR_B_D40	147	VSS34	DQ44	148	DDR_B_D45
DDR_B_D41	149	DQ40	DQ45	150	
	151	DQ41	VSS35	152	DDR_B_DQS#5
	153	VSS36	DQS#5	154	DDR_B_DQS5
	155	DM5	DQS5	156	
DDR_B_D42	157	VSS37	VSS38	158	DDR_B_D46
DDR_B_D43	159	DQ42	DQ46	160	DDR_B_D47
	161	DQ43	DQ47	162	
DDR_B_D52	163	VSS39	VSS40	164	DDR_B_D48
DDR_B_D53	165	DQ48	DQ52	166	DDR_B_D49
	167	DQ49	DQ53	168	
DDR_B_DQS#6	169	VSS41	VSS42	170	
DDR_B_DQS6	171	DQS#6	DM6	172	
	173	DQS6	VSS43	174	DDR_B_D54
DDR_B_D50	175	VSS44	DQ54	176	DDR_B_D55
DDR_B_D51	177	DQ50	DQ55	178	
	179	DQ51	VSS45	180	DDR_B_D56
DDR_B_D60	181	VSS46	DQ60	182	DDR_B_D57
DDR_B_D61	183	DQ56	DQ61	184	
	185	DQ57	VSS47	186	DDR_B_DQS#7
	187	VSS48	DQS#7	188	DDR_B_DQS7
	189	DM7	DQS7	190	
DDR_B_D58	191	VSS49	VSS50	192	DDR_B_D62
DDR_B_D59	193	DQ58	DQ62	194	DDR_B_D63
	195	DQ59	DQ63	196	
DIMM4_SA0	197	VSS51	VSS52	198	
	199	SA0	EVENT#	200	
DIMM4_SA1	201	VDDSPD	SDA	202	DIMM4_SMBDAT @RD39 1 — 2 0_0402_5%~D — DDR_XDP_WAN_SMBDAT <12,13,14,17,18,35,43>
	203	SA1	SCL	204	DIMM4_SMBCLK @RD40 1 — 2 0_0402_5%~D — DDR_XDP_WAN_SMBCLK <12,13,14,17,18,35,43>
	205	VTT1	VTT2	206	+0.75V_DDR_VTT
		G1	G2		

+1.5V_MEM — +1.5V_MEM

DDR3_DRAMRST#_R <12,13,14>

+DIMM4_VREF_CA
@RD34 1 — 2 0_0402_5%~D — +V_DDR_REF
CD85 2.2U_0603_6.3V6K~D
CD86 0.1U_0402_16V4Z~D

JDIMM3 (Ch B1 H=9.2 STD)
JDIMM1 (Ch A1 H=5.2 STD)
TOP
CPU
BOT
JDIMM2 (Ch A0 H=5.2 REV)
JDIMM4 (Ch B0 H=5.2 STD)

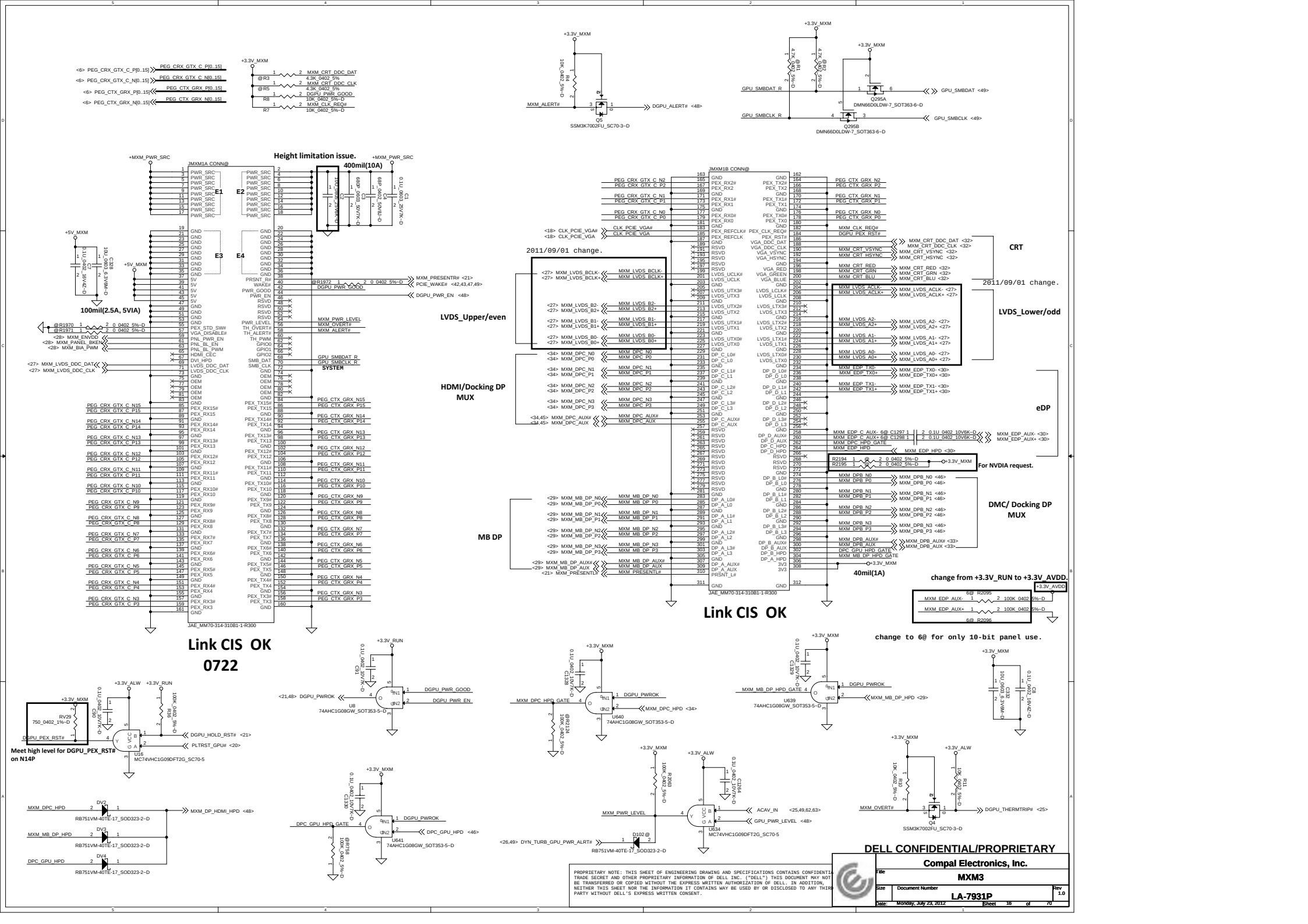
Link CIS OK
0722

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT4
Size: Document Number: LA-7931P
Rev: 1.0
Date: Monday, July 23, 2012
Sheet 15 of 70


Height limitation issue.
400mil(10A)
100mil(2.5A, 5VIA)
2011/09/01 change.
LVDS_Upper/even
HDMI/Docking DP MUX
MB DP
SYSTEM
CRT
LVDS_Lower/odd
eDP
DMC/ Docking DP MUX
40mil(1A)
For NVDIA request.
change from +3.3V_RUN to +3.3V_AVDD.
change to 6@ for only 10-bit panel use.
Meet high level for DGPU_PEX_RST# on N14P
Link CIS OK
0722
Link CIS OK
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
MXM3
LA-7931P
Monday, July 23, 2012

Pop them until ST.

Pop them until ST.

Link CIS OK
0722

Crystal EA.

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs
Low - Enable External VRs

On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low

PCH_AZ_SYNC is sampled at the rising edge of RSMRST# pin. So signal should be PU to the ALWAYS rail.

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

CMOS place near DIMM

INTEL HDA_SYNC isolation circuit

Pop them until ST.

BIOS ROM Select Component		
	X76(Main) X7640631L01	X76(2nd) X7640631L03
	WINBOND	EON
U52	SA000039A2L (W25Q64FVSSIG)	SA000046400 (EN25Q64-104HIP)
U53	SA00003K80L (W25Q32BVSSIG)	SA00004LI00 (EN25Q32B-104HIP)

200 MIL SO8
64Mb Flash ROM
Create X76 BOM for 2nd source.

200 MIL SO8
32Mb Flash ROM
Create X76 BOM for 2nd source.

Follow conn list 1223A.

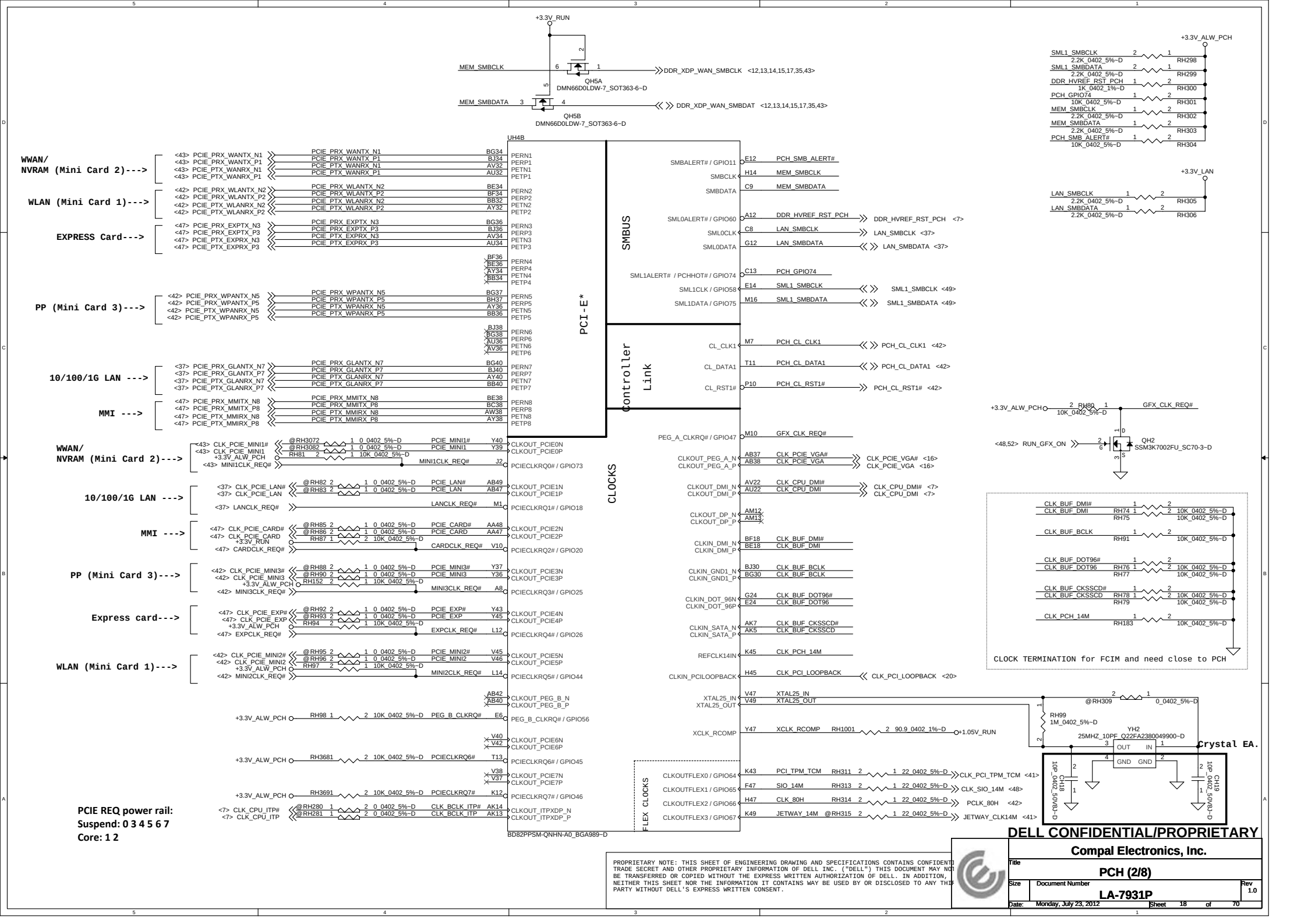
Link CIS OK
0109

No Reboot Strap	
SPKR	Low = Default
	High = No Reboot

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIA TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.		
Title: PCH (1/8)		
Size	Document Number: LA-7931P	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 17 of 70	

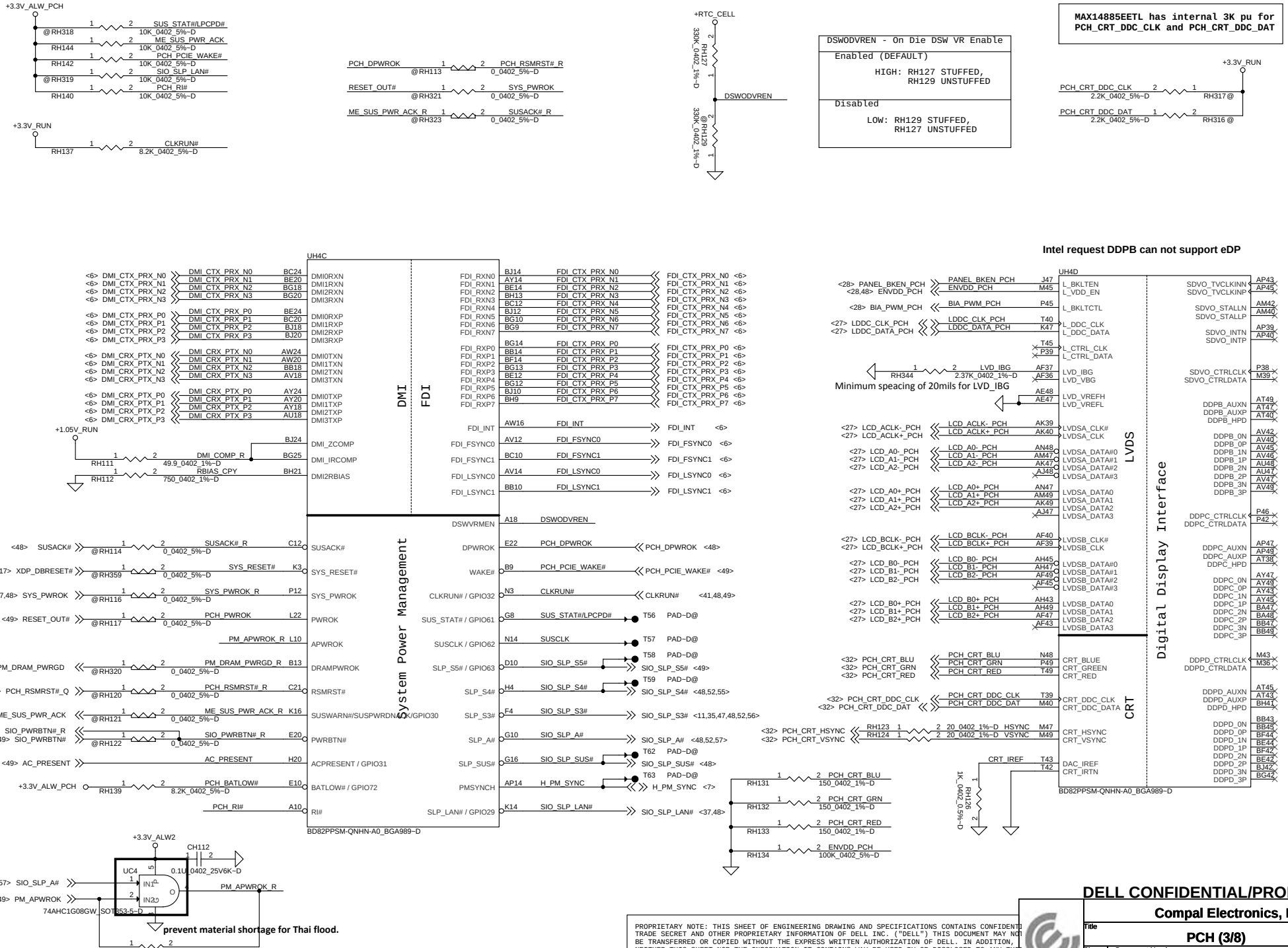


PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTI
TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NO
BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION,
NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THI
PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	PCH (2/8)	
Size	Document Number: LA-7931P	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 18 of 70	

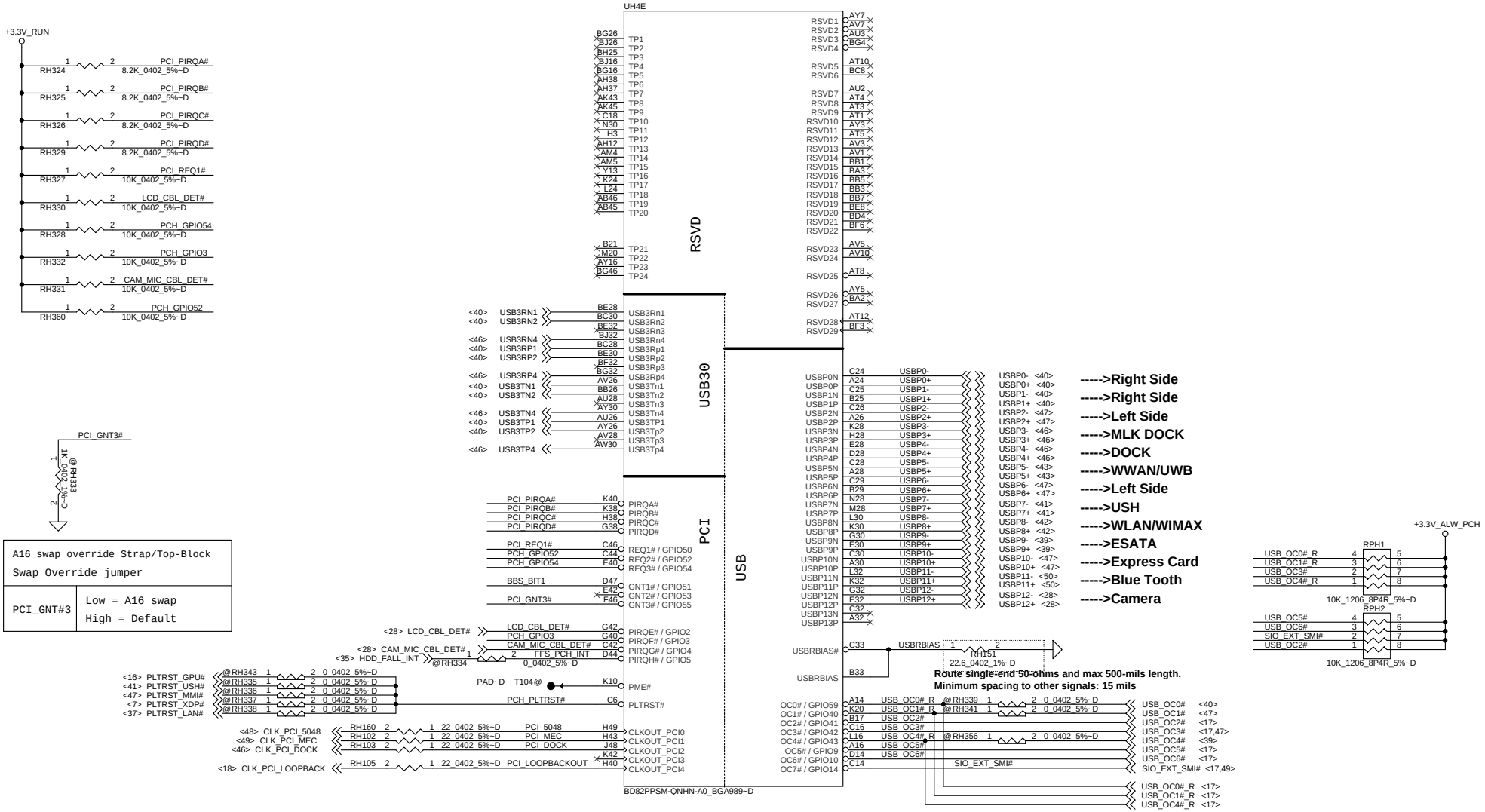


PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	PCH (3/8)	
Size	Document Number: LA-7931P	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 19 of 70	



Boot BIOS Strap		
BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
* 1	1	SPI

DELL CONFIDENTIAL/PROPRIETARY

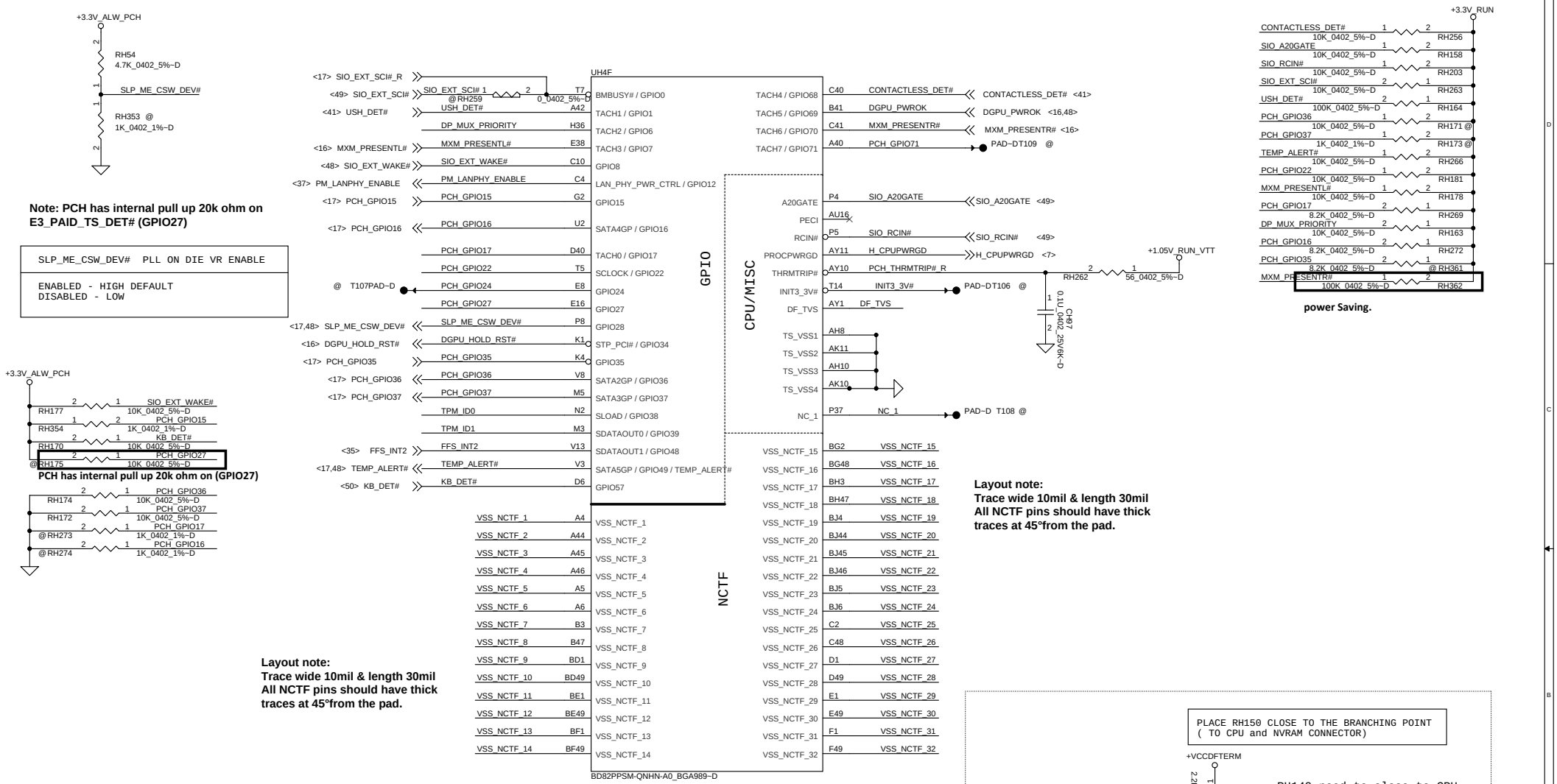
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: PCH (4/8)

Size | Document Number: LA-7931P | Rev: 1.0

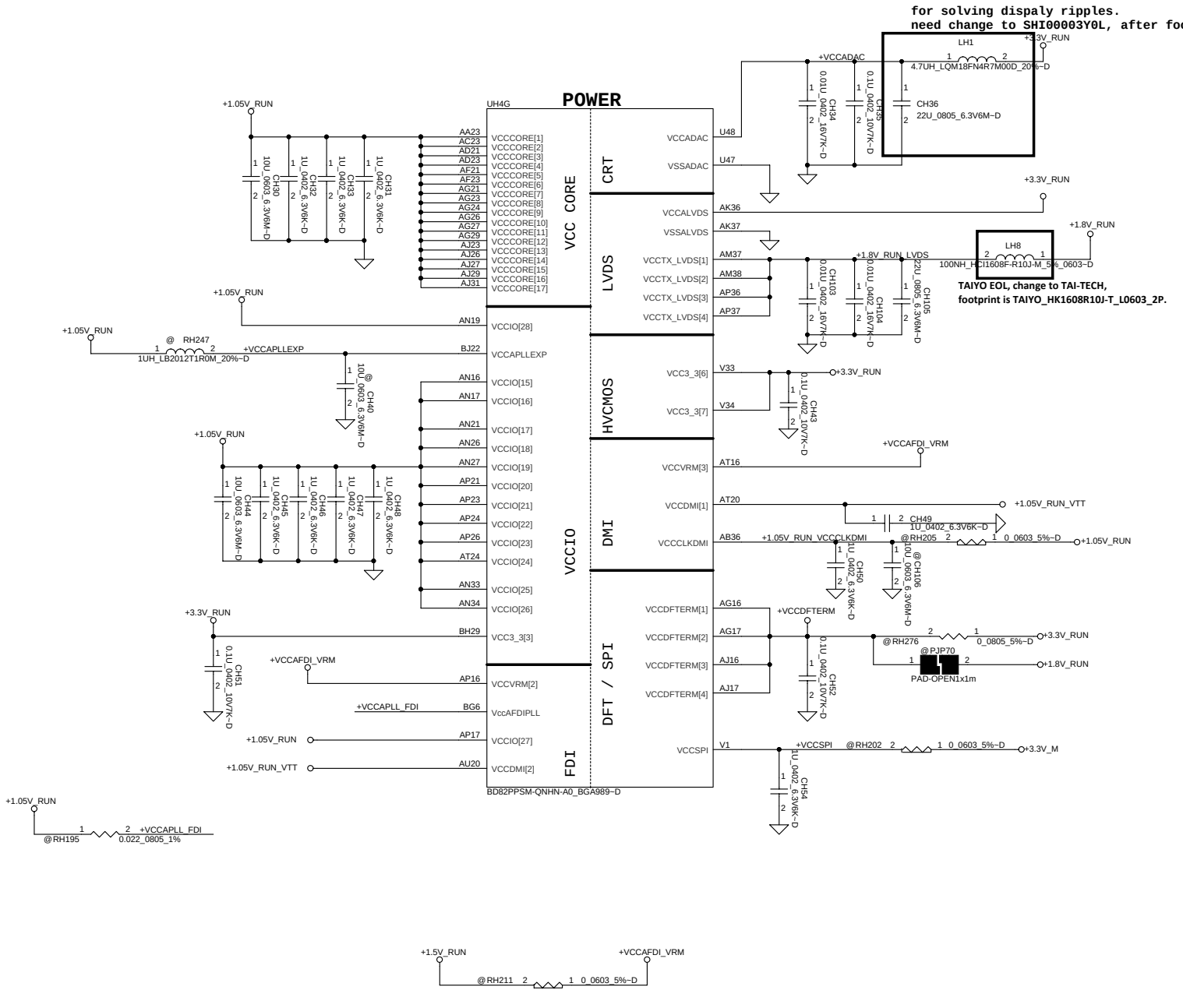
Date: Monday, July 23, 2012 | Sheet 20 of 70



PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTI TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NO BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THI PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	PCH (5/8)
Size	Document Number: LA-7931P
Rev	1.0
Date: Monday, July 23, 2012	Sheet 21 of 70



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC3	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VCCDFTERM	1.8	0.002
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTI
TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NO
BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION,
NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THI
PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

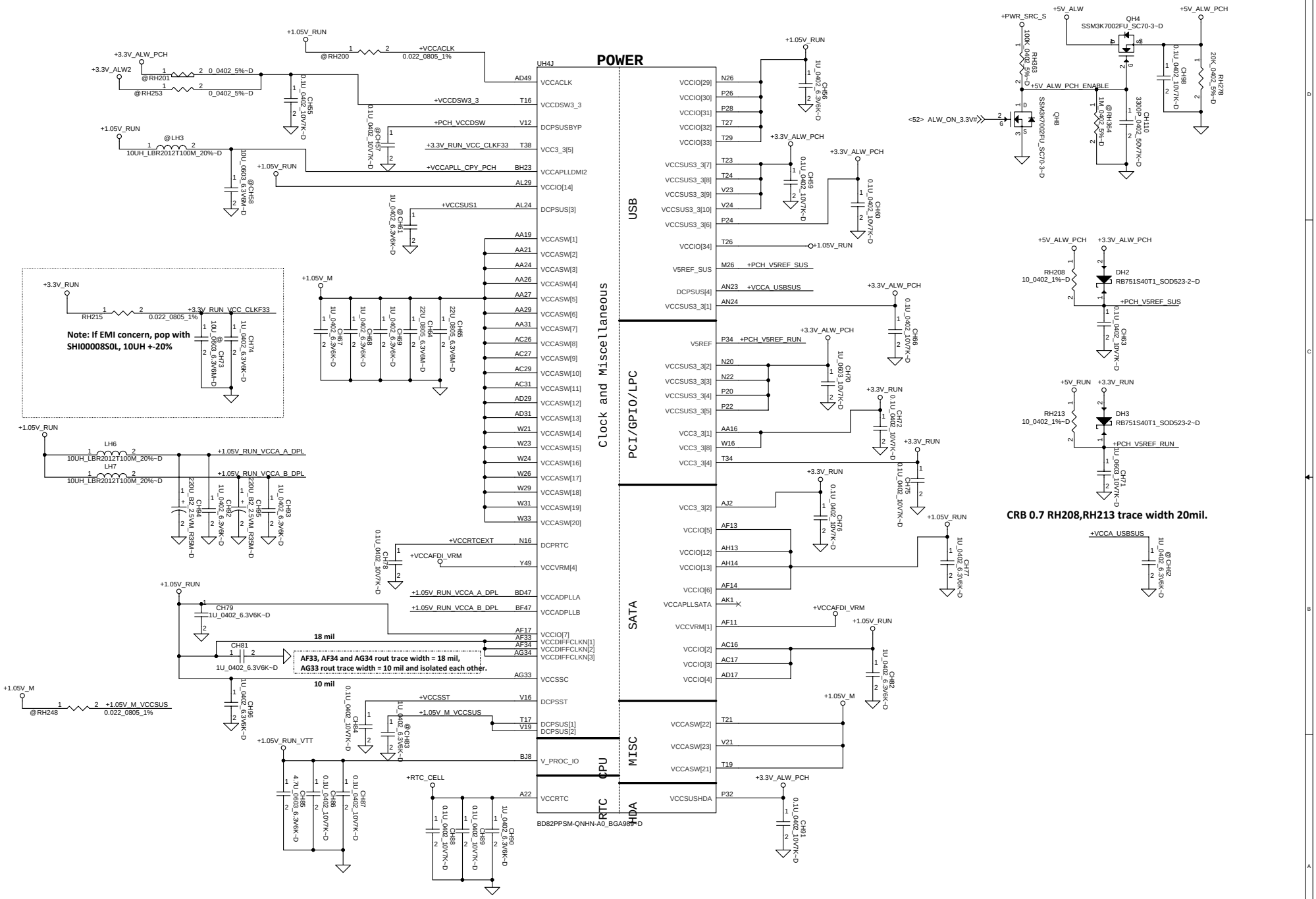
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: PCH (6/8)

Size: | Document Number: LA-7931P | Rev: 1.0

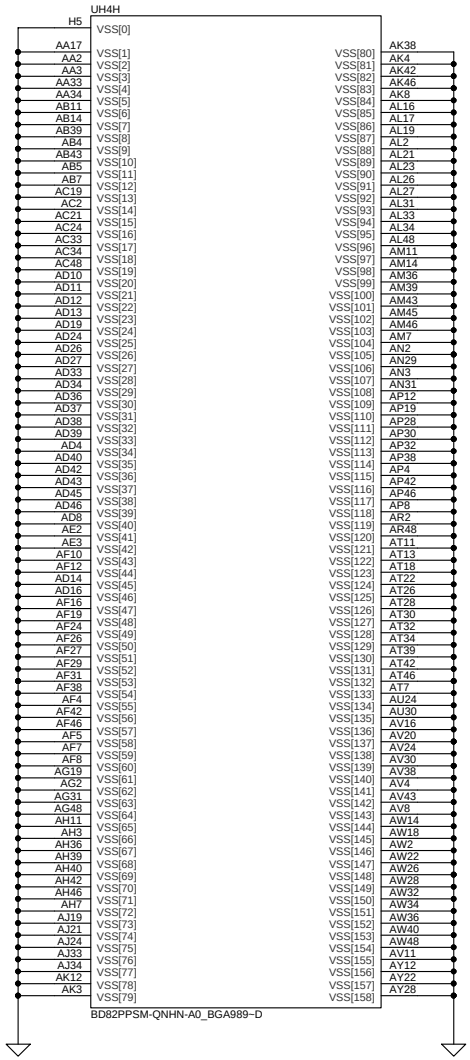
Date: Monday, July 23, 2012 | Sheet 22 of 70

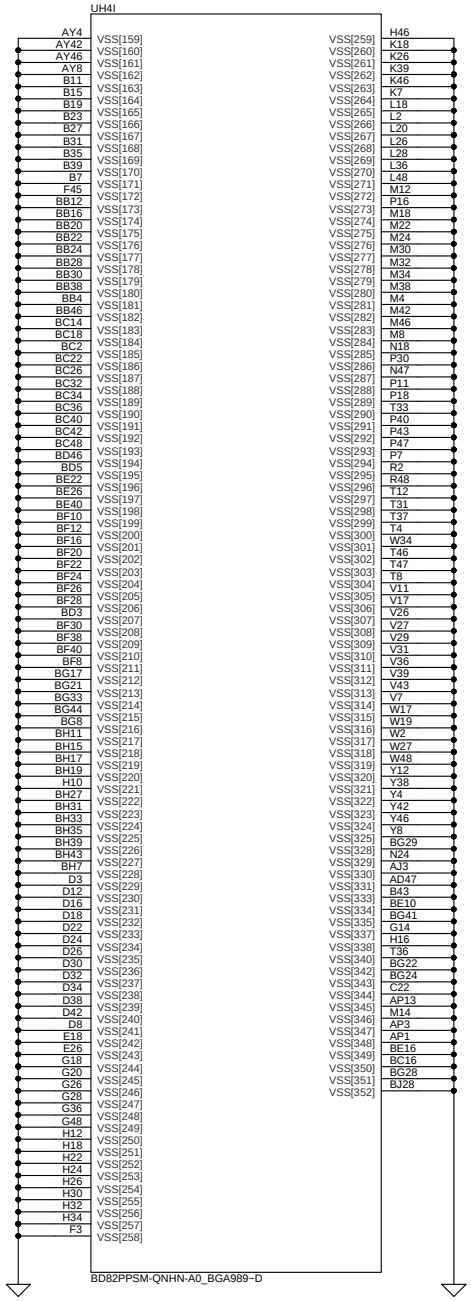


PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	PCH (7/8)
Size	Document Number: LA-7931P
Rev	1.0
Date: Monday, July 23, 2012	Sheet 23 of 70





PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: PCH (8/8)

Size | Document Number: LA-7931P | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 24 of 70

Place Q26 under CPU for OTP sensor.
Place C339 close to the Q26 as possible

Q26
MMBT3904WT1G_SC70-3~D

Q15
MMBT3904WT1G_SC70-3~D

Put Q17 on the Bot side for Skin temperature

Q17
MMBT3904WT1G_SC70-3~D

Place Q33 under Stack_SODIMM on TOP side.

Q33
MMBT3904WT1G_SC70-3~D

Place Q14 near Docking CONN on BOT side

Q14
MMBT3904WT1G_SC70-3~D

Place Q16 under Butterfly's CH B (BOT side).

Q16
MMBT3904WT1G_SC70-3~D

CPU FAN

Follow conn list 0301A.

CONN@ JFAN1
ACES_50271-00401N-001

Link CIS OK
0301

MXM FAN

Follow conn list 0301A.

CONN@ JFAN2
ACES_50271-0040N-001

Link CIS OK
0301

U18
EMC4002-HZH C_QFN48_7X7~D

change VSET from 88℃ to 93℃.

Rest=1330 ohm, Tp=93 degree

prevent material shortage for Thai flood.

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

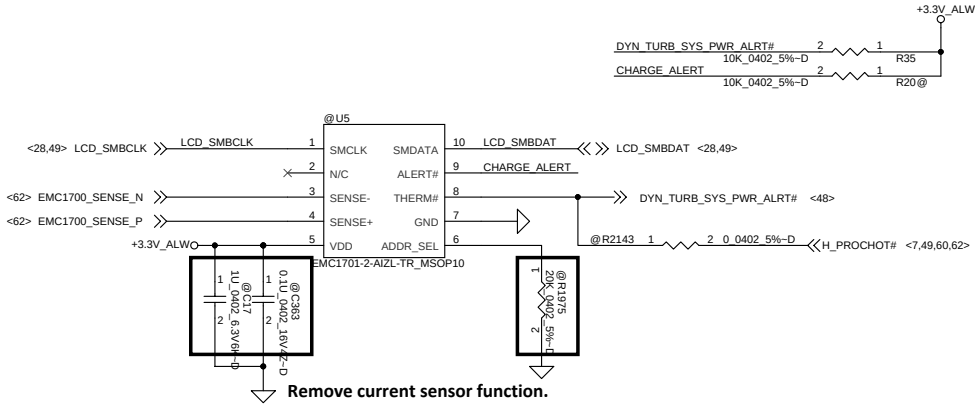
Title: FAN control

Size: | Document Number: LA-7931P | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 25 of 70

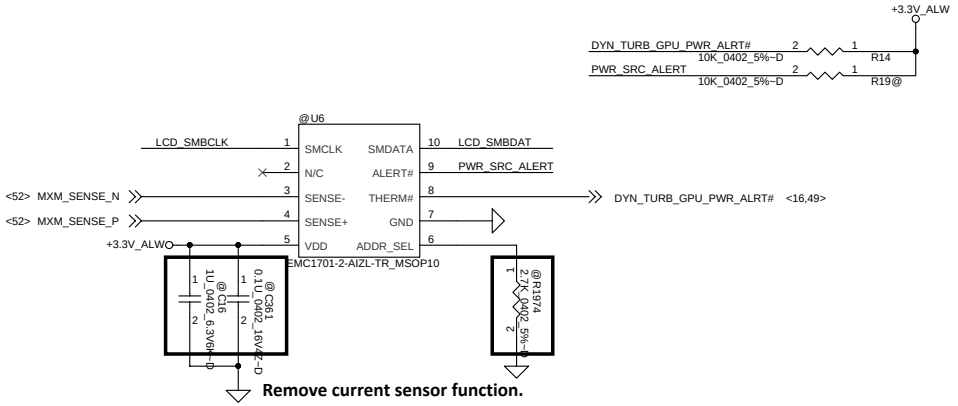
Monitor Charger current

RESISTOR (5%)	SMBUS ADDRESS
0	1001_100(r/w)
100	1001_101(r/w)
180	1001_110(r/w)
300	1001_111(r/w)
430	1001_000(r/w)
560	1001_001(r/w)
750	1001_010(r/w)
1270	1001_011(r/w)
1600	0101_000(r/w)
2000	0101_001(r/w)
2700	0101_010(r/w)
3600	0101_011(r/w)
5600	0101_100(r/w)
9100	0101_100(r/w)
20000	0101_101(r/w)
Open	0011_000(r/w)



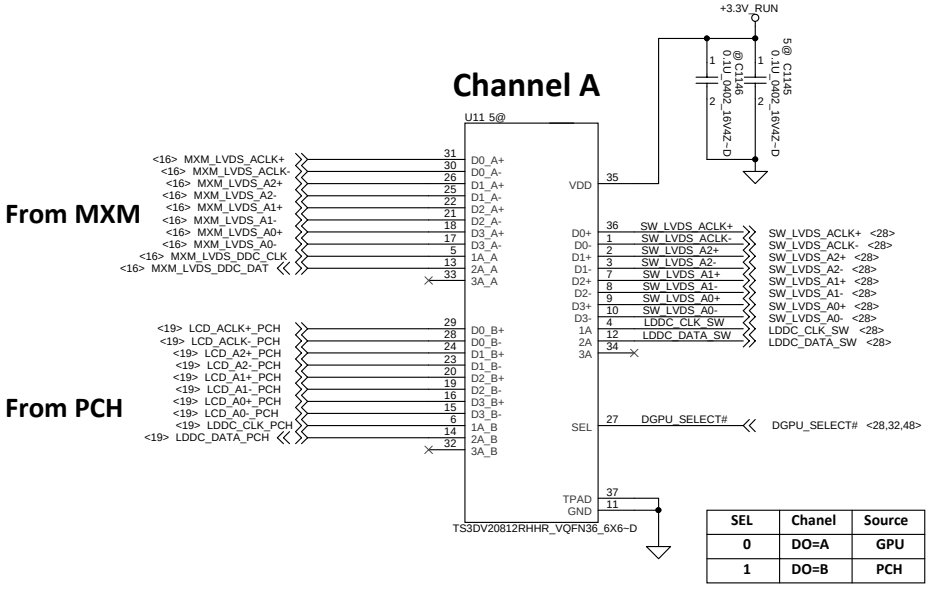
Remove current sensor function.

Monitor PWR_SRC_MXM

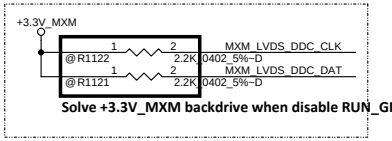


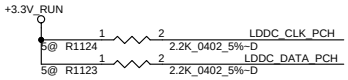
Remove current sensor function.

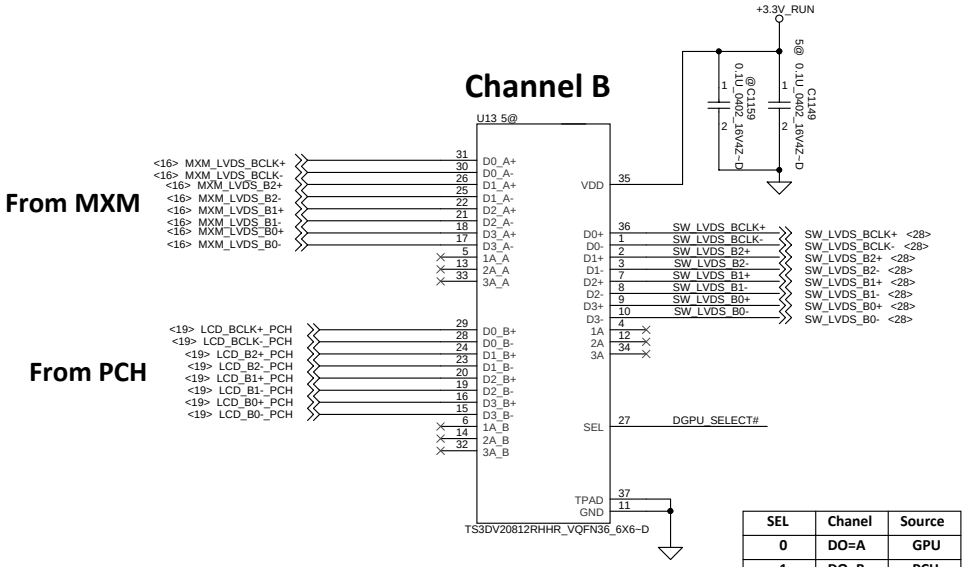
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTI
TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT
BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION,
NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIR
PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.



SEL	Chanel	Source
0	DO=A	GPU
1	DO=B	PCH





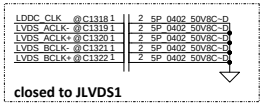


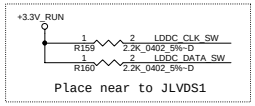
SEL	Chanel	Source
0	DO=A	GPU
1	DO=B	PCH

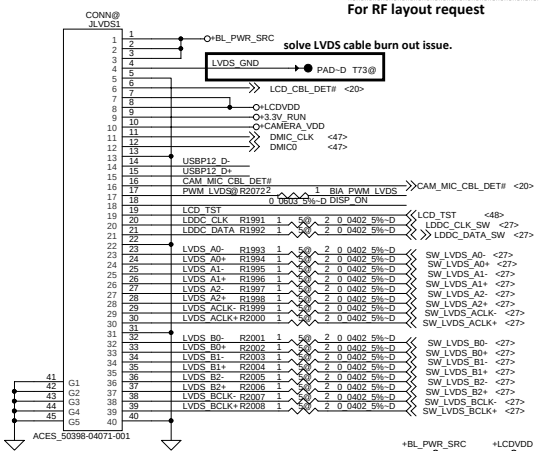
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.
Title: LVDS SW
Size: Document Number: LA-7931P
Rev: 1.0
Date: Monday, July 23, 2012
Sheet 27 of 70

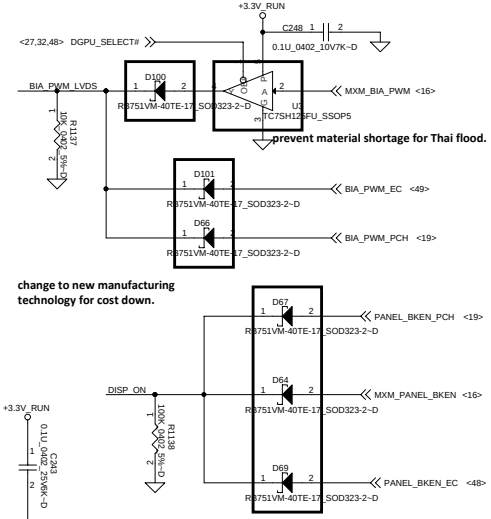
For 6-bit LCD panel



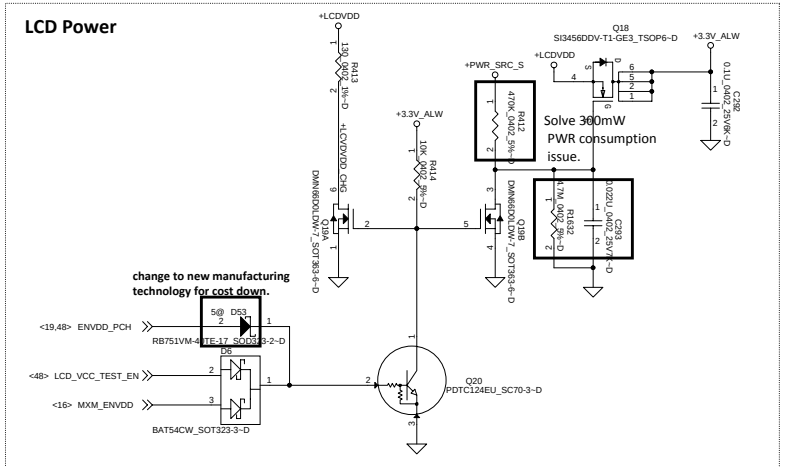




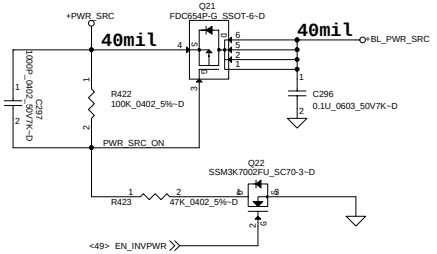
Link CIS OK
0914



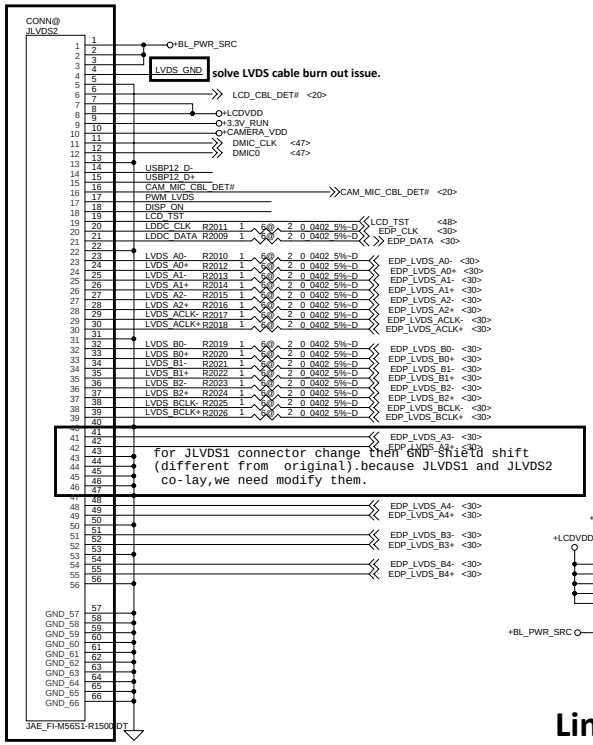
LCD Power



Panel backlight power control by EC

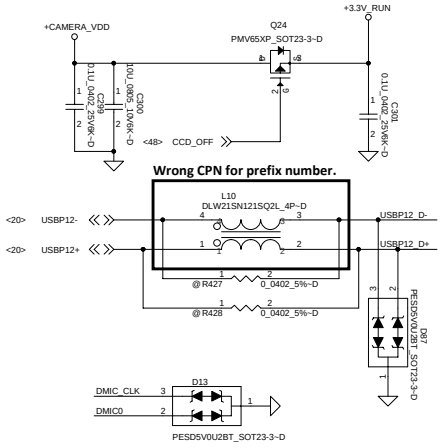


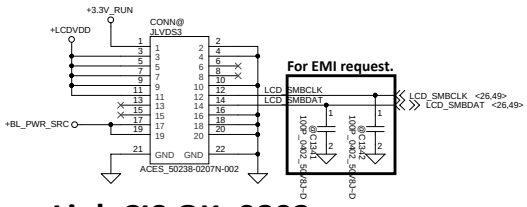
For 10-bit LCD panel



Link CIS OK
CONN list_0511

Webcam Circuit





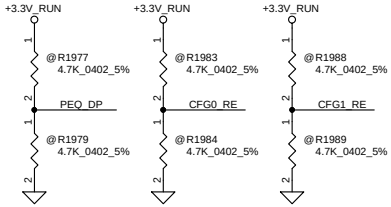
Link CIS OK_0802

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.	
Title	LVDS & CAM & TS
Size	Document Number: LA-7931P
Rev	1.0
Date: Monday, July 23, 2012	Sheet 28 of 70

DP v1.2 Redriver

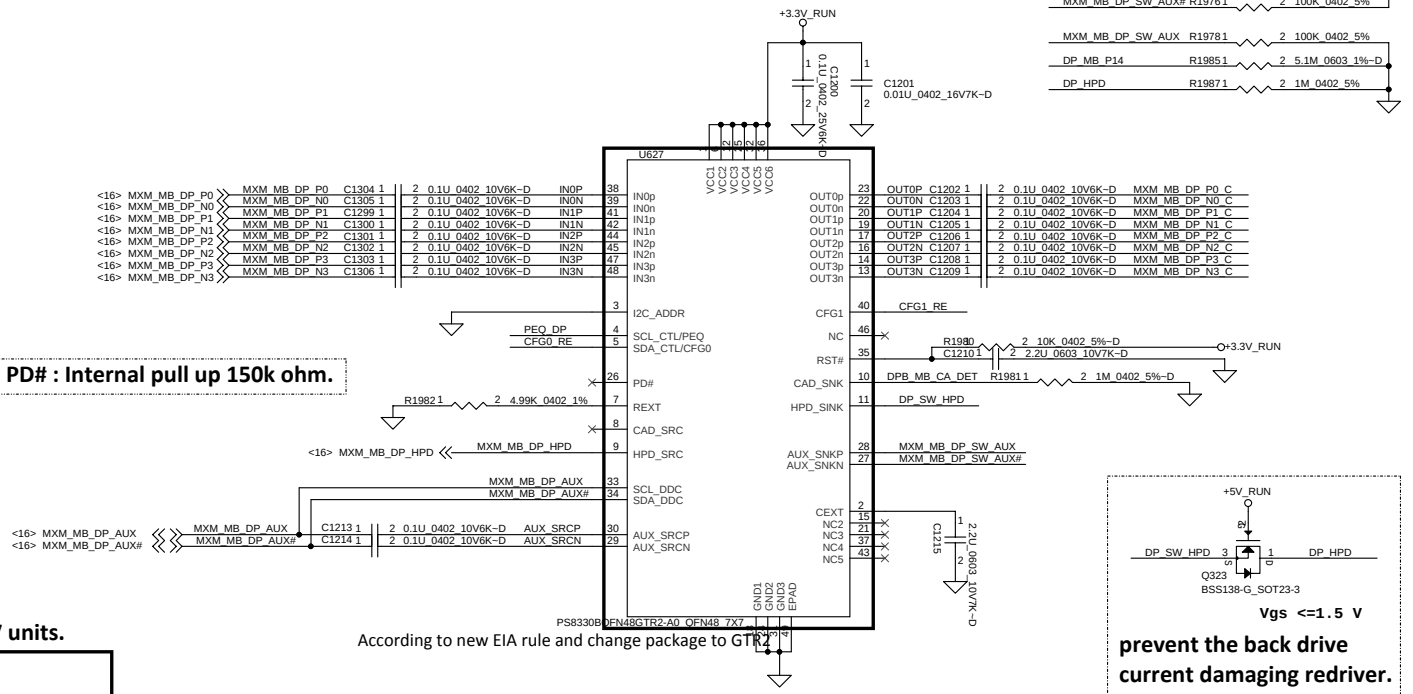


Programmable input equalization levels; Internal pull down at ~150k ohm, 3.3V I/O.
- L: default, LEQ, compensate channel loss up to 12dB @ HBR2
- H: HEQ, compensate channel loss up to 15dB @ HBR2
- M: LLEQ, compensate channel loss up to 5dB @ HBR2

Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k ohm, 3.3V I/O.
- L: default, automatic EQ enable & AUX interception enable
- H: automatic EQ disable & AUX interception enable
- M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
- H: default, auto test disable & input offset cancellation enable
- L: auto test enable & input offset cancellation enable
- M: auto test disable & input offset cancellation disable

PD# : Internal pull up 150k ohm.

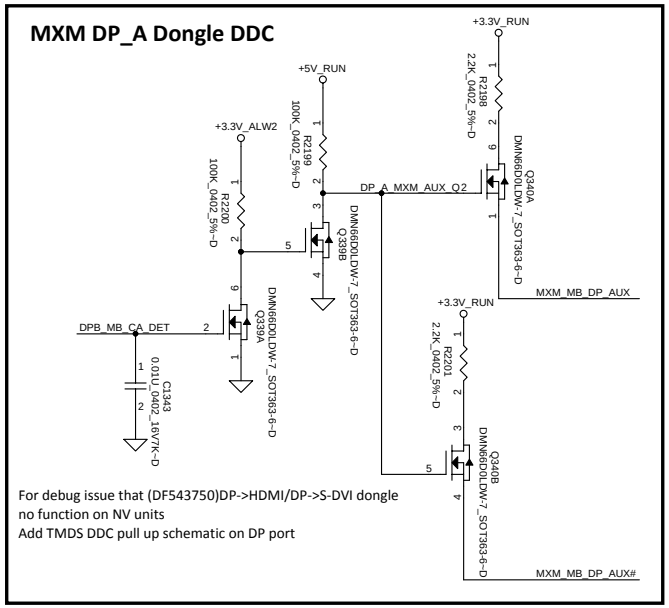


According to new EIA rule and change package to GTR2

Vgs <=1.5 V

prevent the back drive current damaging redriver.

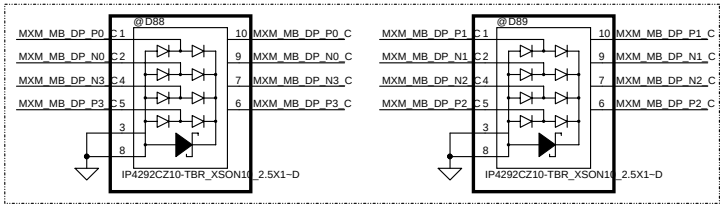
Solve DP->HDMI/DP->S-DVI dongle no function on NV units.

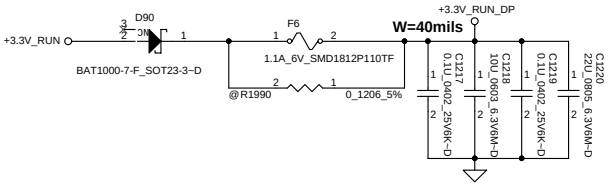


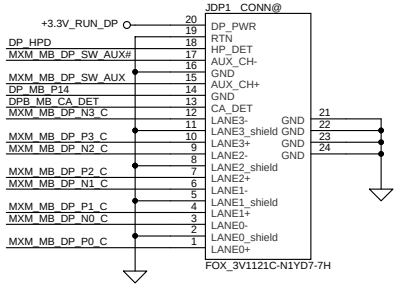
For debug issue that (DF543750)DP->HDMI/DP->S-DVI dongle no function on NV units
Add TMDS DDC pull up schematic on DP port

Place close JDP

ESD request change main source to SC300002F0L.







Link CIS OK_0722

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.	
Title	DP Redriver & DP CONN
Size	Document Number: LA-7931P
Rev	1.0
Date: Monday, July 23, 2012	Sheet 29 of 70

prevent current leakage.

prevent AUX swing overshoot

Pin E4 : General Purpose Schmitt trigger Input / Tri-state Output 14 [5V Tolerant]

meet RGB panel sequencing

meet RGB panel sequencing

meet RGB panel sequencing

PLACE THESE PARTS NEAR STDP4010
vendor suggest.

BootStraps

1Mb Flash ROM

DELL CONFIDENTIAL/PROPRIETARY

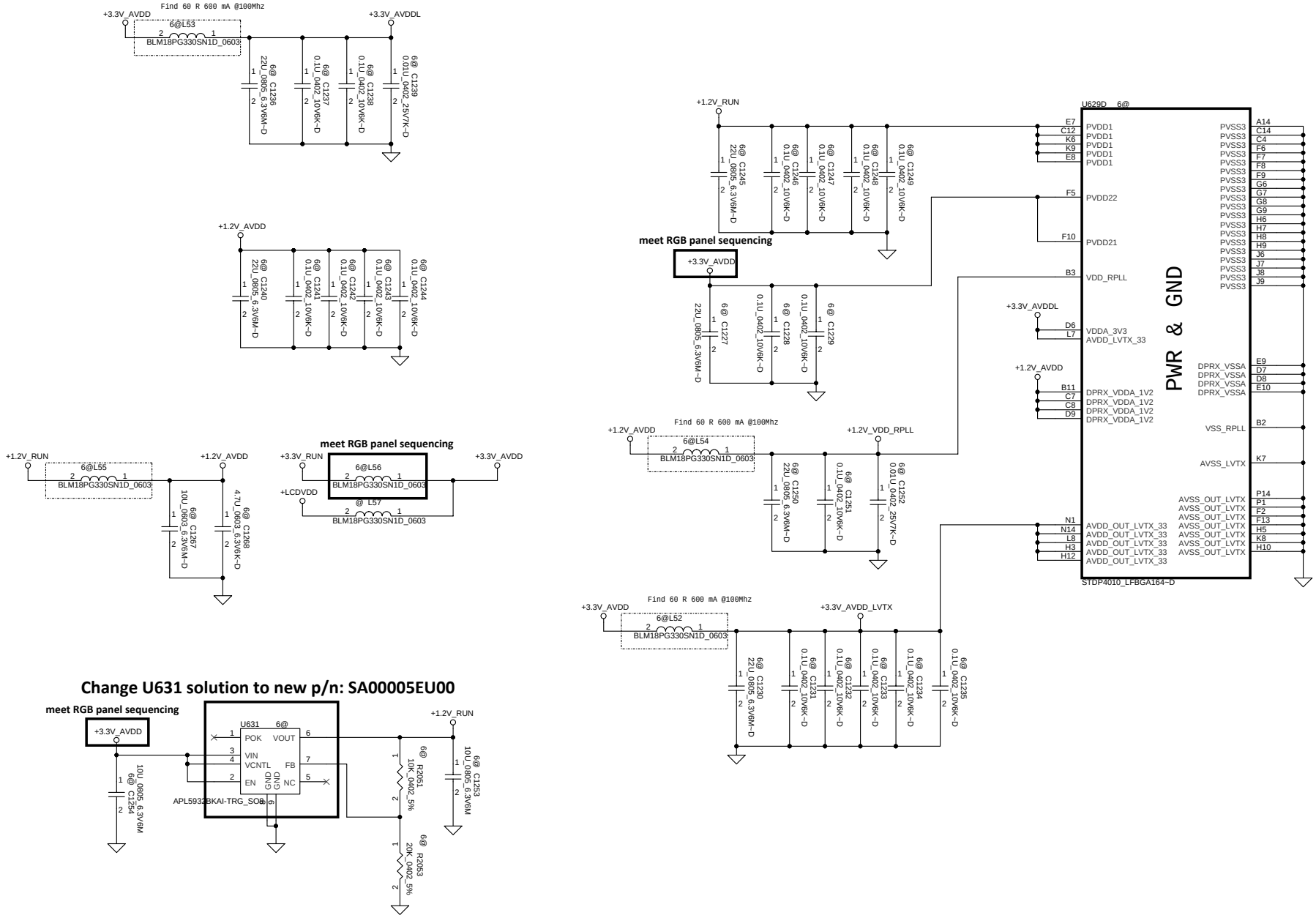
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: eDP to LVDS(1)

Size: | Document Number: LA-7931P | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 30 of 70



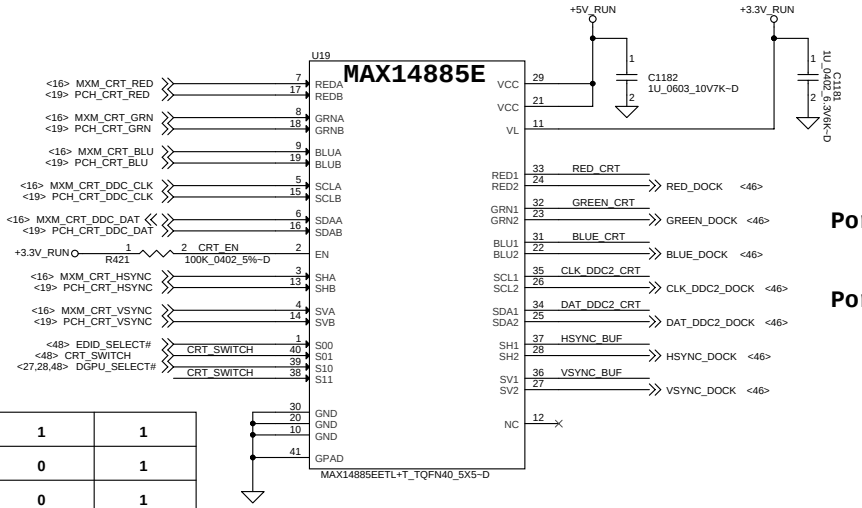
DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTI
TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NO
BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION,
NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THI
PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.	
Title	eDP to LVDS(2)
Size	Document Number: LA-7931P
Rev	1.0
Date:	Monday, July 23, 2012
Sheet	31 of 70

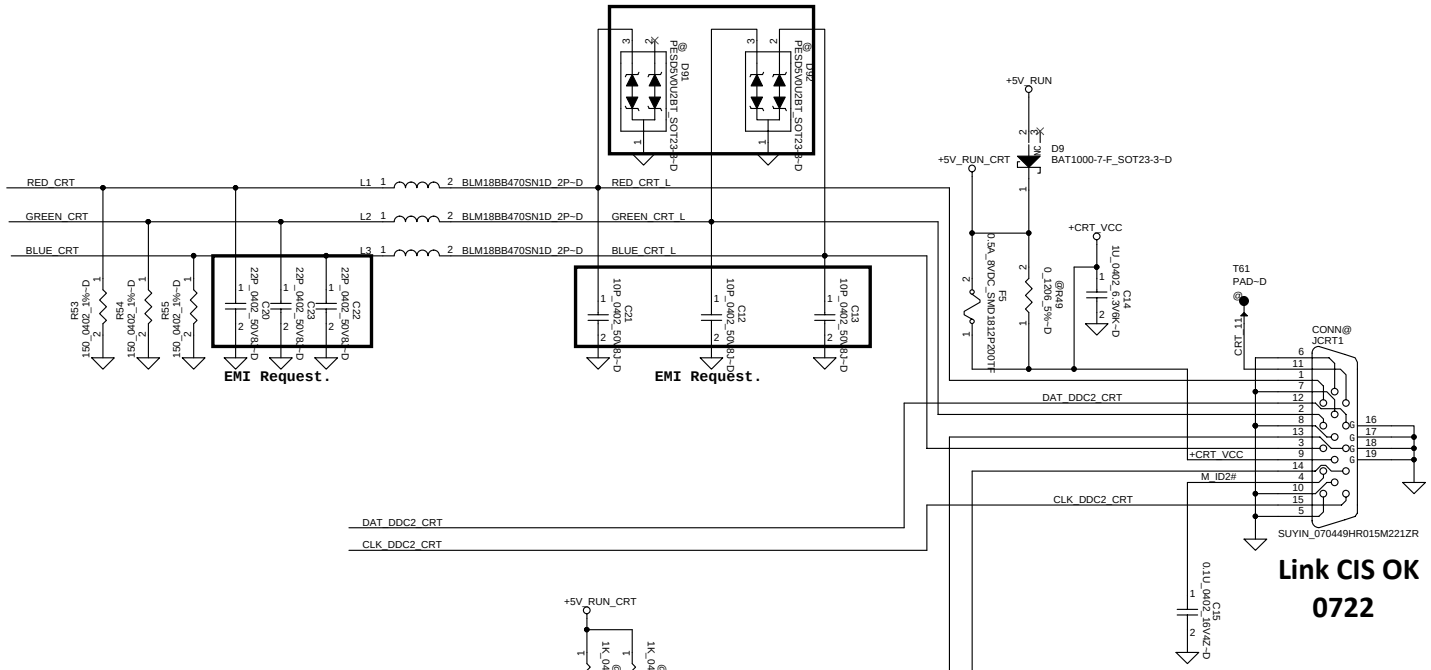
Channel A --> GPU

Channel B --> PCH



CRT_SWITCH	0	0	1	1
DGPU_SELECT#	0	1	0	1
EDID_SELECT#	0	1	0	1
	A --> Port 1	B --> Port 1	A --> Port 2	B --> Port 2

ESD request reserve it.



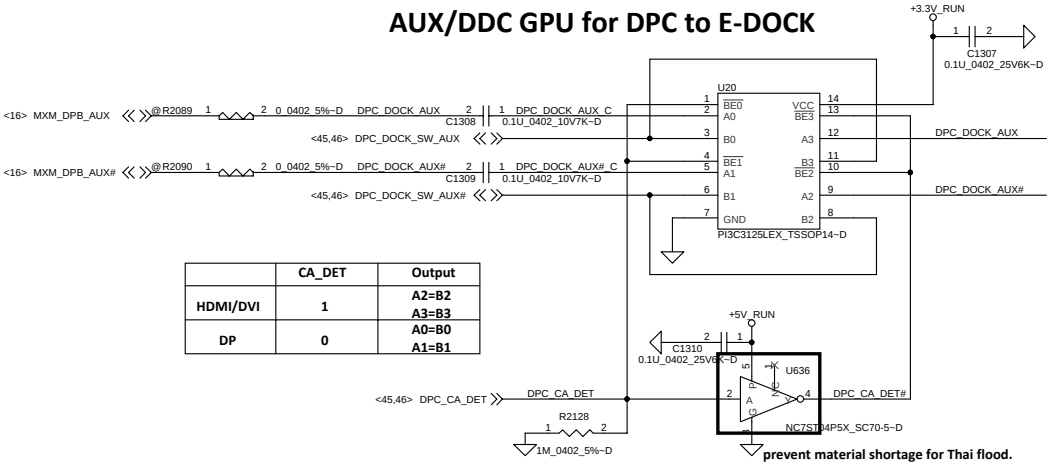
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	VGA	
Size	Document Number: LA-7931P	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 32 of 70	

AUX/DDC GPU for DPC to E-DOCK



	CA_DET	Output
HDMI/DVI	1	A2=B2 A3=B3
DP	0	A0=B0 A1=B1

prevent material shortage for Thai flood.

DELL CONFIDENTIAL/PROPRIETARY

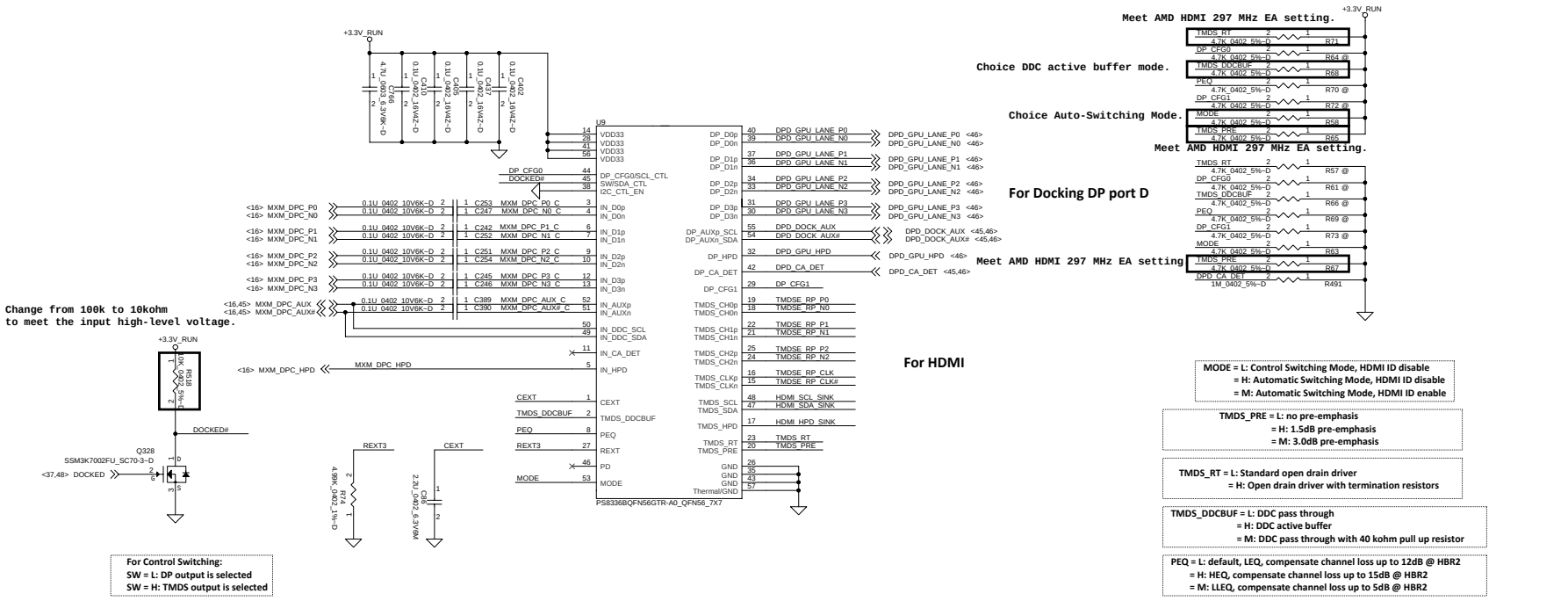
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

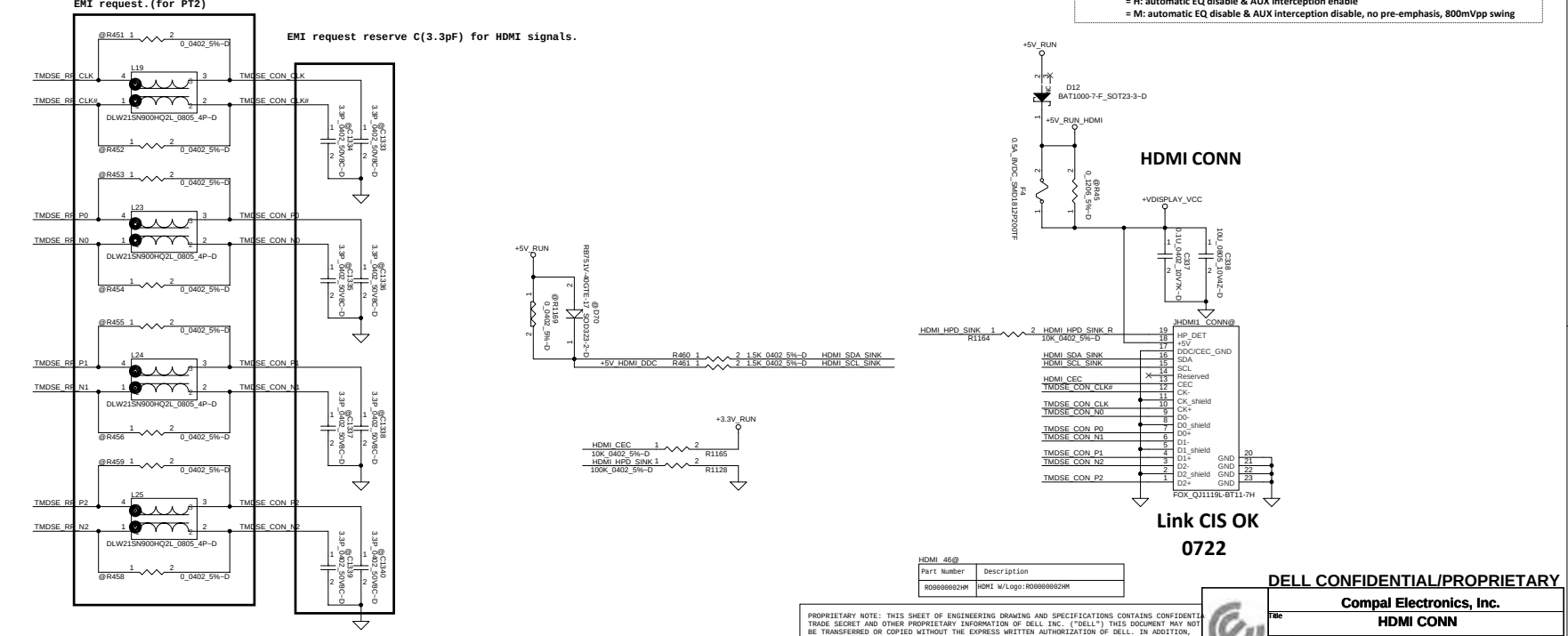
Compal Electronics, Inc.

Title: Docking DP/DMC MUX

Size | Document Number: LA-7931P | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 33 of 70



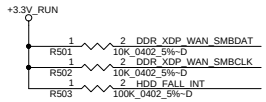


HDMI 46@	
Part Number	Description
R0000002HM	HDMI W/Logo:R0000002HM

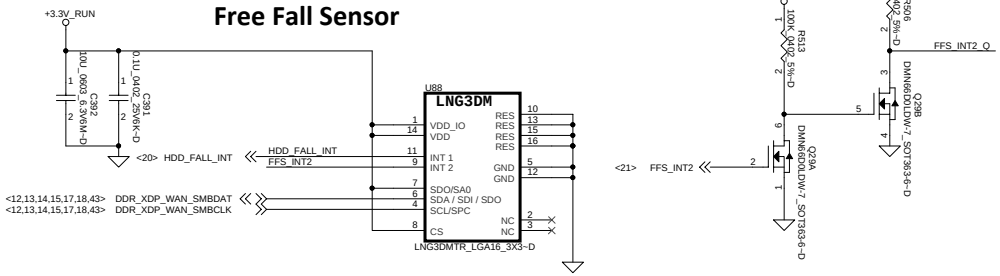
DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

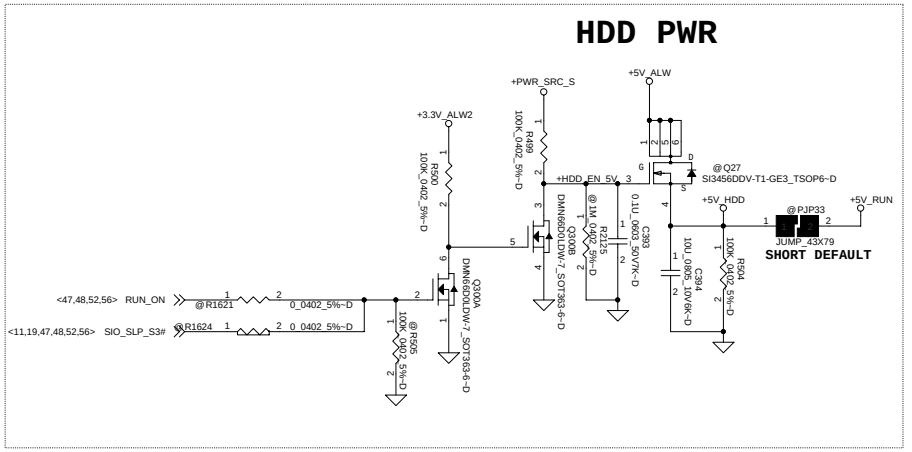
Compal Electronics, Inc.			
Title: HDMI CONN			
Size	Document Number: LA-7931P		Rev: 1.0
Date: Monday, July 23, 2012	Sheet 34 of 70		



Free Fall Sensor

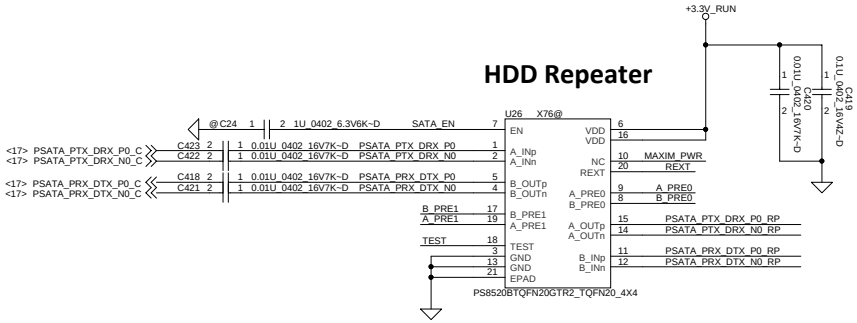


HDD PWR



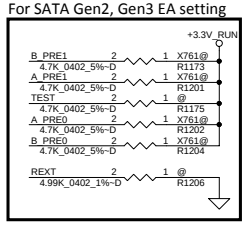
HDD Redriver Select Component		
	X76(Main) X7641231L01	X76(2nd) X7641231L02
	PARADE(Main) SA00004WF00	MAXIM(2nd) SA00002EY1L
U26	V	V
R1173	V	
R1201	V	
R1175		
R1202	V	
R1204	V	
R1206		
R2180		V
R2181		V
R2182		V
R2183		V
R2184		V

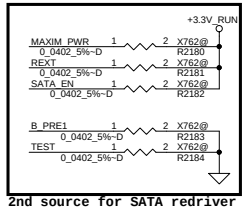
HDD Repeater



Main: SA00004WF00 (PS8520)
2nd: SA00002EY1L (MAX4951)

For SATA Gen2, Gen3 EA setting

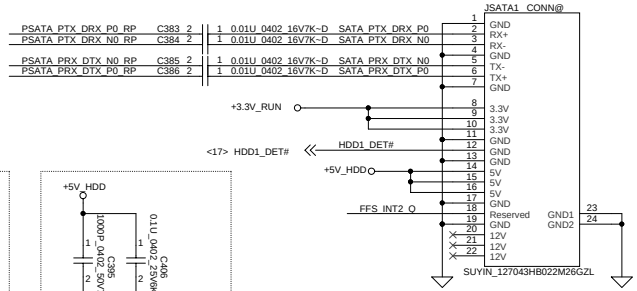




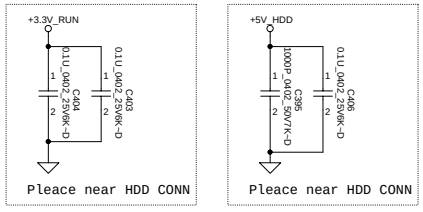
2nd source for SATA redriver

(Add X762@ for 2nd source option.)

For HDD Temp.



Link CIS OK



DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

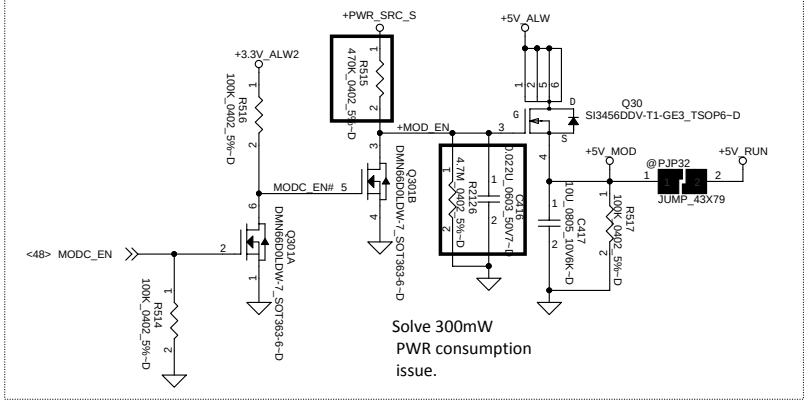
Compal Electronics, Inc.

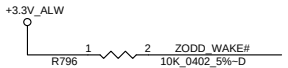
Title: HDD CONN

Size: | Document Number: LA-7931P | Rev: 1.0

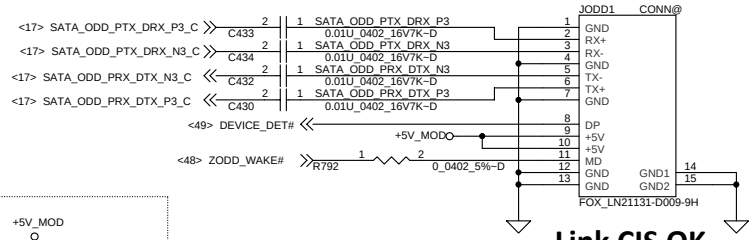
Date: Monday, July 23, 2012 | Sheet 35 of 70

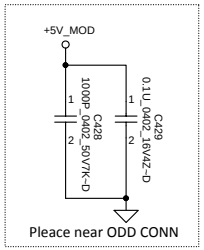
+5VMOD Source





ODD CONN



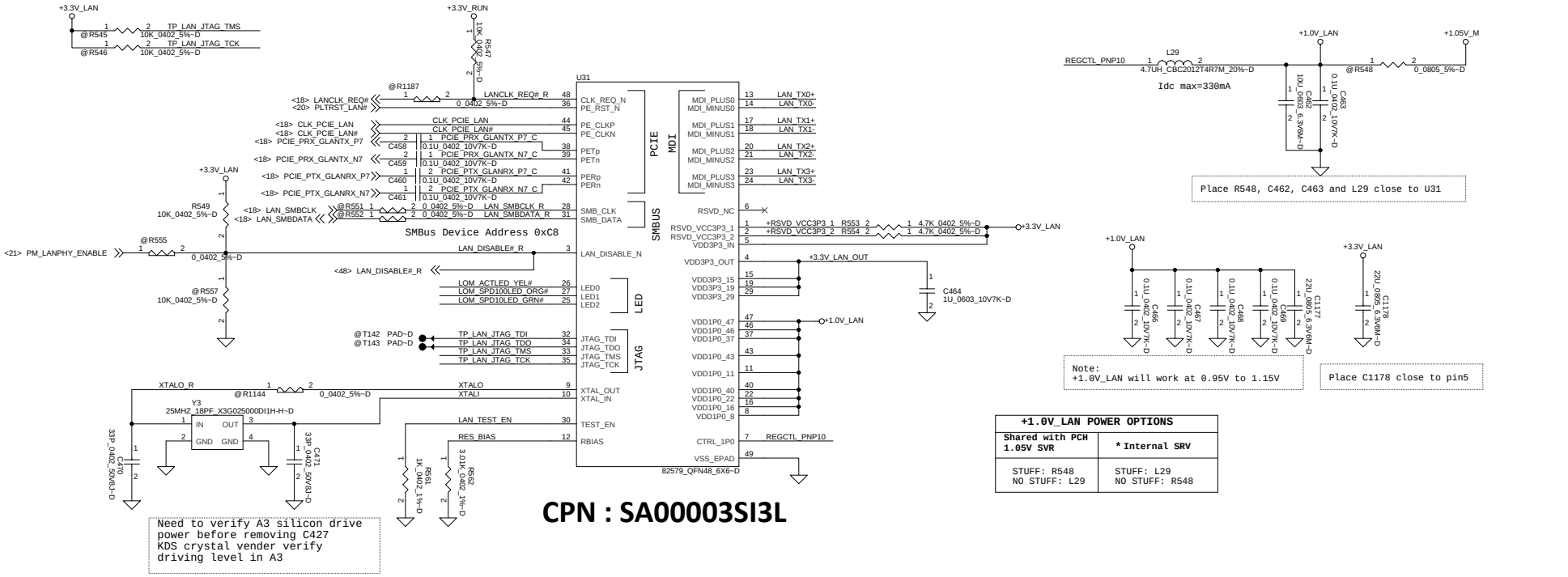


Link CIS OK
0722

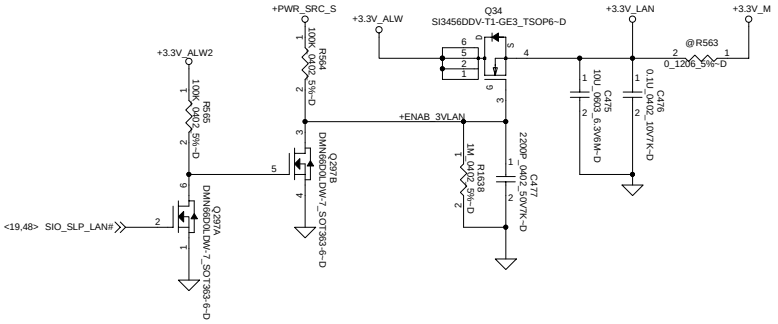
DELL CONFIDENTIAL/PROPRIETARY

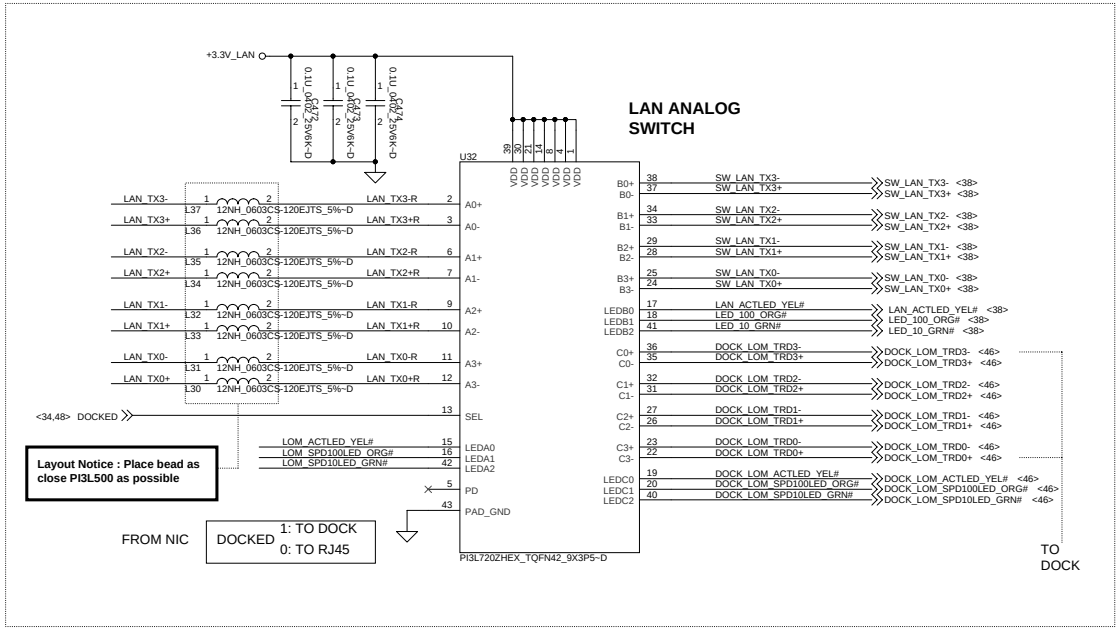
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTI
TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT
BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION,
NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIR
PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

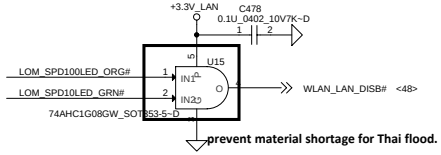
Compal Electronics, Inc.		
Title: ODD CONN		
Size	Document Number: LA-7931P	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 36 of 70	



+1.0V_LAN POWER OPTIONS	
Shared with PCH 1.05V SVR	*** Internal SRV**
STUFF: R548 NO STUFF: L29	STUFF: L29 NO STUFF: R548





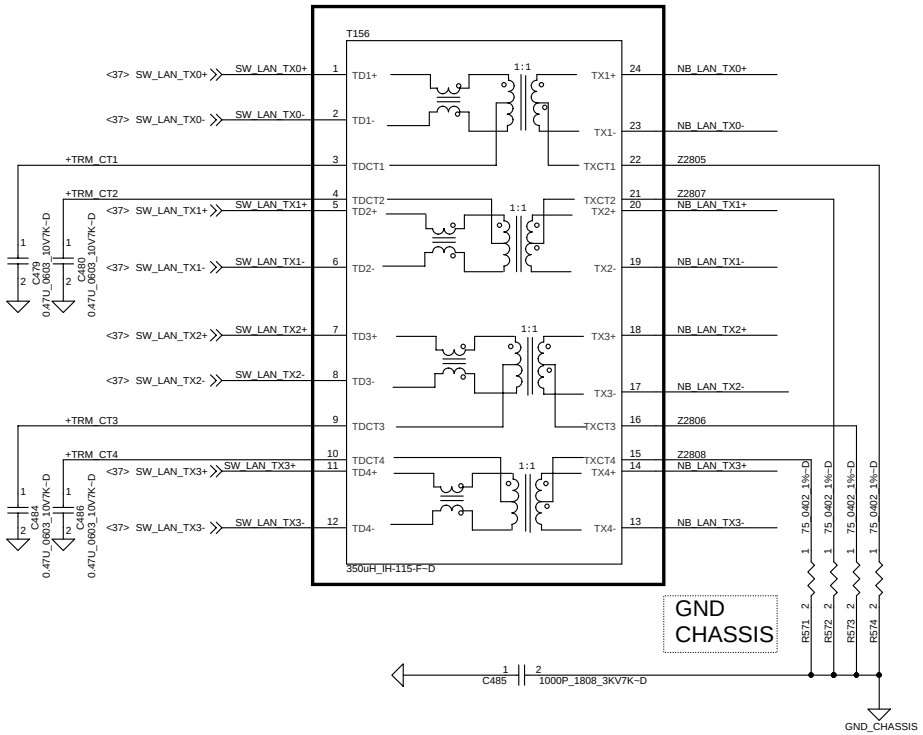


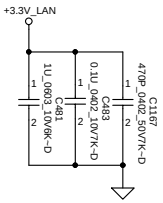
DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

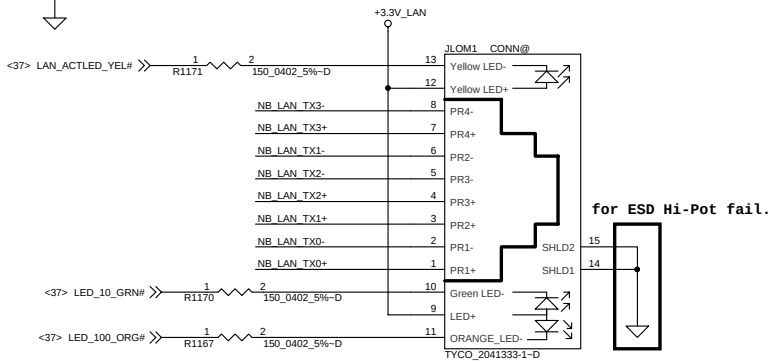
Compal Electronics, Inc.	
Title	LAN/LAN SW
Size	Document Number: LA-7931P
Rev	1.0
Date: Monday, July 23, 2012	Sheet 37 of 70

change to SP050006P0L for LAN EA.





+3.3V_LAN:20mils



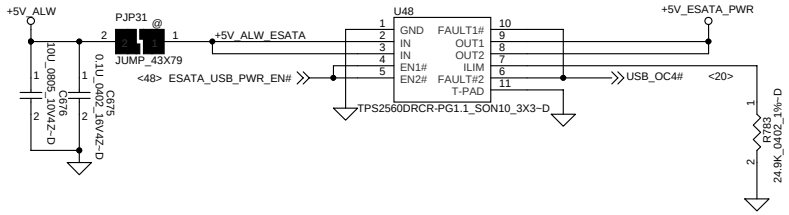
for ESD Hi-Pot fail.

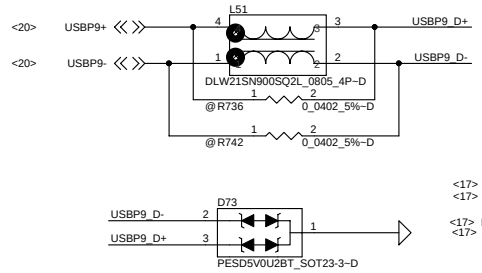
Link CIS OK
0722

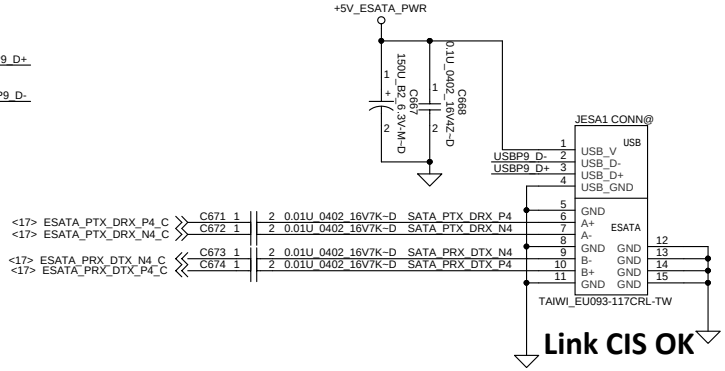
DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.		
Title: RJ45		
Size	Document Number: LA-7931P	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 38 of 70	







Link CIS OK
0722

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

	Compal Electronics, Inc.	
Title	ESATA	
Size	Document Number: LA-7931P	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 39 of 70	

For USB3 redriver 2nd source

Solve kingston issue.

Vender suggest for EA.

EQ : Equalizer control and program,
3.3V tolerant. Internally pulled down at ~150K ohm
[A_EQ1, A_EQ0] ==
LL: program EQ for channel loss up to 4.5dB
LH: program EQ for channel loss up to 7.5dB
HL: program EQ for channel loss up to 9.5dB
HH: program EQ for channel loss up to 13dB

DE : Programmable output pre-emphasis level setting,
3.3V tolerant. Internally pulled down at ~150K ohm
[A_DE1, A_DE0] ==
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 2.7dB de-emphasis
HH: 5dB de-emphasis

TEST : Chip test mode enable.
3.3V tolerant. Internally pulled down at ~150K ohm.
L: Normal operation (default)
H: Test mode enable
for compliance test, this pin should be pulled to high.

Pin 13 : B_EQ0 / SDA_CTL
Pin 14 : B_EQ1 / SCL_CTL
Pin 15 : B_DE0 / I2C_ADDR0
Pin 16 : B_DE1 / I2C_ADDR1
Pin28 : A_DE1 / NC
Pin29 : A_DE0 / NC
Pin31 : A_EQ1 / NC
Pin32 : A_EQ0 / NC

For USB3 redriver 2nd source

For USB3 redriver 2nd source

For USB3 redriver 2nd source

Vender suggest.

PS8720BTQFN32GTR-A0_TQFN32_3X6

PD# : chip power down, active LOW, 3.3V tolerant, internally pulled up at ~ 150K ohm.

HDD Redriver Select Component		
	X76(Main) X7641231L03	X76(2nd) X7641231L04
	PS8720B SA00004UI00	PS8720A SA00005PO00
U638	V	V
R2196	V	
R2197		V

change SILEGO to be main source

SLG55584AVTR_TDFN8_2X2

CB=0	autodetection charger identification active
CB=1	charging downstream port with active USB2.0 data communication mode with 1.5A support

CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

Reserve for samsung mobile issue.

For EMI request

EMI request.

ESD request change main source to SC300002F0L.

For ESD request

IP4292CZ10-TBR_XSON10_1.5X1~D

PESD5V0U2BT_SOT23-3~D

Follow conn list 0220A.

LOTES_AUSB0041-P001A

Link CIS OK

0305

NEC_TOKIN shortage issue for the flood in Tailand and small size for ME space.

For EMI request

EMI request.

ESD request change main source to SC300002F0L.

For ESD request

IP4292CZ10-TBR_XSON10_2.5X1~D

PESD5V0U2BT_SOT23-3~D

Follow conn list 0220A.

LOTES_AUSB0041-P001A

Link CIS OK

0305

NEC_TOKIN shortage issue for the flood in Tailand.

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL"). THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

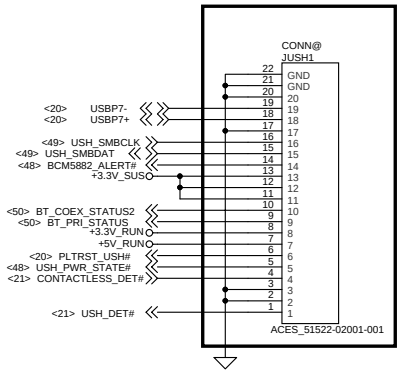
Compal Electronics, Inc.

Title: USB3.0

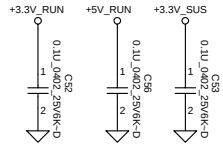
Size: Document Number: LA-7931P Rev: 1.0

Date: Monday, July 23, 2012 Sheet 40 of 70

0914: modify JUSH1 pin define for USH/B pin define change.

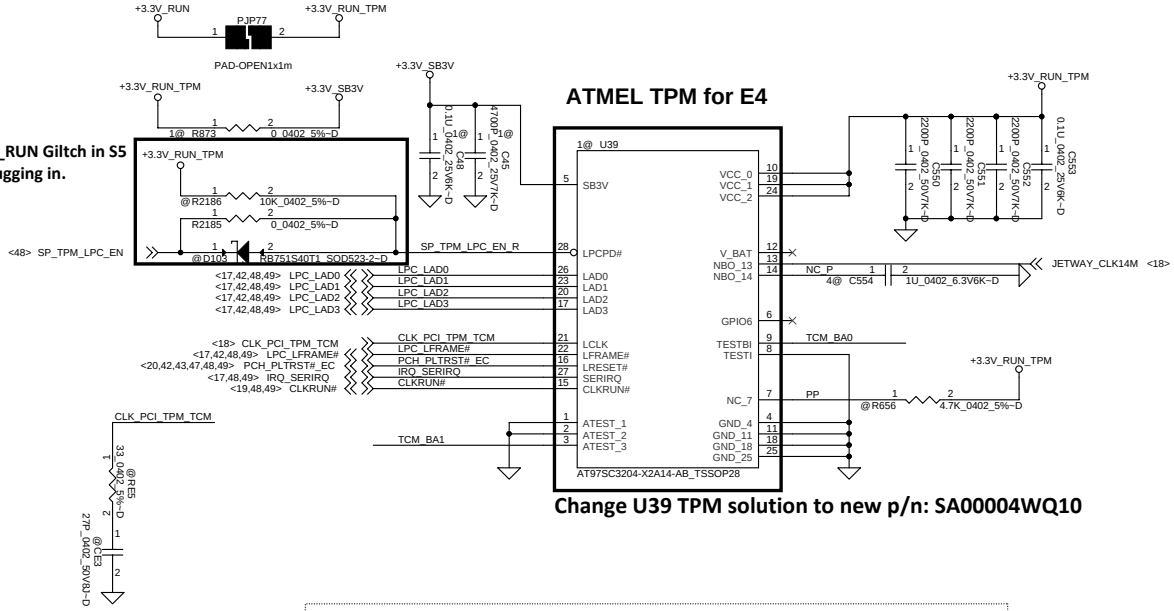


Link CIS OK
0722



Solve +3.3V_RUN Giltch in S5 when AC plugging in.

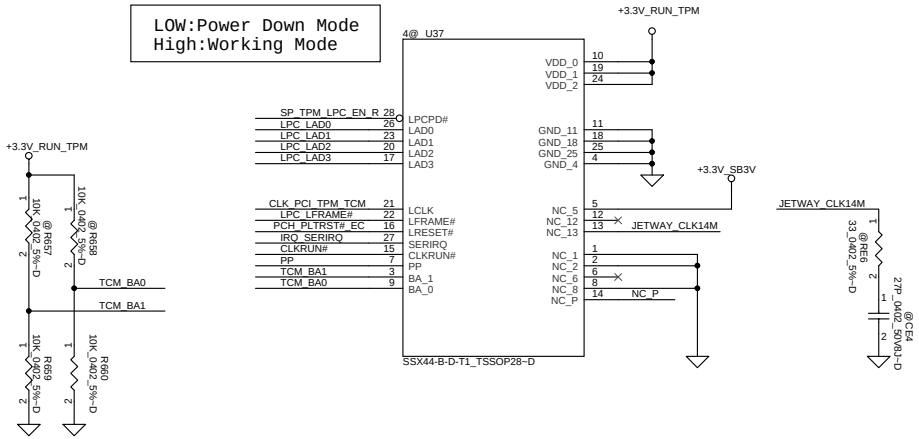
ATMEL TPM for E4



Change U39 TPM solution to new p/n: SA00004WQ10

Co-lay U37 and U39
LPC layout: Place TCM first and then end LPC with TPM.

China TCM: NationZ & Jetway co-lay

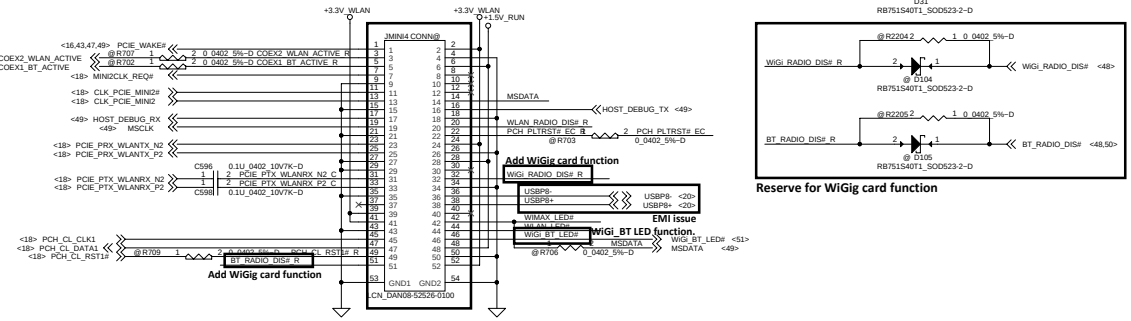


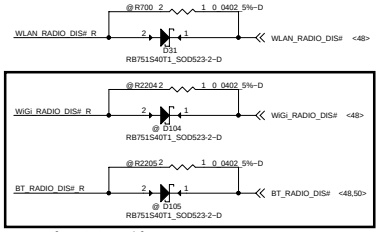
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: TPM/TCM		
Size	Document Number: LA-7931P	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 41 of 70	

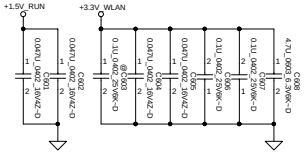
Mini WLAN/WIMAX/WiGig H=4

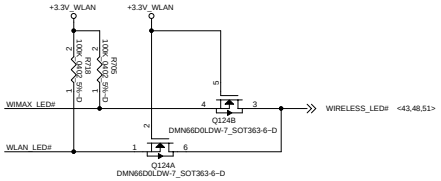


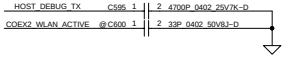


follow connecter list 1005: AAA-PCI-092-P01_A footprint
same as DAN08-52526-0100. next phase need change.

Link CIS OK_0722

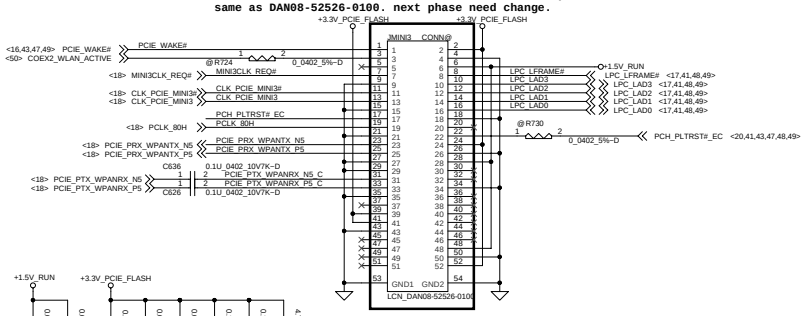






1/2 Minicard Pink Pather

follow connecter list 1005: AAA-PCI-092-P01_A footprint
same as DAN08-52526-0100. next phase need change.



Link CIS OK
0722

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

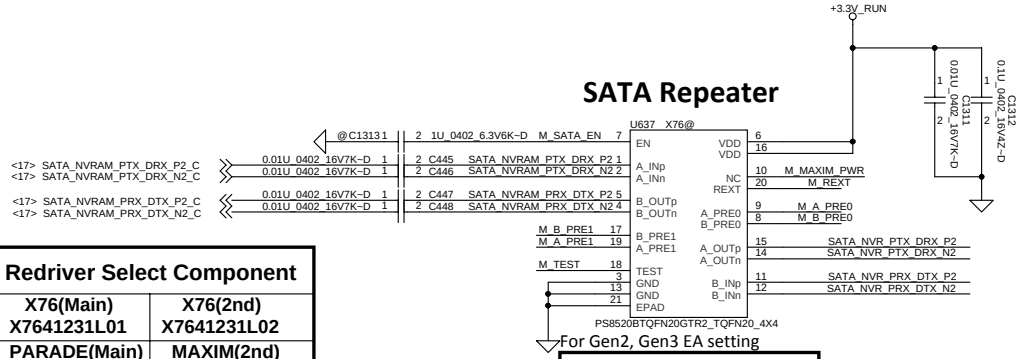
Compal Electronics, Inc.

Title	Mini Card-1/2	
Size	Document Number: LA-7931P	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 42 of 70	

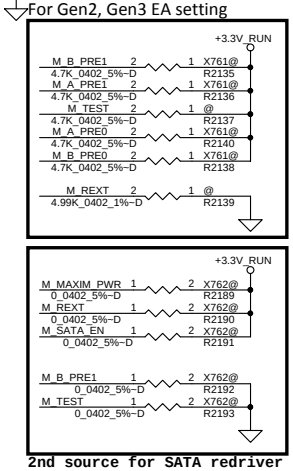
Mini WWAN/GPS/LTE/mSATA

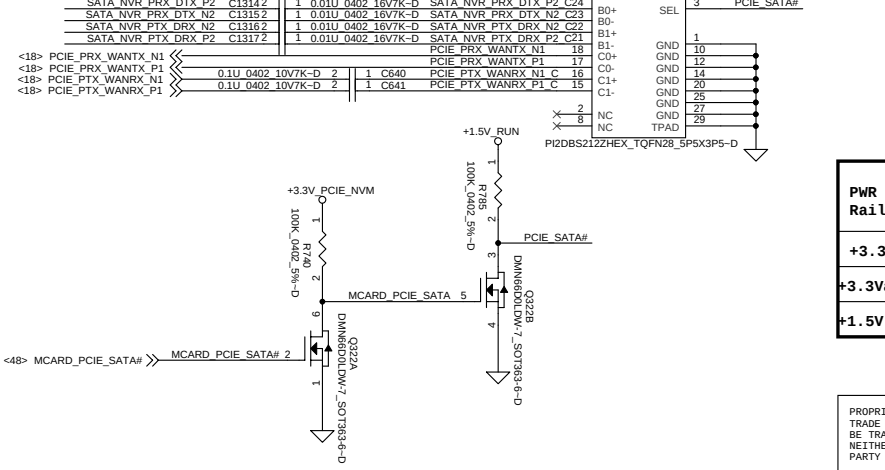
follow connecter list 1005: AAA-PCI-092-P01_A footprint
same as DAN08-52526-0100. next phase need change.

SATA Repeater



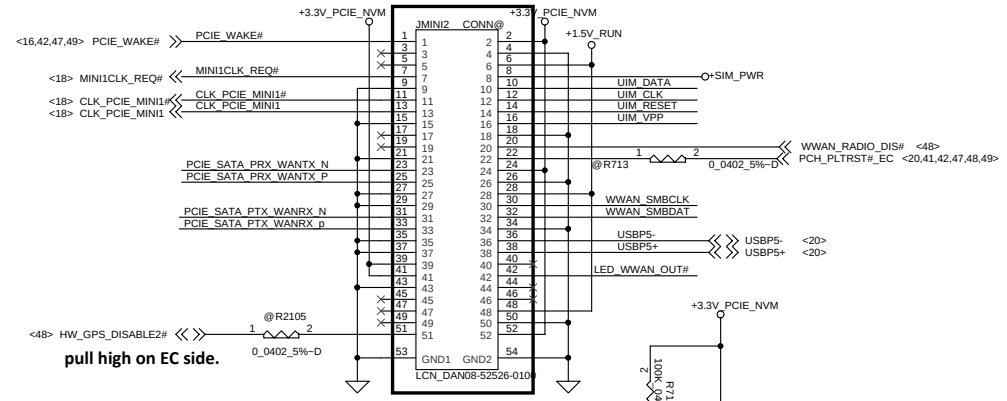
HDD Redriver Select Component		
	X76(Main) X7641231L01	X76(2nd) X7641231L02
	PARADE(Main) SA00004WF00	MAXIM(2nd) SA00002EY1L
U637	V	V
R2135	V	
R2136	V	
R2137		
R2140	V	
R2138	V	
R2139		
R2189		V
R2190		V
R2191		V
R2192		V
R2193		V



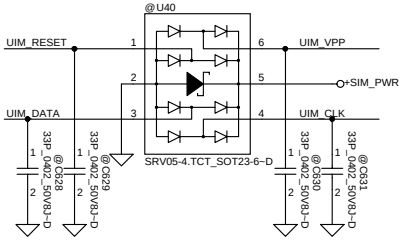


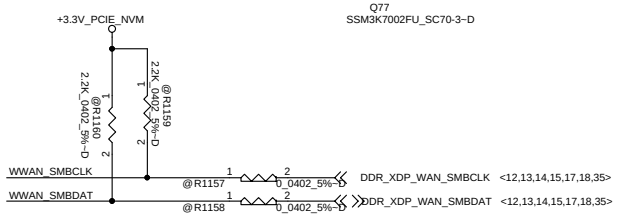
PIN	mSATA	WWAN
23	TX+	PERn0
25	TX-	PERp0
31	RX-	PETn0
33	RX+	PETp0

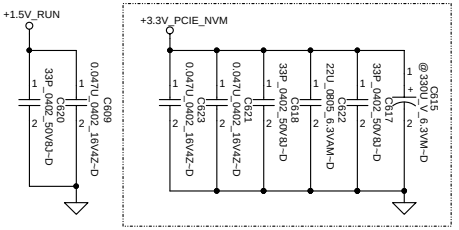
Function	SEL
Port A to Port B	L
Port A to Port C	H



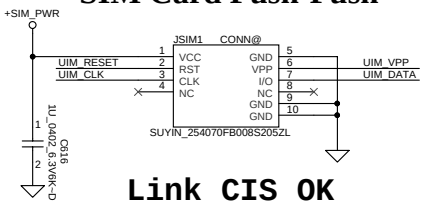
Link CIS OK
0722







SIM Card Push-Push



Link CIS OK
0722

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

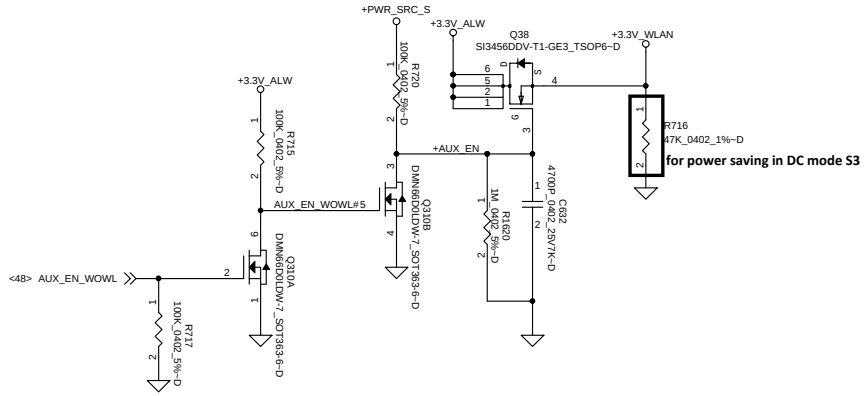
Compal Electronics, Inc.

Title: Mini Card-2/2

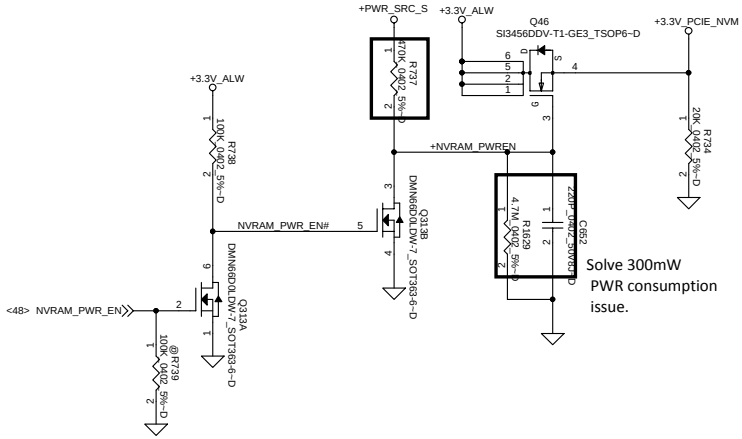
Size: | Document Number: LA-7931P | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 43 of 70

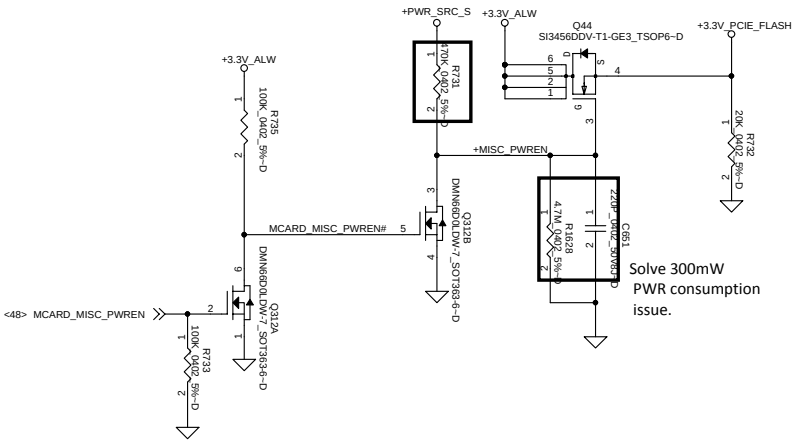
Power Control for Mini card1



Power Control for Mini card2



Power Control for Mini card3

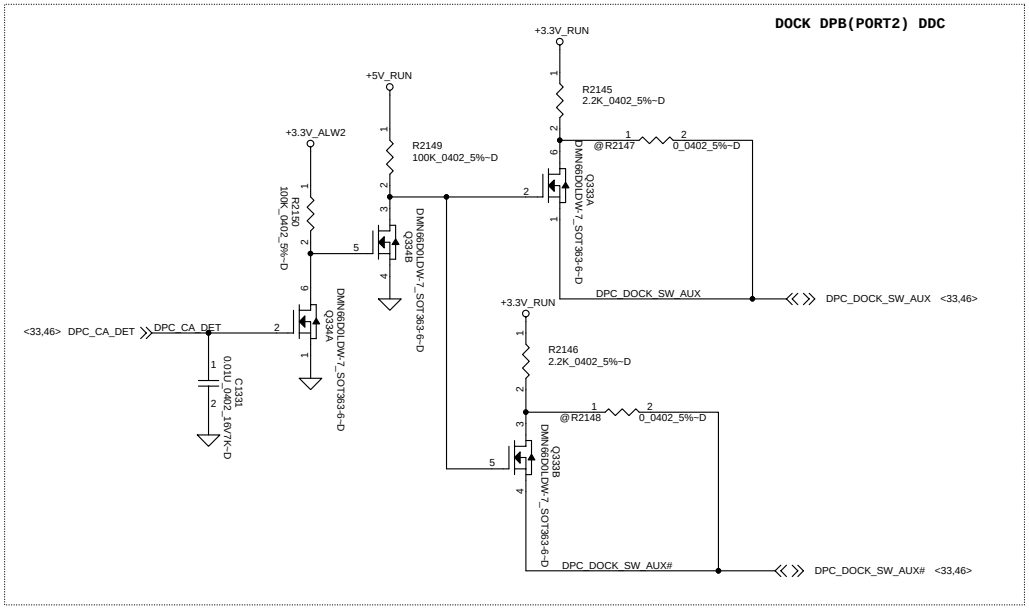


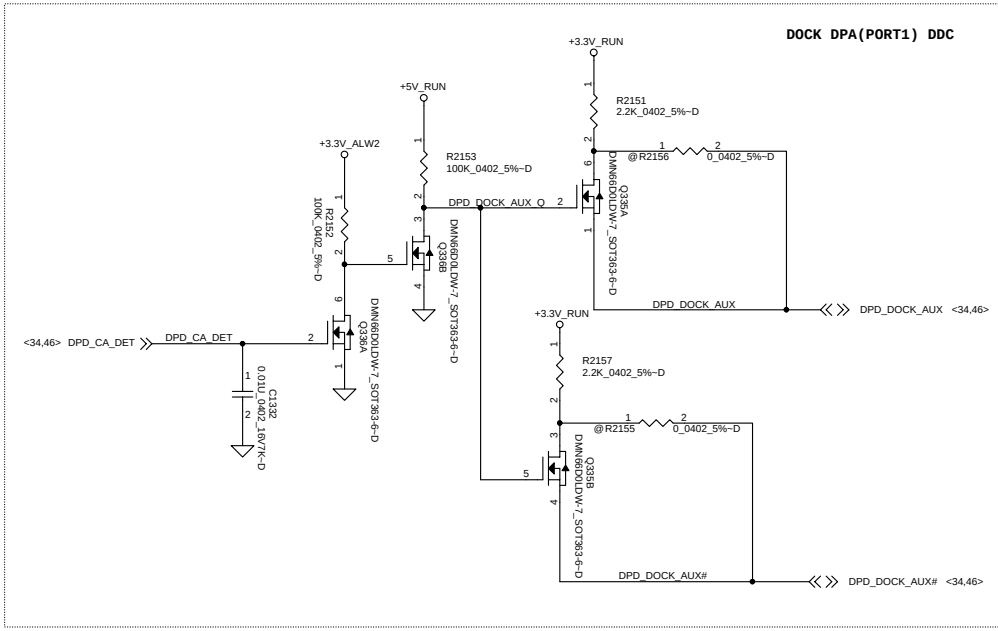
DELL CONFIDENTIAL/PROPRIETARY

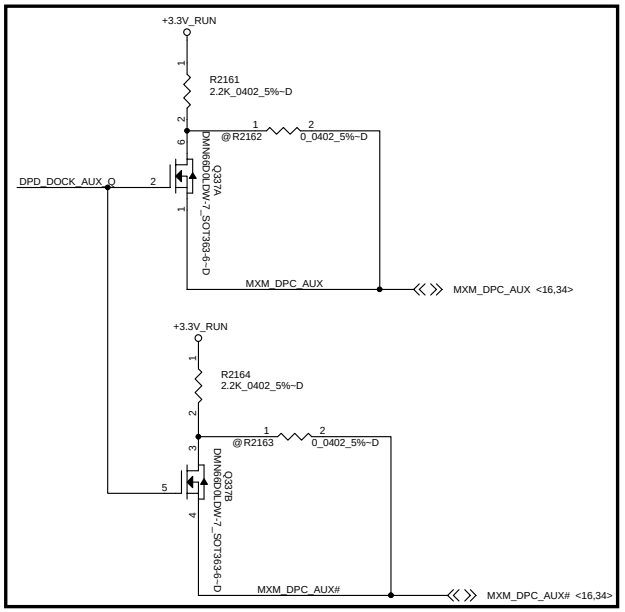
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

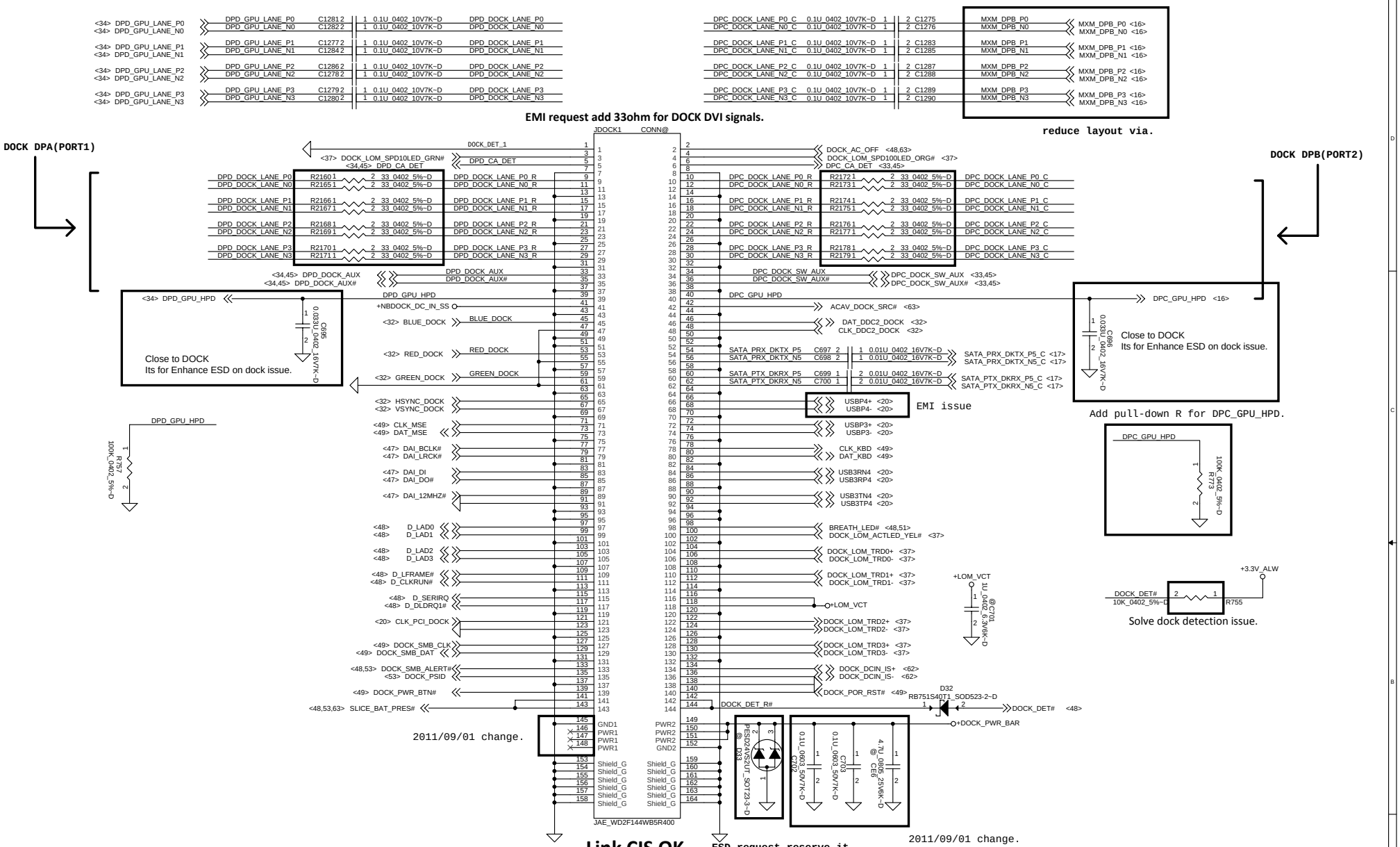
Title	Mini Card PWR	
Size	Document Number: LA-7931P	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 44 of 70	







Compal Electronics, Inc.		
Title: DOCK DP DDC SW		
Size	Document Number: LA-7931P	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 45 of 70	



DELL CONFIDENTIAL/PROPRIETARY

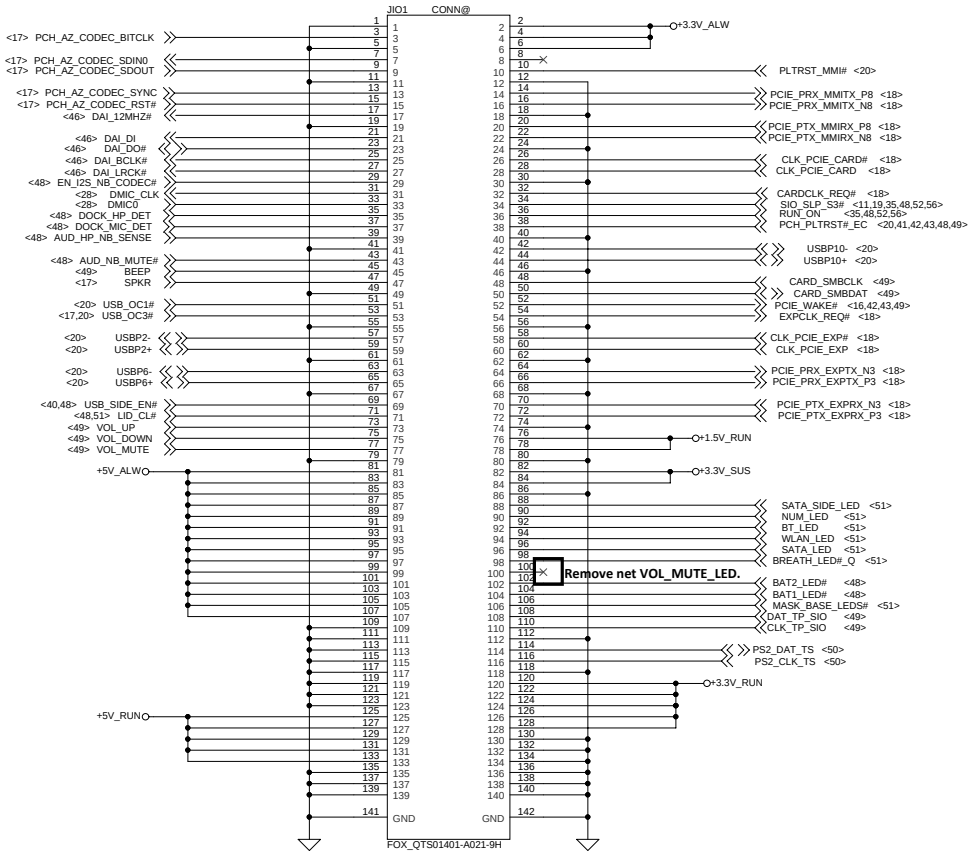
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

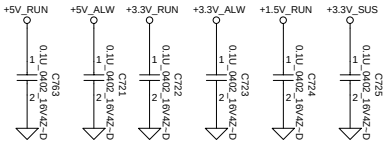
Title: Docking

Size: | Document Number: LA-7931P | Rev: 1.0

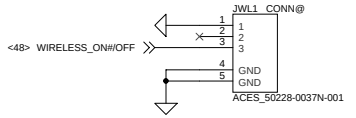
Date: Monday, July 23, 2012 | Sheet 46 of 70



Link CIS OK
0722

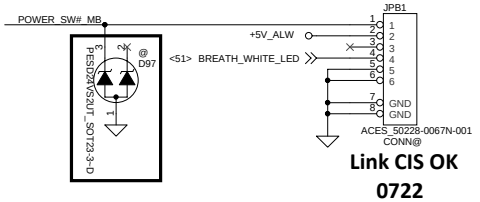


WireLess ON/OFF CONN



Link CIS OK_0722

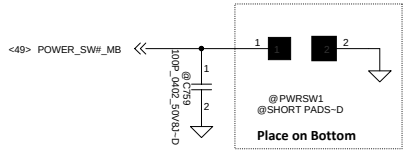
Power Bottom CONN



Link CIS OK
0722

ESD request reserve it.

Power Switch for debug

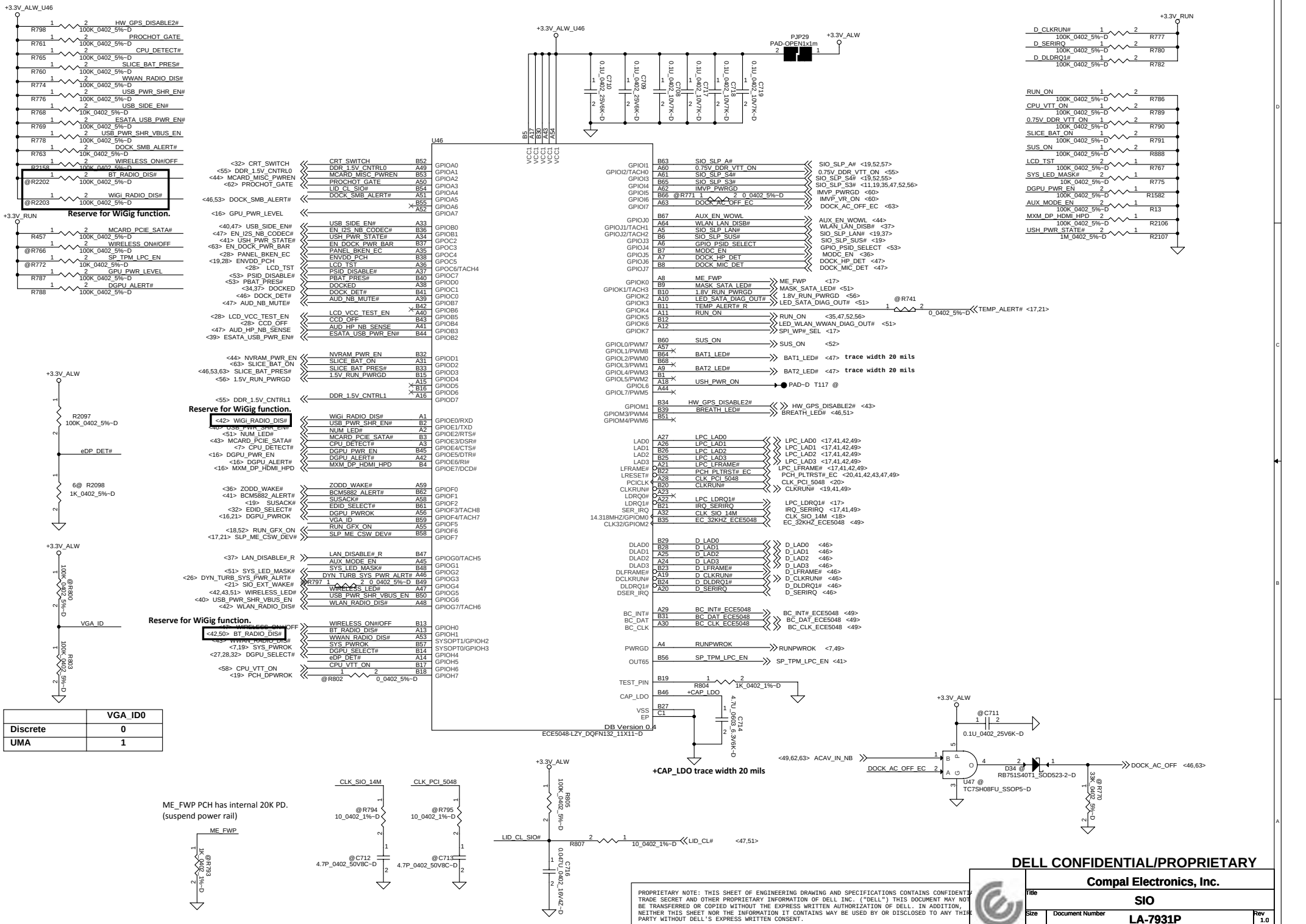


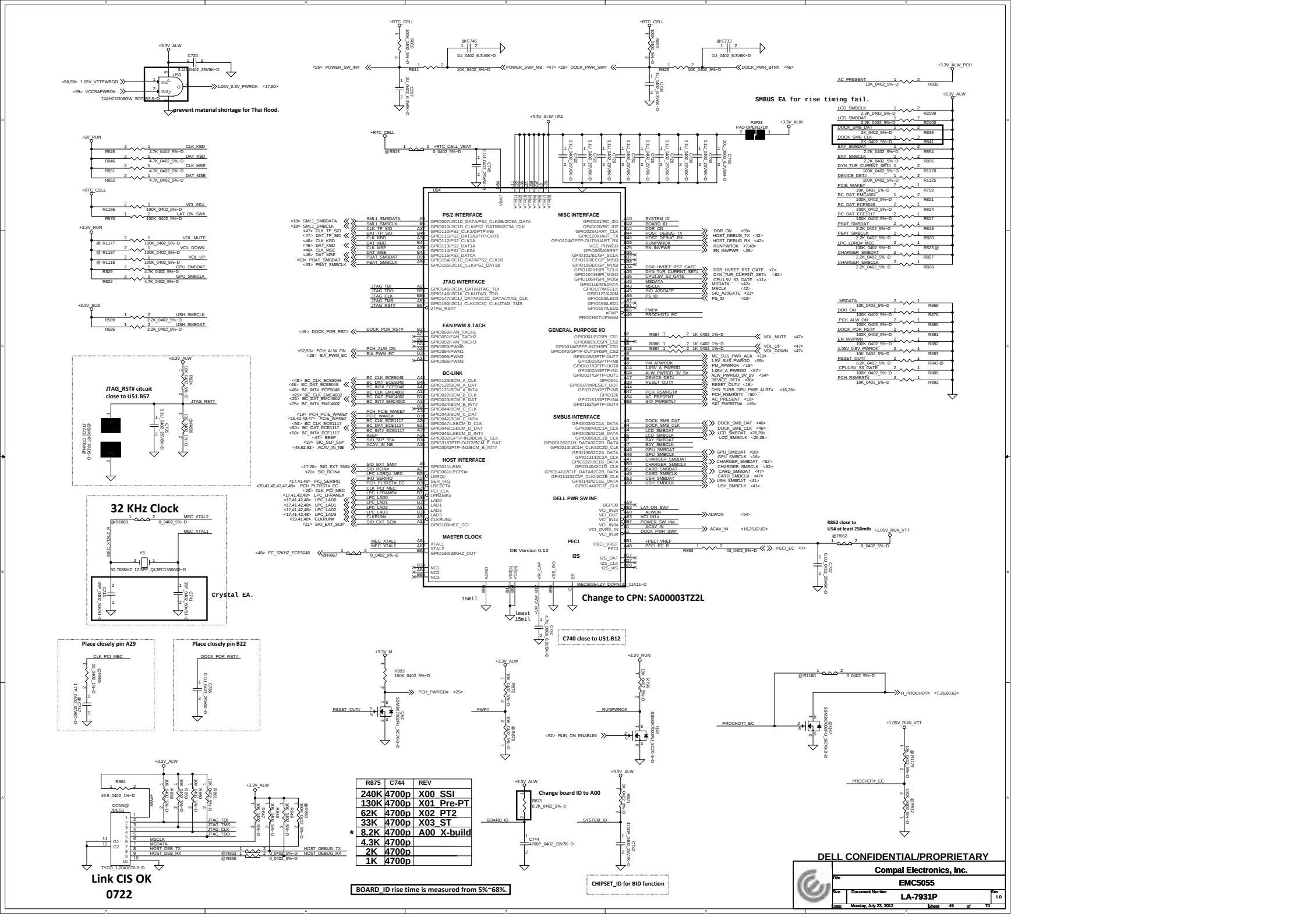
Place on Bottom

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

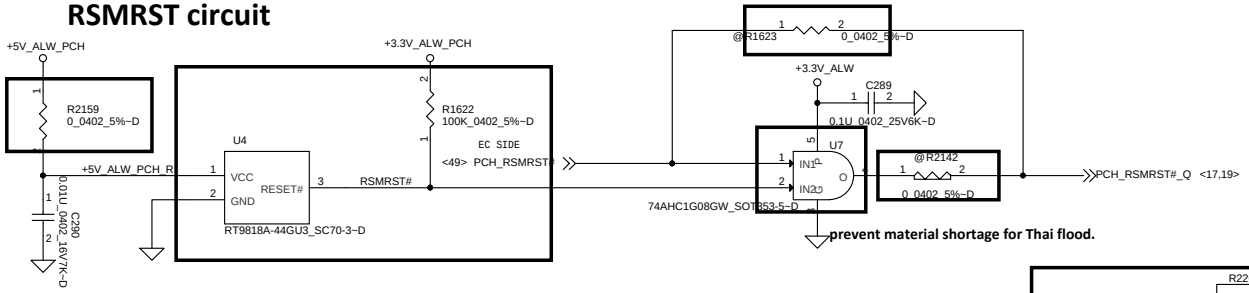
Compal Electronics, Inc.		
Title: I/O board		
Size	Document Number: LA-7931P	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 47 of 70	


+3.3V_ALW_U46
HW_GPS_DISABLE2# R798 100K_0402_5%~D
PROCHOT_GATE R761 100K_0402_5%~D
CPU_DETECT# R765 100K_0402_5%~D
SLICE_BAT_PRES# R760 100K_0402_5%~D
WWAN_RADIO_DIS# R774 100K_0402_5%~D
USB_PWR_SHR_EN# R776 100K_0402_5%~D
USB_SIDE_EN# R768 10K_0402_5%~D
ESATA_USB_PWR_EN# R769 100K_0402_5%~D
USB_PWR_SHR_VBUS_EN R778 100K_0402_5%~D
DOCK_SMB_ALERT# R763 10K_0402_5%~D
WIRELESS_ON#/OFF R2158 100K_0402_5%~D
BT_RADIO_DIS# @R2202 100K_0402_5%~D
WiGi_RADIO_DIS# @R2203 100K_0402_5%~D
Reserve for WiGig function.
+3.3V_RUN
MCARD_PCIE_SATA# R457 100K_0402_5%~D
WIRELESS_ON#/OFF @R766 100K_0402_5%~D
SP_TPM_LPC_EN @R772 10K_0402_5%~D
GPU_PWR_LEVEL R787 100K_0402_5%~D
DGPU_ALERT# R788 100K_0402_5%~D
+3.3V_ALW_U46
PJP29 PAD-OPEN1x1m
+3.3V_ALW
C710 0.1U_0402_25V6K~D
C709 0.1U_0402_25V6K~D
C708 0.1U_0402_10V7K~D
C717 0.1U_0402_10V7K~D
C718 0.1U_0402_10V7K~D
C719 0.1U_0402_10V7K~D
U46
ECE5048-LZY_DQFN132_11X11~D
DB Version 0.4
+3.3V_RUN
D_CLKRUN# R777
D_SERIRQ R780
D_DLDRQ1# R782
RUN_ON R786
CPU_VTT_ON R789
0.75V_DDR_VTT_ON R790
SLICE_BAT_ON R791
SUS_ON R888
LCD_TST R767
SYS_LED_MASK# R775
DGPU_PWR_EN R1582
AUX_MODE_EN R13
MXM_DP_HDMI_HPD R2106
USH_PWR_STATE# R2107
1M_0402_5%~D
100K_0402_5%~D
+3.3V_ALW
R2097 100K_0402_5%~D
eDP_DET#
6@ R2098 1K_0402_5%~D
+3.3V_ALW
100K_0402_5%~D @R2099
VGA_ID
100K_0402_5%~D R803
Reserve for WiGig function.
Reserve for WiGig function.
@R802 0_0402_5%~D
@R771 0_0402_5%~D
@R741 0_0402_5%~D
trace width 20 mils
trace width 20 mils
+CAP_LDO trace width 20 mils
R804 1K_0402_1%~D
4.7U_0603_6.3V6K~D C714
@C711 0.1U_0402_25V6K~D
D34 @ RB751S40T1_SOD523-2~D
U47 @ TC7SH08FU_SSOP5~D
3K_0402_5%~D @R770
ME_FWP PCH has internal 20K PD. (suspend power rail)
ME_FWP
1K_0402_1%~D @R793
CLK_SIO_14M
CLK_PCI_5048
@R794 10_0402_1%~D
@R795 10_0402_1%~D
@C712 4.7P_0402_50V8C~D
@C713 4.7P_0402_50V8C~D
R805 100K_0402_5%~D
R807 10_0402_1%~D
C716 0.047U_0402_16V4Z~D
VGA_ID0
Discrete 0
UMA 1
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Title SIO
Size Document Number LA-7931P Rev 1.0
Date: Monday, July 23, 2012 Sheet 48 of 70


+3.3V_ALW
C720
0.1U_0402_25V6K-D
U50
74AHC1G08GW_SOT353-5_D
<58,59> 1.05V_VTTPWRGD
<59> VCCSAPWROK
1.05V_0.8V_PWROK <17,60>
prevent material shortage for Thai flood.
+RTC_CELL
R810 100K_0402_5%-D
@C746
1U_0402_6.3V6K-D
<25> POWER_SW_IN#
R811 10K_0402_5%-D
POWER_SW#_MB <47> <25> DOCK_PWR_SW#
C757 1U_0402_6.3V6K-D
R825 10K_0402_5%-D
DOCK_PWR_BTN# <46>
@C733
1U_0402_6.3V6K-D
C753 1U_0402_6.3V6K-D
SMBUS EA for rise timing fail.
+3.3V_ALW_PCH
AC_PRESENT
10K_0402_5%-D
R835
+3.3V_ALW
LCD_SMBCLK 2.2K_0402_5%-D R2099
LCD_SMBDAT 2.2K_0402_5%-D R2100
DOCK_SMB_DAT 2K_0402_5%-D R838
DOCK_SMB_CLK 2K_0402_5%-D R841
BAY_SMBDAT 2.2K_0402_5%-D R854
BAY_SMBCLK 2.2K_0402_5%-D R856
DYN_TUR_CURRNT_SET# 100K_0402_5%-D R1178
DEVICE_DET# 100K_0402_5%-D R1125
PCIE_WAKE# 10K_0402_5%-D R759
BC_DAT_EMC4002 100K_0402_5%-D R821
BC_DAT_ECE5048 100K_0402_5%-D R814
BC_DAT_ECE1117 100K_0402_5%-D R817
PBAT_SMBDAT 2.2K_0402_5%-D R818
PBAT_SMBCLK 2.2K_0402_5%-D R820
LPC_LDRQ# MEC 100K_0402_5%-D R823@
CHARGER_SMBDAT 2.2K_0402_5%-D R827
CHARGER_SMBCLK 2.2K_0402_5%-D R828
+5V_RUN
CLK_KBD 4.7K_0402_5%-D R845
DAT_KBD 4.7K_0402_5%-D R846
CLK_MSE 4.7K_0402_5%-D R851
DAT_MSE 4.7K_0402_5%-D R852
+RTC_CELL
VCI_IN1# 100K_0402_5%-D R1156
LAT_ON_SW# 100K_0402_5%-D R870
+3.3V_RUN
VOL_MUTE 100K_0402_5%-D @ R1177
VOL_DOWN 100K_0402_5%-D @ R1197
VOL_UP 100K_0402_5%-D @ R1118
GPU_SMBDAT 4.7K_0402_5%-D R829
GPU_SMBCLK 4.7K_0402_5%-D R822
+3.3V_SUS
USH_SMBCLK 2.2K_0402_5%-D R589
USH_SMBDAT 2.2K_0402_5%-D R585
+3.3V_ALW_U54
PJP28 PAD-OPEN1x1m
+3.3V_ALW
+RTC_CELL
@R815 1 2 +RTC_CELL_VBAT 0_0402_5%-D
C746 1U_0402_25V6K-D
U54
VBAT
PS/2 INTERFACE
GPIO007/I2C1D_DATA/PS2_CLK0B/I2C3A_DATA
GPIO010/I2C1D_CLK/PS2_DAT0B/I2C3A_CLK
GPIO110/PS2_CLK2/GPTP-IN6
GPIO111/PS2_DAT2/GPTP-OUT6
GPIO112/PS2_CLK1A
GPIO113/PS2_DAT1A
GPIO114/PS2_CLK0A
GPIO115/PS2_DAT0A
GPIO154/I2C1C_DATA/PS2_CLK1B
GPIO155/I2C1C_CLK/PS2_DAT1B
JTAG INTERFACE
GPIO145/I2C1K_DATA/JTAG_TDI
GPIO146/I2C1K_CLK/JTAG_TDO
GPIO147/I2C1J_DATA/I2C2C_DATA/JTAG_CLK
GPIO150/I2C1J_CLK/I2C2C_CLK/JTAG_TMS
JTAG_RST#
FAN PWM & TACH
GPIO050/FAN_TACH1
GPIO051/FAN_TACH2
GPIO052/FAN_TACH3
GPIO053/PWM0
GPIO054/PWM1
GPIO055/PWM2
GPIO056/PWM3
BC-LINK
GPIO123/BCM_A_CLK
GPIO122/BCM_A_DAT
GPIO121/BCM_A_INT#
GPIO022/BCM_B_CLK
GPIO023/BCM_B_DAT
GPIO024/BCM_B_INT#
GPIO044/BCM_C_CLK
GPIO043/BCM_C_DAT
GPIO042/BCM_C_INT#
GPIO047/LSBCM_D_CLK
GPIO046/LSBCM_D_DAT
GPIO045/LSBCM_D_INT#
GPIO032/GPTP-IN3/BCM_E_CLK
GPIO031/GPTP-OUT2/BCM_E_DAT
GPIO030/GPTP-IN2/BCM_E_INT#
HOST INTERFACE
GPIO011/nSMI
GPIO061/LPCPD#
LDRQ#
SER_IRQ
LRESET#
PCI_CLK
LFRAME#
LAD0
LAD1
LAD2
LAD3
CLKRUN#
GPIO100/nEC_SCI
MASTER CLOCK
XTAL1
XTAL2
GPIO160/32KHZ_OUT
NC1
NC2
NC3
DB Version 0.12
MISC INTERFACE
GPIO021/RC_ID1
GPIO020/RC_ID2
GPIO025/UART_CLK
GPIO120/UART_TX
GPIO124/GPTP-OUT5/UART_RX
VCC_PRWGD
GPIO060/KBRST
GPIO101/ECGP_SCLK
GPIO103/ECGP_MISO
GPIO105/ECGP_MOSI
GPIO102/HSPI_SCLK
GPIO104/HSPI_MISO
GPIO106/HSPI_MOSI
GPIO116/MSDATA
GPIO117/MSCLK
GPIO127/A20M
GPIO153/LED3
GPIO156/LED1
GPIO157/LED2
nFWP
PROCHOT#/PWM4
SYSTEM_ID
BOARD_ID
DDR_ON <55>
HOST_DEBUG_TX <42>
HOST_DEBUG_RX <42>
RUNPWROK <7,48>
EN_INVPWR <28>
DDR_HVREF_RST_GATE <7>
DYN_TUR_CURRNT_SET# <62>
CPU1.5V_S3_GATE <11>
MSDATA <42>
MSCLK <42>
SIO_A20GATE <21>
PS_ID <53>
FWP#
PROCHOT# EC
GENERAL PURPOSE I/O
GPIO001/ECSPI_CS1
GPIO002/ECSPI_CS2
GPIO014/GPTP-IN7/HSPI_CS1
GPIO040/GPTP-OUT3/HSPI_CS2
GPIO015/GPTP-OUT7
GPIO016/GPTP-IN8
GPIO017/GPTP-OUT8
GPIO026/GPTP-IN1
GPIO027/GPTP-OUT1
GPIO041
GPIO107/nRESET_OUT
GPIO125/GPTP-IN5
GPIO126
GPIO151/GPTP-IN4
GPIO152/GPTP-OUT4
R884 1 2 1K_0402_1%-D VOL_MUTE <47>
R886 1 2 1K_0402_1%-D VOL_UP <47>
R887 1 2 1K_0402_1%-D VOL_DOWN <47>
ME_SUS_PWR_ACK <19>
1.5V_SUS_PWRGD <55>
PM_APWROK <19>
1.05V_A_PWRGD <57>
ALW_PWRGD_3V_5V <54>
DEVICE_DET# <36>
RESET_OUT# <19>
DYN_TURB_GPU_PWR_ALRT# <16,26>
PCH_RSMRST# <50>
AC_PRESENT <19>
SIO_PWRBTN# <19>
SMBUS INTERFACE
GPIO003/I2C1A_DATA
GPIO004/I2C1A_CLK
GPIO005/I2C1B_DATA
GPIO006/I2C1B_CLK
GPIO012/I2C1H_DATA/I2C2D_DATA
GPIO013/I2C1H_CLK/I2C2D_CLK
GPIO130/I2C2A_DATA
GPIO131/I2C2A_CLK
GPIO132/I2C1G_DATA
GPIO140/I2C1G_CLK
GPIO141/I2C1F_DATA/I2C2B_DATA
GPIO142/I2C1F_CLK/I2C2B_CLK
GPIO143/I2C1E_DATA
GPIO144/I2C1E_CLK
DOCK_SMB_DAT <46>
DOCK_SMB_CLK <46>
LCD_SMBDAT <26,28>
LCD_SMBCLK <26,28>
BAY_SMBCLK
BAY_SMBDAT
GPU_SMBDAT <16>
GPU_SMBCLK <16>
CHARGER_SMBDAT <62>
CHARGER_SMBCLK <62>
CARD_SMBDAT <47>
CARD_SMBCLK <47>
USH_SMBDAT <41>
USH_SMBCLK <41>
DELL PWR SW INF
BGPO0
VCI_IN2#
VCI_OUT
VCI_IN1#
VCI_IN0#
VCI_OVRD_IN
VCI_IN3#
LAT_ON_SW#
ALWON <54>
VCI_IN1#
POWER_SW_IN#
ACAV_IN <16,25,62,63>
DOCK_PWR_SW#
PECI
PECI_VREF
PECI
+PECI_VREF
PECI_EC_R
R863 43_0402_5%-D
PECI_EC <7>
I2S
I2S_DAT
I2S_CLK
I2S_WS
JTAG_RST# citcuit close to U51.B57
JTAG_RST#
32 KHz Clock
@R1068 0_0402_5%-D
MEC_XTAL2
MEC_XTAL1
Y6
32.768KHZ_12.5PF_Q13FC1350000-D
Crystal EA.
<48> EC_32KHZ_ECE5048
@R867 0_0402_5%-D
Change to CPN: SA00003TZ2L
15mil
least 15mil
+VR_CAP
C740 4.7U_0603_6.3V6K-D
C740 close to U51.B12
R862 close to U54 at least 250mils
+1.05V_RUN_VTT
@R862 0_0402_5%-D
C737 0.1U_0402_25V6K-D
Place closely pin A29
CLK_PCI_MEC
4.7P_0402_50V8C-D
Place closely pin B22
DOCK_POR_RST#
0.1U_0402_25V6K-D
+3.3V_M
R893 100K_0402_5%-D
PCH_PWRGD# <25>
RESET_OUT#
Q25 SSM3K7002F_SC70-3-D
+3.3V_ALW
R8021 10K_0402_5%-D
FWP#
Q26 SSM3K7002F_SC70-3-D
+3.3V_RUN
R799 10K_0402_5%-D
RUNPWROK
Q27 SSM3K7002F_SC70-3-D
<52> RUN_ON_ENABLE#
@R1180 0_0402_5%-D
H_PROCHOT# <7,26,60,62>
PROCHOT# EC
Q37 SSM3K7002F_SC70-3-D
+1.05V_RUN_VTT
R8119 100_0402_1%-D
PROCHOT# EC
R8022 100K_0402_5%-D
+3.3V_ALW
R864 49.9_0402_1%-D
R865 10K_0402_5%-D
R866 10K_0402_5%-D
R867 10K_0402_5%-D
R868 10K_0402_5%-D
R869 10K_0402_5%-D
R870 10K_0402_5%-D
R871 10K_0402_5%-D
R872 10K_0402_5%-D
R873 10K_0402_5%-D
CONN@ JDEG1
JTAG_TDI
JTAG_TMS
JTAG_CLK
JTAG_TDO
MSCLK
MSDATA
HOST_DEB_TX
HOST_DEB_RX
TYCO_1-2041070-0-D
Link CIS OK
0722
@R853 1 2 0_0402_5%-D HOST_DEBUG_TX
@R855 1 2 0_0402_5%-D HOST_DEBUG_RX
R875 | C744 | REV
240K | 4700p | X00 SSI
130K | 4700p | X01 Pre-PT
62K | 4700p | X02 PT2
33K | 4700p | X03 ST
★ 8.2K | 4700p | A00 X-build
4.3K | 4700p
2K | 4700p
1K | 4700p
BOARD_ID rise time is measured from 5%~68%.
+3.3V_ALW
Change board ID to A00
R875 8.2K_0402_5%-D
BOARD_ID
C744 4700P_0402_25V7K-D
SYSTEM_ID
R8071 1K_0402_1%-D
C752 4700P_0402_25V7K-D
CHIPSET_ID for BID function
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Title EMC5055
Size Document Number LA-7931P Rev 1.0
Date: Monday, July 23, 2012 Sheet 49 of 70

RSMRST circuit

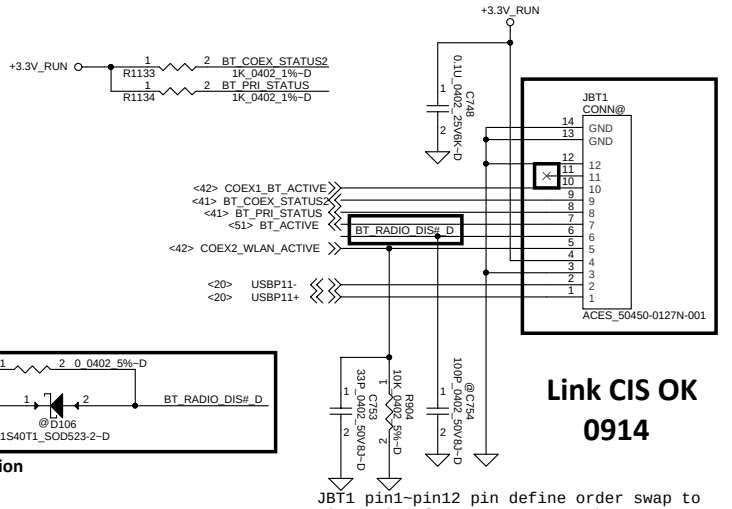
For meet T235(power off)= min 40ns(SPEC).T08a(power on)= max 90ms.

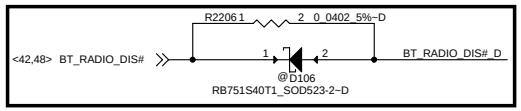


prevent material shortage for Thai flood.

BlueTooth

JBT1 pin11 Need confirm with Dell to add BT_DET or not.



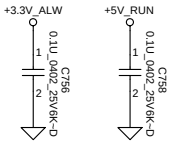


Reserve for WiGig card function

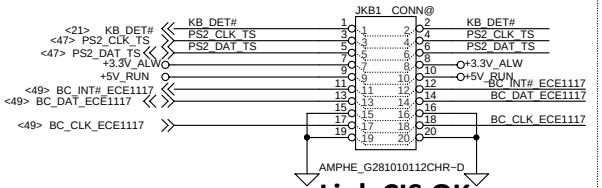
Link CIS OK
0914

JBT1 pin1~pin12 pin define order swap to pin12~pin1 for BT connector change to ACES_50450-0127N-001.
(because footprint different from ACES_50228-0127N_001)

Keyboard



Place close to JKB1



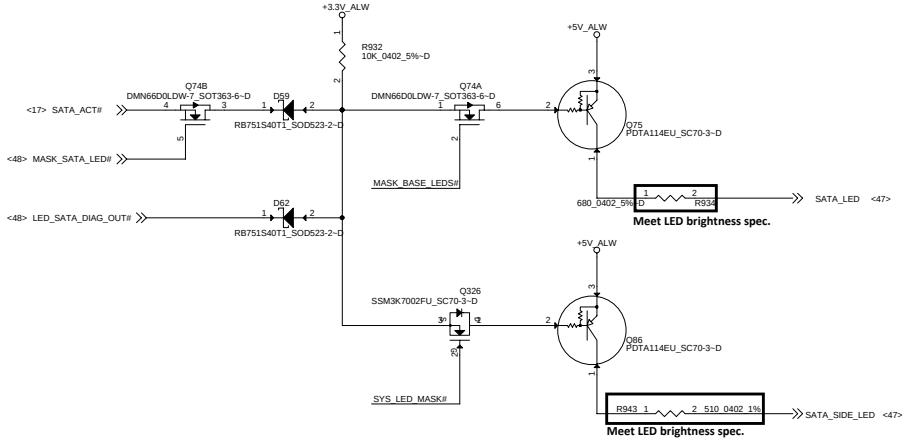
Link CIS OK
0722

DELL CONFIDENTIAL/PROPRIETARY

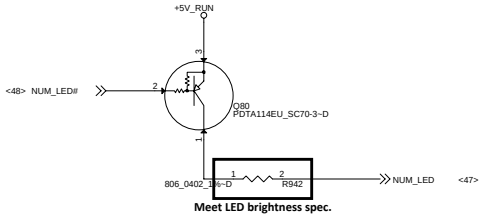
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTI
TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT
BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION,
NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIR
PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.	
Title	Touch PAD/Int KB
Size	Document Number: LA-7931P
Rev	1.0
Date: Monday, July 23, 2012	Sheet 50 of 70

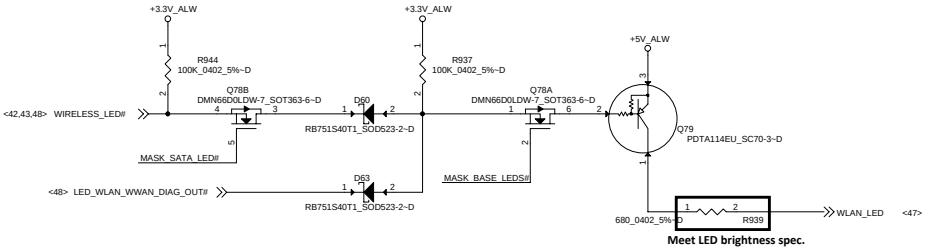
HDD LED



NUM LED



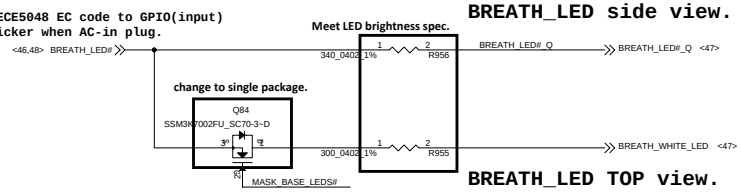
WWAN/WLAN LED



Breath LED

Change B39 of ECE5048 EC code to GPIO(input)
Solving LED flicker when AC-in plug.

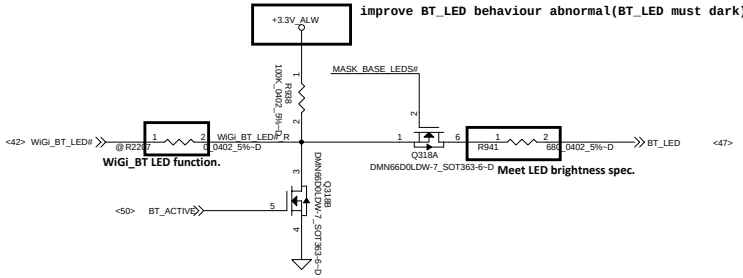
BREATH_LED side view.



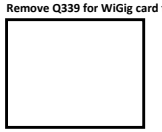
BREATH_LED TOP view.

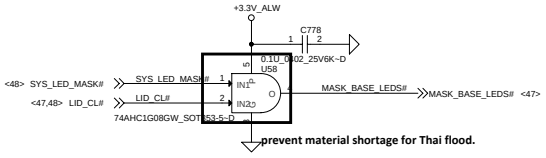
BT LED

improve BT_LED behaviour abnormal(BT_LED must dark) in S3/S4/S5.



Remove Q339 for WiGig card function usage.





LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

for Hi-POT issue.

@H1 H_2P8 @H4 H_2P8 @H5 H_3P2x6P2N @H6 H_2P8 @H7 H_3P8 @H8 H_3P3 @H9 H_3P3 @H10 H_3P3 @H11 H_3P3 @H12 H_2P3 @H13 H_3P2 @H14 H_2P8 @H15 H_2P8 @H16 H_3P8 @H17 H_2P8 @H18 H_4P1 @H19 H_4P1 @H20 H_2P8 @H21 H_4P1x2P1

@H22 H_2P8 @H23 H_4P1 @H24 H_4P1 @H25 H_2P8 @H26 H_2P8 @H27 H_2P3

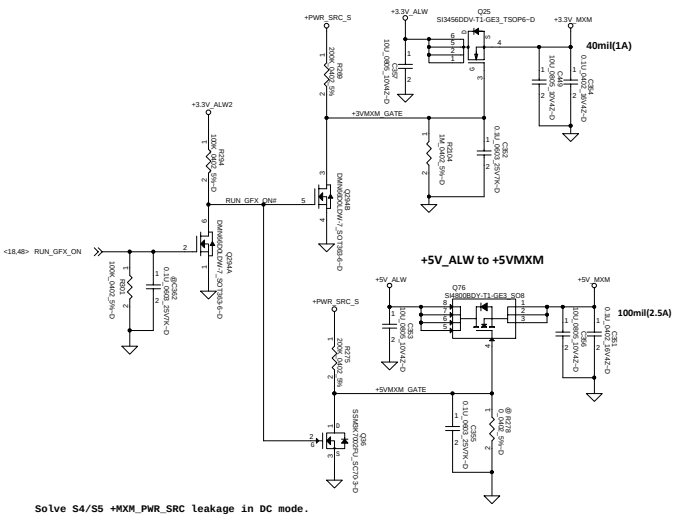
ME request.

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTI
TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT
BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION,
NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIR
PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

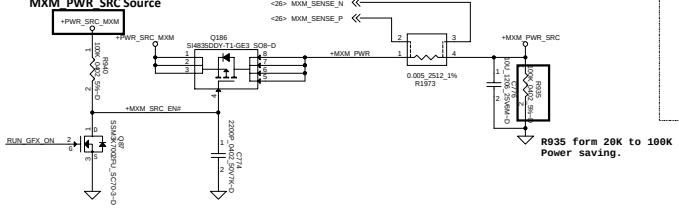
Compal Electronics, Inc.	
Title	PAD & Standoff & LED
Size	Document Number: LA-7931P
Rev	1.0
Date: Monday, July 23, 2012	Sheet 51 of 70

+3.3V_ALW to +3VMXM



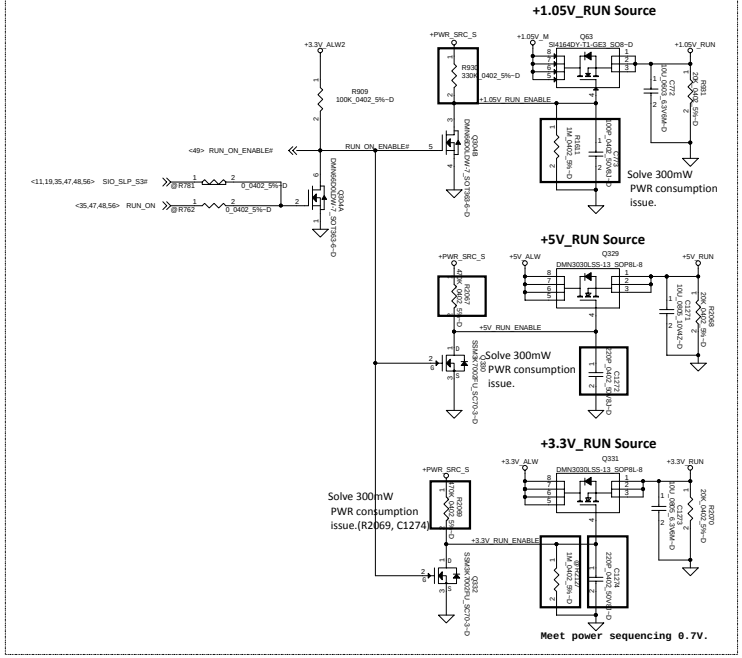
Solve S4/S5 +MXM_PWR_SRC leakage in DC mode.

MXM_PWR_SRC Source



R935 form 20K to 100K
Power saving.

+1.05V_RUN Source

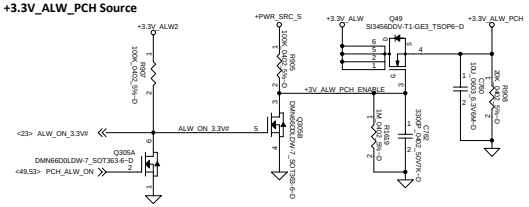


+5V_RUN Source

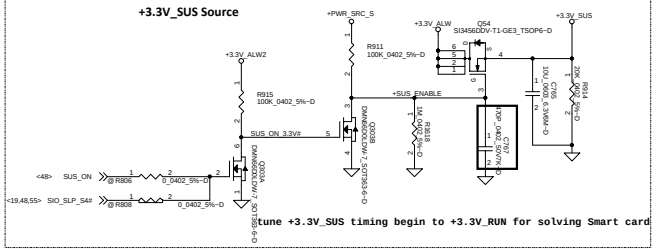
+3.3V_RUN Source

Meet power sequencing 0.7V.

+3.3V_ALW_PCH Source

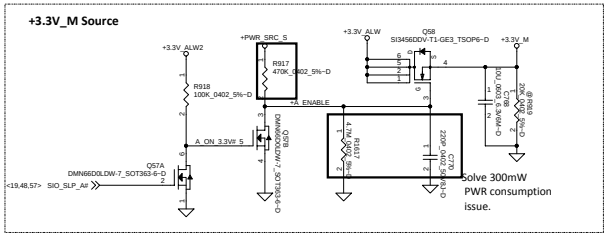


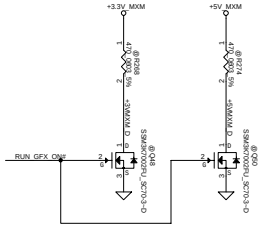
+3.3V_SUS Source



Tune +3.3V_SUS timing begin to +3.3V_RUN for solving Smart card detect issue.

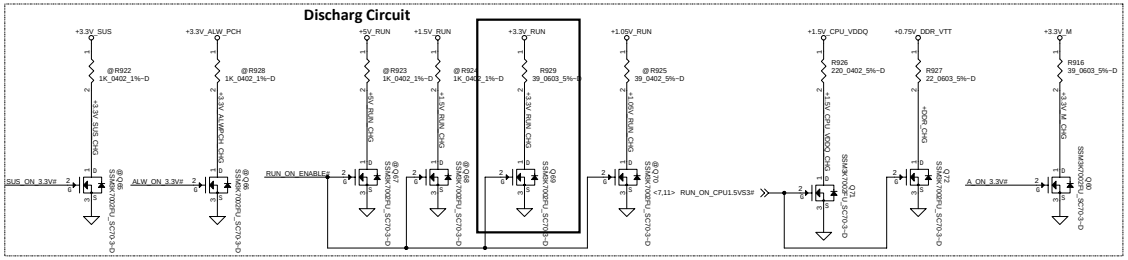
+3.3V_M Source





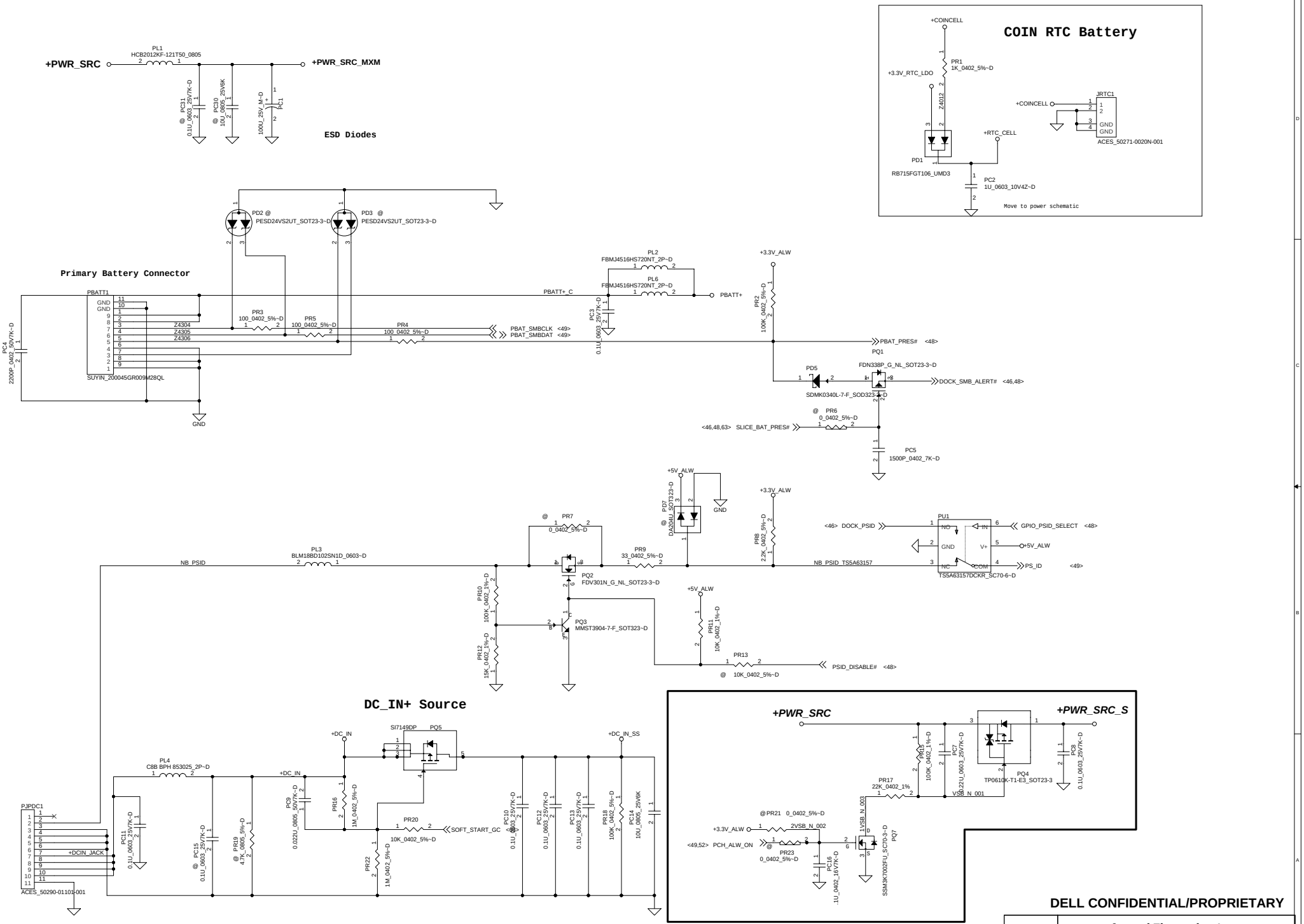
pop for boot leakage to +3.3v_run.

Discharg Circuit

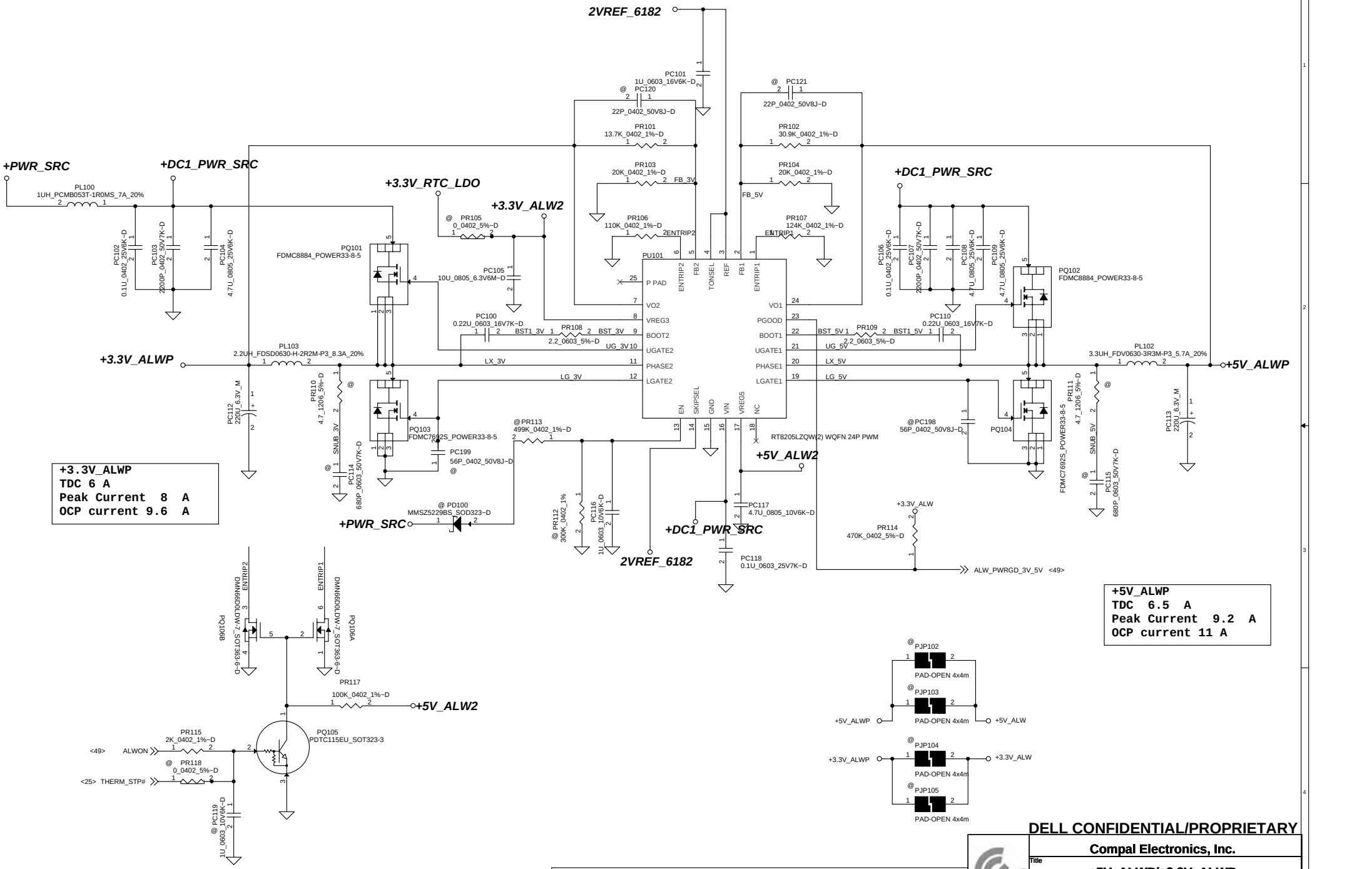


DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
File: Power Control		
Size	Document Number: LA-7931P	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 52 of 70	



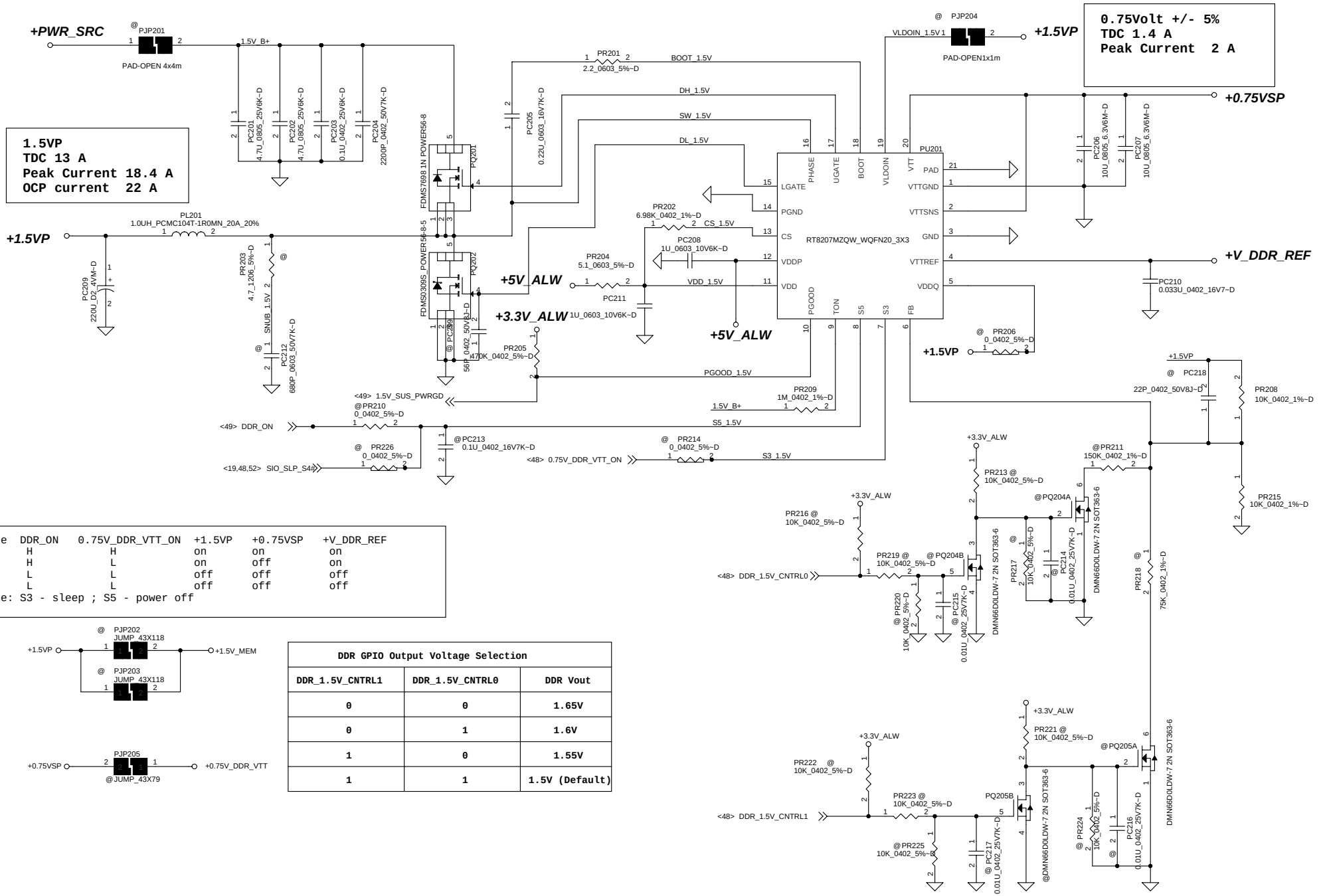
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONF
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTA
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIV
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT C

Compal Electronics, Inc.	
Title	+5V_ALWP/+3.3V_ALWP
Size	Document Number: LA-7931
Rev	1.0
Date:	Monday, July 23, 2012
Sheet	54 of 70



Mode	DDR_ON	0.75V_DDR_VTT_ON	+1.5VP	+0.75VSP	+V_DDR_REF
S0	H	H	on	on	on
S3	H	L	on	off	on
S4	L	L	off	off	off
S5	L	L	off	off	off

Note: S3 - sleep ; S5 - power off

DDR GPIO Output Voltage Selection		
DDR_1.5V_CNTRL1	DDR_1.5V_CNTRL0	DDR Vout
0	0	1.65V
0	1	1.6V
1	0	1.55V
1	1	1.5V (Default)

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

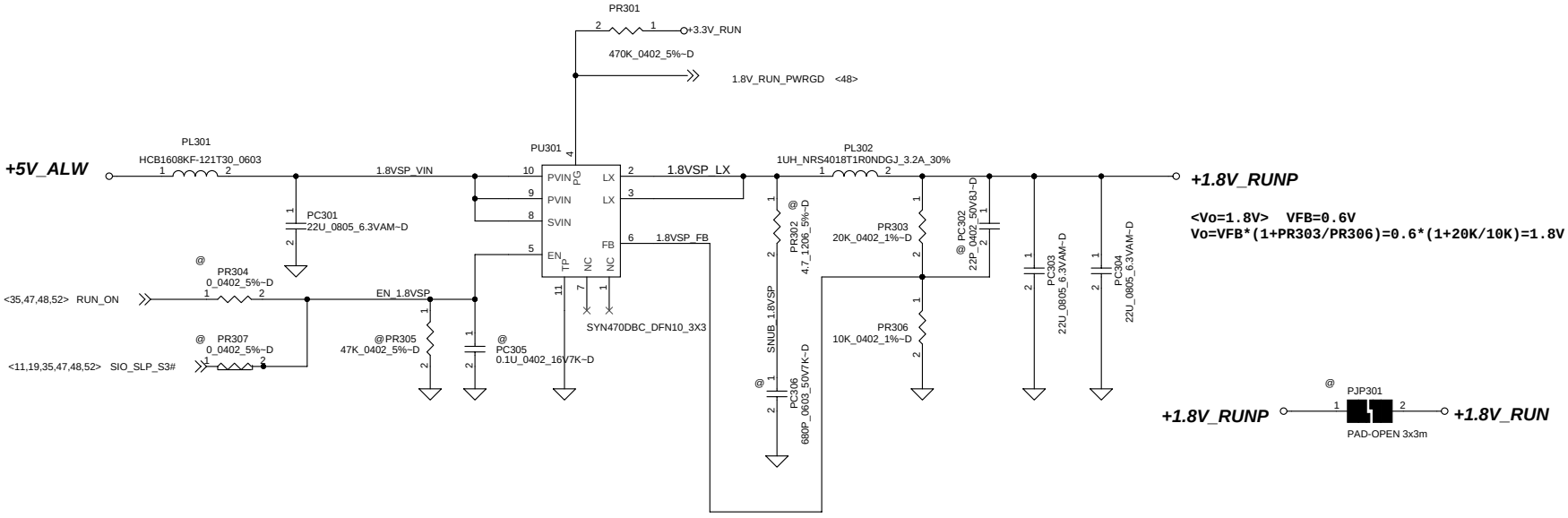
Compal Electronics, Inc.

Title: +1.5VSP/0.75VSP

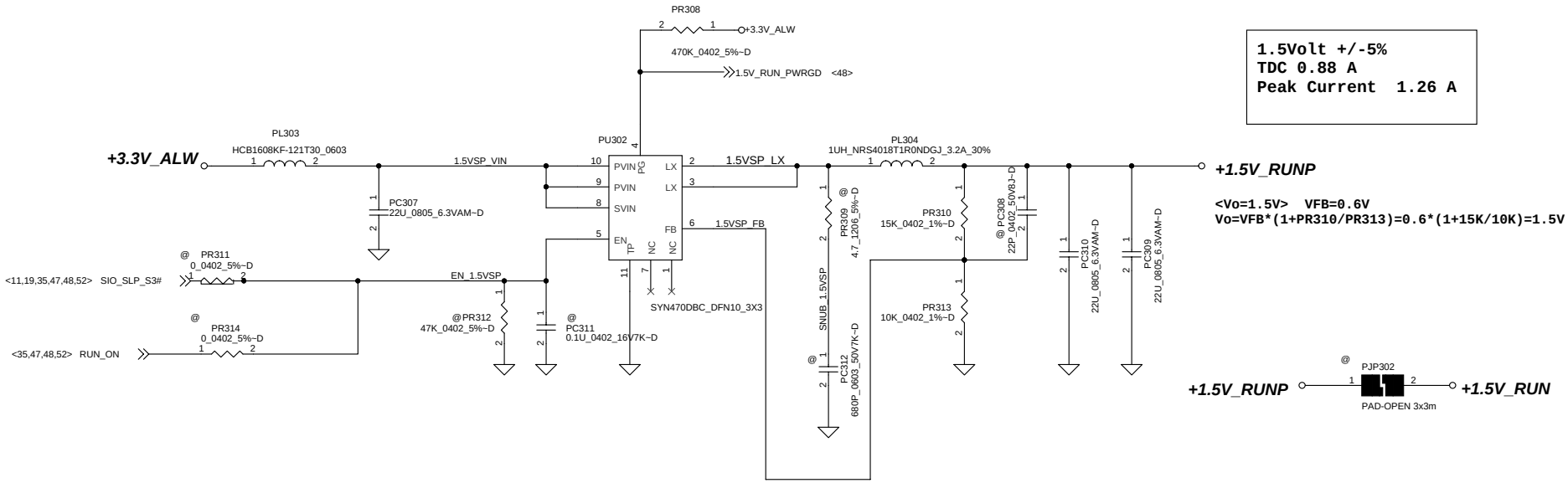
Size: | Document Number: LA-7931 | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 55 of 70

1.8Volt +/-5%
TDC 0.65A
Peak Current 0.93A



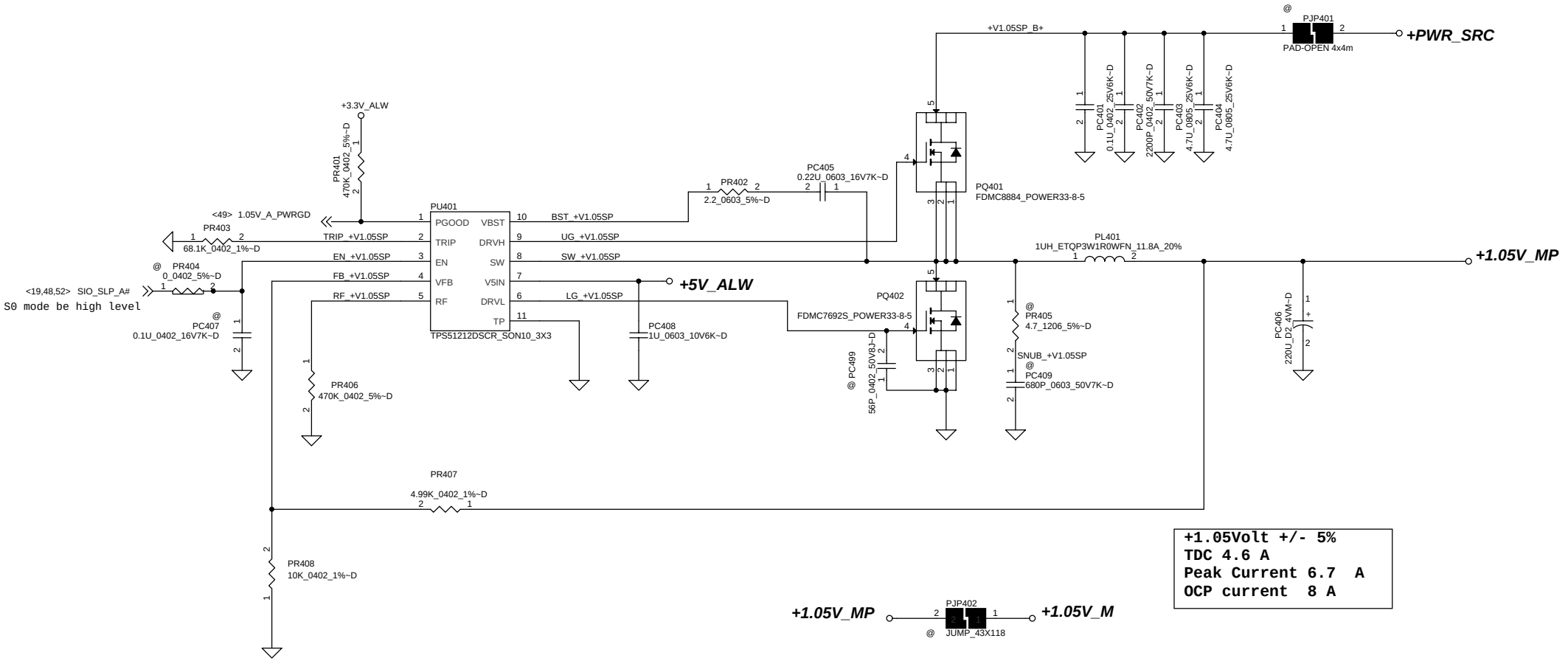
1.5Volt +/-5%
TDC 0.88 A
Peak Current 1.26 A



DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIV
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS,

Compal Electronics, Inc.		
Title: +1.8V_RUN		
Size	Document Number: LA-7931	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 56 of 70	

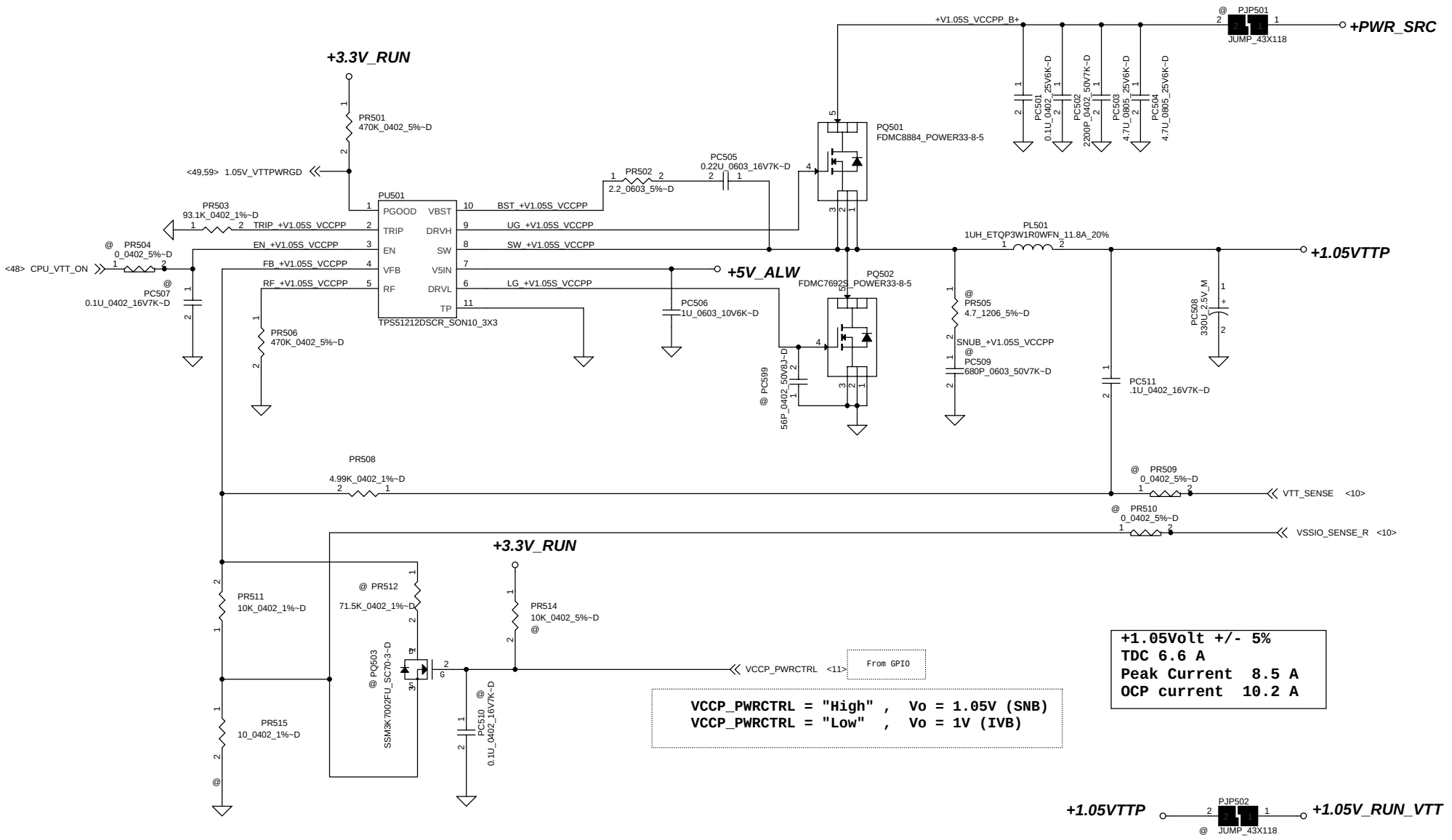


+1.05Volt +/- 5%
TDC 4.6 A
Peak Current 6.7 A
OCP current 8 A

DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIV
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT C
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, IN

Compal Electronics, Inc.	
Title	+1.05V_M
Size	Document Number: LA-7931
Rev	1.0
Date:	Monday, July 23, 2012
Sheet	57 of 70



DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIV
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT C
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, IN

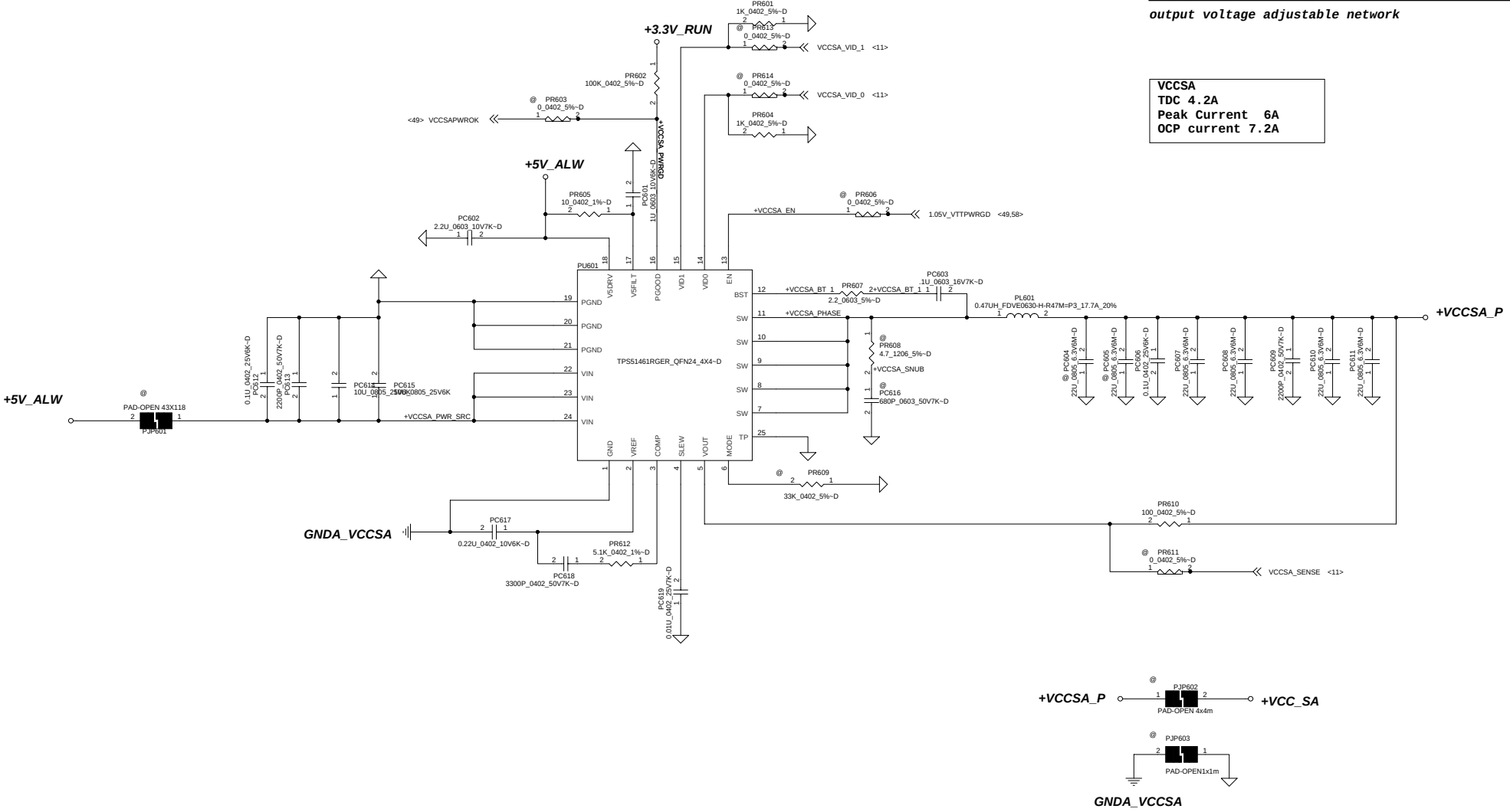
Compal Electronics, Inc.	
Title	+1.05V_RUN_VTT
Size	Document Number: LA-7931
Rev	1.0
Date:	Monday, July 23, 2012
Sheet	58 of 70

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

VCCSA
TDC 4.2A
Peak Current 6A
OCP current 7.2A

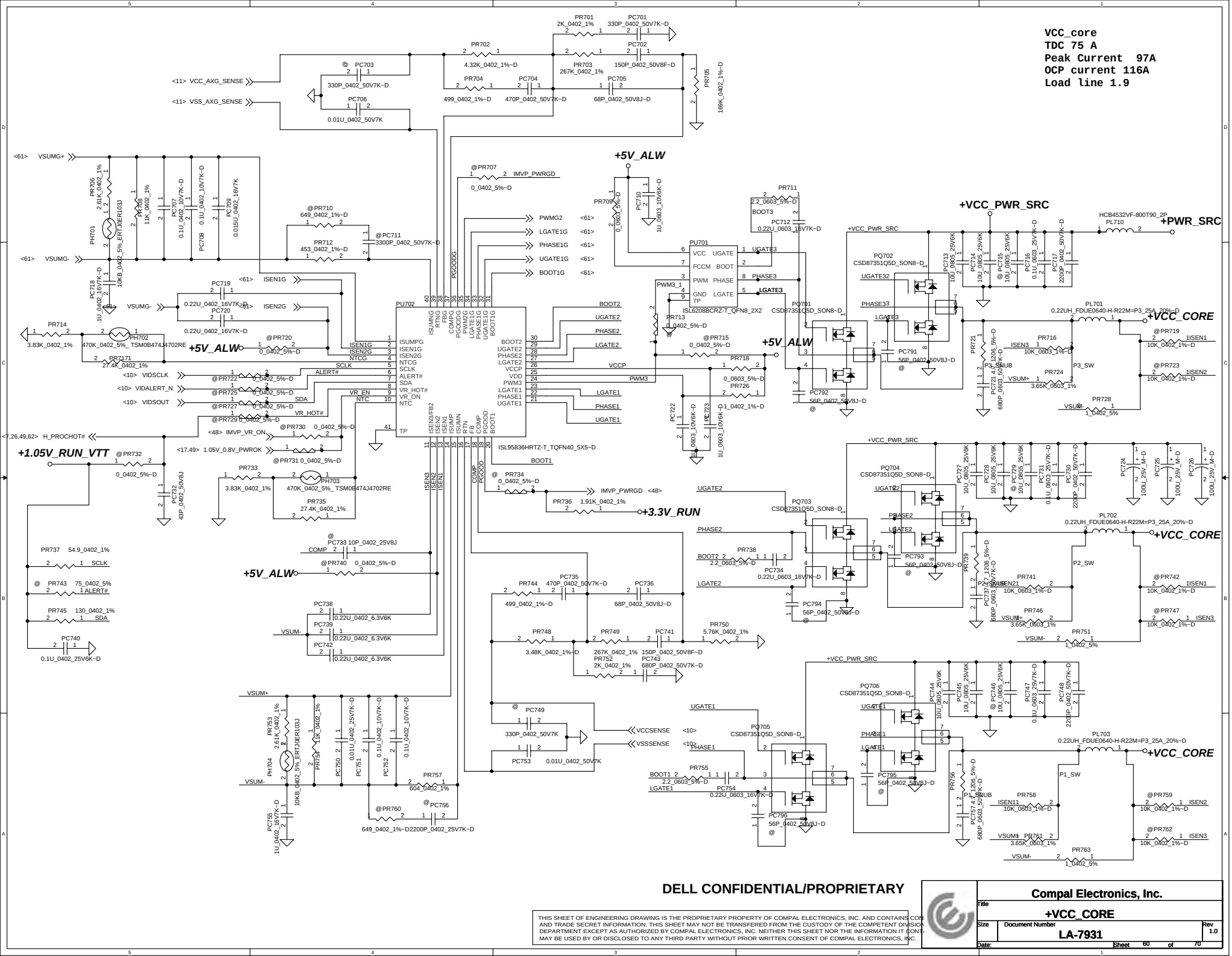
The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



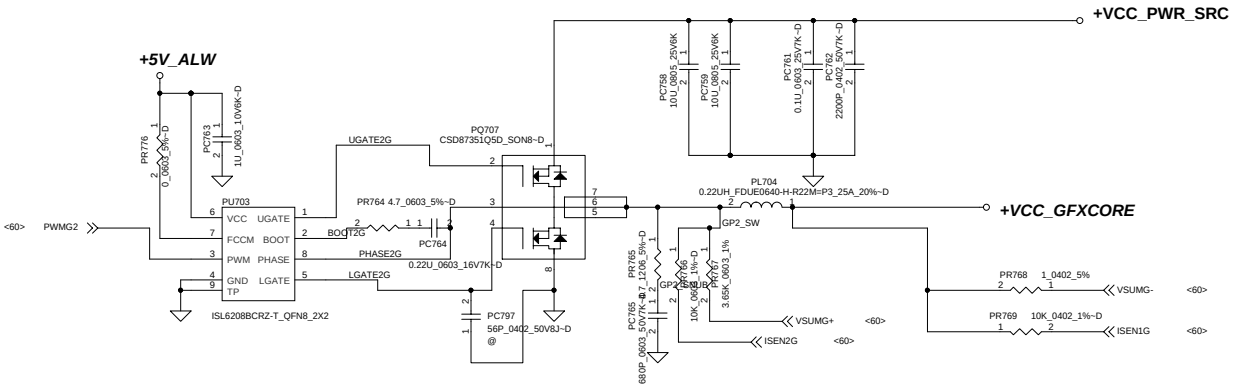
DELL CONFIDENTIAL/PROPRIETARY

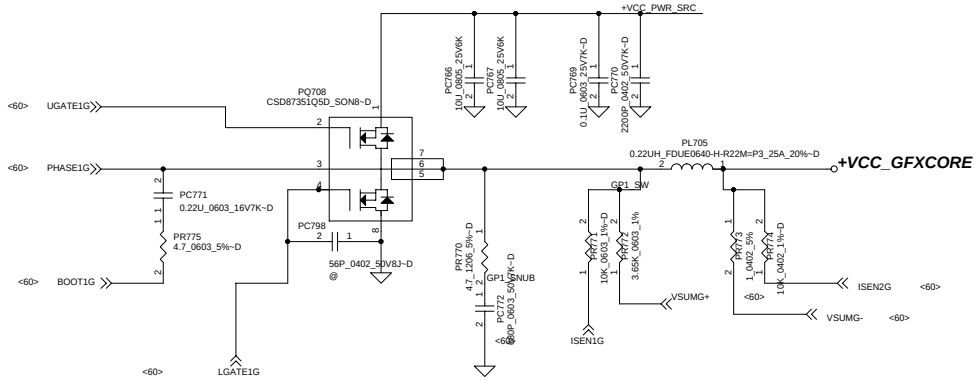
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CO
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISIC
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CON
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.	
Title	+VCC_SA
Size	Document Number: LA-7931
Rev	1.0
Date:	Monday, July 23, 2012
Sheet	59 of 70


VCC_core
TDC 75 A
Peak Current 97A
OCP current 116A
Load line 1.9
+5V_ALW
+VCC_PWR_SRC
+PWR_SRC
+VCC_CORE
+1.05V_RUN_VTT
+3.3V_RUN
PU701
ISL6208BCRZ-T_QFN8_2X2
PU702
ISL95836HRTZ-T_TQFN40_5X5~D
PQ701
PQ702
PQ703
PQ704
PQ705
PQ706
CSD87351Q5D_SON8~D
PL701
PL702
PL703
0.22UH_FDUE0640-H-R22M=P3_25A_20%~D
PL710
HCB4532VF-800T90_2P
<11> VCC_AXG_SENSE
<11> VSS_AXG_SENSE
VCCSENSE
VSSSENSE
DELL CONFIDENTIAL/PROPRIETARY
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CON
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONT
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
+VCC_CORE
Size
Document Number
LA-7931
Rev
1.0
Date:
Sheet 60 of 70

VCC_GFXCORE
TDC 38A
Peak Current 46A
OCP current 57.18A
Load line 3.9





DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CO
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISIC
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CON
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Title	+VCC_GFXCORE	
Size	Document Number: LA-7931	Rev: 1.0
Date:	Sheet 61 of 70	

Iada=0~9.23A(180W)

E2 AC_OK=17.7 Volt

PR913
TI bq24745 = 316K
Intersil ISL88731 = 226K
Maxim = 383K

Vref
TI bq24747 = 3.3V
Intersil ISL88731C = 3.2V
VDDP
TI bq24747 = 6V
Intersil ISL88731C = 5.1V

Maximum charging current is 7.2A

	DYN_TUR_CURRENT_SET#
150W	High
180W	Low

Adapter Protection Circuit for Turbo Mode

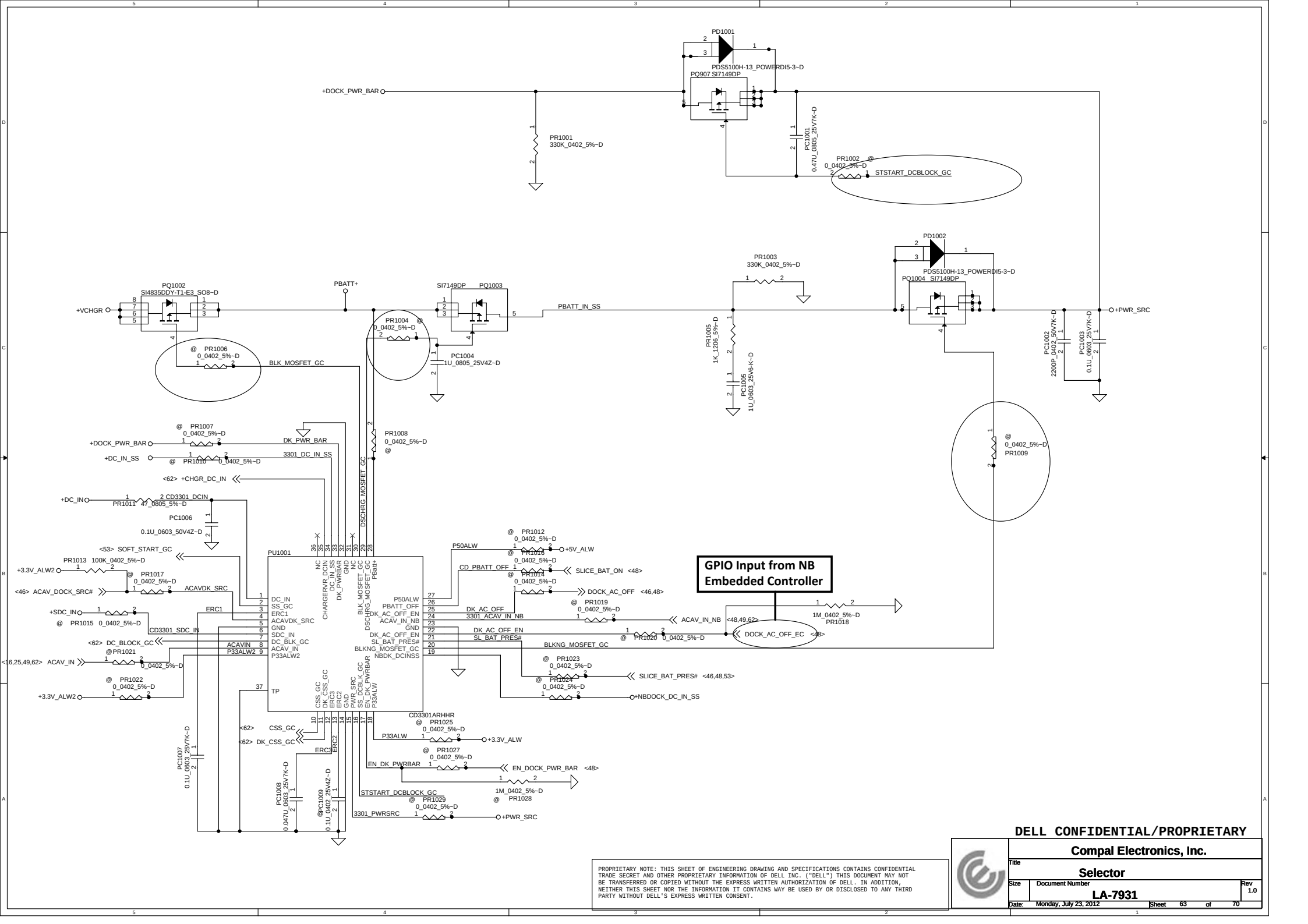
PU901 22@	PR913 22@	PC934 22@	PR927 22@	PR905 22@	PR906 22@	PC905 22@	PR919 22@
BQ24747	316k_0402_1%	0.1U_0603_25V6	0_0402_5%	0_0402_5%	0_0402_5%	0.1U_0402_25V6	1 +-5% 0603

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

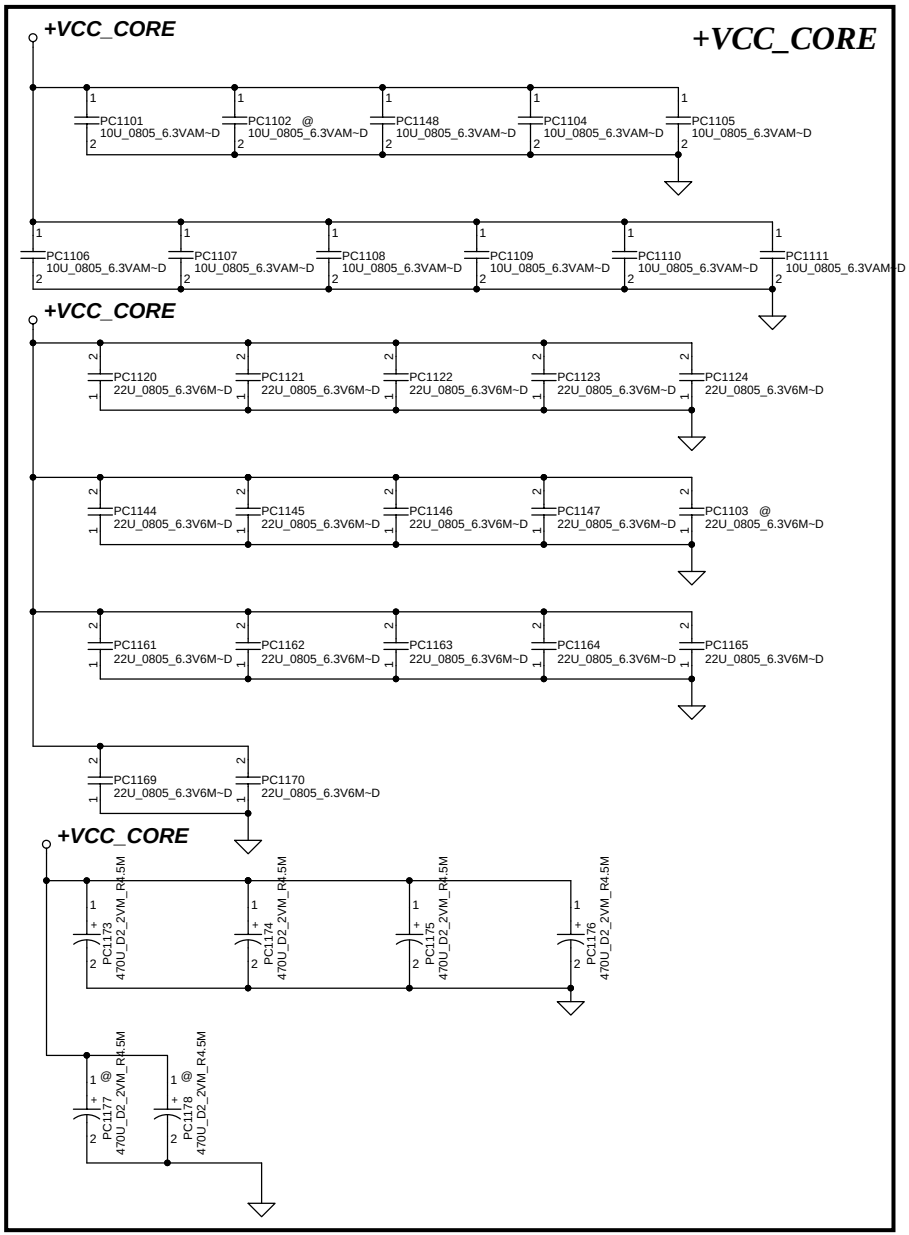
Title	Charger	
Size	Document Number: LA-7931	Rev: 1.0
Date: Monday, July 23, 2012	Sheet 62 of 70	



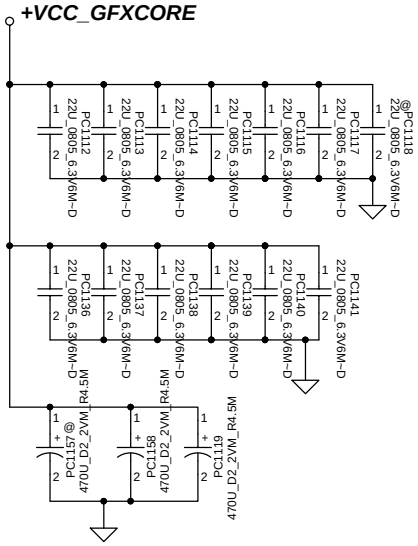
DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.	
Title	Selector
Size	Document Number: LA-7931
Rev	1.0
Date:	Monday, July 23, 2012
Sheet	63 of 70

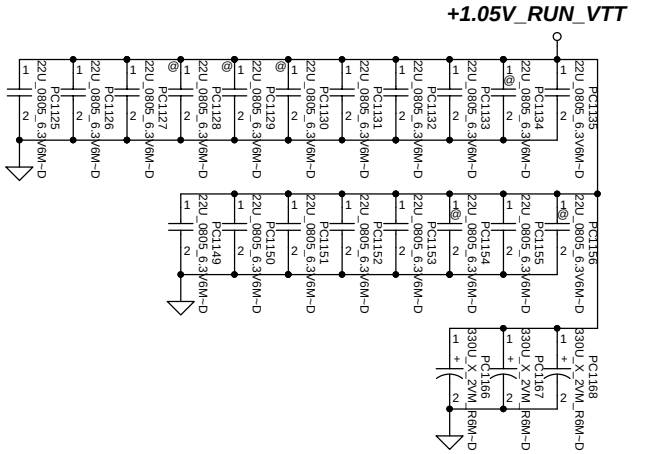


+VCC_GFXCORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS C
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIV
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT C
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, IN

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size | Document Number: LA-7931 | Rev: 1.0

Date: Monday, July 23, 2012 | Sheet 64 of 70

Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	62	PWR	10/11	Intersil	Remove Docking current sense voltage division	Remove PR946、PR948 and PR947	X01
2	53	PWR	10/14	Compal	Change RTC battery connector	Change to SP02000RO00	X01
3	53	PWR	10/14	Compal	Add control singnal to control S5 power consumption	Add PR23 to connect PCH_ALW_ON singal	X01
~~4~~	~~62~~	~~PWR~~	~~10/14~~	~~Compal~~	~~Change H_PROCHOT# voltage source of Compare reference~~	~~PR937 connect to 2VREF_6182~~	~~X01~~
5	53	PWR	10/25	Compal	Change PQ5 Package for layout space	Change footprint from TO252 to SO8_5P	X01
6	60	PWR	11/01	Compal	Change PC707 PC751 footprint from 0603 to 0402	Change PC707 PC751 footprint to 0402	X01
7	61	PWR	11/01	Compal	Remove PJP702	Remove PJP702	X01
8	54,55,57,58,60,61,62	PWR	11/07	Compal	Low side MOSFET Gate induce voltage	Reserve PC198,PC199,PC299,PC499,PC599,PC791,PC792, PC793,PC794,PC795,PC796,PC797,PC798,PC999	X01
9	53	PWR	11/07	Compal	Reserve 10u and 0.1u Cap with MXM_pwr_src	Reserve PC30 and PC31	X01
10	53	PWR	03/01	Compal	Reserve PD7 for ESD requirement	Reserve PD7	X03
11	53,54,55, 56,57,58, 59,59,60, 61,62,63	PWR	04/03	Compal	Change 0 Ω footprint to R0402_0ohm	PR1002,PR1004,PR1006,PR1007,PR1008,PR1009,PR1010,PR1012, PR1014,PR1015,PR1016,PR1017,PR1019,PR1020,PR1021,PR1022, PR1023,PR1024,PR1025,PR1027,PR1029,PR105,PR118,PR206, PR214,PR226,PR23,PR307,PR311,PR404,PR504,PR509,PR510,PR6, PR603,PR606,PR611,PR613,PR614,PR713,PR722,PR725,PR727, PR729,PR731,PR734,PR902,PR903,PR910,PR915,PR935,PR938	X06
12	59	PWR	04/03	Compal	Change PL601 Footprint for DFB issue	Change PL601 footrpint to TAI-T_VMPI0703AR-1R0M-Z01_2P	X06
13	53	PWR	04/03	Compal	Battery ESD protect with ESD diodie	PD3.3 connect with PBATT1.7	X06
14	54,62	PWR	04/03	Compal	Remove jump of co-lay with input choke	Remove PJP901 and PJP101	X06
15	60	PWR	05/04	Compal	Change PL710 Footprint for DFB issue	Change PL701 footrpint to KC_FBMA-L11-453215-121LMA90T_2	X07
16	60	PWR	05/14	Compal	Change 0 Ω footprint to R0402_0ohm	PR928	X07

DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CON AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISIO DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONT MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	16	HW	2011/09/01	COMPAL	correct MXM LVDS signals.	Swap CHA and CHB signals on JMXM1.	0.2(X00)
2	51	HW	2011/09/01	COMPAL	Add current limilt R for Breath LED.	Add R956(374ohm).	0.2(X00)
3	46	HW	2011/09/04	COMPAL	for layout routing easy.	Move D33,C702,CE6 from JDOCK1.146~148 to JDOCK1.149~151. JDOCK1.146~148 change to dummy pin.	0.2(X00)
4	51	HW	2011/09/06	Lite-on	to meet LED min workable current(2mA).	Change R934,R939,R942,R955,R941 from 2.2kohm to 1.2kohm. R943 from 2.2kohm to 374ohm.	0.2(X00)
5	27	HW	2011/09/06	COMPAL	Add MXM DDC signals pull up R.	pop R1121,R1122.	0.2(X00)
6	45	HW	2011/09/09	COMPAL	Add DOCK DP DDC signals control circuit.	Add R2144~R2157,C1331,C1332,Q333~Q336,R2161~R2164,Q337.	0.3(X01)
7	41	HW	2011/09/14	COMPAL	modify JUSH1 pin define for meeting USH/B JUSH1 pin define change.	change JUSH1 pin define.	0.3(X01)
8	50	HW	2011/09/19	COMPAL	modify JBT1 pin define for meeting BT connector change.	Swap JBT1 pin1~pin12 pin define to pin12~pin1.	0.3(X01)
9	46,28,50	ME	2011/09/27	COMPAL	Change connector follow connector list 0913A.	Change JDOCK1 to WD2F144WB5R400,JLVDS1 to 50398-04071-001,JBT1 to 50450-0127N-001.	0.3(X01)
10	52	HW	2011/09/27	COMPAL	+3.3V_RUN boot leakage.	Pop R929,Q69.	0.3(X01)
11	20,48,28	HW	2011/09/28	DELL	Drop touch panel.	Remove net "USBP13-,USBP13+,TOUCH_SCREEN_PD#" and L11,R429,R430,D86,R419, JTS1.	0.3(X01)
12	46	HW	2011/09/28	COMPAL	Add pull-down R for DPC_GPU_HPD.	Add R773(100K ohm).	0.3(X01)
13	34	HW	2011/09/29	COMPAL	Change the R518 value to meet the PS8336B input high-level voltage.	Change R518 from 100k to 10kohm.	0.3(X01)
14	52	HW	2011/09/29	COMPAL	Solve S4/S5 +MXM_PWR_SRC leakage in DC mode.	Change R940 pin1 connect from +PWR_SRC_S to +PWR_SRC_MXM.	0.3(X01)
15	49,17,18	HW	2011/10/04	COMPAL	Crystal EA.	Change C743,C741 from 22pF to 39pF, CH2,CH3 from 15pF to 18pF, CH18,CH19 from 12pF to 10pF.	0.3(X01)
16	17	HW	2011/10/12	COMPAL	Debug component control for pop them until ST.	Add JTAG@ for RH288,RH59,RH44,RH45,RH43,RH47~RH49.	0.3(X01)
17	48	HW	2011/10/12	COMPAL	Wireless switch needs to be pulled to ALW, Without it being pulled to ALW rail AOAC will work incorrect.	Add R2158 let WIRELESS_ON#/OFF pull up to ALW, no stuff R766	0.3(X01)
18	51	HW	2011/10/12	COMPAL	Solve Breath LED flicker when AC-in plug and correct Breath LED top and side view work behavior.	Add Q327 and use"MASK_BASE_LEDS#" to control Breath LED top view. use"SYS_LED_MASK#" to control Breath LED side view.	0.3(X01)
19	28	HW	2011/10/12	COMPAL	JLVDS1 connector change,then GND shield shift(different from original).because JLVDS1 and JLVDS2 co-lay,we need change pin define.	JLVDS2 pin41,42 change to EDP_LVDS_A3-,EDP_LVDS_A3+, pin43~pin46 change to GND.	0.3(X01)
20	34	HW	2011/10/12	COMPAL	Choice DDC active buffer mode.and control switching Mode.	Pop R68 and non-pop R58.	0.3(X01)
21	50	HW	2011/10/13	COMPAL	To meet intel spec: T235(power off)= min 40ns). T08a(power on)= max 90ms.	change U4 from RT9801AGE to RT9818A-44GU3,R1622 to 100kohm.add R2159. remove R2129~R2134. pop R2142 and non-pop R1623.	0.3(X01)
22	14	ME	2011/10/13	COMPAL	Change connector follow connector list 1005A.	Change JDIMM3 to 2-2013310-1.	0.3(X01)
23	38	HW	2011/10/19	COMPAL	LAN EA.	Change T156 to SP050006P0L.	0.3(X01)
24	22	HW	2011/10/19	COMPAL	for solving dispaly ripples. 1/2	Change LH1 to 4.7uH inductor.	0.3(X01)
25	40	HW	2011/10/25	COMPAL	NEC_TOKIN shortage issue for the flood in Tailand.	Change C323,C324 to SGA0000370L(Panasonic).	0.3(X01)
26	34	HW	2011/10/25	COMPAL	HDMI EA.	pop R451~R456,R458,R459 and non-pop L19,L23,L24,L25.	0.3(X01)
27	51	HW	2011/10/25	COMPAL	improve BT_LED behaviour abnormal(BT_LED must dark) in S3/S4/S5.	change R938 PU from +3.3V_RUN to +3.3V_ALW.	0.3(X01)
28	38,51	HW	2011/10/26	COMPAL	for ESD Hi-Pot fail.	change JLOM1 "pin14 and pin15" from "GND_CHASSIS1 and GND_CHASSIS" to GND. change H5 to NPTH.	0.3(X01)
29	41	HW	2011/10/26	COMPAL	TPM chip to new version chip due to OS Win8 supported problem	Change U39 TPM solution to new p/n: SA00004WQ10	0.3(X01)
30	51	ME	2011/10/26	COMPAL	screw hole change follow 1021A ME drawing.	Change H5 to 3P2X6P2 and H18,H19,H23,H24 to 4P1.	0.3(X01)
31	51	HW	2011/10/28	COMPAL	Solve Breath LED flicker when AC-in plug,follow E4 solution.	Remove Q327 and modify EC code from PWM Output to GPIO input on ECE5048 (GPIOM3/PWM4).	0.3(X01)
32	52	HW	2011/10/28	COMPAL	For Inrush current issue.	Change C1274 from 470pF to 2200pF for meeting OCP.	0.3(X01)

DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CON
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISIO
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONT
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
33	52	HW	2011/10/28	COMPAL	For smart card detect issue.	Change C767 from 4700pF to 470pF for turning proper +3.3V_SUS timing begin to +3.3V_RUN.	0.3(X01)
34	14	HW	2011/10/28	COMPAL	For DFX issue.	Change CD45 from 0603 size to 0402 for easy move to keep away battery connector.	0.3(X01)
35	47,46,32 40,29	HW	2011/10/28	COMPAL	For ESD request.	Change D97,D33,D91,D92 to non-pop. D14,D16 change main source(SC30000250L) to SC300002F0L and D88,D89 change main source(SCA00000T0L) to SC300002F0L.	0.3(X01)
36	46	HW	2011/10/31	COMPAL	EMI request,add 33ohm for DOCK DVI signals.	Add R2160,R2165~R2179(33ohm) for DOCK DVI port A,B.	0.3(X01)
37	34	HW	2011/10/31	COMPAL	EMI request,add reserve C(3.3pF) for HDMI signals.	Add reserve C1333~C1340(3.3pF) for HDMI signals.	0.3(X01)
38	21	HW	2011/11/2	COMPAL	PCH has internal pull up 20k ohm on (GPIO27)	No stuff RH175	0.3(X01)
39	21	HW	2011/11/2	COMPAL	Power saving	RH362 change from 10K to 100K	0.3(X01)
40	22	HW	2011/11/2	COMPAL	for solving dispaly ripples. 2/2	Change CH36 to 22uF_0805 size.	0.3(X01)
41	49	HW	2011/11/2	COMPAL	Change board ID to X01	Change R875 to 130K	0.3(X01)
42	52	HW	2011/11/2	COMPAL	Power saving	R935 change from 20K to 100K	0.3(X01)
43	33,46	HW	2011/11/2	COMPAL	reduce layout via.	MXM DP lane for Docking direct connect to JDOCK1.	0.3(X01)
44	45	HW	2011/11/3	COMPAL	remove double pull low R.	remove R2144,R2154.	0.3(X01)
45	16	HW	2011/11/3	COMPAL	only 10-bits panel use.	change R2095,R2096 to 6@ group.	0.3(X01)
46	49	HW	2011/11/3	COMPAL	SMBUS EA.	change R838,R841 to 2Kohm for rise timing fail.	0.3(X01)
47	32	LAYOUT	2011/11/7	COMPAL	Add TEST point for JCRT PIN11.	Add CRT_11 net and test point(T61) for JCRT1.11.	0.3(X01)
48	33	HW	2011/11/7	COMPAL	Add space for easy to layout.	Remove R2081~R2088 and remove Net DPC_DOCK_LANE_P0~P3,DPC_DOCK_LANE_N0~N3.	0.3(X01)
49	40	HW	2011/11/7	Parade	USB3.0 EA fine tune(TX:EQ-->9.5dB,DE-->3.5dB; RX:EQ-->7.5dB,DE-->5dB).	pop R22,R18,R30,R28 and change R2141 from 4.99kohm to 4.7kohm.	0.3(X01)
50	30	HW	2011/11/8	H.ELE	Vender suggested changed small size from 5.0*3.2mm to 3.2*2.5mm.	Change Y7 from SJ100006R00 to SJ10000CZ0L, C1225 from 10pF to 15pF, C1226 from 10pF to 12pF.	0.3(X01)
51	30	HW	2011/11/9	compal	for satisfy ME space limilt.	Change C324 size from D2 to B2.	0.3(X01)
52	46	HW	2011/11/10	COMPAL	Just reserve R for EMI team to test DOCK DVI signals.	Change R2160,R2165~R2179 to 0ohm for DOCK DVI port A,B.	0.3(X01)
53	40	HW	2011/12/30	COMPAL	sourcer request	change USB_PWR_SW from TPS2560 (U45) to G547I2P81U (U642, U643)	0.4(X01)
54	46	EMI	2011/12/30	COMPAL	EMI issue.	Swap USB signal from port 8 to port 4 on JDOCK1.66 & JDOCK1.68	0.4(X01)
55	42	EMI	2011/12/30	COMPAL	EMI issue.	Swap USB signal from port 4 to port 8 on JMINI1.36 & JMINI1.38	0.4(X01)
56	35	HW	2011/12/30	COMPAL	2nd source.	add R2180 ~ R2184, R2189 ~ R2193 for SATA redriver(U26, U637) 2nd source and change R1206 from4.99K ohm to 5.1K ohm.	0.4(X01)
57	41	HW	2012/01/02	COMPAL	Solve +3.3V_RUN Giltch in S5 when AC plugging in.	add R2185, R2186, D103 to SP_TPM_LPC_EN.	0.4(X01)
58	30	HW	2012/01/02	COMPAL	Prevent AUX swing overshoot.	add R2187, R2188 on AUX signal.	0.4(X01)
59	52	HW	2012/01/02	COMPAL	Power sequencing meet 0.7V between +PCH_V5REF_RUN and +3.3V_RUN.	change C1274 from 2200P to 3300P, and No stuff R2127	0.4(X01)
60	34	HW	2012/01/02	COMPAL	HDMI no voice issue	stuff R58.	0.4(X01)
61	51	HW	2012/01/03	COMPAL	Setup Volume mute LED control same as Volume up & down	No stuff Q84B	0.4(X01)
62	46	HW	2012/01/03	COMPAL	EMI request add 33ohm for DOCK DVI signals.	change R2160, R2165 ~ R2179 from 0 ohm to 33 ohm.	0.4(X01)
63	34	HW	2012/01/03	COMPAL	EMI request for HDMI.	stuff L19, L23, L24, L25, No stuff R451~R456, R458, R459	0.4(X01)
64	32	HW	2012/01/03	COMPAL	EMI request for CRT.	change CAP from 3.3P to 12P (C12, C13, C21), and stuff.	0.4(X01)
65	28	HW	2012/01/03	COMPAL	EMI request for Webcam.	stuff L10, No stuff R427, R428	0.4(X01)
66	30,31	HW	2012/01/04	COMPAL	RGB panel sequencing issue.	change power rail from +3.3V_RUN to+3.3V_AVDD on R2039.1, R2040.1, R2038.1, C1227.1, U631.3 Remove C1269, C1270 add L57	0.4(X01)

DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Version Change List (P. I. R. List) Page 3

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
67	16	HW	2012/01/04	COMPAL	Height limitation issue.	change cap from SE142106M8L(1206) to SE00000QK0L(0805)	0.4(X01)
68	40	HW	2012/01/05	COMPAL	change main source.	change main source from SLG55584A to MAX14618 on U2.	0.4(X01)
69	33	HW	2012/01/05	COMPAL	Remove DMC function.	Remove U14, R329~R335, R337, R338, R342~R345, R2091, R2092, C396, C399~C401, C267, C269, C273~C278.	0.4(X01)
70	42	HW	2012/01/05	COMPAL	Remove DMC function.	Remove JMINI1, R493.	0.4(X01)
71	51	ME	2012/01/09	COMPAL	update ME drawing.	Remove H3.	0.4(X01)
72	40	ME	2012/01/09	COMPAL	update ME drawing.	change JUSB1, JUSB2 from FOX_UEA111Y1-C5BDA-7H to FOX_UEA111Y1-C1BD1-7H	0.4(X01)
73	17	ME	2012/01/09	COMPAL	update ME drawing.	change JSPI1 from HRS_FH12-16S-0P5SH(55)~D to TYCO_1-2041070-6~D.	0.4(X01)
74	25	ME	2012/01/09	COMPAL	update ME drawing.	change JFAN1, JFAN2 from ACES_50228-0047N-001 to ACES_50450-0067N-001.	0.4(X01)
75	30	HW	2012/01/10	COMPAL	prevent current leakage.	Change Pull up +3.3V_RUN to +3.3V_AVDD on R2036 and R2037.	0.4(X01)
76	49	HW	2012/01/10	COMPAL	change Board ID to X02.	change R875 to 62K ohm.	0.4(X01)
77	33	HW	2012/01/10	COMPAL	prevent material shortage for Thai flood.	change material from TC7SET04FU to NC7ST04P5X on U636.	0.4(X01)
78	28	HW	2012/01/10	COMPAL	prevent material shortage for Thai flood.	change material from TC7SET04FU to M74VHC1GT125DF2G on U3.	0.4(X01)
79	19,20,25, 37,49,50, 51	HW	2012/01/10	COMPAL	prevent material shortage for Thai flood.	change material from TC7SH08FU to 74AHC1G08GW on U7, U10, U15, U50, U58, UC4, UH3.	0.4(X01)
80	35,43	HW	2012/01/10	COMPAL	add X76 option for main source and 2nd source of SATA redriver .	add X761@ on R1201, R1202, R1206, R2136, R2139, R2140. add X762@ on R2180 ~ R2184, R2189 ~ R2193.	0.4(X01)
81	25	HW	2012/01/11	COMPAL	layout routing swap.	change FAN conn from 4 pin to 6 pin, and swap pin 1, pin6 for JFAN1, JFAN2.	0.4(X01)
82	16	HW	2012/01/11	COMPAL	For NVDIA request.	add R2194, R2195 (No stuff) and pull up to +3.3V_MXM on JMXM1B.268, JMXM1B.270	0.4(X01)
83	32	HW	2012/01/18	COMPAL	EMI request.	change CAP to 22P (C20,C22,C23) and 10P (C12, C13, C21), and all stuff.	0.4(X01)
84	46	HW	2012/01/20	COMPAL	Solve dock detection issue.	change R755 from 100K to 10K.	0.4(X01)
85	49	HW	2012/01/20	COMPAL	Avoid material mixture with E3 project 5055 devices.	change MEC5055 from SA00003TZ1L to SA00003TZ2L.	0.4(X01)
86	11,28,36 44,52	HW	2012/01/20	COMPAL	Change RC value at Gate of MOS Load SW to modify power rail soft start timing.	RC73 from 100K to 330K; RC79 from 330K to 1M; CC71 from 0.1u to 0.022u R412 from 100K to 470K; R1632 from 1M to 4.7M; C293 from 0.1u to 0.022u R515 from 100K to 470K; R2126 from 1M to 4.7M; C416 from 0.1u to 0.022u R731 from 100K to 470K; R1628 from 1M to 4.7M; C651 from 4700p to 220p R737 from 100K to 470K; R1629 from 1M to 4.7M; C652 from 4700p to 220p R917 from 100K to 470K; R1617 from 1M to 4.7M; C770 from 4700p to 220p R930 from 100K to 470K; R1611 from 470K to 2.2M; C773 from 2200p to 100p R2067 from 100K to 470K; C1272 from 2200p to 220p R2069 from 100K to 470K; C1274 from 470p to 220p	0.4(X01)
87	16	HW	2012/02/29	COMPAL	For NVDIA request.	No stuff RV29.	0.5(X01)
88	40	HW	2012/02/29	COMPAL	2nd source.	add R2196 ~ R2197, change power rail from +3.3V_RUN to +USB3 on U638.9 and U638.25	0.5(X01)
89	40	HW	2012/02/29	COMPAL	Reserve for samsung mobile issue.	add Q338 and No stuff.	0.5(X01)
90	51	HW	2012/03/01	COMPAL	change MOS to single package.	change Q84, Q339 from DMN66D0LDW to SSM3K7002FU.	0.5(X01)
91	25	HW	2012/02/29	COMPAL	change FAN conn.	change FAN conn from ACES_50450-0067N-001 to ACES_50271-0040N-001 on JFAN1, JFAN2	0.5(X01)

DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
92	40	HW	2012/03/01	COMPAL	change main source.	change main source from MAX14618 to SLG55584A on U2.	0.5(X01)
93	35	HW	2012/03/01	COMPAL	For SATA Gen2, Gen3 EA setting.	stuff R1173, R1204 and No stuff R1206.	0.5(X01)
94	43	HW	2012/03/01	COMPAL	For SATA Gen2, Gen3 EA setting.	stuff R2135, R2138 and No stuff R2139.	0.5(X01)
95	31	HW	2012/03/01	COMPAL	Meet RGB panel sequencing.	stuff L56 and No stuff L57.	0.5(X01)
96	28	HW	2012/03/01	COMPAL	change to new manufacturing technology.	change from RB751V-40GTE to RB751VM-40TE on D53,D64,D66,D67,D69,D100, D101.	0.5(X01)
97	29	HW	2012/03/02	COMPAL	According to new EIA rule.	Change U627 from PS8330BQFN48GTR-A0 to PS8330BQFN48GTR2-A0.	0.5(X01)
98	28	HW	2012/03/05	COMPAL	Solve LVDS cable burn out issue.	change JLVDS1.4 and JLVDS2.4 to NC.	0.5(X01)
99	16	HW	2012/03/05	COMPAL	Meet high level on DGPU_PEX_RST# for N14P.	change RV29 to 750 ohm and stuff.	0.5(X01)
100	40	ME	2012/03/05	COMPAL	Update Conn list.	change JUSB1, JUSB2 from UEA111Y1-C1BD1-7H to AUSB0041-P001A.	0.5(X01)
101	34	HW	2012/03/05	COMPAL	Meet AMD HDMI 297 MHz EA setting.	stuff R71, R65, R67.	0.5(X01)
102	40	HW	2012/03/06	COMPAL	2nd source.	change power rail from +3.3V_RUN to +USB3 on R26.1	0.5(X01)
103	51	ME	2012/03/07	COMPAL	ME request.	add H27.	0.5(X01)
104	12	HW	2012/03/08	COMPAL	layout space limitation.	Remove RD12, RD13.	0.5(X01)
105	13	HW	2012/03/08	COMPAL	layout space limitation.	Remove RD21, RD22.	0.5(X01)
106	28	HW	2012/03/08	COMPAL	Solve LVDS cable burn out issue.	add one test point on JLVDS1.4 and JLVDS2.4	0.5(X01)
107	28	HW	2012/03/13	COMPAL	Wrong CPN for prefix number.	change CPN from SM01000700L to SM070001I0L on L10.	0.5(X01)
108	11	HW	2012/03/13	COMPAL	Solve backdrive (follow B4).	change CPN from SB00000L800 to SB00000RV00 on QC3.	0.5(X01)
109	16	HW	2012/04/02	COMPAL	Solve AUX signal pull to different power rail.	Change power rail from +3.3V_RUN to +3.3V_AVDD.	0.6(X02)
110	28	EMI	2012/04/02	COMPAL	EMI request.(RGB noise coupling to LVDS cable 224MHz)	Reserve C1341, C1342 on LCD_SMBCLK and LCD_SMBDAT.	0.6(X02)
111	7~52	HW	2012/04/05	COMPAL	short all reserved 0 Ohm resister.	RC24,RC27,RC17,RC18,RC25,RC68,RC69,RC83,RD1,RD2,RD7,RD14, R1157,R1158, RD15,RD16,RD23,RD24,RD25,RD32,RD33,RD34,RD39,RD40,R1169,R1624,R1626 R1970,RH286,RH290,RH307,RH308,RH82,RH83,RH85,RH86,RH88,RH90,RH92,R2089, RH93,RH95,RH96,RH280,RH281,RH359,RH113,RH323,RH116,RH117,R2090,R2105,R2142 RH320,RH120,RH121,RH122,RH334,RH343,RH335,RH336,RH338,RH339,RH341,RH356, RH259,RH150,RH201,R1187,R551,R552,R2159,RC29,RC34,RC40, R555,R1144,R702,R707,R709,R703,R724,R730,R713,R797,R771,R741,R815,RC9,RH1, R1068,R867,R853,R855,R862,R1180,R1633,R781,R808,RH2,RH309,RH337,R2072, R289,RH202,RH205,RH211.	0.6(X02)
112	26	HW	2012/04/05	COMPAL	Remove current sensor function.	No stuff R1974,R1975,C16,C17,C361,C363.	0.6(X02)
113	25	HW	2012/04/09	COMPAL	change VSET from 88 ℃ to 93 ℃.	change R406 from 953 ohm to 1.33K ohm.	0.6(X02)
114	49	HW	2012/04/09	COMPAL	change Board ID to X03.	change R875 from 62K ohm to 33K ohm.	0.6(X02)
115	29	HW	2012/04/09	COMPAL	[DF543750]DP->HDMI/DP->S-DVI dongle no function on NV units.	Add TMDS DDC PU schematic on DP port that include Q339, Q340,R2198~2201, C1343.	0.6(X02)
116	42	HW	2012/04/09	COMPAL	Add WiGig card function.	Add net name WiGi_RADIO_DIS#_R on JMINI4.32, net name BT_RADIO_DIS#_R on JMINI4.51, and reserve R2204, R2205, D104, D105.	0.6(X02)
117	48	HW	2012/04/09	COMPAL	Add WiGig card function.	change net name from VOL_MUTE_LED# to WiGi_RADIO_DIS# on U46.A1 PU 100K ohm on net WiGi_RADIO_DIS# and BT_RADIO_DIS#.	0.6(X02)

DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CON AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISIO DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONT MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
118	51	HW	2012/04/09	COMPAL	Add WiGig card function.	Remove Q339 for WiGig card function usage.	0.6(X02)
119	47	HW	2012/04/09	COMPAL	Add WiGig card function.	Remove net VOL_MUTE_LED on JIO1.100	0.6(X02)
120	50	HW	2012/04/09	COMPAL	Add WiGig card function.	change net name from BT_RADIO_DIS# to BT_RADIO_DIS#_D on JBT1.6 Add R2206 and reserve D106 on net BT_RADIO_DIS#_D.	0.6(X02)
121	27	HW	2012/04/09	COMPAL	Solve +3.3V_MXM backdrive when disable RUN_GFX_ON.	Reserve R1121, R1122.	0.6(X02)
122	44	HW	2012/04/09	COMPAL	for power saving in DC mode S3.	change R716 to 47K ohm.	0.6(X02)
123	40	HW	2012/04/11	COMPAL	Solve kinston storage device re-distinguish issue.	stuff R28 and R30.	0.6(X02)
124	16	HW	2012/04/11	COMPAL	update MXM conn PCB footprint.	change footprint to JAE_MM70-314-310B1-1-_310P-S.	0.6(X02)
125	40	EMI	2012/04/16	COMPAL	EMI request.	change from DLW21SN900HQ2L to DLW21SN900SQ2L on L39, L41.	0.6(X02)
126	51	HW	2012/04/16	COMPAL	Meet LED brightness spec.	change R943 from 374 ohm to 240 ohm. change R956 from 374 ohm to 200 ohm. change R955 from 1.2K ohm to 887 ohm. change R934 from 1.2K ohm to 620 ohm. change R939, R941 from 1.2K ohm to 680 ohm.	0.6(X02)
127	28	ME	2012/05/21	COMPAL	ME request (DFX issue, cancel boss hole).	change JLVDS2 from JAE_FI-M56S1-R1500 to JAE_FI-M56S1-R1500-DT.	1.0(A00)
128	17	HW	2012/05/21	COMPAL	Create X76 BOM for 2nd source.	Main source is WINBOND, 2nd source is EON.	1.0(A00)
129	17	HW	2012/05/21	COMPAL	change to new manufacturing technology.	change p/n from W25Q64CVSSIG to W25Q64FVSSIG.	1.0(A00)
130	49	HW	2012/05/21	COMPAL	change Board ID to A00.	change R875 from 33K ohm to 8.2K ohm.	1.0(A00)
131	42,51	HW	2012/05/22	COMPAL	add WiGi_BT LED function.	add net name WiGi_BT_LED# on JMINI.46, and add R2207(No stuff).	1.0(A00)
132	7,16	HW	2012/05/31	COMPAL	Dalmore 12" warm/cold boot shutdown issue.	change main source from NXP to ON on U16, UC1, U634.	1.0(A00)
133	22	HW	2012/05/31	COMPAL	TAIYO EOL, change to TAI-TECH.	change part from SHI0110BJ0L to SHI0110BJ50 on LH8.	1.0(A00)
134	51	HW	2012/06/05	COMPAL	Meet LED brightness spec.	change R943 from 240 ohm to 510 ohm. change R956 from 200 ohm to 340 ohm. change R942 from 1.2K ohm to 806 ohm. change R955 from 887 ohm to 300 ohm. change R934 from 620 ohm to 680 ohm.	1.0(A00)

DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CON
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISIO
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONT
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.