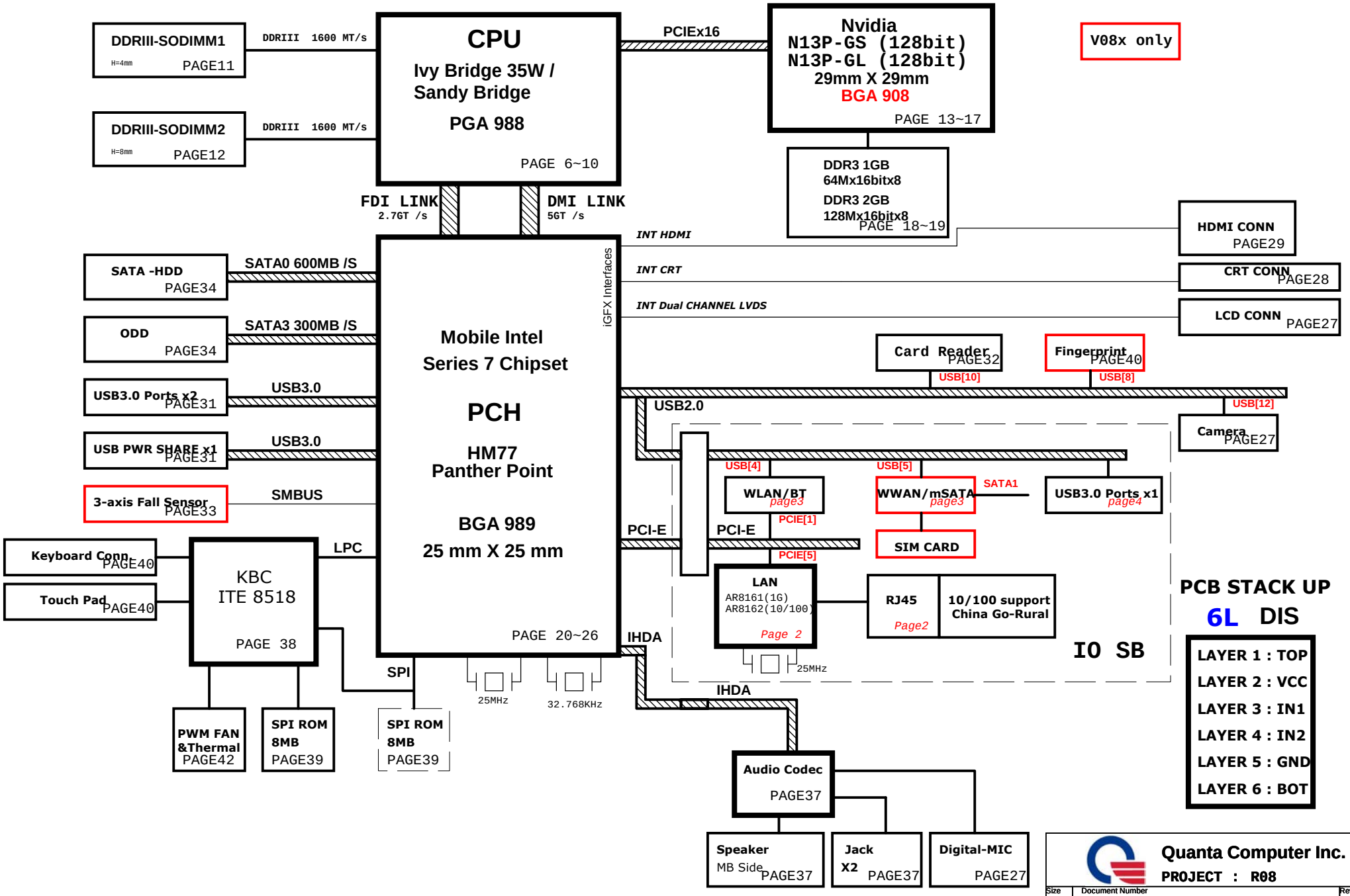
R08/V08 BLOCK DIAGRAM

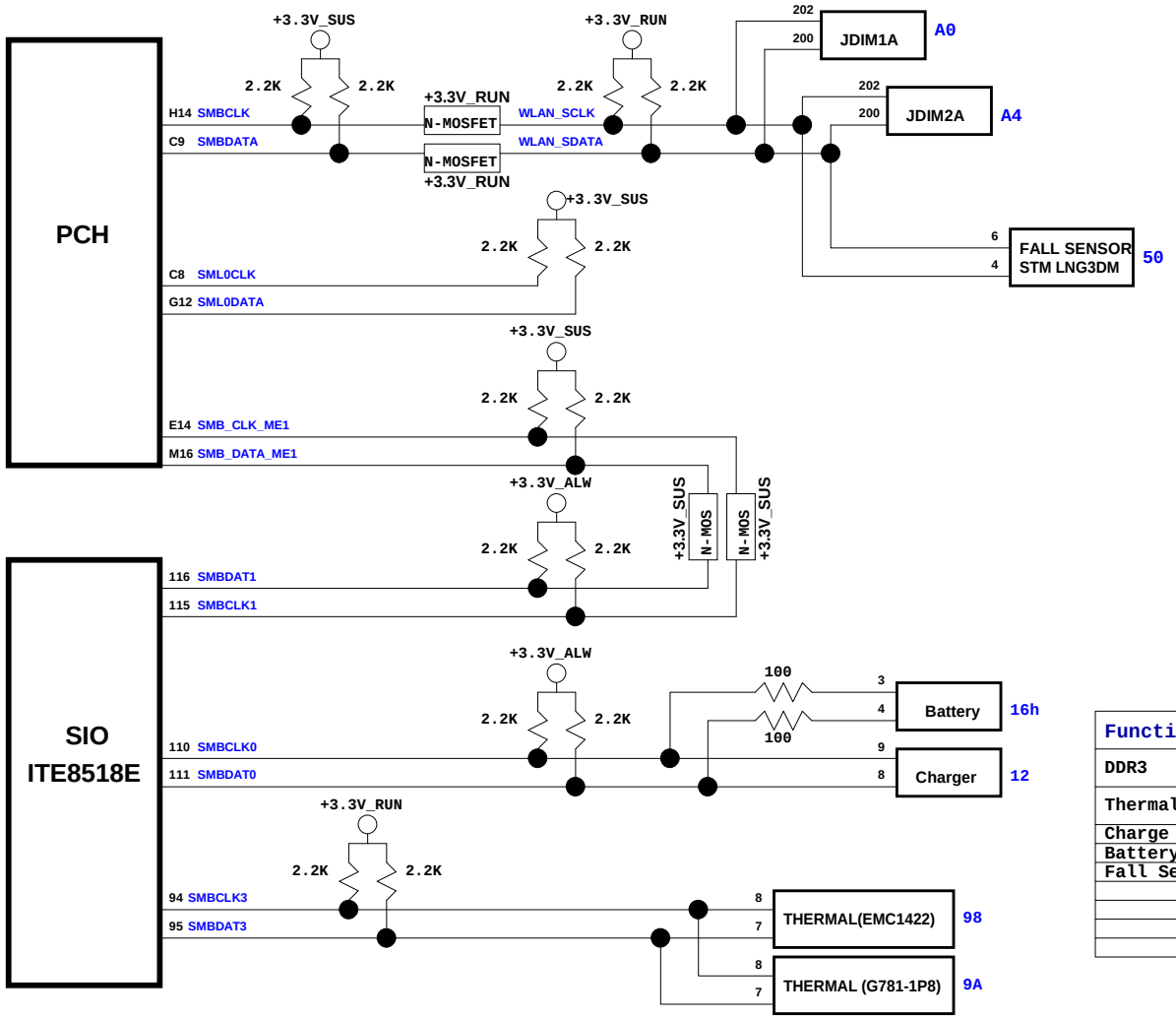


Quanta Computer Inc.

PROJECT : R08

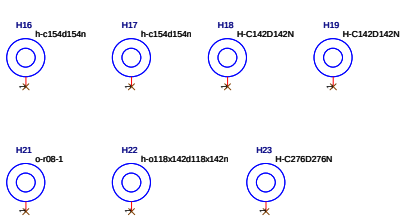
Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Monday, February 13, 2012 Sheet 1 of 55

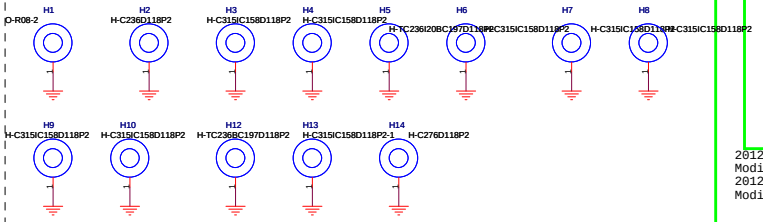


Function	IC	SMBus Address
DDR3	JDIM1A JDIM2A	A0h A4h
Thermal IC	EMC1422	1001100xb (98h)
	G781-1P8	1001101xb (9Ah)
Charge IC	BQ24707ARGRR	0b0001001x (0x12h)
Battery	Battery	16h
Fall Sensor	STM LNG3DM	01010000 (50h)

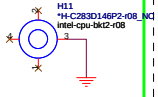
SCREW PAD



MB

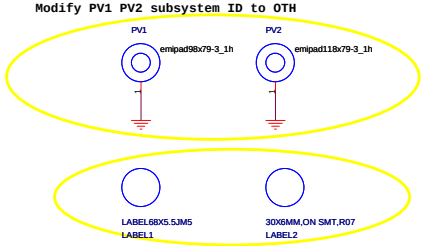


For CPU Use



20120206
Modify H11 pin1,2,3,4 no connect to GND
20120209
Modify H11 pin3 connect to GND

20120204
Modify PV1 PV2 subsystem ID to OTH



20120204
Add two label PN HCR07003010 and HCJM5004013

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	SMB/SCREW PAD	1A

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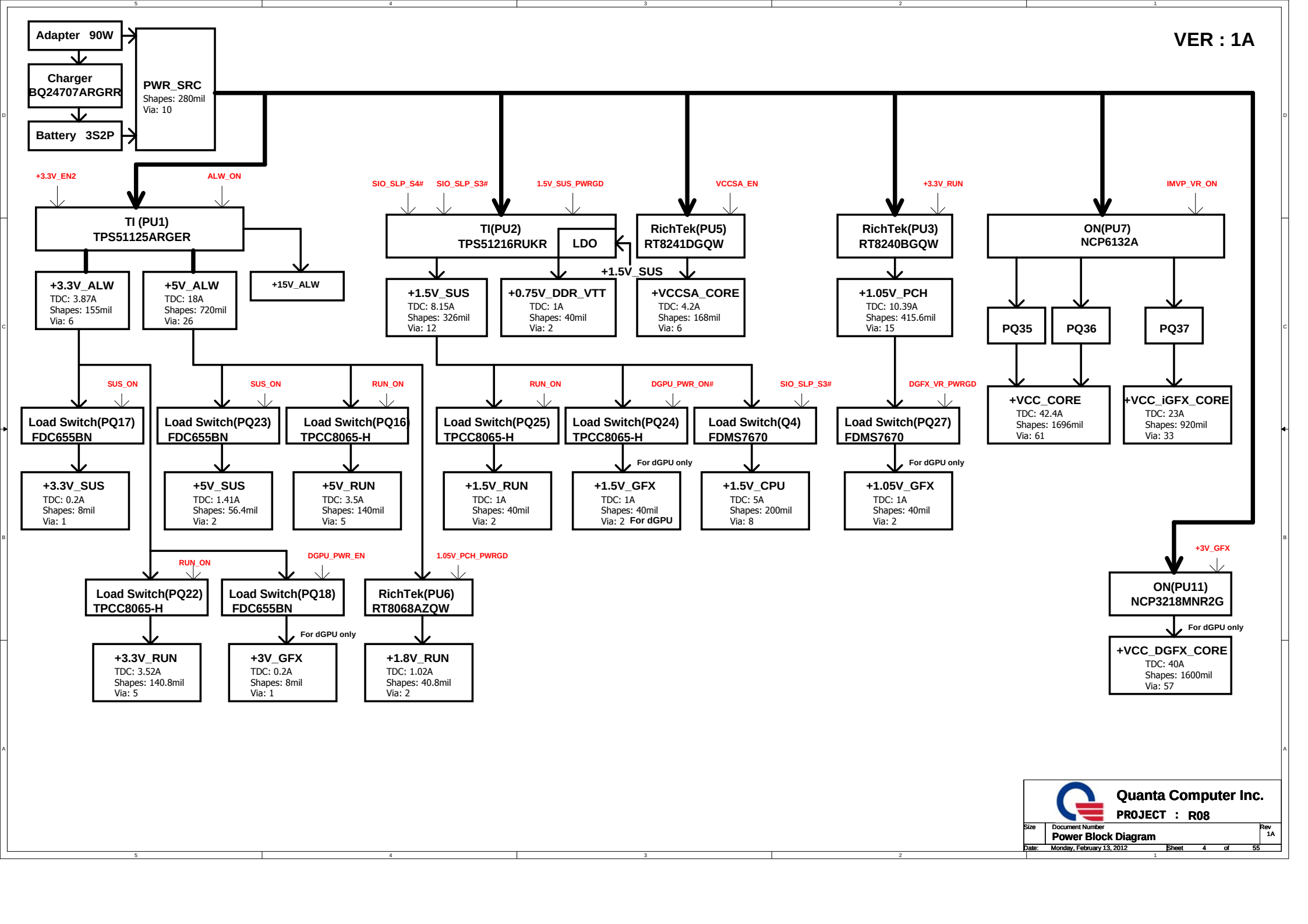
USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0/eSATA/ Power share/ debug port)
USB2	External port#3 (USB3.0)
USB3	External port#4 (USB3.0)
USB4	MiniCard 1 (WLAN/BT)
USB5	MiniCard 2 (WWAN/WiMAX)
USB6	X(FOR HM77)
USB7	X(FOR HM77)
USB8	Fingerprint
USB9	Touch panel (NC, for debug)
USB10	Card Reader
USB11	Express Card (NC)
USB12	Camera
USB13	NC

SATA Master	Port Assignment
SATA0	HDD
SATA1	mSATA
SATA2	NC
SATA3	ODD
SATA4	eSATA (NC)
SATA5	NC

PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	WWAN (NC)
PCIE 3	Card reader (NC)
PCIE 4	NC
PCIE 5	LAN
PCIE 6	Express card (NC)
PCIE 7	NC
PCIE 8	NC


VER : 1A
Adapter 90W
Charger BQ24707ARGRR
Battery 3S2P
PWR_SRC
Shapes: 280mil
Via: 10
+3.3V_EN2
ALW_ON
TI (PU1)
TPS51125ARGER
+3.3V_ALW
TDC: 3.87A
Shapes: 155mil
Via: 6
+5V_ALW
TDC: 18A
Shapes: 720mil
Via: 26
+15V_ALW
SIO_SLP_S4#
SIO_SLP_S3#
1.5V_SUS_PWRGD
TI(PU2)
TPS51216RUKR
LDO
+1.5V_SUS
TDC: 8.15A
Shapes: 326mil
Via: 12
+0.75V_DDR_VTT
TDC: 1A
Shapes: 40mil
Via: 2
VCCSA_EN
RichTek(PU5)
RT8241DGQW
+VCCSA_CORE
TDC: 4.2A
Shapes: 168mil
Via: 6
+3.3V_RUN
RichTek(PU3)
RT8240BGQW
+1.05V_PCH
TDC: 10.39A
Shapes: 415.6mil
Via: 15
IMVP_VR_ON
ON(PU7)
NCP6132A
PQ35
PQ36
PQ37
+VCC_CORE
TDC: 42.4A
Shapes: 1696mil
Via: 61
+VCC_iGFX_CORE
TDC: 23A
Shapes: 920mil
Via: 33
SUS_ON
Load Switch(PQ17)
FDC655BN
+3.3V_SUS
TDC: 0.2A
Shapes: 8mil
Via: 1
SUS_ON
Load Switch(PQ23)
FDC655BN
+5V_SUS
TDC: 1.41A
Shapes: 56.4mil
Via: 2
RUN_ON
Load Switch(PQ16)
TPCC8065-H
+5V_RUN
TDC: 3.5A
Shapes: 140mil
Via: 5
RUN_ON
Load Switch(PQ25)
TPCC8065-H
+1.5V_RUN
TDC: 1A
Shapes: 40mil
Via: 2
DGPU_PWR_ON#
Load Switch(PQ24)
TPCC8065-H
For dGPU only
+1.5V_GFX
TDC: 1A
Shapes: 40mil
Via: 2 For dGPU
SIO_SLP_S3#
Load Switch(Q4)
FDMS7670
+1.5V_CPU
TDC: 5A
Shapes: 200mil
Via: 8
DGFX_VR_PWRGD
Load Switch(PQ27)
FDMS7670
For dGPU only
+1.05V_GFX
TDC: 1A
Shapes: 40mil
Via: 2
RUN_ON
Load Switch(PQ22)
TPCC8065-H
+3.3V_RUN
TDC: 3.52A
Shapes: 140.8mil
Via: 5
DGPU_PWR_EN
Load Switch(PQ18)
FDC655BN
For dGPU only
+3V_GFX
TDC: 0.2A
Shapes: 8mil
Via: 1
1.05V_PCH_PWRGD
RichTek(PU6)
RT8068AZQW
+1.8V_RUN
TDC: 1.02A
Shapes: 40.8mil
Via: 2
+3V_GFX
ON(PU11)
NCP3218MNR2G
For dGPU only
+VCC_DGFX_CORE
TDC: 40A
Shapes: 1600mil
Via: 57
Quanta Computer Inc.
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Document Number
Power Block Diagram
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1A
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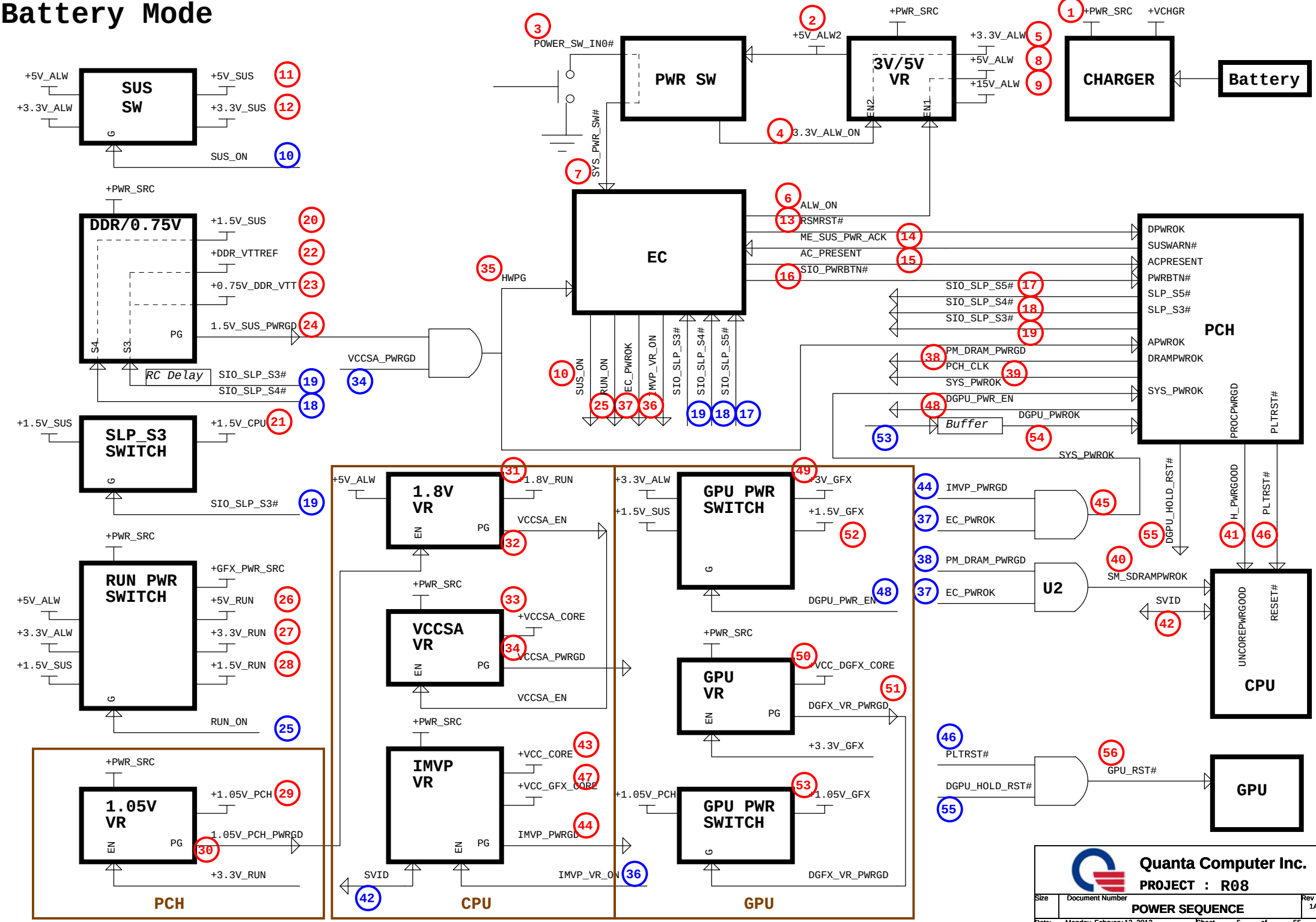
Battery Mode



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Size	Document Number	Rev
	POWER SEQUENCE	1A

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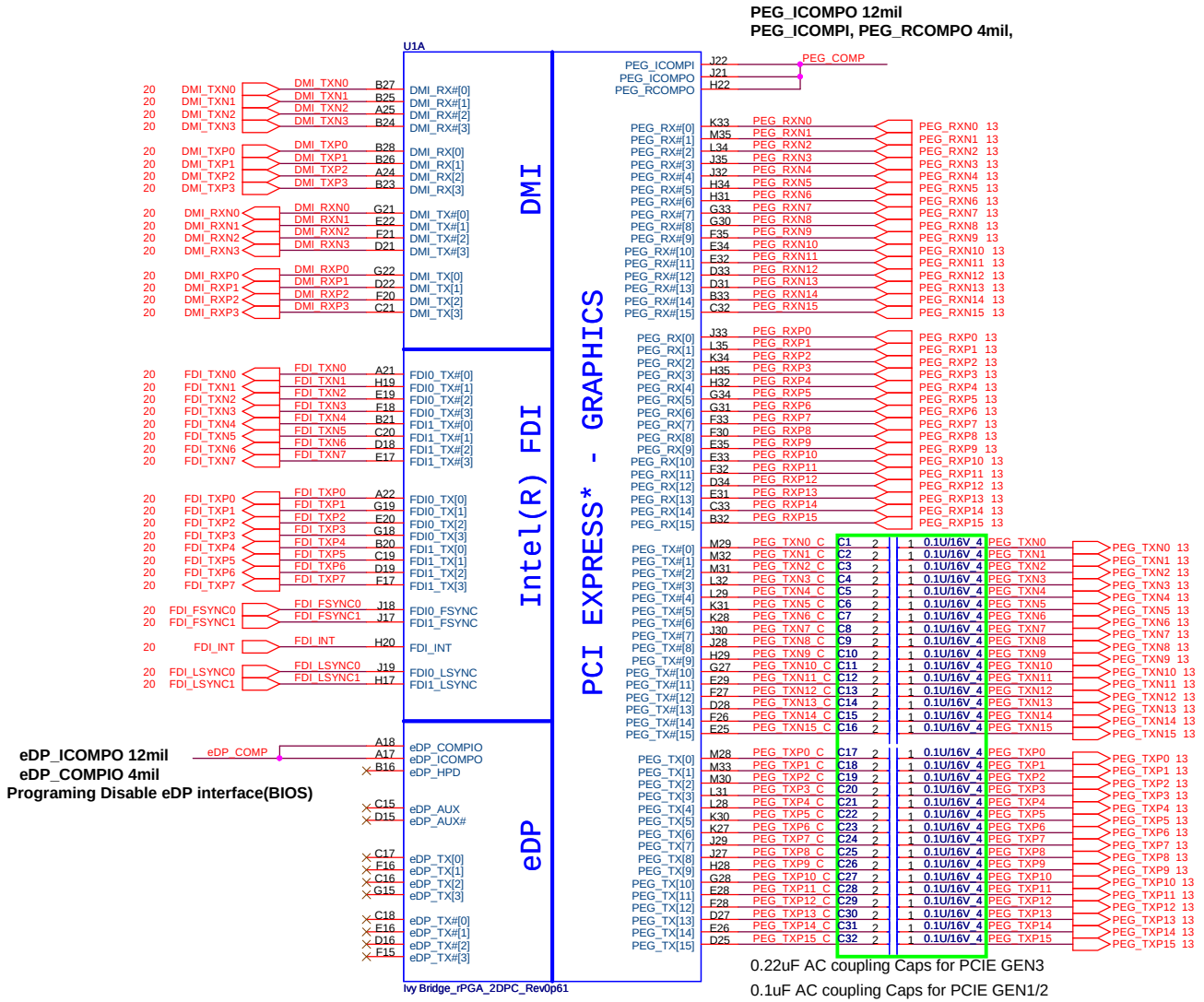
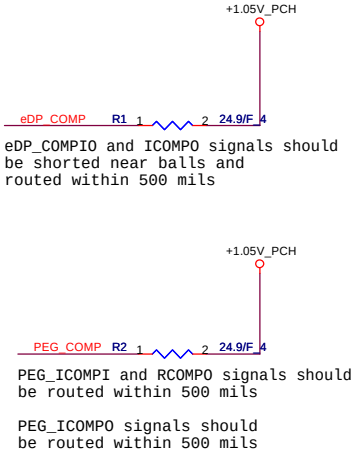
Ivy Bridge Processor (RESERVED, CFG)



DP & PEG Compensation



eDP Hot-plug (Disable)

CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

VGA(U3)	AC coupling Cap	PN	TX location	RX location(page13)
N13P-GL	0.1uF	CH4103K1B08	C1~C32	C144 C145 C147 C149 C150 C152 C154 C156 C157 C158 C159 C160 C161 C162 C163 C164 C165 C166 C167 C168 C169 C171 C173 C175 C176 C177 C178 C179 C180 C182 C184 C185
N13P-GS	0.22uF	CH4223K1B00	C1~C32	C144 C145 C147 C149 C150 C152 C154 C156 C157 C158 C159 C160 C161 C162 C163 C164 C165 C166 C167 C168 C169 C171 C173 C175 C176 C177 C178 C179 C180 C182 C184 C185

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	Ivy Bridge 1/5	1A

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Ivy Bridge Processor (CLK,MISC,JTAG)

U1B

SNB_IVB# N.A at SNB EDS #27637 0.7v1

23 H_SNB_IVB# — H_SNB_IVB# — C26 PROC_SELECT#

38 H_CPUDET# — H_CPUDET# — AN34 SKTOCC#

MISC

TP1 — CATERR# — AL33 CATERR#

38 PECI_EC — PECI_EC — R6 43_4 — PECI_EC_R — AN33 PECI

38,52,54 IMVP7_PROCHOT# — IMVP7_PROCHOT# — R7 56_4 — H_PROCHOT# — AL32 PROCHOT#

25 PM_THRMTRIP# — PM_THRMTRIP# — AN32 THERMTRIP#

THERMAL

Over 130 degree C will drive low

20 H_PM_SYNC — H_PM_SYNC — AM34 PM_SYNC

25 H_PWRGOOD — H_PWRGOOD — AP33 UNCOREPWRGOOD

10K_4 R17

SM_DRAMPWROK — V8 SM_DRAMPWROK

13,23,35,38 PLTRST# — PLTRST# — R19 1.5K/F_4 — CPU_PLTRST#_R — AR33 RESET#

R20 750/F_4

PWR MANAGEMENT

Ivy Bridge_rPGA_2DPC_Rev0p61

Intel spec VinH min =VCCIO X 0.7

CLOCKS

BCLK A28 — CLK_CPU_BCLKP — CLK_CPU_BCLKP 24

BCLK# A27 — CLK_CPU_BCLKN — CLK_CPU_BCLKN 24

DPLL_REF_CLK A16 — CLK_DP_P_R — R4 1K_4

DPLL_REF_CLK# A15 — CLK_DP_N_R — R5 1K_4 — +1.05V_PCH

For eDP

DDR3 MISC

SM_DRAMRST# — R8 — CPU_DRAMRST#

SM_RCOMP[0] AK1 — SM_RCOMP_0 — R8 140/F_4

SM_RCOMP[1] A5 — SM_RCOMP_1 — R9 25.5/F_4

SM_RCOMP[2] A4 — SM_RCOMP_2 — R10 200/F_4

SM_RCOMP_0, SM_RCOMP_1 20mil / SM_RCOMP_2 15mil.

JTAG & BPM

PRDY# AP29

PREQ# AP27

TCK AR26 — XDP_TCLK — TP28

TMS AR27 — XDP_TMS — TP37

TRST# AP30 — XDP_TRST# — TP38

TDI AR28 — XDP_TDI — TP41

TDO AP26 — XDP_TDO — TP42

DBR# AL35 — XDP_DBRST# — R18 1K_4 — +3.3V_RUN

BPM#[0] AT28

BPM#[1] AR29

BPM#[2] AR30

BPM#[3] AT30

BPM#[4] AP32

BPM#[5] AR31

BPM#[6] AT31

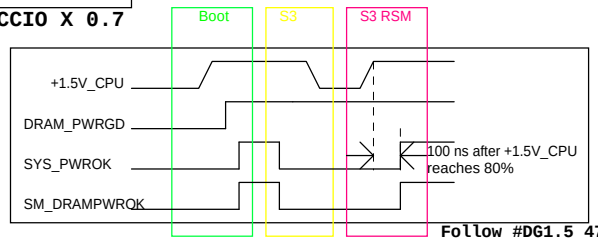
BPM#[7] AR32

+1.05V_PCH

IMVP7_PROCHOT# — R14 62_4

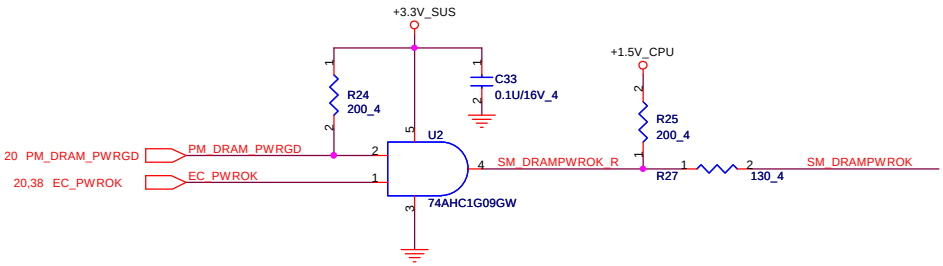
C854 *100P/50V_4_NC — H_PROCHOT#

C860 *100P/50V_4_NC — CPU_PLTRST#_R

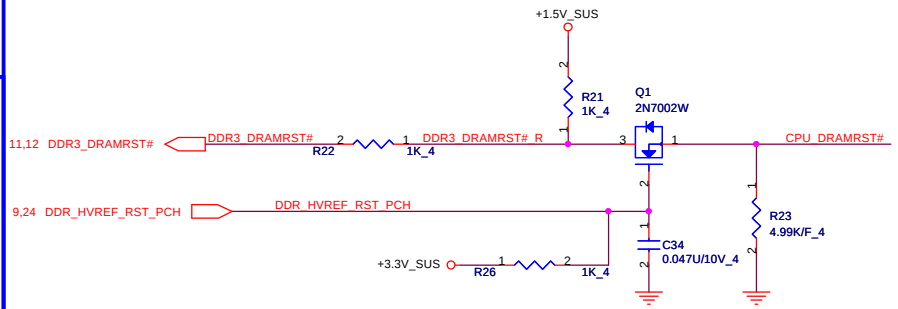


Follow #DG1.5 471984 P119

Follow #DG1.5 471984 P128
DDR Power Gating Topology



Follow #DG1.5 471984 P130
DRAMRST# Routing Illustration



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	Ivy Bridge 2/5	1A

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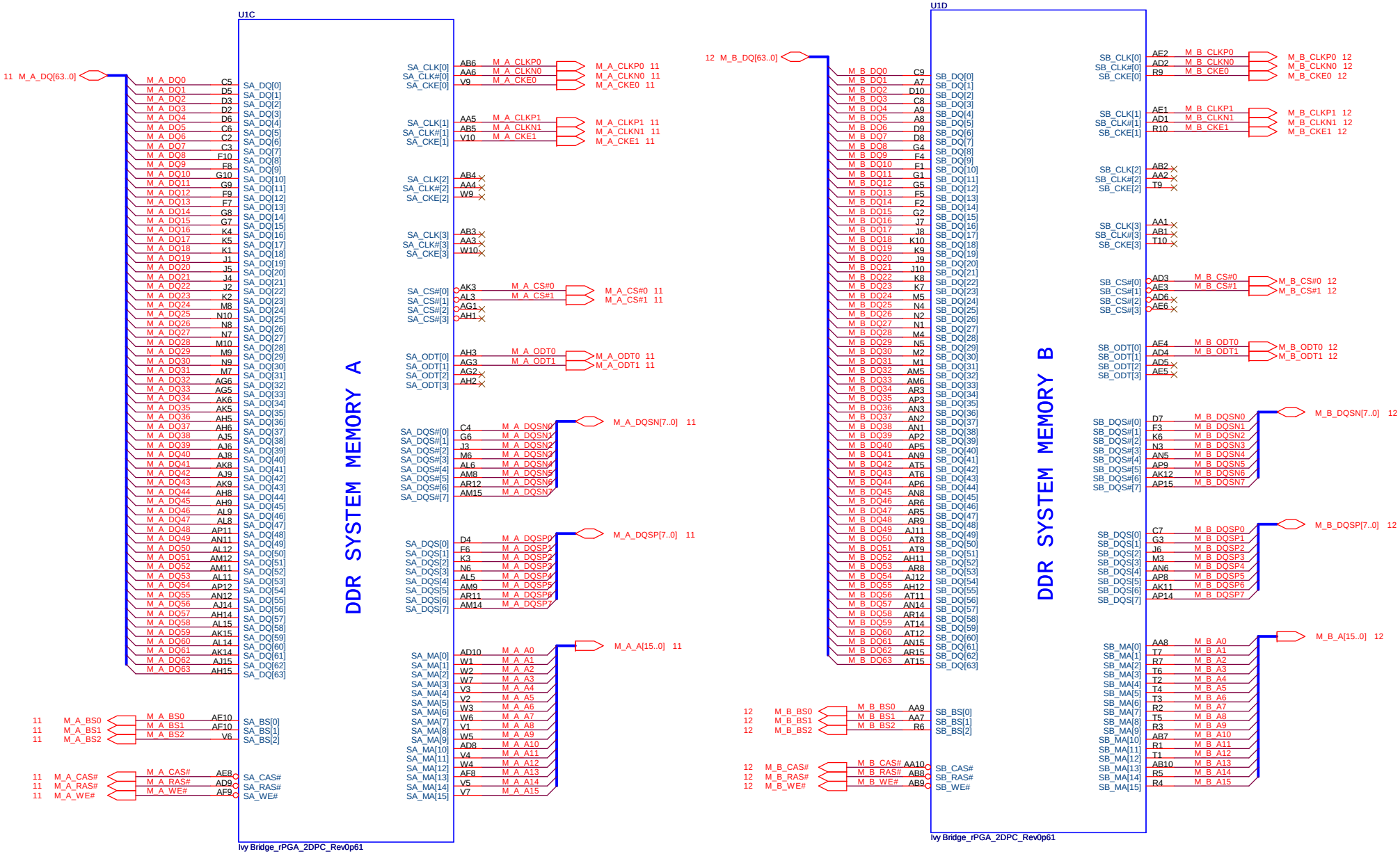
Ivy Bridge Processor (DDR3)



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	Ivy Bridge 3/5	1A

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Ivy Bridge Processor

CPU Core Power
SNB: 53A
IVY: 53A
10uF x 24

1.05V_PCH
SNB: 8.5A
IVY: 8.5A
10F x12

CPU VGT
SNB: 21.5A
IVY: 33A
10uF x 12

Ivy Bridge Processor (GRAPHIC POWER)

CPU CVCCPL
SNB: 1.2A
IVY: 1.2A
10uF x 1
1uF x 2

CPU MCH
SNB: 5A
IVY: 5A
10uF x 6

CPU SA
SNB: 6A
IVY: 6A
10uF x 3

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
VCC_SENSE / VSS_SENSE	100Ω	27-33Ω	<25 mils
VCCAXG_SENSE / VSSAXG_SENSE	100Ω		
VCCIO_SENSE / VSS_SENSE_VCCIO	10Ω	55Ω	
VCCSA	100Ω		

M3 VREF
Vgs=2.5V Rds=115m

S3 Power reduce
5A

Take care Q3 Vgs(MAX)=2.5

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

Place PU resistor close to CPU
SVID DATA

Place PU resistor close to CPU
SVID ALERT

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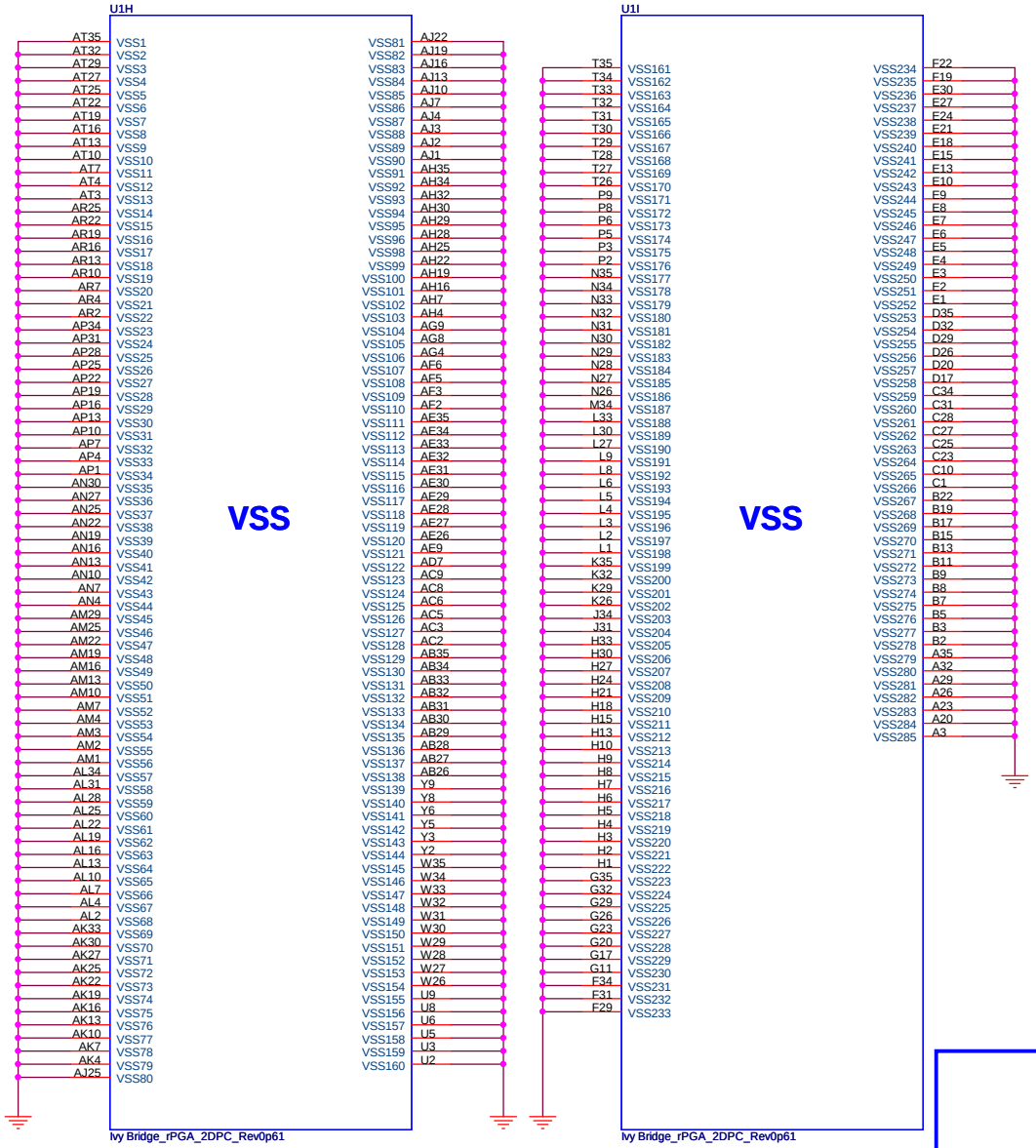
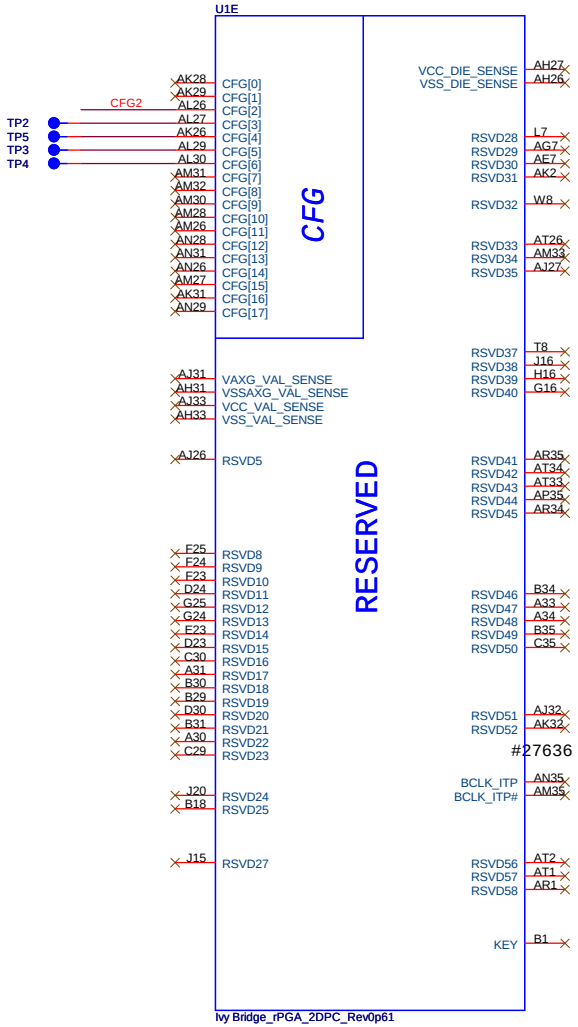
Ivy Bridge Processor (GND)



Ivy Bridge Processor (RESERVED, CFG)



#27636 SNB EDS0.7v1 no function.

For rPGA socket, RSVD59 pin should be left NC

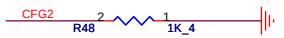
CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



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	Ivy Bridge 5/5	1A
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H=8mm,RVS

12

JDIM1A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0

SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30

8 M_A_A[15..0]

M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12/BC#
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15

8 M_A_BS0 → M_A_BS0 109 BA0
8 M_A_BS1 → M_A_BS1 108 BA1
8 M_A_BS2 → M_A_BS2 79 BA2
8 M_A_CS#0 → M_A_CS#0 114 S0#
8 M_A_CS#1 → M_A_CS#1 121 S1#
8 M_A_CLKP0 → M_A_CLKP0 101 CK0
8 M_A_CLKN0 → M_A_CLKN0 103 CK0#
8 M_A_CLKP1 → M_A_CLKP1 102 CK1
8 M_A_CLKN1 → M_A_CLKN1 104 CK1#
8 M_A_CKE0 → M_A_CKE0 73 CKE0
8 M_A_CKE1 → M_A_CKE1 74 CKE1
8 M_A_CAS# → M_A_CAS# 115 CAS#
8 M_A_RAS# → M_A_RAS# 110 RAS#
8 M_A_WE# → M_A_WE# 113 WE#

RP2 10KX2

DIMM0_SA0 197 SA0
DIMM0_SA1 201 SA1
12,24,33 WLAN_SCLK → WLAN_SCLK 202 SCL
12,24,33 WLAN_SDATA → WLAN_SDATA 200 SDA

8 M_A_ODT0 → M_A_ODT0 116 ODT0
8 M_A_ODT1 → M_A_ODT1 120 ODT1

11 DM0
28 DM1
46 DM2
63 DM3
136 DM4
153 DM5
170 DM6
187 DM7

8 M_A_DQSP[7..0]

M_A_DQSP1 12 DQS0
M_A_DQSP0 29 DQS1
M_A_DQSP2 47 DQS2
M_A_DQSP3 64 DQS3
M_A_DQSP4 137 DQS4
M_A_DQSP5 154 DQS5
M_A_DQSP6 171 DQS6
M_A_DQSP7 188 DQS7

8 M_A_DQSN[7..0]

M_A_DQSN1 10 DQS#0
M_A_DQSN0 27 DQS#1
M_A_DQSN2 45 DQS#2
M_A_DQSN3 62 DQS#3
M_A_DQSN4 135 DQS#4
M_A_DQSN5 152 DQS#5
M_A_DQSN6 169 DQS#6
M_A_DQSN7 186 DQS#7

M_A_DQ12 5 DQ0
M_A_DQ11 7 DQ1
M_A_DQ9 15 DQ2
M_A_DQ14 17 DQ3
M_A_DQ8 4 DQ4
M_A_DQ10 6 DQ5
M_A_DQ15 16 DQ6
M_A_DQ13 18 DQ7
M_A_DQ4 21 DQ8
M_A_DQ5 23 DQ9
M_A_DQ3 33 DQ10
M_A_DQ6 35 DQ11
M_A_DQ0 22 DQ12
M_A_DQ1 24 DQ13
M_A_DQ7 34 DQ14
M_A_DQ2 36 DQ15
M_A_DQ20 39 DQ16
M_A_DQ17 41 DQ17
M_A_DQ19 51 DQ18
M_A_DQ18 53 DQ19
M_A_DQ16 40 DQ20
M_A_DQ21 42 DQ21
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M_A_DQ29 57 DQ24
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M_A_DQ26 69 DQ27
M_A_DQ28 56 DQ28
M_A_DQ24 58 DQ29
M_A_DQ27 68 DQ30
M_A_DQ31 70 DQ31
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M_A_DQ43 157 DQ42
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M_A_DQ41 146 DQ44
M_A_DQ40 148 DQ45
M_A_DQ47 158 DQ46
M_A_DQ46 160 DQ47
M_A_DQ49 163 DQ48
M_A_DQ48 165 DQ49
M_A_DQ54 175 DQ50
M_A_DQ55 177 DQ51
M_A_DQ53 164 DQ52
M_A_DQ52 166 DQ53
M_A_DQ50 174 DQ54
M_A_DQ51 176 DQ55
M_A_DQ60 181 DQ56
M_A_DQ61 183 DQ57
M_A_DQ62 191 DQ58
M_A_DQ63 193 DQ59
M_A_DQ56 180 DQ60
M_A_DQ57 182 DQ61
M_A_DQ59 192 DQ62
M_A_DQ58 194 DQ63

M_A_DQ[63..0] 8

S3 Power reduce

+0.75V_DDR_VTT
R50 22_4
Q7 2N7002W
PS_S3CNTRL → PS_S3CNTRL 9

Place these Caps near So-Dimm0.

+1.5V_SUS
C98 0.1U/16V_4
C99 0.1U/16V_4
C100 0.1U/16V_4
C101 0.1U/16V_4
C102 10U/6.3V_8
C103 10U/6.3V_8
C104 10U/6.3V_8
C105 10U/6.3V_8

+0.75V_DDR_VTT
C106 10U/6.3V_8
C107 1U/6.3V_4
C108 1U/6.3V_4
EC829 *1U/6.3V_4_NC
EC830 *1U/6.3V_4_NC

M1 VREF

+1.5V_SUS
+SMDDR_VREF_DQ0
R51 1K/F_4
R54 1K/F_4
C109 0.1U/16V_4
C110 1U/10V_6

+1.5V_SUS
+SMDDR_VREF_DIMM0
R52 1K/F_4
R55 1K/F_4
C111 0.1U/16V_4
C112 1U/10V_6

20120213
Change C110 C112 to 1U

9 SMDDR_VREF_DQ0_M3 → SMDDR_VREF_DQ0_M3 R53 *0_4_NC

M3 VREF

12

JDIM1B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0

+1.5V_SUS

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

+3.3V_RUN
C97 0.1U/16V_4
VDDSPD 199

NC1 77
NC2 122
NCTEST 125

+3.3V_RUN → R49 *10K_4_NC → DDR3_DRAMRST# 198 EVENT#
7,12 DDR3_DRAMRST# → DDR3_DRAMRST# 30 RESET#

+SMDDR_VREF_DQ0 → VREF_DQ 1
+SMDDR_VREF_DIMM0 → VREF_CA 126

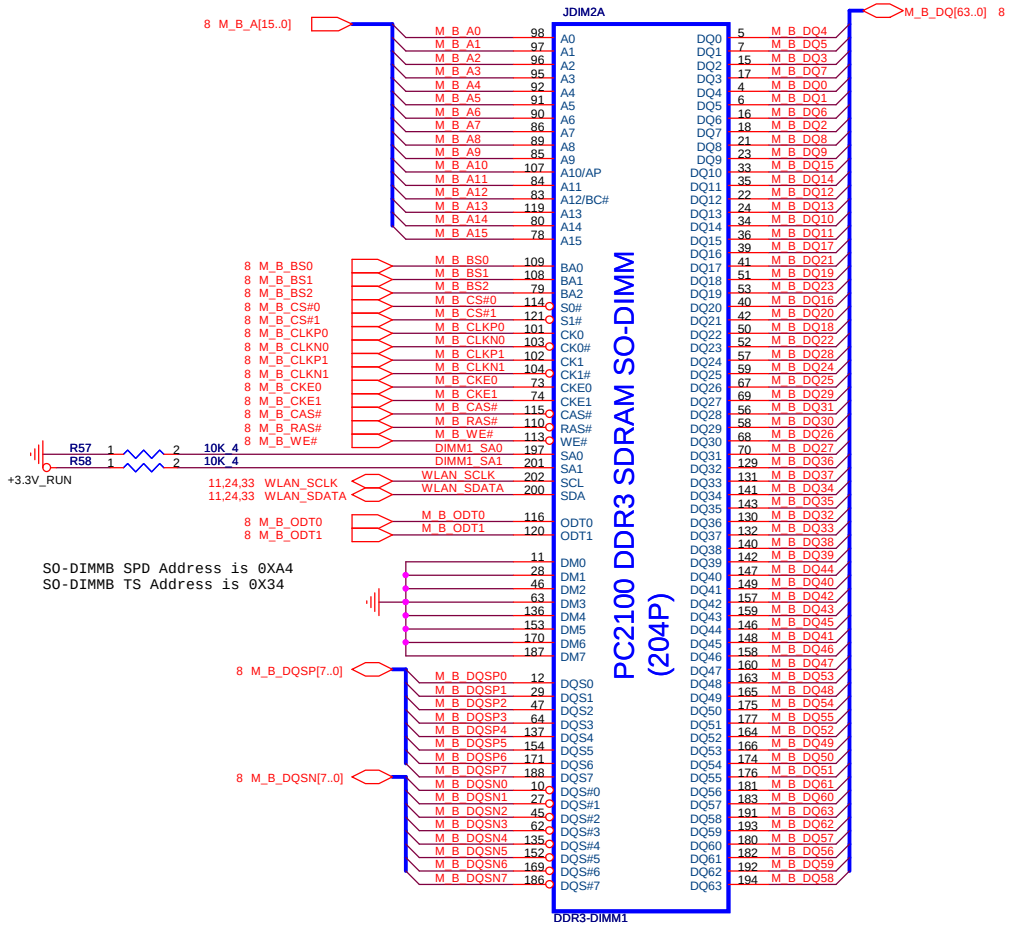
VSS1 2
VSS2 3
VSS3 8
VSS4 9
VSS5 13
VSS6 14
VSS7 19
VSS8 20
VSS9 25
VSS10 26
VSS11 31
VSS12 32
VSS13 37
VSS14 38
VSS15 43

VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 172
VSS44 173
VSS45 178
VSS46 179
VSS47 184
VSS48 185
VSS49 189
VSS50 190
VSS51 195
VSS52 196

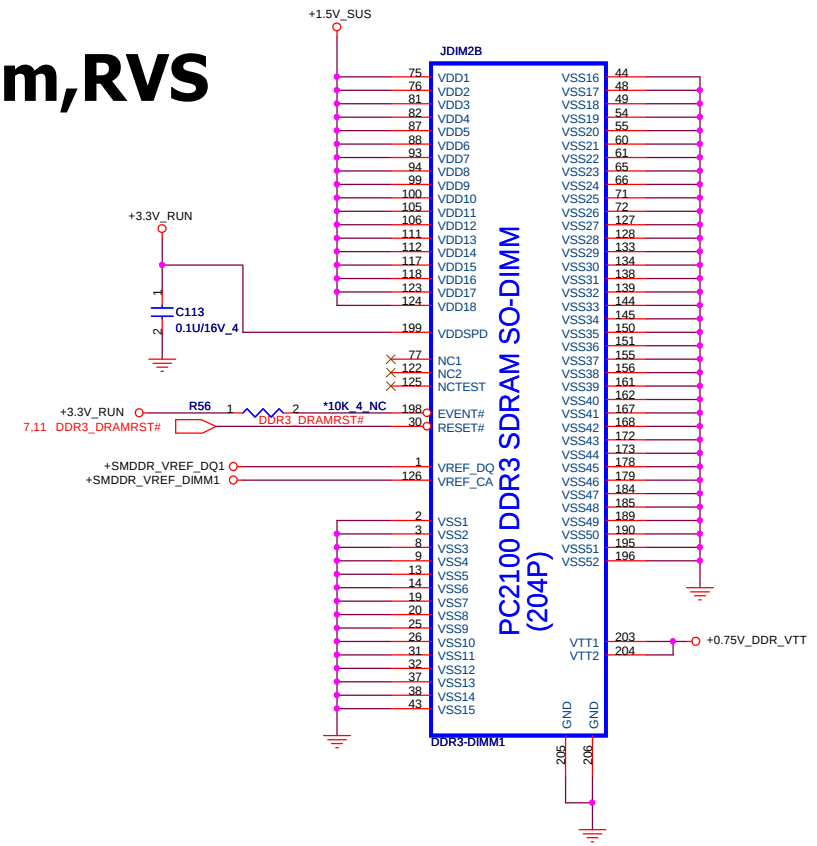
VTT1 203
VTT2 204
+0.75V_DDR_VTT → +0.75V_DDR_VTT

GND 205
GND 206

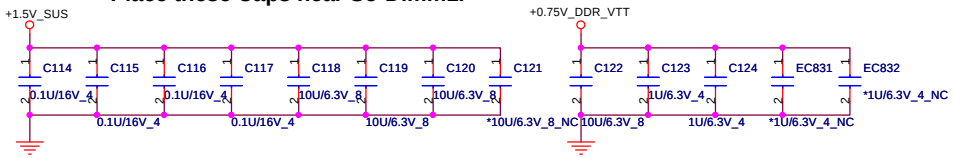
Quanta Computer Inc.		
PROJECT : R08		
Size	Document Number: DDR3 DIMM-0	Rev: 1A
Date: Monday, February 13, 2012	Sheet 11 of 55	



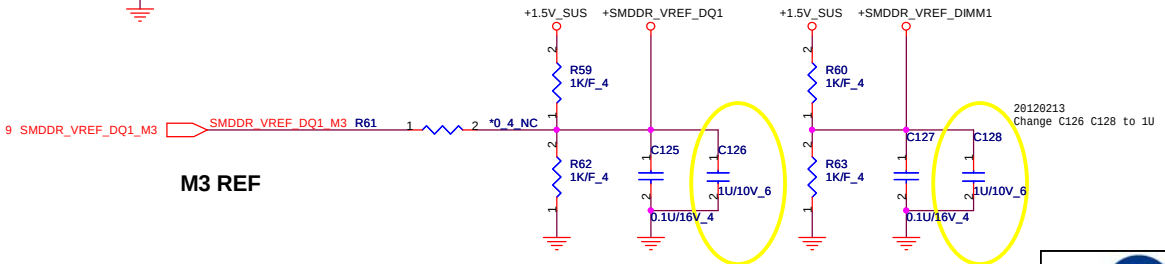
H=4mm,RVS



Place these Caps near So-Dimm1.



M1 VREF



M3 REF

Quanta Computer Inc.			
PROJECT : R08			
Size	Document Number		Rev
	DDR3 DIMM-1		1A
Date: Monday, February 13, 2012		Sheet 12 of 55	

20120203
Change U3 to AJ0N13P0T02(N13P-GL)
20120204
Change U3 to AJ0N13P0T49(WINCON)

PEX_IOVDD+PEX_IOVDDQ >3.3A

~ 1000mA

2300mA

0.1u *4 under GPU
Others Near GPU

0.1u under GPU
Others Near GPU

12~16 mils width

120mA

210mA 12~16 mils width

0.1u under GPU
Others Near GPU

U3A
N13P-GL-A1

GB4-128

PCI EXPRESS

0.22uF AC coupling Caps for PCIE GEN3
0.1uF AC coupling Caps for PCIE GEN1/2

GPU all PWROK

Q9: H(sat), L(cut-off)

20120203
Change C144 C145 C147 C149 C150
C152 C154 C156 C157 C158
C159 C160 C161 C162 C163
C164 C165 C166 C167 C168
C169 C171 C173 C175 C176
C177 C178 C179 C180 C182
C184 C185 to 0.1U/16V_4(CH4103K1B08)

PU in PCH

Power up sequence

VDD33
+3V_GFX
IFP(AB)_IOVDD
+1.8V_GFX
NVVDD
+VCC_DGFX_CORE
FBVDDQ
+1.5V_GFX
PEX_VDD
+1.05V_GFX
IFP(CDEF)_IOVDD
+1.05V_GFX
t>0

NB9M: VGACORE +0.90V (Normal) , +1.09V

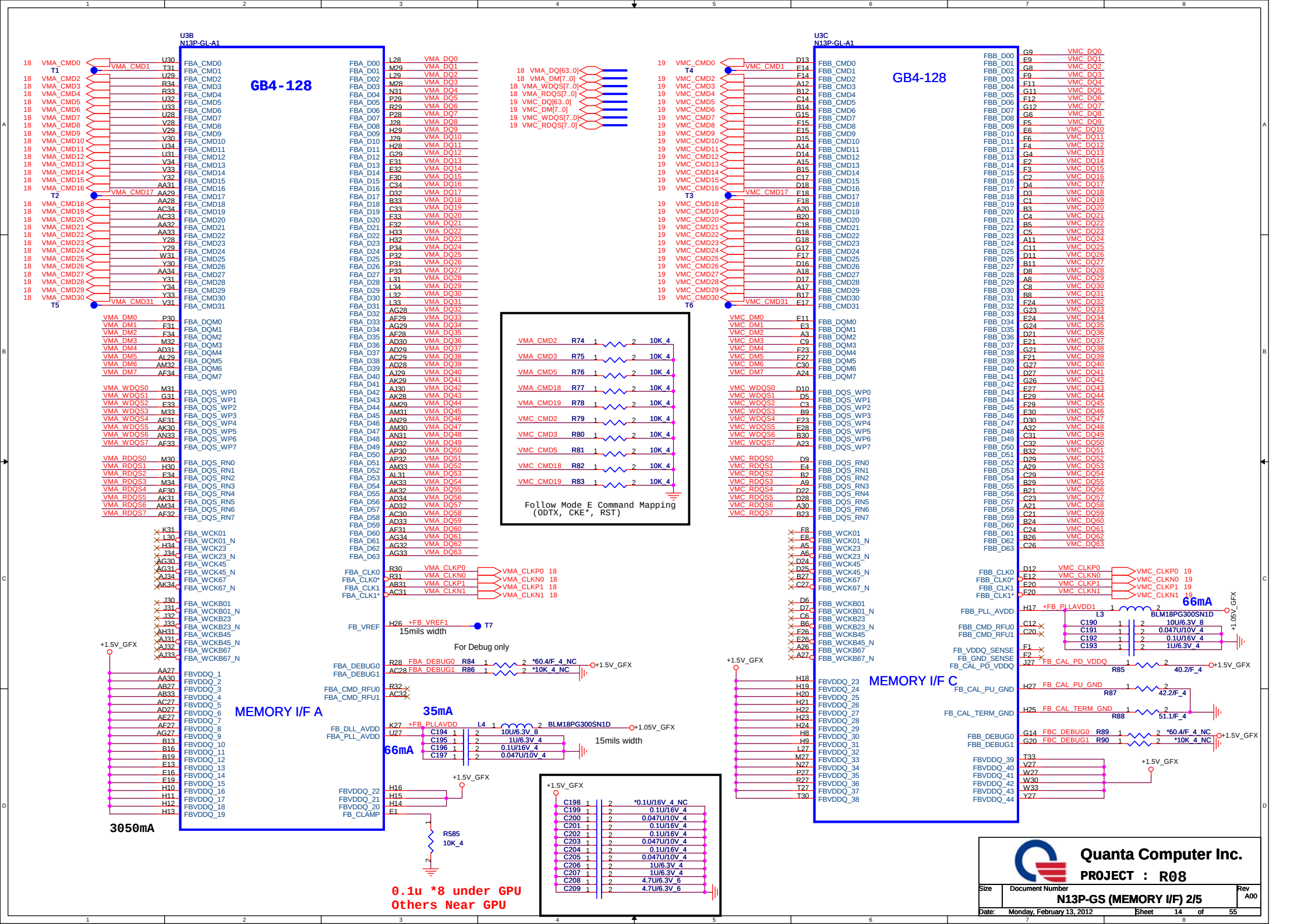
NVVDD Maximum Settling Time

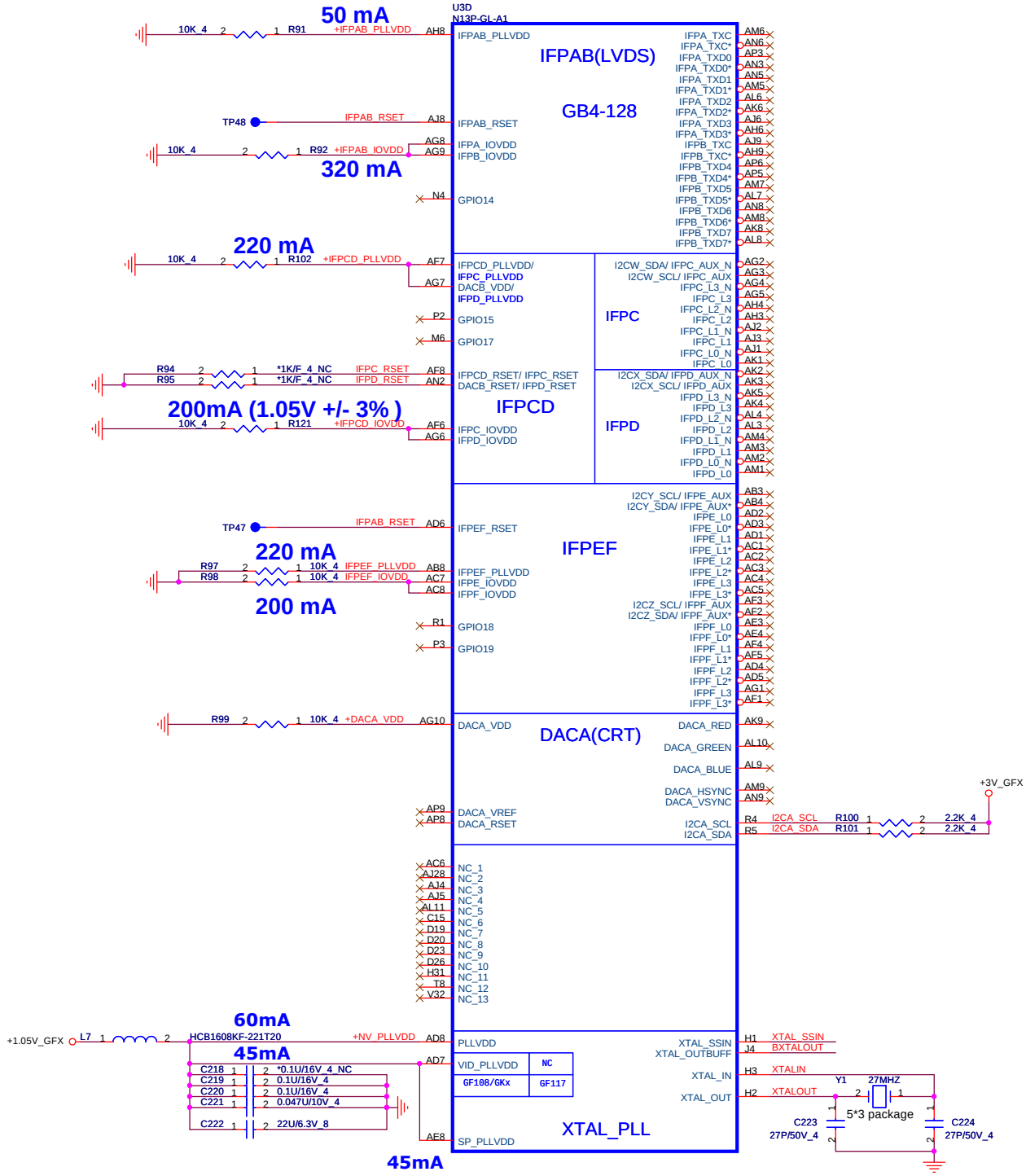
NVVDD
GPIO
tsNVVDD<100us

PEX_RST timing

I/O 3.3V
PEX_RST
Trise >= 1uS
Tfail <=500nS

Quanta Computer Inc.	PROJECT : R08		
Size	Document Number	N13P-GS (PCIE I/F) 1/5	Rev A00
Date: Monday, February 13, 2012	Sheet 13 of 55		


U3B
N13P-GL-A1
GB4-128
MEMORY I/F A
3050mA
35mA
66mA
U3C
N13P-GL-A1
GB4-128
MEMORY I/F C
66mA
Follow Mode E Command Mapping
(ODTX, CKE*, RST)
0.1u *8 under GPU
Others Near GPU
Quanta Computer Inc.
PROJECT : R08
N13P-GS (MEMORY I/F) 2/5
Monday, February 13, 2012



Quanta Computer Inc.		
PROJECT : R08		
Size	Document Number: N13P-GS (DISPLAY) 3/5	Rev: A00
Date: Monday, February 13, 2012	Sheet 15 of 55	

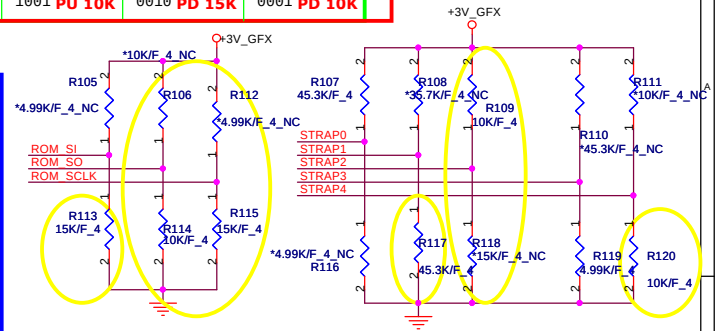
N13P-GL (AJ0N13P0T02)
N13P-GS for Turbo (AJ001070T00)

CHIP	PCI_DEVID:	STRAP2	ROM_SCLK	ROM_SO
N13P-GS	0x0FD2(QS)	0010 PD 15K	1000 PU 5K	1001 PU 10K
N13P-LP	0x0FD3	0011 PD 20K	1000 PU 5K	
N13M-GS	0x1142	0010 PD 15K	0000 PD 5K	
N13P-GL	0x0DE9	1001 PU 10K	0010 PD 15K	0001 PD 10K

Strap Bit		Description
USER[3:0]	1111	EDID is used
3GIO_PADCFG [3:0]	0110	Notebook Default
PCI_DEVID[5:0]	D2	PCI_Device_ID
SORx_EXPOSED [3:0]	0000	Audio capability on each display port Not in use
DP_PLL_VDD33V	1	Default
PCIE_MAX_SPEED	1	PCIE Gen2/3 capable
PCI_SPEED_CHANGE_GEN3	0	Default
RAMCFG[3:0]	0010	Default Hynix1G
PEX_PLL_EN_TERM	0	PCIE PLL termination disable (Default)
SUB_VENDOR	0	No vedio BIOS ROM
FB[1:0]	01	Frame Buffer size Reserve
SMB_ALT_ADDR	0	Default (1GPU)
VGA_DEVICE	1	Default (non 3D)

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111



10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
24.9K/F_4: CS32492FB16 [RES CHIP 24.9K 1/16W +-1%(0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0010
STRAP4	RESERVED	PCI_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	0001
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1001
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0111
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

Default: Hynix VRAM 2G (0110)

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Quanta P/N	Vendor P/N	ROM_SI
0000		Reserved			PD 5K
0001	Reserve	Reserve	Reserve	Reserve	PD 10K
0010	DDR3 64Mx16, 900MHz	Hynix	AKD5LZWTW07	H5TQ1G63DFR-11C	PD 15K
0011	DDR3 64Mx16, 900MHz (G-die)	Samsung	AKD5EGGT509	K4W1G1646G-BC11	PD 20K
0110	DDR3 128Mx16, 900MHz	Hynix	AKD5MGWTW06	H5TQ2G63BFR-11C	PD 35K
0111	DDR3 128Mx16, 900MHz	Samsung	AKD5MGWT507	K4W2G1646C-HC11	PD 45K

U3E
N13P-GL-A1

GB4-128

MISC1
(GPIOS,JTAG,THERM,I2C)

MISC2(ROM)

42 VGA_THERMDN → K4 THERMDN
42 VGA_THERMDP → K3 THERMDP

T8 JTAG_TCK AM10 JTAG_TCK
T9 JTAG_TMS AP11 JTAG_TMS
T10 JTAG_TDI AM11 JTAG_TDI
T11 JTAG_TDO AP12 JTAG_TDO
T12 JTAG_TRST# AN11 JTAG_TRST*

RP31 2.2KX2 I2CS_SCL T4 I2CS_SCL
RP31 2.2KX2 I2CS_SDA T3 I2CS_SDA
RP32 2.2KX2 EXT_EDIDCLK R2 I2CC_SCL
RP32 2.2KX2 EXT_EDIDDATA R3 I2CC_SDA
RP33 2.2KX2 I2CB_SCL_G R7 I2CB_SCL
RP33 2.2KX2 I2CB_SDA_G R6 I2CB_SDA
+3V_GFX

STRAP0 J2 STRAP0
STRAP1 J7 STRAP1
STRAP2 J6 STRAP2
STRAP3 J5 STRAP3
STRAP4 J3 STRAP4

R137 40.2K/F_4 STRAP_REF_GND J1 MULTI_STRAP_REF_GND

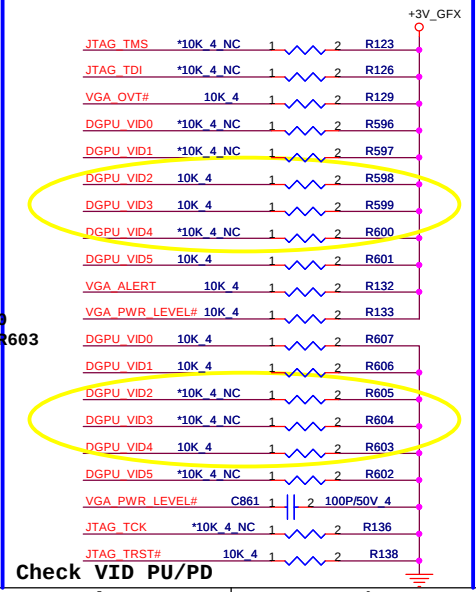
GPIO0 P6 DGPU_VID4 → DGPU_VID4 55
GPIO1 M3 DGPU_VID3 → DGPU_VID3 55
GPIO2 L6
GPIO3 P5
GPIO4 P7
GPIO5 L7 DGPU_VID1 → DGPU_VID1 55
GPIO6 M7 DGPU_VID2 → DGPU_VID2 55
GPIO7 N8
GPIO8 M1 VGA_OVT#
GPIO9 M2 VGA_ALERT
GPIO10 L1
GPIO11 M5 DGPU_VID0 → DGPU_VID0 55
GPIO12 N3 VGA_PWR_LEVEL# → VGA_PWR_LEVEL# 38,55
GPIO13 M4 DGPU_VID5 → DGPU_VID5 55
GPIO16 R8
GPIO20 P4
GPIO21 P1

ROM_CS* H6
ROM_SI H5 ROM_SI
ROM_SO H7 ROM_SO
ROM_SCLK H4 ROM_SCLK

BUFRST* L2
CEC L3

20120203
NC R605 R604 R600
Mount R598 R599 R603

	Output	VID0	VID1	VID2	VID3	VID4	VID5
N13P-GL	0.95V	0	0	1	1	0	1
N13P-GS	0.9V	0	0	0	0	1	1



Check VID PU/PD

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	NVVDD_VID4
1	IN	N/A	NVVDD_VID3
2	OUT	HIGH	NC
3	OUT	HIGH	NC
4	OUT	HIGH	NC
5	OUT	N/A	NVVDD_VID1
6	OUT	N/A	NVVDD_VID2
7	OUT	N/A	NC
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	NC
11	OUT	N/A	NVVDD VID0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	NVVDD VID5

Quanta Computer Inc.
PROJECT : R08

Size	Document Number	Rev
	N13P-GS (GPIO&STRAPS) 4/5	A00
Date: Monday, February 13, 2012	Sheet 16 of 55	

N13P-GS 50 A
N13P-LP 40 A

+VCC_DGFX_CORE

+VCC_DGFX_CORE

U3F
N13P-GL-A1

GB4-128
NVVDD

AA12	VDD_001	VDD_057	V18		
AA14	VDD_002	VDD_058	AB18		
AA16	VDD_003	VDD_059	V20		
AA19	VDD_004	VDD_060	V22		
AA21	VDD_005	VDD_061	W12		
AA23	VDD_006	VDD_062	W14		
AB13	VDD_007	VDD_063	W16		
AB15	VDD_008	VDD_064	W19		
AB17	VDD_009	VDD_065	W21		
AB20	VDD_010	VDD_066	W23		
AB22	VDD_011	VDD_067	Y13		
AC12	VDD_012	VDD_068	Y15		
AC14	VDD_013	VDD_069	Y17		
AC16	VDD_014	VDD_070	Y18		
AC19	VDD_015	VDD_071	Y20		
AC21	VDD_016	VDD_072	Y22		
AC23	VDD_017	XVDD_01	U1		
M12	VDD_018	XVDD_02	U2		
M14	VDD_019	XVDD_03	U3		
M16	VDD_020	XVDD_04	U4		
M19	VDD_021	XVDD_05	U5		
M21	VDD_022	XVDD_06	U6		
M23	VDD_023	XVDD_07	U7		
N13	VDD_024	XVDD_08	U8		
N15	VDD_025	XVDD_09	V1		
N17	VDD_026	XVDD_10	V2		
N18	VDD_027	XVDD_11	V3		
N20	VDD_028	XVDD_12	V4		
N22	VDD_029	XVDD_13	V5		
P12	VDD_030	XVDD_14	V6		
P14	VDD_031	XVDD_15	V7		
P16	VDD_032	XVDD_16	V8		
P19	VDD_033	XVDD_17	W2		
P21	VDD_034	XVDD_18	W3		
P23	VDD_035	XVDD_19	W4		
R13	VDD_036	XVDD_20	W5		
R15	VDD_037	XVDD_21	W7		
R17	VDD_038	XVDD_22	W8		
R18	VDD_039	XVDD_23	Y1		
R20	VDD_040	XVDD_24	Y2		
R22	VDD_041	XVDD_25	Y3		
T12	VDD_042	XVDD_26	Y4		
T14	VDD_043	XVDD_27	Y5		
T16	VDD_044	XVDD_28	Y6		
T19	VDD_045	XVDD_29	Y7		
T21	VDD_046	XVDD_30	Y8		
T23	VDD_047	XVDD_31	AA1		
U13	VDD_048	XVDD_32	AA2		
U15	VDD_049	XVDD_33	AA3		
U17	VDD_050	XVDD_34	AA4		
U18	VDD_051	XVDD_35	AA5		
U20	VDD_052	XVDD_36	AA6		
U22	VDD_053	XVDD_37	AA7		
V13	VDD_054	XVDD_38	AA8		
V15	VDD_055				
V17	VDD_056				

NVVDD Decoupling

+VCC_DGFX_CORE

PLACE UNDER BALLS

C225	1	2	0.01U/25V_4
C226	1	2	0.01U/25V_4
C227	1	2	0.01U/25V_4
C228	1	2	0.01U/25V_4
C229	1	2	0.01U/25V_4
C230	1	2	0.01U/25V_4
C231	1	2	0.01U/25V_4
C232	1	2	0.01U/25V_4
C233	1	2	0.022U/16V_4
C234	1	2	0.022U/16V_4
C235	1	2	0.022U/16V_4
C236	1	2	0.047U/10V_4
C237	1	2	0.047U/10V_4
C238	1	2	0.047U/10V_4
C239	1	2	0.1U/16V_4
C240	1	2	0.1U/16V_4
C241	1	2	0.22U/10V_6
C242	1	2	0.22U/10V_6
C243	1	2	0.22U/10V_6
C244	1	2	1U/6.3V_4

PLACE NEAR BALLS

C245	1	2	4.7U/6.3V_6
C246	1	2	10U/6.3V_8
C247	1	2	10U/6.3V_8
C248	1	2	22U/6.3V_8
C249	1	2	22U/6.3V_8

330uF*2 at power page

U3G
N13P-GL-A1

GB4-128
GROUND

A2	GND_1	GND_105	E22		
A33	GND_2	GND_104	E10		
AA13	GND_3	GND_103	D33		
AA15	GND_4	GND_106	E25		
AA17	GND_5	GND_107	E5		
AA18	GND_6	GND_108	E7		
AA20	GND_7	GND_109	F28		
AA22	GND_8	GND_110	F7		
AB12	GND_9	GND_111	G10		
AB14	GND_10	GND_112	G13		
AB16	GND_11	GND_113	G16		
AB19	GND_12	GND_114	G19		
AB2	GND_13	GND_115	G2		
AB21	GND_14	GND_116	G22		
AB23	GND_15	GND_117	G25		
AB28	GND_16	GND_118	G28		
AB30	GND_17	GND_119	G3		
AB32	GND_18	GND_120	G30		
AB5	GND_19	GND_121	G32		
AB7	GND_20	GND_122	G33		
AC13	GND_21	GND_123	G5		
AC15	GND_22	GND_124	G7		
AC17	GND_23	GND_125	K2		
AC18	GND_24	GND_126	K28		
AC20	GND_25	GND_127	K30		
AC22	GND_26	GND_128	K32		
AE2	GND_27	GND_129	K33		
AE28	GND_28	GND_130	K5		
AE30	GND_29	GND_131	K7		
AE32	GND_30	GND_132	M13		
AE33	GND_31	GND_133	M15		
AE5	GND_32	GND_134	M17		
AE7	GND_33	GND_135	M18		
AH10	GND_34	GND_136	M20		
AH13	GND_35	GND_137	M22		
AH16	GND_36	GND_138	N12		
AH19	GND_37	GND_139	N14		
AH2	GND_38	GND_140	N16		
AH22	GND_39	GND_141	N19		
AH24	GND_40	GND_142	N2		
AH28	GND_41	GND_143	N21		
AH29	GND_42	GND_144	N23		
AH30	GND_43	GND_145	N28		
AH32	GND_44	GND_146	N30		
AH33	GND_45	GND_147	N32		
AH5	GND_46	GND_148	N33		
AH7	GND_47	GND_149	N5		
AJ7	GND_48	GND_150	N7		
AK10	GND_49	GND_151	P13		
AK7	GND_50	GND_152	P15		
AL12	GND_51	GND_153	P17		
AL14	GND_52	GND_154	P18		
AL15	GND_53	GND_155	P20		
AL17	GND_54	GND_156	P22		
AL18	GND_55	GND_157	R12		
AL2	GND_56	GND_158	R14		
AL20	GND_57	GND_159	R16		
AL21	GND_58	GND_160	R19		
AL23	GND_59	GND_161	R21		
AL24	GND_60	GND_162	R23		
AL26	GND_61	GND_163	T13		
AL28	GND_62	GND_164	T15		
AL30	GND_63	GND_165	T17		
AL32	GND_64	GND_166	T18		
AL33	GND_65	GND_167	T2		
AL5	GND_66	GND_168	T20		
AM13	GND_67	GND_169	T22		
AM16	GND_68	GND_170	AG11		
AM19	GND_69	GND_171	T28		
AM22	GND_70	GND_172	T32		
AM25	GND_71	GND_173	T5		
AN1	GND_72	GND_174	T7		
AN10	GND_73	GND_175	U12		
AN13	GND_74	GND_176	U14		
AN16	GND_75	GND_177	U16		
AN19	GND_76	GND_178	U19		
AN22	GND_77	GND_179	U21		
AN25	GND_78	GND_180	U23		
AN30	GND_79	GND_181	V12		
AN34	GND_80	GND_182	V14		
AN4	GND_081	GND_183	V16		
AN7	GND_082	GND_184	V19		
AP2	GND_083	GND_185	V21		
AP33	GND_084	GND_186	V23		
B1	GND_085	GND_187	W13		
B10	GND_086	GND_188	W15		
B22	GND_087	GND_189	W17		
B25	GND_088	GND_190	W18		
B28	GND_089	GND_191	W20		
B31	GND_090	GND_192	W22		
B34	GND_091	GND_193	W28		
B4	GND_092	GND_194	Y12		
B7	GND_093	GND_195	Y14		
C10	GND_094	GND_196	Y16		
C13	GND_095	GND_197	Y19		
C19	GND_096	GND_198	Y21		
C22	GND_097	GND_199	Y23		
C25	GND_098	GND_200	AH11		
C28	GND_099				
C7	GND_100				
D2	GND_101	GND_201	C16		
D31	GND_102	GND_202	W32		

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	N13P-GS (POWER & GND) 5/5	A00

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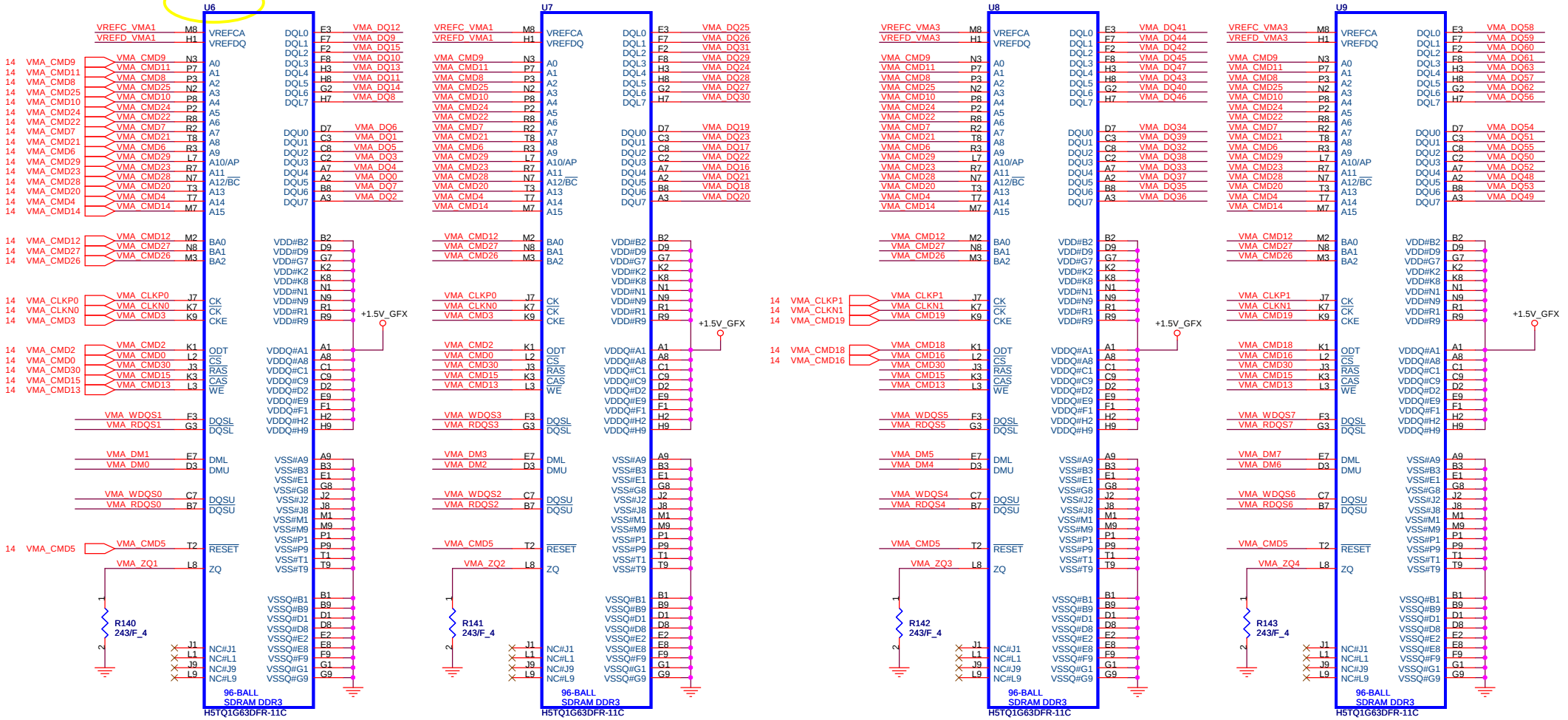
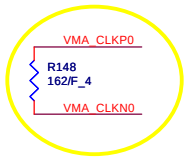
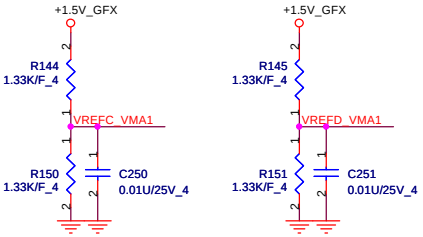
20120203
Change U6~U13 to AKD5LZWTW07 (hynix 1G)

CHANNEL A: 512MB/1024MB DDR3

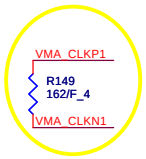
14 VMA_DQ[63..0]
14 VMA_DM[7..0]
14 VMA_WDQS[7..0]
14 VMA_RDQS[7..0]

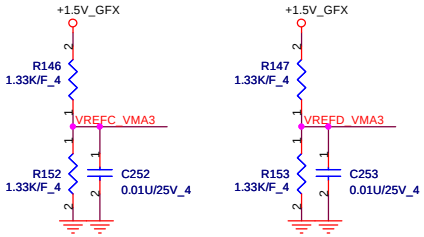


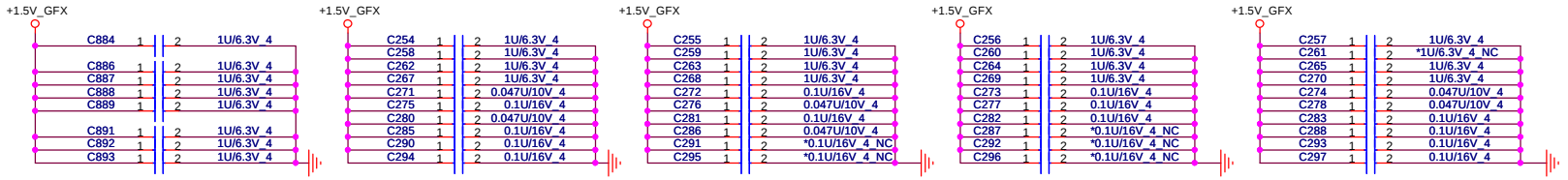




	R148 R149 R162 R163 (MCLK+/MCLK- termination)
N13P-GL	162/F_4 (CS11622FB15)
N13P-GS	80.6/F_4 (CS08062FB19)







Quanta Computer Inc.
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	N13P-GS VRAM-1(DDR3 BGA96)	A00
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CHANNEL B: 512MB/1024MB DDR3

14 VMC_DQ[63..0]
14 VMC_DM[7..0]
14 VMC_WDQS[7..0]
14 VMC_RDQS[7..0]

U10 / U11 / U12 / U13 — 96-BALL SDRAM DDR3 — H5TQ1G63DFR-11C

+1.5V_GFX

R154 243/F_4
R155 243/F_4
R156 243/F_4
R157 243/F_4

VMC_CLKP0 — R162 162/F_4 — VMC_CLKN0
VMC_CLKP1 — R163 162/F_4 — VMC_CLKN1

R158 1.33K/F_4
R159 1.33K/F_4
R160 1.33K/F_4
R161 1.33K/F_4
R164 1.33K/F_4
R165 1.33K/F_4
R166 1.33K/F_4
R167 1.33K/F_4

VREFC_VMC1 / VREFD_VMC1 / VREFC_VMC3 / VREFD_VMC3

C298 0.01U/25V_4
C299 0.01U/25V_4
C300 0.01U/25V_4
C301 0.01U/25V_4

C302 1U/6.3V_4
C310 *1U/6.3V_4_NC
C306 1U/6.3V_4
C312 *1U/6.3V_4_NC
C318 0.1U/16V_4
C322 0.047U/10V_4
C326 0.1U/16V_4
C330 0.1U/16V_4
C334 0.047U/10V_4
C338 0.1U/16V_4

C303 1U/6.3V_4
C315 1U/6.3V_4
C316 *1U/6.3V_4_NC
C307 *1U/6.3V_4_NC
C319 0.1U/16V_4
C335 0.1U/16V_4
C327 0.047U/10V_4
C331 0.1U/16V_4
C323 *0.1U/16V_4_NC
C339 *0.1U/16V_4_NC

C304 *1U/6.3V_4_NC
C308 1U/6.3V_4
C314 1U/6.3V_4
C311 1U/6.3V_4
C320 *0.1U/16V_4_NC
C324 *0.1U/16V_4_NC
C328 *0.1U/16V_4_NC
C332 0.1U/16V_4
C336 0.1U/16V_4
C340 *0.1U/16V_4_NC

C305 1U/6.3V_4
C321 1U/6.3V_4
C313 1U/6.3V_4
C317 1U/6.3V_4
C309 *0.1U/16V_4_NC
C325 *0.1U/16V_4_NC
C329 0.1U/16V_4
C333 0.1U/16V_4
C337 0.047U/10V_4
C341 0.1U/16V_4

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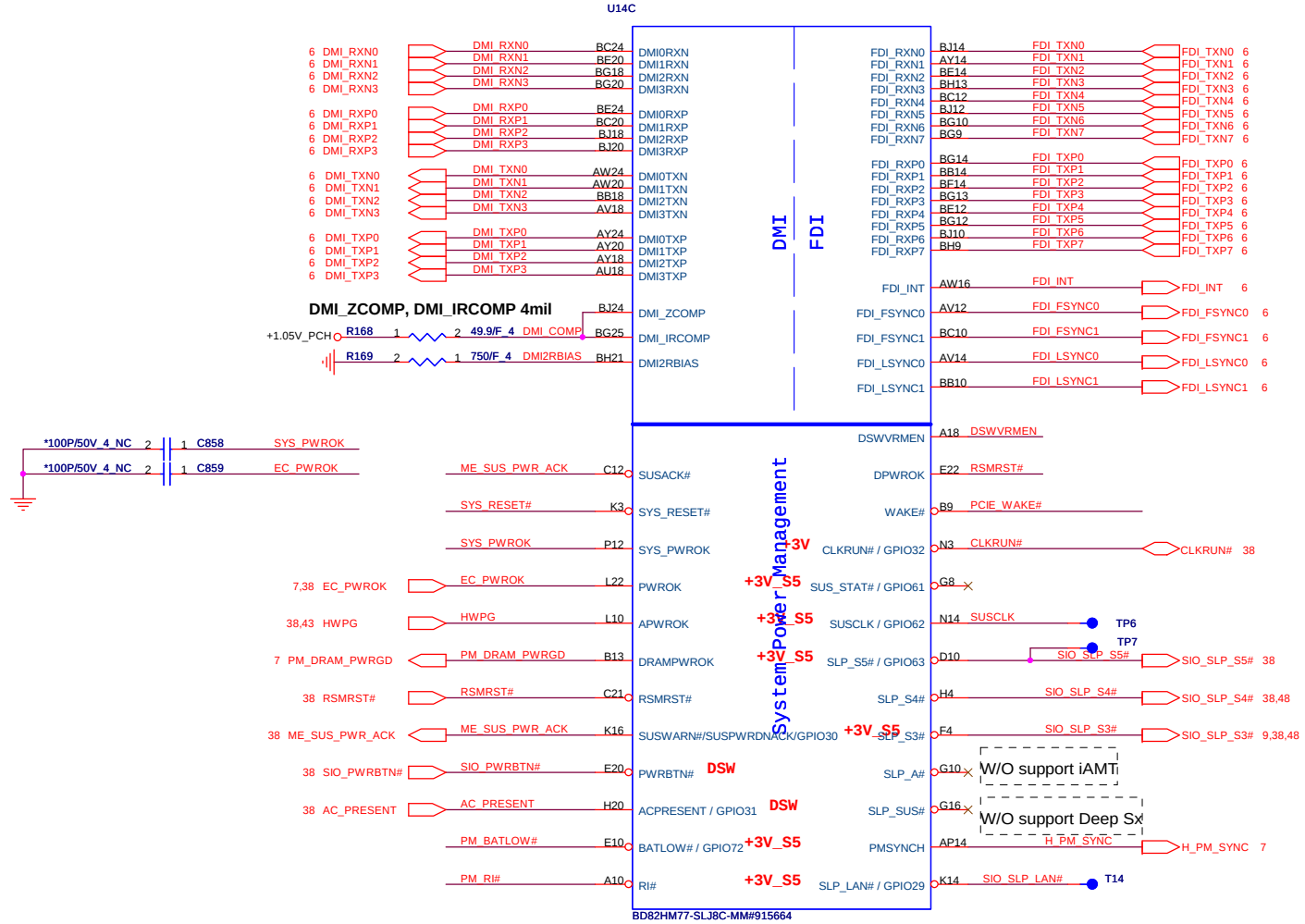
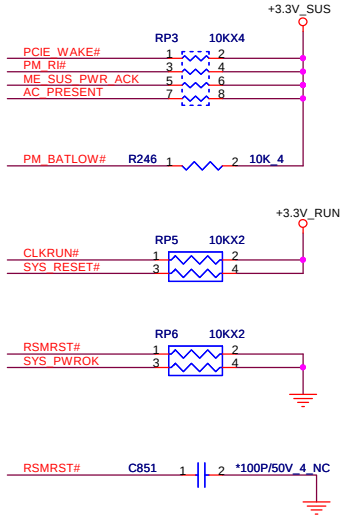
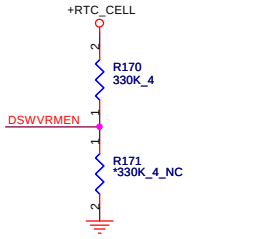
Cougar Point/Panther Point (DMI,FDI,PM)

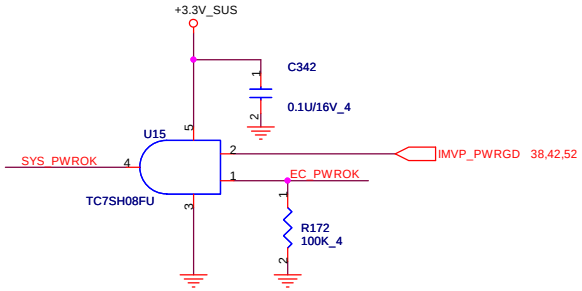


PCH Pull-high/low(CLG)





On Die DSW VR Enable
High = Enable (Default)
Low = Disable



Quanta Computer Inc.

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	Panther Point 1/7	1A
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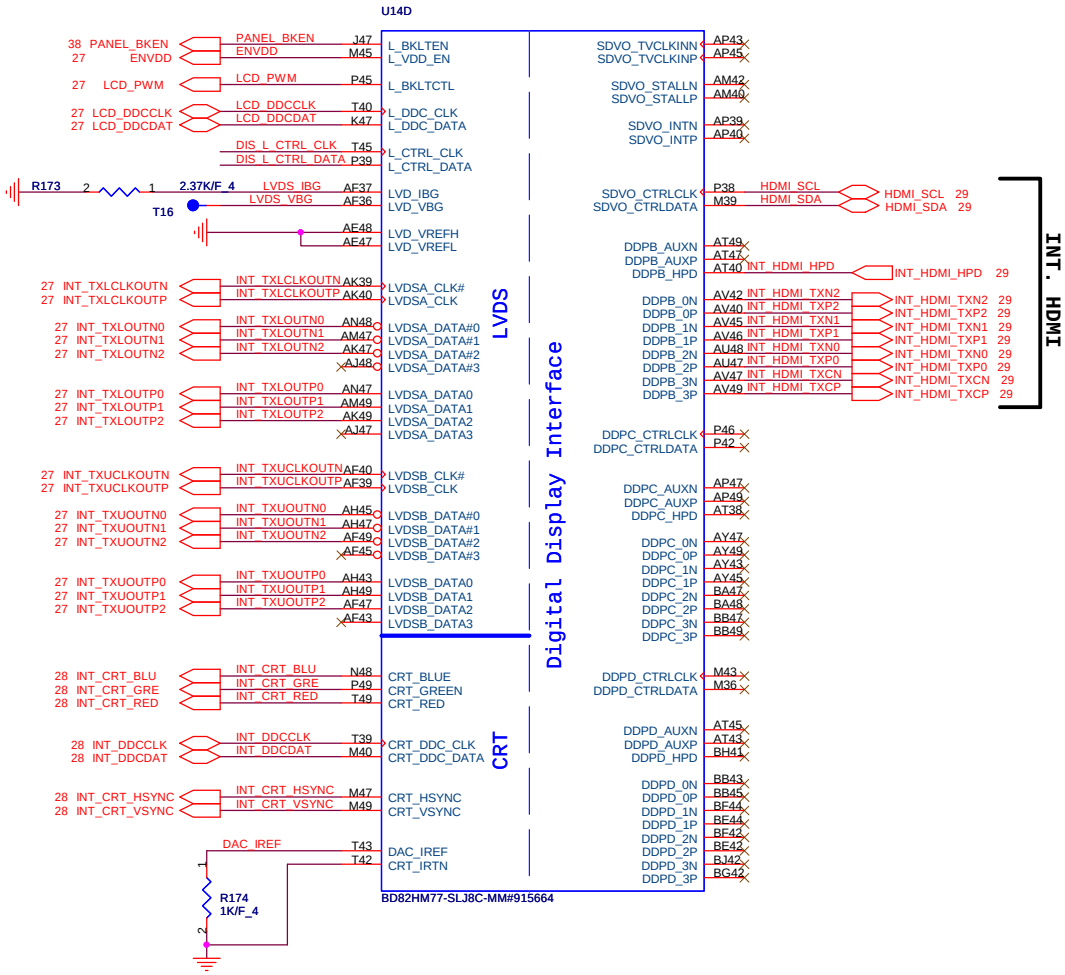
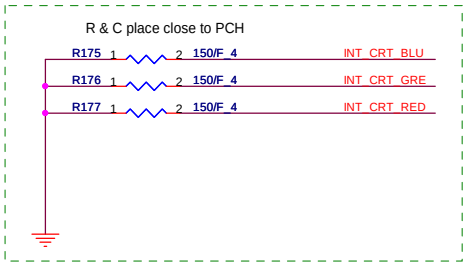
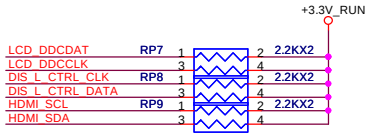
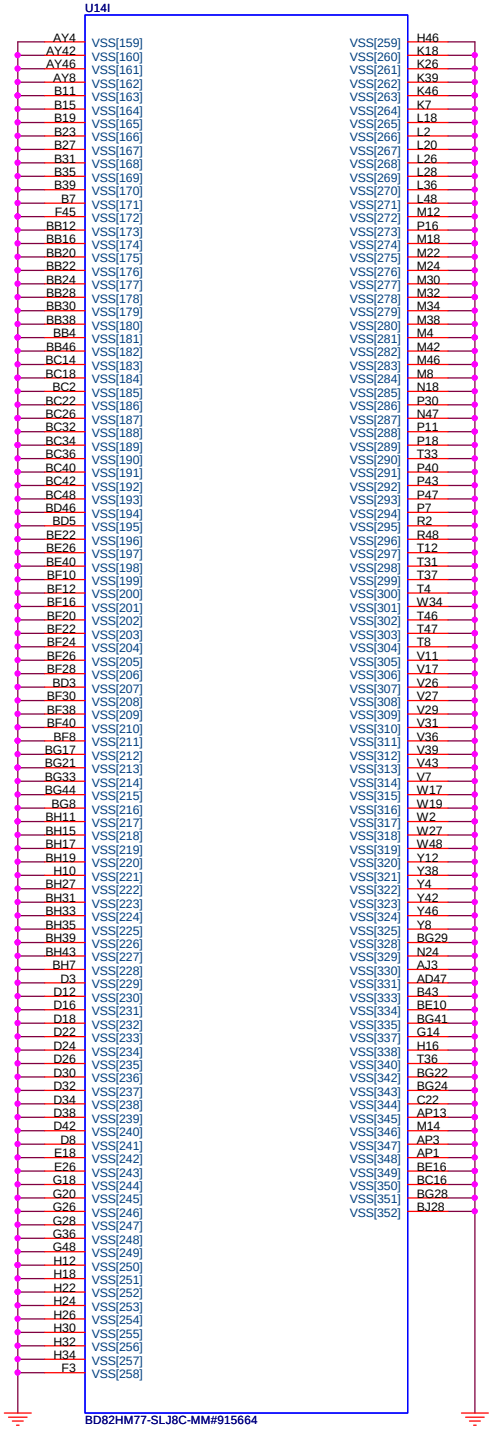
Cougar Point/Panther Point (LVDS,DDI)

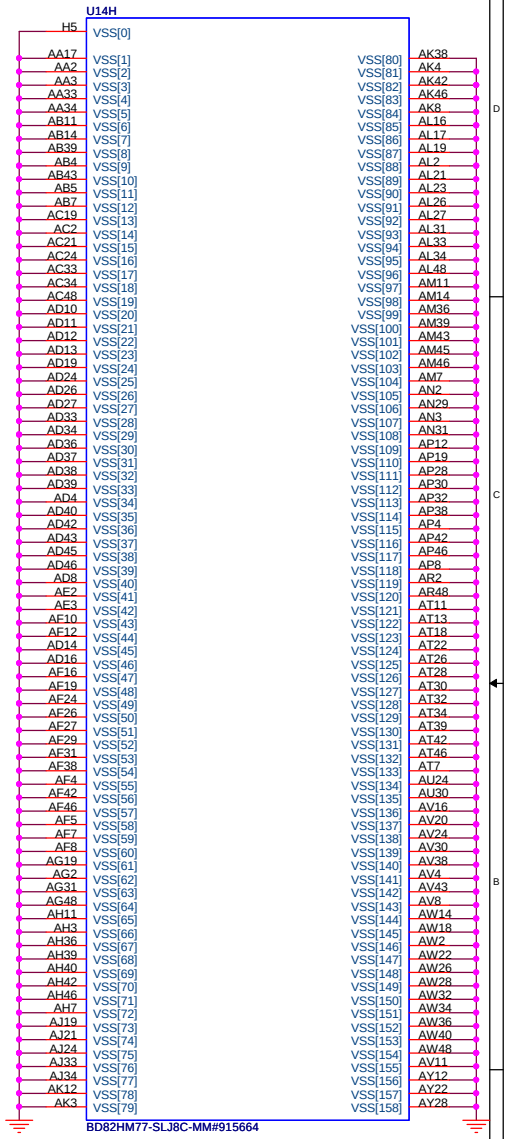






Cougar Point/Panther Point (GND)





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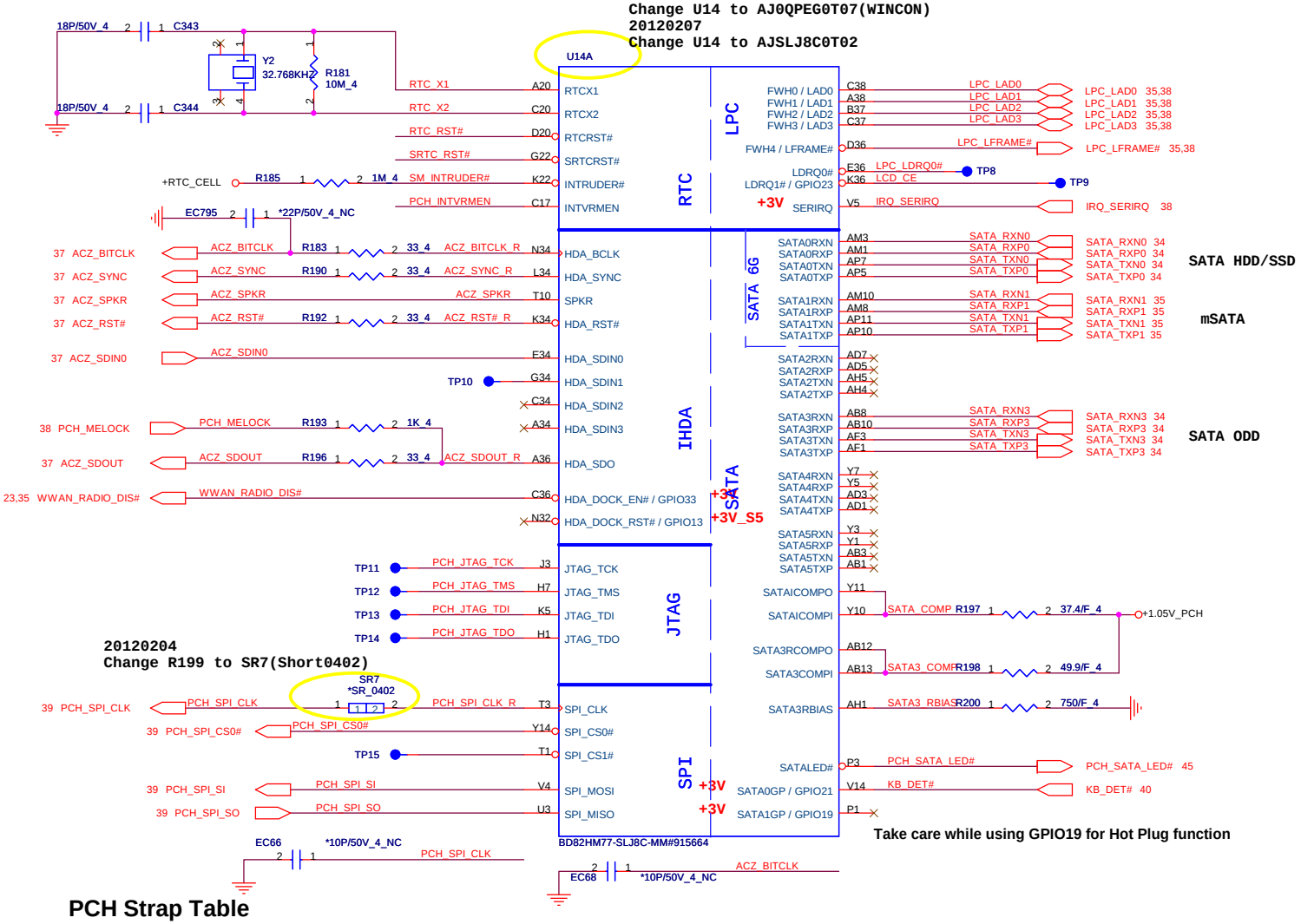
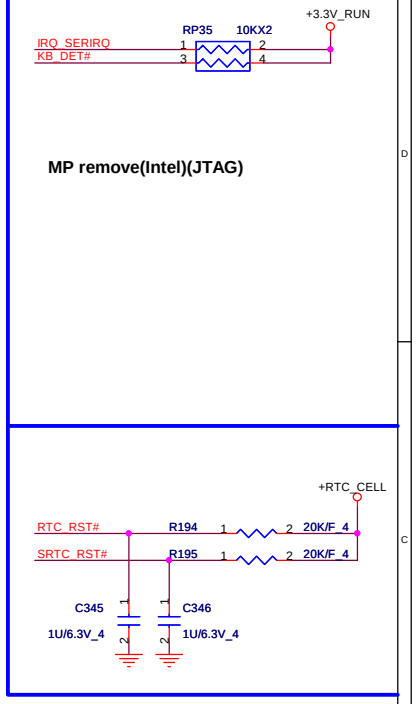
Cougar Point/Panther Point (HDA,JTAG,SATA)

20120204
Change U14 to AJ0QPEG0T07(WINCON)
20120207
Change U14 to AJSLJ8C0T02





20120204
Change R199 to SR7(Short0402)

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+RTC_CELL R203 330K_4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R204 1K_4 ACZ_SYNC_R

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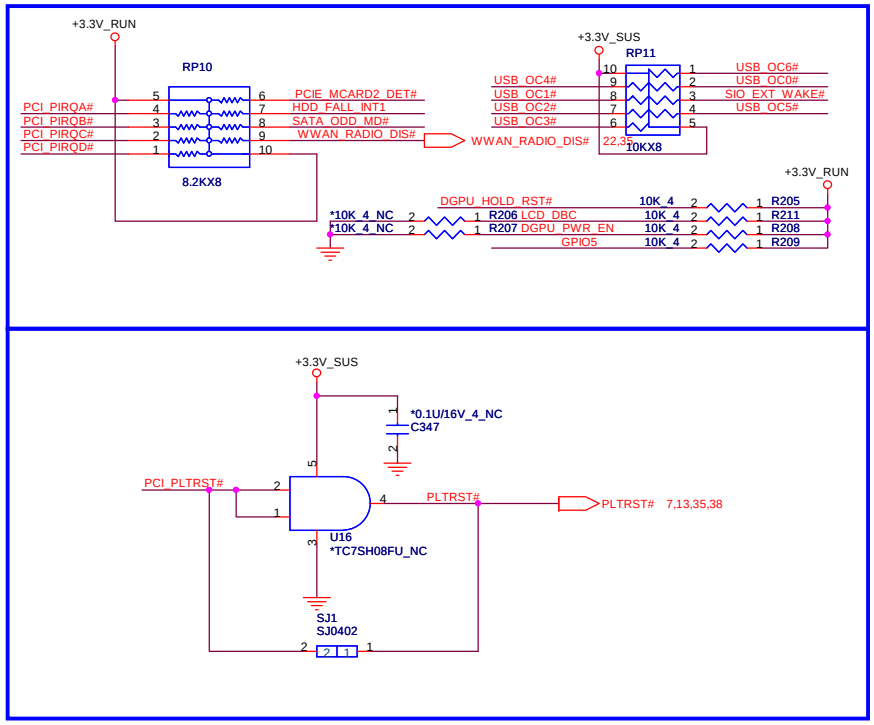
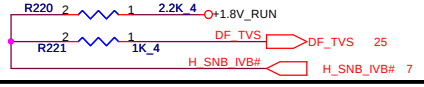
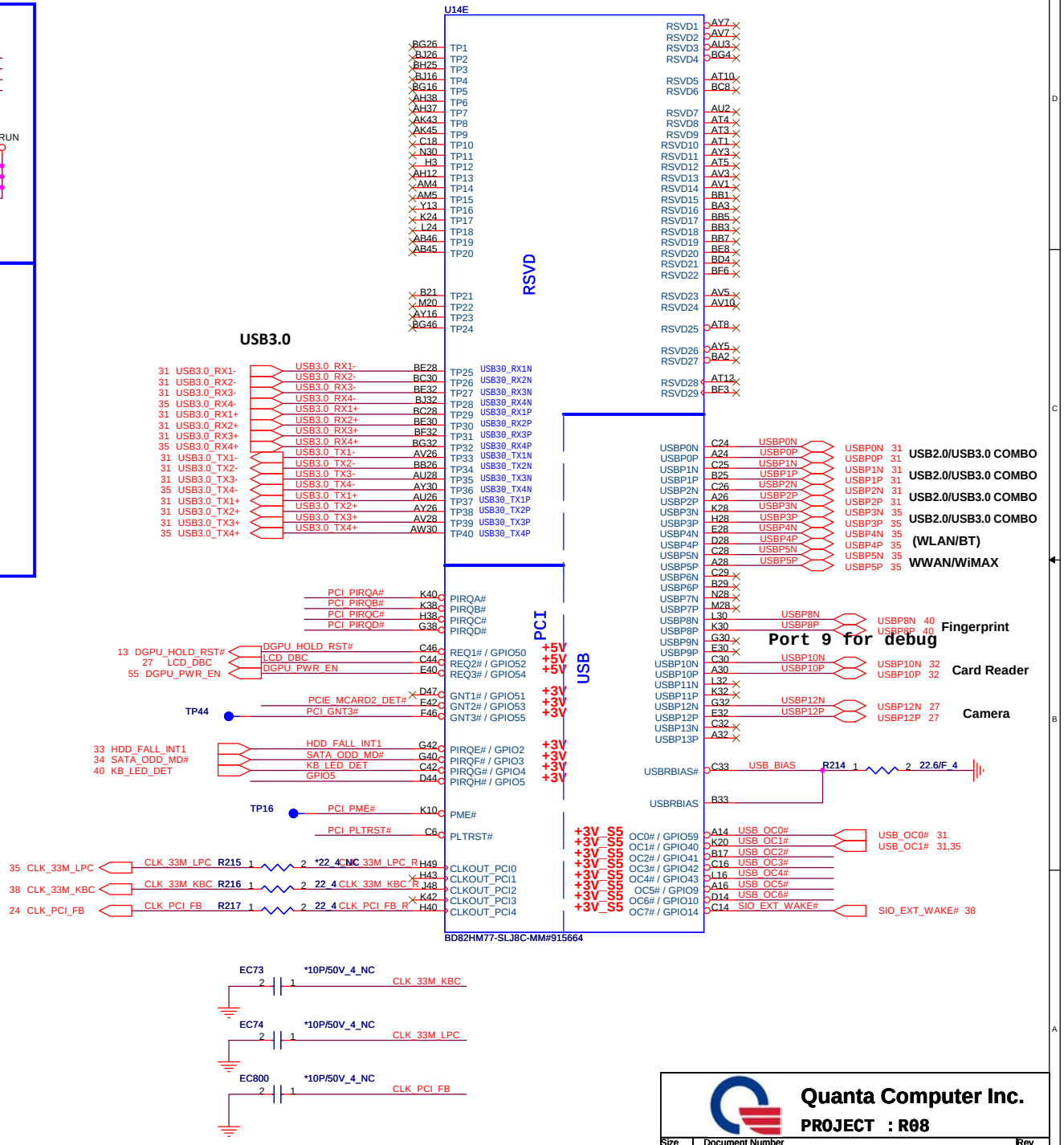
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



Pin Name	Strap description	Sampled	Configuration
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Bit 0 / Bit 1 / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
			Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm





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	Panther Point 4/7	1A

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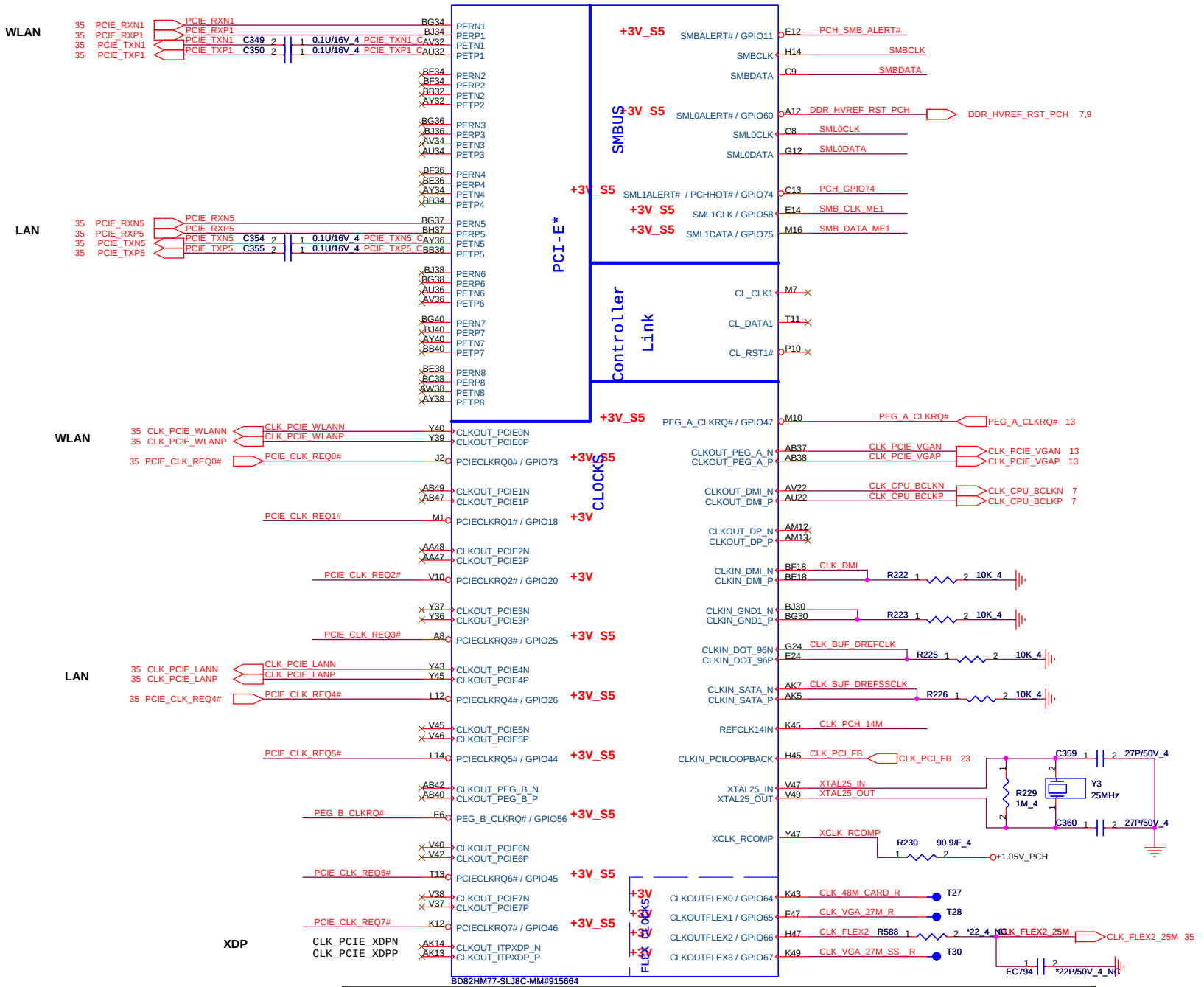
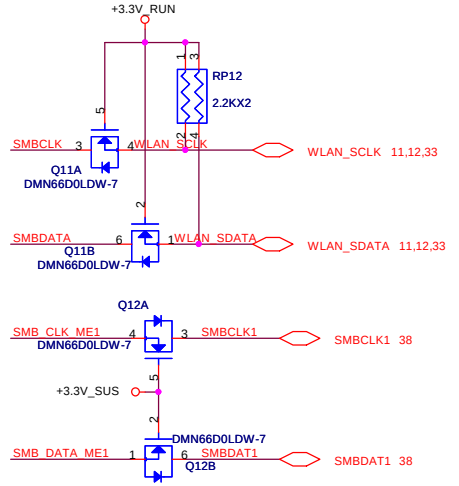
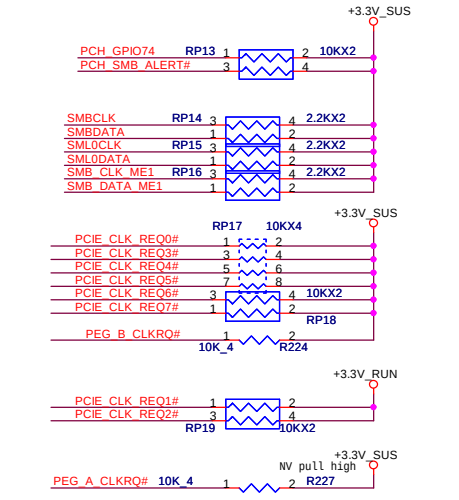
U14B Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 /GPIO64	• 33 /27 /48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 /GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC /48/24 MHz
CLKOUTFLEX2 /GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 /GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

SMBus/Pull-up(CLG)





CLK_REQ/Strap Pin(CLG)

Stuff for Integrated CLK Gen Mode

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	Panther Point 5/7	1A

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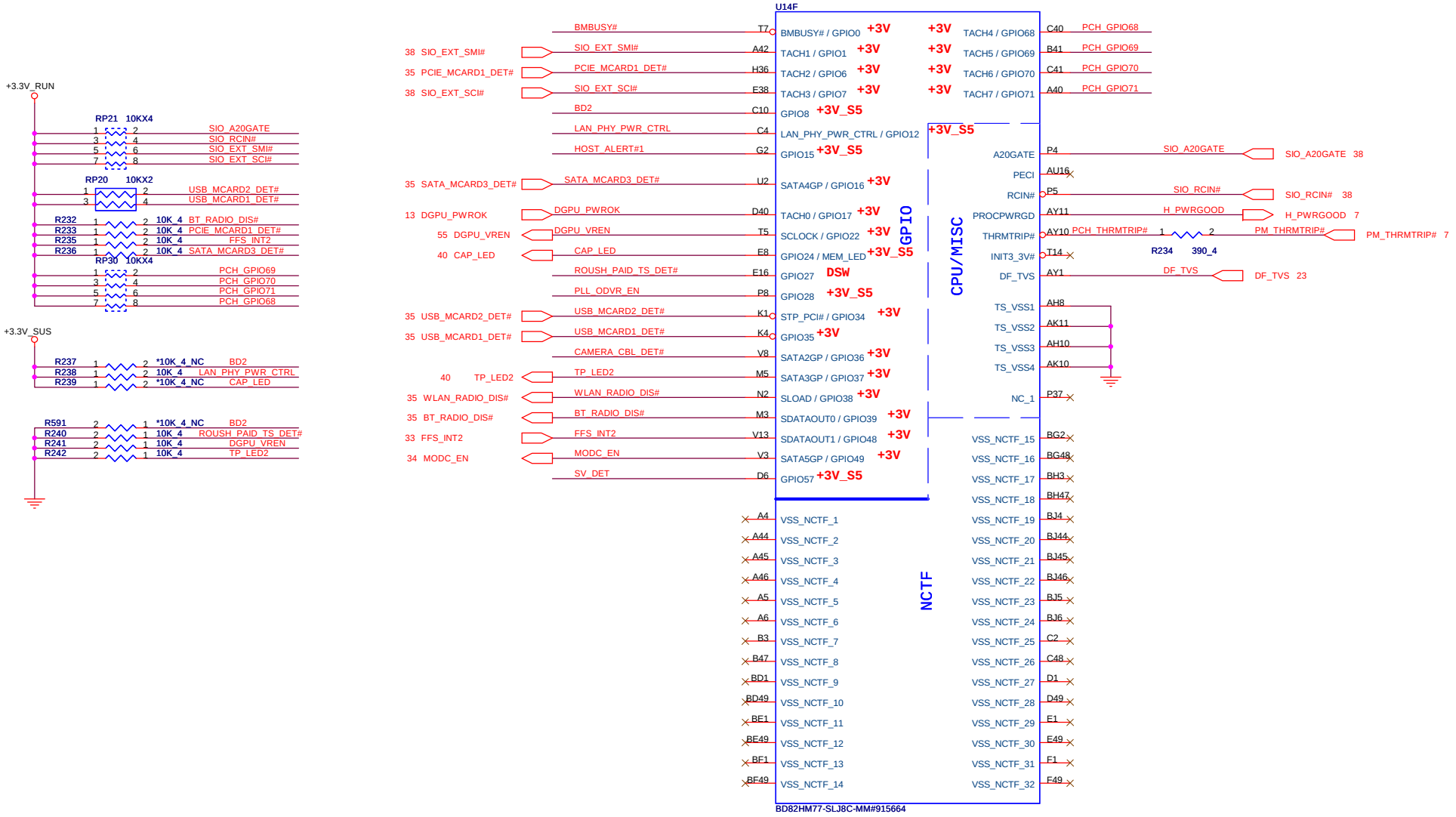
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

R243 1 2 *1K_4_NC PLL_ODVR_EN

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

CAMERA_CBL_DET# R247 1 2 10K_4

SGPIO

+3.3V_RUN

BMBUSY# R248 1 2 10K_4

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

+3.3V_SUS

HOST_ALERT#1 R244 1 2 1K_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

+3.3V_SUS

R245 1 2 10K_4 SV_DET

MFG-TEST

+3.3V_RUN

WLAN_RADIO_DIS# R249 1 2 10K_4
R250 1 2 *0_4_NC

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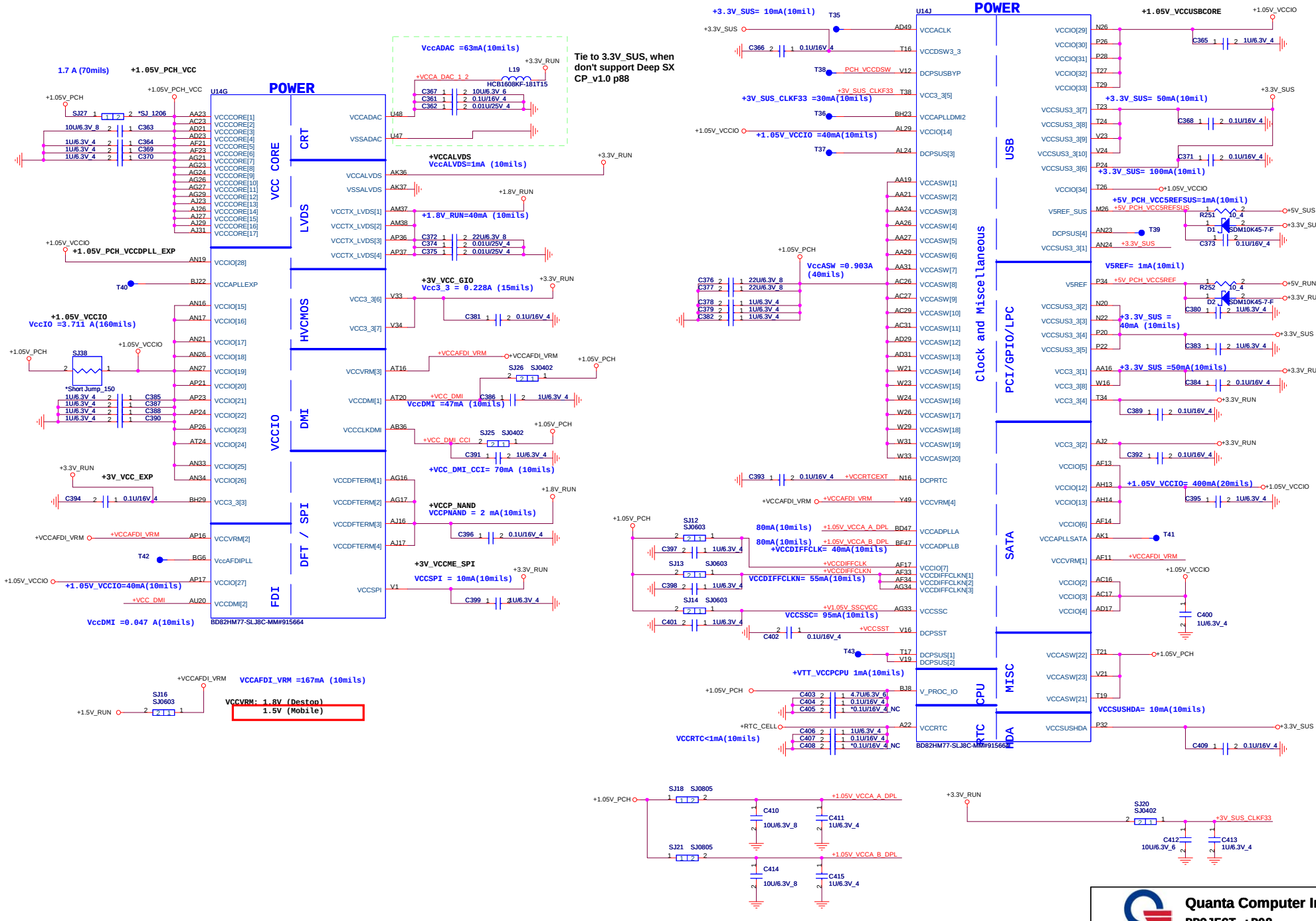
Cougar Point/Panther Point (POWER)

Cougar Point/Panther Point (POWER)



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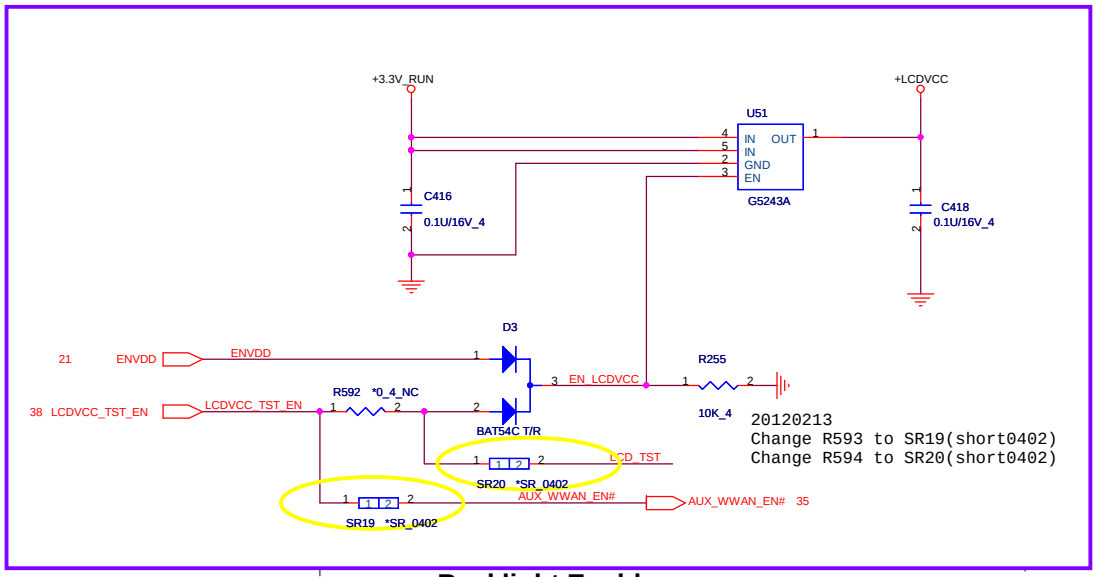
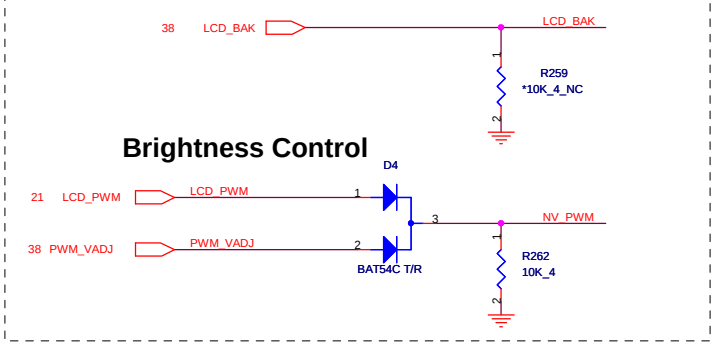
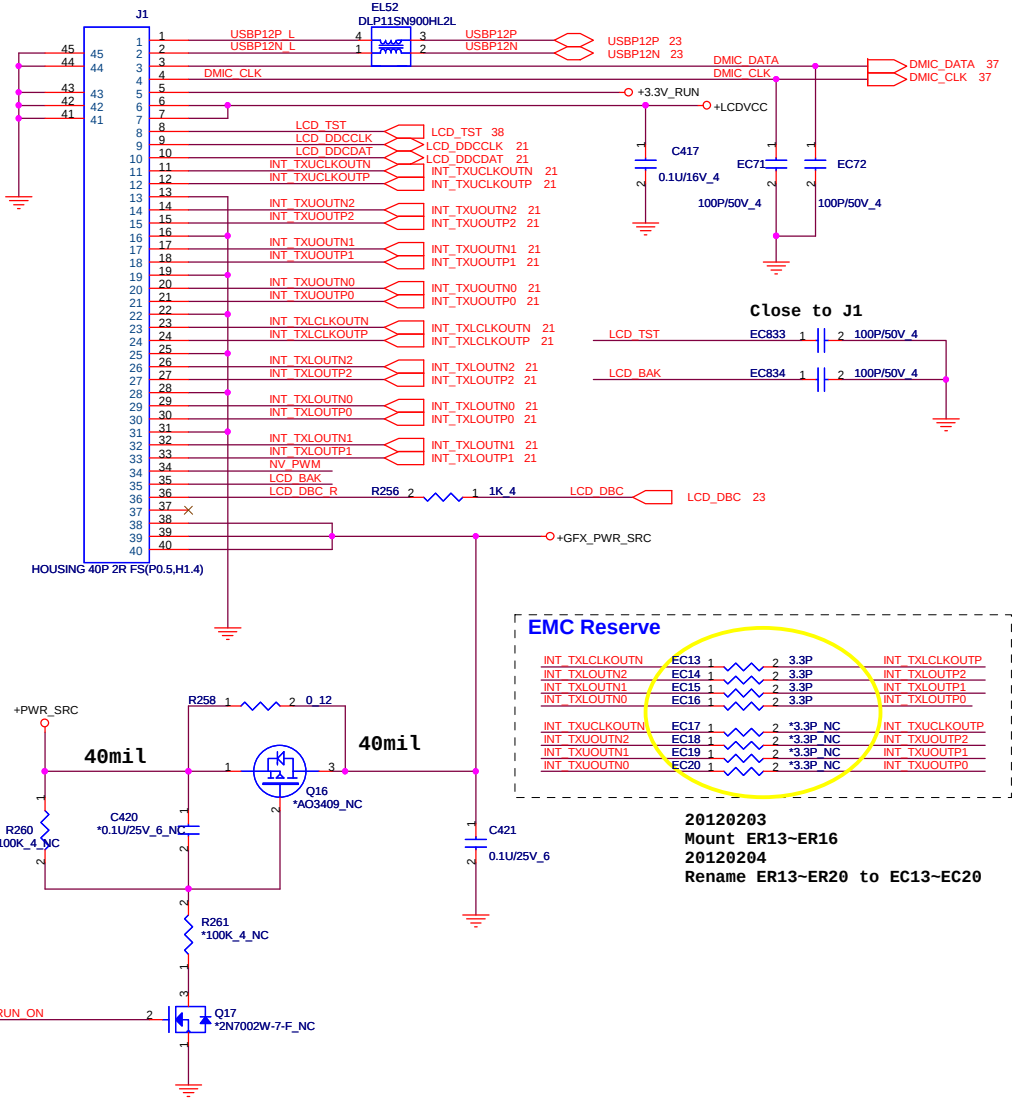
Follow PDC LVDS pin define & LVDS connector P/N.



Backlight Enable





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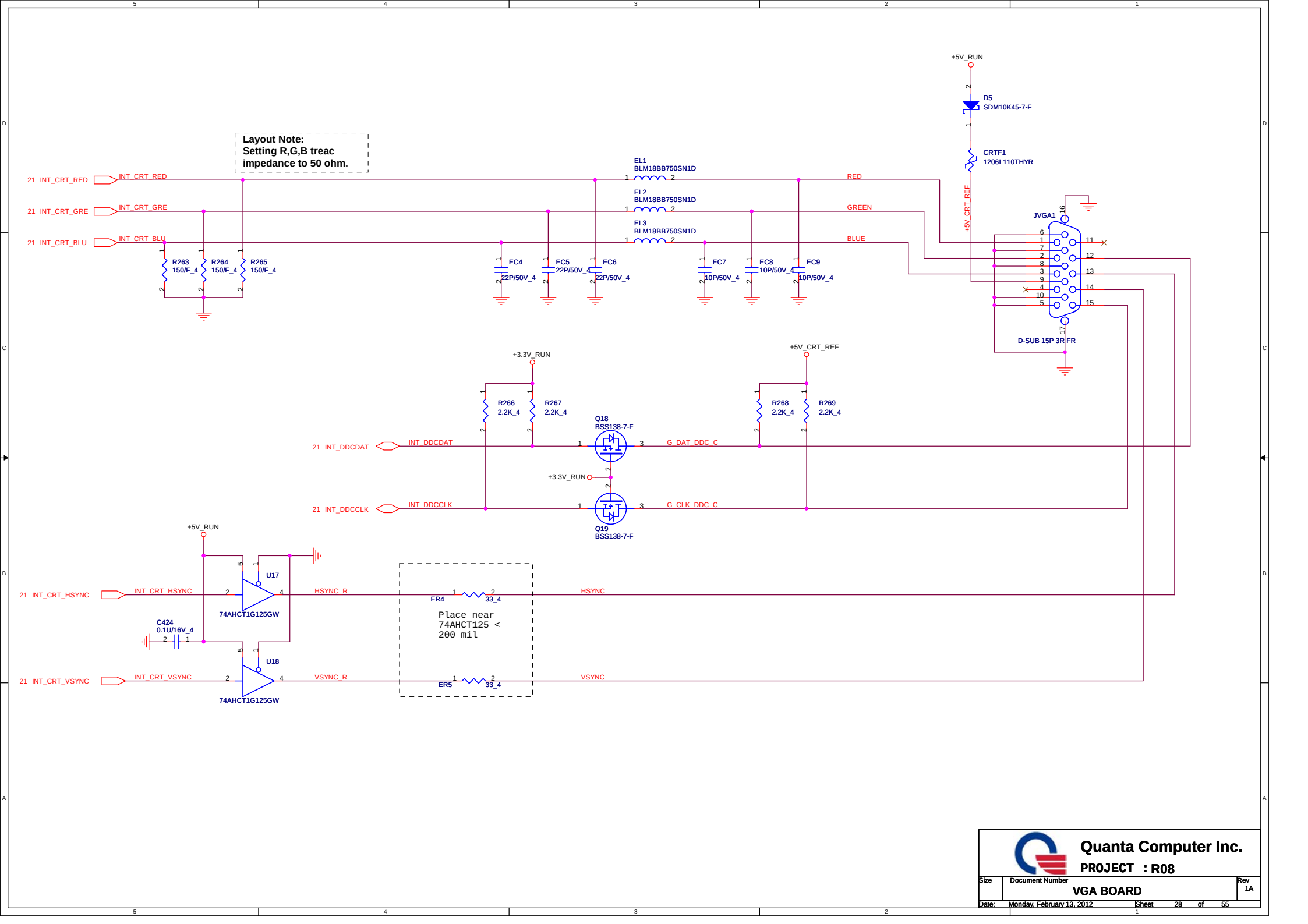

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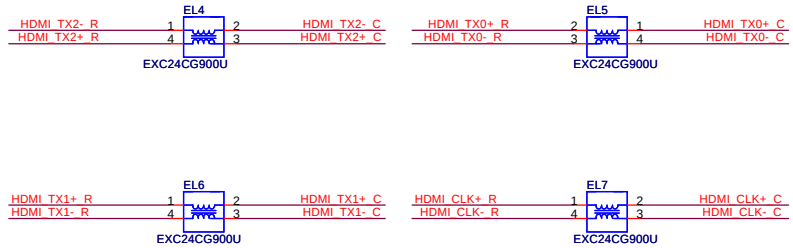
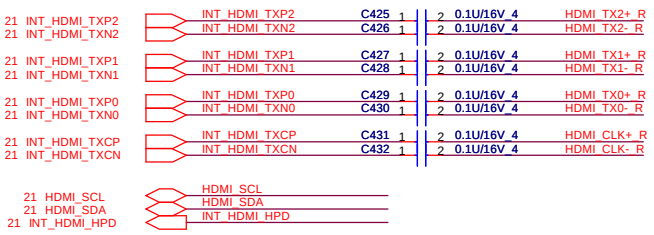
Reserve for EMI and close to HDMI CONN

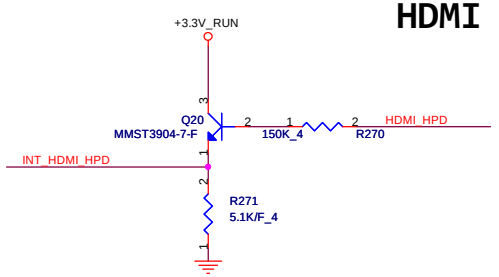


HDMI

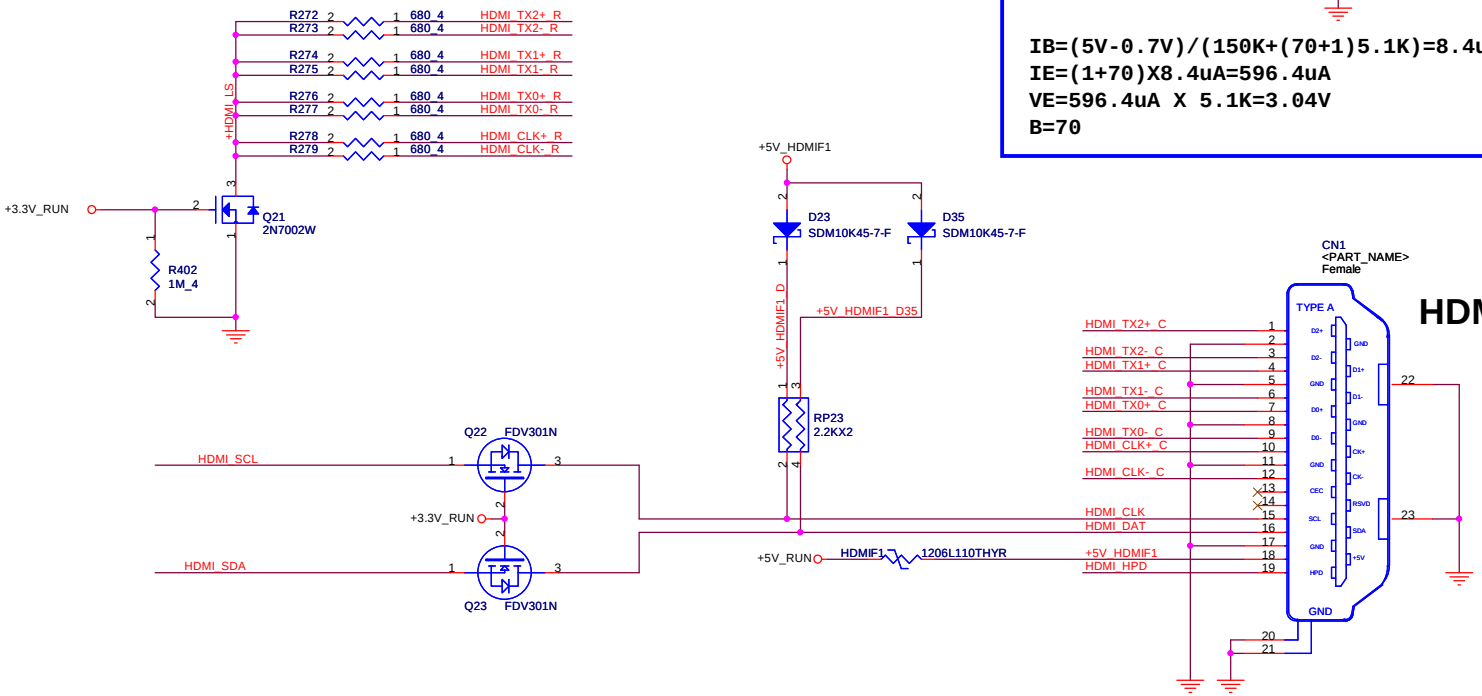


HDMI_HPD spec VinH_min=2.0V

HDMI HPD



IB=(5V-0.7V)/(150K+(70+1)5.1K)=8.4uA
IE=(1+70)X8.4uA=596.4uA
VE=596.4uA X 5.1K=3.04V
B=70



HDMI Conn.

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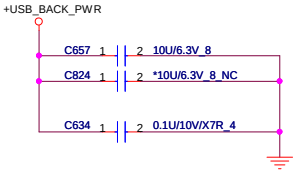
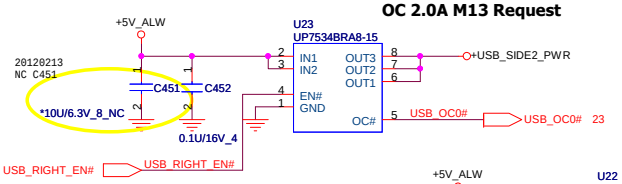
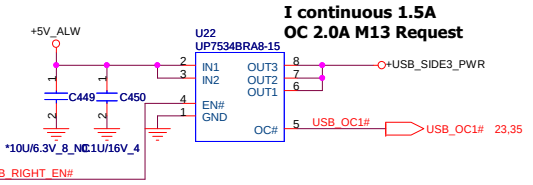
USB Power share

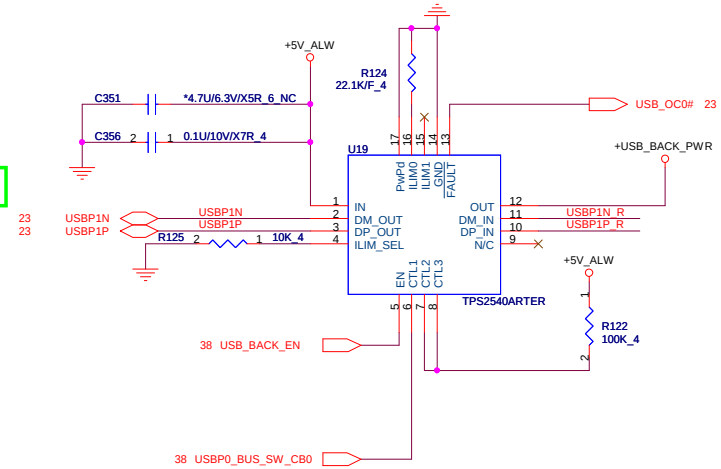
USBP0_BUS_SW_CB0	Mode	Operating at
Low	DCP, Auto-detect	S3/S4/S5, 1.5 A
High	CDP, BC Spec 1.1	S0, 1.5 A

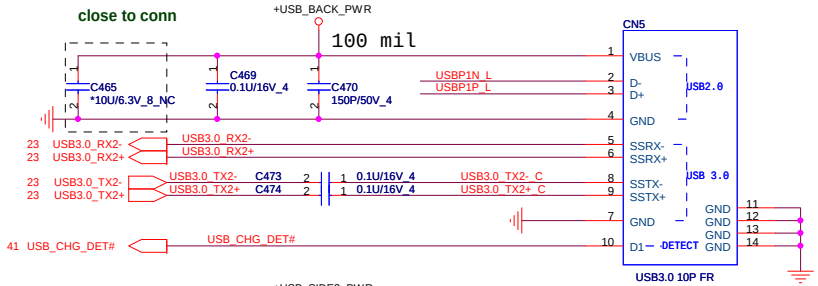
	R109	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

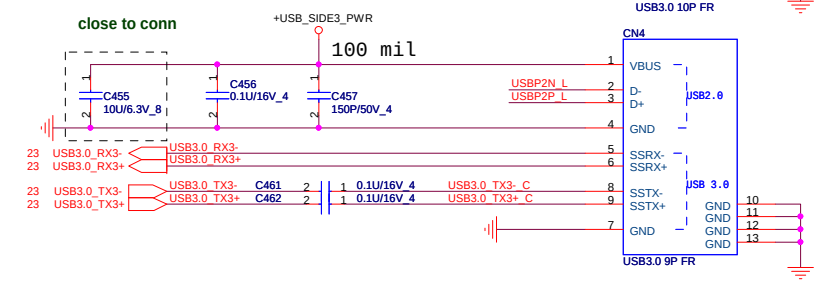


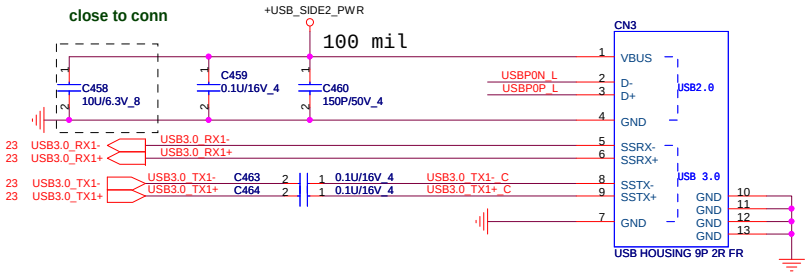


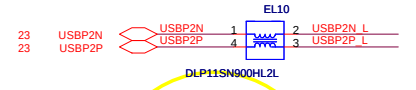


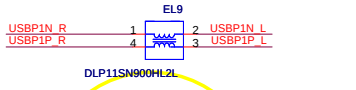


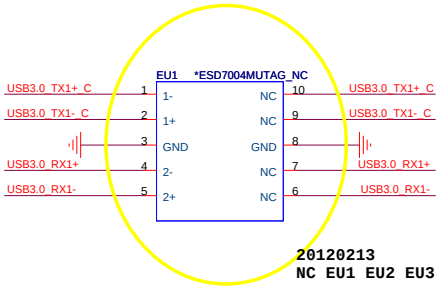


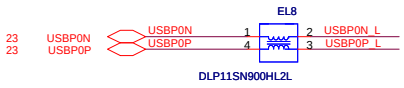


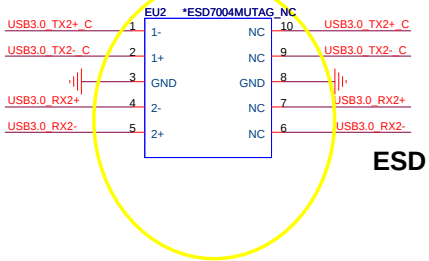


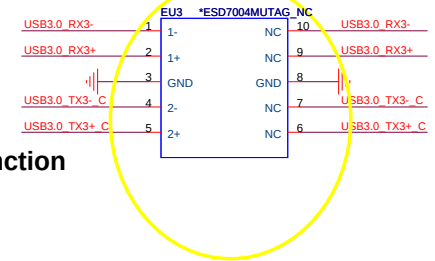




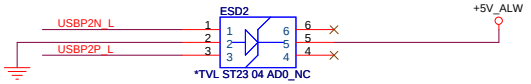








ESD Function



ESD Function

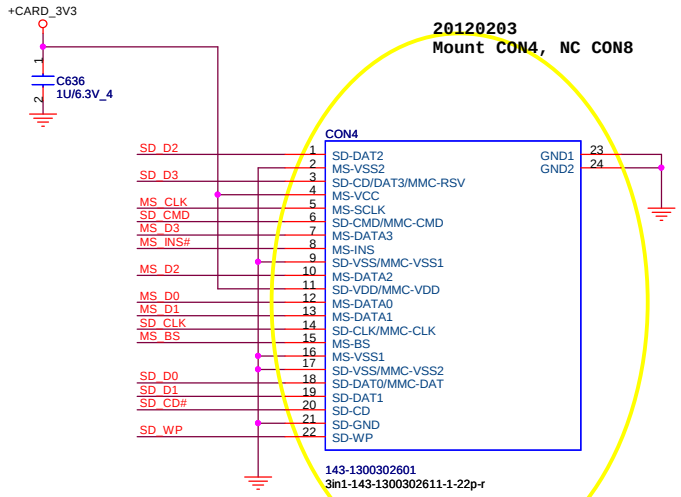
Place ESD diodes as close as USB connector.

Quanta Computer Inc.
PROJECT : R08

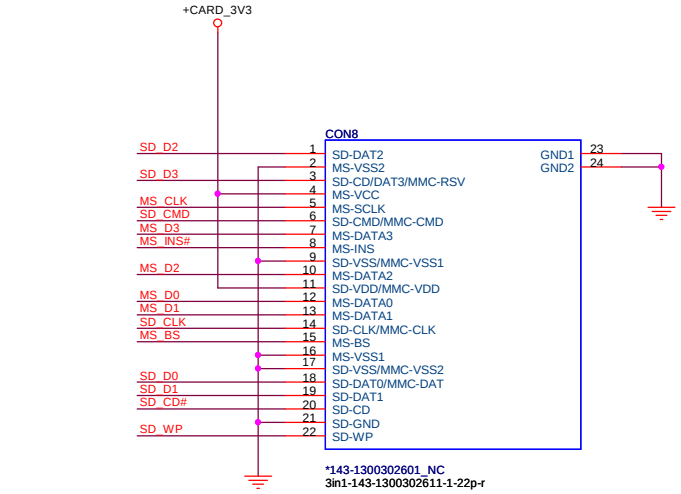
Size	Document Number	Rev
	USB 3.0 port / USB power share	1A
Date: Monday, February 13, 2012	Sheet 31 of 55	

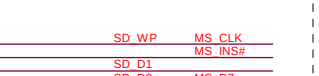
Cardreader (RTS5179GR) Support SD3.0 USH50

For Vostro Placement(V08,V08A)-Far ODD

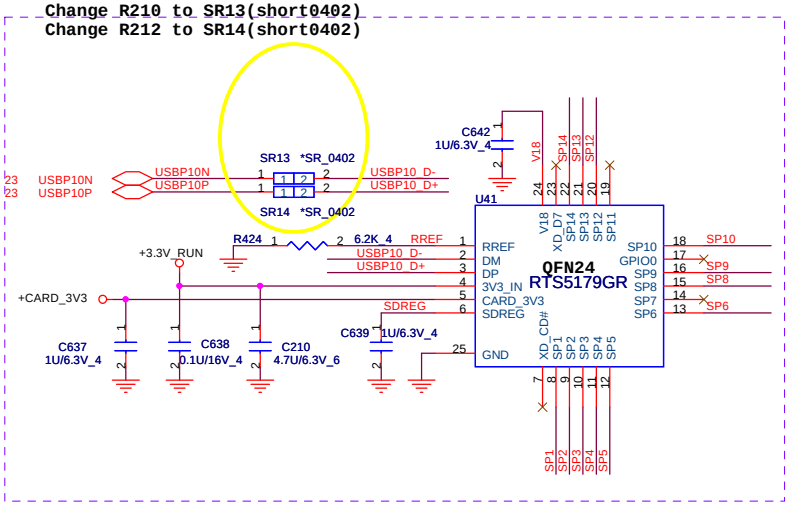


For INSPIRON Placement (R08,R08A,R08T)-Near ODD





20120206
Remove EL47
Change R210 to SR13(short0402)
Change R212 to SR14(short0402)



Share Pin

Quanta Computer Inc.
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Size	Document Number	Rev
	Cardreader (RTS5179GR)	1A
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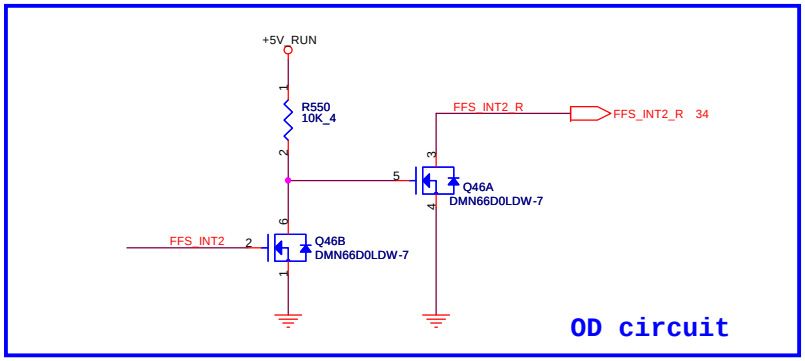
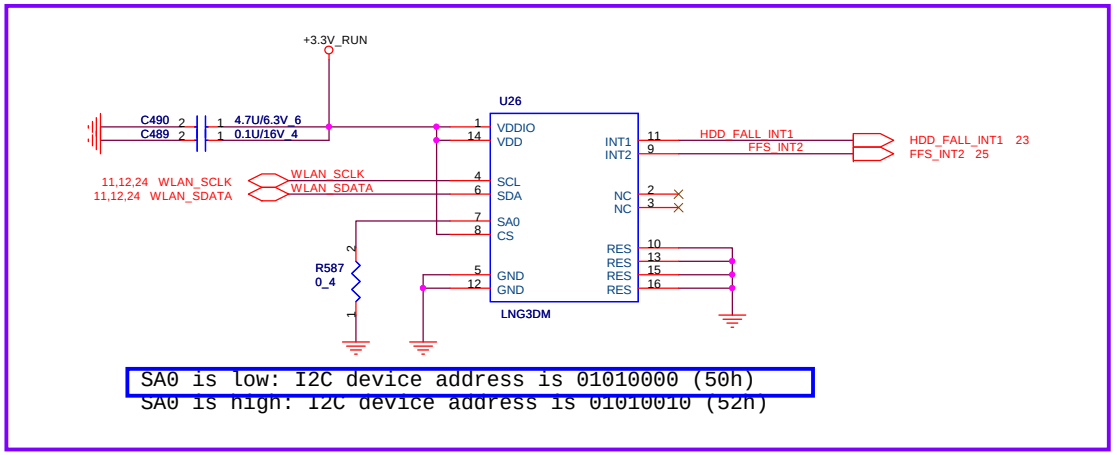
3-axis Fall Sensor

If you have two HDD,need add two OD circuit for Fall sensor interrupt circuit



20120203
Mount Function code "FFS" part



Quanta Computer Inc.
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Size	Document Number	Rev
	3-axis Fall Sensor	1A
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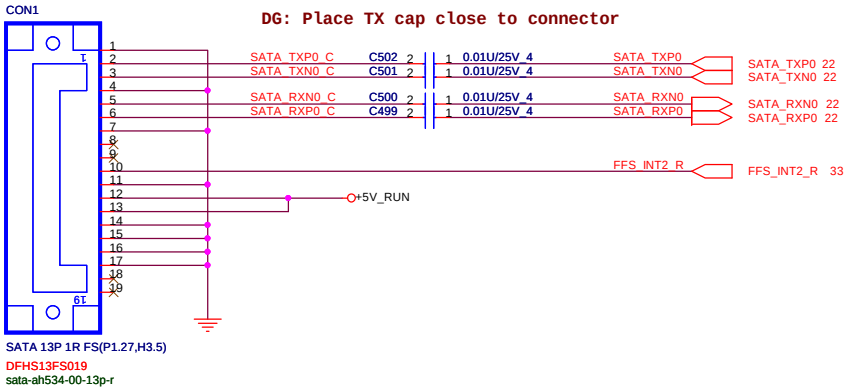
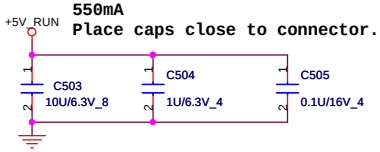
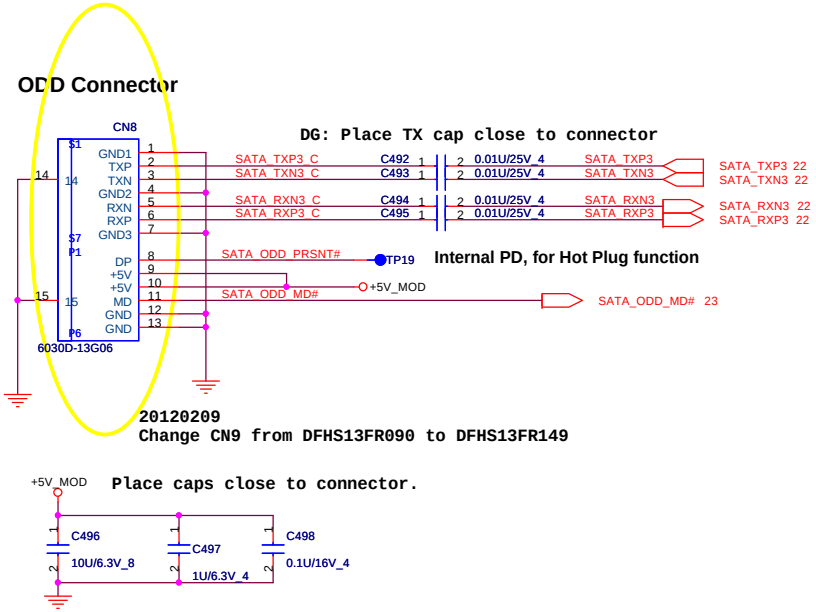
HDD

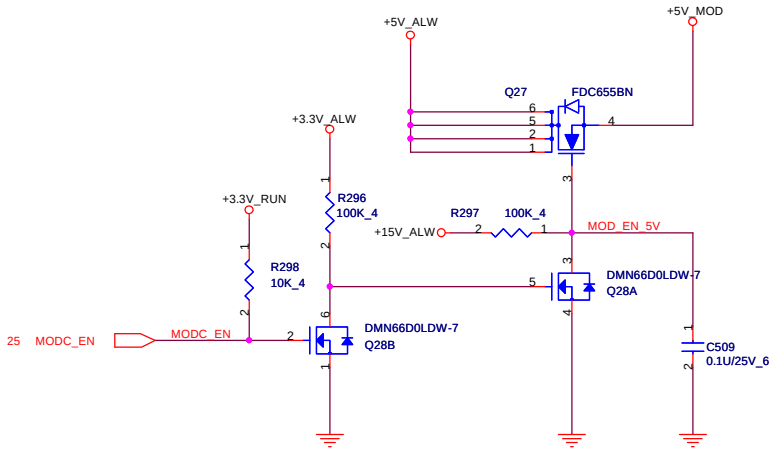




ODD



Support Zero power ODD



Quanta Computer Inc.

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Size	Document Number	Rev
	SATA HDD/ODD	1A

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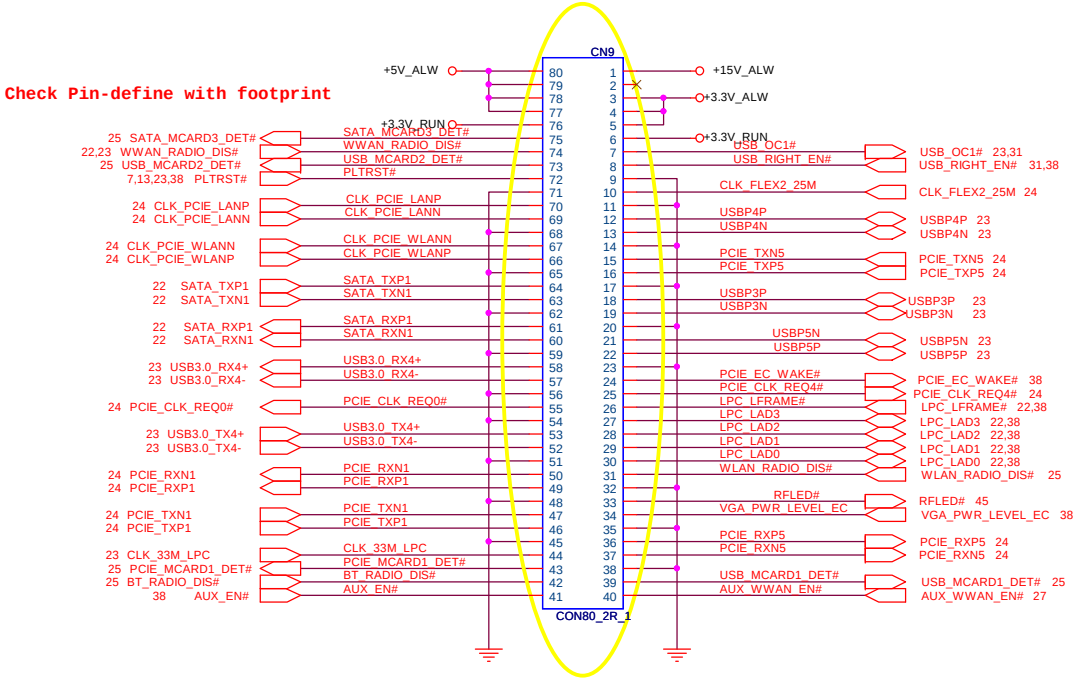
20120203
Change CN9 footprint from "88069-8001b-bs-80p-ldh" to "88069-8001b-bs-80p-ldh-smt"

Check Pin-define with footprint

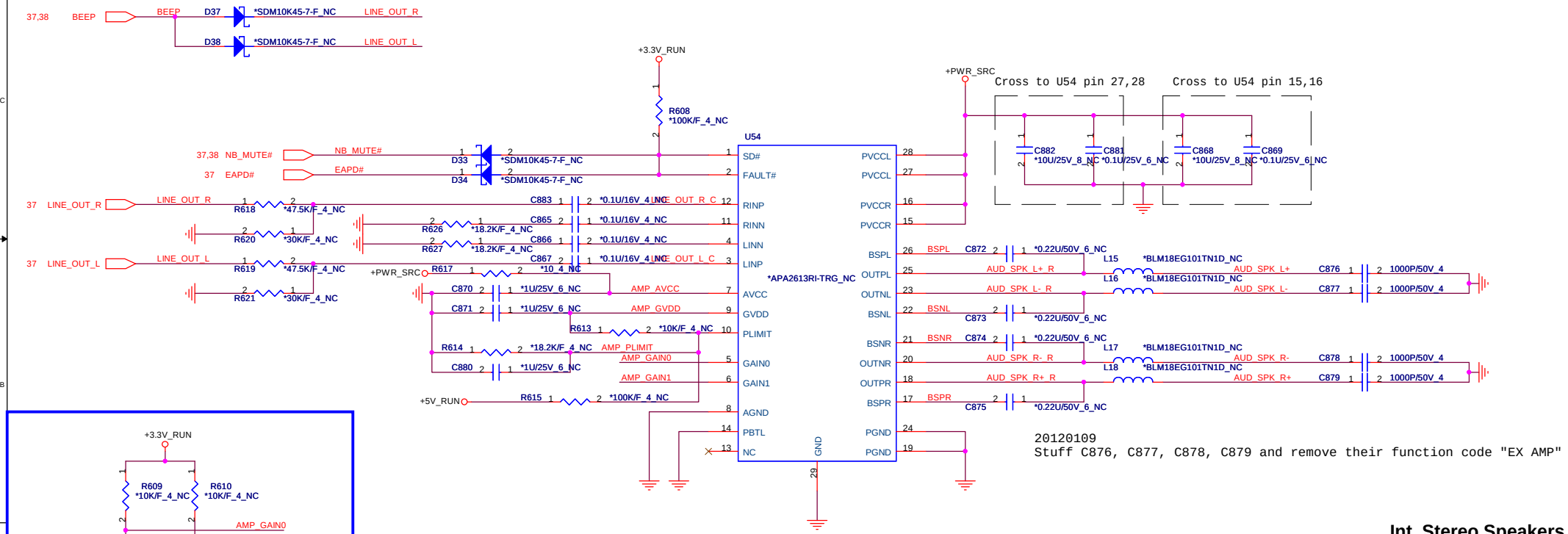


Quanta Computer Inc.

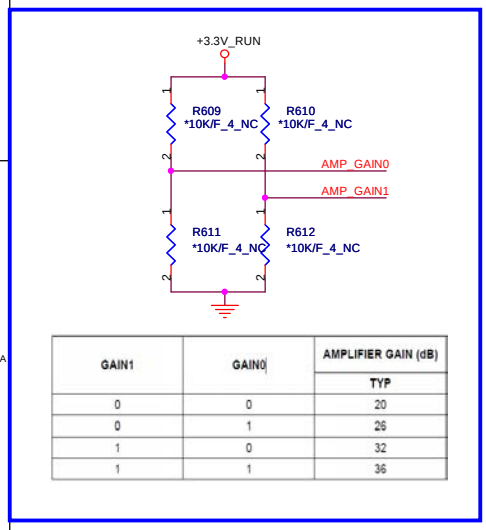
PROJECT : R08

Size	Document Number	Rev
	BTB CONN	3A
Date: Monday, February 13, 2012	Sheet 35 of 55	

ANPEC APA2613 is P2P to TI TPA3113
Default use APA2613



20120109
Stuff C876, C877, C878, C879 and remove their function code "EX AMP"



GAIN1	GAIN0	AMPLIFIER GAIN (dB)
		TYP
0	0	20
0	1	26
1	0	32
1	1	36

Int. Stereo Speakers

	Amplifier	Function code
R08/R08A/V08/V08A	CODEC CX20672	Mount "IN AMP"
R08T	APA2613 or TPA3113	Mount "EX AMP"

Quanta Computer Inc.
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Size	Document Number	Rev
		1A

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AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.

For EMI, close the audio I/O connector.

U50 CX20672-21Z

MIC Decoupling close to Codec

Port B
External Stereo microphone

20120206
Change EL48 to SR15(short0603)
Change EL49 to SR16(short0603)
Change EL50 to SR17(short0603)
Change EL51 to SR18(short0603)

Port A
Headphone

Flow PDC pin define

EMI Reserved Please see Design Guide for audio grounding.

Quanta Computer Inc.
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Size	Document Number	Rev
	CODEC	1A
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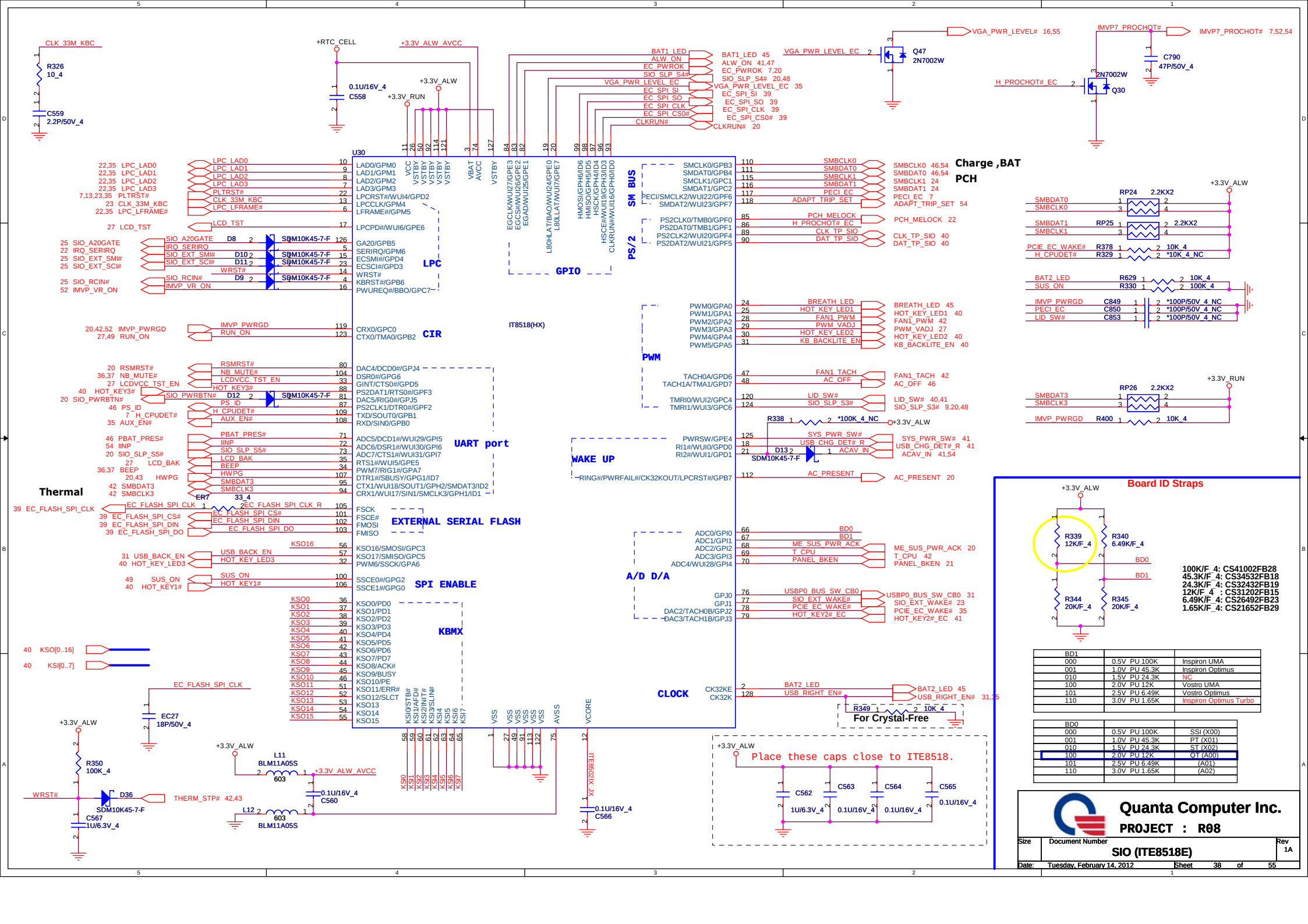
U30
IT8518(HX)
LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Charge ,BAT
PCH
Thermal
Board ID Straps
For Crystal-Free
Place these caps close to ITE8518.
Quanta Computer Inc.
PROJECT : R08
SIO (ITE8518E)
Size
Document Number
Rev 1A
Date: Tuesday, February 14, 2012
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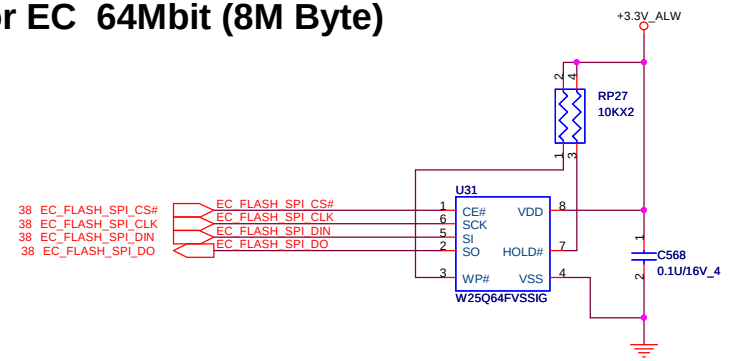
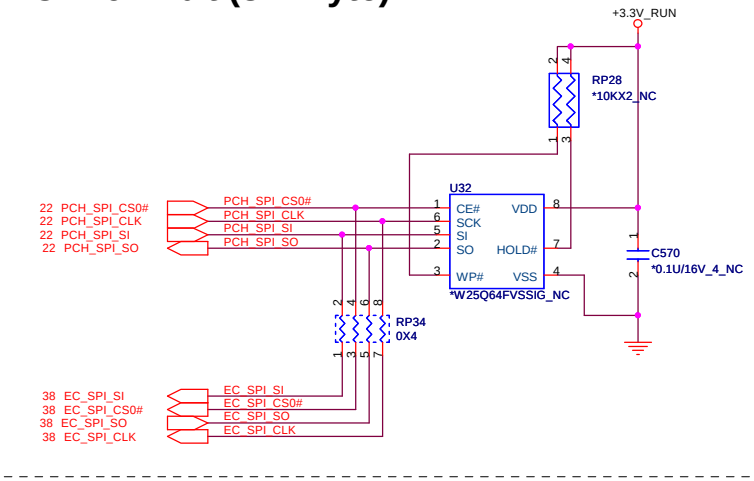
FLASH / RTC

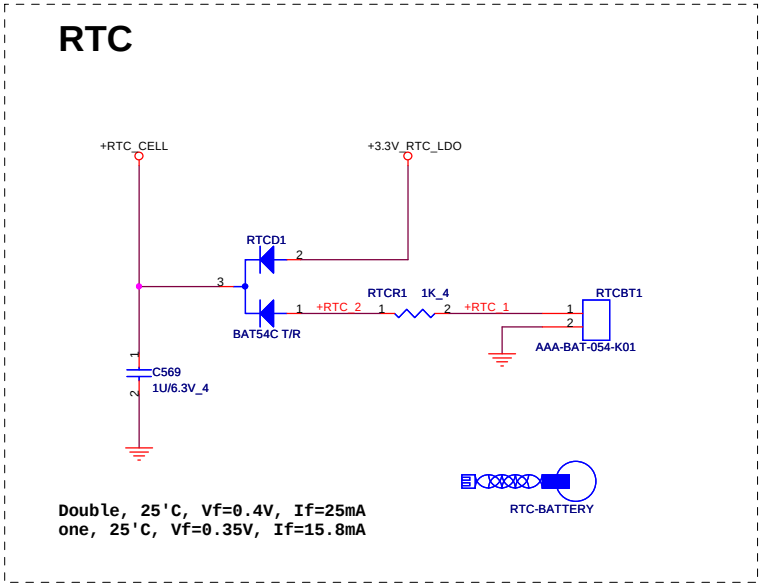
For EC 64Mbit (8M Byte)



For PCH 64Mbit (8M Byte)



RTC



Quanta Computer Inc.		
PROJECT : R08		
Size	Document Number: FLASH / RTC	Rev: 1A
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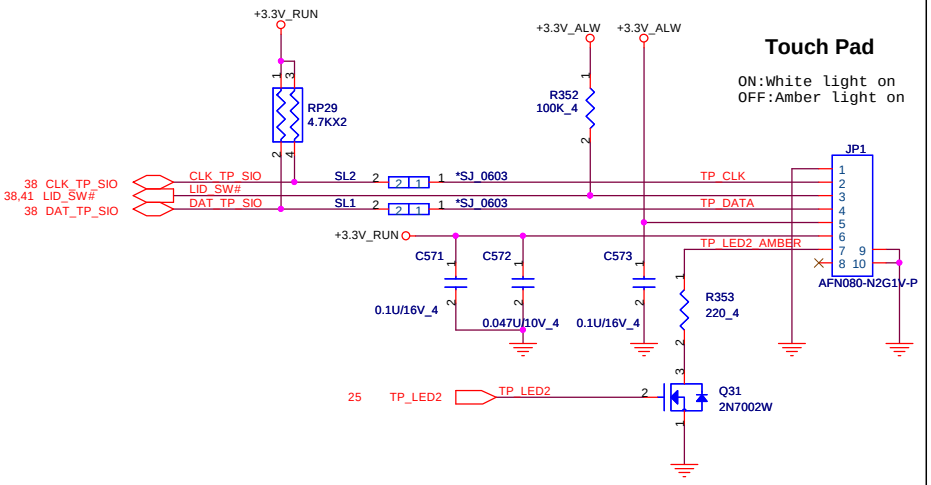
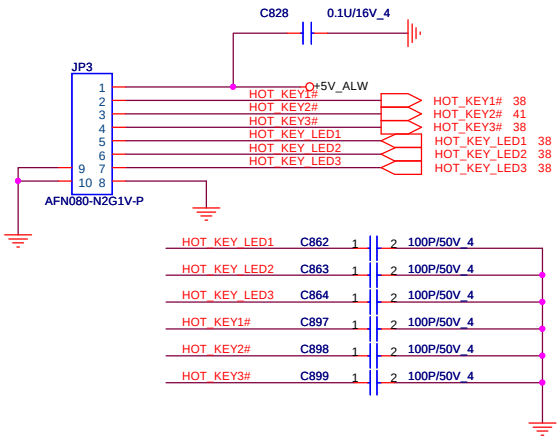
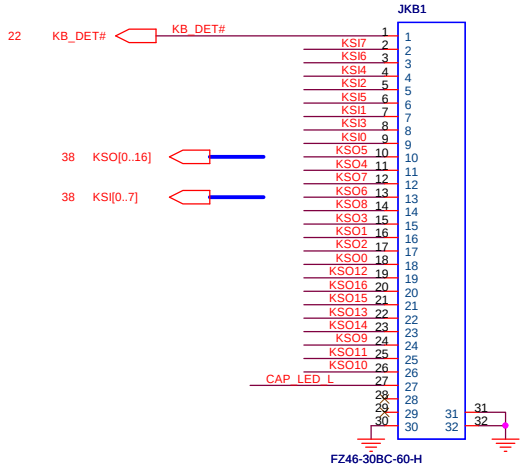
TP CONNECTOR

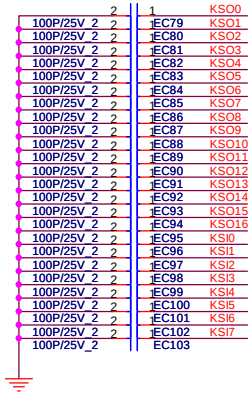


HotKey CONN



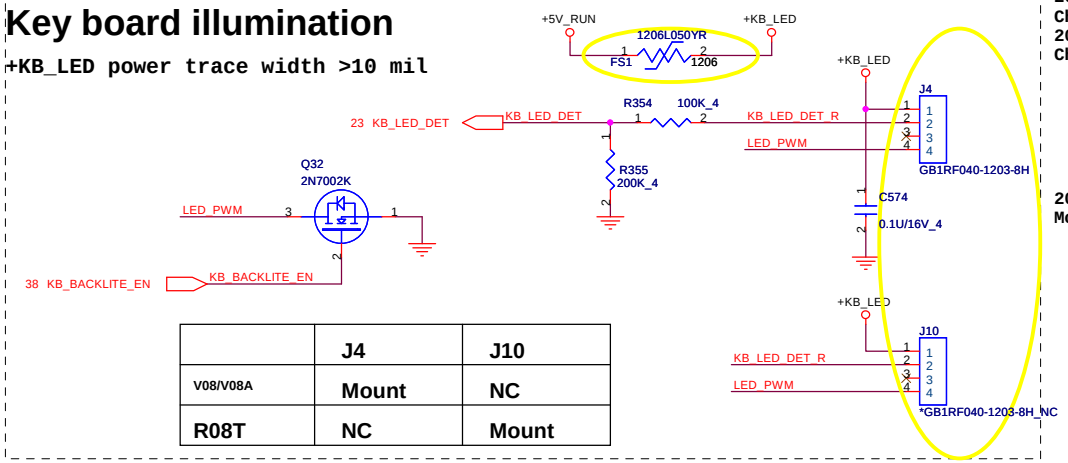
KB CONN





Key board illumination

+KB_LED power trace width >10 mil

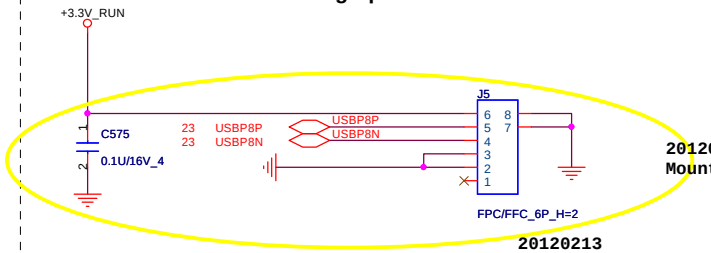


	J4	J10
V08/V08A	Mount	NC
R08T	NC	Mount

20120206
Change FS1 to SR12(short1206)
20120213
Change SR12 back to FS1

20120203
Mount J4, NC J10

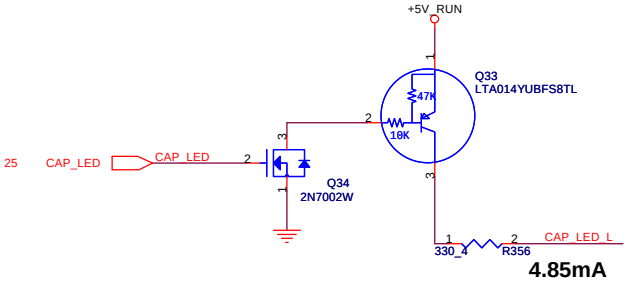
Fingerprint



20120203
Mount C575 J5

20120213
Add wire connect J5.3 to GND

Vi(on_max)= -1.4V
Vi(off_min)=-0.3



4.85mA

Quanta Computer Inc.
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Size	Document Number	Rev
	TP / KB	1A
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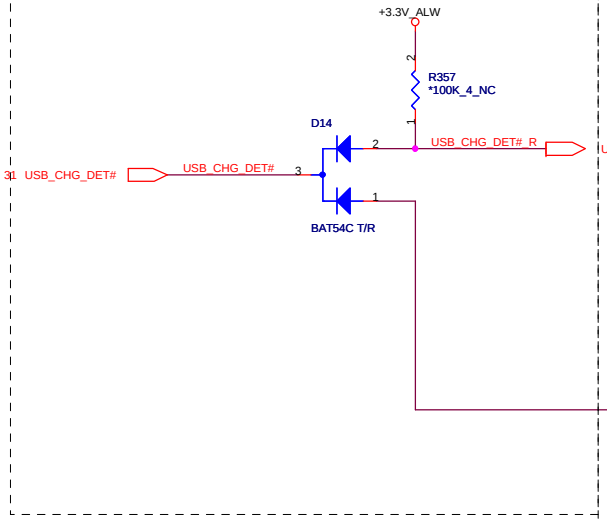
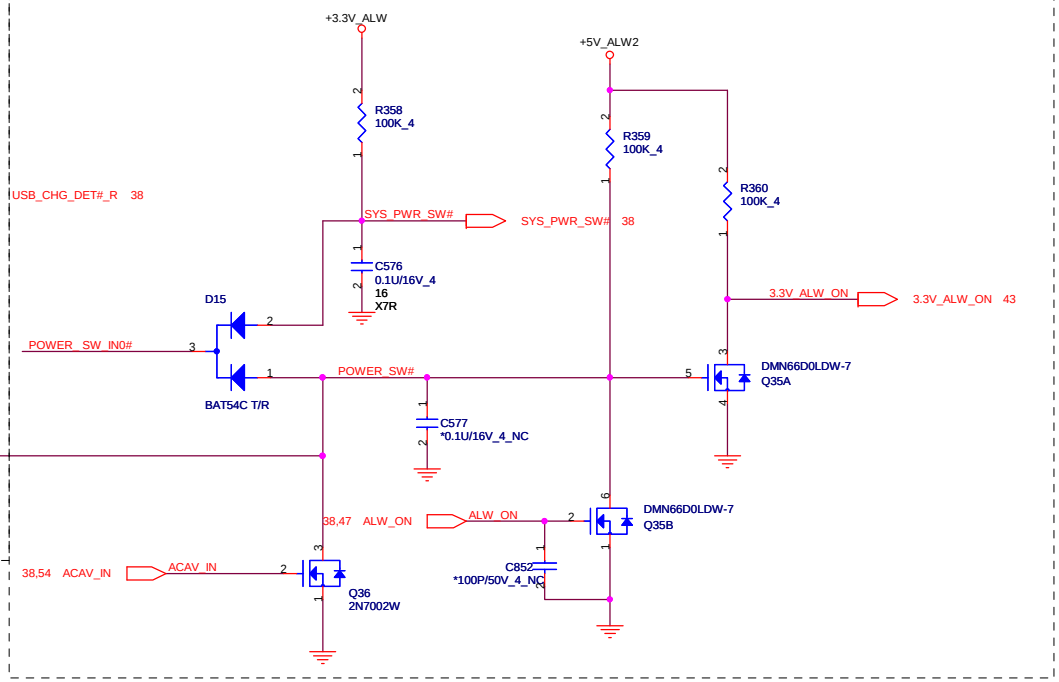
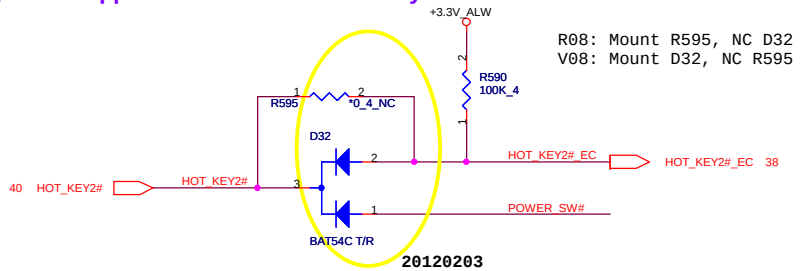
For USB charger usage



3V ALW ON POWER LOGIC



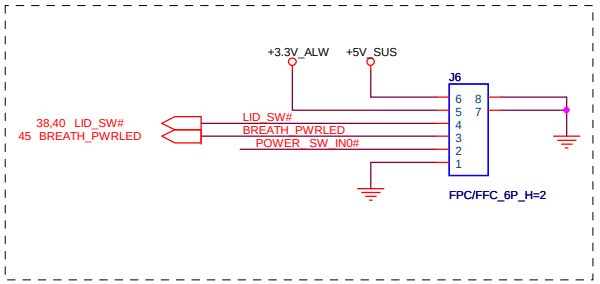
HOT_KEY2 support Pre-Boot Recovery



R08: Mount R595, NC D32
V08: Mount D32, NC R595

20120203
Mount D32, NC R595

TO PWR button board



Quanta Computer Inc.
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Size	Document Number	Rev
	PWR SW/LED	1A
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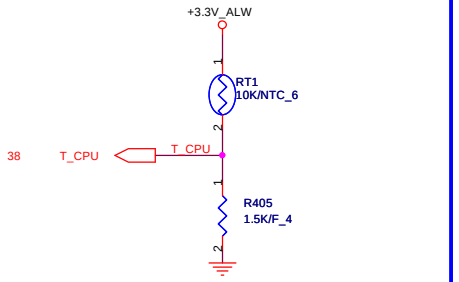
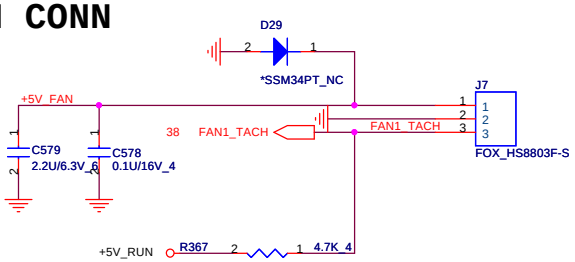
AOAC

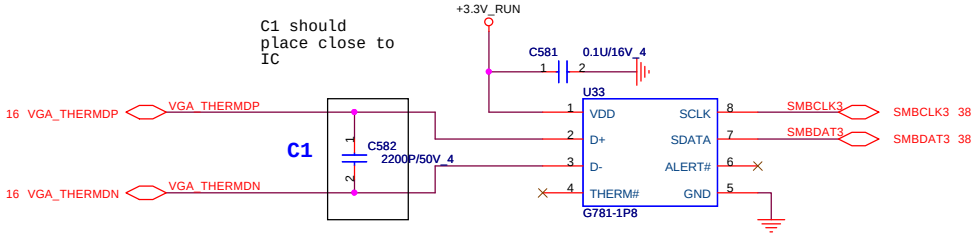


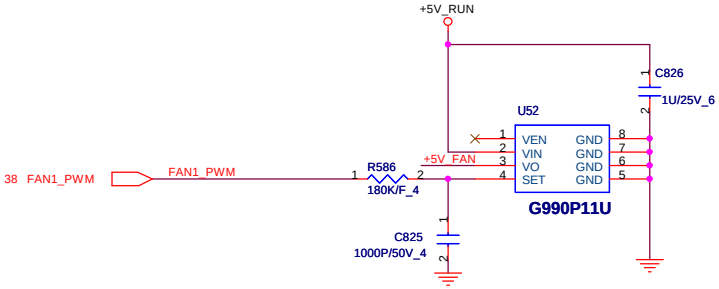
20120203
Mount RT1 R405 for V08A SKU

FAN CONN



G781-1P8
SMBus address is 1001101xb (9Ah) (x is R/W bit).



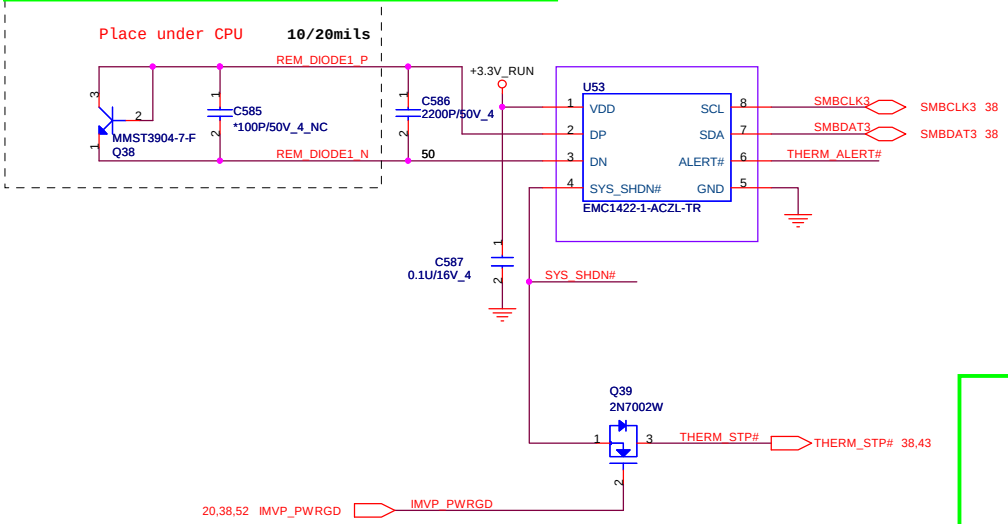


EMC1422 SMBus address is 1001_100xb (98h) (x is R/W bit).

SYS_SHD# / ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C

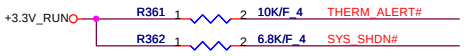
THERMAL IC

1.Place C586 close to EMC1422-U1
2.Place C585 to be close to Q38
Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C586, then C585 should be dummy



CHECK OTP WITH Thermal.

OTP 85 degree C



EMC1422
OTP 85 degree : R361 = 10K, R362 = 6.8K
OTP 90 degree : R361 = 6.8K, R362 = 10K

NTC7718W
OTP 85 degree : R361 = 18.7K, R362 = 2K
OTP 91 degree : R361 = 10.5K, R362 = 7.5K

Quanta Computer Inc.
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Size	Document Number	Rev
	FAN & THERMAL	1A

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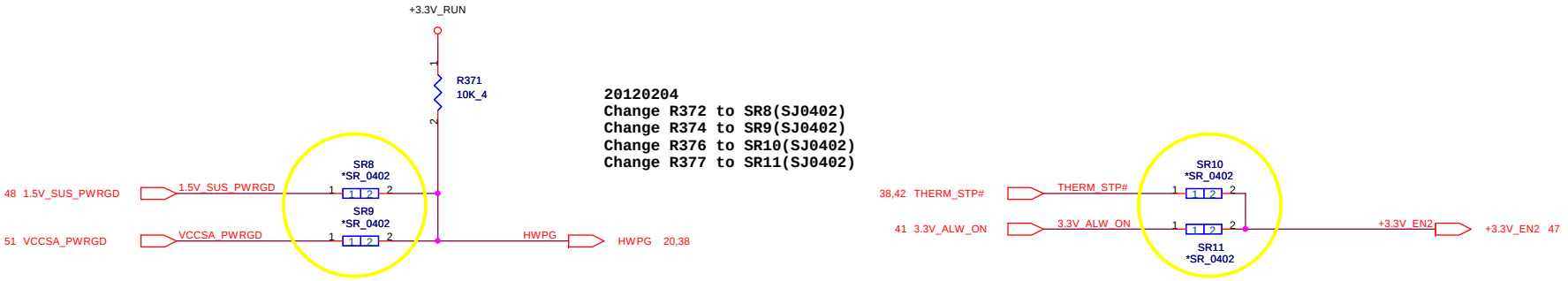

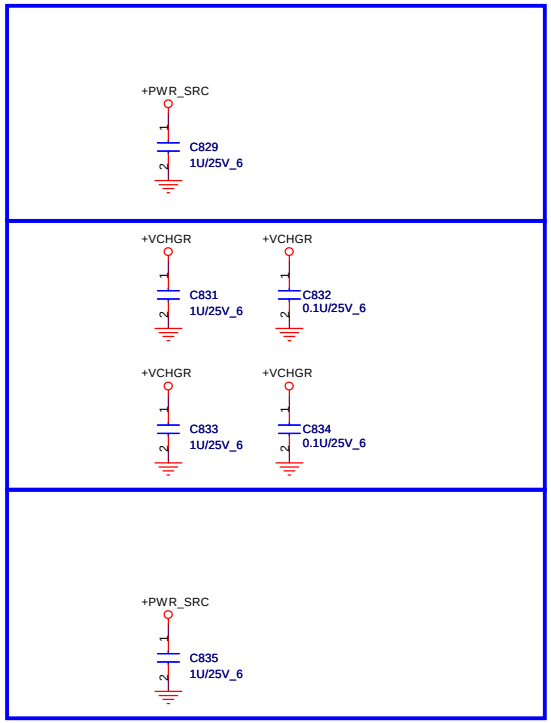

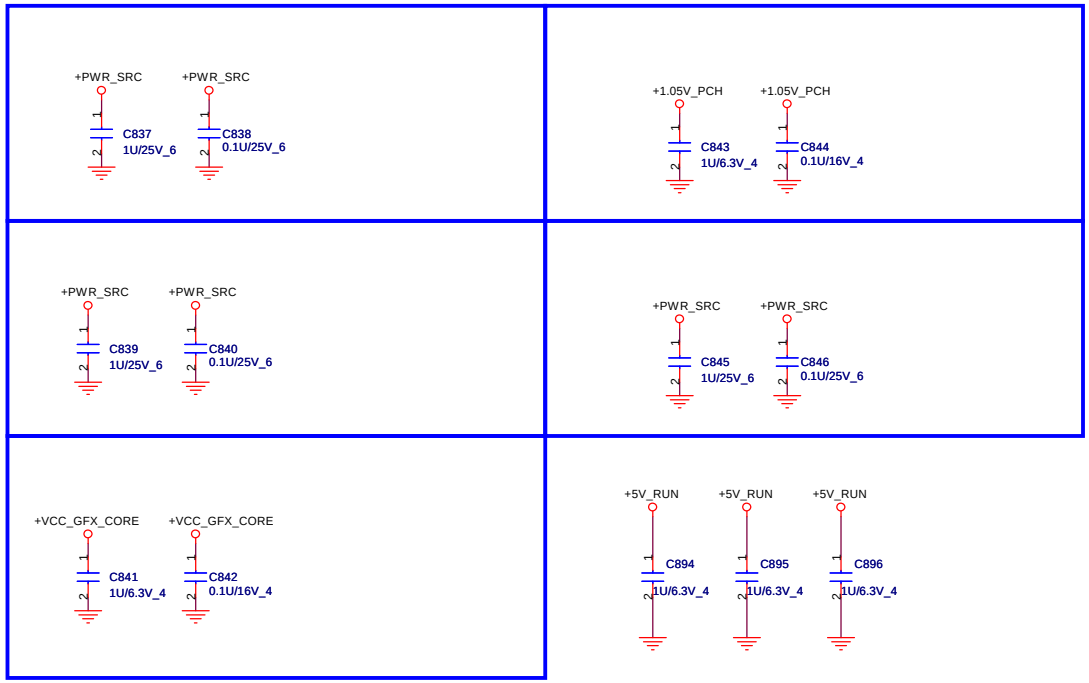

Quanta Computer Inc.

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Size	Document Number	Rev
	System Reset Circuit	1A

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Quanta Computer Inc.

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Size	Document Number	Rev
	MiniCard	1A

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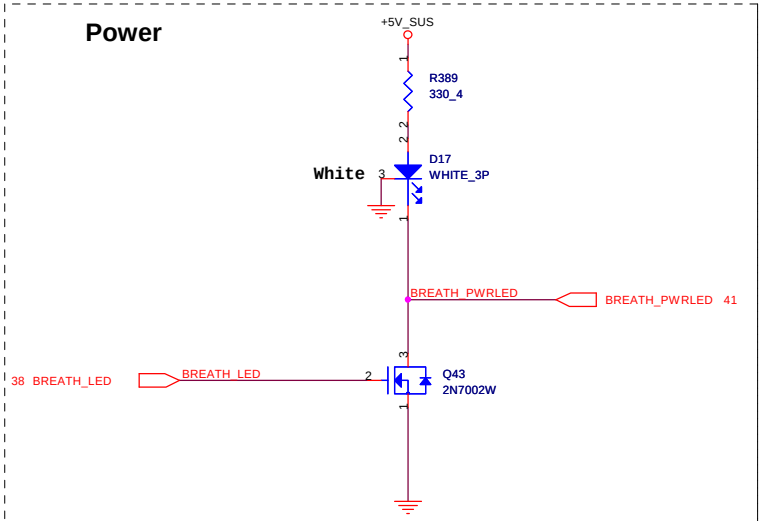
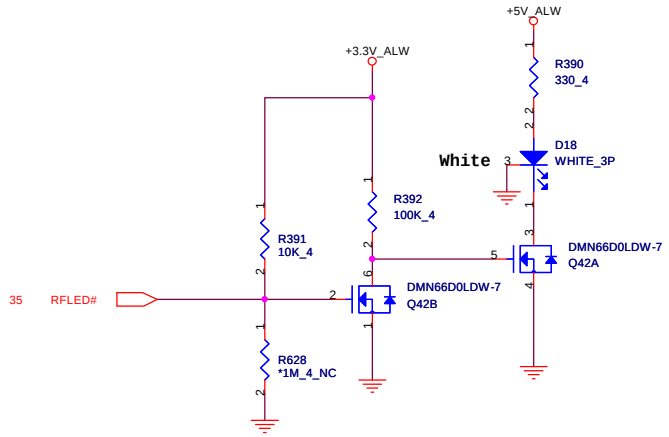
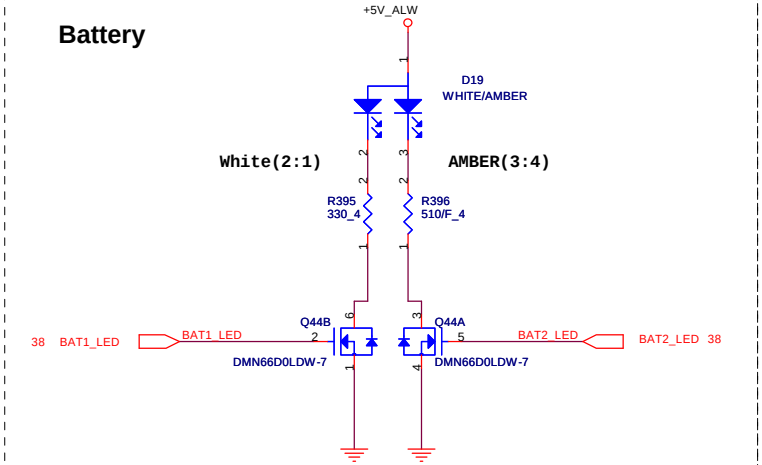
Power



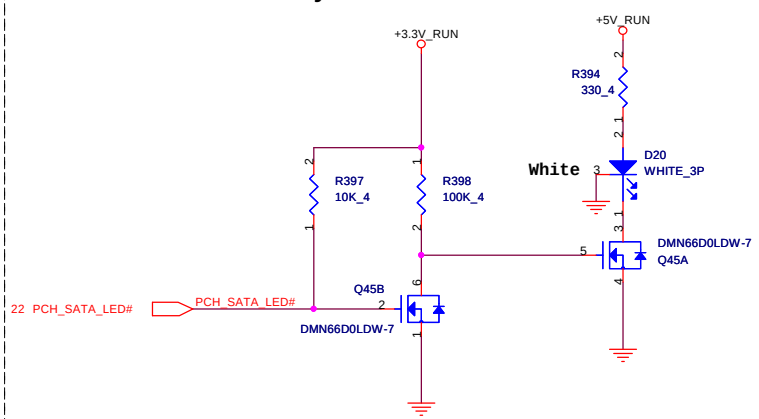
Bluetooth / WLAN on/off LED



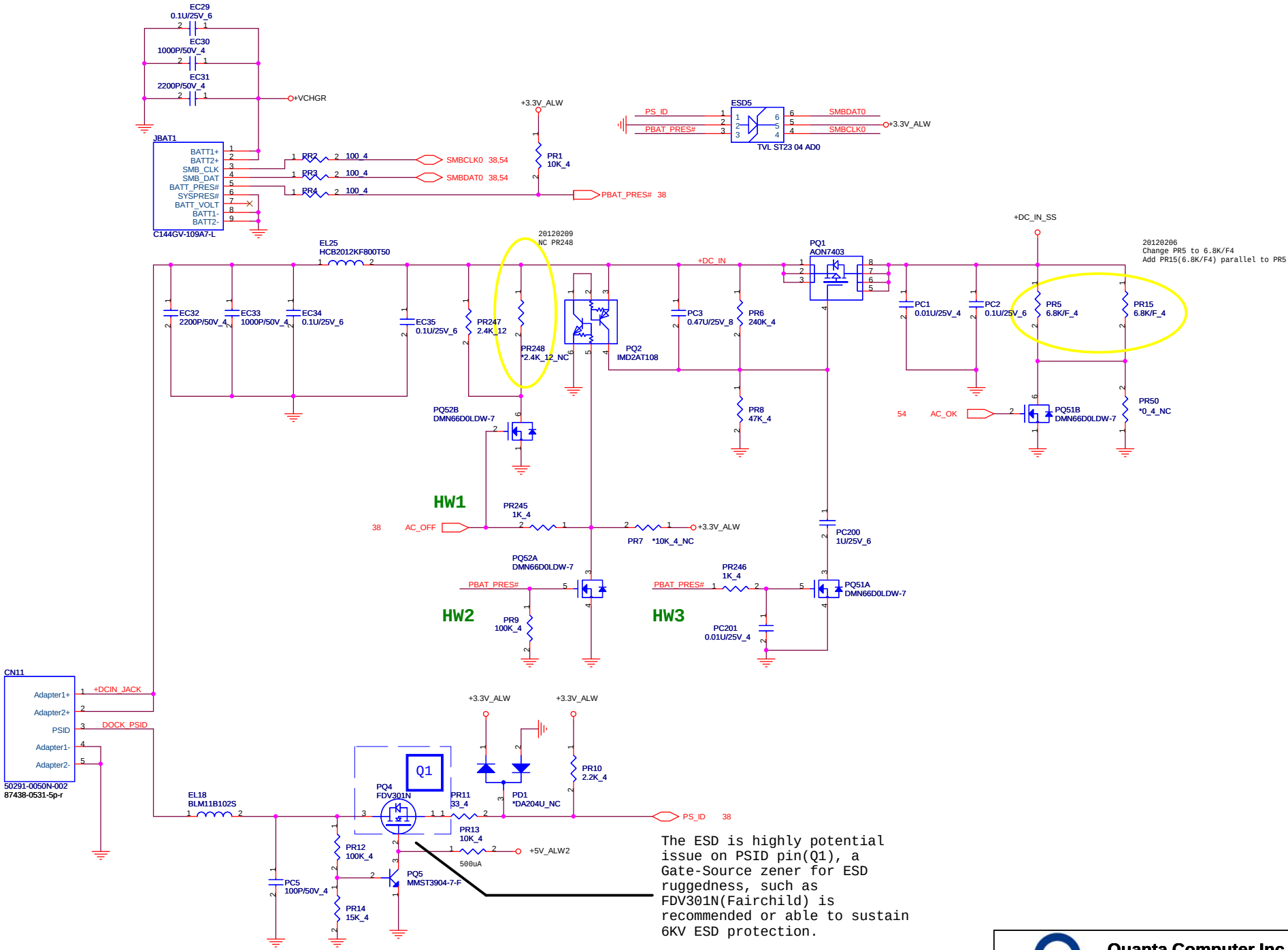
Battery



HDD activity LED.



Quanta Computer Inc.		
PROJECT : R08		
Size	Document Number: LED	Rev: 1A
Date: Monday, February 13, 2012	Sheet 45 of 55	


EC29
0.1U/25V_6
EC30
1000P/50V_4
EC31
2200P/50V_4
+VCHGR
JBAT1
BATT1+
BATT2+
SMB_CLK
SMB_DAT
BATT_PRES#
SYSPRES#
BATT_VOLT
BATT1-
BATT2-
C144GV-109A7-L
PR2 100_4
PR3 100_4
PR4 100_4
SMBCLK0 38,54
SMBDAT0 38,54
+3.3V_ALW
PR1
10K_4
PBAT_PRES# 38
PS_ID
PBAT_PRES#
ESD5
SMBDAT0
SMBCLK0
+3.3V_ALW
TVL ST23 04 AD0
+DC_IN_SS
20120206
Change PR5 to 6.8K/F4
Add PR15(6.8K/F4) parallel to PR5
EL25
HCB2012KF800T50
20120209
NC PR248
+DC_IN
PQ1
AON7403
EC32
2200P/50V_4
EC33
1000P/50V_4
EC34
0.1U/25V_6
EC35
0.1U/25V_6
PR247
2.4K_12
PR248
*2.4K_12_NC
PQ2
IMD2AT108
PC3
0.47U/25V_8
PR6
240K_4
PR8
47K_4
PC1
0.01U/25V_4
PC2
0.1U/25V_6
PR5
6.8K/F_4
PR15
6.8K/F_4
PR50
*0_4_NC
54 AC_OK
PQ51B
DMN66D0LDW-7
PQ52B
DMN66D0LDW-7
HW1
PR245
1K_4
38 AC_OFF
PR7 *10K_4_NC
+3.3V_ALW
PC200
1U/25V_6
PQ52A
DMN66D0LDW-7
PBAT_PRES#
PR246
1K_4
PQ51A
DMN66D0LDW-7
HW2
PR9
100K_4
HW3
PC201
0.01U/25V_4
CN11
Adapter1+
Adapter2+
PSID
Adapter1-
Adapter2-
+DCIN_JACK
DOCK_PSID
50291-0050N-002
87438-0531-5p-r
EL18
BLM11B102S
Q1
PQ4
FDV301N
PR11
33_4
PD1
*DA204U_NC
PR10
2.2K_4
PS_ID 38
PR13
10K_4
+5V_ALW2
500uA
PR12
100K_4
PQ5
MMST3904-7-F
PC5
100P/50V_4
PR14
15K_4
The ESD is highly potential issue on PSID pin(Q1), a Gate-Source zener for ESD ruggedness, such as FDV301N(Fairchild) is recommended or able to sustain 6KV ESD protection.
Quanta Computer Inc.
PROJECT : R08
Size
Document Number
DC IN / BATT
Rev
1A
Date: Monday, February 13, 2012
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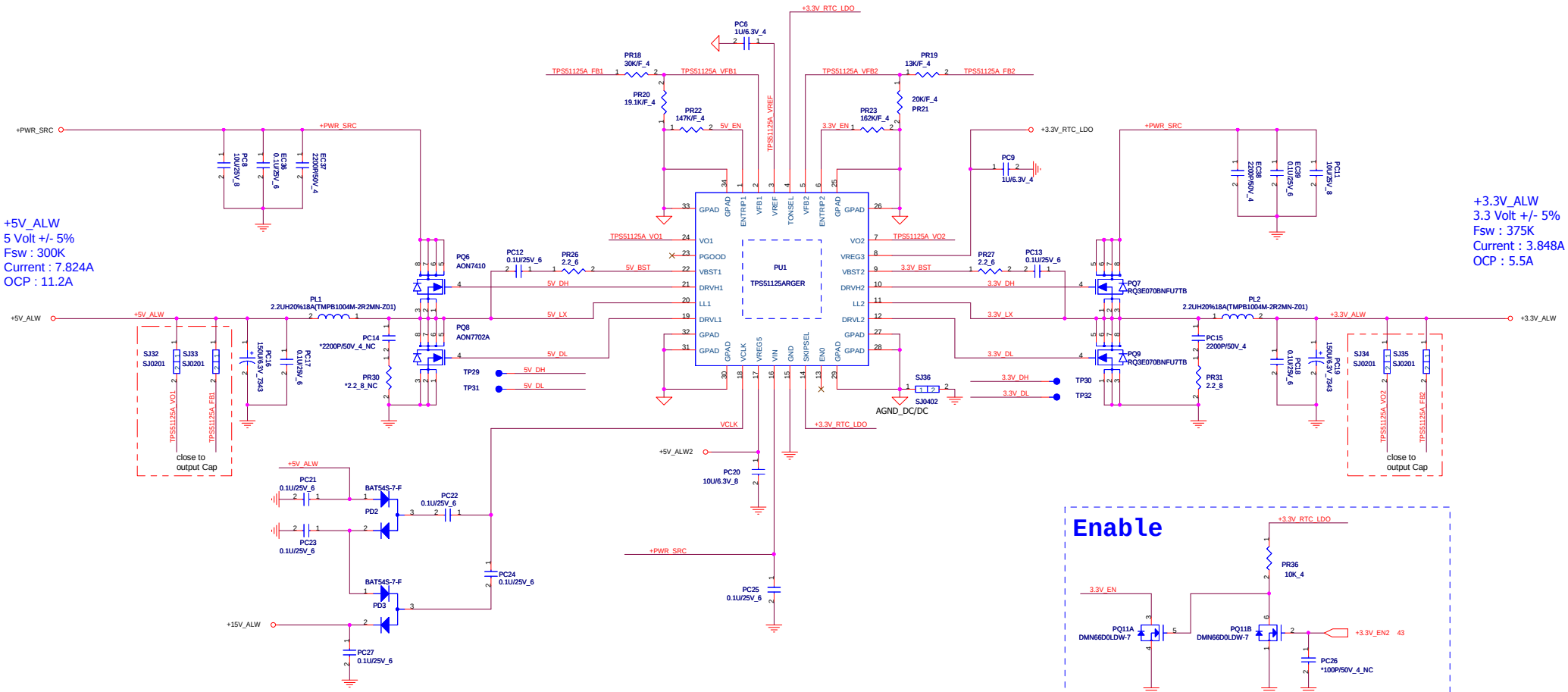
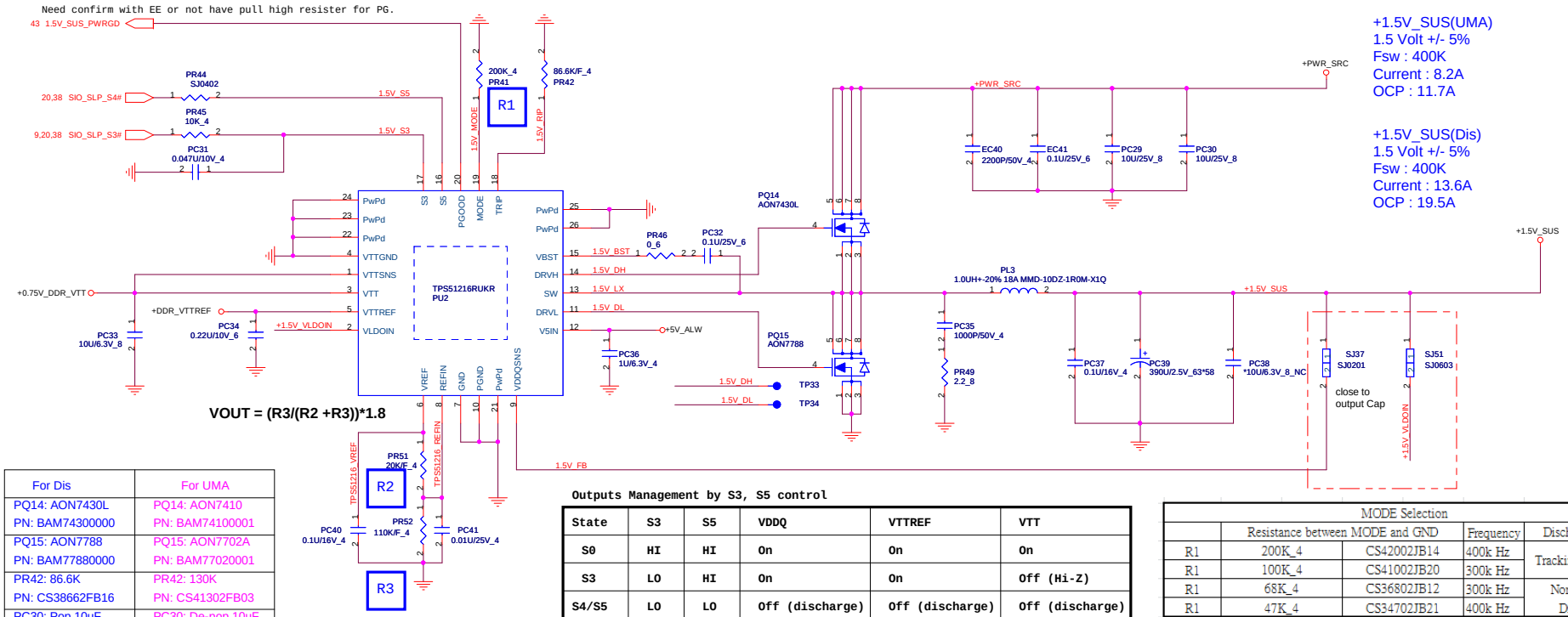


TPS51125A TONSEL Connection and Switching Frequency				
Ton	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz

Quanta Computer Inc.
PROJECT : R08

Size	Document Number	Rev
	3.3V_ALW / 5V_ALW (TPS51125ARGER)	1A
Date: Monday, February 13, 2012	Sheet 47 of 55	



+1.5V_SUS(UMA)
1.5 Volt +/- 5%
Fsw : 400K
Current : 8.2A
OCP : 11.7A

+1.5V_SUS(Dis)
1.5 Volt +/- 5%
Fsw : 400K
Current : 13.6A
OCP : 19.5A

VOUT = (R3/(R2 +R3))*1.8

For Dis	For UMA
PQ14: AON7430L PN: BAM74300000	PQ14: AON7410 PN: BAM74100001
PQ15: AON7788 PN: BAM77880000	PQ15: AON7702A PN: BAM77020001
PR42: 86.6K PN: CS38662FB16	PR42: 130K PN: CS41302FB03
PC30: Pop 10uF	PC30: De-pop 10uF

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

MODE Selection				
	Resistance between MODE and GND		Frequency	Discharge Mode
R1	200K_4	CS42002JB14	400k Hz	Tracking Discharge
R1	100K_4	CS41002JB20	300k Hz	
R1	68K_4	CS36802JB12	300k Hz	Non-tracking Discharge
R1	47K_4	CS34702JB21	400k Hz	

Quanta Computer Inc.
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Size	Document Number	Rev
	1.5_SUS/0.75_DDR_VTT (TPS51216RUKR)	1A

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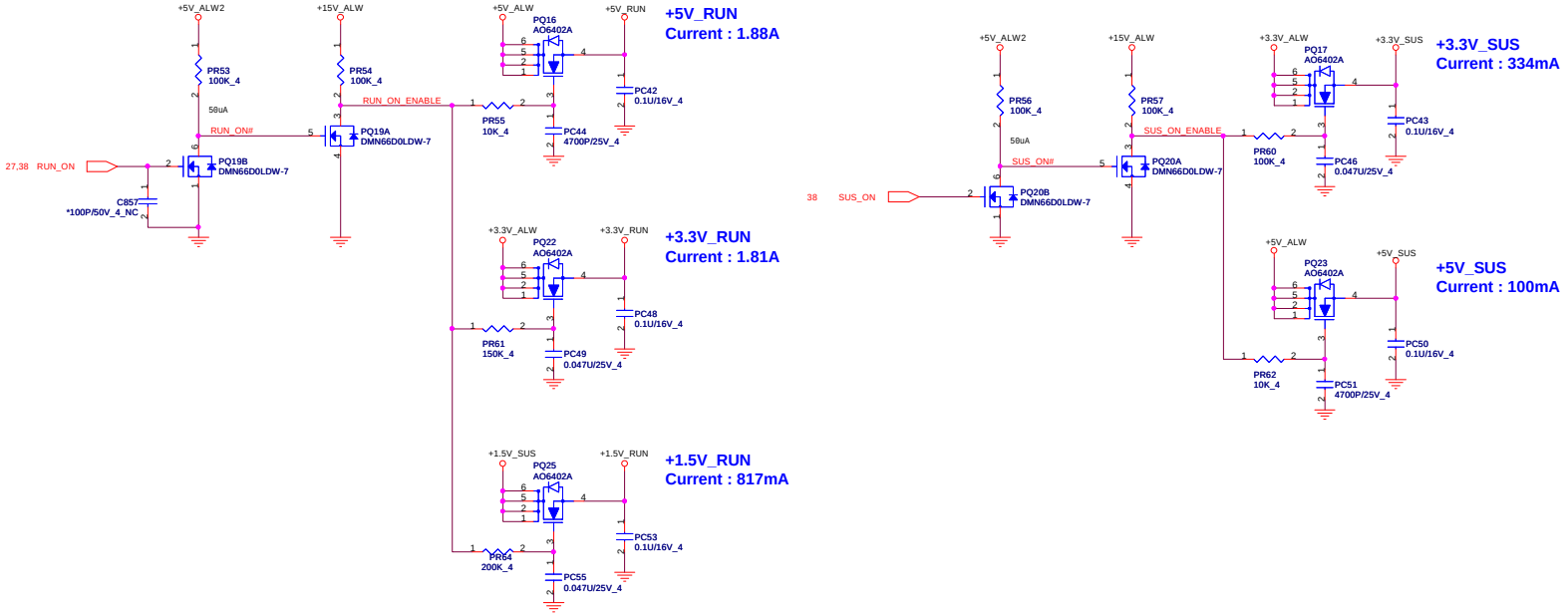

Quanta Computer Inc.

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Size	Document Number	Rev
	Load Switch	1A

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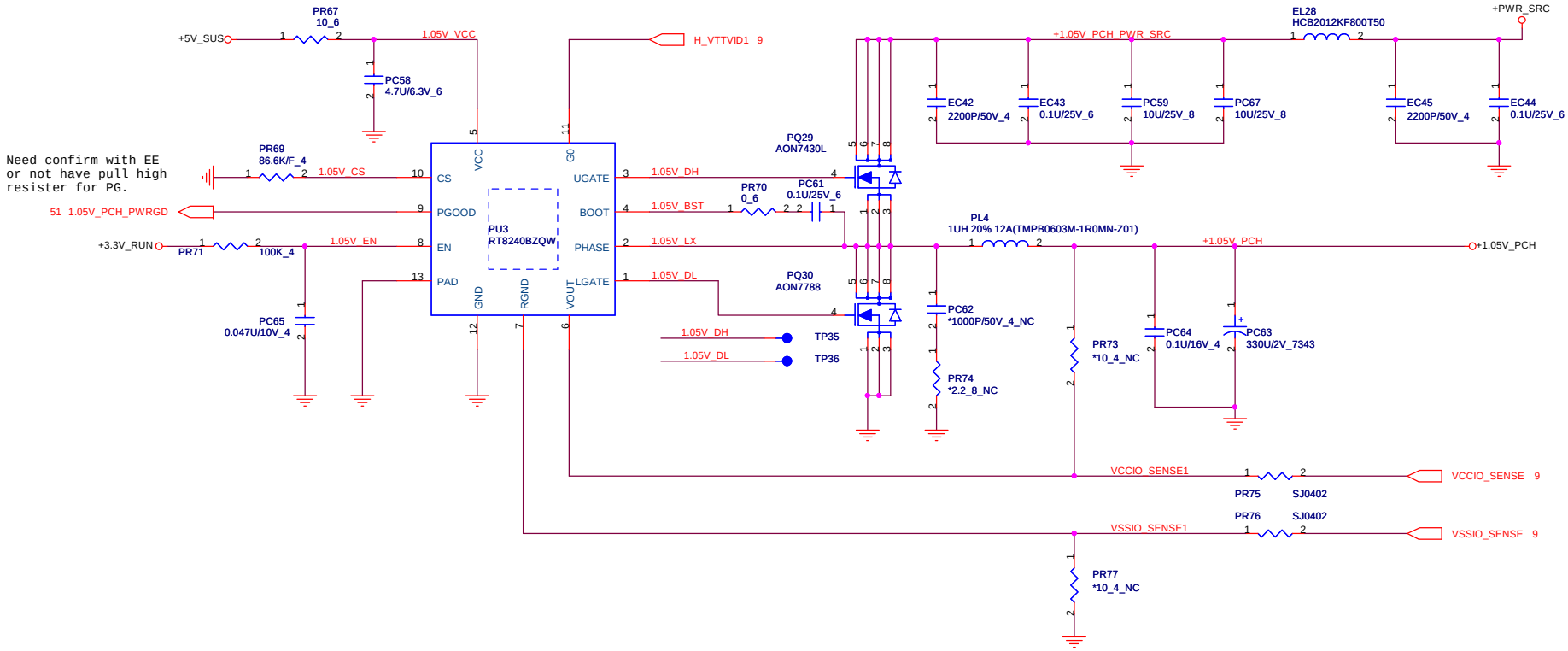

+1.05V_PCH
1.05 Volt DC +/- 2%
Fsw : 400K
TDC : 13.5A
OCP : 19.5A

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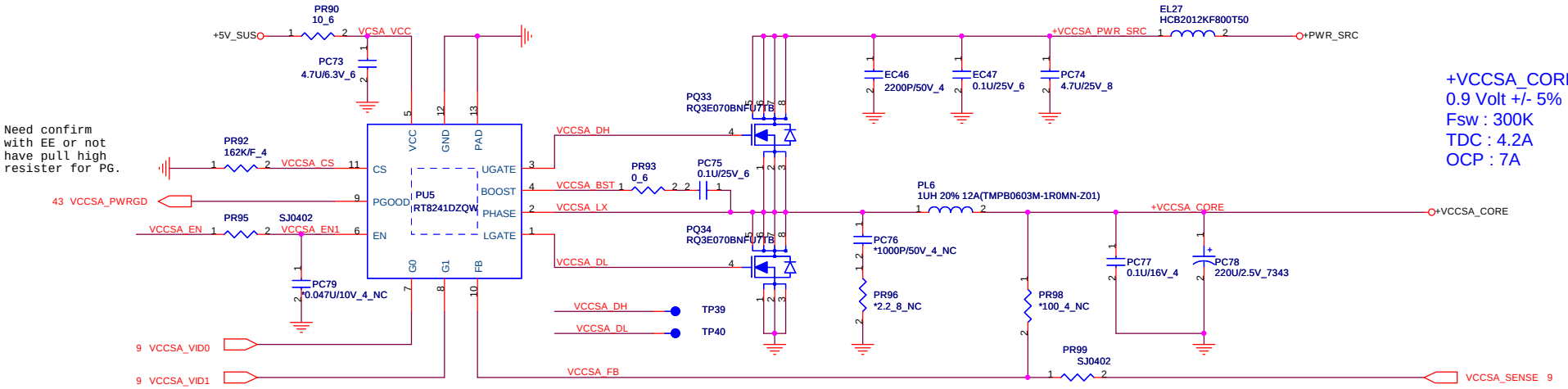
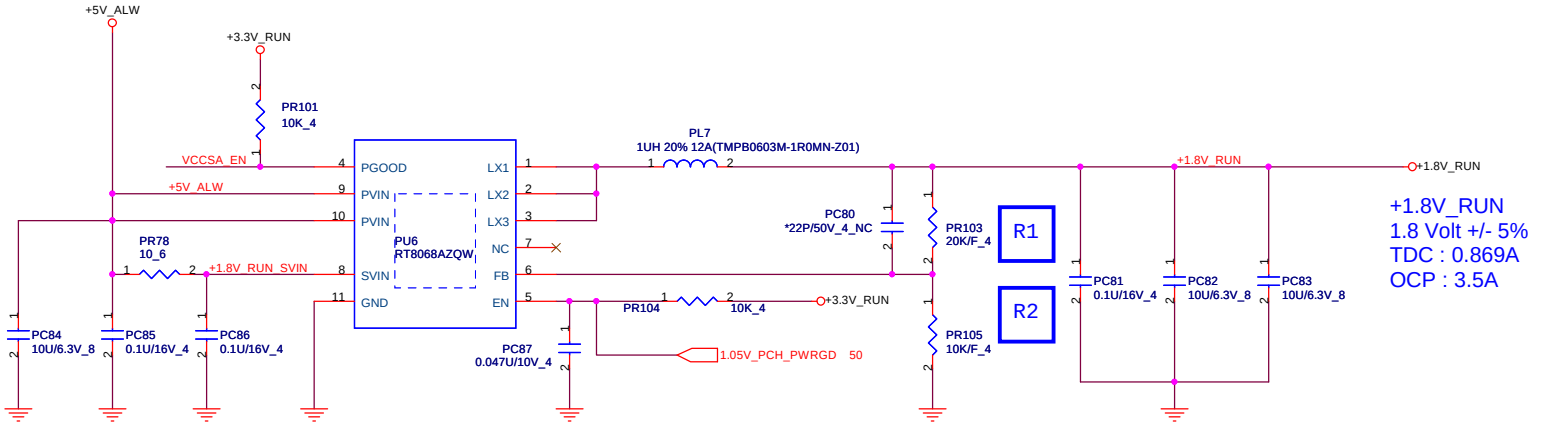
Size	Document Number	Rev
	+1.05V_PCH / VTT (RT8240BGQW)	1A
Date: Monday, February 13, 2012	Sheet 50 of 55	



Need confirm with EE or not have pull high resister for PG.

+VCCSA_CORE
0.9 Volt +/- 5%
Fsw : 300K
TDC : 4.2A
OCP : 7A

VCCSA_VID1	VCCSA_VID0	VCCSA_CORE
Low	Low	0.9V
High	Low	0.8V
Low	High	0.725V
High	High	0.675V



+1.8V_RUN
1.8 Volt +/- 5%
TDC : 0.869A
OCP : 3.5A

VOUT = 0.6(1+R1/R2)

Quanta Computer Inc.
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Size	Document Number	Rev
	VCCSA (RT8241DGQW)	1A
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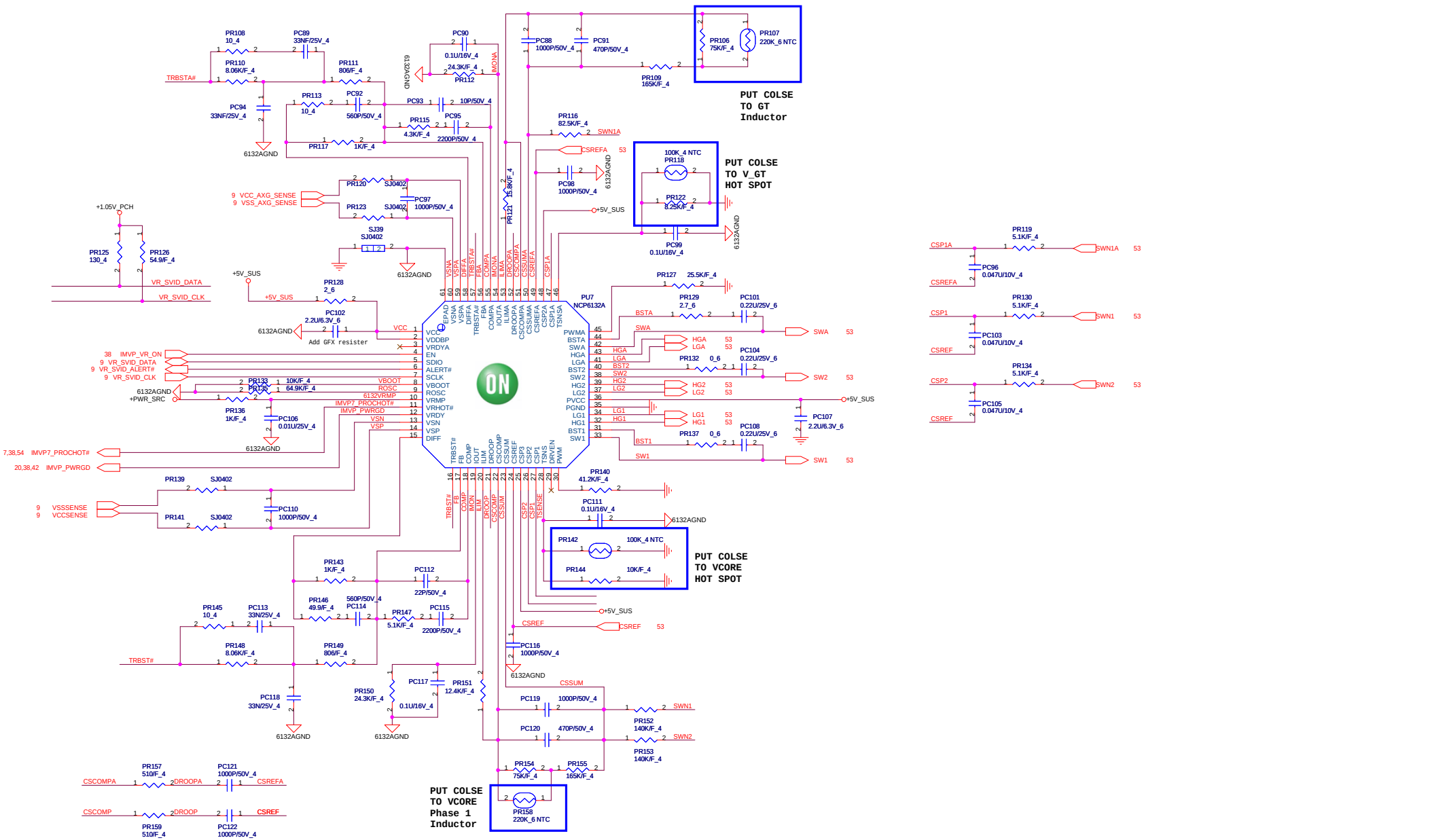
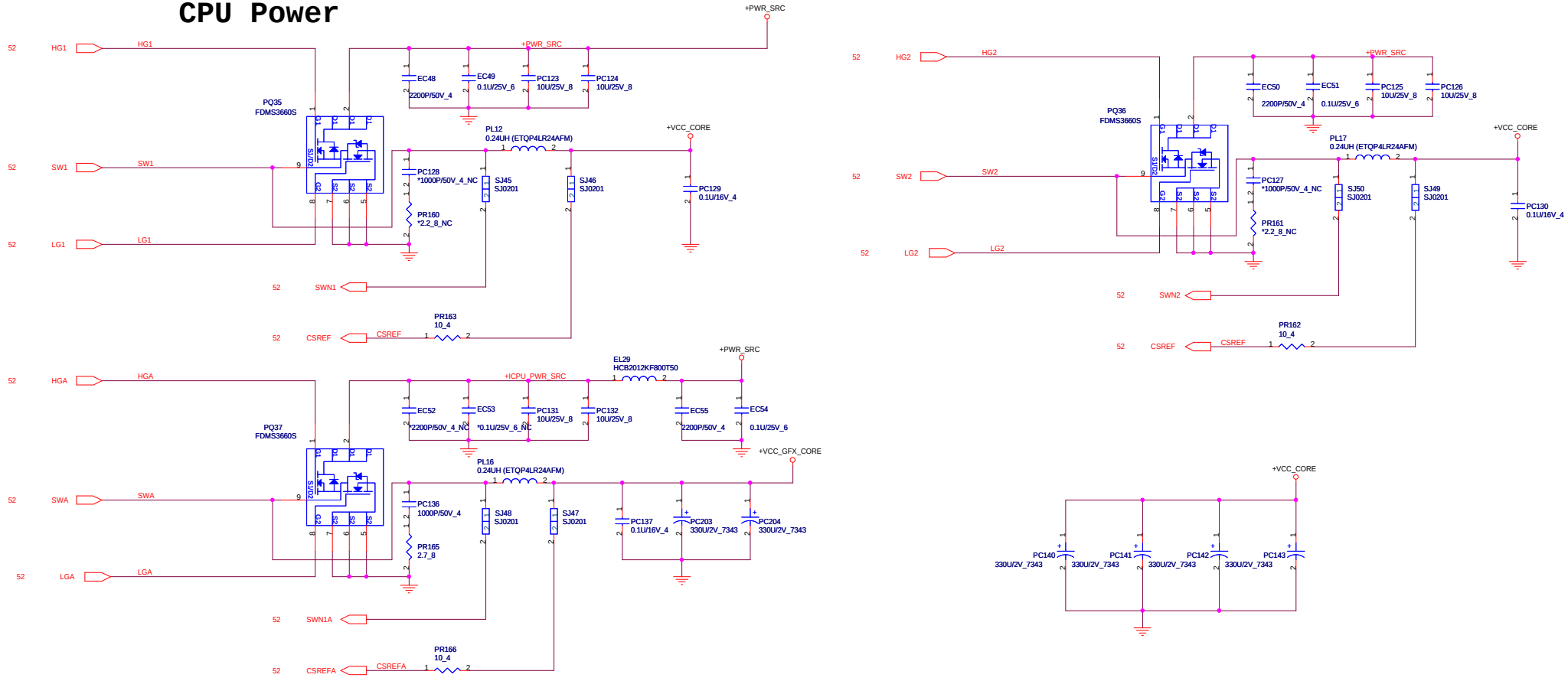

PUT COLSE TO GT Inductor
PUT COLSE TO V_GT HOT SPOT
PUT COLSE TO VCORE HOT SPOT
PUT COLSE TO VCORE Phase 1 Inductor
PU7 NCP6132A
Add GFX resister
+1.05V_PCH
+5V_SUS
6132AGND
VR_SVID_DATA
VR_SVID_CLK
VSSSENSE
VCCSENSE
IMVP7_PROCHOT#
IMVP_PWRGD
CSREF
CSSUM
SWN1
SWN2
SWA
SW1
SW2
HGA
LGA
HG2
LG2
LG1
HG1
BST1
BST2
BSTA
Quanta Computer Inc.
PROJECT : R08
CPU_CORE (NCP6132)
Monday, February 13, 2012

CPU Power



Quanta Computer Inc.		
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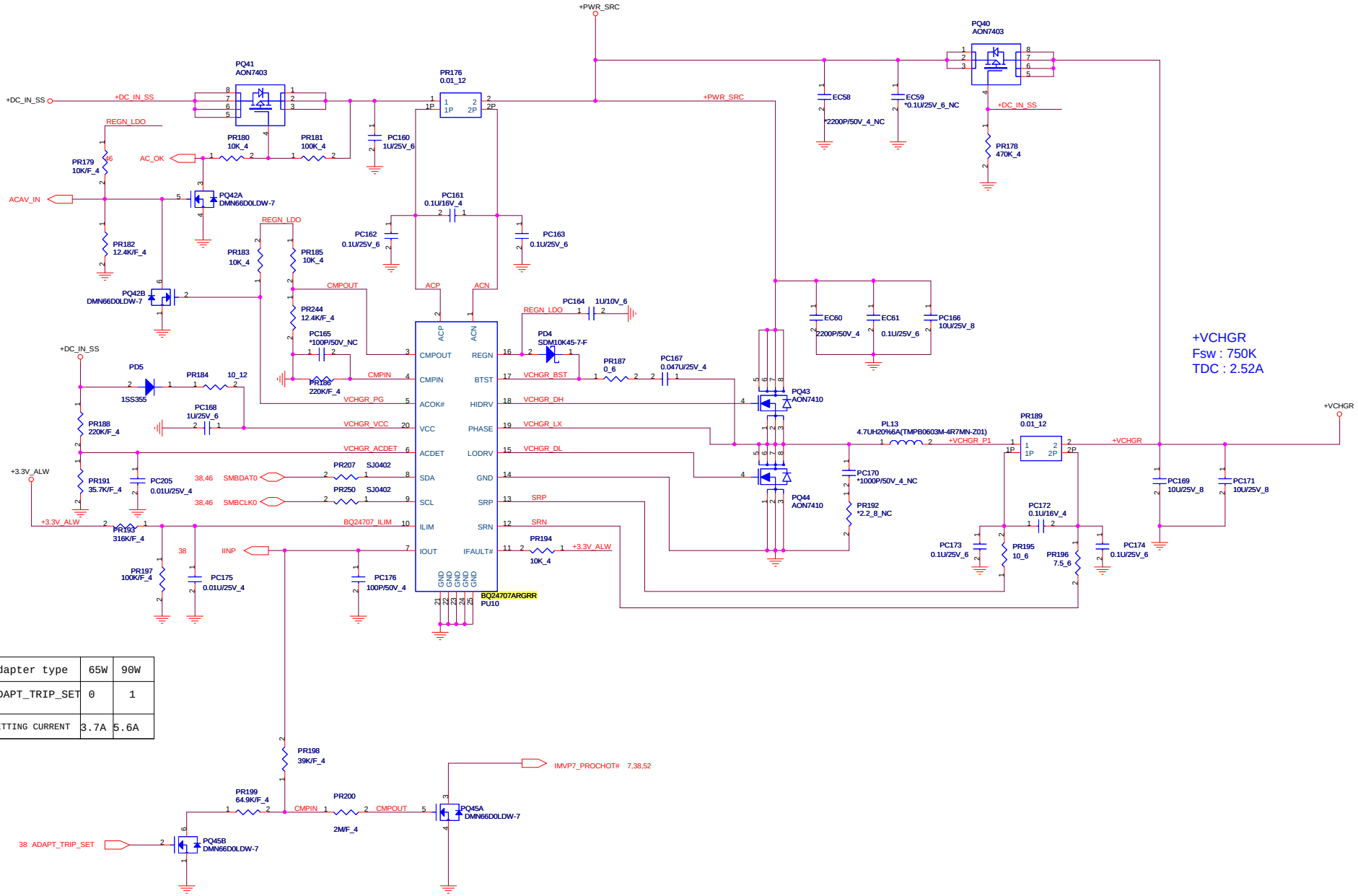
Size	Document Number: CPU_CORE (NCP6132)	Rev: 1A
Date: Monday, February 13, 2012	Sheet 53 of 55	



Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A

Quanta Computer Inc.

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Size	Document Number	Rev
	Charger (BQ24765RUVR)	1A

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+VCC_GFX_CORE
Fsw : 400K
Current : 50A
OCP : 60A

+3V_GFX
Current : 973mA

+1.5V_GFX
Current : 5.4A

+1.05V_GFX
Current : 2.76A

PUT COLSE TO
+VCC_GFX_CORE
Phase 1 Inductor

Close to PR58

Need confirm with EE
or not have pull high
resister for PG.

PU11
NCP3218MNR2G

20120209
Change PR217, PR224 to shortpad(short0603)

Quanta Computer Inc.			
PROJECT : R08			
Size	Document Number		Rev
	VGA_N11P-dGFX (NCP3218MNR2G)		1A
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